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Développement de circuits passifs et d'amplificateurs de puissance en bande D, en tant que blocs de base clés de front-end dans une technologie BiCMOS avancée

Development of D-band passive circuits and power amplifiers as key front-end building blocks in advanced BiCMOS technology

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Abstract

The continuous growth of data traffic and the increasing demand for very high data rates, low latency, and energy-efficient communication systems are driving the development of new front-end solutions for next-generation wireless networks. Wireless backhauling for short-range point-to-point links appears as a key use case for future 6G infrastructure, with target data rates exceeding 100 Gb/s. In this context, operating at higher frequencies is an attractive approach that has been made possible thanks to the steady improvement of integrated technologies in terms of f_T and f_{max}. Among the available frequency ranges, the D-band is especially promising for front-end module design, as it offers large available bandwidth while helping reduce the footprint of passive components and enabling highly integrated antenna solutions.

This thesis investigates the design of D-band front-end modules in STMicroelectronics' B55X SiGe-BiCMOS technology, with a particular focus on two enabling aspects: the development of high-frequency distributed passive components and the design of power amplifiers suited to the strong constraints of this frequency range. In particular, one of the main challenges in the D-band is the combination of high propagation losses, limited transistor gain, parasitic effects in interconnects, and reduced breakdown voltage in advanced high-speed devices. These limitations make the design of efficient and robust transmitter-side circuits especially demanding.

The first part of the work was dedicated to the study, design, fabrication, and characterization of distributed passive structures, including coupled line couplers and an innovative power splitter based on coupled line. Experimental results show good agreement with electromagnetic simulations, confirming both the validity of the modeling tools and the feasibility of highly integrated passive building blocks at around 150 GHz. These devices achieve low insertion loss, good amplitude and phase balance, besides a significant reduction in occupied area compared with more conventional solutions for the power splitter. In addition, the work established a complete design methodology for coupled line-based passive devices, providing a useful foundation for future D-band circuits.

The second part of the thesis focused on the design of multi-stage power amplifier cells using cascode and common-base (CB) topologies. A comparative analysis of both structures highlighted their complementary strengths: the cascode topology offers high gain and strong input-output isolation, while the CB topology provides better efficiency, linearity, and output power capability. Building on these observations, several amplifier architectures were developed, including two-stage and three-stage implementations. To address the losses associated with conventional matching networks and DC-blocking capacitors, new matching solutions based on coupled line couplers loaded with stubs were introduced. These networks also provide inherent DC isolation and improved flexibility for biasing and interstage matching.

2-stage PA measured small-signal results show good agreement with simulations after careful refinement of the electromagnetic and circuit-level design flow. The demonstrated amplifiers exhibit gains above 14 dB, while corrected simulations predict competitive large-signal performance, with an output power at 1dB of compression P_{1dB}= $7.2\ dBm$ and a power-added efficiency $PAE = 8.4\ \%$ for the two-stage version. The three-stage implementation shows an even higher simulated output power and gain, although further investigation is still required to fully understand its experimental behavior. Overall, this work demonstrates the feasibility of implementing D-band power amplifiers and front-end building blocks in B55X technology, while highlighting the key role of distributed passives in enabling compact and efficient high-frequency integrated circuits.

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Introduction

The continuous growth of data traffic and the steady increase in required data rates are driving the development of future wireless communication systems that must operate with both high performance and improved energy efficiency. This challenge is especially important in the context of next-generation networks, and more specifically for 6G-oriented backhauling applications. Among these, short-range point-to-point wireless links stand out as a particularly relevant use case, since they require extremely high throughput over limited distances.

Several approaches can be considered to address this demand. Enhancing coding schemes and carrier aggregation can improve spectral efficiency, but these solutions generally come at the cost of higher power consumption and greater system complexity. Moreover, more advanced coding strategies require better communication quality, typically expressed in terms of signal-to-noise ratio. Another promising direction consists in increasing the operating frequency in order to naturally access larger bandwidths and therefore higher data rates, without necessarily relying on very large modulation constellations. This approach has become increasingly realistic thanks to the continuous progress of integrated technologies in terms of speed and high-frequency performance. However, when moving above 100 GHz, the propagation spectrum exhibits several strong absorption peaks in air. The frequency region located between these peaks, commonly referred to as the D-band, therefore appears as a particularly attractive window for high-data-rate wireless links. For this reason, the present thesis focuses entirely on this frequency range.

Within this framework, the investigation of front-end modules operating in the D-band is highly relevant for wireless backhauling applications. A review of the state of the art shows that such modules are realistic candidates for future systems, although many challenges remain to be addressed. Among them, two topics appear especially critical: power amplification and passive devices quality. Both play a central role in the overall performance of the front-end, and both must be optimized if the advantages of high-frequency operation are to be fully exploited. These two aspects therefore form the core of the present work.

On the active side, the choice of suitable technology is a key enabler for D-band power amplifier design. In this context, STMicroelectronics' B55X SiGe BiCMOS technology, one of the world's most advanced SiGe technologies, was selected for this thesis. A review of the state of the art on D-band power amplifiers highlights several major challenges associated with this frequency range. Parasitic effects in transistor interconnections degrade performance, while skin effect increases losses and further reduces efficiency of passive circuits. In addition, available technologies often provide only limited gain at the target frequency. At the same time, the technological improvements that enable higher f_T and f_{max} often come at the expense of breakdown voltage, thereby limiting both the power capability and the efficiency of the transistor.

On the passive side, the role of passive components is equally decisive. The state of the art reveals both the need for preliminary investigations and the potential for innovation. This makes passive devices design a central milestone of the thesis, with a particular emphasis on distributed passive structures based on transmission lines and their impact on the realization of high-performance D-band front-end circuits.

The manuscript is organized as follows. Chapter 1 presents the overall context, beginning with the evolution of wireless communications and the associated increase in data rates, then narrowing down to front-end module design and to the state of the art of passive components and power amplifiers in the D-band. This overview identifies the main technological limitations and highlights the opportunities that define the objectives of the thesis.

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Chapter 2 is devoted to passive components design. It first investigates couplers, including a theoretical study based on even- and odd-mode decomposition. It then presents the design of power dividers and combiners, including an innovative implementation. Fabrication and measurements are finally reported, confirming both the functionality of the devices and the accuracy of the simulation flow.

These passive structures provide a solid foundation for power amplifier design, which is the focus of Chapter 3. This chapter presents the sizing and design of several amplifier versions, based on the conclusions drawn from the state of the art study. Some of these realizations make use of innovative matching networks enabled by the preliminary passive-device investigations.

Finally, Chapter 4 presents more advanced realizations and design improvements for both power amplifiers and passive devices, with the broader aim of enabling high-performance and innovative components. It discusses the ideas that could not be fully completed within the scope of this thesis, including parallel power amplifier architectures, as well as further improvements in passive structures such as three-dimensional couplers, power combiners, and innovative baluns for differential approaches.

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1.State of the art

1.1 Work context

1.1.1 Increasing data rate tendency

Let us place ourselves at the very beginning of 2023, at the start of the thesis. At that time... The data rate had experienced very rapid growth in recent years, for example, between 2020 and 2022 it roughly doubled in two years according to Ericson mobility report [1], as shown in Figure 1-1.

This increase is driven by both the rise in subscription numbers and the growth in average data consumption per subscription. This trend is primarily fueled and explained by the increasing consumption of higher-quality video content, and to a lesser extent by social networks, updates, and other factors, as illustrated in Figure 1-2.

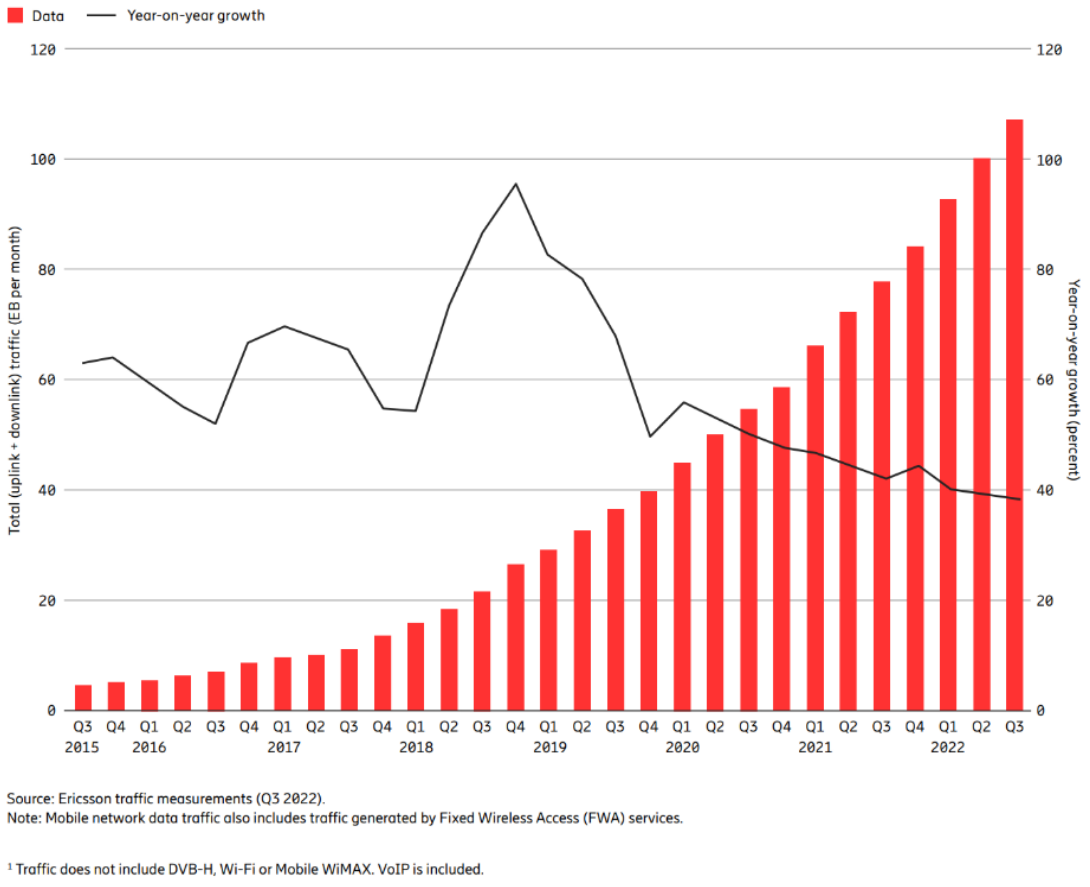
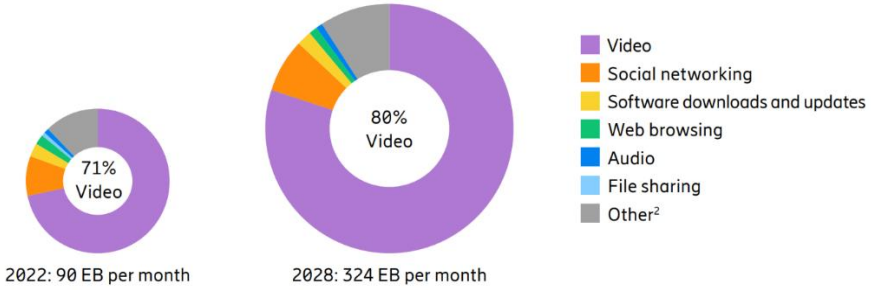


Figure 1-1: Global mobile network data traffic and year-on-year growth (EB per month) from 2022 Ericson mobility report [1]



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Figure 1-2: Mobile data traffic by application category per month [1]

Global mobile data traffic reached over 115 exabytes (EB) per month by the end of 2022, and a drastic increase by a factor of more than 4 is expected between the end of 2022 and 2028, as shown in Figure 1-3. This growth is projected to reach 450 EB per month by the end of 2028. This estimate considers the anticipated rise of virtual reality (VR), augmented reality (AR), and mixed reality (MR) services. Currently, one of the most competitive games in the e-sports scene is called EVA, which incorporates AR/VR (Augmented Reality and Virtual Reality)technologies and is increasingly gaining traction alongside platforms such as PlayStation VR, Google VR, and others, illustrating this growing trend. Moreover, gaming and video applications will be major contributors to this increase, as they require higher video resolutions and higher refresh rates.

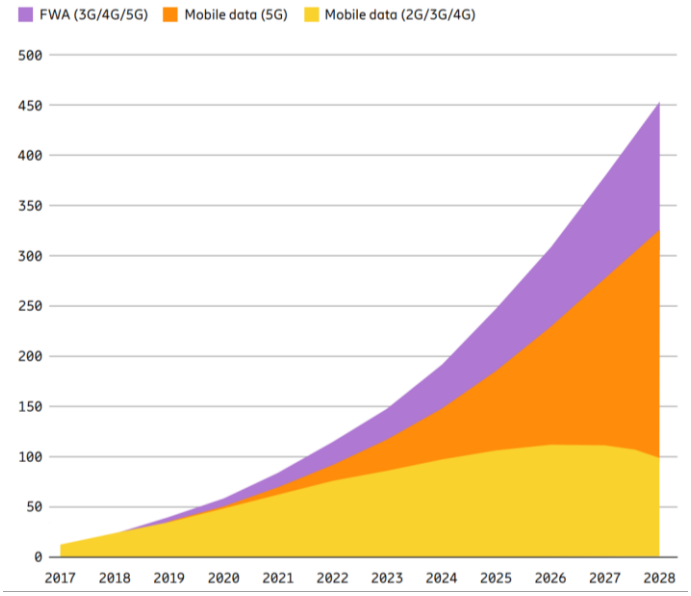


Figure 1-3: Global mobile network data traffic (EB per mounth) [1]

The data presented in Figure 1-1 comes from the Ericsson Mobility Report 2022 published in November 2022 [1], which was the most recent report available before the start of my thesis. Comparing this with a more recent version, the Ericsson Mobility Report 2025 published in November of the same year [2], we observe that the upward trend is confirmed but at a slightly slower pace than previously anticipated. The growth appears more linear, reaching 188 EB per month as shown in Figure 1-4, compared to just over 200 EB projected in the 2022 report. The 2025 report forecasts an increase by a factor of 2.4 to reach 482 EB per month by the end of Q3 2031.

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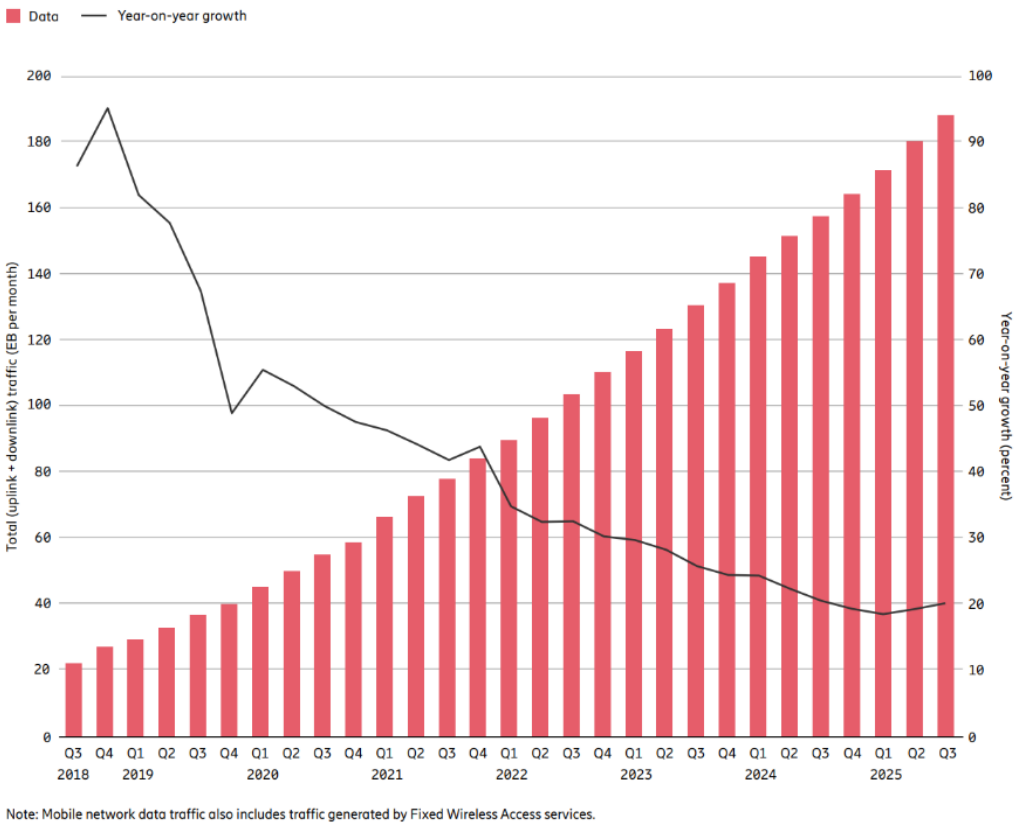


Figure 1-4: Global mobile network data traffic and year-on-year growth (EB per month) from 2025 Ericson mobility report [2].

In [3], the concept of immersive communications is presented, followed by a discussion of their requirements in terms of data rate, latency, and reliability, as illustrated in Figure 1-5.

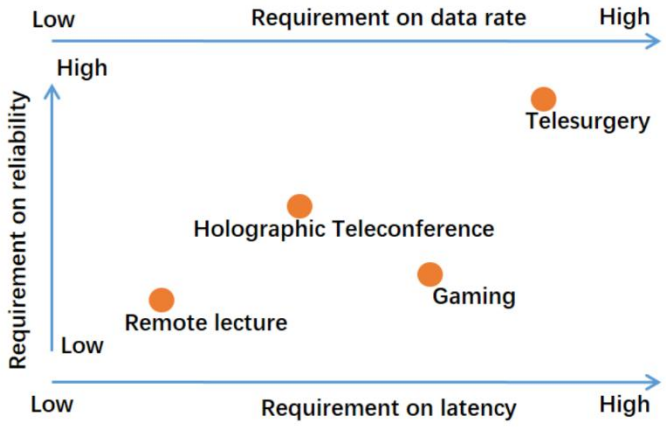


Figure 1-5: Typical use cases of immersive communications and requirement on data rate, reliability and latency [3]

As can be seen in Figure 1-5, an increasing number of applications are demanding in terms of latency and data rate, with a particularly strong demand for the latter. Remote streaming is also on the rise with the availability of 4K viewing options. Finally, certain types of communications will require much higher reliability, such as telesurgery, which will additionally need very low response times. To give an idea of the targeted data rate, more than 100 Gbits/s is expected for 6G according to [4].

To address this challenge, one of the methods used is the enhancement of coding techniques and carrier aggregation. Taking the example of 5G as discussed in [5], the authors analyzes the performance of the 5G UE (Device capable of accessing 5G networks) in terms of data rate and power

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consumption across several scenarios. The use of complex carrier aggregation up to 8 component carriers (CCs) and higher-order modulations up to 256-QAM is presented. Figure 1-6 shows the simulated and measured results for 5G NSA (non-standalone – initial deployment mode of 5G networks, where 5G NR new radio, is deployed alongside with existing 4G LTE infrastructure) in terms of data rate for four different modulation schemes (QPSK, 16-QAM, 64-QAM, 256-QAM) as a function of the complexity of carrier aggregation.

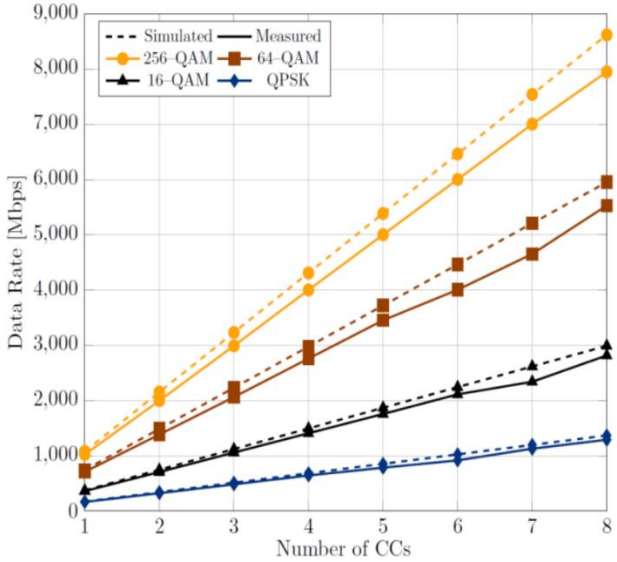


Figure 1-6: Maximum 5G data rate (Mbps) for different orders of QAM modulation in function of complexity of carrier aggregation (Simulation vs measurement) [5].

It can be observed that, generally, the data rate increases linearly with the number of aggregated channels, and thus the bandwidth increases proportionally. For example, QPSK (in blue) starts at 130 Mbps for a single channel and reaches 1050 Mbps for 8 channels. Furthermore, the data rate also increases with the complexity of the coding schemes. For 8 channels (8CC), the data rate rises to 1300 Mbps, 2800 Mbps, 5500 Mbps, and 8000 Mbps for QPSK, 16-QAM, 64-QAM, and 256-QAM, respectively. However, this comes with a noticeable impact on current consumption, as quantified and shown in Figure 1-7 (a).

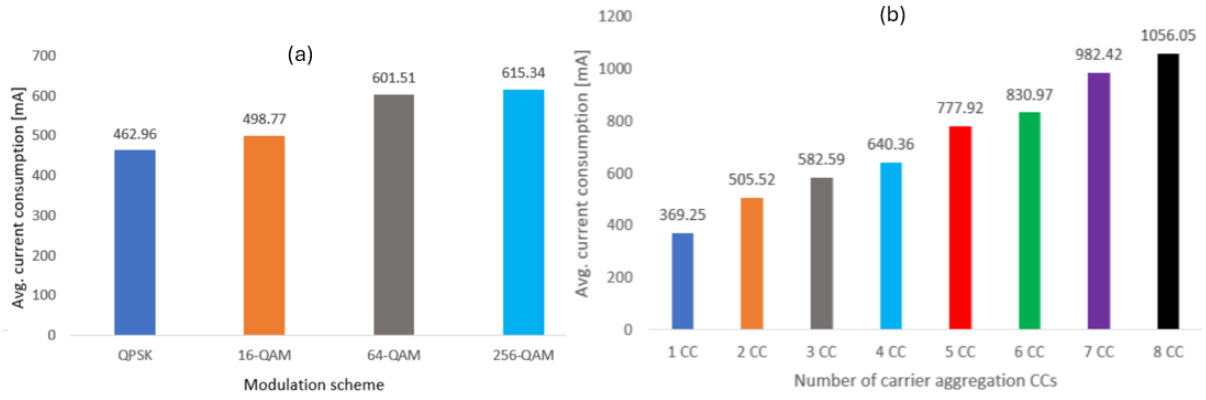


Figure 1-7: Average DC Current Consumption Considering Different Modulations and Carrier Aggregation

It is observed that the average current increases with the modulation order. The current rises from 463 mA for QPSK to 499 mA for 16-QAM, representing an increase of 8.5%. The difference between 16-QAM and 64-QAM is more significant, of 20%, reaching 601.5 mA. Finally, there is a slight increase of 2.3% in consumption to perform a 256-QAM. Globally, from a basic modulation QPSK to the most advanced one, a 33% increase in consumption is observed.

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Figure 1-7 (b) shows the consumption versus the number of aggregated channels. When moving from one channel to two, there is a difference of 136 mA representing 37%, reaching 505 mA. An increase between 50 and 150 mA is observed with each additional channel, reaching 1056 mA for 8 CCs compared to 369 mA for a single channel, representing a considerable increase of 697 mA. Globally, between 7% and 35% increase in consumption is observed each time that a channel is added.

In summary, the increased complexity of coding methods combined with carrier aggregation boosts the data rate but results in a significant increase in power consumption. Moreover, more complex coding schemes require better communication quality, commonly expressed as signal-to-noise ratio (Eb/No), to reduce communication errors. It is also important to recall that some immersive communication applications have stringent reliability requirements.

To support this point, in [6], the author compares the Bit Error Rate (BER), which represents the rate of erroneous bits transmitted, for different constellation sizes of M-QAM as a function of the signal-to-noise ratio, as shown in the Figure 1-8. For each constellation size, the author simulates with and without phase noise ($\theta_e = \pi/180$ is chosen) to quantify its impact on each M-QAM constellation size.

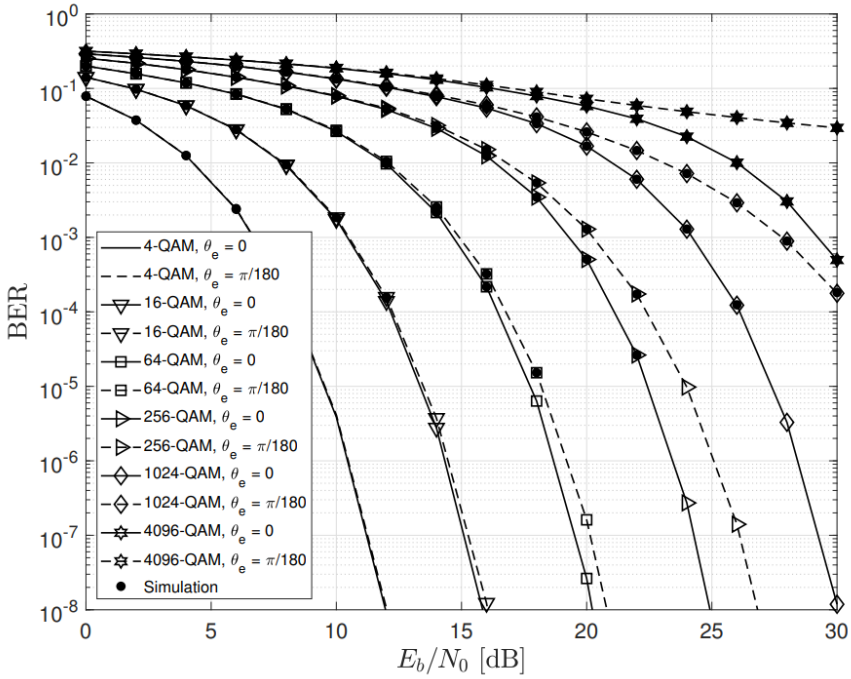


Figure 1-8: BER of square QAM for different constellation sizes. [6]

Overall, if we set a maximum acceptable BER criterion for example, limiting the error rate to 10^{-6} we find a required signal-to-noise ratio (SNR) condition depending on the constellation size. For instance, for 4-QAM, the system remains robust as long as $E_b/N_o > 10\ dB$, whereas under the same condition, 1024-QAM requires $E_b/N_o > 28\ dB$ without phase noise. This confirms the trend that larger constellations demand a much higher SNR to achieve acceptable BER performance.

Moreover, significant performance degradation due to phase noise is observed as the constellation size increases. To summarize, larger constellations are more sensitive to both E_b/N_o and phase noise, in addition to consuming more power than smaller constellations.

To increase data rates, another solution is to increase the operating frequency to naturally obtain wider bandwidths and thus higher data rates without necessarily resorting to very large constellations. In this context, several beyond-5G applications are considered, such as high-capacity backhaul and short-range device-to-device (D2D) communications [7]. Exploring sub-terahertz (sub-THz) frequencies

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appears promising and could be an ideal candidate to address these types of short-distance, point-to-point, very high data rate applications. However, this was not feasible in the past due to technological limitations. Thanks to the advancement of technologies with increasing $f_t/f_{\max}$, this is now becoming achievable. Figure 1-9, extracted from [8], shows an example of SiGe technology in terms of achievable f_t and $f_{\max}$, while, Figure 1-10, extracted from [9], presents SiGe NFET and InP technologies that could address these very high-frequency applications.

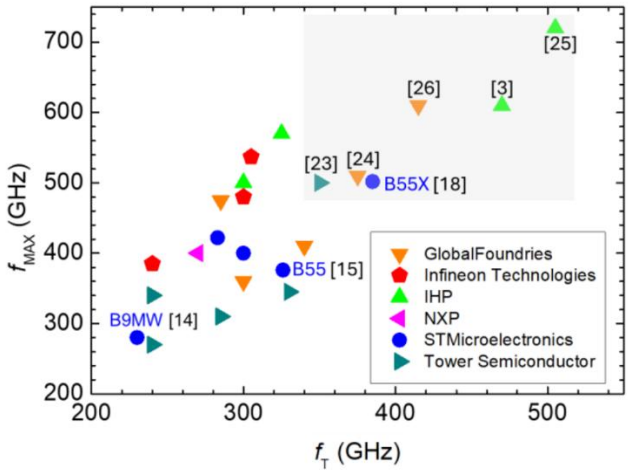


Figure 1-9: Peak f_t and $f_{\max}$ values of hight-speed SiGe HBT technologies (references are provided in [8] for $f_t > 350\ GHz$ and $f_{\max} > 400\ GHz$ and ST technologies).

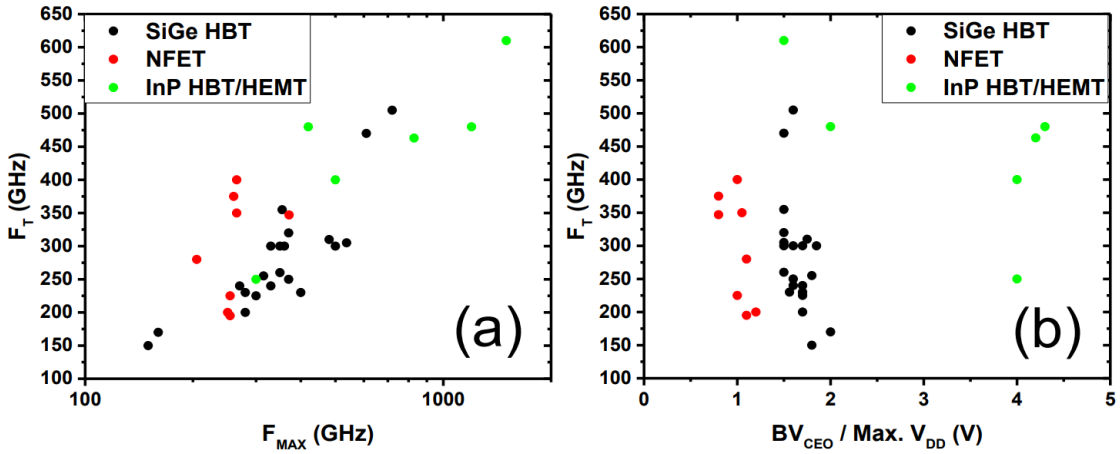


Figure 1-10: comparison of ultra-high-speed transistor technologies. (a) Scatter plot of published f_t vs $f_{\max}$ results, (b) Scatter plot of published f_t vs breakdown voltages from [9].

These high-speed transistor technologies enable operation up to 200 GHz in the sub-terahertz bands, allowing us to benefit from two major advantages. First, the availability of several tens of gigahertz unused bandwidth; second, the capability to develop ultra-massive multiple-input multiple-output (MIMO) antenna arrays within a reasonable spatial footprint, thanks to the size reduction associated with higher frequencies.

However, one of the main challenges to address in these frequency bands is the free-space propagation loss, which increases with the square of the frequency and exhibits absorption peaks, as shown in Figure 1-11, extracted from [10].

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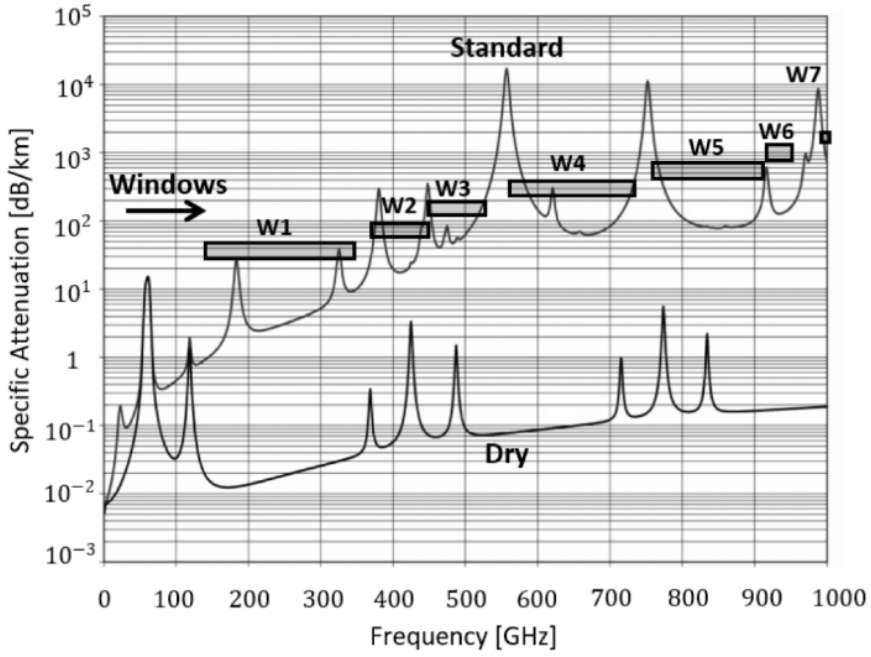


Figure 1-11: Average atmospheric absorption loss versus carrier frequency up to 1000 GHz. The two curves denote the standard, i.e., sea-level attenuation and dry air attenuation, where various peaks and troughs are observed for oxygen- and water-sensitive regions. The figure is from [10].

Figure 1-11 illustrates the increasing attenuation with frequency but also highlights absorption peaks in our band of interest, one around 120 GHz and another near 190 GHz. These absorption peaks make the transmission channel highly lossy. It is, therefore, necessary to avoid these regions. In our case, we will operate between these two peaks, naturally creating a band of interest that is largely unused, above 130 GHz but below 170 GHz (where integrated technologies can still generate gain). We will refer to this frequency range as D-band as defined in [11]. This band will be the focus of the research presented in this manuscript.

In [12], the author situates D-band high-data-rate wireless communication within the context of backhaul for point-to-point (P2P) communications between buildings, as part of a multi-radio access technology system also called wireless backhauling, as shown in Figure 1-12.

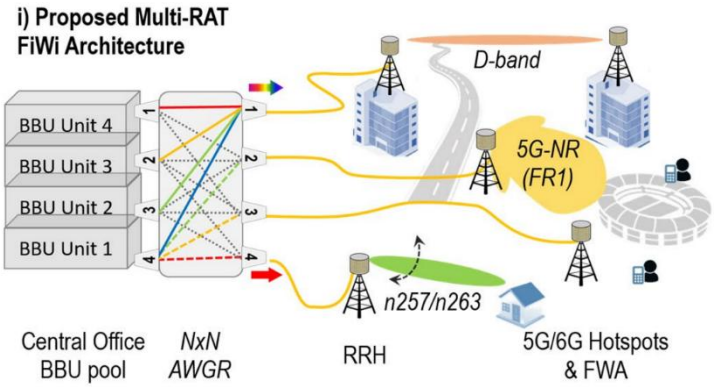


Figure 1-12: Illustration of the Fiber Wireless (FiWi) multi-radio access technology (multi-rate) proposed in [12].

Wireless backhauling has emerged as a crucial aspect in the architecture of modern telecommunication systems, particularly with the integration of millimeter-wave frequencies (mmWave) and the standardization of Integrated Access and Backhaul (IAB) by 3GPP (3rd Generation Partnership Project). This allows the same base station to serve both access and backhaul traffic, offering a cost-effective and flexible solution [13].

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To conclude, it is mandatory to continue to find solutions for enabling the data rate increase. Within the field of possibilities, it appears highly interesting and relevant to evaluate front-end modules (FEM) in the D-band to address wireless backhauling application, which will be presented in the next subsection.

1.1.2 Front End Module in D-band context and challenges:

The D-band frequency range, spanning from 130 to 170 GHz, has gained significant attention for its potential applications in high-capacity wireless links and imaging sensors, as introduced in the previous section. Several research efforts have focused on developing front-end modules for this frequency range. Some of them are presented below.

[14] reports wide-band TX and RX phased-array front ends for D-band using vector modulation, implemented in 0.13 µm SiGe BiCMOS process. The architecture is shown in Figure 1-13.

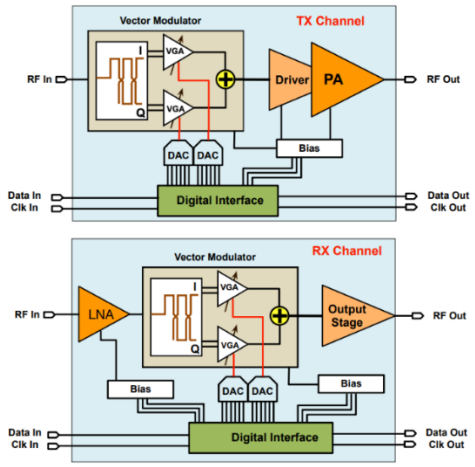


Figure 1-13: Architecture of the D-band TX and RX FEM operating between 130-170 GHz [14]

The TX front end is composed of a vector modulator followed by a two stage differential cascode power amplifier (PA). It yields an output power of 10 dBm, as shown in Figure 1-14, and a total gain of 16 dB.

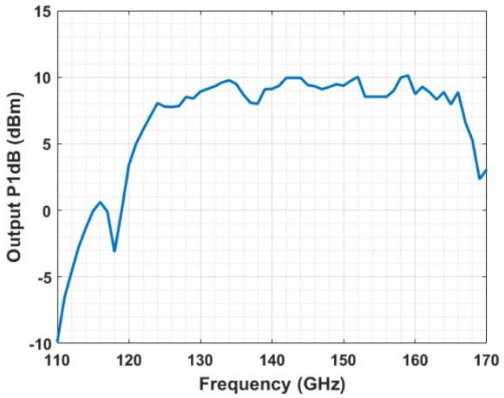


Figure 1-14: Measured TX front end output P1dB compression point [14]

The RX includes an LNA before the vector modulator. The LNA consists of two stages single-ended cascode. It exhibits a gain of 22 dB and a noise figure of 10 dB with an operating bandwidth of 40 GHz, as shown in Figure 1-15.

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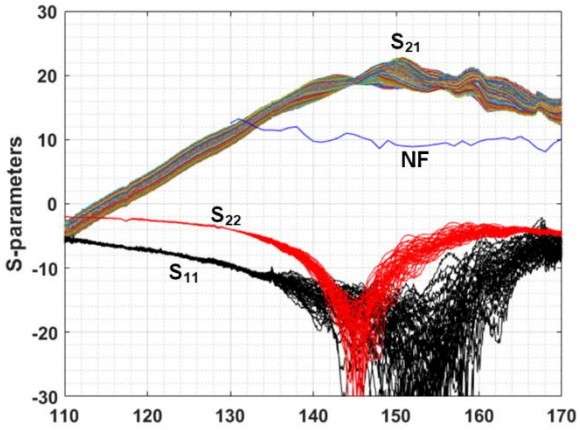


Figure 1-15: Measured S-parameters of the RX front-end module across all phase settings [14]

In addition to these advancements, [15] shows front-end active components, such as PAs and LNAs, which have been realized in InP DHBT technology (FBH's indium phosphide (InP) double heterojunction bipolar transistor (DHBT) transferred-substrate (TS) process). This INP technology showcases a $f_t/f_{\max}$ higher than 350 GHz, and a BV_{ceo} (breakdown voltage) of 4 V. The PA consists of a 2-way combined cascade unit cell of single emitter topology. It shows a small gain of 12 dB and large signal measurement shows an output $P_{1dB} = 13\ dB$ and a $P_{sat} = 14\ dBm$ with a power added efficiency (PAE) of 10%, as shown in Figure 1-16.

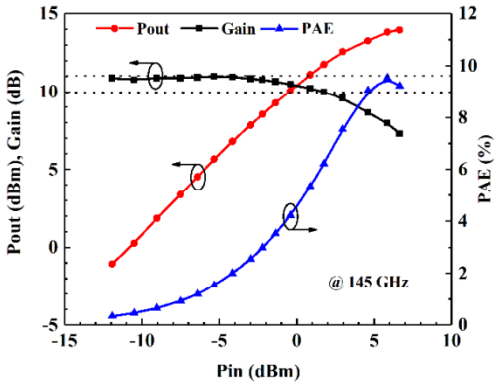


Figure 1-16: Measured gain, output power and PAE of the power amplifier at 145 GHz, from [15]

For the LNA, the authors used a 2-way combined cascode unit cell. The small signal measurement showed a small-signal gain of 10-16 dB and 8.5-11 dB noise figure (NF) with a PAE of 11%.

Another work reports the development of some key building blocks for D-band front-end module in SiGe technology, that shows promising performances [16]. Figure 1-17 summarizes the main building blocks.

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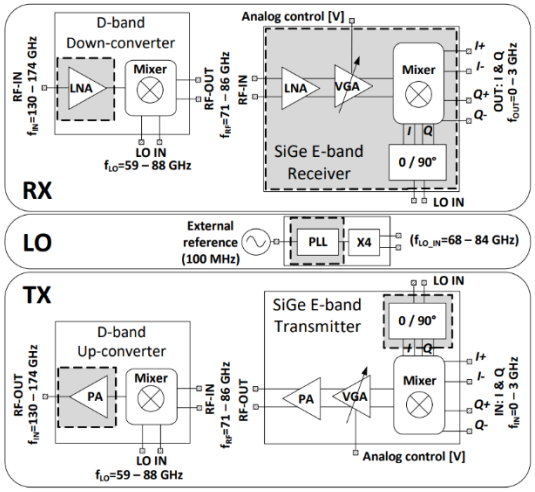


Figure 1-17: FEM block diagram from [16]

Focusing on the TX part, a PA was designed by cascading three common-base stages to achieve a gain of 24 dB, a P_{1dB} of 16.8 dBm, and a PAE of 17%, as shown in figure 1-18.

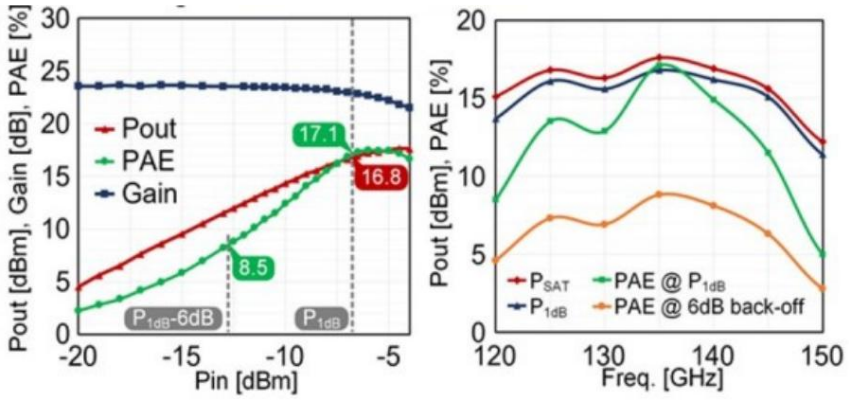


Figure 1-18: D-band multi-stage power amplifier measurement from [16].

Overall, the FEM architecture remains relatively simple. When focusing on the TX side, vector modulation for phase shifting and beamforming is commonly employed, followed by a PA at the output, which is often the limiting device according to the state of the art. Nonetheless, these SiGe D-band front-end modules demonstrate competitive performance with output power at the compression point (P_{1dB}) exceeding 10 dBm and gain higher than 15 dB, showing promising potential for enabling D-band backhaul communications. This motivates our interest in this topic while highlighting some key challenges.

These challenges arise from two main factors: propagation loss in free space, which necessitates high output power from the TX chain, and the good but limited $f_t/f_{\max}$ of active devices, which restricts their ability to generate gain and power at the frequency of interest. This leads to the need for highly performant passive devices that leverage the superior characteristics of distributed passives — a topic that will be discussed in another subsection of this document.

To conclude, the state of the art demonstrates that the consideration of front-end modules in the D-band is realistic, although many challenges remain to be addressed. Thus, the main challenges chosen to be addressed in this document are power amplification and the quality of passive devices. Therefore, our objective is to propose a cost-efficient approach to address these challenges by maximizing the benefits of operating at higher frequencies. To do so, the next subsection will discuss the technologies used for the D-band and the state-of-the-art power amplification methods, focusing on PAs in the D-band.

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The following subsection will then cover the second requirement: high-performance passive components. To this end, we will review the state of the art of some passive building blocks in D-band FEM modules.

1.1.3 Power amplification in D-band

1.1.3.1 Technologies that enable amplification

In the high-frequency FEM design market in general, and specifically in the PA design sector, three technologies are competing, as already mentioned: InP-based HBTs, deep sub-micron CMOS, and SiGe BiCMOS. Figure 1-19, taken from [9], shows a comparison of the published performance of these three ultra-high-speed transistor technologies.

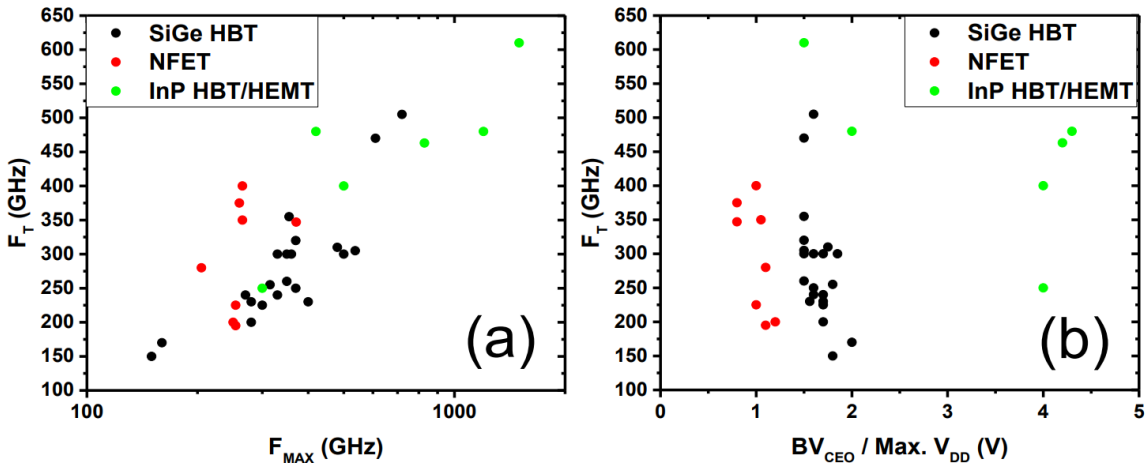


Figure 1-19: comparison of ultra-high-speed transistors. (a) scatter plot of published F_T vs F_{MAX} results, (b) Scatter plot of published f_T vs BV_{CEO} from [9].

Figure 1-19 (a) shows the f_T performance as a function of f_{max}. InP leads with a significant margin, followed by SiGe, and finally CMOS transistors lagging behind. Figure 1-19 (b) presents f_T as a function of the breakdown voltage BV_{CEO}. Once again, the same trend is observed: InP significantly outperforms its two competitors, with BV_{CEO} values reaching up to 4.5 V, followed by SiGe HBT with values around 1.8 V, and finally NFETs around 1 V.

To summarize, SiGe HBTs outperform NFETs in terms of f_T/f_{max} and far exceed them in voltage handling capability. Furthermore, InP-based devices are by far superior to the two silicon-based devices. However, there are very high cost and offer a low integration level. Perhaps more important, they are coming with a poor Back End Of Line (BEOL) quality, which limits their usage, making it even impossible to consider for the design of a fully integrated front-end module with high-quality passives and with digital parts. This restricts their utility to final PA stages, for example, but they must always be mounted on another silicon-based technology.

All these factors, combined with the fact that SiGe BiCMOS 300-mm wafers are by far the cheapest in terms of price per unit area, make it an ideal candidate for designing wideband circuits in the D-band. Finally, Table 1-1 summarizes a qualitative comparison between the three technologies capable of addressing FEM design in the D-band.

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	$CMOS$	$SiGe\ HBT$	$InP\ based\ HBT$
$f_t/f_{\max}$	$-+$	$+$	$++$
BV_{CEO}	$-$	$+$	$+++$
$Cost\ effectiveness$	$+$	$+++$	$--$
$Integration\ capability$	$+++$	$+++$	$---$

Table 1-1: Comparative summary table of the three major technologies capable of addressing high-frequency power amplifier design

As my thesis is conducted within STMicroelectronics, let's have a look at the behavior of its SiGe technologies. Recent technology stands out as one of the world's highest performing while incorporating MOS devices. Figure 1-20 showcases STMicroelectronics's portfolio of these SiGe HBT technologies, highlighting on one hand the performance metrics in terms of f_T and f_{max}, and on the other hand the CMOS technology node, and finally the BV_{CEO}.

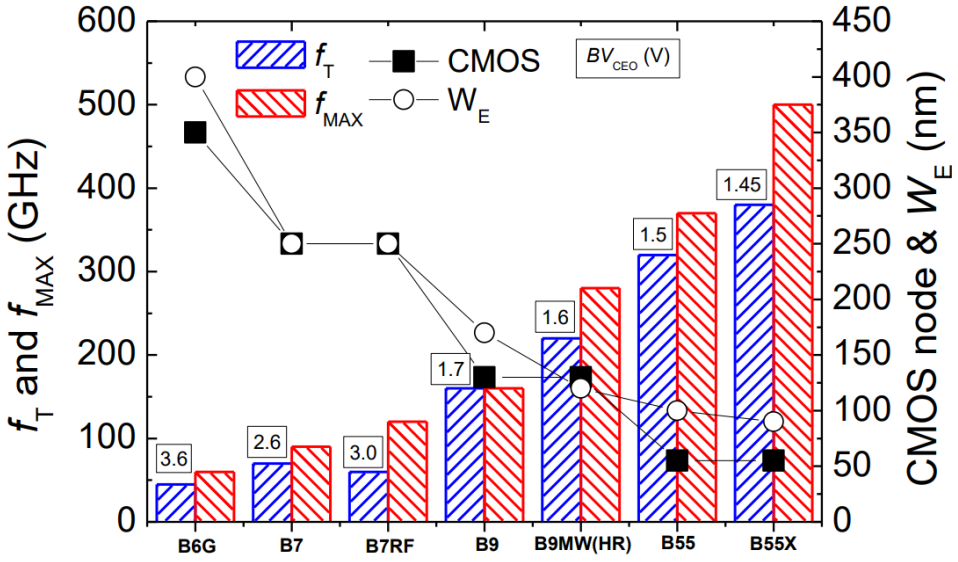


Figure 1-20: STMicroelectronics high-speed SiGe BiCMOS technologies (HBT performance & CMOS node). W_E is the physical emitter width. BV_{CEO} is the emitter-collector breakdown voltage of the HBT with an open base. F_T and f_{MAX} correspond to the peak values measured for the SiGe HBT [8].

An improvement in f_T and f_{max} is observed alongside a decrease of BV_{CEO}, as these parameters are inversely proportional, depending on multiple factors, in particular the collector doping. Starting from the B6G, which exhibits very low f_T and f_{max} but a high BV_{CEO}, up to the B55X, which offers the highest performance among the technologies available today. The latter features an f_T greater than 380 GHz and an f_{MAX} exceeding 475 GHz, with a BV_{CEO} of 1.45 V.

To summarize, having demonstrated the advantages of SiGe technologies over NFET and InP-based devices and given access to one of the world's highest performing SiGe HBT technologies, it was therefore a natural choice for this work to select the B55X technology.

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1.1.3.2 State of art of power amplifiers

In the context of D-band PA design using SiGe-based HBT technologies, the state of the art presents several examples reflecting different strategies and increasingly highlighting challenges that must be addressed to optimally enable this critical PA design block, previously identified as essential for the TX FEM section.

In [17], the author emphasizes two major challenges in D-band PA design with high-speed SiGe HBT technologies. First, the increasing impact of parasitic elements in transistor interconnections, which degrade transistor performance, coupled with increased losses in interconnections due to the skin effect. Second, the scaling down of transistors and modifications in doping and HBT architectures, which indeed increase f_T/f_{max} but simultaneously reduce the transistors' breakdown voltage, thereby limiting achievable power levels. The author's strategy therefore focuses on a well-controlled single-path topology, which reduces the impact of interconnections and greatly simplifies the design. The chosen architecture is a two-stage cascode amplifier employing transmission lines and integrated capacitors, as shown in Figure 1-21. The choice of this cascode topology is largely due to the fact that the common-base transistor (output transistor) can sustain a voltage swing significantly higher than BV_{CEO}, closer to BV_{CBO}, benefiting from the low impedance at the base of the common-base transistor.

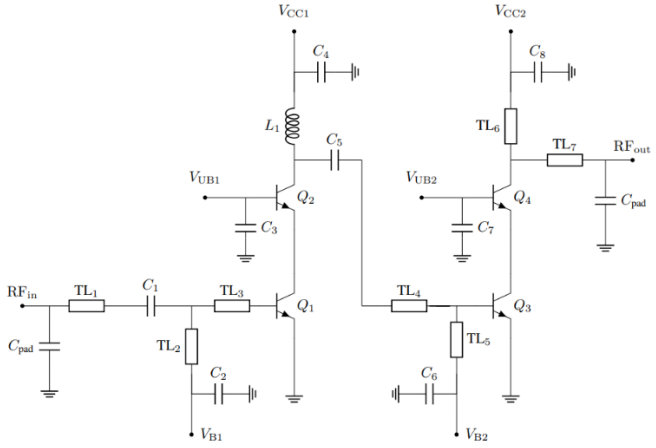
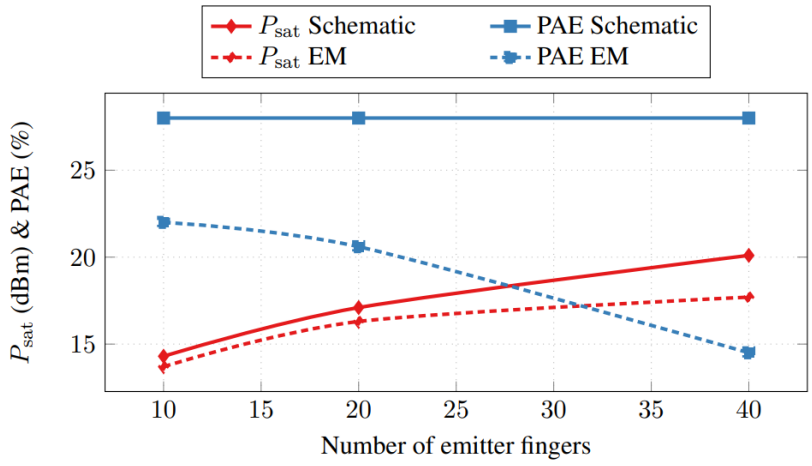


Figure 1-21: Schematic of a 2-stage cascode power amplifier realized in IHP's 0.13 µm SiGe BICMOS [17]

Preliminary studies on transistor sizing were conducted upstream, concluding that due to interconnections degrading transistor performance, the gain on P_{sat} decreases as the transistor size increases. Furthermore, the PAE also decreases with increasing size, as illustrated in Figure 1-22, which shows the saturation power (P_{sat}) and PAE as a function of the number of emitter fingers.



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Figure 1-22: Simulated P_{sat} & PAE vs device size from [17].

The design was implemented and measured using the IHP's 0.13 µm SiGe BiCMOS SG13G2 technology, featuring an f_T/f_{max} of $300/500\ GHz$ and a breakdown voltage (BV_{CEO}) of 1.7 V. The large-signal performance is shown in Figure 1-23.

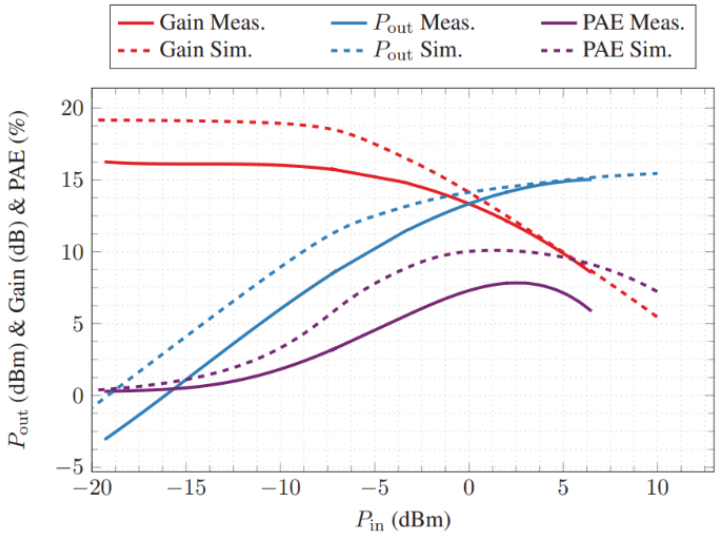


Figure 1-23: Measured and simulated large signal parameters at 140 GHz from [17].

According to the authors, the PA achieves a saturation power (P_{sat}) of 15 dBm and a PAE of 7.8% at 140 GHz. However, our primary focus remains on the compression point. Examining the 1-dB compression point of the large-signal gain, the output power at 1 dB compression (OP_{1dB}) is 11 dBm with a corresponding PAE of approximately 5%. We can notice a difference between simulation and measurement as example for the gain around 2.5 dB of dB is seen.

Small-signal measurements were also performed, revealing a 3-dB bandwidth of 21 GHz, with a maximum gain of 16.7 dB centered at 135 GHz, as illustrated in Figure 1-24.

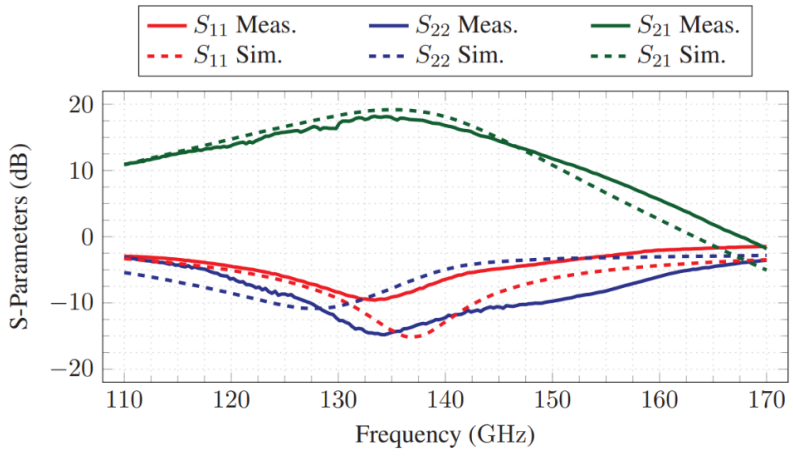


Fig. 5. Measured and simulated small signal S-parameters

Figure 1-24: Measured and simulated small signal S-parameters from [17].

To summarize, one of the main challenges is the interconnection losses and parasitics. Consequently, there is a limit to the trend of increasing transistor size versus increasing P_{sat}. We can also observe a tendency to use cascode topologies to increase the voltage swing (V_c), thanks to the

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impedance presented at the common base (CB) of the cascode transistor. And finally multi-stages PA approach is used because of technology limitations that make hard to deliver enough gain in D-Band.

Another strategy is presented in [18], where the authors adopt a fully differential approach with unit cascode cells. Hence, the amplification topology remains the same, i.e. cascode, but the approach to realize the matching network is completely different. While most works use interstage matching based on transmission lines and capacitors, the authors propose to use an impedance transformer, as shown in the schematic in Figure 1-25. The transformer has the advantage of being a compact and efficient high-order filter.

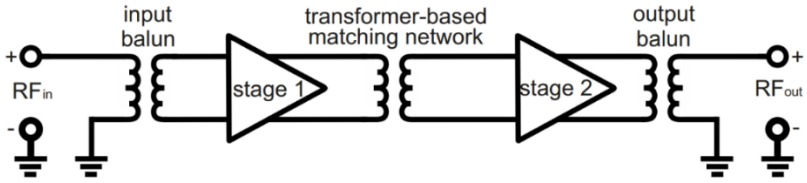


Figure 1-25: Block diagram of the fully differential D-band PA [18]

According to the authors, the advantage of using differential architecture lies in the layout symmetry combined with the presence of an AC virtual ground. The choice was therefore made to be able to implement a fully differential design to suppress even-order harmonics and achieve better common-mode rejection ratio, resulting in improved stability. The transformers are based on coupled lines and are connected as baluns at the input and output stages.

The implementation was carried out using a 0.13 µm SiGe BiCMOS technology but no performance details of the technology were disclosed by the authors. Nevertheless, given the high voltages applied, it is estimated that the BV_{CEO} must be greater than 1.6 V, with an f_T/f_{max} sufficient to provide gain at the desired frequency. Measurements were performed on the circuit, showing output power and gain, then PAE as functions of input power, presented in Figure 1-26 and Figure 1-27, respectively.

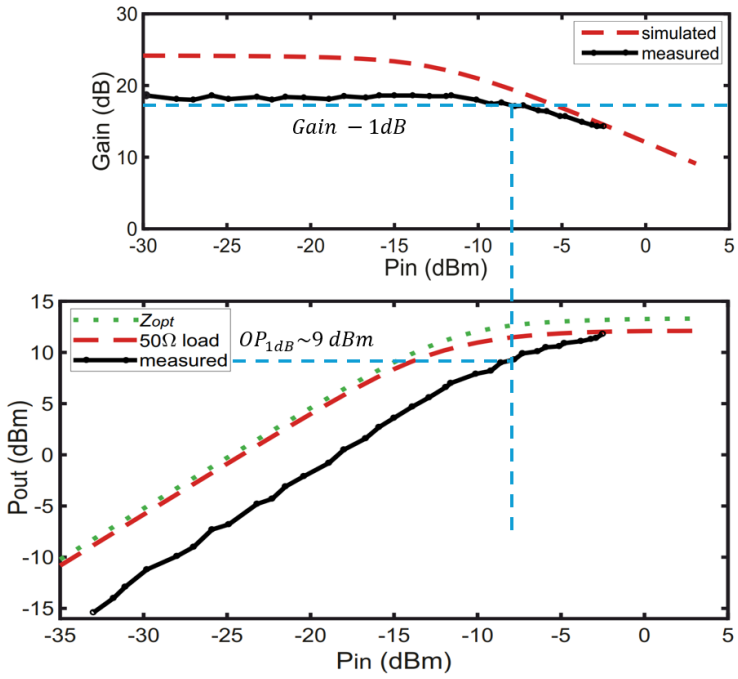


Figure 1-26: gain and P_{out} vs input power, from [18].

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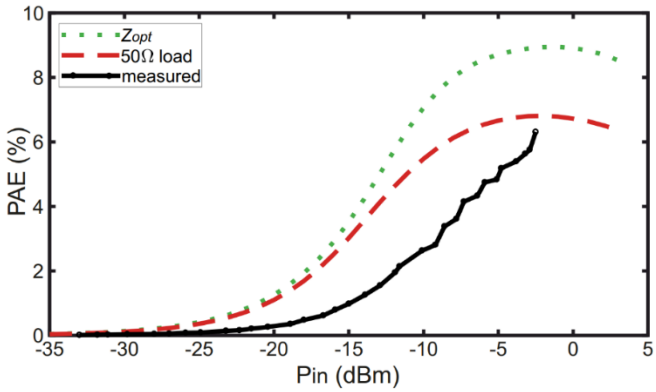


Figure 1-27: PAE vs input power, from [18].

Measurement results, according to the authors, show a maximum PAE of 6.3% and a P_{sat} of 11.8 dBm at 114 GHz in a 50 Ω impedance system, with a power consumption of 231 mW. At the 1-dB compression point, the output power (OP_{1dB}) is 9 dBm, and the PAE at P_{1dB} is below 4%.

To summarize, the authors leveraged the advantages of the differential topology and the compact footprint of transformers compared to simple transmission lines, achieving a reduced chip area of 0.35 mm².

[19] presents another strategy: balanced power amplifiers. This approach uses a two-path PA where the input and output signals are phase-shifted by 90° using an hybrid coupler, as illustrated in the schematic in Figure 1-28.

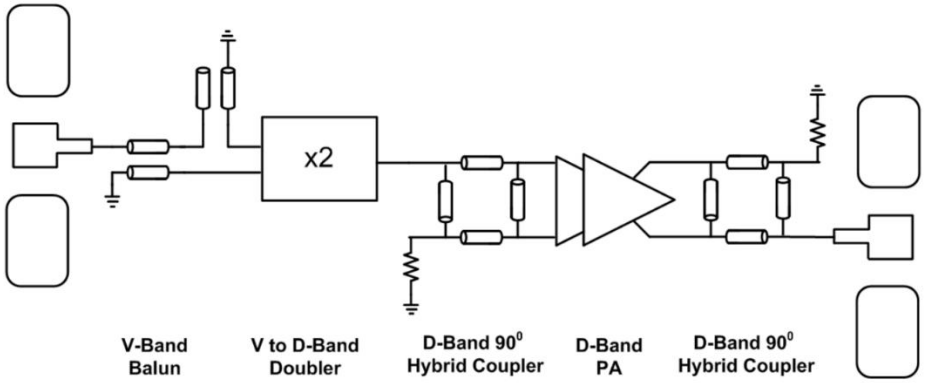


Figure 1-28: Block diagram of the multiplier chain [19].

According to the authors, the isolation of the hybrid coupler is very important in this case because it enhances stability and minimizes mutual loading between the PA output stages. Similarly to the differential case, since this is a two-way PA, it increases the output power by 3 dB, minus the losses of the combining device (in this case, a branch-line coupler). The PA topology consists of a three-stage cascode, as shown in Figure 1-29.

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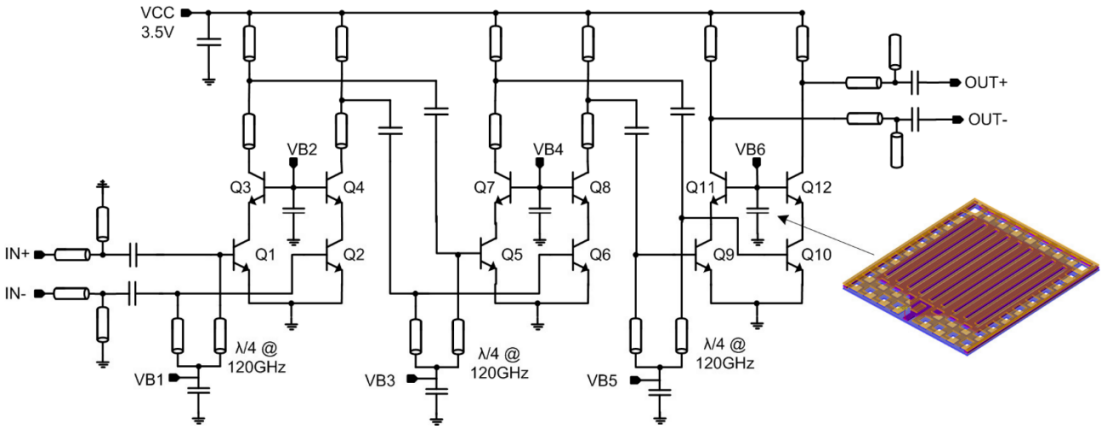


Figure 1-29: Schematic diagram of the D-band Power Amplifier [19].

As seen in Figure 1-29, matching networks rely on microstrip transmission lines and MIM capacitors (Metal Insulator Metal). For the transmission lines, the authors used side-shielded microstrip lines to prevent electromagnetic (EM) coupling between adjacent stages, thereby improving both stability and modeling accuracy in a dense layout. While this approach simplifies modeling and design, it comes at the cost of an increased footprint.

The implementation and measurements were carried out using IBM's 0.12 µm SiGe BiCMOS 8HP technology, featuring an f_T of 200 GHz and an f_{max} of 250 GHz. Figure 1-30 shows the small-signal measurement results.

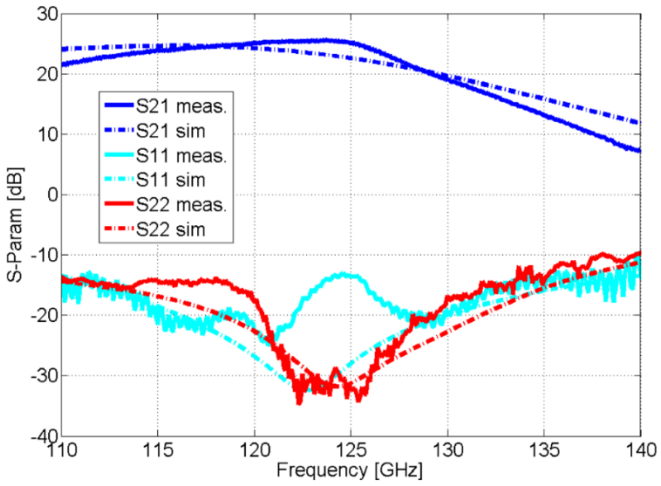


Figure 1-30: Measured S-parameters of the Power Amplifier, from [19].

Measurements show a peak small-signal gain of 25 dB at 123 GHz with a 3-dB bandwidth of 16 GHz. Simulation and measurement feet well. Large-signal measurement results are presented in Figure 1-31.

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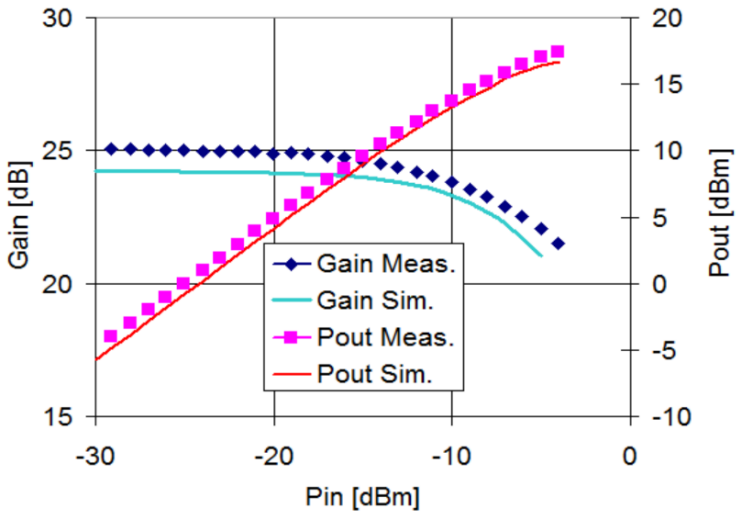


Figure 1-31: Large-signal measurement of the Power Amplifier, from [19].

Figure 1-31 shows the power sweep at 120 GHz. The PA delivers a P_{sat} of 17 dBm and a P_{1dB} of 13.3 dBm, consuming a current of 160 mA at a supply voltage of 3.5 V. This results in a PAE of less than 3%. The quality of the used passive components (this will be discussed in the next subsections) limits the achievable performance, in addition to the relatively low f_T and f_{max} compared to other works. Nevertheless, a clear improvement in output power is observed when employing a multi-path architecture.

[20] presents an approach that is similar to [17], given that it is a single-path design (no parallelization). However, it introduces a topology rarely seen before: the common-base (CB) configuration. The author highlights the merits of this topology in improving power efficiency through several factors, which are as follows: higher breakdown voltage; sharp compression profile due to enhanced linearity; and supply current adapted to the signal amplitude via current clamping [21]. The design is based on a four-stage CB amplifier with matching networks composed of transmission lines and capacitors, as shown in the schematic in Figure 1-32.

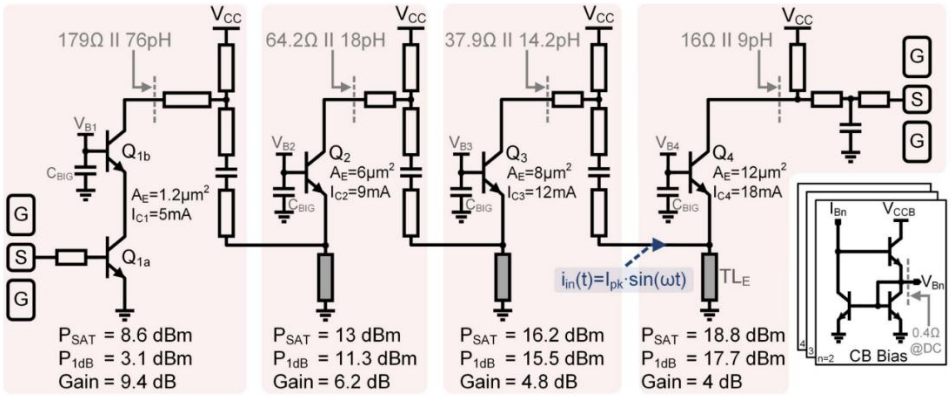


Figure 1-32: Schematic of the single ended 4-stage CB PA, from [20].

The design was done using STMicroelectronics's SiGe 55-nm technology called B55 [22]. Figure 1-33 shows S-parameters measurement results for the single ended 4 stages CB stacked PA.

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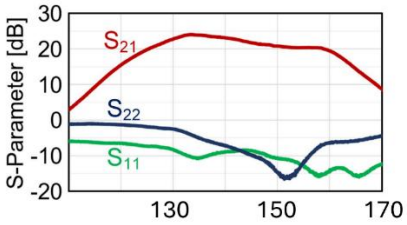


Figure 1-33: Measured S-parameters for single-ended PA [20].

Small-signal measurements of the four-stage CB PA show a maximum gain of 24 dB at 133 GHz. Figure 1-34 presents the large-signal measurements of the PA, including output power, PAE, and gain.

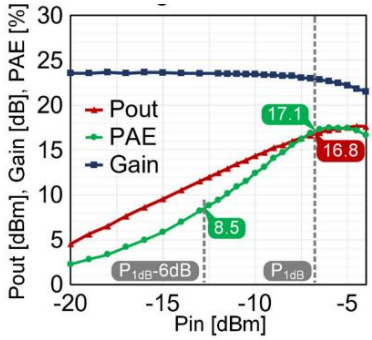


Figure 1-34: Measured large signal performance in terms of output power, PAE and gain of the single ended power amplifier [20].

Large-signal measurements show a P_{sat} of 17.6 dBm and a P_{1dB} of 16.8 dBm at 135 GHz. A very small difference between P_{1dB} and P_{sat} is observed, which confirms the second advantage highlighted by the authors: a "sharp compression profile due to enhanced linearity". One of the breakthroughs of this article is the PAE at P_{1dB}, which reaches 17%, among the best reported and significantly higher than many other designs. The PAE remains at 8.5% even at 6-dB back-off ($P_{1dB-6dB}$).

As shown in Figure 1-35, the measured DC current of the CB stages increases with output power due to current clamping, exhibiting a total DC current consumption of 130 mA at P_{1dB}, and nearly half at $P_{1dB-6dB}$, resulting in a class-B-like back-off profile. This confirms the third advantage claimed by the author: "supply current adapted to the signal amplitude by means of current clamping".

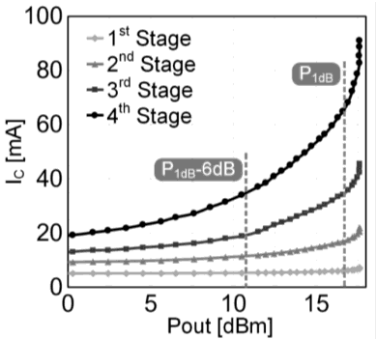


Figure 1-35: Measured DC current for each stage vs Pout [20].

To summarize, the authors employ a classical approach with a four-stage stacked unit cell. The key difference lies in the amplification topology, which is CB. The interest of the innovation claimed by the authors is confirmed by measurements. The power handling capability is indeed superior, as the transistor is biased at 2.2 V, allowing for a higher voltage swing and thus confirming that voltage handling is significantly better for CB topologies due to the impedance presented in the base. Secondly, the P_{1dB} is very close to P_{sat}, indicating a sharp compression profile and demonstrating the improved linearity of the

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CB design. Finally, an excellent PAE is observed, which remains high even at 6-dB back-off. This is justified by the fact that the DC current adapts and varies with output power due to current clamping. Therefore, it seems very interesting to further explore the CB topology in the D-band for PA design.

[23] presents a PA using a parallelized approach based on a two-stage cascode, as shown in Figure 1-36. The authors employ a T-junction power divider at the input and a four-way coupled line combiner at the output. The latter is much more compact and exhibits low loss. This strategy can thus be described as a four-way parallelization using a passive device based on coupled lines, which, according to the authors, improves circuit performance. This highlights again the critical role of passive components in the context of D-band PA design.

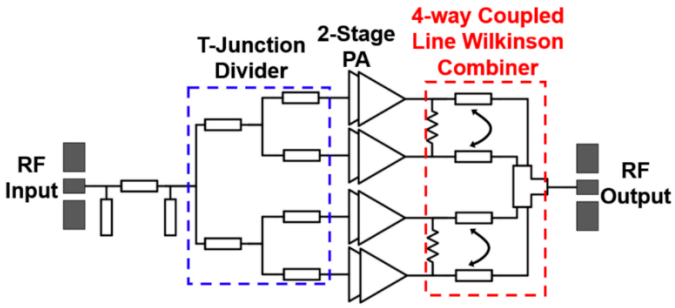


Figure 1-36: Block diagram of the proposed four-way combined PA, from [23].

The driver and power cells are composed of SiGe HBT transistors with parallel emitter fingers and a size chosen to achieve a trade-off between output power and bandwidth. Figure 1-37 shows the schematic of a single PA unit cell.

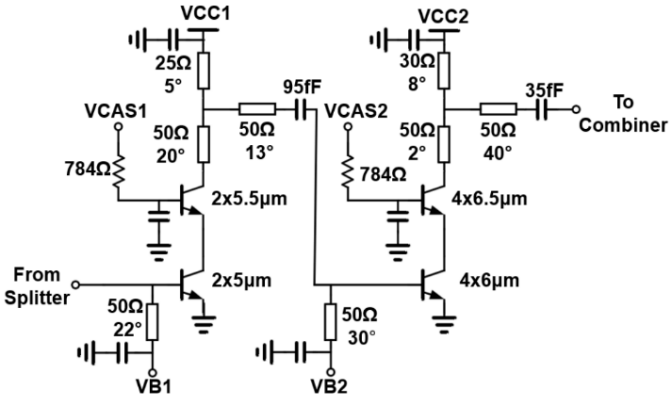


Figure 1-37: Full circuit schematic of the unit PA cells, from [23].

According to the authors, using coupled line-based combiner vs classic Wilkinson topology has several advantages regarding the insertion loss and matching. This will be discussed during the following subsection concerning passives.

Design was done in IBM's SiGe BiCMOS technology showing a f_t/f_{max} of $300/360\ GHz$ and a $BV_{CEO} = 1.7\ V$ [24] . The measured S-parameters are shown in Figure 1-38.

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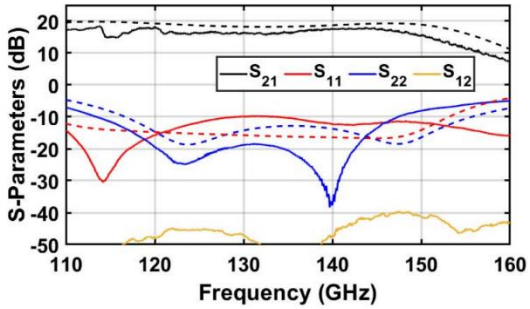


Figure 1-38: Simulated (dashed) and measured (solid) S-parameters for the proposed D-band PA, from [23].

The PA exhibits a peak gain of 18.2 dB with a 3-dB bandwidth spanning from 110 GHz to 145 GHz. The return loss remains around 10 dB across the same bandwidth. Large-signal simulations were carried out, showing a peak output power of 21.9 dBm with a peak PAE of 12.5%. The P_{1dB} is 18.6 dBm, with a corresponding PAE below 9% at the 1-dB gain compression, as shown in Figure 1-39.

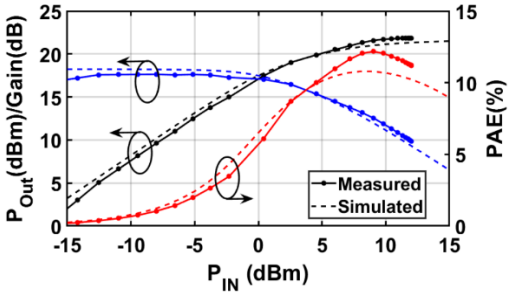


Figure 1-39: Measured large-signal power sweep at 130 GHz for the 4-way PA, from [23].

To sum up, the authors proposed a parallelized approach using an innovative passive device (power combiner) that enables state-of-the-art output power with good PAE. The design employs a classic two-stage cascode with interstage matching based on transmission lines and capacitors, similar to the majority of the works in the D-band. The innovation clearly lies in the power combiner, allowing the achievement of excellent performance in the D-band. Investigating the parallel approach with such power combiners appears very promising.

To review all the papers discussed above, a comparative table of different PAs, with their architecture, the technology, and the corresponding performance, is shown in Table 1-2.

Ref	Topology	SiGe Techno	f_t/f_{max} (GHz)	BV_{CEO} (V)	Frequency (GHz)	Gain (dB)	P_{sat} (dBm)	P_{1dB} (dBm)	$PAE\ @\ P_{1dB}$ (%)	P_{dc} (mW)	Area (mm^2)
[19]	Single 2 stage cascode	IHP's 130 nm	300/500	1.7	125-146	18.2	15	11	5	?	0.46
[20]	Differential 2 stage cascode	? 130 nm	?	?	109-119	18.5	11.8	9	<4	230	0.35
[21]	Balanced 3 stage cascode	IBM's 120 nm	200/250	?	112-128	25.5	17.5	13.3	<3	560	?
[22]	Single 4-stage CB	ST B55 55 nm	325/375	1.5	125-159	24	17.6	16.8	17.1	286	0.18*
[24]	4-way parallel 2-stage cascode	IBM's 90 nm	300/360	1.7	110-145	18.2	21.9	18.6	9	?	1.7

Table 1-2: Summary table of various power amplifiers, their topologies, performance metrics, and technology.

A clear trend emerges from Table 1-2. Multi-stage PAs are commonly used for achieving the desired gain, which naturally creates a need for inter-stage matching. This matching is often implemented using simple transmission lines and capacitors, which occupy significant areas and introduce losses. It is evident that this aspect requires further investigation. Moreover, we have seen that most of the PA area

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is occupied by passive components, highlighting the importance of studying and ultimately reducing their footprint.

Next, an overwhelming majority of designs use the cascode topology, which combines high gain, good isolation between input and output, and a higher voltage swing thanks to the second transistor operating in CB configuration. This is the prevailing topology, and based on the state-of-the-art study, it would be the natural choice for designing a product. However, the authors of [20] demonstrate the interest of the CB cell, which is rarely used, especially in the D-band. This reminds us of the primary advantage of voltage swing that cascodes boast, while also exploiting all the benefits of the CB topology in the D-band. To recall, these advantages are: higher breakdown voltage, sharp compression profile due to enhanced linearity, and supply current adapted to the signal amplitude via current clamping, which improves PAE. Furthermore, the authors achieve the best combined performance, notably with a single-path design. This topology is clearly worth further exploration.

Moving on, where the works differ somewhat is in the choice of architecture, the majority adopt differential designs for their advantages of virtual AC ground and symmetrical layout. Others prefer balanced architectures, which, like differential multi-path approaches, improve robustness against load impedance variations. The least explored approach is parallelization, which offers a significant advantage in output power and appears to be the best solution.

Therefore, we have decided to study parallelized PA structures in the D-band while investigating the topology that provides the best PAE with the second-best P_{1dB}, which is the CB topology. Moreover, to the best of our knowledge, the combination of CB and parallelized PA has never been explored before, which is exactly what we propose to do.

However, given the need for multi-stage designs and thus effective management of matching networks, as well as the necessity to develop power splitters and combiners, it is clear that the study and development of passive components are key to the success of our strategy and, consequently, to the performance of the targeted multi-stage parallelized CB PA topology. More generally, enabling passive building blocks is a necessity for D-band FEM module design. For this reason, we propose a brief state-of-the-art review of passives used in the D-band, which is addressed in the next subsection.

1.1.4 State of art of passives devices in D-band

When discussing front-end module or PA design, traditionally work is done at low frequencies using a library of lumped components such as inductors and capacitors provided by foundries. Taking as an example the B55X technology from STMicroelectronics, which was used throughout this thesis, according to [25], the technology offers microstrip lines, inductors, varactors, and capacitors, with a fairly comprehensive back-end process. Some of the offers are shown in Table 1-3.

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ILLUSTRATION OF REACHABLE PERFORMANCES OF ELECTROMAGNETIC RF/MMW PASSIVES IN B55X 6, 7 AND 9ML CU BEOL (8ML CU OF [3] IS GIVEN FOR COMPARISON)

Devices	Description	Cu BEOL	Performances	
Inductors	800 pH @ 10 GHz	6ML	Qsingle-ended	22.5
		7ML		22.7
		8ML		*19.8*
		9ML		23.2
	300 pH @ 20 GHz	6ML	Qsingle-ended	28.8
		7ML		29.0
		8ML		*26.1*
		9ML		30.2
Microstrip transmission lines	50 Ω @ 28GHz	6ML	α (in dB/mm)	0.284
		7ML		0.272
		8ML		*0.275*
		9ML		0.227
	50 Ω @ 77GHz	6ML	α (in dB/mm)	0.478
		7ML		0.462
		8ML		*0.500*
		9ML		0.379

Table 1-3: Table of reachable performances of passives in B55X from [25]; nowadays only the 6ML and 7ML are produced.

This offer reflects well the demand at RF and low mmWave frequencies below 80 GHz, which currently forms the core of the market. The main issue remains the losses associated with these lumped components.

However, if we want to look forward and prepare for a market addressing high-frequency wireless FEMs, e.g., in the D-band, we must address the needs specific to this frequency range. As shown in the previous section, at high frequencies, even high-speed technologies struggle to generate gain and power due to f_T and f_{MAX} limitations, and low breakdown voltages, which limit efficiency and output power. To address PA design, as seen in the previous section, several strategies were explored, but one key aspect remains critical: passive components.

The founders offer RF-oriented technologies such as B55X, which include thick and medium-thickness metal layers (as shown in Figure 2-10) that improve the quality of passive components by reducing their losses. Unfortunately, there is no high-resistivity (HR) substrate option available for B55X, which could further reduce losses. A comprehensive study of the back-end stack and its optimal usage is therefore required.

According to the state of the art, passives devices used in D-band are mostly distributed. For instance, as reported in [17], [19], and [20], the matching networks are made of simple microstrip lines and capacitors, an approach that is quite simple and easy to model, but involves a large footprint. In addition, the vast majority of the PA area is occupied by these passives, as can be observed, for example, in Figure 1-40 from [20].

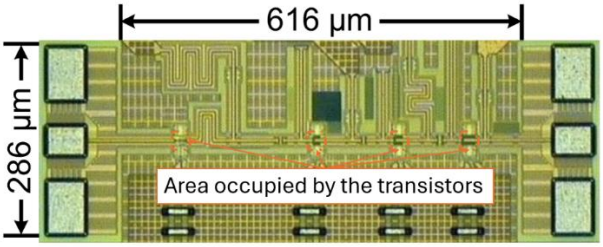


Figure 1-40: Chip microphotography of the cascaded CB PA from [20] with a highlight on the transistor occupied area, showing that the majority or the PA chip area is occupied by the passive components.

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Being an important factor for losses and area contribution, it is evident that there is significant interest in conducting a deeper investigation of passive devices for PA design, with the goal of enhancing overall performance. Moreover, as seen in [18], many differential PAs require baluns and transformers, highlighting another major component of interest. In [19], the authors designed a balanced PA using branch-line couplers at both input and output. The choice of coupler topology is critical, and the integrated branch-line coupler struggles to find its place. Conversely, the coupled line coupler is much more efficient and outperforms in many aspects. Finally, the chosen approach is parallelization, which inherently requires power dividers and combiners. To address some of these challenges, this section is organized as follows: first, a brief overview of couplers used in the state of the art is carried out; then a discussion on power dividers and combiners based on coupled line couplers is achieved.

1.1.4.1 Couplers

If we refer to [19], one common application of couplers is to employ them as power splitters and combiners with a 90° phase difference for the design of balanced power amplifiers, as shown in Figure 1-41. To achieve this, the authors use a branch-line coupler. This coupler consists of four transmission line sections forming a square. Each corner of the square serves as a port, and each pair of parallel sides has the same characteristic impedance.

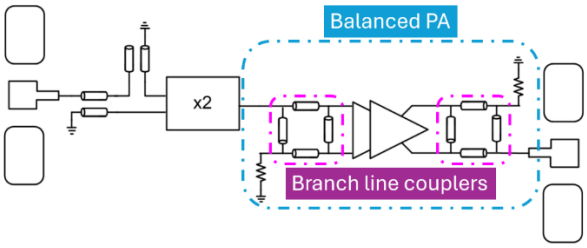


Figure 1-41: Block diagram of the multiplier chain from [19], with a highlight in blue on the balanced PA and in pink into the device of interest that is the branch-line coupler.

According to the authors, the branch-line coupler operates with low insertion loss (IL); simulations show IL around 0.6 dB, which is attributed to its wide transmission lines. It also provides wideband isolation between its input ports. In addition, it shows a reduced area Thanks to a folded configuration, as shown in Figure 1-42.

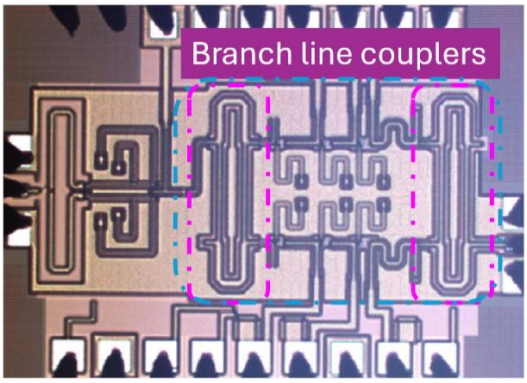


Figure 1-42: Chip microphotography of the balanced PA from [19] (highlighted in blue), with the branch-line couplers highlighted in pink.

The authors were able to reduce its horizontal size to 150 µm; however, the vertical dimension remains large, resulting in a significant footprint for this device. One of the main advantages of this topology is that it is not limited by any technology minimum design rules constraints since the strip lines are wide enough for a 50 Ω matched device, and no minimum spacing constraints apply.

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Another work reports a novel Interstage Matching Network (ISMN) for a multi-stage power amplifier using 60 nm GaN-on-silicon technology in the W-band based on microstrip coupled lines (MCL) [26]. Figure 1-43 shows the simplified schematic of the W-band multi-stage PA featuring the ISMN of interest.

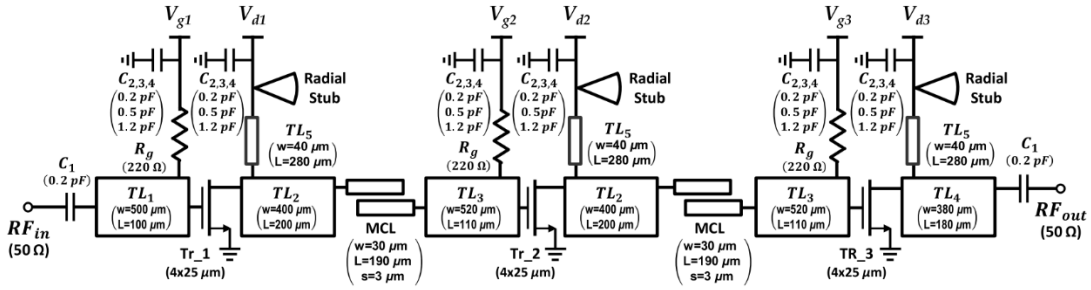


Figure 1-43: Simplified schematic of the W-band multistage PA with the ISMNs based on coupled line couplers from [26].

This approach appears perfectly suitable for the D-band, as it is important to recall that multi-stage PAs are mandatory to achieve sufficient gain. Additionally, the goal of operating at such high frequencies is to achieve wide bandwidth, which is generally limited by passive components, particularly those used in matching networks, and more specifically interstage matching. According to our review of PAs, most of the designs use microstrip lines and capacitors for matching. When different approaches are employed, they generally operate in differential mode, allowing the use of impedance transformers such as baluns.

In contrast, the authors propose a method that seems to work for both single-ended and differential modes, based on coupled line couplers what allows to get rid of the interstage capacitance used to isolate DC in between stages and that suffers from hight losses due to their poor quality factor at higher frequency . The matching network is designed as a two-pole conjugate impedance network to achieve wide bandwidth. This is realized using very low characteristic impedance microstrip lines and optimized coupled lines. Figure 1-44 shows the matching network used by the authors.

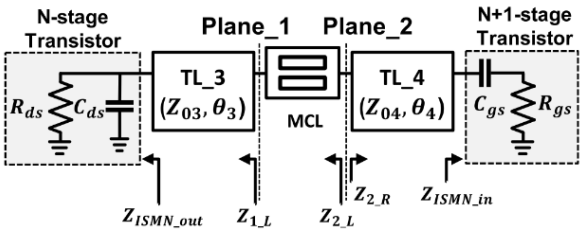


Figure 1-44: Schematic of the ISMN using MCL, from [26].

Coupled lines enable a strong resonance at the desired frequency, allowing for optimal conjugate matching at both ends and at an intermediate frequency simultaneously. To demonstrate the advantage of this approach, the authors compared the response of this type of matching network with that of a simple cascaded matching network consisting of transmission line, capacitor, transmission line, whose schematic is shown in Figure 1-45.

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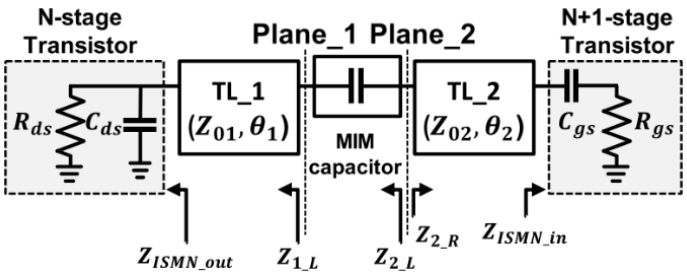


Figure 1-45: Schematic of the ISMN using MIM capacitors, from [26].

The frequency response in terms of insertion loss is shown in Figure 1-46.

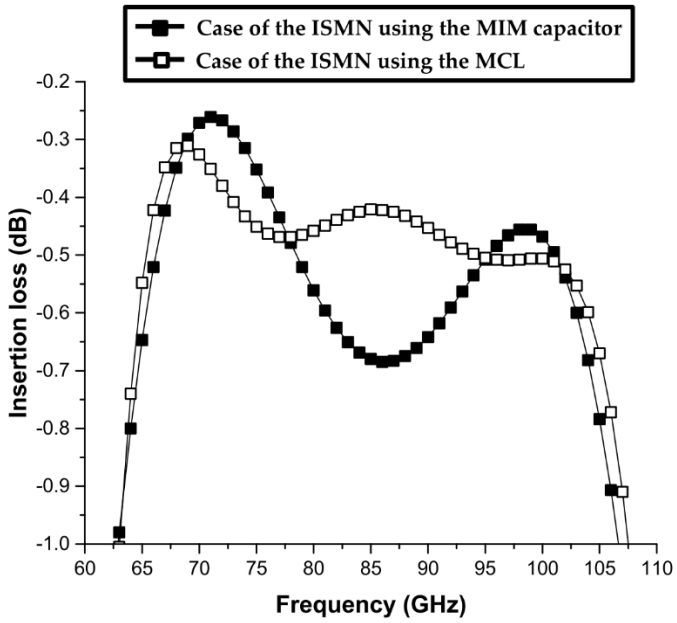


Figure 1-46: Simulated insertion loss of the ISMN frequency response for the case: using MIM capacitance and using MCL, from [26].

The frequency response shows similar behavior in terms of bandwidth and overall shape, but the ISMN based on coupled line couplers exhibits a flatter frequency response with lower insertion loss compared to the one using MIM capacitors. Additionally, coupled line couplers have a very small footprint, especially at high frequencies, as shown in the photograph of the fabricated W-band PA proposed by the authors, shown in Figure 1-47, where the MCL are highlighted in red.

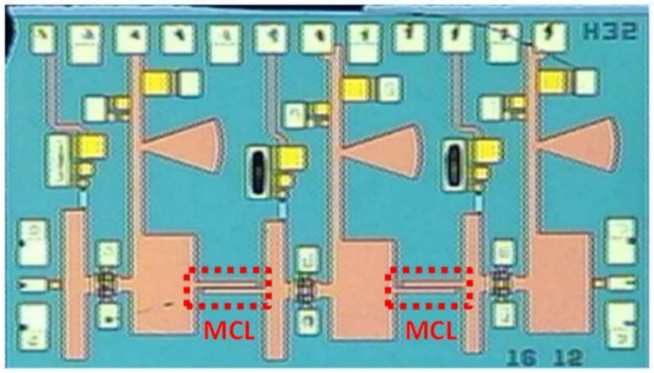


Figure 1-47: Photography of the fabricated W-band PA proposed in [26].

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This demonstrates a strong potential in using couplers in high-frequency PA design, presenting a novel application of couplers, but also highlighting another type of coupler, which is the coupled line coupler. A further comparison between the two topologies of couplers is presented in subsection 2.2.2. Given the multiple applications and clear advantages of using couplers in the D-band, it appears very promising to investigate their use specifically for PA design and more generally for enabling D-band FEM modules.

1.1.4.2 Splitter/ Combiner

As mentioned above, to address parallelized topologies that improve output power, it is essential that the components used for power splitting and combining exhibit good performance. The idea is therefore to review the state of the art regarding power dividers and splitters based on transmission lines. [27] reports an 8-way PA, where the authors use a simple power divider and combiner based on quarter-wavelength microstrip lines followed by baluns, as shown in the schematic view of the D-band PA in Figure 1-48.

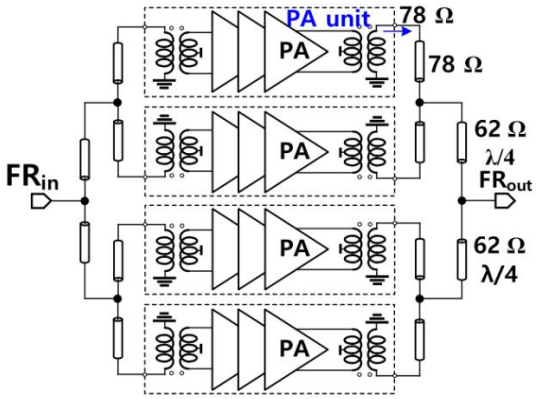


Figure 1-48: Schematic of the proposed D-band PA from [27].

The power splitter and combiner used are the simplest possible, with the design approach relying on quarter-wavelength microstrip lines and considering impedance transformations by varying the characteristic impedance of the microstrip lines. For example, at the output, the authors aim to match 78 Ω to 50 Ω. The first microstrip line section is therefore designed for 78 Ω, and the second for 62 Ω. Although not explicitly explained by the authors, the characteristic impedance of the second microstrip line (62 Ω) is calculated simply as follows:

$$Z_{c2} = \sqrt{Z_{c1} \cdot Z_0} = \sqrt{78 \cdot 50} = 62.4\,\Omega$$

The advantage of this approach lies in the simplicity of analytical calculation and design, as it uses only quarter-wavelength microstrip lines with specific impedances. These values are generally provided in foundry design kits, and even if not, it is straightforward to construct a microstrip line chart giving the characteristic impedance versus signal strip width. This makes the design of this kind of combiner topology relatively quick and easy across different technologies, as there appear to be no fundamental limitations at first glance. However, one can note a limitation in the minimum and maximum characteristic impedances achievable with microstrip lines, which in turn restricts the impedance range that can be matched by the component.

Nevertheless, this approach has several drawbacks. It does not guarantee good isolation or output-matching performance, since no resistive or lossy elements are used for these functions. Moreover, a direct 1-to-4 power combiner or divider is not feasible because of impedance constraints: the required characteristic impedance of the transmission lines would be too high to implement. A more realistic solution, as proposed by the authors, is to cascade two dividers using quarter-wavelength

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microstrip lines, which increases the overall losses. As a result, the final component exhibits a relatively high insertion loss of about 1.6 dB. Additionally, it consumes a large area, as can be seen in the chip photography shown in Figure 1-49.

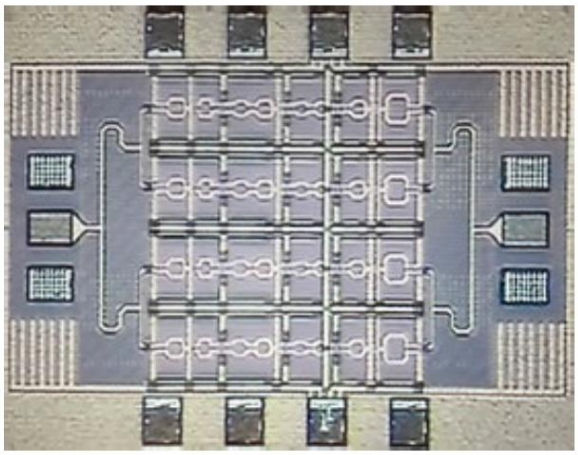


Figure 1-49: Chip photography of the parallelized PA from [27].

To summarize, this approach is very simple to implement but is too bulky in terms of footprint and exhibits mediocre RF performance in terms of isolation and output matching, combined with high losses.

Another work reports a power divider/combiner based on the Wilkinson power splitter [28]. Unlike the previous device, it includes a resistor that ensures isolation and output matching. Figure 1-50shows a view of a 2-way Wilkinson power divider/combiner.

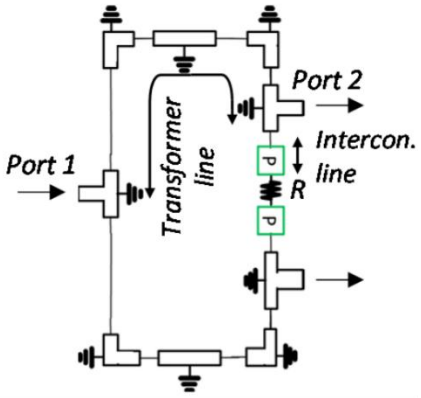


Figure 1-50: 2-way Wilkinson power divider/combiner, from [28].

The authors aim to implement a 4-way power combiner/splitter matched to 50 Ω at all ports. However, due to fabrication limitations of the 28 nm CMOS BEOL technology, specifically the minimum strip width, it is not possible to design a direct Wilkinson 1-to-4 splitter because it would require 100 Ω [28] characteristic impedance microstrip lines. To overcome this, the authors use a 2-way Wilkinson power splitter followed by two identical 2-way power splitters at the output of each branch of the first splitter. This configuration is referred to as a cascaded Wilkinson power divider, as shown in the layout view in Figure 1-51.

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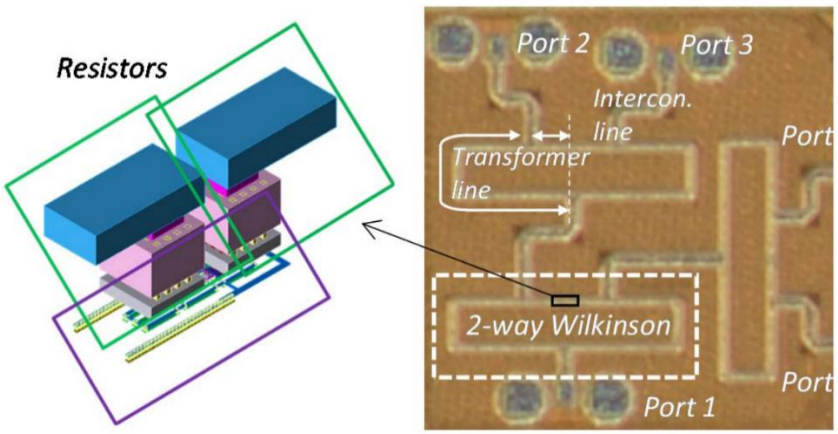


Figure 1-51: Left: resistors layout (purple rectangle) and 3D view of the interconnection with microstrip lines (green rectangle).Right: fabricated 4-ways, from [28].

The authors highlight the design challenges related to parasitic effects in interconnections. Therefore, a full EM simulation of these interconnections was performed, as shown in Figure 1-51 on the left. These interconnections are connected to a bank of dummy resistors to improve the accuracy of the used resistance. After this, fine tuning was carried out in several steps to achieve a final result, which was measured in a two-port configuration by shorting the three unused ports. This method is not the most accurate, as it depends on the accuracy of the 50-Ω shunt resistors employed. Secondly, it does not allow the measurement of all isolation parameters between the output ports, so a real challenge remains for multi-port device measurements in general, and especially at high frequencies.

Moreover, the overall area occupied by this device is quite large. It can be observed from Figure 1-51 that two quarter-wavelength micrsotrip lines are cascaded (each corresponding to a 2-way power splitter), as well as access lines at the input and output, and between the two 2-way power splitter/combiner. This results in a large footprint and, more importantly, significant losses.

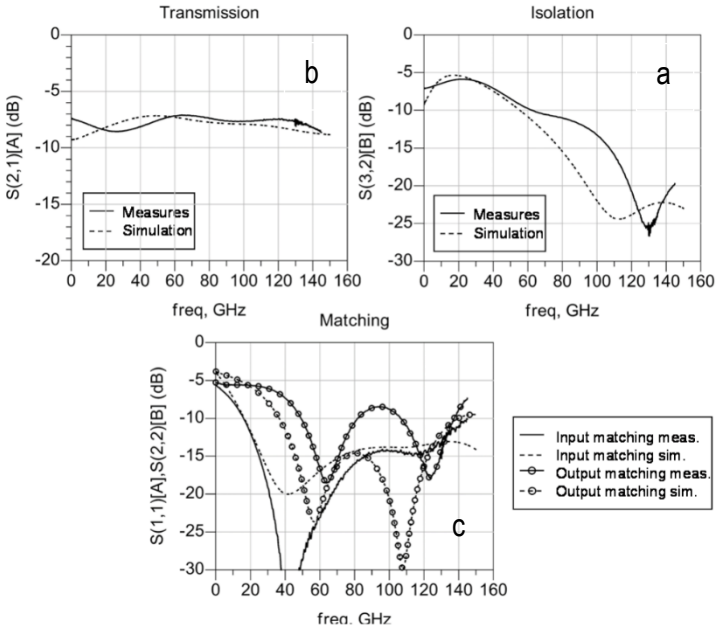


Figure 1-52: EM simulation result vs measurement. Top left: insertion loss. Top Right: Output Isolation. Bottom: Input and output matching, from [28].

Indeed, the loss results are clearly visible in Figure 1-52 b, which shows insertion loss of approximately 2.5 dB. The Figure 1-52 a shows isolation, which is shifted at high frequency but remains very good (better than 20 dB). However, it should be noted that the authors only present one isolation

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parameter. Finally, the Figure 1-52 c shows the input return loss, which is relatively centered at low frequency but remains below 10 dB across the entire band. The output return loss is poorer, suffering from a dip in the middle of the band, making the device less effective as a combiner, with a return loss of around 8 dB at 95 GHz. Overall, the performance of this device is significantly better than that of the power divider without resistors, due to better isolation and output matching. However, a major drawback remains the insertion loss and size of the device, similar to the first case without resistors. Additionally, there is a difficulty related to the rooting of isolation resistors and parasitic effects from the access ports. To summarize, Wilkinson-based power combiners and dividers offer much better output performance, making them good candidates for use as combiners. For divider operation, the two topologies are comparable, as only input matching and insertion loss matter in that mode.

Finally, we report an innovative and interesting topology from an article that we reviewed in the PA state-of-the-art section, specifically regarding parallelized PAs [23]. This time, we focus on dissecting this design by concentrating on the passive components that enabled the authors to achieve state-of-the-art performance. Recall that Figure 1-53 shows the block diagram of the four-way combined PA. At the input, there is a simple T-junction divider, similar to the first case, and at the output, the device of interest highlighted in red, which the authors calls the 4-way coupled line Wilkinson combiner.

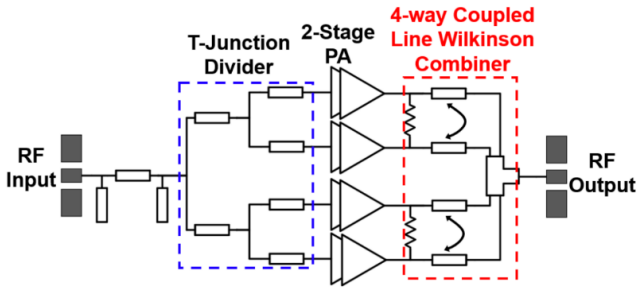


Figure 1-53: Block diagram of the proposed four-way combined PA with a T-junction power splitter at the input and a 4-way coupled line Wilkinson combiner at the output, from [23].

According to the authors, it is a Wilkinson combiner based on coupled lines, implemented as two two-way coupled line Wilkinsons combined with a simple T-junction to combine the power. The shunt capacitance of the T-junction is absorbed into the design of the coupled line combiner to reduce its electrical length to 60°, so the overall circuit length is approximately 60°, primarily composed of the coupler. This results in a 4-way power combiner with a sub-$\lambda/4$ electrical length, compared to about $\lambda/2$ for the 4:1 combiners using two Wilkinson stages. Figure 1-54 shows a photograph of the fabricated cell that demonstrates how area-efficient the coupled line Wilkinson combiner (highlighted in red) is compared to traditional T-junction power divider (highlighted in blue).

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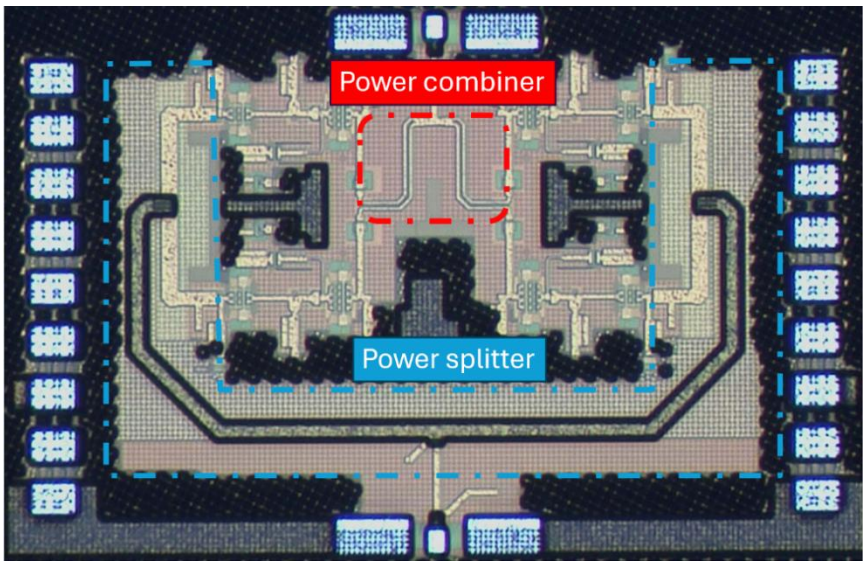


Figure 1-54: Die photograph of the fabricated D-band PA, from [23]. The die area is 1.64 × 1.04 mm2, including pads.

Figure 1-55 shows the top view layout of the combiner on the right side while showing simulated S-parameters (insertion loss and isolation) of the device on the left side.

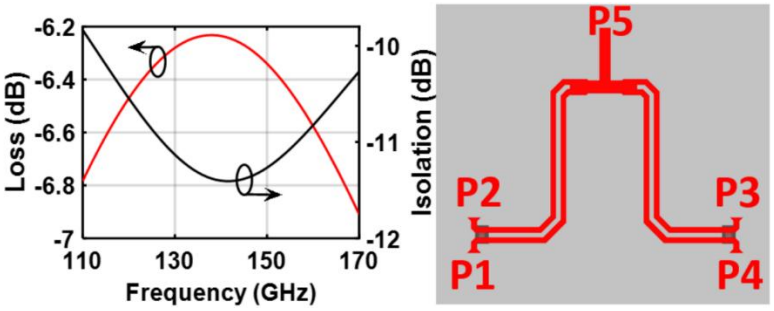


Figure 1-55: EM-simulated results and top-down view of the four-way coupled line Wilkinson power combiner, from [23].

From EM simulation results, we observe a very low additional insertion loss of approximately 0.2 dB at the center frequency, which is excellent compared to the other two cases where insertion loss ranged from 1.6 to 2.5 dB, which represents a significant improvement. This improvement is primarily due to the reduced device length, as mentioned earlier, with a sub-$\lambda/4$ electrical length compared to about $\lambda/2$ for competing designs. However, this alone does not fully explain the substantial reduction in losses.

According to the authors, the coupled line topology offers important advantages over conventional Wilkinson combiners in terms of insertion loss and impedance transformation. In this topology, if the combination occurs in phase, the matching is achieved by considering only the even mode characteristic impedance (see Section 2.2.3) of the coupled lines. Compared to classic microstrip lines, coupled lines provide an additional design parameter, the coupling coefficient. This allows designers to reduce device losses by increasing the width of the signal strips while decreasing the coupling factor to maintain the same impedance transformation. Conversely, for transformations to higher impedances, the coupling coefficient is increased by reducing the spacing between the coupled strips. Overall, for the same impedance transformation ratio, the width of the microstrip lines can be increased while preserving the matching behavior.

Additionally, in conventional Wilkinson combiners, coupling between signal strips and rooting to isolation resistors poses several challenges. In contrast, this device absorbs these effects into the design process and incorporates them into the coupling topology, further reducing the device width. Unfortunately, the freedom provided by the even mode analysis and the coupled line topology is not thoroughly explained, and no equations are provided to describe the device behavior.

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EM simulations also show an isolation of about 11 dB, which may be acceptable for some applications but is generally insufficient. Moreover, only one isolation parameter is presented, whereas a 4-way power splitter has multiple isolation paths to consider. No information is provided regarding the output return loss. Therefore, there remains significant room for improvement in the design methodology, theoretical explanation, and performance optimization of this device, which we find very promising in terms of size and loss reduction versus traditional T-junction or classical Wilkinson power combiner/divider.

Table 1-4 summarizes the key points of the three power combiner topologies presented above using qualitative indicators. No numerical values are included in this table since the authors used different technologies and operated at different frequencies.

	T-junction	Cascaded Wilkinson	Coupled lines based
Area	− −	− −	+ +
Insertion losses	− −	− −	+ +
Isolation	− −	+ +	±
Output return loss	− −	+ +	−
Design flow ⇔ theorical equations	+ +	+	− −

Table 1-4: Comparative table of the three power combiners topologies cited earlier in this sub-section in terms of area, IL, isolation, output RL and presence of design flow and theorical equation

From Table 1-4, we can see that the T-junction power combiner lags significantly behind the other two topologies in terms of output isolation and return loss. Its main advantage lies in ease of design, but it still remains a viable candidate for power splitting. The cascaded Wilkinson power combiner remains a poor solution in terms of footprint efficiency and insertion loss because, like the T-junction, it suffers from cascading at least two quarter-wavelength transmission lines, in addition to access and interconnection lines. This directly increases losses, as the losses of distributed components are calculated per unit length. Moreover, area increases not only in length but also in width, since the transmission lines composing these two devices must maintain a minimum distance to avoid parasitic coupling effects that degrade circuit performance. The key difference introduced by Wilkinson is the addition of an isolation resistor, which improves isolation and output return loss. Furthermore, the presence of theoretical equations and a well-defined design flow make the Wilkinson design easier to understand and implement, although the design is slightly more challenging due to the inclusion of the resistor and its rooting.

Turning to the third topology, the coupled line based power combiner offers significant advantages in terms of insertion loss and area saving compared to the two other topologies. However, its isolation and return loss performance are moderate: better than the T-junction power divider but inferior to the Wilkinson power combiner. Clearly, there is room for performance improvement regarding performance and modeling. Additionally, no detailed theoretical explanations, design flows, or equations are provided for this topology.

Overall, the coupled line based power combiner appears to be the best option according to the state of the art. However, several issues remain to be addressed, such as improving isolation and output

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return loss, as well as developing theoretical models and a complete design methodology. This reinforces the idea that innovation and improvement of existing functions are still possible in the D-band, making it a very interesting area for further research and development.

1.2 Syntheses of the state of art and research opportunities

As a reminder, the context is the constant increase in data traffic and data rates that need to be addressed in an energy efficient way. Focusing on backhauling applications, more precisely on wireless backhauling based on very high data rate for small distances P2P communication. A way to address this need is to increase operating frequency. This is made possible by the ongoing advancements in integrated technologies regarding f_T and f_{max} that are highly increasing. Using high mmWave frequencies naturally leads to an increase in the bandwidth of front-end module components, resulting in a targeted increase in data rates. There are also some additional benefits such as the reduction of passive components footprint and the possibility to integrate increasingly efficient antennas such as massive MIMO antennas. Given all the arguments mentioned above, the D-band frequency range was naturally selected as very promising for front end modules design.

That said, numerous challenges remain to be addressed, one of the most significant being the propagation losses in the air, which increase with the square of the frequency. Coupled with the fact that these technologies have f_T/f_{max} values barely sufficient to start generating gain at the desired frequency, this results in a transmission challenge that must be tackled on both the transmitter and receiver sides. Within the scope of this thesis, we focus on the TX side, where the key component limiting or enabling the integration of functional FEMs at this frequency is the PA. In PA design, several challenges must be addressed, such as the impact of parasitic in the transistor interconnections that degrade the performance, in addition to the skin effect that increases losses and consequently also reduces performance. Technological modifications that enable high f_T/f_{max} also negatively impact the breakdown voltage of high-speed transistors by reducing it, thereby limiting their power generation capability and efficiency.

Several PA design strategies have been implemented; however, clear similarities emerge in the state of the art. To address the low gain of transistors at these frequencies, most designs use multiple stages to achieve the desired gain. Moreover, to overcome the difficulty of generating sufficient power, multi-path architectures are widely explored, with the majority employing differential or balanced topologies. Others propose an alternative approach based on parallelization. Regarding amplification topologies, an overwhelming majority use the cascode, which offers a good tradeoff between output voltage swing and gain. However, some works stand out, such as the common-base topology, which offers numerous advantages including the power swing exploited also by cascodes, since the second transistor in a cascode is a common-base device. Additionally, the common-base topology exhibits excellent linearity, resulting in a sharp compression profile where the 1-dB compression point is very close to P_{sat}. Furthermore, the current supply adapts to the output power via current clamping, significantly improving efficiency and thus the PA's PAE.

Among the best performance observed is that of the cascaded common-base PA followed by the 4-way parallelized PA, both strategies and topologies that are not extensively explored in the state of the art. There is a clear interest in investigating these two approaches, especially since, to the best of our knowledge, no one has yet combined them. This represents a great research opportunity that we intend to seize.

To summarize, we envision developing a multi-stage parallelized PA. However, as highlighted in our state-of-the-art study, the largest contributions to losses and occupied area come from passive

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components. Moreover, most technologies do not offer distributed passive components for the D-band, making it necessary to conduct preliminary studies and enable basic passive building blocks for this band. It also seems highly relevant to improve power divider and combiner topologies based on the coupled line version, which demonstrates significantly lower losses and footprint compared to more classical power combiners. Furthermore, multi-stage designs require interstage matching networks, which, as previously observed, are mostly implemented using simple microstrip lines and capacitors. We have also seen a broadband and more area-efficient approach based on coupled lines. Therefore, studying couplers is particularly interesting, especially to address matching networks in our case and potentially to enable these components for people working on balanced PAs, for example. In this context, there is a significant opportunity for the development and enablement of passive components dedicated to the D-band, such as matching networks, couplers, power dividers/combiners, and baluns.

1.3 Thesis objectives

According to the study and synthesis of the state of the art, several challenges have been identified and must be addressed. This creates promising opportunities:

- On the active side, particularly with the study of parallelized topologies based on the common-base configuration, a topology that is currently underexploited but appears to offer many advantages.

- On the passive side, even greater opportunities exist due to more design freedom and the potential to propose new innovative topologies or improve existing ones.

- Regarding matching networks, further work is needed, for example by exploring approaches based on coupled lines.

- For other building blocks, there is a niche for enabling passive components such as power splitters/combiners based on coupled lines, improving their performance and conducting in-depth theoretical studies and other building blocks.

Based on this summary of opportunities, have focused this PhD work on the D-band frequency range. The chosen technology is one of the world's highest-speed SiGe BiCMOS technologies, the B55X from STMicroelectronics. At the beginning of the PhD, the technology was still under development, which led to frequent model updates to represent the silicon more and more accurately. We propose to challenge this technology by extracting its best potential in D-band without setting fixed specifications due to this technology updates, but with an understanding of the state-of-the-art performance benchmarks. Our priorities has been to achieve a PA with a high P_{1dB}, wide bandwidth, and good PAE. To this end, we have worked on a multi-stage PA design with a cascode input stage for gain and isolation, followed by one or more common-base stages. These will then be parallelized to try to reach or exceed state-of-the-art output power performance. Before reaching this stage, a preliminary study of the passive components has been conducted, starting with mastering simulators to enable the design of complex and innovative passive circuits.

The manuscript is organized as follows: the second chapter addresses passive components, beginning with couplers. We briefly review their applications, then compare the two most used couplers in the state of the art, the branch-line coupler versus the coupled line coupler. This is followed by a theoretical study based on even- and odd mode decomposition, and concluded with a section detailing the design flow, including embedded design, simulation, and measurement focused on the coupled line coupler that has been widely used during the thesis. Next, focus on the second component of interest: power dividers/combiners. We concentrate on 1-to-N power dividers and combiners, exploring different possibilities before focusing on the coupled line based topology. We then improve this topology and

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propose a comprehensive theoretical study, detailing equations that relate the electrical parameters of the microstrip lines and couplers to the expected S-parameter matrix. Building on this experience, we propose a design flow for this component, concluding with several versions of the power divider/combiner we have developed, accompanied by simulation and measurement results. These measurements have been performed on four-port devices up to 220 GHz. We also address the challenge of measuring a five-port device using a four-port Vector Network Analyzer (VNA).

These enablers provide a solid foundation for PA design, which is treated in the third chapter. This chapter first addresses transistor sizing based on foundry guidelines and geometry selection through a comparative study of different layout geometries proposed by the foundry. This is followed by a PA design flow section detailing our strategy. Since the last stage is the most critical, we begin with the study of the common-base topology for the design of a single power stage. Next, the following subsection treats the study of the cascode topology, which provides significantly higher gain than the other two competitors. We thus use this stage as a driver and the first stage of our PA. Once these two building blocks are combined, we assemble our first two-stage PA to be fabricated on silicon, which is the subject of the next subsection. Based on the challenges encountered and the state-of-the-art study, we see opportunities for improvement by optimising the matching networks. Therefore, the following subsection addresses matching networks in general and possible enhancements. Next comes a second version of the two-stage PA (cascode and common-base), this time eliminating the lossy and unsuitable coupling capacitors for high frequencies, replacing them with innovative matching networks based on couplers that we revisit and adapt to our needs. This version was measured on wafer, and a simulation-to-measurement comparison is presented. We finish this chapter with the three-stage PA, including sizing and design of the last stage, as well as the development of the necessary matching networks for its proper operation.

In a last chapter of advanced realizations for PA design, we present other basic building blocks we have enabled during the thesis but have not used in the PA. This includes 3D couplers capable of achieving impedances unattainable by conventional microstrip coupled line couplers, followed by the design and measurement of an innovative D-band balun based on coupled microstrip lines. We also present a new 3D power divider version. The chapter concludes with the assembly and simulation of the parallelized PA.

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2. Passives devices enablement

2.1 Introduction

As discussed in the state-of-the-art chapter, the critical importance of distributed passive components at high frequencies and the growing interest in them are evident. However, for the B55X technology, only microstrip lines are offered in the Design Kit (DK). Additionally, the EM deck and simulator accuracy are only validated up to 110 GHz. This necessitates a comprehensive preliminary study as part of my thesis and for any design in the D-band, while also highlighting the significant need to provide fundamental passive building blocks; some of which were utilized by myself and others offered to the community. Within this context, this chapter first presents part of the studies conducted on couplers, which are considered a highly important and versatile basic building block, before discussing power dividers in the context of parallelization.

2.2 Directional Couplers

Directional couplers are 4-ports devices that allow waves to flow from certain port(s) to other(s) with a certain power ratio and phase difference. Depending on how it's rooted and designed we can categorize different types of couplers and address different applications.

One first way to define a coupler is to talk about directivity. A directive coupler is a device that is recognizable by the presence of an isolated port, which means a null power transmission to this port. In this case with one input, the total amount of power flows through the two non-isolated ports.

A specific case of directional couplers widely used in the state of the art is the 3-dB coupler, which is discussed in a forthcoming subchapter. In this configuration, the power is equally divided between the two outputs, typically with a 90° phase difference. There are two main families widely used: coupled line and branch line.

2.2.1 Applications

Couplers are key components in mmWave systems, particularly in the D-band, offering low losses, wide bandwidth, and compact size with relatively simple design. They are ideal candidates for high-frequency building blocks. Despite these advantages, at the start of my thesis, there was limited research highlighting the benefits of couplers at these frequencies. Furthermore, the technology design kit did not include any coupler, leaving the entire design process to be developed from scratch.

As discussed in SOA chapter, many functions need to be addressed in order to integrate a fully functional front-end module. Among the targeted applications are Baluns in divider topology [29] [12] [7] [30] [31] and Marchand topology [32], which are essential components for the design of differential circuits. Impedance matching networks and DC blocks are also commonly used in the design of most active RF circuits. Filtering functions are similarly important. In the context of backhauling and point-to-point communications, there is a need for phase shifters, with the major topologies being Reflective-Type Phase Shifters (RTPS), which are generally based on coupled lines [33], as well as active phase shifters that perform vector modulation and therefore require I/Q modulators. This application is mainly addressed using Lange coupler based on coupled lines coupler as in [34] or in [35]. Coupled lines are also employed in the design of power dividers/combiners as in [23] and in [36]. We can find also balanced power amplifiers based on couplers.

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Given the promising potential of couplers, we decided to conduct an in-depth study of this component. Part of this work was applied in the PA chapter, specifically the power divider and matching network. Also, some of these devices are already employed in circuits developed by third parties within the SHIFT project [37], for example.

2.2.2 Coupled line coupler vs branch line coupler

Quadrature 3-dB couplers can be divided into two main topologies, branch line coupler and coupled line coupler.

The branch line coupler consists of four quarter wavelength transmission lines, connected in a square configuration. For a branch-line coupler with numbered ports as illustrated in Figure 2-1 and considered ideal, the input is designated as port 1. The power is equally divided between ports 2 and 3, with a power ratio of -3 dB at each port and a phase difference of 90°. The corresponding S-parameter matrix is defined as follows:

$$[S] = \frac{-1}{\sqrt{2}}\begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix}$$

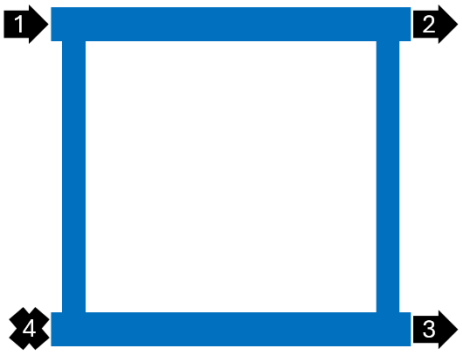


Figure 2-1: Simplified schematic of a branch line coupler with numerated input, output and isolated ports.



Figure 2-2: Simplified schematic of a coupled line coupler with numerated input, output and isolated ports.

Regarding the coupled line coupler, it consists of two conductors' strips that are not physically connected but are coupled electromagnetically. The coupler is shown in Figure 2-2. As with the branch line coupler, the power is equally divided between ports 2 and 3, with a phase difference of 90°.

To illustrate the performance differences between the two topologies, we simulate them at $f_0 = 150\ GHz$ using ideal transmission lines. Figure 2-3 shows the S-parameters for transmission to the thru (S_{21}), coupled (S_{31}), and isolated ports, as well as the input port matching. Figure 2-4 displays the phase difference between the thru and coupled ports. Similarly, Figure 2-5 and Figure 2-6 present the corresponding parameters for the coupled line coupler.

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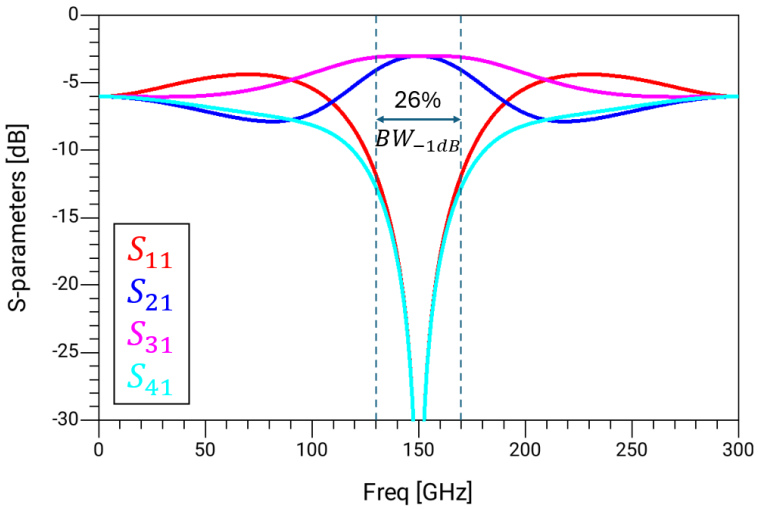


Figure 2-3: S-parameters simulation result of a branch line coupler with ideal transmission lines showing the return loss S_{11}, the isolation S_{41}, the insertion loss S_{21} and S_{31}while illustrating the BW_{-1dB} defined while the difference between the thru and coupled ports transmission is lower than $1\ dB$.

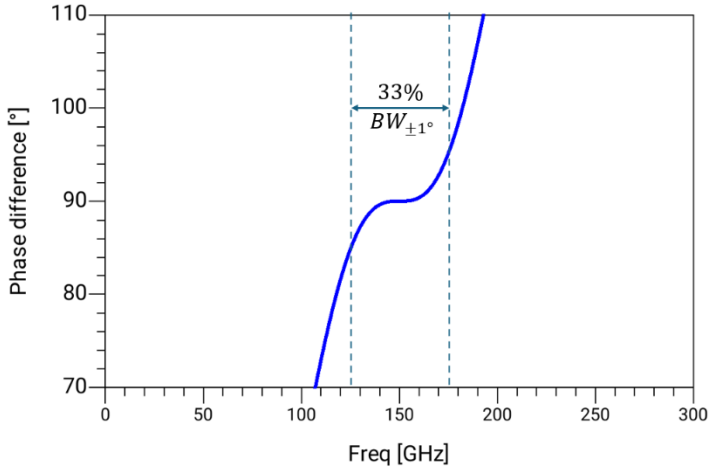


Figure 2-4: S-parameters simulation result of a branch line coupler with ideal transmission lines showing the difference of phase in degrees (°) between the the thru and coupled ports S_{21} and S_{31}, while illustration the $BW_{\pm5°}$ defined when the difference of phase varies within plus or minus 5° from 90°.

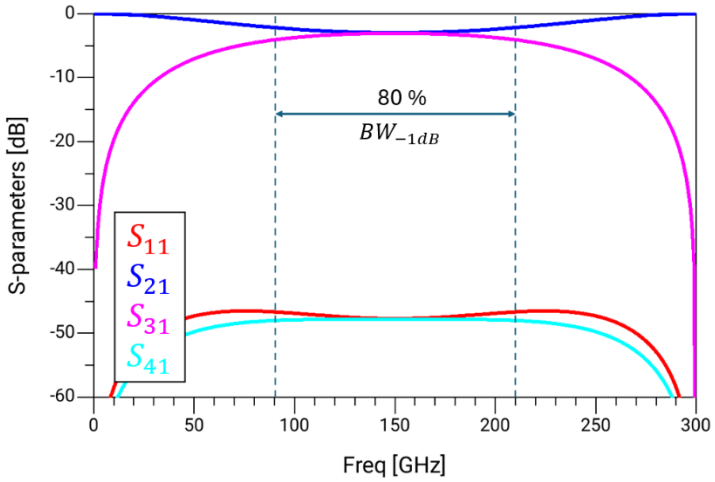


Figure 2-5: S-parameters simulation result of a coupled line coupler with ideal transmission lines showing the matching S_{11}, the isolation S_{41}, the insertion loss of the thru port S_{21} and to the coupled port S_{31} while illustrating the BW_{-1dB} defined while the difference between the thru and coupled ports transmission is lower than $1\ dB$.

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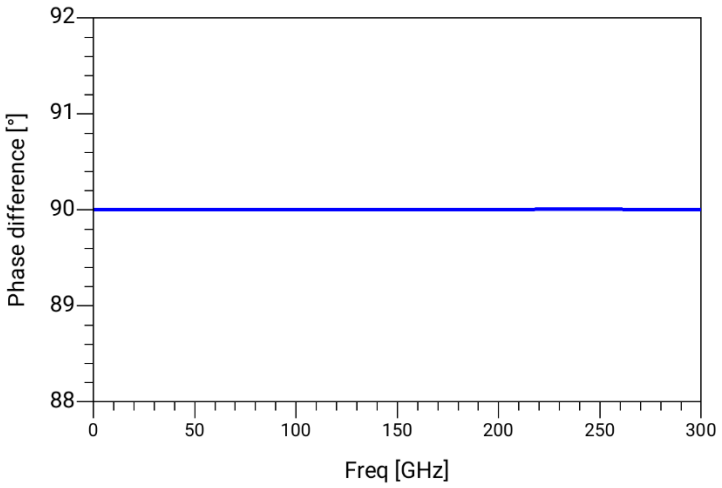


Figure 2-6: S-parameters simulation result of a branch line coupler with ideal lines showing the difference of phase in degrees (°) between the thru and coupled ports transmission S_{21} and S_{31}.

The summarize of the comparison between the two couplers topologies in given in Table 2-1.

	Branch line coupler	Coupled line coupler
BW_{-1dB}	26%	80%
$BW_{\pm 5}°$	33%	∞
$Area$ @ 150 GHz (mm^2)	$\frac{\lambda_G^2}{16} = \frac{\lambda_G}{4} \cdot \frac{\lambda_G}{4} = 0.07$	$\frac{\lambda_G}{4} \cdot (2 \cdot W + G_{ap}) = 0.0013$
Realization	No specific needs	Small gap between the coupled strips

Table 2-1: Comparison table between branch line and coupled line couplers based on various figures of merit (bandwidths $BW_{\pm 5°}$ and BW_{-1dB}, footprint and fabrication requirements).

The branch line coupler is widely used in PCB designs due to its ease of design regardless of the technology, as shown in Table 2-1, since it does not have specific requirements regarding fabrication precision. Additionally, another advantage is that the two output ports are oriented on the same side, as illustrated in Figure 2-1, which can greatly simplify some layouts. However, in terms of performance, it is quite limited, exhibiting a narrow 1-dB bandwidth with a narrow ±5° bandwidth, resulting in a relatively narrowband component that is unsuitable for wideband applications. This is compounded by a large area consumption; for example, at 150 GHz and considering a B55X technology from STMicroelectronics, the device occupies approximately $0.07\ mm^2$. The footprint of the device can be shrunk by meandering to reduce with a factor of 60% the total occupied area as shown in [38], but the area remains relatively large. Other methods can be used as capacitive loading techniques as in [39] to perform as best a factor of 50% of area reduction. Other methods exist based on the use of lumped elements. But this is not an option at high frequency, due to the low quality factor of lumped components in D-band, on particular MOM capacitors.

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In comparison, the coupled line coupler has a very small footprint area of only $0.0013\ mm^2$, making it way smaller than the branch-line coupler. Additionally, it features a theoretically infinite ±5° bandwidth, coupled with a 1-dB bandwidth of 80%, compared to the branch-line's 33% and 26%, respectively. However, one limitation makes the realization of this component very challenging or even impossible on certain technologies: the gap between the coupled strips. Depending on the substrate thickness and effective permittivity $\varepsilon_{r_{eff}}$, this gap can be as small as a few microns. Considering integrated technologies, however, sufficient fabrication precision and etching capabilities exist to realize such small gaps with sufficient accuracy. Hence, given these advantages in terms of drastic footprint reduction and wide bandwidth, combined with the fact that these fabrication constraints can be addressed in silicon technology, the coupled line coupler is the ideal candidate for integrated circuit design and for implementing passive high frequency functions on the B55X technology. Our choice has logically focused on coupled line couplers, and we exclusively discuss this type of coupler in the remainder of the manuscript.

2.2.3 Even/Odd mode theory

The coupling in a coupled line is induced by the interaction between the two modes supported by the structure. These modes are defined as even and odd modes, each exhibiting its own distinct field distribution, as illustrated in Figure 2-7 [40].

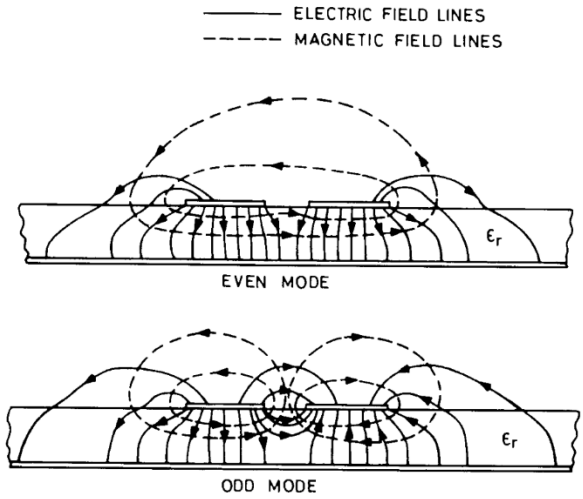


Figure 2-7: Cross-sectional view of a microstrip coupled line coupler showing the electric field distribution (solid lines) and magnetic field distribution (dashed lines) for the two modes: even mode (top) and odd mode (bottom), adapted from [40].

Furthermore, each of the two modes has a proper characteristic impedance, which tends to become equal as the distance between the two microstrip lines increases significantly (resulting in no coupling, i.e., the case of a single microstrip line). The even and odd modes characteristic impedances, Z_o and Z_e, are represented by the characteristic impedance of a single strip to ground when the two strips are excited identically (same source, same voltage), either in phase or out of phase, respectively, as illustrated in Figure 2-8.

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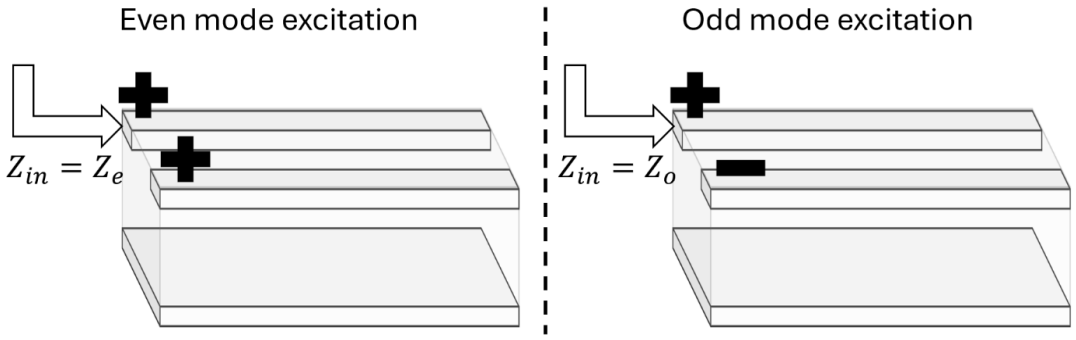


Figure 2-8: Simplified 3D view of a coupled line coupler showing the characteristic impedances (Z_e and Z_o) seen at the input of the coupler for the even and odd modes.

Furthermore, each mode has its own phase velocity, which is identical when designed in a homogeneous substrate. However, this is not the case for microstrip lines, since the dielectric constant above and below the signal strips are not the same.

2.2.4 Design flow for couplers in D-band

Before discussing the design of a passive component, it is important to introduce the BEOL of the technology, which in silicon technology is located at the topmost layers, covering the Front End Of Line (FEOL) and the silicon substrate, as illustrated in Figure 2-9.



Figure 2-9: Silicon technology simplified representation.



Figure 2-10: 7ML BEOL for B55X STMicroelectronics technology representation [25].

Focusing on the BEOL region, it consists of successive layers of metal and dielectric materials, as shown in Figure 2-10. These layers provide a certain degree of design flexibility, both for routing active components and for designing passive circuits. This flexibility requires making a choice that will ultimately determine the quality of the circuits designed during this thesis.

The uppermost BEOL layer was used for the signal strip, as it is the thickest copper layer. Regarding the ground plane, a trade-off must be made between the metal thickness, which should be as thick as possible to reduce electrical losses, and the distance h between the signal strip and the ground, which should be maximized. Knowing that:

$$Z = \sqrt{L/C} \quad ; \quad C \approx \frac{\varepsilon \cdot S}{h}; \quad \text{with: } S = W \cdot l$$

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Increasing the height h reduces the capacitance. To maintain the capacitance value, it is necessary to increase the surface S and consequently the width W. As a result, for the same characteristic impedance value, resistive losses are reduced due to the wider strip width.

Unfortunately, we are limited in height when selecting the ground layer. The farthest one from the top metal are the X layers, but they are very thin and have lower conductivity, resulting in higher losses. Choosing these layers would incur excessive losses, especially considering that the height gain would be negligible compared to the losses caused by the X metal layers. Therefore, our logical choice fell on the intermediate Z layer, which offers a good compromise between height, dielectric thickness, and metallization thickness. Therefore, it offers a better quality factor along with several other advantages that will be discussed later. Hence the microstrip lines are designed on the two layers M7 and M5, as shown in Figure 2-11.

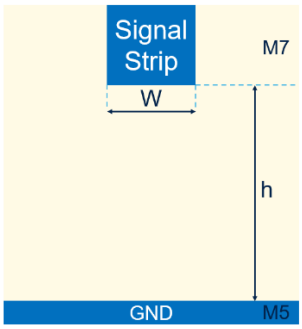


Figure 2-11: Simplified view of a cross section of a µstrip line in 7ML BEOL for B55X STMicroelectronics technology with the selected metals for signal strip and GND plane.

Once the technology part is well defined, for the following subchapter, all metal layers carrying the signal are drawn on M7V and ground is drawn on M5Z. Based on the previous subchapter, the coupler is defined by three parameters: even and odd modes characteristic impedances Z_e, Z_o and its electrical length θ. The methodology I followed for the coupler design is as described below.

Using the ADS tool (citation needed), we start with Ideal Lines library as shown in Figure 2-12.

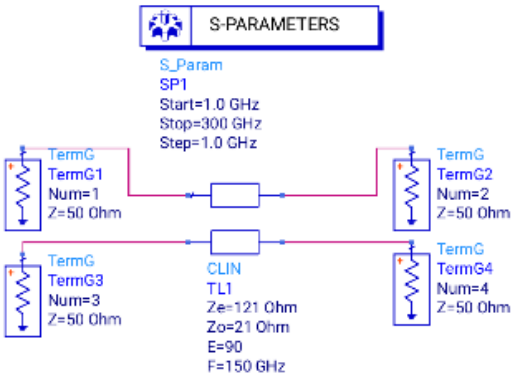


Figure 2-12: SP simulation setup on ADS.

This approach allows verification of simple concepts, such as the response of a 3-dB coupler with a characteristic impedance of $Z_c = 50\ \Omega$, as shown in Figure 2-5 and Figure 2-6 previously.

Next, it is essential to define figures of merit that will allow us to quantify the quality of the component under study. Some of these figures are directly obtained from S-parameters, while others are calculated from equations.

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We consider a backward coupled line coupler, numbered as shown in Figure 2-13.



Figure 2-13: Simplified top view schematic of a coupled line coupler with numbered ports.

Scattering parameters matrix is given by:

$$[S] = \begin{bmatrix} S_{11} & S_{21} & S_{31} & S_{41} \\ S_{21} & S_{11} & S_{41} & S_{31} \\ S_{31} & S_{41} & S_{11} & S_{21} \\ S_{41} & S_{31} & S_{21} & S_{11} \end{bmatrix} \quad \text{2-I}$$

We consider the matrix above as the S-parameter matrix of the coupler shown in Figure 2-13. From this matrix, families of S-parameters can be extracted and grouped according to the figures of merit that they describe. The S_{11} parameters define the impedance matching at port 1, 2, 3 and 4. In decibels, we want these values to be as low as possible. For our devices, an acceptable impedance matching is defined when $S_{11} < -15\ dB$.

Next, S_{21} represents the transmission to the "thru" port, while S_{31} represents the transmission to the "coupled" port. For a 3-dB coupler, as the name suggests, these parameters should be as close as possible to $-3\ dB$ and as identical as possible. A bandwidth criterion can be defined based on these two transmission parameters, for example at ±1 dB. This bandwidth is commonly referred to as BW-1dB. Furthermore, the phase difference between S_{21} and S_{31} should be equal to (or as close as possible to) $90°$.

Finally, S_{41} defines the transmission to the isolated port, or isolation. We want our coupler to be well isolated; therefore, as with matching, these values should be as low as possible. We consider acceptable isolation when $S_{14} < -20\ dB$.

Next, based on the even and odd mode characteristic impedances, the coupler characteristic impedance can be calculated as follows:

$$Z_c = \sqrt{Z_{even} \cdot Z_{odd}} \quad \text{2-II}$$

Finally, the coupling coefficient can be calculated from the even and odd mode characteristic impedances of the coupler as follows. For a quarter-wavelength section of coupled lines in a homogeneous substrate, the coupling coefficient k is given by:

$$k = {Z_{even} - Z_{odd}}/{Z_{even} + Z_{odd}} \quad \text{2-III}$$

From this equation, it is evident that there is a limitation on the maximum coupling coefficient k. To maximize it, the even mode characteristic impedance Z_{even} must be very high, which requires a large height h. However, this height is constrained by the technology, unlike in PCBs where the dielectric thickness can be almost freely chosen. Furthermore, minimizing the odd mode characteristic impedance Z_{odd} requires bringing the strips as close as possible together. In this scenario as well, design rules in integrated technologies impose strict limitations. Moreover, small gaps lead to increased losses due to proximity effects.

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Once the electrical parameters have been identified, several methods are available to determine the corresponding physical parameters. One approach is to rely on analytical equations (see [40] for coupler equations). Alternatively, the Lincalc tool, provided by Advanced Design System [41], can be used to perform these calculations and approximations much more rapidly. Refer to Figure 2-14 for an example of the Lincalc coupler design interface.

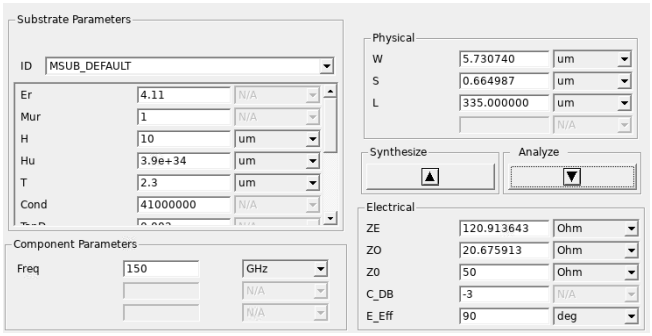


Figure 2-14: Lincalc coupler design interface example.

The window that opens when launching Lincalc is organized into four quadrants as follows: technology inputs at the top left, operating frequency at the bottom left, physical dimensions at the top right, and electrical dimensions at the bottom right. However, our technology is not a single-layer PCB with only one dielectric; instead, it consists of a multilayer dielectric stack. Therefore, we propose to calculate an average value for the relative permittivity ε_r, which will be used at this stage of the flow in the top-right quadrant, where the technology parameters are defined. The output of this step provides physical dimensions (Length l, Width W and Gap G) that will be used in the next subchapter.

2.2.5 Designs and results

This section details the design flow, starting from a basic EM simulation to measurement on wafer. Multiple challenges are described and addressed. This subchapter first treats the layout and EM simulation, then the challenges of its measurement, and finally we compare measurement and simulation results.

2.2.5.1 EM based simulations

Once the three physical dimensions are obtained from the final step of the previous subchapter, we can proceed to design an initial version of the coupler, which will need to be optimized by EM simulations. This step is necessary in most cases because the analytical equations used in Lincalc do not account for all physical phenomena.

After optimization, a coupled line layout is obtained, as shown in Figure 2-15.



Figure 2-15: Layout view of a coupled line coupler centered at 150 GHz on B55x 7ML technology with numbered ports.

The upcoming simulations aim to be compared with differential measurements up to 220 GHz, initially to validate the measurement setup (simulator and EM deck), and subsequently to build confidence

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in our EM base-block simulations. This framework allows us to define the simulator parameters, relying on the expertise of colleagues working on simulations and a working group in which I participated. Among these parameters, the maximum frequency is set to 220 GHz, and meshing is enabled with automatic edge mesh to better account for high-frequency proximity effects. With a similar effect to the skin effect in terms of consequence, this forces electrons to concentrate along the edges of the metal strip, reducing the effective width, which impacts resistance and ultimately the resistive losses.

A. EM simulation results

Electromagnetic simulations performed using Momentum and the EM deck provided by the design kit (DK) yield the S-parameter results for insertion loss, return loss, and isolation, presented in Figure 2-16, along with the phase difference between the coupled port and the thru port, shown in Figure 2-17.

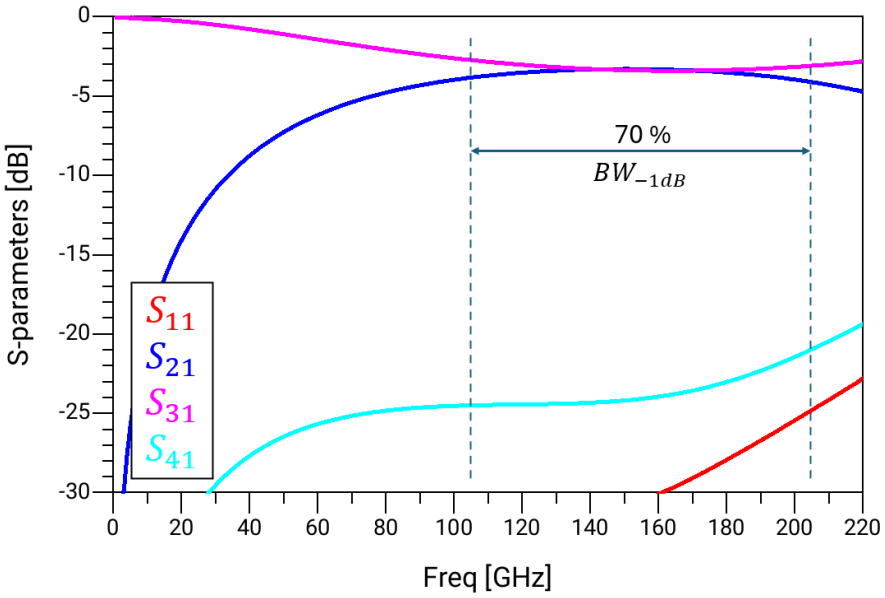


Figure 2-16: EM simulation results of the coupled line coupler showing the S-parameters for transmission to the coupled, thru, and isolated ports, as well as the return loss.

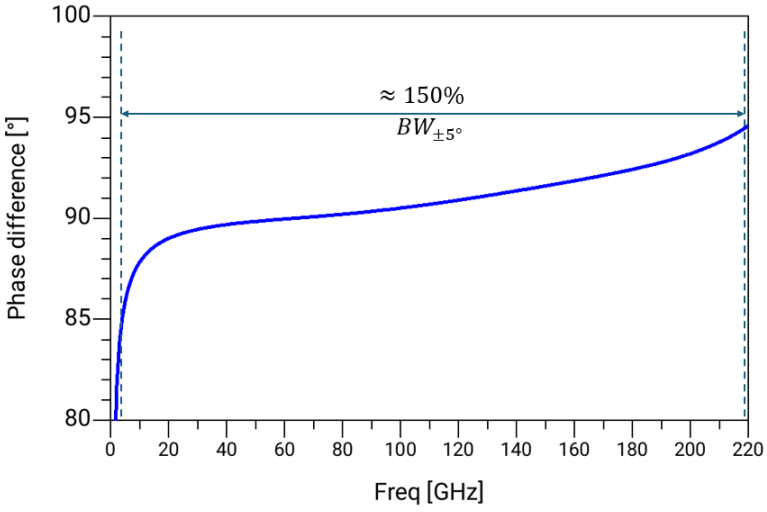


Figure 2-17: Momentum EM simulation results of the coupled line coupler showing the phase difference.

Figure 2-16 shows the S_{41} curve representing the isolation, which remains quite good, better than 20 dB across the entire band, which confirms the directional characteristic of the coupler. However, the isolation is not as ideal as in the perfect case, due to differences in phase velocities and the trade-off

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between phase difference and phase velocity. Regarding transmission to the other two output ports, at the center frequency of 150 GHz, the amplitude difference is approximately 0.07 dB, which is negligible. Therefore, the coupler is considered to perfectly split the power between these two output ports (thru and coupled) with a 3-dB ratio. Losses on these two ports are around 0.35 dB, which is excellent.

Simulations are performed with 50-Ω ports for a coupler designed with a characteristic impedance $Z_c = 50\ \Omega$. This is confirmed by the S_{11} parameter, which remains below -30 dB up to 160 GHz, then slightly increases but stays below -23 dB. This also confirms the wide bandwidth. To further support this, we propose showing the return loss parameter (S_{11}) at all device ports on the Smith chart in Figure 2-18.

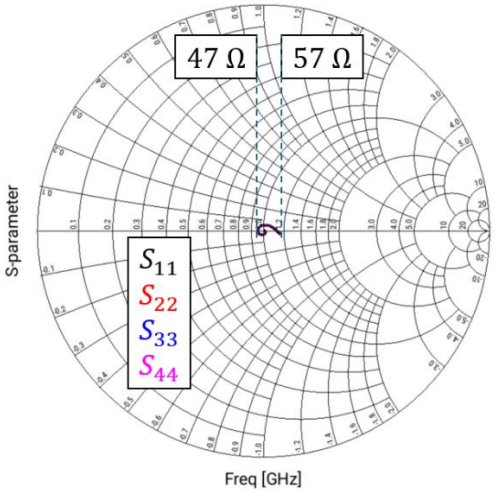


Figure 2-18: Momentum EM simulation results of the coupled line coupler showing the return loss at each of the four ports, which are exactly superimposed showing the perfect symmetry of the device.

As can be seen, the S_{11} curve remains close to the reference impedance, with the furthest point being at $57\ \Omega$. Furthermore, all return loss curves for each device ports overlap, confirming the earlier hypothesis regarding the component's symmetry.

B. Modal even/odd study

We have performed an even and odd mode analysis to verify the characteristic impedances and phase velocities for the coupled line coupler. Two methods are available for this purpose. The first is to feed the coupler with four terminal ports, and then apply some analytical equations to perform the calculation of the desired FOMs (characteristic impedances, coupling coefficient and phase velocity). The second method involves controlling the excitation of the coupler directly in ADS. For each excitation mode a corresponding matrix of SP is obtained, from it the desired FOMs are calculated.

B.1 Method 1: Analytical Calculation Based on a 4-Port S-Parameter Matrix

Based on the EM results, the following equations are directly injected into the ADS ".dds" file.

First step: Calculate the S-parameters of the even and odd modes starting from the 4-port S-matrix of the coupler:

$$S_{11_e} = S_{11} + S_{13} \qquad \text{2-IV}$$

$$S_{12_e} = S_{12} + S_{14} \qquad \text{2-V}$$

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$$S_{11_o} = S_{11} - S_{13} \quad \text{2-VI}$$

$$S_{12_o} = S_{12} - S_{14} \quad \text{2-VII}$$

By exploiting the symmetry:

$$S_{12_e} = S_{21_e} \quad \text{2-VIII}$$

$$S_{11_e} = S_{22_e} \quad \text{2-IX}$$

the two 2-port S-matrices corresponding to the even and odd modes can be reconstructed. Then we convert the two S-matrices of the modes into their corresponding ABCD matrices using the built-in ADS function *StoABCD*. The resulting matrices are as follows:

$$[ABCD_e] = \begin{bmatrix} A_e & B_e \\ C_e & D_e \end{bmatrix} \quad \text{2-X}$$

$$[ABCD_o] = \begin{bmatrix} A_o & B_o \\ C_o & D_o \end{bmatrix} \quad \text{2-XI}$$

The characteristic impedance of the two modes are calculated as follows:

$$Z_e = \sqrt{\frac{B_e}{C_e}} \quad \text{2-XII}$$

$$Z_o = \sqrt{\frac{B_o}{C_o}} \quad \text{2-XIII}$$

Next, the characteristic impedance of the coupler and the coupling coefficient can be calculated.

Finally, the phase velocities can be determined as follows:

$$\varphi_e = \frac{imag\left(arcosh(A_e)\right)}{l} \quad \text{2-XIV}$$

$$\varphi_o = \frac{imag\left(arcosh(A_o)\right)}{l} \quad \text{2-XV}$$

B.2 Methode 2 : Simulation of even and odd modes

In this case, the device is simulated under two different excitation modes as follows.

Even mode excitation:

The coupler is excited with the same terminals in phase, which corresponds to applying the same voltage while dividing the current, as shown in Figure 2-19.

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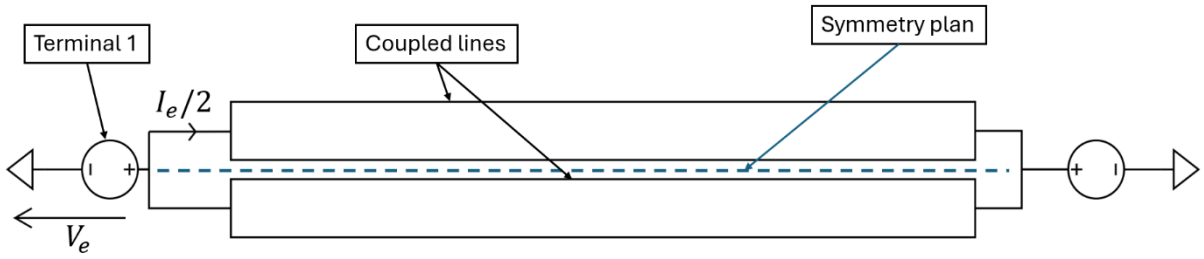


Figure 2-19: Simplified schematic view of a coupled line coupler excited in even mode, showing its axis of symmetry along with the corresponding voltage and current distributions for this mode.

The simulation yields a 2-port S-matrix for the even mode. Calculating the input impedance at terminal 1 (left side) for half the device gives:

$$Z_e = \frac{V_e}{\frac{I_e}{2}} = 2 \cdot \frac{V_e}{I_e} = 2 \cdot Z_{in} \qquad \text{2-XVI}$$

with Z_{in} the input impedance of the two-port device, calculated in ADS.

The even mode S-matrix matrix is then converted into an ABCD matrix, and the even mode characteristic impedance is calculated by multiplying by two:

$$Z_e = 2 \cdot \sqrt{\frac{B_e}{C_e}} \qquad \text{2-XVII}$$

After calculation the result matches that of section B.1.

Finally, to calculate the phase velocity, the same equation used previously is applied, yielding the same result as in section B.1.

Odd mode excitation:

For the odd mode, the coupler is excited with opposite phase signals, as shown in Figure 2-20.

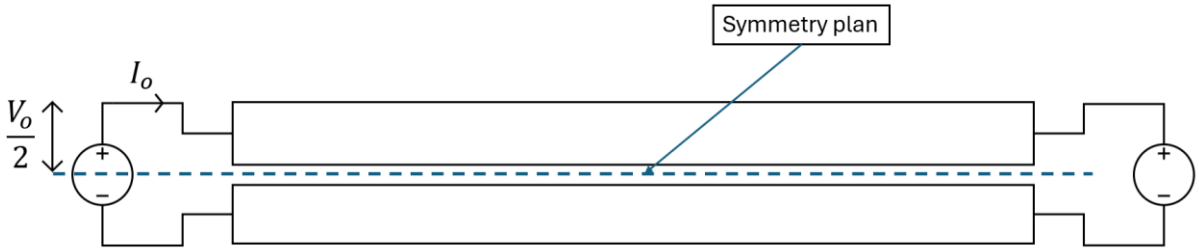


Figure 2-20: Simplified schematic view of a coupled line coupler excited in odd mode, showing its axis of symmetry along with the corresponding voltage and current distributions for this mode.

The simulation yields a 2-port S-matrix for the odd mode. Here, the same current but half the voltage is considered. Calculating the input impedance proceeds then as follows:

$$Z_o = \frac{\frac{V_o}{2}}{I_o} = \frac{V_o}{2 \cdot I_o} = \frac{Z_{in}}{2} \qquad \text{2-XVIII}$$

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Then, the odd mode S-matrix obtained in this subsection is converted into an ABCD matrix. The odd mode characteristic impedance is then calculated by dividing by two:

$$Z_o = \frac{1}{2} \cdot \sqrt{\frac{B_o}{C_o}} \qquad \text{2-XIX}$$

After calculation the result matches that of section B.1.

Finally, the phase velocity is calculated using the same equation as before, resulting in the same value as in section B.1.

C. Result of the two methods

By applying both methods, we obtain the same characteristic impedances, as shown in Figure 2-21.

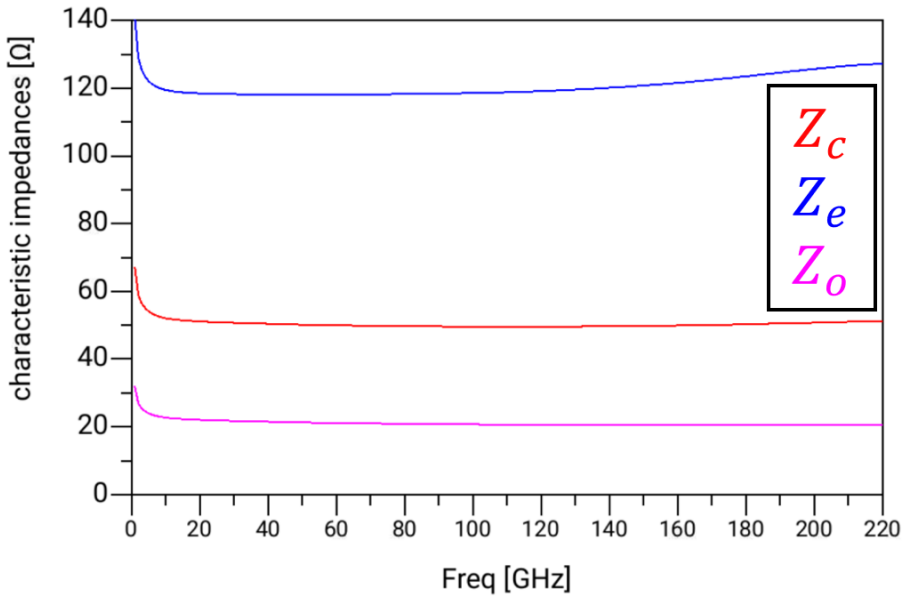
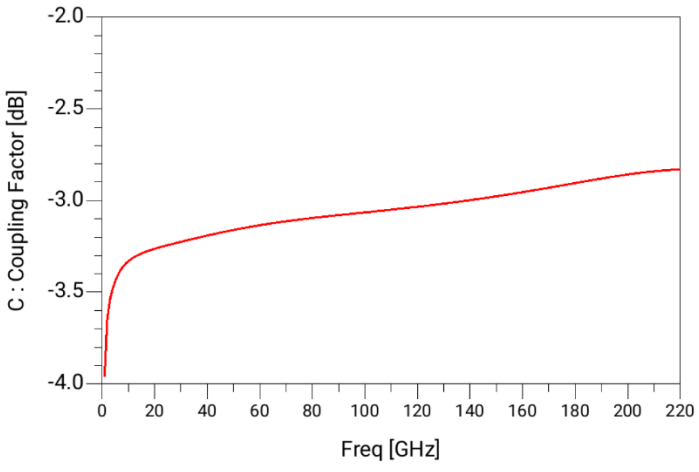


Figure 2-21: characteristics impedances from top to bottom of the even mode, of the coupler and of the odd mode, respectively, in function of the frequency.

It is observed that the even mode characteristic impedance increases more rapidly at high frequencies, likely due to the difference in phase velocities of the modes, which is examined later. Based on these characteristic impedances, the coupling factor can be calculated, as shown in Figure 2-22.



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Figure 2-22: Coupling factor in dB calculated based on characteristics impedances of the two modes, in function of frequency.

We see that this coupling factor increases from -3.3 dB at 40 GHz, up to-2.8 dB at 220 GHz.

Finally, Figure 2-23 presents phase difference of the two modes. Initially, both modes start at the same phase velocity resulting in the same phase, but as the frequency increases, the gap between their phase widens.

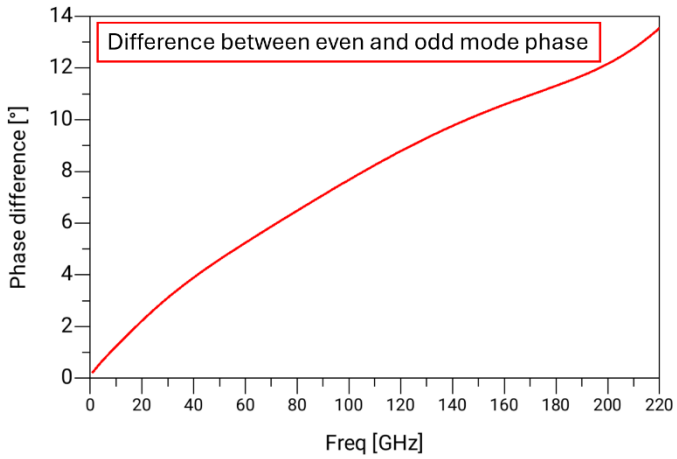


Figure 2-23: Phase velocity of the even (red) and the odd (blue) mode showing an increasing divergence in function of the frequency

This confirms that the phase velocity and with it the phase is mode dependent and that the difference grows with frequency.

In summary, we confirm, through precise EM simulation, the realization of a 3-dB directional coupler with low insertion loss ($IL < 0.4\,dB$), good matching ($RL > 20\,dB$), isolation ($Iso > 20\,dB$), and the correct phase shift (around $90° \pm 5°$) across the entire frequency band $[1\,GHz - 220\,GHz]$.

2.2.5.2 Test structure and measurement strategy

After analytical study and simulation followed by precise EM simulation that confirmed and validated the desired figures of merit in the previous section, we set out to accurately measure this device. This presents two challenges. First, performing 4-port measurements at 220 GHz, which remains quite rare and challenging to date. Second, designing a 4-port test structure that allows connecting the device with a gap of a few microns to a 50-µm pad pitch (100 µm between signal pads for GSGSG pads for differential probes), thereby enabling a transition and effectively matching the gaps.

High-frequency measurements inherently involve parasitic coupling effects (probe-to-probe). It is therefore more effective to introduce a controlled parasitic element, such as a half-thru, and eliminate the uncontrolled parasitic coupling. To achieve this, access lines are added to increase the spacing between the probes. These assess lines are removed by the on-wafer TRL calibration [42].

To perform TRL calibration, it is necessary to integrate the TRL standards directly on-wafer, as close as possible to the DUTs. These standards include Thru (B+C), Reflect (A), and Lines (D), which are presented in Figure 2-24.

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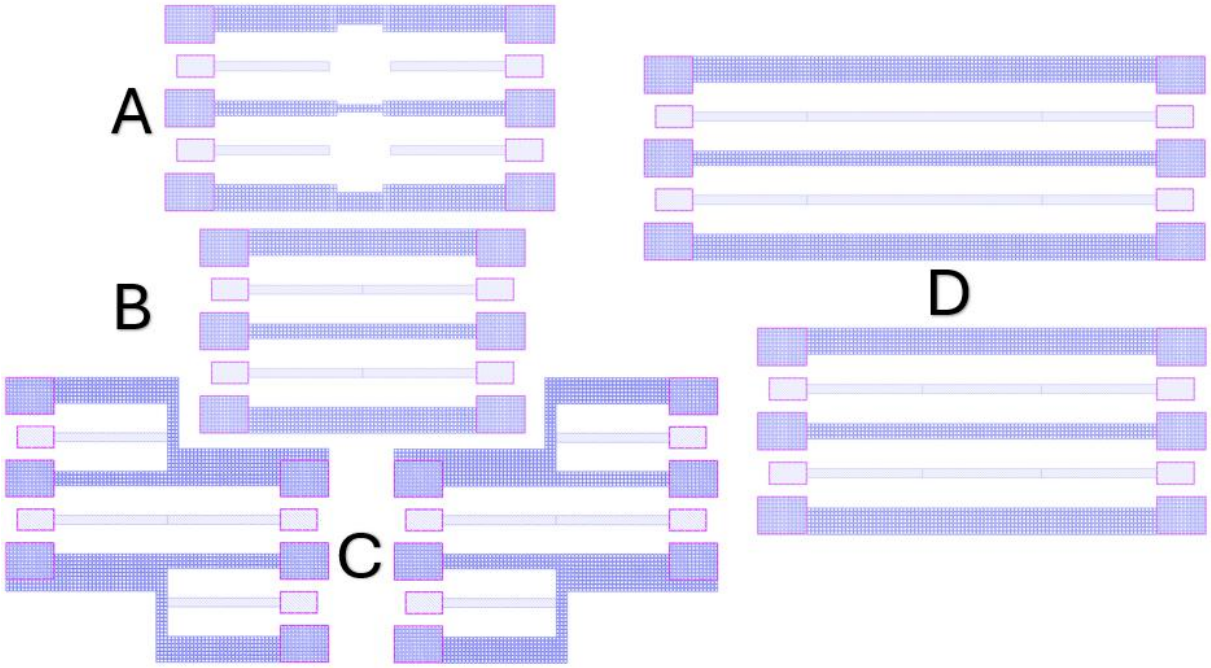
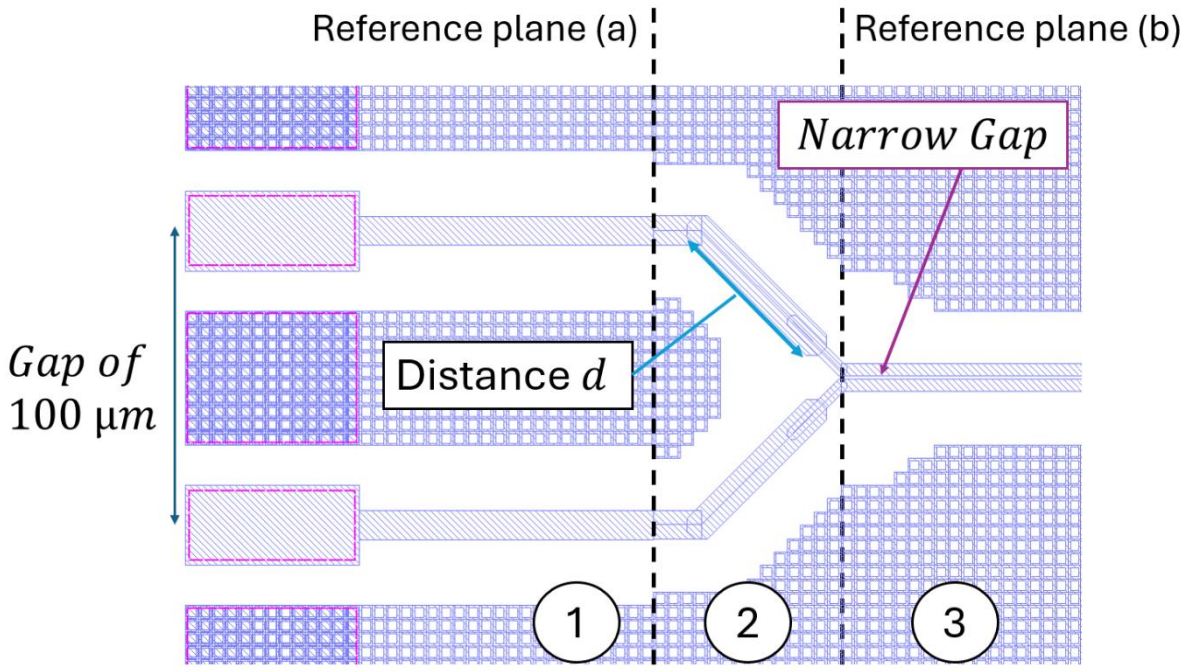


Figure 2-24: Layout view of the different TRL on-wafer standards (Thru (B+C), Reflect (A), and Lines (D)) integrated on silicon.

In our case, we perform a 4-ports (or differential) TRL calibration, which requires adding two additional standards, i.e. the crossed thru (C), to measure the transmission between all access points. We also chose to use two different line standard lengths to cover a broader frequency band. Furthermore, comparing the results from the two different lines helps validating the TRL calibration and the probe placement.

The second challenge is concerning the transition between two coplanar strips of the coupler, placed very close together with a gap of the order of a few microns, to the signal pads separated by 100 µm, as illustrated in Figure 2-25.



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Figure 2-25: Layout view showing the side of a DUT (coupled line coupler) with the access lines, highlighting the difference of gap between the coupled line strips and the measurement pads. Showing also the two reference plans a and b, that determine the three zones 1, 2 and 3.

For that purpose, a 45° access was designed to connect the edges of the DUT to the GSGSG pads. However, we must choose the characteristic impedance of these access lines (whether to keep the same width as the coupler, which differs from 50 Ω, or to directly transition to the same width as the 50 Ω pads access lines). We would like, in order not to impact on the coupler's response, to directly feed its accesses with a 50 Ω line. In this case, the lines would initially touch, creating a short circuit; even if this is avoided, it would result in a section of over-coupling. On the other hand, to mitigate this coupling effect, a thinner stripline could be placed along the entire 45° accesses, but this access line would significantly affect the DUT's response because it would have a characteristic impedance higher than 50 Ω. Thus, a trade-off on the distance d has been chosen to balance the effects of parasitic coupling and characteristic impedance variation. Finally, a taper was designed to join the two strips with different characteristic impedances.

It would be possible to perform calibration up to the device edge (reference plane (b)), but this would be very complicated due to parasitic coupling between the accesses. Moreover, in a realistic scenario, the coupler will always have a small access line to connect to the rest of the circuit. In summary, retaining the effect of these transitions would facilitate calibration and bring us closer to realistic performance in a more complex circuit. Therefore, it was logically decided to keep the reference plane (a) for our calibration, which will only serve to eliminate the impact of zone (1) (pad + half-thru).

We now propose to examine the effect of these access lines, which on one hand will exist in a final embedded version in a circuit, and on the other hand are necessary to ensure accurate measurement. Figure 2-26, Figure 2-27 and Figure 2-28 show the differences between the DUT zone 3 alone versus DUT + 45° access lines (zones 2+3), respectively, for the S-parameters: insertion loss, return loss and isolation, and finally phase difference between the thru and coupled ports.

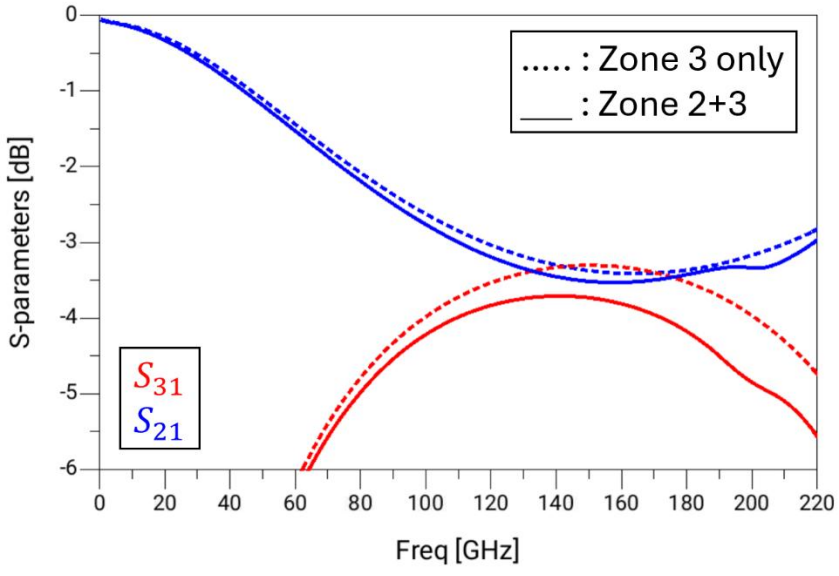


Figure 2-26: EM simulation result of the coupled line coupler with and w/o 45° access lines: transmission.

The additional losses of about 0.3 dB are explained by the added length of the 45° access lines. Furthermore, the slight frequency shift is attributed to the higher characteristic impedance of the access lines as well as parasitic coupling between them. Thus, the reduction in the 1 dB bandwidth can be explained by the introduction of parasitic effects related to the 45° access lines and their impact on the phase velocity.

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Figure 2-27 shows the impact of the access lines on both the return loss and the isolation. At the center frequency of 150 GHz, the return loss degrades from -30 dB in simulation to -20 dB in measurement, while the isolation decreases from 24 dB to 17 dB. Nevertheless, these values remain within an acceptable range.

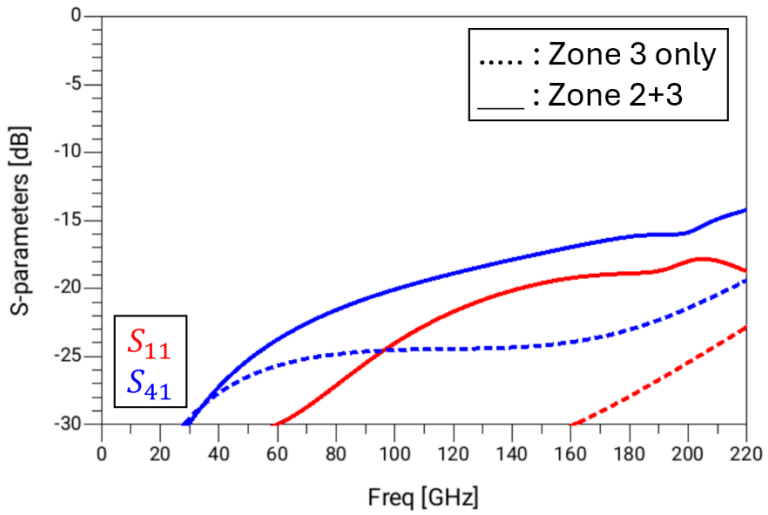


Figure 2-27: EM simulation result of the coupled line coupler with and w/o 45° access lines: return loss and isolation.

We can see a direct impact on the value of the phase difference that is increasing in addition to a reduction of the $\pm$ 5° bandwidth in Figure 2-28.

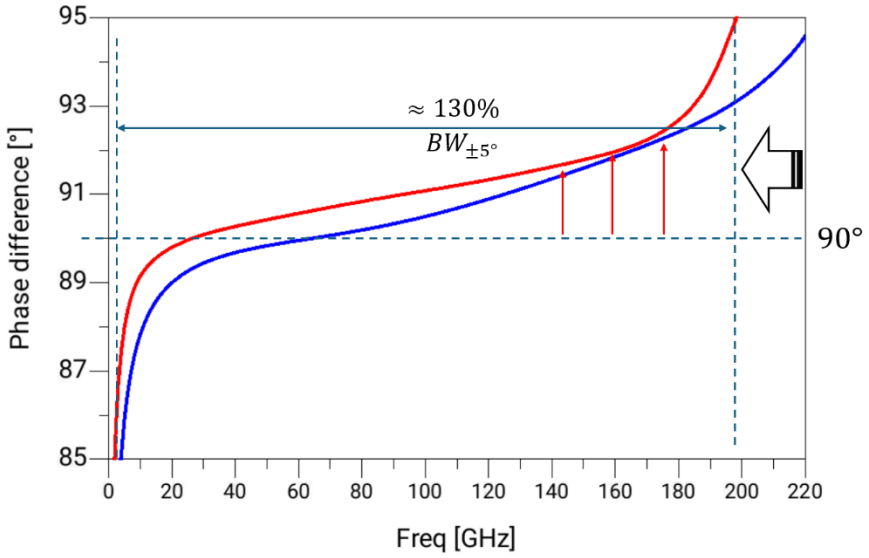


Figure 2-28: EM simulation result of the coupled line coupler with (red) and w/o (blue) 45° access lines : phase difference.

The addition of 45° access lines is necessary for measurement and, in most cases, for integration into more complex circuits, but it has a negative impact on RF performance. Therefore, this part must be handled carefully by the designer. Nonetheless, optimization is feasible. A more refined version could be achieved; however, due to the early stage of the thesis timeline, there was not enough time to fully fine-tune all DUTs before BRAY silicon tape-out deadline.

We used the $50\ \Omega$ coupler as an example in this section, but the same procedure was repeated for 70-Ω couplers. The next two subsections focus on comparing the EM simulation with the 45° access lines to the measurement calibrated up to reference plane (a).

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2.2.5.3 Simulation versus measurement results

This subsection addresses on-wafer 4-port measurements up to 220 GHz and their comparison with simulations for the coupler structures. The measurements were carried out using an Anritsu ME7838G4 VNA together with a Cascade S300 probe station. For 4-port measurements up to 220 GHz, a pair of MPI GSGSG probes MPI_{TITAN}^{TM} was used. Figure 2-29 shows a photograph of the measurement setup, including the probe station, the measurement probes held by the positioners, as well as the frequency extender.

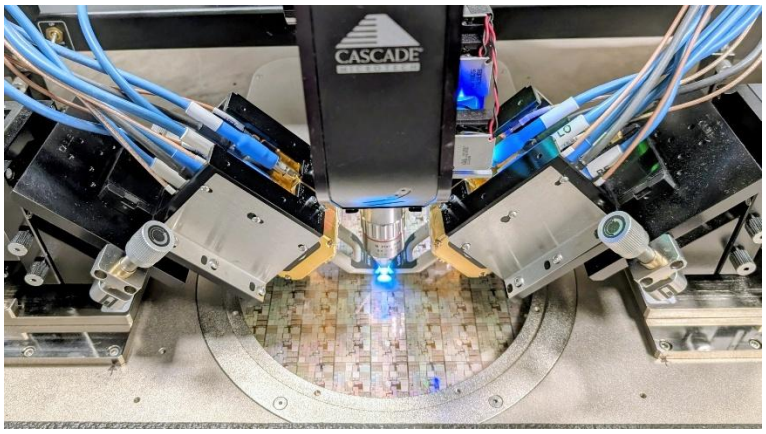


Figure 2-29: 4-ports 220-GHz S-parameters measurement setup picture.

Figure 2-30 shows a zoomed picture showing the measurement probes in a landed position.

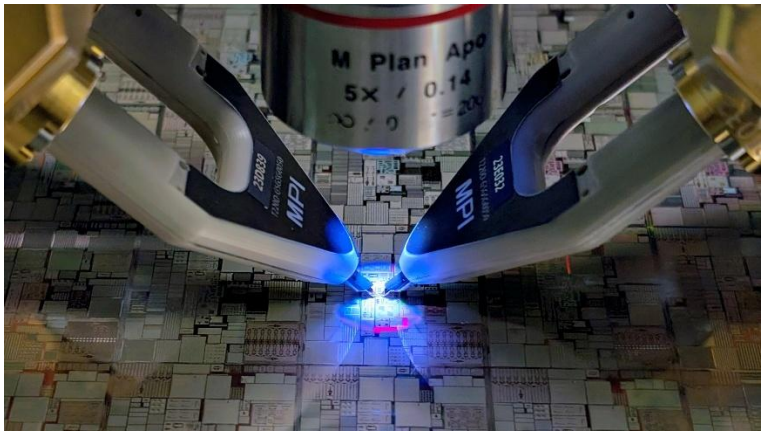


Figure 2-30: Picture of a zoomed view of the measurement setup showing the measurement probes landed on the wafer.

To perform on-wafer TRL calibration, the software provided by Anritsu for 4-port differential calibration was used.

A. 3-dB Coupler @$150GHz$ for $Z_c = 50\ \Omega$

In the case of the 3-dB coupler with $Z_c = 50\ \Omega$, the silicon-embedded layout (BRAY tape-out) is shown in Figure 2-31.

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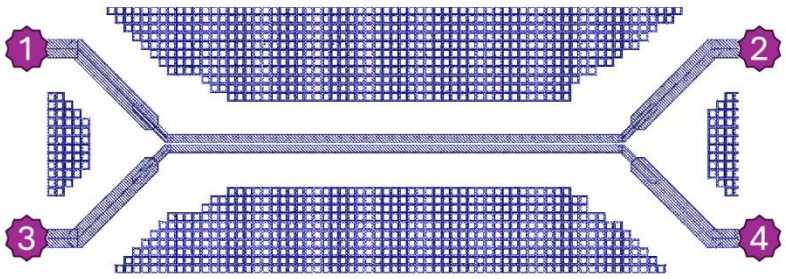


Figure 2-31: Layout view of the 3-dB coupler with $Z_c = 50\ \Omega$, embedded into BRAY tape-out.

The simulation results in the same reference plane are compared with the calibrated measurement results obtained using an on-wafer TRL calibration, as explained above. The measured versus EM-simulated S-parameters, in both magnitude and phase, are shown in Figure 2-32 and Figure 2-33, respectively.

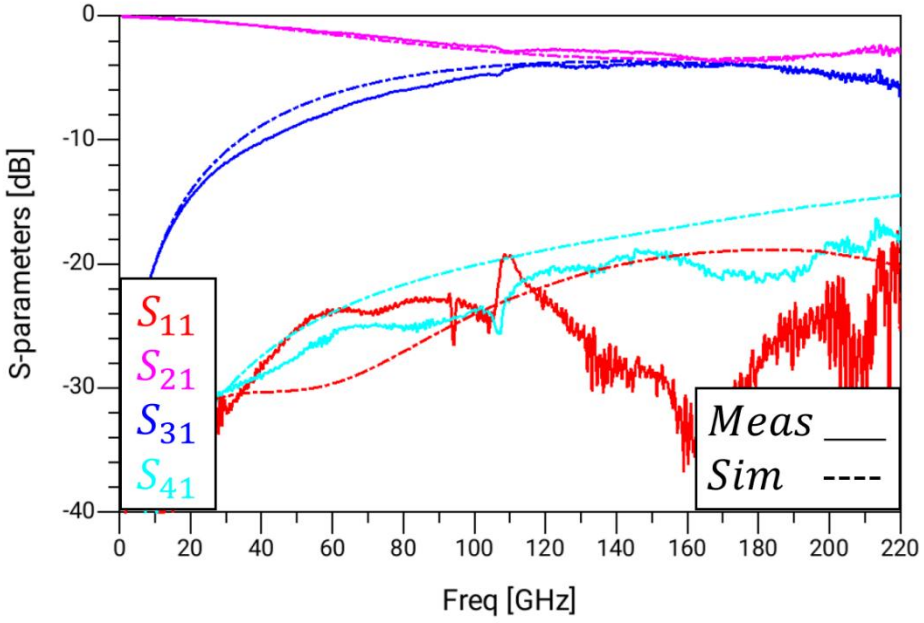


Figure 2-32: S-Parameter simulated vs measured results for return loss (S_{11}) and insertion loss for the coupled (S_{31}), thru (S_{21}) and isolated (S_{41}) ports for the 50-Ω coupled line coupler.

Figure 2-32 shows an overall good agreement between simulation and measurement results. The curves exhibit excellent return loss and isolation, better than 20 dB almost the whole measured frequency band, with a worst case of 17 dB isolation at 212 GHz. We also observe low insertion loss for both the thru and coupled paths, around 0.5-0.6 dB in measurement versus 0.4 dB in simulation.

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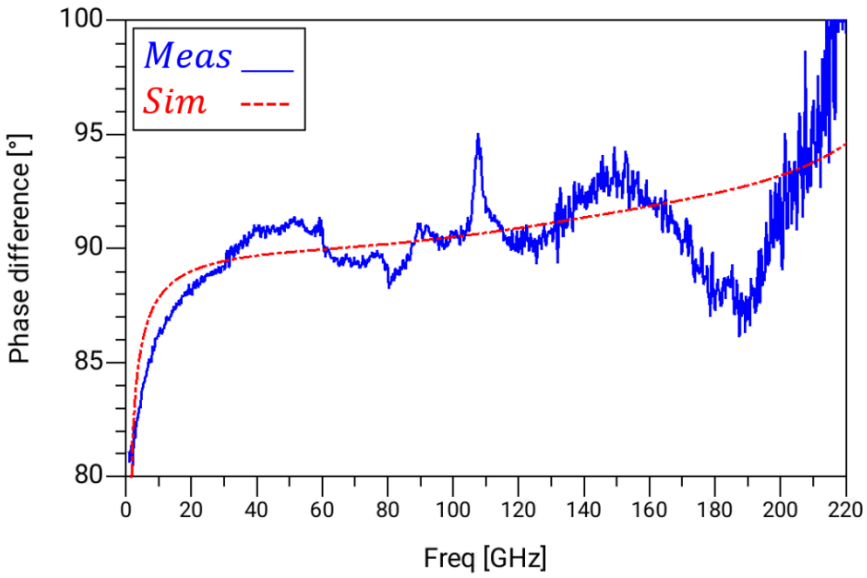


Figure 2-33: S-parameters simulated vs measured results for the difference of phase between the thru and coupled ports for the 50-Ω coupled line coupler.

From Figure 2-33, we can see a good agreement between simulation and measurement results. A phase difference lower than $\pm 5°$ between the thru and coupled ports is observed from 10 GHz up to 210 GHz. This defines a $BW_{\pm 5°}$ of 133%, which is excellent.

From both Figure 2-32 and Figure 2-33, a glitch in the measurement results can be seen on all curves between 105 and 110 GHz.

This can be explained by crosstalk effects in dual probes measurement that occurs especially at high frequencies, as explained in [43] and illustrated in Figure 2-34. This crosstalk effect (in red) introduces additional signal paths crossing between channels. The classical 4-ports TRL calibration does not consider the coupling effects from the adjacent channel, resulting in inaccuracies due to calibration errors.

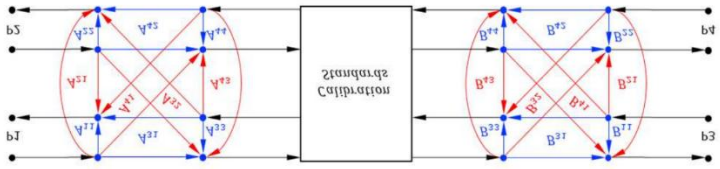


Figure 2-34: A signal path of 4-port dual probe calibration with in-probe crosstalk present in each pair of probe channels from [43].

According to [43], this issue can be mitigated by introducing additional standards called peer-terminated standards. The idea is to incorporate a 50-Ω load termination in the adjacent port for all types of standards in order to establish a consistent calibration environment and thus minimize inaccuracies due to crosstalk. A view of a conventional dual short and the peer-terminated short is shown in Figure 2-35.

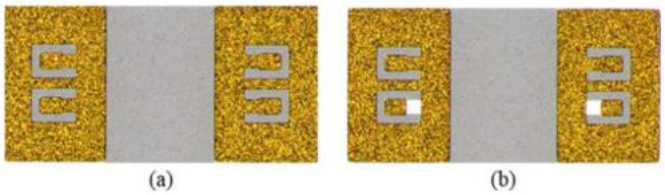


Figure 2-35: Short standards design: (a) dual short; (b) peer-terminated short from [43].

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The authors show a comparison between measurement of calibrated open, short and load for a classic dual mTRL calibration versus a peer terminated mTRL calibration as can be shown in Figure 2-36.

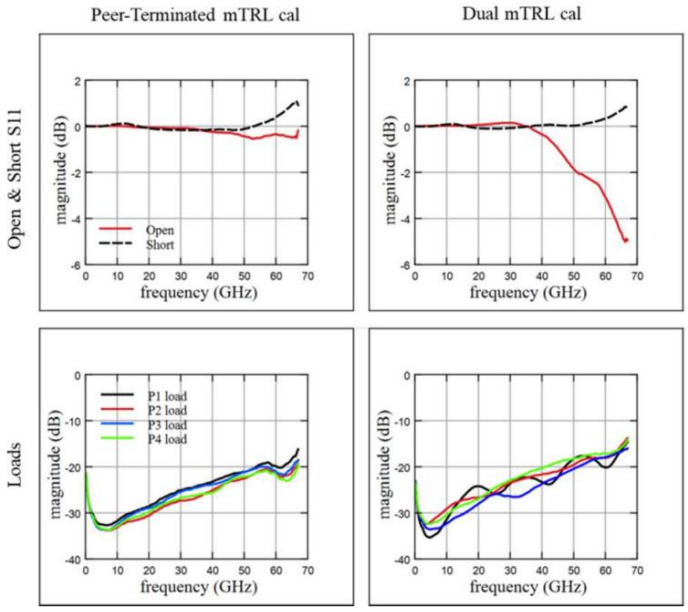


Figure 2-36: Measured S-parameter of mTRL calibrated open, short, load for classic calibration vs peer-terminated calibration, from [43].

As can be seen, the S_{11} magnitude of dual open has a 5-dB roll off at 67 GHz where on peer-terminated case it maintains a high reflection of S_{11} better than 0.5 dB. While for short case it remains comparable since in the dual short case the adjacent port connected to a short creating similar environment. Finally for the load measurement we can see that in the peer-terminated case the results are more consistent compared to the dual calibration case where we can see more fluctuation that can be related to calibration error caused by crosstalk according to the authors.

Unfortunately, this solution was identified at the end of the PhD, just after the 220-GHz 4-port measurements, and has therefore not yet been tested from our side.

A. 3-dB Coupler @$150GHz$ for $Z_c = 70\ \Omega$

In the case of the 3-dB coupler with $Z_c = 70\ \Omega$, the layout (BRAY tape-out) is shown in Figure 2-37.

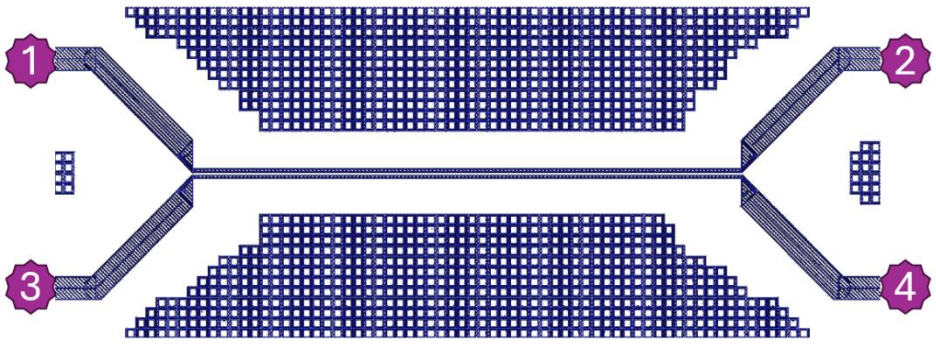


Figure 2-37: Layout view of the 3-dB coupler with $Z_c = 70.7\ \Omega$ embedded into BRAY tape-out.

Compared to the 50-Ω coupler, thinner lines are used to reach a higher characteristic impedance. As a result, this made the transition to the access lines more complex to implement in layout.

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The TRL-calibrated measurement results versus EM simulations for the insertion loss magnitude at the through, coupled, and isolated ports, as well as the input return loss, are shown in Figure 2-38. To do so, the port impedances (Z_0) in ADS were normalized to the characteristic impedance of the target coupler, such that: $Z_0 = Z_c = 70.7\ \Omega$.

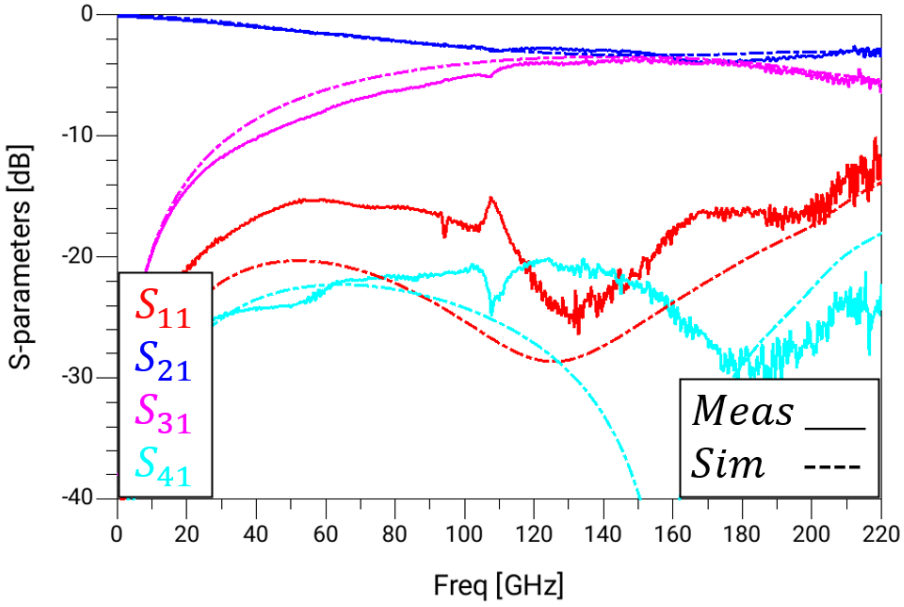


Figure 2-38: S-Parameter simulated vs measured results for return loss (S_{11}) and insertion loss for the coupled (S_{31}), thru (S_{21}) and isolated (S_{41}) port for the 70-Ω coupled line coupler.

As in the case of the 50-Ω coupler, a good correlation between simulation and measurement results is observed. A slight deviation of a few dB can be seen for the return loss; however, it remains better than 15 dB, which is largely sufficient, and can be explained by a small shift in the characteristic impedance of the coupler.

Regarding isolation, it remains excellent, better than 20 dB over the entire measured band. For the insertion loss, the measured results are very close to the simulations, with a maximum difference in the band of interest of about 0.5 dB between simulation and measurement results. For example, at 155 GHz: $S_{21_{sim}} = 3.5\ dB$ vs $S_{21_{meas}} = 3.4\ dB$ and $S_{31_{sim}} = 3.4\ dB$ vs $S_{31_{meas}} = 3.6\ dB$

Figure 2-39 shows the difference between the transmission phase at the through port and at the coupled port for the measurement compared to the EM simulation.

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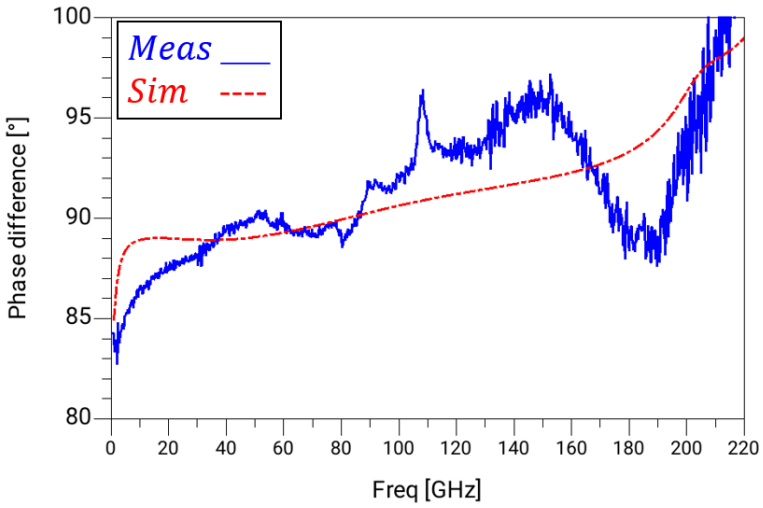


Figure 2-39: S-parameters simulated vs measured results for the difference of phase between the thru and coupled port for the 70-Ω coupled line coupler.

A good correlation between simulation and measurement results can be observed. As with all the 220-GHz 4-port measurements we performed using MPI probes, a glitch appears around 108 GHz. However, if we neglect the few peaks and glitches occurring beyond 108 GHz, we still maintain a very wide $BW_{\pm 5}° = [10 - 210]\ GHz$.

Overall, we have successfully demonstrated good agreement between simulation and measurement results. On the one hand, this validates the accuracy of the EM simulators used, as well as the EM stack provided by the foundry. On the other hand, it confirms the feasibility and quality of 220-GHz 4-port measurements which are quite uncommon as well as the accuracy of the employed on-wafer TRL calibration. From the DUT standpoint, we demonstrate the functionality, manufacturability, and relevance of the coupled line coupler.

In addition, we have highlighted a glitch specific to high-frequency 4-port measurements, along with a mitigation method proposed by MPI that has not yet been tested on our side, based on adding a “peer-terminated” standard to correct this calibration imprecision.

Our short-term perspective is to verify this concept using an EM simulator. First, we will extract the topology of the 220 GHz dual probes used, then create a corresponding model in HFSS in order to quantify the crosstalk effect over the entire simulated frequency band. Based on a 16-term TRL calibration for single probes, we will then propose a multi-term TRL calibration scheme to address this crosstalk issue.

As a longer-term perspective, we intend to apply this peer-terminated topology for on-wafer TRL calibration up to 220 GHz and compare it with the classical dual-TRL approach already in use. This will be done by characterizing the load with a 2-port 16-term calibration to obtain the most accurate estimation of this load, and then designing the peer-terminated (using the same load) standard as close as possible to the classical dual-TRL standard. This will allow a fair comparison between the two calibration approaches. If done, the proposed multi-term TRL scheme could also be embedded and evaluated alongside the two existing TRL approaches.

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2.3 Power splitter

2.3.1 Introduction

As already discussed, with increasing frequency, transistor technology limitations (f_t/f_{max}) affect active components performance, particularly PAs. This primarily impacts gain but also directly affects the P_{sat} and PAE. An effective approach to address this issue is to split the power before the transistors to relax compression requirements, then recombine the signals afterward, thereby increasing the overall saturation power of the circuit.

For that purpose, it is essential to have high-quality passive components because, for example, dividing and recombining by a factor of four yields a 6-dB gain on the saturated output power, as shown in Figure 2-40. Therefore, passive losses for dividing and combining must be kept below 3 dB; otherwise, the gain from parallelization is negated. On the other hand, parallelization requires replicating unit circuits, which consumes silicon area, highlighting our second challenge: reducing the silicon area used, particularly for the passive components involved in power division and recombination. Ultimately, the goal is to achieve a component that combines strong RF performance with reduced size.

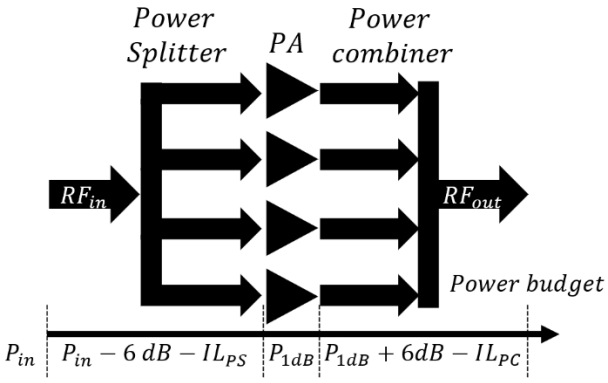


Figure 2-40: Simplified schematic view showing the interest of parallelization and impact of passive component losses on the power budget in the case of a PA parallelized over 4 paths.

2.3.2 1 to N power splitter

As discussed in the state-of-the-art chapter, in the context of improving antenna recombination gain and enhancing PA performance [23], particularly at high frequencies in terms of output power (P_{out}) it is increasingly common to use 1-to-N power splitters/combiners with N greater than 2. However, as N increases, the design of passive components becomes critical to minimize insertion loss and area consumption.

To address this requirement, consider the example of a 1-to-4 power splitter. An attractive approach could be the 1-to-4 Wilkinson power splitter. For a device matched to 50 Ω at both input and output, the characteristic impedance of the Wilkinson branches is 100 Ω, based on the following equation:

$$Z_c = Z_0 \cdot \sqrt{N} = 100\ \Omega$$

Based on the transmission lines available in the design kit (DK), the maximum synthesizable characteristic impedance is 73 Ω. By using custom-designed transmission lines, this maximum characteristic impedance can be increased to about 80 Ω. However, as characteristic impedance

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increases, the signal strip width decreases, which results in higher losses. Therefore, we are constrained both by the technology and by the induced losses.

A practical approach to implement a 1-to-N power splitter is to cascade a 1-to-2 Wilkinson divider $N/2$ times. Considering the 1-to-4 example, this results in a device that is realizable in terms of characteristic impedances but consumes a significant amount of area for two reasons: the overall length of $\frac{\lambda}{2}$ and the width constrained by the coupling limit distance, which depends on the technology and frequency. At higher frequencies, this coupling limit distance increases while the device length λ_G decreases.

Our experience shows that, at 28 GHz, the coupling limit distance can be considered to be equal to 20 µm, whereas $\frac{\lambda}{2} = 2400\ \mu m$, yielding a ratio of 100. At 150 GHz, the coupling limit distance is about 40 µm for a $\frac{\lambda}{2}$ of $500\ \mu m$, resulting in a ratio of 12.5. In conclusion, at higher frequencies, it becomes increasingly important to address devices where the coupling limit distance is a critical factor. Figure 2-41 shows a simplified schematic of a cascaded Wilkinson power splitter, with a limit distance equal to 40 µm.

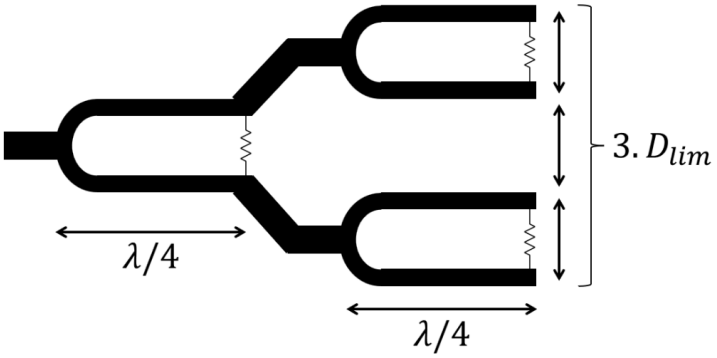


Figure 2-41: simplified schematic of cascaded 1-to-2 Wilkinson power splitter to form a 1-to-4 power splitter.

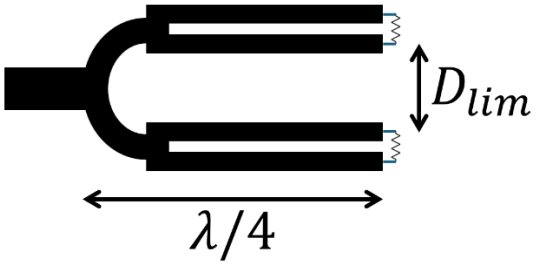
In our case, if we intend to design this circuit at 150 GHz, fully unfolded and without considering the access lines, the length L and total width W of the circuit can be calculated as follows:

$$L = \frac{\lambda}{2} > 550\ \mu m$$

$$W = 3 \cdot D_{lim} + 4 \cdot W = 120 + 40 = 160\ \mu m$$

2.3.3 1-to N power splitter topology based on coupled lines

In the context of size reduction in insertion loss limitation, an interesting concept based on coupled lines was presented in [23]. It consists of a direct 1-to-4 divider using coupled lines to perform power division and recombination, as illustrated in Figure 2-42.



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Figure 2-42: Simplified schematic of the power divider based on coupled lines, from [23].

This topology enables a direct 1-to-4 power division with realizable strips dimensions, effectively halving the total length compared to other approaches. Additionally, the width is reduced because the use of coupled lines mitigates the impact of the coupling limit distance. Overall, this results in a significant reduction in the circuit area. We propose to perform a calculation example at 150 GHz, similar to the cascaded Wilkinson case discussed in the previous section:

$$L = \frac{\lambda}{4} > 270\ \mu m$$

$$W = D_{lim} + 4.W + 2.Gap = 40\ + 8 + 2 = 50\ \mu m$$

Consequently, the area is divided by more than 6.

Furthermore, for space optimization, it is much easier to meander coupled lines than single lines because they are narrower and the electromagnetic field remains mostly confined between the coupled strips, which slightly reduces parasitic coupling effects caused by meandering.

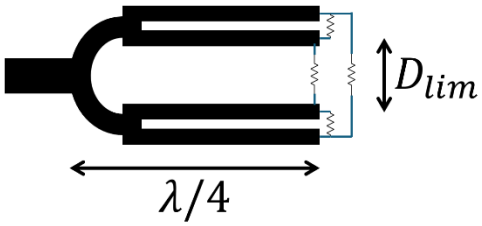
For reference, the unfolded dimensions of the two 1-to-4 dividers at 150 GHz are presented in Table 2-2.

$Power\ Splitter$	$Cascaded\ Wilkinson$	$Coupled\ lines\ based$
$Length\ [\mu m]$	550	270
$Width\ [\mu m]$	160	50
$Area\ [mm^2]$	0.088	0.0135

Table 2-2: Comparison table of dimensions between a cascaded Wilkinson 1-to-4 power divider and the proposed coupled line based power divider, demonstrating a drastic reduction in footprint using the coupled line based splitter.

The concept was proposed in [23], but the output isolation and return loss were not adequately addressed by the authors. These figures of merit (output return loss), which upon verification are around 10 dB, are clearly insufficient for the intended application, particularly for the power combining function. Furthermore, no theoretical equation synthesis was presented or developed, making the design process quite complex and laborious.

Therefore, we aimed to improve the concept by addressing the shortcomings in output isolation and matching by adding resistors of a specific value between the couplers, as shown in Figure 2-43. Also by developing theoretical equations based on even/odd mode analysis and proposing several implementations: a PCB version and an integrated version at 28 GHz (which will not be discussed in this manuscript), a preliminary version at 150 GHz, and finally an optimized, meandered final version at 150 GHz.



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Figure 2-43: Simplified schematic of the power divider based on coupled lines improved by adding resistors.

2.3.4 Theorical equations

To develop the theoretical equations, proceeded as follows. First, we have calculated the return loss and isolation at the output, which requires the decomposition into even and odd modes, and thus the even and odd parameters. Next, we have calculated the input return loss, which only requires the even mode, and finally, by symmetry, we have deduced the remaining parameter(s), which are the transmission coefficients. For thes developments, this section considers ideal, lossless transmission lines.

2.3.4.1 Output return loss and isolation

The theoretical development of the equations is based on the even/odd mode analysis. To achieve this, many symmetry plans were used. The device under study features an horizontal plan of symmetry at the input junction and two secondary plans of symmetry at the junctions at the input of the coupled lines, as illustrated in Figure 2-44. These plans of symmetry were used to apply even and odd modes decomposition.

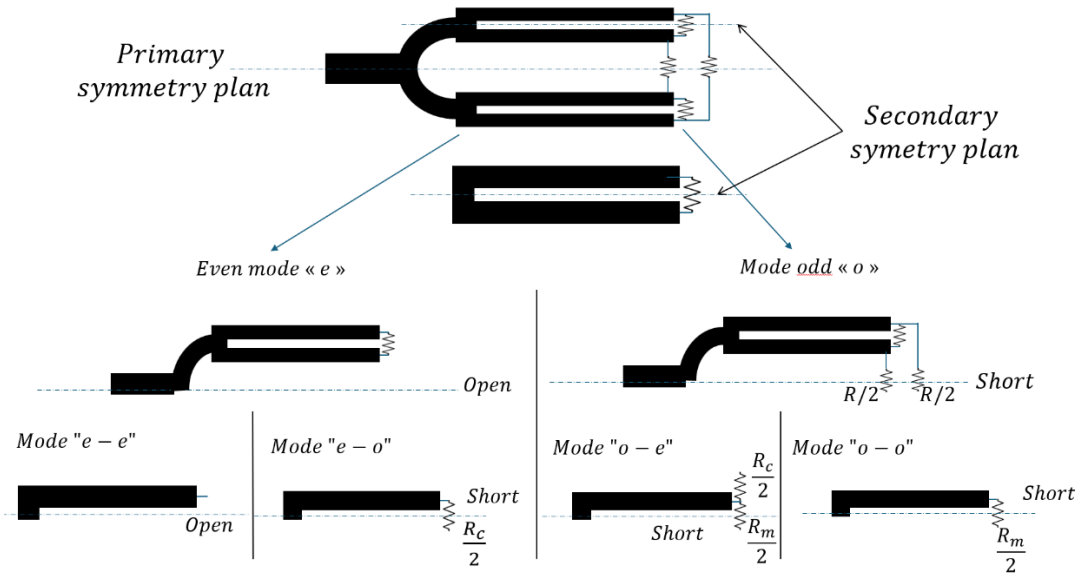


Figure 2-44:Simplified schematic detailing the even and odd mode decomposition method and the symmetry plans used for the double decomposition.

The method thus involves performing a two-step decomposition into four simple subcircuits: ee (“even-even”), eo (“even-odd”), oe (“odd-even”), and finally oo (“odd-odd”). These subcircuits are also illustrated in Figure 2-44.

We propose to show a simplified schematic detailing electrical parameters and the ports of the splitter as shown in Figure 2-45.

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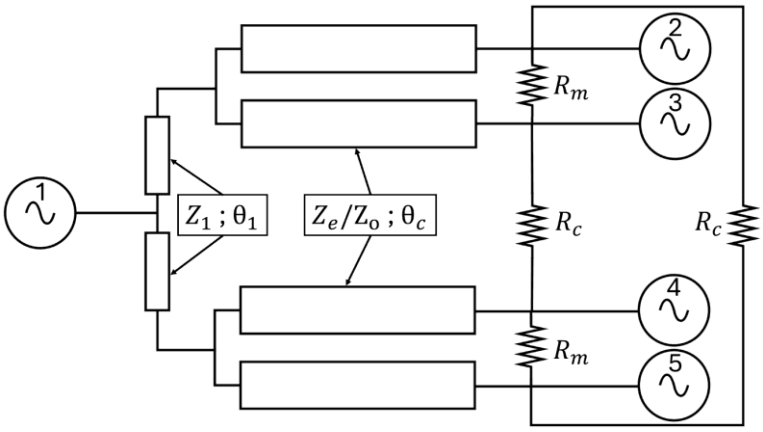


Figure 2-45: simplified schematic detailing electrical parameters and numbering the ports of the splitter

We first want to calculate the output return loss ($S_{22} = S_{33} = S_{44} = S_{55}$, by symmetry):

$$S_{22} = \frac{S_{22_e} + S_{22_o}}{2} = \frac{S_{11_{ee}} + S_{11_{eo}} + S_{11_{oe}} + S_{11_{oo}}}{2} \quad \text{2-XX}$$

We also calculate the isolations between output ports in the same way and considering the symmetries ($S_{23} = S_{45} = S_{32} = S_{54}$; $S_{24} = S_{42} = S_{35} = S_{53}$; $S_{25} = S_{52} = S_{34} = S_{43}$):

$$S_{23} = \frac{S_{12_e} + S_{12_o}}{2} = \frac{S_{11_{ee}} - S_{11_{eo}} + S_{11_{oe}} - S_{11_{oo}}}{2} \quad \text{2-XXI}$$

$$S_{24} = \frac{S_{12_e} - S_{12_o}}{2} = \frac{S_{11_{ee}} - S_{11_{eo}} - S_{11_{oe}} + S_{11_{oo}}}{2} \quad \text{2-XXII}$$

$$S_{25} = \frac{S_{22_e} - S_{22_o}}{2} = \frac{S_{11_{ee}} + S_{11_{eo}} - S_{11_{oe}} - S_{11_{oo}}}{2} \quad \text{2-XXIII}$$

Our hypothesis is that the phase velocities of the even and odd modes are identical. To solve the equations, the four single-port subcircuits were considered as networks. Next, to determine the S_{11} parameter for each mode, we must first calculate the input impedance $Z_{in_{xx}}$ for each subcircuit.

Here is definition of the variables used in the next equations:

- Z_0 : Reference and access lines characteristic impedance.
- Z_1 : Characteristic impedance of the first transmission line.
- Z_{ee} & Z_{eo} : Even mode characteristic impedances of the coupled line.
- Z_{oe} & Z_{oo} : Odd mode characteristic impedances of the coupled line.
- θ_1 : Electrical length of the transmission line performing the first division.
- θ_c : Electrical length of the coupled line pair.
- $Z_{in_{xx}}$: Input impedance seen at the circuit input for mode xx (where $xx = ee, eo, oe, oo$).
- $Z'_{in_{xx}}$: Input impedance seen between two lines in the cascaded case.

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- R_c : Resistance between each coupled access.
- R_m : Resistance between uncoupled accesses.

The equation development proceeds as follows:

Even-even mode:

Figure 2-46 shows a simplified schematic detailing the component and their parameters that constitute the sub circuit of the equivalent mode.

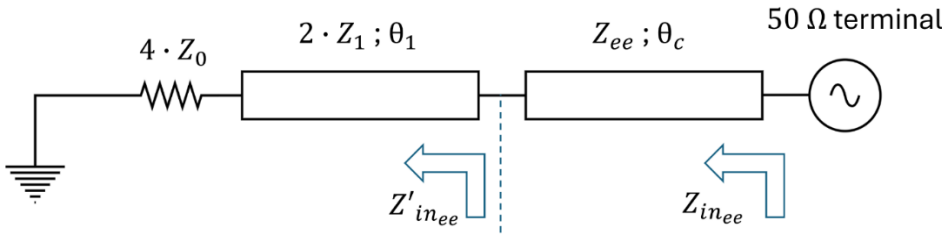


Figure 2-46: Simplified schematic detailing the "even-even" sub circuit after double decomposition showing the electrical parameters of each component

The calculations are carried out as follows:

$$Z'_{in_{ee}} = 2 \cdot Z_1 \cdot \frac{4 \cdot Z_0 + j2 \cdot Z_1 \cdot \tan(\theta_1)}{2 \cdot Z_1 + j4 \cdot Z_0 \cdot \tan(\theta_1)} \quad \text{2-XXIV}$$

$$Z_{in_{ee}} = Z_{ee} \cdot \frac{Z'_{in_{ee}} + jZ_{ee} \cdot \tan(\theta_c)}{Z_{ee} + jZ'_{in_{ee}} \cdot \tan(\theta_c)} \quad \text{2-XXV}$$

$$S_{11_{ee}} = \frac{Z_{in_{ee}} - Z_0}{Z_{in_{ee}} + Z_0} \quad \text{2-XXVI}$$

Even-odd mode:

Figure 2-47 shows a simplified schematic detailing the component and their parameters that constitute the sub circuit of the equivalent mode.

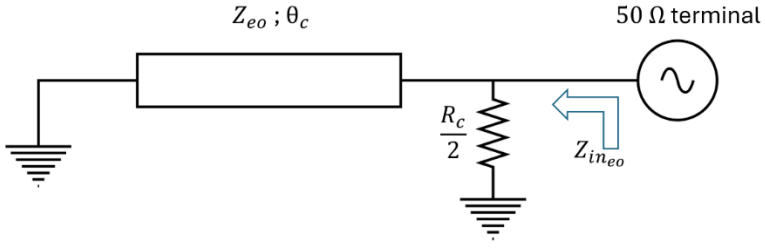


Figure 2-47: Simplified schematic detailing the "even-odd" sub circuit after double decomposition showing the electrical parameters of each component.

The calculations are carried out as follows:

$$Z_{in_{eo}} = jZ_{eo}.tan(\theta_c) \,//\, \frac{R_c}{2} \quad \text{2-XXVII}$$

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$$Z_{in_{eo}} = \frac{jZ_{eo} \cdot tan(\theta_c) \cdot \frac{R_c}{2}}{jZ_{eo} \cdot tan(\theta_c) + \frac{R_c}{2}} \quad \text{2-XXVIII}$$

$$S_{11_{eo}} = \frac{Z_{in_{eo}} - Z_0}{Z_{in_{eo}} + Z_0} \quad \text{2-XXIX}$$

Odd-even mode:

Figure 2-48 shows a simplified schematic detailing the component and their parameters that constitute the sub circuit of the equivalent mode.

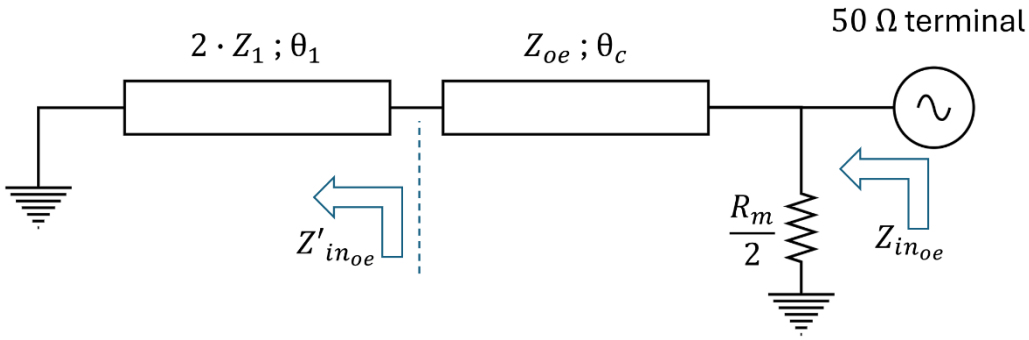


Figure 2-48: Simplified schematic detailing the "odd-even" sub circuit after double decomposition showing the electrical parameters of each component.

The calculations are carried out as follows:

$$Z_{in_{oo}} = jZ_{oo} \cdot \tan(\theta_c) \,//\, \frac{R_c}{2} \,//\, \frac{R_m}{2} \quad \text{2-XXX}$$

$$S_{11_{oo}} = \frac{Z_{in_{oo}} - Z_0}{Z_{in_{oo}} + Z_0} \quad \text{2-XXXI}$$

Odd-odd mode:

Figure 2-49 shows a simplified schematic detailing the component and their parameters that constitute the sub circuit of the equivalent mode.

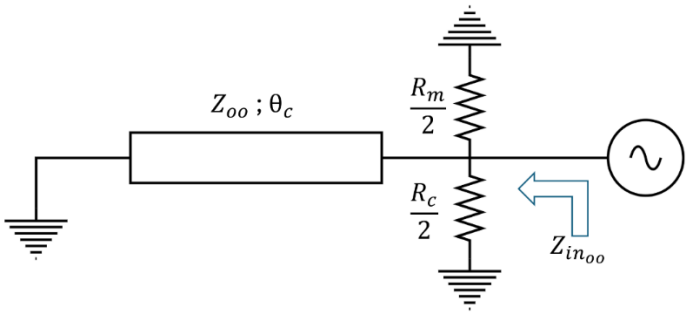


Figure 2-49: Simplified schematic detailing the "odd-odd" sub circuit after double decomposition showing the electrical parameters of each component.

The calculations are carried out as follows:

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$$Z'_{in_{oe}} = Z_{oe} \cdot \frac{j2 \cdot Z_1 \cdot \tan(\theta_1) + jZ_{oe} \cdot \tan(\theta_c)}{Z_{oe} + j(j2 \cdot Z_1 \cdot \tan(\theta_1)) \cdot \tan(\theta_c)} \quad \text{2-XXXII}$$

$$\mathrm{Z_{in}}_{oe} = Z'_{in_{oe}} // \frac{R_m}{2} \quad \text{2-XXXIII}$$

$$S_{11_{oe}} = \frac{Z_{in_{oe}} - Z_0}{Z_{in_{oe}} + Z_0} \quad \text{2-XXXIV}$$

After calculating the $S_{11_{xx}}$ parameters for each of the four subcircuits, we are able to calculate the output isolations and return loss as explained in the beginning of the section.

2.3.4.2 Input return loss and insertion loss

The calculation of S_{11} is performed by considering the "odd-even" mode as follows:

$$Z_{in_2} = \frac{Z_{oe}}{2} \cdot \frac{\frac{Z_0}{2} + J.\frac{Z_{oe}}{2}.tan\,(\theta_c)}{\frac{Z_{oe}}{2} + J.\frac{Z_0}{2}.tan\,(\theta_c)}$$

$$Z_{in_1} = Z_1 . \frac{Z_{in_2} + J.Z_1.tan\,(\theta_1)}{Z_1 + J.Z_{in_2}.tan\,(\theta_1)}$$

$$Z_{in} = \frac{Z_{in_1}}{2}$$

$$S_{11} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0}$$

with Z_{in_2} the input impedance of the coupled lines and Z_{in_1} the input impedance of the power divider, as shown in Figure 2-50.

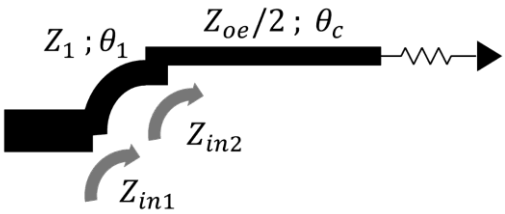


Figure 2-50: Simplified schematic of the device using "odd-even" circuit input impedances for the purpose of calculating the circuit's S_{11}

Considering the symmetry we have:

$$S_{21} = S_{31} = S_{41} = S_{51}$$

And knowing that:

$$S_{11}^2 + S_{21}^2 + S_{31}^2 + S_{41}^2 + S_{51}^2 = 1$$

From the two previous equations we have:

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$$S_{11}^2 + 4 \cdot S_{21}^2 = 1$$

We can finally calculate all the insertion loss as follows:

$$S_{21} = \frac{\sqrt{1 - S_{11}^2}}{2}$$

The equations were validated in ADS using ideal microstrip lines by comparing the results obtained from simulating the four subcircuits, extracting the S_{11} parameter for the relevant mode, and applying the equations presented above against the simulation of the complete circuit. We observed perfect agreement, demonstrating the accuracy of the equations developed in this subchapter for the studied topology. Building on this theoretical foundation, reinforced by simulation tools, we present a summary of the recommended design flow for this device in the next sub-section.

2.3.5 Design flow for 1 to 4 power splitter/combiner based on coupled lines

The design methodology can be summarized in four major steps:

Calculation of ideal element parameters: using the equations presented in the previous section, a MATLAB code has been employed to simplify the calculations. When applying these equations, it is necessary to establish design specifications that set minimum or maximum values for the figures of merit. We put a threshold of 20 dB for both isolation and return loss.

Simulation with ideal microstrip lines: using ADS, simulations were performed with ideal microstrip lines based on the results from step one to validate the calculations according to S-parameters criteria.

Design with real microstrip lines: the design was translated from ideal microstrip lines to real microstrip lines on a specific technology (in our case, B55x 7ML) using the Design Rule Manual (DRM) or design charts to convert electrical parameters ($Z, Z_e, Z_o, \theta, etc.$) into physical parameters (width, gap, length, etc.). Electromagnetic simulations are then conducted without considering isolation resistances. A satisfactory result is confirmed only when $S_{11} < -20\ dB$, allowing progression to the next step.

Adding loads and access lines: loads and their access lines were added, followed by re-simulation and optimization as needed. The success criteria are output isolation and return loss. Subsequently, 50-Ω access lines are incorporated, and final optimization is performed.

Upon completing these four steps, a state-of-the-art, functional structure is obtained. The final task involves layout optimizations, such as meandering coupled lines to optimize silicon area consumption.

2.3.6 Layout & simulation vs measurement results

An additional challenge, beyond those discussed in the previous sections, is that we have only a 4-port VNA to measure a 5-port device. Multiple solutions exist to address this challenge and some of them are discussed in the following sub-section.

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2.3.6.1 Back-to-back power splitter

One solution, albeit with very limited results, is to measure the device in a back-to-back configuration, which provides information only on the insertion loss. Figure 2-51 shows the layout of the back-to-back power divider integrated on BRAY tape-out.

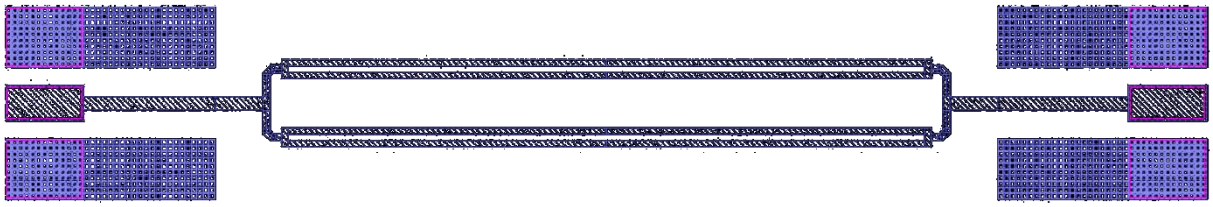


Figure 2-51: Layout view of the 1-to-4 power splitter in back-to-back configuration, embedded into BRAY tape-out

Figure 2-52 presents the comparison between simulation and measurement results of the 1-to-4 back-to-back power divider integrated on BRAY tape-out (B55X 7ML). while Figure 2-53 shows a zoomed view of insertion losses.

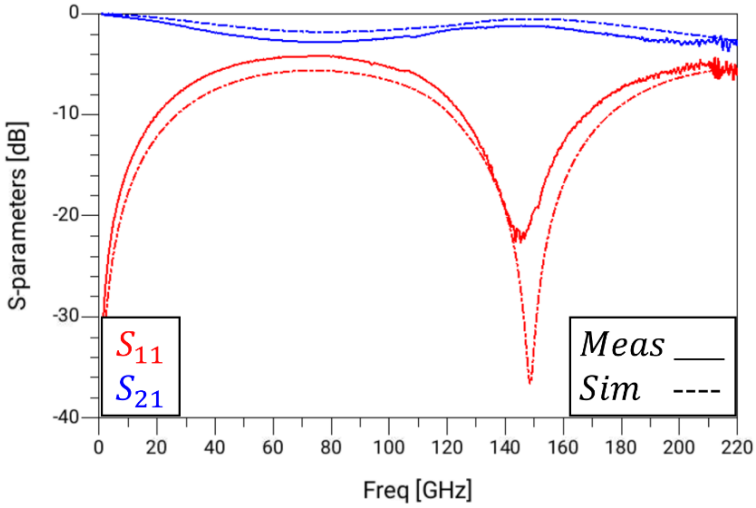


Figure 2-52: Simulation (in dotted line) vs measurement (in solid line) result of the 1-to-4 power divider embedded into BRAY tape-out.

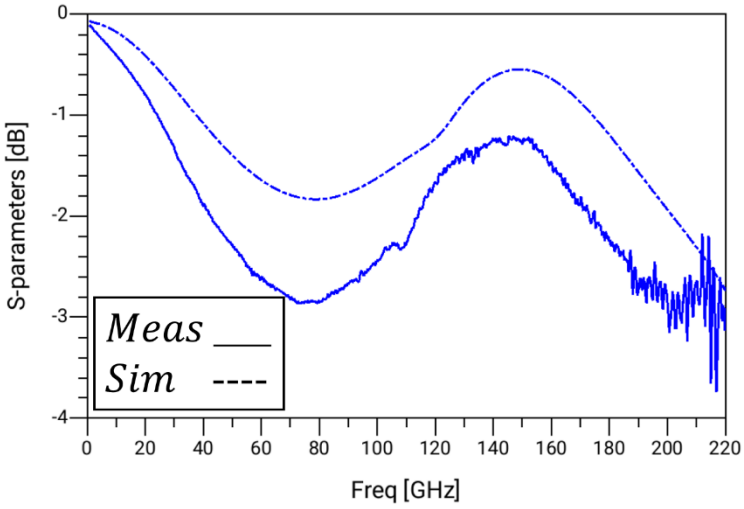


Figure 2-53: Simulation (in dotted line) vs measurement (in solid line) insertion loss of the 1-to-4 power divider embedded into BRAY tape-out.

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The simulation of the back-to-back device shows a 0.7-dB insertion loss, which corresponds to 0.35 dB per power splitter. Meanwhile, the measurement indicates a loss of 1.2 dB, i.e. 0.6 dB per power splitter. The small discrepancy remains relatively constant beyond approximately 50GHz. It mainly corresponds to additional losses captured in measurement but not in simulation, as observed for the other DUTs. Nevertheless, the overall trend of the two curves remains essentially identical despite this slight difference, which is an excellent result.

Overall, the EM simulation curves align well with the measurement results, reflecting both an accurate simulation setup and good device performance. However, to fully qualify a power splitter, it is necessary to evaluate not only its insertion loss but also its isolation and output port balance. These parameters are examined using the next measurement method.

2.3.6.2 Unfold power splitter (BRAY tape-out)

For more comprehensive results, it is necessary to integrate two structures containing the same DUT, alternating the connected ports as illustrated in Figure 2-54 and Figure 2-55. Ports not connected to the VNA during measurement are terminated with on-wafer 50-Ω resistors provided by the design kit. These resistors are measured in standalone to validate the obtained results, and re-normalize the ports if necessary, in case the resistors are not 50 Ω.

The power splitter is unfolded because a parasitic coupling effect was observed between the two couplers just before the tape-out, which degrades performance. To facilitate measurements, this coupling was eliminated by implementing a T-structure.

Moreover, if a parallel structure (non-T) was considered, the four output ports would be located at the same point, making the design of the access lines and thus the routing for measurement with GSGSG pads very challenging, since it is not possible to place the pads side by side; they must be arranged face to face.

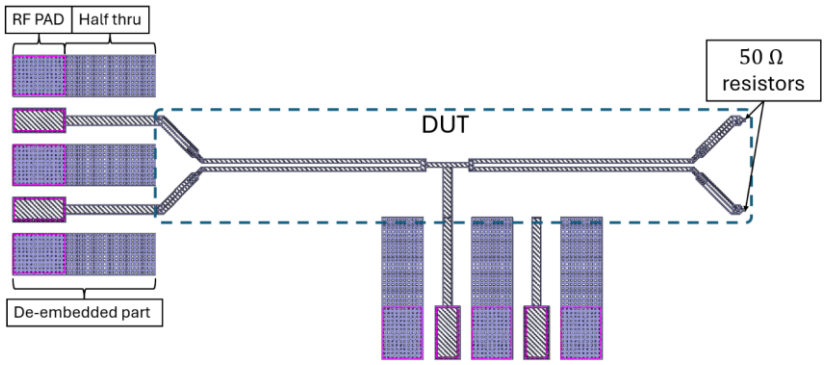


Figure 2-54: Layout view of the unfolded power splitter connected with GSGSG pad in a disposition to measure the transmission parameters and the input return loss, and finally output matching and isolation.

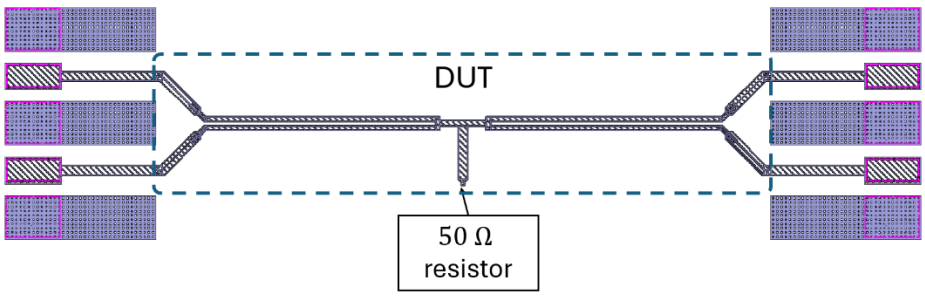


Figure 2-55: Layout view of the unfolded power splitter connected with GSGSG pad in a disposition to measure isolations and output return loss.

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After simulation and measurement, we obtain the insertion loss and return loss shown in Figure 2-56.

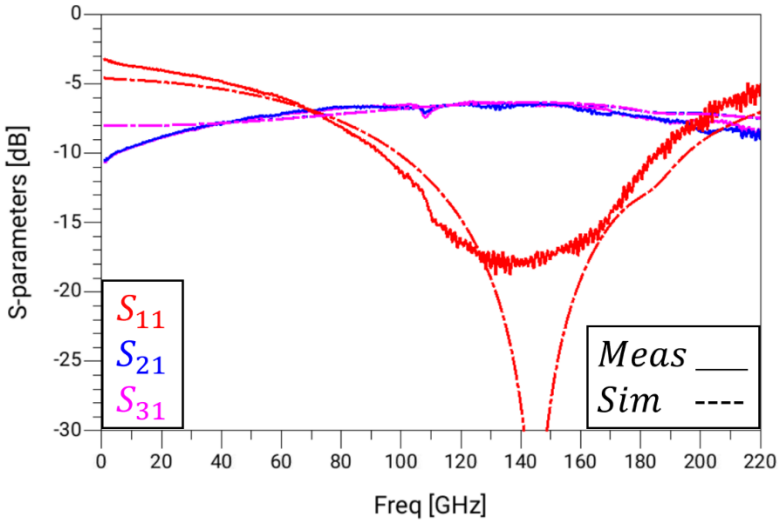


Figure 2-56: Simulation vs measurement results showing the insertion loss and input return loss.

As can be seen across the entire band, the simulation and measurement curves match well. Furthermore, at the frequency of interest, a perfect balance of insertion loss between the two outputs is observed in terms of amplitude as can be seen in Figure 2-35 and in terms of phase as can be seen in Figure 2-57. The measured insertion loss reaches $0.55\ dB$ compared to $0.35\ dB$ in simulation, which is excellent and consistent with the order of magnitude observed in the back-to-back configuration. Additionally, the device is well matched at the frequency of interest with a wide bandwidth for $S_{11} < -15\ dB$ of $[105 - 170]\ GHz$.

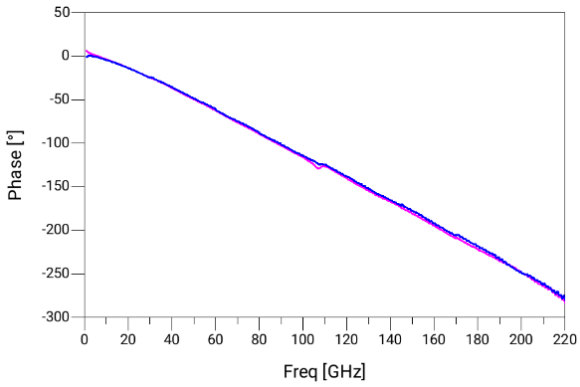


Figure 2-57: Measurement result of the phase of S_{21} and S_{31}showing a perfect phase balance between the two outputs.

Unfortunately, this configuration does not allow us to connect the isolation resistors, so the device can only be used as a splitter. However, a co-simulation including the resistors (120 Ω) was performed to evaluate the expected performance after layout rework.

The results of the co-simulation compared to the measurement are shown in Figure 2-58, detailing the isolation and return loss.

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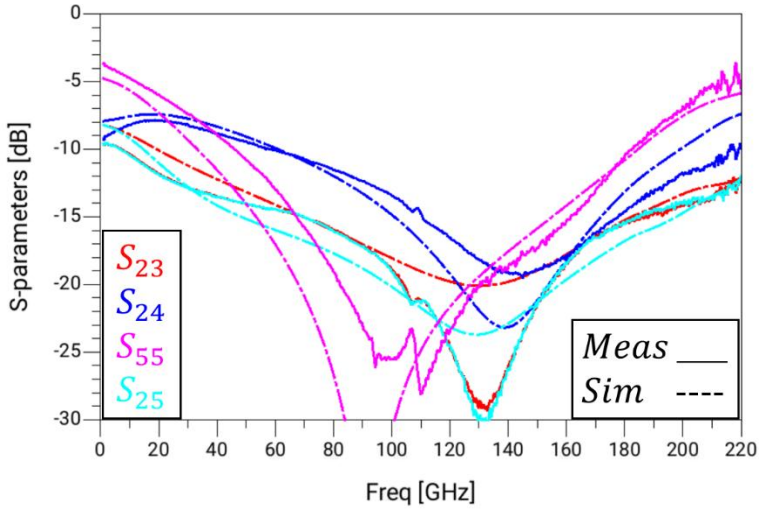


Figure 2-58: Simulation vs measurement results after co-simulation for adding effects of the isolation resistors showing the isolation between output ports and output return loss.

It can be observed that the simulation and measurement curves match closely. Furthermore, at our frequency of interest, all parameters are below or close to -20 dB, confirming both the device functionality and the accuracy of the simulation setup.

2.3.6.3 Meandered version (BOIGU tape-out)

A more advanced version aims to reduce the device footprint while maintaining its excellent loss performance by employing a meandered design while incorporating the isolation resistors. A slight compensation scheme for parasitic coupling effects related to the meandering must be considered. The goal is for each coupler to experience the same, or as closely matched as possible, coupling on both sides. Thus, on one side, there may be short, closely spaced segments (highly coupled), while on the other side, longer but less coupled segments, with the objective of achieving balance. Figure 2-59 shows the finalized layout submitted for BOIGU tape-out in B55X 7M. As for the previous case, the device was embedded twice to be able to reconstruct all its S-parameters matrix.

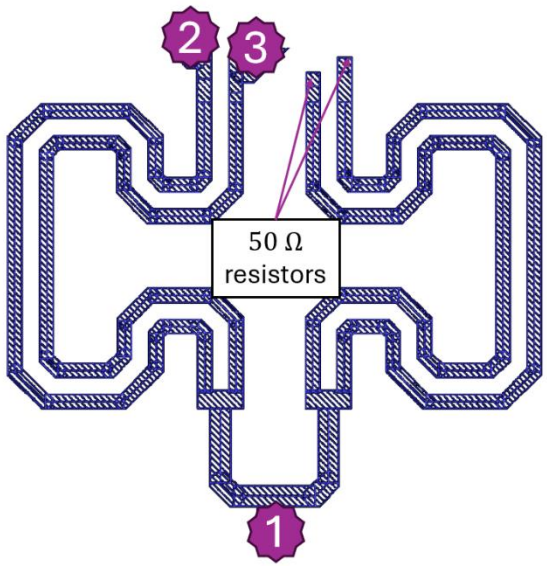


Figure 2-59: Layout view of the meandered power splitter embedded into BOIGU tape-out.

The effective area consumption of the device is $182x153\ \mu m$ compared the unfold case (with no possibility to connect isolation resistors) with a footprint of $600x80\ \mu m$. So, it's twice as small, and it

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adds the possibility of connecting the isolation resistors and not suffering from parasitic coupling because it was considered in the design optimization step. Results of simulation versus measurement of this device are shown in the Figure 2-60 for input RL and IL.

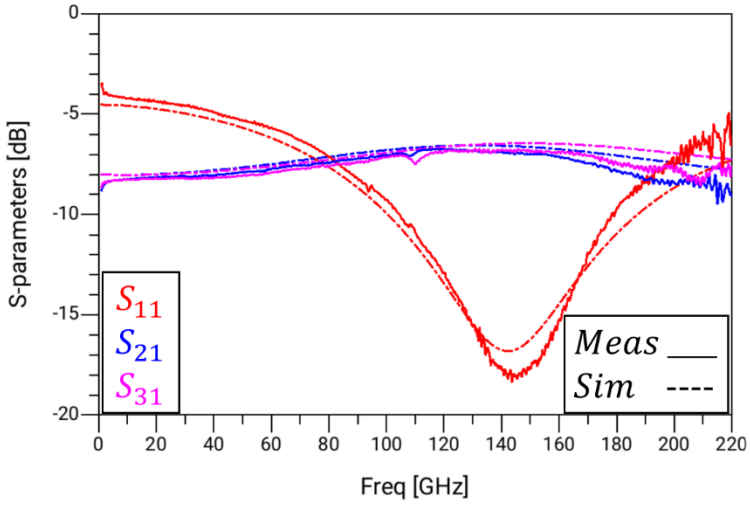


Figure 2-60: Simulation versus measurement results for the meandered power splitter embedded into BOIGU tape-out, showing input RL and IL for two output ports.

We can see very good agreement between simulation and measurement results. The device exhibits very low insertion losses on the order of $0.5\ dB$ on EM simulation and $0.8\ dB$ for measurement results, respectively, while showing similar amplitude level for transmission into the two output ports what shows that the device is balanced in terms of amplitude. Good return loss can be observed better than 17 dB for both simulation and measurement with comparable bandwidths. Also, from Figure 2-61 we can see that the device is perfectly balanced in terms of phase too.

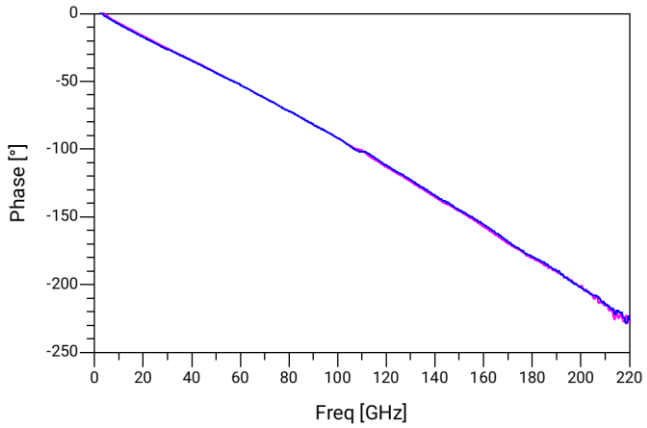


Figure 2-61: Measurement result of the phase of S_{21} and S_{31}, showing a perfect phase balance between the two outputs for the BOIGU tape-out power splitter.

Figure 2-62 shows input and output RL with isolation between the two output ports.

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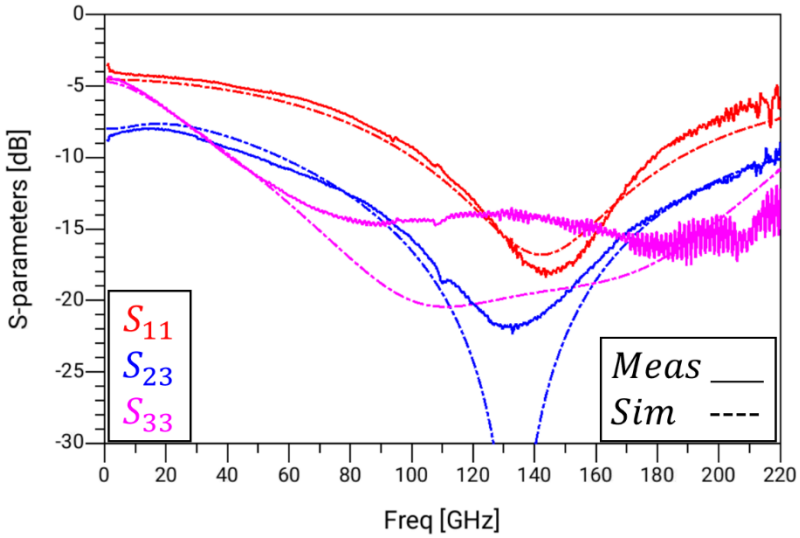


Figure 2-62: Simulation versus measurement results for the meandered power splitter embedded into BOIGU tape-out showing input and output RL and the isolation between the two output ports.

We can also see a good agreement between simulation and measurement results, with all isolation and RL better than $14\ dB$ in the whole band of interest. The measurement results combined with the device's small footprint, putting this device into the state of the art for 1-to-4 splitters integrated on silicon.

	T-junction	Cascaded Wilkinson	Coupled lines based	Proposed power combiner
Area	− −	− −	+ +	+ +
Insertion losses	− −	− −	+ +	+ +
Isolation	− −	+ +	±	+ +
Output return loss	− −	+ +	−	+ +
Design flow ⇔ theorical equations	+ +	+	− −	+ +

Table 2-3: recapitulative and comparative table between the three different power combiner topologies mentioned in the SOA subsection versus the proposed topology

As can be seen in Table 2-3, we were able to take the best from the state of art, address it's weakness and problematic by improving the performanc and developing theorical equations that leads to a comprehensive flow of design. Based on this, embedded measurement were carried out and confirmed the interest of this device, it's functionality and the developed theory behind.

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2.4 Conclusion

Preliminary studies of the simulators and the B55X 7ML technology stack enabled the thesis work to begin under favorable conditions. This allowed for an in-depth study of coupled line couplers, demonstrating their effectiveness and establishing them as essential building blocks for D-band design. The various simulation and measurement results confirm the accuracy of the EM deck and simulators used (Momentum and HFSS). The implementation and validation of certain core building blocks centered at 150 GHz were successful. These passive components exhibit very wide bandwidths and remarkable RF performance, notably low losses when properly optimized, confirming the trend toward designing distributed rather than lumped passive components in the D-band and at higher frequencies.

Among these functions, an innovative power splitter based on coupled lines was studied, and theoretical equations were developed based on even and odd mode decomposition. This enabled the development of a complete design flow applicable to any integrated or other technology. Building on these studies, several designs were fabricated and measured, some of which were detailed in this chapter. The measurement results confirm the value of these devices in terms of RF performance and footprint, with losses reduced by up to a factor of two and area reduced by up to six times. Furthermore, this confirms the potential for innovation and improvement in passive component design and the possibility to design a component that combines excellent RF performance with a reduced size.

With these distributed passive devices developed and studied, we now have the essential building blocks to design our power cells and, ultimately, our power amplifiers. This will be detailed in the following chapter.

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3. Power amplifiers

As discussed in the state-of-the-art chapter, when targeting the design of wideband D-band front-end modules (FEMs), one of the major challenges to be addressed is the generation of sufficient output power to compensate for the very high propagation losses in air. In addition, the limited values of f_T and $f_{\max}$ reduce the available gain, while the breakdown voltage constraints restrict both the achievable output power and the efficiency. These challenges have been highlighted in the state-of-the-art review and naturally lead to several research directions that will be addressed in this chapter. From a technology perspective, SiGe-based processes appear to offer the best trade-off between high-frequency performance, level of integration, and cost efficiency. Consequently, our work is based on the B55X SiGe BiCMOS technology from STMicroelectronics, which is among the most advanced SiGe platforms currently available.

In order to build on solid grounds, we first recall the foundry guidelines for sizing high-speed bipolar transistors and then investigate the different layout geometries available in the design kit. This device-level study forms the content of the first subsection.

Building on this preliminary analysis, we then focus on the design of a CB-based power stage, since the common-base topology has been identified in the state of the art as a very promising candidate for the last stage(s) of a PA. Its strengths and weaknesses will be analyzed in detail.

In a second step, we consider the design of a cascode driver stage, which addresses the lack of gain and provides excellent output–input isolation, thereby compensating for some of the intrinsic limitations of the CB topology. The cascode stage will thus be used as the driver and first stage of our PA.

Once these two building blocks are designed and characterized, they are combined to form a first two-stage PA, which is the subject of the next subsection.

Based on the challenges encountered with this initial implementation and on the lessons learned from the state-of-the-art study, further opportunities for improvement are identified, particularly in the design of the matching networks, the biasing scheme, and the DC-isolation strategy. The following subsection, therefore, introduces an enhanced two-stage PA architecture with a novel matching-network topology. In this version, the lossy and poorly suited coupling capacitors are removed and replaced by innovative matching networks based on coupled line structures, which are revisited and adapted to our specific needs. This second-generation PA is fabricated and characterized on-wafer, and a detailed comparison between simulation and measurement is presented.

Finally, the last part of the chapter is devoted to the design of a three-stage PA. This includes the sizing and design of the additional output stage, as well as the development of the associated matching networks required for its proper operation. The chapter concludes with a summary of the main results and perspectives.

3.1 Transistor sizing and layout geometry choice

To properly address the transistor sizing, we rely on the guidelines and trends reported in publication [25]. Figure 3-1 illustrates: (a) the simulated and measured cutoff frequency f_T as a function of the collector current for different transistor sizes, with a minimum emitter width of $0.2\ \mu$m and emitter lengths varying from 0.45 to $10\ \mu$m; and (b) the maximum oscillation frequency $f_{\max}$ as a function of I_C for different emitter lengths ranging from 1 to $10\ \mu$m.

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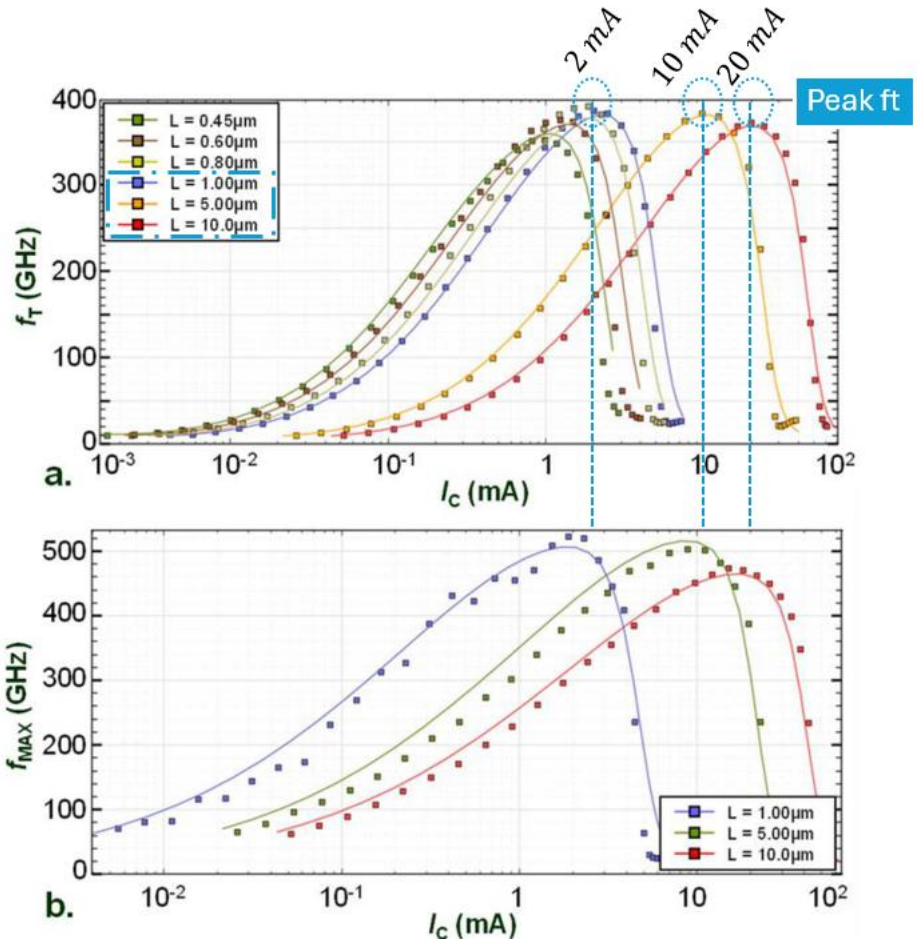


Figure 3-1: High-speed SiGe HBT (without DTI) f_T (a) and f_{MAX} (b) vs. I_C for different (drawn) emitter lengths (0.45 to 10 µm) at V_{CB} = 0.3 V and T=25°C: comparison between measurements (dots) and model (lines) [25].

From these results, it can be observed that, as the transistor size increases, a higher collector current is required to reach the maximum f_T. For example, for a device with an emitter area of $0.2 \times 1\ \mu\text{m}^2$, the "optimal" collector current—defined as the current at which both f_T and $f_{\max}$ are maximized—is around 2mA. For a $0.2 \times 5\ \mu\text{m}^2$ transistor, the optimal current increases to 10 mA, and for a $0.2 \times 10\ \mu\text{m}^2$ device, it reaches approximately 20 mA.

Beyond a certain emitter length, a reduction of the maximum achievable f_T is observed when further increasing the device size, mainly due to the growth of parasitic capacitances and resistances. However, a clear trend emerges that can be used as a design guideline and interpreted in terms of current density. In this case, the optimal current density is about $J_{\text{opt}} \approx 10\ \text{mA}/\mu\text{m}^2$. Since, in practice, the minimum emitter width $W_E = 0.2\ \mu\text{m}$ is usually chosen to reduce parasitics, this guideline can also be expressed as an optimal current per unit emitter length: $> \frac{I_C}{L_E} \approx 2\ \text{mA}/\mu\text{m}$. This relation will be used as a reference for the sizing of the PA transistors.

Another important aspect discussed in publication [25] is the impact of deep trench isolation (DTI), which is commonly employed for device isolation. Figure 3-2 shows the effect of DTI on the collector–substrate capacitance, which is found to increase in the presence of DTI, thereby degrading the high-frequency performance. According to the authors, there is ultimately no real benefit in using DTI for transistor isolation in this context. In addition, the confinement created by the DTI structures enhances self-heating, as illustrated in Figure 3-2, which plots the collector current as a function of the collector–emitter voltage. Overall, the use of DTI appears to offer no advantage and, in fact, mainly introduces drawbacks (increased parasitics and self-heating) for high-frequency PA design in this technology.

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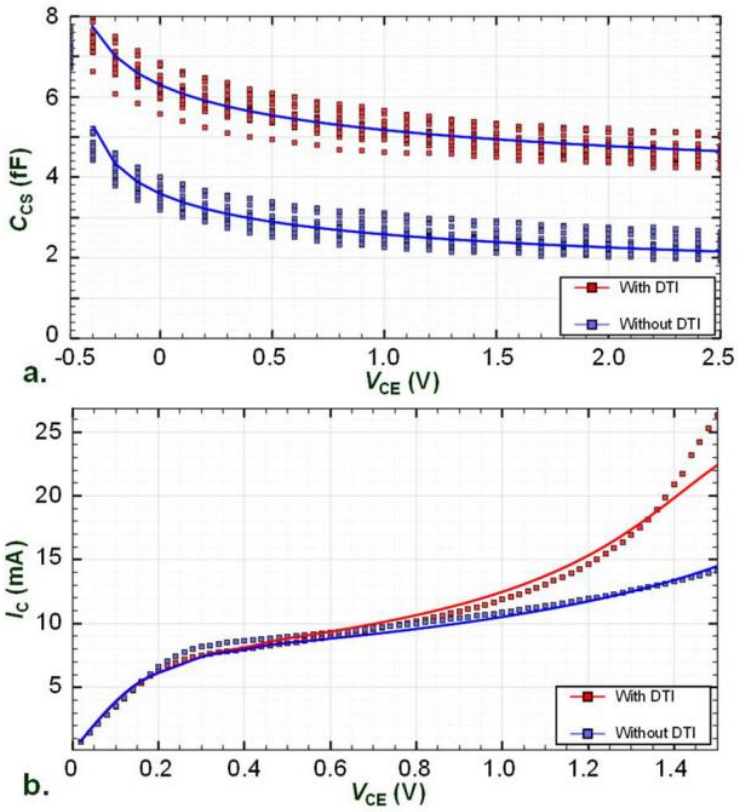


Figure 3-2: Evolution of C_{CS} (a) and I_C (b) vs V_{CE} for a 5 µm L_E (drawn) high-speed SiGe HBT with and without deep trenches (DTI). Dots are for measurements (multi wafers/lots) and lines are for the model. The dots of the I_C (VCE) graphs are median values from several wafers / lots [25].

In summary, a clear correlation is observed between the peak f_T and the transistor size: the maximum achievable f_T decreases as the device size increases. Consequently, small devices are preferable when the main objective is to maximize gain, whereas larger devices are required to deliver higher output power, at the expense of gain and up to a certain limit, as discussed in the state-of-the-art PA section.

Furthermore, to reach the peak f_T, it is preferable to bias the transistor such that the current density is on the order of $J_{\text{opt}} \approx 10$ mA/μm^2. Finally, the use of DTI no longer appears to be beneficial for transistor isolation, since STI alone is sufficient. In addition, DTI structures increase the collector–substrate capacitance C_{CS} and aggravate self-heating, which in turn limits the maximum allowable V_{CE}: excessive self-heating can dangerously increase the collector current.

With these basic guidelines in mind, the next step is to select the most appropriate layout geometry for the PA transistors. To this end, a short comparative study of the available options is carried out. Fig. X shows the layouts of the different geometry provided by the foundry in the design kit, namely (from left to right): CBE, CBEB, and $NX(\text{CBEB})\text{C}$. For simplicity, we consider here the case $N = 1$, which results in a CBEBC configuration.

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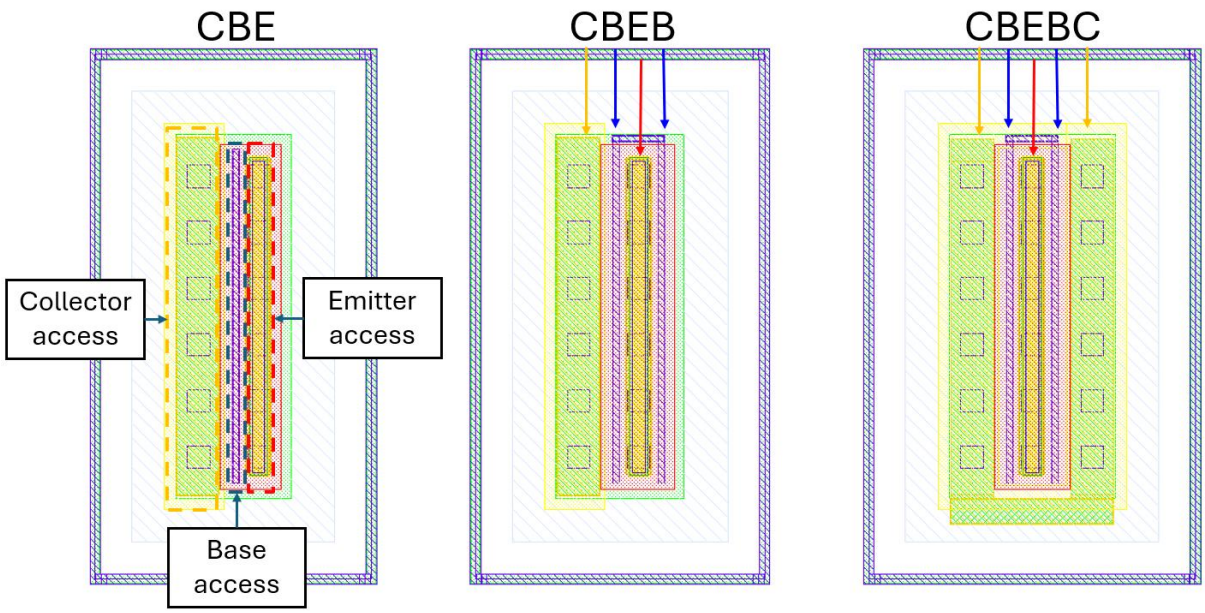


Figure 3-3: Layout view of the three transistor layout geometry available in the design kit, namely, from left to right: CBE, CBEB and CBEBC

Once these geometries are identified, they are compared in terms of their DC characteristics in common-emitter configuration, to determine which option is the most suitable for PA design. Figure 3-4 presents the collector-current characteristics $I_C(V_{CE})$ for the three layout geometries, for different base–emitter voltages V_{BE} ranging from $0.8\ V$ to 0.94 V with a step of 20 mV. These curves highlight the impact of the layout on the R_{on} , avalanche behavior and self-heating.

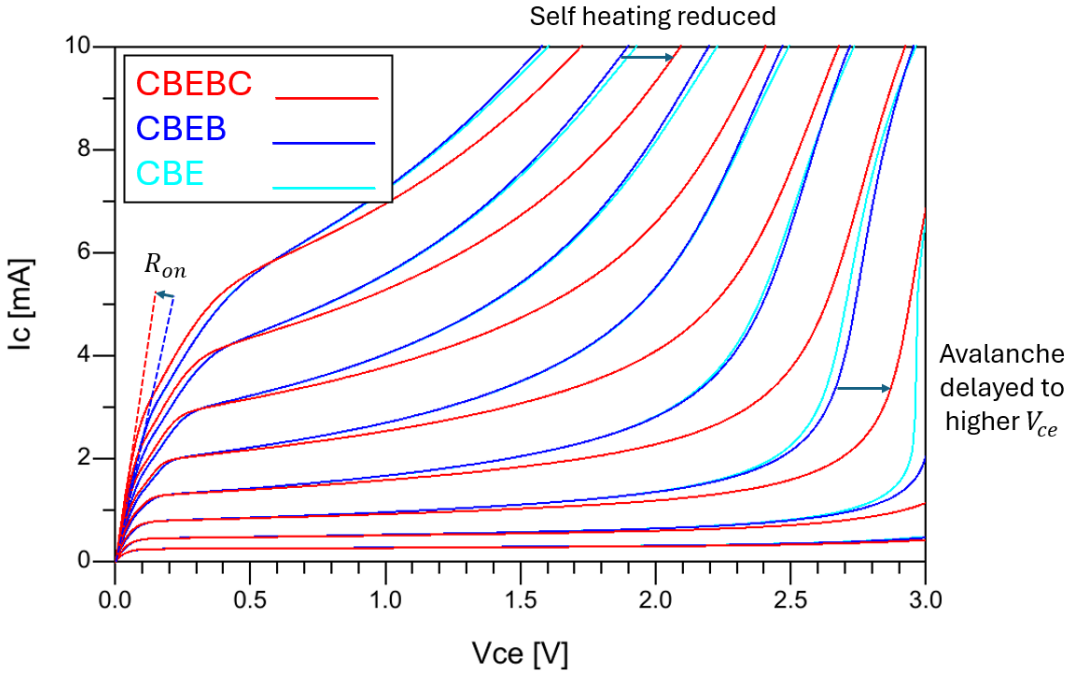


Figure 3-4: $I_C(V_{CE})$ for the three layout geometries, for different base–emitter voltages V_{BE} ranging from 0.8 to 0.94V with a step of 20mV

The three geometries exhibit similar qualitative behavior. However, the CBEBC geometry clearly shows a lower on-resistance R_{on} compared with the two other options, allowing the transistor to enter the conductive region at a lower V_{CE}. In addition, for high V_{BE} values (i.e., high I_C), the dominant destructive mechanism is self-heating, which manifests as a gradual increase of I_C with V_{CE}. From this point of view, the CBEBC topology exhibits a more favorable self-heating behavior, as can be seen in Figure 3-4.

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At higher V_{CE}, another destructive mechanism appears, namely avalanche breakdown, which is characterized by a very abrupt increase of I_C at the right-hand side of the curves. In terms of avalanche robustness, the CBEBC layout is again the most attractive option, as it shifts the onset of avalanche to higher voltages by a few hundred millivolts. For example, for $V_{BE} = 0.84$ V, the avalanche voltage is increased by about 0.2 V compared with the other layouts.

Improving R_{on} and pushing the avalanche limit to higher voltages makes it possible to achieve a larger voltage swing across the device, and therefore a higher output power and potentially a better efficiency, without further degrading the signal—in theory. Based on these observations, the CBEBC layout geometry appears to be the most attractive choice for PA design in this technology.

To conclude this subsection, several good practices and guidelines can be extracted. To optimize f_T and f_{MAX}, use an appropriate current density, on the order of $J_{\text{opt}} \approx 10$ mA/μm^2. Then, avoid using DTI for transistor isolation, since STI is sufficient, and DTI degrades C_{CS} and self-heating. Finally, for the layout geometry choice, select the CBEBC layout geometry to benefit from lower R_{on}, improved avalanche robustness and better high-voltage operation which results in a potential higher voltage swing. The detailed transistor sizing will then be performed on a case-by-case basis, depending on the targeted output power, gain, or a trade-off between both.

3.2 Study and design of power stage with CB topology

3.2.1 CB topology study

Before addressing the design of the power stage, a preliminary study of the common-base (CB) topology is required. This analysis is based on the work of Mazzanti [44] where the author presents a comparative study between common-emitter (CE) and common-base topologies for the same total emitter area.

In CE configuration, the impedance presented at the base can be either high or low. If the device is driven by a base current I_B, as illustrated in Figure 3-4(a), the effect of self-heating appears as a negative slope of the I_C–V_{CE} curves, corresponding to a negative thermal feedback. In this configuration, the output power is limited by the avalanche breakdown voltage, which in the example is around 1.5V and corresponds to BV_{CEO} (i.e., for an open-base condition). The maximum achievable voltage swing is then about 550mV. According to the authors, and assuming lossless matching networks, the expected output power at the 1dB compression point is $P_{1\text{dB}} \approx 9.3$dBm, with a saturated output power $P_{\text{sat}} \approx 11.5$ dBm.

If, instead, the transistor is voltage-driven at the base (constant V_{BE}), the breakdown voltage is significantly increased at low collector currents, and values well above BV_{CEO} can be reached, thereby enabling a much larger voltage swing. However, in a D-band linear PA the transistor typically operates at simultaneously high V_{CE} and high I_C. As shown in Figure 3-4(b), in this region self-heating leads to positive thermal feedback and causes a sharp increase of I_C. One of the main limitations to achieving a high P_{sat} in CE configuration thus becomes the thermal breakdown, since the bias current must be reduced to avoid thermal runaway. Under the same assumptions as in the previous case, the authors reports an expected $P_{1\text{dB}} \approx 10.8$ dBm and $P_{\text{sat}} \approx 13.6$ dBm, i.e., a moderate improvement compared with the current-driven CE case. In both CE cases, the significant gap between $P_{1\text{dB}}$ and P_{sat} is attributed to the signal-dependent variation of the I_C slope and to the smooth transition from the off-state to the active region, characterized by a knee voltage $V_{knee} = 0.4 - 0.5$ V (minimum voltage required to move from the cut-off to the active region).

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In contrast, the CB configuration, illustrated in Figure 3-4(c), exhibits much more remarkable performance. The low impedance presented at the base drastically increases the breakdown voltage up to BV_{CBO}, while at the same time improving the thermal stability. The resulting I_C–V_{CE} curves become almost flat, i.e., nearly independent of V_{CE}, and the transition from the off-state to the active region occurs more abruptly, with a reduced knee voltage $V_{\text{knee}} \approx 0.2$ V. These two improvements—a lower V_{knee}, allowing the device to enter the active region earlier, and a higher breakdown voltage—enable a much larger voltage swing at the output. Under the same operating conditions as in the CE cases (a) and (b), the authors reports an expected $P_{1\text{dB}} \approx 15.6$ dBm and $P_{\text{sat}} \approx 16.6$ dBm, which is a substantial increase in output power.

According to the authors, the CB configuration enables a larger voltage swing and therefore higher achievable output power, while presenting output impedances that are easier to match. As a result, the required impedance transformation ratio is reduced, which in turn helps to limit the losses in the matching networks. In summary, the desirable transistor features for CB operation, as highlighted by the authors, are: a high breakdown voltage and a low knee voltage V_{knee}, so a minimum voltage drop to enter the active region. What gives a bigger voltage swing. And on the other hand, a flat output characteristic (minimal dependence of I_C on V_{CE} in the active region),

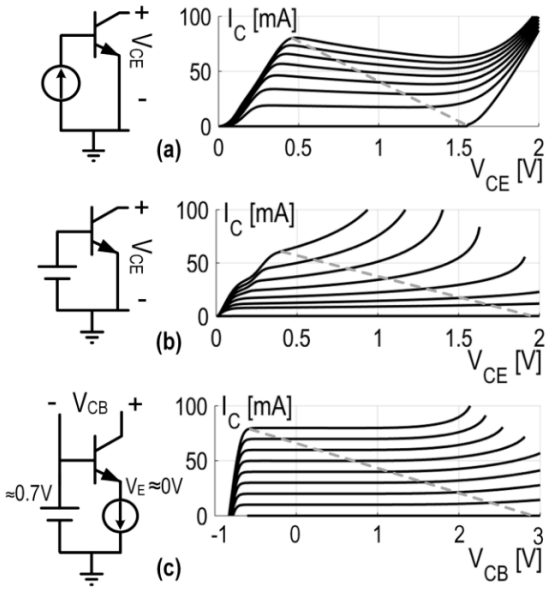


Figure 3-5: I–V curves for the same transistor in different configurations [44].

The authors then discusses current clamping, which is one of the major advantages of the CB topology. The concept is inspired by a diode voltage-clamping circuit, shown in Figure 3-5, which reproduces the input signal at the output, but clamped to ground, while adding a DC voltage equal to the input peak amplitude.

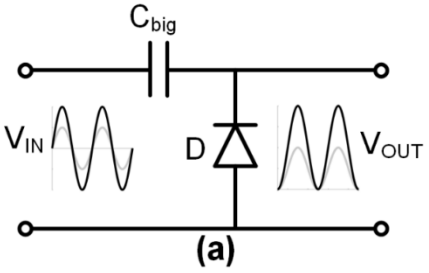


Figure 3-6 : Diode voltage-mode clamping from [44].

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The corresponding current-mode diode-clamping circuit, shown in Figure 3-7, is derived from the voltage-mode version.

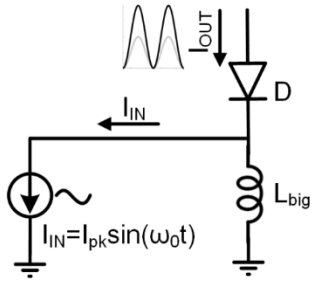


Figure 3-7: Diode current-mode clamping from [44].

This transformation is achieved by replacing the series capacitor with a shunt inductor and by considering the diode current instead of the voltage across the diode. The same concept is then exploited by the authors in the CB topology, as illustrated in Figure 3-8, in order to implement current clamping in a common-base power stage.

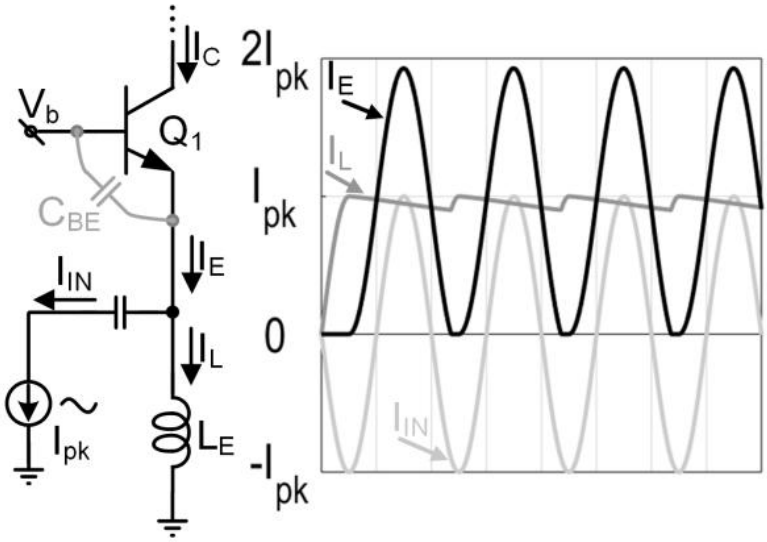


Figure 3-8: Current clamping in CB stage and current waveforms [44]..

The diode and the inductor L_{big} shown in Figure 3-7 represent, respectively, the base–emitter junction of the CB transistor Q_1 and the emitter inductor L_E shown in Figure 3-8. Assuming $C_{BE} = 0\ F$ and a sufficiently low bias voltage (low quiescent current) for Q_1, the transistor remains off during the first half of the negative cycle of the input current I_{in}, while the inductor current I_L is charged up to the peak value I_{pk}. After this transient, the DC current in Q_1 and L_E becomes equal to I_{pk}. When Q_1 turns on, the instantaneous emitter current is then: $I_E(t) = I_{pk} + I_{in}(t)$. If L_E were infinite, Q_1 would never switch off and would effectively operate in class-A mode. If, instead, L_E is large but finite, the inductor is partially discharged through the emitter resistor and Q_1 turns off for a short period of time, which allows the inductor current to be recharged again up to I_{pk}. As a result, the average collector current of the CB stage follows the envelope of the input signal, similarly to a class-B CE stage. In other words, this mechanism implements an intrinsic form of proportional biasing behavior, which can improve the PAE, especially for signals with a varying envelope.

The author's objective, as in the original work, is to exploit this current-clamping concept at very high frequencies, where the effect of C_{BE} becomes increasingly important. When the CB transistor is off, the base–emitter capacitance C_{BE} absorbs part of the input signal, which slows down the charging of I_L,

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as illustrated in Figure 3-9 for different values of L_E normalized to L_0, where L_0 is the inductance value that resonates with C_{BE} at 80 GHz.

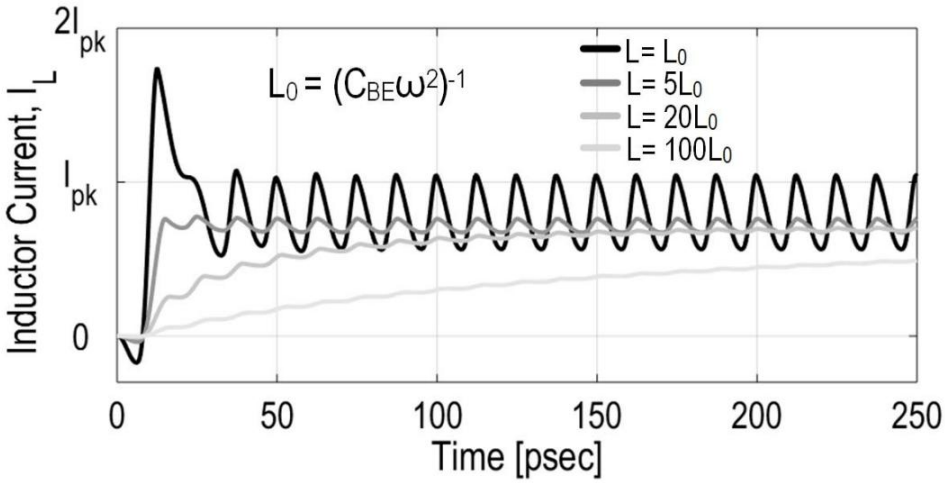


Figure 3-9: Inductor current for the circuit shown in Figure 3-8 versus time when input frequency is 80 GHz, at different values of L_E from [44].

As can be seen, the charging of I_L follows an approximately exponential-like behavior. By reducing the value of L_E down to $L_E = L_0$, the charging time is reduced, and the current reaches its steady-state value almost instantaneously; however, the ripple of I_L increases, while its average value remains almost unchanged. Comparing this case to Figure 3-8, one can observe that I_L stabilizes at a value lower than I_{pk}; thus, one effect of C_{BE} is to reduce the average DC current. In the scenario studied by the authors, the average current can drop to about $0.8 \cdot I_{pk}$, which means that the CB transistor effectively operates closer to class-AB, with a conduction angle smaller than $360\,°$. This behavior is again due to the presence of C_{BE}, which keeps the transistor in the off-state for a longer portion of the RF period. Conversely, if L_E is increased significantly, the ripple on I_L is reduced, but the time required for I_L to reach its steady-state value becomes longer. In other words, a very large L_E slows down the proportional biasing capability of the stage, which is not desirable for a PA driven by amplitude-modulated signals. As a consequence, a trade-off must be found for the choice of L_E:

- A smaller L_E improves the proportional biasing speed but increases the ripple of the inductor current.
- A larger L_E reduces the ripple but degrades the dynamic response and proportional biasing behavior.

The design of L_E in our CB power stage will therefore be based on this compromise between ripple reduction and response time of I_L a parametrique study will be then done to optimize this value for our design.

3.2.2 Design of the CB power stage

The sizing of the first transistor and its corresponding bias conditions is initially carried out using ideal circuit elements, in order to study the intrinsic behavior of the device and to tune the value of the current-clamping inductance. Multiple design iterations were carried out with different emitter lengths. Increasing the emitter length initially improved the achievable output power, up to a point where the transistor parasitics became too dominant and started to degrade the performance confirming the same behavior as in Figure 1-22. For the first version of the power stage, we therefore selected an emitter length

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of $L_{Emitter} = 30\ \mu m$ for a collector's bias voltage of $V_c = 2.2\ V$ and a base bias voltage of $V_b = 820\ mV$. These bias voltages were chosen to remain sufficiently low, as recommended in [44].

Then a PLS extraction is performed, providing the parasitic capacitances between each terminal and the series resistances of the different access lines. These parasitics are then incorporated into the schematic. At this stage, the circuit representation is already significantly closer to the actual implementation.

The next step consists in selecting the load for the power cell. To this end, a large-signal load-pull simulation is performed to determine the optimal load impedance Z_{opt} that maximizes the output power while maintaining an acceptable PAE. Once Z_{opt} is identified, an output matching network is designed, based on transmission lines and capacitors, to transform Z_{opt} to the external $50\ \Omega$ reference, explicitly taking into account the parasitic effects of the RF pads. Figure 3-10 shows the simplified schematic of the µstrip lines based matching network. After validating the large-signal behavior with this output network, an S-parameter simulation is run to extract the input impedance seen at the transistor input. An input matching network is then synthesized based on line stub topology as in [44] to match this input impedance to $50\ \Omega$, again including the pad impedance in the design.

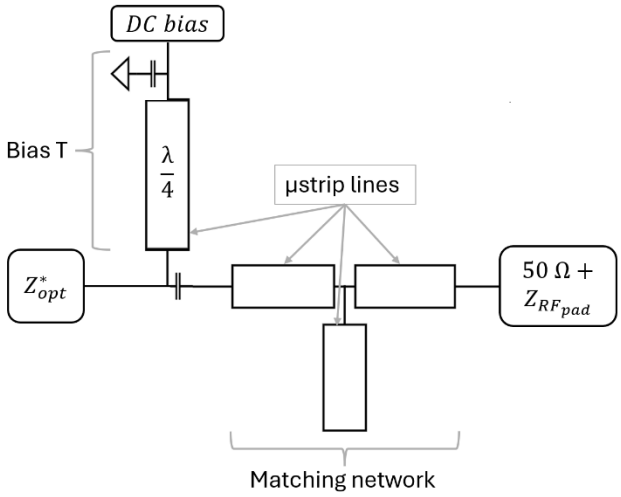
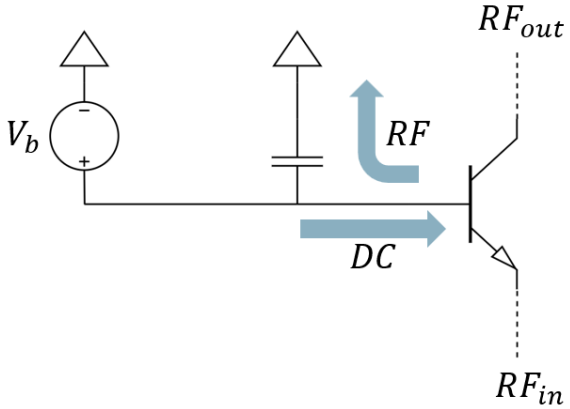


Figure 3-10: simplified schematic of the µstrip lines based matching network with the bias T.

Once the passive bricks (matching networks, bias networks, etc.) are sized and EM-simulated, a more accurate co-simulation is performed combining both the PLS-extracted parasitics and the EM-modeled passives. During the final layout phase, several challenges were encountered, mainly related to routing. The most critical one concerns the base access: in the CB topology used here, the base must be connected to several parallel decoupling capacitors shorted to ground, and then routed to the measurement pads, as illustrated in Figure 3-11.



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Figure 3-11: Simplified schematic of the CB base's rooting.

The base-decoupling capacitance must be sufficiently large and placed as close as possible to the transistor in order to reduce parasitic effects that could degrade the performance or even compromise the correct operation of the device. On the other hand, in our layout the base access is routed on the same side as the emitter access carrying the RF signal on M7, which may lead to parasitic coupling between the RF path and the base-bias line—an effect that we want to minimize. We take advantage of an additional feature of our passives design: the presence of a ground plane on M5Z. This allows us to implement the RF input matching network on M7V with M5Z as its reference ground plane, while routing the base-bias access from M1 to M4 underneath, benefiting from the M5Z ground as an EM shield between the RF signal and the DC-bias network, as illustrated in Figure 3-12.

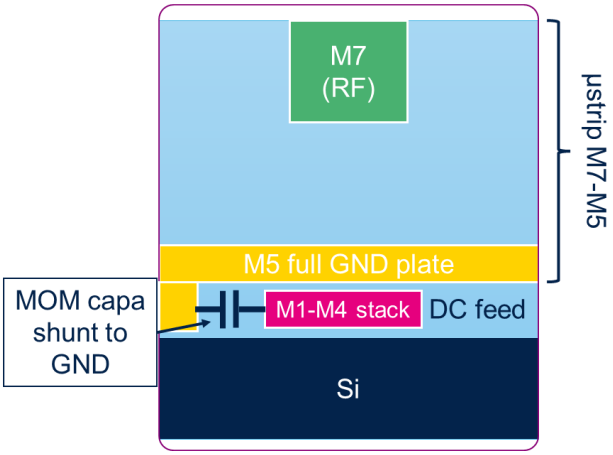
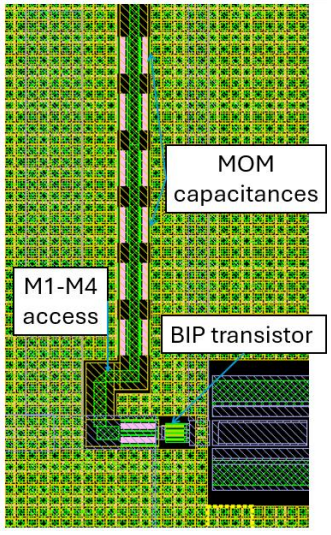


Figure 3-12: Cross-section view of the RF and base-bias routing

Figure 3-12 shows a cross-section of the metal stack where the RF input signal (RF_in) is routed on M7V over the M5Z ground plane, while the base DC-feed is implemented as a metal stack from M1 to M4, with decoupling capacitors connected to ground.

Once this strategy is defined, small MOM capacitors provided by the design kit, with a nominal value of about 50fF (chosen sufficiently small to ease placement and routing), are connected in cascade on both sides of the M1–M4 transmission-line stack. These capacitors are tied to the M5Z ground plane, as shown in Figure 3-13, in order to shunt the RF component at the base to ground and strongly reduce the RF coupling between the base-bias routing and the RF input path on M7V.



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Figure 3-13: Layout view of the base-bias network, where the M1–M4 metal stack used for the base access is connected on both sides to the MOM decoupling capacitors tied to the M5Z ground plane.

The collector is biased using a classical bias-T structure, implemented with a $\lambda/4$ transmission line. Once all elements have been designed brick by brick, the final layout is assembled, this time strictly complying with the foundry design constraints, i.e., the design rules (DR). A final design rule check (DRC) is then performed. Several rules must be validated; thanks to the experience acquired during the design of passive structures, most of the critical issues were already known, in particular those related to metal density. The main novelty and difficulty here is the high metal density required around the MOM capacitors. After DRC, the correctness of the routing is verified using the net-tracer tool. This tool allows short circuits and open circuits to be detected directly on the layout in a very efficient way. Figure 3-14 shows the final layout after verification with net tracer: the input matching network is highlighted in blue, the output matching network in purple, the base-bias supply in red, and the collector-bias supply in orange. The total area occupied by the device with RF and DC pads included is $530X720\ \mu m^2$.

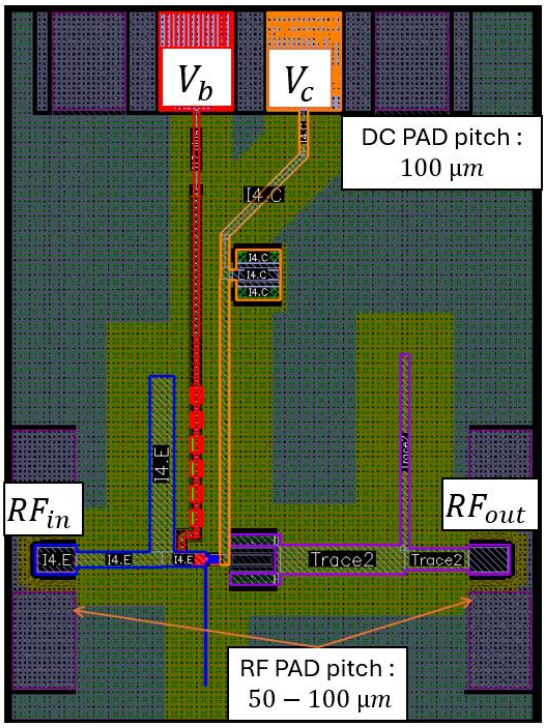


Figure 3-14: final layout of the CB power stage after verification with net tracer

After assembling the full circuit, a first set of block-by-block simulations is performed using the GoldenGate simulator. The resulting S-parameters of the circuit are reported in Figure 3-15.

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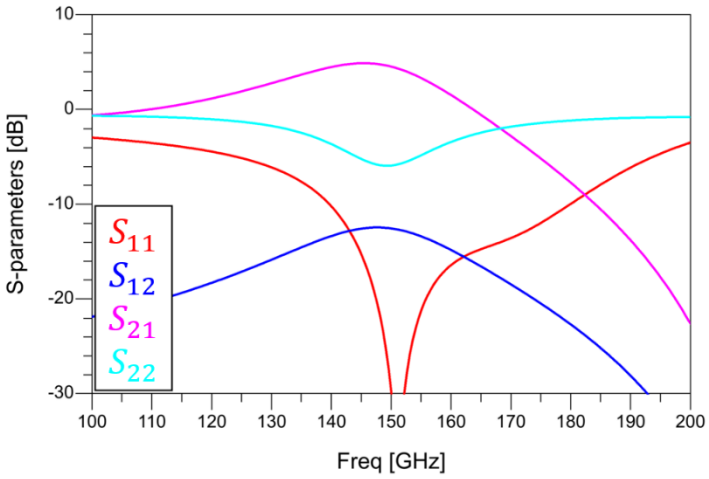


Figure 3-15: Simulated S-parameters for the power stage based on CB topology

Thanks to the line-and-stub topology combined with a custom plate capacitor, a very good input matching better than 30 dB is achieved. The small-signal gain S_{21} is higher than 4 dB at the center frequency. Although this value is relatively low due to the passive losses, the high operating frequency and the intrinsic device parasitics, it remains acceptable for a unit power stage. The output matching is intentionally not optimized in small signal, since the objective is to present the optimal large-signal load to the power cell in order to maximize the delivered output power rather than to minimize S_{22}. Finally, the reverse isolation between output and input is better than 12 dB over the whole band. This level is acceptable but not outstanding and is mainly limited by capacitive coupling, which represents one of the weak points of this topology. To better assess the large-signal behavior of the cell, a large-signal simulation is performed on the same simulator.

Figure 3-16 reports the simulated input power P_{in} at port 1, the output power P_{out} at port 2 (both in dBm), and the power gain (in dB) as a function of the input power

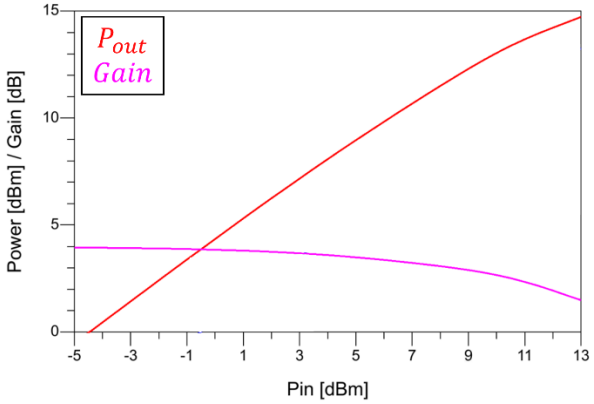


Figure 3-16: Large signal simulation result showing P_{in} and P_{out} (both in dBm) and the power Gain (in dB) as a function of the input power

The small-signal gain of about 4dB is recovered at $P_{\text{in}} = -5$ dBm. The 1dB compression point is obtained by reading on the gain curve the output power for which the gain drops from 4 to 3 dB, yielding: $P_{1\text{dB}} \approx 12$ dBm, which is a very good result for a unit cell. To verify the proportional biasing capability, the DC power consumption is plotted versus the RF input power, as shown in Figure 3-17.

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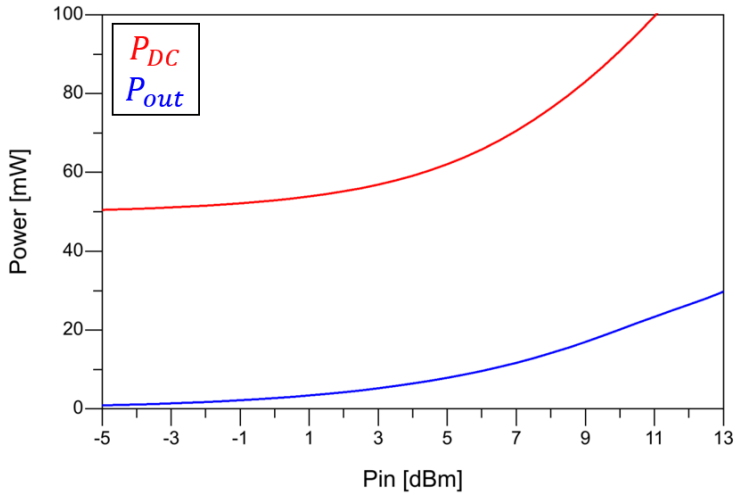


Figure 3-17: Output power P_{out} and the DC power P_{DC}, both expressed in mW, as a function of the input power [dBm]

It can be observed that the DC consumption scales with the input power and thus follows the output power, which confirms one of the expected advantages of the CB topology (proportional biasing behavior) with current clamping. The corresponding PAE versus input power is presented in Figure 3-18.

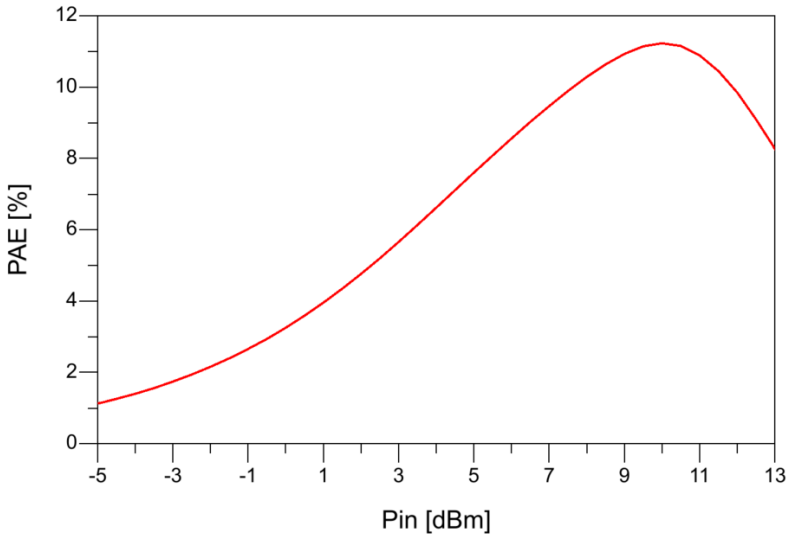


Figure 3-18: PAE [%] vs input power [dBm]

The circuit exhibits a very good maximum PAE, higher than $11\,\%$, while the PAE at the 1dB compression point remains close to this maximum value (around $11\,\%$). In addition, for a 6dB output back-off, the PAE is still better than $5.5\,\%$, which is an excellent result. This behavior stems from the fact that the DC consumption scales with the injected RF power at the input, leading not only to a high peak PAE, but also to a very good efficiency maintained over several dB of back-off. This is particularly advantageous for amplitude-modulated signals.

Table 3-1 resume the performances of this design simulated versus the state of art presented earlier.

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Ref	Topology	SiGe Techno	f_t/f_{max} (GHz)	BV_{CEO} (V)	Frequency (GHz)	Gain (dB)	P_{sat} (dBm)	P_{1dB} (dBm)	$PAE\ @\ P_{1dB}$ (%)	Area (mm^2)
[19]	Single 2 stage cascode	IHP's 130 nm	300/500	1.7	125-146	18.2	15	11	5	0.46
[20]	Differential 2 stage cascode	? 130 nm	?	?	109-119	18.5	11.8	9	<4	0.35
[21]	Balanced 3 stage cascode	IBM's 120 nm	200/250	?	112-128	25.5	17.5	13.3	<3	?
[22]	Single 4 stage CB	ST B55 55 nm	325/375	1.5	125-159	24	17.6	16.8	17.1	0.18
[24]	4-way parallel 2 stage cascode	IBM's 90 nm	300/360	1.7	110-145	18.2	21.9	18.6	9	1.7
This work	Single 1 stage CB	ST B55X 55 nm	325/375	1.5	125-158	4*	15.5*	12*	11*	0.38

Table 3-1: State of art power amplifiers vs proposed one, comparing: their topologies, performance metrics, and technology.

As can be seen, the proposed PA provides a relatively small gain, especially compared with the other reported solutions, with only 4dB. However, in terms of output power capability, it achieves a $P_{1\text{dB}}$ and a P_{sat} that are better than those reported in [19] and [20], with values of 12 dBm and 15.5 dBm, respectively. It also provides a PAE that is better than all the other reported designs, except for the CB-based solution in [22].

The area of this power cell is 0.38mm^2, which can be considered small compared with the state of the art. However, it is important to note that no effort was devoted to meandering or further reducing the footprint of this device. Our objective here is to demonstrate feasibility, while the possibility of significantly reducing the area through meandered lines was already demonstrated in the passive-device section. we aren't even close for the state of art but this first draw confirms in simulation the feasibility of the PA design.

These results confirm the interest of the common-base topology as a very good candidate for the last one (or few) stages of a PA, especially in terms of output power capability and back-off efficiency, despite its two main drawbacks: limited isolation between output and input and relatively low gain. A topology that performs very well on these two aspects is the cascode. Which, according to the state of the art, offers the best trade-off between high gain and excellent reverse isolation. The analysis and design of the cascode stage, intended as a driver stage for the PA, will therefore be the subject of the next chapter.

3.3 Design of the driver stage based on cascode topology

Once the first CB-based power cell is completed, several weaknesses become evident, such as the limited reverse isolation S_{12} and the relatively low gain of this topology. We therefore propose to design a driver cell based on the cascode topology, which is known to provide the highest gain among the three considered topologies, together with good output–input isolation. As a result, this cascode driver is expected to compensate for some of the shortcomings of the common-base power stage.

For this design, we use the same transistor geometry, with an emitter length of $10\ \mu$m, which is smaller than that of the power stage. By reducing the device size, a higher gain is expected, at the cost of a lower maximum output power. Once the device size is fixed, the biasing is chosen such that the same voltage drop is applied across the two transistors of the cascode: $> V_{B2} = V_{B1} + \frac{V_{CC}}{2}$, where V_{B1} biases the cascode's common-emitter and V_{B2} biases the base of the cascode's common-base. To boost the gain, relatively high bias voltages are selected, namely $V_{B1} = 0.89$ V and $V_{B2} = 2.14$ V for a supply voltage $V_{CC} = 2.5$ V. The same design steps as for the CB power cell are then followed. A large-signal

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load-pull simulation is first performed to identify the optimal load impedance Z_{opt}. In our case, the maximum output power is obtained for $Z_{opt} \approx 40 - j40\ \Omega$, while a very attractive gain–power trade-off is observed for a purely real load of $50\ \Omega$. This is particularly interesting, since it removes the need for an output matching network, which both reduces losses and simplifies the design of this stand-alone driver cell. The input matching is designed in a similar way as before. The same type of input coupling capacitor is used, explicitly including the pad parasitics. With a line/open-stub/line topology, the input impedance seen by the transistor can be matched to $50\ \Omega$. The bias-T structures developed previously are reused, which speeds up the design. A simplified schematic of the cascode-based driver stage is shown in Figure 3-19.

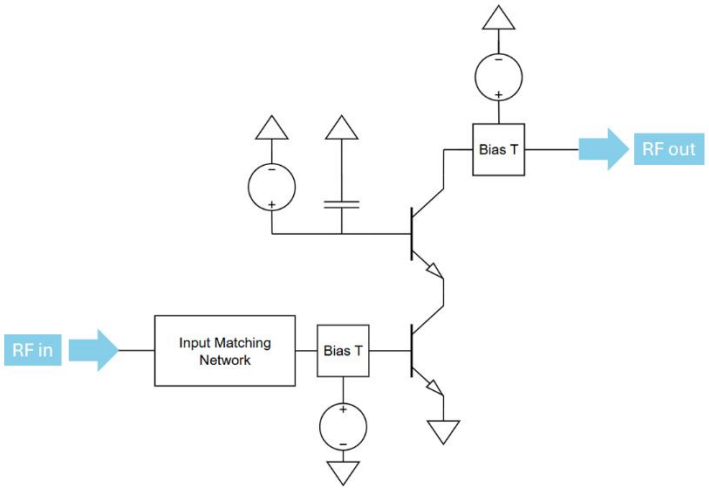


Figure 3-19: Simplified schematic of the cascode-based driver stage.

After PLS extraction and EM simulation of the input matching network, as well as EM verification of the bias-T. A final layout for simulation can be done, that is occupying an area of $610X985\ \mu m^2$, RF and DC pads included, the layout is shown in Figure 3-20.

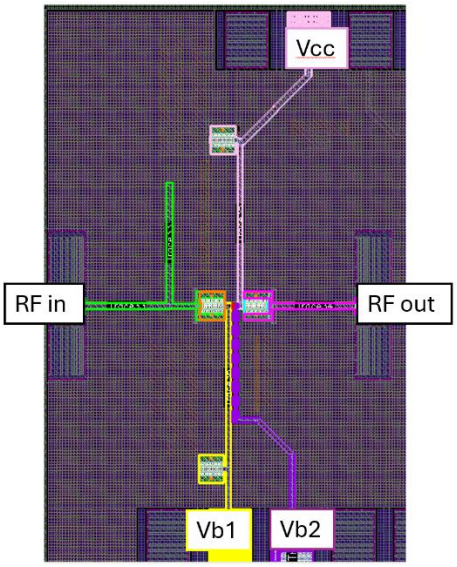


Figure 3-20: Layout view of the driver cell based on cascode topology

Then a full small-signal simulation is carried out with all bricks connected. The resulting S-parameters are reported in Figure 3-21.

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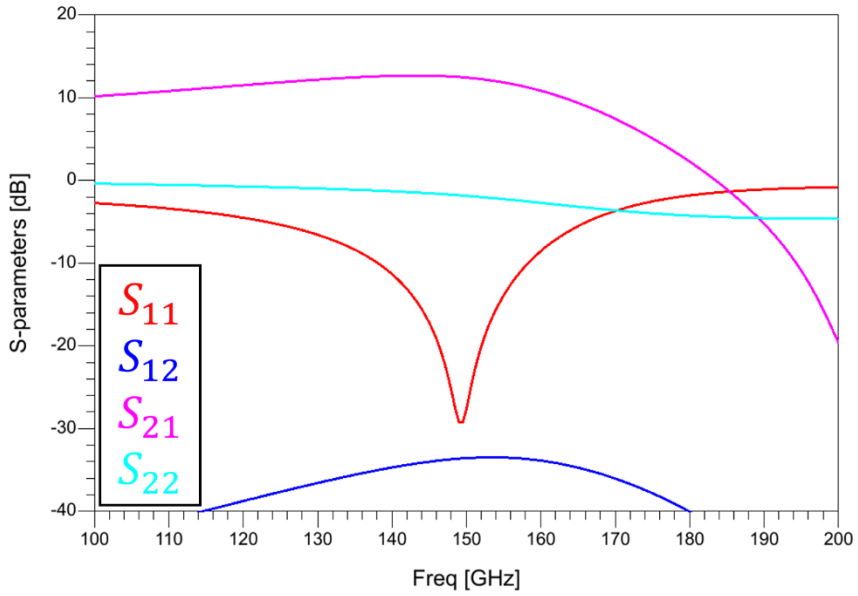


Figure 3-21: Small-signal simulation results of the cascode-based driver.

The simulated small-signal results are very encouraging for D-band operation. The circuit is correctly centered around 150 GHz, as evidenced by the input return-loss resonance at this frequency, with a minimum value close to 30 dB, indicating an excellent input match. The output return loss is not particularly good in small signal, which is expected since the output load has been chosen from a large-signal load-pull optimization rather than from a small-signal matching perspective. In our case, the priority is to generate sufficient output power from the driver stage to saturate the following power stage, rather than to maximize small-signal S_{22}. The maximum small-signal gain reaches about 13 dB, with a 3dB bandwidth extending from roughly 100 to 165 GHz, which is excellent and significantly better than what was obtained with the CB-based cell alone. Finally, the driver exhibits excellent reverse isolation, with S_{12} remaining well below -30 dB over the entire simulated band. These results confirm that the cascode provides much better output–input isolation and a higher gain in the selected technology, which supports our overall design strategy.

However, the ultimate goal of a PA is to deliver output power. We therefore evaluate the large-signal performance of the cascode driver by means of a large-signal simulation using GoldenGate. The corresponding input/output power characteristics and gain are reported in Figure 3-22.

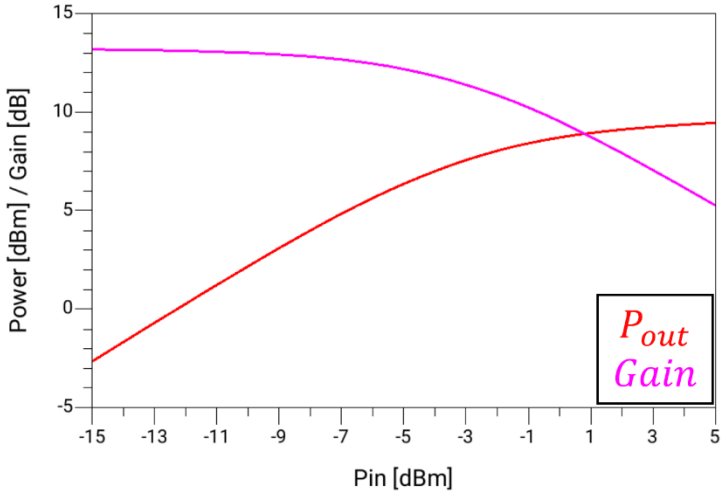


Figure 3-22: Large-signal simulation results of the cascode-based driver

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Large-signal simulations are performed for an input power sweep from -15 to 5 dBm. The simulated gain (pink curve) confirms the small-signal result, with approximately 13 dB gain at low input power. The 1dB compression point is reached for $P_{\text{in}} = -5$dBm, corresponding to an output power $> P_{1\text{dB}} \approx 6.4$ dBm, while the saturated output power is close to $> P_{\text{sat}} \approx 9.5$ dBm. Which is satisfying for a driver stage, but on another hand the difference between $P_{1\text{dB}}$ and P_{sat} doesn't show a sharp compression profile as seen for the CB topology. The PAE as a function of input power is reported in Figure 3-23.

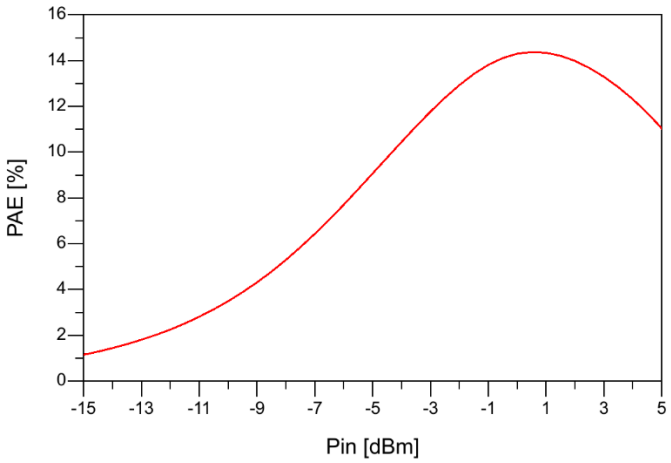


Figure 3-23: PAE of the cascode driver vs. input power

The PAE reaches its maximum for $P_{\text{in}} \approx 0.5$ dBm, with a peak value of about 14.4 %. This value must be interpreted with care, since the driver is already in compression in this operating region. The PAE at the 1dB compression point is approximately 9 %, which remains a very good result. However, for a 6dB back-off in input power, the PAE drops to about 2.8 %, i.e., roughly one third of the PAE at $P_{1\text{dB}}$. This behavior contrasts with that of the common-base stage with current clamping, for which the PAE at 6dB back-off remains close to half of the PAE at $P_{1\text{dB}}$. Table 3-2 present a comparison between state of art power amplifiers versus proposed ones.

Ref	Topology	SiGe Techno	f_t/f_{max} (GHz)	BV_{CEO} (V)	Frequency (GHz)	Gain (dB)	P_{sat} (dBm)	P_{1dB} (dBm)	$PAE\ @\ P_{1dB}$ (%)	Area (mm^2)
[19]	Single 2 stage cascode	IHP's 130 nm	300/500	1.7	125-146	18.2	15	11	5	0.46
[20]	Differential 2 stage cascode	? 130 nm	?	?	109-119	18.5	11.8	9	<4	0.35
[21]	Balanced 3 stage cascode	IBM's 120 nm	200/250	?	112-128	25.5	17.5	13.3	<3	?
[22]	Single 4 stage CB	ST B55 55 nm	325/375	1.5	125-159	24	17.6	16.8	17.1	0.18
[24]	4-way parallel 2 stage cascode	IBM's 90 nm	300/360	1.7	110-145	18.2	21.9	18.6	9	1.7
This work	Single 1 stage CB	ST B55X 55 nm	325/375	1.5	125-158	4*	15.5*	12*	11*	0.38
This work	Single 1 stage cascode	ST B55X 55 nm	380/475	1.5	100-165	13*	9.5*	6.4*	9*	0.6

Table 3-2: State of art power amplifiers vs proposed ones, comparing: their topologies, performance metrics, and technology.

In summary, the cascode unit cell offers superior performance in terms of gain and output–input isolation, but exhibits lower output power and a less favorable PAE, especially at back-off, compared with the CB stage with current clamping. With a gain of 13 dB, a $P_{1\text{dB}}$ of 6.4 dBm, and a PAE of about 9 % at $P_{1\text{dB}}$, this simple unit cascode cell nonetheless confirms the feasibility of D-band PA design in the chosen technology. The next step is therefore to combine the two topologies, which appear highly compatible and complementary, in such a way that each one compensates for the weaknesses of the other. The objective is to implement a multi-stage PA that provides sufficient gain and strong output–input

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isolation (thanks to the cascode driver), while simultaneously delivering high output power, a sharp gain-compression profile, and a favorable efficiency profile, particularly at several dB of output back-off, in order to efficiently handle variable-envelope input signals (thanks to the CB power stage). And this will be the subject of the following sub-sections.

3.4 2 stage power amplifier with line-stub MN

After designing the two unit cells, namely the cascode and the common-base (CB) stages, their respective strengths and weaknesses become clear. The most suitable strategy appears to be to exploit the high gain and good isolation of the cascode stage by using it as the first stage of the PA, and then to employ the CB topology in the power stages to deliver higher output power with improved control of the power consumption and a more favorable linearity profile.

This is precisely the approach adopted in this subsection. The CB stage is resized such that it can be driven into saturation by the maximum output power that can be delivered by the cascode stage what gives an emmiter length of 18 µm for the CB and 10 µm for the cascode. The same transistor routing is reused. A new post-layout extraction (PLS) is then performed, followed by a load-pull simulation. This simulation gave a result of $Z_{opt} = 10 + j30\ \Omega$ for the last stage thus need to be presented instead of $50\ \Omega$ at the output, knowing that the input impedance of the last stage is $Z_in = 5 + j2\ \Omega$. At the end of this design flow, the transistor cells are fully fixed, together with their optimal output impedances and input impedances. The matching network design process starts from the output matching network of the last stage and proceeds backward toward the input, i.e., from right to left. A simplified schematic of the resulting architecture is shown in Figure 3-24.

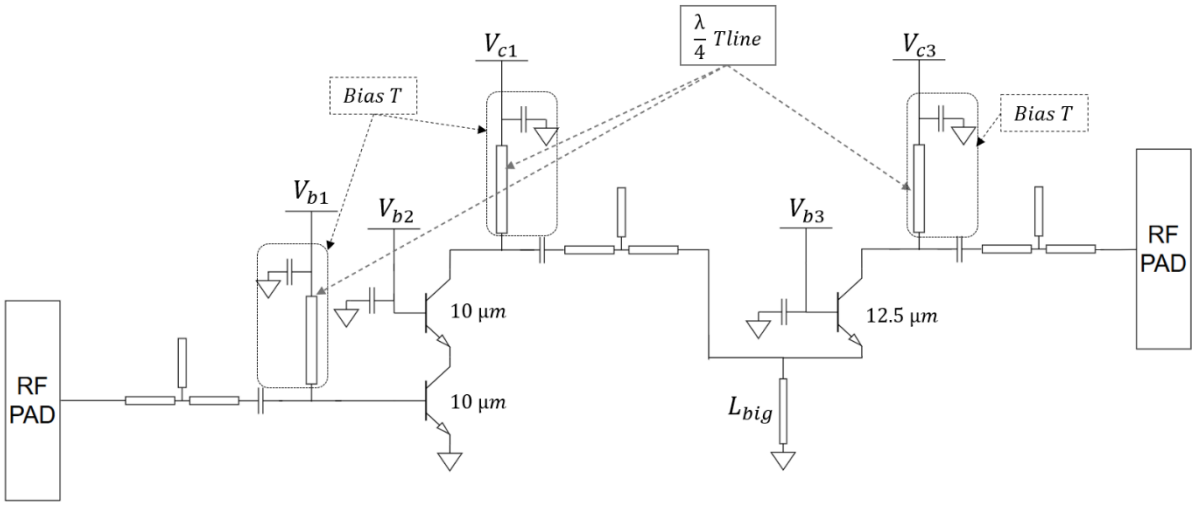


Figure 3-24: Simplified schematic of the 2 stage PA

Once the transistor sizing and the EM simulation of the different passive components have been completed, a final layout is designed according to the DRC restrictions for a total area of $950X985\ \mu m^2$, a layout view is shown in the Figure 3-25.

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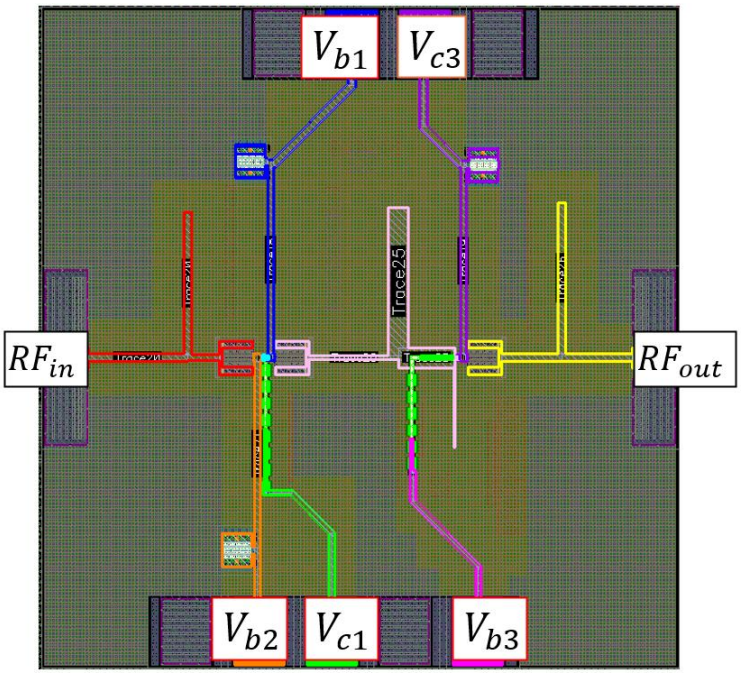


Figure 3-25: Layout view of the 2 stage power amplifier V1

A global, block-by-block simulation of the two-stage PA is performed. The resulting small-signal response is shown in Figure 3-26.

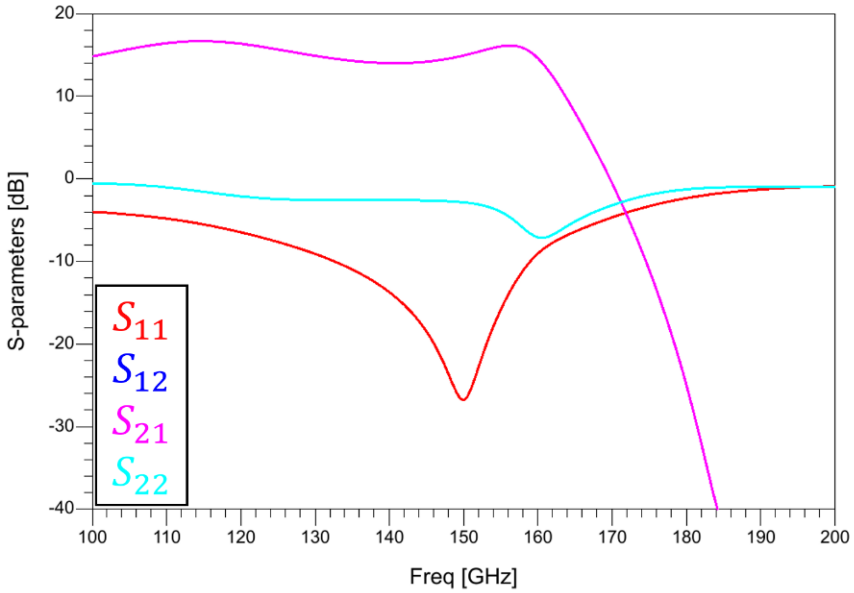


Figure 3-26: The small-signal simulation results of the two-stage PA with only line/stub-based matching

The input return loss is well centered around 150 GHz, with a minimum value of approximately 26 dB, indicating an excellent input match at the targeted operating frequency. The PA exhibits a gain of about 15 dB at 150 GHz, together with a very wide bandwidth, despite the presence of a dip around 138 GHz. Considering a nominal gain of 15 dB, the corresponding 3dB bandwidth is on the order of 65 GHz, which remains a very good result.

In addition, the two-stage PA provides very strong reverse isolation between output and input, better than 45 dB over the entire simulated band, mainly thanks to the cascode input stage. The corresponding large-signal simulation results are shown in Figure 3-27.

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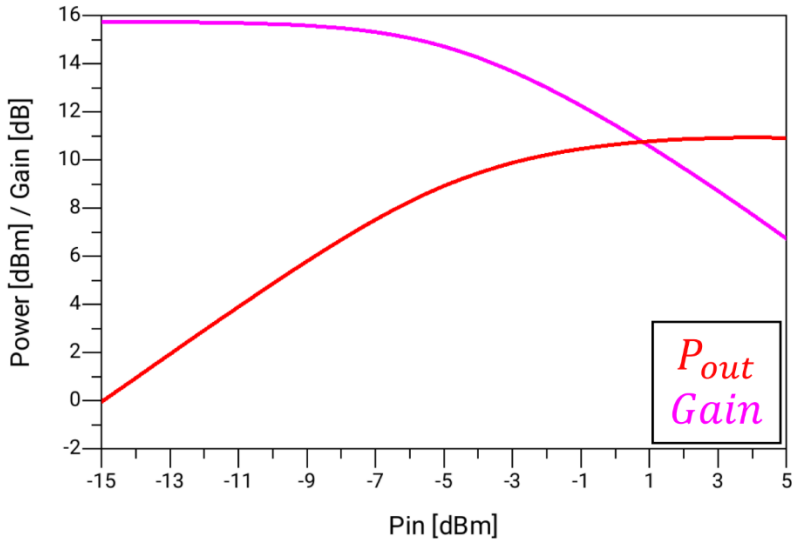


Figure 3-27: Large-signal simulation results of the two-stage PA

The simulated large-signal gain (pink curve) remains above 15 dB, in good agreement with the small-signal results. The 1dB gain compression point is obtained for an input power of -5 dBm, corresponding to an output $P_{1\text{dB}}$ of 9 dBm. The saturated output power P_{sat} reaches approximately 11 dBm, which illustrates the improved compression behavior provided by the CB output stage. The corresponding PAE versus input power, evaluated over the same input power sweep, is reported in Figure 3-28.

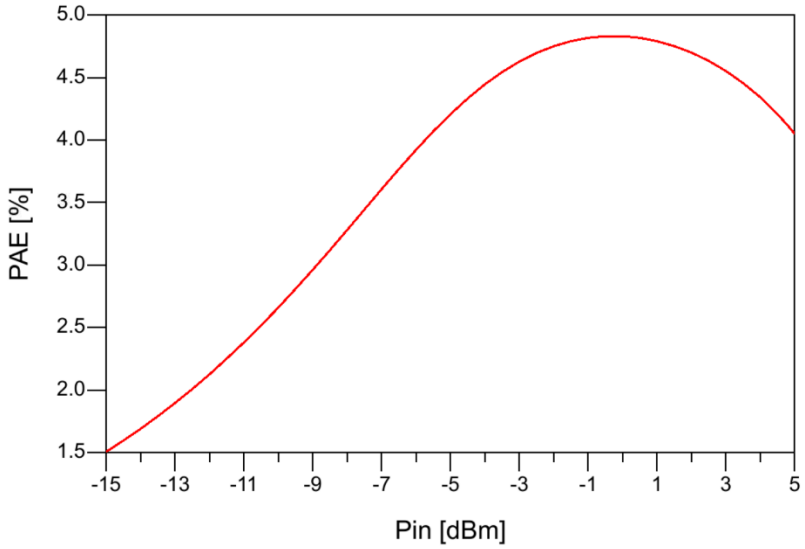


Figure 3-28: PAE versus input power for the two-stage PA

A maximum PAE of 4.8 % is obtained for an input power of 0.5 dBm. At the 1dB compression point, the PAE reaches 4.5 %. For a 6dB output back-off, the PAE is still about 2.6 %, i.e., more than half of the PAE at $P_{1\text{dB}}$. It should be noted that this circuit corresponds to our first two-stage PA implementation. Its PAE is significantly lower than that of the single-stage PA, which can be attributed to the additional losses introduced by the different matching networks. Nevertheless, the overall PAE profile remains very good, with only a reduction of about a factor of two at 6dB back-off, thanks to the current-clamping operation of the second stage. This behavior can be further confirmed from Figure 3-29, which plots the output power versus the DC power consumption as a function of the input drive level.

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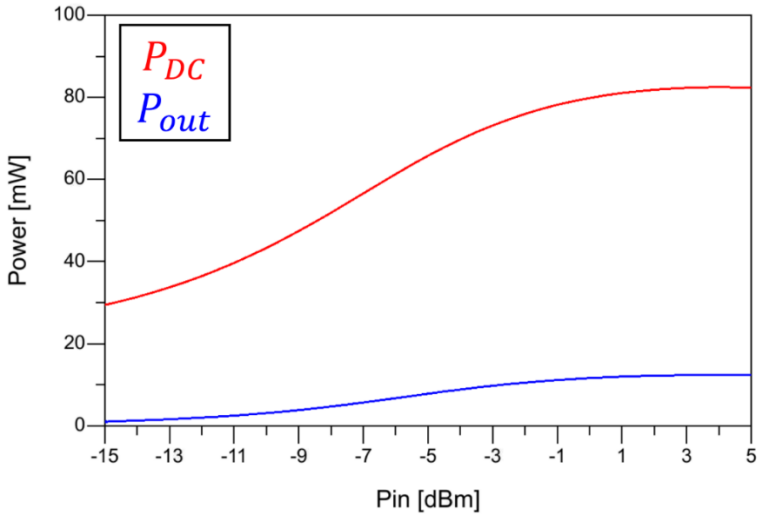


Figure 3-29: Simulated output power (blue curve) and DC power consumption (red curve), both expressed in mW, as a function of the input power in dBm

As expected, the DC power consumption (red curve) scales with the output power (blue curve), confirming the dynamic behavior of the biasing and the effectiveness of the current control in the CB stage.

Table 3-3 shows a comparison between state of art power amplifiers and the three already presented power amplifiers.

Ref	Topology	SiGe Techno	f_t/f_{max} (GHz)	BV_{CEO} (V)	Frequency (GHz)	Gain (dB)	P_{sat} (dBm)	P_{1dB} (dBm)	$PAE\ @\ P_{1dB}$ (%)	Area (mm^2)
[19]	Single 2 stage cascode	IHP's 130 nm	300/500	1.7	125-146	18.2	15	11	5	0.46
[20]	Differential 2 stage cascode	? 130 nm	?	?	109-119	18.5	11.8	9	<4	0.35
[21]	Balanced 3 stage cascode	IBM's 120 nm	200/250	?	112-128	25.5	17.5	13.3	<3	?
[22]	Single 4 stage CB	ST B55 55 nm	325/375	1.5	125-159	24	17.6	16.8	17.1	0.18
[24]	4-way parallel 2 stage cascode	IBM's 90 nm	300/360	1.7	110-145	18.2	21.9	18.6	9	1.7
This work	Single 1 stage CB	ST B55X 55 nm	325/375	1.5	125-158	4*	15.5*	12*	11*	0.38
This work	Single 1 stage cascode	ST B55X 55 nm	380/475	1.5	100-165	13*	9.5*	6.4*	9*	0.6
This work	Single 2 stage CB cascode	ST B55X 55 nm	380/475	1.5	95-160	15*	11*	9*	4.5*	0.94

Table 3-3: State of art power amplifiers vs proposed ones, comparing: their topologies, performance metrics, and technology.

To summarize, the two-stage PA design achieves a gain higher than 15 dB and a very reasonable output power, with an output $P_{1\text{dB}}$ of 9 dBm. It exhibits a good compression and consumption profile thanks to the CB output stage, combined with strong input–output isolation provided by the cascode input stage. This work shows a comparable output power capability and power added efficiency than other works as [19] and [20], while showing a smaller gain and a larger area.

The cascode + CB combination therefore appears to be a very promising topology. However, some difficulties were encountered in designing the different matching networks, which negatively impact the overall performance of the circuit. Alternative matching strategies can be considered. In particular, the objective is to reduce the losses associated with the interstage DC-blocking capacitor, as well as the

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additional losses introduced by the bias-T network. To address this, an alternative matching approach is presented in the next subsection.

3.5 2 stage power amplifiers matched with coupled line coupler

3.5.1 Design and simulation result

In this part, we retain the same overall topology, with a cascode input stage followed by a CB output stage. A slight resizing is performed by reducing the emitter length of the output CB device to 12.5μm. A new PLS extraction is then carried out on the output stage, followed by a load-pull analysis on both stages. The corresponding optimal load impedances are: $> Z_{\text{opt,cascode}} = 24.2 + j36.7\ \Omega$ And $Z_{\text{opt,CB}} = 17 + j43.8\ \Omega$ at 150 GHz. The associated input impedances are: $> Z_{\text{in,cascode}} = 7.8 - j8.3\ \Omega$ and $Z_{\text{in,CB}} = 12.5 + j4.5\ \Omega$. Once these impedances are fixed, the main focus of this section is on redesigning the different matching networks. The interstage DC-blocking capacitor is replaced by a coupled line structure operated in RTPS mode, using identical strip widths in order to simplify the design of this fully custom component. In addition, a short-circuited stub is introduced, which allows the PA to be biased directly through the coupling stub. RF decoupling to ground is provided by combining poly and MoM capacitors to efficiently shunt the RF signal to ground.

Fig. 4-7 shows a simplified schematic of the proposed design. It can be observed that no series "thru" capacitors are used anymore for DC blocking before and after each transistor, and that no additional bias-T network is required, since these functions are now integrated into the matching networks themselves. A simplified schematic of these matching networks is presented in Figure 3-31 with a highlight on possible DC bias points.

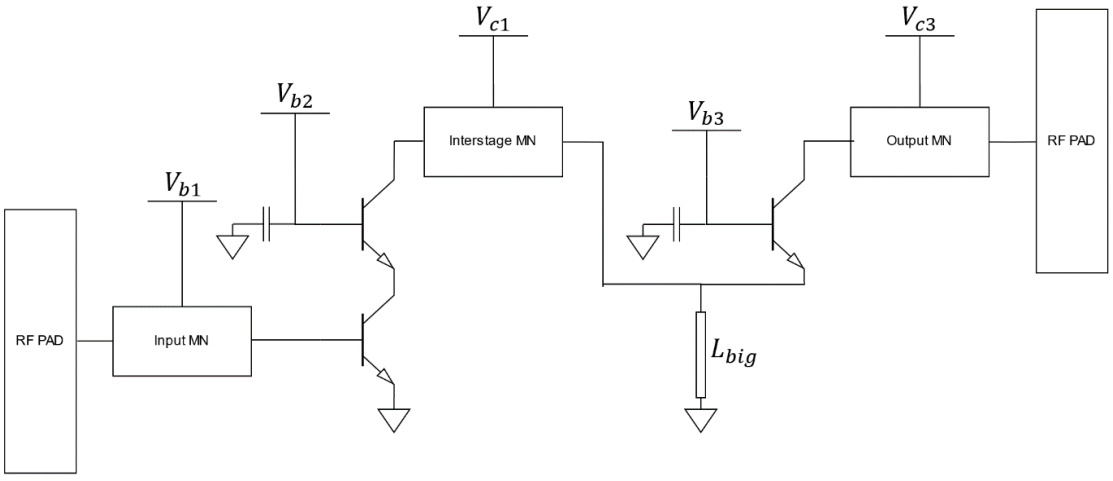


Figure 3-30: simplified schematic of the 2 stage PA based on coupled lines

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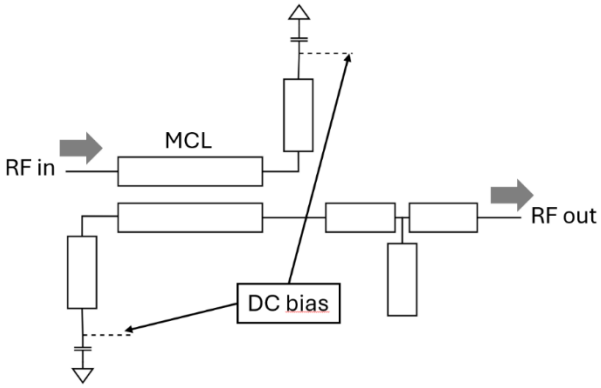


Figure 3-31: Simplified schematic of the matching network based on a coupled line coupler

The coupled line section is followed by a conventional shunt stub, which allows the overall matching network to be decomposed into two successive matching steps. The design procedure starts from the output and proceeds toward the input. With this new matching strategy, the transistors are biased directly through the matching network, so that the interstage series "thru" DC-blocking capacitor is no longer required. The shunt capacitors used to provide RF grounding have values on the order of 1 pF each. This network is designed as follows. To facilitate the design process, ADS is first used with ideal transmission lines and the built-in optimizer to obtain an initial estimate of the key parameters, such as the even/odd mode characteristic impedances and electrical length of the coupled line section, as well as the characteristic impedance and electrical length of each line and stub. In this initial step, the parasitic effects of the input pads are included. Once these target parameters are identified, each passive element is sized and laid out, and all components are then combined into a full EM-based matching-network simulation.

A more detailed analysis of these matching networks will be provided later in this chapter. Once the design is completed, the final layout of the PA is obtained occupying an area of $1200\ X\ 720\ \mu m^2$, as shown in Figure 3-32.

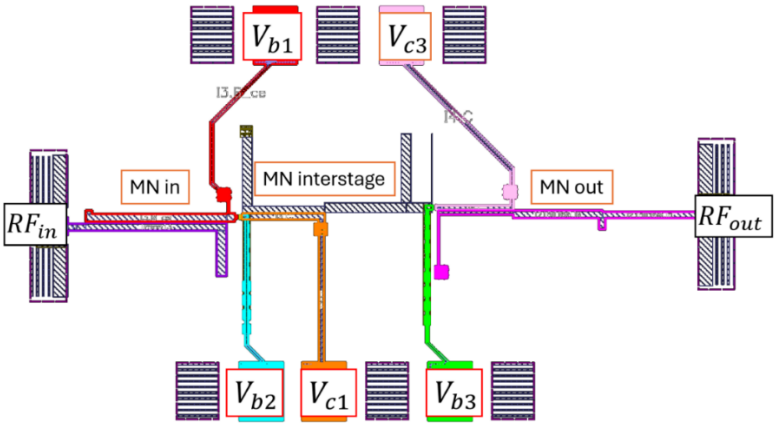


Figure 3-32: Final layout of the 2 stages PA based on MCL

The DC pads connected to each bias node are indicated on the layout, and the corresponding bias voltages applied to these nodes are summarized in Table 3-4.

V_{b1}	V_{b1}	V_{b1}	V_{b1}	V_{b1}
890 mV	2.14 V	2.5 mV	825 mV	1.8 V

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Table 3-4: The bias conditions of the two-stage PA based on MCL

Figure 3-33 shows the small-signal (S-parameter) simulation results of the two-stage PA using the coupled line matching network.

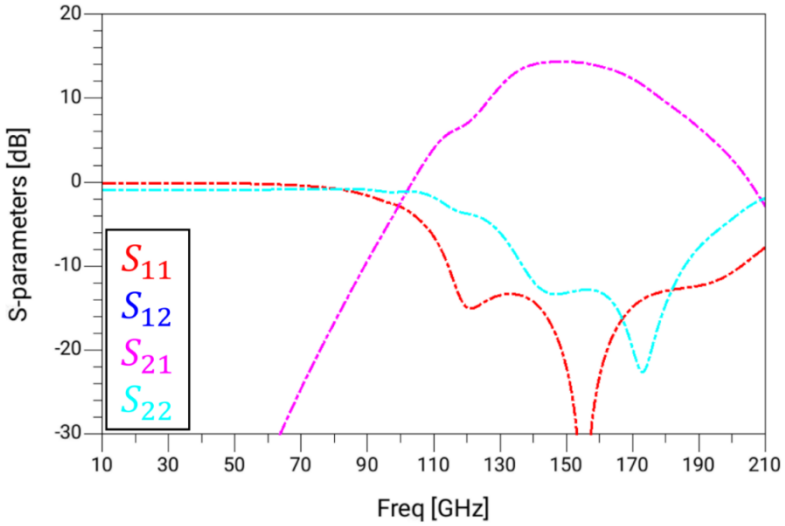


Figure 3-33: Small-signal simulation results of the two-stage PA with coupled line-based matching network

The two-stage PA exhibits a maximum small-signal gain of approximately 14 dB, with a wide 3dB bandwidth extending from 125 to 175 GHz. The input matching is good and is intentionally centered a few gigahertz above the target frequency in order to compensate for the natural gain roll-off at higher frequencies due to technology limitation. The reverse isolation remains better than 30 dB over the entire simulated frequency range. Overall, the small-signal performance is promising. A large-signal simulation is then performed, and the corresponding input/output power characteristics and power gain are reported in Figure 3-34.

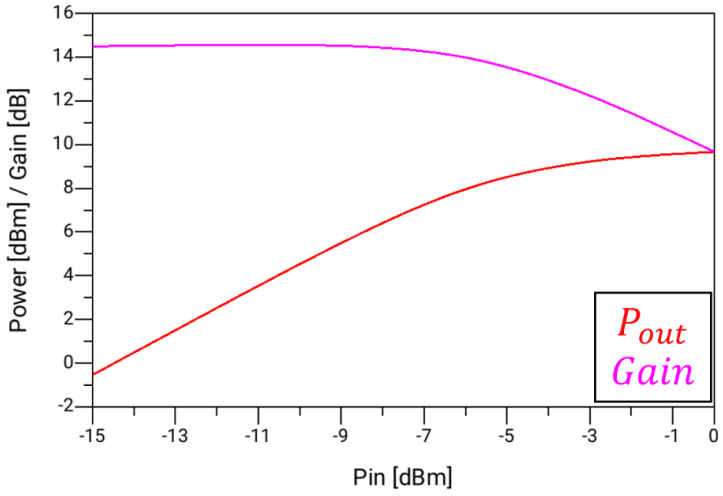


Figure 3-34: Large-signal simulation results result for the 2-stages PA based on MCL

Large-signal simulations are performed for an input power sweep ranging from -15 dBm to 0 dBm. The large-signal gain (pink curve) remains close to 14.5 dB, in good agreement with the small-signal results. The 1dB gain compression point occurs for an input power of -5 dBm, corresponding to an output power $P_{1\text{dB}} = 8.5$ dBm, while the saturated output power P_{sat} is around 9 dBm, indicating a sharp compression profile. The corresponding PAE of the two-stage PA is reported in Figure 3-35.

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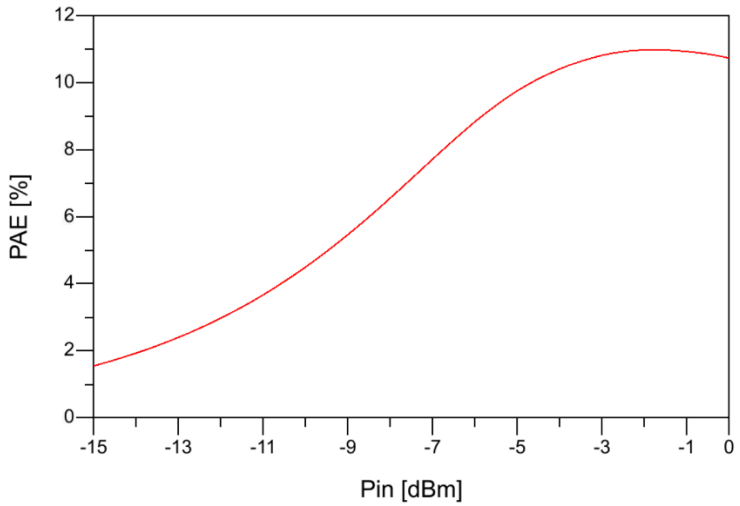


Figure 3-35: PAE of the 2 stage PA with MN base on MCL

The simulated PAE curves show a maximum PAE of about $11\ \%$, and a PAE at $P_{1\mathrm{dB}}$ of $9.8\ \%$, which is a very good result. For a 6dB output back-off, the PAE remains around $4\ \%$, which is still quite satisfactory. In order to analyze the contributions of each stage to the overall power consumption, Figure 3-36 reports the DC current of each stage as a function of the input power.

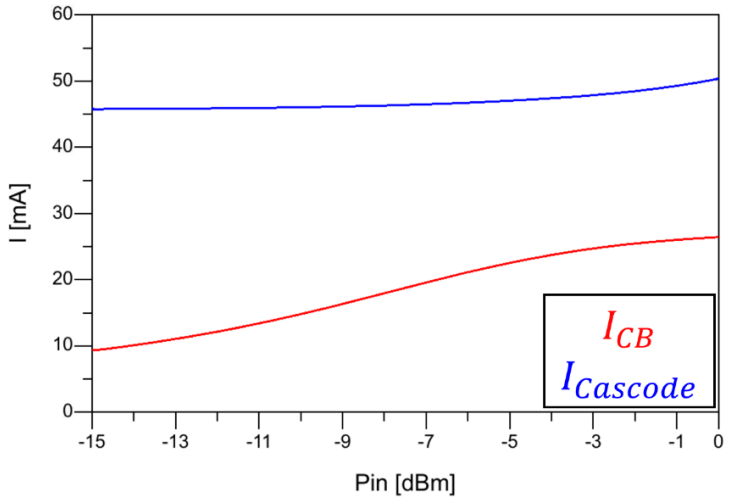


Figure 3-36: DC collector's current for each stage of the 2-stage PA

As can be observed, the DC current of the common-base stage increases with the input power, whereas the DC current of the cascode stage remains essentially constant. This behavior explains the improved PAE at back-off.

3.5.2 Measurement vs simulation

The circuit was sent to fabrication on the B55X mask set. Small-signal measurements of the two-stage PA were performed using the same VNA setup and GSG RF pads. A comparison between measurement and simulation is presented in Figure 3-37.

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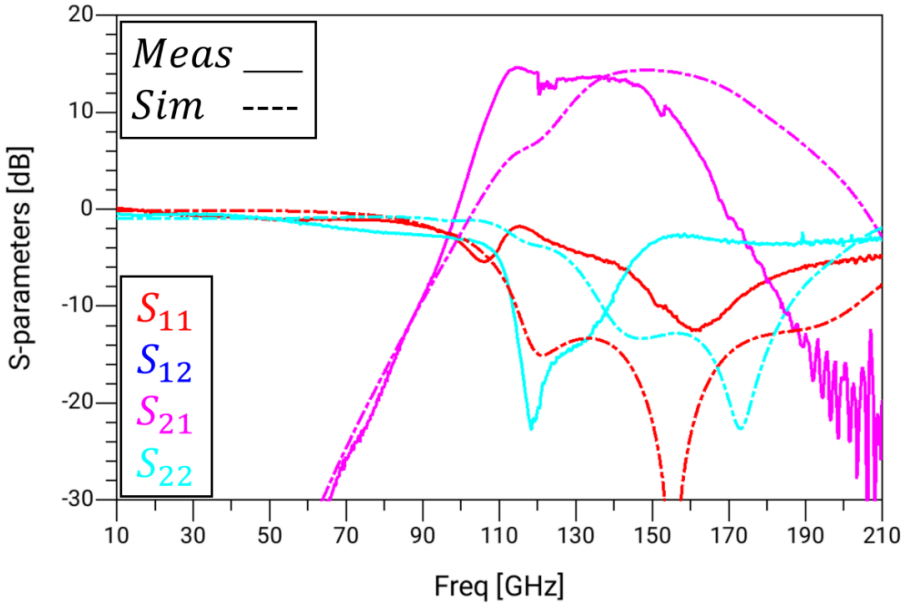


Figure 3-37: Small signal Measurement vs simulation of the 2 stages PA

The measurement results confirm that the PA operates correctly and does not exhibit oscillations under the measurement conditions. A significant frequency shift is, however, observed between simulation and measurement. The measured input return loss is weaker, with a level roughly 10 dB lower than in simulation. Nevertheless, the reverse isolation between output and input remains very good in measurement. This parameter is not shown in the figure because it is too small (below -40dB). For readability, the y-axis was therefore limited to -30dB, and the same convention will be used for all subsequent PA results. The measured gain is promising, but there is a noticeable mismatch between the two families of curves (solid lines vs. dashed lines). As can be seen, the center frequency of the gain has shifted together with the output return loss, which suggests that this shift may be the underlying cause.

Several hypotheses can be put forward to explain this discrepancy. A first one is related to passive component mismatches, which will be investigated by comparing simulation and measurement of the stand-alone matching networks (MNs). Another hypothesis concerns the simulation methodology itself. In the following, we first focus on validating the passive-mismatch hypothesis.

3.5.2.1 Stand-alone matching networks investigation

A. Input matching network

From the complete layout shown in Figure 3-32, three distinct matching networks can be identified. We start our analysis with the input matching network considered in stand-alone configuration. In the measurement context, it may be necessary to add a short extra line section in order to reduce undesired coupling between the matching network (in particular the stub connected to the coupler) and the probe pads.

Unfortunately, performing a proper de-embedding on only one side of the structure is more complex. As a consequence, a symmetric TRL de-embedding is applied on both sides during measurement, and the probe pad is subsequently re-introduced in the EM simulation. The objective is to ensure a consistent comparison between measurement and simulation, even if the absolute performance of the stand-alone structure slightly differs from that of the embedded matching network in the full PA. Figure 3-38 presents the layout of the input matching network under test, as used for stand-alone characterization with a highlight on the DUT region. On the right-hand side, a half-thru line is preserved

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to enable TRL calibration, whereas on the other side the pad is directly connected, since it is an integral part of the design.

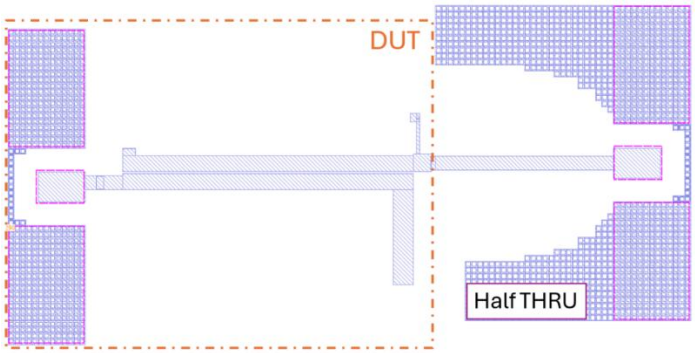


Figure 3-38: Layout view of the input matching network as used for stand-alone characterization.

Figure 3-39 shows the layout for simulation view of the DUT in a simplified form, in order to reduce the EM simulation time. In particular, the original ground mesh (from M1 to M5) has been replaced by a solid ground plane on M5 only.

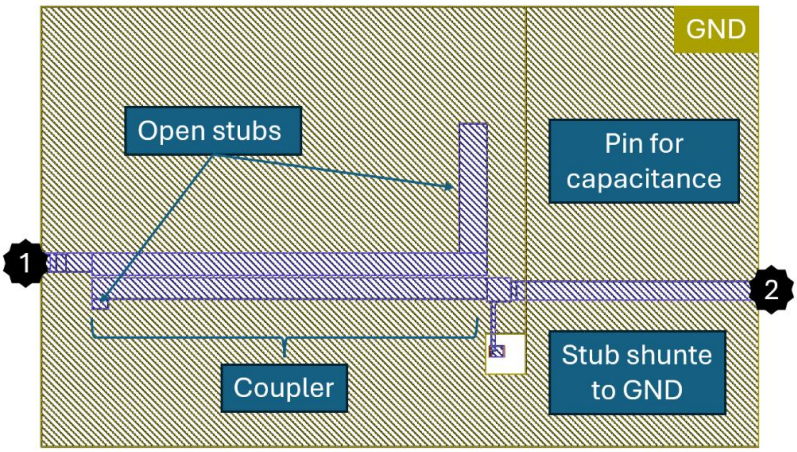


Figure 3-39: Layout view of the input matching network for EM simulation

As can be observed, the matching network is composed of a coupled line coupler connected to two different open-ended stubs, one on the thru port and one on the coupled port. A transmission line followed by a shunt stub to ground through a capacitor (realized as a combination of MoM and poly capacitors) is connected to the output (port 2), i.e., to the input of the cascode stage (base of the common-emitter device of the cascode). The target impedances to be matched are given by:

$$Z_1 = Z_O = 50\ \Omega \text{ and } \quad Z_2 = Z_{\text{in,cascode}} = 8.4 - j8.3\ \Omega$$

A small-signal simulation is then performed with the ports normalized to these target impedances. The obtained S-parameters are shown in Figure 3-40.

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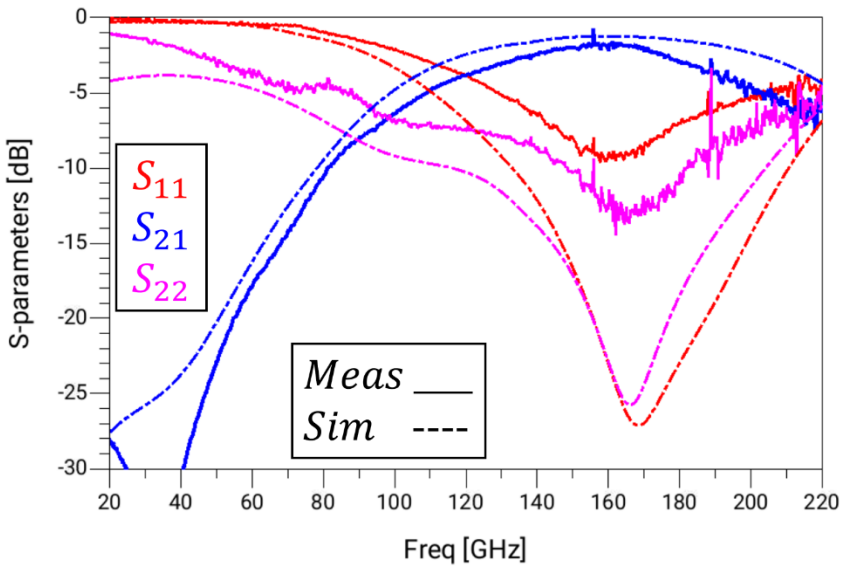


Figure 3-40: Small-signal comparison between EM simulation and stand-alone input matching-network measurements

The figure presents the small-signal comparison between EM simulation and stand-alone measurements of the input matching network. The DUT corresponds to the layout described in the previous subsection, including the coupled line section, the stubs, and the RF shunt capacitors, with de-embedding performed using TRL calibration and the probe pad re-introduced in simulation for a fair comparison. The EM simulation and stand-alone measurement of the input matching network exhibit a very similar overall behavior. However, both input and output matching are degraded in measurement, and additional insertion loss is observed. For example, at 160 GHz, the simulated insertion loss increases from about 1.2 dB to approximately 1.8 dB in measurement. This additional 0.6 dB can be partly attributed to the mismatch clearly visible in the measured S-parameters.

As discussed in the passive-component chapter, EM simulations tend to be slightly optimistic in terms of conductor and dielectric losses, which also contributes to the observed discrepancy. It should also be recalled that a TRL de-embedding was applied to all stand-alone structures. In the present case, the half-thru line is present at the output side of the DUT but not at the input side, as illustrated in Figure 3-38. This asymmetry can significantly affect the quality of the de-embedding and explains, at least in part, the differences observed in terms of input and output matching. Despite these discrepancies, the measured response confirms a behavior that is globally consistent with the EM simulation, with insertion losses that remain reasonably low for this type of structure.

B. Interstage matching network

We now turn to the interstage matching network. In this case, for simulation purposes and in order to mitigate parasitic coupling, short $50\ \Omega$ line sections were added on both the left and right sides of the matching network. The final structure is then placed between two half-thru lines to enable a standard TRL calibration on both ports. The corresponding layout is shown in Figure 3-41.

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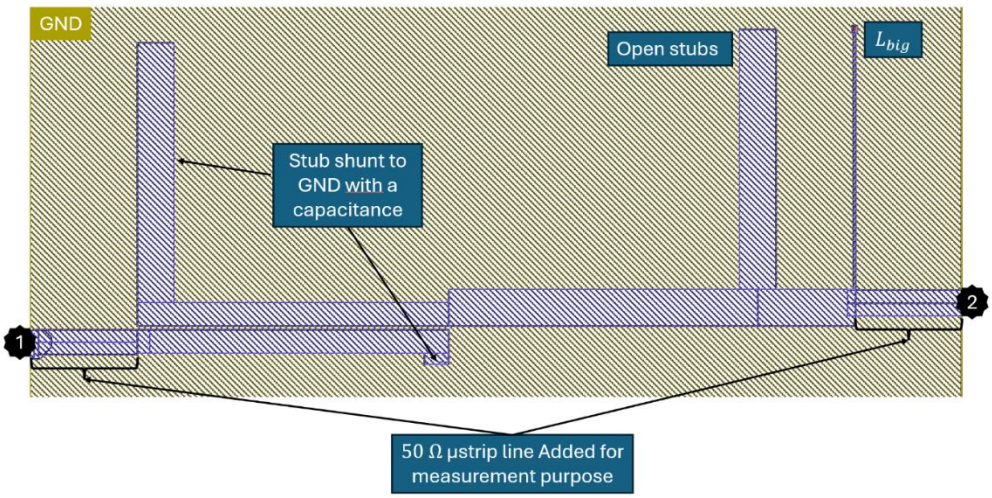


Figure 3-41: Interstage matching-network layout of the two-stage PA

As can be seen, for measurement purposes short $50\ \Omega$ microstrip line sections were added at the input and output of the DUT. This modification affects both simulation and measurement in the same way. Consequently, the S-parameter results presented in the following figures do not directly reflect the intrinsic matching quality of the network itself, but they remain suitable for a consistent comparison between simulation and measurement.

The interstage matching network consists of a custom coupled line coupler whose thru and coupled ports are each terminated by shunt stubs to ground through the same RF shunt capacitor (implemented as a MOM + poly capacitor). At the isolated port of the coupler, an open-circuited line-and-stub network is connected, followed by a further stub tied to ground through a stack of several vias. This last stub corresponds to L_{big} and is required both to implement the current-clamping function of the common-base stage and to connect node 2, i.e., the emitter of the common-base device, to ground. In this interstage configuration, the targeted reference impedances are:

$Z^*_{\text{opt,cascade}} = 24.2 - j36.7\ \Omega$ and $Z_2 = Z_{\text{in,CB}} = 12.5 + j4.5\ \Omega$.

small-signal simulation normalized to Z_1 and Z_2 is then performed, and the resulting S-parameters are shown in Figure 3-42.

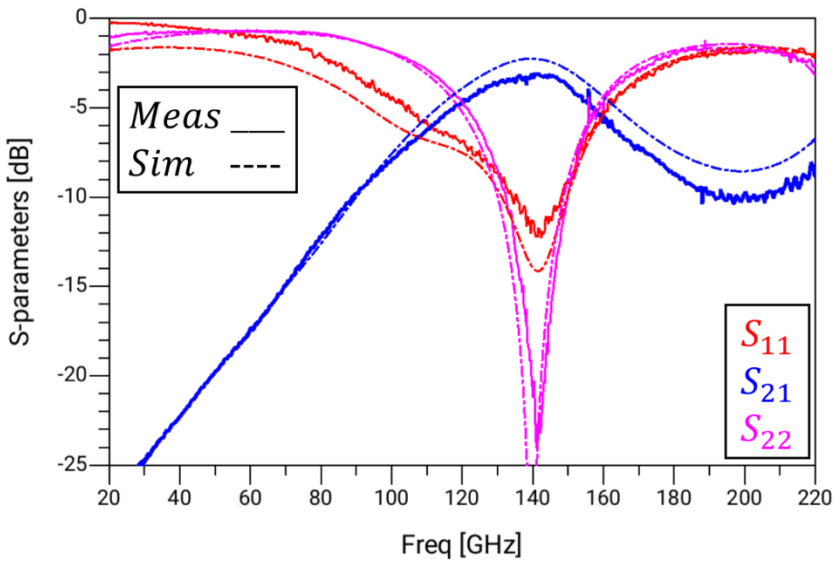


Figure 3-42: Small-signal comparison between EM simulation and stand-alone interstage matching-network measurements

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In this case, an almost perfect agreement between EM simulation and measurement is obtained. As expected, the measured insertion loss is slightly higher than the simulated one. For example, at 141 GHz, the insertion loss increases from about 2.3 dB in simulation to approximately 3 dB in measurement. It should be recalled that the additional $50\ \Omega$ line sections inserted and measured at both ends of the DUT have a strong impact on the reported S-parameters. This explains why the response appears shifted around 140 GHz, why the apparent bandwidth is relatively narrow, and why the overall insertion losses are not negligible. However, the main objective here was to compare simulation and measurement for this block, and this goal is successfully achieved.

C. Output matching network

Finally, the last matching network is designed to match the output of the common-base stage, i.e., the optimal load impedance of the CB, to the external reference impedance of 50Ω. In this case, the parasitic effects of the RF probe pad at the output are explicitly taken into account, since they cannot be de-embedded in power measurements and are, in any case, representative of a realistic product implementation where bump pads would also be present. Thus, for this output matching network we have:

$$Z_1 = Z^*_{\text{opt,CB}} = 17 - j43.8\ \Omega \text{ et } \ Z_2 = Z_0 = 50\ \Omega$$

The layout of the output matching network of the two-stage PA is shown in Figure 3-43: Output matching-network layout of the two-stage PA.

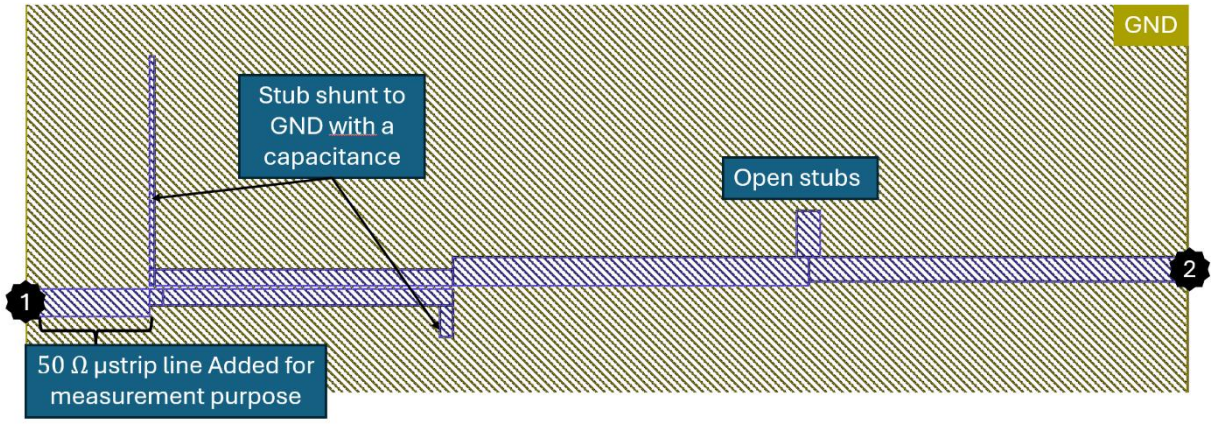


Figure 3-43: Output matching-network layout of the two-stage PA

In this case, as for the interstage network, a short 50Ω line section is added, but only at the input side, for measurement purposes. The DUT consists of a custom coupled line coupler whose thru and coupled RF ports are each terminated by a shunt stub to ground through the same RF shunt capacitor (MOM + poly), followed by an open-circuited line-and-stub network. Port 2 is directly connected to the RF probe pad. As in the input-matching case, a half-thru line is connected only on the input side in order to preserve the effect of the output pad. In practice, a standard TRL calibration is applied to the measurements, and the pad effect is then re-introduced in simulation. This approach may introduce some uncertainties and errors. A comparative S-parameter simulation between EM simulation and de-embedded measurements (with the pad added back in simulation) is presented in Figure 3-44.

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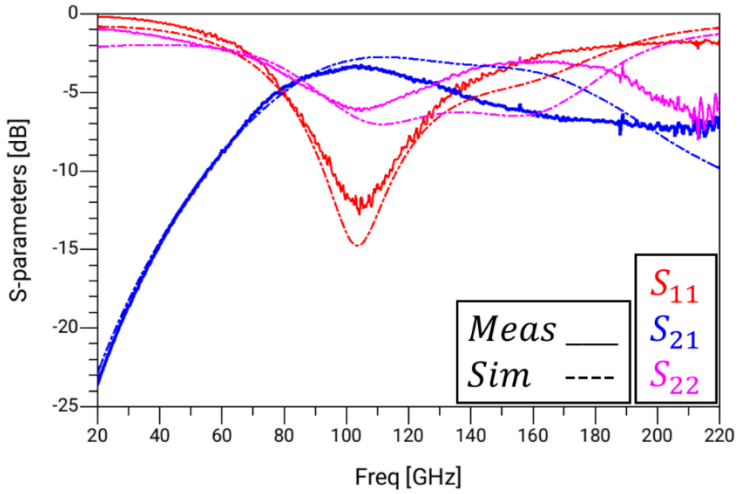


Figure 3-44: Small-signal comparison between EM simulation and stand-alone interstage matching-network measurements.

The EM simulation and the stand-alone measurement of the output matching network exhibit a similar overall behavior, in particular below 120 GHz, where an excellent agreement is observed. At higher frequencies, a noticeable upward shift in the measured response appears, which may be attributed to a non-optimal measurement setup, especially due to the half-thru line being implemented only on one side of the DUT. Overall, and apart from the high-frequency region, the insertion loss levels are relatively close. For instance, at the resonance center around 105 GHz, the simulated insertion loss is about 2.9 dB, compared to 3.5 dB in measurement, which is a reasonable agreement. As frequency increases, the discrepancy tends to grow. The fit remains satisfactory at lower frequencies, although both simulation and measurement exhibit relatively high insertion losses and a narrow bandwidth, mainly due to the additional $50\ \Omega$ line section intentionally inserted for measurement purposes.

Overall, small discrepancies are observed in the input and output matching, which can be attributed in part, or even entirely, to the de-embedding procedure. In this case, an additional half-thru section is subtracted and then artificially reintroduced, whereas the interstage network exhibits an almost perfect agreement between simulation and measurement. The main difference between these cases is that the stand-alone measurement setup is significantly cleaner and more appropriate. In other words, the de-embedding is more accurate, since the pad and the half-thru are removed symmetrically on both sides without requiring any additional reconstruction in simulation.

After validating the first hypothesis, the stand-alone measurements of the different matching networks show a reasonably good agreement with their corresponding EM simulations. Apart from slight mismatches and additional insertion losses, which can explain a very small degradation of the gain or minor shifts in frequency, these discrepancies are clearly not sufficient to justify the much larger mismatch observed between small-signal simulation and measurement of the complete two-stage PA, as shown in Figure 3-37. This indicates that the main source of discrepancy is unlikely to be the passive matching networks alone and further supports the need to investigate the impact of the global simulation methodology (TOP-level EM coupling, modeling assumptions, etc.) what will be done in the following sub-section.

3.5.2.2 Investigation on design methodology

We now turn to the second hypothesis, related to the simulation methodology itself. In our initial design flow, because of the very high operating frequency and the resulting fine meshing required for EM simulations, we relied on a block-by-block approach. Each brick (matching network, transistor cell, bias network, etc.) was simulated and optimized separately, which made it possible to fix issues brick by brick. However, at such high frequencies, parasitic coupling between blocks (bricks) can have a significant

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impact on the overall behavior, and this effect was not explicitly quantified. To address this point, a TOP-level EM simulation was performed including all passive components together, using the RFpro environment and Momentum as the EM solver, while the metal routing of the transistors was modeled through post-layout (PLS) extraction.

Figure 3-45 compares the measured response of the two-stage PA to the corresponding TOP-level simulation using the matching networks based on the MCL structures.

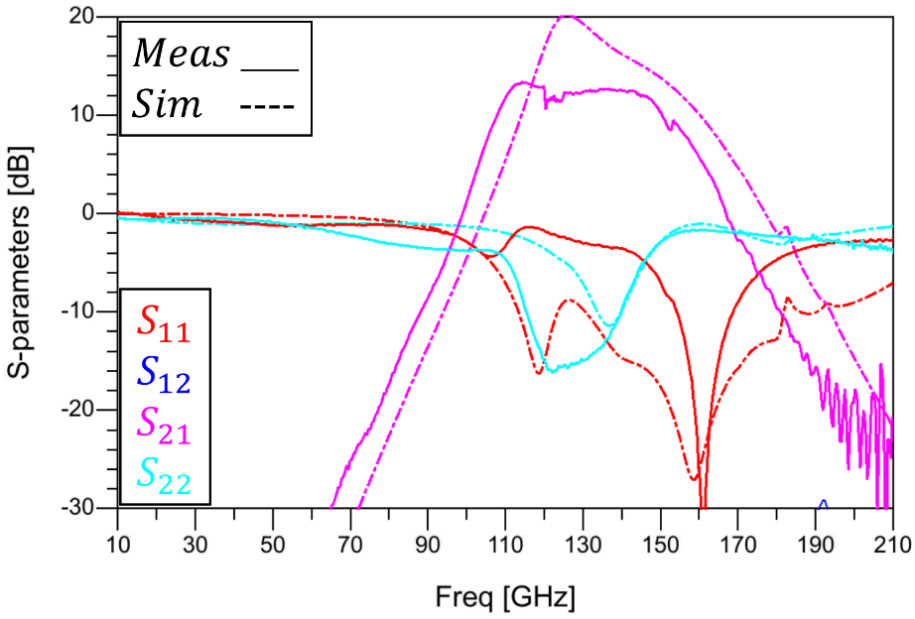


Figure 3-45: TOP-level simulation vs. measurement of the two-stage PA based on MCL

The TOP-level EM simulation provides a significantly better agreement with the measurements compared with the previous block-by-block approach. The overall trends of the simulated and measured curves are now much closer. The graph still indicates a very good reverse isolation, better than 30 dB. The behavior of the input return loss (S_{11}) is also more consistent in terms of shape: both simulation and measurement exhibit a first resonance peak around 120 GHz (shifted slightly lower in measurement) and a second one around 160 GHz. However, a noticeable mismatch remains between these two resonances, which results in a measured input matching that is not as good as in simulation over the whole band. From the gain and transmission point of view (S_{21}), the same overall tendency is observed in both simulation and measurement, with the simulated gain being somewhat higher, which remains physically reasonable. In any case, the correlation is clearly improved when using the TOP-level simulation. Finally, the output return loss (light-blue curve, S_{22}) shows a much better agreement between simulation and measurement, with almost identical trends, which was not the case with the block-by-block simulation flow.

Although the fit is not yet perfect, the use of TOP-level EM simulation instead of a purely block-by-block approach yields results that are much closer to reality, with a consistent trend for each parameter. This is encouraging and confirms the feasibility of PA design in the D-band. To further support this conclusion, the maximum available gain (MAG) extracted from simulation and measurement is compared in Figure 3-46.

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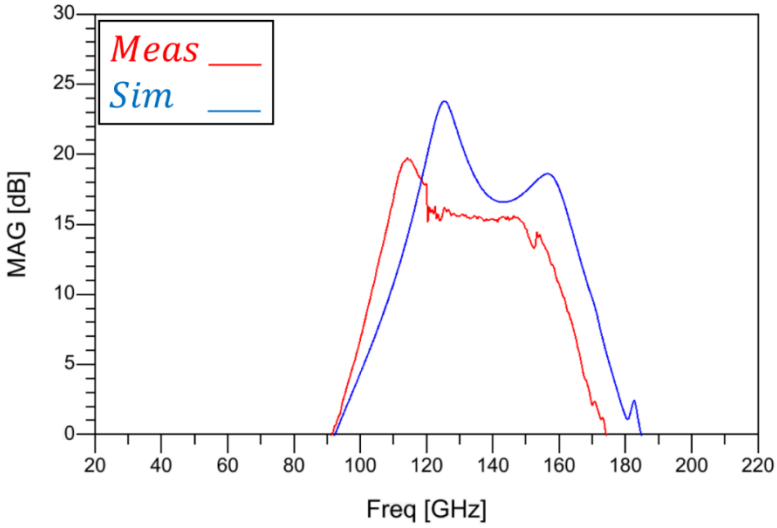


Figure 3-46: Measurement vs. TOP-level simulation of MAG for the two-stage PA with MCL-based matching networks

The figure compares the maximum available gain (MAG) obtained from measurements with the MAG predicted by the TOP-level EM simulation for the two-stage PA using MCL-based matching networks. A very good agreement is again obtained between measurement and TOP-level simulation, which represents a major improvement and provides a valuable guideline for future designs. Block-by-block simulations remain useful for initial sizing and topology optimization, but a full TOP-level EM simulation is clearly necessary to ensure a good correlation between simulations and measurements. A dedicated amount of design time must therefore be allocated to this step. In principle, this step could be completed relatively quickly; however, in our case, the need for fine tuning of custom-designed passive cells required repeated EM re-simulations with very long simulation times for each block, making iterative TOP-level refinement particularly time-consuming.

At this stage, our simulation methodology was reconsidered. As a reminder, the base-bias path was shunted to ground using several small MOM capacitors distributed along the routing. Due to the complexity of the EM problem, this structure was not simulated electromagnetically and was instead modeled as a single lumped capacitor with a low quality factor. In practice, this approximation does not capture the additional parasitic inductances associated with the bias routing and via connections. In summary, the TOP-level EM simulation significantly improves the agreement between simulation and measurement, but the parasitic effects associated with the base access are still underestimated, since they are not included in either the block-by-block simulations or the TOP-level model.

The next step is therefore to explicitly model this base-bias access in RFpro, in order to include its full EM behavior in the overall simulation flow. The bias voltages applied in both TOP-level simulation and measurement, as well as the corresponding DC currents for each access, are summarized in Table 3-5.

	I_{b1}	I_{b2}	I_{c1}	I_{b3}	I_{c3}
Sim	27.6 µA	29 µA	15.7 mA	4.2 µA	4.2 mA
$Meas$	26 µA	29.8 µA	15.6 mA	4.12 µA	4.1 mA

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	V_{b1}	V_{b1}	V_{b1}	V_{b1}	V_{b1}
Sim	$902\ mV$	$2.2\ V$	$2.5\ mV$	$825\ mV$	$1.8\ V$
$Meas$	$890\ mV$	$2.14\ V$	$2.5\ mV$	$840\ mV$	$1.8\ V$

Table 3-5: Bias voltages applied in both TOP-level simulation and measurement, as well as the corresponding DC currents for each access

Figure 3-47 shows small signal TOP-level simulation after taking into account the bias access and measurement for the 2 stage PA based on MCL.

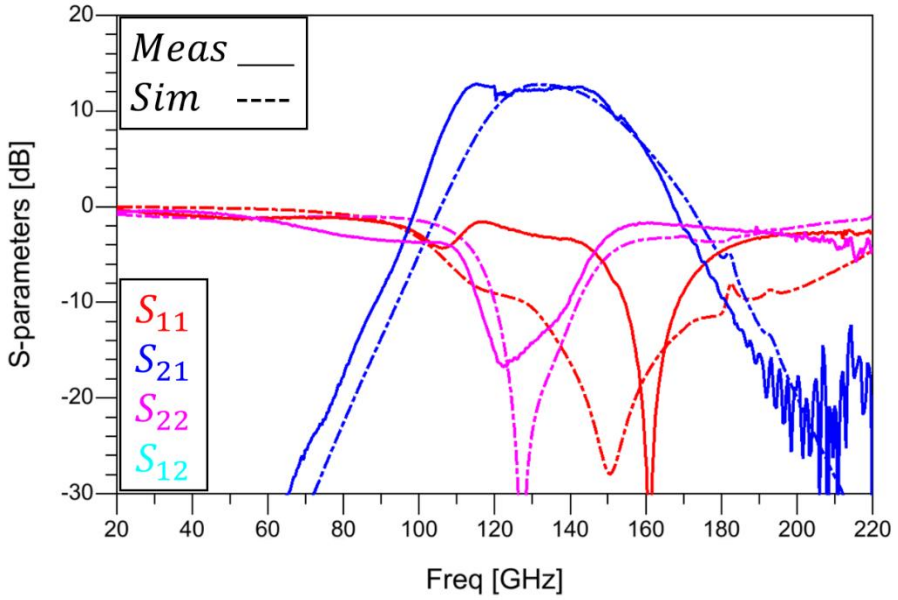


Figure 3-47: Small-signal measurement vs. simulation of the two-stage PA with MCL-based matching networks

The figure shows the comparison between small-signal measurements and TOP-level simulations for the two-stage PA using MCL-based matching networks. A significantly better fit is obtained, and the overall trends of the simulated and measured curves are now very similar. Reverse isolation between output and input remains excellent, with measured values still close to the simulated ones. The input matching (S_{11}) behaves in a better way (more similar) as the two minimums are located in similar frequency for both simulation and measurement, indicating that the impact of the base-bias impedance on the input impedance seen by the transistor is relatively limited. It is better but not perfect.

In contrast, the output matching (S_{22}) shows a much-improved agreement compared with the previous block-by-block flow, which confirms that the base-access impedance has a stronger effect on the output matching and on the effective optimal load impedance. The gain (S_{21}) is also in much better agreement: the simulation and measurement exhibit the same overall tendency and are very close above 120 GHz, with only a slight difference at lower frequencies. Consequently, the measured 3 dB bandwidth is slightly reduced, from about 55 GHz in measirement to approximately 45 GHz in simulation. The gain roll-off is somewhat faster at the lower edge of the band. One possible explanation that has been identified is a small issue in the simulation flow: during the latest co-simulations, the capacitance between the M1 metal layer and the front-end layers was effectively

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counted twice, once in the transistor compact model and once in the PLS extraction. This additional capacitance could account for the observed bandwidth reduction.

To further confirm the improvement, the input and output matching are examined on the Smith chart, comparing measurement and simulation for both S_{11} and S_{22}, as shown in Figure 3-48 and Figure 3-49, respectively.

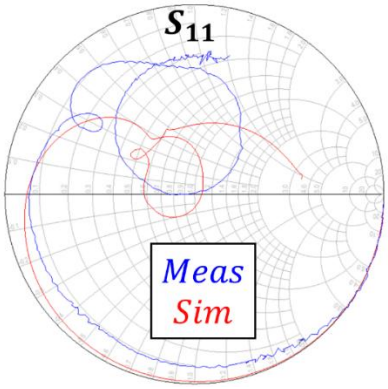


Figure 3-48: Smith-chart comparison of simulated and measured input matching

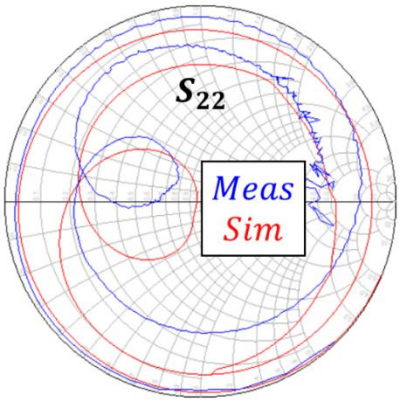


Figure 3-49: Smith-chart comparison of simulated and measured output matching

The Smith-chart comparison of S_{11} shows that the simulated and measured trajectories follow a similar overall trend; however, the measured curve is shifted further away from the center of the Smith chart. As a result, the impedance of interest in measurement is located farther from 50Ω than in simulation, where it remains relatively close to the center.

In contrast, the S_{22} Smith-chart comparison exhibits a much better agreement, with very similar shapes and almost identical behavior between simulation and measurement. This result is encouraging and confirms that the parasitics associated with the base-bias access have a strong impact on the overall circuit behavior, and in particular on the effective output impedance.

Due to time constraints, large-signal measurements could not be performed. The large-signal performance of the DUT is therefore quantified based on the TOP-level simulation taking also into account the EM simulated base access. which has been shown to provide a good fit to the small-signal measurements. Figure 3-50 reports the simulated input power, output power, and power gain of the two-stage PA obtained from this TOP-level large-signal analysis.

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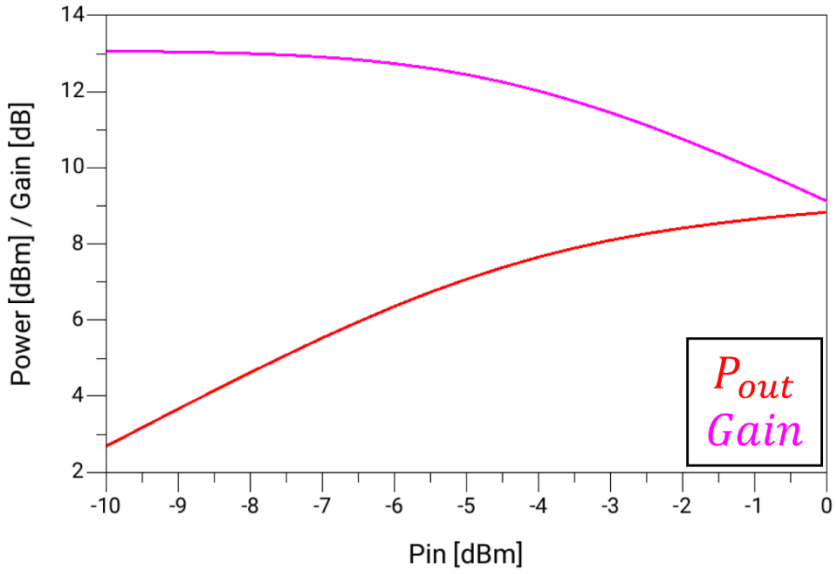


Figure 3-50: Large signal simulation result for output power, and power gain of the two-stage PA obtained from TOP-level simulation + base access

The figure shows the large-signal gain of the two-stage PA, with a simulated gain of approximately 13dB, which is consistent with the corrected simulations and with the small-signal (SP) measurements. It should be noted that the measured small-signal gain is slightly higher, so a somewhat higher large-signal gain can reasonably be expected in measurement. The 1dB gain compression occurs for an input power of -4.5 dBm, leading to an output $P_{1\text{dB}}$ of 7.6 dBm. This is a very good result for a two-stage PA, especially considering that the initial design (before correction of the simulation flow) predicted a $P_{1\text{dB}}$ of 9 dBm. The corresponding PAE obtained with the corrected TOP-level simulation setup is reported in Figure 3-51.

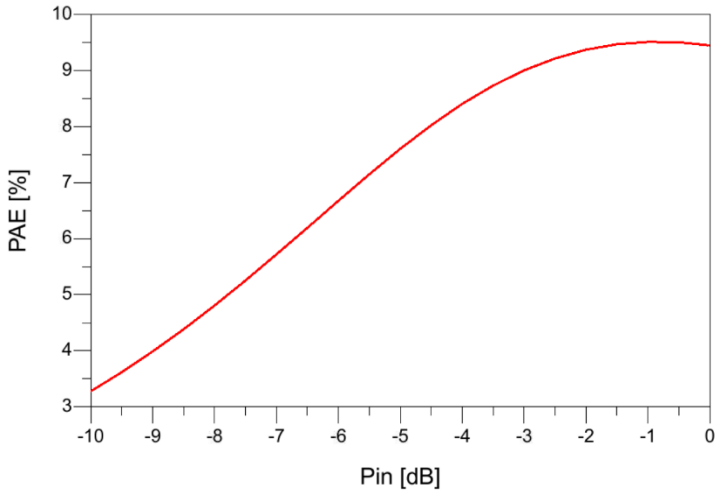


Figure 3-51: Large signal simulation result for PAE of the two-stage PA obtained from TOP-level simulation + base access

The simulated PAE results indicate a maximum PAE of 9.5 %, a PAE at $P_{1\text{dB}}$ of 7.4 %, and a PAE of 3.2 % at 6 dB output back-off. These values are acceptable, but they clearly show that the contribution of the cascode stage is still too large in this PA to significantly improve the PAE profile at back-off. Even thought we are still around half of the PAE what is still verry good. Nevertheless, these results remain very good, especially considering that they are a direct consequence of the corrections applied to the simulation setup.

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A comparison with state of art is proposed in Table 3-6.

Ref	Topology	SiGe Techno	f_t/f_{max} (GHz)	BV_{CEO} (V)	Frequency (GHz)	Gain (dB)	P_{sat} (dBm)	P_{1dB} (dBm)	$PAE\ @\ P_{1dB}$ (%)	Area (mm^2)
[19]	Single 2 stage cascode	IHP's 130 nm	300/500	1.7	125-146	18.2	15	11	5	0.46
[20]	Differential 2 stage cascode	? 130 nm	?	?	109-119	18.5	11.8	9	<4	0.35
[21]	Balanced 3 stage cascode	IBM's 120 nm	200/250	?	112-128	25.5	17.5	13.3	<3	?
[22]	Single 4 stage CB	ST B55 55 nm	325/375	1.5	125-159	24	17.6	16.8	17.1	0.18
[24]	4-way parallel 2 stage cascode	IBM's 90 nm	300/360	1.7	110-145	18.2	21.9	18.6	9	1.7
This work	Single 1 stage CB	ST B55X 55 nm	325/375	1.5	125-158	4*	15.5*	12*	11*	0.38
This work	Single 1 stage cascode	ST B55X 55 nm	380/475	1.5	100-165	13*	9.5*	6.4*	9*	0.6
This work	Single 2 stage CB cascode	ST B55X 55 nm	380/475	1.5	95-160	15*	11*	9*	4.5*	0.94
This work	Single 2 stage CB cascode MCL	ST B55X 55 nm	380/475	1.5	120-151	13*	9*	7.6*	7.4*	0.86
This work Measured	Single 2 stage CB cascode MCL	ST B55X 55 nm	380/475	1.5	108-154	12.7	?	?	?	0.86

Table 3-6: State of art power amplifiers vs proposed ones, comparing: their topologies, performance metrics, and technology.

As can be seen, the proposed work generally demonstrates a bandwidth that is comparable to, or higher than, that of the state of the art. The gain of 13dB is lower than that of some other reported solutions, but it remains satisfactory. The output power capability is still comparable to that reported in [20], while offering a better PAE. The area, however, remains larger than that of some of the other works.

The reported performance mainly results from the corrected design flow. It is clear that further improvements could be achieved through additional optimization, provided that the appropriate design methodology is used.

Globally, we were able to identify several key reasons for the discrepancies observed between the initial simulations and the measurements. First, the parasitic coupling between the different blocks and their mutual interactions were not properly captured in the original block-by-block flow. Second, the parasitics associated with the base-bias access have a strong impact on the effective output impedance and therefore on the PA optimization, since they directly affect the optimal load seen by the transistor. To address these issues, a TOP-level EM simulation was first carried out, which led to a substantial improvement for all S-parameters, allowing the operating frequency to be correctly centered and the global trends to be recovered. Then, a more complete simulation flow was implemented, this time also including the base-bias access in the EM model. This further improved the agreement, in particular for the output matching and the gain, and allowed us to clearly highlight the impact of the impedance presented at the base on the output impedance seen at the collector in the common-base topology.

Regarding the observed bandwidth reduction, our main hypothesis is that it originates from the simplifications made in the TOP-level EM model, as well as from the limited accuracy of the active-device models, which were validated up to 110GHz. Beyond 110GHz, even a small inaccuracy of only a few percent in some bipolar transistor capacitances can lead to a noticeable frequency shift.

In conclusion, we have demonstrated a good agreement between simulation and measurement for a two-stage PA designed exclusively with in-house passive components. The stand-alone passive structures show a very satisfactory correlation between EM simulation and measurement, thanks to the

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experience in passive design acquired during the first years of the PhD. This is encouraging for the final design of the parallel PA, and it also increases our confidence in the overall simulation methodology.

3.6 3-stages PA

Based on the previously designed power amplifier, we now consider a three-stage PA architecture. The first stage is a cascode amplifier, followed by two common-base (CB) stages. To derive this architecture, we start from the existing two-stage PA and remove its output matching network (MN). We then add an additional CB stage, including its corresponding interstage network and output matching network. The size of the final stage is chosen to meet the targeted output power while ensuring that the preceding CB stage can drive it into saturation. For this purpose, we select an emitter length of $L_{\text{emitter}} = 18\ \mu m$.

Figure 3-52 shows a simplified schematic of the three-stage PA. Block **A** corresponds to the part that is identical to the two-stage PA, while block **B** highlights the additional circuitry introduced in this subsection.

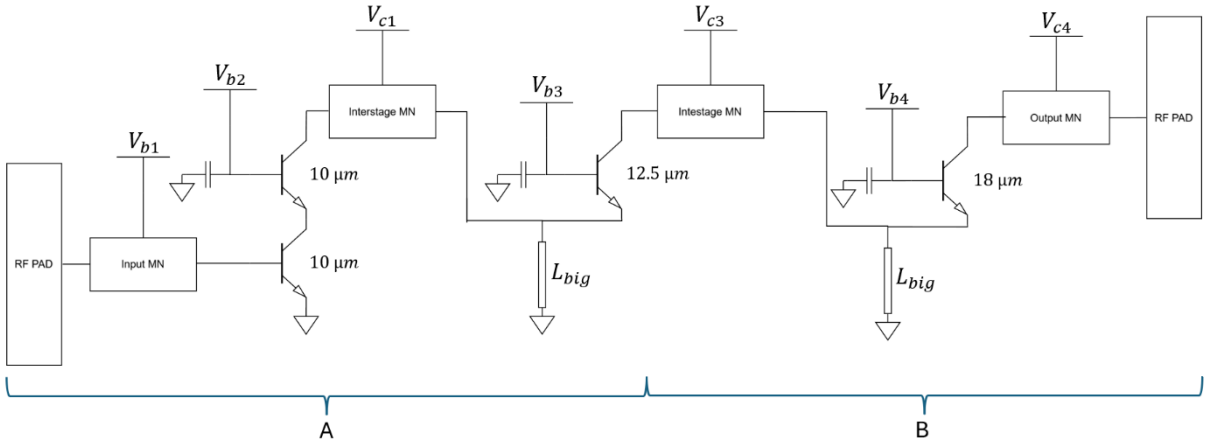


Figure 3-52: Simplifier schematic view of the 3 stages PA with A the part identical to 2 stage PA and B the added part.

The emitter length of each transistor is progressively increased along the signal path: starting from the cascode pair, with an emitter length of 10μm per device, followed by 12.5μm for the first CB stage, and finally 18μm for the CB transistor in the last stage. The topology of both the interstage and output matching networks is identical to that used in the two-stage PA. The interstage network transforms the conjugated optimal load impedance of the preceding stage, $Z^*_{\text{opt,CB1}} = 17\text{-j}43.8\ \Omega$, to the input impedance of the final CB stage, $Z_{\text{in,CB2}} = 7.7+\text{j}2\ \Omega$. The output matching network, including the effect of the pads, is designed such that the conjugated of the optimal load impedance of the second CB stage, $Z^*_{\text{opt,CB2}} = 12.2\text{-j}22.9\ \Omega$, is matched to the reference impedance $Z_0 = 50\ \Omega$. Figure 3-53 presents the corresponding layout occupying an area of $1205\ X\ 1050\ \mu m^2$, with the added circuitry of the third stage highlighted.

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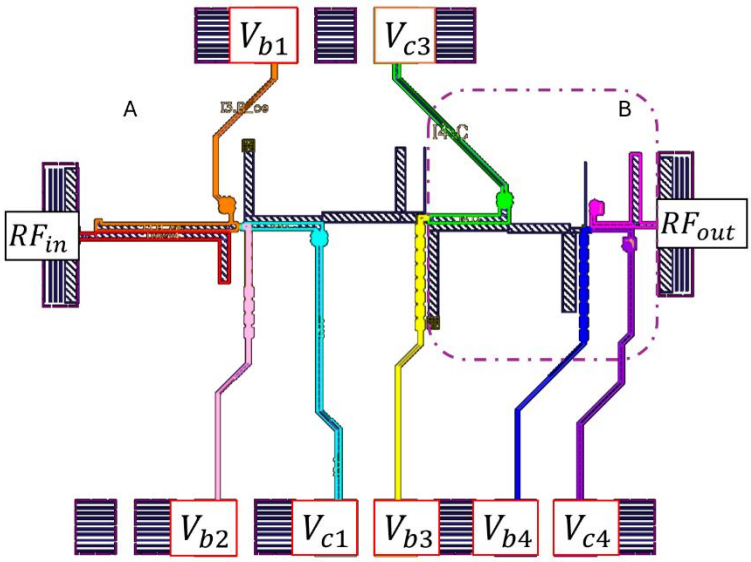


Figure 3-53: Layout view of the three-stage PA, with block **A** corresponding to the part identical to the two-stage PA and block **B** indicating the added circuitry.

The total area of the device under test (Pads included) is $1.2 \times 1\text{mm}^2$. The supply routing and bias access lines are indicated in the layout, while the detailed bias conditions and voltage levels are summarized in Table 3-7.

$\boldsymbol{I_{b1}}$	$\boldsymbol{I_{b2}}$	$\boldsymbol{I_{c1}}$	$\boldsymbol{I_{b3}}$	$\boldsymbol{I_{c3}}$	$\boldsymbol{I_{b4}}$	$\boldsymbol{I_{b4}}$
$20\ \mu A$	$20\ \mu A$	$12.2\ mA$	$18\ \mu A$	$7\ mA$	$25\ \mu A$	$12.1\ mA$
$\boldsymbol{V_{b1}}$	$\boldsymbol{V_{b2}}$	$\boldsymbol{V_{c1}}$	$\boldsymbol{V_{b3}}$	$\boldsymbol{V_{c3}}$	$\boldsymbol{V_{b4}}$	$\boldsymbol{V_{b4}}$
870 mV	$2.12\ V$	$2.5\ V$	$820\ mV$	$1.8\ V$	$820\ mV$	$1.8\ V$

Table 3-7: Bias voltages and the corresponding currents applied to the bases and collectors of each stage. Indices 1 and 2 refer to the two transistors of the cascode stage, index 3 corresponds to the following CB stage, and index 4 to the output power stage.

The result of the SP simulation is shown in Figure 3-54. As a reminder, the transistors and capacitors are modeled using compact device models, while the transistor access lines are included through post-layout extraction (PLS). All remaining passive components are simulated within a single top-level electromagnetic (EM) simulation using RFpro, following the methodology and recommendations described in the previous subsection.

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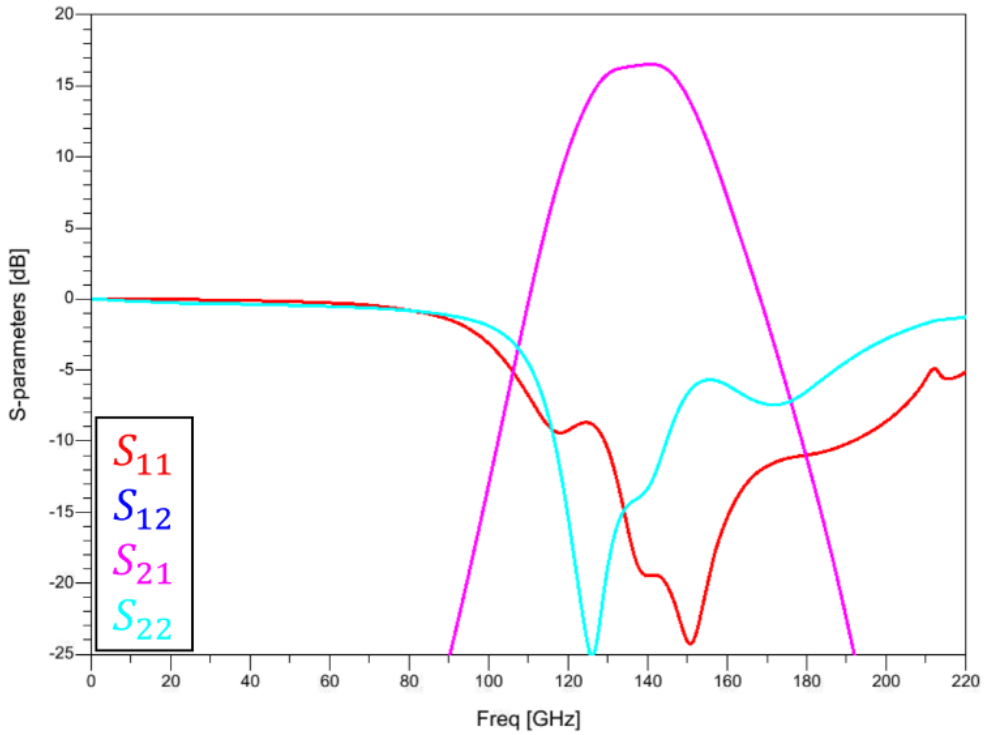
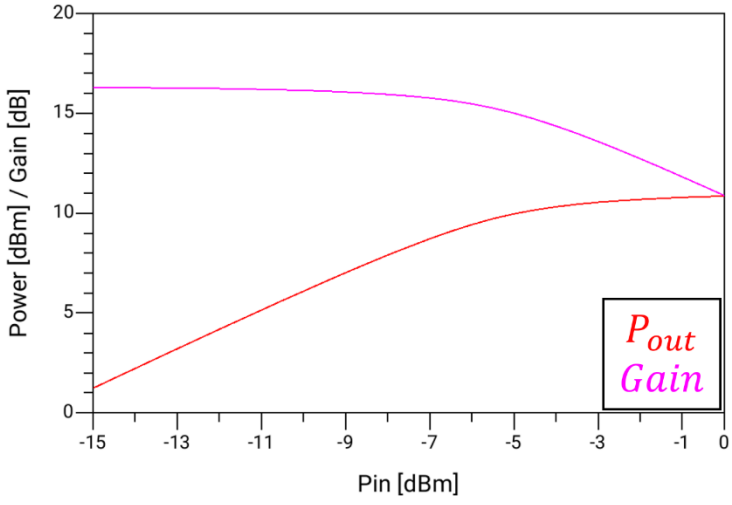


Figure 3-54: TOP-level EM simulation results of the three-stage PA

The three-stage PA exhibits excellent reverse isolation, with an output-to-input isolation better than 30 dB over the entire simulated frequency band. The small-signal gain shows a peak of approximately 17 dB, with a 3dB bandwidth of about 35 GHz. In addition, the input return loss is centered at a slightly higher frequency, and a slight degradation is observed at the lower edge of the band, which is attributed to the impact of the top-level EM simulation.

It is important to note that the initial design of this PA was carried out without applying the recommendations discussed in the previous subsection, since it was submitted for fabrication at the same time as the two-stage PA. This explains the downward shift in the operating frequency, the reduction in bandwidth, and the shift of the return-loss minima. Nevertheless, the overall performance remains satisfactory and fully acceptable for the targeted operating frequency.

Using the same simulation setup, a large-signal analysis is then performed. The corresponding results showing the input power, output power and large-signal gain, are reported in Figure 3-55.



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Figure 3-55: Large-signal simulation results, showing the input power, output power and large-signal gain.

The simulation is performed at 140 GHz instead of 150 GHz to account for the slight downward frequency shift observed in the small-signal analysis. At this frequency, the PA still provides a gain better than 16 dB. The 1dB gain compression point occurs for an input power of -5 dBm, leading to an output P_{1dB} of 10 dBm, which is an excellent result for this frequency range. The saturated output power P_{sat} is around 11dBm, confirming the sharp compression behavior typically associated with common-base stages. Despite the updated and more accurate simulation setup, the output power performance remains very satisfactory. The corresponding power-added efficiency (PAE) is evaluated and presented in Figure 3-56.

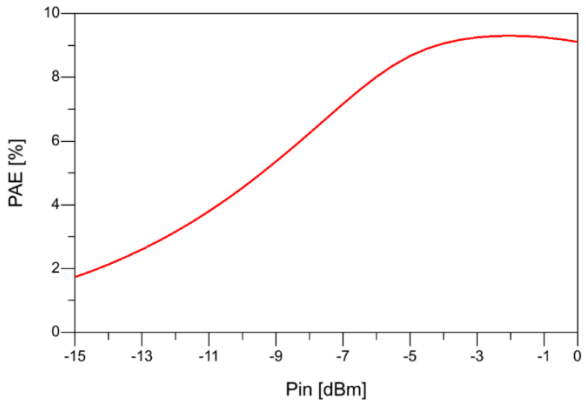


Figure 3-56: The simulated PAE results for the 3 stages PA.

A maximum PAE of 9.3 % is obtained, while the PAE at the 1dB compression point reaches 8.7 %, which remains very reasonable for a three-stage PA operating at this frequency. At 6dB output back-off, the PAE is still around 4 %, i.e., approximately half of the PAE at P_{1dB}. This behavior is very encouraging and further confirms the effectiveness and interest of the current-clamping technique applied to the common-base stages. This can be corroborated by Figure 3-57, which reports the current consumption of the three stages as a function of the output power.

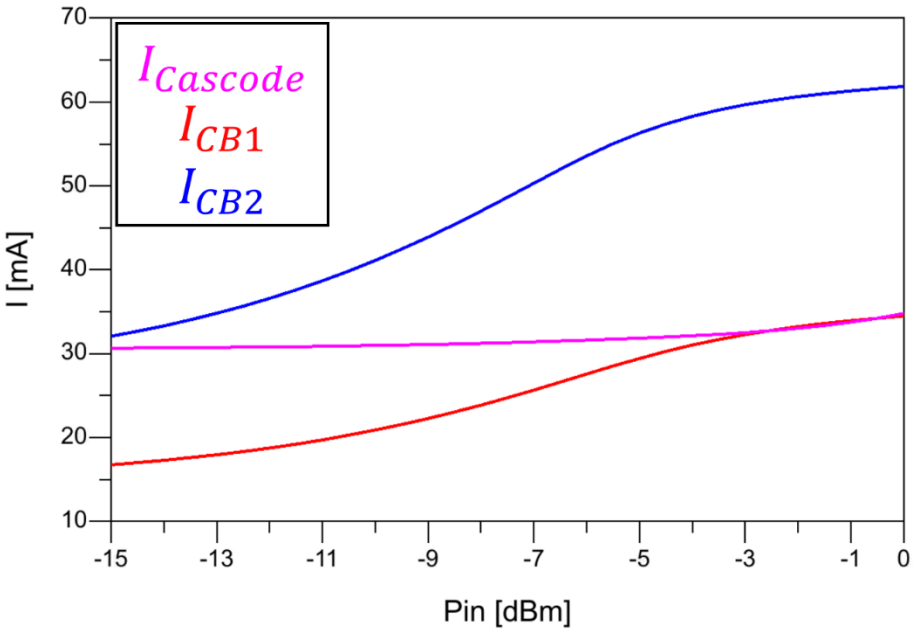


Figure 3-57: Current consumption of each stage of the 3 stages PA

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The current consumption of the cascode stage (plotted in pink) remains essentially constant and does not exhibit any proportional biasing behavior. In contrast, the currents of the two common-base stages evolve in a similar manner and with comparable dynamics, but with different absolute values, as the last stage (plotted in blue) is larger and therefore draws more current to deliver higher output power. This observation further confirms the effectiveness of the current-clamping mechanism applied to the common-base stages.

Table 3-8 present the final comparison of all the PA developed during this section compared to the state of art.

Ref	Topology	SiGe Techno	f_t/f_{max} (GHz)	BV_{CEO} (V)	Frequency (GHz)	Gain (dB)	P_{sat} (dBm)	P_{1dB} (dBm)	$PAE\ @\ P_{1dB}$ (%)	Area (mm^2)
[19]	Single 2 stage cascode	IHP's 130 nm	300/500	1.7	125-146	18.2	15	11	5	0.46
[20]	Differential 2 stage cascode	? 130 nm	?	?	109-119	18.5	11.8	9	<4	0.35
[21]	Balanced 3 stage cascode	IBM's 120 nm	200/250	?	112-128	25.5	17.5	13.3	<3	?
[22]	Single 4 stage CB	ST B55 55 nm	325/375	1.5	125-159	24	17.6	16.8	17.1	0.18
[24]	4-way parallel 2 stage cascode	IBM's 90 nm	300/360	1.7	110-145	18.2	21.9	18.6	9	1.7
This work	Single 1 stage CB	ST B55X 55 nm	325/375	1.5	125-158	4*	15.5*	12*	11*	0.38
This work	Single 1 stage cascode	ST B55X 55 nm	380/475	1.5	100-165	13*	9.5*	6.4*	9*	0.6
This work	Single 2 stage CB cascode	ST B55X 55 nm	380/475	1.5	95-160	15*	11*	9*	4.5*	0.94
This work	Single 2 stage CB cascode MCL	ST B55X 55 nm	380/475	1.5	120-151	13*	9*	7.6*	7.4*	0.86
This work Measured	Single 2 stage CB cascode MCL	ST B55X 55 nm	380/475	1.5	108-154	12.7	?	?	?	0.86
This work	Single 3 stage CB cascode MCL	ST B55X 55 nm	380/475	1.5	122-151	17*	11*	10*	8.7*	1.26

Table 3-8: State of art power amplifiers vs proposed ones, comparing: their topologies, performance metrics, and technology.

The different simulations demonstrate a gain above 16 dB, a P_{1dB} of 10 dBm comparable with [19] and [20] while showing a better PAE at P_{1dB} of 8.7 %, which is very satisfactory despite the updated and more stringent simulation flow. This result is the best globally among all the power amplifiers designed. It is clear that even better performance could be achieved by further optimizing the various matching networks through additional TOP-level EM simulations. Unfortunately, small-signal measurements of this circuit indicate a behavior that suggests potential oscillations, we estimate the oscillation frequency around 7 GHz. Due to time constraints, no corrective action or more in-depth investigation could be carried out.

3.7 Conclusion

In this chapter, several driver and power cells have been designed and analyzed. A detailed study of the cascode and CB topologies has been carried out, highlighting their respective strengths and weaknesses. On the cascode side, the main advantages are a very good gain and an excellent output–input isolation, whereas for the CB topology the key strengths lie in its efficiency, linearity and output-power capability, with a sharp compression profile and a good PAE at 6dB output back-off. The CB cell also exhibits an intrinsic proportional biasing behavior: its DC consumption scales with the

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input power, which makes it particularly attractive for amplitude-modulated signals. In addition, the sharp compression profile improves the linearity and allows higher $P_{1\text{dB}}$ values to be reached.

A first two-stage PA version was then designed, combining the advantages of the two selected topologies, which complement each other rather well. This initial implementation showed promising results, demonstrating the feasibility of D-band PA design in the chosen technology. However, several challenges were identified. First, the numerous series "thru" capacitors used to ensure DC isolation before and after each transistor exhibit mediocre quality factors; custom-designed capacitors turn out to be necessary but remain relatively lossy. Second, the $\lambda/4$-line-based bias-T networks introduce additional losses. Finally, the conventional line-and-stub matching networks, while functional, are relatively area-hungry and lossy.

To address these issues, a new PA architecture was proposed, in both two-stage and three-stage versions, using matching networks based on coupled line (MCL) couplers loaded by stubs, optionally followed by line–stub sections when needed. In this topology, the bias networks are embedded within the matching networks, which greatly reduces the overall losses. The presence of the coupler between input and output naturally provides DC isolation between stages and at the PA input and output, eliminating the need for lossy DC-blocking capacitors. This matching approach enables good matching performance with reduced loss. The comparison between simulation and measurement for the two-stage PA allowed us to identify several issues in our initial design and simulation flow. On this basis, a set of design guidelines was defined. After applying these guidelines—TOP-level EM simulation, explicit modeling of base-access parasitics, careful treatment of pad and bias networks—a very satisfactory agreement between simulation and measurement was obtained, with a measured and simulated gain higher than 14dB and a very good output–input isolation thanks to the cascode driver. Since large-signal measurements could not be performed due to time constraints, the large-signal performance of the DUT is evaluated from the corrected TOP-level simulations. These predict a $P_{1\text{dB}} \approx 7.2$ dBm with a PAE of about 8.4 %, which remains a very good result at these frequencies.

The three-stage PA design shows even better simulated performance in terms of output $P_{1\text{dB}}$ and gain, reaching approximately 10dBm and more than 16dB, respectively. Unfortunately, the measured small-signal behavior exhibits signs of oscillation, and a more in-depth investigation is still required. Nevertheless, the MCL-based matching networks demonstrate several attractive features: increased design flexibility, built-in DC blocking, the ability to bias both the preceding and following stages through the same structure, and a measured behavior in good agreement with EM simulations.

Overall, these investigations confirm the feasibility of D-band PA design in B55X, by simultaneously leveraging the compactness and quality of the passive devices and the current-clamping capability of the common-base topology. It is important to emphasize that no specific effort was devoted to compactness optimization in this chapter; the primary objective was to demonstrate feasibility. However, in the passive-device study, it has been shown that the footprint of passive structures can be significantly reduced by meandering, without degrading their performance.

Finally, a complete power splitter/combiner, including equivalent measurements, has been designed beforehand. Combined with the multi-stage PAs developed in this chapter, the next step—still ongoing at the time of writing—will be the implementation of a parallel PA architecture. Although this final step could not be completed due to time limitations, the feasibility of the approach is supported by stand-alone measurements, and an estimation of the expected performance of the parallel PA will be discussed in the Perspectives section.

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4. Advanced realizations for PA improvement

Regarding the overall implementation, we could not fully complete the original idea of a parallel PA design. Nevertheless, in the passive-device chapter, we demonstrated the feasibility and performance of the power divider, and in the PA chapter, we showed that the two-stage PA is experimentally functional.

Building on these two key results, we now aim to take the concept of a parallel PA to its final stage by quantifying the expected performance through simulations based either on measured RF data or on EM simulations that have already been validated and consolidated through dedicated measurement-to-simulation comparisons. This is why the first subsection of this chapter focuses on the parallel PA and on the performance that can be achieved using the devices already characterized in this work.

In a second step, improving a PA requires considering several aspects simultaneously: the number of stages, parallelization, and the components connecting the different stages, especially the matching networks. For this reason, during this PhD we also investigated innovative components that can positively impact the final PA design, either by improving RF performance or by reducing the overall footprint. In this context, we studied 3D structures such as vertical transmission lines and vertical coupled line couplers, which make it possible to reach a wider impedance range while reducing either the footprint, parasitic coupling, or both. These components can naturally be integrated into the design of the matching networks or power combining/dividing. Based on the advantageous properties of these couplers, we developed a new version of the power splitter/combiner with a significantly reduced footprint, which could be integrated into the PA architecture presented above with the goal of reducing the total circuit area. These three components are the subject of the second subsection, entitled 3D structures.

Finally, as discussed in the state of the art, many reported solutions rely on differential PAs, whereas our approach focuses on parallelization to emphasize output power, which was identified as the main limitation and challenge. Of course, these two architectures can be combined in a long-term perspective to realize a parallel and differential PA. Achieving this would require the development of a divider/combiner that also functions as a balun. To move toward this final objective, we studied a balun based on a 1-to-2 power division principle. A modal analysis and silicon implementations accompany this final subsection.

4.1 Parallel PA

In this subsection, we propose to estimate the performance of the parallelized PA that could not be integrated into silicon during this work. The target architecture is a four-way, multi-stage PA. Since the feasibility of the two-stage PA has already been demonstrated in sub-section 3.5.2, the measured version is used as the amplification cell, i.e., the PA unit cell. A simplified schematic of the overall PA is shown in Figure 4-1.

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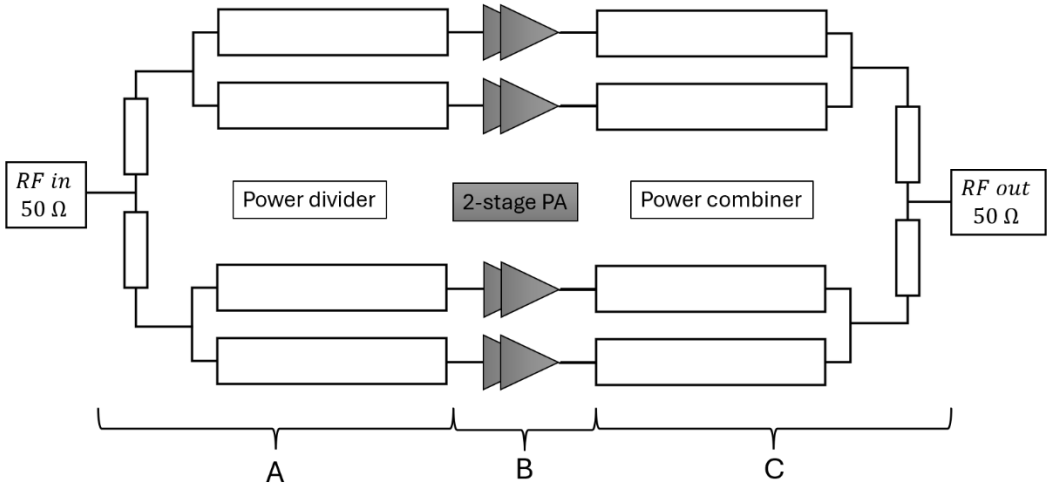


Figure 4-1: Simplified schematic of the 4-way 2-stage PA

As illustrated in Figure 4-1, the complete parallel PA is composed of three main blocks: **A**, the power-splitting device from section **Error! Reference source not found.**; **B**, the amplification device, namely the PA cell, i.e., the two-stage MCL-based PA presented in section **Error! Reference source not found.**; and **C**, the recombination device, which is identical to block A but flipped. For schematic simplicity, the power combiner is drawn without the isolation resistor, although it is present in the layout and in the simulations. It should be noted that, in our case, blocks A and C correspond to the same device, since isolation resistors are used on both sides; however, this is not necessarily the case in most implementations for block A.

The simulated performance of blocks A and C has already been shown to agree very well with measurements. These measurements were performed in two steps, resulting in two 4×4 S-parameter matrices for a five-port device characterization. For simplicity, and since the EM simulations have already been validated by measurement, the EM-simulated power splitter/combiner is used here for blocks A and C.

For block B, i.e., the two-stage PA based on coupled lines matching networks, measured S-parameters are also available and show good agreement with simulation. Therefore, for the small-signal evaluation of the parallel PA, two cases are considered: **Case 1**, using the measured S-parameter file; and **Case 2**, using the simulated S-parameter file. The resulting comparison is presented in the next subsection. The following subsection then addresses the expected large-signal performance. For this part, only the simulated large-signal data for block B can be used, since large-signal measurements were not performed on the two-stage PA due to time constraints.

4.1.1 Small signal performance

The two cases introduced above are detailed in the corresponding schematics.

Case 1: simulation setup is shown in Figure 4-2.



Figure 4-2: simplified view of the figure case 1

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Case 1 is the closest to reality, since the 1-way power-amplification cell is already a measured data.

Case 2: simulation setup is shown in Figure 4-3.



Figure 4-3: simplified view of the figure case 2

In Figure 4-3, the same EM-simulated file is used for the power splitter and power combiner. For the two-stage PA, we use the most accurate TOP-level EM simulated file, which has already shown good agreement with measurement. This approach enables not only a comparison between the two cases in terms of small-signal performance but also provides the only available basis for large-signal qualification.

A small-signal simulation is performed for both cases, and the results are shown in Figure 4-4.

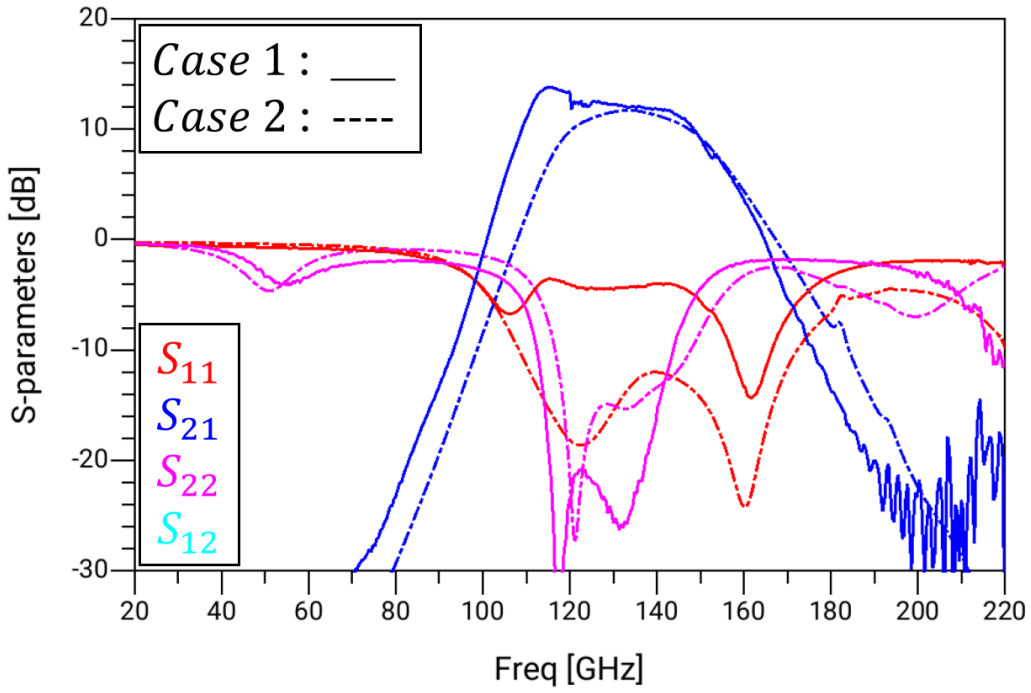


Figure 4-4: Small signal simulation result comparing the figure case 1 and figure case 2

The overall trends are similar between case 1, based on the measured two-stage PA, and case 2, based on the simulated two-stage PA file. In terms of gain, the same slight discrepancy observed previously for the stand-alone two-stage PA is present. However, in the parallelized configuration, both cases exhibit a small gain reduction of about 0.2 dB for the measured case and 0.7 dB for the simulated case, as compared to the two-stage PA. This can be explained, on the one hand, by the additional insertion loss introduced by the passive circuits, which are on the order of 1dB, and on the other hand by a partial compensation from the intrinsic gain of the stand-alone two-stage PA cell, due to the impedance presented by the power combiner, which is not a purely real $50\ \Omega$ load as expected. Therefore, the impedance presented is more suitable for generating slightly higher gain, which explains the slight compensation observed. For example, at 134 GHz, considered as the center frequency in case 1, the stand-alone configuration exhibits 12.2 dB, whereas the parallelized topology shows 12.0 dB. In case 2,

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at the same frequency, the stand-alone value is 12.5 dB, compared with 11.8 dB for the parallelized topology.

In terms of isolation, excellent performance is maintained, with better than 40 dB isolation in all cases. The input return loss preserves the same overall shape, although the mismatch level remains similar to that of the stand-alone two-stage PA. Finally, the output return loss remains better than 10 dB in both cases for a bandwidth of about 40GHz, with good agreement between them.

Overall, the agreement between the two cases can be considered as good. This is particularly important for the next subsection, since case 1 cannot be used for large-signal qualification. As a result, this study justifies the use of case 2 for the large-signal analysis, while also confirming its accuracy with respect to case 1, which is closer to reality.

4.1.2 Large signal qualification of the 4-way 2-stage PA

To quantify the expected large-signal performance of the four-way PA, case 2 was used. The objective is to compare the improvement obtained by moving from a single-path PA to a multi-path parallel architecture. To this end, the input and output powers of the complete device are simulated, as illustrated in Figure 4-5, together with the corresponding gain.

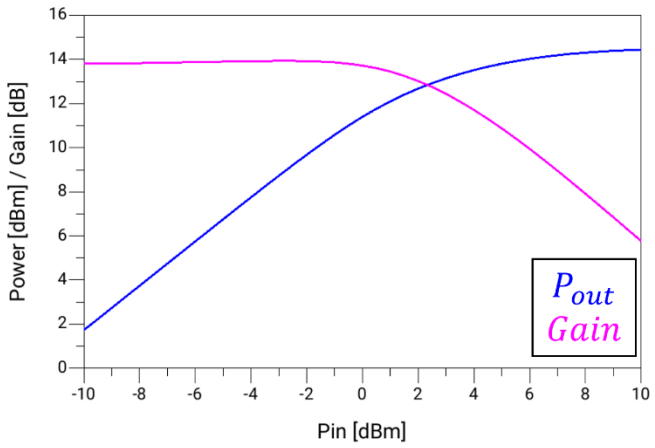


Figure 4-5: Large signal simulation result for 4-way 2-stage PA (133.5 GHz).

The large-signal simulation is performed at 133.5 GHz, which corresponds to the gain peak of the circuit. Overall, a gain of about 13.8 dB is recovered. The 1dB compression point is obtained at $P_{out1\text{dB}} \approx 13$ dBm, with a saturated output power of approximately $P_{\text{sat}} \approx 14.5$ dBm. These results still demonstrate a sharp compression profile and high output power. Compared with the stand-alone two-stage PA, which exhibits a similar gain above 13 dB, a $P_{1\text{dB}}$ of 7.2 dBm, and a P_{sat} of 8.8 dBm, the parallelized version provides a clear improvement. The gain remains slightly higher, which can be explained by the new load impedance presented by the power combiner, which is not a purely real 50 Ω load. More importantly, the output $P_{1\text{dB}}$ increases from 7.2 dBm to 13 dBm, corresponding to an improvement of 5.8 dB, i.e., nearly a fourfold increase in output power. Similarly, P_{sat} improves from 8.8 dBm to 14.5 dBm, i.e., by 5.7 dB. This improvement is mainly due to the parallelization itself, but it is also enhanced by two favorable factors: first, the very low insertion loss of the power splitter/combiner developed in the passive-device section; and second, the output impedance presented by the combiner, which is not a purely 50 Ω real load and therefore brings each PA cell closer to its optimal load impedance, helping maximize P_{out}.

Power consumption, through the PAE, is analyzed next. The corresponding simulation results are shown in Figure 4-6.

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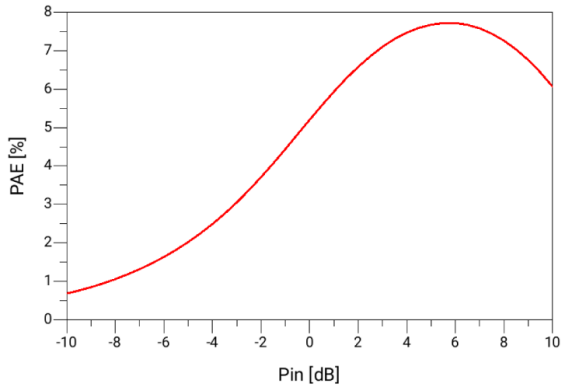


Figure 4-6: Simulated PAE of the 4-way 2-stage PA

As can be seen, when comparing the parallelized topology with the non-parallelized version, a slight reduction in PAE is expected. The detailed comparison is given in Table 4-1.

	$non\ parallelized\ PA$	$Parallelized\ PA$
PAE_{max}	9.5 %	7.7 %
PAE_{P1dB}	7.4 %	6.9 %
PAE_{6dB}	3.2 %	2.8 %

Table 4-1: max PAE, at P1dB, and at 6 dB of back off for the non parallelized PA vs the parallelized one (presented in this sub section)

The impact of 4 way parallelization on PAE is in fact very small. For example, at $P_{1\text{dB}}$, the PAE decreases from 7.4% to 6.9%, i.e., a difference of only 0.5%, which is almost negligible. This small loss was expected and can be explained by the insertion loss introduced by the power splitter and power combiner. More intuitively, the input power remains the same but is divided among the four paths, the output power is ideally multiplied by four minus the losses of the splitter and combiner, and the DC consumption is also multiplied by four. In the ideal lossless case, the PAE should therefore remain unchanged. The fact that the simulated PAE is only very slightly degraded confirms the excellent performance of the power splitter/combiner developed in the passive-devices section, which exhibits much lower losses than conventional 1-to-4 splitter/combiner structures.

We now summarize the impact of parallelization by comparing both small-signal and large-signal performance. The main metrics considered are $P_{1\text{dB}}$, P_{sat}, Gain, PAE at $P_{1\text{dB}}$, and PAE at 6 dB output back-off.

	$P_{1dB}\ [dBm]$	$P_{sat}\ [dBm]$	$Gain\ [dB]$	$PAE_{P1dB}\ [\%]$	$PAE_{6dB}\ [\%]$
$non\ parrallel$	7.2	8.8	13	7.4 %	3.2 %
$parallel$	13	14.5	13.8	6.9 %	2.8 %

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Table 4-2: Performance recap and comparison of the 4-way 2-stage PA versu 1-way 2-stage PA.

As shown in Table 4-2, the gain is slightly improved in large signal, together with a huge improvement of about 5.8 dB in P_{1dB}, corresponding to nearly a factor of four in output power. The PAE remains almost unchanged. In a sense, parallelization allows us to increase the final output power by relaxing the constraints on each stand-alone PA cell, without significantly degrading the gain or the efficiency of the circuit.

Table 4-3 shows the comparison of this version of parallel PA with the other single PA developed along with the state of art PA.

Ref	Topology	SiGe Techno	f_t/f_{max} (GHz)	BV_{CEO} (V)	Frequency (GHz)	Gain (dB)	P_{sat} (dBm)	P_{1dB} (dBm)	PAE @ P_{1dB} (%)	Area (mm^2)
[19]	Single 2 stage cascode	IHP's 130 nm	300/500	1.7	125-146	18.2	15	11	5	0.46
[20]	Differential 2 stage cascode	? 130 nm	?	?	109-119	18.5	11.8	9	<4	0.35
[21]	Balanced 3 stage cascode	IBM's 120 nm	200/250	?	112-128	25.5	17.5	13.3	<3	?
[22]	Single 4 stage CB	ST B55 55 nm	325/375	1.5	125-159	24	17.6	16.8	17.1	0.18
[24]	4-way parallel 2 stage cascode	IBM's 90 nm	300/360	1.7	110-145	18.2	21.9	18.6	9	1.7
This work	Single 1 stage CB	ST B55X 55 nm	325/375	1.5	125-158	4*	15.5*	12*	11*	0.38
This work	Single 1 stage cascode	ST B55X 55 nm	380/475	1.5	100-165	13*	9.5*	6.4*	9*	0.6
This work	Single 2 stage CB cascode	ST B55X 55 nm	380/475	1.5	95-160	15*	11*	9*	4.5*	0.94
This work	Single 2 stage CB cascode MCL	ST B55X 55 nm	380/475	1.5	120-151	13*	9*	7.6*	7.4*	0.86
This work Measured	Single 2 stage CB cascode MCL	ST B55X 55 nm	380/475	1.5	108-154	12.7	?	?	?	0.86
This work	Single 3 stage CB cascode MCL	ST B55X 55 nm	380/475	1.5	122-151	17*	11*	10*	8.7*	1.26
Design in progress	4-way parallel 2 stage CB cascode MCL	ST B55X 55 nm	380/475	1.5	117-151	13*	14.5*	13*	6.9*	?

Table 4-3: State of art power amplifiers vs proposed ones, comparing: their topologies, performance metrics, and technology.

As can be seen, this work provides the best overall result among all the proposed designs in this document. With a gain of 13 dB, it remains lower than that of some other reported works, but this was not the main objective, and it remains quite acceptable. In terms of output power capability, this work achieves the third-best performance, particularly with respect to P_{1dB}, which reaches 13dBm, on par with [21]. The best output-power performances are obtained by the parallel PA and the CB-based design, which were the two main inspirations for this work. The PAE remains satisfactory and is better than those reported in [19], [20], and [21]. Unfortunately, due to the corrections applied to the design flow, we could not surpass the state of the art. This could nevertheless be achieved by starting from a better optimized unit cell, whether a two, three, or four stage PA based on cascode and CB topologies, combined with matching networks based on microstrip coupled lines.

Of course, further improvements are still possible. The purpose of this subsection was primarily to evaluate, on a realistic measured case, the impact of parallelization. It clearly shows a drastic improvement in output power, with no major penalty in gain or PAE, thanks to the excellent performance of the power divider/combiner. The price to pay is the area consumption but this wasn't explored yet.

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We have also to consider that the two-stage PA cell developed in this thesis was not fully optimized, due to limitations in the simulation and design methodology at the design time. For reference, not all parasitic effects were included in our initial design flow. As a result, the building blocks used in this subsection are much more realistic, but they come from the corrections applied to the simulation flow and are therefore not fully optimized.

Now that we are more confident in these design steps and in the correlation between simulation and measurement, the next logical step would be to apply this parallelization strategy to a better optimized two- or three-stage PA cell. This would make the four-way architecture capable of competing with the best reported state-of-the-art [22] and [24].

4.2 3D structures

Traditionally, and as reflected in the state of the art, D-band PAs are implemented using microstrip lines, microstrip couplers, baluns, or power dividers/combiners. These solutions are functional and relatively easy to design, to the point that several foundries provide standard microstrip line models in their design kits. However, they also present several limitations in terms of footprint, achievable minimum and maximum characteristic impedances, and parasitic coupling, among others.

We therefore sought to take advantage of the richness of the B55X back-end stack, which provides two thick metal layers to enable the design of components that we refer to as 3D structures. This term comes from the fact that, in this approach, the design is no longer restricted to a single 2D metal layer; instead, it spans multiple metal layers simultaneously. In practice, this corresponds to taking well-known planar topologies and rotating them by $90°$ into a more vertical implementation. We expect these 3D structures to better address the constraints and requirements identified above.

To this end, several investigations were carried out by Roua Djebbi, a postdoctoral researcher whom I co-supervised to push forward this idea that I proposed. The first study concerned the design of 3D circuits, starting from a simple vertical transmission line intended to achieve higher max and lower min characteristic impedances and lower sensibility to parasitic coupling that is becoming harder to manage in D band, without taking large security distance compared to classic µstrip lines, while assessing the quality factor of this topology. A second investigation was then carried out into 3D couplers with the same objective. Some versions of these basic building blocks were fabricated and measured.

Based on these results, a 3D version of the power splitter was proposed. This work was carried out by the internship student Lucas Eimrich de Sousa, whom I supervised.

This subsection is organized as follows: the first part addresses the vertical strip lines; the second part presents the vertical couplers; and the third part introduces the new version of the power divider I proposed, which is also based on vertical couplers.

4.2.1 3D Vertical transmission lines

Traditionally, a large majority of D-band designs rely on conventional microstrip lines: wide ground planes with a signal strip of prescribed width and length, as illustrated in Figure 4-7.

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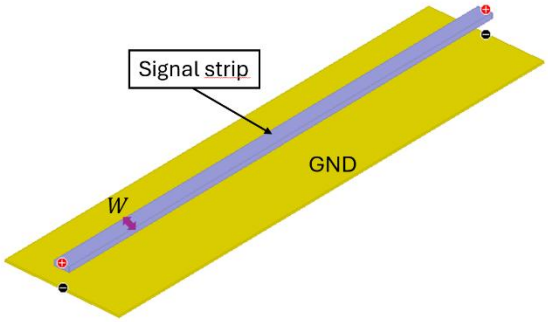


Figure 4-7: 3D view of the classical µstrip line with signal on M7 and GND on M5

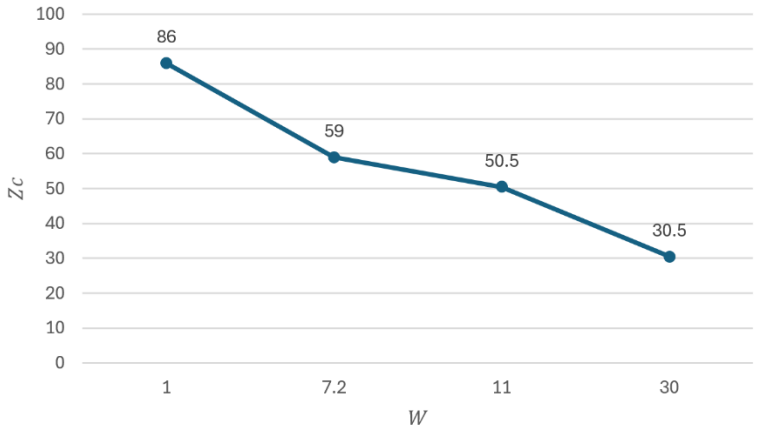
In this configuration, the capacitance C of the transmission line is largely determined by the strip width W. The same width also affects the inductance L of the line. Ultimately, the characteristic impedance of a microstrip line, which depends on L and C, is directly related to W. Since the substrate height h is fixed in an integrated implementation, the available design freedom is limited. Of course, it is possible to use other metal layers, but in the passive enablement section we adopted the convention of using the signal strip on M7 and the ground plane on M5, which appears to be the most suitable choice for our application. Moreover, the variation of h remains low, even if we use M1-M2 to build the ground, with limited gain in maximum characteristic impedance value. A sweep was performed from the minimum to the maximum strip width, i.e., $[1,30]$ μm, in order to extract, on the one hand, the achievable characteristic impedance range and, on the other hand, the quality factor and insertion loss. The length of the simulated microstrip line was 240 µm. The results are summarized in Table 4-4.

W [µm]	Z_c [Ω]	Q	IL [dB/mm]
1	86	25.6	1.0
7.2	59	32.7	0.76
11	50.5	33.2	0.75
30	30.5	34.5	0.73

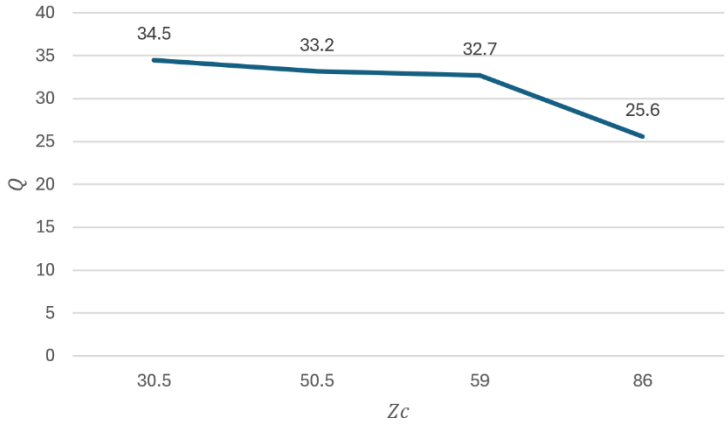
Table 4-4: Physical parameters (width and length) of a microstrip line versus electrical parameters (characteristic impedance, quality factor and insertion loss)

To better visualize the behavior of these parameters, the characteristic impedance is plotted as a function of the strip width W, as shown in Figure 4-8(a). The quality factor is also plotted as a function of the characteristic impedance in Figure 4-8(b).

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(a)



(b)

Figure 4-8: Curves showing (a) the characteristic impedance of a microstrip line as a function of its width W, and (b) the quality factor as a function of the characteristic impedance of the same microstrip line

The minimum strip width for thick metal is $0.6\ \mu$m, but for better accuracy and to avoid abrupt process sensitivity, we limited the minimum width to $1\ \mu$m. The maximum width allowed by the foundry is $30\ \mu$m. These two limits correspond to a characteristic impedance of approximately $86\ \Omega$ and $30\ \Omega$, respectively. We therefore consider these values as the minimum and maximum characteristic impedances achievable with our setup, i.e., the B55X 7ML technology using a signal strip on M7 and ground on M5.

Regarding the quality factor, at 150 GHz, values better than 30 are obtained for characteristic impedances below $60\ \Omega$. The quality factor decreases to about 25 for an $86\ \Omega$ microstrip line, corresponding to a $1\ \mu$m strip width.

4.2.1.1 3D Vertical line topology

For the vertical line, we conceptually rotate the microstrip by $90°$. The M7 and M6 layers are then stacked to form the signal strip on one side and the ground strip on the other side. Fig. Figure 4-9 shows a 3D view of the proposed vertical transmission line.

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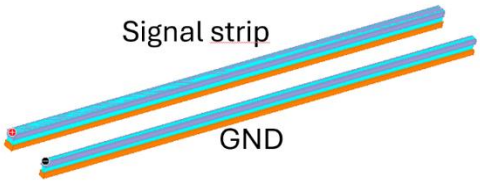


Figure 4-9: 3D view of the vertical transmission line

To better visualize the geometry, Figure 4-10 shows a cross-section of the vertical transmission line.

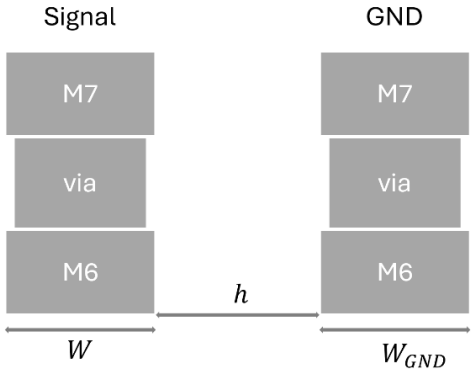


Figure 4-10: Cross-section view of the vertical transmission line

In this case, the characteristic impedance is mainly determined by the distance h between the signal and ground strips, a parameter that in a classic µstrip line is fixed by the technology stack. To investigate the potential of this topology compared to the conventional microstrip line, several sweeps were performed for a fixed line length. We first fix W and W_{GND}, and vary h, since this is the main parameter affecting the characteristic impedance of the vertical line. After several attempts, we retained what we considered to be a good trade-off, with both signal and ground strip widths set to:

$$W = W_{\text{GND}} = 3\ \mu\text{m}.$$

We then sweep the spacing h between the signal and ground strips over the range $[1,20]\ \mu$m. Again, the minimum gap is around $0.6\ \mu$m, but we choose $1\ \mu$m for better accuracy. The maximum value $h = 20\ \mu$m was selected to keep the DUT reasonably compact, although higher values would also be possible. The result of main figures of merit are shown in Table 4-5.

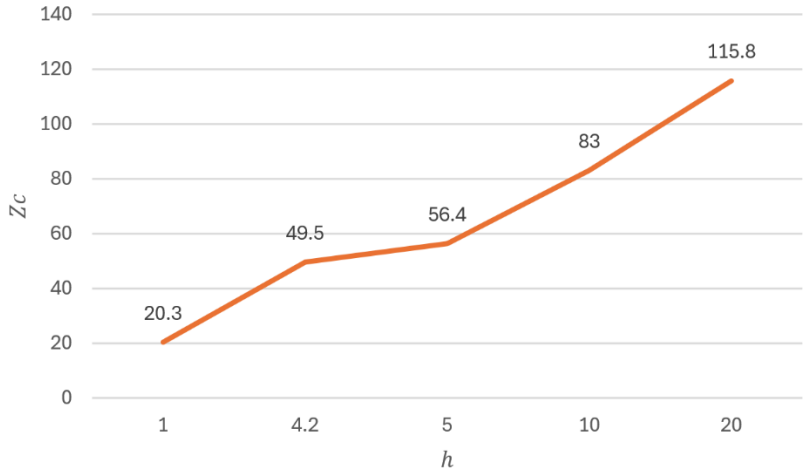
W (µm)	h (µm)	W_{GND} (µm)	$Z_{c\ (\Omega)}$	Q	$IL\ (dB/mm)$
3	1	3	20.3	7.2	3.9
3	4	3	49.5	19.2	1.4
3	5	3	56.4	21.5	1.2
3	10	3	83	27.2	0.9

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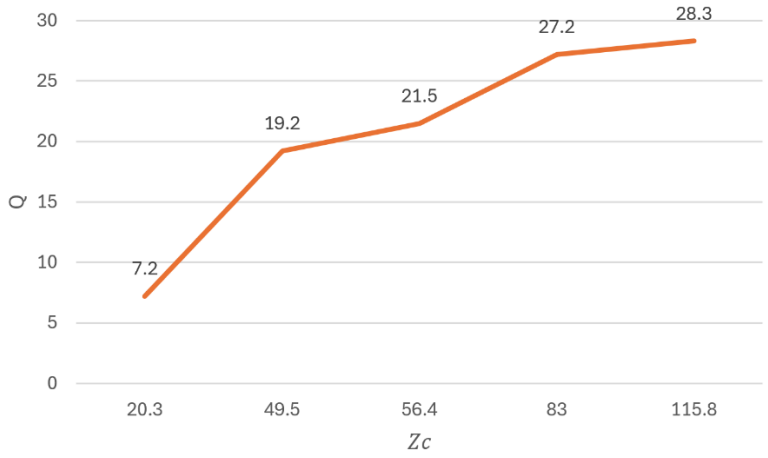
3	20	3	115.8	28.3	0.9

Table 4-5: Physical parameters (signal strip width, ground width, and spacing h) of a vertical transmission line with $W = W_{GND} = 3\ \mu$m, versus electrical parameters (characteristic impedance, quality factor and insertion loss)

As before, the characteristic impedance is plotted as a function of the spacing h, as shown in Figure 4-11(a), and the quality factor is plotted versus the characteristic impedance in Figure 4-11(b).



(a)



(b)

Figure 4-11: Curves showing (a) the characteristic impedance Z_C of a vertical transmission line with $W = W_{GND} = 3\ \mu$m as a function of h, and (b) the quality factor as a function of the characteristic impedance of the same vertical line

The minimum characteristic impedance obtained at $h = 1\ \mu$m is very low, much lower than in the microstrip case ; we obtain $Z_c = 20.3\ \Omega$. Conversely, at the upper end of the range, $h = 20\ \mu$m, the maximum characteristic impedance reaches $Z_c = 115.8\ \Omega$.

The quality factor remains generally acceptable but drops below 20 for characteristic impedances below $50\ \Omega$, reaching about 7 for $20\ \Omega$. On the other hand, the quality factor increases with characteristic impedance as h increases, reaching approximately 28 for $115\ \Omega$.

In summary, the classical microstrip line offers a better quality factor over most of the characteristic impedance range, except at very high characteristic impedances. For example, at $86\ \Omega$,

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the quality factor of the classical microstrip is 25, whereas for the vertical line at $84\ \Omega$, it is 27.9. Thus, the vertical line provides a better quality factor at high characteristic impedances.

Regarding the achievable characteristic impedance range, the classical microstrip is limited to approximately 30 to $86\ \Omega$ with our setup, whereas the vertical line can span from about 16 to $118\ \Omega$. This makes it possible to address matching networks for applications requiring very low impedances—particularly PA output stages with large emitter lengths, where very low impedances are common. It also enables applications such as 1-to-N Wilkinson power dividers with $N > 2$; for example, a direct 1-to-4 implementation becomes feasible, since the required characteristic impedance is $100\ \Omega$, which is readily achievable with a very reasonable quality factor. By contrast, this is simply not feasible with a conventional microstrip line.

Finally, regarding footprint, a conventional $50\ \Omega$ microstrip line is nearly indispensable in most designs. In our setup, the microstrip requires a width of about $11\ \mu$m, whereas the vertical topology can realize $50\ \Omega$ with $W = 1\ \mu\text{m}, W_{\text{GND}} = 3\ \mu\text{m}, \text{and}\ h = 4.2\ \mu\text{m}$, for a total lateral width of only $8.2\ \mu$m. Moreover, lateral fringing is very small in the vertical topology, unlike in the classical one, where a keep-out region of approximately $4h + W$ must be considered. For a $50\ \Omega$ line, this corresponds to about $40\ \mu$m, preventing the insertion of other circuits in that region.

This study clearly demonstrates the interest of the vertical transmission line topology, which offers a much wider characteristic impedance range and a better quality factor at high characteristic impedance, as compared to conventional microstrip lines.

4.2.1.2 Fabrication

To verify the feasibility and accuracy of the simulations, two versions of the vertical transmission line were fabricated: one designed for a characteristic impedance of $50\ \Omega$ and one for $100\ \Omega$. For $50\ \Omega$, the chosen dimensions are $W = 3\ \mu$m and $h = 4\ \mu$m, for a total width of $10\ \mu$m. The length is 250μm. The layout of the $50\ \Omega$ vertical line is shown in Figure 4-12.

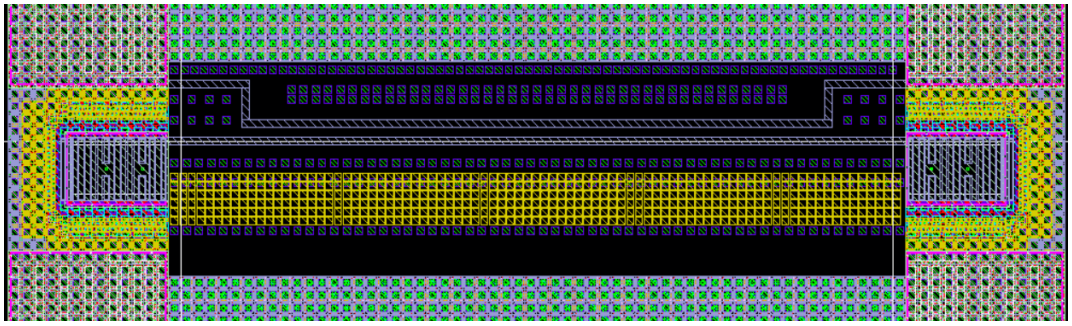
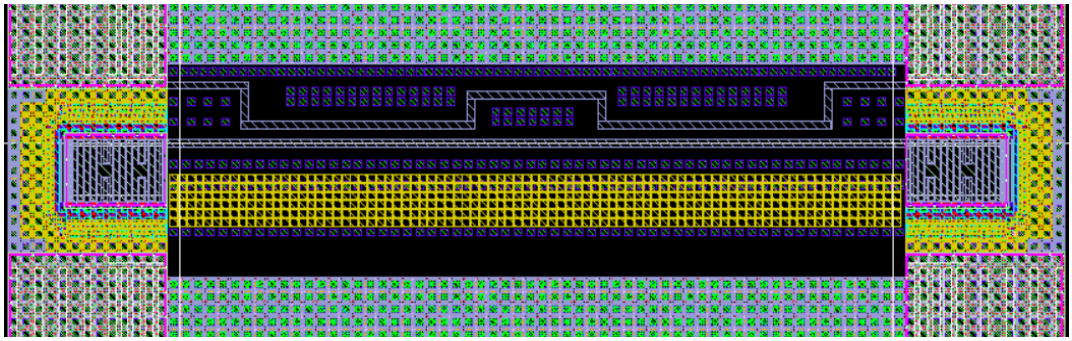


Figure 4-12: Layout view of the 50 Ω vertical line sent to fabrication

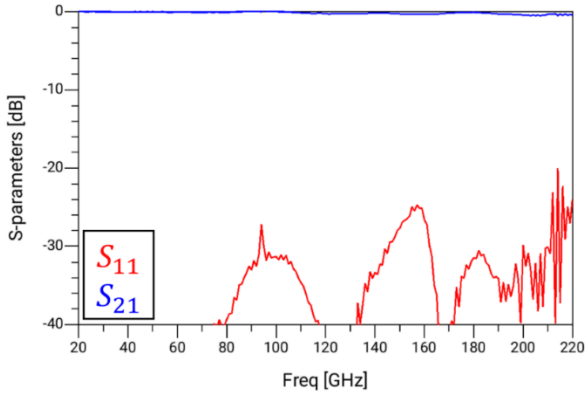
For the $100\ \Omega$ case, the chosen dimensions are $W = 3\ \mu$m for both signal and ground strips, and $h = 16\ \mu$m. The corresponding layout view is shown in Figure 4-13.



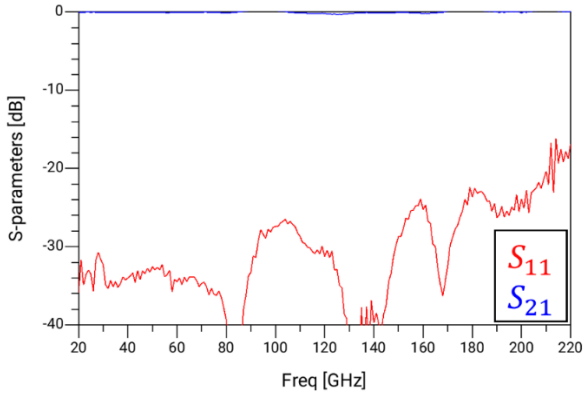
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Figure 4-13: Layout view of the 100 Ω vertical line sent to fabrication

The de-embedded and normalized ($Z_c = Z_o$ with Z_c characteristic impedance of the Tline and Z_0 the impedance of the ports) measurement results of both devices are shown in Figure 4-14(a) and Figure 4-14(b), for the $50\ \Omega$ and $100\ \Omega$ vertical lines, respectively.



(a)



(b)

Figure 4-14: Measurement results of the two vertical transmission lines, where (a) shows the de-embedded result of the $50\ \Omega$ line and (b) shows the de-embedded result of the $100\ \Omega$ line, normalized to $100\ \Omega$.

From both figures, excellent matching over a wide bandwidth is observed. This demonstrates, on the one hand, the functionality of the vertical structures and, on the other hand, the accuracy of the simulated characteristic impedance.

Looking more closely to the insertion loss, Figure 4-15 shows the measured insertion loss of the $50\ \Omega$ vertical line. Unfortunately, a layout issue was identified for the $100\ \Omega$ line.

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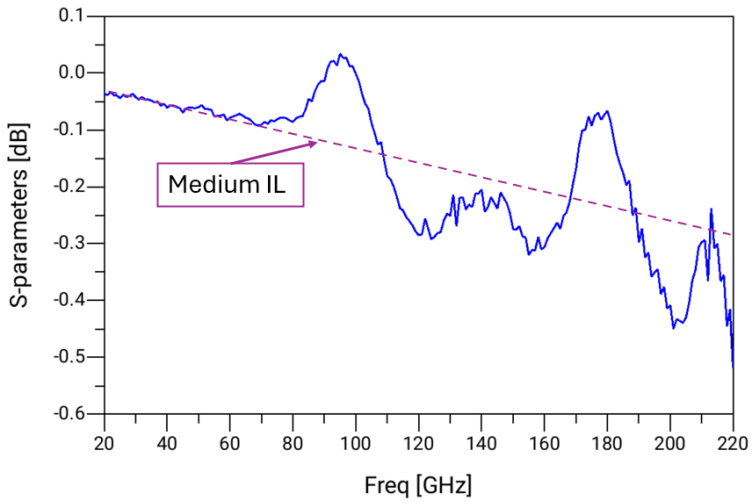


Figure 4-15: Measured insertion loss of the $50\ \Omega$ vertical transmission line with a length of 250 µm

Some oscillations can be observed due to calibration errors that have not yet been fully resolved. If these calibration artifacts are ignored, the dashed pink curve in Figure 4-15 represents the expected loss without calibration errors. The result is excellent, with an insertion loss of about 0.2 dB at 150 GHz for a length of $250\ \mu$m, which is close to $\lambda/4$. This is comparable to what is obtained with a $50\ \Omega$ microstrip line. In addition, this topology also makes it possible to reach much higher impedances, as illustrated by the $100\ \Omega$ line, which is simply not achievable with a microstrip line in most integrated technologies.

4.2.2 3D vertical coupler

4.2.2.1 Topology presentation and basic theory

In the previous subsection, the interest of vertical transmission lines was demonstrated. We now extend this concept to coupled lines and investigate whether a **3D vertical coupler** can provide an attractive alternative to conventional microstrip couplers.

In the proposed topology, the structure follows the same coupling principle as a classical microstrip coupler, except that the two coupled signal conductors are no longer connected through a via between M7 and M6. Instead, they are kept separated, resulting in two identical parallel bars facing a ground plane implemented by stacking M6 and M7 over the same length. Figure 4-16 shows a 3D view of the proposed vertical coupler.

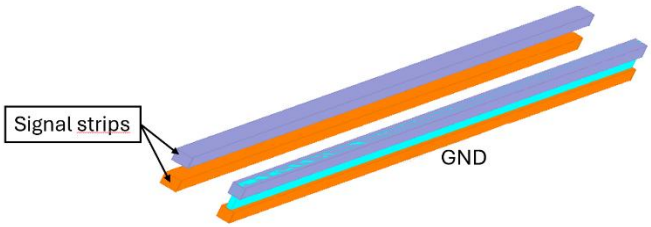


Figure 4-16: 3D view of the vertical coupler

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To better visualize the structure, Figure 4-17 presents a cross-section of the vertical coupler.

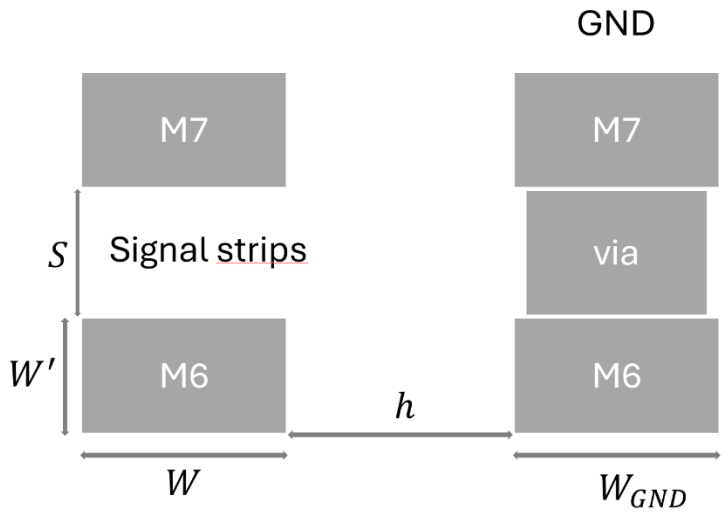


Figure 4-17: Cross-section of the proposed vertical coupler

If we transpose the capacitance model developed for a 2D planar coupler to this 3D vertical configuration, the same physical coupling principle remains valid: the conductors are still coupled through their proximity, but the geometry is now vertically stacked rather than horizontally arranged. In this sense, the vertical coupler can be interpreted as a $90°$ rotation of the conventional 2D structure. The essential electromagnetic behavior is therefore preserved, and the even- and odd mode capacitances can still be defined as follows for a first approximation:

$$C_{odd} = \mathcal{E}_0 \cdot \mathcal{E}_r \cdot \frac{W \cdot l}{S}$$

$$C_{even} = \mathcal{E}_0 \cdot \mathcal{E}_r \cdot \frac{W' \cdot l}{h}$$

With:

$\mathcal{E}_0$: the vacuum permittivity

$\mathcal{E}_r$: the relative permittivity of the dielectric

l : the length of the coupled lines

The remaining parameters are the physical dimensions indicated in Figure 4-17. In the case of the vertical coupler, the even- and odd mode capacitances, C_{even} and C_{odd}, are mainly controlled by the geometric parameters W and h, since W' and S are fixed by the design rules of the technology. More specifically:

C_{odd} is directly related to the conductor width W: increasing W increases C_{odd}, and hence reduces the odd mode characteristic impedance Z_{odd}; C_{even} is mainly controlled by the distance h between the conductors and the ground plane: increasing h reduces C_{even} and therefore increases the even mode characteristic impedance Z_{even}.

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4.2.2.2 Parametric study

A parametric sweep was then carried out to determine the range of characteristic impedances achievable with the different configurations, while confirming the trends predicted by the capacitances simple model. The following ground configurations were investigated:

- **M5 to AP**, with a width of $3\ \mu$m, $5\ \mu$m, or $10\ \mu$m;
- **M6 to M7**, with a width of $3\ \mu$m, as shown in Figure 4-17.

At least four simulation points were used to reach the extremities of each abacus. The coupled line width was swept over $W = [1,30]\ \mu$m, while the spacing between the signal and ground strips was varied over $h = [1.5,30]\ \mu$m. The resulting abacuses of the two modal characteristic impedances, Z_e and Z_o, are shown in Figure 4-18.

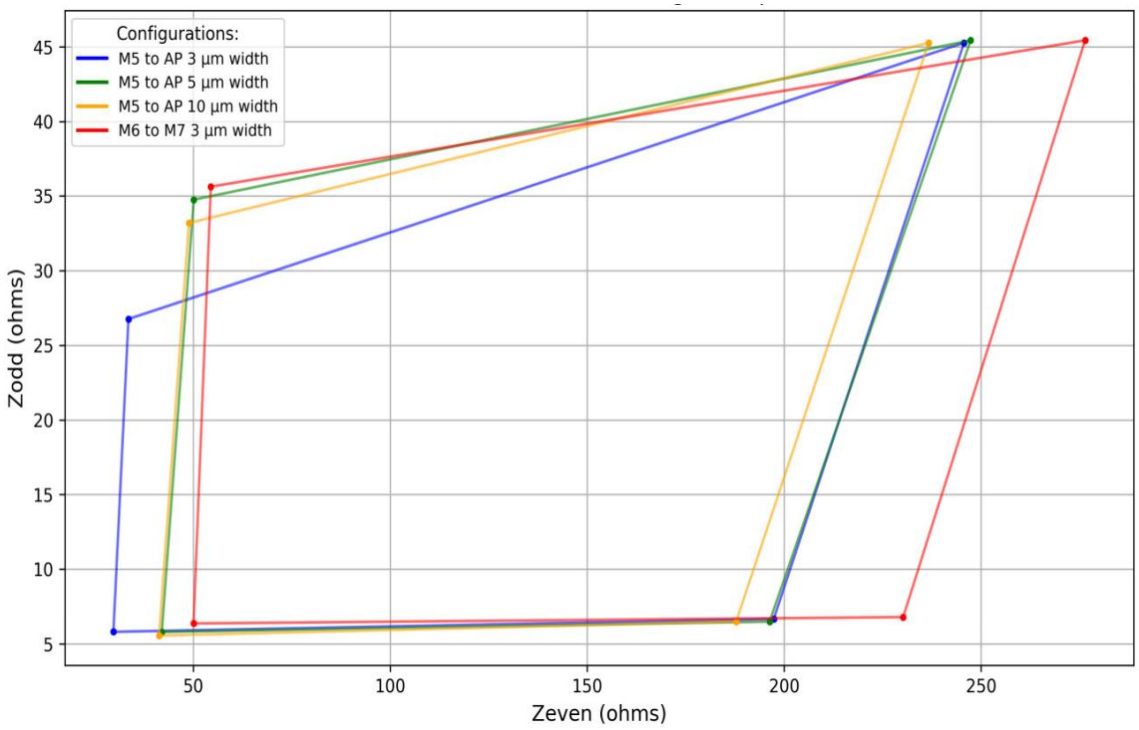


Figure 4-18: Abacus of the different configurations showing the characteristic impedances of the coupler as a function of $W = [1,30]\ \mu$m and $h = [1.5,30]\ \mu$m

As can be seen, the 3D vertical coupler can achieve approximately:

• Z_e: approximately 40–280 Ω

• Z_o: approximately 6–45 Ω

In comparison, the classical microstrip coupler provides:

• Z_e: approximately 50–200 Ω

• Z_o: approximately 15–100 Ω

These results confirm the expected relationships between geometry and modal characteristic impedances: increasing W reduces Z_o, while increasing h increases Z_e.

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Overall, the vertical coupler allows a wider range of modal characteristic impedances as compared to the conventional microstrip coupler, especially in terms of maximum even mode characteristic impedance. The only exception is the maximum odd mode characteristic impedance, where the classical horizontal topology can reach higher values.

This demonstrates that the 3D vertical coupler is a viable alternative to conventional microstrip couplers, offering a wider characteristic impedance range, especially at low characteristic impedances, together with improved design flexibility.

4.2.2.3 Loss comparison for a 3D vertical 3-dB 50 Ω coupler vs classic μstrip

We then compare the insertion loss of the vertical and classical topologies for a standard 3-dB coupler widely used in PA design. For the vertical topology, two different ground-plane configurations were evaluated: **M5 to AP**, with a lateral width of $3\ \mu$m, and **M6 to M7**, also with a width of $3\ \mu$m. The dimensions of each structure were obtained through EM optimization.

For the classical topology, the coupler was designed with: conductor width $W = 2.8\ \mu$m and spacing between the coupled lines $S = 1.2\ \mu$m, with the conductors placed side by side on M7 and the ground plane located below them on M5. The dimensions and insertion loss are summarized in Table 5-5.

Configuration	$Dimensions\ (\mu m, \mu m)$	$Insertion\ loss\ (dB)$
3D – M5 to AP	$(W, h) = (9,7)$	0.36
3D – M6 to M7	$(W, h) = (6.9,6.26)$	0.36
2D planar	$(W_{hor}, S) = (2.8,1.2)$	0.37

Table 4-6: Direct comparison between the planar (2D) and vertical (3D) topologies, both designed for the same target performance: 3 dB, 50 Ω

As can be seen, the insertion loss is very similar across the three configurations. In addition, the vertical implementation is significantly more compact. For the **M5–AP** configuration, with $W_{\text{GND}} = 3\ \mu$m, the total width is: $Width_{tot_{M5,AP}} = 9 + 7 + 3 = 19\ \mu m$. For the **M6–M7** configuration, the total width is: $Width_{tot_{M6,M7}} = 6.9 + 6.26 + 3 \approx 16\ \mu m$. By comparison, the planar 2D coupler must respect a minimum spacing to avoid parasitic coupling, typically at least $20\ \mu$m for each side. This leads to a total width of approximately: $Width_{tot_{2D}} = 20 + 2.8 + 1.2 + 2.8 + 2 \approx 46.8\ \mu m$.

Although the 2D version may appear smaller in layout, it occupies much more area because parasitic coupling forces much larger spacing. This effect is significantly reduced in the vertical configuration, since the fringing fields are oriented vertically rather than horizontally, which relaxes the horizontal spacing constraints.

These results show that the 3D vertical coupler is a promising alternative to the conventional microstrip coupler, with comparable insertion loss, a more compact layout, less impacted by parasitic coupling and, more importantly, access to characteristic impedance regions that are difficult or impossible to reach with standard 2D couplers.

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4.2.2.4 Fabrication

Based on the study carried out in the previous section, two vertical 3-dB couplers, with characteristic impedances equal to 50 Ω and 70 Ω, respectively, were fabricated in B55X. Their dimensions are summarized in Table 4-7.

W [μm]	h [μm]	k	Z_c [Ω]	Z_e [Ω]	Z_o [Ω]
7.9	5.85	−2.96	50.1	121.8	20.6
3.9	10.1	−3.09	71.2	169.7	29.9

Table 4-7: Electrical and physical dimension of the two 3dB couplers embedded into silicon

For measurement simplification, the couplers were not measured as 4-port devices. Instead, they were characterized as 2-port structures by connecting port 1 to the input and port 2 to the isolated port, leaving the thru and coupled ports open. The on-wafer layout views of the 50 Ω and 71 Ω couplers are shown in Figure 4-19 and Figure 4-20, respectively.

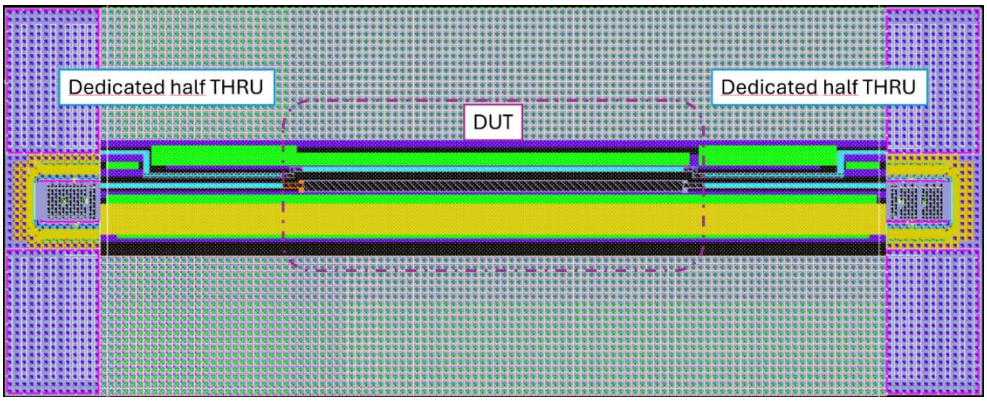


Figure 4-19: Layout view of the vertical 3-dB 50 Ωcoupler embedded in B55X

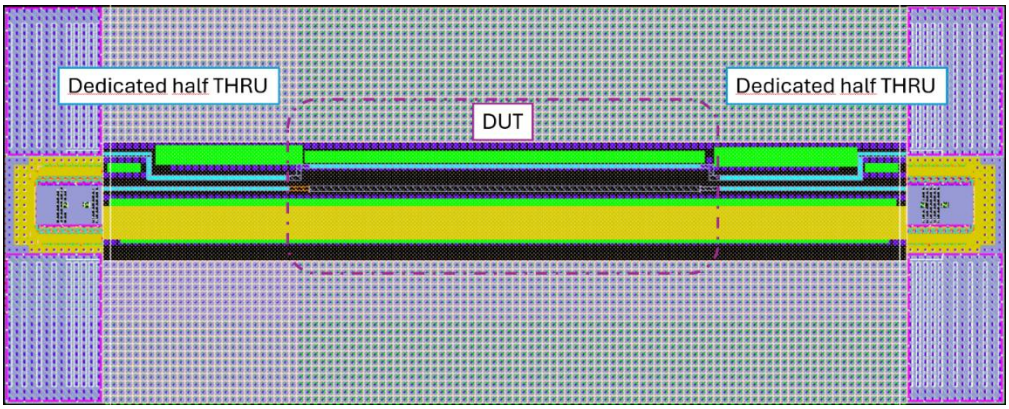


Figure 4-20: Layout view of the vertical 3-dB 71 Ωcoupler embedded in B55X

The measurement setup is identical to the one described previously: GSG probes were used together with a dedicated TRL calibration kit for these 3D structures. The measured results for the 50 Ω vertical coupler are shown in Figure 4-21.

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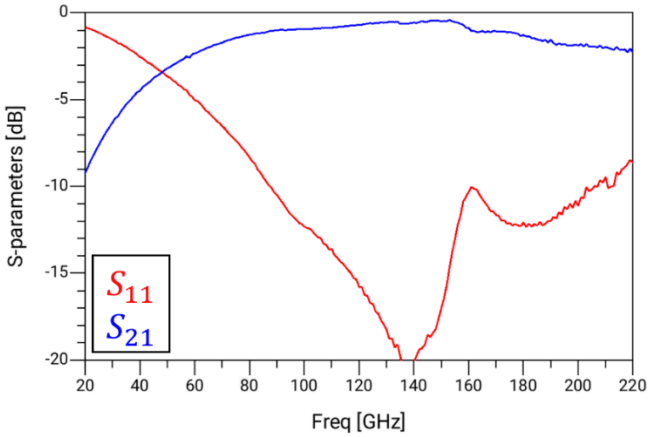


Figure 4-21: S-Parameters measurement results of the vertical 3-dB 50 Ω coupler corrected by TRL

The measured response of the $50\ \Omega$ coupler shows a very wide bandwidth with $S_{11} < -10$ dB from approximately 87 to 206 GHz. The insertion loss is around 0.5 dB at 150GHz, which is an excellent result and comparable to what is obtained with a conventional microstrip coupler. The layout is also much more compact, with a total width of only $W_{\text{tot}} = 16.75\ \mu$m. Some irregularities are visible in the measurement ; they are due to the TRL calibration with a non-ideal transformation from GSG to GS, but these have not yet been investigated in depth.

A second DUT was fabricated for a 3 dB, $71\ \Omega$ coupler, whose layout is shown in Figure 4-20. The corresponding measurement results are shown in Figure 4-22.

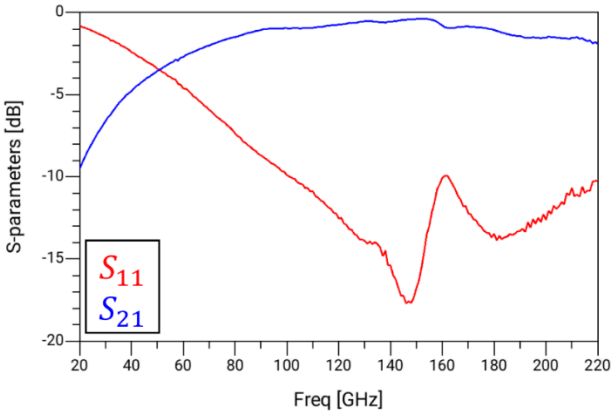


Figure 4-22: S-Parameters measurement result of the vertical 3-dB 71 Ω coupler corrected by TRL

The measured response shows the same irregularities around 160 GHz, which suggests that the issue likely originates from the measurement setup rather than from the DUT itself. This supports the hypothesis of a calibration-related effect and more precisely the calibration kit.

A very wide bandwidth is again observed, with $S_{11} < -10$ dB from about 100 to 220 GHz. The return loss is slightly worse than in the $50\ \Omega$ case. The insertion loss is about 0.4 dB at 150 GHz, which is also an excellent result and again comparable to the conventional microstrip case, while benefiting from a smaller footprint ($W_{\text{tot}} = 17\ \mu$m).

The same overall trend is observed for both couples, as well as a similar shape for the measured curves. This confirms that, despite the change in target impedance, the topology remains highly effective and does not exhibit any critical or excessive loss at either impedance.

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Overall, the measurements confirm the correct operation of the topology and show very low losses, which is highly encouraging. The measured irregularity around 160 GHz remains unexplained due to time constraints, although the TRL calibration kit remains the most likely source.

4.2.3 Novel power splitter using vertical coupler

In this section, we investigate the same basic structure as in the power-divider subsection 2.3.3, but use vertical coupled lines to propose a novel power splitter expected to be significantly more compact. The structure is based on vertically coupled lines separated by only 10 μm, as illustrated in Figure 4-23.

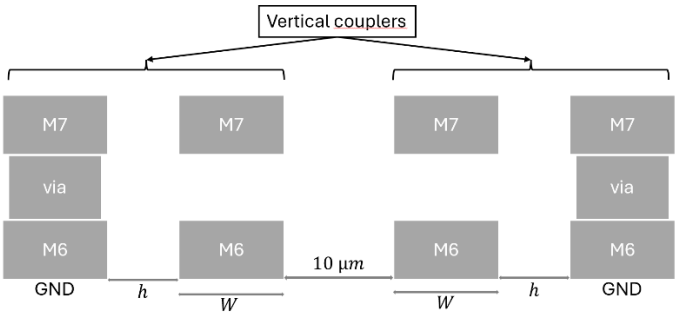


Figure 4-23: Cross section showing the main design parameters

The main geometric parameters are the strip width W of the coupled lines and the distance h between the couplers and the ground plane. The dimensions are chosen to preserve perfect vertical symmetry, so that the left and right couplers are strictly identical. These parameters were optimized using an EM simulator, and the final retained values are: $W = 5.9$ μm and $h = 4.1$ μm.

The final layout is shown in Figure 4-24. It occupies a total area of: 36 μm $\times$ 250 μm, with no need for additional spacing to mitigate parasitic coupling. This is mainly due to the fact that the ground plane is external and effectively surrounds the structure, acting as a shield and preventing undesired coupling with neighboring circuits. The EM simulation shows an excellent input matching, better than 25 dB at the center frequency, together with an insertion loss of about 0.5 dB.



Figure 4-24: Layout view of the power splitter based on vertical couplers

Due to the complexity of the routing and the time constraints, a back-to-back measurement structure was first implemented to obtain a clear assessment of the associated losses. Figure 4-25 shows the layout of the back-to-back structure embedded in B55X.

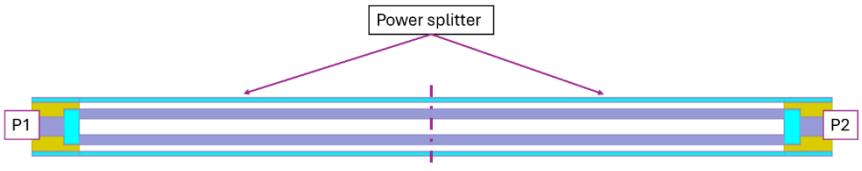


Figure 4-25: Layout view of the power splitter based on vertical couplers in back-to-back configuration

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The EM simulation predicts an overall insertion loss of about 1 dB for the full back-to-back structure, which is consistent with the 0.5 dB loss expected per splitter.

An immediate advantage of this topology is the substantial area reduction compared with the 2D implementation with ana area of $112.5\ \mu m \times 286\ \mu m$ if we consider the needed limit distance to avoid parasitic coupling. Both the two areas were considered without meandering for a fair comparison, going from an area of $9000\ \mu m^2$ for the 3D case to $32175\ \mu m^2$ for the classical case. This correspond to an area divided by 3.5. In other terms this 3D topology is more than three time smaller, what is a huge improvement. Even when compared with the meandered version that is actually the smaller version based on 2D µstrip couplers the area is $138.5\ \mu m \times 222.25\ \mu m$, taking into account the limit distance of coupling what gives an area of $30780\ \mu m^2$, even in this configuration the 3D power splitter is still 3.4 times smaller than the meandered version.

In addition, the structure is shielded from neighboring devices by the external ground, eliminating the need for extra spacing to avoid parasitic coupling. This is particularly valuable in the D-band, where parasitic coupling becomes increasingly severe. The vertical topology also relaxes the constraints on the minimum coupling distance and makes it possible to reach higher maximum characteristic impedances and lower minimum characteristic impedances except for $Z_{odd_{max}}$, which is beneficial both for impedance matching and for multiway power division.

The same measurement setup used for the other two-port structures was employed here, with GSG pads and the corresponding calibration kit. The measured results are reported in Figure 4-26.

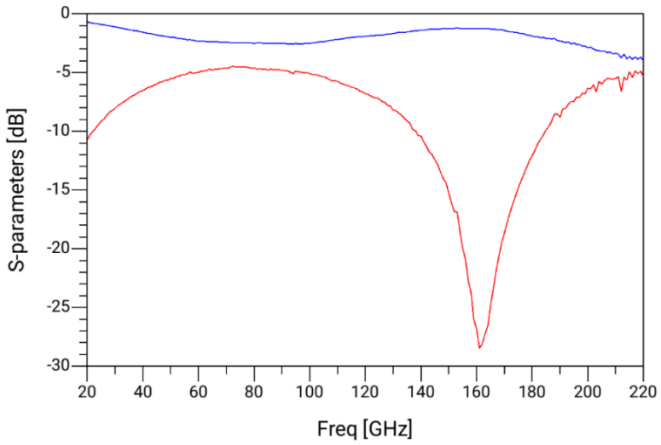


Figure 4-26: Measured results of the 3D power splitter based on vertical couplers

The measurements show excellent agreement with simulation and confirm the expected behavior. The objective of this experiment is mainly to quantify the insertion loss of the DUT. Since the structure is measured in a back-to-back configuration, the measured loss corresponds to twice the loss of a single splitter. The measured insertion loss is approximately:

$$IL \approx 1.25\text{dB at } 160\text{ GHz},$$

which corresponds to less than 0.7 dB per splitter. This is an excellent result, which is comparable to the microstrip implementation of the same device, while offering several important advantages:

- reduced footprint,
- natural shielding by the external ground, allows to reduced sensitivity to parasitic coupling, what results in smaller minimum spacing requirements,

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- and the possibility to reach wider range of modal characteristic impedances.

These features make the vertical power splitter a very attractive solution for D-band designs, especially when compactness and low loss are both required.

4.2.4 Conclusion

We began this section by demonstrating the feasibility and interest of vertical transmission lines compared with conventional microstrip lines. The vertical transmission line provides a better quality factor at high characteristic impedances as compared to the classical microstrip line. In terms of achievable characteristic impedance range, the microstrip line is limited to approximately 30 to $86\ \Omega$ in our setup, whereas the vertical transmission line can span roughly from 16 to $118\ \Omega$. In addition, a conventional $50\ \Omega$ microstrip line requires a width of about $11\ \mu$m, whereas the vertical topology can realize the same characteristic impedance with a total lateral width of only $8.2\ \mu$m. Lateral fringing is also much weaker in the vertical configuration than in the horizontal one. This study clearly demonstrates the interest of vertical transmission lines, which offer a much wider characteristic impedance range and a better quality factor at high characteristic impedance.

Next, 3D vertical couplers were studied, implemented, and experimentally validated. Their design trends were confirmed: increasing W reduces Z_o, while increasing h increases Z_e. Compared with classical microstrip couplers, the vertical coupler offers several advantages. It allows access to a wider range of modal characteristic impedances, with the exception of the maximum odd mode characteristic impedance. Overall, the 3D vertical coupler is a promising alternative to conventional microstrip couplers, with comparable insertion loss, a more compact layout, reduced sensitivity to parasitic coupling, and, more importantly, access to impedance regions that are difficult or impossible to reach with classical microstrip couplers.

Finally, the feasibility of a 3D power splitter based on vertical couplers was demonstrated. Compared to the conventional microstrip coupler implementation presented in the passive-devices section, this solution offers several advantages: more than three times reduced footprint, natural shielding provided by the external ground, lower sensitivity to parasitic coupling, smaller minimum spacing requirements, and the possibility of reaching a wider range of modal characteristic impedances. These features make the vertical power splitter a very attractive solution for D-band designs, especially when compactness and low loss are both required.

4.3 Balun

According to the state-of-the-art study, a significant number of reported D-band PAs rely on differential topologies. Although this solution was not selected as the main approach in the present work, it remains highly attractive. In practice, the output-power limitation still needs to be addressed through 1-to-N parallelization with $N > 2$. Fortunately, parallelization can be combined with differential operation, allowing the two concepts to be exploited simultaneously.

This motivates a revised architecture targeting a parallel differential PA. One possible approach consists in designing the power splitter and the balun separately. The power splitter design has already been addressed and shown to exhibit excellent performance; the remaining challenge is therefore the balun.

Most reported D-band baluns rely on coupled line Marchand-type structures, which impose strict constraints on coupling factor, coupled line characteristic impedances, and layout symmetry. In contrast, a topology derived from the Wilkinson power divider offers an appealing framework, since it naturally

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provides good input matching and straightforward power division while relying only on simple transmission-line sections.

4.3.1 Proposed balun topology

The proposed balun is based on a power-divider architecture. The input signal is first split into two paths by a T-junction. A backward 3-dB, $\sqrt{2}Z_0$ coupled line coupler is then inserted in each branch, where Z_0 denotes the port impedance. The two couplers are terminated at their coupled and thru ports either with short circuits (upper branch) or open circuits (lower branch). As a result, each coupler operates as a two-port network, as shown in Figure 4-27.

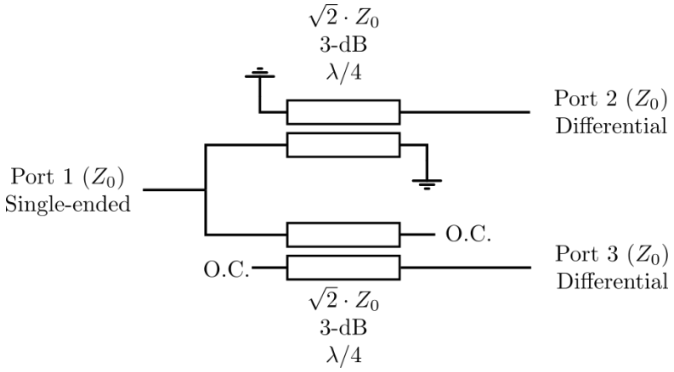


Figure 4-27: Simplified schematic of the proposed balun based on Wilkinson power divider

For a coupler terminated at both its coupled and thru ports, the transmission coefficient is given by: $S_{21} = j\Gamma$, where Γ is the reflection coefficient of the terminations [45]. For ideal short- and open-circuit terminations, this yields a $+j$ factor for the upper coupler and a $-j$ factor for the lower coupler, ultimately producing the required $180°$ phase shift between the two differential outputs in theory.

Compared with a conventional Marchand balun, the main advantage of the proposed topology lies in the flexibility of the interconnection between the two couplers, which can be adapted to layout constraints. By contrast, the interconnection in a Marchand balun generally requires additional analysis and tighter constraints [46]. The only requirement here is that the two couplers be connected symmetrically.

4.3.2 Design, equations and implementation

As for a classical power divider, to match $50\ \Omega$ to $50\ \Omega$ in parallel, the transmission-line characteristic impedance in between must be equal to: $Z_c = Z_0\sqrt{2}$. For a 3-dB coupling factor, the modal characteristic impedances are:

$$Z_e = Z_0 \cdot \sqrt{2}\frac{1+k}{1-k} = 170.7\ \Omega$$

$$Z_o = Z_0 \cdot \sqrt{2}\frac{1-k}{1+k} = 29.3\ \Omega$$

The design procedure is as follows. First, ideal transmission-line models from ADS are used to validate the functionality of the proposed balun and to identify the target electrical parameters, namely the characteristic impedance and electrical length.

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Once the target electrical values are identified, a custom coupled line coupler is designed in Momentum EM to match the required characteristic impedances. This EM simulation already confirms the functionality of the structure, provided that the accesses are correctly routed.

Finally, a refined design is developed by adding short line sections to create the input T-junction and by re-optimizing the structure to account for parasitic coupling, especially between the two couplers. For simulation purposes, a $45°$ taper is introduced between the accesses and the $50\ \Omega$ differential ports. Half-thru structures are also included, as for the other passive devices, so that TRL de-embedding can be applied during measurement.

The final structure was then fabricated in B55X. Figure 4-28 shows the embedded balun layout, with the DUT highlighted in red and the RF pads together with the half-thru structures on both sides.

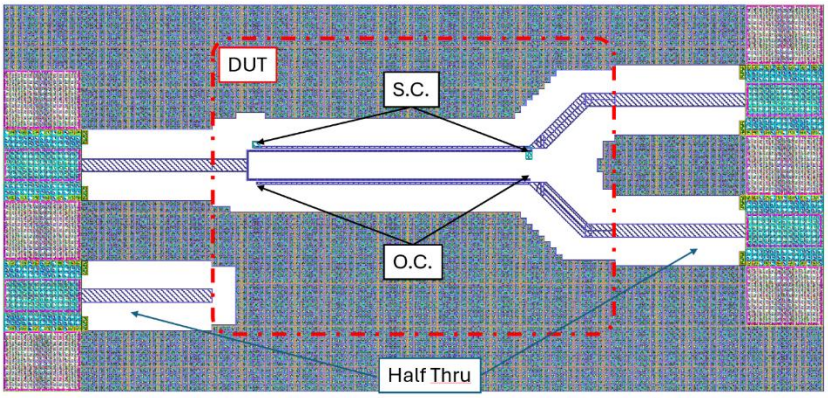


Figure 4-28: Layout view of the embedded Balun based on Wilkinson divider and loaded microstrip coupled lines.

4.3.3 Measurement results of the first balun implementation

The measurement setup is identical to that used for the other four-port devices, using GSGSG probes and the corresponding calibration kit. Figure 4-29 reports the measured and simulated S-parameters, including the transmission coefficients at the two differential outputs along with the input return loss.

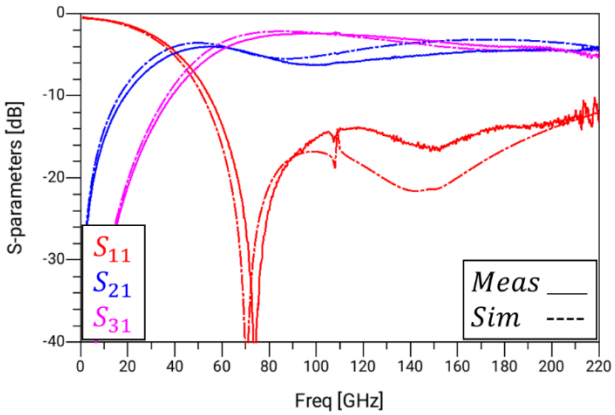


Figure 4-29: S-parameter simulation vs measurement results for input return loss S_{11} and transmission S_{21} and S_{31}.

The magnitude response shows very good agreement between simulation and measurement results. At the operating frequency of 150 GHz, the measured values are approximately: $S_{21_{measured}} = 4.7\ dB$ while $S_{31_{measured}} = 3.7\ dB$ with an amplitude imbalance of about 1 dB, which decreases at higher frequencies. The input return loss also shows good agreement, with a very wide bandwidth

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for $RL > 10$ dB, from about 55 GHz to 220 GHz, i.e. a bandwidth greater than 165 GHz and thus a relative bandwidth greater than 100 %. Overall, this figure confirms a very good fit between simulation and measurement results.

The phase difference between the two differential outputs is shown in Figure 4-30.

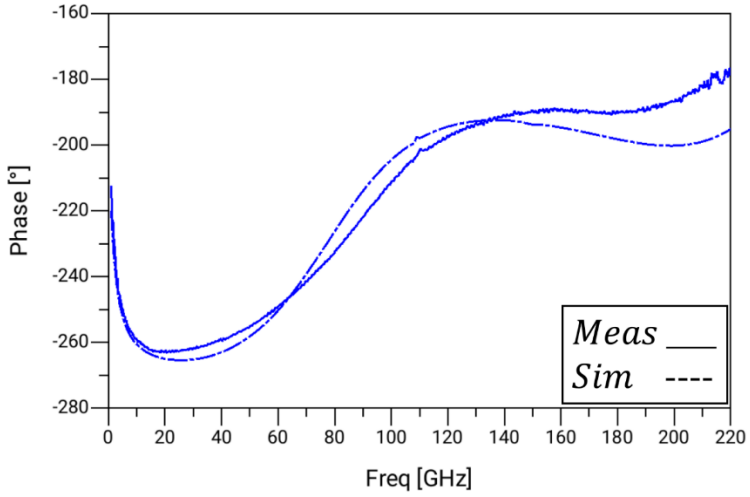


Figure 4-30: S-parameter simulation vs measurement result for phase difference between S_{21} and S_{31}.

Again, simulation and measurement are in good agreement. However, both exhibit a discrepancy with respect to the ideal $180°$ phase shift expected from a perfect balun. At 150 GHz, the simulated phase difference is $193°$, while the measured value is $189°$. Since this issue already appears in simulation, it can in principle be corrected. Our first hypothesis is that it originates from the mismatch between even- and odd mode phase velocities, as already discussed in the passive-device subsection.

The differential parameters are then reconstructed from the single-ended S-parameters using:

$$S_{d1} = \frac{1}{\sqrt{2}} \cdot (S_{21} - S_{31})$$

$$S_{dd} = \frac{1}{\sqrt{2}} \cdot (S_{22} - S_{23} - S_{32} + S_{33})$$

The corresponding insertion loss and return loss are shown in Figure 4-31.

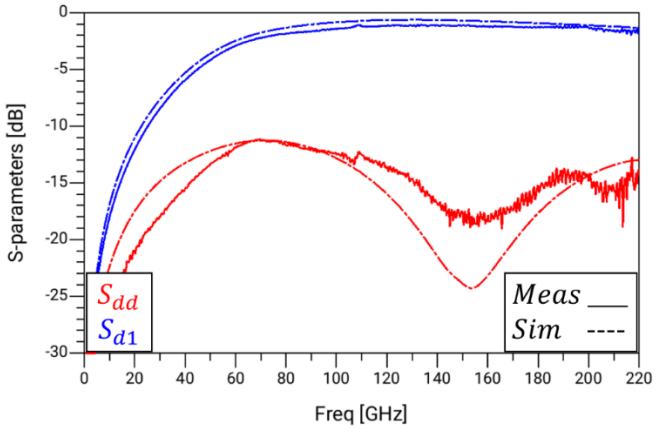


Figure 4-31: S-parameter simulation vs measurement results for both insertion loss and return loss of the differential port, S_{d1} and S_{dd}, respectively.

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A very good agreement between simulation and measurement results is again observed. The return loss remains better than 10 dB over the full measured bandwidth. The measured insertion loss is slightly higher, by about 0.4 dB. For example, at 150GHz, $S_{d1_{meas}} = 1.1\ dB$ while $S_{d1_{sim}} = 0.7\ dB$. This remains a very good result as compared to the state-of-the-art.

Overall, the simulation-to-measurement agreement is very strong, confirming both the accuracy of the simulation setup and the good performance of the proposed Wilkinson-inspired balun. The only remaining issue concerns the phase imbalance, which is observed in both simulation and measurement.

4.3.4 Investigation of the phase imbalance

This aspect was then studied further by an internship student from our laboratory, Gustavo Hama, whom I supervised during my PhD. His objective was to analyze the phase imbalance between the differential outputs, confirm the problem, and propose a performance-improvement solution.

When coupled transmission lines are used to generate the required 180° phase shift, the overall performance becomes sensitive to the difference between even- and odd mode propagation velocities. This modal dispersion is particularly critical at mm-wave frequencies, where a small difference in electrical length can lead to a significant phase imbalance over the operating band.

To better understand this effect, an ideal balun based on lossless couplers was simulated by introducing intentional differences between the even- and odd mode electrical lengths. The corresponding reconstructed S-parameters were obtained using the same methodology as for the power splitter section and the final equations are as follows:

$$S_{11(e,o)} = S_{22(e,o)} = \frac{\left(\frac{Z_{0(e,o)}}{Z_0} - \frac{Z_0}{Z_{0(e,o)}}\right) \cdot sin\left(\beta_{(e,o)} \cdot l\right)}{2 \cdot cos\left(\beta_{(e,o)} \cdot l\right) + \left(\frac{Z_{0(e,o)}}{Z_0} + \frac{Z_0}{Z_{0(e,o)}}\right) \cdot sin\left(\beta_{(e,o)} \cdot l\right)}$$

$$S_{21(e,o)} = S_{12(e,o)} = \frac{2}{2 \cdot cos\left(\beta_{(e,o)} \cdot l\right) + \left(\frac{Z_{0(e,o)}}{Z_0} + \frac{Z_0}{Z_{0(e,o)}}\right) \cdot sin\left(\beta_{(e,o)} \cdot l\right)}$$

Figure 4-32 shows the resulting phase imbalance as a function of the electrical-length difference between the even- and odd modes.

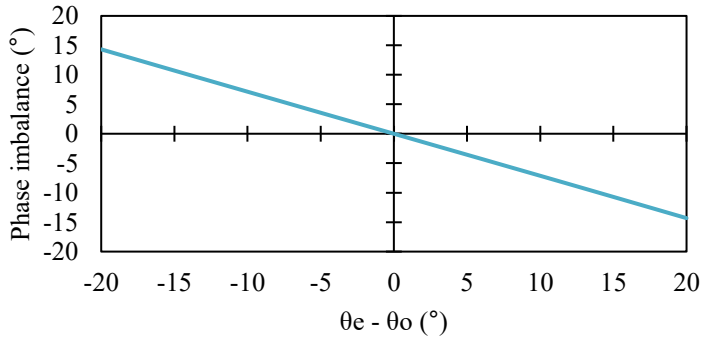


Figure 4-32: Ideal balun phase imbalance in relation to 180° at 150 GHz created by asymmetrical even- and odd mode electrical length, around 90°.

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This confirms that the phase imbalance is strongly governed by the modal velocity mismatch.

4.3.5 Proposed solution

Conventional microstrip couplers suffer from a phase imbalance caused by different phase velocities in the even- and odd modes, with the even mode velocity typically being higher than the odd mode velocity. To compensate for this effect, a defected ground structure (DGS) was introduced [47] [48] [49]. DGS structures are attractive because they are relatively simple to implement and provide additional design degrees of freedom. By introducing controlled perturbations in the ground plane, DGS structures modify the effective inductance and capacitance of the transmission line.

Figure 4-33 shows the geometry of the DGS used.

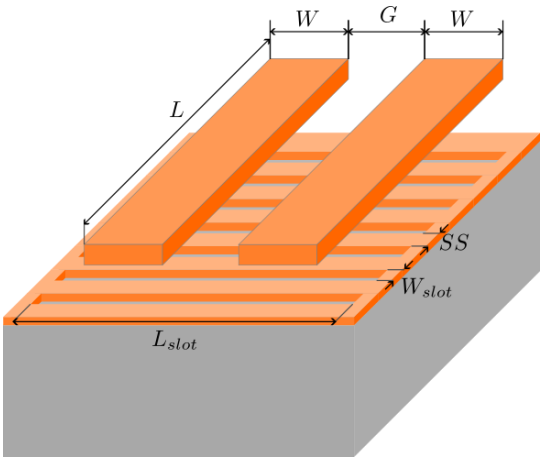
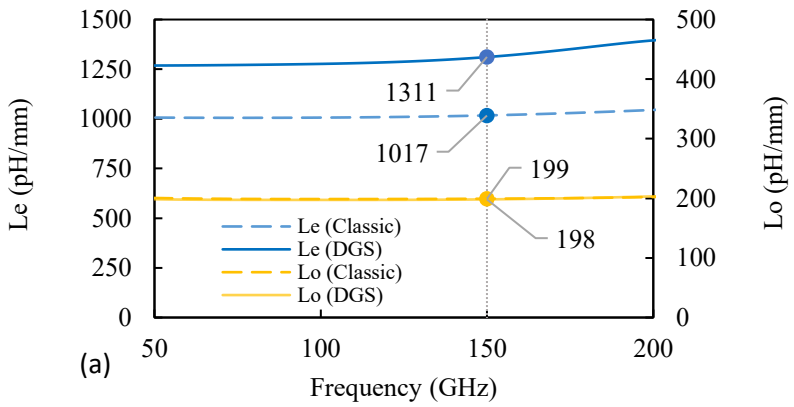


Figure 4-33: Geometry of the DGS structure, commonly used to increase the inductance of a microstrip line

The DGS increases the per-unit-length inductance of the line, thereby reducing the phase velocity of the even mode. In contrast, the odd mode inductance is only slightly affected, since the magnetic field is mostly concentrated around the coupled strips and is therefore less sensitive to the ground-plane perturbation.

The extracted per-unit-length inductances and capacitances are shown in Figure 4-34 for $W_{slot} = 5.4\ \mu m$, $L_{slot} = 27\ \mu m$ and $SS = 2.57\ \mu m$.



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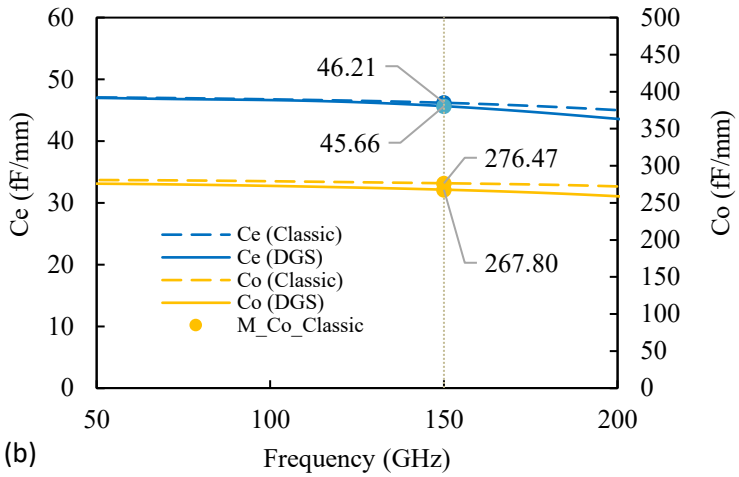


Figure 4-34: Comparison of the (a) inductance and (b) capacitance per unit length for even- and odd mode of the classic coupled lines and the coupled lines with DGS.

The DGS clearly increases the even mode inductance L_e, while leaving the odd mode inductance L_o almost unchanged. The capacitances remain nearly identical between the conventional and DGS-based structures, because the slot dimensions are much smaller than the substrate thickness and the electric field remains largely confined between the strips.

As a result, the DGS enables adjustment of the even mode phase velocity without significantly affecting the odd mode, which makes it possible to compensate for the phase imbalance at the balun output.

The parasitic inductance of the short-circuit terminations must also be considered. By fine-tuning the difference in electrical length between the even- and odd modes, the effect of the via inductance can be compensated, and the final phase difference can be brought close to $180°$.

After optimization, the final layout was fabricated, as shown in the micrograph in Figure 4-35.

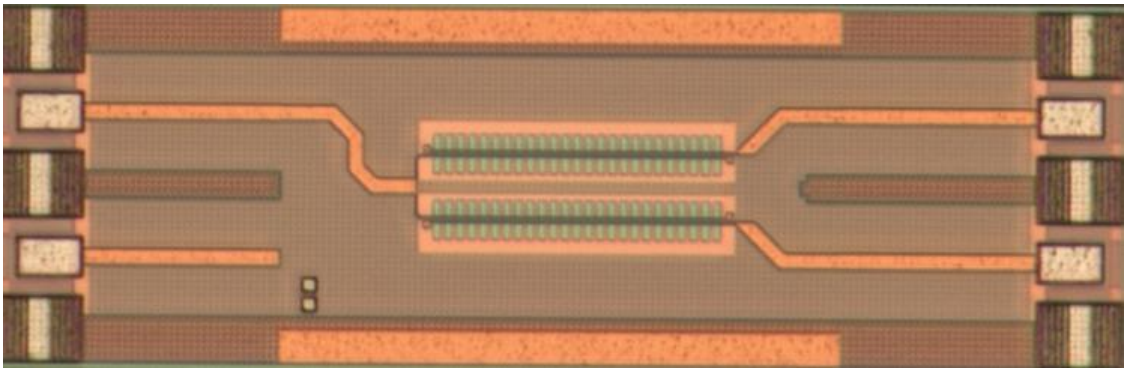
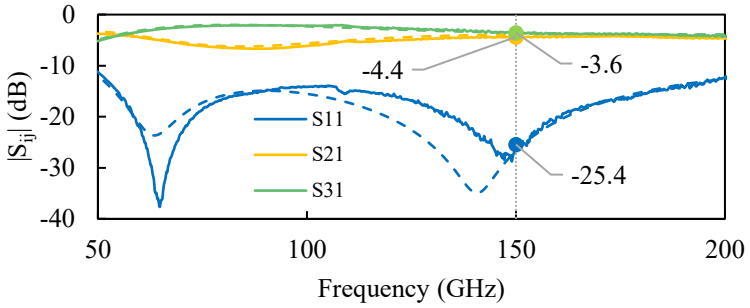


Figure 4-35: Micrograph of the proposed balun with DGS microstrip coupler.

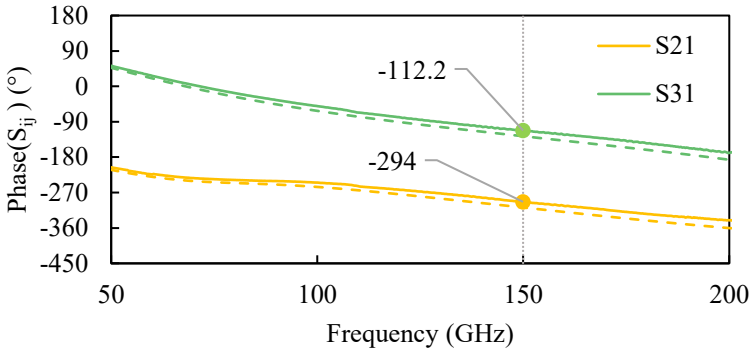
4.3.6 Final balun performance with GDS

The experimental results for the DGS-based balun are shown in Figure 4-36 and compared with EM simulations.

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(a)



(b)

Figure 4-36: (a) Magnitude and (b) phase of the balun with DGS microstrip couplers, dashed lines and solid lines represent simulation and measured values, respectively.

Once again, very good agreement is observed between measurement and simulation results. The magnitude response shows a return loss of 25.4 dB at 150 GHz, remaining below 10 dB over the full bandwidth. The insertion loss is 4.4 dB for the output corresponding to the short-circuited coupler and 3.6 dB for the output corresponding to the open-circuited coupler, leading to an amplitude imbalance of only 0.8 dB.

The phase response is very good: the measured phase difference reaches $181.8°$, which is a substantial improvement compared with the conventional microstrip coupled line-based version. Thus, the proposed balun architecture is fully functional, and the use of DGS-based microstrip couplers provides very good performance in the D-band around 150 GHz. The insertion loss is below 1 dB at 150 GHz, and the bandwidth defined by a phase imbalance within ± 2 ° reaches 73.4 GHz.

4.3.7 Perspective and use case

The proposed balun architecture inherits the logic of a Wilkinson divider. As a result, it can in principle be extended to a 1-to-4 or even 1-to-8 differential splitter. However, as with a classical Wilkinson divider, the characteristic impedance of each branch would need to be $Z_0\sqrt{N}$, where N is the division factor. For $N = 8$, this would require a characteristic impedance of $141\ \Omega$, which is not realistic in CMOS or BiCMOS integrated technologies. However, if the output impedance is in the range of 10 to $15\ \Omega$, which is consistent with the impedance range identified in the PA chapter, then the required characteristic impedance for an eight-way divider falls in the range of 63 to $77\ \Omega$, which is readily achievable with conventional or DGS-based microstrip couplers.

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This makes a 1-to-8 power division highly relevant. More generally, the proposed balun architecture naturally lends itself to a single-ended-to-multi-differential conversion. In our case, thanks to the very low output impedance of the PA cells, this solution has strong potential. Accordingly, considering the balun topology presented in this sub section, a single-to-four differential output conversion can be implemented without significant design effort, as the architecture is very simple, featuring a T-junction at the input and a coupler on each branch, terminated alternately in short- or open-circuit, as illustrated in Figure 4-37.

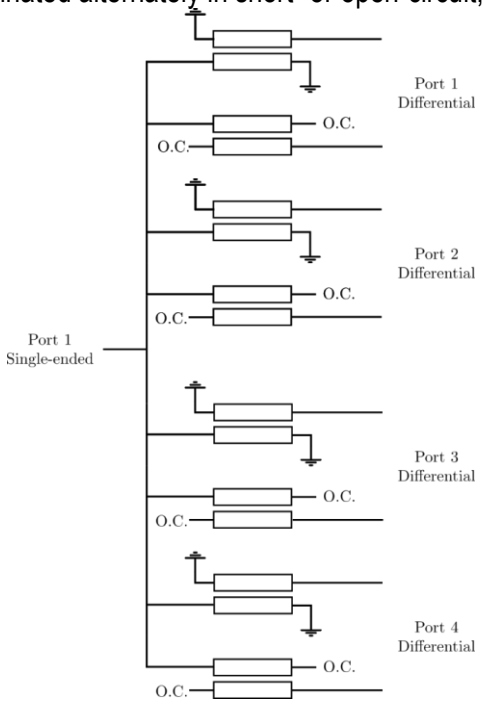


Figure 4-37: Use case: Implementation of the balun architecture proposed for the single-stage generation of four differential signals from a single-ended input.

4.3.8 Conclusion

A novel balun architecture based on a Wilkinson power-divider structure has been proposed. Compared with a conventional Marchand balun, this architecture has the advantage of avoiding the more complex design steps normally required to compensate for the parasitic effects of the short-circuit terminations and account for the additional line section between the coupled lines. In the proposed topology, a simple T-junction feeds two symmetrical branches, each implemented with a coupler: one branch is terminated with short circuits at its thru and coupled ports, whereas the other uses open-circuit terminations. This configuration generates the required $180°$ phase difference at the outputs.

Although this architecture shows very promising results, it unfortunately suffers from a phase-imbalance issue, since the outputs do not reach an exact $180°$ phase shift due to the difference in phase velocities between the coupler fundamental modes.

To compensate for this phase error, which originates from the different phase velocities of the even- and odd modes in the microstrip couplers, as well as from the parasitic inductance introduced by the short-circuit terminations, a microstrip coupler based on a defected ground structure (DGS) was designed to replace the conventional couplers.

The results demonstrate that the proposed balun architecture is fully functional, and that the use of DGS-based microstrip couplers enables excellent performance in the D-band around 150 GHz. The insertion loss remains below 1 dB at 150 GHz, and the bandwidth, defined for a phase imbalance within $\pm 2°$, reaches 73.4GHz.

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Finally, a potential use case was proposed as a perspective of this work. Owing to the architecture of the proposed balun, it becomes relatively straightforward to realize a single-ended input to four parallel differential outputs. Such an approach is particularly attractive in our case for D-band PA applications, where the low input impedance of the transistors becomes a significant advantage for the practical implementation of the couplers.

More generally, the impedance limitations of conventional 1-to-N single-ended-to-differential power dividers remain a challenge when high characteristic impedances are required. In this context, the 3D structures introduced earlier in this chapter show that vertical couplers can achieve higher characteristic impedances for both transmission lines and couplers than conventional microstrip implementations. It is therefore natural to envision a single-ended-to-N-differential power divider based on the developed vertical coupler topology, which would make it possible to match higher characteristic impedances more efficiently.

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5.Conclusion

The first important outcome of this thesis is the establishment of a reliable design and measurement methodology in STMicroelectronics' B55X SiGe BiCMOS technology. Early studies of the simulation environment and technology stack made it possible to validate the electromagnetic tools, the foundry stack, and the calibration procedures used throughout the work. In particular, the agreement obtained between simulation and measurement results, including 220-GHz four-port characterization, confirmed the validity of the adopted flow and provided a solid basis for the subsequent design efforts.

The passive-device part of the thesis revealed the importance of distributed structures at D-band frequencies. Coupled-line couplers were first studied, both theoretically and experimentally, and were shown to be effective and highly relevant building blocks for the addressed frequency range. Based on even- and odd-mode decomposition, a complete design flow was developed, enabling the realization of compact and efficient devices with excellent RF performance. An innovative power splitter based on coupled lines was then proposed, fabricated, and measured. The results show very good agreement with simulations, low insertion loss, good amplitude and phase balance, and a significant reduction in occupied area and insertion loss compared with more conventional solutions. These results strongly support the transition from lumped to distributed passive implementations in D-band design.

This passive exploration was then extended to three-dimensional structures. Vertical transmission lines were shown to offer a wider accessible characteristic impedance range than conventional microstrip lines, while also providing improved compactness and reduced lateral coupling. On this basis, 3D vertical couplers were designed and experimentally validated, confirming that such structures are promising alternatives to traditional planar implementations with the same advantages as those of the vertical Tlines. The same concept was then applied to a vertical power splitter/combiner, whose feasibility was demonstrated through measurements. This solution offers a reduced footprint, natural shielding, lower sensitivity to parasitic coupling, and access to characteristic impedance regions that are not possible to reach with conventional topologies. Finally, a novel balun architecture inspired by a Wilkinson power-divider structure was proposed and improved through a dedicated theoretical study. Although the first implementation revealed a phase-imbalance issue linked to the different modal phase velocities of the couplers, the use of DGS-based microstrip couplers enabled excellent performance around 150 GHz, with low insertion loss and wide bandwidth.

On the active side, the thesis investigated the design of D-band power amplifiers in B55X technology. A detailed comparison between cascode and common-base topologies highlighted their complementary strengths. The cascode offers high gain and excellent input-output isolation, while the common-base topology provides attractive efficiency, linearity, and output-power capability, together with a favorable proportional-biasing behavior. These characteristics made the common-base approach particularly interesting for D-band power amplification. Several amplifier cells and multi-stage architecture were therefore designed and analyzed.

The first two-stage PA implementation demonstrated the feasibility of D-band PA design in the selected technology but also revealed the limitations of conventional design choices. In particular, through capacitors, $\lambda/4$ bias networks, and classical line/stub matching sections were found to be lossy and area consuming. To overcome these limitations, a new architecture based on coupled-line matching networks with integrated biasing was proposed. This approach reduces the need for DC-blocking capacitors and provides greater flexibility for interstage matching. After refinement of the design flow and better inclusion of parasitic effects, the measured small-signal response showed good agreement with simulations, with gain above 14 dB and strong isolation. Corrected simulations predicted a P_{1dB} of about 7.2 dBm and a PAE of around 8.4%, which remains a very encouraging result at these frequencies.

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A three-stage version of the PA was also developed, with improved simulated output power and gain, reaching approximately 10 dBm and more than 16 dB, respectively. Although stability issues were observed in measurement and still require further investigation, the results confirmed the potential of the proposed architecture.

The parallelized PA approach was also explored. While its final realization could not be fully completed within the available time, the measurements of the constitutive blocks confirmed its feasibility. The estimated performance shows the best overall output-power result of the thesis, with a gain of 13 dB, a P_{1dB} of 13 dBm, and a PAE close to 8 %. This clearly illustrates the benefit of parallelization when combined with efficient splitter/combiner structures, even though the area penalty remains to be assessed more thoroughly.

Overall, this thesis demonstrates the feasibility of D-band front-end building blocks design in B55X technology and emphasizes the central role of innovation on passive circuits in enabling compact and efficient integrated circuits. Beyond the validation of several key building blocks, from coupled-line couplers and power splitters/combiners to vertical passive structures and novel baluns, the work also provides a realistic assessment of D-band PA architectures. The results obtained in this thesis lay a solid foundation for future developments, particularly in the direction of more compact, more stable, and more performant D-band front-end building blocks.

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6. Perspectives

As emphasized in the conclusion, the results obtained in this thesis provide a solid foundation for the future development of innovative and high-performance D-band building blocks in B55X technology. Several ideas were investigated throughout this work, but not all of them could be brought to completion within the available time. This naturally opens up a number of perspectives, which can be grouped into short, medium, and long term directions.

In the short term, the priority is to complete the characterization of the two-stage power amplifier and to further investigate the oscillatory behavior observed on the three-stage version. Now that the design flow has been refined and its correlation with measurements has improved, the next logical step would be to apply it to a better optimized version of the two-stage PA, and then extend the approach to three-stage or even four-stage amplifiers, still relying on a cascode driver stage and common-base power stages. A final short-term objective on the active side would be the design of a fully parallelized power amplifier based on an optimized multi-stage cell. Such architecture could make the four-way approach competitive with the best reported state-of-the-art performance.

On the passive side, an important perspective is to continue the development of innovative distributed building blocks. A first natural step would be the complete characterization of the power splitter based on 3D couplers. Another promising direction is the further exploration of the balun concept proposed in this thesis. Based on a Wilkinson-inspired architecture, this solution appears particularly well suited to the realization of a single-ended input to four differential outputs. This is especially attractive for D-band PA applications, since the low input impedance of the transistors can be exploited to ease the practical implementation of the couplers. More generally, conventional single-ended-to-differential power dividers remain limited when high characteristic impedances are required. The 3D vertical structures introduced in this work offer a wider characteristic impedance range than classical microstrip implementations, and it is therefore natural to envision a single-ended-to-N-differential power divider based on the proposed vertical coupler topology.

In the medium term, the objective would be to integrate most of the advanced PA realizations proposed in this thesis, while making use of vertical lines and couplers whenever a wider impedance range or improved compactness is required. In that perspective, a 4-way differential power amplifier would be a particularly valuable enabler, since it would allow the exploitation of N-way parallelization while also benefiting from the advantages of differential operation. Such an approach could significantly improve performance.

Finally, in the long term, the ultimate goal would be to assemble a complete transmit-receive chain using the building blocks developed in this work together with those investigated by other colleagues working on the same frequency range, but on different circuit functions, such as low-noise amplifiers, phase shifters, and other passive components. This would make it possible to experimentally validate a complete D-band front-end module and to demonstrate its potential for very high data-rate short-range wireless links. In other words, it would provide a practical proof of concept for wireless backhauling based on point-to-point D-band communications.

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Appendix

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