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Etude de la méthodologie de conception Gm/ID pour circuits très faible consommation de synthèse de fréquence RF/mmW en technologie SOI

Study of the Gm/ID design methodology for low-power RF/mmW frequency synthesizers in SOI technology

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"L’avenir appartient à ceux qui croient en la beauté de leurs rêves."
Eleanor Roosevelt.

À ma grand-mère, Lucette,

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1

General Introduction

1.1 Introduction

Over the past decade, the proliferation of connected devices has accelerated dramatically. As presented in [1], the number of active IoT devices has surpassed several billions worldwide and continues to grow at double-digit rates. This expansion is driven by applications such as smart cities, industrial monitoring, environmental sensing, wearable health systems, and large-scale distributed sensor networks. In all these domains, the ability to deploy autonomous and battery-powered nodes over long durations, often without the possibility of maintenance or battery replacement, is becoming a key technological challenge. Such constraints place stringent requirements on every subsystem of an IoT node, from sensing and data processing to wireless communication. In particular, frequency synthesizers and local oscillators represent a major contributor to the overall energy budget, as they must often remain active to ensure timing, carrier generation, or wake-up functionality. Consequently, the development of ultra-low voltage (ULV) and ultra-low power (ULP) frequency generation circuits has emerged as a central research direction to enable next-generation, energy-efficient IoT systems. Designing circuits that operate reliably at deeply scaled supply voltages is inherently difficult but they can enable overall power reduction given by the supply's lower value. Reducing the supply voltage simultaneously degrades device overdrive, transistor gain, noise margin, and timing robustness. For analog and RF blocks, such as voltage-controlled oscillators (VCOs), mixers, and frequency dividers, this often translates into reduced tuning range, limited signal swing, degraded phase noise, and increased sensitivity to process and temperature variations. For frequency synthesizers, the challenges are compounded by the requirements of spectral purity, frequency stability, and predictable phase noise behavior across operating conditions. In a ULV/ULP context, where supply voltages are typically close to (or even below) transistor threshold voltages, conventional design methodologies often reach their limits. Meeting these constraints requires new design strategies that exploit device physics more efficiently, advanced modeling approaches that remain accurate in the near-threshold regime, and technological platforms offering enhanced electrostatic control. In this perspective, fully-depleted silicon-on-insulator (FD-SOI) CMOS technologies provide unique advantages that make them particularly well-suited for ULV/ULP analog and RF design. FD-SOI CMOS technology combines an ultra-thin body with a thin buried oxide (BOX), offering excellent electrostatic control of the channel and reduced parasitic capacitances. One of its most distinctive features is the ability to apply large and energy-efficient back-gate biases, enabling wide-range threshold voltage modulation without incurring the leakage penalties typically observed in bulk CMOS. For ULV/ULP circuit design, this back-gate control is a powerful asset: it allows performance recovery at low supply voltage, dynamic tuning of delay and frequency, compensation of process variations, and improved robustness against temperature fluctuations. These capabilities have

positioned FD-SOI as a leading candidate for advanced IoT architectures, RF transceivers, and energy-constrained mixed-signal systems. In the context of frequency synthesizers, FD-SOI CMOS enables new design paradigms and forms the technological foundation of the work presented in this manuscript, which explores both device-level modeling and circuit-level innovations to push the limits of ULV/ULP frequency generation.

1.2 Manuscript's Overview

The present manuscript is structured to progressively guide the reader from the technological and theoretical foundations of FD-SOI CMOS devices to the development, design, and validation of innovative ultra-low-voltage (ULV) and ultra-low-power (ULP) voltage-controlled oscillators. The work presented in this thesis has been carried out in two different FD-SOI CMOS technologies form STMicroelectronics: the 28nm and the 18nm ones.

Chapter 2 firstly introduces the physical principles and advantages of FD-SOI CMOS technology followed by an overview of charge-based compact models and their relevance to ULV/ULP analog and RF design. The chapter concludes with a survey of inverter-based ring voltage-controlled oscillators (VCOs) and their integration into modern PLL architectures, providing a comprehensive state-of-the-art analysis.

Chapter 3 focuses on charge-based MOSFET modeling studied in the 28nm FD-SOI CMOS technology from STMicroelectronics. Several original contributions are presented, including enhanced formulations accounting for velocity saturation at both source and drain sides, a refined consideration of a particular short-channel parameter, and an optimized mathematical implementation linking terminal voltages to inversion charges in a fully consistent manner. These developments aim at strengthening the predictive capability of charge-based models for circuit design at lower V_{DD} voltages.

Chapter 4 bridges device-level modeling and circuit-level design by introducing a new analytical framework for the preliminary sizing of inverter-based ring VCOs. The chapter proposes a SPICE-like transient-based methodology derived from charge-based modeling, enabling efficient evaluation of frequency, delay, power, and noise metrics while avoiding large LUT-based extraction flows. This work is also mapped in the 28nm FD-SOI CMOS technology from STMicroelectronics.

Chapter 5 is dedicated to innovative design techniques for inverter-based ULV/ULP ring oscillators for 2.4 GHz band IoT applications. Two consecutive circuits implemented in 18nm FD-SOI CMOS technology are presented. The first is an analog multi-tuning RF ring voltage-controlled oscillator exploiting adaptive back-gate biasing to achieve state-of-the-art energy efficiency and extremely constraint phase noise performance; this circuit has been designed, fabricated, and experimentally measured. The second is a digitally controlled ring VCO featuring a fully integrated mixed-signal tuning system based on $\Sigma\Delta$ modulation. This circuit, still under fabrication at the time of writing, targets integration within next-generation low-power PLLs.

Chapter 6 finally wraps up this work and provides perspectives.

2

FD-SOI Technology and Charge-Based Models: A Contemporary Review with Applications in Voltage-Controlled Oscillator Design

This second chapter reviews FD-SOI technology and its applications, explores charge-based MOSFET modeling, and discusses VCO design. The chapter concludes with a state-of-the-art review of ring oscillators, comparing their performance and recent innovations.

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2.1 Introduction

The continuous scaling of CMOS technologies has reached a point where conventional bulk transistors face major limitations in variability, leakage, and voltage headroom. These challenges have motivated the development of advanced device architectures and modeling methodologies that preserve energy efficiency and analog performance at nanometer scales. Among these, Fully-Depleted Silicon-On-Insulator (FD-SOI) CMOS technology has emerged as a strong contender for ultra-low-voltage (ULV) and ultra-low-power (ULP) applications, providing superior electrostatic control and unique body-biasing capabilities.

In parallel, accurate transistor modeling has become a key enabler for predicting circuit behavior under such stringent conditions. Charge-based compact models, which express terminal currents as the time derivatives of conserved charges, offer the physical rigor needed to capture transient and small-signal phenomena in modern FD-SOI CMOS devices.

This chapter presents a comprehensive review of FD-SOI CMOS technology and charge-based modeling principles, setting the foundation for the voltage-controlled oscillator (VCO) architectures and body-biasing techniques analyzed in later chapters. Section 2.2 details the technological evolution and design advantages of FD-SOI CMOS. Section 2.3 discusses the fundamentals and relevance of charge-based modeling for ULV/ULP circuit design. Finally, Section 2.4 surveys the state of the art in VCO and PLL design, emphasizing the use of FD-SOI CMOS ring oscillators as key building blocks in modern frequency synthesizers.

2.2 FD-SOI CMOS Technology Overview

The migration from bulk CMOS to FD-SOI CMOS represents a paradigm shift in how designers approach power efficiency and variability control. FD-SOI CMOS transistors combine planar manufacturability with advanced electrostatic confinement, offering a unique trade-off between cost, performance, and power. This section outlines the historical evolution of FD-SOI CMOS technology, its key physical and technological features, and the specific advantages it brings to ULV and ULP circuit design. The final subsection discusses the remaining challenges and current research directions driving FD-SOI CMOS' continued relevance in advanced system-on-chip design.

2.2.1 Evolution and Historical Background of FD-SOI CMOS

Silicon-On-Insulator (SOI) technology was introduced in the 1960s [2] to mitigate parasitic capacitances and leakage currents inherent to bulk CMOS. Early SOI implementations used thick silicon films and partially depleted (PD) channels, which improved isolation and speed but suffered from floating-body effects and limited electrostatic control.

In the late 1990s, fully depleted (FD) thin-film transistors emerged as a promising alternative. The group at Université Catholique de Louvain demonstrated that FD-SOI CMOS devices exhibit near-ideal subthreshold slope, reduced body effect, and improved drive current compared with bulk CMOS, while maintaining process simplicity and isolation advantages [3]. These studies established the physical basis of FD-SOI for analog, RF, and low-voltage mixed-signal circuits.

Concurrently, work on energy-efficient CMOS design by A.Chandrakasan and D.Antoniadis highlighted the importance of voltage scaling for power reduction [4]. The convergence of these circuit-level techniques with the electrostatic advantages of FD-SOI CMOS formed the conceptual framework for modern low-power FD-SOI CMOS design.

In the 2000s, CEA-LETI and STMicroelectronics transformed these concepts into an industrial process. Improvements in thin-film uniformity and buried-oxide (BOX) control led to the demonstration of Ultra-Thin Body and Buried oxide (UTBB) FD-SOI devices compatible with advanced CMOS nodes [5]. These transistors combine excellent electrostatic integrity with dynamic threshold-voltage control through back-biasing, offering a planar and power-efficient alternative to bulk CMOS.

Figure 2.1 summarizes the main technological milestones leading to the industrial deployment of FD-SOI at STMicroelectronics. A schematic cross-section is shown in Figure 2.2, illustrating the evolution from PD-SOI to UTBB FD-SOI and the resulting improvement in body control and isolation.

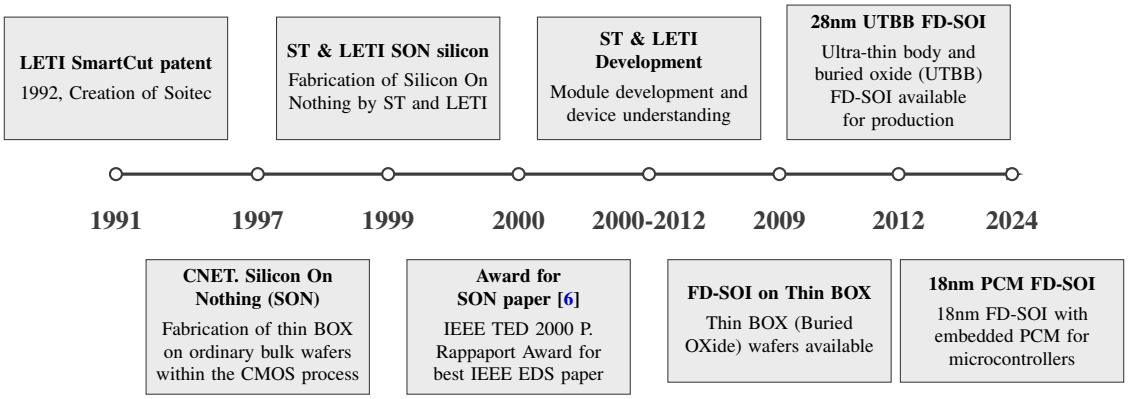


Figure 2.1: Timeline of FD-SOI technology evolution at STMicroelectronics and CEA-LETI. Reproduced with permission from STMicroelectronics.

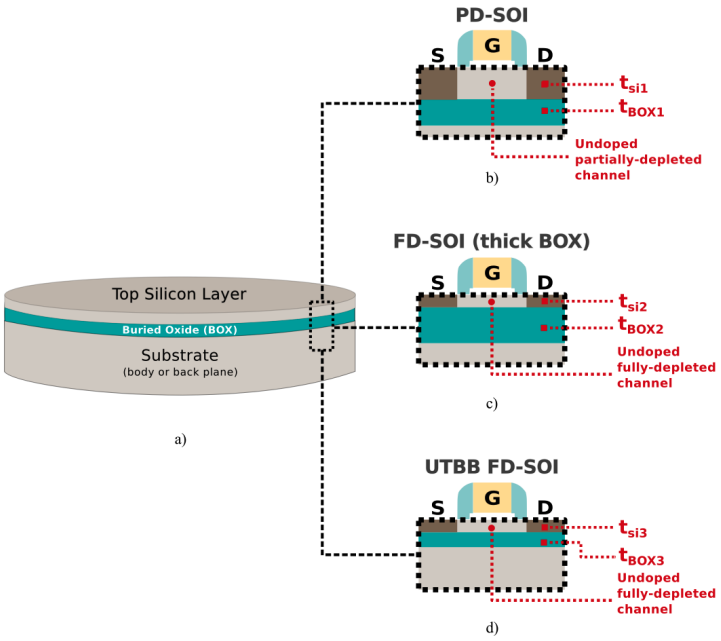


Figure 2.2: Cross section of PD-SOI (b), FD-SOI (thick box) (c) and UTBB FD-SOI (d) transistors built from silicon-on-insulator base wafer (a). t_{si} represents the thickness of the top silicon layer and t_{BOX} represents the thickness of the BOX. $t_{si1} > t_{si2} = t_{si3}$; $t_{BOX1} > t_{BOX2} > t_{BOX3}$. Reproduced from [7].

Although FinFETs later improved scalability through 3D structuring, as presented in Figure 2.3, FD-SOI retained several decisive advantages for analog, RF, and ultra-low-voltage digital design: planar processing, predictable electrostatics, and efficient body-bias tuning. FD-SOI thus remains a robust and energy-efficient CMOS platform for integrated systems requiring high reliability and low power consumption. Also, FD-SOI CMOS offers a planar device architecture with simpler fabrication steps [8], making it attractive for cost-sensitive applications. The technology has been brought into an industrial format by STMicroelectronics, and then has been licensed to several other companies, with process nodes ranging from 28 nm down to 12 nm and beyond.

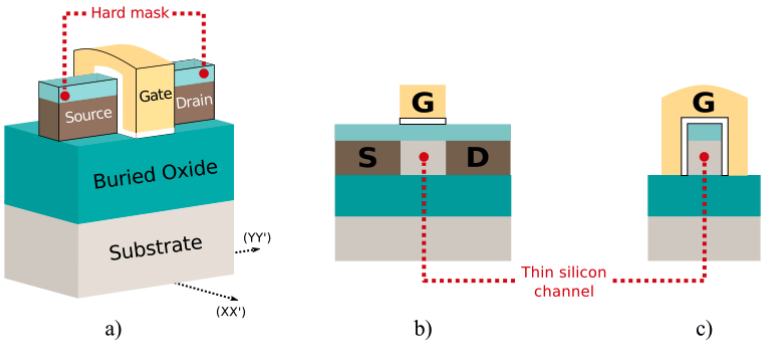


Figure 2.3: 3D schematic (a) and cross-section YY' (b) and XX' (c) of a FinFET transistor. Reproduced from [7].

2.2.2 Key Technological Features of FD-SOI CMOS

FD-SOI CMOS technology is characterized by several distinctive features that contribute to its performance and power advantages [9]:

- **Fully Depleted Channel:** The silicon channel is very thin (typically <10 nm), fully depleted of carriers, which reduces short-channel effects and improves electrostatic control.
- **Ultra-Thin Buried Oxide (BOX) Layer:** A thin buried oxide layer ($\tilde{2}$0 nm or less) electrically isolates the transistor channel from the substrate, reducing parasitic capacitances and leakage currents.
- **Low Leakage Current:** The FD-SOI structure significantly reduces leakage currents compared to bulk CMOS, enabling ultra-low power operation.
- **Body Biasing Capability:** The thin BOX allows efficient back-biasing (forward or reverse), enabling dynamic threshold voltage adjustment for performance and power optimization.
- **Reduced Short-Channel Effects:** Excellent electrostatic control of the channel suppresses drain-induced barrier lowering (DIBL) and other short-channel effects, improving device scalability.
- **High Drive Current and Performance:** The fully depleted channel and excellent electrostatics enable high drive currents and improved transistor switching speeds.
- **Lower Parasitic Capacitance:** The isolation by BOX reduces junction capacitances, leading to faster switching and lower dynamic power consumption.
- **Compatibility with Advanced CMOS Nodes:** FD-SOI technology is compatible with advanced lithography and scaling down to sub-20 nm nodes.

- **Simplified Process Integration:** Compared to FinFETs, FD-SOI offers planar transistor architecture, simplifying fabrication and reducing manufacturing complexity and cost.
- **Improved Analog/RF Performance:** The thin BOX and fully depleted channel improve device matching, reduce flicker noise, and enhance analog and RF characteristics.

These properties jointly provide a transistor technology that bridges the gap between bulk CMOS and FinFET solutions, offering both low-power operation and analog/RF versatility.

2.2.3 Advantages for ULV/ULP Circuit Design

FD-SOI CMOS technology offers several advantages that make it particularly suitable for ultra-low-voltage and ultra-low-power circuit design. Owing to its planar architecture and fully depleted channel, FD-SOI CMOS enables energy-efficient operation with enhanced analog and RF performance. The main benefits can be summarized as follows:

- **Low Leakage Current:** The fully depleted channel and high-quality BOX significantly reduce leakage currents, a critical factor for battery-powered and always-on applications. The leakage current in FD-SOI CMOS technology is typically an order of magnitude lower than that of an equivalent bulk CMOS process [10].
- **Threshold-Voltage Tunability:** Back-biasing enables dynamic adjustment of threshold voltages, allowing circuits to trade off speed and power consumption on demand.
- **Improved Analog and RF Performance:** Reduced variability and superior electrostatic control enhance device linearity and noise performance, benefiting analog/RF blocks such as voltage-controlled oscillators (VCOs), phase-locked loops (PLLs), and low-noise amplifiers.
- **Enhanced Energy Efficiency:** The ability to operate at supply voltages as low as 0.5 V while maintaining reasonable drive strength enables energy-per-operation levels unattainable with bulk CMOS.

The benefits of FD-SOI CMOS over bulk CMOS for analog and ultra-low-power design can be quantitatively illustrated through key device metrics. Figure 2.4 compares 28nm FD-SOI CMOS and 28nm bulk CMOS technologies, highlighting the improved electrostatic control, transconductance efficiency, and reduced variability enabled by full channel depletion. In particular, FD-SOI devices exhibit higher intrinsic gain (G_m/G_{ds}), lower

mismatch (ΔV_T), enhanced transconductance efficiency (G_m/I_D), and reduced gate capacitance (C_{gg}), which together translate into superior analog performance and lower noise levels. These characteristics make FD-SOI particularly attractive for energy-efficient analog and RF circuits operating at ULV/ULP standards.

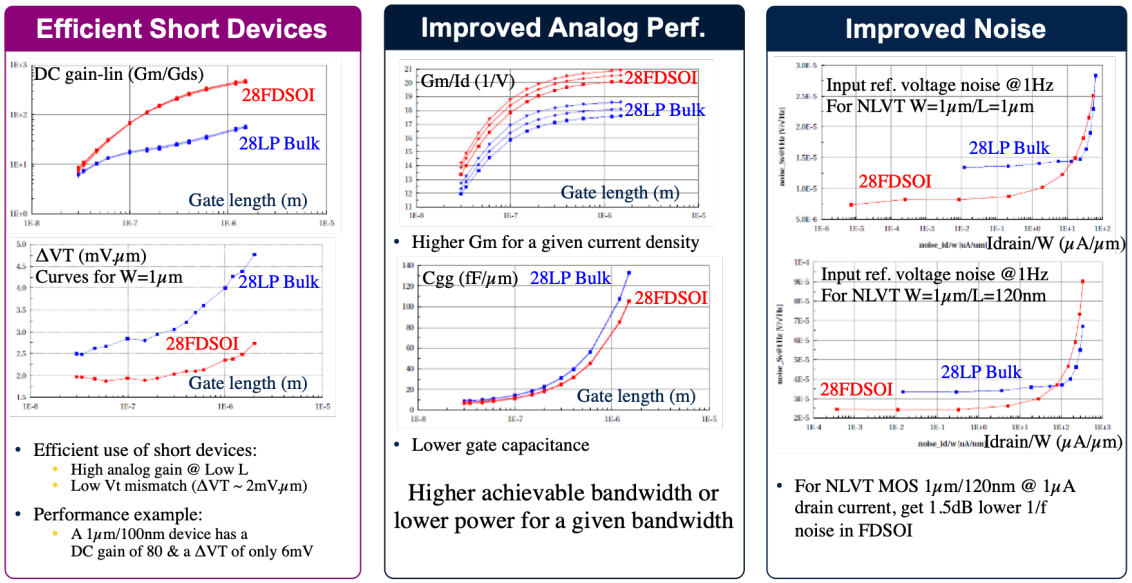


Figure 2.4: Comparison between 28nm FD-SOI CMOS and 28nm bulk CMOS technologies: (left) higher intrinsic gain and lower variability for short devices, (center) improved transconductance efficiency and lower gate capacitance, and (right) reduced input-referred noise, highlighting the benefits of FD-SOI CMOS for analog and ultra-low-power circuit design. Courtesy of STMicroelectronics, used with permission.

These features collectively enable the design of energy-efficient circuits with robust performance, making FD-SOI CMOS a preferred technology for IoT, mobile, and automotive applications requiring extended battery life and high reliability.

2.2.4 Challenges and Current Research Trends

Despite its advantages, FD-SOI CMOS technology faces several challenges that continue to motivate active research at both device and circuit levels.

At the device level, the ultra-thin silicon film requires tight control of thickness uniformity and interface quality to ensure consistent electrical characteristics [11]. Variations in silicon or BOX thickness can lead to threshold-voltage dispersion and degraded matching for analog circuits [12, 13]. Moreover, as supply voltages continue to scale, variability in back-bias efficiency and self-heating effects in thin-BOX structures become more pronounced, affecting circuit reliability and noise behavior [14].

At the circuit level, the limited intrinsic gain of short-channel FD-SOI CMOS transistors constrains the design of high-linearity analog blocks, particularly under sub-0.7 V operation. While forward body biasing (FBB) can recover speed at low voltage, it simultane-

ously increases leakage and thermal noise, requiring fine-grained bias control schemes. The accurate modeling of back-gate influence, charge distribution, and dynamic capacitances is thus essential to predict circuit performance under varying bias conditions.

Current research trends focus on improving compact models such as Leti-UTSOI [15] and BSIM-IMG [16] to capture multi-physical interactions in FD-SOI CMOS devices, including quantum confinement, parasitic coupling, and non-quasi-static effects. In parallel, novel circuit techniques exploit dynamic body-bias modulation [17], adaptive threshold control [18] to optimize performance and energy efficiency in mixed-signal and RF systems.

These ongoing developments demonstrate the continued relevance of FD-SOI CMOS for energy-constrained electronics, particularly when combined with accurate charge-based modeling and body-bias-aware design methodologies, as discussed in the following sections.

2.3 Charge-Based Modeling

Compact modeling lies at the heart of reliable circuit simulation, bridging the physics of the transistor and its electrical representation in design tools. As CMOS technologies scaled to nanometer dimensions and ultra-low-power operation, charge-based models emerged as the most physically consistent and design-oriented approach. Unlike purely empirical or current-based descriptions, charge-based formulations ensure current continuity, energy conservation, and accurate small-signal behavior across all regions of operation—from weak to strong inversion—making them essential for ULV/ULP circuit design.

In FD-SOI CMOS technologies, where device behavior is governed by precise electrostatic control of charge in ultra-thin, fully depleted bodies, charge-based formulations provide a natural and physically meaningful framework. Their explicit dependence of current on stored charge inherently captures front–back gate coupling, buried-oxide effects, and the continuous transition across inversion regimes—key aspects for accurately modeling FD-SOI devices at low voltage [19, 20].

The following subsection introduces the theoretical foundations of charge-based modeling, outlining how the fundamental electrostatic relations lead to continuous and charge-conserving compact formulations.

2.3.1 Fundamentals of Charge-Based Modeling Theory

Charge-based modeling provides a physically consistent description of MOSFET operation by expressing terminal currents as the time derivatives of the charges stored within the device. Unlike current-based or voltage-based models, which approximate device behavior through empirical relations, charge-based formulations derive directly from fundamental electrostatic and transport principles. In its general form, the drain current I_D is expressed as

$$I_D = -\frac{dQ_D}{dt}, \tag{2.1}$$

where Q_D denotes the charge associated with the drain terminal. By enforcing charge conservation across all terminals, the model ensures

$$I_G + I_S + I_D + I_B = 0, \tag{2.2}$$

with I_G, I_S, I_D, and I_B representing gate, source, drain, and bulk currents, respectively. This explicit charge conservation property makes charge-based models particularly suitable for transient and RF simulations, where current continuity and dynamic effects play critical roles.

A common foundation of charge-based models lies in the Ward–Dutton charge partition-

ing scheme [21], which provides a physically meaningful distribution of channel charge between source and drain terminals. The total channel charge Q_{ch} is related to the local inversion charge density $q_i(x)$ as

$$Q_{ch} = \int_0^L q_i(x)\,dx, \tag{2.3}$$

and its partition into source and drain charges Q_S and Q_D follows a linear weighting along the channel of length L. This approach ensures correct modeling of transcapacitances and transient responses, maintaining charge conservation and reciprocal behavior in small-signal conditions.

Starting from Poisson's equation under the gradual channel approximation, the local inversion charge density $q_i(x)$ can be linked to the surface potential $\psi_s(x)$, which represents the electrostatic potential at the semiconductor–oxide interface. The modeling approach can be conceptually divided into three main steps:

1. **Electrostatic formulation:** In weak and moderate inversion, the charge in the channel originates from carriers controlled by the surface potential $\psi_s(x)$, which satisfies Poisson's equation. The inversion charge per unit area can be expressed as

$$q_i(x) \propto -qn_i \exp\left(\frac{\psi_s(x) - V(x)}{U_T}\right), \tag{2.4}$$

   where n_i is the intrinsic carrier concentration, t_{si} the silicon film thickness, and U_T the thermal voltage. This expression highlights the exponential dependence of inversion charge on surface potential in the weak inversion regime.

2. **Surface potential to terminal voltage link:** In compact modeling, solving Poisson's equation for $\psi_s(x)$ is computationally demanding. The ACM model [20] replaces it with an analytical approximation relating $\psi_s(x)$ to the terminal voltages, using the gate overdrive $(V_{GS} - V_T)$ and the local channel potential $V(x)$. The coupling between the gate and the channel is represented by the channel control factor η, while the slope factor n accounts for the contribution of depletion charge. The resulting first-order approximation is written as:

$$\psi_s(x) \approx \eta\,(V_{GS} - V_T) - nV(x). \tag{2.5}$$

3. **Analytical charge expression:** Combining the above relations and expressing the inversion charge in terms of measurable terminal voltages yields the compact logarithmic expression adopted by the ACM formulation:

$$q_i(x) = -C_{ox}\,nU_T \ln\left(1 + e^{\frac{\eta(V_{GS}-V_T)-V(x)}{nU_T}}\right), \tag{2.6}$$

which provides a continuous and differentiable description of the channel charge across all inversion regions. While $\psi_s(x)$ has been eliminated from the final expression, its electrostatic role remains implicitly embedded in the exponential dependence on $(V_{GS} - V_T - V(x))$. This formulation ensures charge conservation, physical continuity, and accuracy from weak to strong inversion.

Equation (2.6) thus forms the analytical foundation of continuous charge-based models such as ACM and its derivatives, which extend this formulation to include short-channel effects, mobility degradation, and velocity saturation. In FD-SOI CMOS transistors, the thin silicon body and buried oxide demand precise modeling of front- and back-gate coupling, depletion effects, and quantum confinement—all naturally incorporated in this charge-based framework.

Integrating $q_i(x)$ along the channel yields the total channel charge, which—through the Ward–Dutton partitioning—defines the source and drain terminal charges:

$$Q_S = \int_0^L \left(1 - \frac{x}{L}\right) q_i(x)\, dx, \tag{2.7}$$

$$Q_D = \int_0^L \frac{x}{L} q_i(x)\, dx. \tag{2.8}$$

Under the quasi-static approximation, the drain current follows from charge conservation:

$$I_D = -\frac{dQ_D}{dt} = \mu C_{ox} \frac{W}{L} \int_0^{V_{DS}} q_i(V)\, dV. \tag{2.9}$$

In its normalized ACM form, the drain current is expressed as:

$$I_D = I_S \left[\ln^2\left(1 + e^{\frac{V_P - V_S}{2U_T}}\right) - \ln^2\left(1 + e^{\frac{V_P - V_D}{2U_T}}\right) \right], \tag{2.10}$$

where $I_S = 2n\mu C_{ox}(W/L)U_T^2$ is the specific current and $V_P = \eta(V_{GS} - V_T)$ represents the pinch-off voltage. This formulation preserves source–drain symmetry and provides analytical continuity across weak, moderate, and strong inversion, making it particularly suited for low-voltage analog and RF design.

2.3.2 Assets of Charge-Based Models for ULV/ULP Design

The unified charge-based formulation provides three major benefits for ULV and ULP design:

- **Continuity across operation regimes:** By basing current on the inversion charge, the model remains valid from deep subthreshold to strong inversion, eliminating discontinuities between regions. This is essential for circuits operating near or below threshold, such as energy-harvesting front-ends or low-voltage oscillators.

- **Charge conservation and capacitance accuracy:** Since all terminal currents derive from time-varying conserved charges, small-signal capacitances and transcapacitances obey reciprocity and energy conservation. This ensures physically consistent transient and AC behavior—critical for RF blocks like VCOs and PLLs.
- **Compact analytical form:** The resulting closed-form equations involve a limited number of physically meaningful parameters (e.g., n, η, V_T, μ, I_S), facilitating parameter extraction and circuit-level intuition.

Furthermore, charge-based models explicitly expose the link between charge storage and energy consumption. The switching energy per transition in a logic or analog node,

$$E_{sw} = \int V \, dQ, \tag{2.11}$$

can be directly evaluated, enabling accurate estimation of dynamic power in ULV circuits. In FD-SOI CMOS technologies, the inclusion of back-gate charge and coupling capacitance terms extends the model to four-terminal operation, supporting dynamic body-bias control and adaptive performance tuning.

2.3.3 Drawbacks and Limitations

While conceptually elegant, charge-based models face practical challenges in numerical implementation:

- The transcendental nature of the equation linking charges and terminal voltages increases the implementation complexity of charge-based mdodels, leading to the requirement of iterative or approximate solutions.
- Maintaining charge conservation under non-quasi-static (NQS) and short-channel conditions increases computational burden [22].
- Accurate modeling of parasitic overlap and fringe capacitances still depends on semi-empirical corrections.

Despite these limitations, charge-based models remain the most physically grounded approach for nanoscale device simulation, and their extensions (e.g., EKV, ACM2) have been implemented to be integrated in mainstream EDA tools.

2.3.4 Proposed Improvements and Research Contributions

Building on these foundations, recent researches [23, 24]—including the developments presented in Chapter 3—aims to refine the analytical continuity of charge-based models.

The proposed work enhances the computation of inversion charge densities in function of terminal voltages and propose a novel manner of considering low-field mobility degradation, ensuring robust convergence while preserving the physical compactness of the model. By unifying the modeling of forward and reverse charge flows and introducing explicit charge–voltage symmetry, the extended formulation bridges device-level accuracy and circuit-level efficiency, providing an improved predictive framework for low-voltage oscillators, PLLs, and analog front-ends.

2.4 Voltage-Controlled Oscillator (VCO) and Modern PLL State of the Art

Frequency generation circuits, such as VCOs and phase-locked loops (PLLs), are among the most sensitive to device-level nonidealities. Their oscillation frequency and phase stability directly depend on the intrinsic delay and noise characteristics of the underlying transistors. Small variations in threshold voltage, carrier mobility, or parasitic capacitances can alter the propagation delay of inverter stages or the resonance condition of LC tanks, leading to noticeable frequency deviations. In addition, thermal, flicker, and shot noise are upconverted through nonlinearities in the oscillator core, degrading phase noise and timing jitter [25]. Under low-voltage operation, limited voltage headroom further increases sensitivity to supply and substrate noise, while in FD-SOI CMOS technologies, variations in back-bias efficiency or temperature can modulate the effective threshold voltage and thus the oscillation frequency. Consequently, frequency generation circuits act as amplifiers of device-level imperfections in both the time and frequency domains.

The use of FD-SOI CMOS devices in these circuits enables significant gains in power efficiency and tuning agility, with the back gate often serving as a frequency-tuning control [26, 27, 28]. While LC-tank oscillators generally offer superior phase-noise performance due to their high-quality resonant networks, they require large passive components that occupy substantial silicon area and increase fabrication cost. By contrast, ring oscillators rely solely on active devices and interconnect capacitances, offering compact layouts, straightforward integration, and excellent scalability with CMOS nodes. In the context of FD-SOI CMOS and IoT applications—where minimizing area, power, and cost is critical—ring oscillators constitute the most practical and efficient solution. The need for extremely low-cost IoT devices, combined with the fact that FD-SOI CMOS technologies are implemented in advanced nodes such as 28 nm and 18 nm—where fabrication costs remain relatively high—necessitates strong area minimization. Consequently, compact ring-based VCOs are preferred over LC-tank counterparts, despite their inherently higher phase noise [29]. Moreover, the body-bias tunability intrinsic to FD-SOI CMOS devices provides an additional degree of freedom to enhance frequency control and energy efficiency, reinforcing the suitability of ring oscillators for ultra-low-voltage and ultra-low-power frequency generation.

This section reviews the operating principles of ring oscillators, their evolution within modern PLL architectures, and recent state-of-the-art implementations that illustrate the synergy between FD-SOI CMOS technology and body-bias-assisted frequency control.

2.4.1 Ring Oscillators as Technology and Process Markers

Basic Structure of Ring Oscillators

Ring oscillators (ROs) are widely used as compact on-chip frequency references and technology monitors. They are composed of an odd number N of inverting delay stages connected in a closed loop, providing the necessary 180° phase shift and loop gain to sustain oscillation, as presented in Figure 2.5. Each inverting delay stage contributes a propagation delay, so that the total oscillation period is the sum of all stage delays. The simplicity of this topology allows straightforward integration in standard CMOS technologies without requiring inductors or large passive components, making it an ideal structure for process characterization, frequency generation, and built-in self-test circuits.

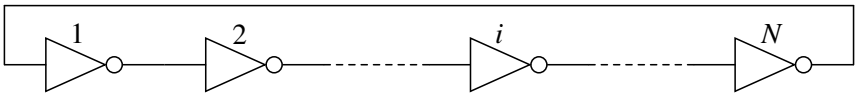


Figure 2.5: Single-ended ring oscillator architecture composed of N inverters.

Oscillation Frequency

The oscillation frequency f_{osc} is defined as:

$$f_{osc} = \frac{1}{N \cdot (t_r + t_f)}, \tag{2.12}$$

where t_r and t_f represent the rise and fall propagation delays of a single inverter, respectively, and N the number of inverters composing the ring. Both delay components depend on transistor dimensions, load capacitance, and supply voltage. Consequently, f_{osc} directly reflects the electrical performance of the underlying technology. Any variation in process parameters, temperature, or supply voltage translates into frequency shifts, making ring oscillators a sensitive indicator of process corners and device variability.

Process Sensitivity

The propagation delay of CMOS inverters is primarily governed by carrier mobility, threshold voltage, and parasitic capacitances [29]. As technology scales, short-channel effects and device variability increasingly influence the oscillation frequency and phase noise. In FD-SOI CMOS, body-bias conditions and supply fluctuations further modulate the delay of each stage, resulting in frequency deviations. Consequently, monitoring ring oscillators under varying biasing and temperature conditions provides valuable insight into device performance, leakage mechanisms, and process dispersion across wafers or fabrication lots.

Technology Monitoring and Benchmarking

Ring oscillators (ROs) have long been standard process control structures for evaluating delay, variability, and speed–power trade-offs in advanced CMOS nodes. Their compact area, simplicity, and scalability enable the integration of large RO matrices for statistical characterization, primarily aimed at monitoring the digital well behavior of the technology at low operating frequencies. Metrics such as frequency per stage, power consumption, and delay–energy product are commonly extracted to benchmark process performance. In FD-SOI CMOS technologies, body-bias tuning further introduces post-fabrication calibration capability, allowing adaptive compensation of process and temperature variations. The present approach extends this concept toward RF monitoring by employing simple RF-oriented RO structures to probe the RF well behavior of MOS transistors, offering a compact and efficient means to assess analog and high-frequency device performance within the same framework.

2.4.2 Towards the Usage of FD-SOI CMOS Ring Oscillator in Modern PLL Design

FD-SOI CMOS Technology Benefits

FD-SOI CMOS technology features a thin buried oxide and an ultra-thin silicon body that provide strong electrostatic control over the channel. One of its key advantages is the capability for body biasing, which enables dynamic modulation of the transistor threshold voltage without inducing excessive leakage. This feature offers an efficient means to tune the propagation delay, as illustrated in Figure 2.6, and, consequently the oscillation frequency of ring oscillators. Moreover, FD-SOI CMOS devices exhibit reduced parasitic capacitances, improved device matching, and superior substrate noise isolation, making them particularly well suited for low-voltage and low-jitter VCO design.

RO Performance Enhancements

Several design techniques enhance the performance of FD-SOI CMOS ring oscillators. Body-bias control enables wide frequency tuning and process compensation, while differential and pseudo-differential topologies improve phase noise and supply rejection [31]. Current-starved inverters and digitally controlled delay cells allow fine frequency resolution and low power consumption [29]. The reduced device variability in FD-SOI CMOS results in predictable delay behavior, facilitating accurate modeling of K_{VCO} and improved control linearity.

Integration in PLLs

Integrating FD-SOI CMOS ring oscillators within phase-locked loops (PLLs) has emerged as a promising alternative to LC-based VCOs, particularly for compact and low-voltage

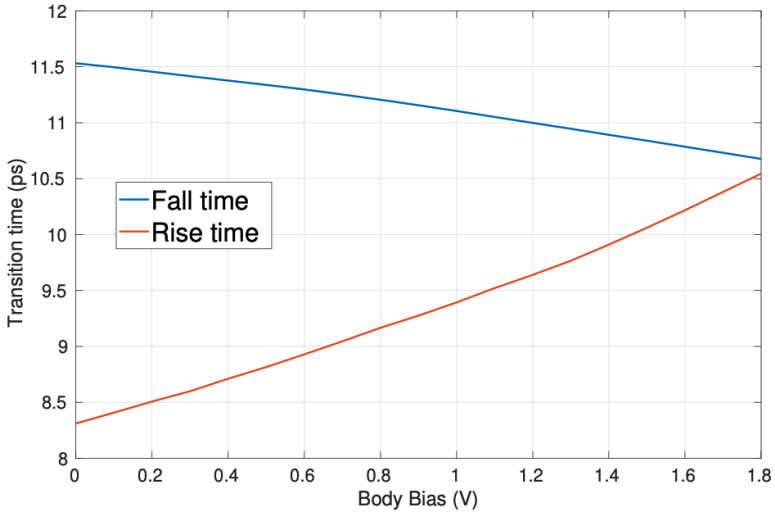


Figure 2.6: Effect of body biasing on the rise and fall times of an inverter output in 28 nm FD-SOI CMOS technology. The same back-gate voltage is applied simultaneously to the NMOS and PMOS transistors forming the inverter. Reproduced from [30].

systems. Their minimal silicon area enables full on-chip integration without the need for external passive components, a key advantage for cost-sensitive IoT and sensor applications. When combined with body-bias tuning, FD-SOI ring VCOs achieve competitive phase-noise and power-efficiency trade-offs, typically exhibiting phase noise below -80 dBc/Hz at 1 MHz offset for power consumption of less than 1 mW [26, 32, 27]. Furthermore, digital-to-analog converters (DACs) and switched-capacitor filters can be employed to generate precise body-bias voltages, providing fine-grained control of oscillation frequency and enabling noise shaping within the loop.

Challenges

Despite these advantages, FD-SOI CMOS ring oscillators face limitations in phase noise, supply sensitivity, and intrinsic Q factor compared with LC oscillators [29]. The achievable phase noise is constrained by the delay-cell noise and the number of stages, while supply noise directly modulates frequency through delay variations. Maintaining low jitter at GHz frequencies under low-voltage operation remains a demanding task, requiring careful biasing, layout symmetry, and noise filtering.

2.4.3 State of the Art

PLL Architecture Overview

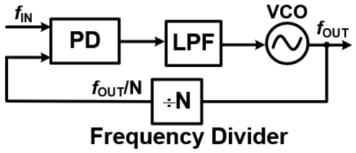
Modern PLLs can be categorized according to their implementation strategy and performance trade-offs. The main architectures include [33]:

- **Analog PLLs (APLLs):** classical charge-pump loops offering low phase noise and

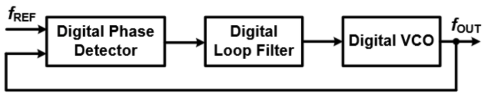
high spectral purity, typically used in RF transceivers and clock synthesizers.

- **Digital and All-Digital PLLs (DPLLs/ADPLLs):** architectures replacing analog blocks with time-to-digital converters (TDCs) and digitally controlled oscillators (DCOs), providing superior programmability and scalability in advanced CMOS and FD-SOI technologies.
- **Integer-*N* and Fractional-*N* PLLs:** frequency synthesizers based on integer or fractional frequency division, balancing tuning resolution and spurious performance.
- **Sub-Sampling and Injection-Locked PLLs:** specialized topologies optimized for ultra-low-power operation and low jitter, particularly suited for IoT and energy-constrained systems.

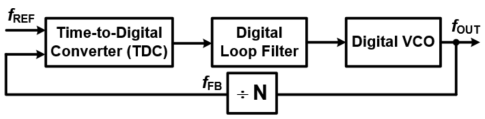
The different architectures are summarized in Figure 2.7.
Each architecture represents a specific trade-off among integration level, noise performance, power consumption, and tuning range. In the context of FD-SOI CMOS, body-bias control and low-voltage operation further enhance the flexibility of these PLL implementations, enabling efficient and scalable frequency synthesis for modern mixed-signal systems.



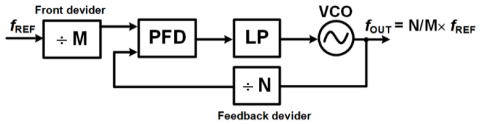
(a) Analog PLL block diagram.



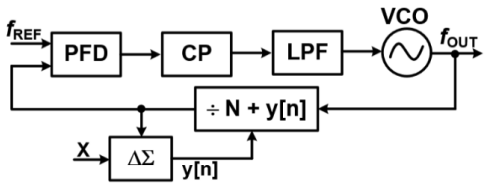
(b) Digital PLL block diagram.



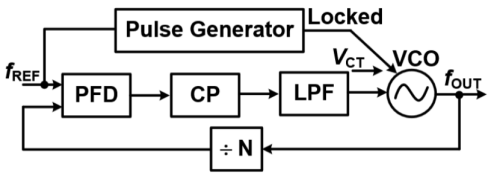
(c) All-Digital PLL block diagram.



(d) Integer-N PLL block diagram.



(e) Fractional-N PLL block diagram.



(f) Injection-Locked PLL block diagram.

Figure 2.7: Overview of the main PLL architectures: (a) Analog PLL, (b) Digital PLL, (c) All-Digital PLL, (d) Integer-N PLL, (e) Fractional-N PLL, and (f) Injection-Locked PLL (IL-PLL). Reproduced from [33].

Performance Metrics

The main performance indicators of phase-locked loops PLLs are phase noise, jitter, frequency range, power consumption, and lock time. A key figure of merit for oscillators is the phase-noise FoM, defined as:

$$\mathrm{FoM}_{\mathrm{PN}} = L(\Delta f) - 20\log_{10}\left(\frac{f_{\mathrm{osc}}}{\Delta f}\right), \tag{2.13}$$

where $L(\Delta f)$ denotes the single-sideband phase noise at an offset Δf from the carrier, and f_{osc} the oscillation frequency. For state-of-the-art FD-SOI CMOS ring VCOs—such as those presented in Table 2.1 and reported by D. Gaidioz *et al.* [32] and A. Asprilla [27]—typical $L(1\ \mathrm{MHz})$ values range from -82 to -96 dBc/Hz, corresponding to $\mathrm{FoM}_{\mathrm{PN}}$ values between -150 and -160 dBc/Hz. These results highlight the steady improvement in achieving competitive spectral purity through device optimization and biasing techniques. In ULV/ULP design contexts, power efficiency becomes an equally critical performance factor. Two complementary metrics are commonly used to evaluate this aspect. The first is the power-normalized phase noise figure of merit:

$$\mathrm{FoM}_{\mathrm{Power}} = \mathrm{FoM}_{\mathrm{PN}} + 10\log_{10}\left(\frac{P_{\mathrm{DC}}}{1\ \mathrm{mW}}\right), \tag{2.14}$$

where P_{DC} is the oscillator's DC power consumption.

The second, introduced by D. Gaidioz [26], is the *power spent per frequency*, defined as:

$$\text{Power spent per frequency} = \frac{\text{Power Consumption (mW)}}{\text{Output Frequency (GHz)}}. \tag{2.15}$$

This last metric provides an intuitive measure of energy efficiency by directly relating the consumed power to the oscillation frequency. In FD-SOI CMOS technologies, both Gaidioz *et al.* [32] and Asprilla [27] report values below 0.7 mW/GHz, confirming the excellent energy efficiency achievable through body-bias optimization and low-voltage operation.

Together, these figures of merit enable fair comparison of oscillator performance across different technology nodes and biasing conditions, offering a unified framework for evaluating phase noise and power efficiency in modern PLL and VCO design.

State of the Art of Ring Oscillators in Modern PLLs

A review of recent works demonstrates the rapid evolution of ring oscillators and their integration into modern PLLs working around 2.4 GHz across both FD-SOI CMOS and bulk CMOS technologies. Table 2.1 summarizes representative designs reported in the literature, highlighting progress in phase noise, tuning range, and especially energy efficiency.

In FD-SOI CMOS technologies, such as the 28 nm node studied by D. Gaidioz *et al.* [32], body-bias tuning provides wide frequency agility (up to 120%) while maintaining sub-milliwatt power consumption. A. Asprilla [27] further demonstrated that combining a ring VCO with a voltage-controlled delay line (VCDL) can enhance frequency linearity at the expense of area, achieving a power spent per frequency as low as 0.15 mW/GHz. These results confirm the strong potential of FD-SOI CMOS for energy-efficient frequency generation at low supply voltages.

Bulk CMOS realizations, such as those by Y. Choi *et al.* [34] and Q. Zhang *et al.* [35], still achieve competitive phase noise performance (-89 to -126 dBc/Hz at 1 MHz offset) but at significantly higher power consumption, typically in the milliwatt range per gigahertz. This difference highlights the intrinsic advantage of FD-SOI CMOS technology, where low leakage and body-bias control enable operation closer to the energy-delay optimum. The wideband implementation by Z. Xu *et al.* [36] in 22 nm CMOS confirms that, even in bulk processes, ring-based oscillators remain viable for broadband PLLs when energy efficiency is traded for frequency range.

Overall, the evolution of ring oscillators in modern PLLs reveals two complementary trends: (i) the steady enhancement of spectral purity, with $\mathrm{FoM_{PN}}$ values reaching -160 dBc/Hz, and (ii) a growing focus on energy efficiency, with $\mathrm{FoM_{Power}}$ below -155 dBc/Hz and power spent per frequency under 1 mW/GHz in optimized FD-SOI CMOS designs. These advances demonstrate that ring-based VCOs, once limited to low-performance applications, are now credible solutions for fully integrated, low-voltage PLLs targeting IoT, sensor, and communication systems. This evolution motivates the exploration of new body-bias and switched-capacitor control techniques, which will be discussed in the following chapters.

Table 2.1: Representative FD-SOI CMOS and Bulk CMOS Ring VCOs / PLLs Reported in Literature

Reference	**D. Gaidioz et al.** [32]	**A. Asprilla** [27]	**Y. Choi et al.** [34]	**Q. Zhang et al.** [35]	**Z. Xu et al.** [36]
Technology	28nm FD-SOI CMOS	28nm FD-SOI CMOS	65 nm CMOS	28nm CMOS	22 nm CMOS
Topology	PD-RVCO	RVCO	PD-RVCO	PD-RVCO	RVCO
f_{osc} **[GHz]**	1.76	2.5	4.0	1.5	2.27
PN@1MHz [dBc/Hz]	-95.7	-82*	-89.3	-78*	-73.8
Power [mW]	1.1	0.387*	4.28	6.16†	1.8
$\mathbf{FoM}_{\mathbf{PN}}^{(1)}$	-160.61	-149,96	-161.38	-141.52	-140.87
$\mathbf{FoM}_{\mathbf{Power}}^{(2)}$	-160.2	-154.08	-155.07	-133.63	-138.32
Tuning Range (%)	119.5	24.3	N/A	N/A	149.8
Supply Voltage [V]	1.0	1.0	1.0	1.0	N/A
Area [μm^2]	800	7290*	N/A	N/A	N/A
Power spent per frequency$^{(3)}$ **(mW/GHz)**	0.625	0.155	1.07	4.11	0.793

* VCO + VCDL.
† All analog part.
* Obtained from graphical extrapolation.
(1) $\mathrm{FoM_{PN}} = PN@1MHz - 20\log_{10}\left(\frac{f_0}{1\mathrm{MHz}}\right)$.
(2) $\mathrm{FoM_{Power}} = PN@1MHz - 20\log_{10}\left(\frac{f_0}{1MHz}\right) + 10\log_{10}\left(\frac{P}{1\mathrm{mW}}\right)$
(3) Power spent per frequency = Power Consumption (mW) / Output Frequency (GHz)

2.5 Conclusion

This chapter has reviewed the technological and theoretical foundations that underpin the work developed in the subsequent chapters. The overview of FD-SOI CMOS technology emphasized its capacity to combine planar scalability with body-bias-driven performance modulation, positioning it as a leading solution for energy-efficient analog and RF design. The discussion on charge-based modeling highlighted its critical role in enabling accurate simulation and optimization of such devices under low-voltage and dynamic biasing conditions. Finally, the state-of-the-art analysis of VCOs and PLLs demonstrated how these concepts converge in practice, yielding fully integrated, body-bias-controlled oscillators that bridge the gap between device physics and system-level innovation. These insights collectively form the basis for the modeling and design strategies proposed in the following chapters.

3

Charge-Based Modeling: Theoretical Advances from Mathematical Insights and Experimental Validation in 28nm FD-SOI CMOS Technology

This third chapter introduces charge-based modeling for MOSFET transistors using the ACM formalism. It presents a novel implementation of charge-based models through an analytical approximation of the Lambert function's principal branch. The proposed model is validated by comparing it to an industry-standard model one, demonstrating the effectiveness and accuracy of the new implementation.

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3.1 Introduction

Ultra-low power and ultra-low voltage requirements, as commonly encountered in IoT applications, impose stringent constraints on circuit energy consumption. Unlike digital circuits, which readily benefit from technology scaling, analog designers working with advanced technologies must shift transistor operation away from the strong inversion region toward the moderate and weak inversion regimes to meet these demands [37]. Describing the physical behavior of the transistor in these regimes taking into account the emergence of short-channel effects in advanced nanometric technologies is a challenging endeavor. Simple models like the long-channel strong-inversion approximation are no longer valid and designers have to rely on complex simulation-based transistor models that accurately describe the transistor behavior and computer-based optimization campaigns to appropriately size their circuits. This simulation-based design methodology is lengthy, resource-intensive and makes difficult to gain an intuitive understanding of the link between design performance and transistor parameters.

In order to overcome the issues of simulation-based design methodologies, simplified design methodologies have been proposed such as the g_m/I_D or the inversion coefficient (IC) based methodologies [38] [39] [40] [41] [42] [43] [44] [45] [46]. These design methods propose an efficient design-space exploration based on simplified design-oriented models that approximate the transistor behavior using a reduced set of model parameters. Accurate and simple design-oriented models describing with precision the behavior of the transistor in all operating regions and regimes are then required to make the best use of these design methods.

In this regard, design-oriented inversion charge-based models have been presented in the last few years [47] [48] [49] [24] [50] [23] [51] [52] [53], usually based on the ACM or EKV formalisms. Different implementations of these design-oriented models have been developed with different levels of complexity, from the classical three-parameter model for long-channel transistors presented in [47] to a seven-parameter model considering short-channel effects for advanced technologies in [24]. These models are well-suited for design applications because of their reduced set of parameters and their fully continuous behavior. It should be noted that these models are compatible with all types of transistors based on the MOS technology operation principles. Thus, the ACM model was initially proposed for bulk CMOS transistors [47] and was subsequently extended to SOI transistors [24] [23]. Recent articles, such as [54], demonstrate that a charge-based model can effectively describe the behavior of FinFET transistors, considering specific physical characteristics of FinFETs. However, the drawback of these all-regime all-region models is the lack of an explicit analytical link between the drain current and the transistor node voltages. Indeed, these models express both the transistor's DC drain current and the transistor's node voltages as a function of the normalized inversion charges at the source

and drain sides of the transistor. The resulting system of equations defines a set of transcendental equations[1] and requires a numerical solver to finally obtain the transistor's DC drain current for a given set of values of the transistor's node voltages.

Due to the transcendental nature of the model equations, even if the models remain simple, the intuitive link between voltage and current is unfortunately lost behind the use of a numerical solver, which leads again to computation complexity and complicates the understanding of the transistor behavior.

In this chapter, a single-piece continuous and explicit MOSFET model for advanced technologies is presented. This model, based on the ACM inversion charge formalism, expresses the MOS transistor's drain current as an explicit function of the transistor's node voltages in a closed-form analytical expression valid for all the operation zones of the transistor. Although the ACM formalism is employed in this manuscript, it should be noticed that the proposed approach is directly applicable to other charge-based models such as EKV. The proposed explicit model is based on a recently proposed approximation of the Lambert W-function [55] that avoids the need of a numerical solver in the model implementation, combined with a new description of the transistor's saturation based on a modification of the Unified Charge Control Model (UCCM) [50], that lead to express the transistor's drain current as a single-piece equation.

It is worth noting that, while the ACM model is founded on a physically based approach, our methodology takes a complementary empirical and mathematical perspective. This approach was adopted to effectively address certain discrepancies observed in specific performance metrics, which may arise from the inherent simplifications in the physical modeling of some effects within the ACM framework. By doing so, our model seeks to provide an enhanced transistor description with an explicit analytical formulation that supports intuitive analysis and practical design.

[1] A transcendental equation is an equation that is not algebraic, that is, at least one of its sides contains a transcendental function. A transcendental function, such as the exponential, logarithmic and trigonometric function, in contrast to an algebraic function, cannot be expressed algebraically using a finite amount of terms. Transcendental equations are common in applied mathematics and cannot be solved through simple algebraic manipulations.

3.2 Design-Oriented 6-Parameter Inversion Charge-Based Model

3.2.1 Parameters Overview

The aim of a design-oriented model is to assist designers during the initial stages of circuit design. These models have to be built to offer a good trade-off between the model simplicity and accuracy in such a way that the model remains simple to manipulate while approximating the transistor's behavior as closely as possible. In this regard, the proposed 6PM design-oriented model describes the transistor's DC behavior based on only 6 DC parameters linked to different physical effects.

The proposed 6PM model, presented hereafter, is built on the basis of the ACM formalism [20]. Thus, the model includes the three classical parameters from the basic ACM model: the subthreshold slope factor, n, the equilibrium threshold voltage, V_{T0}, and the specific current, I_{S0}, which are enough to approximate the behavior of a long-channel MOS transistor. Three other parameters are added to account for short-channel effects. The first one is the drain-induced barrier lowering (DIBL) effect, which leads to a reduction of the carrier's barrier potential occurring at the source side as the drain voltage increases. This effect is represented in the model by the dimensionless DIBL effect factor, σ, that modulates the threshold voltage depending on the DC voltages applied to the source and drain terminals. The effective mobility of the carriers in the inversion layer is directly linked to the vertical electrical field along the channel. The mobility decreases as the applied electrical field increases, which results in a reduction of the drain current and is represented in the model by the mobility reduction factor, θ. Finally, the carrier velocity saturation effect models the limited increase of the velocity of the carriers when the horizontal electric field increases, which again results in an effective reduction of the drain current. This effect is represented in the model by the carrier velocity saturation effect parameter, ζ. This dimensionless parameter is defined as,

$$\zeta = \frac{\mu U_T}{L} \cdot \frac{1}{v_{sat}}, \tag{3.1}$$

where μ is the effective mobility of the carriers, $U_T = \frac{kT}{q}$ is the thermal voltage, L is the transistor length, and v_{sat} is the saturation velocity of the carriers. The presented parameters are summarized in Table 3.1.

Concerning the dependence of the model parameters with the transistor geometry, that is, its Length, L, and Width, W, it is important to emphasize that parameters n, V_{T0}, σ, ζ, and θ are influenced exclusively by L. Conversely, parameter I_{S0}, has a dependency on both W and L, although the dependence with W is linear. Consequently, the geometrical dependencies of the inversion charges, the drain current and its derivatives, are directly

Table 3.1: Summary of the 6PM model parameters

Symbol	Name	Variation with
n	Sub-threshold slope factor (-)	L
V_{T0}	Equilibrium threshold voltage (V)	L
I_{S0}	Specific current (A)	L, W
σ	DIBL effect factor (-)	L
ζ	Carrier velocity saturation factor (-)	L
θ	Mobility reduction factor (-)	L

incorporated into the MOSFET model parameters. In a practical application, the usual modeling approach consists in extracting a different set of model parameters for each of the transistor's lengths considered. Nevertheless, it is also possible to derive geometrical scaling laws that represent the model parameters as a function of the transistor dimensions, as demonstrated in [56].

3.2.2 Model Equations

The main equation in the proposed model describes the behavior of the DC drain current I_D taking into account both drift and diffusion currents as well as the saturation velocity and mobility reduction phenomena. Thus, the normalized drain current, i_D, is expressed as,

$$\boxed{i_D = \frac{I_D}{I_{S0}} = \frac{(q_S - q_D)(q_S + q_D + 2)}{[1 + \zeta(q_S - q_D)][1 + \theta(q_S + q_D)]}}, \tag{3.2}$$

where I_{S0} is the specific current, and q_S and q_D are the normalized inversion charge densities at the source and drain sides of the transistor, respectively.
The specific current is defined as,

$$I_{S0} = \mu n C'_{ox} \frac{U_T^2}{2} \frac{W}{L_{eff}}, \tag{3.3}$$

where C'_{ox} is the oxide capacitance per unit area, W is the width of the transistor and L_{eff} is its effective length.
The normalized inversion charge densities are defined as,

$$q_i = \frac{Q_i}{Q_P}, \tag{3.4}$$

where, Q_i represents a charge density (corresponding to source or drain) and Q_P is the pinch-off charge per unit area defined as

$$Q_P = \pm n C'_{ox} U_T, \tag{3.5}$$

where the plus sign refers to a p-channel transistor and the minus one indicates an n-channel transistor.

The model equations are completed by the relationship between the normalized inversion charges and the transistor node voltages. These equations are defined by the Unified Charge-Control Model (UCCM). We employ the formalism first introduced in [50] to describe the saturation effect directly in the UCCM equations, as

$$\boxed{v_P - v_{S(D)B} = q'_{S(D)} - 1 + \ln\left(q'_{S(D)}\right)}, \tag{3.6}$$

where drain and source voltages are normalized with respect to U_T and v_P is the normalized pinch-off voltage approximated as,

$$v_P \approx \frac{1}{U_T} \cdot \frac{V_{GB} - V_{T0} + \sigma\left(V_{DB} + V_{SB}\right)}{n}. \tag{3.7}$$

Introducing the modulated threshold voltage, defined as

$$V_T = V_{T0} - \sigma\left(V_{DB} + V_{SB}\right), \tag{3.8}$$

(3.7) can be expressed as,

$$v_P \approx \frac{1}{U_T} \cdot \frac{V_{GB} - V_T}{n}. \tag{3.9}$$

In order to consider the carrier velocity saturation effect, modulated normalized source and drain inversion charges, q'_S and q'_D, respectively, have been introduced. They are defined as,

$$q'_{S(D)} = q_{S(D)} - q_{sat}, \tag{3.10}$$

where q_{sat} represents the normalized saturation drain charge ratio and is related to the normalized saturated drain current by

$$i_{Dsat} = \frac{2}{\zeta} q_{sat}. \tag{3.11}$$

The introduction of q_{sat} in the UCCM equations allows for a continuous description of the transistor behavior across the different operation zones, avoiding the definition of a saturation voltage leading to a piece-wise set of equations and a higher calculation com-

plexity. It is also worth noticing that by modulating both the source and drain inversion charges, the resulting equations are symmetrical, in the sense that interchanging drain and source terminals results in a change of sign of V_{DS} but the transistor behavior remains the same.

Expressions (3.2) and (3.6) define a system of equations that determines the value of the transistor's DC drain current as a function of the transistor's DC node voltages. The analytical solution of the system can be written in terms of the Lambert W-function, which is defined as the solution of the transcendental equation (3.6), as,

$$q'_{S(D)} = W(x_{S(D)}), \tag{3.12}$$

where,

$$x_{S(D)} = e^{\left[v_P - v_{S(D)B} + 1\right]}. \tag{3.13}$$

The normalized saturation drain charge ratio q_{sat} can then be expressed as

$$q_{sat} = \frac{\zeta}{2}\left[(W(x_S)+1)^2 - 1\right]. \tag{3.14}$$

Substituting (3.12) and (3.14) in (3.10) leads to,

$$\boxed{q_{S(D)} = W(x_{S(D)})\left[1 + \frac{\zeta}{2}W(x_{S(D)}) + \zeta\right]}, \tag{3.15}$$

which can be introduced in (3.2) to compute the transistor drain current. It is interesting to note that $\frac{\zeta}{2}W(x_{S(D)}) \ll 1$ when the transistor is not saturated which leads to

$$q_{S(D)} = W(x_{S(D)})\,[1+\zeta] \approx W(x_{S(D)}), \tag{3.16}$$

and thus to $q'_{S(D)} \approx q_{S(D)}$, which enables to create a link between the modified UCCM used in this paper and the classical one, not taking into account the carrier velocity saturation effect, which is commonly used in the literature.

3.2.3 Historical Implementation

Owing to the transcendental nature of Equation (3.6), the solution given by (3.12) requires the use of a numerical solver. This limitation is common to models based on the UCCM equation. Consequently, the classical implementation of these models relies on an efficient numerical solver, such as the acm 443 algorithm, to compute the solution of the UCCM equations.

The numerical implementation of the proposed model is conceptually depicted in Figure 3.1. For a given set of DC node voltages (V_{GB}, V_{DB}, V_{SB}), the evaluation of the corre-

sponding DC drain current I_{DC} begins by calculating the transistor's modulated threshold voltage and the associated pinch-off voltage. From there, all the variables of the modified UCCM equation are set and the modulated normalized source and drain inversion charges, as well as the normalized saturation drain charge can be determined by using the 443 algorithm to solve the modified UCCM equations (3.6). Once the charges are computed, they are introduced in the current equation (3.2) to evaluate the DC drain current of the transistor.

Although the ACM 443 algorithm is computationally efficient, relying on a numerical solver complicates manual calculations and limits intuitive insight into the transistor's behavior.

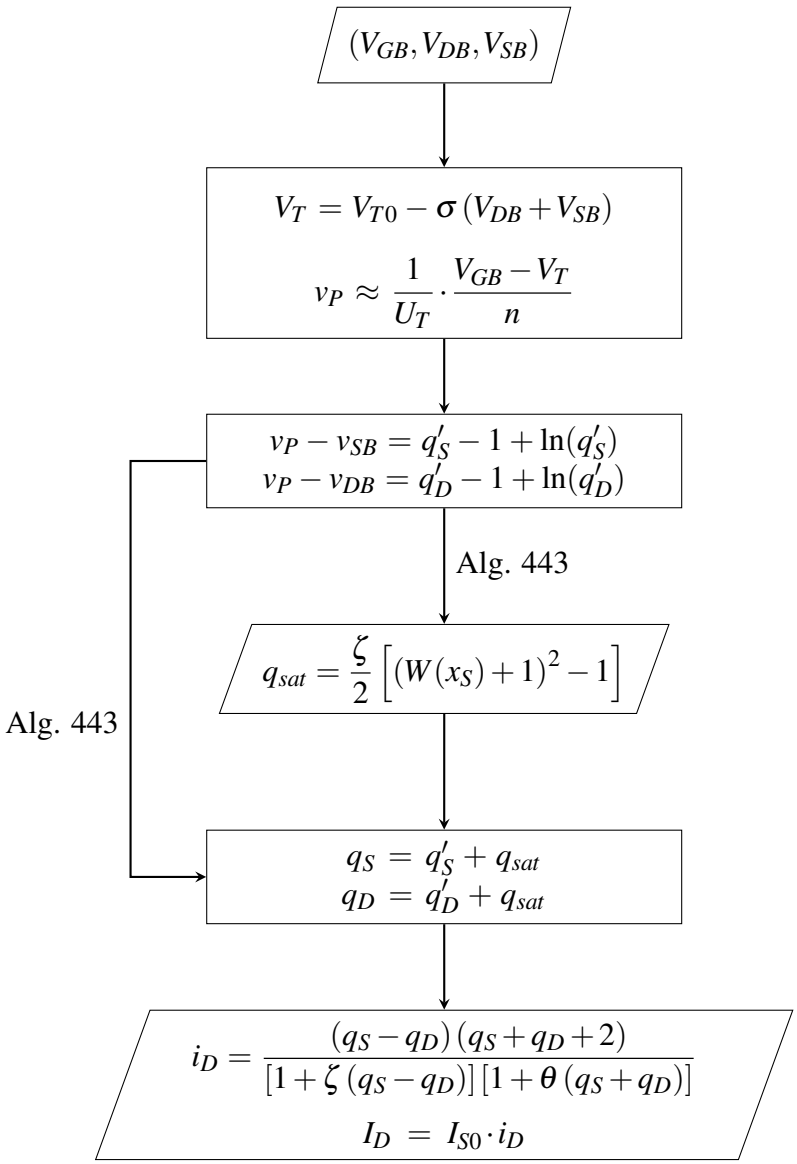


Figure 3.1: Conceptual flowchart for DC current evaluation using the proposed model and the acm 443 numerical solver.

3.2.4 Parameters Extraction

The parameters extraction is divided into three main steps, first the extraction of the three long-channel parameters, to be known the sub-threshold slope factor n, the equilibrium threshold voltage V_{T0}, and the specific current I_{S0} by the g_m/I_D method presented in [57] ; secondly the extraction of the drain-induced barrier lowering effect factor σ by modulating the drain-to-bulk voltage ; finally the carrier velocity saturation factor ζ and the mobility reduction factor θ are extracted by curves fitting.

3.2.4.1 Sub-threshold Slope Factor, Equilibrium Threshold Voltage, and Specific Current

In order to extract the three main long-channel parameters, a common source configuration, with V_{DS} fixed to $U_T/2$, as presented in Figure 3.2 is used. The long-channel parameters extraction process assumes the short-channel parameters to be zero. This assumption is justified because the long-channel parameters are determined in the linear region of the MOSFET's characteristic, where short-channel effects are negligible and thus do not significantly influence the results.

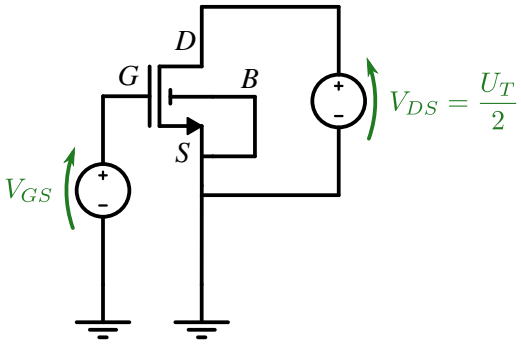


Figure 3.2: Common source configuration for the three long-channel parameters extraction.

Sub-threshold Slope Factor n: The transconductance-to-drain current ratio $\frac{g_m}{I_D}$ is expressed as

$$\frac{g_m}{I_D} = \frac{2}{n \cdot U_T \cdot \left(\sqrt{1+i_F} + \sqrt{1+i_R}\right)}, \tag{3.17}$$

where i_F is the normalized forward current, defined as

$$i_F = \frac{I_F}{I_{S0}} = (q_S + 1)^2 - 1, \tag{3.18}$$

and i_R is the normalized reverse current, defined as

$$i_R = \frac{I_R}{I_{S0}} = (q_D + 1)^2 - 1. \tag{3.19}$$

According to [58], the asymptotic value of the g_m/I_D curve in weak inversion, $\left(\frac{g_m}{I_D}\right)_{max}$, is related to the sub-threshold slope factor n by

$$\left(\frac{g_m}{I_D}\right)_{max} \approx \frac{1}{n \cdot U_T}, \tag{3.20}$$

which leads to Equation 3.21.

$$\boxed{n \approx \frac{1}{\left(\frac{g_m}{I_D}\right)_{max} \cdot U_T}} \tag{3.21}$$

Equilibrium Threshold Voltage V_{T0}: Assuming $\sigma = 0$ in Equation 3.7 leads to

$$v_P \approx \frac{1}{U_T} \cdot \frac{V_{GB} - V_{T0}}{n}. \tag{3.22}$$

Thus, when $V_{GB} = V_{T0}$, $v_P = 0$, leading to $q_S = 1$ and $i_F = 3$. Additionally, with $V_{DS} = \frac{U_T}{2}$, $q_D = 0.77$ and $i_R = 2.12$. Substituting these values in Equation 3.17 leads to Equation 3.23.

$$\boxed{V_{GB} = V_{T0} \Rightarrow \left(\frac{g_m}{I_D}\right)_{V_{GB}=V_{T0}} = 0.531 \cdot \left(\frac{g_m}{I_D}\right)_{max}} \tag{3.23}$$

Specific Current I_{S0}: From the previous results, Equation 3.2 leads to Equation 3.24.

$$\boxed{I_{S0} = \frac{I_D\,|_{V_{GB}=V_{T0}}}{0.88}} \tag{3.24}$$

3.2.4.2 Drain-Induced Barrier Lowering Effect Factor

The drain-induced barrier lowering effect factor σ can be extracted using the $I_D(V_{GB})$ curve for $V_{DS} = U_T/2$ and for another polarization that could be set to the nominal supply value of the technology, here corresponding to $V_{DS} = 1V$. From the two curves, the corresponding V_{GB} for a given drain current, denoted as I_{D0} are extracted and σ is calculated using Equation 3.25.

$$\boxed{\sigma = \left|\frac{\Delta V_{GB}\,|_{I_{D0}}}{\Delta V_{DB}}\right|} \tag{3.25}$$

3.2.4.3 Carrier Velocity Saturation Factor and Mobility Reduction Factor

Carrier velocity saturation factor ζ and mobility reduction factor θ are extracted from fittings. Several $I_D(V_{GB})$ curves in common source configuration are plotted for several V_{DB}, as well as several $I_D(V_{DB})$ curves in common source configuration for several V_{GB}, to cover different inversion regions and operating regimes. Equation 3.2 is plotted along the different curves, first for $\theta = 0$ to extract ζ. Then keeping the found ζ value, θ is modulated.

3.3 Explicit I-V 6PM Model

3.3.1 Lambert W-Function Approximation

A novel formulation of the solution to the UCCM equations is proposed, allowing to get an explicit and single-piece equation linking the transistor's DC drain current and its node voltages.

Using analytical expressions instead of numerical solvers has its benefits. Firstly, it enables a faster and more efficient exploration of the design space, leading to a better understanding of the circuit performances and their relationship with the physics of the transistor. Moreover, it will be shown that the proposed formulation is derivable, and hence, it facilitates to establish links between circuit performances, usually related to the derivatives of the drain current, and the transistor parameters.

The formulation of the proposed explicit $I-V$ model is based on a recently published approximation of the Lambert W-function [55]. As seen before, the normalized source and drain charge ratios are determined by evaluating the Lambert W-function, which is the solution to the transcendental equation defined as

$$W(x)e^{W(x)} = x. \tag{3.26}$$

This function has two real branches. The branch of interest for our study is the one for $x \in \left[-\frac{1}{e}, \infty\right[$, which is called the principal branch and contains the domain of application of our model, defined from (3.13), as $x \in [0, \infty[$.

From [55], the Lambert W-function, for $x \geq 0$, can be approximated by the terms of the series,

$$W_0(x) = \ln\left[1 + \alpha(x)x\right], \tag{3.27}$$

$$W_n(x) = \frac{W_{n-1}(x)}{1 + W_{n-1}(x)}\left[1 + \ln\left(\frac{x}{W_{n-1}(x)}\right)\right], \tag{3.28}$$

where $n = 1, 2, 3\ldots$, and function $\alpha(x)$ is defined by

$$\alpha(x) = \frac{1}{1 + \dfrac{\ln(1+x)}{2}}. \tag{3.29}$$

The approximation of the Lambert W-function improves as n increases. For $n = 0$, the maximum relative error in the approximation for all the considered branch is below 4%. For $n = 1$ this error is reduced below 0.022%. The series matches the accuracy of numerical solvers for $n = 3$.

In this work, we will employ the approximation $W(x) \approx W_0(x)$, which gives us a good trade-off between model complexity and accuracy.

3.3.2 Explicit $q_{S(D)}$ and I_D Expressions as a Function of the Transistor's Node Voltages

Based on the proposed approximation of the Lambert W-function, the modulated normalized source and drain inversion charges can be obtained from equations (3.12), (3.13), and (3.27) as,

$$q'_{S(D)} = \ln\left[1 + \frac{e^{v_P - v_{S(D)B} + 1}}{1 + \frac{1}{2}\ln\left(1 + e^{v_P - v_{S(D)B} + 1}\right)}\right]. \tag{3.30}$$

Equation (3.30) can be expanded in order to get a continuous single-piece expression for the normalized source and drain inversion charges dependent on the transistor's terminal voltages, which leads to (3.31).

$$\boxed{q_{S(D)} = \ln\left[1 + \frac{e^{v_P - v_{S(D)B} + 1}}{1 + \frac{1}{2}\ln\left(1 + e^{v_P - v_{S(D)B} + 1}\right)}\right]\left[1 + \frac{\zeta}{2}\ln\left[1 + \frac{e^{v_P - v_{S(D)B} + 1}}{1 + \frac{1}{2}\ln\left(1 + e^{v_P - v_{S(D)B} + 1}\right)}\right] + \zeta\right].} \tag{3.31}$$

Similarly, the explicit expressions of the normalized charges (3.31) can be directly injected in (3.2) to obtain a continuous single-piece explicit equation for the transistor's DC drain current expressed as a function of the transistor's node voltages as (3.36), where A, B, C, and D are defined as,

$$A = W_0(x_S) - W_0(x_D), \tag{3.32}$$

$$B = W_0(x_S) + W_0(x_D), \tag{3.33}$$

$$C = W_0^2(x_S) - W_0^2(x_D), \tag{3.34}$$

$$D = W_0^2(x_S) + W_0^2(x_D). \tag{3.35}$$

The obtained I_D approximation makes no assumption on the values of the DC node voltages and hence it is valid in all regions (linear to saturation) and regimes of operation (weak to strong inversion).

$$\boxed{I_D = I_{S0}\frac{\left[(1+\zeta)A + \frac{\zeta}{2}C\right]\left[(1+\zeta)B + \frac{\zeta}{2}D + 2\right]}{1 + \zeta\left[(1+\zeta)A + \frac{\zeta}{2}C\right] + \theta\left[(1+\zeta)B + \frac{\zeta}{2}D\right] + \zeta\theta\left[(1+\zeta)A + \frac{\zeta}{2}C\right]\left[(1+\zeta)B + \frac{\zeta}{2}D\right]}}. \tag{3.36}$$

3.3.3 Explicit g_m Expression as a Function of the Transistor's Node Voltages

The obtained explicit $I-V$ model is continuous and derivable, which allows to compute, analytically, the small signal parameters of the transistor. Thus, the small signal transconductance g_m of the transistor can be directly evaluated as,

$$g_m = \frac{\partial I_D}{\partial V_{GS}}. \tag{3.37}$$

Before computing the derivative, it is convenient to rearrange the DC current equation (3.2) as,

$$i_D = \frac{E\,(F+2)}{1+\zeta E+\theta F+\zeta\theta EF}, \tag{3.38}$$

where E and F are given by,

$$E = (1+\zeta)A + \frac{\zeta}{2}C, \tag{3.39}$$

$$F = (1+\zeta)B + \frac{\zeta}{2}D. \tag{3.40}$$

Simply applying the definition of the transconductance (3.37), we can arrive to a single-piece closed-form expression for the transistor's small signal transconductance that, again, is valid in all regions and regimes of operation. The equation of the transconductance is expressed in (3.41) as a function of the derivatives of E and F and considering that the bulk and source terminals are connected. The derivatives of E and F are detailed hereafter in equations (3.45) and (3.46).

$$\boxed{g_m = \frac{I_{S0}}{U_T}\frac{[E'(F+2)+EF'][1+\zeta E+\theta F+\zeta\theta EF]-E[F+2][\zeta E'+\theta F'+\zeta\theta(E'F+F'E)]}{[1+\zeta E+\theta F+\zeta\theta EF]^2}}. \tag{3.41}$$

In order to compute the derivatives of E and F, the derivatives of W_0 and W_0^2 are expressed as,

$$W_0'(x_{S(D)}) = \frac{\partial W_0}{\partial v_{GB}}\left(x_{S(D)}\right) = \frac{\dfrac{\Gamma_{S(D)}}{n} - \dfrac{\Gamma_{S(D)}^2}{2n\left(1+x_{S(D)}\right)}}{\Gamma_{S(D)}+1}, \tag{3.42}$$

and,

$$\frac{\partial W_0^2}{\partial v_{GB}}\left(x_{S(D)}\right) = 2\cdot\frac{\partial W_0}{\partial v_{GB}}\left(x_{S(D)}\right)\cdot\ln\left[\Gamma_{S(D)}+1\right], \tag{3.43}$$

where function $\Gamma_{S(D)}$ is given by,

$$\Gamma_{S(D)} = \frac{x_{S(D)}}{\frac{1}{2}\ln\left(1+x_{S(D)}\right)+1}. \tag{3.44}$$

The derivatives of E and F can be written as a function of $W_0'(x_{S(D)})$ and $\Gamma_{S(D)}$ as,

$$E' = \frac{\partial E}{\partial v_{GB}} = W_0'(x_S)\left(1+\zeta\left(1+\ln\left(1+\Gamma_S\right)\right)\right) - W_0'(x_D)\left(1+\zeta\left(1+\ln\left(1+\Gamma_D\right)\right)\right) \tag{3.45}$$

$$F' = \frac{\partial F}{\partial v_{GB}} = W_0'(x_S)\left(1+\zeta\left(1+\ln\left(1+\Gamma_S\right)\right)\right) + W_0'(x_D)\left(1+\zeta\left(1+\ln\left(1+\Gamma_D\right)\right)\right) \tag{3.46}$$

3.4 Results and Validation

3.4.1 Simulation Results

In order to validate the proposed model, comparisons were made from a low-threshold voltage NMOS transistor from the 28nm FD-SOI CMOS technology of STMicroelectronics. Simulation results were obtained for a common source configuration of the transistor, as depicted in Figure 3.3, connecting the source to the bulk, i.e., $V_S = V_B = 0V$.

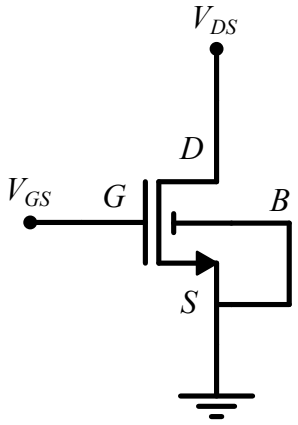


Figure 3.3: Common source configuration.

Using this configuration, Figures 3.5, 3.6, and 3.7 represent the obtained I_D-V_{GB} and I_D-V_{DB} curves for different values of V_{GB} for the former and V_{DB} for the latter. It is noteworthy that the common-source topology seems to appear as the most widely used topology in many analog, RF, and mmW designs implemented in integrated circuits, especially in CMOS technologies.

The considered voltage sweeps cover all operation regions and regimes of the transistor. Figure 3.5 corresponds to a short-channel transistor with a length of $L = 30\,\text{nm}$, Figure 3.6 corresponds to $L = 60$ nm and Figure 3.7 corresponds to a long-channel transistor of $L = 150\,\text{nm}$. All transistors have a width of $W = 1\ \mu\text{m}$ and their parameters are presented in Table 3.2. Figure 3.8 shows the I_D-V_{GB} curves in semilog scale to highlight the modeling of the subthreshold region for the three considered transistor's lengths.

Additionally, to better highlight the dependency of the drain current with the geometrical dimension of the transistor, W and L, Figure 3.4 illustrates a three-dimensional representation of I_D as a function of the channel width W and length L, at a constant gate-to-bulk voltage V_{GB} and drain-to-bulk voltage V_{DB} of $0.5V$, with the source-to-bulk voltage V_{SB} set to $0V$.

Figures 3.5, 3.6, 3.7, and 3.8 offer a direct comparison between the proposed design-oriented 6PM model (both numerically computed based on 443 algorithm and analytical based on explicit expressions), the industry-standard L-UTSOI compact model, and the

Table 3.2: Design-oriented 6PM model parameters for 28nm FD-SOI CMOS NMOS transistors ($W = 1\ \mu m$ for all considered transistors).

L	$30\,nm$	$60\,nm$	$150\,nm$
n	1.31	1.16	1.11
V_{T0} (mV)	352	388	414
I_{S0} (μA)	4.58	3.25	1.4
σ	0.093	0.023	0.0082
ζ	0.026	0.014	0.008
θ	0.039	0.041	0.018

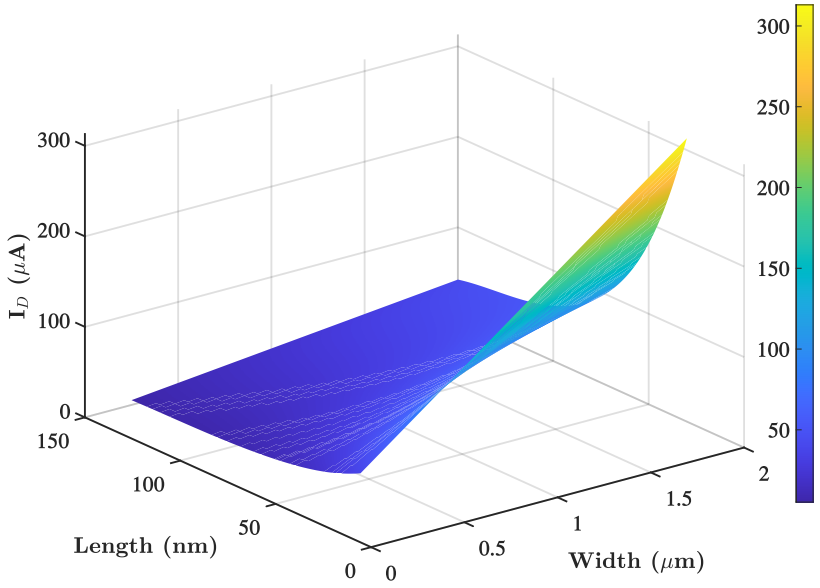


Figure 3.4: Three-dimensional plot of the drain current I_D as a function of the transistor channel width W and length L at $V_{GB} = V_{DB} = 0.5\,V$ and $V_{SB} = 0\,V$, using the proposed ACM 6PM.

5PM design-oriented model of [50] based on 443 algorithm resolution. Additionally, we represent also the relative error of the proposed 6PM model (both numerical and analytical solutions) with respect to the L-UTSOI model. For Figures 3.5, 3.6, 3.7, and 3.8, the proposed relative errors are defined as follows:

$$Rel.Error_{An.Res} = \frac{I_{D,An.Res} - I_{D,L-UTSOI}}{I_{D,L-UTSOI}}, \tag{3.47}$$

$$Rel.Error_{443} = \frac{I_{D,An.Res} - I_{D,443}}{I_{D,443}}. \tag{3.48}$$

As it can be seen, the proposed design-oriented 6PM model offers a very good approximation of the transistor behavior, very close to the L-UTSOI curves. Compared to the previously presented 5PM design-oriented model, the introduction of the mobility reduction parameter, θ, not present in the 5PM model, allows us to better model the transistor behavior for strong values of V_{GS}, both for short-channel and long-channel transistors.

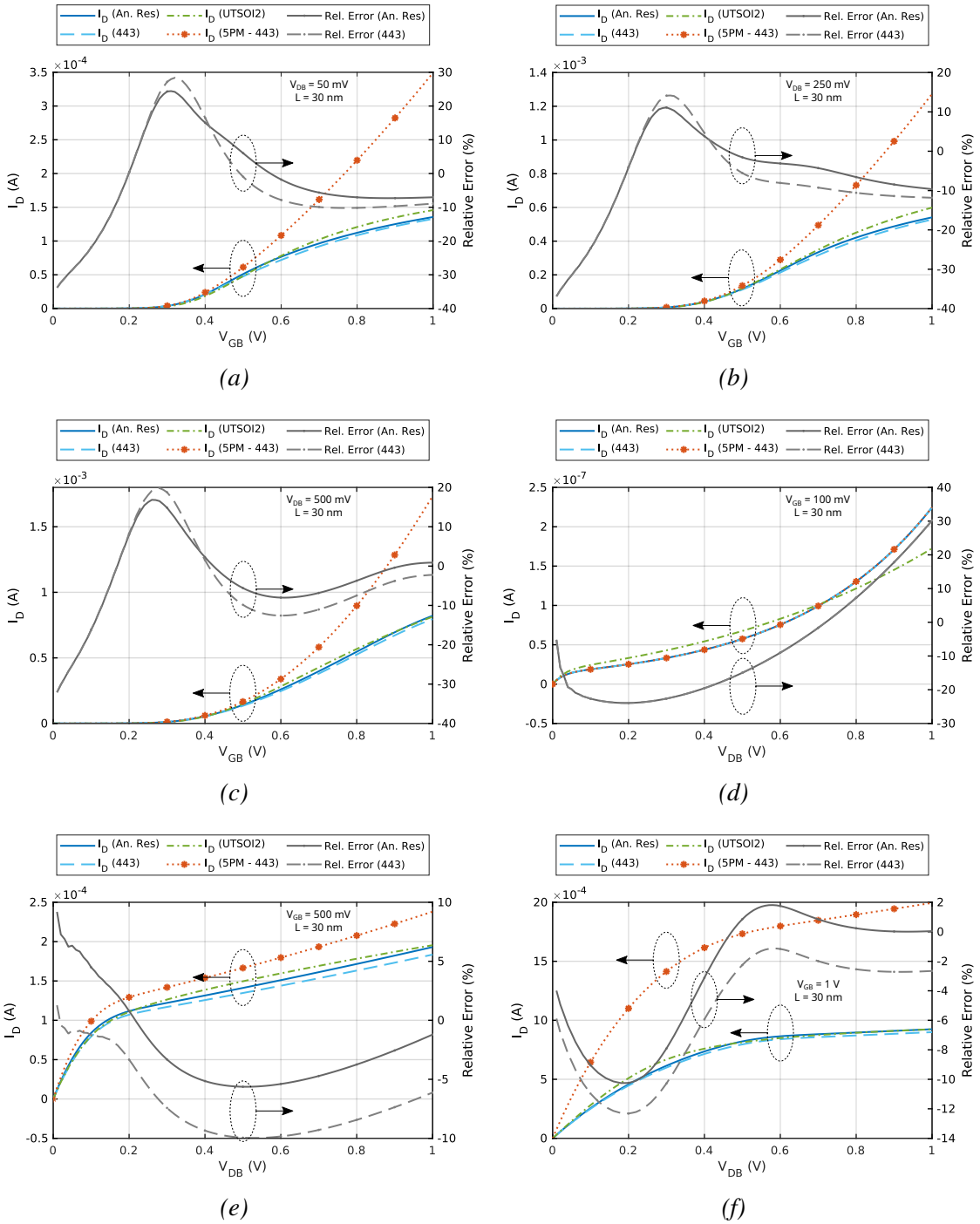


Figure 3.5: Comparison with simulation: I_D-V_{GB} (V_D = 50 mV (a), V_D = 250 mV (b), and V_D = 500 mV (c)) and I_D-V_{DB} (V_G = 100 mV (d), V_G = 500 mV (e), and V_G = 1 V (f)) curves of 28nm FD-SOI CMOS NMOS transitor with L = 30 nm and W = 1 µm.

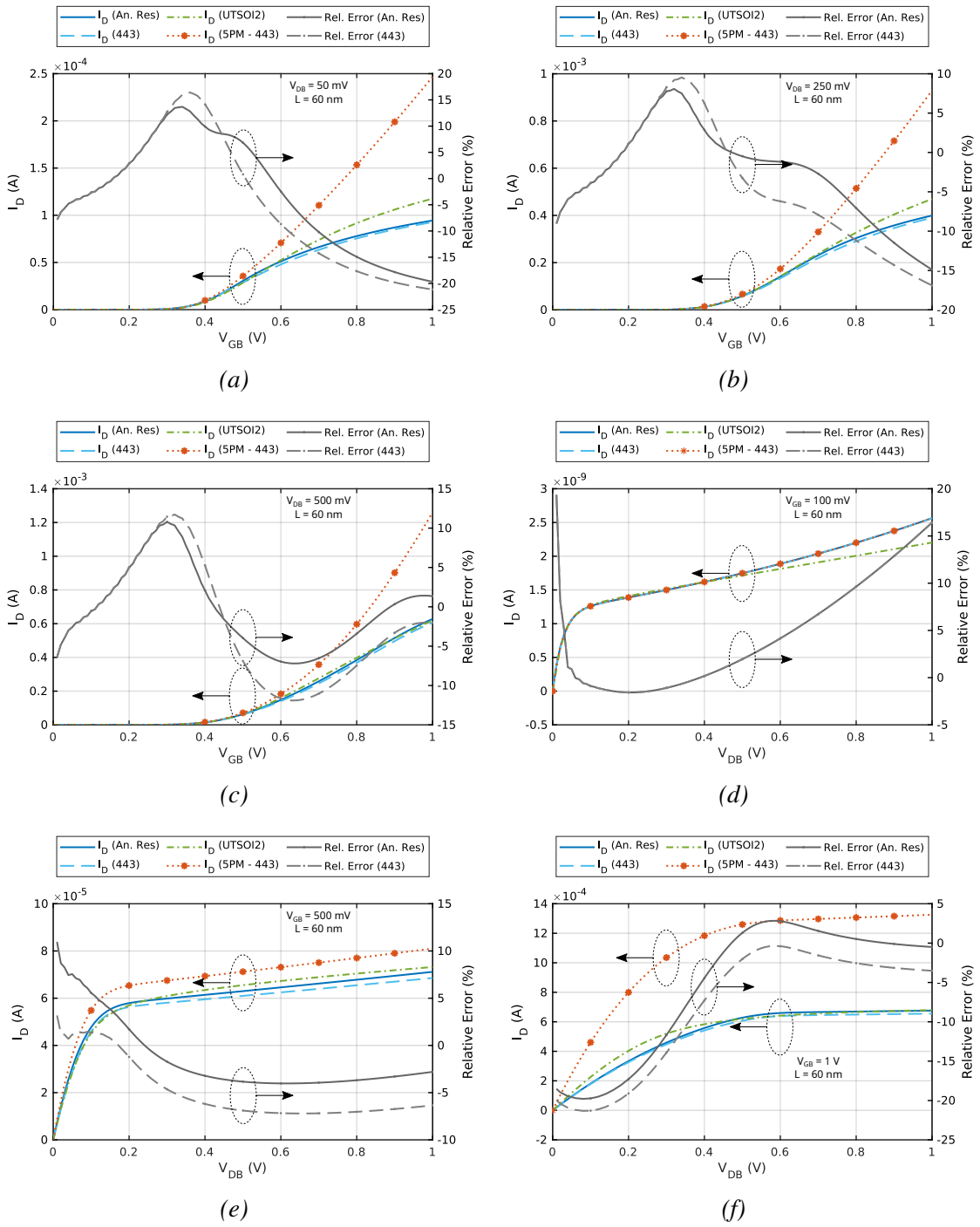


Figure 3.6: Comparison with simulation: I_D-V_{GB} (V_D = 50 mV (a), V_D = 250 mV (b), and V_D = 500 mV (c)) and I_D-V_{DB} (V_G = 100 mV (d), V_G = 500 mV (e), and V_G = 1 V (f)) curves of 28nm FD-SOI CMOS NMOS transitor with L = 60 nm and W = 1 µm.

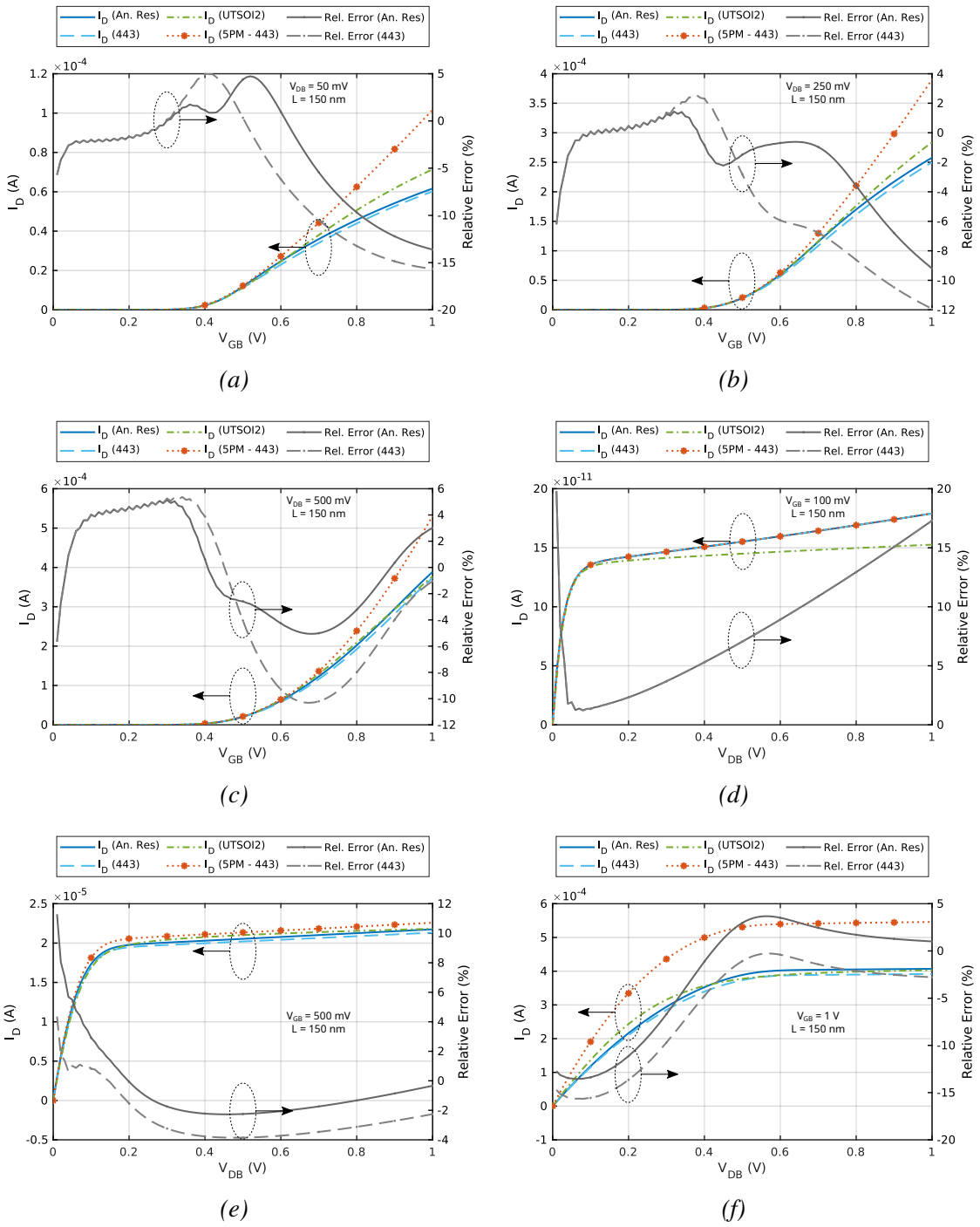


Figure 3.7: Comparison with simulation: I_D-V_{GB} (V_D = 50 mV (a), V_D = 250 mV (b), and V_D = 500 mV (c)) and I_D-V_{DB} (V_G = 100 mV (d), V_G = 500 mV (e), and V_G = 1 V (f)) curves of 28nm FD-SOI CMOS NMOS transitor with L = 150 nm and W = 1 µm.

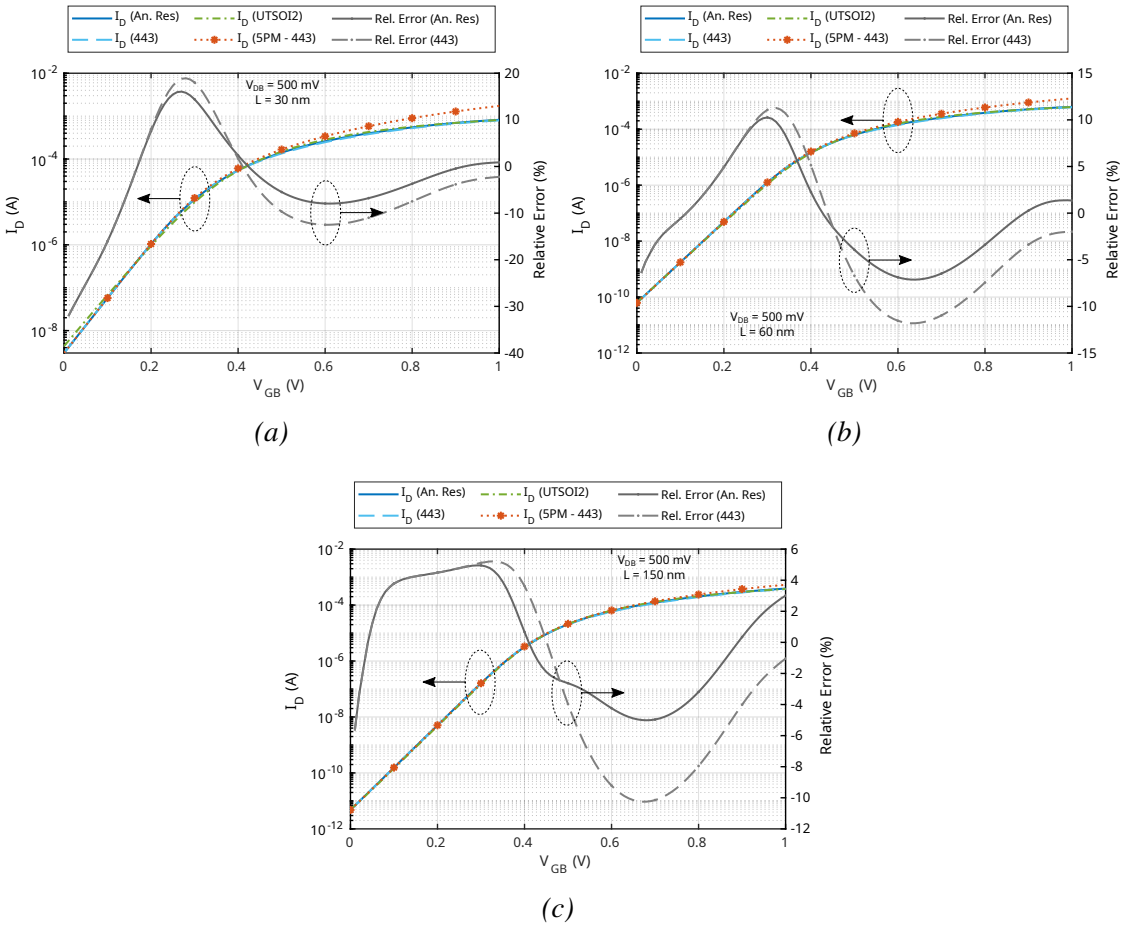


Figure 3.8: Comparison with simulation: I_D-V_{GB} (V_D = 500 mV) curves of 28nm FD-SOI CMOS NMOS transitor with L = 30 nm (a), 60 nm (b), and 150 nm (c) and W = 1 µm in semilog scale.

The proposed model is considered design-oriented due to its simplicity and its precision in characterizing the behavior of the transistors. In this regard, designers often employ specific transistor metrics –other than the drain current– to correlate their circuit specifications with the transistors' capabilities. Analog designers typically utilize the transistor's transconductance g_m, which is closely associated with analog specifications such as the gain of an amplifier. In contrast, digital designers frequently consider the I_{on}/I_{off} ratio as a significant metric to evaluate the energy efficiency of a technology, where I_{on} and I_{off} are defined as,

$$I_{on} = I_D|_{V_{GS}=V_{DS}=V_{DD}}, \tag{3.49}$$

$$I_{off} = I_D|_{V_{GS}=0V,V_{DS}=V_{DD}}. \tag{3.50}$$

Thus, Figure 3.9 shows a direct comparison between the proposed explicit expression

for the transistor's transconductance g_m and the transconductance evaluated from the L-UTSOI model. In order to highlight the contribution of the mobility reduction parameter θ to g_m, we have plotted the complete analytical expression (3.41), and the same expression neglecting the mobility reduction contribution by making $\theta = 0$. As it can be seen, the complete 6PM analytical expression follows closely the L-UTSOI model. On the other hand, neglecting the mobility reduction effect leads to an overestimation of g_m for moderate and strong values of V_{GS}.

Finally, Figure 3.10 presents a comparative analysis of the I_{on}/I_{off} ratio. The ratio obtained using the proposed explicit expression for the drain current I_D is compared against the results derived from the L-UTSOI model. To better highlight the impact of mobility reduction and the advantage of our proposed 6PM model, we have illustrated the obtained I_{on}/I_{off} ratio using both the complete analytical expression of I_D as per equation (3.36) and the same expression with $\theta = 0$, thereby omitting the mobility reduction effect. The findings are consistent with the transconductance analysis; the comprehensive 6PM analytical expression closely mirrors the L-UTSOI model. Conversely, once strong inversion is established, disregarding the mobility reduction effect results in an overestimation of the I_{on}/I_{off} ratio.

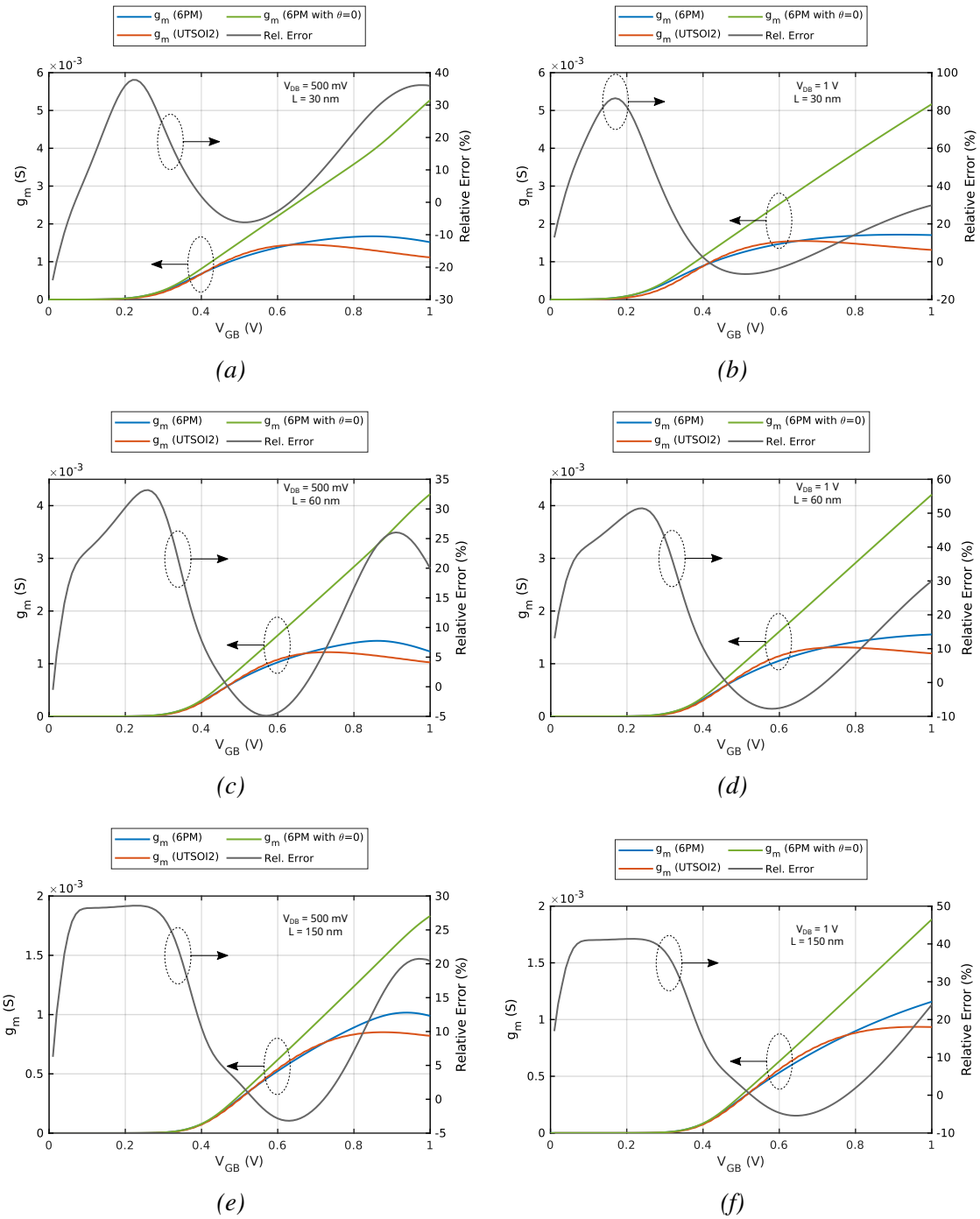


Figure 3.9: Comparison with simulation: g_m-V_{GB} for L = 30 nm (V_D = 500 mV (a), V_D = 1 V (b)), L = 60 nm (V_D = 500 mV (c), V_D = 1 V (d)), and L = 150 nm (V_D = 500 mV (e), V_D = 1 V (f)) curves of 28nm FD-SOI CMOS NMOS transistor with W = 1 µm.

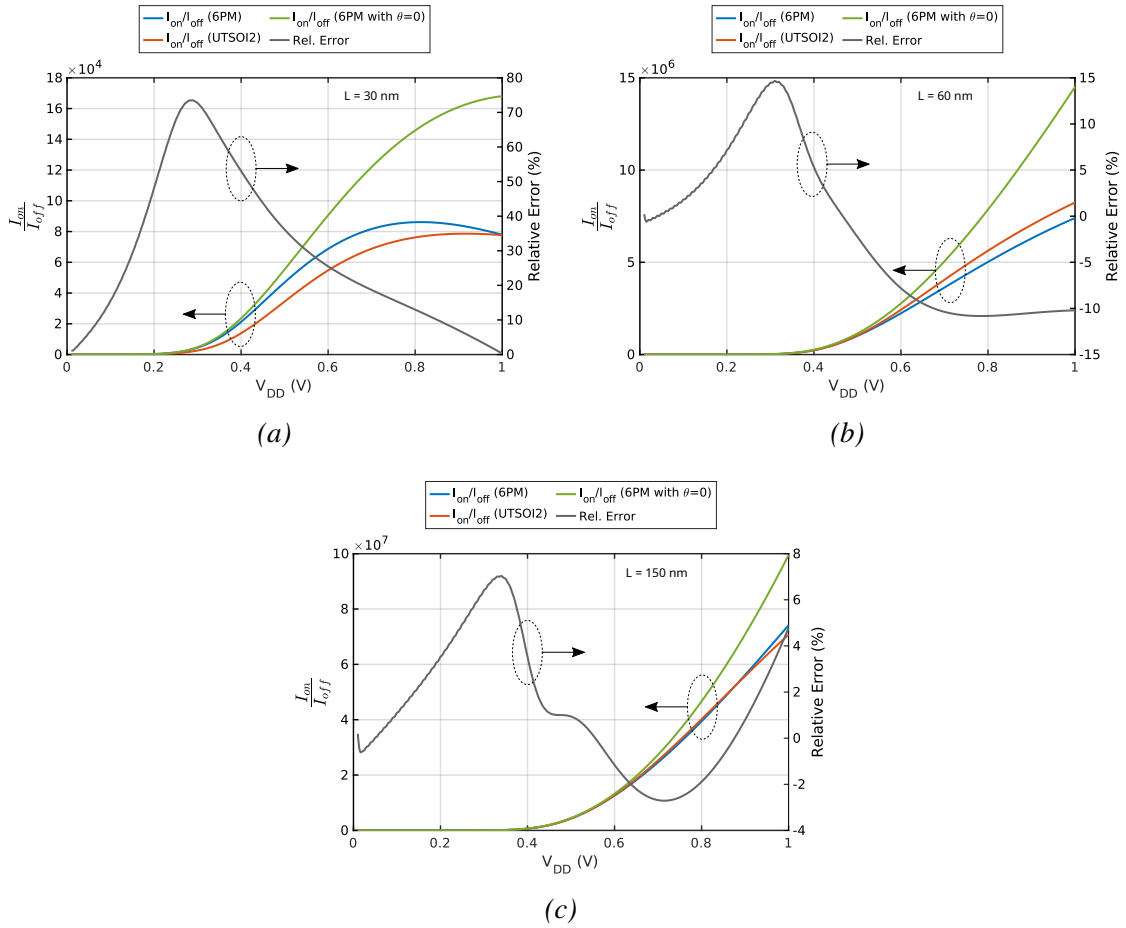


Figure 3.10: Comparison with simulation: I_{on}/I_{off}-V_{DD} for L = 30 nm (a), L = 60 nm (b), and L = 150 nm (c) curves of 28nm FD-SOI CMOS NMOS transistor with W = 1 µm.

In summary, Figures 3.5, 3.6, 3.7, 3.8, 3.9, and 3.10 highlight the key contributions of the proposed model. Firstly, they demonstrate the precision of the approximation, validating the implementation of the proposed model. Secondly, they underscore the necessity of introducing the mobility reduction factor θ, to enhance accuracy across all the operating regions and regimes of the transistor. Furthermore, it is noteworthy that the introduction of the mobility reduction factor θ mathematically introduces a new pole compared to the I_D expression of the 5PM ACM model presented in [23]. This theoretical addition accounts for the differences observed between the 5PM curves and those of the model presented here.

3.4.2 Measurements Results

Figures 3.11 and 3.12 show a comparison between the proposed closed-form 6PM design-oriented model and experimental characterization measurements for a set of fabricated NMOS transistors in STMicroelectronics 28nm FD-SOI CMOS technology.
Figure 3.11 shows the obtained I_D-V_{GB} curves for $V_{DS} = 500\,\text{mV}$ and I_D-V_{DB} curves for

$V_{GS} = 500\,\text{mV}$, for the three considered transistor's lengths, $L = 30\,\text{nm}$, $L = 60\,\text{nm}$ and $L = 150\,\text{nm}$. As can be seen, the proposed analytical model approximates closely the measured behavior of the transistor.

Finally, Figure 3.12 shows a comparison between the analytical expression for the transistor's transconductance g_m, and the transconductance evaluated from the transistor's characterization measurements. Again, it is clear to see that the proposed closed-form expression follows the behavior observed in the experimental measurements.

The various measurement results corroborate the conclusions drawn from the simulation results: the necessity of introducing of the mobility reduction factor θ, and the precision of the new approximation leading to the novel implementation of the proposed model. The close agreement between the measurement data and our proposed model, both qualitatively and quantitatively, reinforces the notion that the proposed model could be a highly useful tool for preliminary design. It could serve both analog and digital designers and offers a valuable asset for easily characterizing new technologies through simple DC measurements on individual transistors.

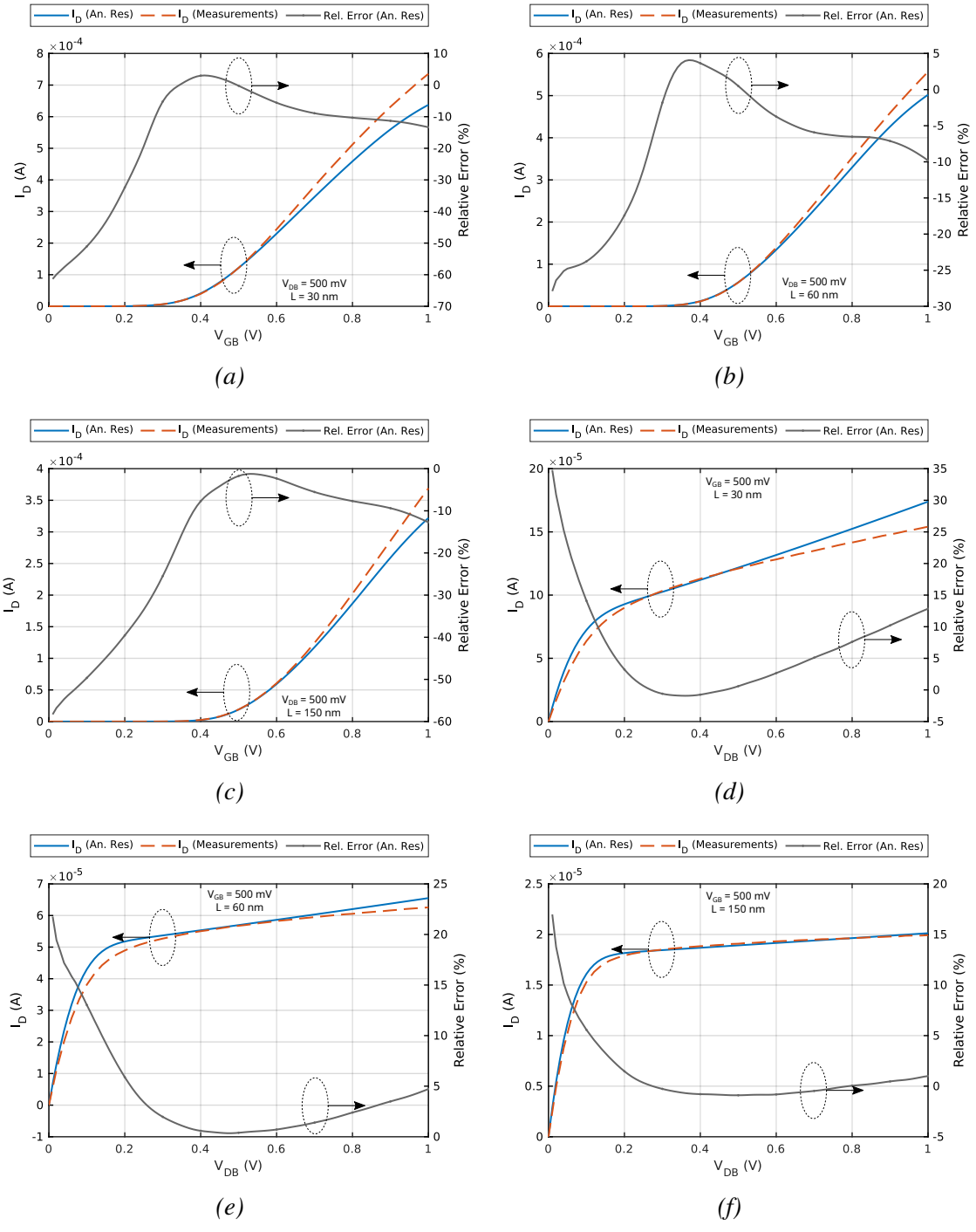


Figure 3.11: Comparison with measurements: I_D-V_{GB} at V_D = 500 mV (L = 30 nm (a), L = 60 nm (b), and L = 150 nm (c)) and I_D-V_{DB} at V_G = 500 mV (L = 30 nm (d), L = 60 nm (e), and L = 150 nm (f)) curves of 28nm FD-SOI CMOS NMOS transistor with W = 1 µm.

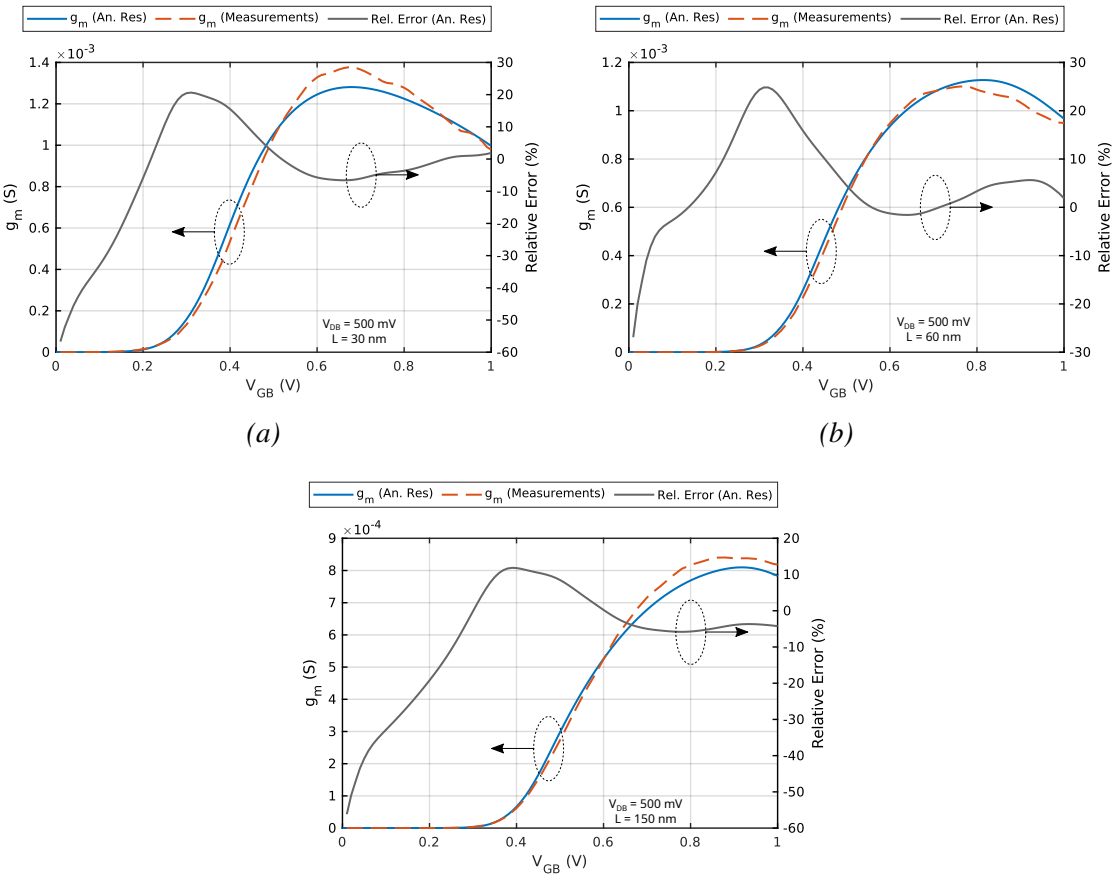


Figure 3.12: Comparison with measurements: g_m-V_{GB} for L = 30 nm (V_D = 500 mV (a)), L = 60 nm (V_D = 500 mV (b)), and L = 150 nm (V_D = 500 mV (c)) curves of 28nm FD-SOI CMOS NMOS transistor with W = 1 µm.

3.4.3 Comparison to Others Charge-Based Models

Table 3.3: Comparison between different versions of the ACM model and the industry-standard L-UTSOI model.

Features	*L-UTSOI* [59]	This work	ACM 4PM [51]	ACM 7PM [24]	ACM 5PM [23]
Natural transition from triode to saturation regions and weak to strong inversion zones	*No*	Yes	Yes	Yes	Yes
$q_i - V_{ij}$ explicit link	*Not applicable*	Yes	No	No	No
Number of DC parameters	*tens of*	6	4	7	5
Body-biasing consideration	*Yes*	No	No	No	Yes
I_D error [%] (*)	*close to zero*	5.94	32.73	4.46	12.81
Short-Channel Effects					
Velocity Saturation	*Yes*	Yes	No	Yes	Yes
DIBL	*Yes*	Yes	Yes	Yes	Yes
Mobility Reduction	*Yes*	Yes	No	Yes	No
CLM	*Yes*	No	No	Yes	No

(*) The main drain current error is calculated from $I_D - V_{GB}$ curves, in the saturation region, using the following formula: $I_{D,error} = \frac{1}{N}\sum_1^N |\frac{I_{D,model} - I_{D,meas}}{I_{D,meas}}|$, where N is the number of data points.

In the view of the obtained simulation and measurement results, we observe a compelling alignment between the behavior of the proposed 6PM model and the industry-standard L-UTSOI model. Moreover, this alignment is observed for both the numerically computed model using the 443 algorithm and for the proposed analytical approximation that offers, for the first time, a single-piece explicit $I - V$ equation for the transistor DC behavior valid for all inversion regions and operation regimes.

Concerning possible future applications of the proposed model, the primary objective is not to replace the comprehensive L-UTSOI model provided in the technology PDKs, but to provide a streamlined alternative that can be especially beneficial during the initial stages of technology development and circuit design. For instance, in the context of a PDK that is still under development, our model offers a rapid and efficient means to characterize the technology, which can be particularly advantageous. Furthermore, the model's simplicity and analytical nature allow for swift exploration of the design space,

which is crucial during preliminary design efforts.

When considering the implementation of short-channel effects, the ACM 6PM model introduced in this work proposes a good trade-off between simplicity and precision. While the ACM 7PM model incorporates a more complex approach to account for channel length modulation (CLM) in addition to DIBL and velocity saturation, our ACM 6PM model achieves a similar level of accuracy with less complexity. In this regard, the model dependency in V_D is controlled by the balance of two model parameters (i.e., σ and ζ, related to DIBL and velocity saturation, respectively). It has to be noted that the shorter the channel length, the stronger the short-channel effects are expected to be. The working principles of the model do not present a structural limitation on the scaling of the device. However, a decrease in precision could be anticipated if non-considered short-channel effects become significant for deeply scaled transistors.

In order to put our results into perspective, Table 3.3 offers a direct comparison between the proposed 6PM model and previous design-oriented MOSFET models presented in the literature. Table 3.3 presents a summary of the advantages and trade-offs associated with each model. By presenting a direct comparison with various ACM model versions and the L-UTSOI model, we aim to highlight the practical utility and analytical strengths of the proposed 6PM model in the broader context of transistor modeling. As it can be seen, the proposed 6PM model offers a fair trade-off between model complexity and precision.

3.5 Conclusion

This chapter has presented a novel and explicit charge-based MOSFET model tailored for advanced nanometric CMOS technologies, specifically targeting the 28nm FD-SOI CMOS node. By leveraging an analytical approximation of the Lambert W-function, the proposed six-parameter model (6PM) overcomes the limitations of previous implicit formulations that relied on numerical solvers, thus enabling a continuous, single-piece, and closed-form expression for the transistor drain current valid across all inversion and operating regions.

The inclusion of key short-channel effects—such as drain-induced barrier lowering (DIBL), velocity saturation, and mobility reduction—within a compact parameter set ensures improved accuracy while maintaining model simplicity. Extensive validation against industry-standard L-UTSOI compact models and experimental measurements demonstrates that the 6PM model achieves excellent agreement in both DC characteristics and small-signal parameters such as transconductance, as well as important digital metrics like the on/off current ratio.

Importantly, the analytical nature of the model facilitates intuitive understanding and rapid exploration of transistor behavior, supporting efficient preliminary design and technology characterization. This capability is critical for designers working on ultra-low power and ultra-low voltage circuits, where accurate modeling of transistor physics across all regimes is essential.

Overall, the proposed 6PM charge-based model enables a fair compromise between complexity and precision, offering a valuable tool for both analog and digital circuit designers. It lays a solid foundation for subsequent transient and noise analyses, enabling comprehensive and physically grounded design methodologies for inverter-based circuits and oscillators in advanced CMOS technologies.

Future work will focus on extending the model to incorporate additional effects such as channel length modulation and variability, as well as integrating it within automated design flows to further accelerate technology development and circuit optimization.

4

Innovative Design Approaches for Voltage-Controlled Oscillators Based on Charge-Based Models

This fourth chapter presents a transient-based analysis approach for inverter-based circuits leveraging the charge-based model introduced in the previous chapter. The methodology is demonstrated on a single-ended ring oscillator implemented in 28nm FD-SOI CMOS technology, with simulation results compared against those obtained using the industry-standard UTSOI2 model.

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4.1 Introduction

Voltage-controlled oscillators (VCOs) are fundamental building blocks in a wide range of analog/RF and mixed-signal systems, including frequency synthesizers, phase-locked loops, and communication transceivers. As CMOS technology scales into advanced nodes such as 28nm FD-SOI CMOS, the design of VCOs faces increasing challenges due to complex device physics, short-channel effects, and stringent power and performance requirements.

Traditional compact models used for circuit simulation often involve large parameter sets and computationally intensive simulations, which can hinder rapid design space exploration and intuitive understanding of circuit-device-technology interactions. Charge-based MOSFET models, characterized by a reduced number of physically meaningful parameters and continuous behavior across all inversion and operating regions, offer a promising alternative for efficient and accurate large-signal circuit analysis, especially for design space exploration and preliminary sizing.

This chapter presents innovative transient analysis methodologies leveraging the charge-based MOSFET model presented in Chapter 3 to enable detailed time-domain characterization of inverter-based ring oscillators. The approach facilitates simultaneous evaluation of frequency, power, and noise performance metrics, providing designers with a powerful tool for preliminary sizing and optimization. Furthermore, the integration of polynomial L-based scaling laws for device parameters significantly accelerates design space exploration, making the methodology practical for advanced CMOS technologies. Indeed, charge-based models are often employed through extensive look-up tables (LUTs) containing extracted parameters used for design optimization in preliminary phases. However, generating and maintaining these LUTs is computationally intensive, as it depends both on the degree of automation in parameter extraction [60] and on the complexity of the extraction methodology itself. This process becomes particularly inefficient when LUTs must be regenerated for each update of a design kit in a given technology. Therefore, the development of *L*-based analytical scaling laws—requiring only a limited number of extraction points and easily updatable—represents an appealing alternative for compact and efficient model calibration.

The chapter is organized as follows: Section 4.2 develops the transient analysis framework for CMOS inverters, including intrinsic capacitance modeling. Section 4.3 applies this framework to inverter-based ring oscillators, analyzing frequency and power consumption and discussing noise perspectives. Section 4.4 introduces the use of scaling laws for efficient parameter extraction and compares the approach with conventional design methods. Finally, conclusions and perspectives are drawn in Section 4.5.

4.2 Transient Analysis Method for CMOS Inverter

The objective of this section is to develop a transient analysis methodology for CMOS inverters based on the reduced-parameter charge-based MOSFET model introduced in the previous chapter. By leveraging the model's ability to accurately describe transistor behavior across all inversion and operating regions with a minimal parameter set, this approach enables detailed time-domain evaluation of inverter switching dynamics. This transient-like analysis forms the foundation for subsequent frequency and noise characterization of inverter-based circuits, providing designers with an intuitive and computationally efficient tool for large-signal circuit exploration.

4.2.1 Mathematical Framework

To enable large-signal circuit analysis using charge-based models, we first focus on the transient analysis of a CMOS inverter, as illustrated in Figure 4.1. Existing methods, such as those presented in [61, 62, 63], primarily aim at determining the inverter propagation delay without fully capturing its temporal behavior. While these methods are effective for delay estimation, they limit the ability to perform detailed noise and harmonic analyses in inverter-based circuits.

The approach proposed here is based on a transient-like analysis of the CMOS inverter, which allows for simultaneous evaluation of both frequency and noise characteristics in circuits composed of inverters. Specifically, the method focuses on analyzing a single switching transition of the inverter between its two stable output states. The overall methodology relies on discretizing time and applying the Euler numerical integration method to solve the transient behavior. The propagation time τ for the output voltage

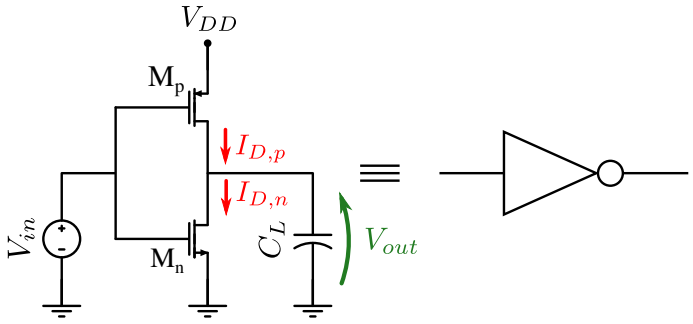


Figure 4.1: CMOS inverter schematic.

to transition from level V_A to V_B during a single switching event is defined by the integral:

$$\tau = \int_{V_A}^{V_B} \frac{C_L}{I_L} dV_{out}, \tag{4.1}$$

where the load current I_L is given by:

$$I_L = I_{D,p} - I_{D,n}. \tag{4.2}$$

As illustrated in Figure 4.1, C_L is the load capacitance at the inverter output node, $I_{D,p}$ and $I_{D,n}$ are the drain currents of the PMOS and NMOS transistors, respectively, and V_{out} is the voltage across C_L.
To evaluate the transient evolution of the drain current, the total transition time is divided into sufficiently small time steps. Within each time step, the current flowing through the load capacitance is approximated using a first-order Taylor expansion. This discretization and approximation enable the numerical integration of the transient response using the Euler method as presented in Figure 4.2.

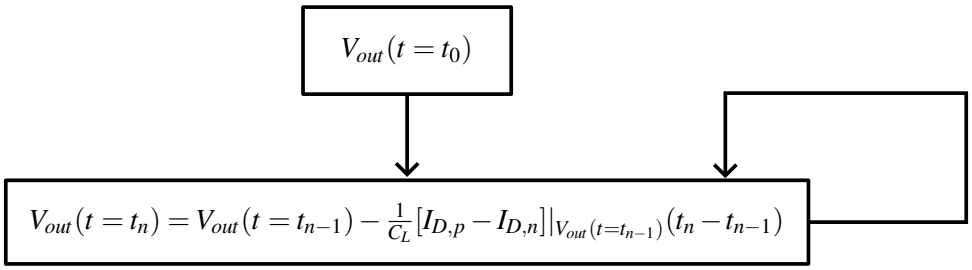


Figure 4.2: Flowchart of the considered Euler method.

4.2.2 Modeling of Intrinsic Capacitances

Accurate modeling of intrinsic capacitances is essential for the transient and frequency analysis of large-signal circuits such as inverter-based ring oscillators. These capacitances, which arise from charge storage within the MOSFET channel and junctions, strongly depend on both the transistor geometry and its biasing conditions. Therefore, their precise modeling is crucial to capture the circuit dynamics accurately. In this subsection, a detailed description of MOSFET intrinsic capacitances consistent with the charge-based model framework introduced in the previous chapter is provided, focusing on their analytical formulation.
In the context of inverter-based voltage-controlled ring oscillators, this work considers two main intrinsic capacitances: the gate-to-bulk intrinsic capacitance of the PMOS and the NMOS transistors, denoted as $C_{GB,p}$ and $C_{GB,n}$ respectively, and the drain-to-bulk intrinsic capacitance of the PMOS and NMOS transistors, denoted as $C_{DB,p}$ and $C_{DB,n}$ respectively. These intrinsic capacitances depend of the terminal voltages as well as the transistor geometry, and are described using the equations proposed in [64].
Following this approach, the intrinsic gate-to-drain capacitance for the PMOS (respec-

tively NMOS) transistor is expressed as:

$$C_{GD,p(n)} = \left(1 - \frac{\sigma_{p(n)}}{n_{p(n)}}\right) C_{GD0,p(n)} - \frac{\sigma_{p(n)}}{n_{p(n)}} C_{GS0,p(n)}, \tag{4.3}$$

where $n_{p(n)}$ is the subthreshold slope factor and $\sigma_{p(n)}$ the DIBL effect factor.
The intrinsic capacitances $C_{GD0,p(n)}$ and $C_{GS0,p(n)}$ are given by:

$$C_{GD0,p(n)} = \frac{2}{3} C_{ox,p(n)} \alpha_{p(n)}^2 \left(1 + \alpha_{p(n)}\right)^2 \frac{q_{D,p(n)}}{1 + q_{D,p(n)}}, \tag{4.4}$$

$$C_{GS0,p(n)} = \frac{2}{3} C_{ox,p(n)} \left(1 + 2\alpha_{p(n)}\right) \left(1 + \alpha_{p(n)}\right)^2 \frac{q_{S,p(n)}}{1 + q_{S,p(n)}}, \tag{4.5}$$

with

$$\alpha_{p(n)} = \frac{1 + q_{D,p(n)}}{1 + q_{S,p(n)}}. \tag{4.6}$$

Here, $C_{ox,p(n)} = C'_{ox,p(n)} \cdot W_{p(n)} \cdot L$ is the oxide capacitance of the transistor, where $C'_{ox,p(n)}$ is the oxide capacitance per unit area, and $W_{p(n)}$, L are the device width and length, respectively.
The drain-to-bulk capacitance is related to the gate-to-drain capacitance by:

$$C_{DB,p(n)} = \left(n_{p(n)} - 1\right) C_{GD,p(n)}. \tag{4.7}$$

4.2.3 Inverter Propagation Times in Ring Oscillator Architecture

Leveraging the transient-like approach combined with the charge-based model's capability to accurately describe the behavior of CMOS inverter transistors across all inversion and operating regions, this subsection aims to precisely determine the rising and falling propagation times of a classical CMOS inverter. The inverter under study is part of a single-ended ring oscillator (SERO) architecture composed of N inverters, where N is an odd number, as illustrated in Figure 4.3.

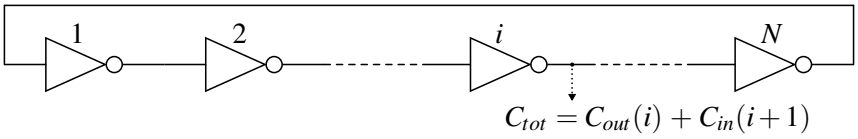


Figure 4.3: Single-ended ring oscillator architecture composed of N inverters.

To accurately determine the inverter propagation times, it is essential to consider the parasitic capacitances of each transistor. Applying Miller's theorem and following the analysis

in [61], the equivalent load capacitance seen at each inverter output stage is expressed as:

$$C_{tot} = 4 \cdot (C_{GD,p} + C_{GD,n}) + C_{DB,p} + C_{DB,n} + C_{ext}, \tag{4.8}$$

where $C_{GD,p}$ and $C_{GD,n}$ represent the intrinsic gate-to-drain capacitances of the PMOS and NMOS transistors, respectively, and $C_{DB,p}$ and $C_{DB,n}$ denote their respective intrinsic drain-to-bulk capacitances, as described in the previous subsection. These intrinsic capacitances depend on both the terminal voltages and the transistor geometry and must be recalculated dynamically for each voltage change during the transient analysis. In contrast, C_{ext} accounts for extrinsic capacitances, which are largely voltage-independent but depend on device geometry. To model C_{ext}, numerical $W \cdot L$-based scaling laws have been extracted from the UTSOI2 compact model.

The rising time (t_r) and falling time (t_f) are defined as the durations for the output voltage to transition between 10% and 90% of the supply voltage V_{DD}. Although the nominal supply voltage of the 28nm FD-SOI CMOS technology is 1 V, the analysis is performed at $V_{DD} = 0.75\,V$ to reflect typical operating conditions in ultra-low voltage (ULV) and ultra-low power (ULP) designs. Operating below nominal voltage enables significant power savings and is common in energy-constrained applications, making 0.75 V a practical and relevant choice for inverter characterization.

To achieve minimal and balanced rising and falling times, we refer to the study conducted on 28nm FD-SOI CMOS technology in [27], where the NMOS transistor width is fixed at $W_n = 0.35\,\mu$m. For this supply voltage, the ratio t_r/t_f is plotted in Figure 4.4 as a function of the transistor length L and the width ratio $k = W_p/W_n$. The figure shows that the equilibrium point where t_r equals t_f varies with L and occurs at different values of k. Figure 4.4 demonstrates that charge-based model, when applied to this analysis, enables efficient exploration of a wide design space using a reduced set of parameters. Furthermore, this study can be extended to different supply voltages and MOS widths, providing designers with a practical tool to achieve balanced rising and falling times in inverter-based circuits and thereby simplify the pre-sizing phase of the design process.

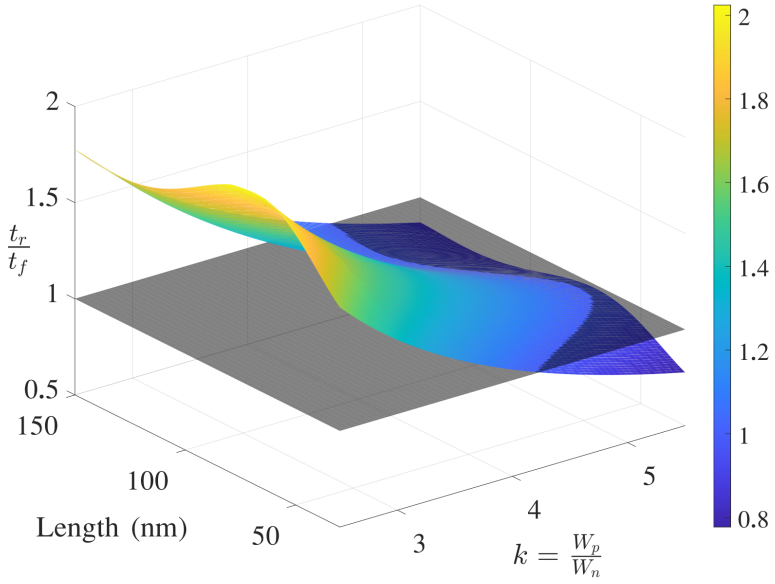


Figure 4.4: Ratio of rising to falling times (t_r/t_f) as a function of transistor length $L \in [30\,\text{nm}, 150\,\text{nm}]$ and width ratio $k = W_p/W_n \in [2.5, 5.5]$ in 28nm FD-SOI CMOS technology, with fixed $W_n = 0.35\,\mu m$ and $V_{DD} = 0.75\,V$.

4.3 Application to Inverter-Based Ring Oscillator Design

Building upon the transient analysis methodology and intrinsic device modeling developed in the previous sections, this section applies the proposed charge-based framework to the comprehensive study of inverter-based ring oscillators. By leveraging the accurate characterization of inverter propagation delays and intrinsic capacitances, we analyze key performance metrics such as oscillation frequency and power consumption. The results are validated against industry-standard compact models, demonstrating the efficiency of the proposed approach for practical oscillator design and optimization.

4.3.1 Frequency Analysis

To evaluate the accuracy of the proposed transient analysis, a single-ended ring oscillator (SERO) composed of $N = 5$ CMOS inverters was simulated using both the ACM charge-based model and the UTSOI2 compact model. Three different transistor lengths (60 nm, 90 nm, and 120 nm) were considered over a supply voltage range from $V_{DD} = 0.6\,\mathrm{V}$ to 0.9 V. The oscillator frequency predicted by each model was compared, and the results are shown in Figure 4.5.
The oscillation frequency is defined as:

$$f = \frac{1}{N \cdot (t_r + t_f)}, \tag{4.9}$$

where N is the number of inverters in the ring, and t_r and t_f are the rising and falling propagation times of a single inverter, respectively, as defined in the previous subsection. Figure 4.5 demonstrates that the dynamic analysis conducted using the proposed ACM charge-based model achieves a high level of accuracy when compared to circuit simulations based on the UTSOI2 model. The slight loss of precision observed at higher supply voltages in predicting the maximum achievable frequency is likely attributable to the underestimation of mobility reduction effects or other second-order phenomena not explicitly accounted for in the current model. Nonetheless, the accuracy attained, combined with the model's reduced parameter set describing a single transistor—and consequently a CMOS inverter—makes this approach a compelling alternative for the preliminary sizing and design space exploration of inverter-based circuits such as ring oscillators.

4.3.2 Power Consumption Analysis

In addition to frequency, the transient simulation approach enables the analysis of power consumption. Using the same set of transistor lengths (60 nm, 90 nm, and 120 nm) and supply voltage range (0.6 V to 0.9 V), the dynamic efficiency of the single-ended ring oscillator was evaluated. The results are presented in Figure 4.6.

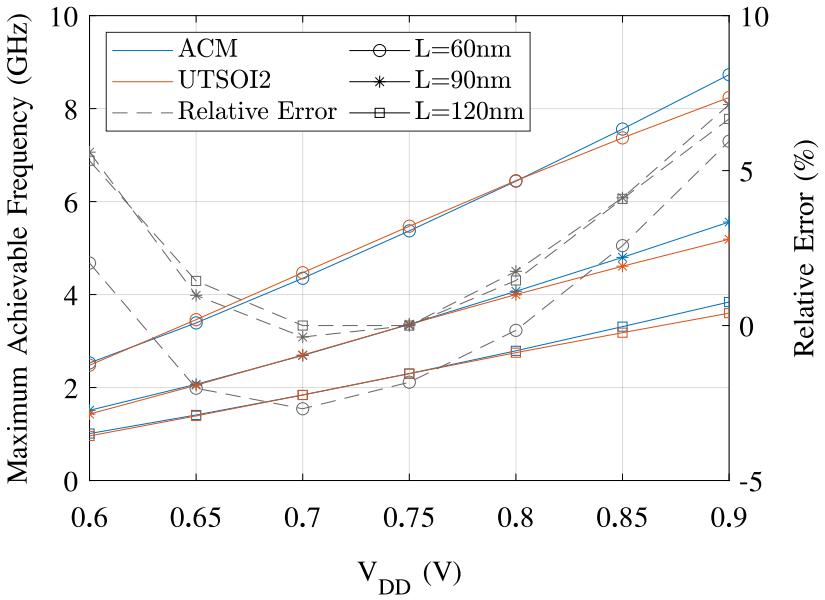


Figure 4.5: Comparison of maximum achievable frequency predicted by the ACM and UTSOI2 models for a 5-stage SERO with transistor lengths $L_p = L_n = 60\,\text{nm}$, 90 nm, and 120 nm, NMOS width $W_n = 0.35\,\mu\text{m}$, and PMOS widths $W_p = 1.18\,\mu\text{m}$, $1.31\,\mu\text{m}$, and $1.38\,\mu\text{m}$ in 28nm FD-SOI CMOS technology.

The dynamic efficiency η_{dyn} is defined as:

$$\eta_{dyn} = \frac{f_{osc}}{P_{dyn}}, \tag{4.10}$$

where f_{osc} is the oscillation frequency computed as above, and P_{dyn} is the associated dynamic power consumption. Figure 4.6 further confirms the observations and conclusions presented earlier. The reduced dynamic power consumption at lower supply voltages primarily reflects the model's focus on capacitive switching power, as short-circuit power is not explicitly accounted for. Nevertheless, these results demonstrate that the proposed analysis offers a reliable and efficient first-order tool for the preliminary design and optimization of inverter-based large-signal circuits, including ring oscillators.

4.3.3 Perspective on Noise Analysis

4.3.3.1 Impulse Sensitivity Function Theory

While transient-like approaches, such as the one developed in this work, are inherently more complex than simpler methods like effective current analysis [62], they provide a natural and rigorous framework for noise analysis through the Impulse Sensitivity Function (ISF) theory introduced by Hajimiri and Lee [25].
The ISF quantifies how sensitive an oscillator's phase is to small and instantaneous pertur-

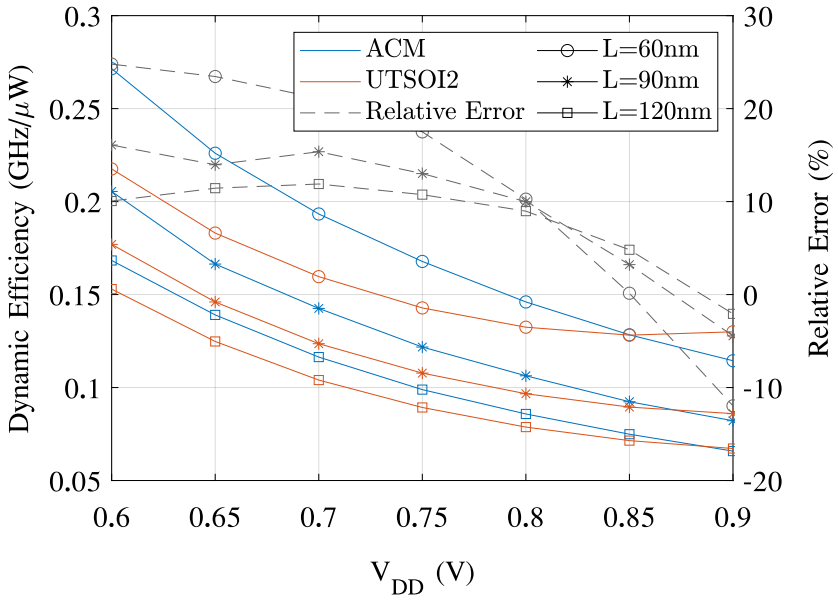


Figure 4.6: Comparison of dynamic efficiency predicted by the ACM and UTSOI2 models for a 5-stage SERO with transistor lengths $L_p = L_n = 60\,\text{nm}$, 90 nm, and 120 nm, NMOS width $W_n = 0.35\,\mu\text{m}$, and PMOS widths $W_p = 1.18\,\mu\text{m}$, $1.31\,\mu\text{m}$, and $1.38\,\mu\text{m}$ in 28nm FD-SOI CMOS technology.

bations (impulses) applied at different points in its oscillation cycle. For sufficiently small impulses—comparable in energy to typical noise fluctuations—the oscillator's response can be approximated as linear, allowing the computation of a time-varying, dimensionless function $\Gamma(\theta)$, where $\theta = \omega_0 \tau$ represents the phase within the oscillation period. Mathematically, the ISF relates the phase shift $\Delta\phi$ induced by a voltage impulse ΔV at a given node to the normalized impulse magnitude via:

$$\Delta\phi = \Gamma(\omega_0 \tau) \frac{\Delta V}{V_{max}}, \tag{4.11}$$

where $\omega_0 = 2\pi f_0$ is the angular frequency of the oscillator, and V_{max} is the peak voltage swing at the node.

4.3.3.2 Practical Use and Benefits

In the context of this work, the ISF provides a direct means to evaluate how noise injected at different nodes and phases of the ring oscillator affects its phase stability and spectral purity. By computing the ISF using the proposed transient-like charge-based model as presented in Figure 4.7, designers can:

- Identify the most noise-sensitive nodes and critical timing intervals within the oscillator cycle.

- Quantify the contribution of various noise sources to overall phase noise, enabling targeted noise mitigation strategies.

- Incorporate noise analysis early in the design flow, complementing frequency and power evaluations.

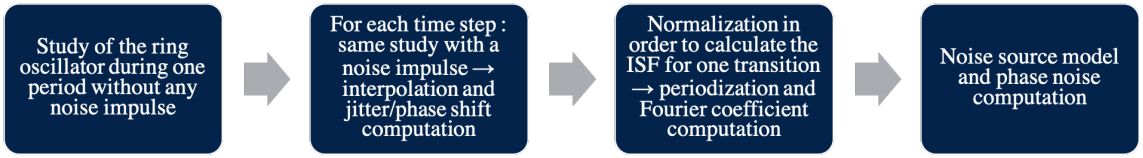


Figure 4.7: Flowchart presenting the computational steps involved in deriving the ISF and highlighting its role in quantitative phase-noise analysis of ring oscillators.

Using the ISF, valuable qualitative guidelines can be derived from the shape of the curve itself. For instance, the symmetry or asymmetry between the positive and negative lobes of the ISF—corresponding respectively to the rising and falling transitions of the oscillator waveform—provides direct insight into the balance of the inverter stages. Achieving a more symmetric ISF shape generally indicates balanced switching behavior, which is known to reduce phase noise by minimizing timing jitter contributions during transitions [25]. Therefore, designing inverters that produce similar waveform characteristics during both rising and falling edges can be guided effectively by analyzing the ISF, enabling improved oscillator spectral purity at the circuit level.
Figure 4.8 illustrates an example ISF computed at the node between two inverters in a single-ended ring oscillator, highlighting the time-dependent sensitivity profile obtained from our transient analysis.

4.3.3.3 Phase Noise Estimation

The ISF can be integrated with the power spectral densities of intrinsic noise sources to estimate the oscillator's phase noise spectrum, particularly in the $1/f^2$ region, through the relation:

$$\mathfrak{L}\{\Delta\omega\} = 10\log\left(\frac{\Gamma_{RMS}^2}{q_{max}^2}\cdot\frac{\bar{i_n^2}/\Delta f}{2\cdot\Delta\omega^2}\right), \tag{4.12}$$

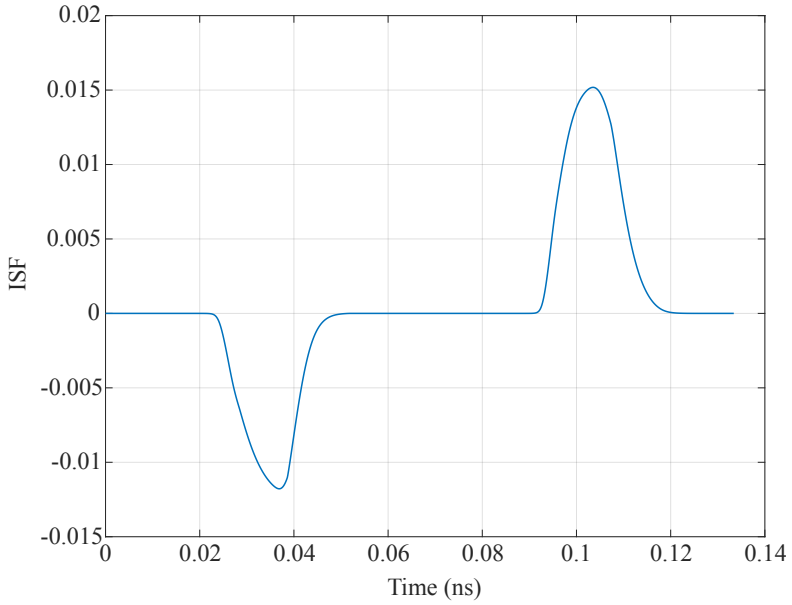


Figure 4.8: Impulse Sensitivity Function (ISF) computed at the node between two inverters in a single-ended ring oscillator using the proposed transient-like analysis.

where Γ_{RMS} is the root-mean-square value of the ISF over one period, $q_{max} = C_{node}V_{max}$ is the maximum charge swing at the node, $\bar{i_n^2}/\Delta f$ is the noise current power spectral density, and $\Delta\omega$ is the frequency offset from the carrier.

4.3.3.4 Outlook

By integrating the ISF-based noise analysis into the charge-based transient framework, this work lays the foundation for a comprehensive oscillator design methodology that simultaneously addresses frequency, power, and noise. Future developments will focus on incorporating detailed noise source models and validating phase noise predictions against measurements, ultimately enabling optimized ring oscillator and VCO designs within advanced CMOS technologies.

4.4 Practical Design Using Scaling Laws

To further enhance the efficiency and applicability of the charge-based transient analysis, this section introduces the use of polynomial scaling laws for device parameters. These scaling laws enable rapid and accurate estimation of transistor characteristics across varying geometries without resorting to exhaustive simulations or look-up tables. Integrating these scaling laws with the transient framework facilitates fast design space exploration and preliminary sizing of inverter-based circuits, providing a practical and scalable methodology that significantly reduces design cycle time.

4.4.1 Extraction of Scaling Laws

As introduced in Chapter 3, one of the key advantages of charge-based models is their reduced number of physically meaningful parameters. Despite this simplification, many design methodologies still rely on look-up tables (LUTs) for design space exploration. However, many existing design methodologies still rely on LUTs for design space exploration, which can be computationally intensive and require frequent recalibration as technology evolves.

To overcome these limitations, we developed numerical scaling laws based on transistor length (L) extracted from a limited set of device simulations. Our results show that polynomial scaling laws of up to third order ($X(L) = \alpha L^3 + \beta L^2 + \gamma L + \delta$) accurately capture the variation of key model parameters such as threshold voltage (V_{T0}), specific current (I_{S0}), sub-threshold slope factor (n) and all of the short-channel effect factors presented in Chapter 3 across the technology node. It is important to emphasize that these scaling laws were derived empirically and are purely numerical constructs; they do not stem from, nor do they reflect, any underlying physical mechanisms.

Nonetheless, these scaling laws enable designers to quickly predict transistor behavior for arbitrary geometries within the studied range, drastically reducing the computational burden and enabling rapid iteration during the early design stages.

Figure 4.9 illustrates the extraction of 13 data points (blue dots) for the equilibrium threshold voltage V_{T0} of a low-threshold voltage NMOS transistor in 28nm FD-SOI CMOS technology, along with its corresponding length-based polynomial scaling law (blue solid line). The use of polynomial scaling laws not only reduces the computational burden but also enhances the model's adaptability to technology variations without the need for exhaustive LUT extraction. This approach enables designers to rapidly evaluate the impact of device geometry on key parameters such as threshold voltage, mobility, and short-channel effects, thereby facilitating faster and more intuitive preliminary sizing and optimization of inverter-based circuits.

Furthermore, combining these scaling laws with the transient-like charge-based analy-

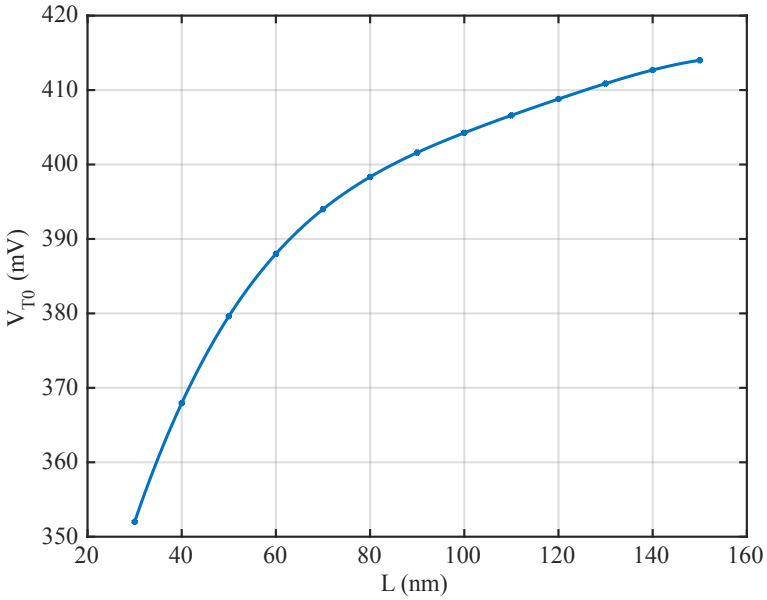


Figure 4.9: Extracted length-based scaling law for the equilibrium threshold voltage V_{T0} of 28nm FD-SOI CMOS LVT NMOS transistor.

sis framework presented earlier allows for a comprehensive yet efficient methodology to explore frequency, power, and noise trade-offs in inverter-based ring oscillators.

4.4.2 Comparison with Conventional Approaches

To concretely illustrate the advantages of the proposed scaling law methodology integrated with the charge-based transient analysis, Table 4.1 compares key performance and usability metrics across three common design approaches for a 5-stage ring oscillator implemented in 28nm FD-SOI CMOS technology: the classical simulation approach, LUT-based methods, and the proposed scaling law approach.

Table 4.1: Performance and usability comparison of design approaches for 5-stage ring oscillators in 28nm FD-SOI CMOS technology.

Metric	**Classical Simulation**	**LUT-based**	**Proposed Scaling Law**
Simulation Time	Seconds	Seconds	Seconds
Frequency Prediction Error	Nominal	<10%	<10%
Design Space Exploration	Time-consuming	Extensive	Easy and extensive
Parameter Updates	–	Time-consuming	Simple polynomial update

As shown, while all three methods achieve comparable frequency prediction accuracy—with the classical simulation approach providing nominal accuracy and both LUT-based and scaling law approaches maintaining errors below 10%—the proposed scaling law approach offers significant practical advantages.

In particular, the scaling law method drastically simplifies parameter updates through straightforward polynomial recalculations, in contrast to the time-consuming recalibration required by LUT-based approaches. This feature enhances adaptability to technology variations and accelerates iterative design cycles.

Moreover, the scaling law approach facilitates easy and extensive design space exploration by providing continuous parameter variation without the need for large LUT datasets or exhaustive device simulations. This contrasts with the classical simulation approach, which, despite its accuracy, is time-consuming and less suited for rapid exploration.

Traditional design techniques such as the g_m/I_D and C/I_D methods, while effective for small-signal circuits, are generally insufficient for comprehensive temporal and noise analysis of oscillators. They often focus on isolated performance metrics, limiting their ability to provide a unified and physically grounded description across all operating regions.

The charge-based model combined with polynomial scaling laws bridges this gap by delivering a compact, continuous, and physically meaningful representation of MOSFET behavior. This unified framework enables designers to efficiently analyze and optimize inverter-based ring oscillators with improved accuracy and reduced computational overhead compared to conventional methods.

In summary, the proposed scaling law methodology not only matches the accuracy of established approaches but also significantly enhances usability and design efficiency, making it a valuable tool for modern large-signal circuit design in advanced CMOS technologies.

4.5 Conclusion

This chapter has introduced a comprehensive and efficient approach for the analysis and design of inverter-based voltage-controlled oscillators using charge-based MOSFET models. By employing a reduced-parameter transient analysis framework, it enables accurate modeling of inverter switching dynamics, intrinsic capacitances, and their impact on ring oscillator performance.

Validated against industry-standard compact models in 28nm FD-SOI CMOS technology, the proposed methodology demonstrates high accuracy in predicting oscillation frequency and dynamic efficiency across a range of device geometries and supply voltages. The use of polynomial scaling laws further enhances the practicality of the approach by enabling rapid parameter extraction and facilitating extensive design space exploration without reliance on large look-up tables.

Additionally, the chapter has outlined how the transient framework naturally extends to noise analysis through the Impulse Sensitivity Function, offering a pathway toward comprehensive phase noise characterization and optimization.

Overall, the presented work bridges the gap between device-level physics and system-level oscillator design, providing a valuable toolset for designers aiming to achieve optimal performance and power efficiency in advanced CMOS technologies. Future work could focus on integrating noise source modeling and extending the methodology to differential and injection-locked oscillator architectures for example.

5

Circuits Design and Experimental Validation in 18nm FD-SOI CMOS Technology

This fifth chapter presents two voltage-controlled oscillators designed and fabricated in 18nm FD-SOI CMOS technology. Emphasis is placed on ultra-low voltage operation, body-bias-based tuning, and the integration of a digital control system for next generation RF PLLs.

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5.1 Introduction

Charge-based transistor models provide circuit designers with an effective tool to systematically explore transistor operating regimes, facilitating the identification of optimal supply voltages for ultra-low power circuits. The preceding chapter introduced a theoretical framework leveraging charge-based modeling to navigate the design space of ultra-low voltage and ultra-low power RF ring oscillators.

While this theoretical foundation is essential, practical circuit design techniques play a critical role in reducing power consumption and enhancing the efficiency of RF building blocks. This chapter focuses on the application of such design methodologies to RF ring voltage-controlled oscillators (VCOs), presenting two distinct circuit implementations developed with complementary objectives.

The first taped-out circuit is an analog multi-tuning wide-band RF ring oscillator operating at low supply voltage. This design serves as a technological benchmark to evaluate the 18nm FD-SOI CMOS process capabilities for RF applications, particularly targeting RF PLL frequency synthesis for IoT applications around 2.4 GHz, and to delineate the technology's performance limits in this context.

The second circuit introduces a pseudo-differential ring oscillator featuring a modified core topology. This design integrates a fully digital frequency control system based on a switched-capacitor digital-to-analog converter (DAC). Key improvements include transistor length reduction and the use of asymmetrical inverters to optimize the oscillator core. Developed with a system-level perspective, this second implementation aims to provide a compact, fully integrated functional block suitable for direct integration as the oscillating core and frequency control element within modern RF PLL architectures.

5.2 Analog Multi-Tuning Low Power Ring Oscillator

5.2.1 Introduction

5.2.1.1 Objectives

This first tape-out targets several key objectives. Primarily, it aims to characterize the technological capabilities of the 18nm FD-SOI CMOS process for ultra-low voltage (ULV) and ultra-low power (ULP) RF frequency synthesis applications. Additionally, it seeks to demonstrate the advantages offered by the 18nm FD-SOI CMOS technology, particularly with respect to its adaptive and extensive body-biasing capability. Finally, inspired by methodologies commonly used in the digital domain, this work proposes a novel approach to establish a clear and practical RF technology marker based on a inverter-based ring oscillator block. This approach is in line with the recent trend of massively digital RF circuits.

5.2.1.2 Design Goals

While maintaining the objective of characterizing the technological capabilities of the 18nm FD-SOI CMOS technology for ultra-low voltage (ULV) and ultra-low power (ULP) RF frequency synthesis applications, the specifications have been defined with industrial relevance in mind. In particular, stringent requirements typical of Wake-up Radio applications are considered. The design targets a central oscillation frequency of 2.442 GHz, aiming for a frequency resolution (digital frequency step) of 100 kHz achievable with an acceptable control voltage step on the order of tens of millivolts. The circuit is required to operate at a supply voltage of 0.9 V or below, with power consumption constrained to less than 200 μW, and an active area limited to under 0.01 mm^2. Furthermore, stringent phase noise performance targets are set to -80 dBc/Hz at a 1 MHz offset and -100 dBc/Hz at a 20 MHz offset from the carrier frequency. The output stage is specified to provide differential signals to ensure compatibility with typical RF system architectures. The targeted specifications are summarized in Table 5.1.

5.2.1.3 Section Structure

The remainder of section 5.2 is organized as follows: section 5.2.2 details the technological context and design constraints relevant to the proposed circuit. Section 5.2.3 presents an in-depth description of the circuit design, followed by section 5.2.4, which covers the associated layout implementation. Section 5.2.5 discusses the obtained measurement results and their comparison with simulations. Finally, section 5.2.6 concludes the section with a benchmarking analysis, comparing the proposed circuit against state-of-the-art ring oscillators meeting similar specifications.

Parameter	Specification
Frequency range (MHz)	[2412 ; 2472]
Digital frequency step (kHz)	< 100
Supply Voltage (V)	< 0.9
Power consumption (μW)	< 200
Area (mm^2)	< 0.01
Phase noise at 1 MHz offset (dBc/Hz)	-80
Phase noise at 20 MHz offset (dBc/Hz)	-100
Output	Differential

Table 5.1: Specifications table.

5.2.2 Technological Context and Design Constraints

5.2.2.1 18nm FD-SOI CMOS Technology Features

Prior to the circuit design phase, several key technological choices were made to fully leverage the capabilities of the 18nm FD-SOI CMOS technology, particularly in the context of IoT applications characterized by stringent power consumption and frequency modularity requirements.

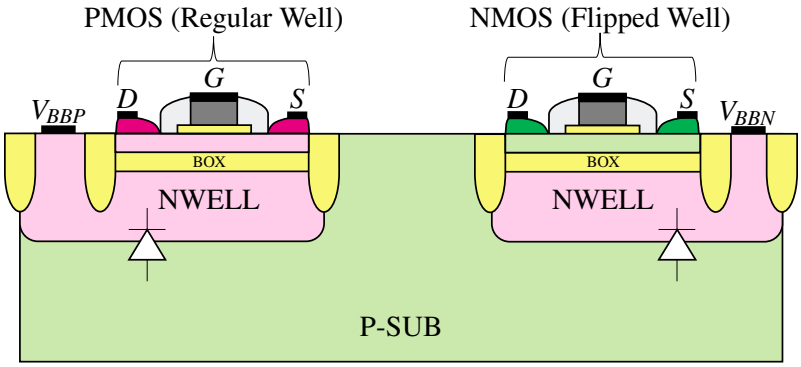
Given the target application domain, an inverter-based ring voltage-controlled oscillator (RVCO) was selected over an LC voltage-controlled oscillator (LC-VCO), primarily due to cost considerations related to the significantly larger silicon area demanded by LC-VCOs compared to RVCOs.

With this architectural choice established, the stringent power consumption constraints motivated a reduction in the supply voltage to the achievable minimal from the nominal 0.9 V of the technology down to approximately 0.6 V. To ensure reliable operation of the ring oscillator at this reduced voltage, low-threshold voltage (LVT) transistors were employed, as illustrated in Figure 5.1a. The use of LVT devices facilitates robust switching behavior while enabling supply voltage scaling.

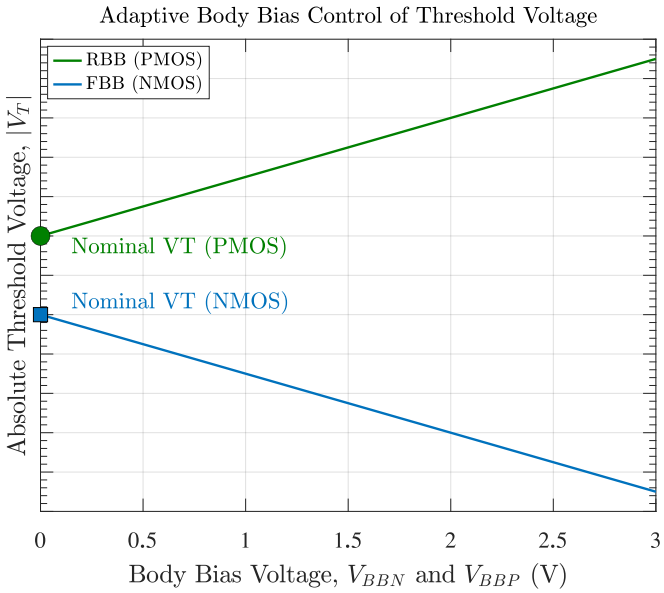
To achieve the required high frequency tunability without compromising power efficiency, body-bias tuning was adopted as the primary frequency control mechanism. In particular, the concept of adaptive body biasing, as detailed in [18], was explored. This technique enhances the tunability of CMOS blocks, such as inverters, while simultaneously improving circuit robustness against variability. Consequently, adaptive body biasing allows compensation for process variations without degrading the oscillator's frequency control range.

To minimize circuit complexity and avoid the overhead associated with negative voltage generation, only positive body-bias voltages were utilized. This design decision re-

duces both area and power consumption. Regarding the transistor flavor selection within the CMOS blocks, the NMOS devices are implemented with flipped wells, whereas the PMOS devices use regular wells, as depicted in Figure 5.1a. This configuration was retained among others since it offers the required capability for adaptive body-biasing in CMOS circuitry while maintaining a compact layout. Thus, these technological choices establish a foundation optimized for energy-efficient, tunable, and compact circuit implementation in 18 nm FD-SOI CMOS.



(a)



(b)

Figure 5.1: (a) Cross-section of LVT transistors in 18nm CMOS. (b) Body-bias control mechanism for threshold voltage tuning.

5.2.2.2 ULV/ULP Design Challenges

Building upon the technological choices previously presented, the design of ULV/ULP circuits in 18nm FD-SOI CMOS technology faces several intrinsic challenges that must be carefully managed.

The adoption of LVT transistors, as introduced in Figure 5.1a, enables operation at re-

duced supply voltages, which is essential to meet stringent power consumption targets. However, this advantage comes at the cost of increased leakage currents, which can significantly impact the overall power budget—particularly in always-on or standby modes common in IoT applications. Effective leakage management is therefore critical and often relies on complementary techniques such as adaptive body biasing, which was discussed previously, to dynamically tune transistor thresholds and mitigate static power dissipation without sacrificing performance.

Another fundamental limitation arises from the extent of supply voltage scaling. While lowering the supply voltage from the nominal 0.9 V towards 0.6 V reduces dynamic power consumption, it also reduces the transistor drive current exponentially as the voltage approaches the threshold level. This reduction leads to slower switching speeds and increased sensitivity to process, voltage, and temperature (PVT) variations, which can degrade the oscillator's frequency stability and phase noise performance. The design must thus carefully balance supply voltage reduction against these adverse effects to ensure reliable operation.

Furthermore, operating in the ULV regime amplifies the impact of device variability and mismatch, which can cause significant deviations in transistor behavior and circuit characteristics. The adaptive body-biasing strategy, as introduced earlier, plays a crucial role in enhancing robustness by compensating for these variations, thereby maintaining consistent oscillator performance.

Finally, the design must address the inherent trade-offs between power consumption, frequency tunability, and noise performance. Achieving an optimal balance requires judicious transistor sizing, biasing schemes, and architectural decisions tailored to the specific application constraints.

In conclusion, the ULV/ULP design challenges in 18nm FD-SOI CMOS technology necessitate a comprehensive approach that integrates leakage control, supply voltage scaling limits, variability mitigation, and performance optimization to realize efficient, robust RF circuits suitable for IoT applications.

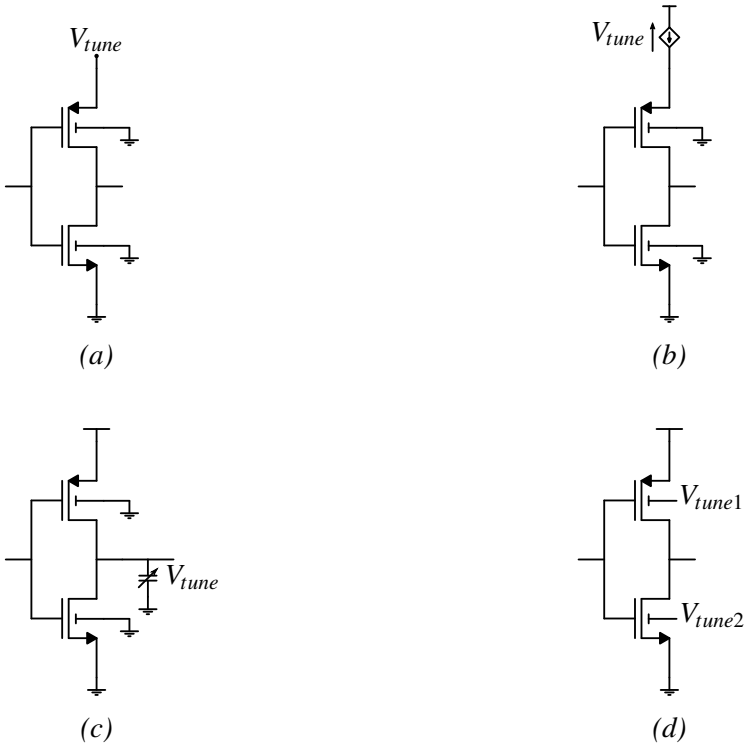


Figure 5.2: Tuning strategies of a CMOS inverter-based delay cell: (a) supply voltage variation, (b) current starving, (c) capacitive loading modulation, and (d) back-gate (body) bias tuning.

5.2.3 Circuit Design

5.2.3.1 Overall Architecture & Tuning Strategies

Several frequency tuning strategies are commonly employed for voltage-controlled ring oscillators. Figure 5.2 summarizes the four most prevalent methods for tuning the propagation delay of a CMOS inverter-based delay cell, and consequently the oscillation frequency of a ring oscillator composed of such cells.

The first technique, illustrated in Figure 5.2a, consists of varying the supply voltage of the delay cell itself. While this approach offers a large frequency gain relative to the applied voltage variation around the nominal supply, it has the primary drawback of causing the output waveform amplitude and shape to vary with the supply voltage, potentially impacting signal integrity. The second method, depicted in Figure 5.2b and commonly referred to as "current starving," controls the bias current of the delay cell without modulating its supply voltage. Although this technique provides fine frequency control, it requires an additional voltage-to-current conversion stage, which may not be ideal for ultra-low voltage (ULV) and ultra-low power (ULP) applications due to increased complexity and power overhead. The third approach, shown in Figure 5.2c, modulates the load capacitance between delay cells. This capacitive tuning alters the delay by changing the effective capacitive load, offering a relatively linear frequency control mechanism without affecting

the supply voltage or bias current. Finally, the fourth technique, illustrated in Figure 5.2d, leverages the unique properties of SOI transistors by modulating the threshold voltage of the NMOS and respectively PMOS devices via back-gate (body) biasing. This method provides efficient frequency tuning by adjusting the transistor thresholds, thereby controlling the delay without significantly affecting the output waveform amplitude or power consumption.

The overall architecture of the proposed circuit is illustrated in Figure 5.3. It comprises a pseudo-differential inverter-based voltage-controlled ring oscillator (VCO) core, followed by two symmetrical buffer chains. The two output signals, denoted as $V_{out,+}$ and $V_{out,-}$, are in phase opposition, providing differential outputs. The VCO core and the buffer stages are powered by independent supply voltages, referred to as $V_{DD,core}$ and $V_{DD,buffer}$, respectively. Additional voltage control inputs, labeled V_{BBN}, V_{BBP}, $V_{BBN,var}$, and $V_{BBP,var}$, are dedicated to frequency tuning. This choice of basing the tuning strategy on the modulation of the MOS transistors' back gates is particularly efficient in FD-SOI CMOS technology [9], where the back-gate voltage tuning range generally spans from 0 V to 3 V.

Our proposed multi-tuning low-power ring oscillator combines three of the tuning techniques described above to achieve a wide range of frequency control, spanning from GHz/V-level coarse tuning to kHz/V-level fine tuning. This hierarchical approach enables both broad frequency coverage and precise adjustment. The employed tuning strategies are summarized in Table 5.2. While supply voltage tuning follows a conventional approach, the threshold voltage and load capacitance tuning methods are more novel and are detailed later in subsubsection 5.2.3.2.

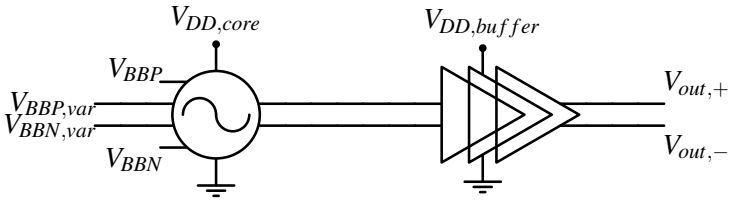


Figure 5.3: Overall architecture.

Tuning Strategy	Control Type	Voltage Control Node
Supply Voltage	Continuous Analog	$V_{DD,core}$
Threshold Voltage (NMOS)	Continuous Analog	V_{BBN}
Threshold Voltage (PMOS)	Continuous Analog	V_{BBP}
Load Capacitance (NMOS)	Digital Step	$V_{BBN,var}$
Load Capacitance (PMOS)	Digital Step	$V_{BBP,var}$

Table 5.2: Summary of employed tuning strategies.

5.2.3.2 Ring Oscillator

The proposed ring oscillator is based on a pseudo-differential inverter-based ring architecture, as illustrated in Figure 5.4a.

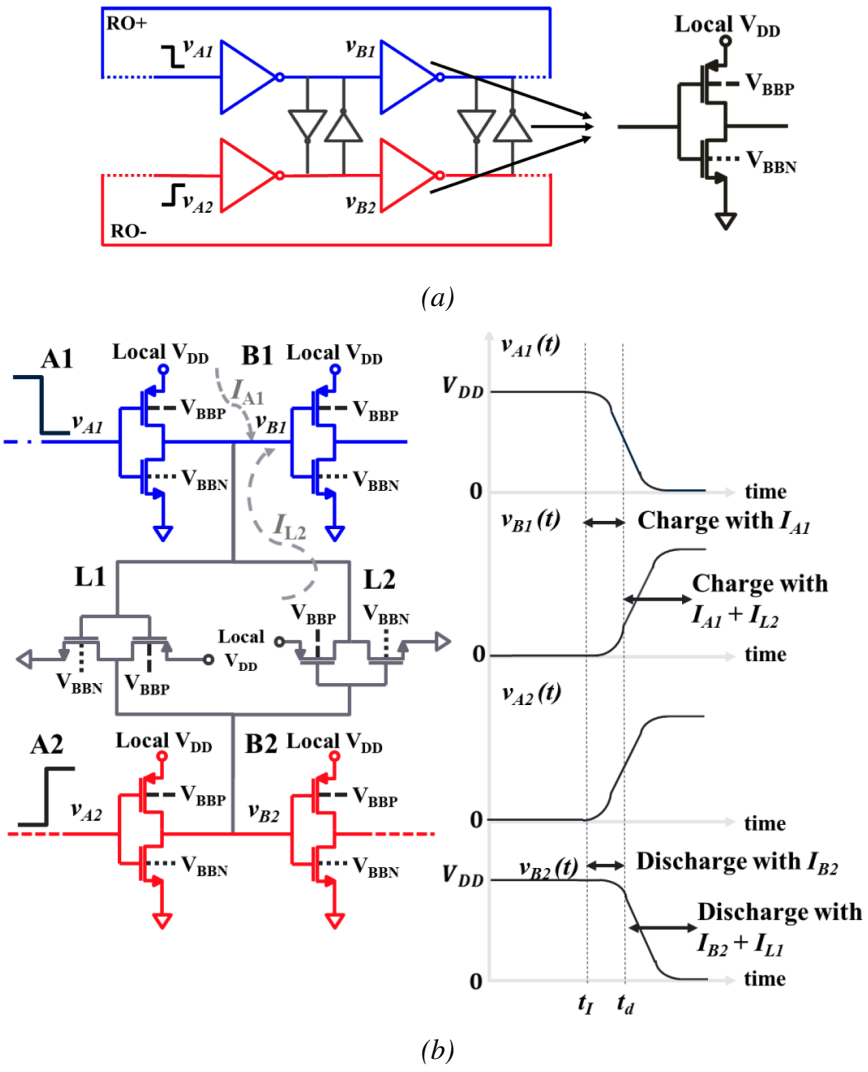


Figure 5.4: Classical architecture of a pseudo-differential inverter-based ring voltage-controlled oscillator (a) and its associated charging and discharging timing zones during a transition (b). Courtesy of David Gaidioz [26, 32], used with permission.

As shown in Figure 5.4b, this architecture operates by pre-charging (and respectively pre-discharging) the main inverter lines (highlighted in blue and red) through auxiliary latch inverters (in gray). This pre-charging and pre-discharging mechanism sharpens the signal transitions, thereby improving the overall phase noise performance of the oscillator while introducing only a limited increase in power consumption. Moreover, these auxiliary inverters reinforce the differential nature of the oscillator outputs by dynamically maintaining the two main lines in antiphase, ensuring a consistent 180° phase difference between them.

In order to meet the stringent phase-noise requirements while preserving the differential nature of the output signals, the proposed ring oscillator adopts a pseudo-differential core architecture in which one of the latch stages is replaced by CMOS varactors, as illustrated in Figure 5.5. This design enhances the controllability of the oscillation frequency without degrading phase-noise performance or output symmetry. Furthermore, the proposed core integrates its own output buffer stage, implemented using the same inverter-based topology as the PD-RVCO. This approach ensures minimal loading effects and maintains the intrinsic differential balance of the oscillator outputs.

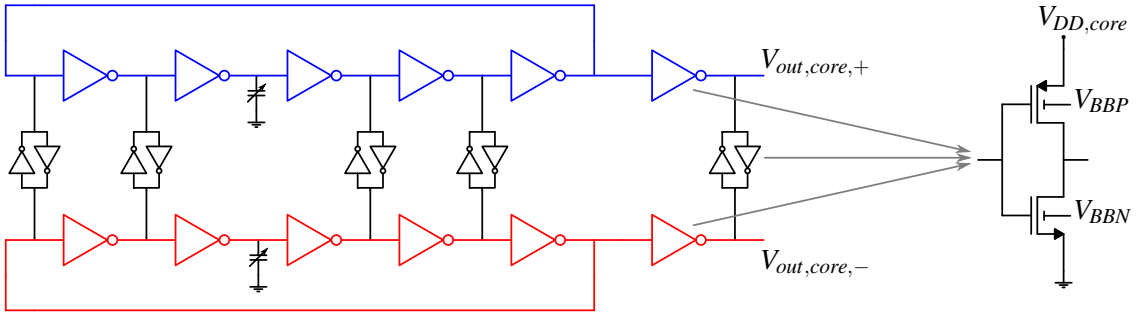


Figure 5.5: Proposed pseudo-differential ring oscillator core architecture incorporating CMOS varactors and an integrated buffer stage.

Replacing a latch stage with varactors enables fine frequency tuning by modulating the effective capacitance within the oscillator loop, thereby adjusting the oscillation period. This approach preserves the differential nature of the core, which is essential for minimizing common-mode noise and achieving balanced output waveforms.
The transistor geometries selected for the ring oscillator core are summarized in Table 5.3, the length of each transistor being to reduce variability issues. The main inverters transistors are sized to provide sufficient drive strength and speed, while the latch inverters and varactors transistors are dimensioned to optimize tuning range and linearity. As reported in [31], the optimal sizing between the transistors of the main inverter and those of its corresponding latch inverter follows a width ratio of approximately 1:4. Due to technological constraints, this ratio has been applied only to the PMOS devices, while the NMOS transistors were designed with the closest achievable ratio, namely 5:12. For layout uniformity and design simplicity, the MOSFETs composing the latch inverters and those used in the CMOS varactors share identical dimensions.

	Main Inverter	**Latch Inverter**	**CMOS Varactor**
Length (nm)	75	75	75
NMOS Width (μm)	1.2	0.5	0.5
PMOS Width (μm)	2	0.5	0.5

Table 5.3: Geometry of the transistors composing the ring oscillator core.

The varactors are implemented using body-bias tuning, as depicted in Figure 5.6. This configuration exploits the back-gate control available in FD-SOI CMOS technology to modulate the threshold voltage of the transistors, effectively varying their capacitance. The body-bias voltages $V_{BBN,var}$ and $V_{BBP,var}$ serve as tuning knobs, enabling fine frequency adjustment with minimal impact on power consumption. Each transistor has its source and drain terminals shorted together and connected to a respective "cold" node, while their gates are tied together to form the active terminal, denoted as V_{ring}.

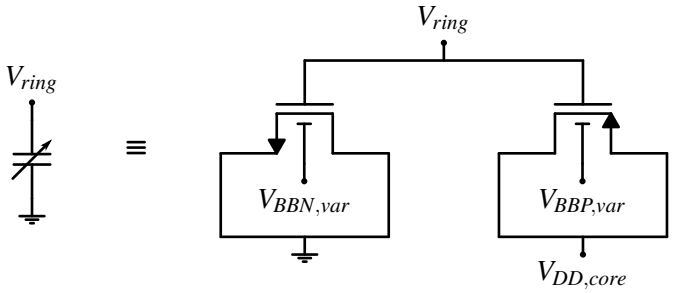


Figure 5.6: Proposed body-bias-tuned CMOS varactor. The two transistors composing the varactor are controlled through body biasing. Each transistor has its source and drain terminals shorted together and connected to a respective "cold" node, while their gates are tied together to form the active terminal, denoted as V_{ring}.

By applying body-bias voltages to each of the transistors composing the varactor, the shape of the bell-shaped C/V curve can be independently modified. Specifically, the body bias applied to the PMOS device controls the position of the rising edge of the curve along the voltage axis, while the body bias of the NMOS device modulates the position of the falling edge. When identical body-bias voltages are applied to both transistors, as in Figure 5.7, the modulation affects primarily the height of the bell, corresponding to the effective capacitance value.

The operation of the ring oscillator is governed by the successive charging and discharging of the capacitances within its inverter stages. In this context, the effective capacitance of the varactor corresponds to the integrated area under the C/V curve between the low logic level (typically 0 V) and the high level (typically V_{DD}). Table 5.4 presents the extracted capacitance variation associated with the curve shown in Figure 5.7. This configuration illustrates the minimum achievable capacitance difference between two adjacent body-bias states. In the present case, between 0 V and 2 V, a variation slope of approximately -3 aF/V is obtained.

This pseudo-differential architecture, combined with body-bias controlled varactors, offers a robust and power-efficient solution for achieving wide tuning range and fine frequency resolution, critical for RF PLL applications in ultra-low voltage environments.

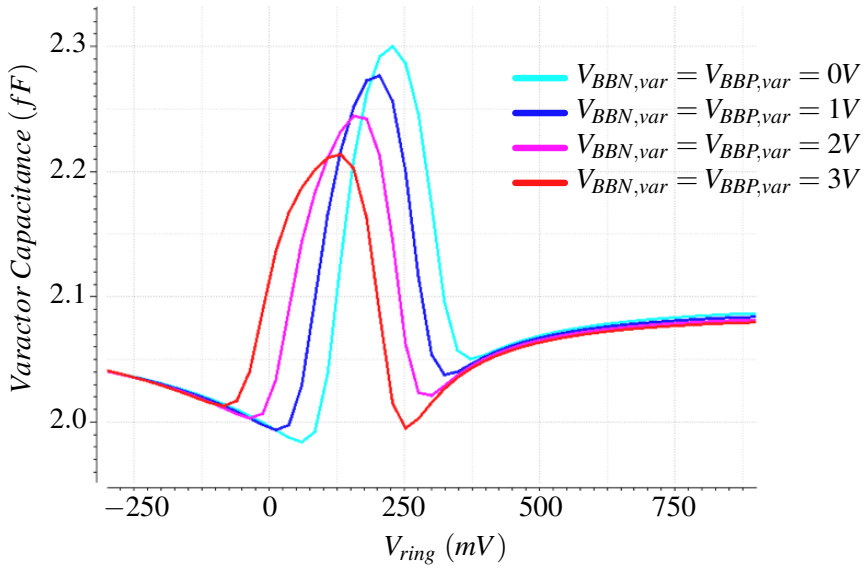


Figure 5.7: C/V characteristic of the proposed varactor used in the RVCO. The curve illustrates the minimum achievable capacitance difference between two adjacent tuning states, obtained by jointly varying the two body-bias control voltages, $V_{\mathrm{BBN,var}}$ and $V_{\mathrm{BBP,var}}$.

$V_{BBN,var} = V_{BBP,var} = V_{BB}\ (V)$	*Varactor Capacitance* (fF)	$\Delta C\ (aF)$ *wrt* $V_{BB} = 0V$
0	1.890	0
1	1.887	−3
2	1,884	−6
3	1,877	−13

Table 5.4: Extracted capacitance values of the proposed body-bias-tuned CMOS varactor as a function of the applied back-gate voltage $V_{\mathrm{BBN,var}} = V_{\mathrm{BBP,var}} = V_{\mathrm{BB}}$. The variation ΔC is computed with respect to the reference case $V_{\mathrm{BB}} = 0\,\mathrm{V}$, highlighting the fine tuning capability of the varactor within the RVCO architecture.

5.2.3.3 Output Buffers

The output buffer stage, illustrated in Figure 5.8, consists of two symmetrical inverter chains driving the differential output signals $V_{\mathrm{out},+}$ and $V_{\mathrm{out},-}$. Each chain comprises five inverter stages, with the fourth stage uniquely implemented as a pseudo-differential structure incorporating latches to enhance signal integrity and drive capability.
The transistor dimensions for each buffer stage are summarized in Table 5.5. The NMOS and PMOS widths progressively increase along the chain to ensure sufficient drive strength and preserve signal fidelity across transitions. The fourth stage integrates additional latch transistors to implement the pseudo-differential latch functionality, which is essential to maintain the symmetry between the two output paths and suppress common-mode noise.

The remaining stages consist of standard inverters optimized for speed and power efficiency. The fifth and final stage acts as a power driver capable of delivering an output power of approximately 0 dBm, ensuring that the differential signal amplitude is high enough for accurate phase-noise measurements. All buffer stages share a common supply voltage of 900 mV and a total on-chip decoupling capacitance of 18.25 pF is distributed across the layout according to the instantaneous current demands of each stage, providing supply stabilization and reducing noise coupling into the oscillator core.
A transient simulation of the differential output signals $V_{\text{out},+}$ and $V_{\text{out},-}$ from the buffer chain is shown in Figure 5.9, confirming the correct operation and symmetry of the output waveforms.

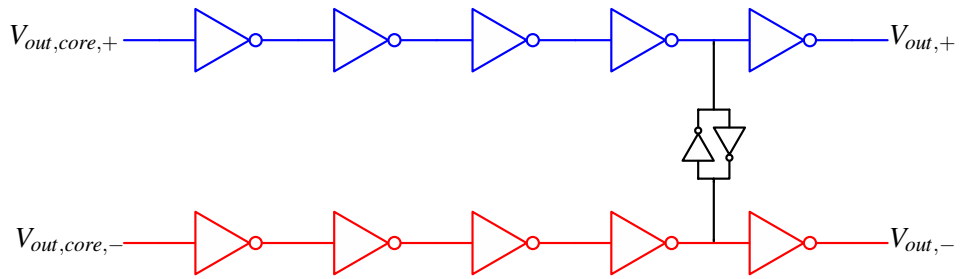


Figure 5.8: Architecture of the differential output buffer stage composed of five cascaded inverter stages. The fourth stage implements a pseudo-differential latch configuration to preserve signal symmetry at the oscillator outputs.

Table 5.5: Transistor dimensions of the output buffer stages. The NMOS and PMOS widths increase progressively along the tapered chain to ensure sufficient drive strength. The fourth stage incorporates additional latch transistors implementing a pseudo-differential structure for enhanced output balance.

Buffer Stage	**NMOS Width (µm)**	**PMOS Width (µm)**	**Latch NMOS Width (µm)**	**Latch PMOS Width (µm)**	**Latches**
1	1.2	2	-	-	No
2	1.2	2	-	-	No
3	2.4	4	-	-	No
4	4.8	8	2.4	4	Yes
5	9.6	16	-	-	No

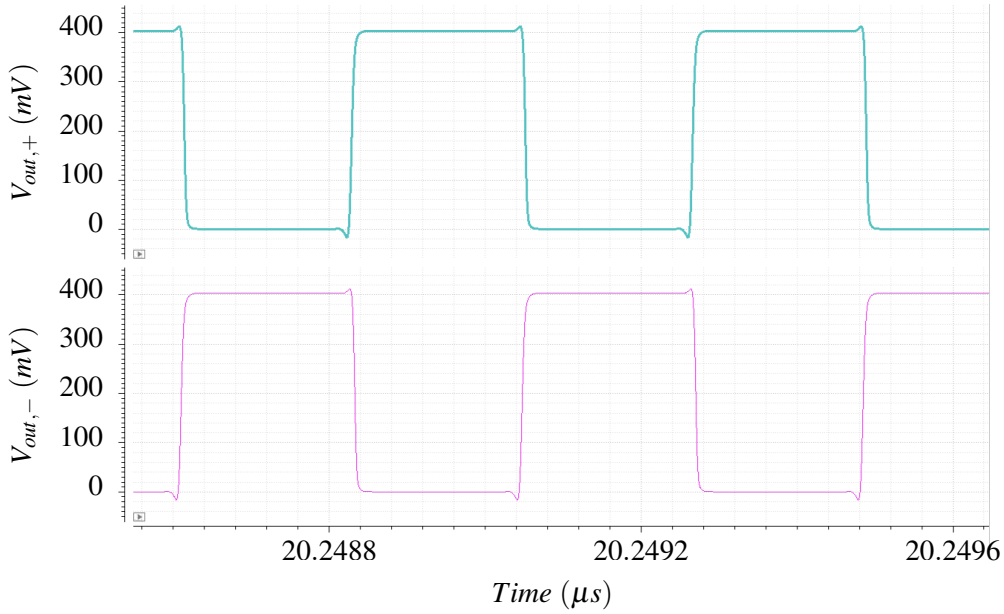


Figure 5.9: Transient simulation of the differential output signals $V_{\text{out},+}$ and $V_{\text{out},-}$ at the final buffer stage. The simulation confirms balanced amplitude, waveform symmetry, and correct phase opposition at the outputs, validating the effectiveness of the pseudo-differential latch configuration.

5.2.4 Circuit Integration

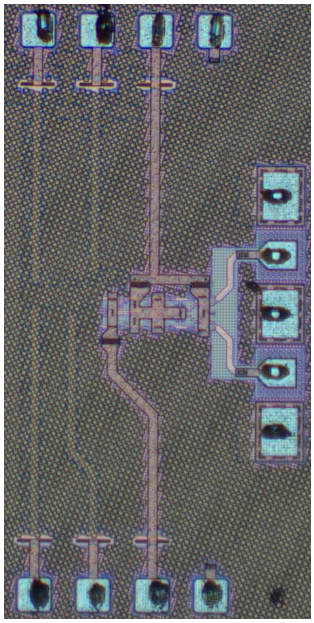
This section presents the overall layout of the previously presented design, detailing the integration approach and the key layout constraints applied to ensure optimal circuit performance and manufacturability. The layout encompasses the VCO core and the supporting circuitry, arranged to satisfy both general and 18nm FD-SOI CMOS technology-specific requirements presented below. Figures 5.10a and 5.10b depict the complete circuit as well as the DC and RF pads alongside the DC and RF lines and a close-up view on the circuit core.

5.2.4.1 General Layout Constraints

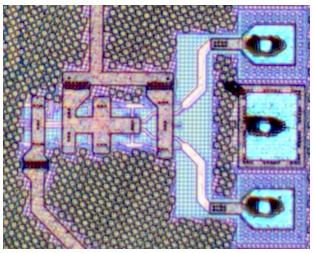
Because inverter-based designs exhibit extremely high sensitivity to supply variations and noise, the following general layout techniques were implemented throughout the design :

- **Internal Decoupling Capacitance:** Decoupling capacitors are strategically placed in close proximity to critical blocks, particularly the output buffer stages, to stabilize the supply voltage and suppress high-frequency noise.

- **Supply Path Segmentation:** The supply lines are segmented with added series resistance to isolate different circuit blocks, preventing supply noise propagation and reducing interference between the different stages of the output buffer. The VCO core and the output buffer stages are supplied by independent DC lines, firstly



(a)



(b)

Figure 5.10: Chip microphotograph presenting the circuit core as well as the DC and RF pads (a) and chip microphotograph presenting a close-up view on the circuit core (b).

because the two blocks were designed to be supplied differently, and secondly to be able to monitor the power consumption of the VCO core on one side and of the output buffers on the other side.

5.2.4.2 18nm FD-SOI CMOS Specific Layout Constraints

In addition to the general constraints, the 18nm FD-SOI CMOS technology imposes specific layout requirements to fully exploit its advantages and ensure yield:

- **Double Patterning Compliance:** Because it is a deep nm process, there are very constrained rules on the photolithography. They are alleviated by using the double patterning technique.
- **Co-integration of Regular Well LVT PMOS and Flipped Well LVT NMOS FETs:** Special attention is paid to wells separation between the two devices to ensure the adaptive body-biasing technique without increasing the parasitic resistances and capacitances of the composed inverters.
- **Poly Dummies:** Dummy polysilicon gates are uniformly inserted around active devices to maintain consistent processing conditions, ensuring uniform current density and mitigating stress-induced variability.
- **Metal Fill and Density Rules:** Metal fill patterns are applied to satisfy density requirements, preventing dishing and erosion during chemical-mechanical polishing

(CMP), thereby preserving metal integrity and planarity.

The layout also incorporates symmetric device placement and matched routing for the two output buffer paths to minimize mismatch and common-mode noise. The placement and routing of the decoupling capacitors is optimized to minimize inductive paths, and to enhance the stability of the voltage supply of each block.
Figures 5.11 and 5.12 provide detailed views of the VCO core and of the VCO core alongside its output buffers stage, respectively, illustrating the implementation of the aforementioned constraints.

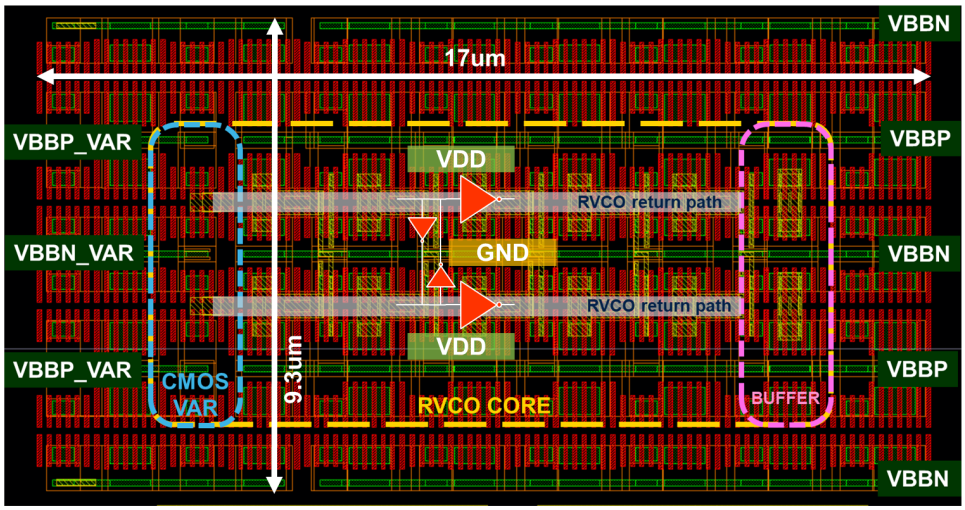


Figure 5.11: Layout of the VCO core, presenting wells co-integration, and poly dummies utilization.

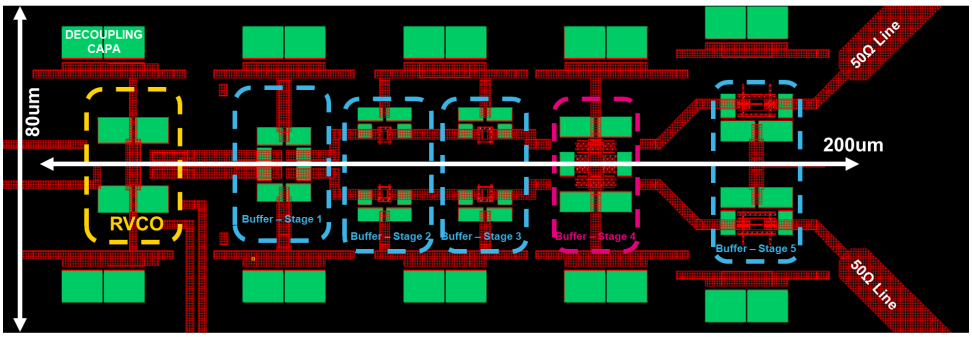


Figure 5.12: Layout of the VCO accompanied with its output buffers stage, highlighting the decoupling capacitors placement strategy and the symmetric strategy placement of the two output paths.

5.2.5 Simulation and Measurement Results

The frequency performance of the proposed ring oscillator was characterized through simulation and and then confirmed through extensive silicon measurements, focusing on the dependence of the oscillation frequency on the supply voltage (V_{DD}) and the body-bias voltage (V_{BBN}). The core supply voltage ($V_{DD,core}$) was set equal to the positive body-bias voltage (V_{BBP}), while the buffer stages were powered at a fixed 900 mV ($V_{DD,buffer} = 900$ mV). This choice is motivated by the frequency–supply sensitivity of the proposed VCO. Since the oscillation frequency exhibits a negative slope with respect to V_{BBP}, tying $V_{DD,core}$ to the positive body-bias voltage causes both quantities to vary coherently. This co-variation partially compensates the intrinsic dependence of the oscillation frequency on $V_{DD,core}$, thereby reducing its effective sensitivity to supply fluctuations. As a result, the amount of supply noise that is upconverted into phase noise is significantly reduced, improving the spectral purity of the oscillator under low-voltage operation.
Figure 5.13 presents the measured and simulated extremum frequencies as a function of V_{DD}, comparing the cases of zero body-bias ($V_{BBN} = 0$ V) and elevated body-bias ($V_{BBN} = 3$ V). The results demonstrate strong agreement between simulation and measurement across the entire supply voltage range from approximately 0.5 V to 1.0 V.

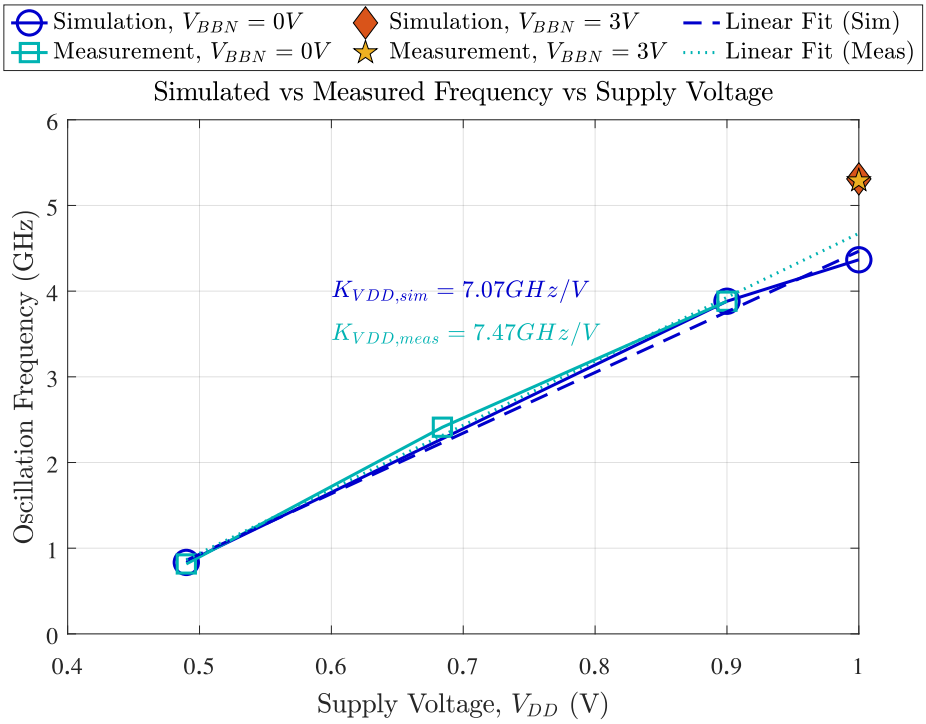


Figure 5.13: Simulated and measured oscillation frequencies of the ring oscillator as a function of supply voltage V_{DD} and for different body-bias voltages V_{BBN}. Simulations were performed under the typical process corner.

The frequency tuning sensitivity with respect to the supply voltage, denoted as K_{VDD}, was

extracted from linear fits of the data. Measurements indicate a tuning gain of $K_{VDD,meas} = 7.47$ GHz/V, closely matching the simulated value of $K_{VDD,sim} = 7.1$ GHz/V. This agreement validates the accuracy of the transistor models and simulation methodology employed.

Furthermore, applying a positive body-bias of 3 V ($V_{BBN} = 3$ V) shifts the frequency response upward, enabling an extended tuning range at a given supply voltage. This confirms the effectiveness of body-bias tuning in enhancing oscillator performance.

The coarse frequency tuning capability was further investigated by varying the negative body-bias voltage (V_{BBN}) while maintaining the core supply voltage at $V_{DD,core} = V_{BBP} = 680$ mV and the buffer supply voltage fixed at $V_{DD,buffer} = 900$ mV. The varactor tuning voltages were held at zero ($V_{BBN,var} = V_{BBP,var} = 0$ V) to isolate the coarse tuning effect.

Figure 5.14 compares simulated and measured oscillation frequencies as a function of V_{BBN}. The measured frequency increases from approximately 2.41 GHz to 2.48 GHz over the tested V_{BBN} range, corresponding to a tuning sensitivity of $K_{VBBN,meas} = 348$ MHz/V. Simulation results predict a slightly lower tuning gain of $K_{VBBN,sim} = 288$ MHz/V. The small 2.43% deviation attests to the excellent agreement between simulation and measurement in 18nm FD-SOI CMOS.

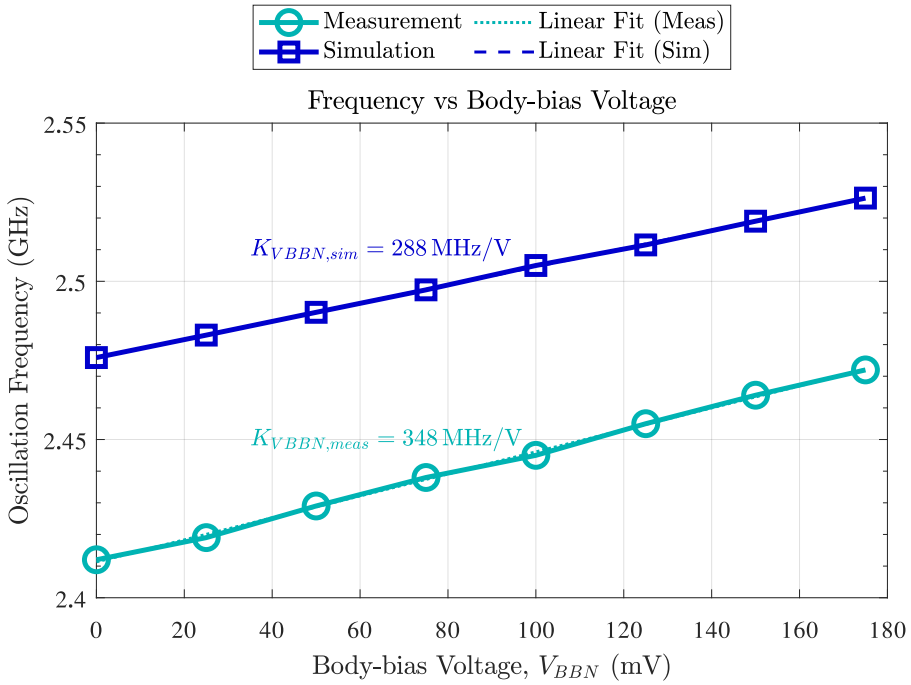


Figure 5.14: Measured and simulated oscillation frequency as a function of body-bias voltage V_{BBN}. The plot includes linear fits and annotated tuning slopes for both measurement and simulation data. Simulations were performed under the typical process corner.

Simultaneously, Figure 5.15 presents the power consumption versus V_{BBN}. Measurements show a power increase from about 282 μW to 288 μW, yielding a sensitivity of 38.9

μW/V. Simulated power consumption is lower, increasing from 247 μW to 254 μW, with a slope of 35.7 μW/V. The measured power exceeds simulation by approximately 12.2%, which may be due to parasitic effects and measurement setup overhead.
These results demonstrate effective coarse frequency tuning via body-bias control with moderate power trade-offs. The close agreement between simulation and measurement validates the design methodology and the accuracy of the device models used.

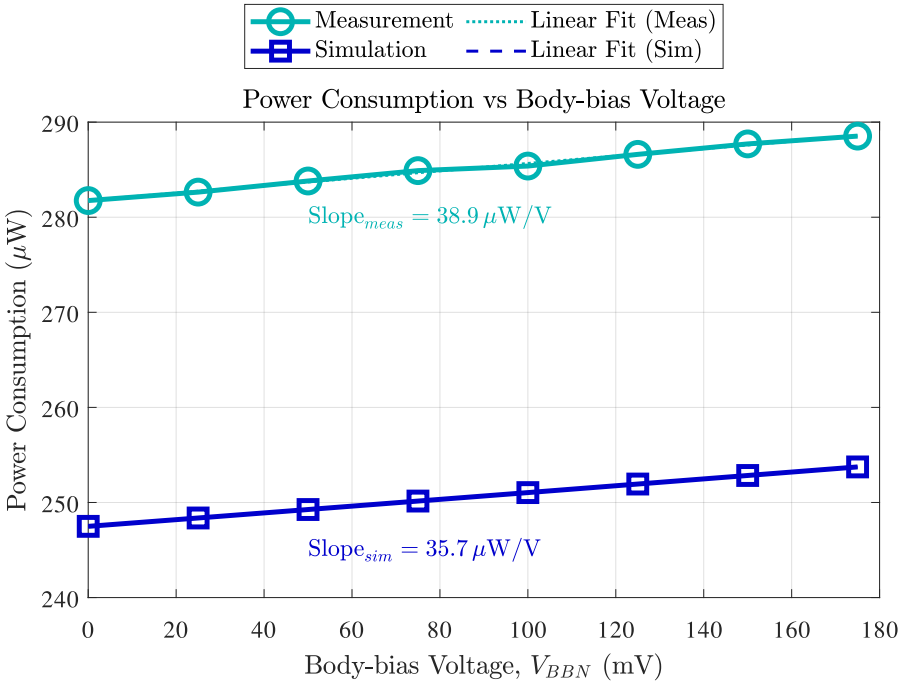


Figure 5.15: Measured and simulated power consumption as a function of body-bias voltage V_{BBN}. Linear fits and annotated slopes are shown for both measurement and simulation results. Simulations were performed under the typical process corner.

The fine tuning capability of the oscillator is realized through a varactor-like structure integrated within the ring oscillator core. As illustrated in Figure 5.16, the oscillator frequency is plotted as a function of the varactor control voltages. The measurements were conducted with the core supply voltage set to $V_{DD,core} = VBBP = 680\,\text{mV}$, the buffer supply fixed at $V_{DD,buffer} = 900\,\text{mV}$, and a constant body-bias voltage of $V_{BBN} = 86\,\text{mV}$.
The horizontal axis presents two complementary voltage scales: the bottom axis corresponds to the negative varactor control voltage $V_{BBN,var}$ ranging from 0 to 3 V, while the top axis corresponds to the positive varactor control voltage $V_{BBP,var}$ ranging from 0 to 3 V but mirrored. This dual-axis representation highlights the symmetrical tuning mechanism enabled by the varactor structure.
The oscillator frequency exhibits a linear dependence on the varactor control voltage for both measurement and simulation. The tuning sensitivities extracted from the linear fits are $K_{\text{varactor},meas} = 2.12\,\text{MHz/V}$ and $K_{\text{varactor},sim} = 1.74\,\text{MHz/V}$, respectively. The minor

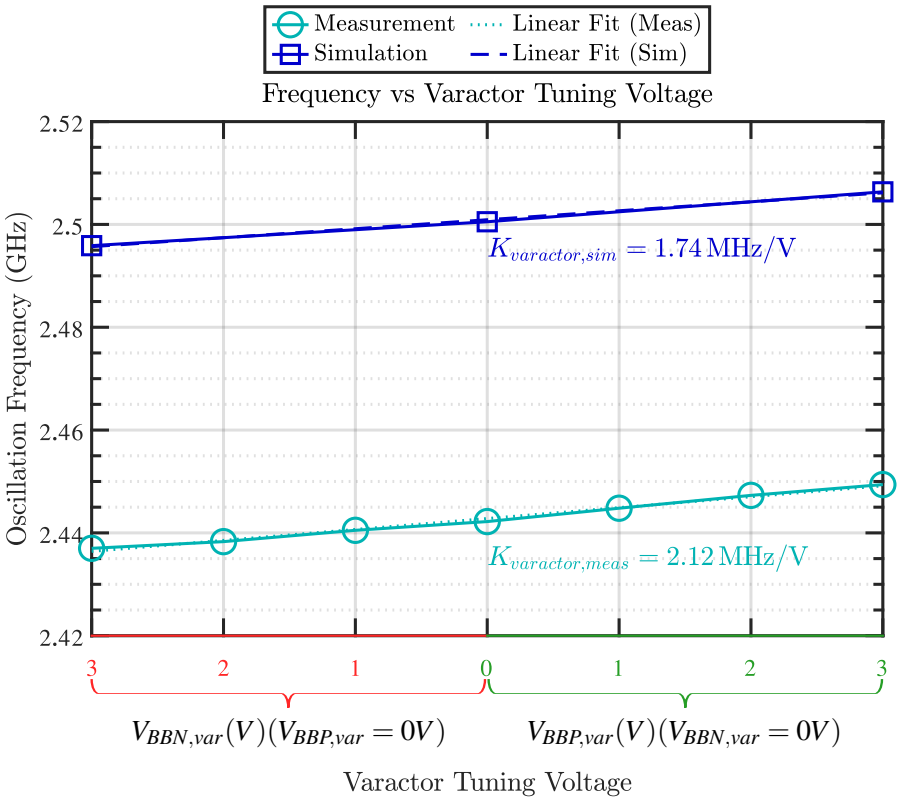


Figure 5.16: Oscillation frequency versus varactor tuning voltage, showing measurement and simulation results. Simulations were performed under the typical process corner.

discrepancy of approximately 2.4% between measurement and simulation at zero tuning voltage reflects the very strong agreement between the two and confirms the accuracy of the modeling.

This fine tuning range, although smaller compared to coarse tuning methods, provides precise frequency control essential for oscillator calibration and phase noise optimization in ultra-low power applications. The results validate the effectiveness of the varactor-like structure in achieving fine frequency modulation with minimal impact on power consumption and area.

The phase noise performance of the proposed oscillator was characterized through both measurement and simulation, as depicted in Figure 5.17. The measurements were conducted with the core supply voltage set to $V_{DD,core} = V_{BBP} = 680\,\mathrm{mV}$, the buffer supply fixed at $V_{DD,buffer} = 900\,\mathrm{mV}$, and the body-bias voltage at $V_{BBN} = 0\,\mathrm{V}$.

The plot displays the phase noise spectral density as a function of offset frequency over a wide range, from 100 kHz to 3 GHz. The measured phase noise exhibits the expected $1/f^3$ slope at low offset frequencies, transitioning to a $1/f^2$ region before flattening at higher offsets.

Simulation results closely follow the measured data across the entire frequency span, with the simulated phase noise at 1 MHz offset reaching $-82.0\,\mathrm{dBc/Hz}$ compared to the mea-

sured $-83.7\,\mathrm{dBc/Hz}$, indicating a difference of approximately 1.7 dB.
This slight discrepancy is attributed to the supply filtering network used during measurement, which effectively presents the oscillator with a current-source-like supply rather than an ideal voltage source. Although further investigation is required, preliminary observations suggest that the filtering network of the supply equipment behaves as a high impedance—almost an open circuit—at the oscillation frequency, thereby forcing the VCO to operate as if driven by a current source.

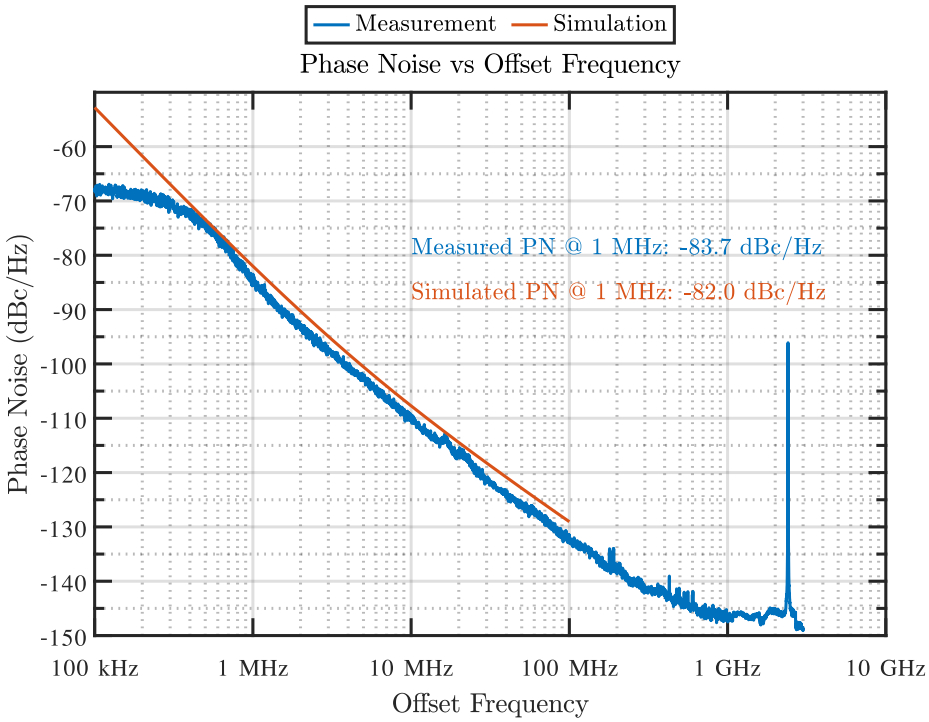


Figure 5.17: Phase noise versus offset frequency for the proposed oscillator at an oscillation frequency of 2.412 GHz, showing measured and simulated data. Simulations were performed under the typical process corner.

5.2.6 Benchmarking and Discussion

A key strength of the proposed multi-tuning ring oscillator lies in its operation at a notably low supply voltage below 0.7 V, which is significantly below the nominal voltage of many state-of-the-art designs. This low-voltage operation is particularly advantageous for ultra-low voltage (ULV) and ultra-low power (ULP) applications, such as wake-up radios and energy-harvesting IoT nodes, where minimizing power consumption is paramount. By exploiting the inherent advantages of the 18nm FD-SOI CMOS technology, especially its adaptive back-gate biasing capability, the design achieves robust functionality and wide frequency tunability without compromising noise performance.

Table 5.6 presents a comprehensive performance summary comparing the proposed oscillator with recent ring oscillator implementations spanning various technology nodes and architectural choices. The comparison includes critical parameters such as output frequency, frequency tuning range (FTR), supply voltage, power consumption, phase noise at 1 MHz and 20 MHz offsets, active area, and two widely accepted figures of merit: the phase noise figure of merit (FoM_{PN}) and the power-aware figure of merit (FoM_{Power}). Additionally, the power spent per frequency metric, initially presented in [26] provides a normalized measure of energy efficiency, facilitating fair comparison across designs operating at different frequencies.

Figures 5.18 and 5.19 visually complement this tabular comparison by plotting the phase noise at 1 MHz offset and power efficiency per frequency, respectively, against the oscillation frequency for the proposed design and reference works.

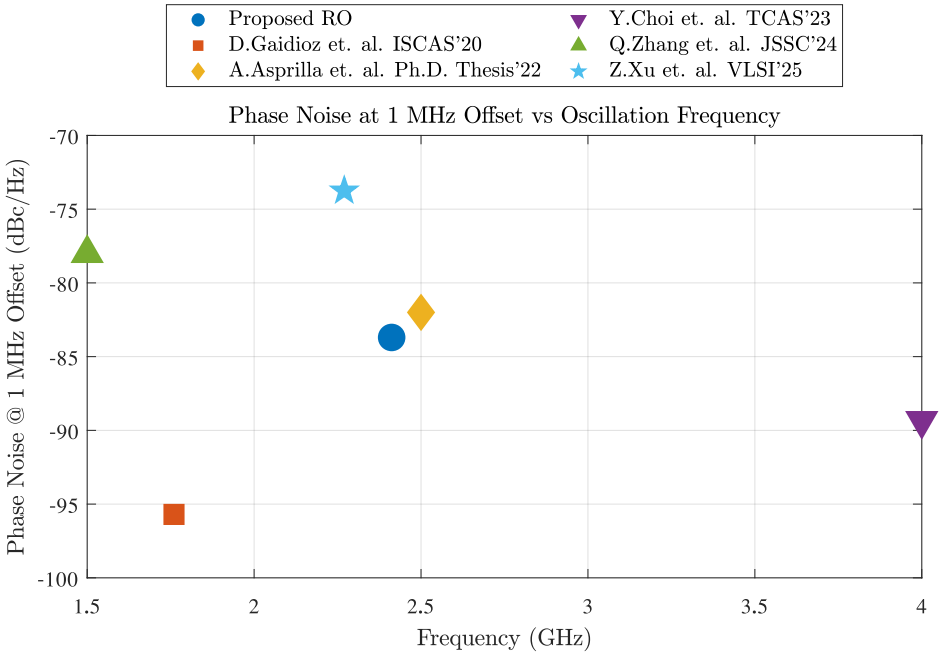


Figure 5.18: Phase noise at 1 MHz offset versus oscillation frequency for the proposed and reference ring oscillators. Lower values indicate better spectral purity.

The proposed oscillator attains a phase noise figure of merit (FoM_{PN}) of -151.35 dBc/Hz and a power-aware figure of merit (FoM_{Power}) of -156.85 dBc/Hz. These values indicate competitive noise performance relative to the power consumed, especially notable given the significantly reduced supply voltage of 0.68 V compared to many references operating at or near 1 V. The normalized power consumption per frequency of 0.117 mW/GHz is among the lowest reported, underscoring the design's excellent energy efficiency and suitability for ULV/ULP applications.

The benchmarking highlights the classical trade-off between phase noise and power consumption. Designs achieving ultra-low phase noise often incur higher power costs, whereas

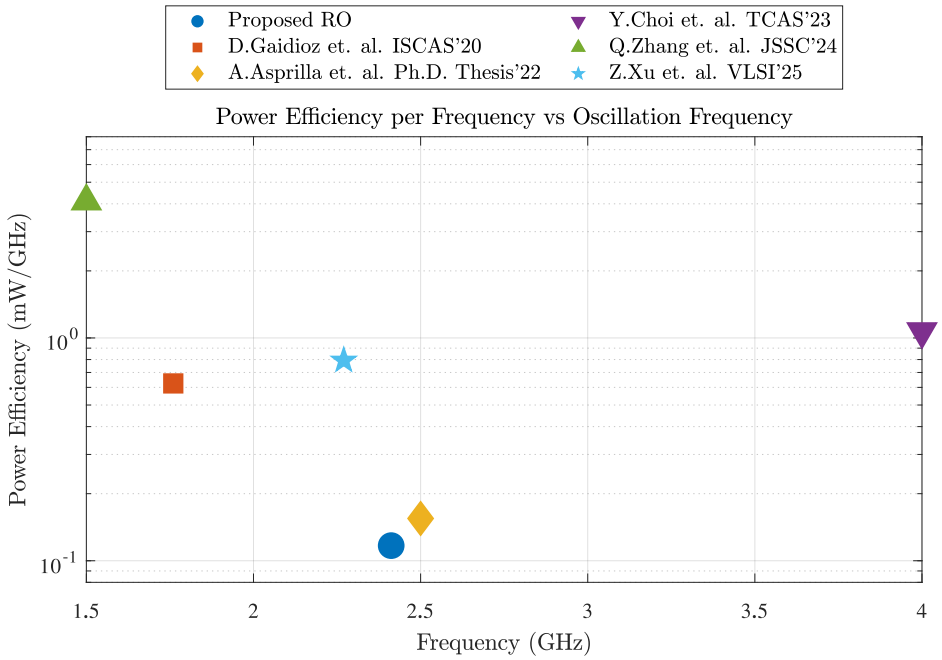


Figure 5.19: Power efficiency per frequency (mW/GHz) versus oscillation frequency for the proposed and reference ring oscillators. Lower values indicate higher energy efficiency.

ultra-low power designs may exhibit slightly degraded noise performance. The proposed design leverages the adaptive back-gate biasing and hierarchical multi-tuning approach to navigate this trade-off effectively, achieving a balanced operating point that meets stringent noise and power requirements simultaneously.

The 18nm FD-SOI CMOS technology's unique back-gate biasing capability is a critical enabler for the proposed design. This feature allows efficient threshold voltage modulation, facilitating wide frequency tuning with minimal power overhead and robust compensation for process-voltage-temperature (PVT) variations. Such intrinsic advantages position FD-SOI CMOS as a highly promising platform for future ultra-low power, high-performance RF oscillators.

In summary, the proposed multi-tuning ring oscillator establishes a strong technological marker for RF design in advanced CMOS processes. It achieves a well-rounded balance between power, phase noise, and frequency tunability, making it highly suitable for integration in next-generation ultra-low power PLLs and frequency synthesizers.

Table 5.6: Performance summary and comparison with state of the art.

	This work	**D. Gaidioz et. al. ISCAS'20 [32]**	**A. Asprilla Ph.D. Thesis'22 [27]**	**Y. Choi et. al. TCAS'23 [34]**	**Q. Zhang et. al. JSSC'24 [35]**	**Z. Xu et. al. VLSI'25 [36]**
Topology	Varactor PD-RVCO	PD-RVCO	RVCO	PD-RVCO	PD-RVCO	RVCO
Control Type	Analog	Analog	Analog	N/A	Digital	Analog
Technology	18nm FD-SOI CMOS	28nm FD-SOI CMOS	28nm FD-SOI CMOS	65nm CMOS	28nm CMOS	22nm CMOS
Output Frequency (GHz)	2.412	1.76	2.5	4	1.5	2.27
FTR (%)	0.816 - 5.29 (146.5%)	0.7 - 2.78 (119.5%)	2.35 - 3 (24.3%)	N/A	N/A	2.27 - 15.83 (149.8%)
Supply Voltage (V)	0.68	1	1	1	1	N/A
Power Consumption (mW)	0.282	1.1	0.387*	4.28	6.16†	1.8
PN@1MHz (dBc/Hz)	-83.7	-95.7	-82*	-89.34	-78*	-73.75
PN@20MHz (dBc/Hz)	-116.2	-126	-124*	-126	-105*	-108*
Area (μm^2)	153	800	7290*	N/A	N/A	N/A
FoM$_{PN}^{(1)}$	-151.35	-160.61	-149.96	-161.38	-141.52	-140.87
FoM$_{Power}^{(2)}$	-156.85	-160.2	-154.08	-155.07	-133.63	-138.32
Power spent per frequency$^{(3)}$ (mW/GHz)	0.117	0.625	0.155	1.07	4.11	0.793

* VCO + VCDL.

† All analog part.

* Obtained from graphical extrapolation.

(1) $\text{FoM}_{\text{PN}} = PN@1MHz - 20\log_{10}\left(\frac{f_0}{1MHz}\right)$

(2) $\text{FoM}_{\text{Power}} = PN@1MHz - 20\log_{10}\left(\frac{f_0}{1MHz}\right) + 10\log_{10}\left(\frac{P}{1\text{mW}}\right)$

(3) Power spent per frequency = Power Consumption (mW) / Output Frequency (GHz)

5.3 Ring Oscillator with Fully Integrated Digital Control System

5.3.1 Introduction

5.3.1.1 Objectives & Design Goals

This second tape-out addresses a distinct set of objectives compared to the previous design. Its primary aim is to deliver a compact, fully integrated functional block that can be directly embedded as the oscillating core and frequency control element within modern RF PLL architectures targeting IoT applications around 2.4 GHz. The analog/RF blocks maintain the same stringent specifications as the previous circuit as provided in Table 5.1, ensuring continuity in performance benchmarks such as phase noise, frequency range, and power consumption.

A key focus of this work is a digital control system, developed as a proof of concept with an emphasis on achieving the lowest possible power consumption while preserving very high frequency tuning precision. The current design prioritizes demonstrating the feasibility and benefits of integrating a switched-capacitor DAC-based digital control within the 18nm FD-SOI CMOS technology.

Moreover, the design leverages minimum transistor lengths in the analog/RF blocks to reduce area and parasitic effects, aligning with a more digital-centric design philosophy. This approach also aims to highlight the advantages of the 18nm FD-SOI CMOS process in supporting mixed-signal integration, combining digital and analog/RF functionalities efficiently on a single die. It is noteworthy that the VCO core as well as the output buffers implemented in this second circuit are entirely different from those designed for the first circuit, both in terms of architecture and design philosophy.

5.3.1.2 Section Structure

The remainder of section 5.3 is structured as follows: section 5.3.2 introduces the overall circuit architecture, highlighting the key design choices. Section 5.3.3 provides a detailed description of the individual building blocks and their implementation. Section 5.3.5 then describes the testability framework of the circuit, presenting the top-level view, supply domains, and required clocking schemes. Section 5.3.4 follows with the layout strategy adopted for each building block and for the overall circuit. Finally, section 5.3.6 presents the post-layout simulation results and offers a comparative discussion, benchmarking the proposed design against recent ring oscillators with similar performance targets.

5.3.2 Overall Architecture

The overall architecture of the proposed circuit is presented in Figure 5.20, while the corresponding supply domains are summarized in Table 5.7. The system is organized into four primary blocks. The first block is the oscillating core, consisting of an inverter-based voltage-controlled oscillator (VCO) whose frequency is tuned via body-bias voltages, denoted as V_{BBN} and V_{BBP}, applied to the back-gates of the composing inverters. The second block is the digital control system, comprising a serial peripheral interface (SPI) and a 2×12-bits sigma-delta digital-to-analog converter ($\Sigma\Delta$-DAC), which includes a pulse-width modulation (PWM) generator, a non-overlapping clock (NOC) generator, and a switched-capacitor filter. The choice of a $\Sigma\Delta$-DAC over resistor-ladder or current-source architectures is motivated by the need for a high-resolution, ultra-low-power conversion scheme, while no stringent constraint is imposed on the output update rate. The dimensioning of the DAC is detailed below in section 5.3.3.2. This digital control system generates the analog voltages that precisely control the oscillator frequency. The third block includes low-leakage switches that serve a recovery function for the digital control system. Finally, the fourth block is the output buffer, which consists of a gain stage followed by a power stage.

Control signals flow from the SPI interface to the $\Sigma\Delta$-DAC, which generates the analog control voltages V_{BBP} and V_{BBN} applied to the VCO core. The low-leakage switches are powered separately at $V_{DD,Switches}$ and controlled via the switch disable bits to selectively isolate or connect parts of the control circuitry as needed.

This architecture leverages the unique features of the 18nm FD-SOI CMOS technology, including efficient back-gate biasing for frequency tuning. The design targets ultra-low voltage operation with precise frequency control suitable for IoT applications, and is readily integrable in mixed-signal systems.

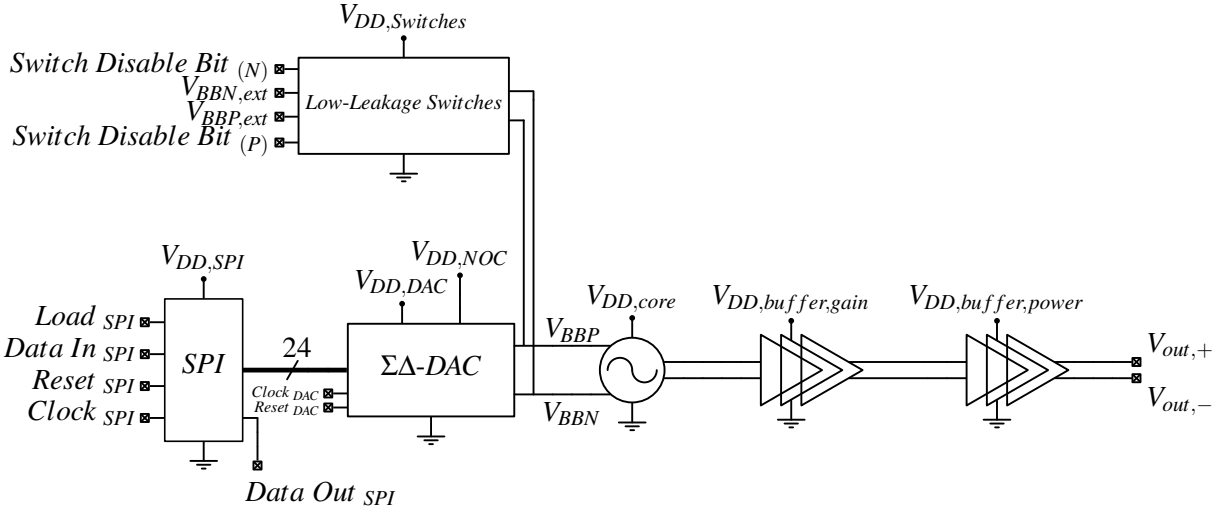


Figure 5.20: Overall architecture of the proposed circuit.

Voltage Node	$V_{DD,core}$	$V_{DD,buffer,gain}$	$V_{DD,buffer,power}$	$V_{DD,DAC}$	$V_{DD,NOC}$	$V_{DD,SPI}$	$V_{DD,Switches}$
Supply Voltage	0.6 V	0.9 V	0.9 V	0.9 V	0.9 V	0.9 V	1.8 V

Table 5.7: Supply domains associated with each functional block of the proposed circuit.

5.3.3 Circuit Design

5.3.3.1 Ring Oscillator

The proposed ring oscillator adopts a fundamentally different design approach compared to the one presented in subsection 5.2.3.2. The selected topology, shown in Figure 5.21 and based on the work in [31], embraces a digital-centric design philosophy by fixing the MOSFET channel length to the technology minimum of 18nm ($L = 18\,nm$). This choice reflects a deliberate shift towards leveraging the advantages of minimum-length devices to optimize area and speed within the constraints of ultra-low voltage operation.
Drawing upon insights gained from the previous design iteration, a stringent supply voltage specification has been established for the RF core, set at two-thirds of the nominal technology supply voltage. This results in a fixed core supply voltage $V_{DD,core}$ of 600 mV, aligning with the ULV and ULP requirements of target IoT systems in which this oscillator is intended to be integrated.
Taking into account layout constraints, carrier mobility disparities, signal symmetry considerations, and empirical observations regarding the variation of MOSFET parasitic capacitances and drive currents as a function of transistor width, a modified inverter topology is selected, as depicted in Figure 5.21. This topology aims to balance the rising and falling edges of the output signal by maintaining equal transistor widths for both NMOS and PMOS devices within the ring oscillator stages.
Contrary to the conventional approach of strengthening the PMOS transistor by increasing its width relative to the NMOS, here the NMOS transistor is deliberately weakened by effectively increasing its channel length. This is achieved by placing two identical NMOS devices in series, thereby doubling the effective channel length without introducing variability imbalance, since both devices share the same nominal length. This strategy mitigates variability-induced mismatches and contributes to improved signal symmetry and timing balance within the oscillator core.

The sizing of the inverters composing the ring oscillators is presented in Table 5.8. Each inverter stage, as shown in Figure 5.21 is made of one PMOS and two NMOS transistors of equal width ($W = 3\,\mu m$) and nominal length ($L = 18\,nm$). This choice leads to an effective length of 36 nm for the NMOS branch. The aim of this technique is to equalize the rising and falling times of the inverter, with a crossing at around 50% of the voltage dynamic (as depicted in Figure 5.22), keeping very compact transistors, avoiding to increase

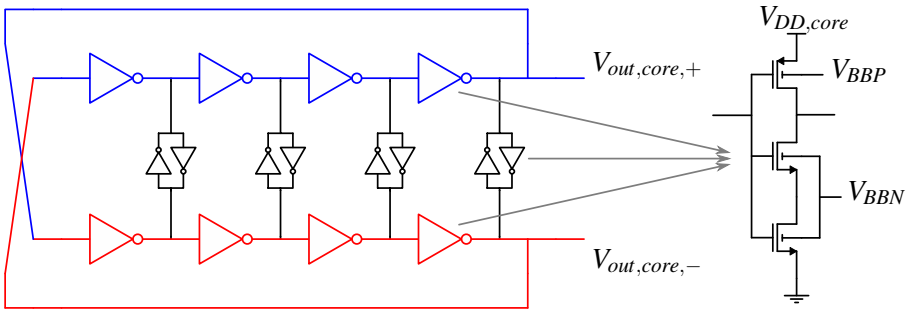


Figure 5.21: Ring oscillator core structure and the associated proposed inverter.

drastically the width of the PMOS transistor as usually made when designing inverters. It leads to a more area-efficient and power-effective cell with a natural balanced behavior between falling and rising times. Furthermore, by employing adaptive body-biasing techniques, as introduced in the previous circuit section, the inverter's nominal operating point can be finely tuned by applying 0 V to the back-gates of the transistors, optimizing the overall tunability of the circuit.

	Main Inverter	**Latch Inverter**
Length (nm)	18	18
NMOS Width (μm)	3	3
PMOS Width (μm)	3	3

Table 5.8: Geometry of the transistors composing the ring oscillator core.

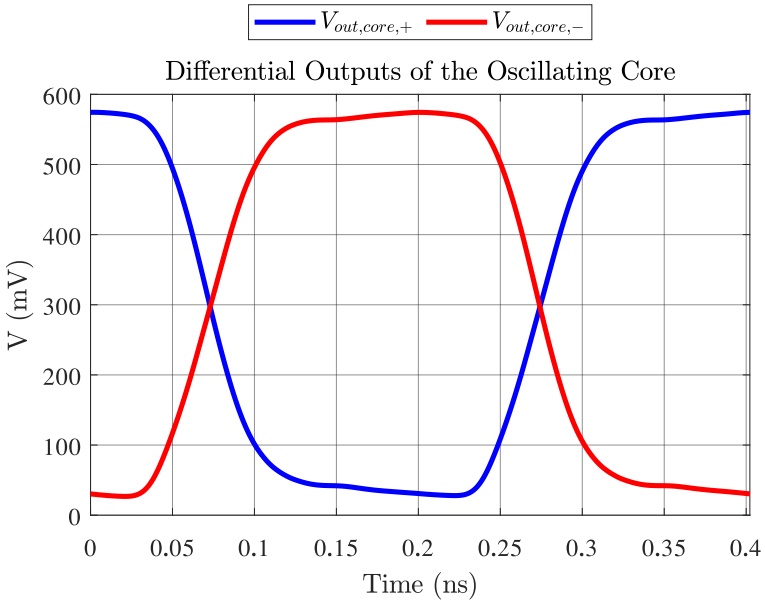


Figure 5.22: Differential outputs of the oscillating core.

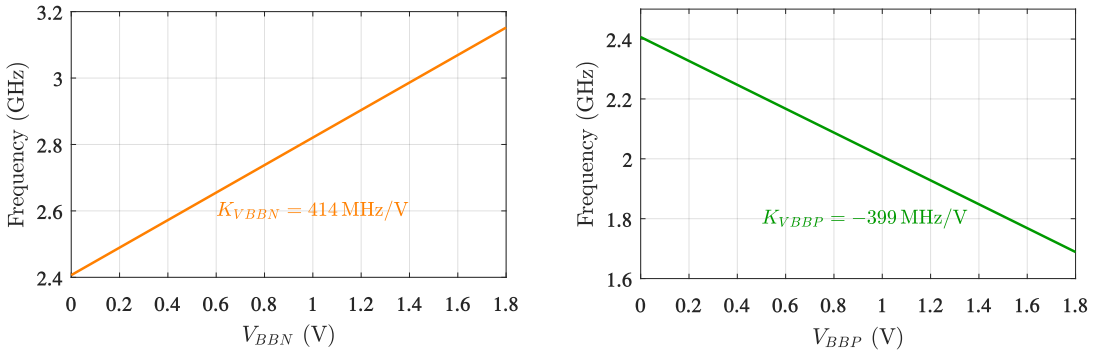


Figure 5.23: Body-bias voltage sensitivities of the proposed RVCO at a supply voltage of $V_{DD} = 0.6\,V$: (a) as a function of V_{BBN} with $V_{BBP} = 0\,V$, and (b) as a function of V_{BBP} with $V_{BBN} = 0\,V$.

5.3.3.2 ΣΔ-DAC

The digital control system consists of a ΣΔ-DAC composed of a ΣΔ modulator or PWM generator, a non-overlapping clock generator and a low-pass filter. A SPI serves as the communication interface, managing the control bitstream received from an external source, such as a microcontroller, and forwarding it to the DAC. This facilitates precise and flexible frequency tuning of the ring oscillator. The PWM generator produces a modulated digital signal representing the desired analog control voltage, while the non-overlapping clock generator ensures temporal coherence and prevents signal overlap in the switching phases. The low-pass filter, implemented as a second-order switched-capacitor network, smooths the PWM signal to generate a stable analog voltage. This voltage modulates the threshold voltages of the MOSFETs in the ring oscillator core via their back-gate terminals, enabling fine frequency control through body-biasing.

SPI Interface

To facilitate the interfacing between the oscillating core, the ΣΔ-DAC, and the control inputs provided by an external generator, a 24-bit SPI interface has been implemented, as illustrated in Figure 5.24. This SPI interface not only transmits control commands but also outputs 24-bit data words, enabling verification of correct synchronization and functional behavior of the system. In the event of communication issues, this design allows for direct adjustment of the SPI clock and the timing of the input data signals to ensure reliable operation and proper alignment between the SPI interface and the cadenced input data. The 24 bits digitally represent the body-bias voltages of the NMOS and PMOS transistors within the oscillating core, with the first 12 bits allocated to the NMOS devices and the remaining 12 bits to the PMOS devices. This design partitioning is directly dictated by the system specifications (presented in Table 5.1, which impose a digital resolution enabling

100 kHz frequency steps across a body-bias tuning range of 0 V to 0.9 V. Consequently, a 12-bit resolution per transistor type is necessary to achieve the desired least significant bit (LSB) weighting, ensuring that each digital increment corresponds to a maximum frequency deviation of 100 kHz. This resolution is implemented through an ideal DAC that provides an output voltage range from 0 V to 0.9 V, corresponding to the nominal supply voltage of the digital domain. Notably, the digital blocks are powered at 0.9 V, higher than the 0.6 V supply of the RF oscillating core. This deliberate increase in supply voltage is intended to guarantee robust operation and reliable performance of the digital cells composing the control circuitry.

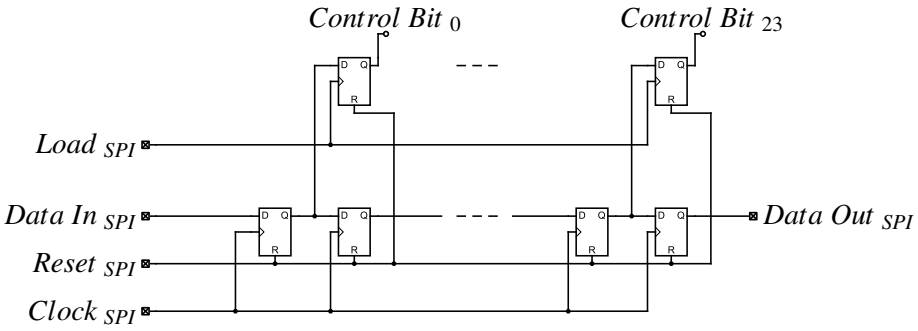


Figure 5.24: SPI architecture.

Sigma-Delta Modulator

The proposed ΣΔ-DAC architecture is composed of three principal blocks as depicted

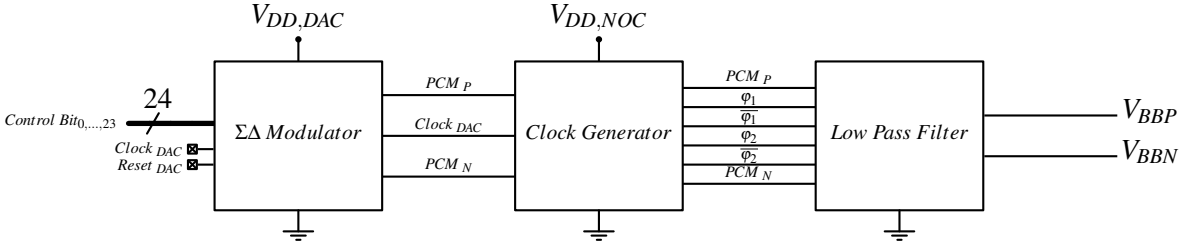


Figure 5.25: Architecture of the proposed ΣΔ DAC.

in Figure 5.25: a pulse-code (or width) modulated signal generator, corresponding to the ΣΔ modulator (Figure 5.27); a non-overlapping clock generator ensuring correct timing between switching phases (Figure 5.29); and a switched-capacitor (SC) filter performing analog reconstruction of the modulated signal (Figure 5.30).

DAC Modulator Dimensioning

As detailed in Figure 5.27, the ΣΔ modulator consists of two mirrored sub-blocks, which generate complementary PWM signals PCM_N and PCM_P. These signals encode the body-bias control voltages applied to the NMOS and PMOS transistors of the VCO core.

As presented above, each body-bias control voltage is encoded using 12 bits. This requirement results from the DAC supply voltage, $V_{DD,\mathrm{DAC}} = 0.9,\mathrm{V}$—which serves as its reference voltage—the minimum digital frequency step specification (see Table 5.1) (Max. Dig. Step = 100 kHz), and the maximum body-bias sensitivity, $\max\left(|K_{VBBN}|,|K_{VBBP}|\right) = 414\,\mathrm{MHz/V}$ as presented in Figure 5.23. To guarantee that the DAC resolution is fine enough to meet the required frequency step, the number of bits N used to encode each body-bias voltage must satisfy:

$$N \geq \log_2\left(\frac{V_{DD,\mathrm{DAC}} \times \max\left(|K_{VBBN}|,|K_{VBBP}|\right)}{\text{Max. Dig. Step}}\right) \approx 11.86. \tag{5.1}$$

Thus, a 12-bit resolution per body-bias control voltage is required.

DAC Modulator Noise Shaping

Structurally, the modulator comprises a cascade of adders and latches forming an accumulator-based feedback loop. For analytical purposes, its equivalent model is shown in Figure 5.26, where N_Q represents the quantization error introduced by the 1-bit quantizer, and $J(z)$ denotes the feedback filter transfer function responsible for shaping this quantization noise.

In the z-domain, the overall signal and noise transfer characteristics of the ΣΔ modulator

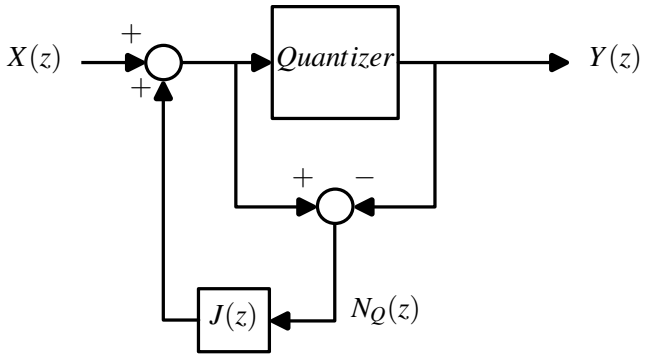


Figure 5.26: Equivalent model of the ΣΔ modulator.

can be written as:

$$Y(z) = X(z) + [J(z) - 1]N_Q(z), \tag{5.2}$$

where $X(z)$ and $Y(z)$ are the input and output spectra, respectively. If the feedback filter corresponds to a single latch, it can be modeled as a unit delay, $J(z) = z^{-1}$. Substituting this into (5.2) and applying the mapping $z = e^{j\omega T_S}$, with T_S the sampling period, gives the frequency-domain expression:

$$Y(\omega) = X(\omega) + \left[e^{j\omega T_S} - 1\right] N_Q(\omega). \tag{5.3}$$

The term in brackets describes the noise transfer function (NTF) of the modulator. Its magnitude indicates how the quantization noise is shaped in frequency:

$$|NTF(\omega)|^2 = \left|\frac{Y(\omega)}{N_Q(\omega)}\right|^2 = 2-2\cos(\omega T_S) = 4\sin^2(\omega T_S) = 4\sin^2\left(\pi\frac{f}{f_S}\right), \qquad (5.4)$$

where $f_S = 1/T_S$ is the sampling frequency. The squared magnitude of the NTF as a function of f/f_S is plotted in Figure 5.28. The curve exhibits a 20 dB/decade slope, confirming that the proposed modulator implements a first-order noise shaping, which pushes the quantization noise toward higher frequencies. Consequently, the SC low-pass filter following the modulator should efficiently remove this out-of-band noise, improving the effective resolution of the reconstructed analog signal.

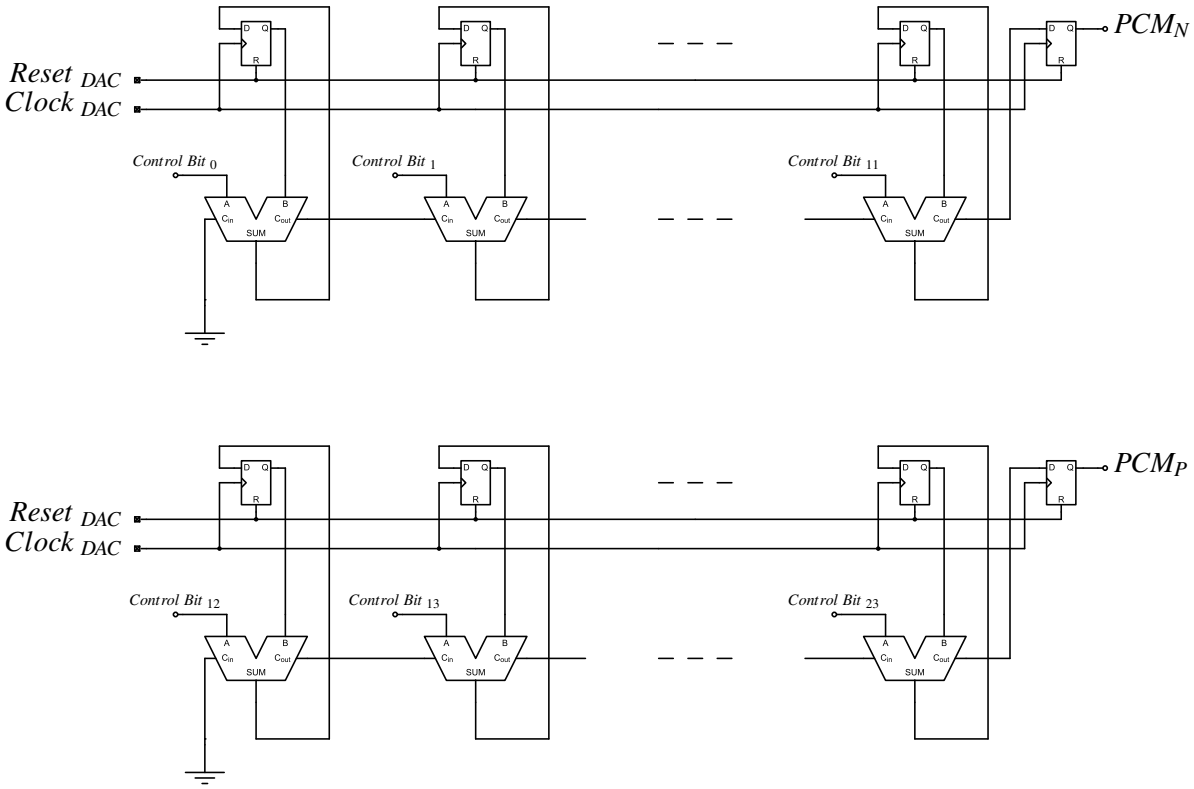


Figure 5.27: ΣΔ modulator.

Switched-Capacitor Filter

The switched-capacitor (SC) filter stage performs the analog reconstruction of the pulse-coded modulation (PCM) signals generated by the ΣΔ modulator. As the modulator is duplicated for the generation of PCM_N and PCM_P, two mirrored SC filters are implemented to independently process these signals and generate the body-bias control voltages V_{BBN} and V_{BBP} applied to the NMOS and PMOS transistors of the VCO core. The complete

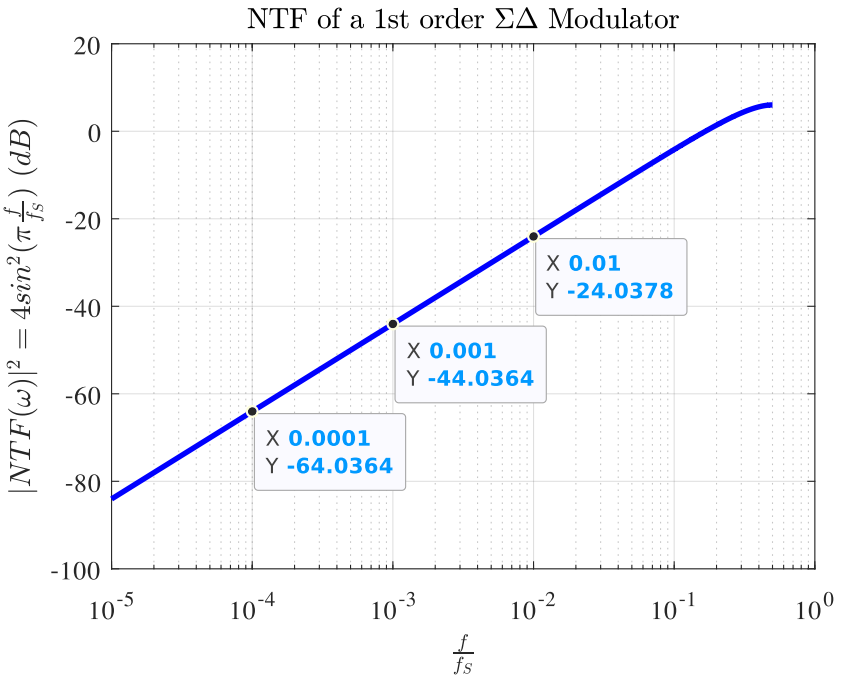


Figure 5.28: Power of the noise transfer to the output function of the proposed 1st order ΣΔ modulator.

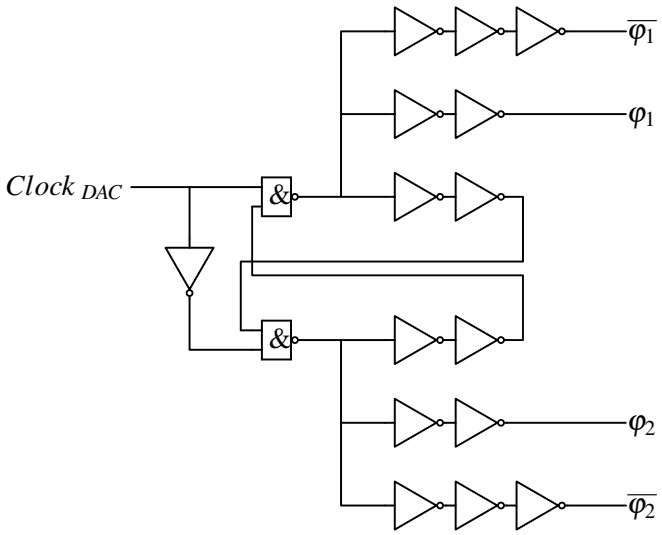


Figure 5.29: Non-overlapping clock generator architecture.

architecture of one filter branch is shown in Figure 5.30.

Each SC filter consists of two consecutive first-order low-pass stages clocked by the non-overlapping phases Φ_1 and Φ_2 generated by the circuit of Figure 5.29. During phase Φ_1, the input voltage is sampled onto a small capacitor $C_S = 50$ fF; during phase Φ_2, the stored charge is transferred to a larger integrating capacitor C_F (5 pF for the first stage and 25 pF for the second). This periodic charge redistribution emulates a continuous-time

RC filter with an equivalent resistance

$$R_{\text{eq}} = \frac{T_S}{C_S}, \tag{5.5}$$

where $T_S = 1/f_S$ is the clock period. The approximate single-stage cutoff frequency is therefore

$$f_{\text{c}} \approx \frac{1}{2\pi R_{\text{eq}} C_F} = \frac{C_S}{2\pi T_S C_F}. \tag{5.6}$$

For a 10 MHz sampling clock, the two stages present characteristic pole frequencies of about $f_{p1} = 15.8$ kHz and $f_{p2} = 3.2$ kHz, producing an overall -3 dB bandwidth near $f_{3\,\text{dB}} \approx 3.3$ kHz.

It must be noted, however, that these values assume that the two sections are perfectly isolated. In practice, no active buffer separates the stages, and charge is exchanged between them during the sampling phase Φ_1, when the sampling capacitor C_{S2} of the second stage loads the output node of the first. Consequently, the overall transfer function cannot be written as the simple product $H(z) = H_1(z)H_2(z)$, since both stages are dynamically coupled. Charge conservation for the two stages leads to the coupled discrete-time system

$$\begin{aligned} (C_{S1} + C_{F1})V_1[n] &= C_{F1}V_1[n-1] + C_{S1}V_{in}[n] - C_{S2}\big(V_1[n] - V_2[n-1]\big), \\ (C_{S2} + C_{F2})V_2[n] &= C_{F2}V_2[n-1] + C_{S2}V_1[n], \end{aligned} \tag{5.7}$$

which, after z-transformation and algebraic rearrangement, yields the non-separable second-order transfer function

$$H(z) = \frac{V_2(z)}{V_{in}(z)} = \frac{C_{S1}C_{S2}z^{-1}(1 - z^{-1})}{\big(C_{S2} + C_{F2} - C_{F2}z^{-1}\big)\big(C_{S1} + C_{F1} + C_{S2} - C_{F1}z^{-1}\big) - C_{S2}^2 z^{-1}}. \tag{5.8}$$

The cross-term $-C_{S2}^2 z^{-1}$ in the denominator represents the inter-stage charge sharing that couples the dynamics of both stages. When $C_{S2} \ll C_{F1}$, this term is small and the cascade approximation remains valid; otherwise, it slightly lowers the effective cutoff frequency and modifies the damping. Circuit-level transient simulations confirm a -3 dB bandwidth of approximately 2.9 kHz for the coupled case, compared with 3.3 kHz predicted by the ideal cascade, consistent with a minor pole shift of roughly 10%.

Overall, the dual SC filter branches implement a second-order low-pass response with about -12 dB/octave out-of-band attenuation, as depicted in Figure 5.31. They effectively suppress the high-frequency quantization noise shaped by the $\Sigma\Delta$ modulator and provide stable, low-ripple body-bias voltages V_{BBN} and V_{BBP} for the VCO core.

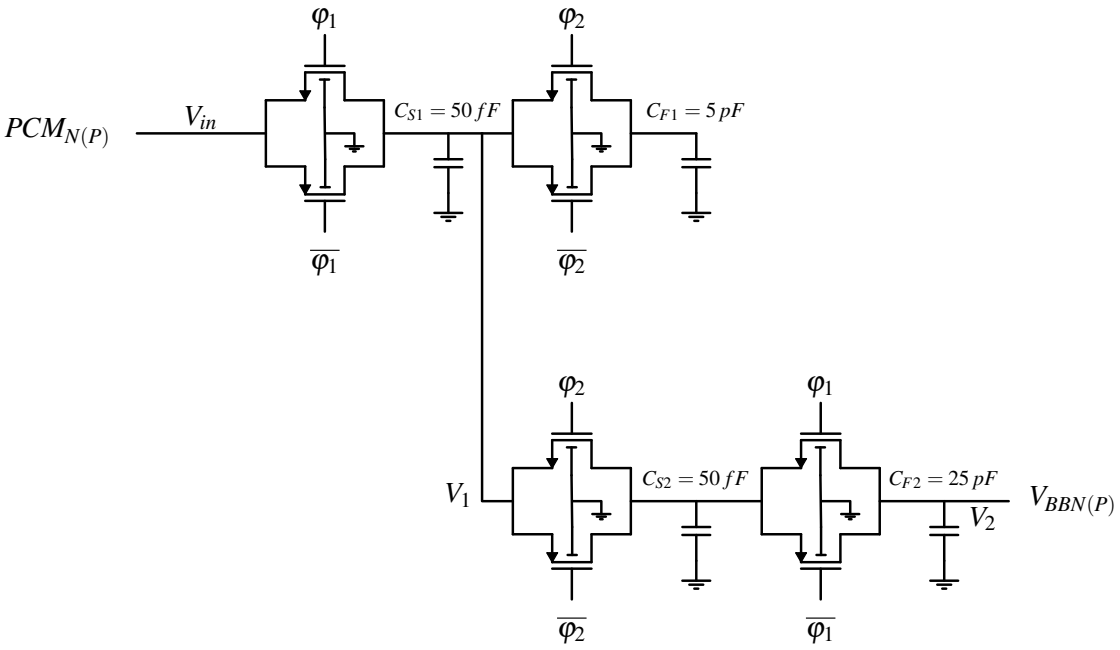


Figure 5.30: Switched-capacitor filter architecture implementing the reconstruction of the ΣΔ-DAC outputs PCM_N and PCM_P into the body-bias control voltages V_{BBN} and V_{BBP}.

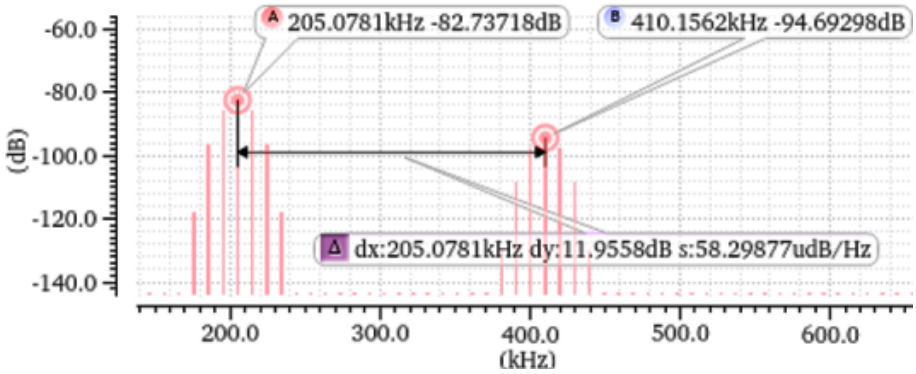


Figure 5.31: Frequency response of the proposed SC filter, showing an attenuation close to -12 dB/octave, which confirms the expected second-order characteristic of the transfer function nature.

5.3.3.3 Output Buffers

The output buffer stage, illustrated in Figure 5.32, ensures proper delivery of the differential oscillating signals generated by the VCO core to the measurement interface and the external 50 Ω loads. Each buffer branch consists of a cascade of CMOS inverters with progressively increasing transistor widths, as summarized in Table 5.9. This tapered structure minimizes propagation delay and dynamic power consumption while providing the required current drive to achieve an output power of approximately -3 dBm into a 50 Ω load.

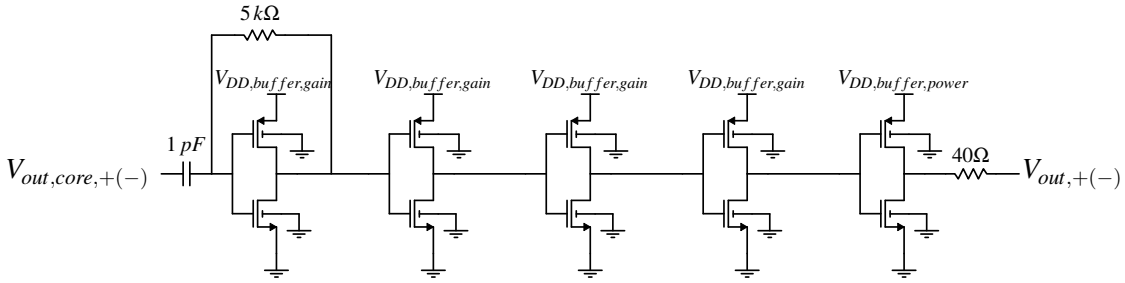


Figure 5.32: Output buffer architecture including the auto-zero interface and tapered inverter chain for each differential branch.

Table 5.9: Transistor dimensions of the output buffer inverter stages.

Buffer Stage	NMOS Width (µm)	PMOS Width (µm)
1	3	4
2	6	8
3	12	16
4	24	32
5	24	32

Auto-zero Interface

Each differential buffer chain begins with an auto-zero RC interface followed by the first inverter; one such chain is implemented per differential branch. This RC–inverter stage provides the voltage-domain transition between the VCO core supplied at $V_{DD,\text{core}} = 0.6$ V and the output buffer domain powered at $V_{DD,\text{buffer}} = 0.9$ V. It also performs DC restoration of the oscillating signal around the inverter's switching threshold and isolates the sensitive core from the switching activity of the subsequent buffer stages (see Figure 5.33).

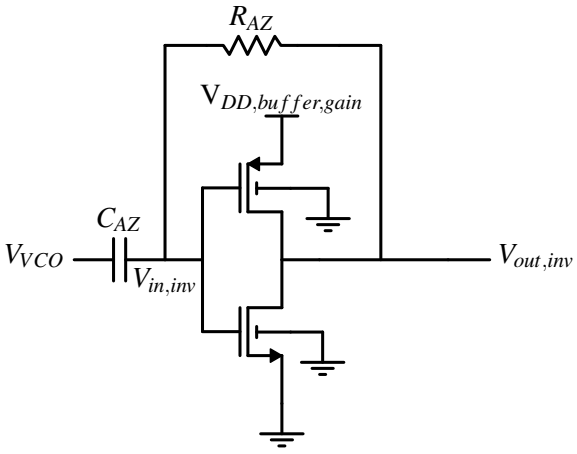


Figure 5.33: Schematic of the auto-zero RC interface and first inverter stage providing level adaptation between the 0.6 V VCO core and the 0.9 V output buffer domain.

The auto-zero network is realized as a series coupling capacitor C_{AZ} feeding an input

node biased to the 0.9 V domain through a resistor R_{AZ}. Its small-signal transfer function corresponds to a first-order high-pass filter:

$$H_{AZ}(s) = \frac{V_{in,inv}(s)}{V_{VCO}(s)} = \frac{sR_{AZ}C_{AZ}}{1+sR_{AZ}C_{AZ}}, \tag{5.9}$$

with cutoff frequency

$$f_{AZ} = \frac{1}{2\pi R_{AZ}C_{AZ}}. \tag{5.10}$$

For the implemented design, $R_{AZ} = 5$ kΩ and $C_{AZ} = 1$ pF, which gives:

$$R_{AZ}C_{AZ} = 5\times10^{-9}\ \text{s}, \qquad f_{AZ} = \frac{1}{2\pi\times5\times10^{-9}} \approx 31.8\ \text{MHz}.$$

Given that the oscillation frequency is $f_{osc} = 2.4$ GHz, the auto-zero stage passes the carrier with negligible attenuation since $\omega_{osc}R_{AZ}C_{AZ} \gg 1$. The magnitude response at the oscillation tone is:

$$|H_{AZ}(j\omega_{osc})| = \frac{\omega_{osc}R_{AZ}C_{AZ}}{\sqrt{1+(\omega_{osc}R_{AZ}C_{AZ})^2}} \approx 1,$$

confirming that the AC amplitude is preserved while DC and low-frequency components are effectively removed. The chosen values ensure (i) a cutoff more than one decade below the oscillation frequency, (ii) high input impedance to limit VCO loading, and (iii) correct biasing of the first inverter in the 0.9 V domain.

Tapered Inverter Chain and Output Matching

Following the auto-zero interface, the first inverter restores full logic swing and isolates the VCO from the higher-voltage domain. Subsequent inverter stages are progressively up-scaled in transistor width to increase drive strength while maintaining signal integrity. The transistor dimensions of each stage are reported in Table 5.9.

The final inverter in each chain directly drives the measurement environment. Its intrinsic output resistance is approximately $R_{inv} = 10\ \Omega$, and a $R_{series} = 40\ \Omega$ on-chip resistor is placed in series to achieve the desired source impedance:

$$R_{source} = R_{inv} + R_{series} \approx 10\ \Omega + 40\ \Omega = 50\ \Omega.$$

This configuration provides proper impedance matching with the external 50 Ω measurement setup, minimizing reflections and ensuring accurate power delivery. The 40 Ω resistor also damps output transients and protects the final inverter against load-induced overstress.

The differential nature of the oscillator output requires two mirrored buffer chains, each

beginning with its own auto-zero stage, ensuring symmetry and minimal even-order distortion. The complete output buffer chain thus achieves (i) level shifting and DC restoration between 0.6 V and 0.9 V domains, (ii) preservation of signal amplitude and phase integrity, (iii) robust 50 Ω matching, and (iv) isolation of the VCO core from load perturbations. These features guarantee faithful extraction of phase noise and output power during measurements without distortion or bias interference.

5.3.4 Layout Implementation

Building upon the layout strategy established for the previously presented circuit and following the same methodological principles outlined in section 5.2.4, this section details the physical implementation of the blocks composing the proposed circuit which top schematic is depicted in Figure 5.34.

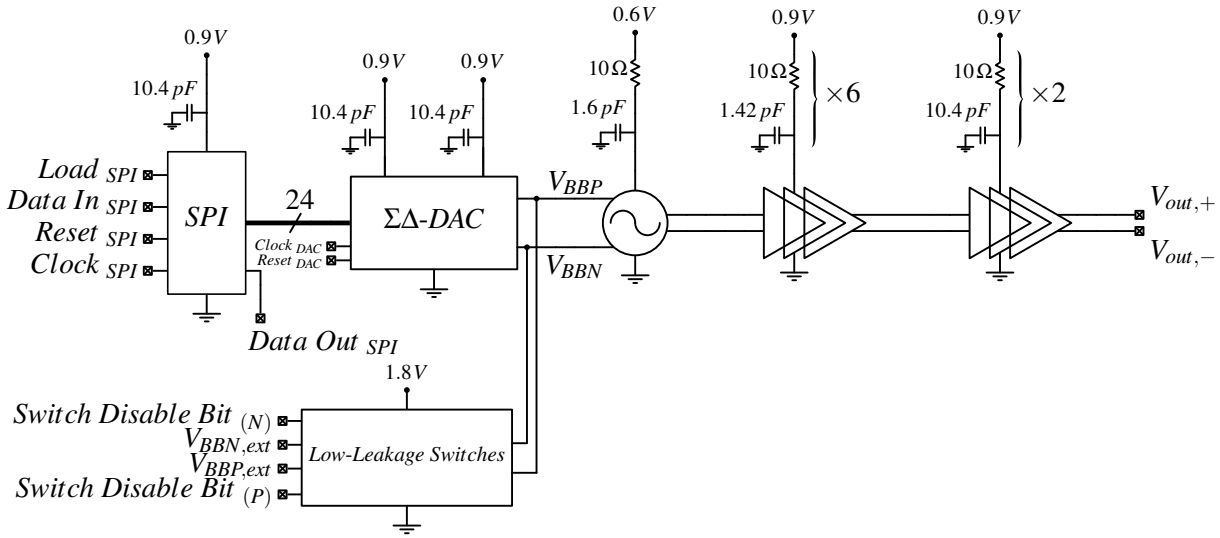


Figure 5.34: Top schematic of the proposed circuit.

5.3.4.1 Ring Oscillator

As presented in Figure 5.35, the layout of the proposed ring oscillator was designed to preserve symmetry and timing balance between the differential paths while minimizing parasitic effects that could degrade phase noise performance. The layout follows a ring-based organization, where the main inverters are placed at the center of the structure, and the auxiliary inverters are symmetrically distributed along the north and south sides. The VCO core alone occupies an area of 14 μm × 9 μm, corresponding to a total of 126 μm^2. Each delay cell is arranged in a fully symmetrical configuration to ensure matched routing lengths and equivalent parasitic loading on both branches of the pseudo-differential structure. Flipped wells were used for NMOS devices to enable independent back-gate biasing, whereas regular wells were maintained for PMOS transistors, consistent with the

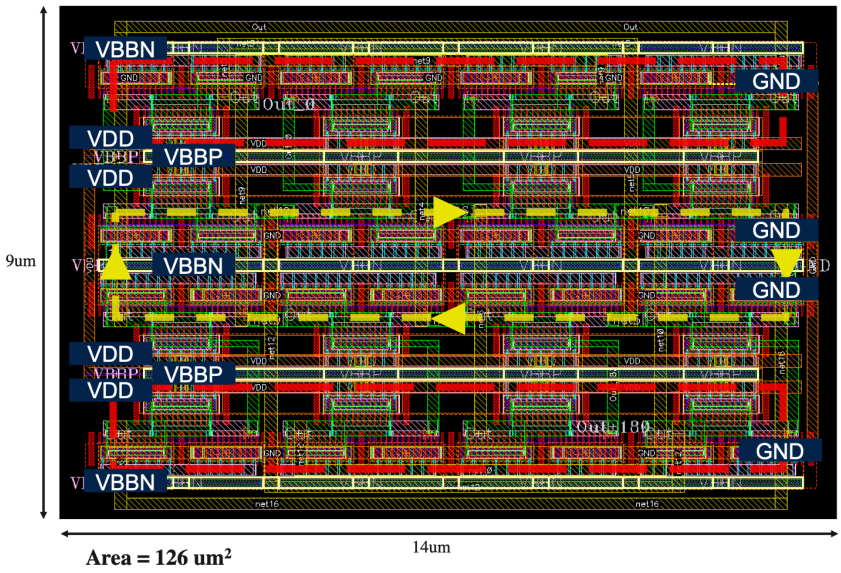


Figure 5.35: Layout of the VCO core following a ring-based organization. The main inverters are placed at the center of the structure, while the auxiliary inverters are symmetrically distributed along the north and south sides.

adopted body-biasing scheme.

As shown in Figure 5.36, local decoupling capacitors were placed close to the supply nodes of each delay cell to stabilize the supply voltage and suppress noise coupling. A total decoupling capacitance of 1.6 pF is integrated as close as possible to the VCO core, bringing the total area of the complete block to 20 μm $\times$ 40 μm (800 μm^2).

The resulting layout minimizes delay mismatch between differential paths and ensures robust phase-noise performance under low-voltage operation.

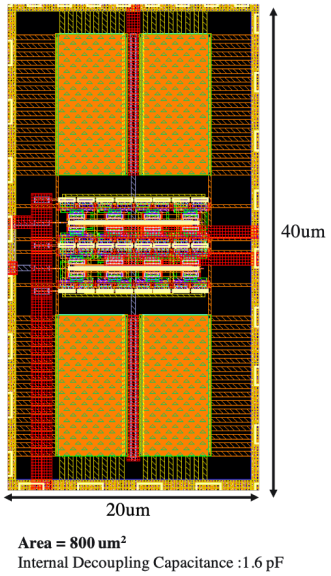


Figure 5.36: Layout of the VCO core including its locally integrated decoupling capacitors, positioned near the supply nodes to stabilize the voltage suuply.

5.3.4.2 Pad Ring & ESD Strategy

As illustrated in Figure 5.37, the implemented pad ring comprises 48 pads, arranged symmetrically with 12 pads on each side of the die. The pad ring was carefully organized to partition the different supply domains in order to minimize coupling phenomena between functional blocks. Each supply region is clearly annotated, and the control signals associated with each block are routed within their respective power domains to ensure proper isolation and reduce substrate noise propagation.

As visible in Figure 5.37, the overall signal flow progresses naturally from left to right across the die—from the digital inputs and SPI interface located on the left-hand side to the power-stage buffer outputs positioned on the far right.

Electrostatic discharge protection was implemented using diode-based voltage clamps. Three fixed-voltage rings are distributed beneath the pad ring, biased at 0 V, 0.9 V, and 3.3 V, respectively. This configuration ensures that all circuit blocks are protected against overvoltage events originating from measurement equipment or electrostatic discharges.

The complete pad ring occupies an area of 1100 μm $\times$ 1100 μm, corresponding to a total area of 1.21 mm^2.

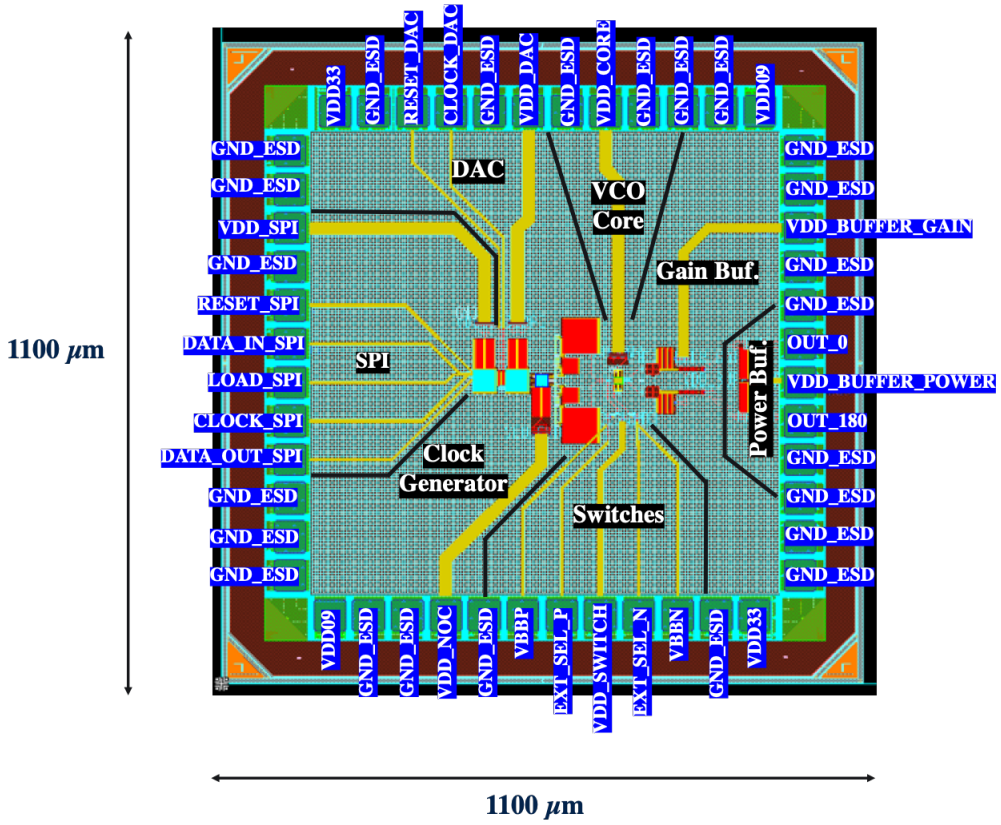


Figure 5.37: Layout of the implemented pad ring showing the different supply domains. The power zones are organized to minimize coupling between functional blocks.

5.3.4.3 Digital Control System

The layout of the digital control system comprises four main blocks: the SPI interface, the ΣΔ modulator, the clock generator, and the switched-capacitor filter. The first three blocks were implemented in layout using standard-cell libraries and digital design tools, whereas the switched-capacitor filter was manually laid out following the same methodology as the other analog/RF blocks. The corresponding layout of each digital block is presented in Appendix A.

Each layout includes a guard ring surrounding the entire core to ensure electrical isolation from adjacent circuitry and reduce substrate coupling. A dedicated power grid was implemented to uniformly distribute the supply voltage across the standard cells composing each block. The switched-capacitor filter constitutes the only analog block within the digital control system and was therefore laid out following analog design practices to ensure parasitic control.

As shown in Figure 5.38, the layout adopts a symmetric organization between the PCM_N and PCM_P signal paths. The CMOS pass-gate switches were placed in close proximity to their associated capacitors to minimize routing parasitics and charge injection effects. The overall layout of the switched-capacitor filter occupies an area of 17 600 μm^2 (80 μm $\times$ 220 μm).

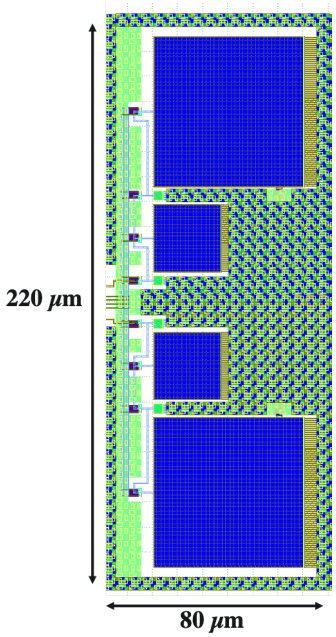


Figure 5.38: Layout of the switched-capacitor filter core. The layout exhibits a symmetric structure between the PCM_N and PCM_P paths.

5.3.4.4 Output Buffers

As shown in Figure 5.39, the output buffers are divided into two functional blocks: the gain stage—comprising the auto-zero interface and the first four inverters of the tapered chain—located on the left; and the power stage with its output resistance network—located on the right. These two blocks are duplicated and symmetrically positioned with respect to the horizontal mid-axis of the die to minimize mismatch between the differential output paths, thereby reducing phase jitter and ensuring waveform balance.

Each inverter stage is equipped with its own local decoupling capacitors, except for the first two inverters of the gain stage, which share a common set of capacitors for layout compactness.

The gain stage and its auto-zero interface are highlighted in Figure 5.40, while Figure 5.41 focuses on the power stage and its output resistance network.

The gain stage, including its auto-zero interface, occupies an area of 5 250 μm^2 (105 μm $\times$ 50 μm), whereas the power stage occupies 3 750 μm^2 (50 μm $\times$ 75 μm), both including their associated decoupling capacitors. The total area of the complete output buffer structure amounts to 32 250 μm^2 (215 μm $\times$ 150 μm).

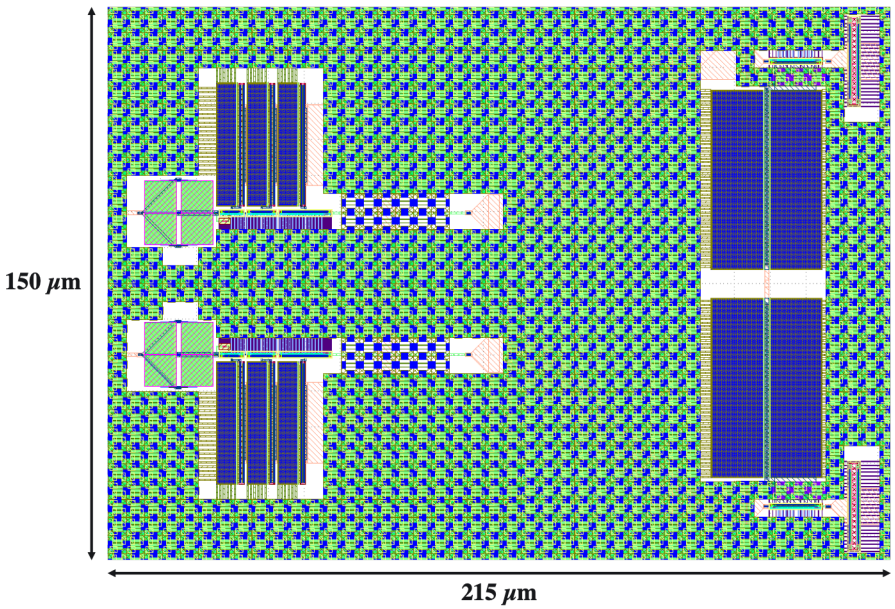


Figure 5.39: Overall layout of the output buffers. The layout comprises two replicated buffer chains symmetrically positioned with respect to the horizontal mid-axis of the die. Two distinct functional regions can be identified: the gain stage with its auto-zero interface on the left, and the power stage with its output resistance network on the right.

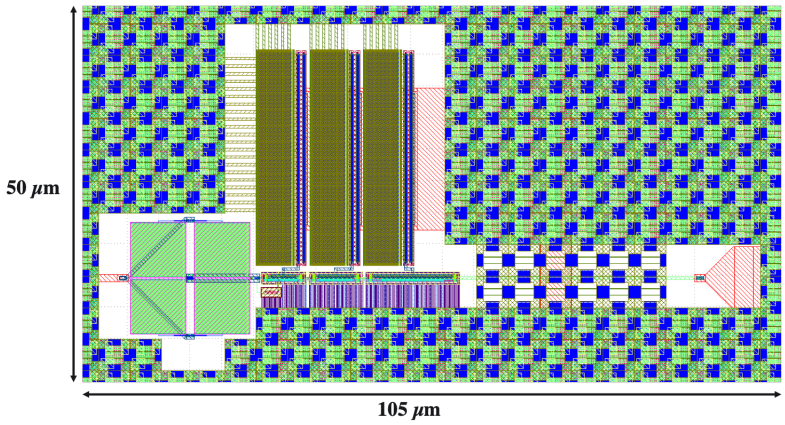


Figure 5.40: Layout of the gain stage and its auto-zero interface, responsible for ensuring symmetry and minimizing offset prior to amplification.

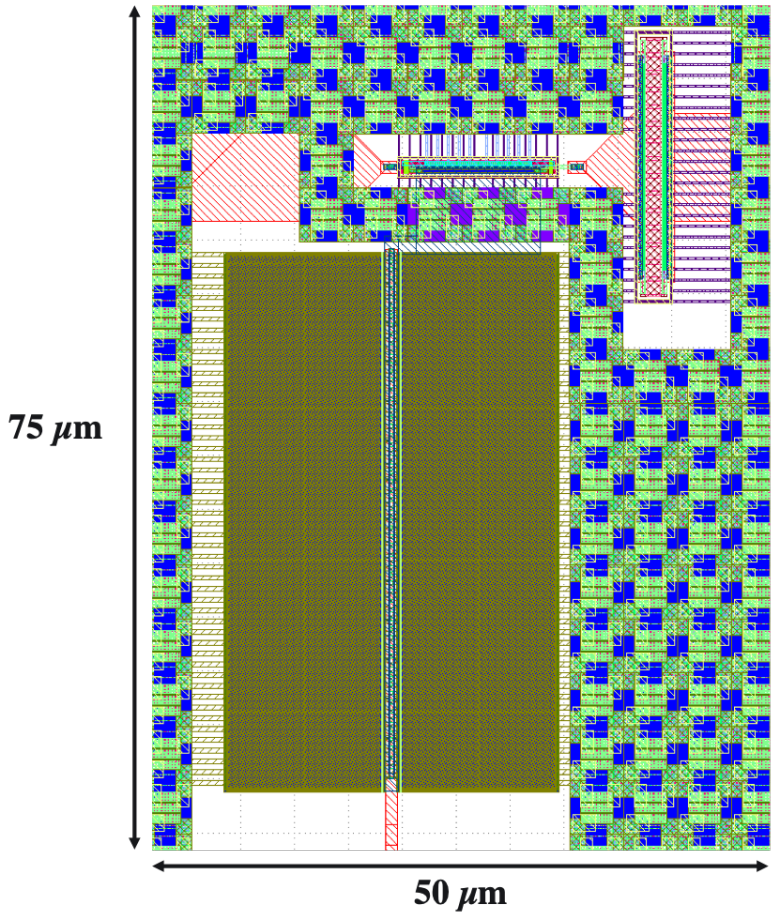


Figure 5.41: Layout of the power stage and its output resistance network, designed to provide the required drive capability for off-chip measurements.

5.3.4.5 Overall Layout

The complete layout of the proposed circuit is presented in Figure 5.42. The chip integrates all functional blocks described in the previous subsections — the pseudo-differential

ring VCO core, its output buffers, and the digital control system composed of the SPI interface, ΣΔ modulator, clock generator, and switched-capacitor filter — within a compact floorplan optimized for symmetry and noise isolation.

The analog/RF section, including the VCO core and the output buffers, is placed on the right-hand side of the die to minimize coupling from the digital control circuitry. Conversely, the digital control blocks are grouped on the left-hand side. Dedicated supply rails and decoupling capacitors have been strategically distributed throughout the layout to maintain stable operation and reduce supply-induced jitter.

Routing of critical signals — such as the differential oscillator outputs and body-bias control lines — has been kept fully symmetric to preserve timing balance and reduce parasitic mismatch. The clock and control signals distributed from the digital section to the analog one are routed through shielded interconnects to limit capacitive coupling.

As shown in Figure 5.42, the overall layout exhibits a high level of regularity and modularity, easing future design scalability or block reuse.

The complete die measures 1100 μm × 1100 μm, corresponding to a total area of 1.21 mm^2 including the pad ring and ESD structures, and is currently being fabricated at the time of writing this manuscript.

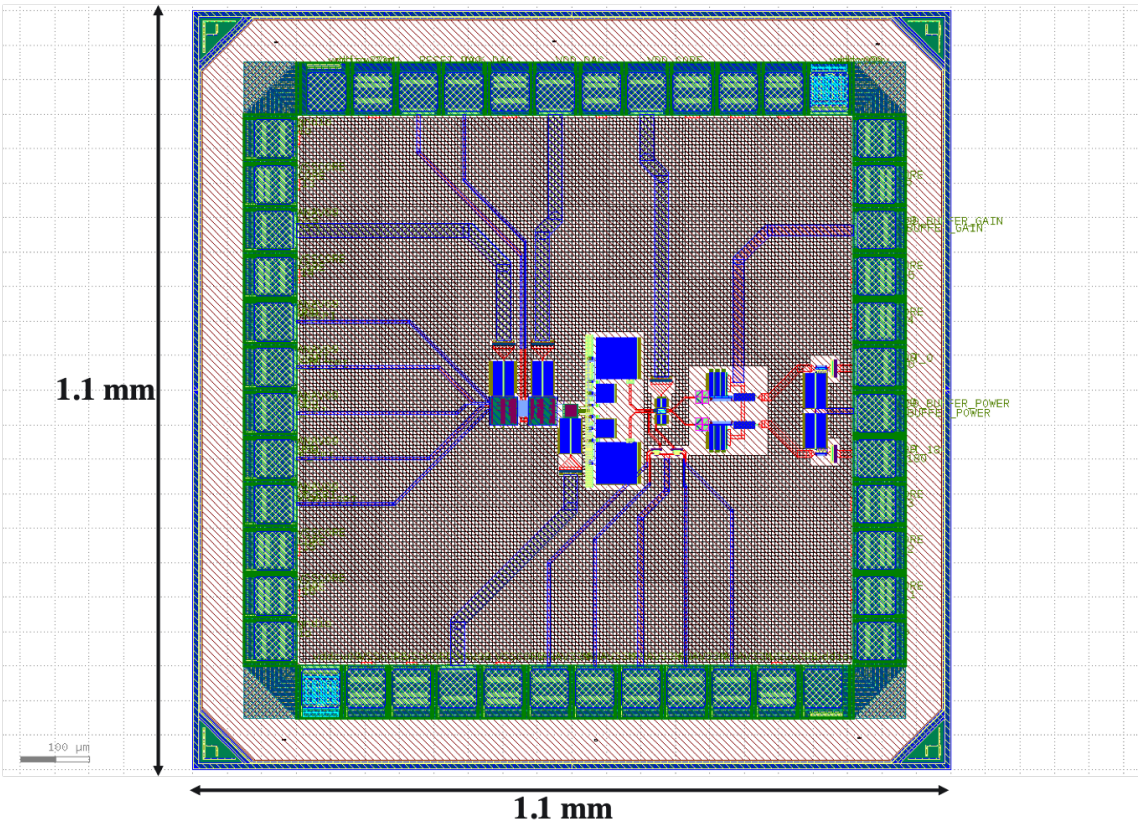


Figure 5.42: Top-level layout of the complete MPW6 circuit integrating all analog and digital sub-blocks. The analog/RF section is placed on the right-hand side, while the digital control system occupies the left-hand side of the die.

5.3.5 Circuit Testability

This section presents the testability framework for the proposed circuit. Figure 5.43 illustrates the top-level schematic of the full system, highlighting the different inputs and outputs as well as that the different supply domains.

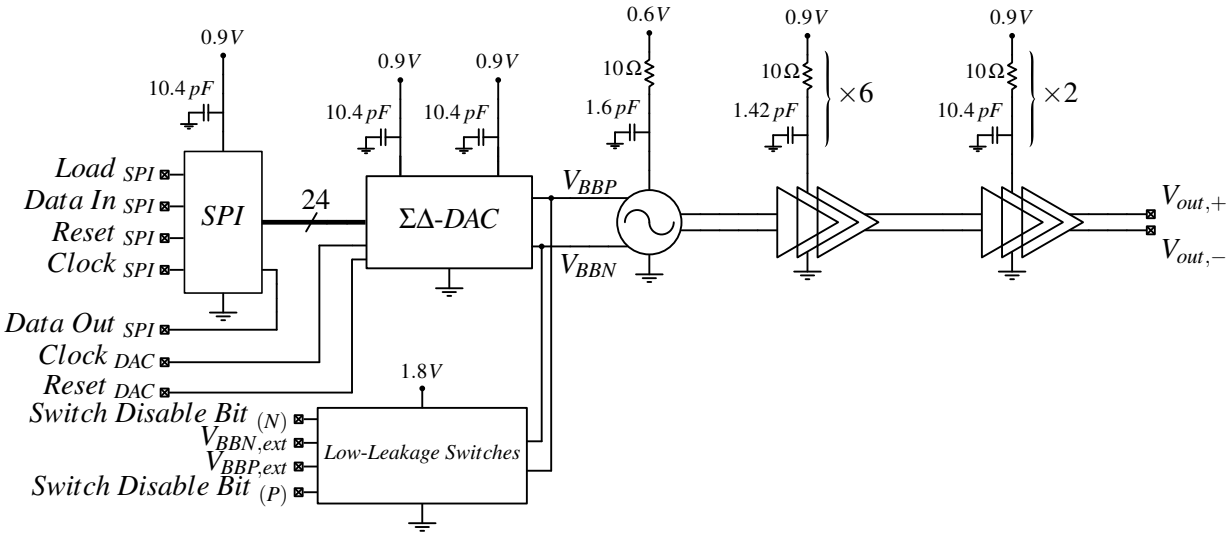


Figure 5.43: Top schematic of the proposed circuit.

In the case of analog body-biasing through the low-leakage switches, the SPI and the ΣΔ-DAC must remain unpowered. In this operating mode, both *Switch Disable Bit* $_{(N)}$ and *Switch Disable Bit* $_{(P)}$ must be set to '0', enabling external control of the body-bias voltages. The external nodes $V_{BBN,ext}$ and $V_{BBP,ext}$ can then be driven within the range 0 V to 0.9 V.

In the case of digital control through the SPI and the ΣΔ-DAC, the low-leakage switches must remain powered at 1.8 V, and both $Switch\ Disable\ Bit_{(N)}$ and $Switch\ Disable\ Bit_{(P)}$ must be set to '1'. The signals $Clock_{SPI}$ and $Clock_{DAC}$ should be operated at a frequency of 10 MHz with a voltage swing between 0 V and 0.9 V. In addition, the $Reset_{DAC}$ bit must be set to '0' to enable normal DAC operation.

The data transmission to the SPI must follow the timing diagram shown in Figure 5.44. At initialization, the $Reset_{SPI}$ signal shall be asserted to '1'. The $Load_{SPI}$ signal must remain at '0' during the shifting operation. The input data stream $Data\ In_{SPI}$ must be clocked synchronously with $Clock_{SPI}$, and the data loading sequence begins on the first rising edge of $Clock_{SPI}$ following the de-assertion of $Reset_{SPI}$ from '1' to '0'.

To guarantee correct transfer of the 24-bit word toward the DAC modulator, $Load_{SPI}$ must toggle from '0' to '1' after exactly 24 clock rising edges, and remain high for one full clock period before returning to '0'.

The data stream $Data\ In_{SPI}$ must be transmitted in the following order (first to last):

1. the 12 control bits associated with V_{BBN}, from the MSB ($Control\ Bit_{(0)}$) to the LSB ($Control\ Bit_{(11)}$), followed by

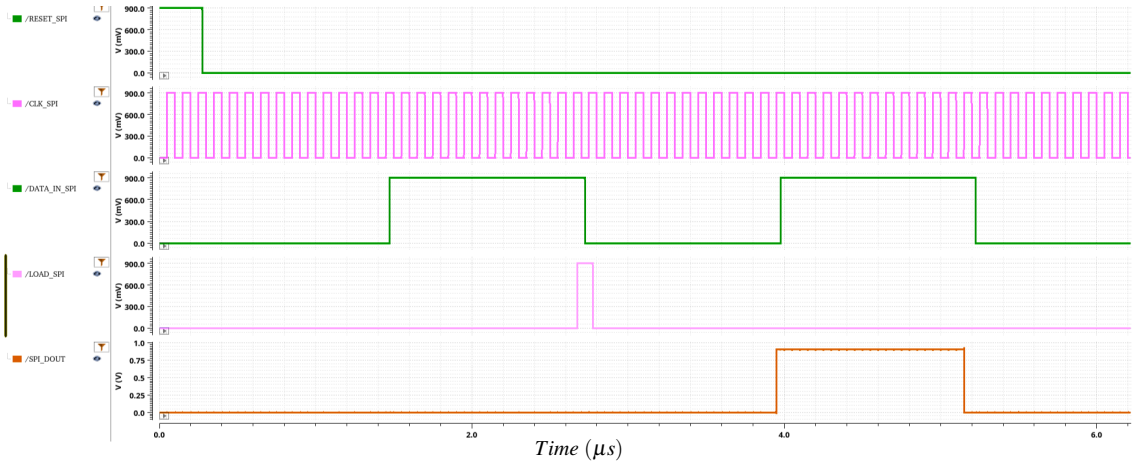


Figure 5.44: Timing diagram presenting data transmission across the SPI.

2. the 12 control bits associated with V_{BBP}, from the MSB ($Control\,Bit_{(12)}$) to the LSB ($Control\,Bit_{(23)}$).

Accordingly, the digital-to-analog truth tables for V_{BBN} and V_{BBP} are:

$$V_{BBN} = \frac{V_{DD,DAC}}{2^{12}} \sum_{i=0}^{11} Control\,Bit_i \cdot 2^{11-i}, \tag{5.11}$$

$$V_{BBP} = \frac{V_{DD,DAC}}{2^{12}} \sum_{i=12}^{23} Control\,Bit_i \cdot 2^{23-i}. \tag{5.12}$$

5.3.6 Results, Discussion, and Benchmarking

The performance of the proposed circuit was evaluated through post-layout simulations to first assess its frequency tuning characteristics. Figures 5.45 and 5.46 summarize the simulated oscillation frequency as a function of the back-gate bias voltages applied to the NMOS and PMOS transistors, respectively. Figure 5.45 presents the variation of the oscillation frequency with V_{BBN} for a fixed PMOS back-gate bias of $V_{\mathrm{BBP}} = 0$ V (0000 0000 0000) and a core supply voltage of $V_{\mathrm{DD,core}} = 0.6$ V, corresponding to two-thirds of the nominal supply voltage of the technology. The resulting tuning sensitivity is $K_{\mathrm{VBBN}} = 414$ MHz/V. Figure 5.46 shows the complementary tuning characteristic obtained when varying the PMOS back-gate voltage V_{BBP}, with V_{BBN} fixed at 0 V (0000 0000 0000) and the same core supply voltage of 0.6 V. The associated tuning sensitivity is $K_{\mathrm{VBBP}} = -399$ MHz/V. The achieved minimum and maximum frequencies are summarized in Table 5.10. Overall, the combined tuning mechanisms allow the oscillator to achieve a total frequency tuning range of 30.2%, demonstrating again the effectiveness of the adaptive body-bias-based frequency control in 18nm FD-SOI CMOS technology.

Table 5.10: Minimum and maximum oscillation frequencies obtained from back-gate tuning of the proposed VCO at $V_{\mathrm{DD,core}} = 0.6$ V.

Tuning Knob	Digital Code	Frequency (GHz)	Condition
V_{BBN} (with $V_{\mathrm{BBP}} = 0$ V : 0000 0000 0000)	0000 0000 0000	2.407	$f_{\min}$
	1111 1111 1111	2.780	$f_{\max}$
V_{BBP} (with $V_{\mathrm{BBN}} = 0$ V : 0000 0000 0000)	0000 0000 0000	2.407	$f_{\max}$
	1111 1111 1111	2.050	$f_{\min}$

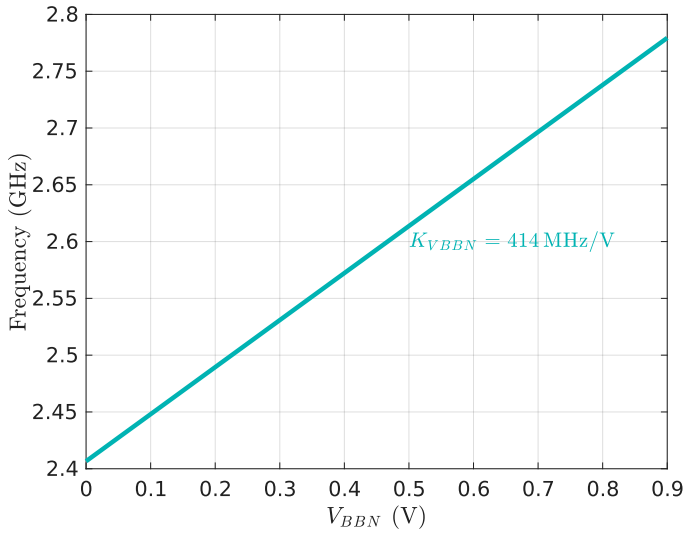


Figure 5.45: Post-layout simulated oscillation frequency as a function of body-bias voltage $\mathrm{V_{BBN}}$ *for a fixed* $\mathrm{V_{BBP}} = 0\,\mathrm{V}$ *and* $V_{\mathrm{DD,core}} = 0.6\,\mathrm{V}$. *Simulations were performed under the typical process corner.*

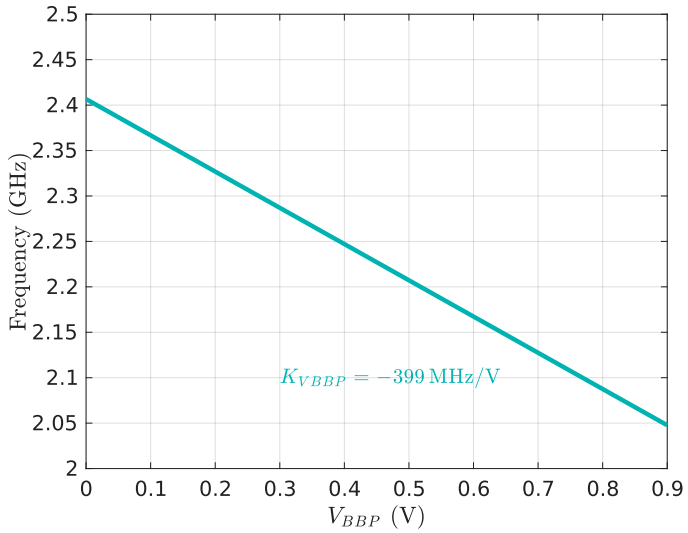


Figure 5.46: Post-layout simulated oscillation frequency as a function of body-bias voltage $\mathrm{V_{BBP}}$ *for a fixed* $\mathrm{V_{BBN}} = 0\,\mathrm{V}$ *and* $V_{\mathrm{DD,core}} = 0.6\,\mathrm{V}$. *Simulations were performed under the typical process corner.*

The phase noise performance of the proposed oscillator was evaluated through post-layout simulations, as illustrated in Figure 5.47. The simulations were performed at an oscillation frequency of 2.407 GHz with a core supply voltage of $V_{\mathrm{DD,core}} = 0.6$ V. The obtained phase noise spectrum exhibits the expected $1/f^2$ dependence characteristic of thermal noise-dominated regions, confirming stable oscillation and consistent biasing across the inverter stages. The simulated phase noise reaches -82.2 dBc/Hz at a 1 MHz offset and -115.1 dBc/Hz at 20 MHz offset. These results demonstrate the good noise performance achievable under low-voltage operation in 18nm FD-SOI CMOS technology, validating the robustness of the body-bias-based tuning architecture and the effectiveness of the adopted layout symmetry in minimizing phase noise degradation. Considering the different design choices compared to the circuit presented in section 5.2, this phase noise metric was arguably the most challenging to maintain or improve. Indeed, as discussed in [28], both the reduction of the channel length and the supply voltage inherently degrade phase noise performance due to increased device noise and reduced signal swing.

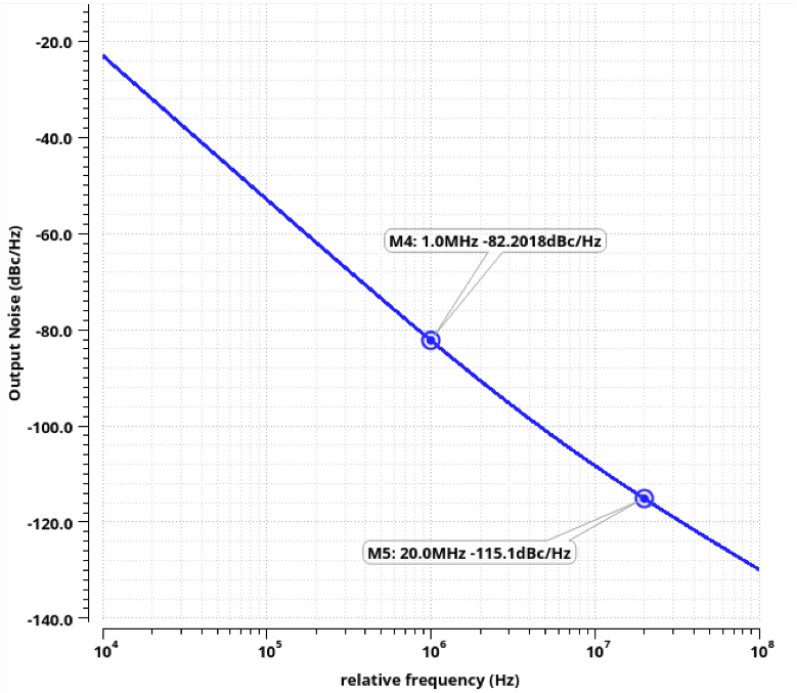


Figure 5.47: Post-layout simulated phase noise versus offset frequency for the proposed oscillator operating at 2.407 GHz. The phase noise reaches -82.2 dBc/Hz *at 1 MHz offset and* -115.1 dBc/Hz *at 20 MHz offset. The VCO core operates with a supply voltage of* $V_{\mathrm{DD,core}} = 0.6$ V. *Simulations were performed under the typical process corner.*

The total power consumption of the proposed system was evaluated through post-layout simulations, as illustrated in Figures 5.48 and 5.49. All blocks were biased at a nominal supply voltage of 0.9 V, except for the VCO core, which operated at a reduced voltage of $V_{\mathrm{DD,core}} = 0.6$ V to enhance energy efficiency. Table 5.11 summarizes the simulated power consumption of each functional block.

The overall circuit consumes a total of 9.592 mW, with the output buffer stages representing the dominant contribution. Specifically, the power stage of the output buffers accounts for approximately 78% of the total consumption, while the gain stage contributes around 18%. In contrast, the VCO core itself consumes only 393.5 μW, corresponding to roughly 4% of the total power. The digital control circuitry—including the SPI interface, $\Sigma\Delta$ modulator, and clock generator—exhibits negligible consumption (each below 2.5 μW), validating the low-overhead design of the digital front-end.
Figure 5.48 presents the global power distribution across buffers blocks, while Figure 5.49 provides a view focusing on the core blocks composing the circuit, i.e. the $\Sigma\Delta$ modulator, the clock generator, and the VCO core.

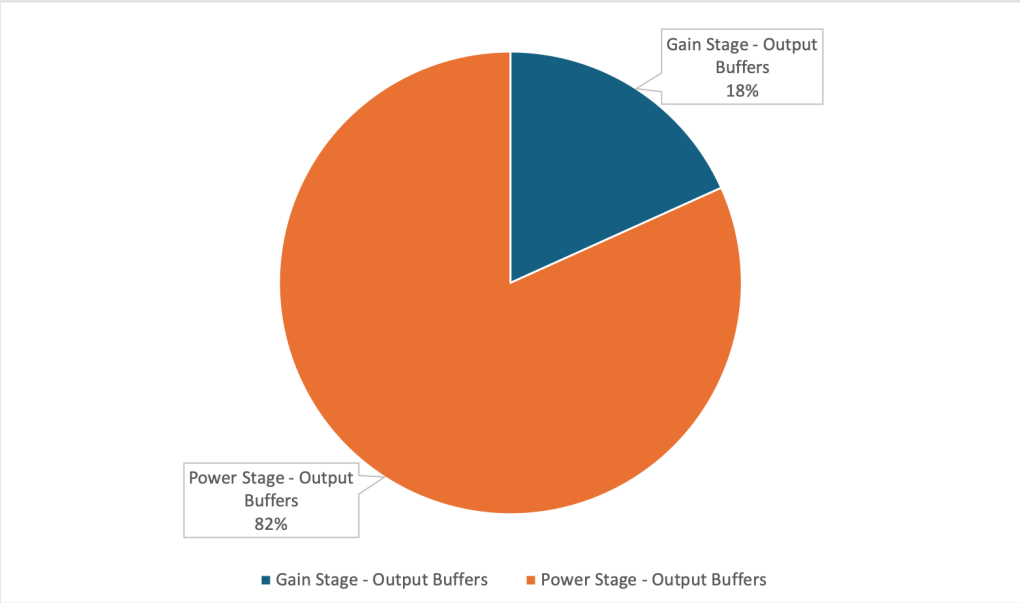


Figure 5.48: Post-layout simulated power distribution among buffers blocks. Simulations were performed under the typical process corner.

The proposed 18nm FD-SOI CMOS ring oscillator achieves excellent trade-offs between spectral purity, energy efficiency, and area compactness when compared with state-of-the-art designs, as summarized in Table 5.12. The benchmarking includes the same references as the one presented in section 5.2. Figures 5.50 and 5.51 complement this comparison by illustrating, respectively, the evolution of phase noise and normalized power efficiency as a function of the oscillation frequency.
Despite operating at an ultra-low supply voltage of 0.6 V—significantly below most reference designs—the proposed oscillator achieves a phase noise of $-82.2\,\mathrm{dBc/Hz}$ at 1 MHz offset and $-115.1\,\mathrm{dBc/Hz}$ at 20 MHz offset. This results in a phase noise figure of merit ($\mathrm{FoM_{PN}}$) of $-149.8\,\mathrm{dBc/Hz}$ and a power-aware figure of merit ($\mathrm{FoM_{Power}}$) of $-153.86\,\mathrm{dBc/Hz}$, values that remain competitive with or superior to other FD-SOI implementations operating at higher voltages.
The overall power consumption of the VCO core is limited to 393.5 μW, corresponding to

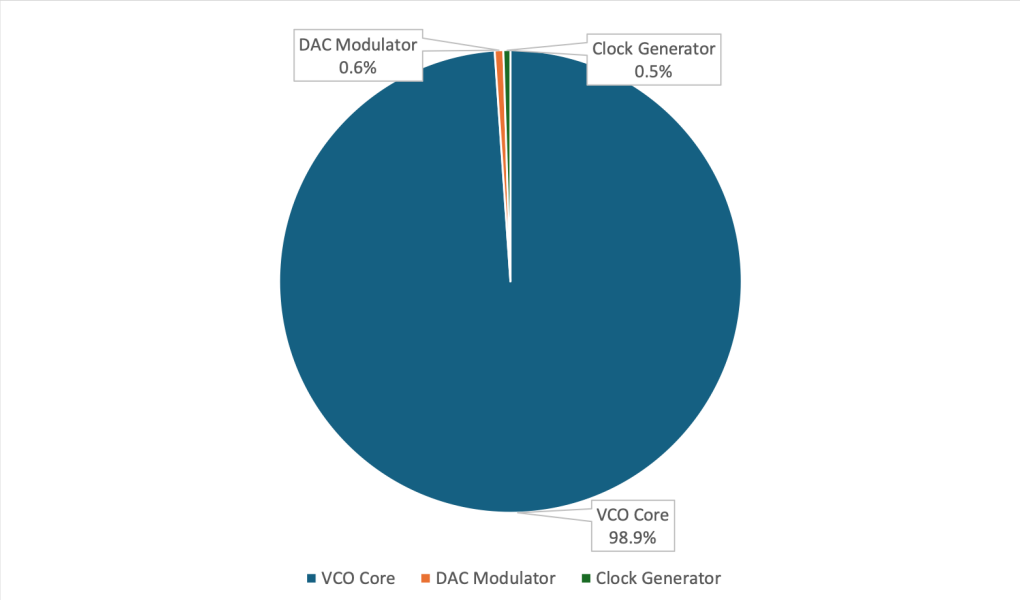


Figure 5.49: Zoomed view of the post-layout power consumption for the core blocks, highlighting the VCO core and the digital control system (DAC modulator, and clock generator). Simulations were performed under the typical process corner.

Table 5.11: Post-layout simulated power consumption of each block composing the circuit.

Block	**Power Consumption**	**Supply Voltage**
Gain Stage – Output Buffers	1.678 mW	0.9 V
Power Stage – Output Buffers	7.514 mW	0.9 V
VCO Core	393.5 μW	0.6 V
DAC Modulator	2.383 μW	0.9 V
Clock Generator	1.958 μW	0.9 V
SPI	1.825 μW	0.9 V
Total	**9.592 mW**	

a normalized energy efficiency of 0.164 mW/GHz—a remarkably low value considering the constrained voltage headroom.

In comparison, the previous design presented in section 5.2 consumed 0.282 mW and exhibited a slightly better phase noise, yet at a higher supply voltage (0.68 V), highlighting the robustness of the proposed low-voltage optimization strategy.

The frequency tuning range extends from 2.05 GHz to 2.78 GHz (30.2%), primarily enabled by the adaptive body-bias control implemented through back-gate modulation. The area efficiency is also significantly improved, with the active VCO core occupying only 126 μm^2, a fivefold reduction compared to the 28 nm FD-SOI reference by Gaidioz *et al.* [32].

The plots in Figures 5.50 and 5.51 further emphasize the design's balance between performance and efficiency. The oscillator achieves a phase noise trend comparable to the one of Asprilla [27]. This confirms the benefits of FD-SOI's body-bias tunability and the proposed low-voltage design methodology, which jointly mitigate the degradation typically observed when scaling supply voltage and transistor dimensions [28].
In summary, the proposed oscillator extends the design philosophy initiated in the previously presented one by pushing further toward ultra-low-voltage operation and improved integration density, while maintaining competitive phase noise and superior energy efficiency. These results highlight the 18nm FD-SOI CMOS process as a mature and energy-efficient platform for next-generation ultra-low-power RF oscillators and PLLs.

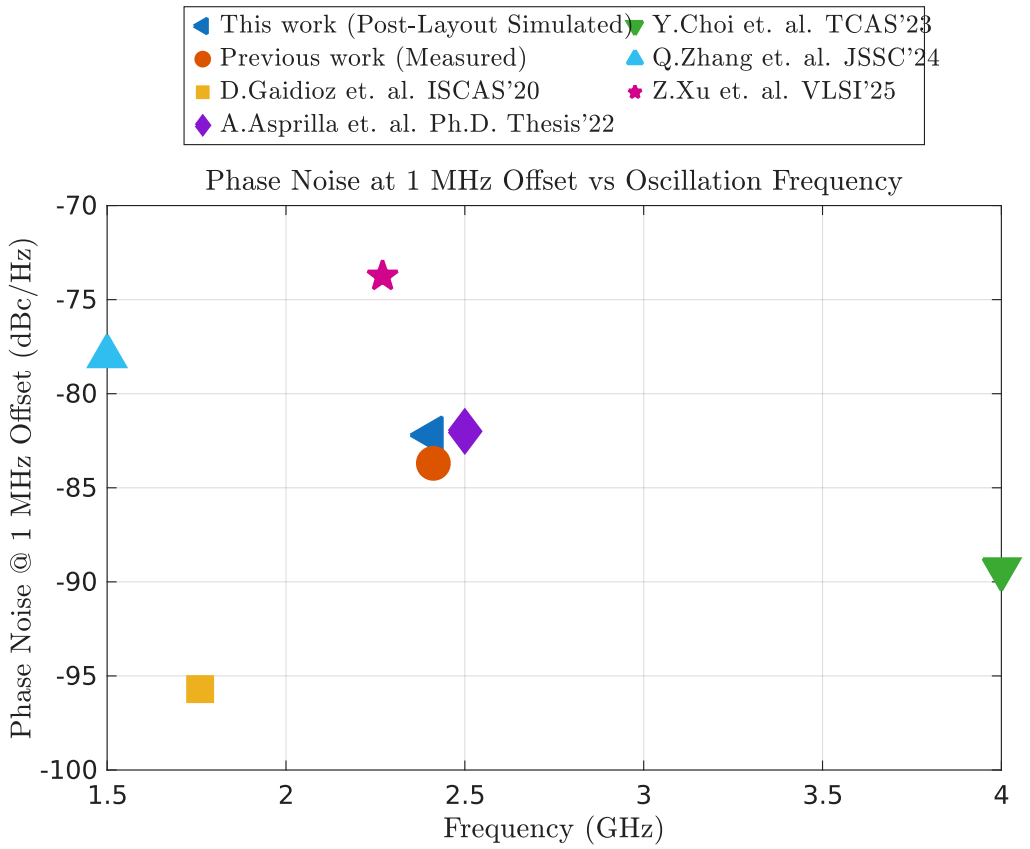


Figure 5.50: Phase noise at 1 MHz offset versus oscillation frequency for the proposed and reference ring oscillators. Lower values indicate better spectral purity.

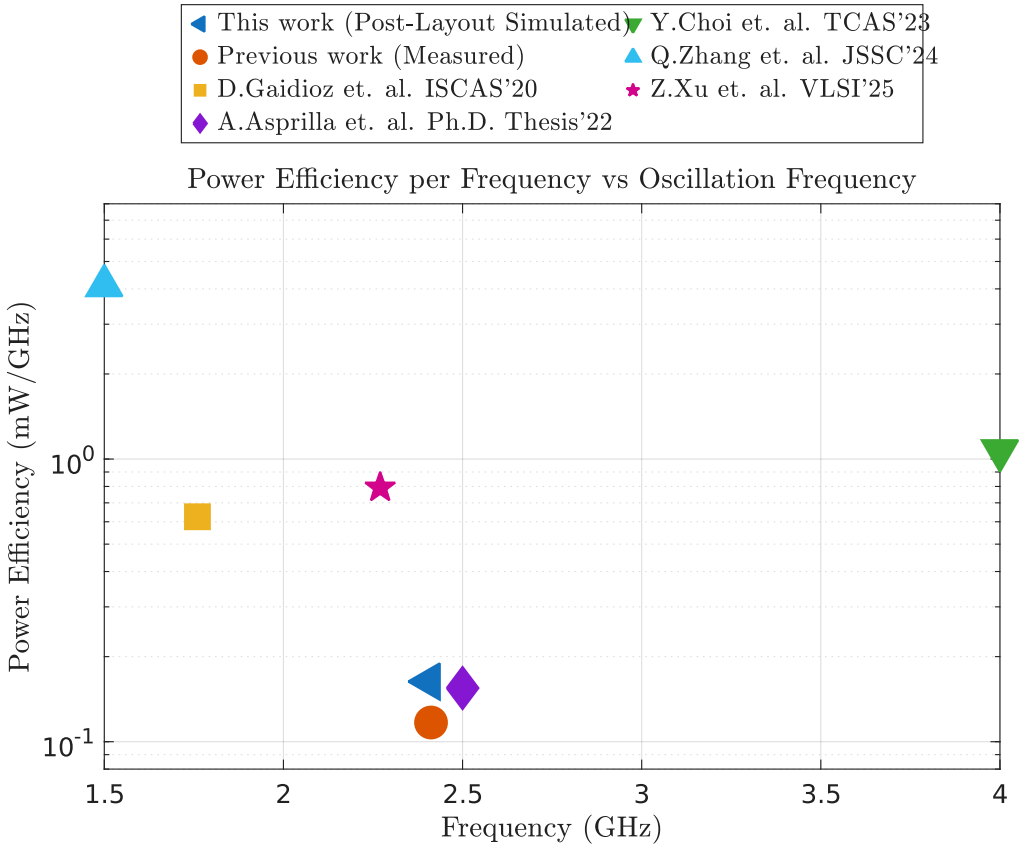


Figure 5.51: Normalized power efficiency (mW/GHz) versus oscillation frequency for the proposed and reference ring oscillators. Lower values correspond to higher energy efficiency.

Table 5.12: Performance summary and comparison with state of the art.

	This work (Post-Layout Simulated)	**Previous work (Measured)**	**D. Gaidioz et. al. ISCAS'20 [32]**	**A. Asprilla Ph.D. Thesis'22 [27]**	**Y. Choi et. al. TCAS'23 [34]**	**Q. Zhang et. al. JSSC'24 [35]**	**Z. Xu et. al. VLSI'25 [36]**
Topology	PD-RVCO	Varactor PD-RVCO	PD-RVCO	RVCO	PD-RVCO	PD-RVCO	RVCO
Control Type	Digital (step: 91 kHz)	Analog	Analog	Analog	N/A	Digital (step: N/A)	Analog
Technology	18nm FD-SOI CMOS	18nm FD-SOI CMOS	28nm FD-SOI CMOS	28nm FD-SOI CMOS	65nm CMOS	28nm CMOS	22nm CMOS
Output Frequency (GHz)	2.407	2.412	1.76	2.5	4	1.5	2.27
FTR (%)	2.05 - 2.78 (30.2%)	0.816 - 5.29 (146.5%)	0.7 - 2.78 (119.5%)	2.35 - 3 (24.3%)	N/A	N/A	2.27 - 15.83 (149.8%)
Supply Voltage (V)	0.6	0.68	1	1	1	1	N/A
Power Consumption (mW)	0.398‡	0.282	1.1	0.387⋆	4.28	6.16†	1.8
PN@1MHz (dBc/Hz)	-82.2	-83.7	-95.7	-82*	-89.34	-78*	-73.75
PN@20MHz (dBc/Hz)	-115.1	-116.2	-126	-124*	-126	-105*	-108*
Area (μm^2)	126	153	800	7290⋆	N/A	N/A	N/A
FoM$_{PN}^{(1)}$	-149.8	-151.35	-160.61	-149.96	-161.38	-141.52	-140.87
FoM$_{Power}^{(2)}$	-153.86	-156.85	-160.2	-154.08	-155.07	-133.63	-138.32
Power spent per frequency$^{(3)}$ (mW/GHz)	0.164	0.117	0.625	0.155	1.07	4.11	0.793

⋆ VCO + VCDL.
† All analog part.
‡ VCO + DAC.
* Obtained from graphical extrapolation.
(1) $\text{FoM}_{\text{PN}} = PN@1MHz - 20\log_{10}\left(\frac{f_0}{1MHz}\right)$
(2) $\text{FoM}_{\text{Power}} = PN@1MHz - 20\log_{10}\left(\frac{f_0}{1MHz}\right) + 10\log_{10}\left(\frac{P}{1\text{mW}}\right)$
(3) Power spent per frequency = Power Consumption (mW) / Output Frequency (GHz)

5.4 Conclusion

This chapter has presented two complementary ring oscillator realizations in 18nm FD-SOI CMOS, each validated at a different design stage.

Firstly, a multi-tuning, inverter-based RVCO operating at a core supply of $V_{DD,core} = 0.68\,\mathrm{V}$ and centered around 2.412 GHz, achieving a phase noise of $-83.7\,\mathrm{dBc/Hz}$ at 1 MHz and $-116.2\,\mathrm{dBc/Hz}$ at 20 MHz offset was proposed. The oscillator consumes only 0.282 mW with a core area of $153\,\mu\mathrm{m}^2$. By exploiting FD-SOI's back-gate control, a hierarchical multi-tuning approach enables a very wide effective tuning capability, leading to competitive figures of merit — $\mathrm{FoM}_{PN} = -151.35\,\mathrm{dBc/Hz}$, $\mathrm{FoM}_{Power} = -156.85\,\mathrm{dBc/Hz}$ — and a normalized power-per-frequency ratio of $0.117\,\mathrm{mW/GHz}$. These results confirm the suitability of the proposed approach for ultra-low-voltage and ultra-low-power applications, as well as that the suitability of RF voltage-controlled ring oscillator as technological marker.

Secondly, a pseudo-differential RVCO with an integrated digital control system composed of an SPI interface, a $\Sigma\Delta$ modulator, a clock generator, and a switched-capacitor filter was presented. With the VCO core biased at $V_{DD,core} = 0.6\,\mathrm{V}$, simulations predict a phase noise of $-82.2\,\mathrm{dBc/Hz}$ at 1 MHz and $-115.1\,\mathrm{dBc/Hz}$ at 20 MHz offset, for a total core power of $393.5\,\mu\mathrm{W}$ and an active area of $126\,\mu\mathrm{m}^2$. The frequency tuning range extends from 2.05 GHz to 2.78 GHz (30.2%), driven by adaptive body-bias modulation.

Taken together, the results confirm that FD-SOI CMOS back-gate biasing is an effective mechanism for achieving ultra-low-voltage operation while maintaining competitive phase noise and energy efficiency. Moreover, the integration of a compact, digitally assisted control chain demonstrates the potential of ring-based VCOs for cost- and area-constrained IoT and RF systems.

6

General Conclusion

6.1 Conclusion

Over the course of this manuscript, several topics have been explored—topics which may initially appear distant from one another. This work aims to bring together in a unified perspective. From MOSFET modeling to circuit design methodologies, this PhD thesis leverages complementary techniques to advance the design of ultra-low-voltage (ULV) and ultra-low-power (ULP) frequency synthesizers in FD-SOI CMOS technology and under low V_{DD} conditions.
IoT-related challenges are numerous, particularly for frequency synthesizers. Beyond the central objective of minimizing power consumption, designers must also meet increasing demands on silicon area, achieve ever-lower phase noise, and support higher communication frequencies to enable efficient RF and millimeter-wave wireless links. Addressing these requirements simultaneously calls for innovations spanning multiple levels of abstraction: technological advances, improved device-level understanding, enhanced modeling techniques, and refined circuit-level methodologies.
In this context, the present manuscript attempts to explore and connect these different aspects:

- Chapter 2 introduces FD-SOI CMOS technology, its origins, key technological features, and intrinsic advantages for ULV/ULP design. Charge-based transistor modeling is then presented, with emphasis on its benefits for low-voltage operation. The chapter concludes with an overview of inverter-based ring VCOs, their integration into modern ULV/ULP PLLs, and a state-of-the-art review of recent inverter-based ring oscillators.

- Chapter 3 focuses on the development of charge-based modeling. Several improvements are proposed to enhance its relevance for ULV/ULP circuit design, ranging from refined physical considerations to improved mathematical formulations and computational implementations.

- Chapter 4 bridges the gap between charge-based modeling and large-signal circuit design by introducing a mathematical framework enabling preliminary sizing and performance prediction of inverter-based ring VCOs.

- Chapter 5 explores design techniques for ULV/ULP inverter-based ring oscillators. Two circuits are presented, each leveraging distinct advantages of 18nm FD-SOI CMOS. The first is a multi-tuning low-power ring oscillator exploiting the adaptive body-biasing capabilities of 18nm FD-SOI to achieve state-of-the-art power spent per frequency. This design has been fabricated, measured, and used to define a technological marker for RF design in this technology node. The second circuit is a ring oscillator with a fully integrated digital control system, intended as a building block

for modern frequency synthesizers. It demonstrates the benefits of mixed-signal architectures for ULV/ULP operation. At the time of writing of this manuscript, this circuit is undergoing fabrication.

The main scientific contributions of this thesis are summarized as follows:

- Improvements to charge-based modeling formulations through explicit consideration of carrier velocity saturation at both the drain and source sides of the MOSFET.
- Extension of charge-based models through the integration of a sixth physical parameter, improving model accuracy without incurring significant additional mathematical complexity.
- Enhanced mathematical implementation linking transistor terminal voltages, inversion charge densities, and drain current through a continuous formulation.
- Development of a SPICE-like analytical model of a single-ended ring oscillator based on charge-based descriptions, enabling rapid transient prediction and preliminary sizing.
- Proposal of an innovative tuning technique for voltage-controlled oscillators using adaptive body-biasing applied to a MOS varactor.
- Proposal of circuit architecture, design and layout implementation for two circuits in the 18nm FD-SOI CMOS technology from STMicroelectronics, together with a complete test strategy and the corresponding on-wafer experimental validation.

Altogether, the developments and results presented in this manuscript demonstrate how device-level modeling, circuit-level innovation, and technology-aware design can be jointly leveraged to advance the state of the art in ultra-low-power frequency synthesis.

6.2 Perspectives

The contributions of this thesis give rise to several promising perspectives, ranging from advances in charge-based device modeling to further developments in ultra-low-voltage and ultra-low-power circuit design.

First, the developments on charge-based modeling could be extended by incorporating additional short-channel effects, such as channel-length modulation, as well as FD-SOI-specific phenomena like the body-bias sensitivity factor. Although these topics have already been explored in previous works [23, 24], they have not yet been integrated within the proposed mathematical framework developed in this thesis. Doing so could further enhance their accuracy and computational efficiency, and provide a more unified and physically consistent modeling approach for advanced CMOS nodes.

Second, the large-signal analytical methodology developed for inverter-based ring oscillators could be extended to a broader class of CMOS circuits, including purely digital blocks. Such a generalization would pave the way for a unified analytical tool capable not only of supporting the preliminary sizing of inverter-based large-signal circuits—such as ring oscillators—but also of establishing a quantitative link between digital performance metrics and underlying technological advancements. In parallel, the proposed methodology should be further enhanced to incorporate a complete treatment of phase noise in ring oscillators. This extension would enable a fully comprehensive design framework, combining transient behavior, frequency tuning, power estimation, and noise analysis within a single modeling approach.

As presented in [65], V. Colrat et al. have already integrated the first proposed VCO into a sequential dual-loop digital–analog PLL, whose architecture is shown in Figure 6.1. A natural continuation of this work is the full integration of the second proposed VCO architecture into a complete PLL. Such an effort would combine the proposed VCO and its digital control system within a closed-loop system incorporating a frequency divider, a phase detector, and a loop filter. This integration would enable a comprehensive evaluation of system-level performance metrics—lock time, spur behavior, long-term stability, and resilience to supply perturbations—thereby assessing the true advantages of FD-SOI CMOS technologies for ultra-low-power frequency synthesis. Ultimately, such studies could help establish FD-SOI CMOS ring-based PLLs as strong contenders for next-generation IoT transceivers and energy-constrained RF systems.

Finally, the experimental validation of the second circuit—currently in fabrication—will constitute a major follow-up step. Its measurement will provide critical feedback on both the accuracy of the technological models and the associated design tools, particularly for the digital blocks, as well as on the practical viability of integrating the proposed digitally controlled VCO into a complete PLL architecture.

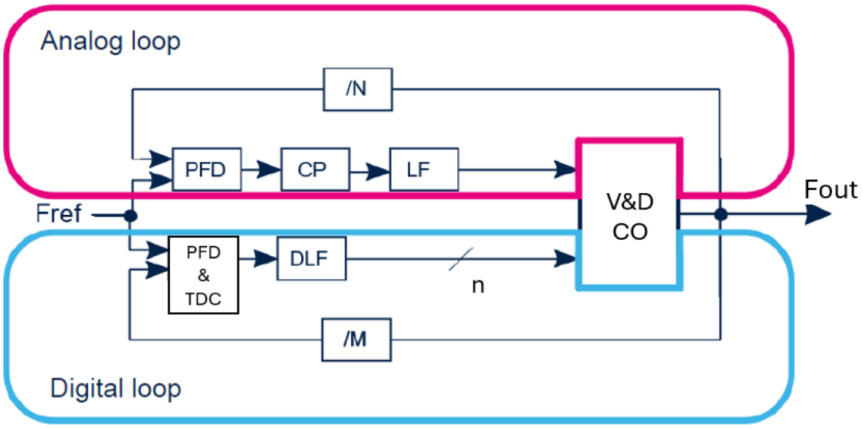


Figure 6.1: Architecture of the sequential dual-loop digital and analog PLL proposed in [65]. Used with permission.

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A

Appendix 1 : Layout Details of the SPI, ΣΔ-DAC, and Clock Generator

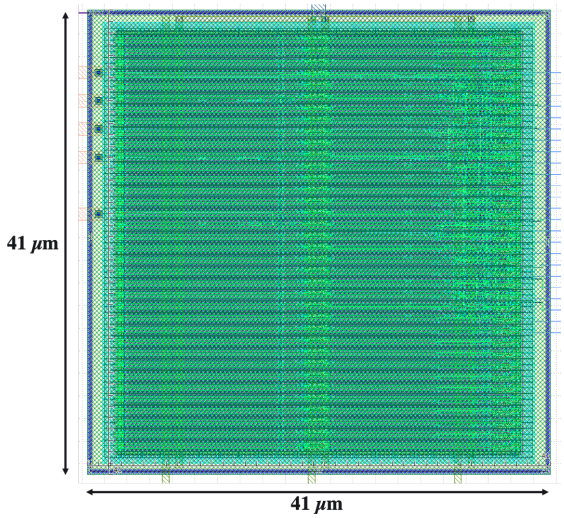


Figure A.1: Layout of the SPI core.

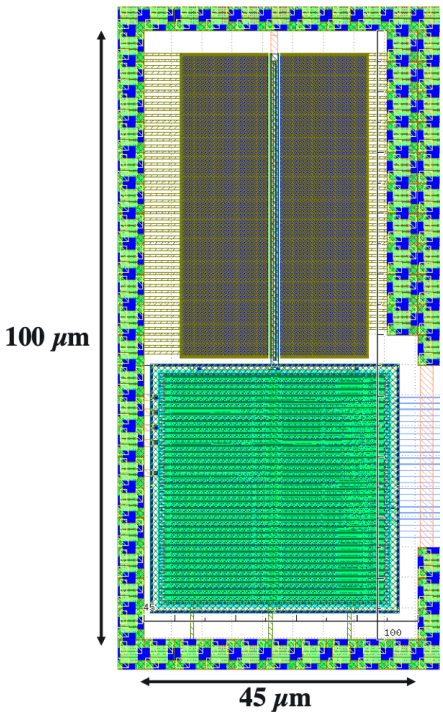


Figure A.2: Layout of the SPI core including its decoupling capacitors (b). The guard ring provides isolation from adjacent circuitry, while the dedicated power grid ensures uniform voltage distribution across the standard cells. This layout structure is representative of all blocks synthesized using the digital design flow.

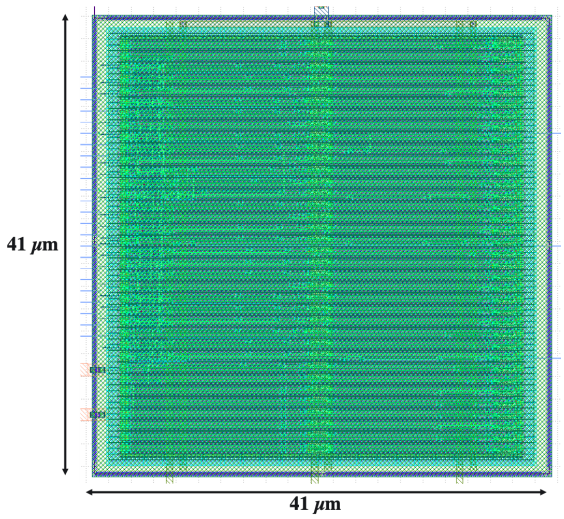


Figure A.3: Layout of the ΣΔ modulator core.

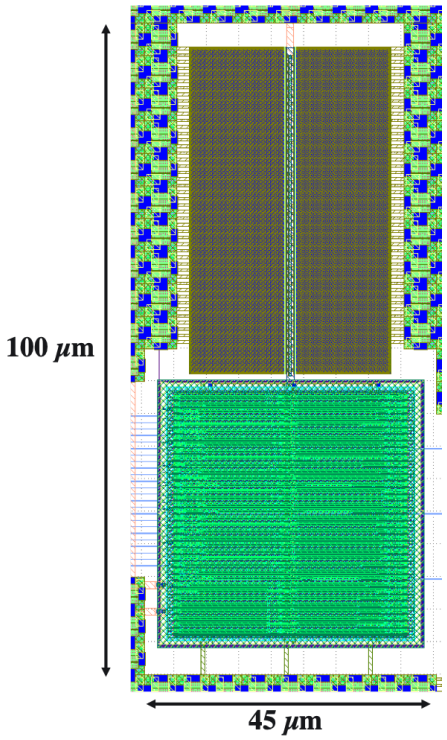


Figure A.4: Layout of the ΣΔ modulator core including its local decoupling capacitors.

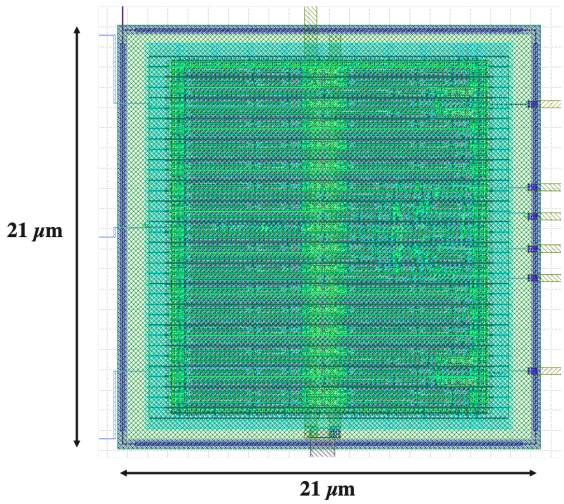


Figure A.5: Layout of the clock generator core.

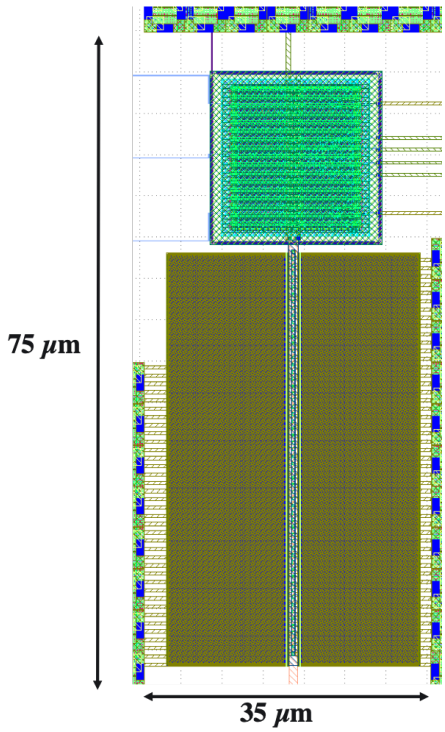


Figure A.6: Layout of the clock generator core including its local decoupling capacitors.