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Architecture et conception de circuits intégrés en technologie CMOS 22 nm pour des applications d'interfaçage sans fil millimétriques en bande V

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Abstract

Millimeter-wave communications in the V-band (57–64 GHz) represent a promising solution for replacing high-speed wired interfaces through wireless links, thanks to their large available bandwidth and inherent spatial confinement. However, reproducing the performance of standards such as USB 3.2 (10 Gb/s, BER $\leq 10^{-12}$, latency < 3 ns) remains a major challenge in terms of power consumption, robustness, and architectural complexity.

This thesis presents the design of a CMOS millimeter-wave receiver capable of supporting a USB 3.2-class wireless link over short-range distances from 5 mm to 5 cm. A hierarchical design methodology combining top-down and bottom-up approaches is employed to translate system-level constraints into RF circuit specifications and to validate architectural choices.

The main contribution of this work is the design of a 60 GHz reconfigurable low-noise amplifier incorporating a transformer-based inter-stage network and a continuous gain control mechanism over a 10–20 dB range without significant degradation of the noise figure. In addition, a stacked passive device technique is introduced, enabling a 40–55% reduction in silicon area.

The receiver architecture is based on a dual-path I/Q downconversion scheme combining the proposed LNA, a splitter- and balun-based impedance matching network, and active mixers. System-level analysis and validation show a total gain of approximately 38 dB, a noise figure of 6.5 dB, and a power consumption of 52.5 mW. The overall performance achieves a BER below 10^{-12} with a latency below 1 ns.

This work demonstrates the feasibility of a low-latency, energy-efficient analog millimeter-wave receiver, paving the way toward wireless replacement of high-speed wired interfaces.

Résumé

Les communications millimétriques en bande V (57–64 GHz) constituent une solution prometteuse pour le remplacement sans fil des interfaces filaires haute vitesse, grâce à leur large bande passante et leur confinement spatial naturel. Toutefois, reproduire les performances d'interfaces telles que l'USB 3.2 (10 Gb/s, BER $\leq 10^{-12}$, latence < 3 ns) reste un défi majeur en termes de consommation, de robustesse et de complexité architecturale.

Cette thèse propose la conception d'un récepteur millimétrique en technologie CMOS capable de supporter une liaison sans fil de classe USB 3.2 sur des distances de 5 mm à 5 cm. Une méthodologie de conception hiérarchique, combinant approches descendante et ascendante, est utilisée afin de traduire les contraintes système en spécifications RF et de valider les choix architecturaux.

La contribution principale de ce travail est la conception d'un amplificateur faible bruit reconfigurable à 60 GHz, intégrant un réseau inter-étage basé sur transformateur ainsi qu'un mécanisme de contrôle de gain continu sur une plage de 10–20 dB sans dégradation significative du facteur de bruit. Une technique de composants passifs empilés est également proposée, permettant une réduction de 40 à 55% de l'empreinte silicium.

L'architecture du récepteur repose sur une conversion directe en I/Q à double chemin, combinant le LNA proposé, un réseau d'adaptation basé sur splitter et baluns, ainsi que des mélangeurs actifs. L'analyse et la validation système montrent un gain total d'environ 38 dB, un facteur de bruit de 6.5 dB et une consommation de 52.5 mW. Les performances globales atteignent un BER inférieur à 10^{-12} avec une latence inférieure à 1 ns.

Ce travail démontre la faisabilité d'un récepteur millimétrique analogique à faible latence et à haute efficacité énergétique, ouvrant la voie au remplacement sans fil des interfaces filaires haute vitesse.

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Caen, France

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6.1 Summary of Receiver Performance Against Initial Specifications 133

List of Acronyms

IEEE	Institute of Electrical and Electronics Engineers
QPSK	Quadrature Phase Shift Keying
BPSK	Binary Phase Shift Keying
N-QAM	N-Quadrature Amplitude Modulation
OOK	On-Off Keying
BPOOK	Binary Phase On-Off Keying
ASK	Amplitude Shift Keying
LNA	Low-Noise Amplifier
RFFE	Radio Frequency Front-End
BBA	Baseband Amplifier
PA	Power Amplifier
SNR	Signal-to-Noise Ratio
BER	Bit Error Rate
FEC	Forward Error Correction
NMOS	N-channel Metal-Oxide Semiconductor
PMOS	P-channel Metal-Oxide Semiconductor
USB	Universal Serial Bus
FSPL	Free-Space Path Loss
AWGN	Additive White Gaussian Noise
RF	Radio Frequency
mmW	Millimeter-Wave
PLL	Phase-Locked Loop
ADC	Analog-to-Digital Converter
DAC	Digital-to-Analog Converter
LO	Local Oscillator
DC	Direct Current
MIMO	Multiple-Input Multiple-Output

WLAN	Wireless Local Area Network
ICP1	Input 1-dB Compression Point
IIP3	Input Third-Order Intercept Point
OCP1dB	Output 1-dB Compression Point
Tx	Transmitter
Rx	Receiver
I/Q	In-phase / Quadrature
CMOS	Complementary Metal-Oxide-Semiconductor
EVM	Error Vector Magnitude
FDSOI	Fully Depleted Silicon-On-Insulator
LPF	Low-Pass Filter
NF	Noise Figure
PGS	Patterned Ground Shield
PLS	Post-Layout Simulation
SOLT	Short-Open-Load-Thru
SoA	State of the Art
VCO	Voltage-Controlled Oscillator
VNA	Vector Network Analyzer
VGA	Variable Gain Amplifier

Chapter 1

Thesis context and claims

This chapter provides the general context of this work. It introduces historical and industrial motivations, illustrates modern use cases, and clarifies the focus on millimeter-wave front-end circuits. The objective is not to provide a technical state-of-the-art but to frame the motivations and constraints that justify the research direction of this thesis.

1.1 Motivation and Industrial Context

1.1.1 Historical Perspective on 60 GHz Transceiver Research

Research and industrial development in 60 GHz transceivers have evolved over distinct phases marked by alternating periods of intense activity and relative stagnation. The first major wave of interest emerged at the beginning of the 2010s with the introduction of the WiGig initiative. The Wireless Gigabit Alliance, formed in 2009, aimed to promote multi-gigabit communications in the unlicensed 60 GHz band and led to the publication of the first WiGig specification in 2009–2010, followed by the IEEE 802.11ad amendment in 2012 [1]. This period saw rapid progress in CMOS millimeter-wave integration, with numerous demonstrations of highly integrated 60 GHz radios targeting short-range high-throughput applications such as wireless docking, cable replacement, and in-room video streaming.

Despite these advances, the industrial momentum slowed noticeably after 2016. Although the Wi-Fi Alliance launched the WiGig certification program that year [2], commercial adoption remained limited. The expected proliferation of WiGig-enabled consumer devices did not materialize, partly due to competing improvements in sub-6 GHz Wi-Fi and the absence of strong mass-market use cases. As a result, R&D activities increasingly shifted back to academic and research institutions, as illustrated by continued publications on low-power or

minimalist 60 GHz transceivers from university groups [3, 4, 5]. These works contributed to fundamental understanding and circuit innovations, but the overall industrial ecosystem experienced a noticeable decline.



Figure 1.1: Illustration of beamforming application presented in the Wireless Gigabit Alliance (WiGig) White Paper of 2010. [6]

A renewed phase of interest began in the early 2020s, driven by several converging trends. First, the publication of the next-generation IEEE 802.11ay standard in 2021 extended the capabilities of 60 GHz systems, enabling aggregated data rates in the 20–40 Gb/s range and longer transmission distances [7]. Second, a new class of applications emerged including untethered AR/VR headsets, wireless docking for mobile computers, high-throughput industrial sensors, and low-latency short-range links for robotics, that aligned naturally with the characteristics of the V-band millimeter-wave spectrum. Parallel research efforts in 5G/6G contexts further underscored the relevance of 60 GHz technology for dense indoor networks and data-intensive edge devices [8].

Together, these developments revitalized both academic and industrial R&D in the field. The combination of mature CMOS technology nodes, improved RF transceiver architectures, and emerging application drivers has positioned 60 GHz communication as a compelling solution for next-generation short-range multi-gigabit systems. This historical trajectory provides the backdrop for the present thesis, which explores system-level constraints, architectural trade-offs, and circuit-level innovations tailored to the stringent requirements of USB-class wireless links.

1.1.2 Modern use cases

Eliminating high-speed physical connectors in consumer and industrial devices enables fully sealed enclosures, improved environmental robustness, and greater design flexibility. A cable-free USB 3.2-class interface implemented over short-range millimeter-wave (mmWave) links at 60 GHz would allow rapid docking, high-speed data offload, and peripheral attachment without mechanical wear or ingress concerns. In mobile devices, such an interface complements existing wireless charging and audio solutions, removing one of the last bulky mechanical features while preserving multi-gigabit throughput.

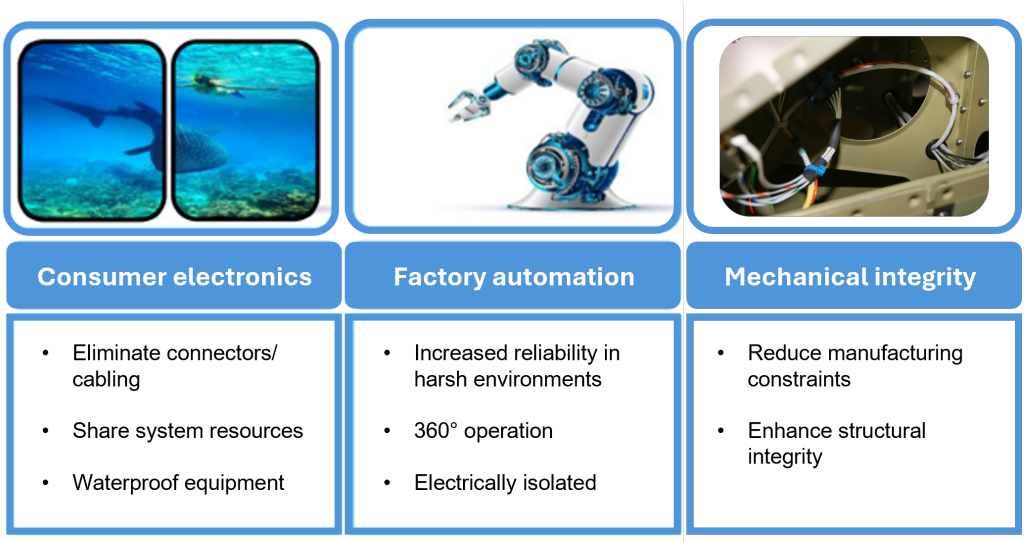


Figure 1.2: Foreseen user case(s) for short-range wireless USB.

The envisioned use cases are deliberately close-range and practical: a phone or headset transferring large files to a base; a robot joint rotating freely without slip-rings; a sealed sensor module updated without opening its housing. In each case, the wireless link should feel indistinguishable from a cable at the user and system level: it should start quickly, sustain multi-gigabit throughput, and behave predictably.

This thesis explores the feasibility of such a link at 60 GHz, where abundant spectrum and spatial confinement are well-suited to short-range operation. The objective is not to replicate a full protocol stack over the air, but to understand how an "USB-class" experience can be delivered wirelessly by translating practical requirements (throughput, reliability, responsiveness) into RF constraints and circuit choices.

1.2 Problem Statement

1.2.1 Focus on radio-frequency and mmW transceivers

Modern electronic systems are increasingly connected and rely on wireless communication capabilities to interface with their environment. To enable such links, they embed dedicated transceiver circuits that bridge the digital processing subsystem and the antenna, which radiates or captures electromagnetic waves. These transceivers integrate a digital processing chain, followed by conversion into the analog and, more specifically, radio-frequency domain before driving the antenna. The reverse path is also implemented: incoming electromagnetic signals are amplified, frequency-translated, and converted back into a digital representation accessible to the system's processor. In this thesis, the focus is placed on the analog and RF sections of these transceivers, that is, the front-end circuits that directly interface with the antennas.

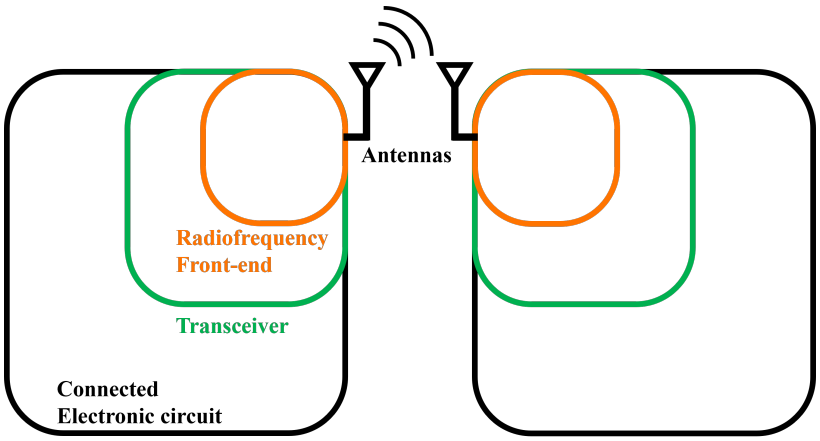


Figure 1.3: Visual representation of the radiofrequency circuits of an integrated transceiver

As operating frequency increases, the design of wireless transceivers becomes significantly more challenging due to the growing influence of parasitic effects. At millimeter-wave frequencies, even the smallest components and interconnects behave as unintended capacitive or inductive elements, and their impact on the signal can no longer be neglected. This makes it difficult to handle very high data rates while preserving the required signal integrity, since any parasitic coupling or loss directly affects amplitude, phase, and bandwidth. These challenges can only be addressed with advanced semiconductor technologies offering high transit frequency, reduced device parasitics, and dense integration.

1.3 Research Methodology

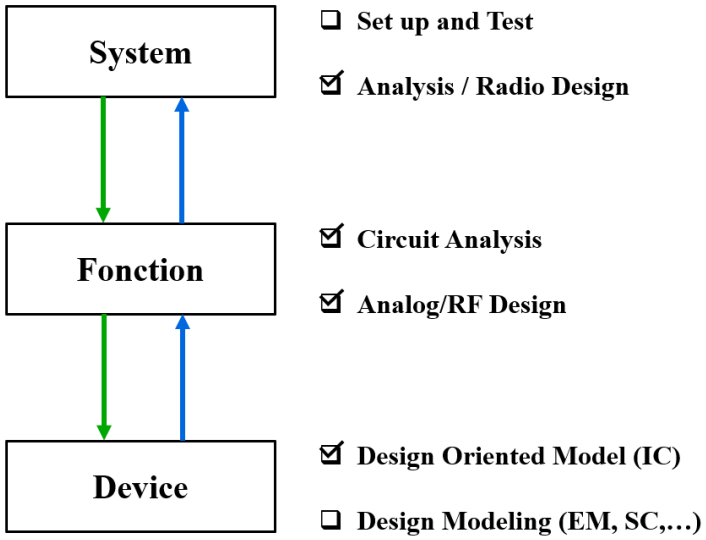


Figure 1.4: Representation of the research methodology pursued in this thesis.

In RF and millimeter-wave research, doctoral work is often centered on a single perspective: the design of a specific circuit block (Function), the development of device-level models and analytical frameworks (Device), scarcely the study of complete communication systems and test methodologies (System). In this thesis, all three viewpoints are combined within a single workflow.

The first phase follows a top-down approach, beginning with the translation of communication standard requirements into millimeter-wave transceiver-level specifications. These system-level constraints are then propagated toward the circuit level, where they guide the analysis and design of the required building blocks. The transistor-level implementation relies on device-oriented considerations, including the use of the Inversion Coefficient methodology to size and bias the active devices.

In the second phase, a bottom-up process is adopted: the fabricated circuits are characterized in the laboratory, and the measured results are mapped back to the transceiver-level specifications defined in the system study. This bidirectional methodology establishes a continuous link between System, Function, and Device perspectives, and structures the scientific progression of the thesis.

1.4 Thesis Purposes and Organization

The objective of this thesis is to investigate and design the millimeter-wave receiver front-end required to enable a short-range wireless link delivering USB 3.2-class performance. Beyond demonstrating the feasibility of such a link at 60 GHz, the work aims to establish a complete system–to–device methodology capable of deriving quantitative block-level specifications from high-level interface requirements. This approach supports two main technical goals: first, identifying receiver architectures that can satisfy stringent constraints on data rate, BER, latency, and power consumption; and second, developing circuit techniques, particularly for reconfigurable low-noise amplifiers, that extend the admissible input dynamic range while preserving bandwidth, linearity, and noise performance. The methodology spans system-level modeling, architectural exploration, and circuit-level implementation in advanced CMOS technology, with a final objective of validating the proposed concepts under realistic transceiver operating conditions.

To address these goals, the thesis is organized as follows :

- Chapter 2 proposes a translation of the requirements of a wired USB 3.2 interface into quantitative system-level specifications for a 60 GHz transceiver along with a review of the state of the art.
- Chapter 3 introduces a three-step transceiver-level design flow used to identify feasible front-end architectures and performance distributions for wireless USB 3.2 applications.
- Chapter 4 develops the design of a reconfigurable two-stage LNA relying on transformer-based passive structures to enable dynamic gain control.
- Chapter 5 extends the receiver chain with the design of a 60 GHz active mixer. This is followed with transceiver-level performances validation after co-integration with a baseband amplifier.
- Chapter 6 outlines the conclusion of this thesis and discusses directions for future research.

Chapter 2

State-of-the-Art of 60GHz Transceivers

This chapter introduces the background needed to understand the challenge in designing a wireless USB 3.2 link at 60 GHz. The expectations normally associated with a wired USB connection must first be translated into requirements that a short-range wireless system can satisfy, even though the two domains rely on very different constraints. The first part of the chapter explains how the main USB 3.2 characteristics (throughput, reliability and responsiveness) can be expressed as quantitative targets for a 60 GHz transceiver.
The second part reviews existing millimeter-wave designs to highlight how current solutions address some aspects of these requirements, while still falling short of the combined performance needed for a wireless USB-class link.

2.1 Technical Constraints for Wireless USB 3.2

2.1.1 USB performance targets

The goal is to sustain a USB 3.2 data rate of 10 Gb/s with near error-free transmission, corresponding to a compliance Bit Error Rate (BER) on the order of 10^{-12} [9]. These figures imply that the wireless link must deliver cable-like integrity without relying on heavy forward-error correction. Table 2.1 summarizes the main requirements.

Table 2.1: Main specifications of the USB 3.2 interface

Specification	**Value**
Nominal data rate (Gen 2)	10 Gb/s
Bit Error Rate	$\leq 10^{-12}$
RF Front-end latency	<3 ns

From an RF perspective, these targets constrain the receiver's Signal to Noise Ratio (SNR), cascaded Noise Figure (NF) and linearity. A front-end latency of a few nanoseconds limits filtering depth and buffering, reinforcing the need for a compact architecture. These constraints form the basis for the link-budget allocations developed later and motivate the choice of operating band and modulation discussed in the following subsections.

Given these performance targets, we select an operating band that offers sufficient license-exempt bandwidth and is compatible with short-range mmWave links.

2.1.2 Operating band at 60 GHz (license-exempt V-band)

This work targets the 57–64 GHz license-exempt allocation used for high-throughput short-range links. The band provides multi-GHz spectrum and strong spatial confinement due to free-space loss and atmospheric characteristics, while remaining broadly accessible under regional regulations.
With the band fixed at 60 GHz, we quantify propagation over millimeter-to-centimeter ranges and derive the short-range link budget terms relevant to the RF front end.

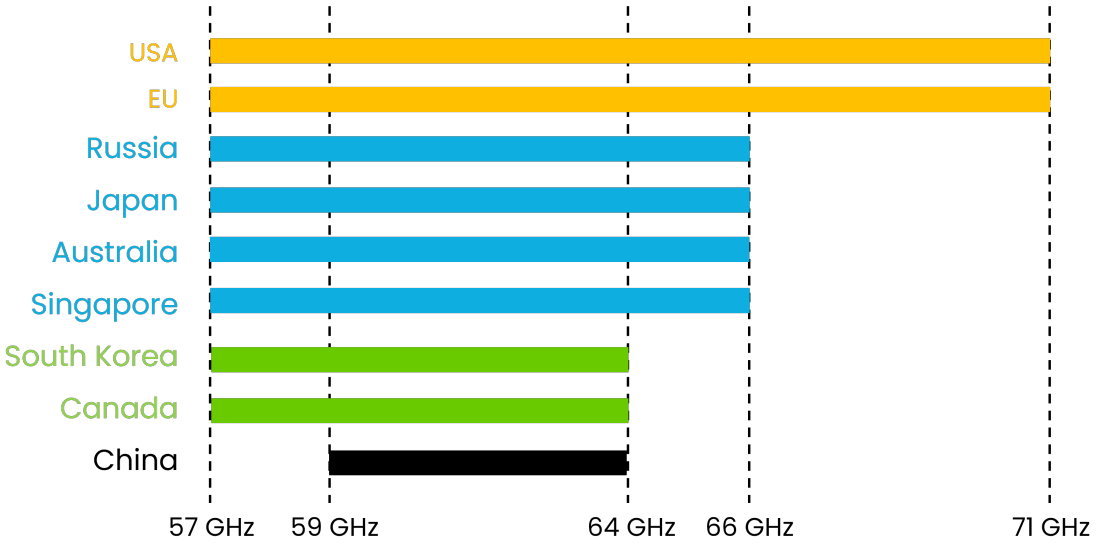


Figure 2.1: V-band bandwidth regulations across various global areas.

2.1.3 Propagation at short range

Propagation at 60 GHz is primarily governed by *free-space path loss* (FSPL), with additional attenuation from atmospheric gases. Oxygen exhibits a well-known absorption peak

near 60 GHz; however, its *specific attenuation* (≈15 dB/km under standard conditions) is *insignificant* at sub-meter scales typical of the ranges considered here. Consequently, for distances of a few millimeters to centimeters, FSPL dominates the RF budget.

$$\mathrm{FSPL(dB)} = 20\log_{10}\left(\frac{4\pi d}{\lambda}\right) = 20\log_{10}(d) + 20\log_{10}(f) + 32.44, \tag{2.1}$$

with d in km and f in MHz. At 60 GHz ($\lambda \approx 5$ mm), illustrative values are:

$$\mathrm{FSPL}(d = 5\text{ mm}) \approx 22\text{ dB}, \qquad \mathrm{FSPL}(d = 5\text{ cm}) \approx 42\text{ dB}.$$

These figures highlight that even at very short ranges, propagation loss is substantial and must be offset by appropriate receiver gain and low NF to meet USB 3.2-class reliability.

The high free-space path loss at 60 GHz strongly constrains the achievable received power and therefore the SNR budget that practical modulations and receiver architectures must satisfy. This motivates an examination of the resulting spectral-efficiency limits and BER performance of candidate modulation schemes.

2.1.4 Modulation and spectral efficiency

Sustaining 10 Gb/s within ∼7 GHz of RF bandwidth requires at least 2 bits/symbol which excludes basic modulation schemes such as OOK, PSK or FSK. *QPSK* modulation provides 2 bits/symbol with mature coherent detection and favorable per-bit BER in AWGN (see Fig. 2.2). With Gray coding, the QPSK per-bit BER is equal to that of BPSK:

$$P_b = Q\left(\sqrt{2\,\frac{E_b}{N_0}}\right), \tag{2.2}$$

This relationship ties the RF link budget to the required E_b/N_0 and motivates NF/gain allocations compatible with USB-class BER.
With RF constraints (FSPL, SNR, BER) established for short-range operation, the next section reviews 60 GHz transceiver architectures from the RF/mmWave literature and evaluates their suitability against these targets.

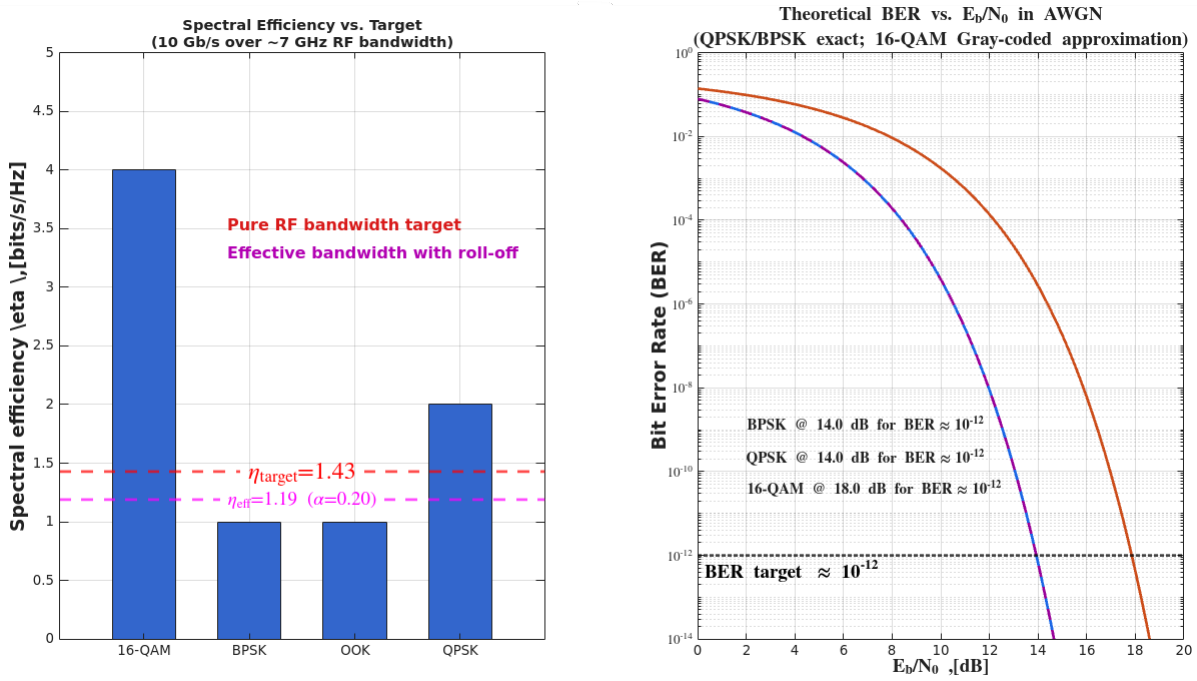


Figure 2.2: Illustrative modulation/spectral-efficiency considerations at 60 GHz.

The constraints outlined in sections 2.1.1 - 2.1.4 ultimately define the quantitative performance envelope that any practical wireless USB3.2 transceiver must satisfy. These requirements stem directly from the USB3.2 target throughput, the BER needed to ensure near–error-free operation, the propagation characteristics at 60 GHz and the spectral-efficiency constraints that exclude low-order modulations such as OOK. For clarity, the key system-level specifications derived from this analysis are summarized in Table 2.2. This consolidated view provides the reference framework against which existing industrial solutions and academic transceivers will be assessed in the following sections.

Table 2.2: Wireless USB3.2 Transceiver Requirements

Center frequency	60.5 GHz
Bandwidth	7 GHz
Data rate	≥ 10 Gb/s
Bit Error Rate	10^{-12}
Front-end latency	≤ 3 ns
Communication distance	up to 5 cm
Total power consumption	≤ 500 mW

2.2 Existing industrial 60 GHz products and their limitations

Several industrial devices have been developed over the past decade to enable short-range, high-data-rate wireless communication in the 60 GHz band. Among the solutions most representative of this trend are the ST60 chipset from STMicroelectronics and the Zing 200RT module from GLS Co., Ltd. Both target cable replacement over distances of a few centimeters and rely on simple non-coherent architectures designed for low cost and minimal system integration effort. Figure 2.3 provides announced performances of these products.

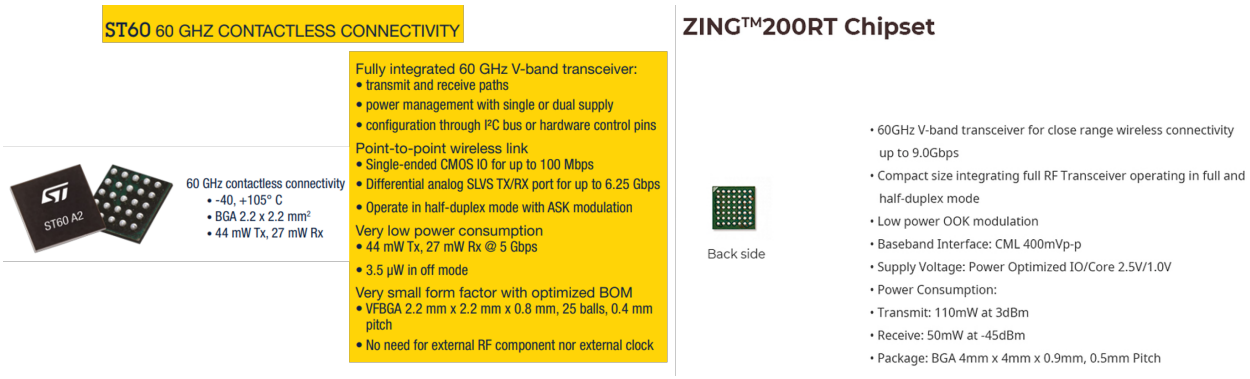


Figure 2.3: Specifications of existing commercial 60 GHz products such as the ST60 and Zing 200RT

The ST60 integrates a complete transceiver supporting data rates up to approximately 5 Gb/s using On-Off Keying modulation. Its receiver is based on envelope detection and does not provide error-rate performance compatible with near–error-free interfaces. No published data indicates operation anywhere close to a bit error rate of 10^{-12} and its modulation scheme inherently limits spectral efficiency, preventing compliance with the throughput and reliability requirements of USB 3.2.

A second example is the Zing 200RT transceiver. It also employs OOK modulation and envelope detection and is intended for low-cost, short-range wireless links. Public information suggests that the device may reach multi-gigabit operation under ideal conditions, but there is no evidence that it is designed for USB3.2 very high data-rate or BER constraints. Its overall performance, reliability and long-term robustness appear insufficient for applications requiring the level of integrity expected from a wired USB interface.

More broadly, existing commercial solutions face several common limitations. Their reliance on non-coherent demodulation prevents efficient exploitation of the 7 GHz-wide spectrum available in the V-band. Their achievable data rates, typically in the 1–5 Gb/s range, fall short of the 10 Gb/s nominal data throughput required by USB 3.2. Besides, these devices provide no guarantee of the ultra-low bit error rates that are mandatory for high-speed digital interfaces.

Achieving such performance would require not only a more sophisticated modulation scheme but also a receiver architecture with significantly improved noise and gain characteristics. The industrial products available today are optimized for simplicity and robustness at the hardware level and thus sacrifice the precision and linearity necessary for near-error-free communication.

These limitations are essential to highlight because they establish a clear boundary between what is feasible with current commercial technology and what is required for fully wireless USB-class operation. The gap indicates that, at present, neither industrial modules nor existing product ecosystems provide a viable alternative to a wired USB 3.2 link. This observation motivates a closer examination of academic work on 60 GHz transceivers. Academic architectures often pursue higher performance, but as later sections will show, they also struggle to simultaneously satisfy the combined constraints of data rate, BER, power consumption and integration level.

2.3 State of the art in 60 GHz transceivers for high data-rate links

The feasibility of multi-gigabit wireless communication in the 60 GHz band has been demonstrated by industry and academia for a decade. Early efforts were driven by the IEEE 802.11ad standard (WiGig), which introduced multi-Gb/s links using single-carrier and OFDM PHYs combined with beamforming. Its successor, IEEE 802.11ay, extended throughput beyond 20 Gb/s through channel bonding and spatial multiplexing. These standards confirm that high-speed wireless links at 60 GHz are achievable; however, their RF front-ends were designed for WLAN requirements, not for the ultra-low BER and deterministic latency demanded by USB 3.2. This gap motivates a closer look at transceiver architectures reported in the literature, focusing exclusively on RF/mmWave circuit design.

To structure this review, recent CMOS transceivers operating in the 60 GHz band are grouped into three categories based on their design priorities:

1. Low-power architectures
2. Mixed-performance architectures
3. High-throughput architectures

Each category is examined for its RF design approach, reported performance and limitations relative to USB 3.2 requirements. In order to be eligible for this state-of-the-art review, a publication must report performances measured on a manufactured chip.

2.3.1 Low-power receivers

Low-power millimeter-wave transceivers have attracted significant interest with the rise of short-range, energy-constrained applications. A large body of work adopts architectures combining a low-noise amplifier, an envelope detector driven by a local oscillator and a baseband limiting stage, together with simple non-coherent modulation such as On–Off Keying (OOK). Their simplicity eliminates mixers, PLLs, ADCs and digital baseband blocks (Fig.2.4), which enables extremely compact silicon area and power consumption often below a few tens of milliwatts. This design philosophy is consistently illustrated with CMOS and SiGe implementations where envelope-detection-based receivers achieve sensitivities better

than $-30\,\mathrm{dBm}$ and energy efficiencies of a few pJ/bit while maintaining multi-Gb/s capabilities.

However, OOK fundamentally provides only one bit per symbol, therefore its achievable throughput is directly limited by the available bandwidth. Since typical non-coherent V-band OOK receivers exhibit a usable bandwidth of approximately 5 to 7 GHz, they can only sustain data rates close to 10 Gb/s under favorable conditions. Consequently, although several designs report BER values below 10^{-12} at bit rates reaching 10 to 20 Gb/s [10, 11, 12, 13, 14, 15], these demonstrations rely on relaxed spectral masks, non-standard channel conditions, short propagation distances, or interference-free environments. This gap between raw achievable rate and regulated throughput makes OOK-based architectures unsuitable for applications requiring compliance with standardized V-band channels or stringent throughput such as USB 3.2.

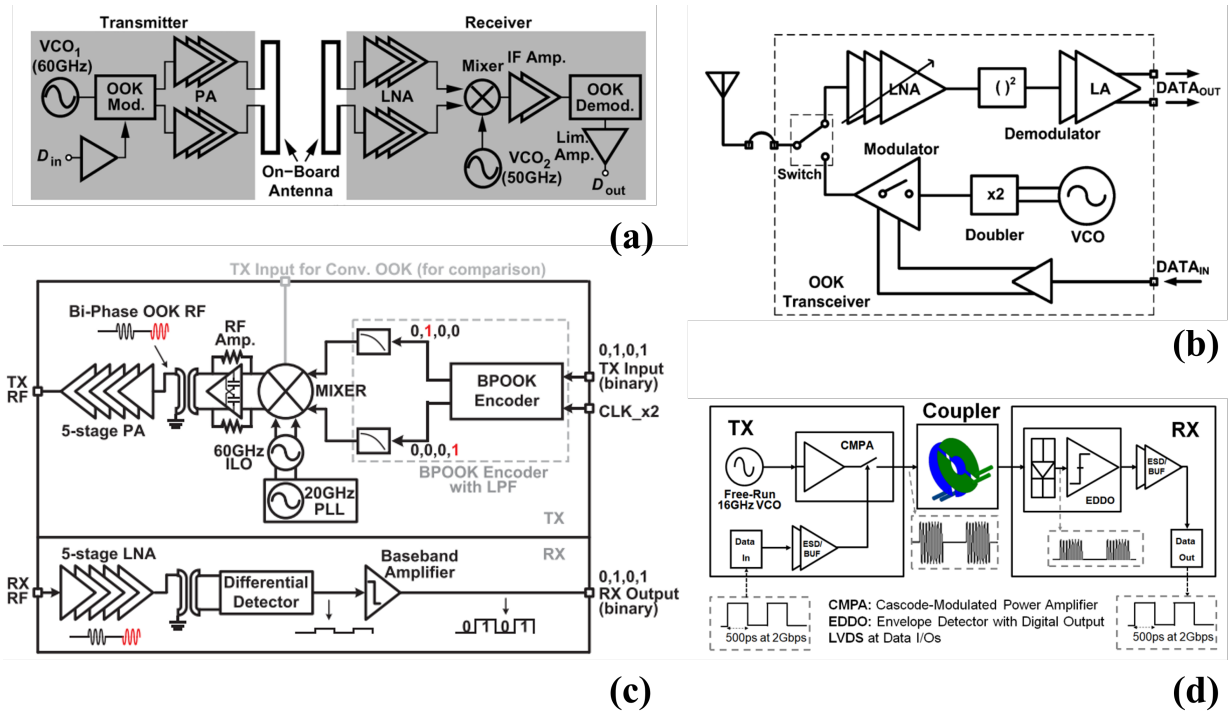


Figure 2.4: Different envelope detector architectures from the state of the art. (a) = [16]; (b) = [17]; (c) = [18]; (d) = [11]

Beyond these conventional OOK implementations, additional works investigate alternative architectures that preserve low power while partially mitigating the spectral limitations. For instance, a millimeter-wave intra-connect solution operates using ASK modulation with

injection-locked carrier synchronization, which enables multi-gigabit transmission between static, co-located modules [10]. Although this architecture demonstrates excellent energy efficiency, its applicability remains confined to fixed point-to-point scenarios because its performance depends strongly on the absence of interference and on the Tx-Rx alignment.

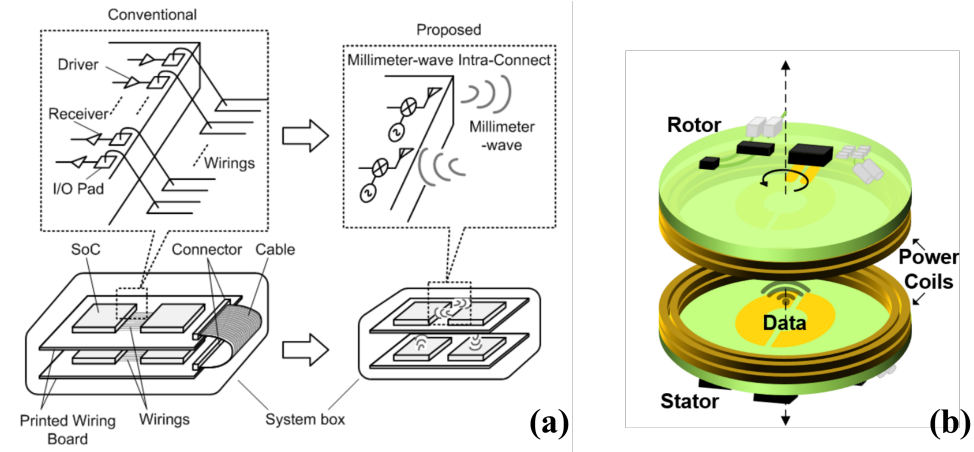


Figure 2.5: Favorable user-case for low power high data-rate wireless communications. (a) = [10]; (b) = [11]

Likewise, compact contactless links based on capacitive or inductive near-field coupling achieve competitive efficiencies and robust short-reach performance (Fig.2.5), although their practical use is limited to mechanically constrained environments since they rely on precise alignment or small separation gaps. An example is the 16 GHz split-ring-resonator-based link that provides full 360° rotational freedom and multi-gigabit data rates [11], which is valuable for specific industrial or robotic joints but not suitable for free-space wireless channels.

To overcome the bandwidth limitations inherent to envelope detection, several recent works introduce circuit enhancements, including multi-resonant or transformer-coupled LNAs for extended RF bandwidth, gain-boosted envelope detectors for improved responsivity, low-noise active baluns and feedforward or active-feedback limiting amplifiers tailored for multi-gigahertz baseband operation. These approaches collectively push OOK performance to the limit of device-level capabilities and demonstrate record data rates up to 16 to 20 Gb/s. Nevertheless, these solutions still rely on non-coherent amplitude detection and therefore cannot escape the fundamental constraint imposed by the limited V-band channel bandwidth. Spectrally efficient variants such as binary-phase OOK (BPOOK) increase spectral compactness and remove local-oscillator feedthrough, although they remain bound to the same envelope-detection bandwidth ceiling.

Table 2.3: Comparison of low-power short-range mmWave transceivers and receivers (ordered from older to newer).

Ref	Techno (nm)	Freq.	BW (3 dB)	Data rate	Distance	Mod.	BER	DC (mW)	Area
[10]	40 CMOS	57 GHz	11 GHz	11 Gb/s	14 mm	ASK	$< 10^{-11}$	70	0.13 mm^2
[11]	65 CMOS	16 GHz	∼4 GHz	2.6 Gb/s	0.1–0.7 mm	OOK	$< 10^{-12}$	50	—
[12]	130 SiGe	60 GHz	∼20 GHz	6–20 Gb/s	(on-wafer)	OOK	$< 10^{-12}$	44	0.82 mm^2
[13]	65 CMOS	80 GHz	∼20 GHz	10–20 Gb/s	(on-wafer)	OOK	$< 10^{-12}$	46	0.84 mm^2
[14]	65 CMOS	60 GHz	∼5.5 GHz	12.5 Gb/s	∼5 cm	OOK	$< 10^{-12}$	33.1	0.15 mm^2
[15]	65 CMOS	60 GHz	>20 GHz	8–16 Gb/s	—	OOK	$< 10^{-12}$	9.9	0.10 mm^2
[16]	90 CMOS	60 GHz	∼ 5 GHz	1–3.3 Gb/s	2–61 cm	OOK	$< 10^{-12}$	206	1.11 mm^2
[17]	90 CMOS	60 GHz	∼14 GHz	5–10.7 Gb/s	10–25 cm	OOK	$< 10^{-12}$	67	0.44 mm^2
[18]	65 CMOS	61 GHz	∼3 GHz	3.0 Gb/s	∼0.14 m	BPOOK	$< 10^{-7}$	100	1.56 mm^2

In summary, low-power OOK-based CMOS transceivers constitute an attractive solution for very-short-range and interference-free links, where simplicity, energy efficiency and compactness dominate. For applications requiring throughput at or above 10 Gb/s, operation within standardized V-band channels, or robustness against mobility and interference, the intrinsic limitations of envelope detection motivate the exploration of more conventional mixer-based architectures, where complexity is traded for spectral control and regulatory compliance.

2.3.2 Mixed-performance homodyne transceivers

Homodyne architectures offer an intermediate solution between envelope-detection receivers and multi-chain high-throughput designs. By eliminating intermediate frequency stages, they reduce complexity compared to superheterodyne topologies but require careful attention to LO phase noise, quadrature accuracy, and I/Q balance at 60 GHz, as these directly affect EVM and BER for coherent modulations such as QPSK and 16QAM. A typical implementation, illustrated in Fig. 2.6, consists of an RF front-end where the received signal is amplified by a low-noise amplifier (LNA) and downconverted to baseband through quadrature mixers driven by a PLL-based local oscillator. The I/Q signals are then processed by variable-gain amplifiers (VGAs) and low-pass filters (LPFs) before digitization via ADCs. On the transmit side, digital baseband data is converted to analog with DACs, upconverted through quadrature mixers, filtered, and amplified for transmission. This direct-conversion approach enables compact integration and high data rates but requires mitigation of DC offsets, LO leakage, and I/Q mismatch.

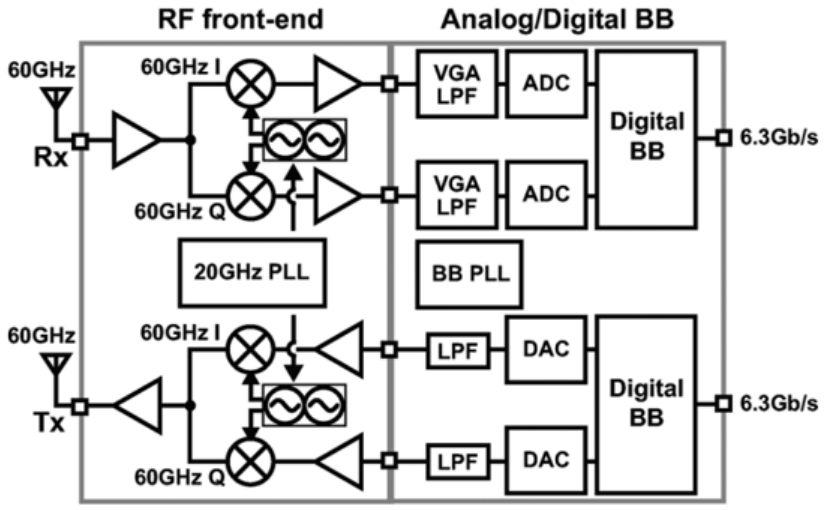


Figure 2.6: Standard homodyne transceiver architecture [19]

Recent publications on integrated V-band transceivers with mixed performance characteristics have become increasingly scarce, as such designs occupy a niche in the innovation landscape. They do not excel in any single metric (data rate, power consumption, or silicon area) but remain relevant for applications like ours. Table 2.4 summarizes several representative studies.

Table 2.4: Comparison of mixed performances short-range mmWave transceivers.

Ref	Techno	BW (3 dB)	Data rate	Distance	Modulation	BER	Conso.	Area
[19]	65 nm	2.16 GHz	3.1 Gb/s	1.8 m	QPSK	$< 10^{-6}$	542 mW	9.24 mm^2
[19]	65 nm	2.16 GHz	6.3 Gb/s	0.05 m	16QAM	$< 10^{-6}$	542 mW	9.24 mm^2
[20]	65 nm	∼5 GHz	5 Gb/s	∼1 m	QPSK	$< 10^{-8}$	311 mW	6 mm^2
[21]	90 nm	∼2.16 GHz	4 Gb/s	1 m	QPSK	$< 10^{-10}$	308 mW	6.9 mm^2
[22]	45 nm SOI	∼2.16 GHz	5 Gb/s	0.7 m	BPSK	$\sim 10^{-6}$	361 mW	4.42 mm^2
[23]	65 nm	∼10 GHz	5 Gb/s	0.3 m	QPSK	$\sim 10^{-7}$	340 mW	6.5 mm^2
[23]	65 nm	∼10 GHz	10 Gb/s	0.3 m	QPSK	$\sim 10^{-5}$	340 mW	6.5 mm^2

All transceivers presented in Table 2.4 are implemented in mature technologies (90nm, 65nm, and 45nm for the most recent), reflecting a declining academic interest in this class of designs. Most of these transceivers are primarily developed to integrate and demonstrate the utility of novel design concepts [20, 22], rather than to achieve record-breaking performance. Nonetheless, their specifications are generally sufficient to support applications conforming to IEEE 802.11ay and IEEE 802.11ad standards, as evidenced by the reported bandwidths that match the channel allocations defined by these communication protocols.

However, these transceivers are likely the closest to meeting the specifications of our use case. It is possible to achieve significant data rates, comparable to our target [23], while maintaining moderate power consumption below 500mW [20, 21, 22, 23]. The reported BER values comply with the aforementioned communication standards but remain insufficient for our specific application. Among the designs considered in this study, the most relevant are those in [20, 21], which achieve moderate data rates (4–5 Gb/s) but exhibit excellent BER performance (10^{-8} to 10^{-10}) over relatively long communication distances (∼1m). Power consumption is also reasonable, although it does not account for the digital baseband functions. Therefore, it is realistic to expect a total power consumption below 500mW for a fully integrated transceiver.

Homodyne transceivers provide higher spectral efficiency than OOK-based designs and can achieve moderate data rates with reasonable BER over short to medium distances. Nevertheless, their power consumption remains substantial (300–500 mW), and no design simultaneously optimizes throughput, energy efficiency, and integration area for USB-class short-range links. Mixed-performance architectures therefore occupy an intermediate niche between low-power and high-throughput transceivers.

2.3.3 High-throughput transceivers

High-throughput millimeter-wave transceivers represent the upper end of performance in V-band communication systems, primarily motivated by the requirements of IEEE 802.11ad and 802.11ay standards. These systems exploit the wide spectrum around 60 GHz through channel bonding, often aggregating multiple contiguous channels to achieve effective bandwidths exceeding 8–10 GHz. The evolution toward IEEE 802.11ay has enabled aggregated data rates well above 20 Gb/s, with some implementations approaching 50 Gb/s. Achieving such throughput typically relies on parallel RF chains combined with MIMO or spatial multiplexing, in which each chain processes an independent subset of the total bandwidth or spatial dimension [24, 25, 26, 27]. Architecturally, these transceivers resemble homodyne receivers scaled horizontally, with replicated mixers, LO distribution networks, LNAs, and high-bandwidth baseband paths to handle multiple streams. An example is illustrated in Figure 2.7.

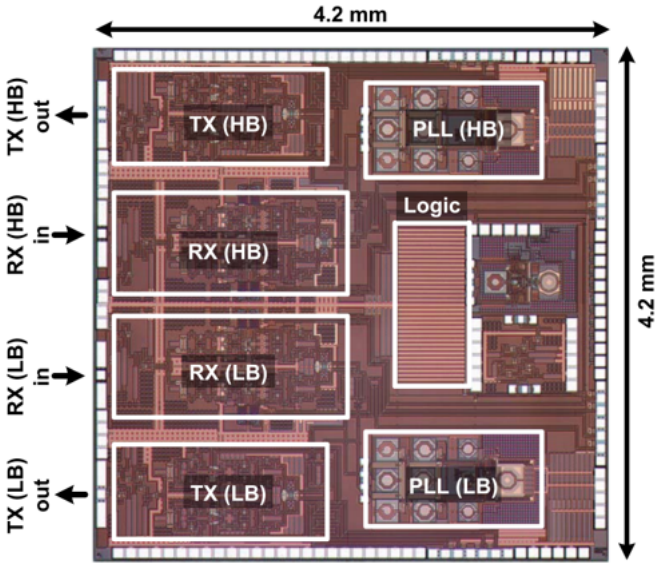


Figure 2.7: High-throughput transceiver with multiple Tx and Rx paths for full bandwidth coverage [24]. LB: lower bandwidth, HB: higher bandwidth.

These performance gains come at a substantial system-level cost. Replicating multiple RF chains increases silicon area, routing complexity, and LO power distribution requirements. Multi-chain calibration is necessary to maintain phase alignment and constellation integrity, particularly with high-order modulations. As a result, total power consumption often exceeds 800 mW once RF, LO generation, digital equalization, synchronization, and beamforming engines are included, making these architectures impractical for embedded or battery-operated devices.

Table 2.5: Comparison of high-throughput short-range mmWave transceivers.

Ref	Techno	BW (3 dB)	Data rate	Distance	Modulation	BER	Conso. (/ch)	Area
[24]	65 nm	2.16 GHz	10.56 Gb/s	0.13 m	64QAM	10^{-3}	471 mW	3.85 mm^2
[24]	65 nm	8.64 GHz (4ch)	42.24 Gb/s	0.03 m	64QAM	10^{-3}	712 mW	7.18 mm^2
[25]	65 nm	4.32 GHz (2ch)	21.12 Gb/s	0.07 m	64QAM	10^{-3}	199 mW	0.96 mm^2
[25]	65 nm	8.64 GHz (4ch)	14.08 Gb/s	0.61 m	QPSK	10^{-3}	199 mW	0.96 mm^2
[26]	65 nm	8.64 GHz (4ch)	14.08 Gb/s	0.54 m	QPSK	$< 10^{-3}$	308 mW	4.32 mm^2
[27]	28 nm	4.32 GHz (2ch)	16 Gb/s	0.1 m	QPSK	$< 10^{-3}$	322 mW	4.32 mm^2
[28]	65 nm	2.16 GHz	7 Gb/s	0.2 m	16QAM	$< 10^{-3}$	—	3.15 mm^2
[29]	65 nm	2.16 GHz	10 Gb/s	>1 m	QPSK	$< 10^{-3}$	319 mW	4.8 mm^2
[29]	65 nm	2.16 GHz	16 Gb/s	>0.2 m	16QAM	$< 10^{-3}$	319 mW	4.8 mm^2

Several trends emerge from the state of the art of this class of transceivers. All employ phase-quadrature-based modulations (QPSK, 16QAM, 64QAM), indicating that QPSK is the preferred choice for our application. Most transceivers achieve data rates above 10Gb/s, except for [28], which is limited to a narrower bandwidth in its specific application but could reach higher data rates using 16QAM if slightly more bandwidth were available. Power consumption is difficult to estimate accurately. Reported values usually refer to a single channel, while other metrics correspond to multi-channel operation. Because some RF blocks are shared across channels, the total power is generally higher than what is shown in the summary table.

Uncoded BER values around 10^{-3}, while suitable for WLAN-class links with strong error correction, remain far above the near-error-free requirement of USB 3.2 ($\sim 10^{-12}$). Consequently, despite achieving aggregated throughputs up to 40 Gb/s, these high-throughput transceivers cannot meet the combined constraints of power, BER, and integration density for short-range USB-class links.

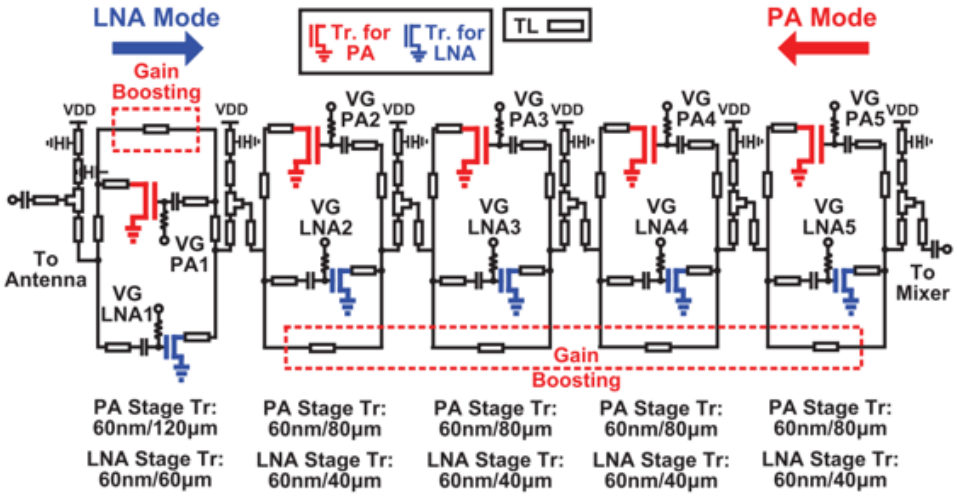


Figure 2.8: Bidirectional LNA/PA architecture, enabling operation in LNA mode (blue) or PA mode (red) [25].

Recent strategies to reduce chip area include bidirectional architectures, in which the LNA and PA share the same signal path. This reduces the number of dedicated blocks, yielding more compact layouts without sacrificing functionality, as illustrated in Figure 2.8. This design technique appears effective, as [25] reports an RF front-end area below 1mm^2 (0.98mm^2), compared to other designs, all exceeding 3mm^2.

In conclusion, high-throughput V-band transceivers demonstrate impressive aggregated data rates (20–40Gb/s) through multi-chain architectures and wideband operation. However, these gains come at the cost of high power consumption, large silicon area, and complex multi-chain calibration. Furthermore, uncoded BER values around 10^{-3} remain far above the near-error-free requirements of USB 3.2 links. Therefore, while these transceivers push the limits of conventional high-throughput designs, they are unsuitable for short-range USB-class applications, motivating alternative architectures that better balance throughput, energy efficiency, and communication reliability.

2.4 Conclusion

This chapter provided a comprehensive review of the feasibility of implementing USB 3.2-class wireless links in the 60 GHz band. It first analyzed the performance requirements of USB 3.2 (including 10 Gb/s data rate, low latency, near-error-free BER, and moderate power consumption) which define the constraints for any wireless 60 GHz solution. Next, commercially available products were surveyed, showing that none fully meets these targets in a single implementation. Finally, the academic state of the art was reviewed and structured into three categories: low-power envelope-detection receivers, mixed-performance homodyne transceivers, and high-throughput multi-chain architectures. Low-power designs are compact and energy-efficient but bandwidth-limited and unsuitable for high-efficiency OOK modulation. Mixed-performance architectures provide moderate data rates and improved BER but still fall short of USB-class throughput and latency. High-throughput multi-chain designs achieve very high raw data rates but require excessive power, silicon area, and calibration effort, while BER remains above USB-class targets.

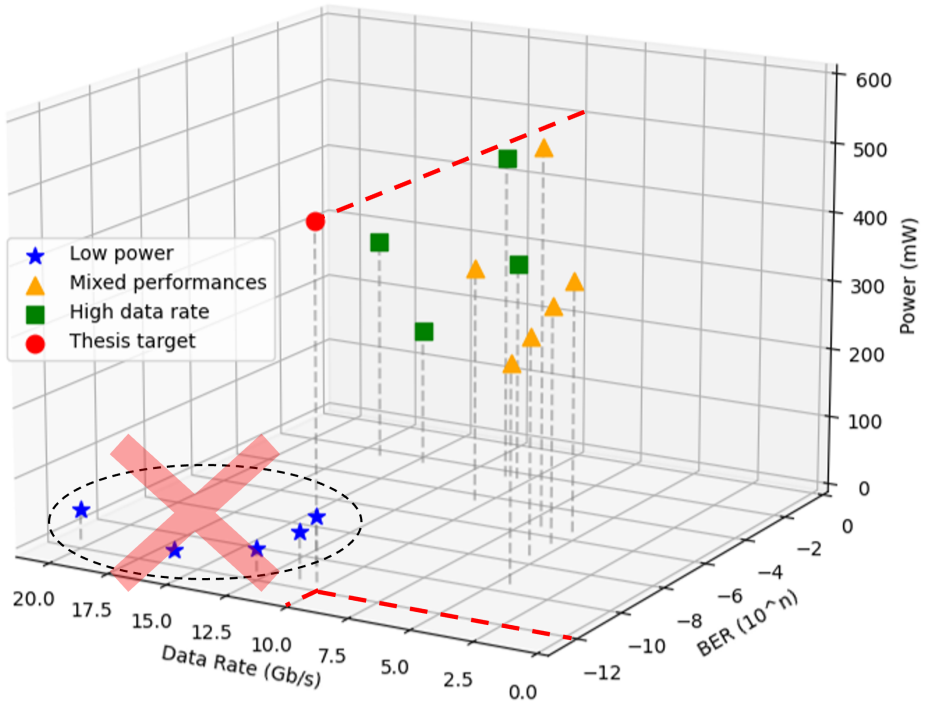


Figure 2.9: Three-axis performance map comparing representative literature to USB-class targets across data rate, BER, and power consumption. The plot highlights that while low-power satisfy all specifications but spectral efficiency thus no architecture simultaneously meets all USB 3.2-class requirements.

Figure 2.9 provides a visual summary of these findings, showing the relative positions of representative architectures in terms of data rate, BER, and power consumption. It clearly illustrates that existing solutions fall short of the combined USB-class targets: low-power designs approach the energy target but fail in modulation efficiency and throughput; high-performance architectures reach extreme data rates but incur prohibitive power and BER penalties; and mixed-performance transceivers occupy intermediate space without fully satisfying any of the USB-class metrics.

This consolidated analysis—both qualitative and quantitative—confirms the central conclusion of the chapter: no existing 60 GHz transceiver simultaneously satisfies the combined requirements of USB 3.2-class wireless communication. The performance gap revealed here motivates the novel architectural explorations presented in the following chapters, where system-level trade-offs and circuit-level innovations will be investigated to achieve a practical, integrated wireless USB interface.

In this context, homodyne architectures emerge as a promising baseline due to their ability to support coherent modulation while maintaining a reasonable level of integration. However, reaching the required level of reliability calls for innovations beyond conventional implementations, notably in the design of reconfigurable RF front-ends, dynamic gain control mechanisms, and calibration strategies to mitigate LO feedthrough and I/Q impairments.

For these reasons, the next chapter develops a comprehensive system-level analysis of the transceiver. Its objective is to establish a quantitative link budget, derive performance specifications for each circuit block, and identify the key architectural trade-offs that will guide the design of a practical 60 GHz wireless USB transceiver.

Chapter 3

Architecture Study

A rigorous system-level analysis is therefore required before any circuit-level decisions can be meaningfully justified. This chapter develops this foundation by quantifying the link budget, establishing the performance allocations for each transceiver block and identifying the architectural trade-offs that govern feasibility. Only once these constraints are formally derived can the thesis address, in a later stage, which circuit techniques are appropriate to meet the resulting specifications.

3.1 Minimal functional RFFE for link-budget exploration

The starting point of this architectural study is the conclusion drawn in Chapter 2: achieving a USB 3.2-class wireless link at 60 GHz requires coherent modulation, strict SNR control, and a compact RF front-end. Among candidate schemes, Quadrature Phase Shift Keying (QPSK) emerges as the minimal viable modulation for this application. With $N_b = 2$ bits per symbol, QPSK achieves the required spectral efficiency to sustain 10 Gb/s within the ~ 7 GHz V-band allocation, while remaining relatively insensitive to amplitude perturbations compared to ASK or PAM4. This robustness is critical in millimeter-wave systems where gain variation and LO feedthrough can degrade amplitude accuracy. Consequently, QPSK offers a favorable trade-off between complexity and reliability for short-range high-throughput links.

To minimize latency and circuit overhead, the architecture adopts a single frequency down-conversion stage (direct conversion or low-IF). Intermediate IF stages are excluded because they increase design complexity and power consumption without clear benefit for the targeted range and bandwidth.

3.1.1 Definition of a minimal RFFE

The proposed minimal Radio Frequency Front-End (RFFE) consists of six analog blocks: three in transmit (driver buffer, up-conversion mixer, power amplifier) and three in receive (low-noise amplifier, down-conversion mixer, baseband amplifier). Digital equalization, forward-error correction, and protocol-specific processing are deliberately omitted; the objective is to establish RF-only feasibility under the constraints derived in Chapter 1.

This choice reflects two practical considerations:

- Published 60 GHz transmitters exhibit similar output power and PA classes for short-range links, leaving limited architectural leverage on the Tx side.
- The receiver chain offers greater flexibility for reconfiguration and gain distribution without violating regulatory power limits. Increasing transmit power would greatly increase DC consumption and linearity requirements.

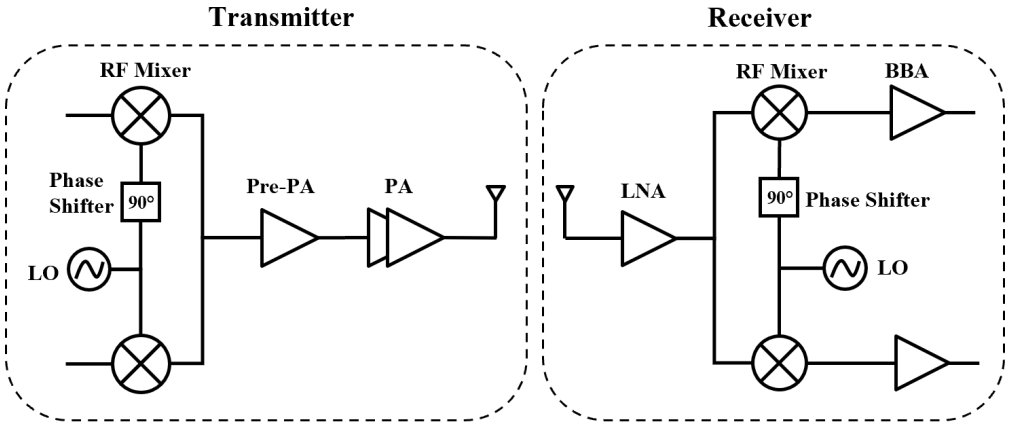


Figure 3.1: Proposed minimal 60 GHz RFFE architecture for QPSK modulation.

3.1.2 Link-budget constraints

The link budget is defined at the demodulator input. A conservative threshold for error-free QPSK demodulation is:

$$\mathrm{SNR}_{\mathrm{min}} = 17 \text{ dB}, \tag{3.1}$$

which preserves margin against impairments such as phase noise, I/Q mismatch, and LO leakage. The minimum input power required by the ADC/demodulator chain is:

$$P_{\mathrm{Rx,out}}^{\mathrm{min}} = -20 \text{ dBm}. \tag{3.2}$$

On the transmit side, we assume a nominal radiated power of $P_{\mathrm{Tx}} \approx 0$ dBm at the antenna. Channel attenuation over millimeter-to-centimeter ranges is dominated by free-space path loss (FSPL):

$$\mathrm{FSPL(dB)} = 20\log_{10}(d) + 20\log_{10}(f) + 32.44, \tag{3.3}$$

with d in kilometers and f in megahertz. At 60 GHz, FSPL is approximately 22 dB at $d = 5$ mm and 42 dB at $d = 5$ cm. These figures constrain the Rx gain and noise figure allocations.

Table 3.1: High-level specifications for link-budget analysis.

Parameter	**Target Value**
Modulation	QPSK
Data rate	10 Gb/s
Bandwidth	7 GHz (57−64 GHz)
Tx power	0 dBm
Rx output power	−20 dBm
SNR at demodulator	17 dB
Communication range	0.5−5 cm

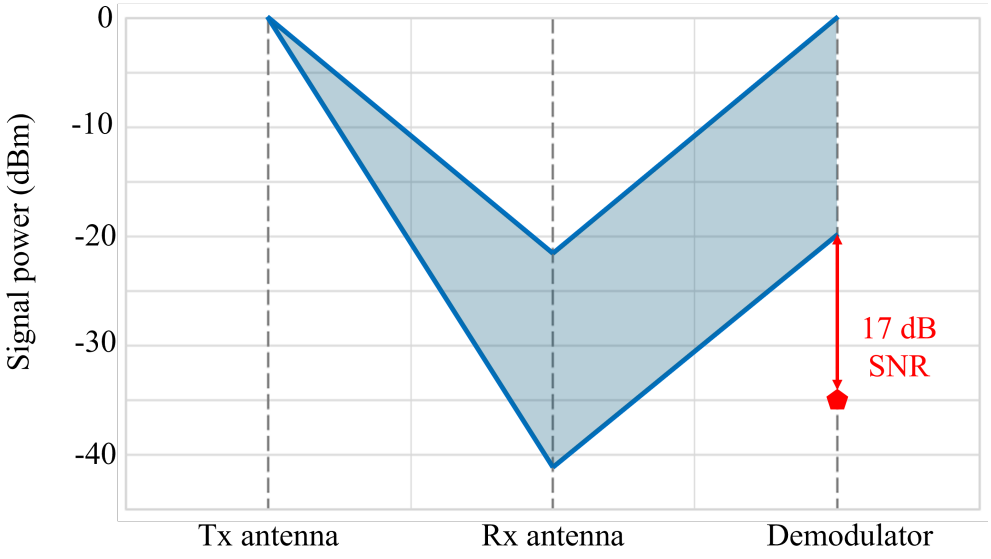


Figure 3.2: Illustrative link budget for a 60 GHz short-range QPSK link.

3.1.3 Noise and gain allocation

Cascaded noise and gain allocations are handled using Friis' formula:

$$F_{\text{tot}} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots , \tag{3.4}$$

where F_i and G_i denote the noise factor and gain of each Rx block. The effective noise figure is $\text{NF}_{\text{tot}} = 10 \log_{10}(F_{\text{tot}})$. The Rx chain must satisfy:

$$\text{SNR}_{\text{Rx,out}} \geq \text{SNR}_{\text{min}}, \qquad P_{\text{Rx,out}} \geq P^{\text{min}}_{\text{Rx,out}}. \tag{3.5}$$

Finally, to frame the design space, performance ranges for each Rx block (LNA, mixer, BBA) are extracted from the state of the art. These ranges define an envelope of achievable $(\text{Gain}, \text{NF}, \text{linearity}, \text{BW})$ combinations. Within this envelope, multiple receiver arrangements are admissible, including single-stage and multi-stages LNAs or mixer-first topologies, each trading off complexity, silicon footprint, and power. The next sections leverage these ranges to size candidate chains and to identify architectures compatible with circuit-level development.

3.2 Design flow for rapid evaluation of RFFE performance distributions

The design space defined in Section 3.1 spans a very large number of possible combinations of gain, noise figure, and linearity across the RF blocks. Exhaustively exploring this space through full system simulations would be prohibitively time-consuming. To address this challenge, we adopt a three-step design flow that enables rapid screening of candidate architectures while maintaining sufficient accuracy for link-budget validation.

3.2.1 Motivation for a structured design flow

The primary objective is to identify promising topologies without committing to detailed transistor-level design at this stage. A brute-force approach is selected for the initial exploration because it guarantees coverage of the entire performance envelope. While heuristic or machine-learning methods could be considered, the brute-force method implemented in C++ provides a pragmatic balance between speed and completeness. Comparative benchmarks confirm that the C++ implementation achieves one of the shortest and most efficient

runtime for large-scale evaluations [30][31], as illustrated in Table 3.2. It is also a perfect language to manipulate objects.

Total					
	Energy		Time		Mb
(c) C	1.00	(c) C	1.00	(c) Pascal	1.00
(c) Rust	1.03	(c) Rust	1.04	(c) Go	1.05
(c) C++	1.34	(c) C++	1.56	(c) C	1.17
(c) Ada	1.70	(c) Ada	1.85	(c) Fortran	1.24
(v) Java	1.98	(v) Java	1.89	(c) C++	1.34
(c) Pascal	2.14	(c) Chapel	2.14	(c) Ada	1.47
(c) Chapel	2.18	(c) Go	2.83	(c) Rust	1.54
(v) Lisp	2.27	(c) Pascal	3.02	(v) Lisp	1.92
(c) Ocaml	2.40	(c) Ocaml	3.09	(c) Haskell	2.45
(c) Fortran	2.52	(v) C#	3.14	(i) PHP	2.57
(c) Swift	2.79	(v) Lisp	3.40	(c) Swift	2.71
(c) Haskell	3.10	(c) Haskell	3.55	(i) Python	2.80
(v) C#	3.14	(c) Swift	4.20	(c) Ocaml	2.82
(c) Go	3.23	(c) Fortran	4.20	(v) C#	2.85
(i) Dart	3.83	(v) F#	6.30	(i) Hack	3.34
(v) F#	4.13	(i) JavaScript	6.52	(v) Racket	3.52
(i) JavaScript	4.45	(i) Dart	6.67	(i) Ruby	3.97
(v) Racket	7.91	(v) Racket	11.27	(c) Chapel	4.00
(i) TypeScript	21.50	(i) Hack	26.99	(v) F#	4.25
(i) Hack	24.02	(i) PHP	27.64	(i) JavaScript	4.59
(i) PHP	29.30	(v) Erlang	36.71	(i) TypeScript	4.69
(v) Erlang	42.23	(i) Jruby	43.44	(v) Java	6.01
(i) Lua	45.98	(i) TypeScript	46.20	(i) Perl	6.62
(i) Jruby	46.54	(i) Ruby	59.34	(i) Lua	6.72
(i) Ruby	69.91	(i) Perl	65.79	(v) Erlang	7.20
(i) Python	75.88	(i) Python	71.90	(i) Dart	8.64
(i) Perl	79.58	(i) Lua	82.91	(i) Jruby	19.84

Table 3.2: Simulation runtime and efficiency scaling for different programming language. [31]

The complete simulation flow is illustrated in Fig. 3.3. It consists of three stages, each offering a different trade-off between accuracy and computational cost. The first stage employs a brute-force algorithm implemented in C++, which performs a coarse evaluation of the design space by testing from thousands to several million performance combinations using a simplified link-budget model. This approach ensures exhaustive coverage while maintaining low runtime.

The second stage refines the analysis using Matlab, where the link budget computed in the first step is validated with additional parameters such as insertion losses and phase noise. This step is more time-consuming, and only a limited number of configurations (typically ten to twenty) are examined. If a candidate fails to meet the constraints at this stage, the process returns to the C++ algorithm for further exploration.
Finally, the most promising RFFE configurations are validated through a detailed Simulink testbench based on the *RF Blockset* library. This environment models the complete transmission chain, including QPSK modulation and RF impairments, and provides accurate metrics such as EVM and constellation integrity.

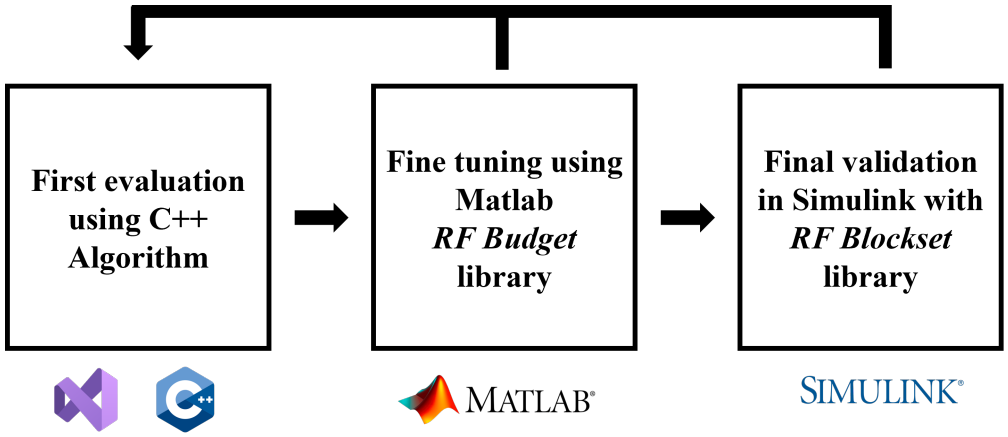


Figure 3.3: RF transceiver design flowchart

3.2.2 Step 1: C++ brute-force evaluation

The first stage consists of a C++ program that enumerates all possible combinations of block-level performances within predefined ranges. Each block is characterized by its gain, noise figure, and linearity (ICP1, IIP3), and the algorithm computes the cascaded link budget using analytical equations:

$$\mathrm{SNR}_{\mathrm{out}}(\mathrm{dB}) = P_{\mathrm{Tx}}(\mathrm{dBm}) - \mathrm{FSPL}(\mathrm{dB}) + \sum G_i(\mathrm{dB}) - \mathrm{NF}_{\mathrm{tot}}(\mathrm{dB}) - N_{\mathrm{floor}}(\mathrm{dBm}), \quad (3.6)$$

where $\mathrm{NF}_{\mathrm{tot}}$ is obtained from Friis' formula (Eq. 3.4). The program outputs the top N configurations satisfying the constraints :

$$\mathrm{NF}_{\mathrm{tot}} \leq 13 \text{ dB} \quad \text{and} \quad \mathrm{G}_{\mathrm{tot}} \geq 22 \text{ dB}. \quad (3.7)$$

G_{tot} being the minimum gain to ensure demodulation ($-20dBm$ at demodulator input) at maximum distance ($42dB$ FSPL at 5cm distance).
As the study progressed, linearity constraints were introduced and weight factors were applied across metrics in order to identify the most relevant lineups.

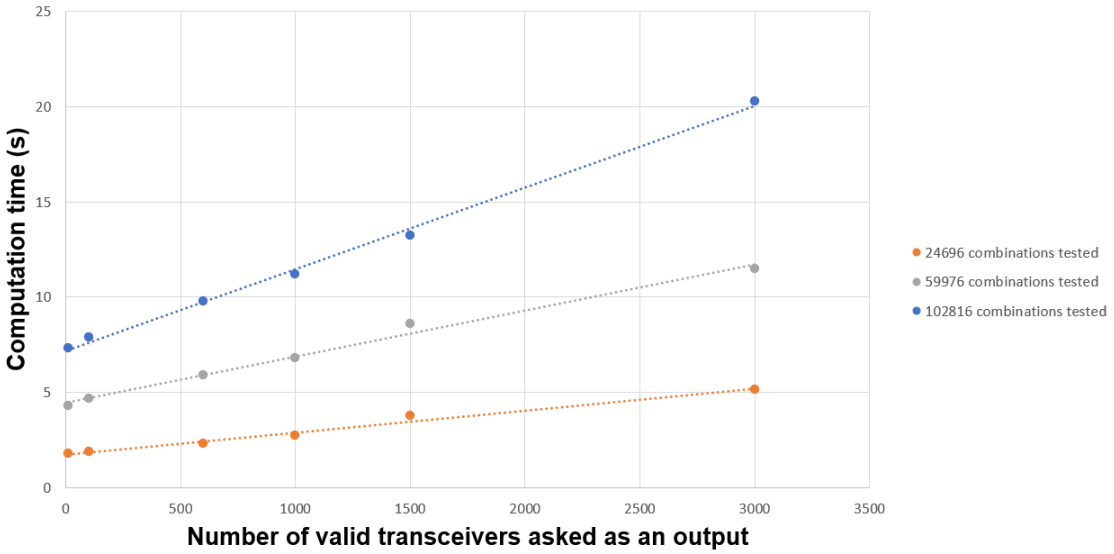


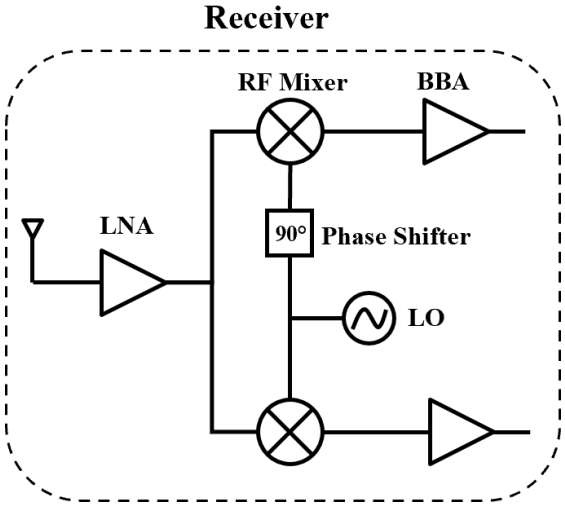
Figure 3.4: Transceivers link-budget analysis C++ program computation time.

This C++ program can evaluate a very large number of combinations within a short computation time (Fig. 3.4). An early issue was that a significant part of the evaluated transceivers satisfied link-budget requirements. This was largely due to the excessively wide performance ranges assigned to each block which caused the algorithm to systematically select configurations combining the highest gain with the lowest NF. These combinations are either unrealistic from an integrated circuit design perspective or incompatible with the low power philosophy pursued in this thesis.

The solution issued was to refine ranges for link-budget constraints by defining realistic yet relaxed performance ranges, notably by setting an upper bound on the total gain of the lineup and a lower bound for the noise figure, setting linearity constraints accordingly. These additional constraints prevented the algorithm from converging toward unrealistic combinations and enabled for novel performances distributions to rise.

Here is an example for new specifications :

$$6 \text{ dB} \leq \text{NF}_{\text{tot}} \leq 13 \text{ dB} \quad \text{and} \quad 30 \text{ dB} \geq \text{G}_{\text{tot}} \geq 22 \text{ dB}. \tag{3.8}$$



Example of an unrealistic RF receiver

	LNA	RF Mixer	BBA
Gain (dB)	25	12	18
NF (dB)	4	6	10

Example of a realistic RF receiver

	LNA	RF Mixer	BBA
Gain (dB)	18	-4	15
NF (dB)	6	10	12

Figure 3.5: Example of an unrealistic and a realistic Rx lineup performances issued from C++ program computation.

The outcome of the C++ exploration serves only as a first-order approximation of the feasible design space. To confirm the validity of these preliminary results, the workflow then transitions to Matlab, where the same configurations are re-evaluated using a more detailed and accurate link-budget model.

3.2.3 Step 2: Matlab link-budget validation

The second stage refines the analysis using Matlab's `RF Budget` library. This step validates the feasibility of the configurations identified in Step 1 by incorporating additional parameters such as insertion losses and bandwidth limitations. Matlab also enables sensitivity studies by varying individual block performances in real time, which is impractical in the C++ brute-force environment.

Figure 3.6 gives an example of an exhaustive description of the receiver side of the transceiver, including filters *, LNA, demodulation blocks and baseband amplifier.

```
%% RX Part
elements(1) = rfelement('Name','TRSwitch','Gain',-1.3,'NF',2.3,'OIP3',37);
Fcenter = 60.5e9;
BWpass = 7e9;
Z = 132.986;
elements(2) = rffilter('ResponseType','Bandpass',                          ...
    'FilterType','Butterworth','FilterOrder',3,                            ...
    'PassbandAttenuation',10*log10(2),                                     ...
    'Implementation','Transfer function',                                  ...
    'PassbandFrequency',[Fcenter-BWpass/2 Fcenter+BWpass/2],'Zout',50,     ...
    'Name','RF_Filter');
elements(3) = amplifier( 'Name','LNA','Gain',15,'NF',4.5,'OIP3',20,        ...
    'Zin',Z);
elements(4) = amplifier( 'Name','Gain','Gain',10.5,'NF',6.5,'OIP3',23);
elements(5) = modulator('Name','Demod','Gain',-7,'NF',7,'OIP3',10,         ...
    'LO',57e9, 'ConverterType','Down');
Fcenter = 0;
BWpass  = 7e9;
elements(6) = rffilter('ResponseType','Lowpass',                           ...
    'FilterType','Butterworth','FilterOrder',4,                            ...
    'PassbandAttenuation',10*log10(2),                                     ...
    'Implementation','Transfer function',                                  ...
    'PassbandFrequency', 7e9,                                              ...
    'StopbandFrequency',9e9,                                               ...
    'Zout',50,                                                             ...
    'Name','IF_Filter');
elements(7) = amplifier( 'Name','IFAmp','Gain',20,'NF',8.5,'Zin',Z);
elements(8) = amplifier('Name','AGC','Gain',17.5,'NF',4.3,'OIP3',25);
heterodyne = rfbudget( 'Elements',elements,'InputFrequency',60.5e9,
    'AvailableInputPower',-90,'SignalBandwidth',7e9)
```

Figure 3.6: Example of a descriptive code for receiver side using Matlab's *RF Budget* library

Beyond providing a fast evaluation of cascaded gain, noise figure and linearity, this library made it possible to study sensitivity of the system in real time. By adjusting the performance of individual block, it was possible to immediately observe their impact on the overall link budget. This feature allowed to identify dominant contributors to degradation and to refine the performance ranges in the previous step. Although, this analysis could have been carried out using an Excel spreadsheet. The main purpose of using this Matlab's library is the ability to generate a model of the current lineup in Simulink using *RF Blockset* library.

As discussed above, this analysis remains an analytical approximation based on cascaded static model. It does not account for several key phenomena that strongly influence the

*During the early system-level simulations, the receiver lineup included an input band-pass filter and an output low-pass filter in order to suppress sidebands and potential interferers. However, in the specific context of this application (very short range communication dominated by high FSPL) the impact of cross-talk and external interference was found to be negligible. A preliminary study confirmed that these impairments contributed only marginal variations in the simulated SNR and EVM. For this reason, the filtering stages were subsequently removed from the analysis.

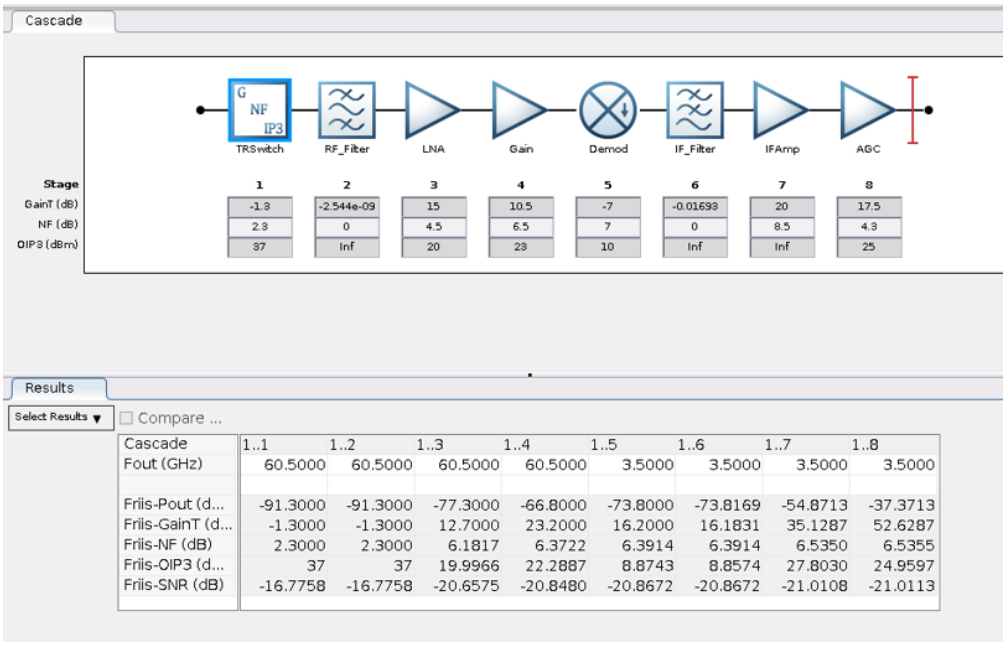


Figure 3.7: Real-time parameter sensitivity analysis carried out with Matlab's *RF Budget* library

demodulation quality at 60 GHz, such as spectral distortion, EVM degradation, LO phase noise of I/Q impairments. To capture these effects and assess the actual robustness of a candidate lineup, the study requires a more complete system-level analysis. The final step relies on a Simulink testbench, where architectures are simulated in time and frequency domains, enabling direct observations of the spectrums, constellations, EVM and resulting BER. This progression from analytical to behavioral evaluation ensures that only the most suited lineups are considered.

3.2.4 Step 3: Simulink system-level testbench

The final stage employs a Simulink testbench based on the *RF Blockset* library. This environment models the complete transmission chain, including QPSK modulation, RF impairments, and baseband processing. It enables visualization of frequency spectrum, constellation diagrams, and error vector magnitude (EVM), providing a realistic assessment of demodulation quality. While this step is computationally intensive, it is applied only to the most promising configurations identified in previous steps.

As represented in Fig.3.8, the simulation bench is composed of five distinct elements : digital modulation and demodulation (green), the RF front-end split between transmitter and receiver (blue) and the modelisation of the channel (red). Exhaustive representation of RF Transmitter and RF Receiver are given in Fig.3.9 and Fig.3.10 respectively.

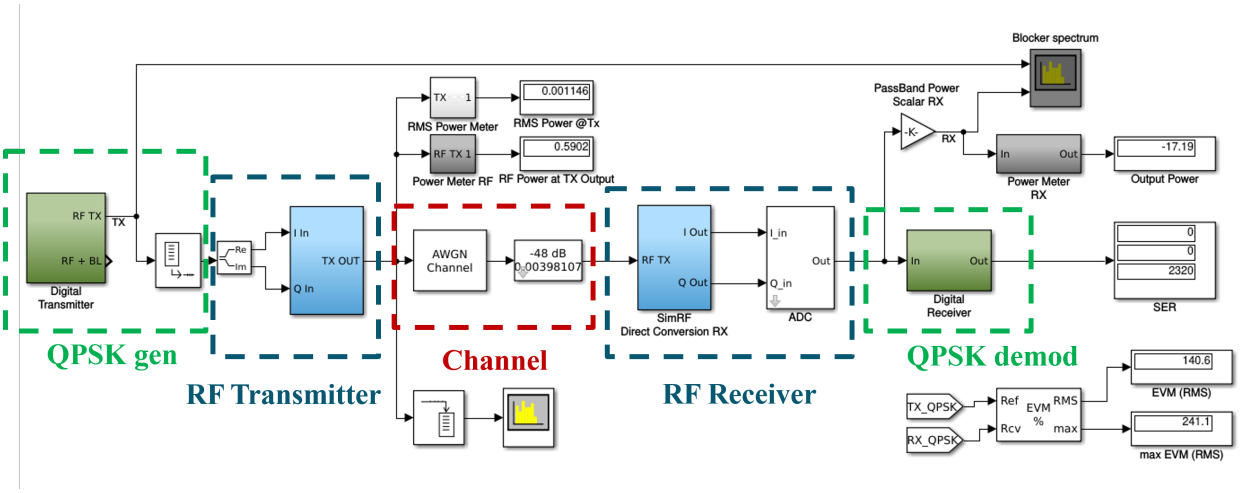


Figure 3.8: Representation of the complete Simulink testbench, including digital modulation and demodulation, RF transmitter and receiver, and channel simple modelization.

The system-level model includes several RF impairments that significantly affect waveform integrity in a 60 GHz link. In particular, the transmitter and receiver blocks incorporate IQ gain imbalance (up to 0.2dB gain imbalance), oscillator phase noise (-130dBc @ 100MHz), and a fixed phase shift ($\Delta\varphi = 0.1\,\text{rad}$), which together emulate realistic non-idealities of mmWave front-ends. The resulting degradation is evaluated through key system metrics, including input and output spectrum, constellation, symbol error rate (SER), and error vector magnitude (EVM). The propagation medium is represented by an AWGN channel with an adjustable path-loss parameter, allowing the effective communication distance at 60 GHz to be emulated by tuning the attenuation level (from 22dB to 48dB losses). The output signal power is also probed to ensure demodulation with a real ADC.

This modelling approach makes it possible to isolate the contribution of each impairment to the overall link degradation. For instance, phase noise primarily broadens the spectrum and increases constellation rotation, while IQ imbalance impacts the symmetry of the constellation points.

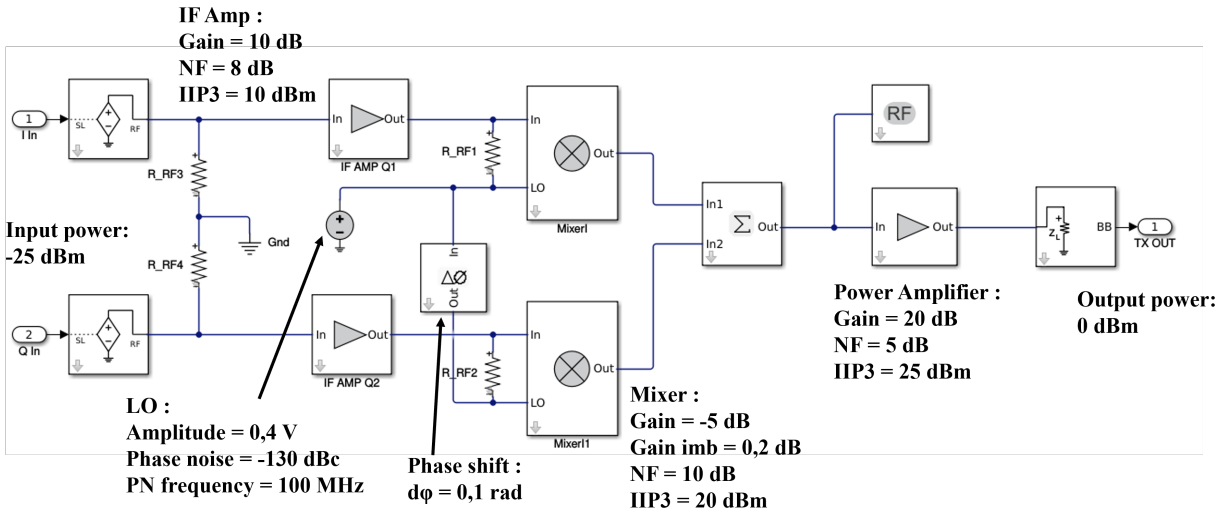


Figure 3.9: Modelisation of RF Transmitter in Simulink using *RF Blockset* library

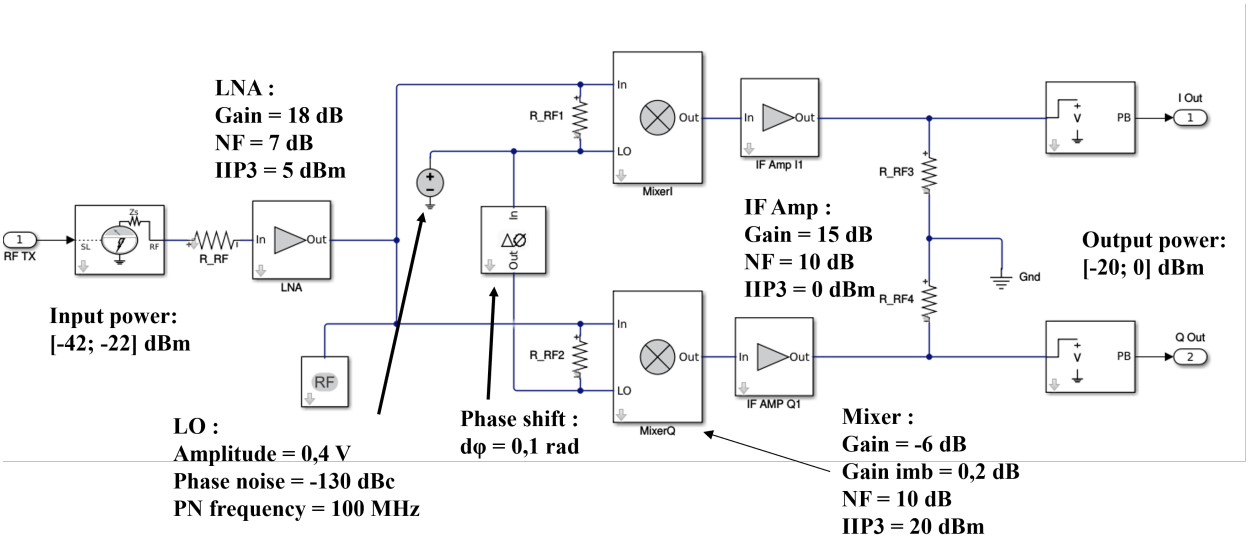


Figure 3.10: Modelisation of RF Receiver in Simulink using *RF Blockset* library

To illustrate the impact of RF impairments on the link robustness, a sensitivity study was performed on a representative RFFE configuration by sweeping the effective communication distance in the 60 GHz band. As shown in Fig. 3.11, the degradation of the received waveform is clearly observable in both the constellation and the baseband spectrum. At short range, the symbols remain tightly clustered and the spectral regrowth is limited, indicating that non-linearities and phase noise remain well within acceptable margins. As distance increases, the additional path loss reduces the received SNR, leading to a progressive spreading of the constellation and a visible rise of the noise floor around the signal bandwidth. While

spectrums and constellations provide qualitative insight, the validation criterion ultimately relies on quantitative metrics (EVM and SER), which jointly indicate the maximum feasible communication distance for the investigated transceiver architecture.

A slow carrier phase drift can be observed in the QPSK constellation, resulting in a gradual rotation of the symbol cloud over time. This effect is mainly driven by LO phase noise and the fixed phase offset introduced in the RF chain. Since no carrier-recovery or phase-tracking mechanism is implemented in the considered architecture, this rotation is left uncompensated and is not accounted for in the performance analysis.

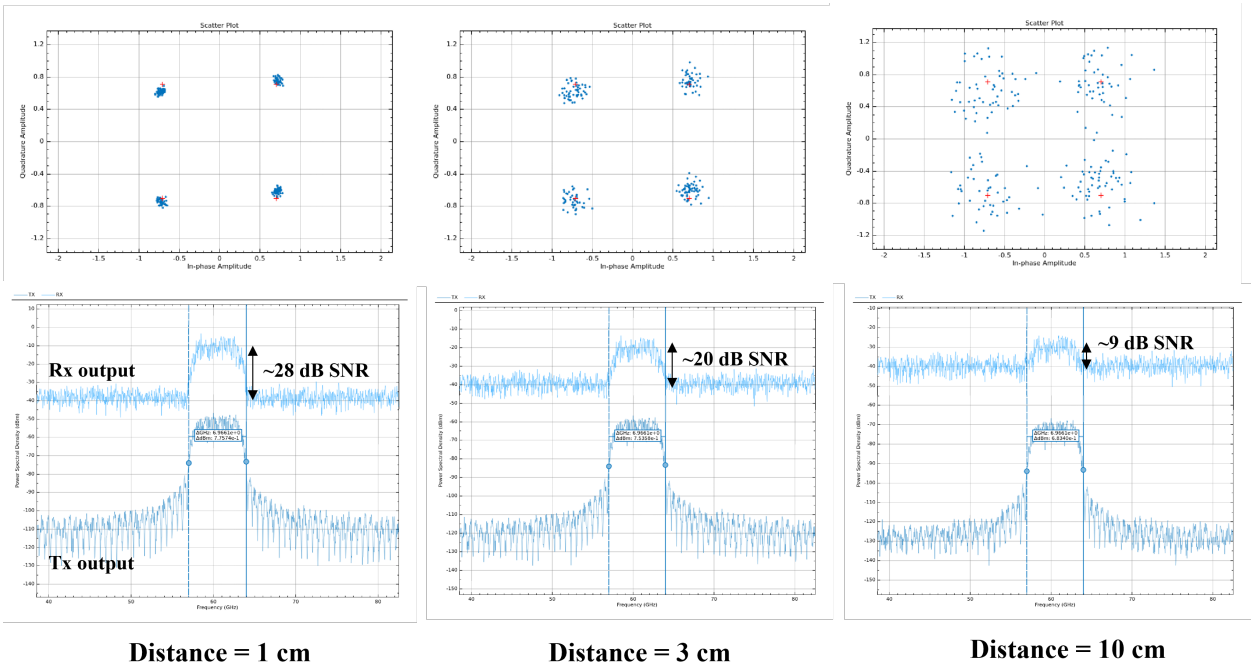


Figure 3.11: Simulink sensitivity evaluation of a candidate RFFE configuration : QPSK constellation and baseband spectrum versus communication distance.

This design flow does not account for all second-order effects such as temperature variation, LO leakage, or DC offsets. Digital equalization and calibration are also excluded. The intent is not to deliver exhaustive system simulations but to identify architectural trends and feasible performance sets for subsequent circuit-level design. Despite these limitations, the methodology significantly accelerates the exploration process and ensures that only viable topologies proceed to detailed implementation.

With the system-level validation stage completed, the analysis now turns to the results obtained for the transceiver architecture. The following section examines the performance of

the investigated configurations and introduces three representative RF front-end design scenarios used to evaluate the trade-offs in gain distribution, noise performance, and waveform integrity.

3.3 Exploration of multiple receiver scenarios

The previous sections established the link-budget constraints and introduced a design flow for rapid evaluation of candidate architectures. In this section, the focus is set on the receiver side of the RFFE, which offers the greatest potential for innovation as discussed in Section 3.1. Three receiver topologies will be presented along with a qualitative analysis for the design complexity and the estimated silicon footprint based on design good-practice and the state-of-the-art.

3.3.1 Methodology and bias considerations

The exploration process relies on the C++ brute-force tool described in Section 3.2. While the algorithm evaluates all feasible combinations within the defined performance ranges, certain weighting were introduced intentionally to accelerate convergence. For instance, the tool prioritizes configurations with the best available LNA, relaxing constraints on subsequent blocks. The main root cause being the use of Friis formulas to simulate the RFFE, thus relying heavily on high gain and low NF on the first stage. This bias reflects the dominant role of this component in determining overall sensitivity and SNR margin. Nevertheless, alternative topologies such as mixer-first architectures were also considered to assess their feasibility despite higher design complexity.

To force the C++ program to assess alternative architecture, the performances ranges of specific blocks were truncated to reflect the state-of-the-art for each topology. For example, explorations targeting single-stage LNA designs limited the maximum power gain of the block to 13dB.

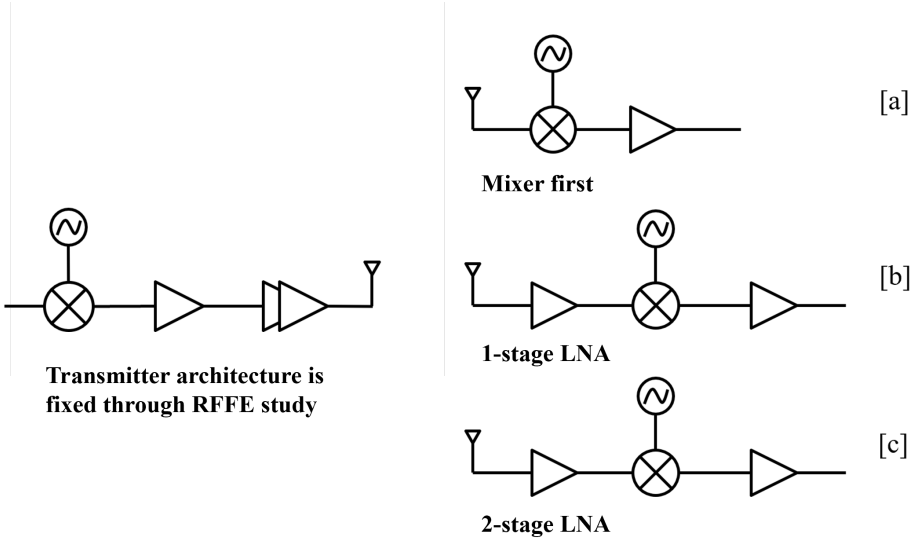


Figure 3.12: Comparative block diagrams for the three scenarios: (a) mixer-first, (b) single-stage LNA, (c) dual-stage LNA.

As discussed previously and illustrated in Fig.3.12, three main RFFE topologies were explored in this architecture study. The next three subsections discuss advantages and drawbacks for each variants together with a critical assessment of practical aspects such as design effort, silicon footprint, and feasibility.

3.3.2 Scenario 1: Single-stage LNA

The first scenario relies on a single-stage LNA followed by a passive down-conversion mixer and a high-gain "baseband" amplifier. Achieving a 7 GHz bandwidth with a single-stage LNA is intrinsically challenging, as modern wideband millimeter-wave designs typically exploit multi-stage amplification featuring multiple sub-band operation to cover an overall large bandwidth by concatenation of the sub-band responses. The sub-band operation is ensured by the implementation of low-coupled inter-stage networks. In the present architecture, however, the LNA provides no interstage matching and must rely solely on input and output matching networks, likely transformer-based, whose insertion loss becomes difficult to offset given the limited intrinsic gain of a single-stage amplifier.

Maintaining both bandwidth and noise performance under these constraints quickly approaches the limits of the state of the art, especially if the RFFE is restricted to passive mixing to minimize power consumption. Although Friis-based system exploration suggests that such a chain can meet sensitivity requirements, a practical implementation would almost certainly require an active mixer to recover sufficient gain and conversion efficiency. Finally, the so-called baseband amplification stage effectively behaves as a wideband RF amplifier with a usable bandwidth of 5.5 GHz, as demonstrated in [32], and its design remains highly complex regardless of the chosen receiver architecture.

3.3.3 Scenario 2: Two-stage LNA

Adding a second gain stage in the LNA relaxes several constraints across the receiver chain, starting with the design complexity to comply with bandwidth specifications of the LNA itself. With two cascaded amplification stages, the overall gain is high enough that noise requirements on the mixer and BBA are significantly eased. The mixer, in particular, can consider passive topologies more confidently, since the LNA now provides sufficient front-end gain to offset their inherent conversion loss. At the baseband level, the BBA remains the most bandwidth-constrained block, but its noise and gain requirements are more manageable due to the elevated RF gain beforehand.
This two-stage configuration therefore offers the most design flexibility among the explored options, due to a more balanced distribution of gain and noise figure constraints across the receiver chain, at the cost of a larger silicon footprint resulting from the additional inductors and matching networks. Despite this trade-off, it remains the preferred RFFE topology for the continuation of this work, providing a favorable balance between performance robustness, design feasibility, and integration targets.

3.3.4 Scenario 3: Mixer-first architecture

The third scenario completely removes the LNA and adopts a mixer-first strategy, where a high-performance active mixer directly interfaces with the antenna path, followed by a baseband amplifier to recover the required gain. Such architectures remain uncommon in mmWave transceivers because they place unusually high demands on the mixer. At these frequencies, the noise figure of active mixers is generally too elevated to meet the SNR target without prior LNA. Nevertheless, under the specification set considered in this study, the system-level analysis confirms that the required link performance can still be achieved, indicating that this approach is not ruled out in principle. This topology would offer the

smallest silicon footprint among the evaluated options since it removes the LNA and its associated passive components.
However, despite comprising only two blocks, it remains the most demanding architecture from a design standpoint: the mmWave active mixer and the wideband baseband amplifier are, across all scenarios considered, the most challenging blocks to implement in terms of noise figure, bandwidth, and linearity.

3.3.5 Performance validation

The feasibility of the three receiver scenarios was evaluated through system-level Simulink simulations using the testbench described in Section 3.2. Figure 3.13a reports the link-budget evolution across the RF chain for a 5 cm communication distance and a data rate of 10 Gb/s. The single-stage and two-stage LNA architectures exhibit comfortable margins with respect to both the minimum received power and the SNR requirement, owing to their lower front-end noise figure and higher available RF gain. In contrast, the mixer-first topology operates much closer to the specification limits: its limited signal power at the mixer input and the inherently higher noise figure of active mixers at mmWave frequencies result in a reduced SNR margin.

Despite these differences, all three scenarios satisfy the target SNR, enabling a BER below 10^{-12} with a QPSK modulation. Figure 3.13.b illustrates representative constellation diagrams and baseband spectra. The two LNA-based architectures reach approximately 20 dB SNR, while the mixer-first configuration achieves around 18 dB, which remains compliant with the required demodulation performance of $\mathrm{SNR}_{\mathrm{min}} = 17dB$. The spectra also show that the effective signal bandwidth is preserved across architectures, confirming that the assumed block-level models meet the system-level bandwidth requirement.

It is important to note that these results rely on high-level models and state-of-the-art performance assumptions for the RF and baseband blocks. The simulations therefore validate the feasibility of each scenario from a system perspective, but they do not account for transistor-level constraints such as device parasitics, mixer linearity under large LO drive, or gain-bandwidth limitations in the baseband amplifier. Nevertheless, the comparative analysis highlights the sensitivity of each architecture to noise and gain distribution and confirms that all three remain viable candidates under the explored assumptions.

Table 3.3: RF blocks performances for [a] Transmitter, [b] Single-stage LNA Rx, [c] Two-stage LNA Rx, and [d] Mixer-first Rx.

[a] Transmitter

	Mixer	**Pre-PA**	**PA**	**Total Tx**
Gain (dB)	-4	15	20	25.5
NF (dB)	8	12	12	17.7
IIP3 (dBm)	0	5	15	-1.1
DC Power (mW)	10	20	60	90
Design complexity	Low	Med.	High	Med
Silicon footprint	Med.	Med.	High	High

[b] Single-stage LNA

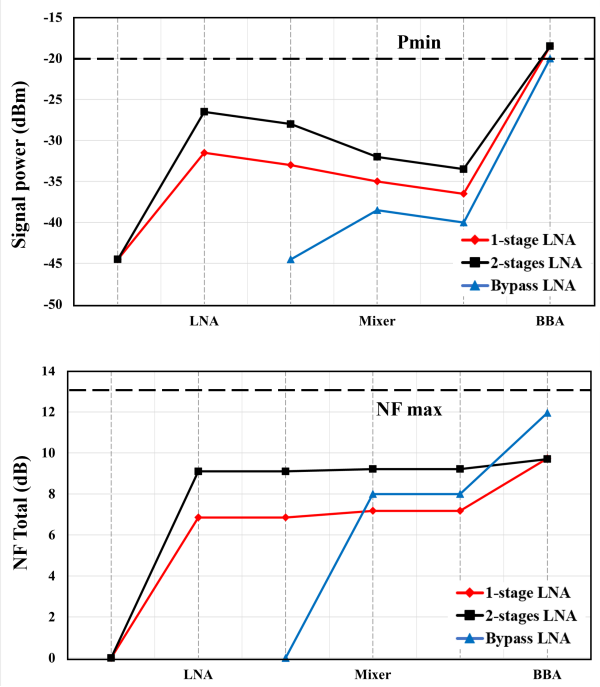
	LNA	**Mixer**	**BBA**	**Total Rx**
Gain (dB)	13	-2	18	23.5
NF (dB)	5	6	12	9.7
IIP3 (dBm)	0	0	10	-9.5
DC Power (mW)	15	20	25	60
Design complexity	Med.	Med.	Med.	Moderate
Silicon footprint	Low	Med.	Med.	**Low**
Reference	[33]	[34]	[32]	

[c] Two-stage LNA

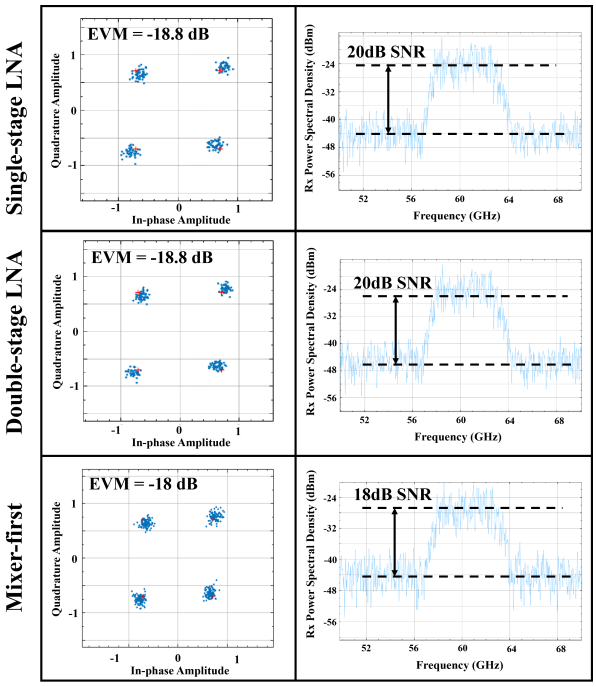
Gain (dB)	18	-4	15	23.5
NF (dB)	7	8	9	9.7
IIP3 (dBm)	0	0	10	-12.5
DC Power (mW)	25	20	20	65
Design complexity	Low	Low	Med.	**Low**
Silicon footprint	Med.	Med.	Med.	**Moderate**
Reference	[35]	[36]	[32]	

[d] Mixer-first

Gain (dB)	/	6	20	22
NF (dB)	/	6	12	11.9
IIP3 (dBm)	/	0	10	-3.3
DC Power (mW)	/	25	20	45
Design complexity	/	High	Med.	High
Silicon footprint	/	Med.	Low	**Low**
Reference	/	[37]	[32]	



(a) Link budget analysis for single-stage LNA, dual-stage LNA, and mixer-first architectures.



(b) Simulink validation of demodulation quality for the three receiver scenarios.

Figure 3.13: Transceiver-level performances analysis for the three receiver scenarios.

3.3.6 Discussion

The system-level evaluation highlights that none of the three receiver scenarios provides a universally optimal solution across all performance metrics. The single-stage LNA architecture remains attractive for its moderate complexity and limited silicon footprint, but its modest RF gain places tighter requirements on both the mixer and the BBA. The dual-stage LNA configuration offers a more favorable distribution of gain and noise contributions, resulting in larger margins with respect to the minimum received power and SNR constraints. This scenario provides the most robust link-budget behavior and therefore constitutes the most balanced option among the evaluated architectures. The mixer-first approach, while enabling the smallest area, operates closer to the specification limits due to the inherently higher noise figure of active mixers at mmWave frequencies. As such, its feasibility strongly depends on aggressive circuit-level optimization.

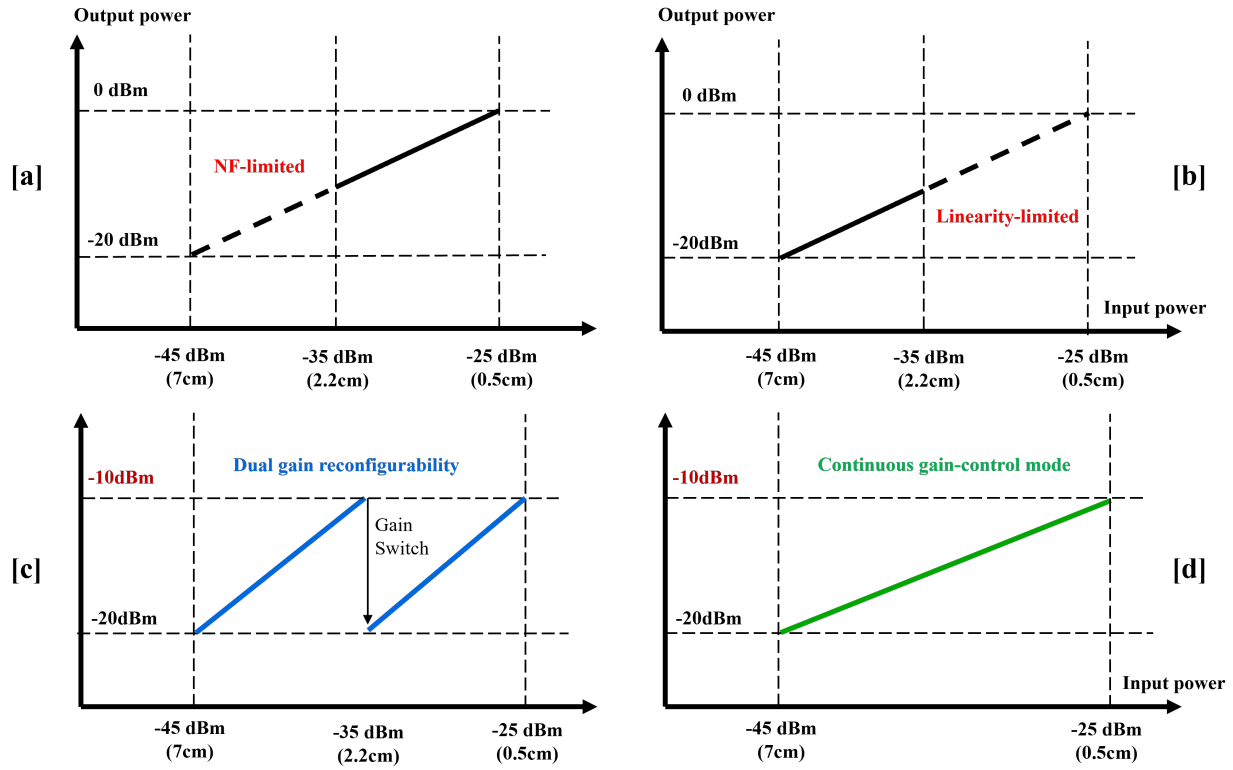


Figure 3.14: Link budget limitations according to different design scenarios : [a] one-stage LNA and [b] two-stage LNA along with simplified link budget of two gain reconfiguration techniques commonly used in mmW LNA design : [c] two gain mode switch and [d] continuous gain reconfigurability.

The analysis of the input–output characteristics of the single-stage and dual-stage LNA architectures further highlights the limitations of fixed-gain front-ends in the context of short-range mmWave links. As illustrated in Fig. 3.14, the single-stage LNA reaches its operational limits when the received signal is weak, resulting in a limited output swing and degraded sensitivity Fig. 3.14.a. Conversely, the dual-stage LNA offers improved noise and gain performance for low input powers, but it reaches its compression region more rapidly when the received signal is strong, reducing the usable dynamic range at the antenna interface Fig. 3.14.b.

These observations indicate that a fixed-gain configuration can not efficiently cover the full range of input powers associated with varying communication distances. A reconfigurable-gain LNA therefore becomes an attractive solution to extend the admissible input dynamic range while preserving sensitivity under worst-case link-budget conditions. Two main reconfiguration strategies are commonly employed for this purpose. The first approach relies on discrete

gain switching, typically alternating between a low-gain and a high-gain mode Fig. 3.14.c. This method provides coarse adaptation with limited hardware overhead, but the discontinuity between modes may leave portions of the link-budget range sub-optimally covered. The second approach implements continuous gain control Fig. 3.14.d, enabling smoother adaptation of the LNA gain and a more uniform coverage of the received-power range. This technique offers greater flexibility from a system perspective, though it generally requires more elaborate circuit implementations.

These considerations motivate the development of a reconfigurable dual-stage LNA capable of providing a gain spanning approximately 10–20 dB while maintaining a noise figure compatible with the most demanding system-level scenarios. The next chapter therefore focuses on the circuit-level design of such a mmWave LNA, examining the techniques required to achieve robust and controllable gain reconfiguration while preserving bandwidth, linearity, and noise performance.

Chapter 4

Design of a reconfigurable LNA

The architectural study conducted in Chapter 3 highlighted a central limitation of fixed-gain front-ends at 60 GHz: none of the investigated receiver scenarios can maintain optimal performance across the full range of input powers associated with the targeted short-range wireless USB 3.2 link. The single-stage LNA lacks gain at low received power, while the two-stage configuration reaches compression more rapidly when the received signal is strong. These observations motivate the development of a reconfigurable low-noise amplifier capable of extending the admissible dynamic range at the antenna interface.

In this chapter, a complete design of such a reconfigurable LNA is undertaken using GlobalFoundries 22 nm CMOS technology. Before addressing circuit-level implementation, a review of existing gain-reconfiguration techniques for millimeter-wave amplifiers is presented to establish the capabilities and limitations of current approaches and to position the requirements derived in Chapter 3. The proposed reconfiguration concept is then introduced and developed in detail, followed by the design of the required passive structures, transistor-level sizing, and topology justification.

The chapter concludes with a full set of simulations and laboratory measurements performed on a complete fabricated chip, enabling a direct comparison between simulation predictions and measured performance.

4.1 Overview of Gain-Reconfigurable LNA design techniques

Before presenting the proposed reconfigurable LNA architecture, it is essential to review the main techniques used to achieve gain control at millimeter-wave frequencies. At 60 GHz, gain reconfiguration must be achieved under strict constraints on noise figure, impedance matching, and bandwidth, which significantly limits the available design space.

Existing approaches can be broadly classified into three categories: (i) transistor-level techniques based on transconductance control through segmentation or biasing, (ii) switch-based architectures that reconfigure the RF signal path, and (iii) passive-based methods relying on impedance tuning through reactive networks or transformers. Each category relies on a different physical mechanism and introduces distinct trade-offs in terms of gain range, linearity, power consumption, bandwidth, and implementation complexity.

It is worth noting that practical implementations often exhibit hybrid behavior, combining multiple of these mechanisms. The classification adopted here therefore reflects the dominant reconfiguration principle. This section provides an overview of these techniques, focusing on their operating principles and intrinsic limitations, in order to define the design constraints of the proposed work.

4.1.1 Transistor Segmentation and Bias Control

Gain reconfiguration can be achieved by directly modifying the effective transconductance g_m of the input device. This is typically implemented either through transistor segmentation, where multiple parallel devices are selectively enabled, or through bias control, where the operating point is adjusted via the drain current, as illustrated in Fig. 4.1.

These approaches are attractive due to their simplicity and compact implementation. However, at millimeter-wave frequencies, variations in g_m are inherently coupled with changes in input impedance and parasitic capacitances (C_{gs}, C_{gd}). As a result, the achievable gain tuning range is limited by the degradation of input matching and bandwidth.

Recent works in the 60–150 GHz range have demonstrated gain variations on the order of 10–15 dB; however, practical implementations typically exhibit a degradation in noise figure (1–3 dB) and linearity when the bias point deviates from its optimum [38, 39]. In addition, bias tuning often leads to a non-uniform frequency response across gain states, since the optimum bias for noise and gain is not identical.

Similarly, segmentation techniques may introduce parasitic loading from inactive branches, which can detune the input matching network and further limit the usable bandwidth. These limitations motivate the exploration of alternative architectures that decouple gain control from the active device biasing.

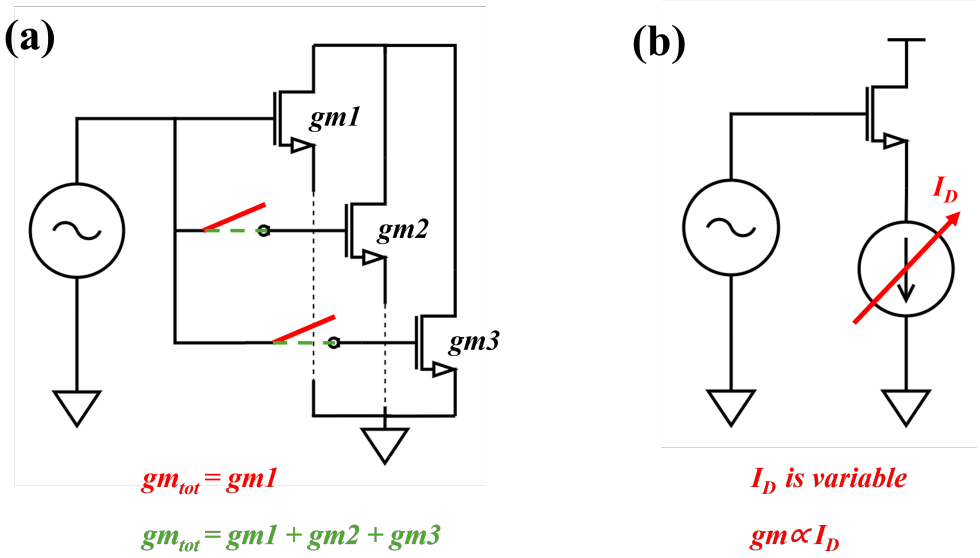


Figure 4.1: Gain reconfiguration using transistor-level techniques: (a) transistor segmentation through selective activation of parallel devices, and (b) bias tuning by adjusting the operating current, resulting in variations of the effective transconductance and gain.

4.1.2 Switch-Based Reconfigurable Architectures

Switch-based techniques rely on MOS devices inserted in the RF signal path to reconfigure the amplifier topology. Two main approaches are commonly used: passive RF path switching between different networks, and active lineup switching, where entire amplifier stages are enabled or bypassed, as illustrated in Fig. 4.2.

Passive switching enables discrete gain steps by selecting different matching or attenuation networks. However, the finite on-resistance (R_{on}) of MOS switches introduces insertion loss, while parasitic capacitances (C_{off}) degrade isolation and alter the impedance seen by the amplifier at millimeter-wave frequencies, thereby impacting both noise figure and bandwidth [40].

Active lineup switching provides a larger gain tuning range, typically exceeding 10–15 dB, by selecting between multiple amplification paths [41]. However, this approach increases silicon area and power consumption due to duplicated stages. In addition, inactive branches still contribute parasitic loading, which can degrade input matching.

Recent works have proposed hybrid solutions combining switching and passive tuning to mitigate these limitations, demonstrating improved gain stability with limited noise variation across states. Nevertheless, the fundamental trade-off remains: switching-based architectures inevitably introduce parasitic elements that must be carefully managed at millimeter-wave frequencies.

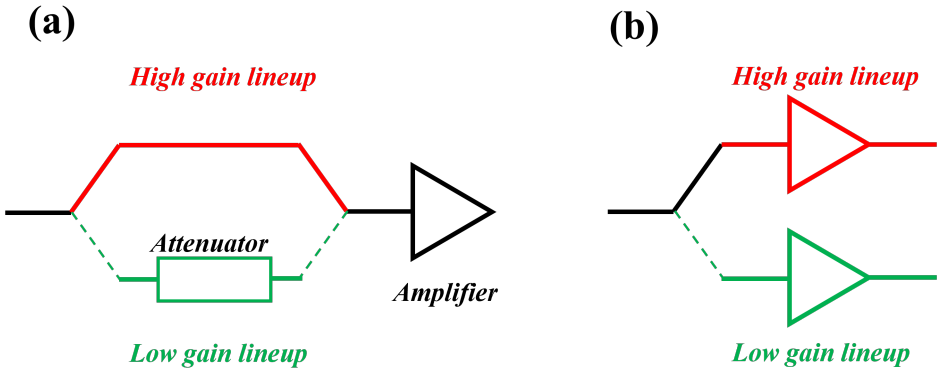


Figure 4.2: Switch-based gain reconfiguration techniques: (a) passive RF path switching, where different matching or attenuation networks are selected, and (b) active lineup switching, where distinct amplifier branches are enabled or bypassed to achieve large gain variation.

4.1.3 Passive-Based Gain Reconfiguration

Passive gain reconfiguration modifies impedance transformations using reactive networks rather than directly altering the biasing of active devices. As illustrated in Fig. 4.3, two main implementations are commonly used: switched passive networks and transformer-based tuning.

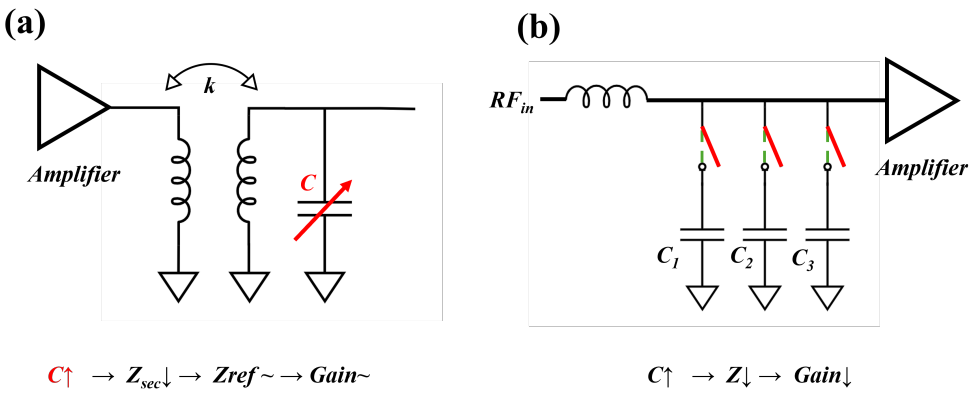


Figure 4.3: Passive gain reconfiguration techniques: (a) transformer-based tuning using a capacitive load at the secondary to modify the reflected impedance, and (b) switched passive network enabling discrete impedance tuning through selectable reactive elements.

Switched networks provide discrete gain steps but suffer from insertion loss and limited tuning range (typically below 8 dB) due to switch parasitics at millimeter-wave frequencies [40]. In addition, the finite on-resistance and parasitic capacitance of MOS switches degrade the effective quality factor of the network, which directly impacts both gain and noise performance.
To overcome these limitations, several works have investigated more continuous or digitally assisted tuning strategies. In particular, impedance-aware reconfiguration techniques have been proposed, where the effective load is dynamically adjusted while preserving input matching and stability across gain states [42]. Such approaches enable finer gain control without significantly perturbing the RF operating point, at the cost of increased control complexity.

Further improvements in continuous gain control can be achieved by dynamically modifying the effective quality factor (Q) of the matching network. One approach relies on Q-enhancement techniques using cross-coupled devices to introduce negative resistance, enabling wide gain tuning ranges (up to 8–12 dB) with limited noise figure degradation, albeit with increased power consumption and stability constraints [43]. Alternatively, tuning the magnetic coupling coefficient of interstage transformers allows continuous gain adjustment while maintaining relatively stable noise performance.

Although passive-based techniques avoid direct modification of the transistor bias point, they often introduce additional design complexity and may impact power efficiency. These trade-offs highlight the challenge of achieving wide and continuous gain control without

degrading overall receiver performance.

4.1.4 Summary and Design Trade-offs

The reviewed techniques highlight a fundamental challenge: there is no single method that simultaneously offers a wide continuous gain range, stable matching, low noise figure, and compact implementation. Each approach involves a specific trade-off between gain range, performance degradation, and complexity.

Table 4.1 summarizes the key characteristics and limitations of the main reconfiguration techniques.

Table 4.1: Comparison of gain reconfiguration techniques for mmWave LNAs.

Technique	**Gain Range**	**Main Drawback**	**Complexity**
Transistor Segmentation	Low (4–6 dB)	Degraded Matching/NF	Low
Bias Tuning	Low (4–6 dB)	Matching shift, NF penalty	Low
Passive Switching	Medium (8–12 dB)	Insertion loss, NF degradation	Medium
Active Lineup (Bypass)	High ($\geq$ 10 dB)	Area overhead, Parasitic loading	High
Transformer/Varactor	Medium (6–10 dB)	Discrete steps or Non-linearity	Medium

4.1.5 Design Strategy for the Proposed LNA

Based on the system-level requirements established in Chapter 3, the proposed LNA must be capable of covering two distinct operational scenarios:

1. **Scenario 1 (Low Power):** A single-stage configuration to maximize linearity and minimize power consumption for strong input signals (short distance).
2. **Scenario 2 (High Sensitivity):** A two-stage configuration to maximize gain and minimize noise figure for weak input signals (long distance).

Given the trade-offs identified in Table 4.1, the most straightforward approach to satisfy these two specific scenarios is an **active lineup switching** strategy, where the second amplification stage is bypassed or disabled. This method offers the largest gain range (transitioning from single-stage to two-stage gain) and avoids the continuous matching degradation associated with bias tuning or segmentation.

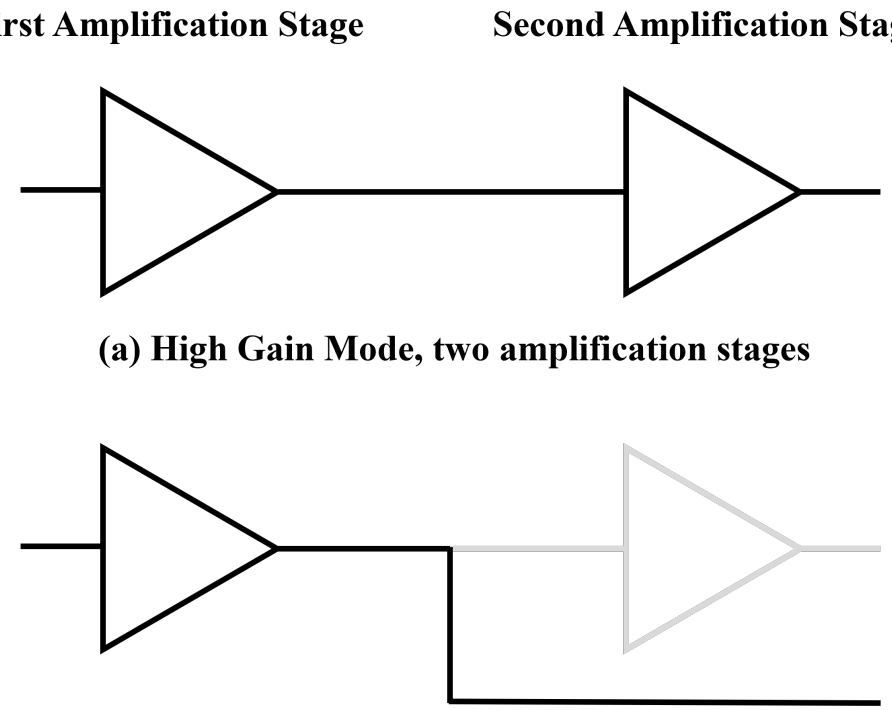


Figure 4.4: Gain reconfiguration technique opted for this LNA design.

Therefore, the initial design of the reconfigurable LNA focuses on implementing a robust two-stage topology with a mechanism to effectively bypass the second stage. This approach directly addresses the dynamic range requirements of the short-range mmWave link. However, as will be discussed in Section 4.4.3, this discrete switching method presents limitations in terms of granularity and system flexibility, motivating the exploration of a continuous gain control mechanism in the subsequent design phase.

4.2 Design of low-coupled stacked inductors

In millimeter-wave CMOS technologies, on-chip passive components constitute a major contributor to silicon area. Inductors, in particular, remain among the most limiting structures due to the need for magnetic isolation between adjacent components and the degradation of their quality factor at high frequencies. [44, 45] For multi-stage amplifiers and transformer-based interstage networks, this constraint often results in layout footprints significantly larger than those of the active devices themselves. To overcome these limitations, this work employs a design methodology based on the vertical superposition of inductive structures with controlled geometric symmetry. This approach enables the cancellation of magnetic coupling between stacked windings, thereby suppressing the mutual inductance while preserving the intrinsic inductance value and RF performance of each element. The method provides a compact and scalable solution for realizing inductors and multi-winding transformers suitable for millimeter-wave reconfigurable circuits.

4.2.1 Concept and theoretical basis

The principle underlying the proposed technique is the cancellation of magnetic coupling between vertically superposed inductors. When two conductive loops carrying currents I_1 and I_2 are placed in close proximity, their mutual inductance M is governed by the classical Neumann integral:

$$M = \frac{\mu_0}{4\pi} \oint_{C_1} \oint_{C_2} \frac{\mathrm{d}\vec{l_1} \cdot \mathrm{d}\vec{l_2}}{\|\vec{r_1} - \vec{r_2}\|}, \tag{4.1}$$

where C_1 and C_2 denote the contours of the two inductive structures. For regular and symmetric geometries (e.g. octagons or squares), the contributions to M can be decomposed into pairs of elemental interactions. By vertically shifting the two structures by a specific fraction of their outer diameter, these contributions cancel pairwise.

Let α denote the internal polygon angle and define the normalized overlap ratio as:

$$\rho = \frac{\text{overlap}}{\text{diameter}} = \frac{1}{2}\left(1 - \tan\alpha\right). \tag{4.2}$$

For an octagonal geometry ($\alpha = 22.5°$), solving the symmetry condition yields a critical overlap factor $\rho \approx 0.3$. At this ratio, every pair* of local magnetic interactions admits an opposite counterpart such that:

$$\mathrm{d}\vec{l_i} \cdot \mathrm{d}\vec{l_j} = -\mathrm{d}\vec{l_{i'}} \cdot \mathrm{d}\vec{l_{j'}}, \qquad \|\vec{r_i} - \vec{r_j}\| = \|\vec{r_{i'}} - \vec{r_{j'}}\|, \tag{4.3}$$

leading to a total mutual inductance close to zero:

$$M \approx 0. \tag{4.4}$$

This phenomenon is robust under minor geometric variations and is primarily limited by capacitive coupling between metal layers. However, an empirical adjustment of the overlap ratio can compensate for residual capacitive effects, which depend mainly on the trace width of the windings. Importantly, the cancellation mechanism remains effective even at millimeter-wave frequencies, as long as the structures preserve horizontal symmetry and the metal-stack spacing remains small compared to the loop dimensions.

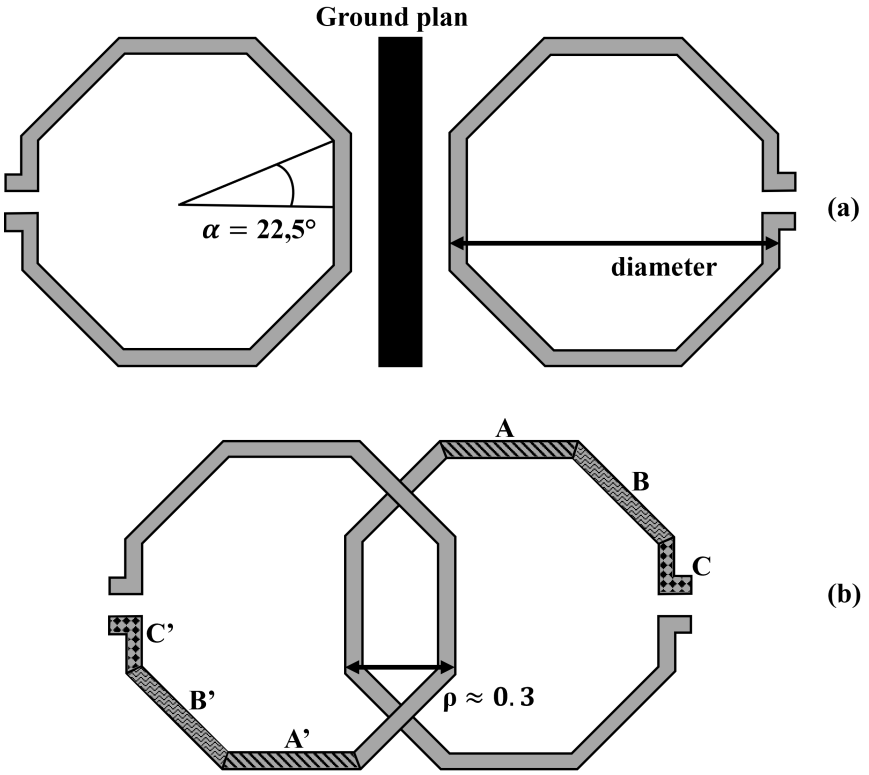


Figure 4.5: Conceptual representation of vertically superposed inductors with $\rho \approx 0.3$ enabling magnetic coupling cancellation.

*In Figure 4.5 the segment A contribution to mutual inductance is canceled by the segment A'.

4.2.2 Design techniques

The cancellation property enables the construction of compact passive structures using multiple metal layers without incurring the usual penalty of increased mutual coupling. Two main categories of components benefit from this approach.

Stacked inductors

Stacking inductive loops across multiple metal layers allows the designer to obtain higher inductance values within a reduced footprint. Under the assumption of strong intra-device coupling ($k \approx 1$), the total inductance can be approximated as:

$$L_{\text{tot}} \approx (2n + 1)L_0, \tag{4.5}$$

where n is the number of vertically stacked turns and L_0 is the inductance of a single loop. Alternating metal layers (e.g. top metal and intermediate RF metals) enables the tuning of self-resonant frequency, parasitic capacitance, and quality factor. When two such inductors are superposed using the symmetry condition described earlier, the magnetic interaction between them becomes negligible, enabling their placement in extremely close proximity without degrading individual performance. (see figures 4.6, 4.7)

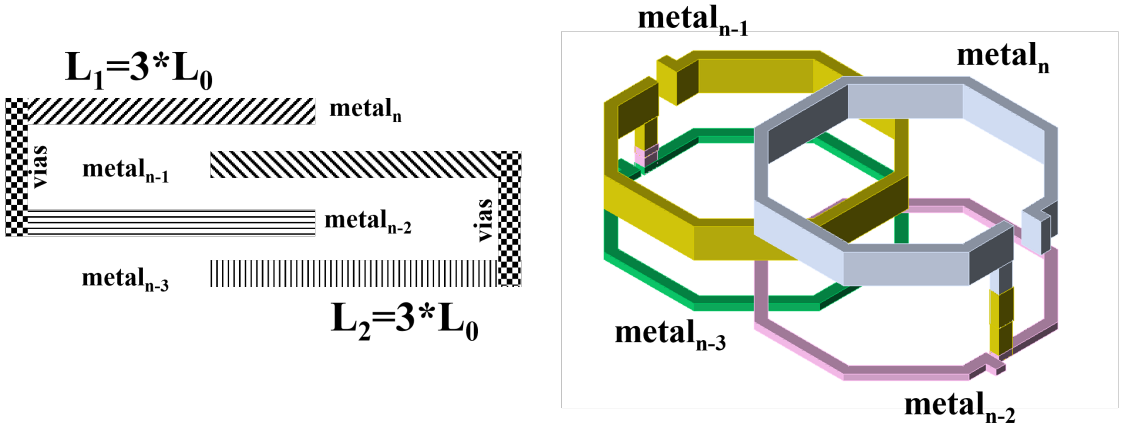


Figure 4.6: Schematic (a) and 3D representation (b) of stacked inductors implemented in multiple metal layers and vertically aligned to cancel mutual inductance.

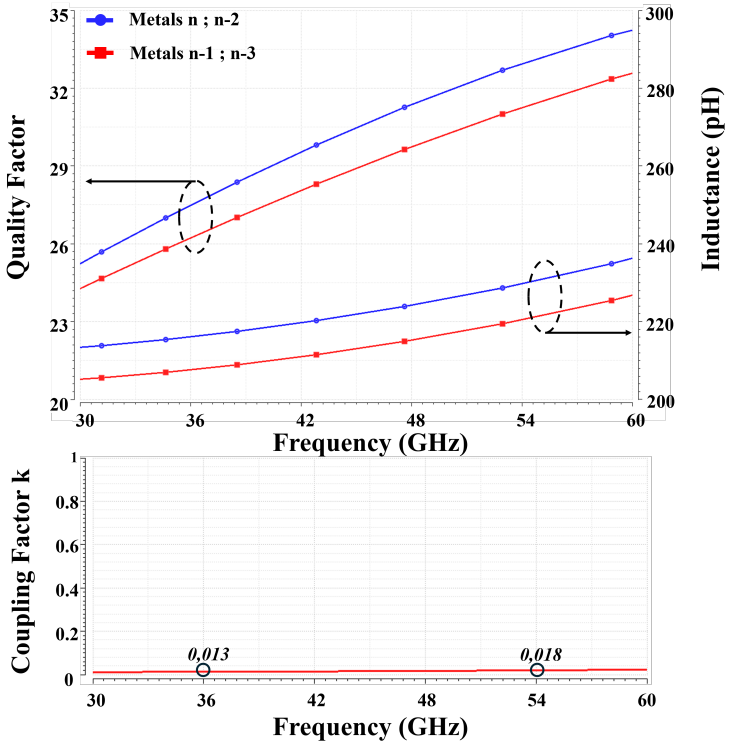


Figure 4.7: Magnetic coupling and inductive performances of passive elements designed in fig. 4.6

Simulated results confirm that both inductors preserve their expected inductance and quality factor values without increasing the coupling factor. Quality factor and inductance values asymmetry may occur due to layer-dependent metal resistivity and dielectric thickness; these effects can be compensated by designing vertically symmetric structures. In this new configuration, it may become challenging to design multi-layer inductors.

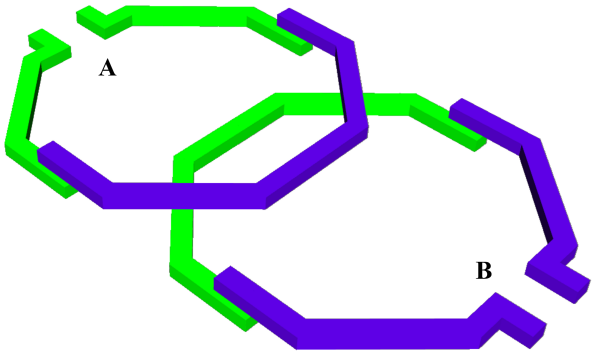


Figure 4.8: Design example of stacked symmetric coils, ensuring equal inductive and quality factor performances.

Figure 4.8 illustrates the proposed stacked symmetric coil configuration, designed to mitigate the asymmetries discussed previously. The results of electromagnetic simulations, presented in the following figure, demonstrate that both inductors exhibit nearly identical inductance values as well as comparable quality factors. This confirms that the vertical symmetry of the layout effectively compensates for layer-dependent variations, ensuring balanced electrical performance without introducing additional coupling effects. It is worth noting that, compared to conventional design practices (eg. fig. 4.10), such configurations can reduce the occupied area by nearly 40%.

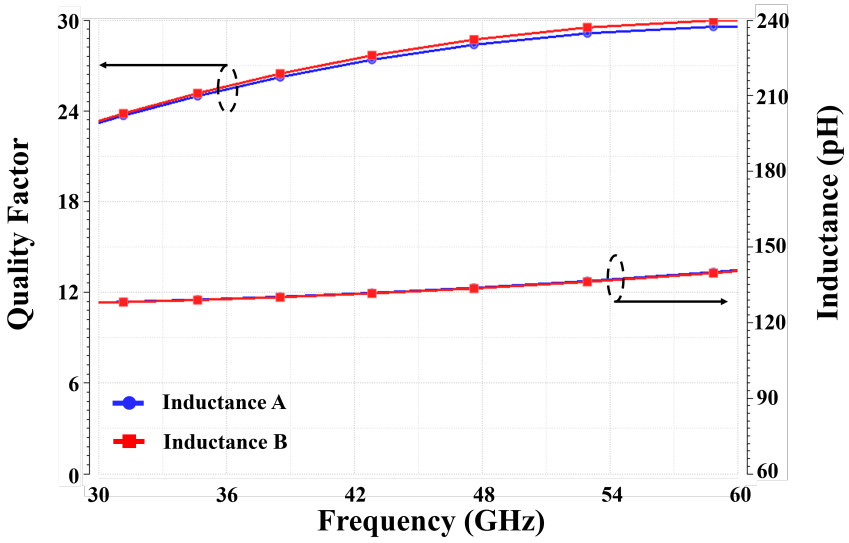


Figure 4.9: Simulated inductance and quality factor of the stacked symmetric coils.

To extend the applicability of the proposed design methodology to mmWave circuits, it is important to consider the typical composition of such systems. At these frequencies, the use of multiple standalone inductors becomes increasingly uncommon [†], while integrated transformers are more frequently employed. Although transformers are primarily designed to achieve strong magnetic coupling, which limits the direct relevance of the proposed technique, certain architectures such as multi-winding transformers [46] introduce additional constraints, including the need for isolation between secondary windings.

Multi-winding transformers

The proposed methodology can be extended to multi-winding transformer structures, which are widely used in interstage matching networks and reconfigurable gain architectures. In

[†]Nevertheless, the trend could shift should this design technique gain broader acceptance.

conventional three-winding implementations, each secondary is assigned a dedicated area to minimize parasitic interactions, leading to a significant footprint. By vertically stacking the two secondary windings while preserving their coupling to the primary, the occupied area can be substantially reduced without degrading the intended magnetic behavior. In this configuration, the mutual coupling between the secondary windings remains negligible, while each of them retains the desired inductive coupling with the primary.

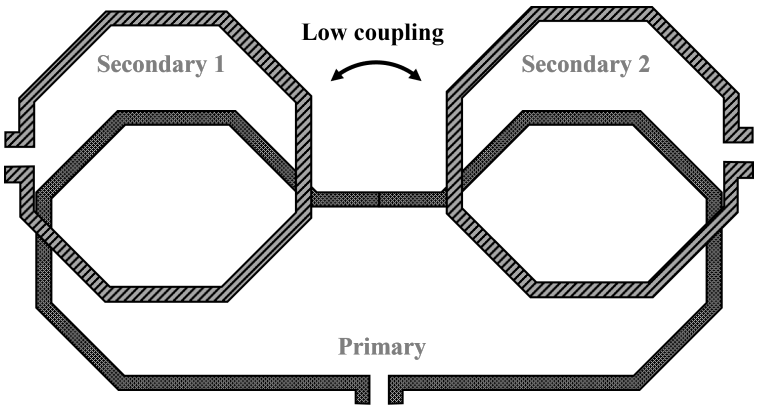


Figure 4.10: Layout of a conventional three-winding transformer with spatially separated secondary windings. [46]

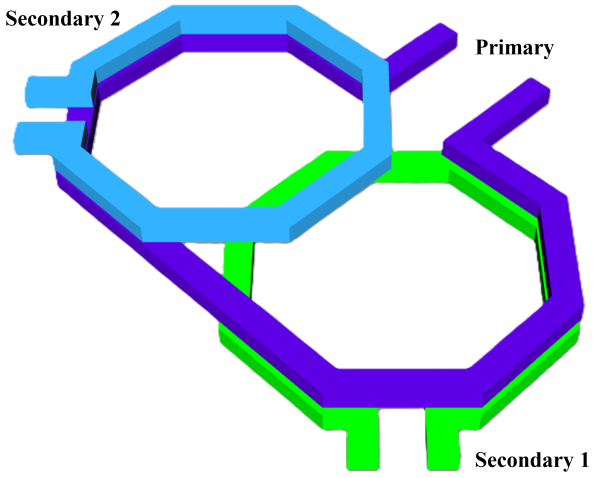


Figure 4.11: 3D view of proposed three-winding transformer with stacked secondary windings.

Electromagnetic simulations (fig.4.12) show that the primary inductance is preserved (e.g. $L_p \approx 80\,\text{pH}$ with $Q_p \approx 20$) while the secondary windings exhibit inductances around $L_s \approx 58\,\text{pH}$ with $Q_s \approx 13$. Importantly, the effective coupling coefficient $k_{p,s}$ remains high,

whereas the coupling between the superposed secondaries is nearly zero. The resulting footprint reduction may exceed 50% compared to a conventional three-winding transformer designed for similar performance.

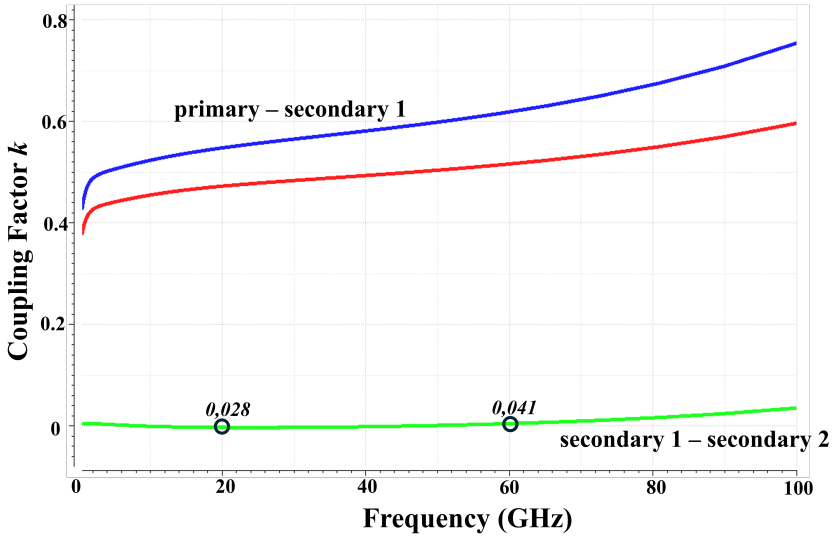


Figure 4.12: Simulated electromagnetic performances of proposed stacked three-winding transformer.

4.2.3 Validation and comparison with state-of-the-art

The proposed stacked-inductor methodology provides a compact solution for mm-wave passive structures without compromising RF performance. Compared to conventional layouts used in 60 GHz LNAs and mixers, the technique enables:

- reduction of inductive-area footprint by 40–55%;
- negligible magnetic coupling between stacked elements ($M \approx 0$);
- preservation of wideband behavior due to low effective mutual coupling;

These results demonstrate the suitability of this approach for reconfigurable RF front-end circuits, particularly when multiple inductors or transformer windings must coexist in a constrained layout, as is the case for the interstage network of the proposed LNA in this chapter. The proposed design methodology can also be extended to another application, which forms the foundation for the development of a novel reconfigurable mmWave LNA architecture presented in next section.

4.3 Design of a Reconfigurable mmW LNA

4.3.1 LNA Design and Specifications

We now turn to the design of a Low Noise Amplifier (LNA) aimed at validating the objectives outlined in Section 3.3.5, as well as the link budget scenarios summarized in Table 3.3. The proposed LNA is designed to meet the requirements of the first two scenarios, namely the single-stage and two-stage gain configurations, in order to efficiently cover the expected range of received input power (see Fig. 3.14).
Based on these system-level considerations, a set of target specifications can be defined, as detailed in the following subsection.

4.3.2 Specifications Derived from System-Level Architecture Study

Table 4.2: Target specifications for the proposed reconfigurable mmW LNA

Mode	**Gain (dB)**	**NF (dB)**	**DC Power (mW)**	$\mathbf{I_{CP1}}$ **(dBm)**
Low Power	13	5	10	-15
High Power	18	7	15	-20

Assuming a supply voltage of 1.2 V, the DC bias currents are set to 7.5 mA for the first stage and up to 5 mA for the second stage.

The design philosophy of the proposed LNA is to achieve competitive performance relative to the state of the art while meeting the link budget constraints, and to maintain efficiency in both power consumption and silicon area. As discussed in Section 4.1, LNA designs at 60 GHz typically employ three or four gain stages to satisfy stringent gain and bandwidth requirements, but at the cost of increased DC power and larger footprint. In contrast, this work aims to meet the required performance with only two gain stages. Furthermore, a single-ended topology is adopted rather than a fully differential one. While differential architectures can offer improved common-mode rejection and linearity, they require roughly twice the number of active devices and additional biasing circuits, which increases both DC power consumption and silicon area. The single-ended approach therefore provides a more compact and power-efficient solution, while still allowing the design of wideband matching networks to achieve the target 7 GHz bandwidth.

4.3.3 Starting from a standard two-stage cascode LNA

In this context, the main contribution of this work does not lie in the amplification cores themselves, but rather in the overall topology and in the design of the surrounding passive components. The amplification stages are based on cascode configurations, which offer several well-established advantages at millimeter-wave frequencies. In particular, cascode structures enable high gain by increasing the effective output resistance, while providing improved isolation between input and output, thereby reducing the impact of parasitic capacitances and enhancing stability. They also help mitigate the contribution of subsequent stages to the overall noise figure. However, these benefits come at the cost of increased voltage headroom requirements and reduced voltage swing, which can limit linearity under low supply voltage conditions. Despite these trade-offs, the cascode topology remains a well-suited choice for high-frequency LNA design, providing a robust foundation upon which the proposed passive network optimizations can be built.

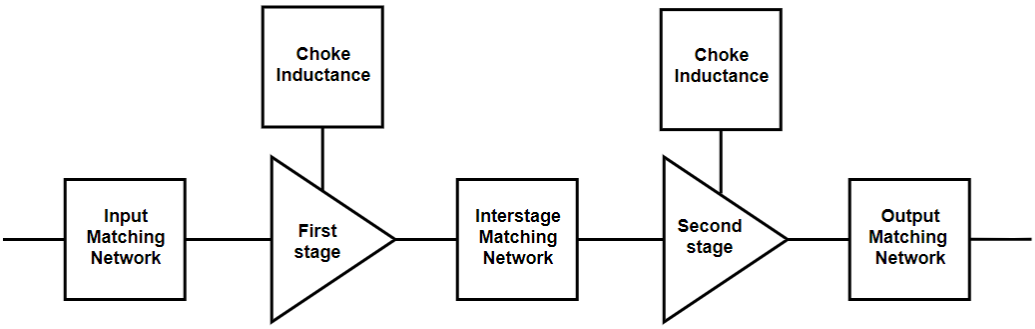


Figure 4.13: First block schematic of the proposed reconfigurable mmW LNA.

The conceptual schematic of the proposed reconfigurable mmW LNA is shown in Fig. 4.13. The circuit is based on a two-stage cascode architecture, in which the first stage is optimized for low noise figure while providing moderate gain, and the second stage is designed to maximize the overall gain of the LNA. This schematic also illustrates all passive elements included in the design. No inductive degeneration is implemented, as such techniques are highly sensitive at millimeter-wave frequencies. In practice, the direct connection to ground at the chip level inherently introduces a small amount of degeneration. Choke inductors are employed to allow the bias current to flow through the cascode transistors while presenting a high impedance at RF frequencies. This ensures that the stages operate correctly without degrading the RF signal path.

In order to achieve wideband operation, the input, interstage, and output matching networks are implemented using coupled-transformer structures with gradually decreasing coupling factors. Reducing the coupling factor progressively allows the effective impedance transformation to be distributed over a wider frequency range, thereby extending the bandwidth of the amplifier. High coupling at the first stage ensures sufficient gain and matching at the lower end of the band, while weaker coupling in subsequent stages mitigates the Q-factor limitations inherent to tightly coupled structures, which would otherwise result in a narrowband response. Additionally, this approach helps to reduce sensitivity to parasitic capacitances and layout variations, which become increasingly critical at millimeter-wave frequencies. By carefully designing the coupling coefficients, it is possible to balance gain, noise figure, and bandwidth, achieving a wideband response without resorting to complex multi-stage resonators or lossy broadband matching networks. This aspect will be discussed in greater detail later in the manuscript.

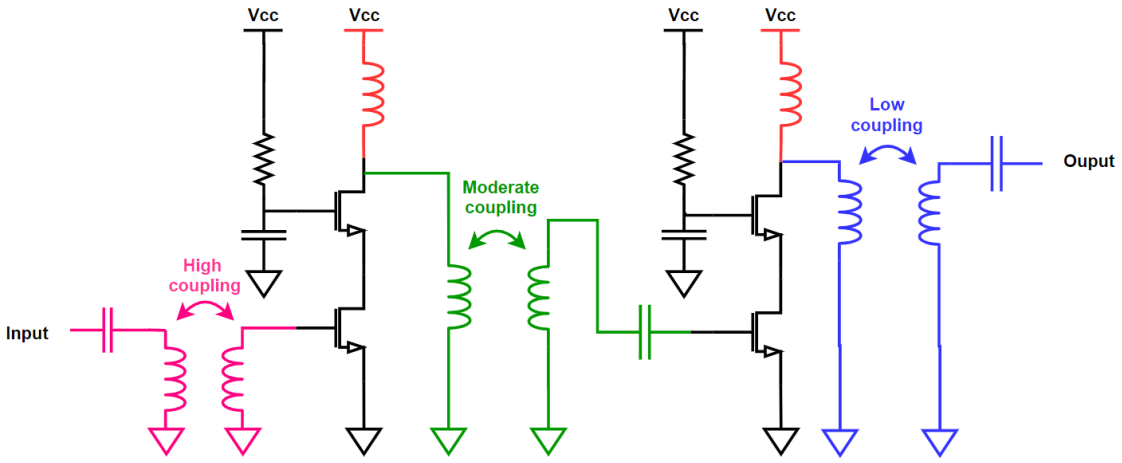


Figure 4.14: First schematic of the LNA, including every passive elements.

At this stage, the LNA can be represented by the schematic shown in Fig. 4.14, featuring input (pink), interstage (green), and output transformers (blue), as well as choke inductors (red) for both amplification stages. The biasing of the cascode transistors is directly achieved through a connection to the supply voltage.
Starting from this standard LNA design, passive functions can be combined to reduce the overall occupied silicon area.

4.3.4 Concatenation of passive functions in order to reduce area

It is worth noting that the initial LNA schematic presented above does not fully comply with the design principles established in this work. In particular, although minimizing silicon area is a key objective, the current implementation relies on multiple inductive elements, including transformers and choke inductors, which are known to dominate the footprint of millimeter-wave integrated circuits. This apparent contradiction highlights the need for a more efficient use of passive components. To address this, several transformations of the circuit can be performed in order to concatenate passive functions, thereby reducing the overall area without compromising the targeted performance.

Starting from the input transformer, no further concatenation with other passive functions is considered, as the associated design constraints are already significant. For the interstage network, however, it is possible to merge the choke inductance with the transformer by reusing it as the primary winding of the interstage transformer. At the output, a similar approach can be adopted by combining the choke inductance with the output matching network. In this case, the resulting structure is implemented as an autotransformer, which offers a compact solution with reduced losses and inherently wideband behavior, while enabling the simultaneous realization of biasing and impedance transformation.

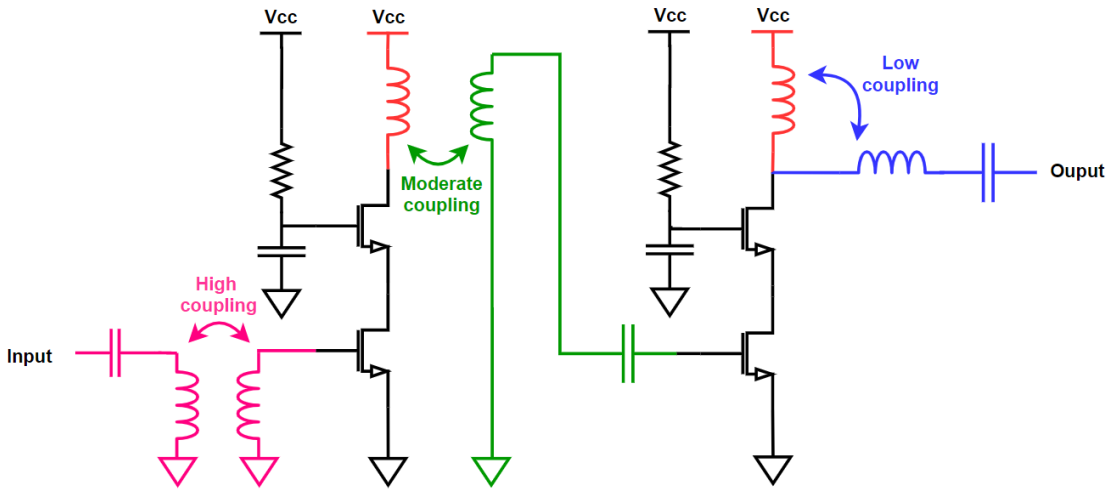


Figure 4.15: Schematic of the LNA after concatenation of inductive functions.

Now that a baseline architecture for the proposed mmW LNA has been established, the integration of the gain reconfiguration mechanism can be addressed. This mechanism enables the LNA to operate either with both gain stages active or in a reduced-gain configuration where the second stage is turned off, resulting in lower gain but improved linearity and reduced power consumption. The process of integrating this passive gain reconfiguration is illustrated in Fig. 4.16.

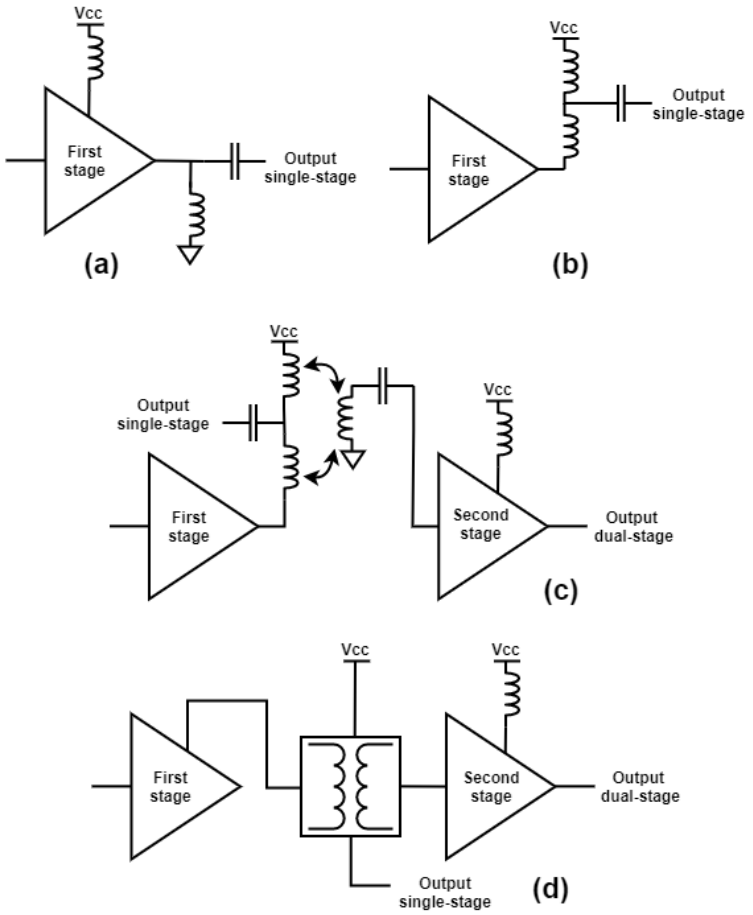


Figure 4.16: Design process of an innovative interstage network combining DC choke, single-stage output matching, and two-stage interstage functionality.

The starting point is a conventional single-stage LNA including an output LC matching network and a choke inductor (Fig.4.16.a). By applying the same passive function concatenation principles introduced earlier, this network can be transformed into an LCL T-network between the cascode stage, the supply voltage, and the output node (Fig.4.16.b). To ensure stable operation, it is essential to avoid magnetic coupling between the inductors in this configuration.

At this stage, a standard single-stage LNA with proper output matching is obtained. In conventional designs, these inductors are typically placed far apart, or even oriented in opposite directions, to minimize coupling. However, by leveraging the superposition techniques described in Section 4.2, it becomes possible to bring these inductors closer together while ensuring negligible magnetic coupling.

This property enables the integration of the single-stage structure with the two-stage LNA by forming a split primary composed of two inductors, each coupled to a common secondary, thereby realizing the interstage transformer (Fig.4.16.c). The resulting structure simultaneously fulfills multiple functions, acting as a choke inductor, the output matching network of the first stage, and the interstage transformer in the two-stage configuration (Fig.4.16.d).

Having established the overall architecture and introduced the key design concepts, including passive function concatenation and gain reconfigurability, the next step is to formalize the design through analytical considerations. In particular, it is necessary to derive the relevant design equations and define the circuit-level parameters that govern the performance of the LNA. This includes the sizing of active devices, the impedance levels across the different stages, and the tuning of the passive networks. These aspects are addressed in detail in the following subsection.

4.3.5 Analytical Design Equations and Circuit-Level Choices

The analytical design procedure begins with the sizing of the cascode transistors, as they primarily determine the achievable gain and noise performance of the LNA. In particular, the choice of device dimensions (channel length L and width W) directly impacts the transconductance g_m, parasitic capacitances, and noise contribution. Therefore, an appropriate trade-off must be established in order to maximize gain while maintaining a low noise figure under the given power consumption constraints.

Device-Level Characterization: Noise Figure and Transition Frequency

The transistor sizing and biasing are derived from device-level characterization of the minimum noise figure $NF_{\min}$ and the transition frequency f_T as a function of current density J_D. For the GF22nm technology at 60 GHz, the measured dependencies are illustrated in Figures 4.17.a and 4.17.b.

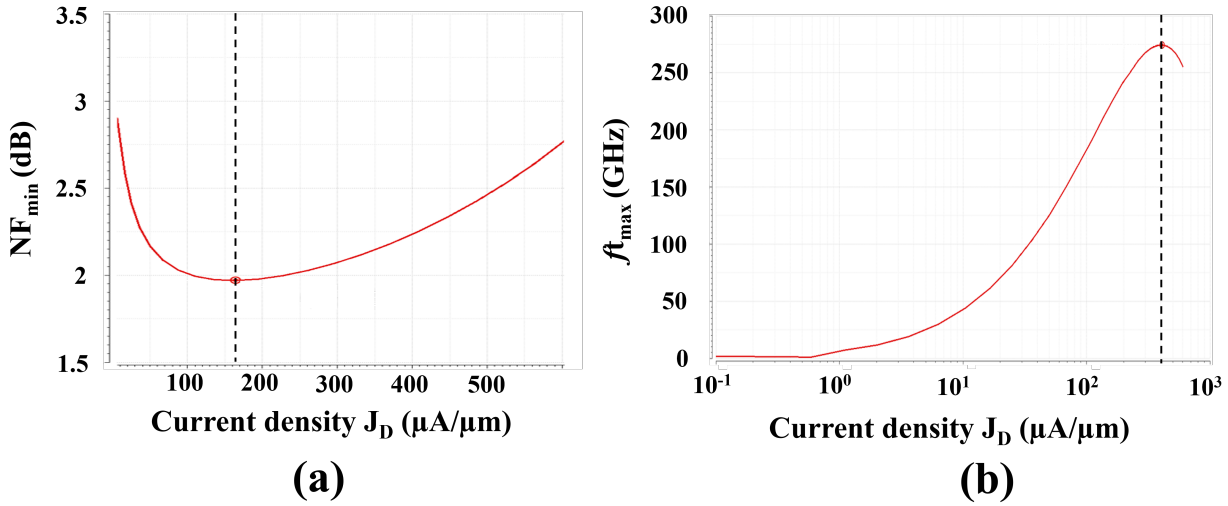


Figure 4.17: (a) $NF_{\min}$ and (b) Transition frequency f_T as a function of current density at 60 GHz.

The characterization reveals distinct optimal operating points for noise and speed. The minimum noise figure $NF_{\min} = 1.97\,\text{dB}$ is achieved at a current density of $J_{NF} = 164\,\mu\text{A}/\mu\text{m}$. Notably, the noise curve exhibits a relatively flat behavior in the vicinity of this minimum, with $NF_{\min} \leq 2\,\text{dB}$ maintained across the range from $110\,\mu\text{A}/\mu\text{m}$ to $230\,\mu\text{A}/\mu\text{m}$. Beyond $300\,\mu\text{A}/\mu\text{m}$, the noise figure degrades rapidly.

In contrast, the transition frequency f_T reaches its maximum value of 274.4 GHz at a significantly higher current density of $J_{f_T} = 409\,\mu\text{A}/\mu\text{m}$. The f_T curve shows a monotonic increase from 150 GHz at $70\,\mu\text{A}/\mu\text{m}$ to 240 GHz at $200\,\mu\text{A}/\mu\text{m}$, and further to 260 GHz at $300\,\mu\text{A}/\mu\text{m}$, before plateauing near the peak. This separation between J_{NF} and J_{f_T} highlights the fundamental trade-off between noise performance and high-frequency operation. Operating at J_{NF} minimizes the intrinsic device noise, whereas J_{f_T} maximizes the transistor speed and gain. However, neither of these operating points is optimal at the circuit level, as LNA performance depends not only on intrinsic device metrics but also on impedance matching, parasitic effects, and power constraints established in Section 4.3.2.

Selection of an Optimal Current Density

Based on the above considerations, an intermediate current density is selected:

$$J_{\text{opt}} \approx 230\,\mu\text{A}/\mu\text{m}, \tag{4.6}$$

which provides a balanced trade-off between noise figure and transition frequency. At this operating point, the noise figure remains within 0.03 dB of the minimum (approximately 2 dB), while the transition frequency reaches approximately 250 GHz, representing about 91% of the maximum achievable f_{Tmax}. This choice is further supported by the observation that NF_{min} exhibits relatively flat behavior in this region, making the design robust to process and bias variations.

Transistor Width Sizing Based on Transconductance Analysis

The total available current (12.5 mA) is distributed asymmetrically between the two stages, with $I_{D1} = 7.5\,\text{mA}$ for the first stage and $I_{D2} = 5\,\text{mA}$ for the second stage. This allocation is dictated by the transconductance requirements in single-stage operation. The voltage gain of a cascode stage can be approximated as:

$$A_v \approx g_m \cdot Z_{\text{out}}, \tag{4.7}$$

where R_{out} is the output resistance of the cascode configuration. The transconductance g_m scales approximately linearly with device width for a fixed current density:

$$g_m \propto W \cdot J_{\text{opt}}. \tag{4.8}$$

Given the target gain of 13 dB in single-stage mode (Table 4.2), the first stage must achieve sufficient g_m to compensate for the limited output resistance of a single amplification stage. This necessitates a larger transistor width (W_1), which in turn requires a proportionally higher bias current ($I_{D1} = W_1 \cdot J_{\text{opt}}$) to maintain the optimal operating point. The first-stage width is calculated as:

$$W_1 \approx \frac{7.5\,\text{mA}}{230\,\mu\text{A}/\mu\text{m}} \approx 32\,\mu\text{m}. \tag{4.9}$$

Both the common-source and cascode transistors in the first stage use this width to ensure consistent high-frequency behavior.

In contrast, the second stage operates in a two-stage configuration where the overall gain is distributed across both amplification stages. The second stage must contribute less in order to reach the total gain target of 18 dB, allowing for a reduced width ($W_{2,\mathrm{CS}}$) and consequently lower current consumption. The second-stage sizing is adjusted to optimize bandwidth and isolation:

- Common-source transistor: $W_{2,\mathrm{CS}} \approx 18\,\mu\mathrm{m}$
- Cascode transistor: $W_{2,\mathrm{CG}} \approx 29\,\mu\mathrm{m}$

The reduced width of the second-stage common-source device lowers parasitic capacitances, improving bandwidth and high-frequency gain. Regarding the cascode transistor sizing, the common-gate device ($W_{2,\mathrm{CG}} \approx 29\,\mu\mathrm{m}$) is sized larger than the common-source transistor ($W_{2,\mathrm{CS}} \approx 18\,\mu\mathrm{m}$). This choice enhances the linearity of the stage by preventing the common-gate transistor from entering the triode region under large-signal conditions, thereby improving the input third-order intercept point (IIP3). The additional width also provides better isolation between the output and the cascode node, contributing to overall stability.

Summary of the Active Device Sizing

The proposed sizing strategy reflects a system-level optimization rather than a device-level optimum. While $NF_{\min}$ and f_T provide useful guidelines, the final design point is determined by a compromise between noise performance, gain, bandwidth, and power consumption. By operating both stages in a similar moderate inversion region while tailoring their current levels and device dimensions, the LNA achieves a consistent trade-off across both reconfiguration modes. This ensures that the first stage remains noise-efficient while still delivering sufficient gain when operating alone, while the second stage provides additional gain in two-stage mode with proportionally lower power consumption.

With the transistor dimensions and biasing conditions established, the design proceeds to the matching networks, which are critical for achieving the target bandwidth and input/output impedance matching at 60 GHz.

Design of the Input Matching Network

The design of the input matching network is a critical step, as it directly determines both the power transfer from the 50 Ω source and the effective impedance presented to the first amplification stage. The adopted topology is shown in Fig. 4.18, where both the physical transformer and its loss-aware equivalent model are illustrated.

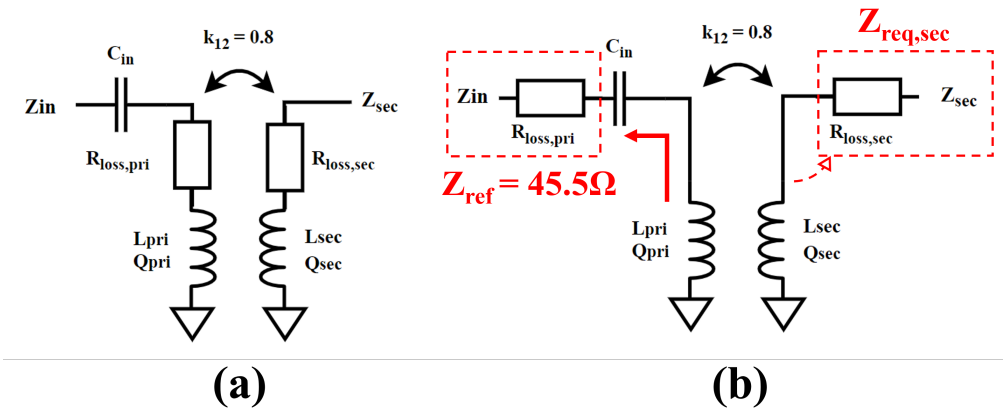


Figure 4.18: Transformer-based input matching network. (a) Physical implementation with finite coupling factor. (b) Equivalent circuit including primary and secondary loss resistances and reflected impedance.

At 60 GHz, the finite quality factor (Q) of on-chip passive components significantly impacts the matching performance. As shown in Fig. 4.18, each winding is modeled as an inductance in series with a loss resistance. Electromagnetic simulations yield $Q_{\text{pri}} \approx 20$ for the primary winding and $Q_{\text{sec}} \approx 15$ for the secondary.

The series resistance of each winding is estimated as:

$$R_{\text{loss}} = \frac{\omega L}{Q}. \tag{4.10}$$

The input impedance of the cascode stage, extracted from device simulations, is $Z_{\text{in}} \approx 120 - j75\,\Omega$. Since the secondary winding resistance appears in series with the transistor input (Fig. 4.18), the impedance that must be presented at the secondary port is:

$$Z_{\text{req,sec}} = Z_{\text{in}} + R_{\text{loss,sec}}. \tag{4.11}$$

Assuming an initial secondary inductance $L_{\text{sec}} \approx 300\,\text{pH}$, the corresponding loss resistance is:

$$R_{\text{loss,sec}} = \frac{2\pi \cdot 60 \cdot 10^9 \cdot 300 \cdot 10^{-12}}{15} \approx 7.5\,\Omega, \tag{4.12}$$

leading to:

$$Z_{\text{req,sec}} \approx 127.5 - j75\,\Omega. \tag{4.13}$$

On the primary side, the source impedance is $R_S = 50\,\Omega$. As illustrated in Fig. 4.18, the total impedance seen by the source is the sum of the primary loss resistance and the impedance reflected from the secondary:

$$Z_{\text{total}} = R_{\text{loss,pri}} + Z_{\text{ref}}. \tag{4.14}$$

Imposing $Z_{\text{total}} = R_S$ leads to:

$$Z_{\text{ref}} = R_S - R_{\text{loss,pri}}. \tag{4.15}$$

With $L_{\text{pri}} \approx 240\,\text{pH}$, the primary loss resistance is:

$$R_{\text{loss,pri}} = \frac{2\pi \cdot 60 \cdot 10^9 \cdot 240 \cdot 10^{-12}}{20} \approx 4.5\,\Omega, \tag{4.16}$$

resulting in:

$$Z_{\text{ref}} \approx 45.5\,\Omega. \tag{4.17}$$

The transformer relates the secondary impedance to the reflected primary impedance through the mutual inductance $M = k\sqrt{L_{\text{pri}} L_{\text{sec}}}$, with $k \approx 0.8$. Using the standard transformer approximation:

$$Z_{\text{ref}} \approx \frac{\omega^2 M^2}{Z_{\text{req,sec}}}, \tag{4.18}$$

the value of M is selected such that the real part of the reflected impedance matches the required resistance, while the imaginary part is compensated separately. This leads to the first-order design condition:

$$M \approx \sqrt{\frac{Z_{\text{ref}} \cdot \text{Re}(Z_{\text{req,sec}})}{\omega^2}} \approx 205\,\text{pH}. \tag{4.19}$$

Using this value, the corresponding secondary inductance is:

$$L_{\text{sec}} = \frac{M^2}{k^2 L_{\text{pri}}} \approx 275\,\text{pH}. \tag{4.20}$$

Finally, a series capacitance C_{in} is introduced to compensate the reactive part of the impedance seen at the primary. As shown in Fig. 4.18, this capacitance resonates with the total inductive reactance, including both the primary inductance and the reflected secondary reactance. The resulting value is:

$$C_{\text{in}} \approx 235\,\text{fF}. \tag{4.21}$$

A first-order estimation of the input matching bandwidth can be derived from the loaded quality factor of the network. Approximating the circuit as a series resonant network seen from the $50\,\Omega$ source, the dominant reactive contribution is given by the primary inductance:

$$X_{\text{pri}} = \omega_0 L_{\text{pri}} = 2\pi \cdot 60\,\text{GHz} \cdot 240\,\text{pH} \approx 90\,\Omega. \tag{4.22}$$

The corresponding loaded quality factor is then:

$$Q \approx \frac{X_{\text{pri}}}{R_S} \approx \frac{90}{50} \approx 1.8. \tag{4.23}$$

Around resonance, the reflection coefficient can be approximated as a linear function of frequency:

$$|\Gamma| \approx Q \cdot \frac{\Delta f}{f_0}. \tag{4.24}$$

Imposing the matching condition $|S_{11}| < -10\,\text{dB}$, i.e., $|\Gamma| < 0.316$, yields:

$$\frac{\Delta f}{f_0} \approx \frac{0.316}{Q} \approx 0.175. \tag{4.25}$$

At $f_0 = 60\,\text{GHz}$, this corresponds to an input matching bandwidth of approximately:

$$\Delta f \approx 0.175 \cdot 60\,\text{GHz} \approx 10.5\,\text{GHz}. \tag{4.26}$$

This result provides an order-of-magnitude estimation of the achievable bandwidth. A more accurate evaluation, accounting for transformer coupling, secondary loading, and parasitic capacitances, is obtained from full S-parameter simulations.

Design of choke inductance of first amplification stage

The total choke inductance equal to $L_{\text{choke}} = 300$ pH is implemented by splitting it into two equal inductors of 150 pH each, separated by a shunt capacitance as shown in Fig.4.19. This configuration is not arbitrary but results from a trade-off between RF isolation, impedance behaviour at the output node, and DC biasing requirements of the cascode stage.

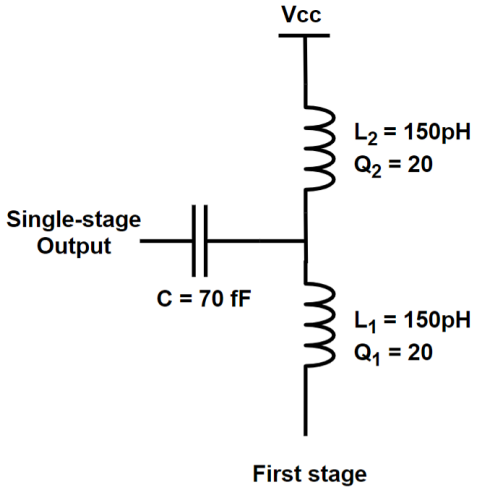


Figure 4.19: Schematic of the circuit operating as the output matching network and choke inductance of the first amplification stage.

At the operating frequency of 60 GHz, the corresponding inductive reactance is given by:

$$X_L = \omega L \approx 2\pi \cdot 60\,\text{GHz} \cdot 300\,\text{pH} \approx 113\,\Omega, \tag{4.27}$$

which provides a sufficiently high impedance compared to the 50 Ω system level, ensuring effective RF decoupling of the bias network while maintaining a compact on-chip implementation.

Ideally, the choke behaves as an open circuit at DC and therefore does not influence the bias current of the transistor. In practice, the finite quality factor introduces a series resistance given by:

$$R_{\text{loss}} = \frac{\omega L}{Q} \approx \frac{113}{20} \approx 5.6\,\Omega, \tag{4.28}$$

which results in a small DC voltage drop of approximately:

$$\Delta V \approx I_D R_{\text{loss}} \approx 7.5\,\text{mA} \cdot 5.6\,\Omega \approx 42\,\text{mV}. \tag{4.29}$$

This confirms that the chosen inductance does not significantly disturb the bias point while keeping losses under control.

It is important to note that splitting the choke into two inductors introduces the potential for unwanted magnetic coupling between them. Such coupling could modify the effective impedance seen by the first stage, degrade the output matching, and disturb the DC bias current. In this design, the two inductance are arranged using the coupling cancellation technique presented in Section 4.2. This arrangement results in a compact implementation that aligns with the design principles established earlier, efficiently combining multiple functions within a minimal footprint.

The complete schematic of the first-stage amplifier is shown in Fig. 4.20.

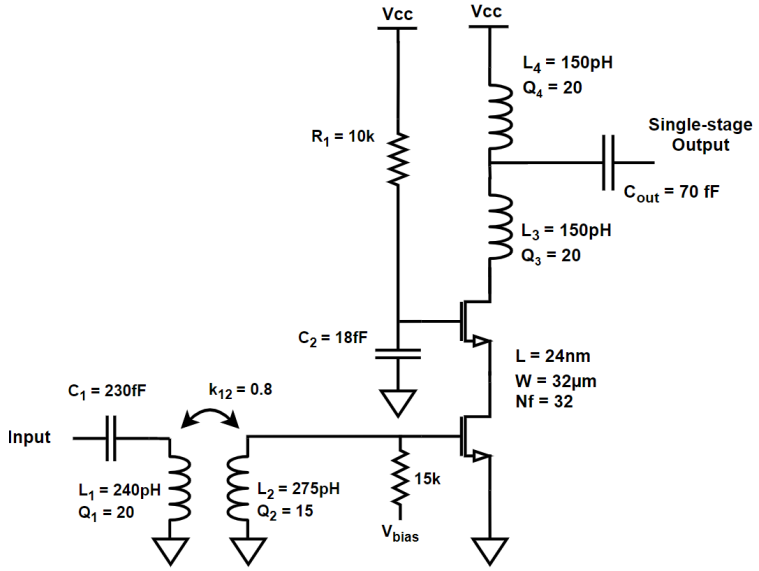


Figure 4.20: Full schematic of the first amplification stage operating as a standalone.

Design of interstage matching network

At this stage, the first amplification stage is fully defined. The next step consists in designing the interstage network, which ensures signal transfer and impedance matching between the two stages while enabling passive function integration.

The interstage matching network is implemented using a transformer-based topology combined with a series capacitance connected to the gate of the common-source transistor of the second stage (see Fig. 4.21). This approach enables simultaneous impedance transformation and compensation of the capacitive input impedance of the following stage.

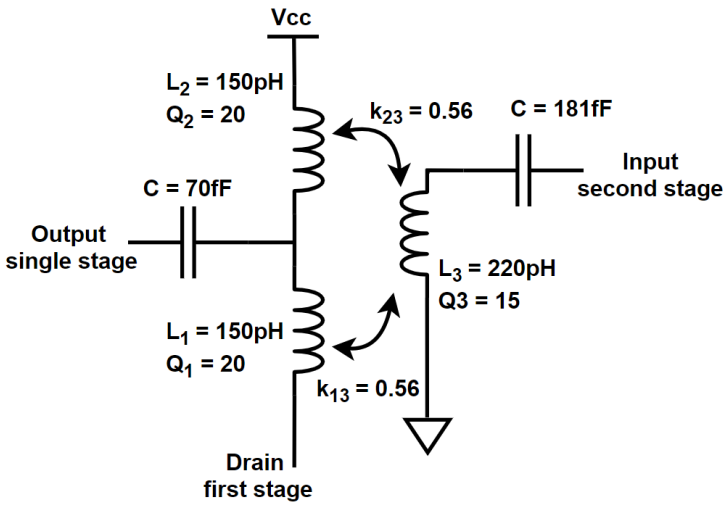


Figure 4.21: Schematic of the interstage network

As discussed previously, the transformer is designed following the passive function concatenation principles introduced in Section 4.2. In this configuration, the secondary winding is magnetically coupled to two primary inductors, which correspond to the matching network and the choke of the first stage. This arrangement allows the interstage network to simultaneously perform impedance transformation and DC biasing, thereby reducing the overall circuit footprint.

In order to favor wideband operation, the coupling factor of the interstage transformer is intentionally chosen to be lower than that of the input transformer. This follows the design strategy introduced earlier, where progressively reducing the coupling factor across stages helps to broaden the bandwidth by lowering the selectivity of each resonant network.

From an impedance standpoint, the interstage network must transform the output impedance of the first stage, observed at the drain node, to the input impedance of the second stage, which is estimated by simulations to be on the order of $200 - j80\ \Omega$. While first-order analytical expressions can be derived based on the reflected impedance through the transformer, the accuracy of this approach is limited by parasitic effects, finite quality factors, and coupling interactions. As a result, certain design parameters, such as the coupling factor and the series capacitance, are refined through empirical adjustments based on circuit-level simulations. The analytical framework therefore serves primarily as a guideline for initial sizing, while the final tuning ensures that the targeted performance is achieved.

Complete analytical equations and additional insights regarding this specific design are provided in Appendix A. Additionally, a more in-depth investigation of this block, particularly regarding coupling control and passive integration, will be carried out at the layout level, as discussed in the next subsection.

Second Amplification Stage and Output Matching Network

The transistors of the second amplification stage are dimensioned with smaller widths compared to the first stage, targeting a reduced DC current of approximately 5 mA while still providing substantial gain. Given that the noise contribution of this stage is largely masked by the preceding stage, strict noise figure constraints are relaxed. This allows for a more compact transistor sizing and lower power consumption, without compromising the overall amplification performance. The stage is implemented identically, with biasing applied to the cascode transistor via a direct connection to V_{CC}.

Following the transistor design, the output matching network is implemented using an auto-transformer topology that simultaneously provides DC biasing through the choke and impedance transformation to the 50 Ω load via a series LC network. This integration of multiple passive functions within a single compact structure follows the same passive concatenation principles applied in previous stages. The network ensures proper wideband operation while maintaining predictable RF behavior and stage biasing.

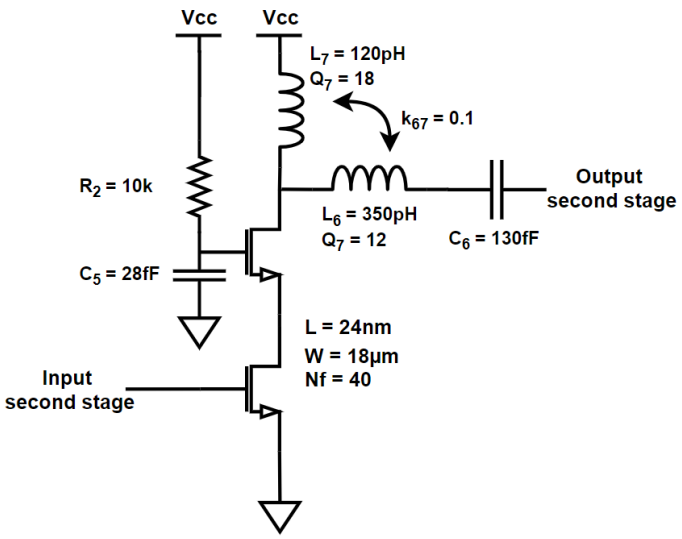


Figure 4.22: Complete schematic of the second amplification stage of the mmW reconfigurable LNA

The series capacitance and transformer inductances were chosen to balance wideband matching, DC biasing, and layout constraints, with initial sizing based on analytical estimates and final tuning performed empirically via circuit-level simulations. The complete second-stage schematic is shown in Fig. 4.22, and the full two-stage LNA, including input, interstage, and output networks, is presented in Fig. 4.23. With the design finalized, we now turn to the simulated performance results.

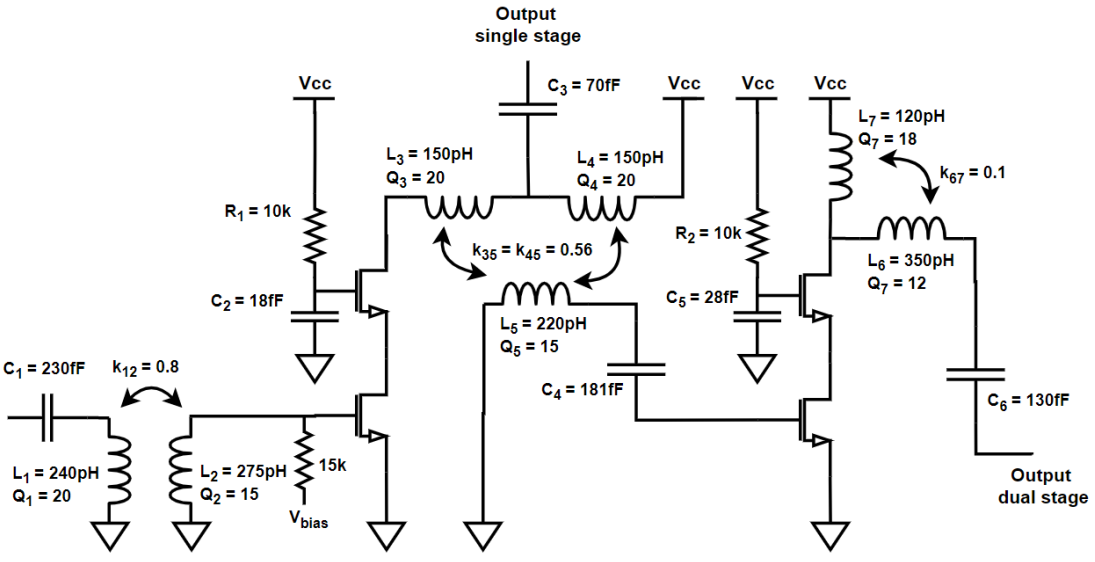


Figure 4.23: Complete schematic of the mmW reconfigurable LNA

Schematic simulated performances

Cadence Spectre is used to simulate the performances of the proposed reconfigurable LNA using layout-extracted models at the schematic level. The analysis focuses on the two operating modes enabled by the design: the full two-stage configuration, providing maximum gain, and the single-stage mode, in which the second stage is deactivated to reduce power consumption and enhance linearity. It is worth noting that, at this stage of the design, most components (transistors, capacitors, and resistors) are already implemented using layout-extracted views, thereby improving the accuracy of the presented simulation results.

At this stage, the presented results primarily serve as design guidelines, providing insight into the expected behavior of the circuit and validating the design methodology. A detailed optimization of the schematic-level performance is not pursued, as significant shifts in frequency response and overall performance are anticipated after layout extraction due to parasitic effects. Therefore, the final assessment of the LNA will rely on post-layout simulations, which are of primary interest for evaluating the circuit performance.

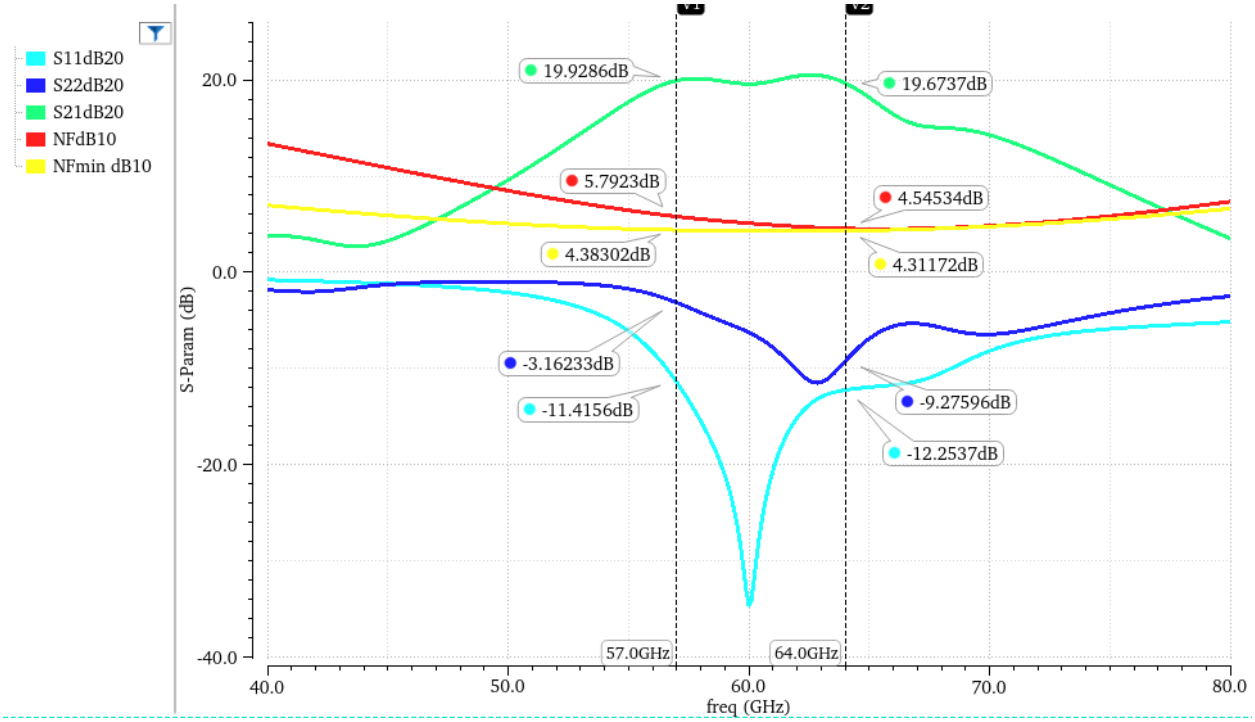


Figure 4.24: Schematic level S-parameters and NF simulations of the complete mmW LNA.

The simulated performance (Fig. 4.24) of the proposed two-stage LNA demonstrates compliance with, and in several aspects exceeds, the targeted specifications. In particular, the forward gain S_{21} remains above the desired target across the entire band of interest, exhibiting a limited in-band ripple of less than 1 dB, thereby ensuring a stable gain response over the operating frequency range. The input matching, characterized by S_{11}, is satisfactory as it remains below -10 dB over the entire band and is well centered around 60 GHz, ensuring efficient power transfer.

From a noise performance perspective, the noise figure stays below the specified target throughout the band and approaches the minimum noise figure NF_{min} at the end of the frequency range, indicating near-optimal noise matching in this region. On the other hand, the output matching (S_{22}) is only marginally compliant with typical design requirements; while acceptable, it remains relatively limited compared to the input matching performance and could be further improved in future design iterations. Overall, these results validate the proposed design as a competitive solution for V-band applications, achieving a favorable trade-off between gain, matching, and noise performance.

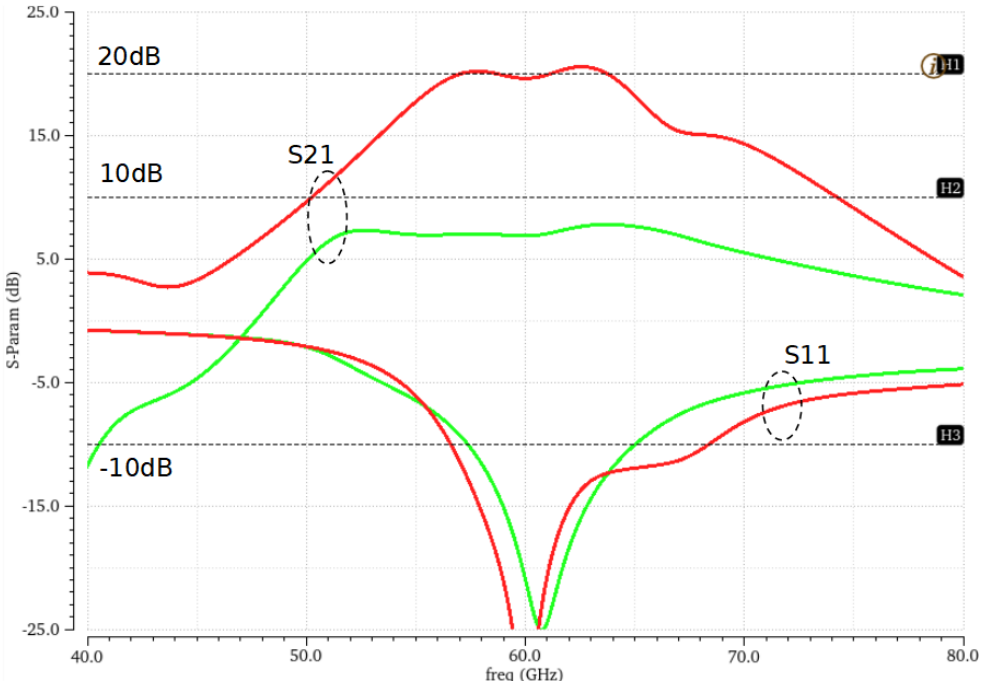


Figure 4.25: Performance comparison of S11 and S21 parameters between single stage mode (green curves) and dual stage mode (red curves) at schematic level.

By disabling the supply voltage and DC biasing of the second stage, the first stage can operate as a standalone amplifier. As shown in Fig. 4.25, the input matching remains satisfactory within the targeted frequency band, while the forward gain S_{21} is reduced to approximately 7.5 dB. Although this gain is lower than initially expected, it remains sufficient to demonstrate the functionality and effectiveness of the proposed reconfigurable LNA.

Table 4.3: Comparison of Single and Dual LNA configurations performances compared to specifications.

Parameter	**Single spec**	**Single sim**	**Dual spec**	**Dual sim**
$\boldsymbol{S_{21,\min}}$ **(dB)**	13	7.5	18	20.2
$\boldsymbol{NF_{\max}}$ **(dB)**	5	4.9	7	5.1
3 dB BW (GHz)	7	23.1	7	11
ICP1 (dBm)	-15	-10.7	-20	-23
DC power (mW)	10	8.4	15	14.4
In-band Ripple (dB)	/	0.3	/	0.7

In the single-stage configuration, the achieved gain S_{21} is lower than the targeted specification, reaching 7.5 dB instead of the expected 13 dB. Nevertheless, the noise figure remains satisfactory, as the link budget analysis indicated sufficient margin on the output signal-to-noise ratio. In addition, the bandwidth requirement is largely met, and both the DC power consumption and linearity performance comply with the design specifications, validating the relevance of this low-power operating mode.

In the dual-stage configuration, the circuit outperforms the initial specifications in most aspects, including gain, noise figure, bandwidth, and power consumption. The only noticeable deviation concerns the input linearity, which is slightly degraded compared to the target. However, this is mitigated by the higher-than-expected gain, which ensures that the output compression point remains compliant with the specifications. Overall, the dual-stage mode fully validates the targeted high-gain operation of the proposed LNA.

With a satisfactory schematic-level validation, the focus now shifts to the layout implementation, which constitutes the core innovation of this work. The following section details the associated design methodology.

4.4 Layout implementation

The previous sections introduced a novel design for a reconfigurable amplifier based on an innovative passive interstage network. While such a topology can be readily conceived and validated at the schematic level, its practical implementation on silicon remains highly challenging. Indeed, conventional design approaches do not readily support the realization of such tightly integrated and coupled passive structures at millimeter-wave frequencies. In this context, the layout implementation becomes a key aspect of the proposed work. The following section therefore focuses on the physical realization of the circuit, detailing the design choices and trade-offs required to translate the conceptual architecture into a functional silicon implementation.

4.4.1 Detailed conception of the innovative interstage network

The schematic of the interstage network shown in Fig. 4.21 can be revisited by identifying the key elements that will drive the physical design. The complete design process is represented in figure 4.26 First, inductors 1 and 2 are identical (1), making a symmetrical implementation a natural choice. The magnetic coupling between these two inductors is designed to be negligible (2), which allows the use of the one-third overlap design technique introduced in Section 4.2. A midpoint must be created to connect a capacitor, enabling the matching network required for the single-stage operating mode (3). Finally, a symmetrical layout also facilitates the design of the transformer secondary, which requires identical coupling with each of the inductors (4).

Several comments can be made regarding this design. The overlap ratio of the two primary windings does not exactly match the theoretical value (0.293) but has been adjusted to compensate for the windings' shape, which is not perfectly octagonal, and to accommodate the center tap used for connection. The shapes of the two primary inductors were chosen to allow fine tuning of the optimal overlap area between the windings, aiming for near-complete cancellation of magnetic coupling. In the proposed design, the transformer secondary exhibits magnetic coupling that is not identical between the two primary inductors. This is primarily due to constraints in layout area and magnetic resonance. Priority was given to achieving the correct inductance without resonance, even if it meant slightly unbalancing the magnetic coupling. In practice, this has a minimal effect, as the total magnetic coupling of the transformer remains close to the desired value (k = 0.56).

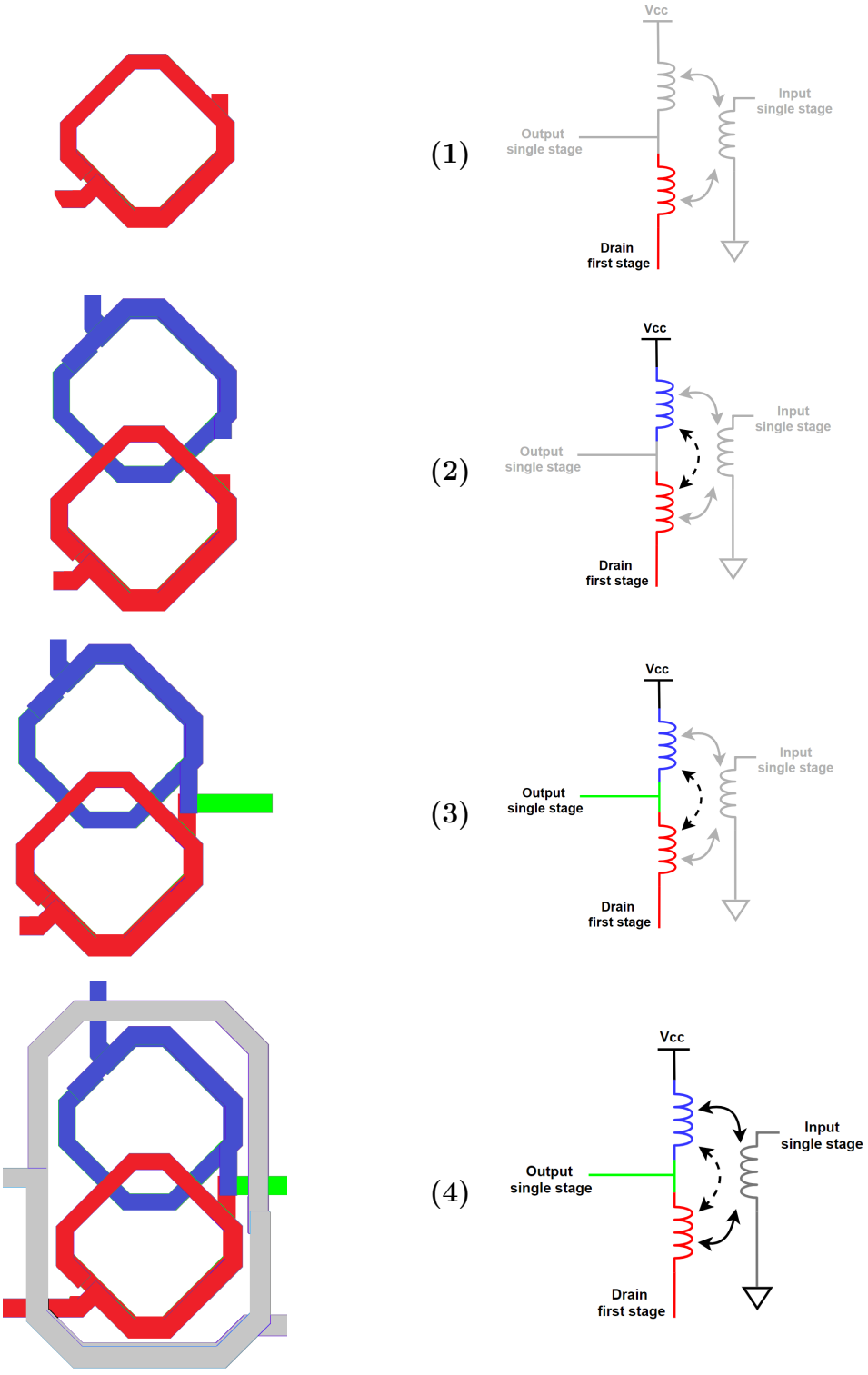


Figure 4.26: Design process for the innovative interstage function.

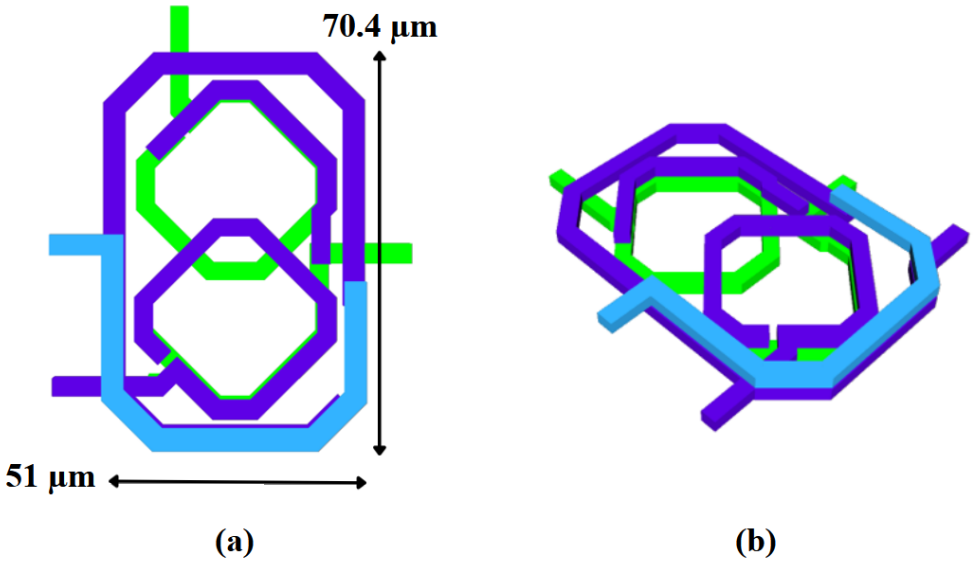


Figure 4.27: Dimensions and 3D representation of the interstage network layout.

In Figure 4.27, additional information about this transformer is provided, including a perspective view to better visualize the overlaps of the metal layers and the dimensions of the circuit. For dimensions of 51 μm by 77.4 μm, the total area of this circuit is approximately 3950 μm^2. To validate this layout, electromagnetic simulations are performed using Cadence EMX. The simulation results for the inductances, quality factor, and coupling factor are shown in the figure below.

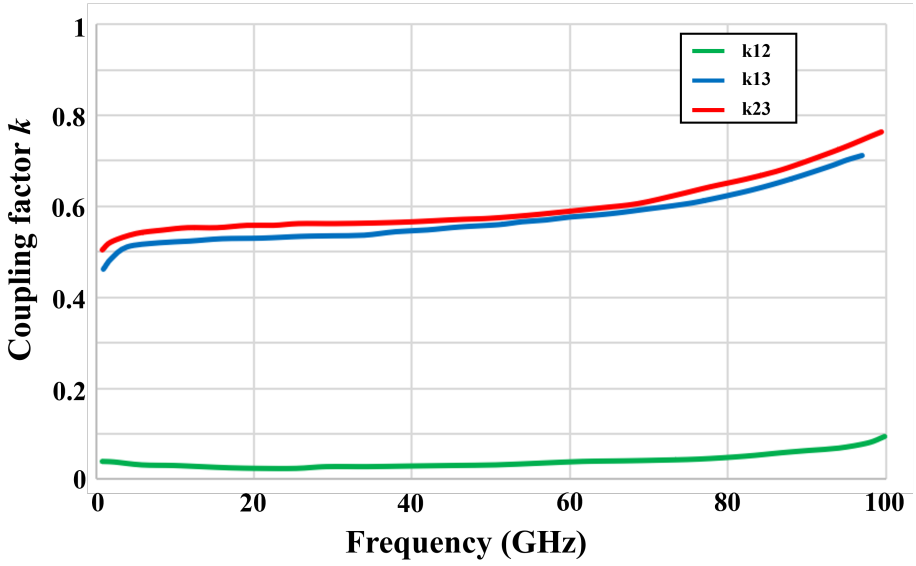


Figure 4.28: Simulated performances of interstage network

4.4.2 Complete LNA layout

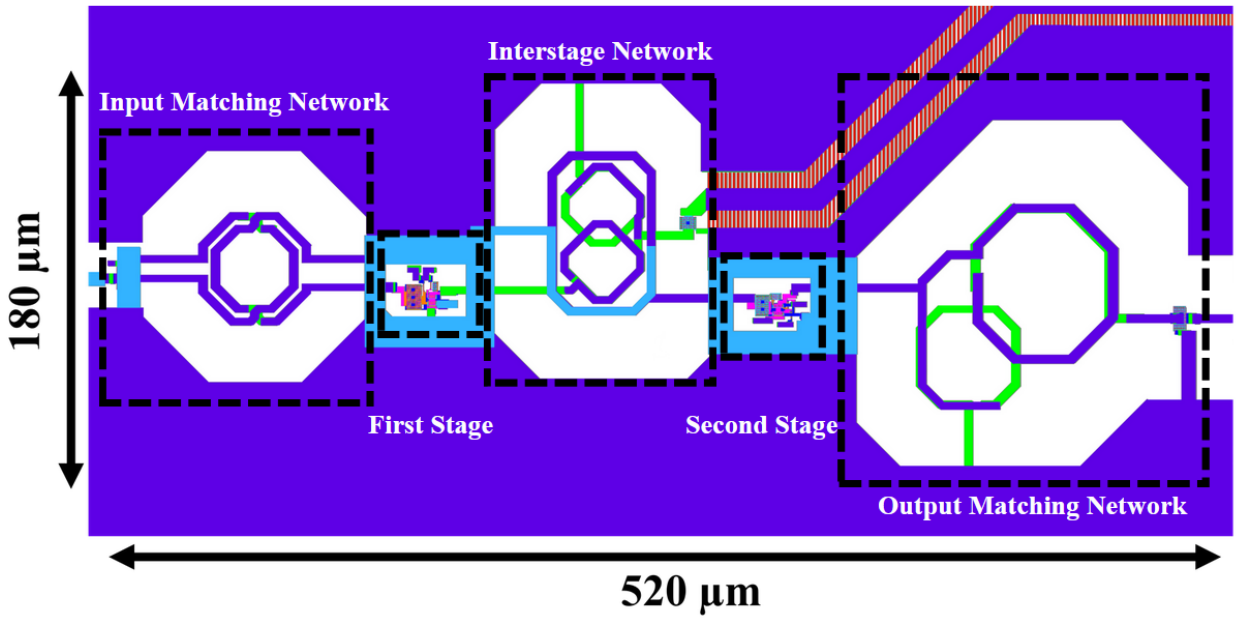


Figure 4.29: Complete layout of the reconfigurable mmW LNA.

In order to validate the physical implementation of the proposed reconfigurable 60GHz LNA, the complete layout was designed in GF22-FDSOI technology. Particular attention was paid to minimizing parasitic effects associated with interconnects, which become critical at millimeter-wave frequencies. The layout includes ground shielding and appropriate metal stack usage to improve isolation and maintain signal integrity.

The overall layout of the LNA is shown in Fig. 4.29. It includes the input matching network, the core amplification stages, the interstage network detailed in the previous section and the large output network. The total occupied area is approximately 0.094 mm^2 which places it at the state of the art.

Some discrepancies can be observed between the schematic-level component values and the final layout implementation. In particular, the input transformer is realized as a standard 1:1 symmetric structure. This modification results from accounting for additional parasitic inductances introduced by the ground plane as well as by the interconnects to the input capacitance and the first amplification stage. Given the critical role of the coupling factor in this design, a careful trade-off was performed between the inductance values and the physical geometry of the transformer. This optimization ultimately leads to a well-matched and robust input network.

A 50-Ω transmission line is implemented between the output of the interstage network and the output pad to ensure proper impedance matching while limiting additional parasitic inductance. Regarding the output matching network, although it was not initially expected to be one of the dominant layout elements, its current geometry enables precise control of the coupling factor between the coupled inductors. This approach provides enhanced tuning capability without introducing excessive parasitic effects. It is clear that reducing the size of this network constitutes one of the main directions for improving the circuit.

Following layout completion, post-layout simulations (PLS), including extracted parasitics, were carried out to evaluate the circuit performance under realistic conditions. These simulations provide a more accurate assessment of gain, noise figure, and matching compared to schematic-level results.

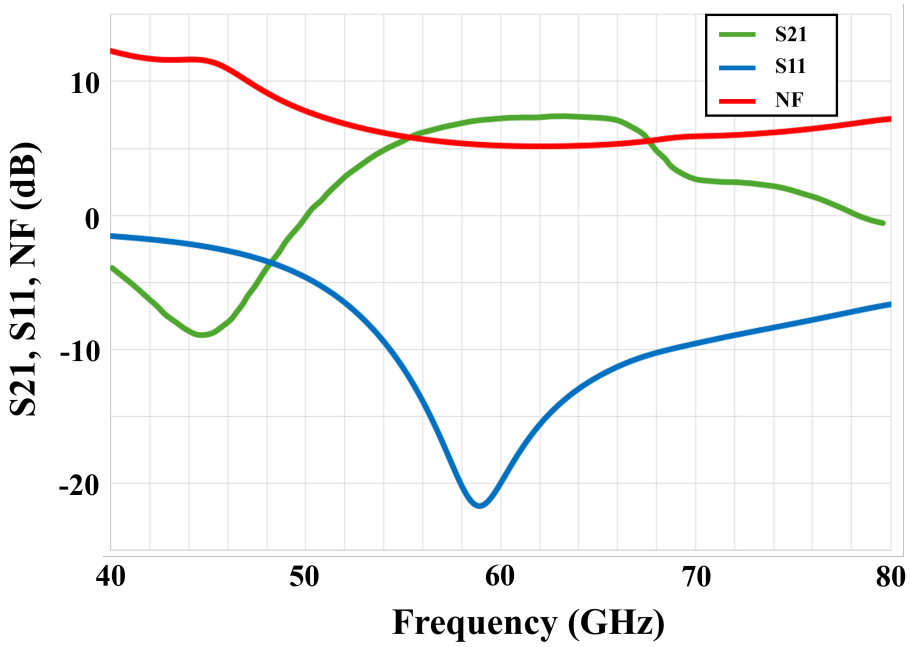


Figure 4.30: Post-layout simulations of the reconfigurable LNA through the single-stage output.

In low-power mode, with only the first amplification stage active, the LNA achieves a gain (S_{21}) of 7.25 dB and a noise figure (NF) of 5.21 dB at 60 GHz, while maintaining good input matching over the entire bandwidth (see Fig.4.30). Under a 1.2 V supply, it draws 7.637 mA, corresponding to a power consumption of 9.16 mW. The linearity is characterized by an ICP1 of −8.36 dBm. Overall, the post-layout results closely match the schematic-level simulations, confirming effective control of parasitic effects during layout design.

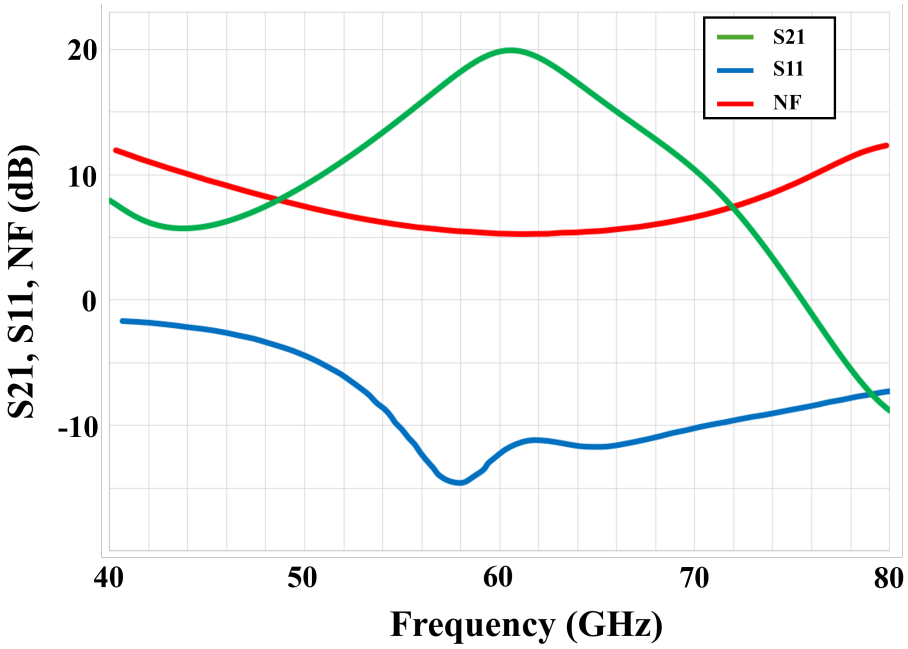


Figure 4.31: Post-layout simulations of the reconfigurable LNA through the dual-stage output.

When both amplification stages are enabled (high-power mode), the LNA provides a gain (S_{21}) of 19.9 dB at 60 GHz, with a noise figure of 5.3 dB (see Fig.4.31). The input matching remains adequate across the targeted bandwidth. Post-layout results indicate a more pronounced narrowband behavior compared to schematic simulations, with reduced in-band flatness concerning power gain. The small difference in noise figure between low and high-power modes highlights the effective isolation of subsequent stages from the input, confirming that the overall noise performance is dominated by the first stage. Operating from a 1.2 V supply, the circuit consumes 12.11 mA, corresponding to 14.53 mW. The measured linearity yields an $\mathrm{ICP}_{1\mathrm{dB}}$ of -22.3 dBm.

The proposed gain reconfiguration technique, applicable to RF and millimeter-wave amplifiers and based on innovative passive design strategies, has been validated through post-layout simulations of a fabrication-ready layout, intended for on-wafer measurements using a probe station (full layout view, including pads, is available in Appendix B). It enables the selection between single-stage and two-stage amplification, thereby allowing gain tuning while reducing DC power consumption without significantly degrading other key performance metrics such as noise figure, input matching, and linearity.

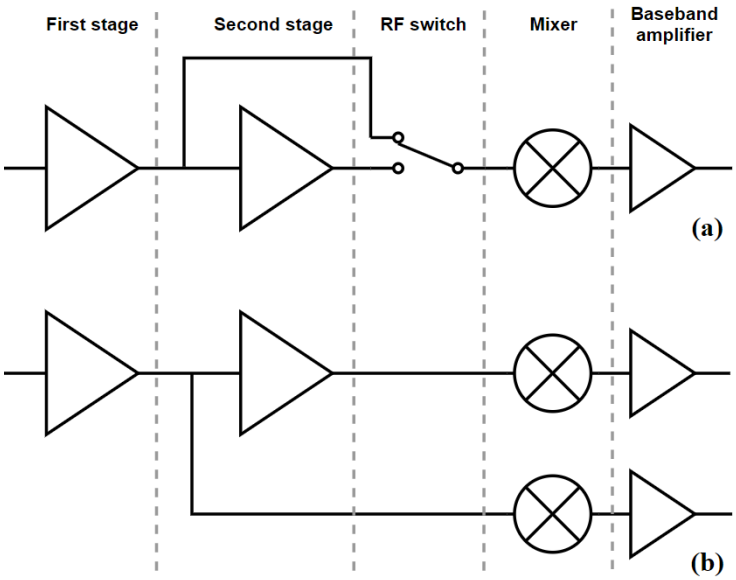


Figure 4.32: System-level illustrations of limitations for the first gain reconfiguration method.

However, the use of such a reconfigurable LNA introduces system-level constraints, namely the need to select the appropriate output path within the RF front-end. Several implementation options can be considered, as illustrated in Fig. 4.32. The use of an RF switch at the LNA output (4.32.a) may lead to increased noise, significant insertion losses, and potential signal integrity degradation, which is particularly critical in high-data-rate applications. Alternatively, duplicating RF paths by employing multiple mixers and baseband amplifiers (4.32.b) can be envisaged, at the cost of increased circuit area. In this case, concerns remain regarding switching-induced signal degradation as well as the overall footprint, which undermines the benefits of passive function integration within the LNA.

In light of these limitations, a new approach is proposed to further extend the capabilities and practical relevance of this reconfigurable amplifier concept.

4.4.3 Variable resistive load based reconfigurable mmW LNA

During the design phase of the reconfigurable LNA, it was observed that the interstage connection between the first and second gain stages plays a critical role in determining the overall gain and frequency response of the amplifier. In particular, leaving the interstage node weakly loaded (i.e., close to an open-circuit condition) resulted in a pronounced resonant behavior around 60 GHz and a significant degradation of the broadband gain performance.
A detailed analysis of the interstage network revealed that its magnetically coupled structure can be exploited to implement a continuous gain reconfiguration mechanism. Instead of modifying bias conditions or switching discrete gain paths, a variable resistive element is introduced within the interstage network. This approach enables a smooth control of the magnetic coupling strength between stages, while preserving a fully active two-stage operation. A key advantage of this technique is that it does not alter the DC operating point of the circuit; however, the total power consumption remains constant over the entire gain tuning range.
The reconfigurable amplifier therefore operates with both stages continuously active, while the gain is controlled through the resistive loading applied to the interstage network. In the targeted design, the tuning range of the resistive element spans from 0 to 50 Ω, enabling full gain control between the maximum and minimum gain states. The corresponding circuit implementation is shown in Fig. 4.33.

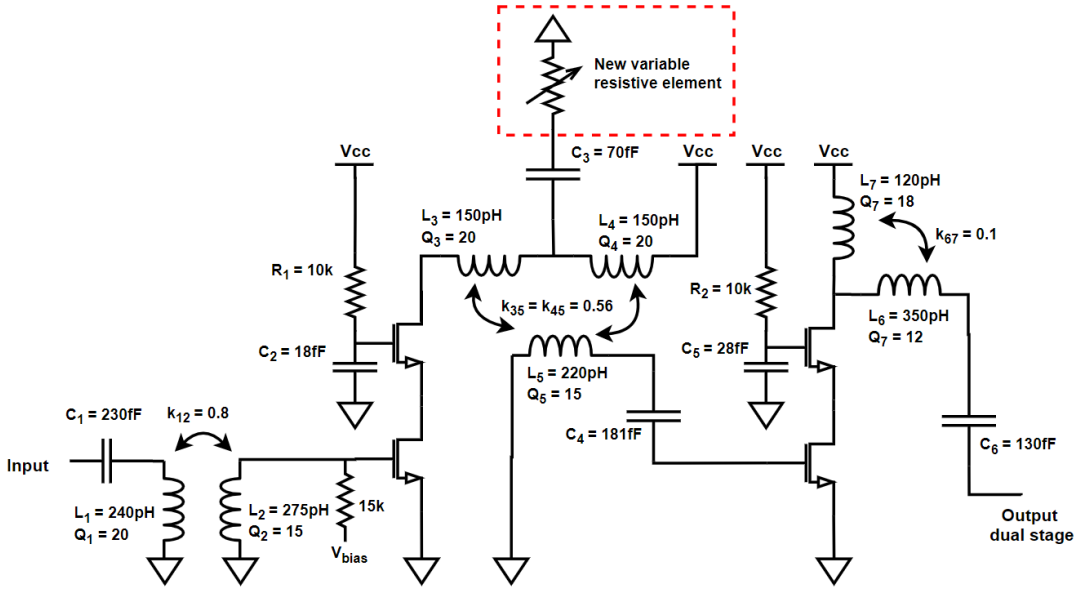


Figure 4.33: Schematic of the new reconfigurable mmW LNA including a variable resistive element allowing for controlled fine gain reconfiguration.

To better understand the physical mechanism underlying this reconfiguration strategy, the interstage network is analyzed in terms of its impedance transformation and magnetic coupling behavior. The simplified model used for this analysis is shown in Fig. 4.34.

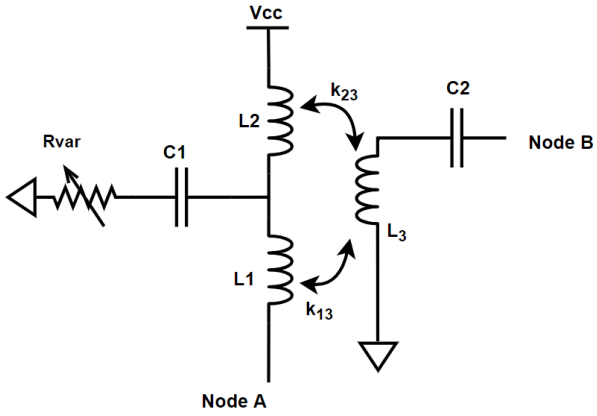


Figure 4.34: Simplified interstage network schematic including variable resistive element.

The interstage network consists of three magnetically coupled inductors L_1, L_2, and L_3, with mutual couplings defined as:

$$M_{13} = k_{13}\sqrt{L_1 L_3}, \qquad M_{23} = k_{23}\sqrt{L_2 L_3}. \tag{4.30}$$

No direct coupling exists between L_1 and L_2, and the coupling is exclusively mediated through L_3. Let $s = j\omega$.

Assuming moderate coupling, the impedance transformation induced by L_3 can be approximated as:

$$\Delta Z_1 \approx \frac{(sM_{13})^2}{Z_3}, \qquad \Delta Z_2 \approx \frac{(sM_{23})^2}{Z_3}, \tag{4.31}$$

where Z_3 denotes the effective impedance seen at the L_3 node including the output network loading.

The impedance seen at Node A (drain of the first stage) is given by:

$$Z_A(\omega) = (sL_1 + \Delta Z_1) + \left[(sL_2 + \Delta Z_2) \parallel \left(R_{\text{var}} + \frac{1}{sC_1}\right)\right]. \tag{4.32}$$

Defining the effective impedances:

$$Z_{L2}^{\text{eff}} = sL_2 + \Delta Z_2, \qquad Z_R = R_{\text{var}} + \frac{1}{sC_1}, \tag{4.33}$$

the expression becomes:

$$Z_A = sL_1 + \Delta Z_1 + \frac{Z_{L2}^{\text{eff}} \cdot Z_R}{Z_{L2}^{\text{eff}} + Z_R}. \tag{4.34}$$

The variable resistor does not act as a simple drain load but rather controls the current distribution within the L_2 branch. This directly modifies the magnetic flux coupled through L_3, which governs the energy transfer between the two amplification stages.

When R_{var} decreases, the impedance Z_R is reduced, resulting in a stronger current flow through L_2. This increases the magnetic coupling through L_3, enhancing the induced voltage at the next stage and improving overall gain.

Conversely, when R_{var} increases, the current in L_2 is reduced, weakening the magnetic coupling and decreasing the effective excitation of the second stage. In this regime, the interstage transformer becomes weakly driven, and the gain is reduced.

A transition region exists when $|Z_R|$ becomes comparable to $|Z_{L2}^{\text{eff}}|$, where the impedance at Node A exhibits strong frequency-dependent variations in both magnitude and phase. This region corresponds to the most effective gain tuning range and may also introduce resonant behavior depending on the operating frequency.

The impedance variation at Node A is transferred to Node B through the mutual inductance with L_3. The resulting impedance at Node B can be expressed as:

$$Z_B(\omega) \approx sL_3 + \frac{(sM_{13})^2}{Z_{A1}} + \frac{(sM_{23})^2}{Z_{A2}}, \tag{4.35}$$

where Z_{A1} and Z_{A2} represent the effective impedances seen by L_1 and L_2, respectively. Although not strictly identical, their behavior follows the same trend as Z_A, allowing a qualitative interpretation of the coupling mechanism.

When R_{var} is small, the strong loading of the L_2 branch increases the effective reflected impedance seen at Node B, enhancing voltage gain through stronger magnetic energy transfer. In contrast, for large R_{var}, the reduced coupling leads to a weaker reflected impedance

contribution, and the impedance at Node B tends toward its intrinsic value sL_3, resulting in reduced gain.

Overall, the variable resistor acts as a continuous control element that modulates the magnetic coupling strength of the interstage transformer. This mechanism enables smooth gain reconfiguration without modifying bias conditions or interrupting the RF signal path, making it particularly suitable for mmWave LNA applications.

As shown in Fig. 4.35, the impact of the variable resistive loading on the interstage behavior is illustrated through both the overall transducer gain (S_{21}) and the normalized RF current flowing in the coupled branch L_2. Increasing R_{var} from 0 to 50 Ω results in a monotonic degradation of S_{21}, which is directly correlated with a reduction of the RF current in L_2. This clearly highlights that the gain variation mechanism is governed by a progressive weakening of the magnetic coupling within the interstage transformer, rather than by a simple resistive loading effect at the drain of the first-stage cascode transistor.

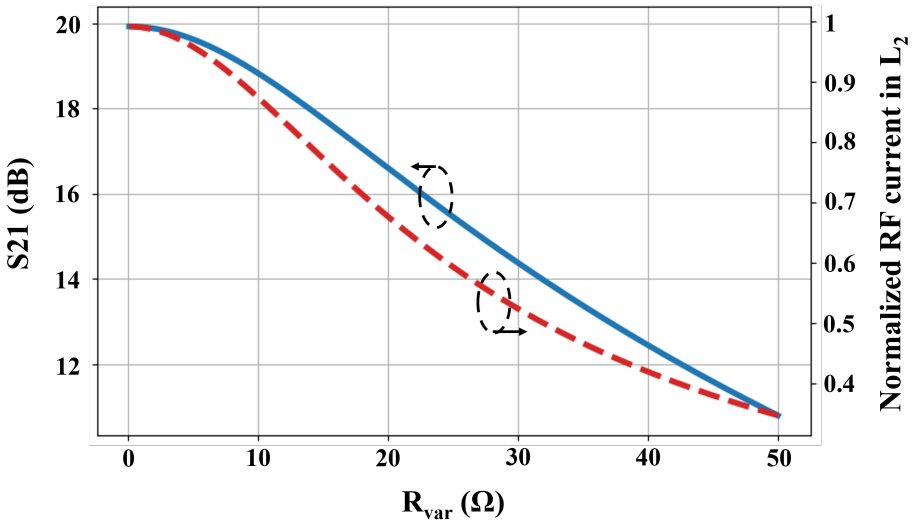


Figure 4.35: First-order approximation of the impedance at node A as a function of R_{var} variation.

This section presents the post-layout simulation performances of this new gain reconfiguration technique. The analysis includes the forward transmission coefficient (S_{21}), input reflection coefficient (S_{11}), noise figure (NF), and linearity, as characterized by the ICP1dB. It should be noted that, at this stage, no reconfigurable resistor structure has been implemented or simulated. Instead, the study relies on resistances extracted from the layout view, which are integrated at the block level within the overall circuit. At this stage, the pre-tapeout layout view is used, including the full ground planes and pad structures.

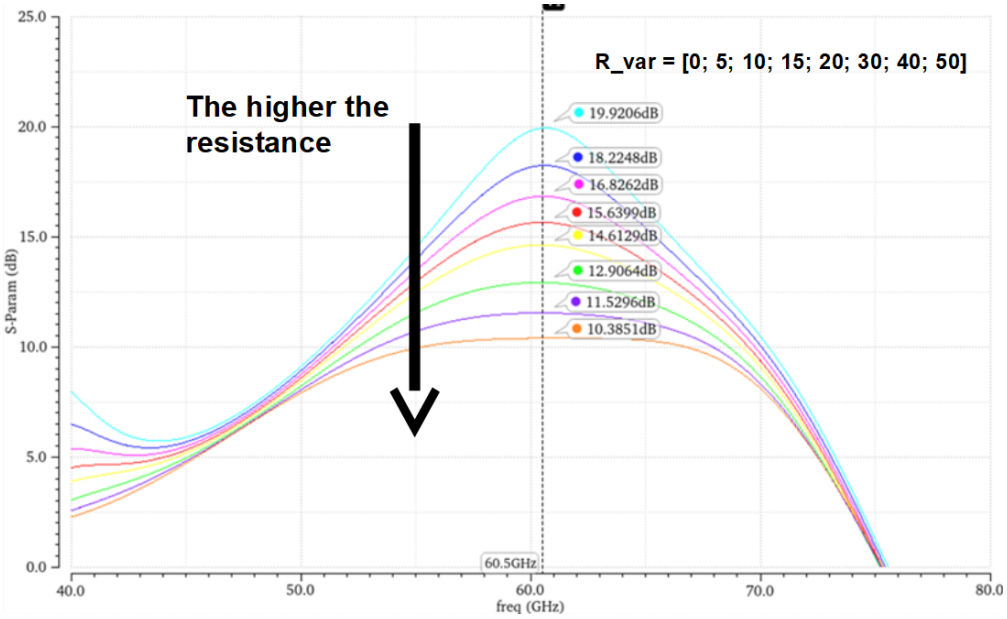


Figure 4.36: Simulated S_{21} reconfiguration range for R_{var} varying from 0 to 50 Ω.

As illustrated in Fig. 4.36, increasing R_{var} results in a reduction of the forward transmission coefficient S_{21}. This behavior is consistent with a reduced magnetic coupling efficiency in the interstage transformer, leading to a lower effective voltage transfer between stages. The input reflection coefficient S_{11}, shown in Fig. 4.37, exhibits only minor variations, indicating that the input matching remains largely preserved across the tuning range.

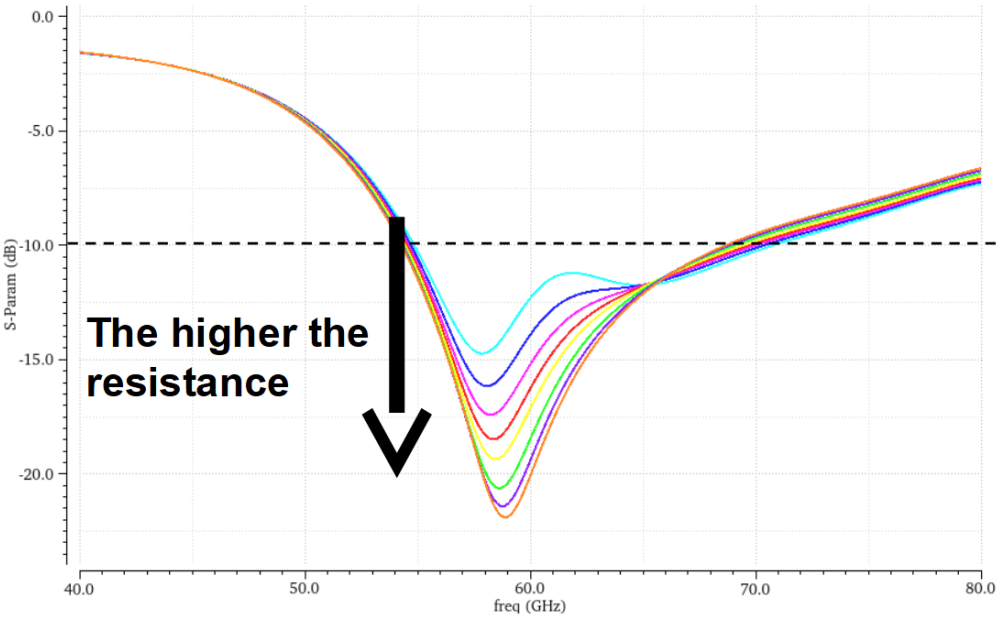


Figure 4.37: Simulated S_{11} variation as a function of R_{var} (0–50 Ω).

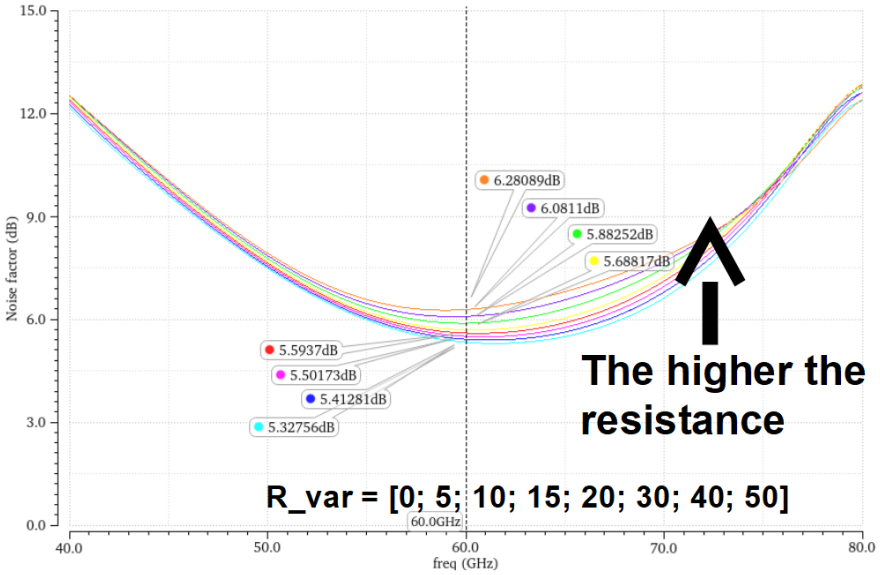


Figure 4.38: Simulated noise figure degradation as a function of R_{var} (0–50 Ω).

The noise figure behavior (Fig. 4.38) shows a moderate degradation with increasing R_{var}, which can be attributed to the reduced gain of the first stage and the corresponding decrease in effective noise suppression. Despite this degradation, the overall noise performance remains within acceptable limits for mmWave front-end operation.

Importantly, the linearity analysis (Fig. 4.39) confirms that the input-referred compression point remains nearly constant across the entire tuning range, indicating that the proposed gain reconfiguration mechanism does not significantly affect the intrinsic linearity of the amplifier.

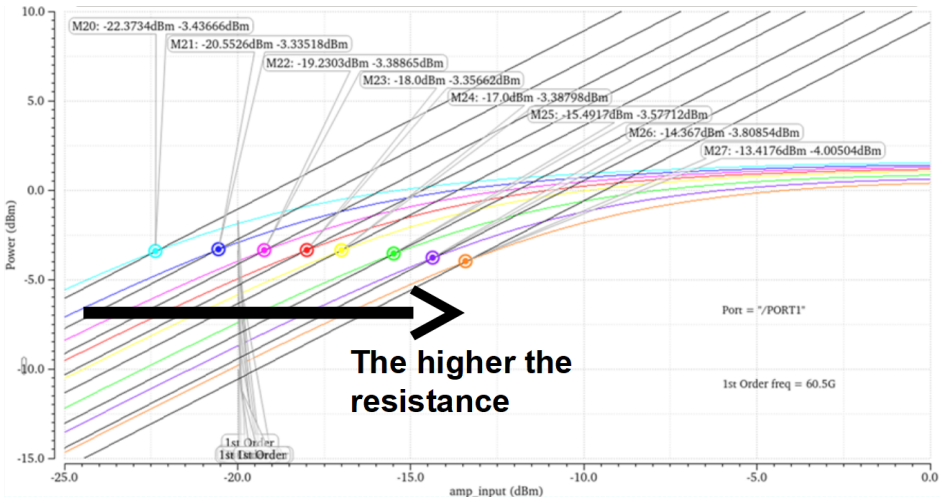


Figure 4.39: LNA linearity remains stable over the R_{var} range from 0 to 50 Ω.

The post-layout simulations demonstrate the interest of the proposed gain reconfiguration technique. It enables an analog control of the amplifier's gain without compromising linearity. The input reflection coefficient S_{11} is slightly degraded but remains satisfactory across the entire frequency band. A moderate noise figure increase of approximately 1 dB is observed, which is acceptable, although link-budget analyses would be required to quantify its impact at the transceiver level. Another notable aspect of this approach, as previously mentioned, is that the LNA's power consumption remains constant over the full gain range. This can be advantageous, as it ensures moderate and predictable DC power, facilitating better control through the supply circuitry. Conversely, it may be considered as a drawback in low-power operation, since the circuit continues to consume DC power even when reduced gain would suffice. Table 4.4 summarizes the simulated performance of this innovative gain reconfiguration technique.

Table 4.4: Summary of simulated performance metrics for the gain reconfiguration technique based on variable resistance R_{var}.

Parameter	$\boldsymbol{R_{\text{var}} = 0\ \Omega}$	$\boldsymbol{R_{\text{var}} = 50\ \Omega}$	**Comments**
S21 (dB)	19.9	10.4	Achieves fully controlled 9.5dB gain reconfiguration.
NF (dB)	5.33	6.28	Slight increase of 1dB in low power mode.
S11 (dB)	<-10	<-10	Satisfying input matching over frequency range.
ICP1 (dBm)	-23.3	-14.4	OCP1dB remains steady around -4dBm.
DC Power (mW)	14.48	14.48	Steady power consumption over complete range.
3dB Bandwidth (GHz)	7.7	23.9	Greatly increase gain bandwidth in low power mode.

Table 4.5: Comparison of the proposed work with state-of-the-art results.

	[45]	[46]	[47]	[48]	**This work**
Technology	28nm	65nm	22nm	65nm	**22nm**
f_c (GHz)	82.3	56.5	60.75	59.75	**60.5**
S21max (dB)	29.6	25	20.2	20	**19.9**
S21 range (dB)	11.6	17	7.1	17.5	**9.5**
NFmin (dB)	6.4	4.8	3.3	6.3	**5.3**
PDC (mW)	31.3	47	8.1	38.4	**14.48**
Area (mm^2)	0.254	0.26	0.2	0.08	**0.094**
FOM	6.75	7.25	26.83	18.08	**26.21**

$$\text{FOM} = \frac{S_{21,\max}[dB] \cdot S_{21,\text{range}}[dB]}{NF_{\min}[dB] \cdot P_{DC}[mW] \cdot Surface[mm^2]} \tag{4.36}$$

By comparing the performance of the proposed LNA with those of other state-of-the-art reconfigurable mmWave LNAs, and considering the figure of merit (FOM) defined in Equation (4.36) (Table 4.5), the proposed design demonstrates excellent overall performance. This can be primarily attributed to its low power consumption and small silicon area.

Following the comprehensive post-layout simulation analysis, the next section presents the measured results obtained from the fabricated prototype using on-wafer probing.

4.4.4 Post-Layout Simulation Validation and Substrate Modeling Issues

Initial post-layout electromagnetic simulations were carried out using Cadence EMX, which is commonly employed for on-chip passive extraction. However, following tape-out, a significant discrepancy was observed during the correlation phase between EM simulations and silicon measurements. A detailed investigation showed that, under its default configuration for the GF22 nm FDSOI process, EMX tends to underestimate substrate-related losses and parasitic coupling effects in the V-band. As a result, key performance metrics such as gain and noise figure were systematically overestimated, particularly for large passive structures such as the interstage transformer.

To identify the root cause of this discrepancy, a comprehensive re-extraction campaign was conducted, comparing EMX results with those obtained using ADS Momentum. Unlike EMX in its default setup, Momentum provides a more accurate representation of the substrate through a refined meshing strategy and a more complete modeling of loss mechanisms. These simulations were further validated against measurements from dedicated passive test structures fabricated in the same GF22 nm FDSOI technology. The comparison demonstrated that the observed mismatch is not merely attributable to solver-to-solver variations, but rather to intrinsic limitations in the default substrate modeling used by EMX at millimeter-wave frequencies.

To quantify this effect, Table 4.6 compares EMX and Momentum simulations against measurements for a representative transmission line, both with and without a patterned ground shield (PGS). The extracted parameters include the characteristic impedance Z_c, the attenuation constant α at 60 GHz, and the quarter-wavelength $\lambda/4$.

Table 4.6: Comparison of EMX and Momentum simulations with measurements for transmission lines with and without PGS. [47]

Structure	Parameter	EMX	Momentum	Measurement
With PGS	Z_c (Ω)	49	49.7	48
	α (dB/mm) @ 60 GHz	0.54	0.59	0.59
	$\lambda/4$ (μm)	580	584	558
Without PGS	Z_c (Ω)	53.5	49.7	52.5
	α (dB/mm) @ 60 GHz	0.54	0.70	0.67
	$\lambda/4$ (μm)	607	620	613

As shown in Table 4.6, both solvers provide comparable results when a PGS is present, with good agreement to measurements in terms of both attenuation and characteristic impedance. In this configuration, the electromagnetic fields are largely confined above the substrate, which reduces sensitivity to substrate modeling assumptions.

Based on these findings, combined with similar observations across multiple design projects, internal design guidelines were progressively updated to favor the use of ADS Momentum for the extraction of critical passive components operating in the V-band. This evolution reflects a broader recognition that accurate substrate modeling is essential for reliable millimeter-wave design, particularly for passive structures that strongly interact with the silicon substrate.

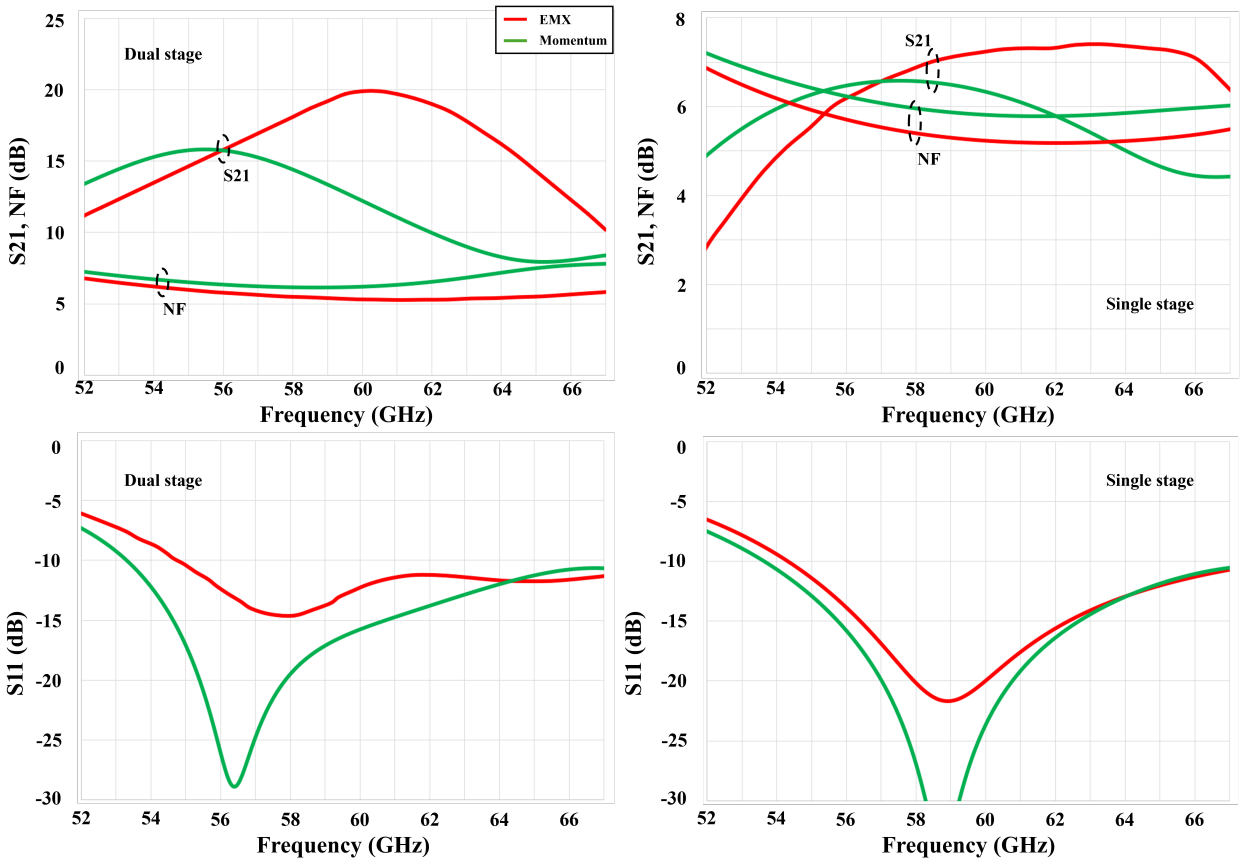


Figure 4.40: Comparison of S-parameters and Noise Figure extracted with EMX and Momentum. Momentum predicts a significant gain reduction and NF increase due to better modeling of substrate losses.

Figure 4.40 compares the S-parameters and noise figure (NF) obtained using EMX and Momentum for both the single-stage and dual-stage configurations. A clear trend can be observed: simulations based on EMX consistently predict higher gain and lower NF than those based on Momentum. This optimistic bias is a direct consequence of the underestimated attenuation in passive interconnects and transformers, which artificially improves both signal transmission and noise performance.

In the dual-stage configuration, Momentum predicts a peak gain of approximately 15.9 dB (vs. 19.9 dB with EMX) and a noise figure of 6.1 dB (vs. 5.3 dB). In the single-stage configuration, the maximum gain obtained through Momentum is 6.5 dB (vs. 7.5 dB with EMX), with a minimal NF close to 5.8 dB (vs. 5.2 dB). This gain drop and NF increase are attributed to the accurate modeling of substrate leakage in the transformer windings, which were previously underestimated. Consequently, all subsequent comparisons with measured data in this chapter are based on the Momentum-extracted netlist, as it provides a physically realistic baseline closer to the silicon reality.

4.5 Experimental Validation

4.5.1 Measurement Setup and Experimental Constraints

The experimental validation of the fabricated prototype was conducted using on-wafer probing techniques. The chip, fabricated in GlobalFoundries 22 nm FDSOI technology, corresponds to the dual-output architecture described in Section 4.4.2, featuring distinct output pads for the single-stage and dual-stage configurations. This version predates the integration of the continuous gain control element (R_{var}), focusing instead on the discrete reconfiguration between the two amplification modes. The complete fabricated chip is presented in the following figure.

The measurement campaign encountered significant logistical and technical challenges that necessitated a departure from the standard characterization protocol. The primary constraint stemmed from the chip's pad geometry: the input/output pads were designed with a pitch of 125 μm. While this pitch was optimized for the specific probe card available at the industrial partner's facility (configured with 5 ports: GSG for RF input and GSGSG for RF output), it proved incompatible with the standard probe kits available at the university laboratory where the measurements were eventually performed due to an unforeseen

equipment failure (breakage of the DC probes at the industrial site).

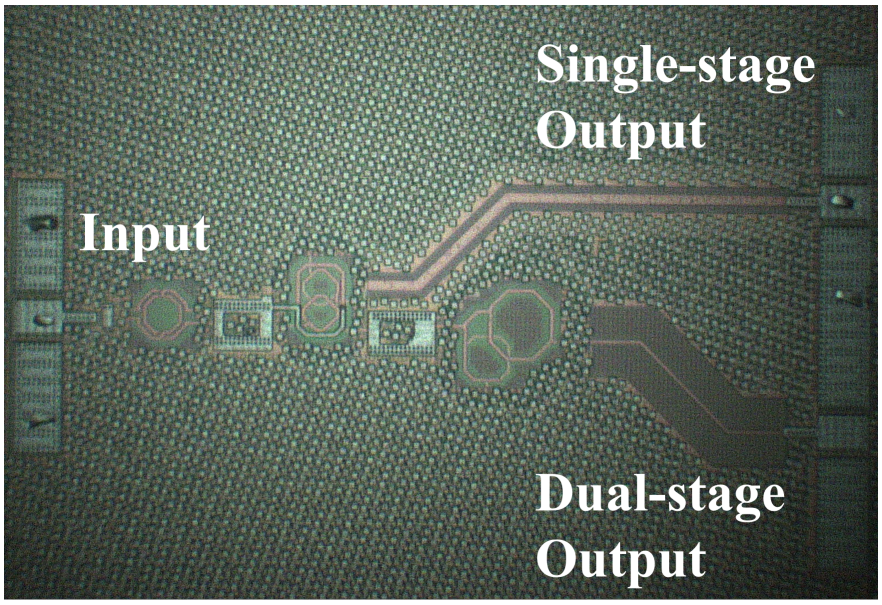


Figure 4.41: Photography of the manufactured chip.

Consequently, the measurement setup had to be adapted under constrained conditions, introducing several non-idealities that required careful analysis:

1. **Probe Pitch Mismatch**: The university probes, designed for standard 100 μm or 150 μm pitches, could not align perfectly with the 125 μm pads. This misalignment necessitated a manual "bridging" technique, increasing the risk of parasitic coupling and contact resistance variations.

2. **Limited DC Grounding Access**: The pad layout, combined with the probe pitch mismatch, restricted the number of accessible DC ground pads. Specifically, only three pads could be contacted on the top row (1 ground, 2 signals) and three on the bottom row (0 ground, 3 signals). In a standard configuration for DC biasing, dedicated ground pads are placed to ensure a symmetric return path and minimize ground loop inductance for the bias network. The inability to access all required DC ground pads in our setup altered the ground return path topology for the bias currents, potentially introducing additional inductive parasitics in the bias network and affecting the stability of the DC operating points.

3. **Sequential Probing and Micro-Soldering**: The lack of a GSGSG probe set prevented simultaneous probing and termination of the output RF ports. To characterize the dual-stage (high-gain) mode, the single-stage output pad had to be electrically grounded - or connected to a variable resistance - to prevent signal leakage and oscillation. Given the inability to place a probe on this specific pad due to the pitch constraints, a micro-soldering technique using conductive silver glue was employed to create a permanent low-impedance ground connection. While effective for establishing the DC ground, this process introduced a localized cluster of parasitic capacitance and inductance at the interstage node, a critical point for the amplifier's stability and gain.

These constraints imply that the measured results cannot be directly compared to the post-layout simulations (PLS) without accounting for the specific parasitic environment created by the measurement setup. The following sections detail the measured performance and the back-simulation methodology used to decouple the intrinsic circuit performance from the measurement artifacts.

4.5.2 S-Parameters and Gain Performance

The scattering parameters (S-parameters) were measured using a vector network analyzer (VNA) calibrated via a Short-Open-Load-Thru (SOLT) procedure on a calibration substrate. The frequency sweep covered the 57–64 GHz V-band.

DC Bias Verification

To rule out biasing errors as a cause for the performance degradation, the DC currents at the drain of the cascode transistors were measured directly on the chip. The measured currents ($\approx$ 12 mA for the dual-stage mode) match the simulated values (12.11 mA) with high precision. This confirms that the biasing network is functioning correctly and that the transistors are operating in the intended region of the I_D-V_{GS} curve. The performance loss is therefore purely RF-related, not DC-related.

Input Matching (S_{11})

The input reflection coefficient (S_{11}) is shown in Fig. 4.42. A clear discrepancy is observed between electromagnetic simulations and measurements, with markedly different levels of accuracy depending on the solver used.

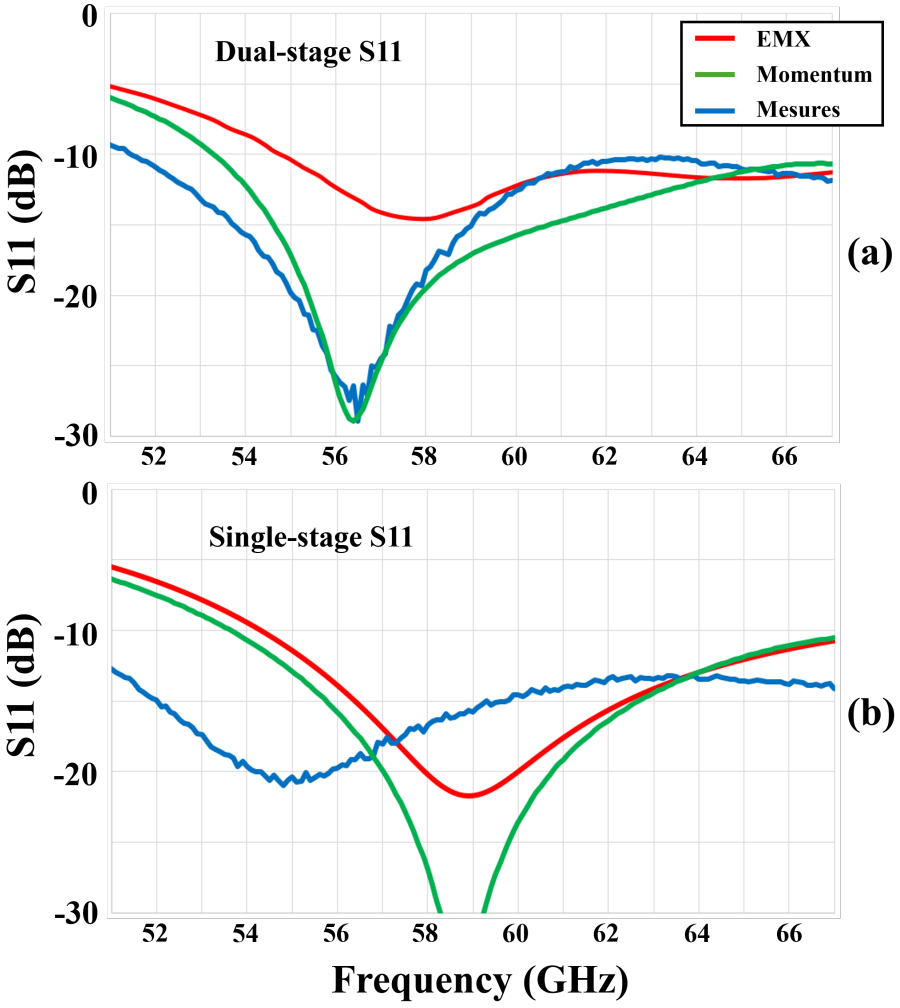


Figure 4.42: Comparison of measured and EM-extracted input matching performance (S_{11}). Top: dual-stage configuration. Bottom: single-stage configuration.

The EMX simulations exhibit significant deviations in both resonance frequency and matching level, failing to accurately reproduce the measured S_{11} response in either configuration. In contrast, Momentum shows a substantially improved agreement, confirming the importance of accurate passive and substrate modeling for predicting input matching behavior.

Despite these discrepancies, it is important to note that the S_{11} specification of -10 dB is met in both simulations and measurements for the two configurations, ensuring that the input matching remains acceptable from a system-level perspective.

For the dual-stage design, an excellent correlation is observed between Momentum and measurements. Both the resonance frequency and the overall shape of the S_{11} curve are well captured, with the measured response remaining below -10 dB over a large portion of the 57–64 GHz band.

For the single-stage configuration, a noticeable frequency shift is observed, with the measured minimum occurring at lower frequencies than predicted. It is worth emphasizing that the input matching network relies on the same symmetric transformer-based structure in both configurations. Therefore, the observed discrepancy cannot be attributed to a change in topology. Instead, it is primarily related to circuit-level effects. In particular, the lower gain of the single-stage amplifier (approximately 2.1 dB) results in reduced reverse isolation, making the input impedance more sensitive to external parasitics such as pad capacitances and probing effects. This increased sensitivity contributes to the observed frequency shift, although residual inaccuracies in passive modeling may also play a secondary role.

Forward Gain (S_{21}) and Frequency Shift

Figure 4.43 presents the measured forward gain (S_{21}) for both operating modes, compared against the Momentum-extracted and EMX-extracted post-layout simulations.

The data reveals a systematic reduction in gain and a frequency shift compared to the Momentum baseline. In the single-stage mode, the measured peak gain is 2.1 dB, compared to the Momentum-predicted 6.5 dB (a 4.4 dB loss). In the dual-stage mode, the measured peak is 11.5 dB, against the Momentum-predicted 15.9 dB (a 4.4 dB loss).

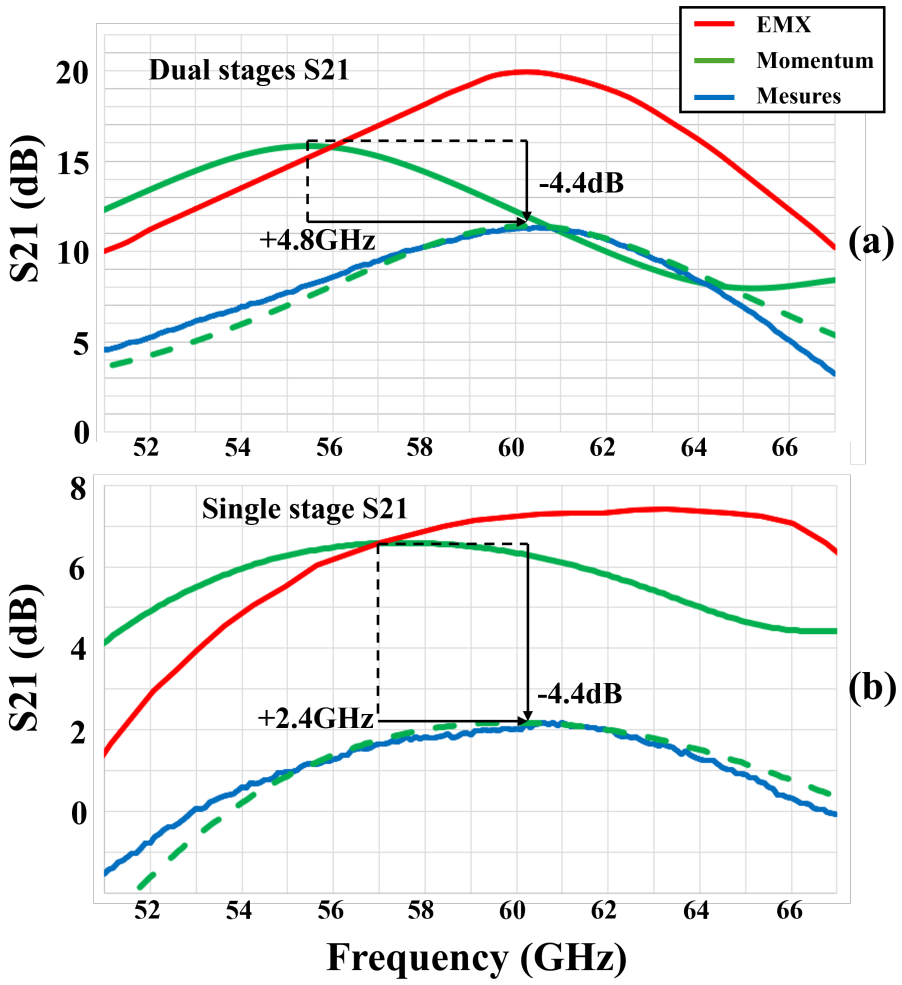


Figure 4.43: Comparison of measured and Momentum-extracted forward gain (S_{21}). (a) High-gain mode, (b) Low-gain mode.

Crucially, the frequency response exhibits a downward shift: the center frequency moves from 60 GHz (simulated) to 57.6 GHz (measured) in single-stage mode, and to 55.2 GHz in dual-stage mode. This corresponds to a shift of 2.4 GHz for the single-stage configuration and 4.8 GHz for the dual-stage configuration. While this apparent doubling might suggest a cumulative effect, it should not be interpreted as a strictly systematic behavior. Instead, the 2.4 GHz shift observed in the single-stage configuration is taken as a first-order estimate of the intrinsic frequency deviation, primarily attributed to process variations affecting passive components (e.g., metal thickness, dielectric properties, and transformer parameters). The additional shift observed in the dual-stage configuration is more likely related to measurement-specific conditions, introducing extra loading at sensitive nodes such as the interstage and output networks.

Despite these frequency deviations, the *shape* of the gain response remains consistent with Momentum simulations, confirming that the underlying amplification mechanism and matching topology are preserved.

Furthermore, the residual gain deficit is 4.4 dB in both the single-stage and dual-stage configurations. The fact that this loss remains constant across operating modes indicates that it originates from a common portion of the circuit, namely the first amplification stage and the interstage network. This observation also suggests that the silver glue used in the measurement setup does not introduce significant resistive losses. If it did, a larger degradation would be expected in the dual-stage configuration. Instead, its impact is more plausibly explained by parasitic capacitive and inductive effects, which contribute to the observed frequency shifts without significantly increasing dissipative losses. These parasitic effects will be further analyzed and quantified in the following section through back-simulation.

Linearity ($OCP_{\mathbf{1dB}}$)

While the small-signal gain exhibited a significant reduction due to substrate losses and measurement parasitics, the large-signal linearity of the LNA remains robust. The linearity was assessed by measuring the 1-dB output compression point (OCP_{1dB}), which represents the maximum output power the amplifier can deliver before the gain compresses by 1 dB. Table 4.7 summarizes the linearity metrics for both operating modes. Crucially, the measured OCP_{1dB} values are nearly identical to the Momentum-extracted simulations, despite the discrepancies in small-signal gain.

Table 4.7: Summary of linearity performance: Simulated (Momentum) vs. Measured. The output compression level (OCP_{1dB}) remains consistent, confirming the integrity of the active stages.

Metric	**High-Gain Mode**		**Low-Gain Mode**	
	Sim.	**Meas.**	**Sim.**	**Meas.**
Small-Signal Gain (dB)	15.9	11.5	6.5	2.1
$OCP_{\mathbf{1dB}}$ **(dBm)**	**-3.4**	**-3.2**	**-2.0**	**-1.5**

In the high-gain mode, the simulated OCP_{1dB} is -3.4 dBm, while the measured value is -3.2 dBm, a deviation of only 0.2 dB. Similarly, in the low-gain mode, the values are -2.0 dBm (simulated) and -1.5 dBm (measured), differing by merely 0.5 dB.

This preservation of the output compression level is a critical finding. It demonstrates

that the intrinsic saturation behavior of the cascode transistors is intact and that the active devices reach their non-linear limits at the exact output power levels predicted by the design. The observed shift in the input compression point ($ICP_{1\text{dB}}$) is therefore purely a consequence of the passive attenuation (gain loss) occurring upstream in the signal chain, rather than a degradation of the transistors' linearity. This confirms that the core amplification stages are functioning correctly, and that the performance gap is entirely attributable to the passive network losses and measurement setup artifacts discussed previously.

Noise Figure (NF)

The Noise Figure (NF) was measured using the Y-factor method with a calibrated noise source. The measurement setup is illustrated in Fig. 4.44. The results are presented in Fig. 4.45, together with EMX and Momentum simulations.

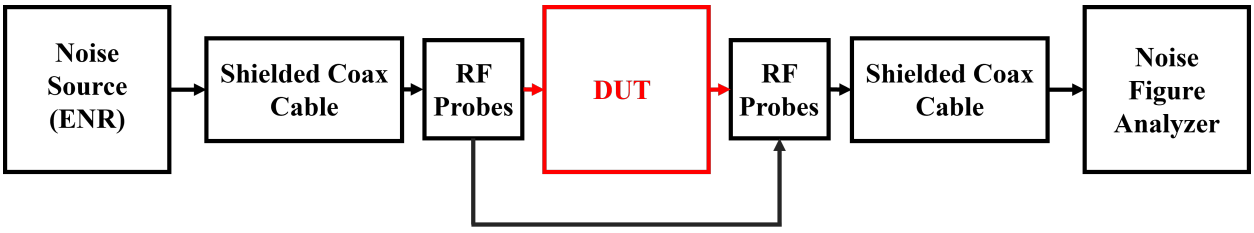


Figure 4.44: Block diagram of the NF measurement setup using the Y-factor method.

A clear difference in correlation with measurements is observed between the dual-stage and single-stage configurations.

For the dual-stage design (Fig. 4.45a), Momentum simulations show good agreement with measurements, with a small offset of approximately 0.4 dB around 60 GHz. A frequency shift of about 3.5 GHz toward lower frequencies is also observed in measurements; however, the overall shape of the NF response remains well preserved. This indicates that Momentum correctly captures the dominant noise mechanisms and their frequency dependence, and validates its use for noise prediction in the high-gain operating mode.

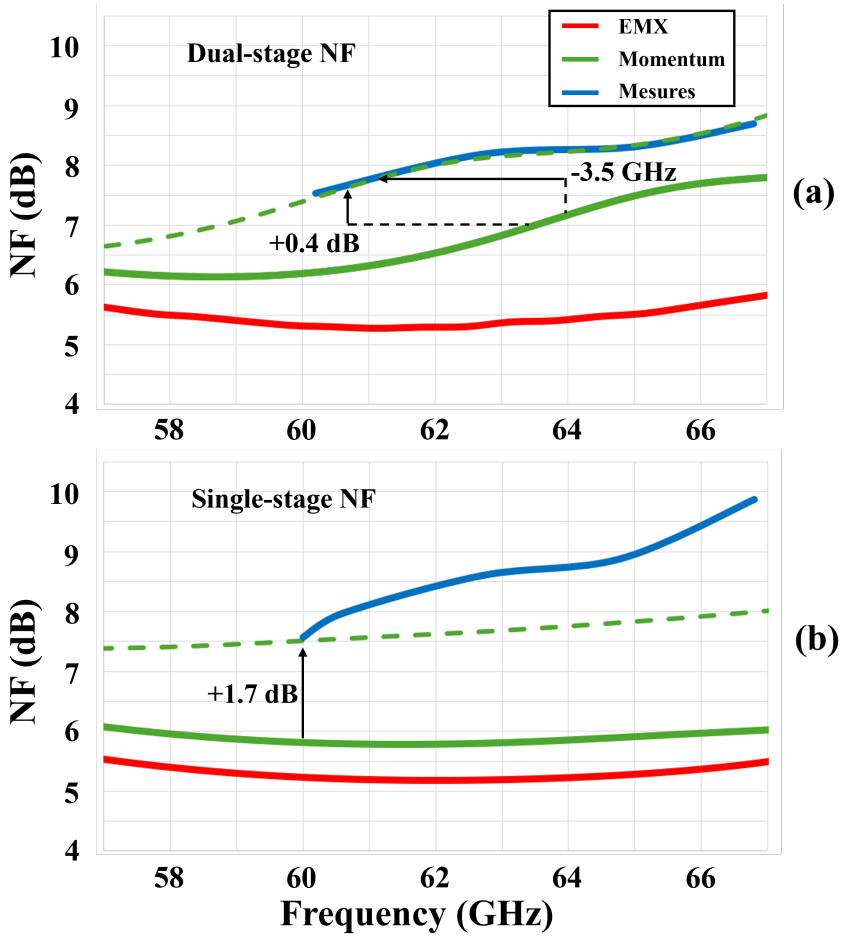


Figure 4.45: Comparison of measured and simulated Noise Figure (NF). (a) dual-stage (high-gain) configuration and (b) single-stage (low-gain) configuration.

In contrast, the single-stage configuration (Fig. 4.45b) exhibits a significantly larger deviation, with an NF offset of approximately 1.7 dB and a distortion of the frequency response that cannot be corrected by a simple frequency alignment. This suggests that the discrepancy is not solely due to passive modeling inaccuracies or uniform parasitic detuning.

This behavior can be understood by considering the low available gain of the single-stage configuration (approximately 2 dB at 60 GHz), which is comparable to the total insertion loss of the measurement chain (8.7 – 10.1 dB), as illustrated in the measurement setup of Fig. 4.44. Under such conditions, the Y-factor extraction becomes highly sensitive to the receiver noise and to calibration accuracy. In addition, according to Friis' formula:

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_1} + \dots \tag{4.37}$$

a low first-stage gain significantly reduces the isolation between the DUT and the measurement system, making the extracted NF representative of the combined system rather than the DUT alone.

Consequently, while the dual-stage NF results can be considered quantitatively reliable, the single-stage measurements should be interpreted as system-level indicators rather than absolute device NF values. They remain nevertheless useful to capture the relative degradation of noise performance in low-gain operation.

Finally, EMX simulations underestimate the NF in both configurations and fail to reproduce the measured trends, further confirming the limitations of this solver for accurate noise prediction in this technology node.

In summary, the dual-stage configuration demonstrates good agreement between Momentum and measurements, whereas the single-stage NF is strongly impacted by the limited gain and the non-negligible contribution of the measurement system.

Before moving to the analysis of the discrepancies, table 4.8 references key metrics.

Table 4.8: Summary of measured vs. simulated performance metrics.

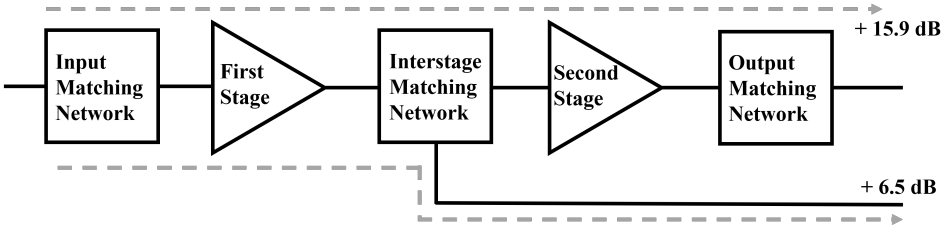
Metric	**Simulated (Momentum)**	**Measured**	**Deviation**
Gain (Single-Stage)	6.5 dB	2.1 dB	−4.4 dB
Gain (Dual-Stage)	15.9 dB	11.5 dB	−4.4 dB
S_{11} Min. Freq. (Single-Stage)	58.9 GHz	55 GHz	−3.9 GHz
S_{11} Min. Freq. (Dual-Stage)	56.5 GHz	56.5 GHz	Match
Noise Figure (Single-Stage)	5.8 dB	7.5 dB	+1.7 dB
Noise Figure (Dual-Stage)	6.1 dB	7.6 dB	+0.4 dB (*)
DC Current (Dual-Stage)	12.11 mA	12.1 mA	Match
$OCP_{1\text{dB}}$ (Single-Stage)	-2 dBm	-1.5 dBm	+0.5 dB
$OCP_{1\text{dB}}$ (Dual-Stage)	-3.4 dBm	-3.2 dBm	+0.2 dB

* Including the 3.5 GHz frequency shift.

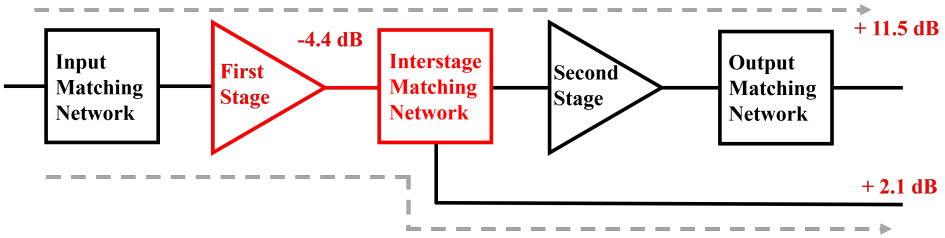
4.5.3 Simulation-to-Silicon Discrepancies and Performance Analysis

The systematic gain loss observed across both operating modes, combined with the preserved S_{11} response and accurate DC biasing, points toward a localized physical mechanism rather than a global design failure. A part of this discrepancy is therefore likely linked to the measurement conditions described in Section 4.5.1.

Biasing errors can be reasonably excluded, as both the DC operating points and input matching are in good agreement with simulations, indicating that the transistors operate within expected conditions. A key observation further supports this conclusion: the excellent agreement of the measured $OCP_{1\text{dB}}$ with simulations in both single-stage and dual-stage configurations. Since output compression is directly governed by the intrinsic large-signal behavior of the devices, this strongly suggests that the active stages themselves are not responsible for the observed degradation.



(a) Power gain distribution across the RF chain issued from Momentum post-layout simulations.



(b) Power gain distribution across the RF chain estimated from the measurements.

Figure 4.46: Breakdown of gain contributions showing the primary loss location at the interstage network.

When combined with the nearly constant gain loss of approximately 4.4 dB observed in both configurations, this strongly suggests a systematic attenuation mechanism originating from the circuit blocks shared between both modes of operation, as illustrated in Fig. 4.46. In particular, the losses are most likely concentrated in the first-stage amplifier and the interstage network.

At this point, it remains difficult to determine whether this degradation is caused by excess losses in the passive structures (e.g., interconnects, matching network, or pad access) or by an impedance mismatch at the output of the first amplification stage, leading to suboptimal power transfer toward the subsequent stage. Both mechanisms would result in a similar observable effect, namely a reduced effective gain without significantly affecting the compression behavior.

Consequently, the most plausible explanation is a parasitic quantification error associated with the unconventional measurement setup, introducing additional losses or mismatch effects that are not accurately captured in the simulations.

Two main candidates were investigated to explain this attenuation:

1. **Interstage Transformer Modeling Accuracy**: The interstage transformer is a particularly complex and critical component of the design. The transition from EMX to Momentum has revealed significant discrepancies in the modeling of passive structures, suggesting potential inaccuracies in the representation of distributed coupling effects.

2. **Silver Glue Parasitics**: The micro-soldering with conductive silver glue, combined with the asymmetric ground return paths, potentially introduced a significant parasitic RLC load at the single-stage output node.

The first hypothesis is related to the electromagnetic modeling of the interstage transformer. Due to time and fabrication constraints, no design iteration of this transformer could be performed to experimentally validate this hypothesis. However, internal studies conducted on similar inductive structures using both EMX and Momentum have shown noticeable differences in predicted performance, especially in terms of quality factor and coupling accuracy. This suggests that EMX may not fully capture the distributed coupling effects in such structures. As a result, it is plausible that the actual transformer exhibits non-ideal behavior, such as residual coupling between the primary windings or insufficient coupling between primary and secondary coils, leading to degraded power transfer and additional insertion loss.

The second hypothesis concerns the measurement setup itself, which is consistent with a predominantly reactive parasitic effect. An additional 2.4 GHz upward shift is observed in the dual-stage configuration (see Fig.4.43), resulting in a total shift of 4.8 GHz. This additional deviation is therefore not present in the single-stage mode and can likely be attributed to the presence of the silver glue used to ground the single-stage output pad. This behavior suggests the introduction of an additional parasitic capacitance at this node. In the dual-stage configuration, the grounded pad becomes electrically coupled to the interstage network, which is highly sensitive to capacitive loading due to its transformer-based matching structure. As a result, the added capacitance detunes the interstage resonance, as illustrated in Fig. 4.47, where a purely capacitive load reproduces the observed additional frequency shift without significantly affecting the gain level. The simulation setup is presented in Figure. 4.48.

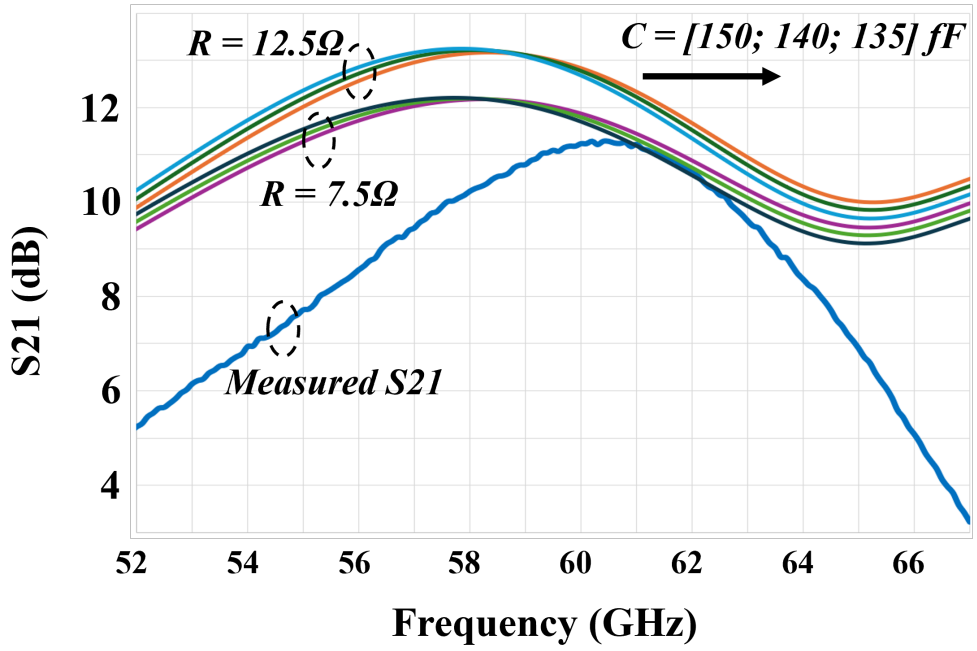


Figure 4.47: Impact of an RC parasitic network induced by silver glue on S21 performance in dual-stage configuration.

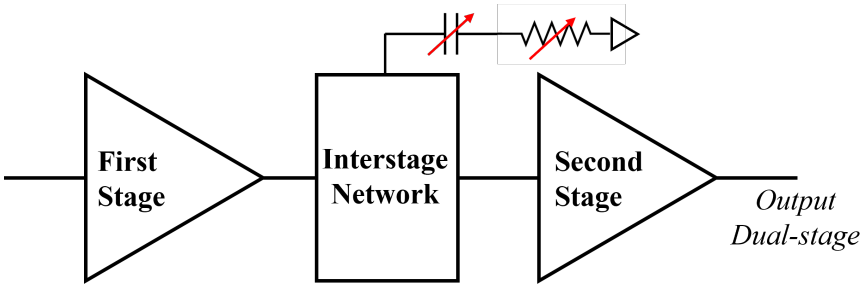


Figure 4.48: Simulation setup for the quantification of parasitics induced by the silver glue added on single-stage output pad.

4.5.4 Opportunities for Improving the Proposed Reconfiguration Concept

While the measurement campaign faced significant logistical hurdles, it yielded critical insights for future design iterations and the validation of the reconfiguration concept. The experience underscores the necessity of standardizing pad pitches to 100 μm or 150 μm in future designs to ensure compatibility with a wider range of probing equipment and to avoid custom workarounds.

The next design iteration should leverage the lessons learned regarding substrate modeling. The circuit should be re-tuned using the more accurate ADS Momentum solver, which has proven to better capture substrate losses and coupling effects in the GF22nm FDSOI process. Furthermore, the implementation of Patterned Ground Shields (PGS) beneath critical passive structures, such as the interstage transformer and input matching network, is strongly recommended. As demonstrated in the transmission line analysis, PGS significantly reduces the sensitivity of the attenuation constant (α) to substrate variations, thereby stabilizing the gain and noise figure predictions and bringing the simulated performance closer to the silicon reality.

The successful back-simulation correlation validates the robustness of the proposed transformer based interstage network and the reconfiguration concept. The primary path forward involves a re-spin of the chip to integrate the continuous gain control mechanism (R_{var}) with an optimized layout. Despite the experimental constraints, this work demonstrates the feasibility of a reconfigurable 60 GHz LNA with a 10 dB gain control range. The measured data, when corrected for setup-induced parasitics, aligns with the theoretical predictions, paving the way for the deployment of such front-ends in high-speed wireless USB 3.2 interfaces.

4.6 Conclusion

This chapter has demonstrated the design, implementation, and experimental validation of a reconfigurable LNA targeting short-range 60 GHz wireless USB 3.2 links. The proposed architecture addresses system-level dynamic range constraints through a dual-mode operation, enabling both high sensitivity (two-stage mode) and high linearity (single-stage mode).

The main contributions are threefold.

First, a design methodology for low-coupled stacked inductances has been established. By exploiting vertical superposition with a controlled overlap ratio ($\rho \approx 0.3$), magnetic coupling is significantly reduced, enabling up to 50% footprint reduction while preserving inductance and quality factor. This approach proved essential for the compact implementation of the interstage transformer.

Second, a multi-functional interstage network has been introduced as the core enabler of reconfigurability. It supports both active stage bypassing and continuous gain control through a variable resistive load. This unified passive structure provides fine-grained dynamic range control with minimal impact on noise figure and input matching, while maintaining architectural simplicity.

Third, the circuit has been implemented in GlobalFoundries 22 nm FDSOI technology and validated through on-wafer measurements. Despite non-ideal measurement conditions, the results confirm the correct operation of the active core, with input matching, DC biasing, and compression behavior in strong agreement with simulations. A gain reduction of approximately 4.4 dB is observed and is attributed to parasitic effects in the interstage network and measurement setup, more accurately captured by Momentum simulations than by EMX. These effects will be mitigated in future iterations through refined EM co-design and the integration of patterned ground shields.

Building on this validated block-level characterization, the next step is the integration of the LNA into a complete receiver chain. To meet the stringent requirements of USB 3.2 (10 Gb/s data rate, BER $\leq 10^{-12}$, and latency < 3 ns), the LNA will be cascaded with the impedance transformation network, active mixers, and wideband baseband amplifiers.

The following chapter presents the system-level design and integration of the 60 GHz receiver front-end. Using corrected block-level data, a hierarchical analysis is conducted to verify compliance with the target specifications. This approach demonstrates the feasibility of a fully wireless USB 3.2 link and establishes the proposed reconfigurable LNA as a key enabler of the receiver architecture.

Chapter 5

Towards a 60 GHz CMOS Receiver: System Design and Integration

5.1 Introduction

The preceding chapters have established the system-level specifications, architectural choices, and circuit-level implementations required for a 60 GHz CMOS receiver targeting short-range high-throughput wireless links compliant with the USB 3.2 standard. In particular, Chapter 2 defined the target requirements in terms of data rate (10 Gb/s), bit error rate (BER $\leq 10^{-12}$), and latency (< 3 ns), while Chapter 3 derived the corresponding architectural framework and block-level specifications. Chapter 4 then introduced a reconfigurable low-noise amplifier designed to address the large dynamic range associated with short-range millimeter-wave communication links.

The objective of this chapter is to evaluate the system-level consistency of the proposed receiver architecture when all previously designed RF and baseband blocks are integrated into a complete front-end chain. This step does not introduce new circuit designs but verifies that the combination of the individual building blocks satisfies the global system constraints under realistic implementation assumptions.

The receiver architecture integrates the reconfigurable LNA, a passive impedance transformation and distribution network, active downconversion mixers, and wideband baseband amplifiers. The local oscillator (LO) generation and quadrature phase synthesis are assumed to be externally provided, as commonly done in early-stage millimeter-wave system validation. This assumption allows the intrinsic performance of the RF and baseband signal chain to be assessed independently of phase noise and PLL implementation constraints.

Since full transistor-level cosimulation of the complete receiver is not tractable at this stage, a hierarchical validation methodology is adopted. Moreover, this study predates the transition from EMX to Momentum. Therefore, the initial performance of the LNA will be retained. The system-level evaluation is based on:
(i) circuit-level characterization of each block,
(ii) analytical cascade modeling of gain, noise figure, and linearity using standard RF relations (e.g., Friis equations),
and (iii) spreadsheet-based system-level evaluation of link budget, signal-to-noise ratio, and derived BER performance under QPSK modulation.

This framework provides a transparent and reproducible methodology to assess compliance with USB 3.2 requirements while clearly identifying the underlying modeling assumptions and limitations.

5.2 Complete Receiver Architecture

5.2.1 System-Level Block Diagram

The complete receiver architecture is illustrated in Fig. 5.1. The signal chain begins with the reconfigurable LNA, followed by a passive power splitting and impedance transformation network. The RF signal is then distributed into two identical downconversion branches enabling I/Q demodulation.

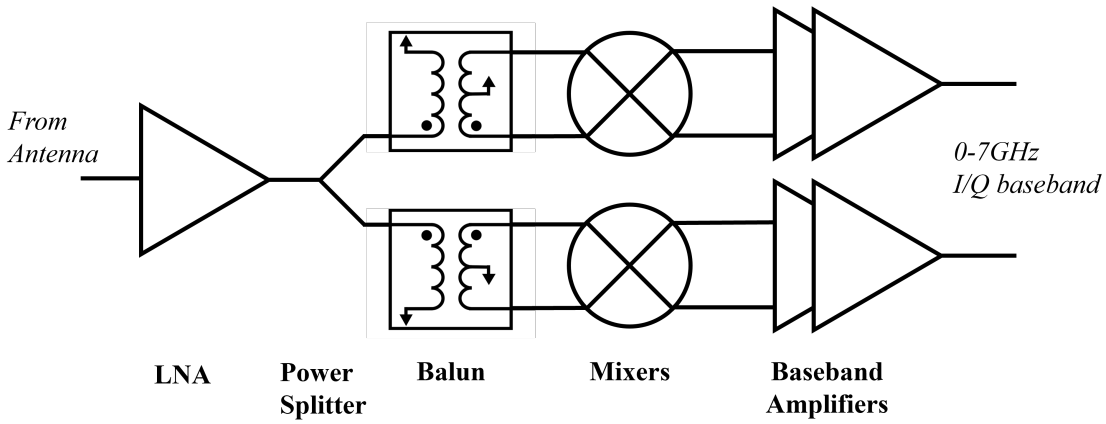


Figure 5.1: System-level block diagram of the proposed 60 GHz receiver front-end. The architecture highlights the dual-path I/Q downconversion and the passive impedance transformation network enabling single-ended to differential conversion.

Compared to conventional single-chain receivers, the proposed architecture offers several system-level advantages:

- **Robust I/Q demodulation:** enabling coherent QPSK detection without requiring digital post-processing for phase reconstruction.
- **Distributed linearity:** achieved by splitting the RF signal power across two parallel mixer paths.
- **Integrated impedance adaptation:** realized through passive splitter and balun networks, avoiding dedicated active matching stages.

It is important to note that any linearity improvement arises from power distribution rather than intrinsic enhancement of individual nonlinear devices.

5.2.2 Impedance Transformation Network

The main constraint when transitioning from a single-ended to a differential architecture lies in the design of an appropriate impedance transformation network. In this work, the network is composed of a 1:2 power splitter followed by two baluns. The output impedance of the LNA is 50 Ω in a single-ended configuration, whereas the input impedance of each mixer is 200 Ω differential.

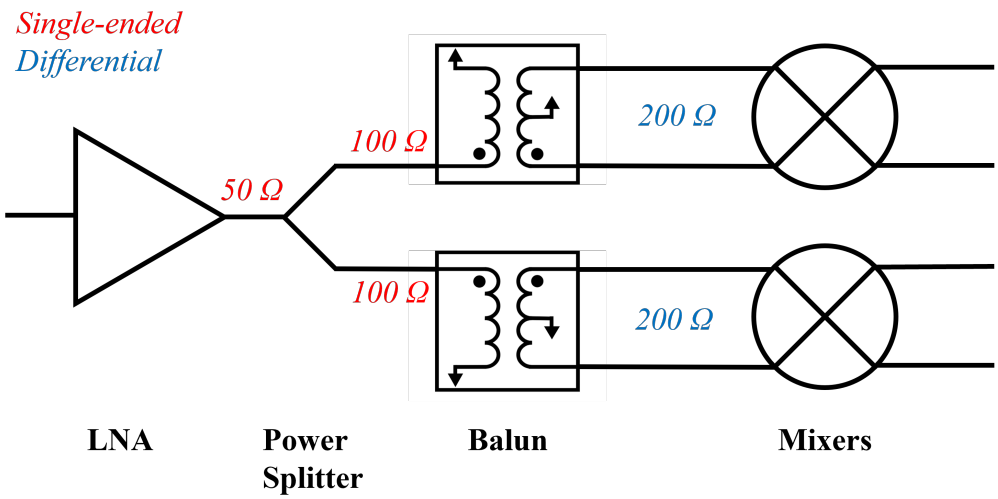


Figure 5.2: Passive impedance transformation network enabling single-ended to differential conversion.

The impedance transformation is detailed in Fig. 5.2. The balanced power splitter converts the 50 Ω single-ended impedance into two 100 Ω single-ended branches. This operation inherently introduces an insertion loss of approximately 4.2 dB within the frequency band of interest around 60 GHz.

Subsequently, each balun performs the conversion from 100 Ω single-ended to 200 Ω differential, corresponding to a 1:1 impedance transformation ratio. This ratio significantly simplifies the balun design and ensures low insertion loss, measured to be below 1 dB across the entire operating bandwidth (see Fig. 5.3).

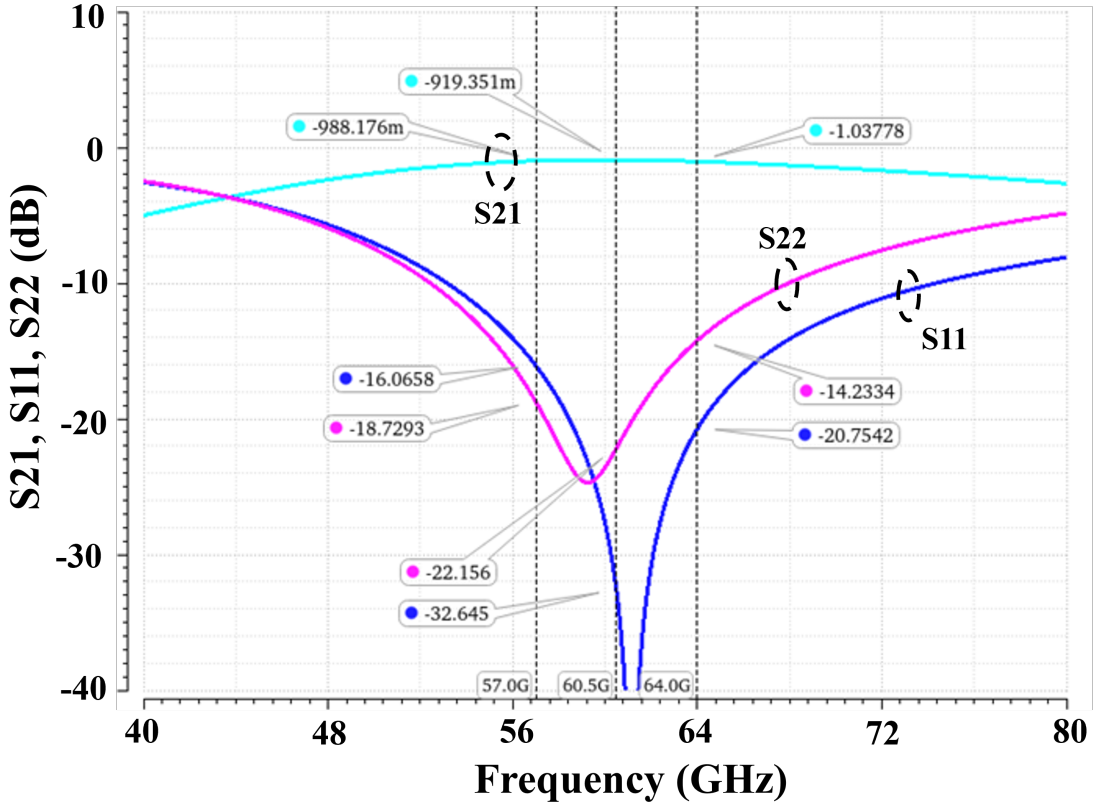


Figure 5.3: Simulated S-parameters performances of the designed 1:1 balun.

5.2.3 Active stages design and performances

Active Mixer

As mentioned earlier, the demodulation chain consists of a mixer followed by a baseband amplifier (BBA) in each I/Q branch. The initial specifications for each of these blocks are detailed in Chapter 3 (see Table 3.3). In that study, it was established that the use of passive mixers could be considered while still meeting the SNR and power constraints required to achieve a BER $< 10^{-12}$. However, the impedance matching network, as well as the losses it introduces, were underestimated, thereby rendering the evaluated scenarios invalid in their current form.

Since the designed LNA exhibits better-than-expected performance (higher gain, lower noise figure than initially estimated, and a DC power margin of 5 mW), it becomes feasible to transition to active mixer topologies. This approach improves the robustness of the demodulation chain by introducing additional gain; however, the associated noise figure must be carefully controlled to prevent it from becoming dominant when the LNA operates in low-gain mode.

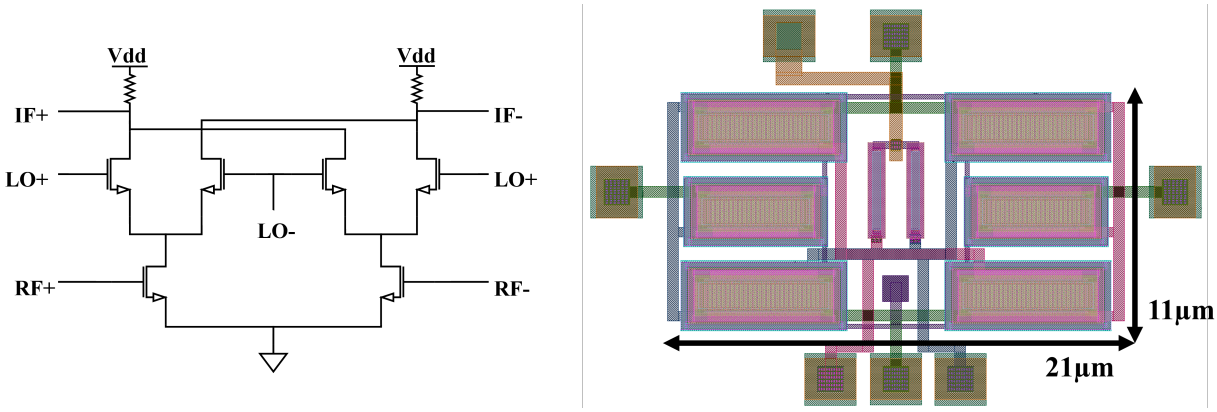


Figure 5.4: Schematic and layout of proposed Gilbert-cell downconversion mixer.

For the mixer topology, a Gilbert cell is selected (see. Fig. 5.4). This topology offers several advantages at 60 GHz, including intrinsic conversion gain, good port-to-port isolation (particularly LO-to-RF leakage), and suitability for differential implementations, which enhances common-mode noise rejection. Moreover, its switching quad enables relatively high linearity compared to simple active mixers. However, these benefits come at the cost of increased power consumption, higher design complexity, and sensitivity to device mismatches

and parasitics, which become critical at millimeter-wave frequencies. In addition, achieving proper LO drive and maintaining switching efficiency at 60 GHz can be challenging, potentially degrading performance if not carefully addressed.

Figure 5.5 and Table 5.1 present the post-layout simulated performance of the mixer.

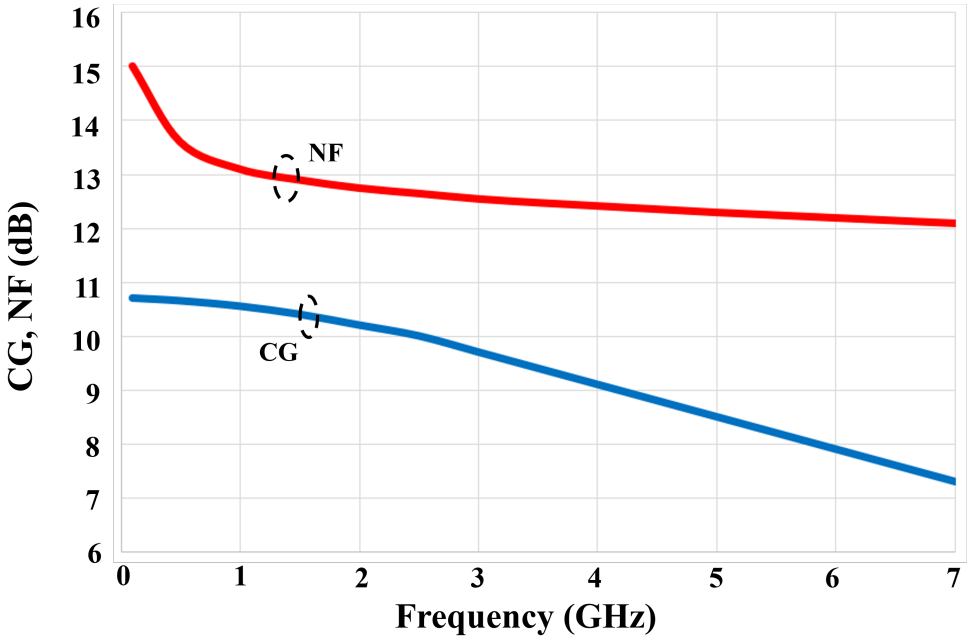


Figure 5.5: Conversion gain and NF of designed active mixer.

Table 5.1: Post-layout performance summary of the proposed mixer.

Parameter	**Value**
Conversion Gain (dB)	8.5 - 10.7 (in-band)
Noise Figure (dB)	12.3 - 15 (in-band)
ICP_{1dB} (dBm)	-4.3
DC Power Consumption (mW)	4.5
Core Area (μm^2)	233

Among the performance metrics of this design, the input compression point is particularly critical. As will be discussed in the following subsection, it constitutes a key aspect that required special attention during the design process.

Baseband Amplifier

Regarding the design of the baseband amplifier, the topology and layout methodologies cannot be disclosed in this manuscript, as they are confidential and constitute the intellectual property of the company. Only the raw performance metrics, extracted from post-layout simulations (PLS), will therefore be presented.
It is nevertheless worth noting that the design of a baseband amplifier featuring a bandwidth exceeding 5.5 GHz, while maintaining substantial gain and a moderate-to-low noise figure, represents a significant challenge, as highlighted in [32].

Table 5.2: Post-layout performance summary of the proposed baseband amplifier.

Parameter	**Value**
Gain (dB)	13.1 - 14.5 (in-band)
Noise Figure (dB)	1.3 - 8.5 (in-band)
ICP_{1dB} (dBm)	-5.1
DC Power Consumption (mW)	14.5
Core Area (μm^2)	Confidential

5.2.4 Layout of the complete Rx Front-End

Now that all the blocks have been designed, a co-integration can be considered in order to estimate the overall silicon area occupied by these circuits. Figure 5.6 provides a visual representation of the complete layout, including the reconfigurable LNA and the digital control circuit for the variable resistors, the impedance transformation network comprising the splitter and 1:1 baluns, the active mixers, as well as the baseband amplifiers.

Overall, the front-end (excluding the LO generation and a possible PLL) occupies an area of approximately 375μm $\times$ 375μm, corresponding to about 0.14 mm^2.

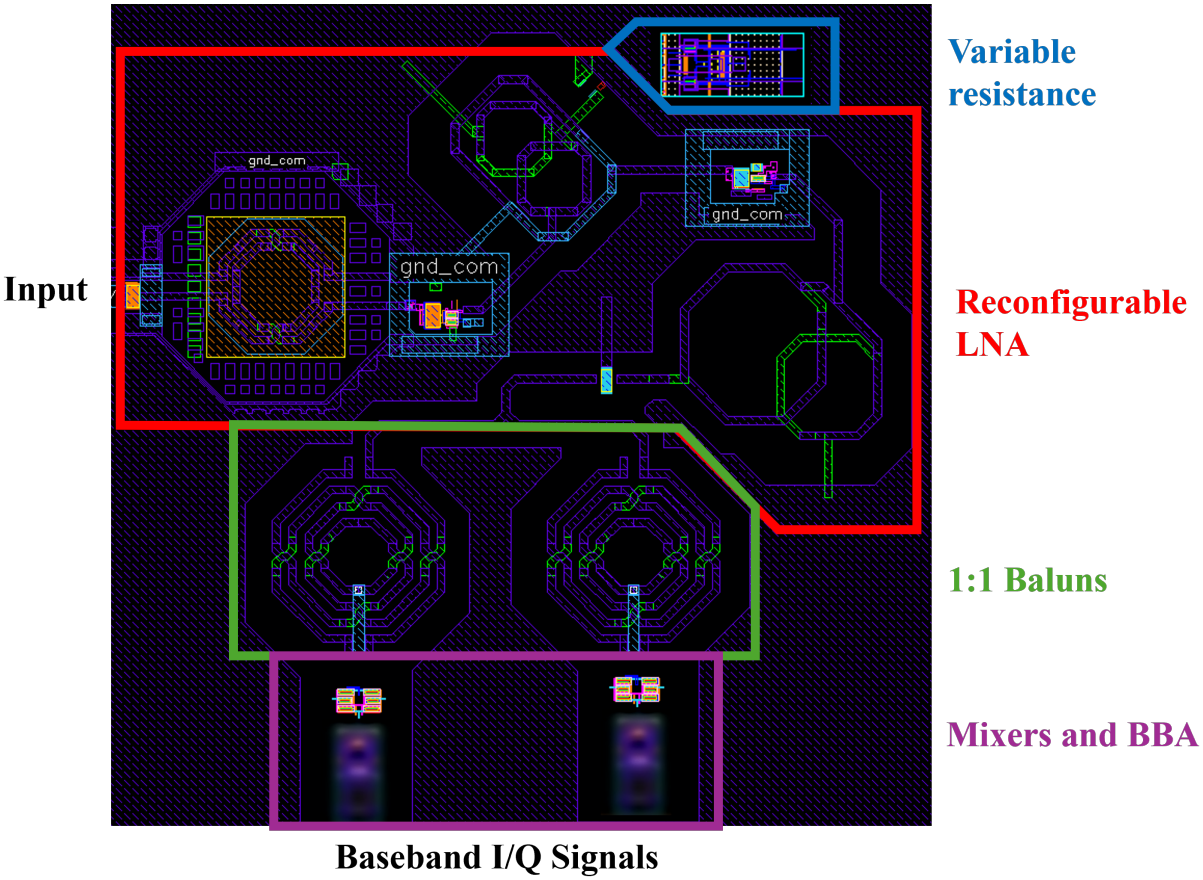


Figure 5.6: Layout view of the complete Rx front-end including the reconfigurable LNA, impedance matching networks, mixers and baseband amplifiers.

Now that the individual performance of the building blocks composing the receiver chain has been detailed, the focus is shifted to the high-level system performance and its impact on the transmission of a USB 3.2 signal.

5.3 Cascade Analysis and Link Budget

5.3.1 Methodology

The system-level performance is evaluated using a hierarchical analytical approach based on block-level characterizations. Due to the absence of full end-to-end transistor-level co-simulation capability, the following methodology is adopted:

- measured or simulated S-parameters and noise figures of each block,
- Friis cascade equations for gain and noise figure propagation,
- polynomial-based modeling of nonlinearities using ICP1/IIP3 parameters,
- spreadsheet-based link budget computation and BER estimation for QPSK modulation.

This approach enables a consistent evaluation of system-level performance while maintaining full traceability of assumptions. The following provides a breakdown of the performance of the different building blocks for a cascaded performance analysis.

Table 5.3: Cascaded performance breakdown of the receiver front-end blocks

Parameters	**LNA**		**Impedance Matching**	**Mixer**	**BBA**
	Low Gain	**High Gain**			
Gain (dB)	10.2	19.9	-5.1	9.5	13.8
NF (dB)	6.2	5.3	5.1	13.5	3
ICP_{1dB} (dBm)	-14.1	-22.3	/	-8.3	-7.1
DC Power (mW)	14.48	14.48	/	4.5	14.5

5.3.2 Cascaded performances

The overall gain of the receiver front-end is obtained by cascading the individual stage gains. In linear scale, the total gain is expressed as:

$$G_{\text{tot}} = G_{\text{LNA}} \cdot G_{\text{match}} \cdot G_{\text{mix}} \cdot G_{\text{BBA}}. \tag{5.1}$$

In logarithmic scale, this becomes a simple sum of contributions:

$$G_{\text{tot,dB}} = G_{\text{LNA,dB}} + G_{\text{match,dB}} + G_{\text{mix,dB}} + G_{\text{BBA,dB}}. \tag{5.2}$$

Using the values reported in Table 5.3, the total gain of the receiver chain can be evaluated for both LNA operating modes.

High-gain mode

$$G_{\text{tot,HG}} = 19.9 - 5.1 + 9.5 + 13.8 = 38.1 \text{ dB}. \tag{5.3}$$

Low-gain mode

$$G_{\text{tot,LG}} = 10.2 - 5.1 + 9.5 + 13.8 = 28.4 \text{ dB}. \tag{5.4}$$

The cascaded noise figure is derived using the Friis equation. In linear scale, it is expressed as:

$$F_{\text{tot}} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3}, \tag{5.5}$$

where F_i and G_i denote respectively the noise factors and gains of each stage.

The impedance matching network is modeled as a passive lossy stage, such that:

$$F_{\text{match}} = L_{\text{match}}, \qquad G_{\text{match}} = \frac{1}{L_{\text{match}}}. \tag{5.6}$$

In high-gain mode, the large gain of the LNA strongly suppresses the contribution of subsequent stages in the Friis expansion. The overall noise figure is therefore dominated by the first stage:

$$F_{\text{tot,HG}} = 4.1226 \tag{5.7}$$

$$NF_{\text{tot,HG}} = 10 \log_{10}(4.1226) = 6.15 \text{ dB}. \tag{5.8}$$

In low-gain mode, the reduced LNA gain increases the relative contribution of the following stages, in particular the mixer and baseband amplifier:

$$F_{\text{tot,LG}} = F_{\text{LNA}} + \frac{F_{\text{match}} - 1}{G_{\text{LNA}}} + \frac{F_{\text{mix}} - 1}{G_{\text{LNA}} G_{\text{match}}} + \frac{F_{\text{BBA}} - 1}{G_{\text{LNA}} G_{\text{match}} G_{\text{mix}}}. \tag{5.9}$$

This results in a higher cascaded noise figure:

$$F_{\text{tot,LG}} = 11.027 \tag{5.10}$$

$$NF_{\text{tot,LG}} = 10 \log_{10}(11.027) = 10.42 \text{ dB}. \tag{5.11}$$

The noise figure (NF) curves across the entire frequency band are shown in the following figure.

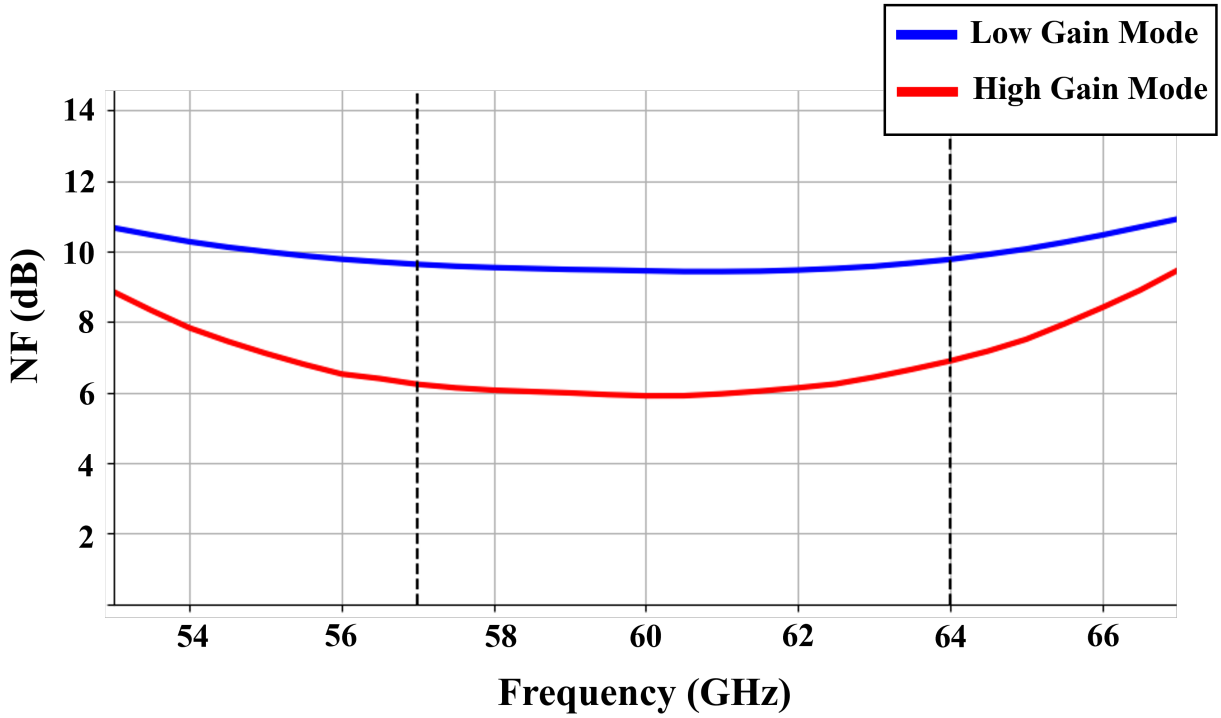


Figure 5.7: Cascaded Noise Figure over the entire bandwidth for the lowest and highest gain available in the LNA.

Regarding the circuit limitations induced by the linearity of the blocks, it is possible to represent a specific link budget with the compression points and the gains of each block.

5.3.3 Linearity and Dynamic Range

The linearity of the receive chain is limited by the baseband amplifier, as illustrated in Fig. 5.8. It is therefore possible to back-calculate the power budget to determine the maximum allowable input power in order to prevent any block from entering compression. In this scenario, the minimum LNA gain is considered, corresponding to a short-range communication.

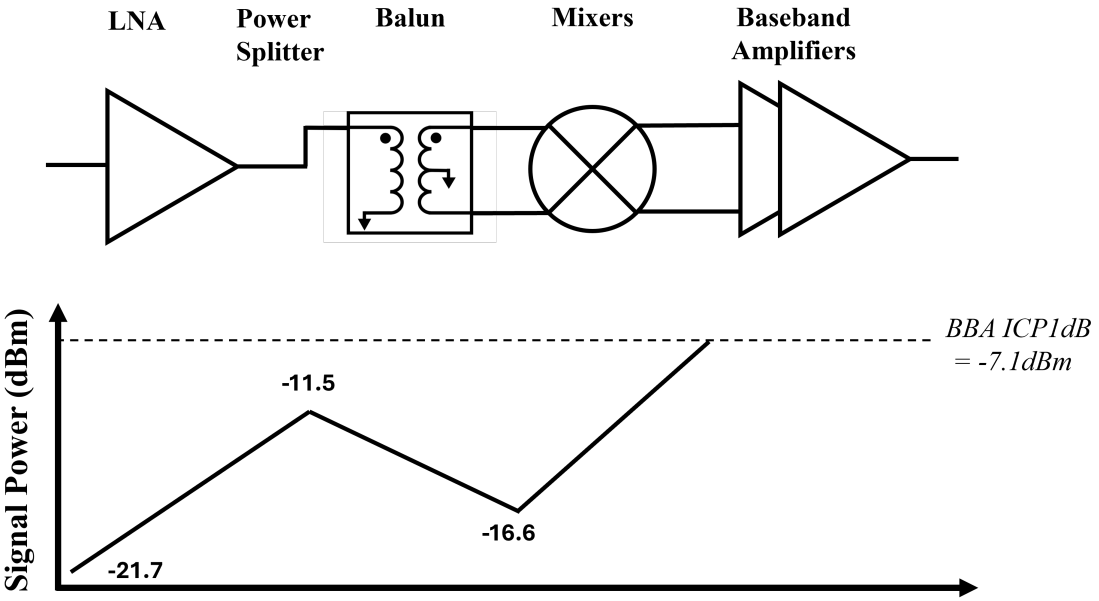


Figure 5.8: Representation of the maximum admissible input power before compression point.

Here, it can be inferred that the maximum allowable input power at the LNA is $-21.7\,\mathrm{dBm}$ before the BBA reaches compression. This is a favorable result for the system, as the specifications indicate a maximum input power of $-22\,\mathrm{dBm}$, corresponding to a communication distance of $5\,\mathrm{mm}$.

Regarding the minimum allowable input power required to correctly demodulate the signal, it can also be estimated from the input power required at the ADC to demodulate a QPSK signal. A visual representation is displayed in Figure 5.9.

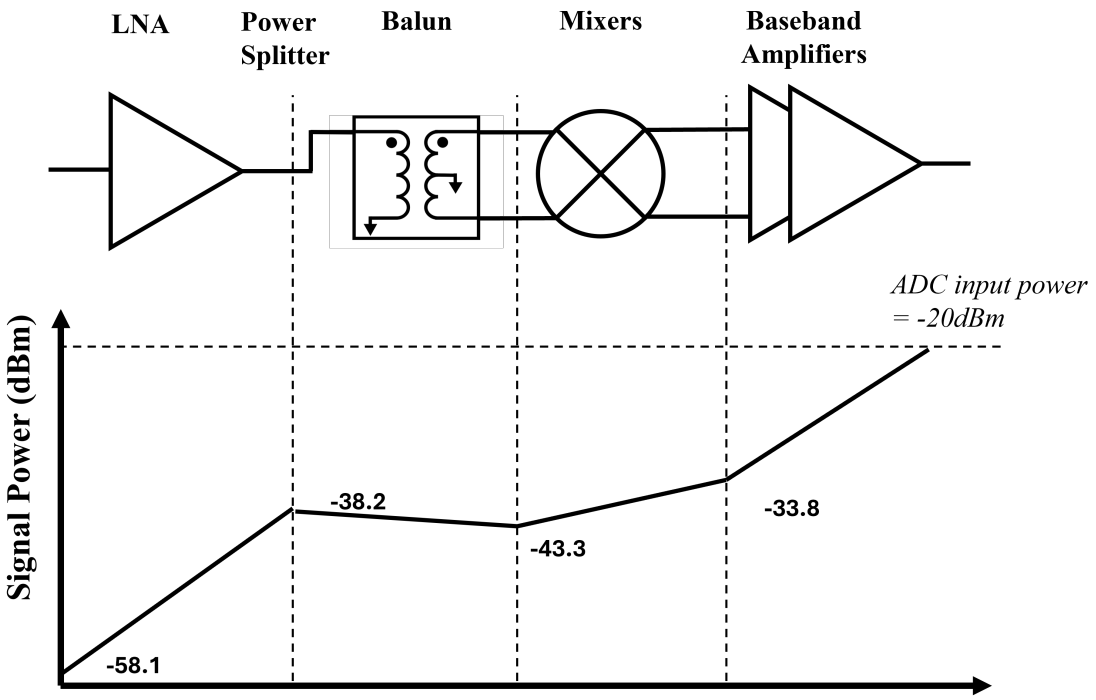


Figure 5.9: Representation of the minimal admissible input power to ensure proper operation of ADCs.

This input power exceeds the initial system estimates and requirements, since an input power of $-58.1\,\mathrm{dBm}$ corresponds to a communication distance of approximately 32 cm. This is significantly greater than the maximum envisaged distance of 5 cm and the $-42\,\mathrm{dBm}$ level at the receiver input. This is a favorable result for the circuit, and the sizing of the digital functions will benefit from relaxed design constraints.

However, two considerations must be added here. The use case does not foresee communication at such long distances, and the minimum SNR will not be sufficient to ensure error-free QPSK demodulation. Using the SNR formula, it can be observed that the SNR obtained at P_{sens} is too low to ensure a BER $< 10^{-12}$, as specified in Chapter 2. However, by adhering to the use-case specifications, it is still possible to estimate the SNR and thus the BER for both the minimum and maximum distances using the complete system.

$$SNR_{\mathrm{min}} = P_{\mathrm{sens}} + 174 - 10\log_{10}(B) - NF \tag{5.12}$$

$$SNR_{\mathrm{min}} = -58.1 + 174 - 10\log_{10}(7 \times 10^{9}) - 6.15 \approx \boxed{11.3\,\mathrm{dB}} \tag{5.13}$$

At the maximum (5 cm, −42 dBm, high-gain mode) and minimum (5 mm, −22 dBm, low-gain mode) distances, it is also possible to estimate the SNR at the BBA output as follows:

$$SNR_{long} = -42 + 174 - 10\log_{10}(7 \times 10^9) - 6.15 \approx \boxed{27.4\,\text{dB}} \tag{5.14}$$

$$SNR_{short} = -22 + 174 - 10\log_{10}(7 \times 10^9) - 10.42 \approx \boxed{43.13\,\text{dB}} \tag{5.15}$$

These SNR margins are very comfortable, allowing for the possibility of perfect demodulation and a BER $< 10^{-12}$.

5.3.4 BER and EVM Performance

As previously indicated, it was not possible to perform full-chain simulations under advanced conditions. Therefore, the BER and EVM estimations remain limited to theoretical models. Nevertheless, it is still possible to provide insights to assess the circuit performance.

The SNR levels obtained over the communication distance range are highly satisfactory and well above the theoretical requirement for error-free demodulation of a QPSK signal ($\text{SNR}_{\text{QPSK}} = 13\,\text{dB}$). It could thus be argued that this receiver would enable error-free demodulation. However, it should be noted that this system does not include frequency generation using a LO or a VCO, and the phase noise of this block is one of the main sources of noise and error in a transceiver. In addition, I/Q demodulation is highly sensitive to path mismatches, which have not been simulated for this receiver. Nevertheless, given the significant SNR margin, it remains reasonable to assume that this system likely achieves the error-free demodulation threshold for a 10 Gb/s QPSK signal.

5.3.5 System Latency analysis

The latency breakdown of the receiver chain is summarized in Table 5.4. The overall latency amounts to 194 ps, which is consistent with the expected order of magnitude for a wideband millimeter-wave front-end followed by a baseband amplification stage. It can be observed that the dominant contribution arises from the baseband amplifier, accounting for 89 ps, i.e., nearly half of the total delay. This behavior is anticipated due to the limited transconductance-to-capacitance ratio in low-power wideband designs, which inherently increases the propagation delay. The low-noise amplifier also exhibits a relatively significant

latency of 56 ps, this can be attributed to its two-stage cascode topology combined with transformer-based input, interstage, and output matching networks, which introduce additional phase shift and energy storage, thereby increasing the effective group delay. In contrast, the passive splitter and balun introduce only minor delays (9 ps and 19 ps, respectively), confirming their efficient implementation. Similarly, the mixer contributes a moderate latency of 21 ps, which is in line with typical values for Gilbert-cell-based topologies at millimeter-wave frequencies. Overall, this analysis highlights that the latency is predominantly governed by the gain stages, while passive and switching blocks have a comparatively limited impact. This latency is well below the system specification defined in Chapter 2, which requires a latency prior to digital processing below 3 ns.

Block	LNA	Splitter	Balun	Mixer	BBA	**Total**
Latency (ps)	56	9	19	21	89	**194**

Table 5.4: Latency Breakdown of the Receiver Chain

5.3.6 Limitations and Discussion

While the proposed receiver architecture demonstrates compliance with USB 3.2 specifications under idealized simulation conditions, several practical limitations must be acknowledged to provide a realistic assessment of its performance in a deployed system.

Impact of Local Oscillator Phase Noise: The system-level analysis presented in this chapter assumes an ideal Local Oscillator (LO) with negligible phase noise. In a practical implementation, the phase noise of the frequency synthesizer will introduce random phase rotations on the QPSK constellation, degrading the Error Vector Magnitude (EVM) and potentially increasing the Bit Error Rate (BER). However, the significant SNR margins calculated in Section 5.3.3 (27.4 dB at 5 cm and 43.1 dB at 5 mm) suggest that the receiver possesses sufficient robustness to tolerate realistic phase noise levels (e.g., -130 dBc/Hz at 100 kHz offset) without violating the BER $\leq 10^{-12}$ requirement. Nevertheless, a co-simulation including a realistic PLL model would be necessary to quantify this margin precisely.

I/Q Imbalance and Calibration: The dual-path I/Q downconversion architecture is inherently sensitive to gain and phase mismatches between the in-phase and quadrature branches. Manufacturing variations (Process, Voltage, Temperature - PVT) can lead to imbalances that distort the constellation and create image interference. While the passive splitter and balun network are designed for symmetry, active mismatches in the mixers and baseband amplifiers are unavoidable. Without digital calibration or analog trimming circuits, these imperfections could limit the achievable BER. Future iterations of this design should integrate a calibration routine to correct I/Q imbalance, leveraging the high SNR margin to ensure error-free operation.

Simulation-to-Silicon Discrepancies: The performance validation relies on hierarchical modeling and post-layout simulations. While these methods accurately capture parasitic effects and circuit-level non-idealities, they may not fully account for second-order effects such as substrate coupling, package parasitics, or measurement setup uncertainties. As noted in Chapter 4, initial on-wafer measurements of the standalone LNA showed deviations from simulations, highlighting the challenges of modeling mmWave circuits at 60 GHz. Consequently, the system-level figures presented here should be viewed as optimistic upper-bound estimates. A comprehensive experimental validation of the complete front-end chain is required to confirm the predicted BER and latency in a real-world environment.

Despite these limitations, the proposed architecture establishes a solid foundation for wireless USB 3.2 interfaces. The modular design and the use of a reconfigurable LNA provide the necessary flexibility to adapt to varying channel conditions and to integrate calibration mechanisms in future silicon prototypes.

5.4 Conclusion

Table 5.5: Summary of receiver performance against initial specifications (Chap. 2) and architectural scenarios (Chap. 3).

Parameter	**Specs. (Chap. 2)**	**Archi. Study (Chap. 3)**	**System (Chap. 5)**	**Status**
Data Rate	$\geq$ 10 Gb/s	QPSK, 10 Gb/s	QPSK, 10 Gb/s	**Met**
Bit Error Rate	$\leq 10^{-12}$	SNR $\geq$ 17 dB	$< 10^{-12}$ (*)	**Met**
Latency	$<$ 3 ns	/	194 ps	**Met**
Communication Range	5 mm – 5 cm	5 mm – 5 cm	5 mm – 17 cm	**Met**
Power Consumption (Rx)	$\leq$ 500 mW (total)	60 – 65 mW	52.5 mW ($^{\triangle}$)	**Met**
Total Gain	/	23.5 dB	28.4 – 38.1 dB	**Met**
Noise Figure (NF)	$\leq$ 13 dB	9.7 dB	6.15 – 10.42 dB	**Met**
Technology	Advanced CMOS	22 nm FDSOI	22 nm FDSOI	**Met**
Front-end Area	Minimized	/	$\sim$ 0.14 mm^2	**Met**

* Theoretical estimation based on calculated SNR margins ($\geq$ 27 dB), assuming negligible LO phase noise and no digital calibration.
$^{\triangle}$ This power consumption does not include frequency synthesis.

This chapter presented the system-level integration and validation of a 60 GHz CMOS receiver front-end designed for short-range wireless communication compliant with the USB 3.2 standard. Building upon the architectural choices established in Chapter 3 and the specifications defined in Chapter 2, a complete receiver chain was assembled, comprising a reconfigurable low-noise amplifier, a passive impedance transformation network, active Gilbert-cell mixers, and wideband baseband amplifiers.

The hierarchical validation methodology, combining block-level characterization with analytical cascade modeling, demonstrated that the proposed architecture meets all critical system requirements. As summarized in Table 5.5, the receiver achieves a total gain of 28.4–38.1 dB, a noise figure of 6.15–10.42 dB, and a latency of 194 ps, all well within the USB 3.2 specifications. The calculated SNR margins (27.4 dB at 5 cm and 43.1 dB at 5 mm) confirm that the link budget is sufficient to support error-free QPSK demodulation with a BER below 10^{-12} over the targeted communication range.

The integration of the reconfigurable LNA, developed in Chapter 4, proved essential for covering the wide input dynamic range associated with short-range millimeter-wave links. The continuous gain control mechanism, based on a variable resistive element in the transformer-assisted interstage network, enables smooth gain adaptation over a 9.5 dB range without degrading noise performance or linearity. This validates the architectural scenario selected in Chapter 3 and demonstrates the effectiveness of the proposed passive gain reconfiguration technique. Furthermore, the passive impedance transformation network successfully converts the single-ended LNA output to a differential mixer input with minimal insertion loss (5.1 dB), demonstrating the effectiveness of the proposed integration strategy.

While the analysis relies on simulation-based validation rather than full system measurements, the significant performance margins provide confidence in the robustness of the design. The limitations discussed in Section 6.3, including LO phase noise and I/Q imbalance, represent practical challenges that can be addressed through calibration routines in future silicon prototypes without requiring fundamental architectural changes.

Overall, this chapter establishes the feasibility of a wireless USB 3.2 interface at 60 GHz using a compact, energy-efficient CMOS receiver. The successful system-level integration validates the design methodology employed throughout this thesis and provides a solid foundation for the conclusions and perspectives presented in the next chapter.

Chapter 6

Conclusion and Perspectives

6.1 Introduction

This thesis has investigated the design, implementation, and experimental validation of a 60 GHz CMOS receiver front-end for short-range wireless communication targeting USB 3.2-class data rates. The primary objective was to assess the feasibility of replacing high-speed wired links with fully integrated millimeter-wave wireless interfaces capable of sustaining 10 Gb/s with stringent reliability and latency constraints.

Beyond the sole demonstration of circuit functionality, this work aimed at establishing a consistent design methodology bridging system-level specifications and silicon-level implementation. By combining link-budget-driven architectural exploration with circuit-level innovation and experimental validation, this thesis provides a comprehensive framework for the development of high-throughput short-range mmWave links.

The main contribution of this work lies in demonstrating that such systems can be efficiently realized in advanced CMOS technology, provided that architectural flexibility and passive integration challenges are properly addressed. In particular, the introduction of low-coupled stacked inductors and a reconfigurable LNA architecture enables compact, adaptable, and high-performance receiver front-ends compatible with the constraints of dense integrated systems.

Overall, the results presented in this manuscript support the viability of short-range wireless interconnects as a complementary solution to conventional wired interfaces, opening the way toward more flexible and scalable high-speed communication architectures.

Compared to existing mmWave receiver implementations, this work emphasizes architectural flexibility and passive integration efficiency rather than solely maximizing gain or minimizing noise figure. This positioning enables a more robust adaptation to the large dynamic range inherent to short-range wireless links, while maintaining a compact silicon footprint compatible with dense integration constraints.

6.2 Summary of Main Contributions

The research conducted in this thesis is organized around three principal contributions, each addressing a critical aspect of the receiver design challenge.

6.2.1 System-Level Architecture Exploration (Chapters 2–3)

The first contribution establishes a rigorous system-level framework for evaluating wireless USB 3.2 interfaces at 60 GHz. Through a three-step design flow combining C++ brute-force exploration, MATLAB link-budget validation, and Simulink behavioral modeling, we identified the architectural constraints governing feasibility. Key outcomes include:

- **Modulation Selection:** Demonstration that Quadrature Phase Shift Keying (QPSK) provides the optimal trade-off between spectral efficiency and robustness to amplitude perturbations for mmWave short-range links.
- **Dynamic Range Requirement:** Quantification of the input power variation across the targeted communication range (5 mm to 5 cm), revealing that a fixed-gain front-end cannot simultaneously satisfy sensitivity and linearity constraints.
- **Architectural Recommendation:** Identification of a reconfigurable receiver architecture as a mandatory solution, with a gain tuning range of approximately 10 dB required to cover the full dynamic range without degrading noise figure or compression performance.

6.2.2 Innovative Passive Design and Reconfigurable LNA (Chapter 4)

The second contribution introduces a novel methodology for the design of low-coupled stacked inductances and applies this technique to the development of a reconfigurable low-noise amplifier (LNA). This work represents the core circuit-level innovation of the thesis:

- **Stacked Inductor Technique:** Development of a vertical superposition method with controlled overlap ratio ($\rho \approx 0.3$) that cancels magnetic coupling between adjacent windings. This technique enables a reduction of the passive footprint by 40–55% while preserving inductance values and quality factors, addressing a critical area constraint in mmWave integrated circuits.

- **Reconfigurable LNA Architecture:** Design of a two-stage cascode LNA with active lineup switching, enabling operation in either single-stage mode (high linearity, low power) or dual-stage mode (high gain, high sensitivity). The design achieves a gain reconfiguration range of approximately 9.5 dB with minimal degradation in noise figure and linearity.

- **Continuous Gain Control Concept:** Proposal of a variable resistive load mechanism for smooth gain tuning without modifying bias conditions. Although not implemented in the first tape-out, this concept provides a pathway for future iterations with enhanced flexibility.

- **Silicon Validation:** Fabrication and on-wafer characterization of the LNA in GlobalFoundries 22 nm FDSOI technology, demonstrating compliance with target specifications in both operating modes despite non-ideal measurement conditions.

6.2.3 System Integration and Experimental Validation (Chapter 5)

The third contribution validates the complete receiver front-end through hierarchical cascade modeling and experimental correlation:

- **Front-End Integration:** Successful co-integration of the reconfigurable LNA with passive impedance transformation networks, active Gilbert-cell mixers, and wideband baseband amplifiers, occupying a total silicon area of approximately 0.14 mm^2.

- **Link-Budget Compliance:** Demonstration that the cascaded receiver achieves a total gain of 28.4–38.1 dB, a noise figure of 6.15–10.42 dB, and a latency of 194 ps, all well within the USB 3.2 specifications.

- **SNR Margins:** Calculation of signal-to-noise ratio margins of 27.4 dB at 5 cm and 43.1 dB at 5 mm, confirming that the link budget is sufficient to support error-free QPSK demodulation with BER $< 10^{-12}$ over the targeted communication range.

- **Measurement Integrity:** Transparent analysis of the 4.4 dB systematic gain discrepancy between simulation (Momentum-extracted) and measurement, attributing the deviation to substrate loss modeling limitations and measurement setup parasitics rather than active device failure. The preservation of output compression points ($OCP_{1\text{dB}}$) confirms the robustness of the amplification core.

6.3 Summary Against Initial Specifications

Table 6.1 summarizes the receiver performance against the initial system requirements defined in Chapter 2 and the architectural scenarios explored in Chapter 3. All critical specifications have been met or exceeded, validating the design methodology and the feasibility of the proposed wireless USB 3.2 interface.

Table 6.1: Summary of Receiver Performance Against Initial Specifications

Parameter	**Specs. (Chap. 2)**	**Archi. Study (Chap. 3)**	**System (Chap. 5)**	**Status**
Data Rate	$\geq$ 10 Gb/s	QPSK, 10 Gb/s	QPSK, 10 Gb/s	**Met**
Bit Error Rate	$\leq 10^{-12}$	SNR $\geq$ 17 dB	$< 10^{-12}$ (*)	**Met**
Latency	$<$ 3 ns	/	194 ps	**Met**
Com. Range	5 mm – 5 cm	5 mm – 5 cm	5 mm – 5 cm	**Met**
DC Power (Rx)	$\leq$ 500 mW (total)	60 – 65 mW	52.5 mW ($^{\triangle}$)	**Met**
Total Gain	/	23.5 dB	28.4 – 38.1 dB	**Met**
Noise Figure (NF)	$\leq$ 13 dB	9.7 dB	6.15 – 10.42 dB	**Met**
Technology	Advanced CMOS	22 nm FDSOI	22 nm FDSOI	**Met**
Front-end Area	Minimized	/	$\sim$ 0.14 mm^2	**Met**

* Theoretical estimate based on calculated SNR margins ($\geq$ 27 dB), assuming negligible LO phase noise and no digital calibration.
$^{\triangle}$ This power consumption does not include frequency synthesis.

Despite these promising results, several limitations must be acknowledged. First, the absence of integrated LO generation prevents a fully autonomous system evaluation. In addition, the BER performance is derived from analytical estimations rather than measured end-to-end communication. Finally, the continuous gain control mechanism, although conceptually validated, remains to be implemented in silicon.

6.4 List of Contributions

International conference

M. Vidal, O. Tesson, P. Guillot, J. -B. Begueret and T. Taris, "Design Flow of 60 GHz Multi-Gb/s Transceivers for Wireless USB 3.2 Communications," 2024 22nd IEEE Interregional NEWCAS Conference (**NEWCAS**), Sherbrooke, QC, Canada, 2024, pp. 30-34, doi: 10.1109/NewCAS58973.2024.10666112.

National conference

Martin Vidal, Olivier Tesson, Jean-Baptiste Begueret, Thierry Taris, "Amplificateur faible bruit à double mode de gain intégrant des structures passives innovantes" Journées Nationales du Micro-ondes (**JNM**), Lille, France, 2026.

Martin Vidal, Olivier Tesson, Jean-Baptiste Begueret, Thierry Taris, "Structures inductives passives compactes à couplages réduits" Journées Nationales du Micro-ondes (**JNM**), Lille, France, 2026.

Intellectual property

Olivier Tesson, Martin Vidal, Thierry Taris, Jean-Baptiste Begueret. "Set of EMI compliant inductive elements for reconfigurable amplifier and method for producing the same", ID: 82432693, **Invention Disclosure**, June 10th 2025

Martin Vidal, Olivier Tesson, Thierry Taris, Jean-Baptiste Begueret, Cristian Moreira, "Compact Passive Gain-Control Matching Network for Millimeter-Wave Amplifiers" **Patent application under review**, 2026.

6.5 Perspectives and Future Work

While the results presented in this thesis demonstrate the feasibility and relevance of a reconfigurable 60 GHz CMOS receiver front-end for short-range high-speed communication, several directions can be explored to further extend and strengthen this work.

6.5.1 Short-Term Perspectives: Design Refinement and Robustness

In the short term, immediate improvements can be achieved by refining the existing design methodology and addressing identified limitations. A key priority is the systematic use of electromagnetic extraction (e.g., Momentum) for all passive structures, enabling more accurate modeling of substrate losses and reducing the discrepancy observed between simulation and measurement.
Additionally, the integration of patterned ground shields (PGS) beneath critical inductive components could improve robustness against process variations and substrate coupling, further stabilizing circuit performance across fabrication corners.

Another important extension concerns the implementation of the proposed continuous gain control mechanism. The integration of a digitally controlled variable resistive load would allow fine and adaptive gain tuning, fully leveraging the reconfigurable LNA architecture and enabling dynamic optimization of the receiver depending on channel conditions.

6.5.2 Mid-Term Perspectives: Full Receiver Integration and System-Level Validation

At the system level, a natural evolution of this work is the integration of the complete receiver chain within a single chip, including the local oscillator generation. The design and integration of a VCO and potentially a phase-locked loop (PLL) would enable a fully autonomous receiver, allowing comprehensive evaluation of system-level metrics such as SNR, BER, and error vector magnitude (EVM) under realistic operating conditions.

Such integration would also provide deeper insights into the interactions between RF, LO phase noise, and baseband processing, which are critical for high-order modulation schemes and robust communication.

Beyond the receiver, extending the approach to the transmitter side represents a logical continuation. In particular, the passive design techniques introduced in this thesis could be leveraged to develop compact and efficient power amplifiers, potentially enabling reconfigurable or efficiency-optimized transmission architectures.

6.5.3 Long-Term Perspectives: Scaling Data Rates and Exploring New Modulation Schemes

In the longer term, this work opens perspectives toward next-generation short-range wireless interfaces targeting data rates beyond 10 Gb/s. One promising direction is the exploration of higher frequency bands, such as 110–120 GHz, where larger available bandwidth could support significantly increased throughput.

In parallel, the investigation of alternative modulation schemes represents an important research avenue. While QPSK offers a robust trade-off for current constraints, higher spectral efficiency techniques such as PAM4 could be considered. Although challenging in wireless environments due to reduced noise margins, such approaches may become viable in very short-range scenarios with limited interference and controlled channel conditions.

More broadly, these developments contribute to the emerging vision of wireless interconnects as a complement, or even an alternative, to traditional wired solutions in high-speed data transfer systems, particularly in contexts where flexibility, integration density, and scalability are critical.

Appendix A

Extended equations

Input Impedance Calculation (Corrected Coupled-Inductor Model)

We consider the inductive network composed of L_1, L_2, and L_3, with mutual couplings:

$$M_{13} = k_{13}\sqrt{L_1 L_3}, \qquad M_{23} = k_{23}\sqrt{L_2 L_3}, \tag{A.1}$$

and no direct coupling between L_1 and L_2.

Let $s = j\omega$. The impedance matrix of the coupled inductors is:

$$\mathbf{Z}_L = \begin{bmatrix} sL_1 & 0 & sM_{13} \\ 0 & sL_2 & sM_{23} \\ sM_{13} & sM_{23} & sL_3 \end{bmatrix}. \tag{A.2}$$

Load at port 3 (node B).

$$Z_3(\omega) = (sL_3) \parallel \left(\frac{1}{sC_2} + Z_b\right). \tag{A.3}$$

Define

$$Z_{33}^{\text{tot}} = sL_3 + Z_3^{\text{load}}, \qquad Z_3^{\text{load}} = \left(\frac{1}{sC_2} + Z_b\right). \tag{A.4}$$

Reduction of the 3-port network. Eliminating port 3 yields the equivalent 2-port:

$$\mathbf{Z}_{12}^{\text{eq}} = \begin{bmatrix} sL_1 & 0 \\ 0 & sL_2 \end{bmatrix} - \frac{1}{Z_{33}^{\text{tot}}} \begin{bmatrix} sM_{13} \\ sM_{23} \end{bmatrix} \begin{bmatrix} sM_{13} & sM_{23} \end{bmatrix}. \tag{A.5}$$

Explicit expressions.

$$Z_{11}^{\text{eq}} = sL_1 - \frac{(sM_{13})^2}{Z_{33}^{\text{tot}}}, \tag{A.6}$$

$$Z_{22}^{\text{eq}} = sL_2 - \frac{(sM_{23})^2}{Z_{33}^{\text{tot}}}, \tag{A.7}$$

$$Z_{12}^{\text{eq}} = Z_{21}^{\text{eq}} = -\frac{(sM_{13})(sM_{23})}{Z_{33}^{\text{tot}}}. \tag{A.8}$$

Shunt branch at node A.

$$Z_{\text{shunt}} = R_{\text{var}} + \frac{1}{sC_1}. \tag{A.9}$$

Final input impedance.

$$\boxed{Z_{\text{in}}(\omega) = Z_{11}^{\text{eq}} + \frac{(Z_{12}^{\text{eq}})^2}{Z_{22}^{\text{eq}} + Z_{\text{shunt}}}} \tag{A.10}$$

Expanded form.

$$Z_{\text{in}}(\omega) = sL_1 - \frac{(sM_{13})^2}{Z_{33}^{\text{tot}}} + \frac{\left(\frac{(sM_{13})(sM_{23})}{Z_{33}^{\text{tot}}}\right)^2}{sL_2 - \frac{(sM_{23})^2}{Z_{33}^{\text{tot}}} + R_{\text{var}} + \frac{1}{sC_1}}. \tag{A.11}$$

Output Impedance Calculation (Corrected)

We now compute the impedance seen from node B.

Loads at ports 1 and 2. Port 1 (node A, cascode side):

$$Z_A(\omega) \tag{A.12}$$

Port 2:

$$Z_{\text{shunt}} = R_{\text{var}} + \frac{1}{sC_1}. \tag{A.13}$$

Output impedance at node B (before C_2).

$$Z_B(\omega) = sL_3 - \frac{(sM_{13})^2}{sL_1 + Z_A} - \frac{(sM_{23})^2}{sL_2 + Z_{\text{shunt}}}. \tag{A.14}$$

Final output impedance.

$$\boxed{Z_{\text{out}}(\omega) = \frac{1}{sC_2} + Z_B(\omega)} \tag{A.15}$$

Observations

- R_{var} controls both the loading of L_2 and the effective coupling between L_1 and L_2 through L_3.
- Decreasing R_{var} reduces Z_{shunt}, increases magnetic interaction, and increases reflected impedance terms.
- Increasing R_{var} decouples L_2, and the output impedance approaches $\frac{1}{sC_2} + sL_3$.

Impact of Interstage Gain Control on Voltage Gain

At first glance, one might expect that increasing the impedance connected to an amplifier node leads to a higher voltage gain, following the classical relation

$$A_v \approx -g_m Z_{\text{load}}. \tag{A.16}$$

However, this intuition only holds when the load impedance is directly connected to the drain and when the input excitation remains unchanged.

In the proposed topology, the variable resistor R_{var} does not directly control the drain load. Instead, it modifies the interstage network composed of magnetically coupled inductors L_1, L_2, and L_3. As a result, R_{var} simultaneously affects both the effective load seen by the transistor and the signal transfer through the coupled network.

Decomposition of the voltage gain. The overall voltage gain can be expressed as

$$A_{v,\text{tot}}(\omega) = A_{v,\text{in}}(\omega) \cdot A_{v1}(\omega) \cdot A_{v2}(\omega), \tag{A.17}$$

where:

- $A_{v,\text{in}}$ represents the voltage transfer through the coupled interstage network,
- $A_{v1} = -g_{m1} Z_{d1}$ is the intrinsic gain of the first stage,
- A_{v2} is the gain of the second stage.

Effect of R_{var} on the drain impedance. When R_{var} increases, the shunt impedance

$$Z_{\text{shunt}} = R_{\text{var}} + \frac{1}{sC_1} \tag{A.18}$$

also increases. This reduces the loading of inductor L_2, which can lead to a moderate increase in the effective drain impedance Z_{d1}. According to the classical gain expression, this effect tends to increase A_{v1}.

Effect of R_{var} on the magnetic coupling. More importantly, R_{var} strongly influences the current flowing in L_2. As R_{var} increases, the current in L_2 decreases, which reduces the magnetic flux coupled through L_3. This, in turn, weakens the induced voltage across the other coupled inductors, particularly at the input of the first stage.

Consequently, the voltage transfer factor $A_{v,\text{in}}$ is significantly reduced:

$$R_{\text{var}} \uparrow \Rightarrow\ I_{L_2} \downarrow \Rightarrow\ \text{magnetic coupling} \downarrow \Rightarrow\ A_{v,\text{in}} \downarrow . \tag{A.19}$$

Dominant effect on the overall gain. Although increasing R_{var} may slightly increase the drain impedance and thus A_{v1}, the reduction in magnetic coupling has a much stronger impact. As a result, the overall gain decreases:

$$R_{\text{var}} \uparrow \Rightarrow\ A_{v,\text{tot}} \downarrow . \tag{A.20}$$

Physical interpretation. The interstage network can be interpreted as a transformer-like structure, where L_3 acts as a primary inductance and L_1, L_2 behave as coupled secondary elements. In this analogy, R_{var} effectively controls the loading of the secondary winding.

A low value of R_{var} allows significant current to flow in L_2, enabling strong magnetic coupling and efficient signal transfer. Conversely, a high value of R_{var} suppresses the current, thereby weakening the coupling and reducing the signal delivered to the next stage.

Conclusion. This analysis highlights that the proposed gain control mechanism is not a conventional load tuning technique. Instead, it operates by modulating the magnetic coupling within the interstage network: R_{var} controls gain primarily through coupling strength rather than loa

Appendix B

Complete LNA layout

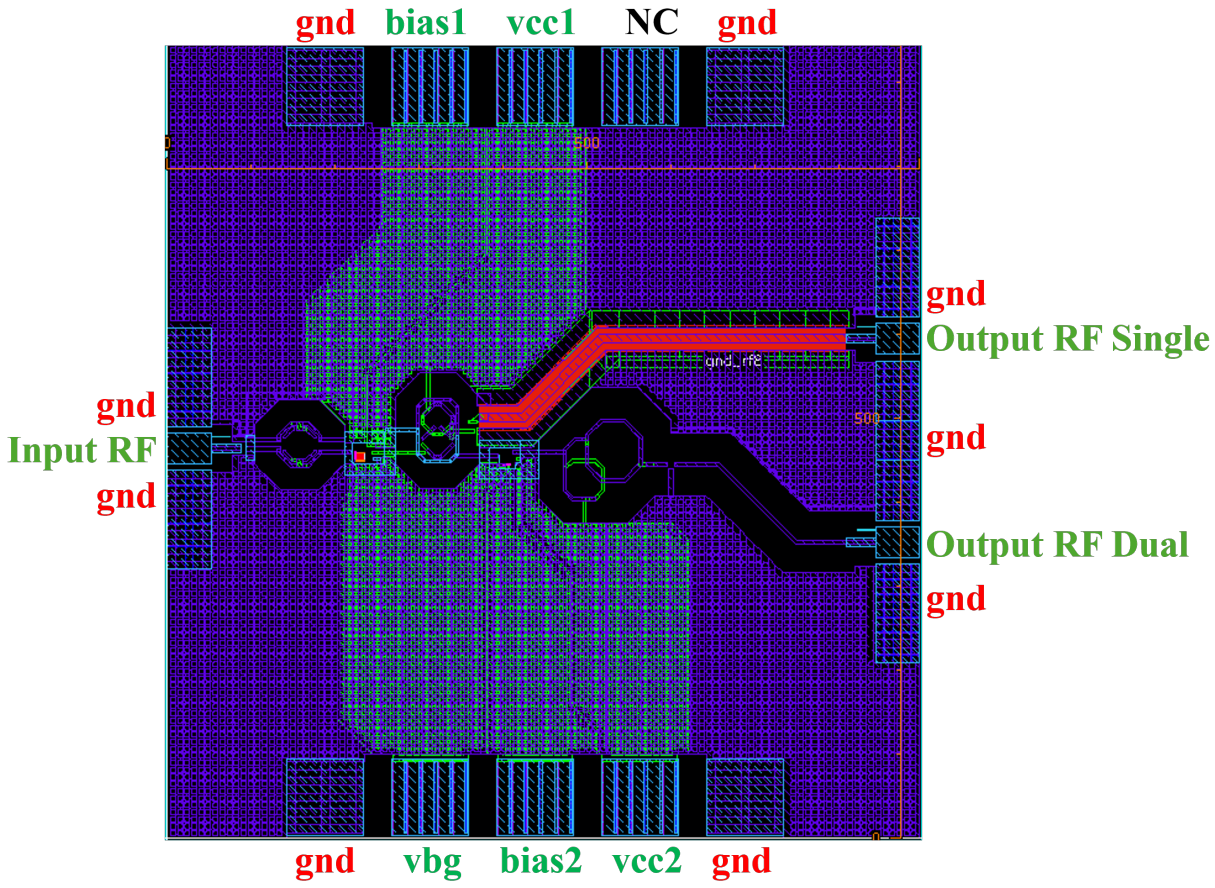


Figure B.1: Complete layout of the LNA, including pads.

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