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Emerging Ferroelectric Devices

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Université de Strasbourg

Doctoral Thesis:

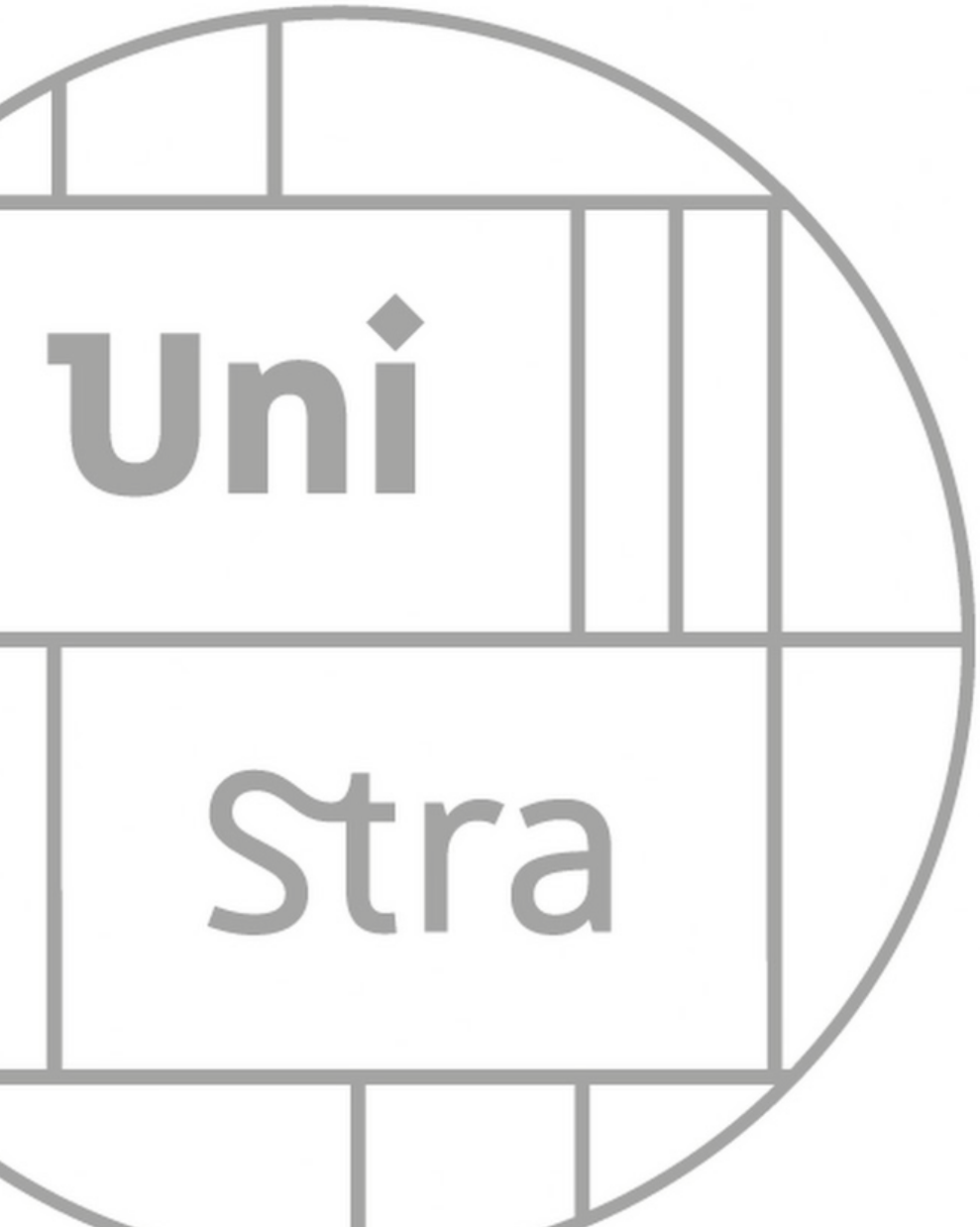
Emerging Ferroelectric Devices

Presented by:
Ankita Ram

Supervisor: Jean-François Dayen

Defended on 20 March, 2025

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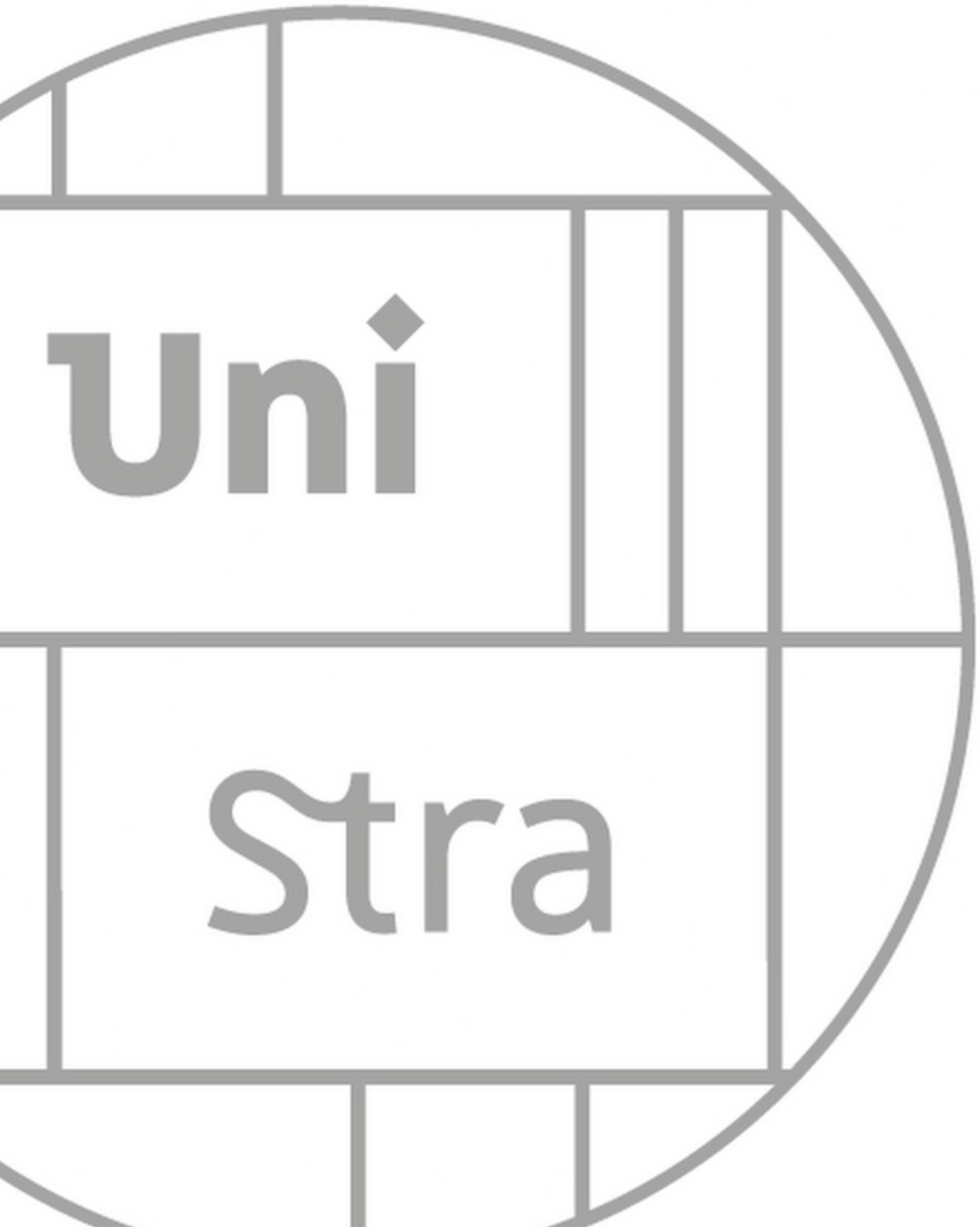
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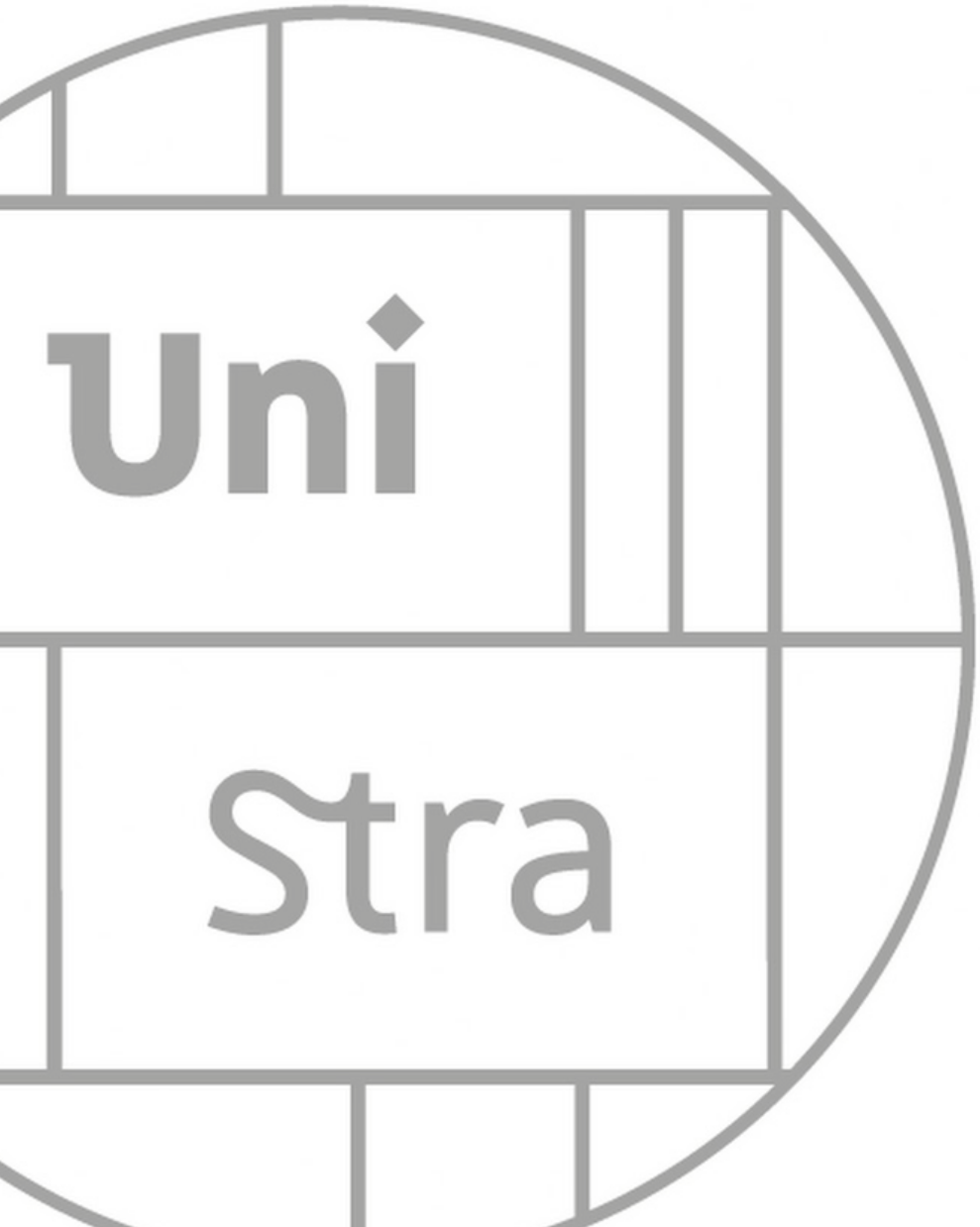
Abstract

As conventional CMOS technology approaches its physical scaling limits, exploring alternative device concepts and materials is essential to maintain advances in energy-efficient information processing. Ferroelectric field-effect transistors (FeFETs), particularly those based on van der Waals (vdW) materials, have emerged as promising candidates owing to their non-volatile switching and compatibility with multifunctional integration. This thesis presents a comprehensive investigation of emerging ferroelectric devices, focusing on their design, fabrication, and applications in reconfigurable electronics, logic, in-memory computing, and neuromorphic architecture.

A key contribution of this work is the development of a reconfigurable split-gate FeFET (Re-FeFET) based on a $CuInP_2S_6$/hBN/WSe_2 heterostructure, enabling programmable switching between *p*-type, *n*-type, and ambipolar conduction through dual-gate control. This architecture supports the implementation of various logic functions, such as Fe-NAND, Fe-AND, and XNOR, within a single device. It also exhibits a photovoltaic response, indicating potential for nanoscale optoelectronic applications. Scaling behavior is investigated through short-channel FeFETs down to 50 nm, which show improved subthreshold swing and reversible drain-induced barrier lowering driven by the negative capacitance of $CuInP_2S_6$, while maintaining reconfigurability via a floating gate and back-gate. Neuromorphic potential is demonstrated through ferroelectric domain switching to emulate synaptic plasticity with reversible conductance modulation under voltage pulses. Finally, a split-gate ferroelectric-semiconductor FET (FeS-FET) using α-In_2Se_3 is studied, where the coexistence of semiconducting and ferroelectric properties, combined with independent dual-gate control, enables reconfigurable logic with multilevel operation and threshold-voltage tunability. Overall, these studies highlight the potential of 2D ferroelectric transistors as building blocks for future energy-efficient, compact, and multifunctional electronics.

Keywords: FeFET, 2D materials, $CuInP_2S_6$, WSe_2, α-In_2Se_3, van der Waals heterostructures, reconfigurable electronics, logic, neuromorphic computing, optoelectronics.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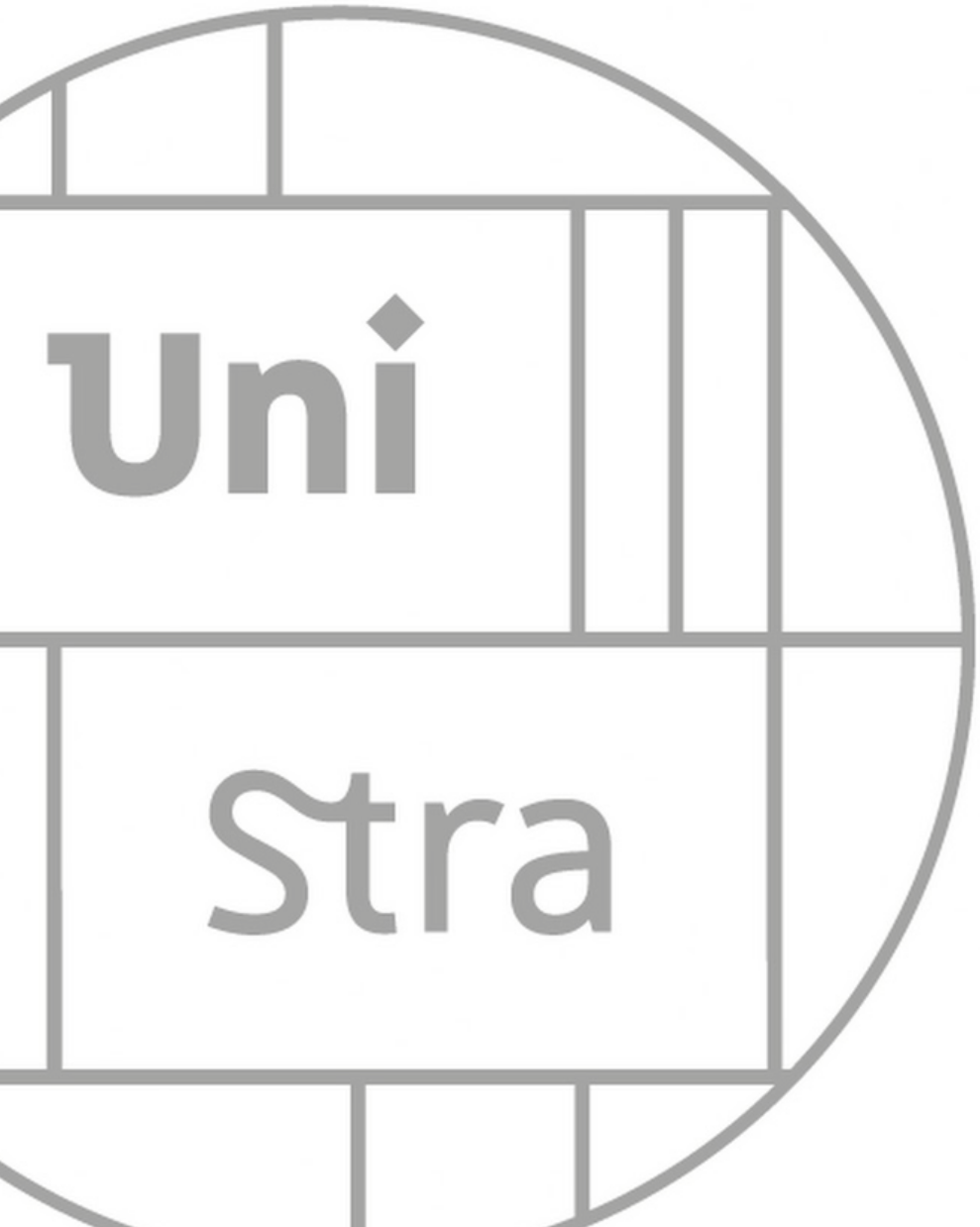
Résumé

À mesure que la technologie CMOS conventionnelle atteint ses limites physiques de miniaturisation, l'exploration de concepts et de matériaux alternatifs devient essentielle pour maintenir les avancées dans le traitement de l'information à faible consommation d'énergie. Les transistors à effet de champ ferroélectriques (FeFET), en particulier ceux basés sur des matériaux de van der Waals (vdW), apparaissent comme des candidats prometteurs grâce à leur commutation non volatile et à leur compatibilité avec une intégration multifonctionnelle. Cette thèse présente une étude approfondie des dispositifs ferroélectriques émergents, en se concentrant sur leur conception, leur fabrication et leurs applications dans l'électronique reconfigurable, la logique, le calcul en mémoire et l'architecture neuromorphique.

Une contribution clé de ce travail est le développement d'un FeFET à grille divisée reconfigurable (Re-FeFET) basé sur une hétérostructure $CuInP_2S_6$/hBN/WSe_2, permettant une commutation programmable entre conduction de type *p*, *n* et ambipolaire grâce à la modulation électrostatique du canal. Cela permet l'implémentation fonctions logiques, telles que Fe-NAND, Fe-AND et XNOR, dans un seul dispositif. Il présente également une réponse photovoltaïque, indiquant un potentiel pour des applications optoélectroniques nanométriques. Le comportement d'échelle est exploré à travers des FeFET à canal court jusqu'à 50 nm, qui montrent une amélioration de la pente sous-seuil et un abaissement réversible de la barrière induit par le drain, dus à la capacitance négative du $CuInP_2S_6$, tout en maintenant la reconfigurabilité via une grille flottante et une grille arrière. Le potentiel neuromorphique est démontré par l'utilisation de la commutation des domaines ferroélectriques pour imiter la plasticité synaptique avec une modulation réversible de la conductance sous impulsions de tension. Enfin, un transistor ferroélectrique-semiconducteur (FeS-FET) utilisant α-In_2Se_3 est étudié, où la coexistence des propriétés semiconductrices et ferroélectriques permet une logique reconfigurable avec fonctionnement multivalué et ajustabilité de la tension de seuil. Dans l'ensemble, ces études mettent en évidence le potentiel des transistors ferroélectriques 2D comme éléments de base pour une électronique future économe en énergie, compacte et multifonctionnelle.

Mots-clés : FeFET, matériaux 2D, $CuInP_2S_6$, WSe_2, α-In_2Se_3, hétérostructures de van der Waals, électronique reconfigurable, logique, calcul neuromorphique, optoélectronique.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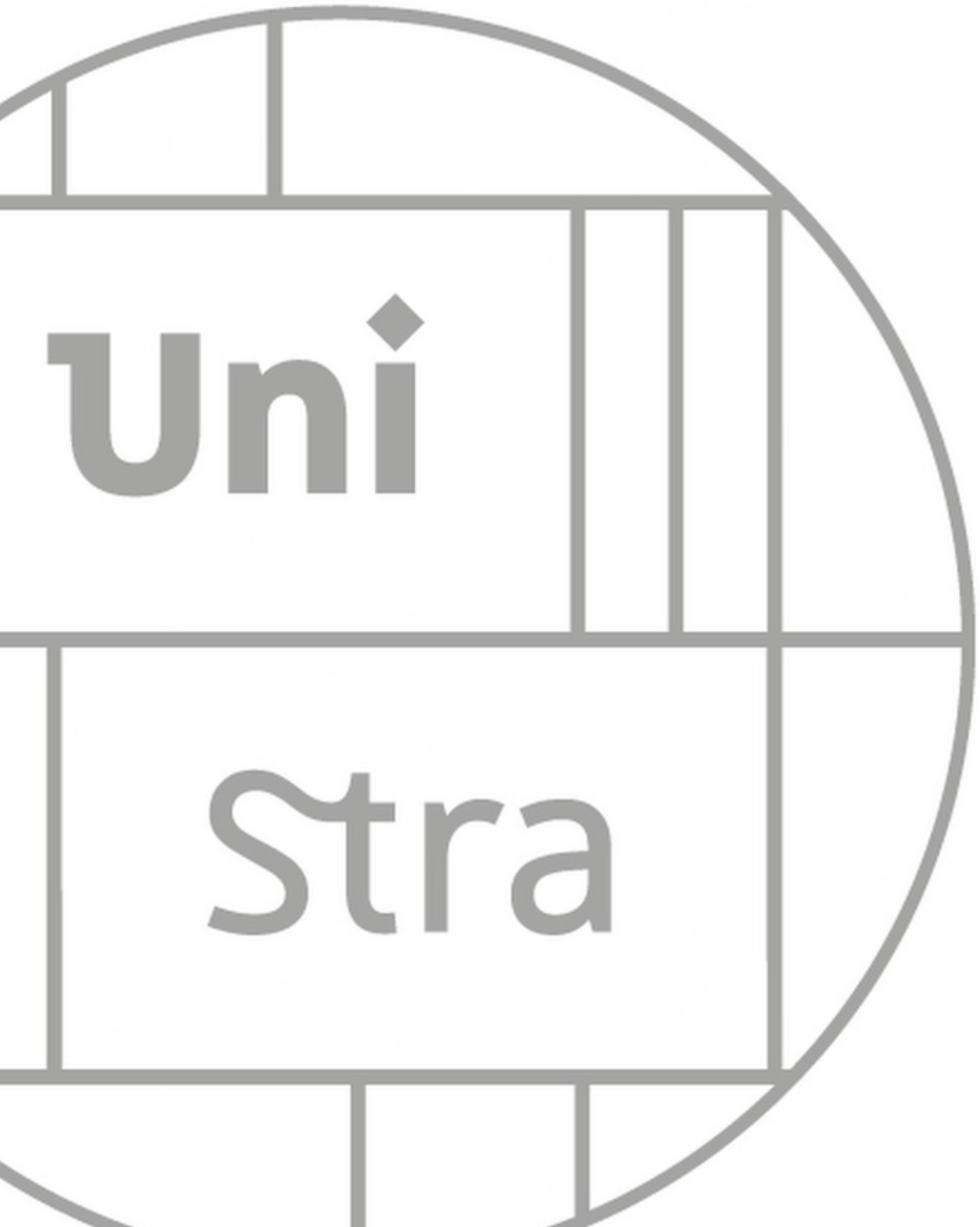
To my beloved parents...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♡Ankita

Synthèse de la thèse (version française)

Contexte et Motivation

1. Contexte historique et évolution du dimensionnement CMOS

L'invention du transistor en 1947 a révolutionné l'électronique en remplaçant les tubes à vide encombrants par des interrupteurs compacts et écoénergétiques. Elle a été suivie par le développement des circuits intégrés en 1959, permettant l'intégration de plusieurs transistors sur une seule puce. L'émergence du transistor à effet de champ métal-oxyde-semiconducteur (MOSFET), suivie de l'adoption de la technologie CMOS (Complementary Metal-Oxide-Semiconductor) dans les années 1970, a permis une intégration à grande échelle avec une consommation minimale, posant ainsi les bases de l'informatique moderne.

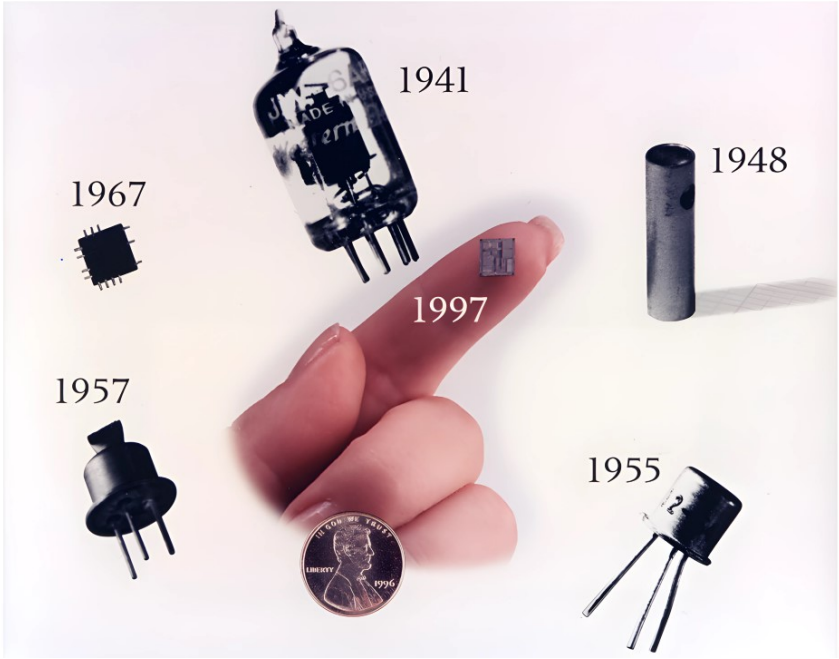


Figure 1: Évolution du transistor, des tubes à vide aux processeurs numériques modernes.

Pendant des décennies, la loi de Moore a guidé l'industrie des semi-conducteurs, prédisant un doublement de la densité de transistors sur les circuits intégrés environ tous les deux ans. En parallèle, le dimensionnement de Dennard suggérait que la réduction de taille des transistors permettait d'augmenter la vitesse de commutation tout en maintenant la densité de puissance constante. Toutefois, au début des années 2000, ce paradigme a atteint ses limites physiques et thermiques, notamment à cause de courants de fuite accrus, d'une dissipation thermique excessive et d'une saturation des performances, menant à ce que l'on appelle le « mur thermique ».

Pour maintenir les progrès, l'industrie a évolué d'un modèle « More Moore » vers une diversification « More-than-Moore », axée sur des innovations fonctionnelles par de nouveaux matériaux, des architectures 3D, et des composants économes en énergie. Cela inclut des percées architecturales telles que les FinFETs, les transistors à grille tout autour (GAA), les diélectriques à haute constante (high-k), ainsi que des technologies d'empilement 3D qui améliorent la densité et les performances sans réduction supplémentaire de la taille.

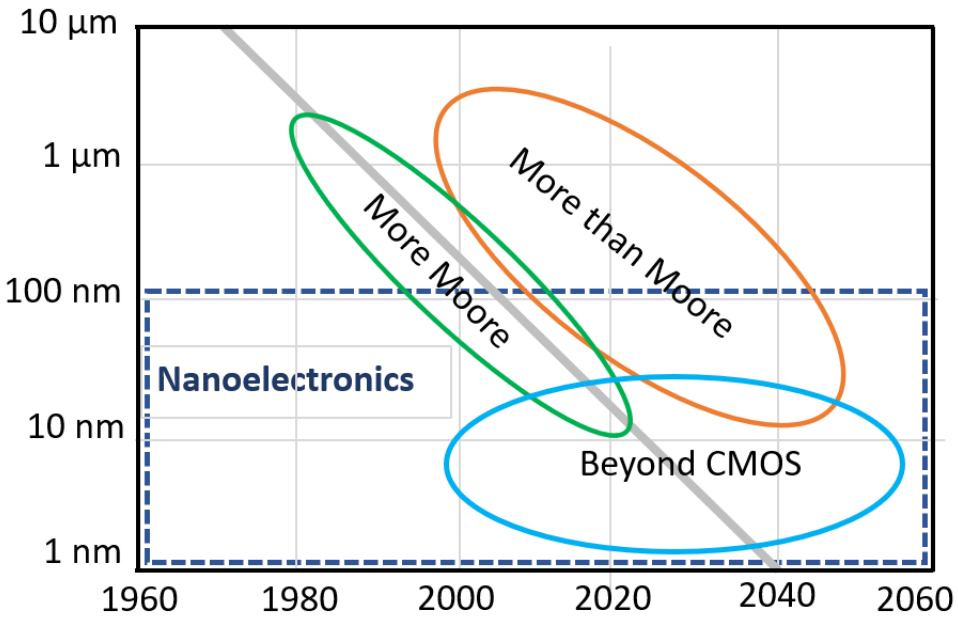


Figure 2: Feuille de route de la nanoélectronique.

Ces avancées approchent elles-mêmes des limites physiques. Par conséquent, les chercheurs explorent de nouveaux concepts de dispositifs, notamment les transistors à effet de champ ferroélectrique (FeFETs), les transistors à capacité négative (NCFETs), et les circuits logiques reconfigurables à base de matériaux bidimensionnels (2D). Ces plateformes émergentes offrent une faible consommation d'énergie, une commutation non-volatile et des capacités d'intégration multifonctionnelle.

Cette thèse explore ces dispositifs ferroélectriques de nouvelle génération, en mettant l'accent sur leur intégration avec des matériaux 2D pour permettre des solutions évolutives et économes en énergie destinées aux applications logiques, mémoire et neuromorphiques.

2. Électronique reconfigurable et ferroélectricité

L'électronique reconfigurable représente une nouvelle classe de dispositifs capables de modifier dynamiquement leur fonctionnalité en fonction de signaux de commande externes. Contrairement aux transistors conventionnels à comportement fixe, ces dispositifs peuvent commuter entre conduction de type n et de type p, permettant à un seul composant d'assumer plusieurs rôles. Cette flexibilité réduit la complexité des circuits et améliore leur efficacité. Comme illustré à la Fig.3, la modulation électrostatique dans les matériaux 2D permet diverses configurations dynamiques telles que l'inversion de polarité, le contrôle de la tension de seuil, et la reconfiguration logique.

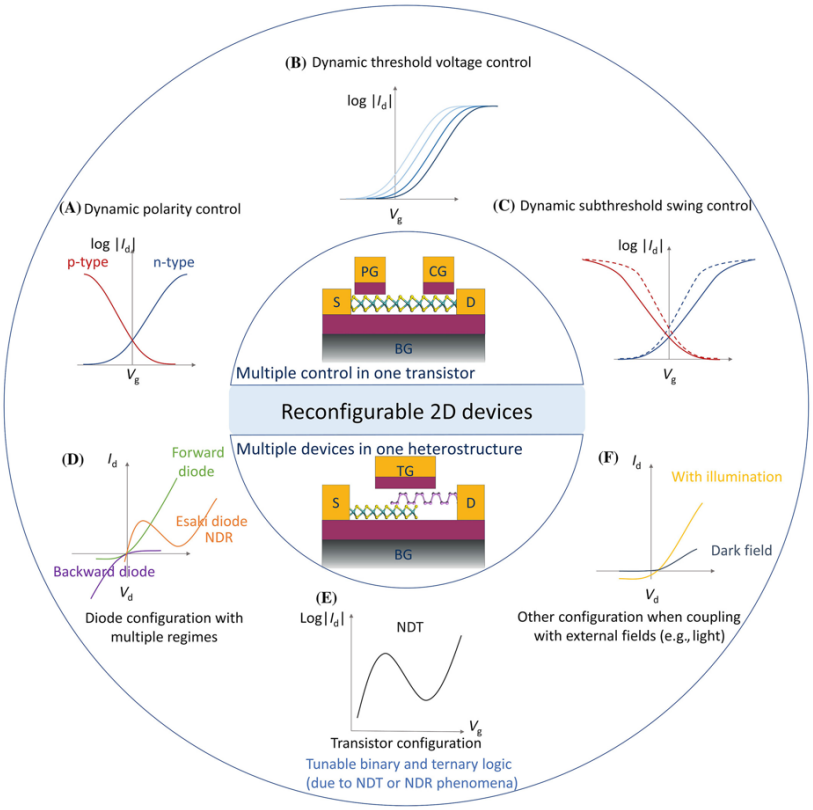


Figure 3: Modes de fonctionnement dynamiques dans des dispositifs reconfigurables à base de matériaux 2D via commande électrostatique.

Les matériaux ferroélectriques, quant à eux, possèdent une polarisation spontanée réversible. Cette polarisation est conservée sans alimentation continue, permettant une commutation

non-volatile et une très faible consommation énergétique. Dans le contexte des matériaux 2D, la ferroélectricité ouvre de nouvelles possibilités pour des dispositifs compacts et efficaces. La Fig.4 classe les types de matériaux ferroélectriques et d'architectures utilisées dans l'électronique 2D, allant des éléments mémoire à la logique, en passant par les systèmes neuromorphiques. Leur structure en couches facilite leur intégration dans les dispositifs électroniques à l'échelle nanométrique.

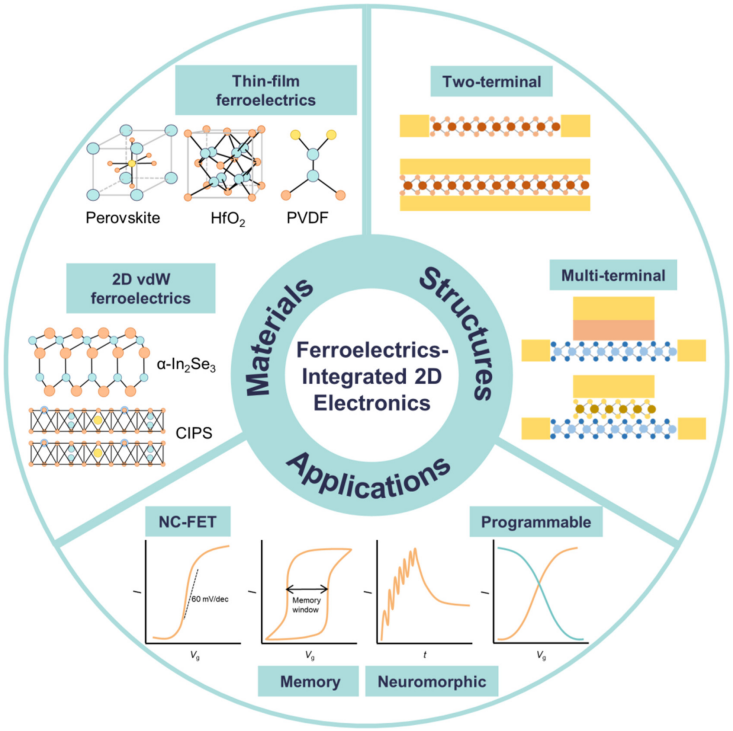


Figure 4: Classification des matériaux ferroélectriques et leurs rôles dans l'électronique 2D : mémoire, logique, et applications neuromorphiques.

En combinant reconfigurabilité et mémoire non-volatile, l'électronique reconfigurable basée sur la ferroélectricité représente une voie prometteuse pour dépasser les limitations de la technologie CMOS traditionnelle.

3. Matériaux bidimensionnels utilisés dans cette étude

Les matériaux bidimensionnels (2D) présentent des propriétés structurales et électroniques uniques grâce à leur épaisseur atomique, leur faible dimensionnalité, et des interfaces propres exemptes de liaisons pendantes. Leur compatibilité entre eux permet la formation d'hétérostructures de van der Waals (vdW) sans contrainte de maille, combinant des propriétés isolantes, semiconductrices et ferroélectriques dans une seule pile verticale, stratégie essentielle dans ce

travail.

Isolant vdW : hBN

Le nitrure de bore hexagonal (hBN) est un cristal isolant 2D à large bande interdite avec une structure en nid d'abeilles. Sa surface chimiquement inerte et atomiquement plate minimise les pièges de charge à l'interface, réduisant la diffusion et améliorant le transport de charge. Son absence de liaisons pendantes et son champ de claquage élevé en font un diélectrique idéal dans les hétérostructures vdW.

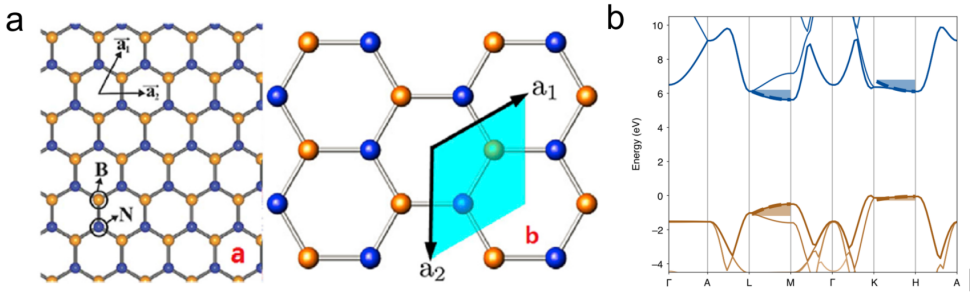


Figure 5: (a) Structure en nid d'abeilles du hBN 2D avec vecteurs de réseau de Bravais (gauche) et maille élémentaire (droite). (b) Structure de bande du hBN, montrant ses propriétés électroniques essentielles pour son rôle d'isolant.

Semi-conducteur vdW : WSe_2

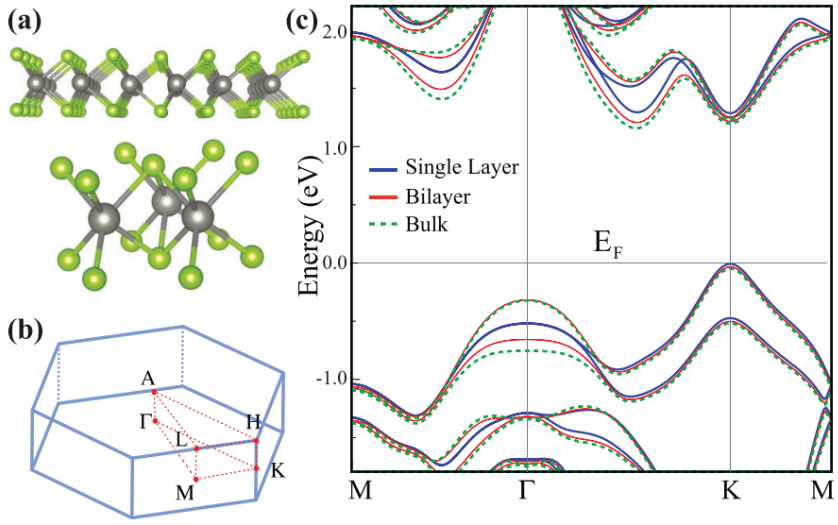


Figure 6: (a) Structure cristalline du WSe_2 (vues latérale et de dessus). (b) Zone de Brillouin avec les points de haute symétrie. (c) Évolution de la bande interdite du vrac vers la monocouche. La transition indirecte-directe améliore les propriétés optoélectroniques.

Le diséléniure de tungstène (WSe_2) est un dichalcogénure de métal de transition qui présente une transition de bande interdite indirecte à directe à l'échelle de la monocouche. Sa structure permet une conduction ambipolaire et une réponse électronique dépendant de l'épaisseur. Il constitue un excellent canal semi-conducteur avec des mobilités symétriques pour les électrons et les trous.

Isolant ferroélectrique vdW : $CuInP_2S_6$

Le $CuInP_2S_6$ (CIPS) est un matériau ferroélectrique 2D rare présentant une polarisation spontanée à température ambiante. Sa structure en couches permet une commutation ferroélectrique jusqu'à des épaisseurs nanométriques, rendant son intégration dans les hétérostructures vdW robuste et évolutive.

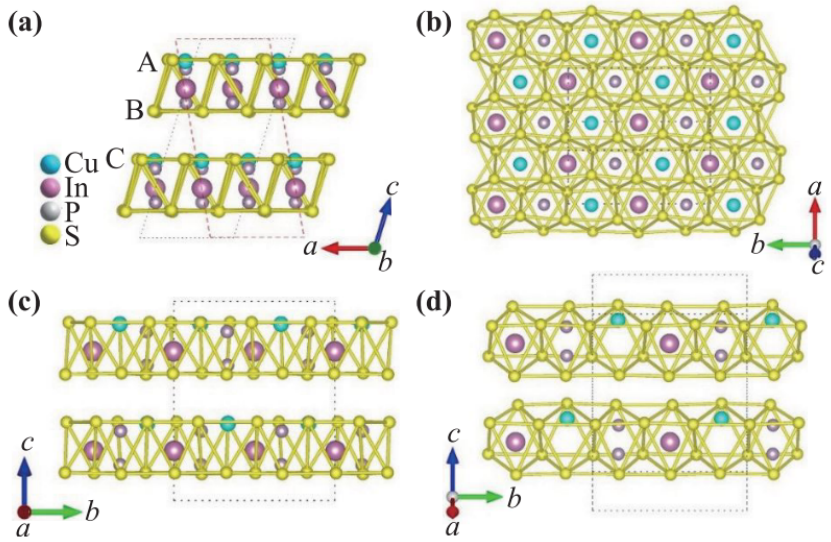


Figure 7: Structure cristalline de CIPS montrant l'empilement des sous-réseaux de soufre, de cuivre, d'indium et de phosphore. Les interactions faibles de van der Waals permettent l'exfoliation.

Semi-conducteur ferroélectrique vdW : α-In_2Se_3

L'α-In_2Se_3 est un semi-conducteur ferroélectrique présentant des composantes de polarisation aussi bien dans le plan qu'hors du plan. Cette asymétrie structurelle induite par les déplacements atomiques dans les couches de Se permet une commutation ferroélectrique même dans des films ultra-minces.

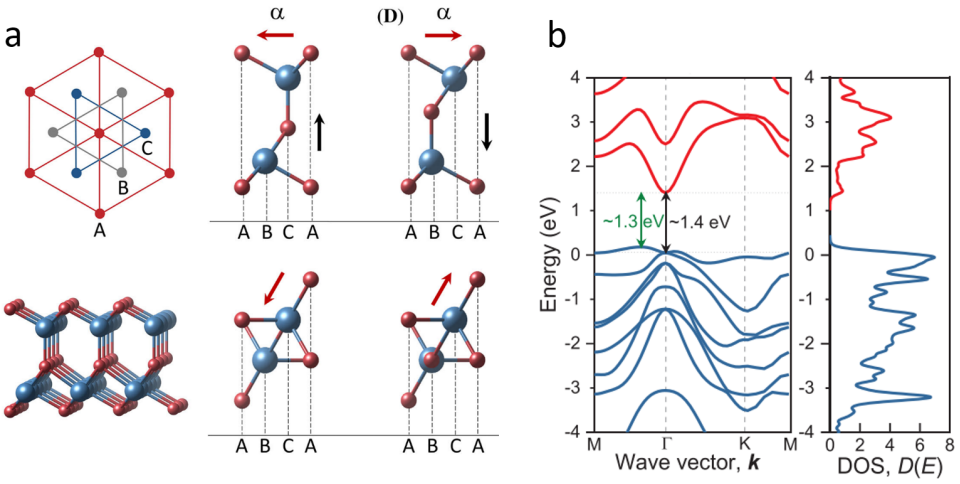


Figure 8: (a) Structure cristalline et directions de polarisation de α-In_2Se_3. (b) Structure de bande obtenue par DFT.

4. Principes Fondamentaux et Concepts de Dispositifs

MOSFET : Les transistors à effet de champ (FET) constituent les éléments de base de l'électronique moderne, offrant un contrôle électrique du transport de porteurs via la modulation par la grille. Parmi eux, le transistor à effet de champ métal-oxyde-semiconducteur (MOSFET) utilise une couche isolante d'oxyde entre la grille et le semiconducteur, où la tension de grille module la conductance du canal par effet de champ électrostatique.

FeFET : Une avancée majeure dans la technologie des FETs consiste à remplacer la couche isolante conventionnelle par un matériau ferroélectrique, donnant naissance au transistor à effet de champ ferroélectrique (FeFET). Ce remplacement introduit une commutation de polarisation non-volatile, permettant une fonctionnalité mémoire directement au sein du transistor. Le comportement du FeFET est influencé à la fois par la charge de surface et la polarisation spontanée, modifiant sa tension de seuil. L'hystérésis résultant de la commutation de polarisation permet aux FeFETs de fonctionner dans des régimes bistables, utiles pour les applications mémoire et neuromorphiques.

FeS-FET : Un autre concept de dispositif repose sur l'intégration de la ferroélectricité directement dans le canal. Le transistor à effet de champ à semiconducteur ferroélectrique (FeSFET) utilise un semiconducteur ferroélectrique comme matériau actif du canal. Cette structure permet une contribution conjointe des charges liées à la polarisation et des charges mobiles, modifiant fondamentalement la dynamique de transport. Le champ électrique de grille module à la fois la charge et la polarisation dans le canal, produisant un comportement d'hystérésis distinct qui dépend de la profondeur de pénétration du champ électrique. La Fig.9 illustre les

différences structurelles et fonctionnelles clés entre les dispositifs FeFET et FeSFET.

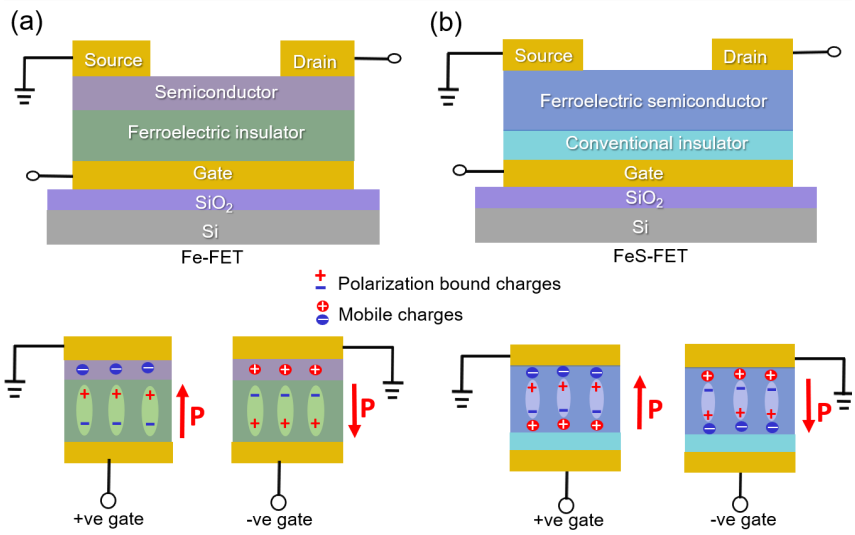


Figure 9: Comparaison structurelle entre FeFET et FeS-FET. (a) Structure FeFET avec un isolant ferroélectrique comme diélectrique de grille, où les charges liées à la polarisation modulent la conductance du canal. (b) Structure FeS-FET, où un semiconducteur ferroélectrique remplace le diélectrique, entraînant une accumulation conjointe de charges liées à la polarisation et de charges mobiles. Les panneaux inférieurs illustrent les distributions de charges sous différentes tensions de grille, montrant l'impact de la polarisation sur le transport de charge.

Dispositifs Synaptiques : Au-delà de la logique et de la mémoire, les transistors ferroélectriques servent également de synapses artificielles pour le calcul neuromorphique. Inspirés des synapses biologiques, qui modulent l'intensité des signaux via la dynamique des neurotransmetteurs, les dispositifs synaptiques artificiels cherchent à reproduire ce comportement à l'aide de signaux électriques. Les synapses à base de FeFET ajustent leur conductance via la commutation de polarisation induite par des impulsions appliquées à la grille. Ce changement de conductance, représentant le courant post-synaptique, est analogue à la réponse post-synaptique biologique. La Fig.10 compare les synapses biologiques avec leurs équivalents artificiels à base de FeFETs à matériaux bidimensionnels.

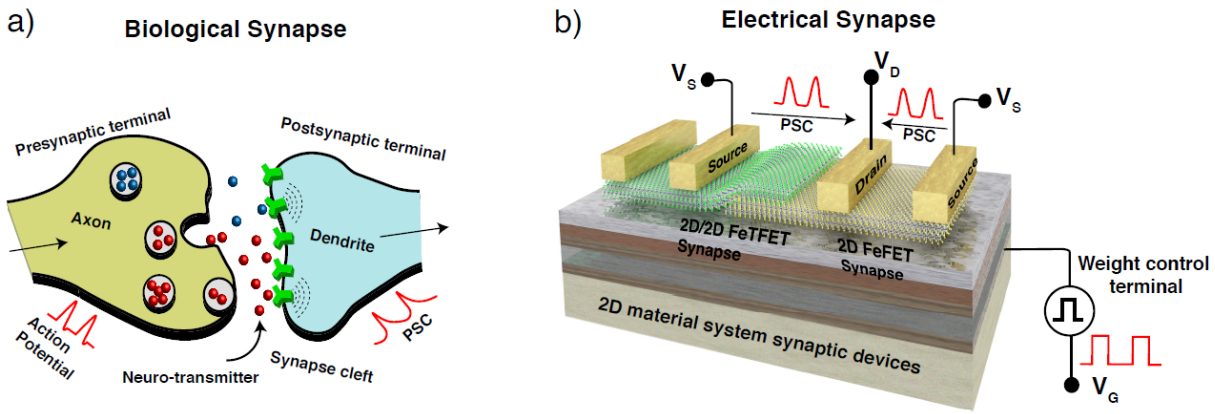


Figure 10: (a) Schéma d'une synapse biologique où les neurotransmetteurs assurent la transmission du signal, produisant un courant post-synaptique (PSC) au niveau du terminal post-synaptique. (b) Dispositifs synaptiques ferroélectriques basés sur les structures FeFET à WSe_2 et FeTFET à $WSe_2/SnSe_2$, où des impulsions de tension de grille induisent une commutation de polarisation pour simuler la variation du poids synaptique. Le PSC (courant post-synaptique), représenté par le courant de drain, est enregistré après chaque impulsion pour refléter la réponse synaptique.

Cette section expose comment la ferroélectricité améliore les conceptions conventionnelles de transistors et étend leur fonctionnalité vers les domaines de la mémoire et du calcul neuromorphique grâce à des innovations architecturales et à l'intégration de nouveaux matériaux.

Travail Expérimental et Résultats

5. Fabrication et Techniques de Caractérisation des Dispositifs

La fabrication des dispositifs Re-FeFET présentés dans ce travail a impliqué l'empilement déterministe de matériaux de van der Waals (vdW) par techniques de transfert à sec, suivi par un motifage lithographique à l'échelle nanométrique et un dépôt métallique. Un processus systématique a été adopté afin d'assurer des interfaces de haute qualité et des performances reproductibles.

Exfoliation des Matériaux 2D

Des feuillets 2D de haute qualité de WSe_2, hBN, $CuInP_2S_6$ (CIPS) et α-In_2Se_3 ont été obtenus par exfoliation mécanique à partir de cristaux massifs à l'aide de ruban adhésif. Les feuillets

exfoliés ont ensuite été transférés sur des films transparents de PDMS ou sur des substrats Si/SiO_2 pour une inspection optique et un tri par épaisseur. Les feuillets sélectionnés ont été identifiés par contraste optique et vérifiés par AFM.

Transfert à Sec et Assemblage des Empilements

Deux méthodes de transfert à sec ont été utilisées pour construire les hétérostructures souhaitées :

- **Transfert ascendant (bottom-up) :** Les feuillets ont été prélevés et empilés séquentiellement à l'aide d'un tampon de PDMS sous chauffage contrôlé. Cette méthode permet un alignement couche par couche et minimise la contamination.
- **Transfert descendant (top-down) :** Un tampon PC/PDMS a été utilisé pour prélever individuellement les couches depuis le substrat et assembler l'hétérostructure complète. L'empilement final a ensuite été déposé sur le substrat cible à température élevée, suivi par la dissolution du PC dans l'acétone.

Ces méthodes ont permis une intégration précise des couches ferroélectriques et semi-conductrices avec une dégradation minimale des interfaces.

Lithographie par Faisceau d'Électrons (EBL)

Des motifs nanométriques, tels que les électrodes source-drain et les grilles divisées, ont été définis par EBL. Une pile bilayer de résine PMMA a été optimisée pour l'épaisseur, le lift-off, et la dissipation de charge, en particulier sur des surfaces isolantes. Après exposition et développement, les contacts métalliques (Ti/Au ou Cr/Au) ont été déposés par évaporation par faisceau d'électrons. Le lift-off dans l'acétone a révélé des structures de contact bien définies. Des dispositifs à canal court jusqu'à 50 nm ont été réalisés en utilisant une EBL calibrée en dose et un contrôle précis de l'ouverture.

Lithographie Optique par Laser

Les grandes zones de contact ont été définies par lithographie laser optique avec de la résine AZ 1505. Cette méthode a été privilégiée pour sa simplicité et son efficacité dans la définition de motifs de grande taille ne nécessitant pas de résolution nanométrique.

Intégration Finale et Schéma de Fabrication

La séquence complète de fabrication du dispositif est résumée dans la Fig. 11. Elle commence par le motifage des grilles divisées sur des substrats Si/SiO_2 à l'aide de l'EBL. Après identification des feuillets 2D appropriés sur PDMS par microscopie optique, les couches individuelles de CIPS, hBN et WSe_2 sont empilées séquentiellement par transfert à sec pour former l'hétérostructure active. L'épaisseur de chaque feuillet est vérifiée par AFM. Une fois l'empilement réalisé, des électrodes supérieures alignées sont définies par EBL et déposées par évaporation Ti/Au. Un contact supérieur plus épais assure la stabilité mécanique de l'empilement multicouche. Le bonding du dispositif est ensuite réalisé avec de la pâte d'argent et de l'époxy, suivi par un montage dans un cryostat pour les mesures à basse température et les tests optoélectroniques.

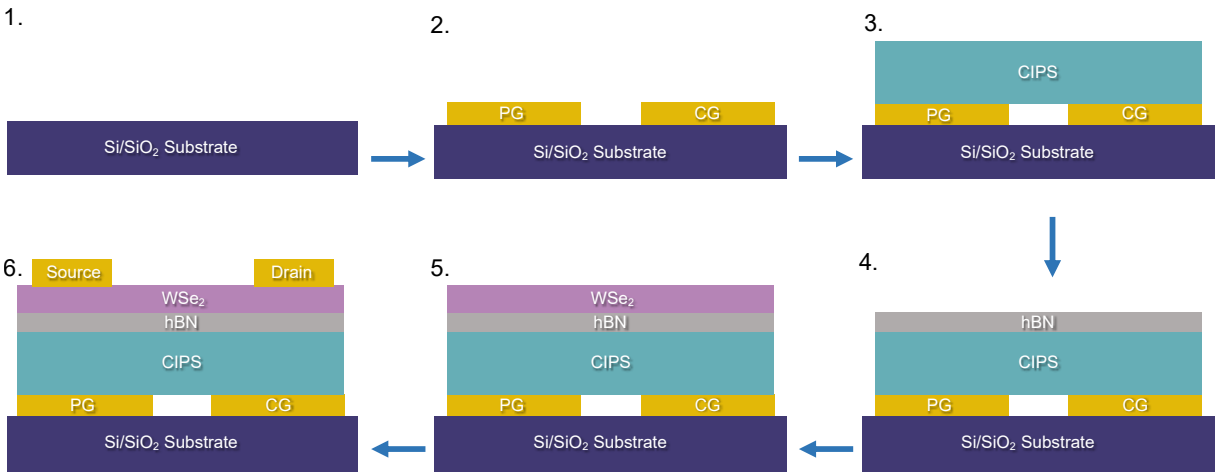


Figure 11: Schéma du processus de fabrication des dispositifs. Les étapes clés incluent l'exfoliation des feuillets 2D, l'empilement à sec des matériaux vdW, le motifage des grilles divisées, et le dépôt final des électrodes supérieures.

Des images optiques des feuillets exfoliés et des principales étapes de fabrication sont présentées en Fig.12.

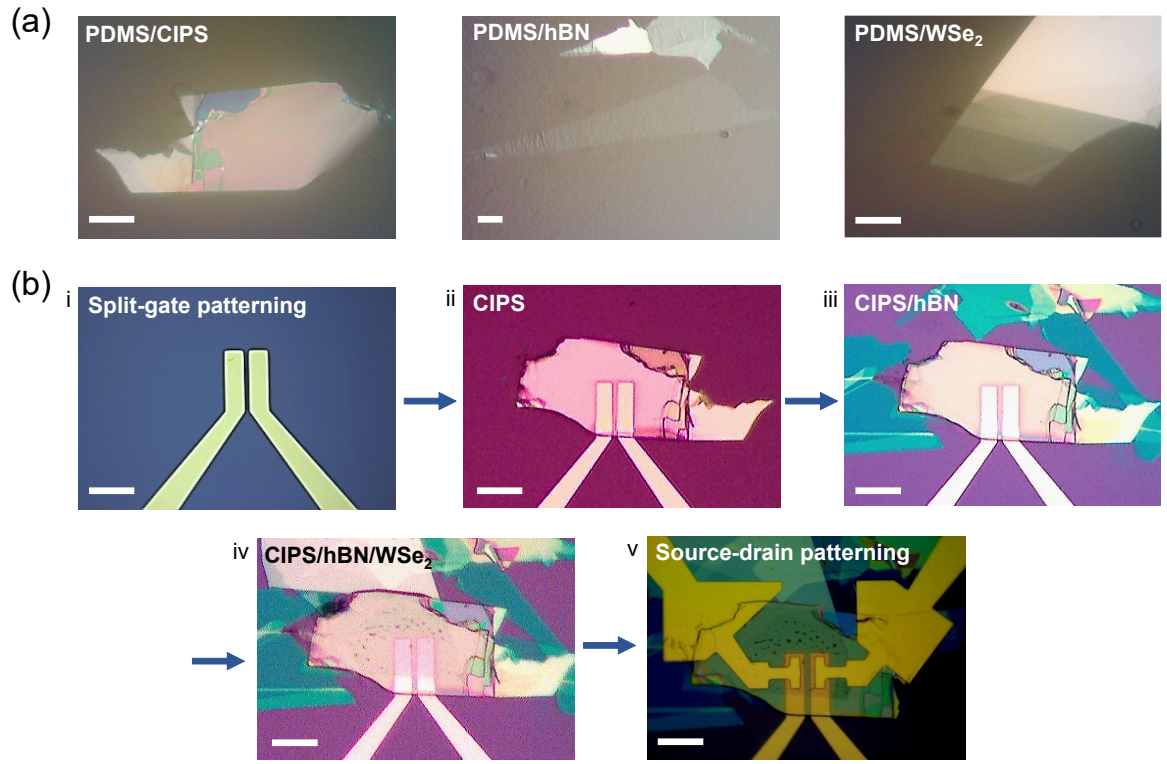


Figure 12: Images au microscope optique (barre d'échelle = 20 μm) de (a) feuillets exfoliés de CIPS, hBN et WSe_2 sur des substrats PDMS indépendants, (b) différentes étapes de fabrication d'un dispositif Re-FeFET typique.

Techniques de Caractérisation

Microscopie à Force Atomique (AFM) : L'épaisseur des feuillets et la morphologie de surface ont été mesurées à l'aide d'un AFM Bruker Dimension Icon en mode tapping avec des pointes TESPA-V2 en silicium.

Microscopie à Force de Piezoréponse (PFM) : La commutation des domaines ferroélectriques et l'hystérésis de polarisation ont été étudiées à l'aide d'un système AFM Nanoscope V Multimode avec amplificateurs externes à verrouillage de phase. Les mesures ont été effectuées avec des pointes conductrices à une fréquence d'excitation d'environ 35 kHz.

Spectroscopie Raman : Un système Horiba Labram avec un laser de 532 nm a été utilisé pour identifier les phases matérielles, le dopage et les contraintes. Les mesures ont été réalisées à température ambiante avec une puissance incidente d'environ 250 μW.

Mesures Cryogéniques et de Photo-Transport : Les caractérisations électriques et optoélectroniques ont été réalisées dans des cryostats à circulation d'hélium. Un source-mètre K2634B et un nanovoltmètre K2182A ont été utilisés pour les mesures I-V et les tests de cir-

cuits logiques. Les mesures de photo-réponse ont été effectuées à l'aide d'un laser de 522 nm via une fibre optique in situ.

6. Dispositifs Ferroélectriques Multifonctionnels et Reconfigurables à Base de van der Waals et Circuits Logiques

Ce chapitre présente un transistor à effet de champ ferroélectrique reconfigurable multifonctionnel (Re-FeFET), fabriqué à partir d'une hétérostructure van der Waals (vdW) composée de $CuInP_2S_6$ (CIPS), hBN et WSe_2. L'architecture unique à double grille (split-gate) permet un dopage modulable et un contrôle opérationnel basé sur la polarisation, réalisant dans un seul dispositif des fonctions reconfigurables de logique, de mémoire et d'optoélectronique.

Structure et Configuration du Dispositif

Le Re-FeFET intègre un canal semiconducteur en WSe_2, une couche ferroélectrique de CIPS et un intercalaire hBN (Fig.13). Les grilles divisées permettent un contrôle indépendant de deux régions du canal. La programmation de la polarisation du CIPS via la tension de grille permet un contrôle non-volatile du type de dopage dans le WSe_2 (soit n-type, soit p-type), permettant ainsi la formation dynamique d'états homojonction p–p, n–n, p–n et n–p.

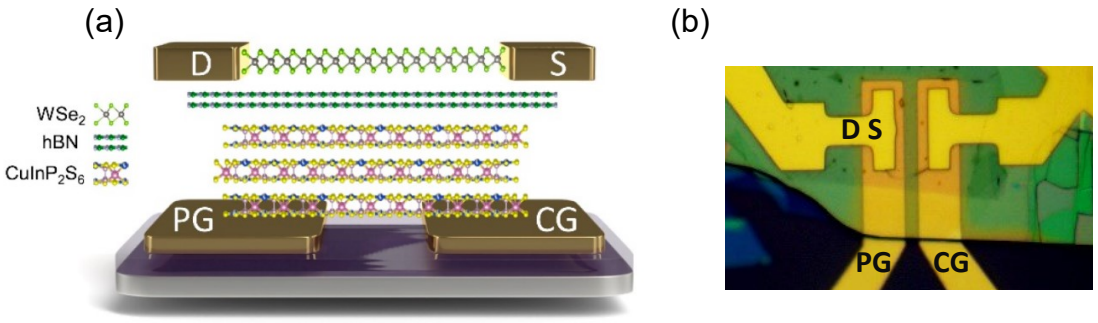


Figure 13: (a) Schéma du dispositif et (b) image optique.

Transconductance Reconfigurable

Le comportement en transconductance (Fig.14) révèle trois modes de fonctionnement distincts :

- **Mode ambipolaire :** Les deux grilles sont balayées simultanément, produisant une courbe de transfert symétrique avec des branches p et n bien définies, chacune présentant une hystérésis ferroélectrique.

- **Modes unipolaires :** En fixant la tension de la grille de programmation au-dessus ou en dessous du seuil coercitif ferroélectrique, le dispositif adopte un comportement de n-FeFET ou p-FeFET. La grille de contrôle module ensuite la conductivité du canal, montrant des boucles d'hystérésis nettes et réversibles associées à la commutation ferroélectrique.

Ces caractéristiques valident l'efficacité de la structure à double grille pour un fonctionnement programmable, stable, avec des rapports on/off élevés et des fenêtres mémoire robustes.

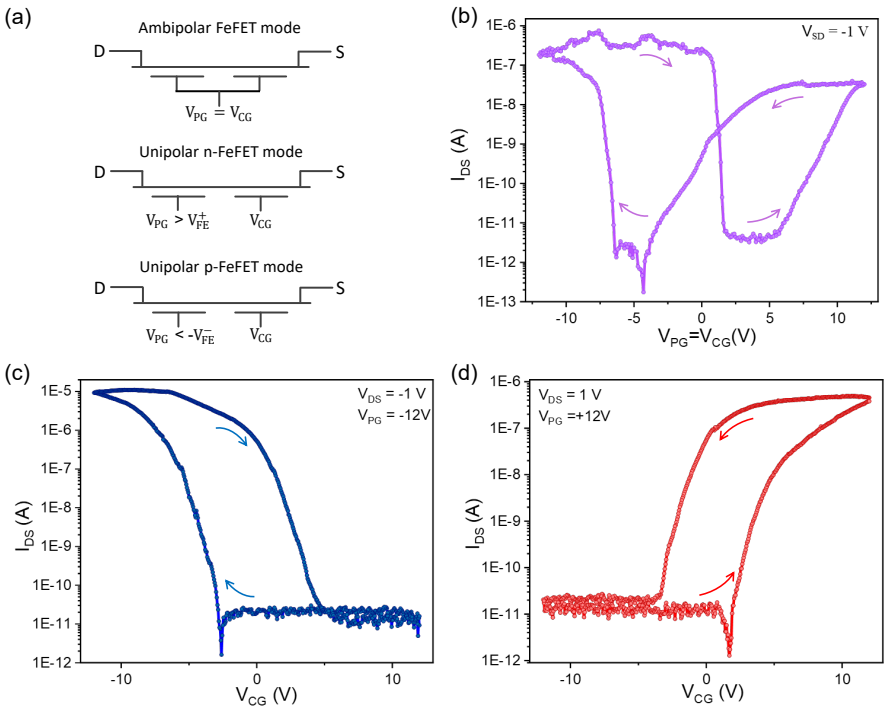


Figure 14: Transistor à effet de champ ferroélectrique à polarités reconfigurables. (a) Schéma des différents modes de fonctionnement du Re-FeFET. En mode ambipolaire, les deux grilles sont polarisées par une tension identique. En mode unipolaire n-FeFET (resp. p-FeFET), la tension de la grille de programmation V_{PG} est fixée au-dessus (resp. en dessous) de la tension coercitive ferroélectrique V_{FE}, tandis que la tension de la grille de contrôle V_{CG} est balayée. (b) Boucle de transconductance du Re-FeFET en mode ambipolaire, montrant une hystérésis ambipolaire avec une boucle antihoraire dans la branche n et une boucle horaire dans la branche p. (c, d) Boucles de transconductance du Re-FeFET en mode p-FeFET et n-FeFET, respectivement. La commutation de polarisation ferroélectrique du CIPS est responsable de l'hystérésis antihoraire (resp. horaire) dans le mode n-FeFET (resp. p-FeFET).

Fonctionnalité Optoélectronique

En configuration ambipolaire, le dispositif fonctionne comme une photodiode photovoltaïque (Fig.15). Le champ électrique intégré aux jonctions p–n ou n–p facilite la séparation des porteurs, générant un courant de court-circuit significatif (I_{SC}) et une tension de circuit ouvert (V_{OC}). Notamment, V_{OC} atteint jusqu'à $\pm$0,7 V et I_{SC} jusqu'à $\pm$1,3 nA—parmi les plus élevés rapportés pour des dispositifs à base de WSe_2.

La cartographie spatiale de V_{OC} et I_{SC} en fonction des tensions de grille montre que la réponse photovoltaïque n'apparaît que dans les états ambipolaires, tandis que les états unipolaires (n–n et p–p) ne présentent aucune photo-réponse, ce qui est cohérent avec un comportement de phototransistor. Cette double réponse optique renforce la polyvalence fonctionnelle du Re-FeFET.

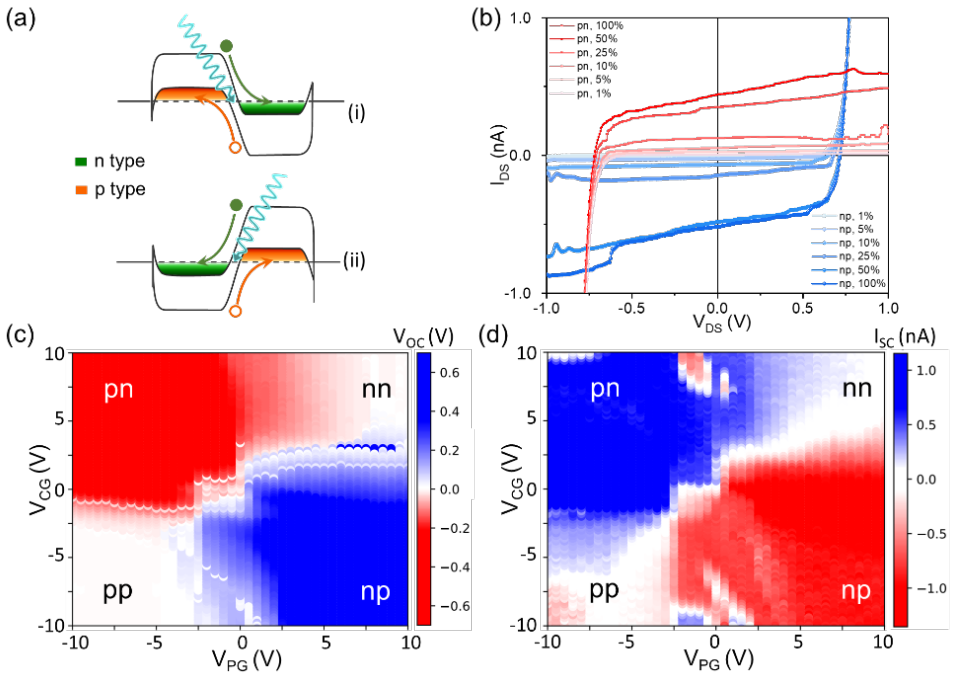


Figure 15: Propriétés optoélectroniques et photovoltaïques du Re-FeFET. (a) Diagramme de bandes illustrant l'effet photovoltaïque dans une configuration homojonction (i) p-n et (ii) n-p du canal en WSe_2. (b) Caractéristiques courant–tension source-drain du Re-FeFET programmé en configurations p-n (rouge) et n-p (bleu), sous diverses excitations lumineuses (Puissance = 0,1 mW·mm^{-2}, $\lambda = 522$ nm). (c) Carte en couleurs de la tension de circuit ouvert V_{OC} ($I_{DS} = 0$ A) en fonction des tensions des grilles de programmation (V_{PG}) et de contrôle (V_{CG}). (d) Carte en couleurs du courant de court-circuit I_{SC} ($V_{DS} = 0$ V) selon le balayage indépendant des deux grilles latérales.

Opération Logique avec Mémoire Intégrée

Le Re-FeFET permet des opérations logiques polymorphes :

- **Mode électronique :** Le contrôle par double grille permet l'implémentation de la fonction XNOR sans inverseurs supplémentaires.
- **Mode ferroélectrique :** Des états de polarisation préprogrammés définissent des portes logiques FE-AND et FE-NAND, en utilisant les états rémanents pour un fonctionnement à consommation nulle en veille. Les quatre états logiques présentent une rétention prolongée supérieure à 10^4 secondes.

Intégration en Circuit

En combinant deux Re-FeFETs en série, les six portes logiques fondamentales (NOT, AND, OR, NAND, NOR, XOR) peuvent être implémentées avec un nombre minimal de transistors. Comparé aux circuits CMOS classiques, cela permet une réduction de taille allant jusqu'à 6×, offrant une plateforme extrêmement compacte et économe en énergie pour des circuits logiques reconfigurables et sécurisés.

7. Effet d'échelle dans les transistors à effet de champ ferroélectriques (FeFETs) à base de $CuInP_2S_6/WSe_2$ en hétérostructure de van der Waals

Ce chapitre étudie le comportement d'échelle des transistors à effet de champ ferroélectriques (FeFETs) à base de $CuInP_2S_6$ (CIPS)/WSe_2, en fabriquant des dispositifs avec des longueurs de canal systématiquement variées, jusqu'à 50 nm, en utilisant une architecture à grille supérieure unique. L'objectif principal est de comprendre comment les effets de canal court influencent le transport de charge, la commutation ferroélectrique et la reconfigurabilité dans les FeFETs bidimensionnels (2D) à liaisons de van der Waals (vdW). Les dispositifs incorporent des couches exfoliées de WSe_2, hBN et CIPS, empilées à l'aide d'une méthode de transfert à sec. Les électrodes source-drain ont été définies par lithographie par faisceau d'électrons. La structure globale est représentée dans la Fig. 16.

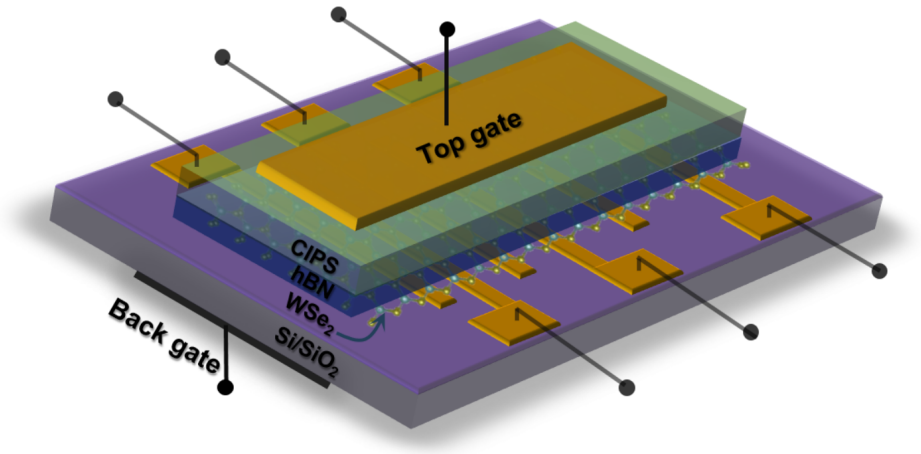


Figure 16: Schéma du FeFET avec différentes longueurs de canal.

Les mesures électriques démontrent un comportement ambipolaire clair avec des boucles de transconductance hystérétiques. Une hystérésis antihoraire est observée dans la branche n, tandis qu'une hystérésis horaire est observée dans la branche p, ce qui signifie des effets de polarisation ferroélectrique contrôlés par la grille. Comme montré dans la Fig. 17, les diagrammes de bandes clarifient l'accumulation d'électrons et de trous sous différentes tensions de grille, mettant en évidence l'impact des barrières de Schottky et de la grille ferroélectrique sur l'injection des porteurs.

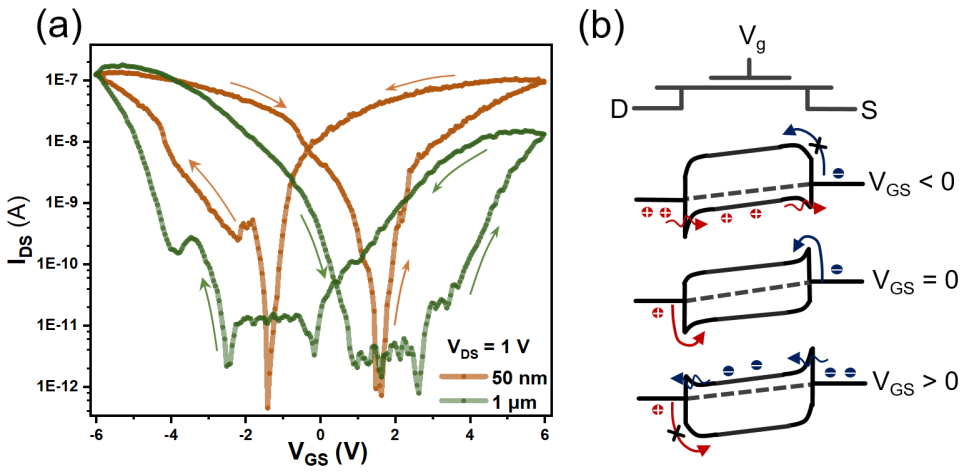


Figure 17: Boucle de transconductance du FeFET ambipolaire, montrant une hystérésis antihoraire dans la branche n et une hystérésis horaire dans la branche p pour les dispositifs à canal de 50 nm et 1µm. (b) Diagrammes de bandes illustrant l'accumulation d'électrons et de trous.

Résultats clés et enseignements :

- **Effets d'échelle :** Les dispositifs à canal plus court montrent une transconductance plus élevée en raison d'un effet tunnel accru et d'une largeur réduite de la barrière de Schottky.
- **Modulation par la tension de drain :** La tension de seuil (V_T) et la tension de commutation de la polarisation se décalent avec V_{DS}, permettant un réglage assisté par le drain.
- **Comportement de canal court :** Une réduction de barrière induite par le drain (DIBL) et une DIBL inversée sont observées, confirmant les effets de capacitance négative.
- **Performance en sous-seuil :** Le swing en sous-seuil (SS) descend en dessous de la limite thermionique de 60 mV/décade dans les dispositifs à canal court, confirmant un comportement de commutation efficace.
- **Reconfigurabilité :** Grâce à la programmation par la grille supérieure ferroélectrique et à la détection via la grille arrière, le dispositif peut commuter entre les modes de fonctionnement n-type, p-type et ambipolaire avec une excellente rétention.

8. Synapse ferroélectrique reconfigurable basée sur une hétérostructure de van der Waals

Ce chapitre présente la démonstration d'une synapse artificielle reconfigurable basée sur un transistor à effet de champ ferroélectrique (FeFET) en hétérostructure de van der Waals, utilisant une structure $CuInP_2S_6$ (CIPS)/hBN/WSe_2. Cette étude vise à reproduire la plasticité synaptique biologique par le contrôle électrique des états de polarisation ferroélectrique et l'exploitation du transport de charge ambipolaire dans le WSe_2. Cela permet un fonctionnement synaptique bimode (excitateur et inhibiteur) avec une modulation analogique des poids synaptiques.

Commutation des domaines ferroélectriques via étude PFM : La microscopie à force piézoréponse (PFM) a confirmé la ferroélectricité robuste à température ambiante ainsi qu'une commutation partielle des sous-domaines dans la couche de CIPS. Cette inversion partielle de polarisation constitue la base de la modulation contrôlable et réversible de la conductance du dispositif.

Cinétique de commutation et contrôle électrique : L'application d'impulsions de tension

de grille ajustées permet un contrôle précis du degré de commutation des domaines. Cela conduit à un réglage continu de la tension de seuil et de la conductance du canal, directement corrélé à la modulation analogique du poids synaptique.

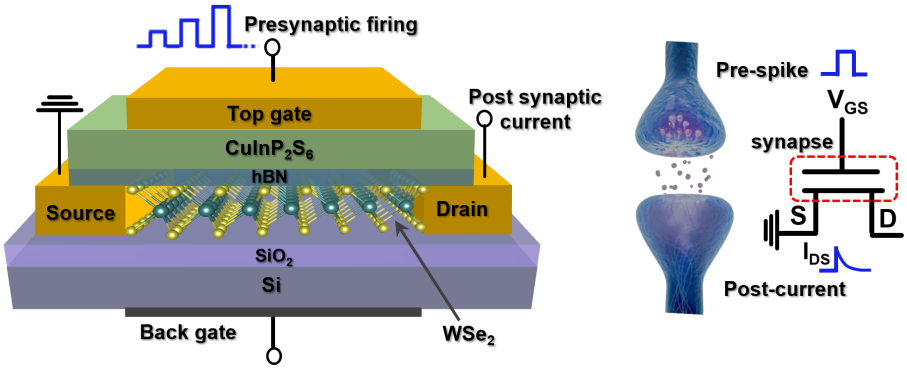


Figure 18: Schéma illustrant la synapse artificielle basée sur un FeFET. La polarisation ferroélectrique module la concentration de porteurs dans le canal de WSe_2, imitant les variations de poids synaptique biologiques.

Fonctionnalité synaptique reconfigurable : En raison du comportement ambipolaire du WSe_2, le même dispositif FeFET peut fonctionner comme une synapse excitatrice ou inhibitrice. Lorsqu'il est polarisé dans la région de type n, le dispositif montre une potentialisation à long terme (LTP) et une dépression (LTD) de type excitateur. En revanche, dans la région de type p, des caractéristiques synaptiques inhibitrices sont observées. Ces fonctionnalités ont été réalisées à l'aide de séquences d'impulsions en forme de croissant, permettant une modulation de conductance fluide et linéaire.

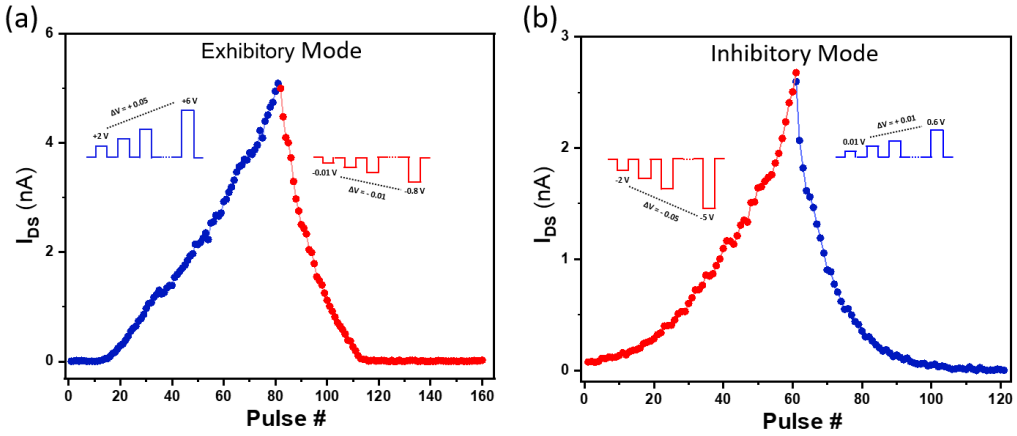


Figure 19: Modulation du poids synaptique à l'aide d'impulsions de tension en forme de croissant. (a) LTP et LTD en mode excitateur (branche n). (b) LTP et LTD en mode inhibiteur (branche p).

Simulation ANN et précision d'apprentissage : Le comportement synaptique analogique et bimode a été évalué dans un réseau de neurones artificiels (ANN) à trois couches effectuant une classification de chiffres manuscrits. Le réseau a atteint jusqu'à 90

En résumé, ce travail démontre une synapse FeFET analogique, reconfigurable électriquement et compatible avec l'intégration, présentant une plasticité inspirée du fonctionnement biologique. La capacité de commuter entre les modes excitateur et inhibiteur dans un seul dispositif ouvre la voie à un matériel neuromorphique écoénergétique de nouvelle génération.

9. Fonctionnalité logique et conception de circuits à base de FeS-FET en α-In_2Se_3

Ce chapitre présente la conception et la mise en œuvre d'un transistor à effet de champ ferroélectrique à semi-conducteur (FeS-FET) reconfigurable, utilisant le α-In_2Se_3 comme canal semi-conducteur ferroélectrique et le hBN comme diélectrique dans une architecture à grille divisée (split-gate). Cette configuration à double grille permet un contrôle indépendant de la polarisation ferroélectrique, rendant possible l'intégration de fonctions logiques programmables et de mémoire dans un seul dispositif.

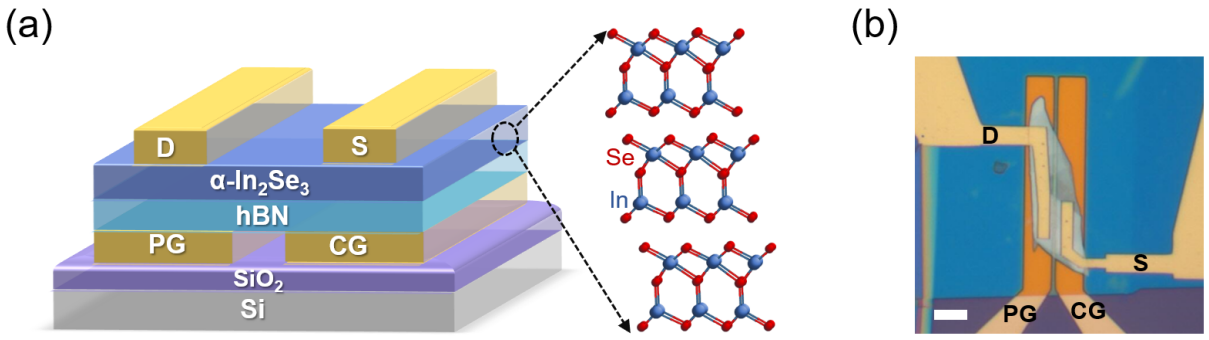


Figure 20: (a) Schéma du transistor à effet de champ à semi-conducteur ferroélectrique (FeS-FET). (b) Image au microscope optique du dispositif fabriqué (barre d'échelle de 5 μm).

Le FeS-FET utilise une hétérostructure hBN/α-In_2Se_3, où le hBN sert de diélectrique et le α-In_2Se_3 constitue le canal semi-conducteur.

Ce dispositif présente des signatures caractéristiques de la ferroelectricité à travers des mesures électriques. Les caractéristiques de transfert mesurées à $V_{DS} = -1$ V montrent une hystérésis marquée dans le sens horaire lorsque les deux grilles sont balayées simultanément, indiquant une polarisation ferroélectrique hors plan et un basculement partiel des domaines en raison

d'une épaisseur équivalente d'oxyde (EOT) élevée. De plus, les courbes I_{DS}-V_{DS} à polarisation de grille fixe ($V_{PG} = V_{CG} = 3$ V) révèlent une hystérésis antihoraire attribuée au basculement de la polarisation dans le plan. Les diagrammes de bandes montrent que l'hystérésis observée résulte d'un basculement localisé et de la modulation de la barrière de Schottky aux contacts.

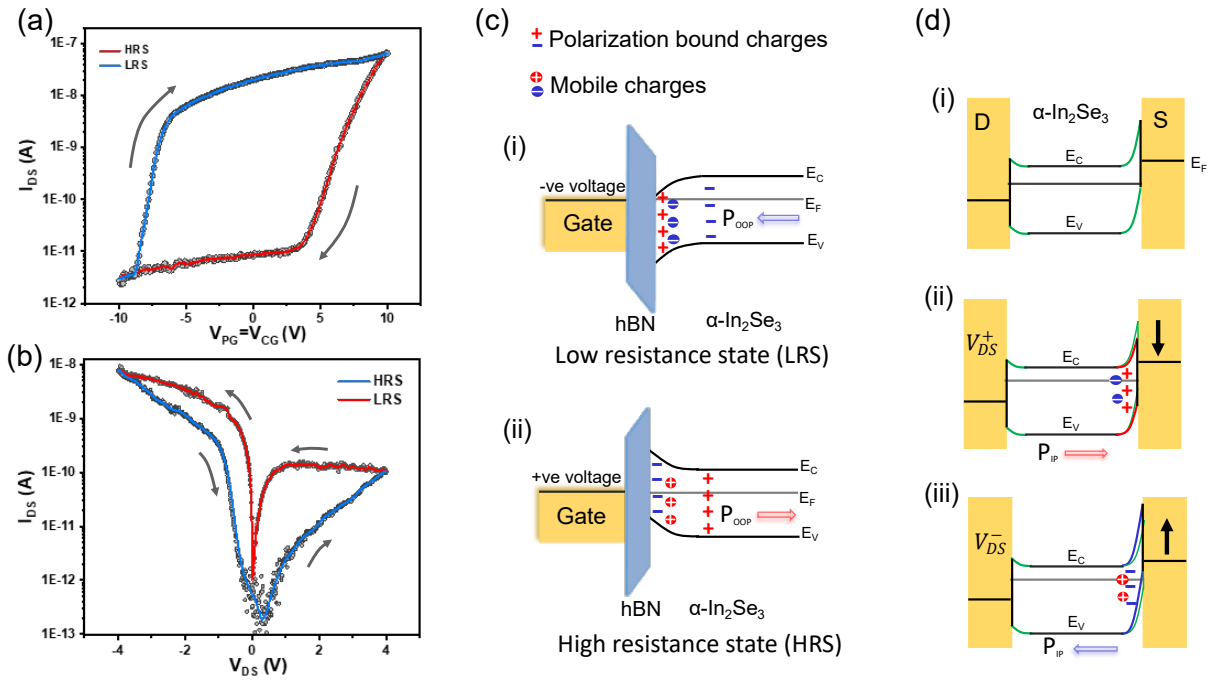


Figure 21: (a) Caractéristique de transfert du FeS-FET à $V_{DS} = -1$ V avec balayage simultané des deux grilles, montrant une hystérésis dans le sens horaire. (b) Caractéristique I_{DS}-V_{DS} sous $V_{PG} = V_{CG} = 3$ V, révélant un basculement de polarisation dans le plan. (c) Diagrammes de bandes sous tensions de grille négatives et positives montrant un basculement partiel de la polarisation dans un régime de forte EOT. (d) Effet du basculement dans le plan sur la barrière de Schottky, menant à des états de résistance faible et élevée distincts.

Fonctionnalités du dispositif démontrées :

- **Portes logiques volatiles :** La conception à grille divisée permet la réalisation d'une logique NAND lorsqu'elle est utilisée avec une charge passive, fournissant une fonctionnalité booléenne via les états de polarisation contrôlés par les grilles.
- **Logique ferroélectrique reconfigurable :** Le dispositif peut être programmé comme une porte logique Fe-NAND ou Fe-NOR non volatile en ajustant la polarisation ferroélectrique via la tension de grille.
- **Comportement logique multiniveau :** Le contrôle à double grille permet d'accéder

à plusieurs états de conductance stables, essentiel pour une logique multi-bits.

- **Opération par décalage de la tension de seuil :** Les états de polarisation programmables modifient la tension de seuil du canal, permettant un réglage dynamique et un comportement de circuit adaptatif.

10. Conclusion et Perspectives d'Avenir

Au cours de cette thèse, les transistors à effet de champ ferroélectriques à base de matériaux de van der Waals (FeFETs) ont été étudiés pour leur multifonctionnalité dans l'électronique reconfigurable, la logique et le calcul neuromorphique. Des Re-FeFETs à grilles divisées basés sur l'hétérostructure $\mathrm{CuInP_2S_6/WSe_2}$ ont permis un contrôle dynamique du type de porteurs et des fonctions logiques, rendant possible l'implémentation de portes logiques Fe-NAND, Fe-AND et XNOR avec un nombre réduit de dispositifs. Le passage à des longueurs de canal de 50 nm a révélé une pente sous-seuil inférieure à la limite thermique et un dopage modulable via une grille flottante ferroélectrique. Ces dispositifs ont également été utilisés comme synapses artificielles, présentant une plasticité excitatrice et inhibitrice, avec une précision allant jusqu'à 90% dans les simulations de réseaux de neurones. En outre, des FeFETs basés sur α-$\mathrm{In_2Se_3}$ ont été démontrés pour une logique reconfigurable multiniveau.

Perspectives d'Avenir

Les axes prioritaires pour le développement futur des FeFETs à base de matériaux de van der Waals incluent :

- **Couches ferroélectriques plus fines :** Réduction de l'épaisseur du $\mathrm{CuInP_2S_6}$ afin d'améliorer la capacité, la vitesse de commutation et la compacité des dispositifs.
- **Nouveaux systèmes de matériaux :** Exploration de ferroélectriques de glissement et de semi-conducteurs ambipolaires comme $\mathrm{MoTe_2}$ ou le phosphore noir pour une meilleure polyvalence.
- **Calcul neuromorphique :** Développement de synapses et de neurones à base de FeFET en exploitant la dynamique des domaines pour un apprentissage et un traitement des signaux à faible consommation.

Thesis Overview

This thesis presents the potential of emerging ferroelectric devices based on van der Waals materials and explores their applications in reconfigurable electronics, neuromorphic computing, and logic-in-memory architectures. The thesis is divided into three parts:

- **Part I:** Introduces CMOS scaling, its limitations, and beyond-CMOS technologies while covering fundamental principles, device concepts, and ferroelectric integration in nanoelectronics.
- **Part II:** Details experimental work, including fabrication, characterization, and novel device architectures, followed by an in-depth analysis of key results and their practical applications.
- **Part III:** Concludes the key findings and discusses future perspectives.

Part I: Background and Motivation

The first part of the thesis addresses the limitations of traditional CMOS scaling and the need for alternative electronic technologies. It discusses the state-of-the-art materials and device architectures, along with the theoretical background for emerging devices.

Chapter 1: CMOS Scaling and Evolution

Traces the historical evolution of CMOS scaling, discussing Moore's Law, the transition from More Moore to More-than-Moore, and innovations in device architectures.

Chapter 2: Emerging Technology beyond CMOS

Highlights the potential of reconfigurable electronics and ferroelectric materials, emphasizing their unique properties and integration with 2D materials for advanced memory and logic applications.

Chapter 3: 2D Materials and Their Electronic Properties

Introduces the electronic properties of key 2D materials used in this work, including hexagonal boron nitride (hBN), tungsten diselenide (WSe_2), copper indium thiophosphate ($CuInP_2S_6$), and indium selenide (In_2Se_3), emphasizing their dielectric, semiconducting, and ferroelectric properties.

Chapter 4: Fundamental Principles and Device Concepts

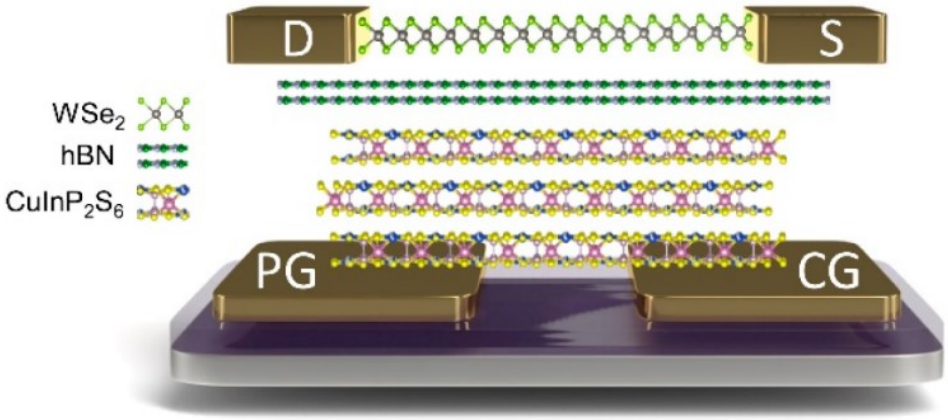
Covers the fundamental principles of field-effect transistors (FETs), including conventional MOSFETs, ferroelectric FETs (FeFETs), negative capacitance FETs (NCFETs), ferroelctric-semiconductor FETs (FeSFET) and synaptic devices, which form the foundation of the experimental work presented in this thesis.

Part II: Experimental Work and Results

Chapter 5: Device Fabrication and Characterization Techniques

This chapter outlines the methodologies used for fabricating ferroelectric devices, along with key characterization techniques essential for evaluating their properties and performance.

Chapter 6: Reconfigurable Multifunctional van der Waals Ferroelectric Devices and Logic Circuits

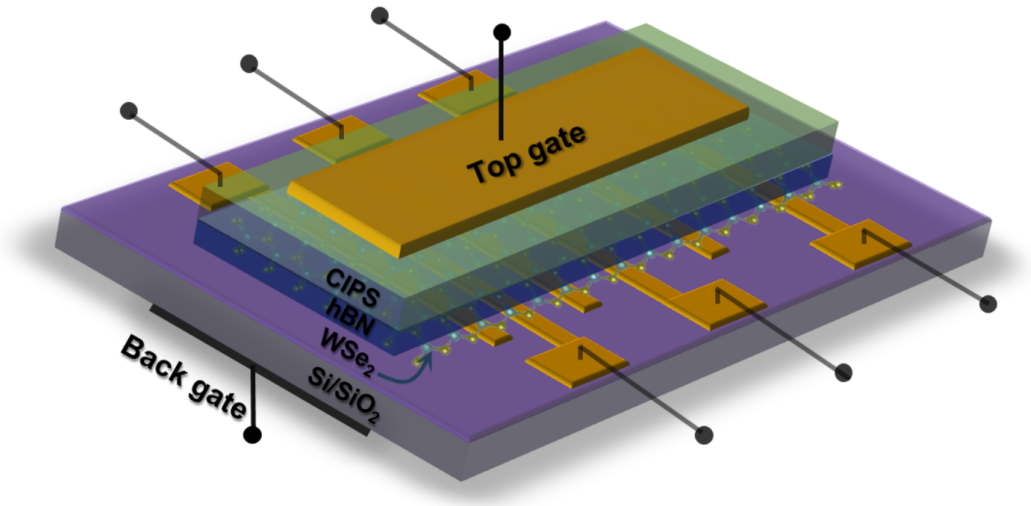


Device architecture: Reconfigurable Ferroelectric Field-Effect Transistors (Re-FeFETs) based on a $CuInP_2S_6$/hBN/WSe_2 van der Waals heterostructure with a split-gate configuration.

This chapter explores the development of a reconfigurable ferroelectric field-effect transistor (Re-FeFET) based on a van der Waals heterostructure, integrating a ferroelectric gate insulator ($CuInP_2S_6$), a dielectric layer (hBN), and a semiconducting channel (WSe_2). The split-gate architecture provides precise electrostatic control over the charge transport, enabling seamless reconfigurability between p-type, n-type, and ambipolar operation. Optoelectronic characterization reveals robust photo-transport properties, highlighting the potential of the device in diode-mode applications.

Additionally, the multifunctionality of the Re-FeFET is demonstrated through its ability to implement both electronic and ferroelectric logic operations. Circuit-level simulations further validate its efficiency, showing a significant reduction in transistor count, up to 80% compared to conventional CMOS technology. These findings suggest that Re-FeFET-based circuits reduce the complexity of integrated circuits and offer an energy-efficient alternative for future electronic systems.

Chapter 7: Scaling Effects in $CuInP_2S_6/WSe_2$-Based van der Waals FeFETs

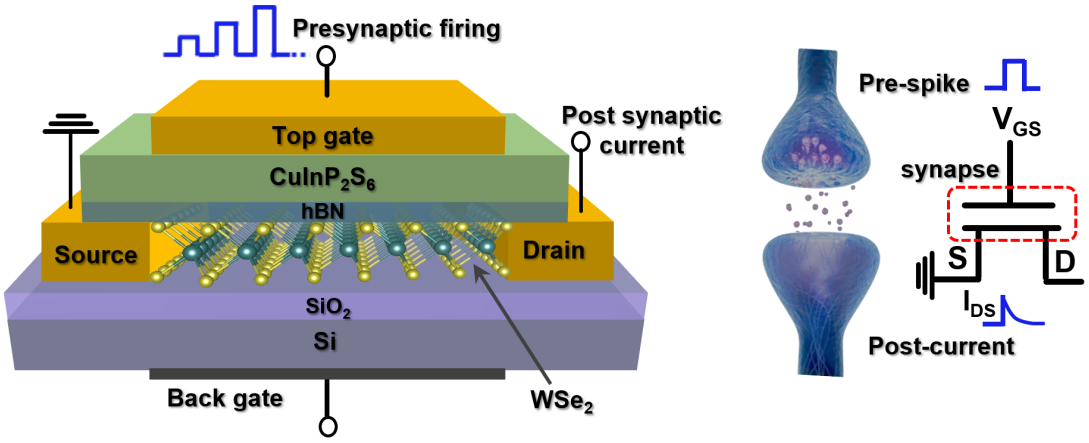


Device architecture: Similar to the previous configuration, but with a varying channel length ranging from 50 nm to 1 µm and with a single top-gate.

This chapter examines the influence of channel length scaling on the performance of ferroelectric field-effect transistors (FeFETs), with device fabrication spanning a range of nanoscale dimensions. The study explores key short-channel effects, including drain-induced barrier lowering (DIBL) and reverse DIBL, while also highlighting the role of negative capacitance in enhancing energy efficiency. Subthreshold swing (SS) analysis across different channel lengths

provides insights into the device switching characteristics at reduced dimensions. Furthermore, the integration of a ferroelectric floating top gate and a back gate enables dynamic reconfigurability, allowing precise modulation of doping states and seamless transitions between different operational modes. These findings contribute to a deeper understanding of FeFET behavior in nanoscale electronics and their potential for energy-efficient, reconfigurable device applications.

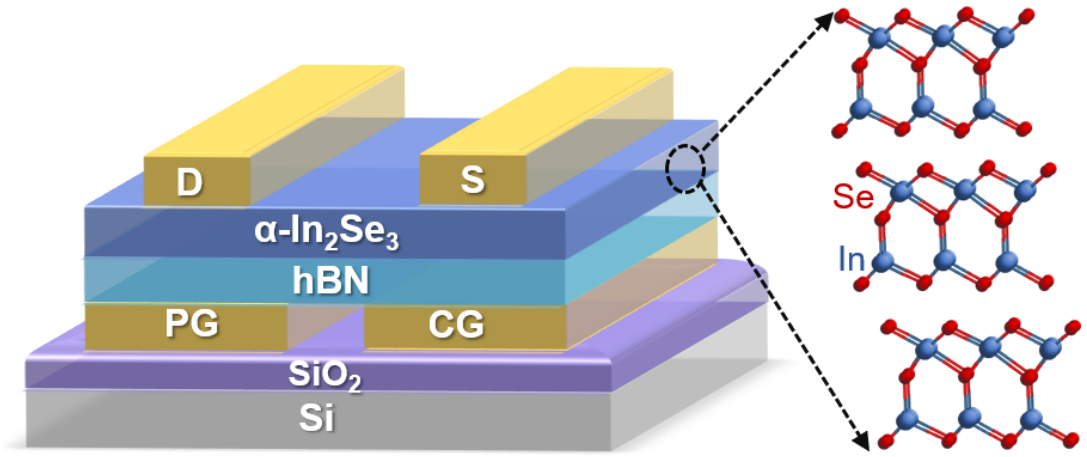
Chapter 8: Reconfigurable Excitatory/Inhibitory Ferroelectric Synapse Based on van der Waals Heterostructures



Device architecture: Same configuration as described in Chapter 7.

This chapter explores the reconfigurable neuromorphic potential of FeFETs, focusing on their performance in nanoscale devices. Piezoresponse force microscopy (PFM) studies reveal that multidomain ferroelectric polarization tuning directly modulates channel conductance, enabling synaptic weight adjustment. By applying carefully designed voltage pulse schemes, the device achieves continuous and reversible conductance tuning, mimicking biological synapses. The ambipolar nature of the WSe_2 semiconducting channel allows the device to reconfigure between excitatory and inhibitory synaptic functionalities, enhancing its adaptability for neuromorphic computing. Artificial neural network (ANN) simulations further validate its effectiveness, demonstrating high accuracy in pattern recognition tasks and underscoring its potential for highly adaptive and low-power neural processing units.

Chapter 9: Logic Functionality and Circuit Design of α-In_2Se_3-Based Ferroelectric Field-Effect Transistor

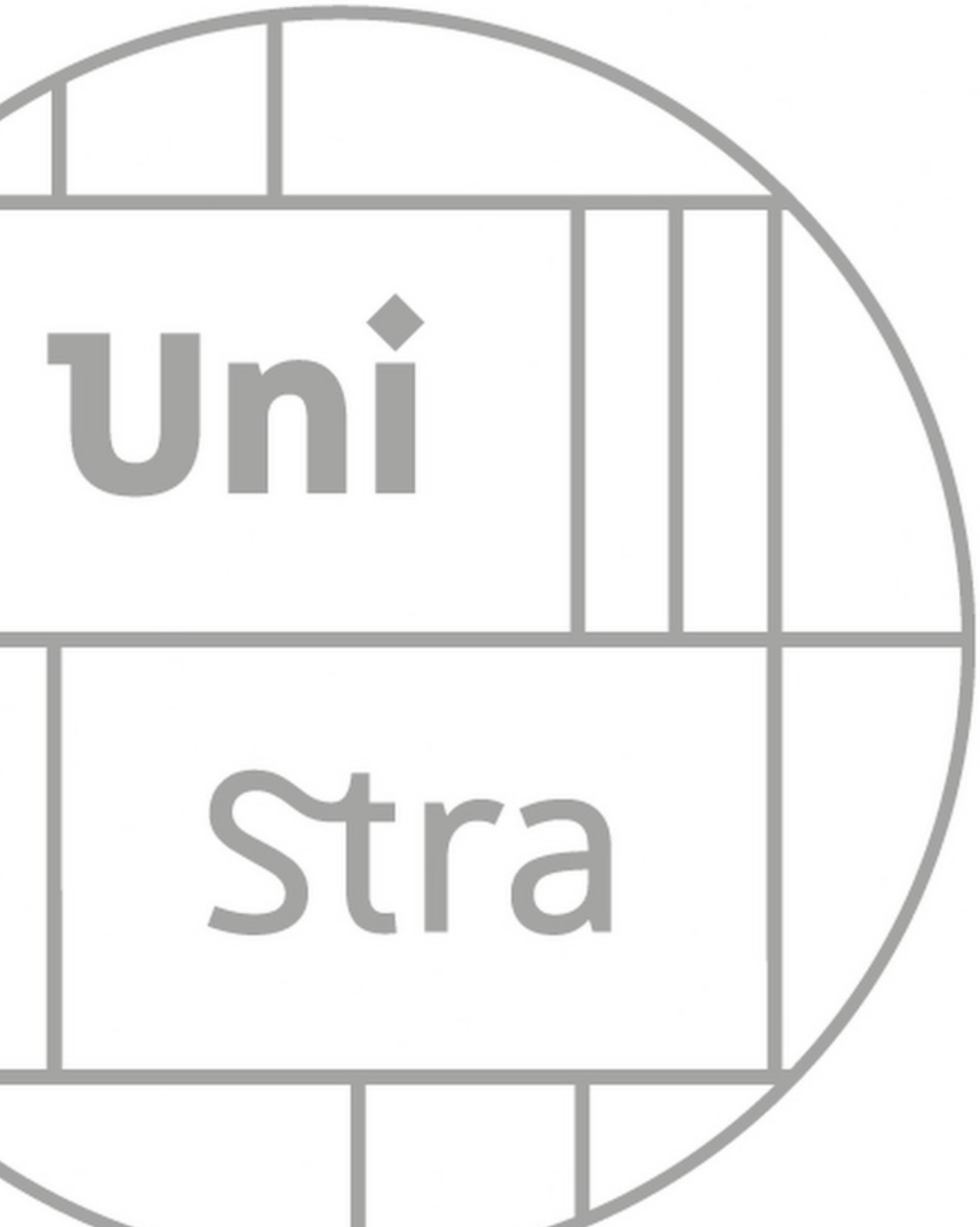


Device architecture: Split-gate FeS-FET with a ferroelectric semiconductor layer.

This chapter presents the development of a split-gate ferroelectric semiconductor field-effect transistor (FeS-FET) based on a van der Waals heterostructure, incorporating $\alpha - In_2Se_3$ as the ferroelectric semiconducting channel and hBN as the dielectric spacer. The dual-gate architecture enables independent control of ferroelectric polarization states, enabling the realization of reconfigurable logic elements. The device exhibits multilevel logic operations and threshold voltage tunability, underscoring its versatility in programmable electronics. Circuit simulations further confirm that two FeS-FETs connected in parallel can be configured to implement all fundamental logic functions, highlighting its potential for reconfigurable logic circuits.

Part III: Conclusion and Perspectives

This chapter summarizes the key findings of the thesis, highlighting its contributions to the advancement of next-generation electronics. It also discusses future perspectives, including potential improvements in device design, material exploration, and emerging applications, opening new possibilities for reconfigurable and high-performance electronic technologies.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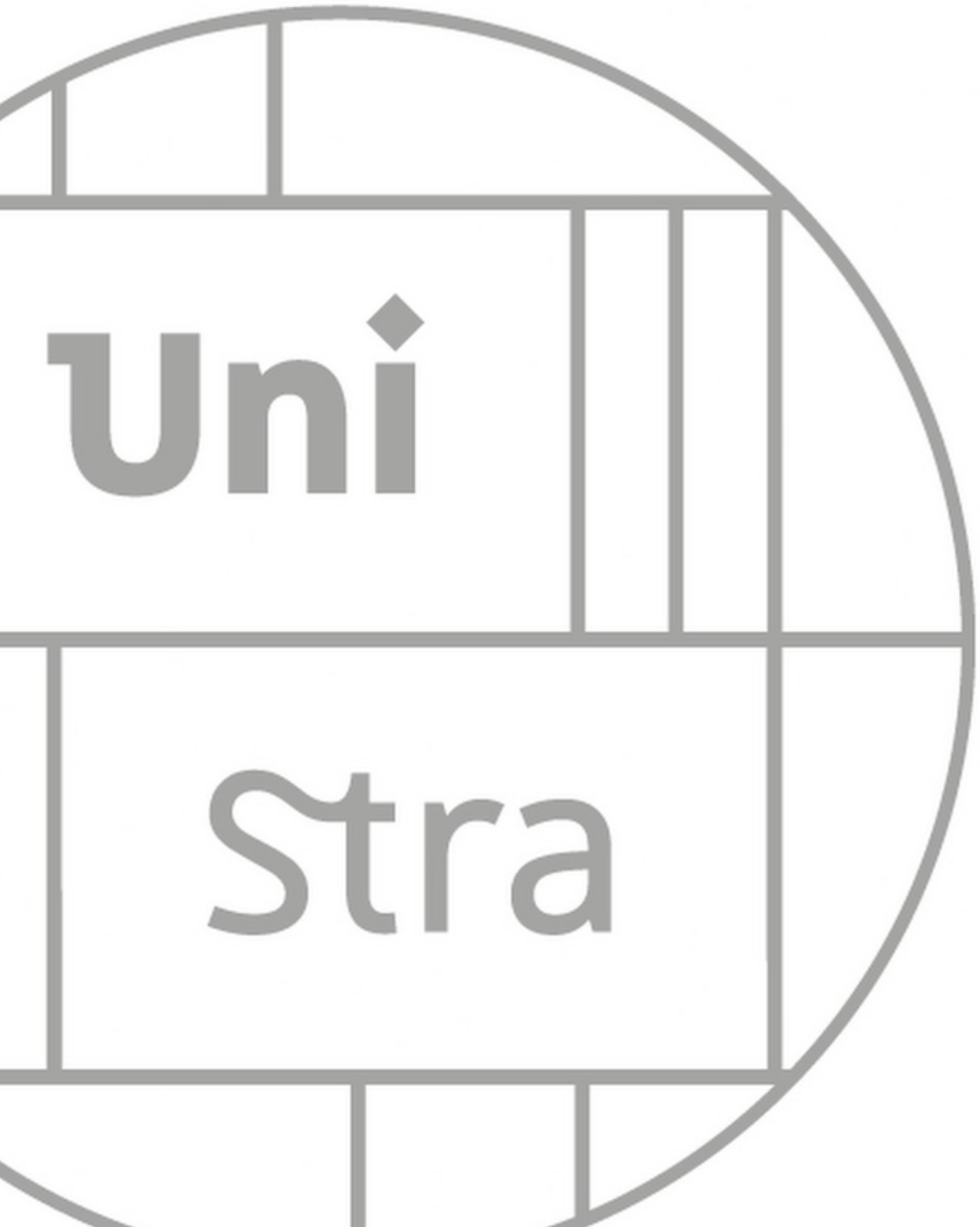
Part I

Background and Motivation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1 | CMOS Scaling and Evolution

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1.1. Historical Context of CMOS Scaling

The invention of the transistor in 1947 [1] by John Bardeen, Walter Brattain, and William Shockley at Bell labs marked the beginning of modern electronics. This tiny device transformed how electrical signals were amplified and switched, replacing bulky vacuum tubes and revolutionizing the field. By 1959, Jack Kilby and Robert Noyce introduced the first monolithic integrated circuit (IC), allowing multiple transistors to be fabricated on a single chip [2]. This breakthrough laid the foundation for the development of the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), which became the heart of modern computing [3].

The introduction of Complementary Metal-Oxide-Semiconductor (CMOS) technology in the 1970s was another key milestone [4]. CMOS enabled millions of transistors to be integrated onto a single chip while consuming minimal power. This advancement fueled the rapid growth of the semiconductor industry, leading to innovations in computing, communication, and everyday electronics.

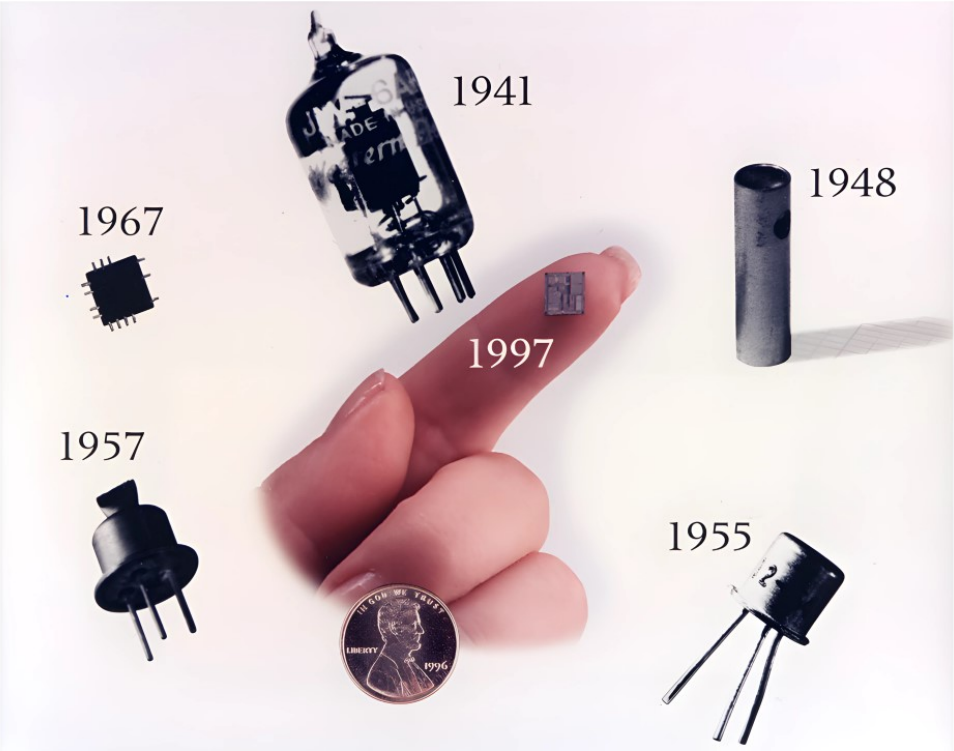


Figure 1.1: Evolution of the transistor from vacuum tubes to modern digital signal processors [5].

Over time, transistors have evolved significantly in size and function. Initially, vacuum tubes facilitated telephone communication, but they were soon replaced by point-contact transistors

in 1948 [6]. As technology progressed, transistors became smaller, faster, and more efficient, culminating in modern digital signal processor chips that contain millions of transistors and power today's communication devices.

1.2. Evolution of CMOS Scaling

1.2.1. Moore's Law and the Path to Miniaturization

In 1965, Gordon Moore, co-founder of Intel, noticed a trend that transistor density on an integrated circuit was doubling roughly every two years [4]. This observation, now known as Moore's Law, became a guiding principle for technological progress in the semiconductor industry.

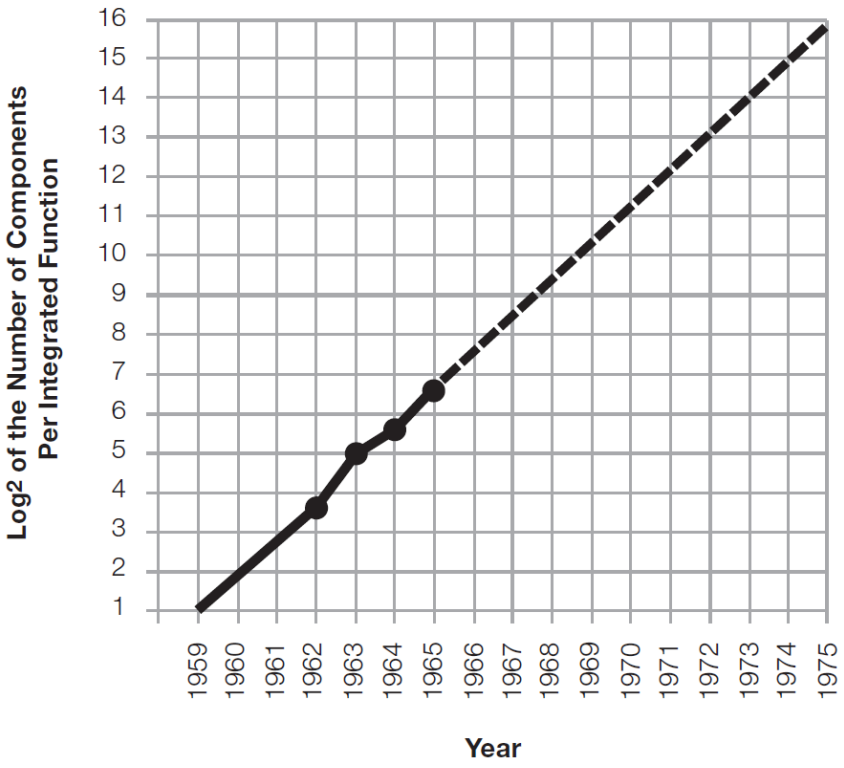


Figure 1.2: Original adapted graph of Moore's Law, showing the exponential growth in the number of components per integrated function over time [7].

The success of Moore's Law was closely tied to Dennard Scaling, introduced in 1974, which proposed that as transistors shrink in size, power density remains constant while operating speeds increase [8]. This allowed for the continued improvement of computational power without significant increases in power consumption. However, by the early 2000s, physical

limitations emerged, including increased leakage currents, excessive heat generation, and diminishing performance gains [9]. These issues led to the so-called power wall, where simply adding more transistors no longer resulted in proportional performance improvements [10].

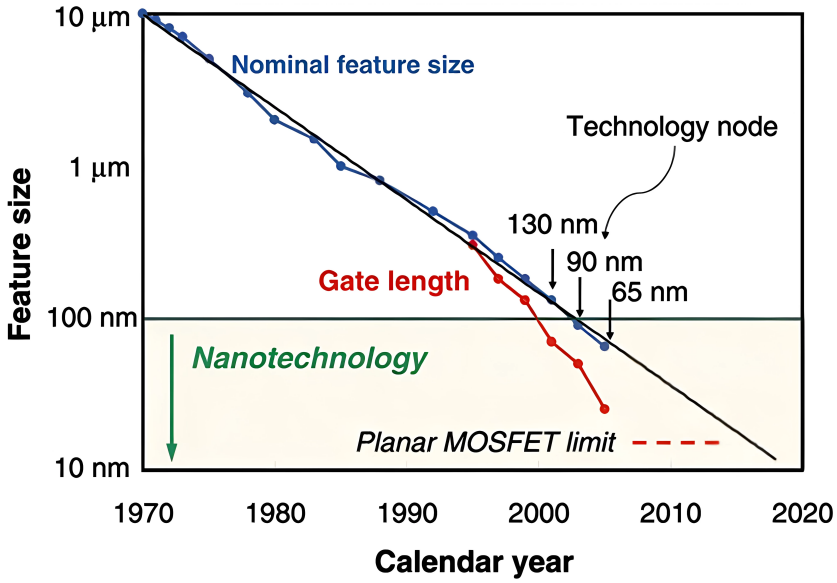


Figure 1.3: The curve of transistor gate length versus the calendar year [11].

As depicted in Figure 1.3, the miniaturization of MOSFET gate lengths has followed a steady trajectory, with transistors reaching the nanometer scale [12] around the year 2000. By the 0.13-µm technology node, the industry had successfully incorporated transistors with gate lengths of approximately 70 nm . This aggressive scaling enabled higher performance and energy efficiency, driving the continuous evolution of microprocessors and memory devices.

1.2.2. Transition from More Moore to More-than-Moore

As transistors approached atomic-scale limitations, the semiconductor industry began shifting its focus from pure miniaturization (More Moore) [13, 14] to functional diversification (More-than-Moore) [15]. This transition involved integrating new materials, heterogeneous architectures, and multifunctional components to overcome the physical barriers of conventional scaling.

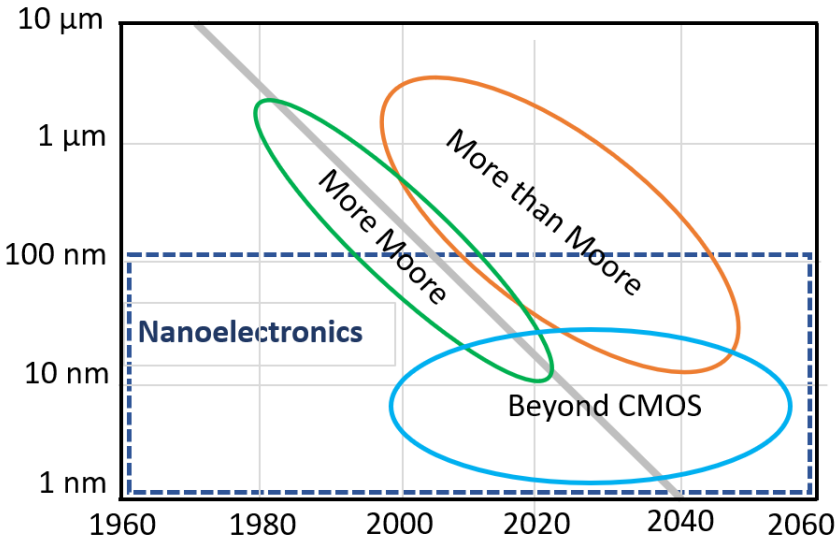


Figure 1.4: Nanoelectronics roadmap.

Figure 1.4 illustrates the evolution of transistor technology from micrometer-scale to nanometer-scale nodes. As transistors approach sub-3nm dimensions, quantum mechanical effects become increasingly dominant, requiring novel solutions beyond traditional CMOS technology.

1.2.3. Innovations in Architectures and Materials

In order to sustain progress in semiconductor technology, researchers have focused on advancements in device architectures and materials. Architectural innovations include FinFETs [16, 17], which are three-dimensional transistors that improve control over current flow, enhancing performance and efficiency [18]. Gate-All-Around (GAA) transistors[19] provide even better electrostatic control compared to FinFETs, reducing leakage currents and power consumption. 3D stacking technologies enable increased transistor density without requiring smaller nodes, improving data transfer rates and reducing latency. New interconnect technologies utilize advanced materials to reduce resistance and power loss, enhancing overall system performance.

The introduction of high-k materials, such as hafnium-based compounds, improved the ability to control leakage and enabled further transistor miniaturization while maintaining efficiency [20].

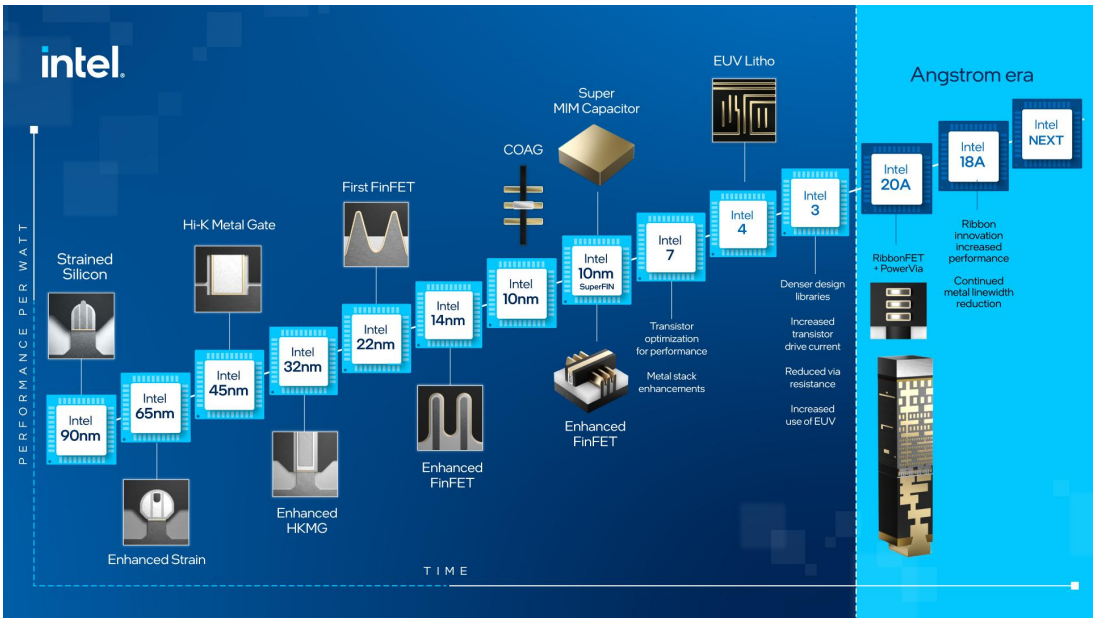


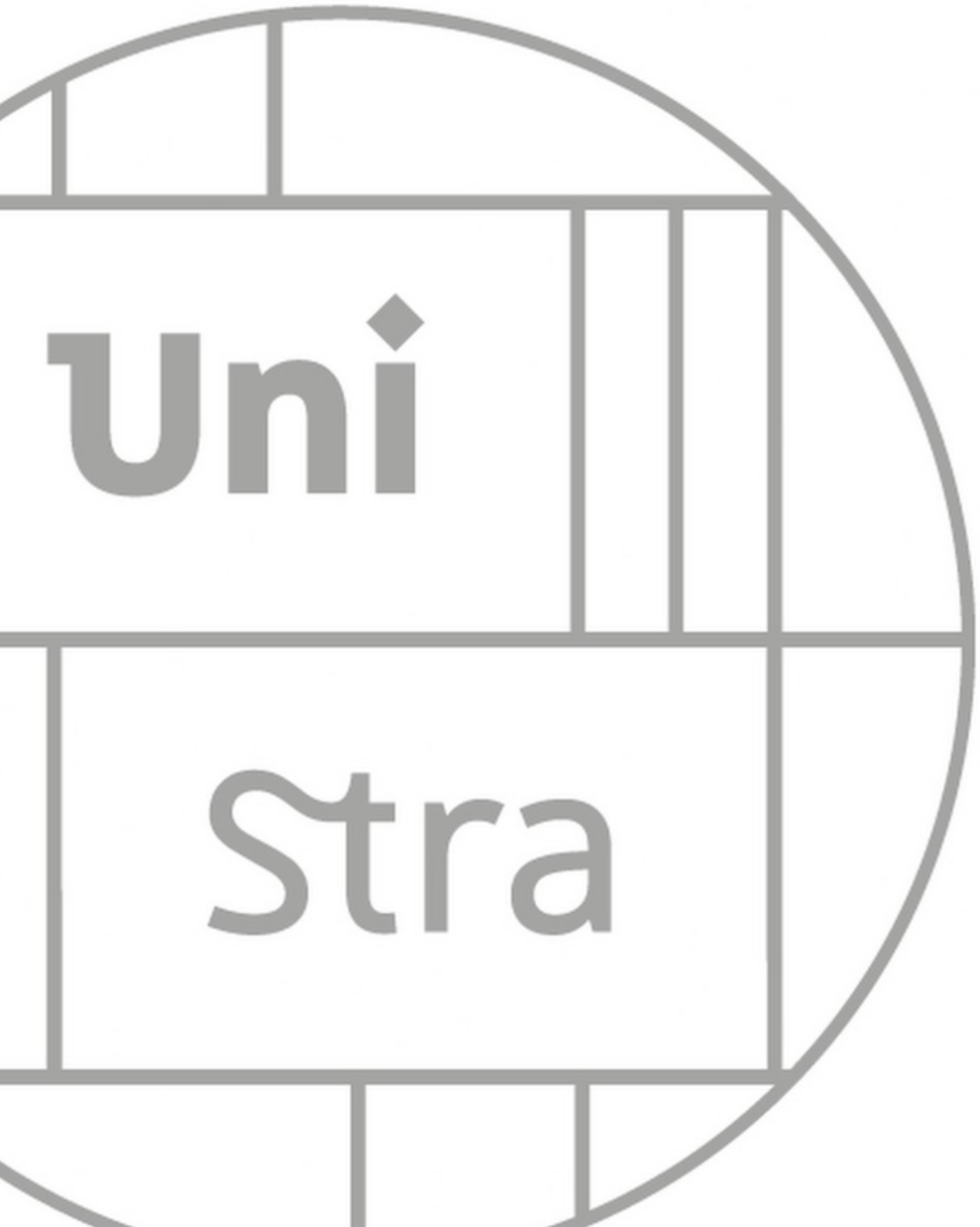
Figure 1.5: Advances in Intel Chip, showing continuous innovations in transistor design [21].

Conclusion

The evolution of CMOS scaling [22] has been a journey of continuous innovation, from early transistors to today's nanometer-scale devices. While Moore's Law has driven technological progress for decades, fundamental physical and material limits are making further miniaturization increasingly difficult. As a result, the industry is transitioning from a focus on reducing transistor size (More Moore) to exploring new materials, architectures, and functionalities (More-than-Moore). Technologies like FinFETs, gate-all-around transistors, and 3D stacking have pushed CMOS to its limits, prompting researchers to find alternative paths for continued advancement.

One more challenge in computing today is the memory bottleneck—processors have advanced at a much faster pace than memory, leading to inefficiencies. Researchers are now exploring new paradigms such as compute-in-memory architectures to bridge this gap and improve performance.

In the next chapter, I will talk about cutting-edge approaches that extend beyond traditional CMOS scaling. These include 2D semiconductors, 2D ferroelectric materials, and reconfigurable electronics, which hold great potential for the future of semiconductor technology. Along with emerging fields such as neuromorphic computing and beyond-CMOS [23, 24] innovations, these advancements will define the next era of computing, ensuring sustained improvements in performance, energy efficiency, and adaptability.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2 | Emerging Technology Beyond CMOS

In this chapter, I provide an overview of two emerging technologies that are gaining attention as alternatives to conventional CMOS: reconfigurable electronics and ferroelectronics. These technologies offer new functionalities, such as dynamic control over device behavior and non-volatile switching, which are valuable for building energy-efficient and versatile electronic systems. Rather than going into full technical depth, this chapter aims to highlight the core principle and motivations behind these concepts, which serve as the basis for the device strategies developed in my PhD research.

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2.2 Ferroelectronics 52

2.2.1 Ferroelectric Materials and 2D Electronics 52

2.2.2 Classification and Applications of 2D Ferroelectrics 53

2.2.3 2D Ferroelectric Transistor Architectures 54

2.1. Reconfigurable Electronics

Reconfigurable electronics [25] is a rapidly evolving field that introduces new possibilities for the design and functionality of electronic devices. Unlike traditional CMOS (complementary metal-oxide-semiconductor) technology, which relies on fixed doping during fabrication to determine the behavior of transistors, reconfigurable electronics [26] offers flexibility. Devices in this category can dynamically switch between operational modes, such as n-type and p-type configurations, through electrical inputs. This adaptability not only reduces the need for separate components but also optimizes space, energy, and functionality, addressing many limitations of traditional CMOS systems as they approach their physical and practical scaling limits. This section is adapted from Fei et al. (2022) [26] and Wu et al. (2021) [27].

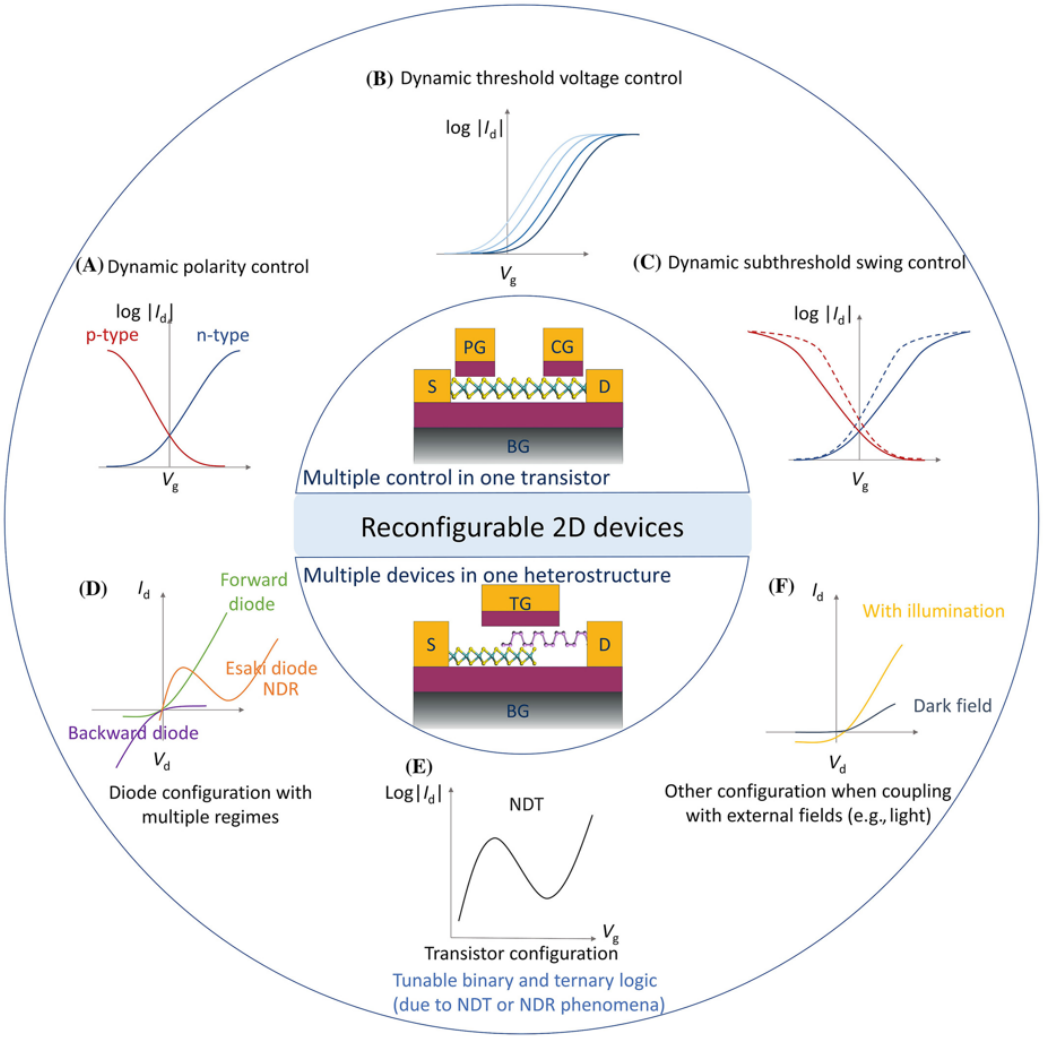

Figure 2.1: Dynamic operation modes in 2D reconfigurable devices enabled by electrostatic gating [26].

Fig. 2.1 highlights the versatility of 2D-material-based reconfigurable devices, which operate under different modes through precise electrostatic control. These modes include carrier polarity switching (n-type to p-type), threshold voltage tuning, and multifunctional operation. For instance, a single device can be configured to act as a transistor, diode, or optoelectronic device depending on the applied gate voltage. This reconfigurability is enabled by the unique properties of 2D materials [28], such as their atomic-scale thickness and high sensitivity to electric fields.

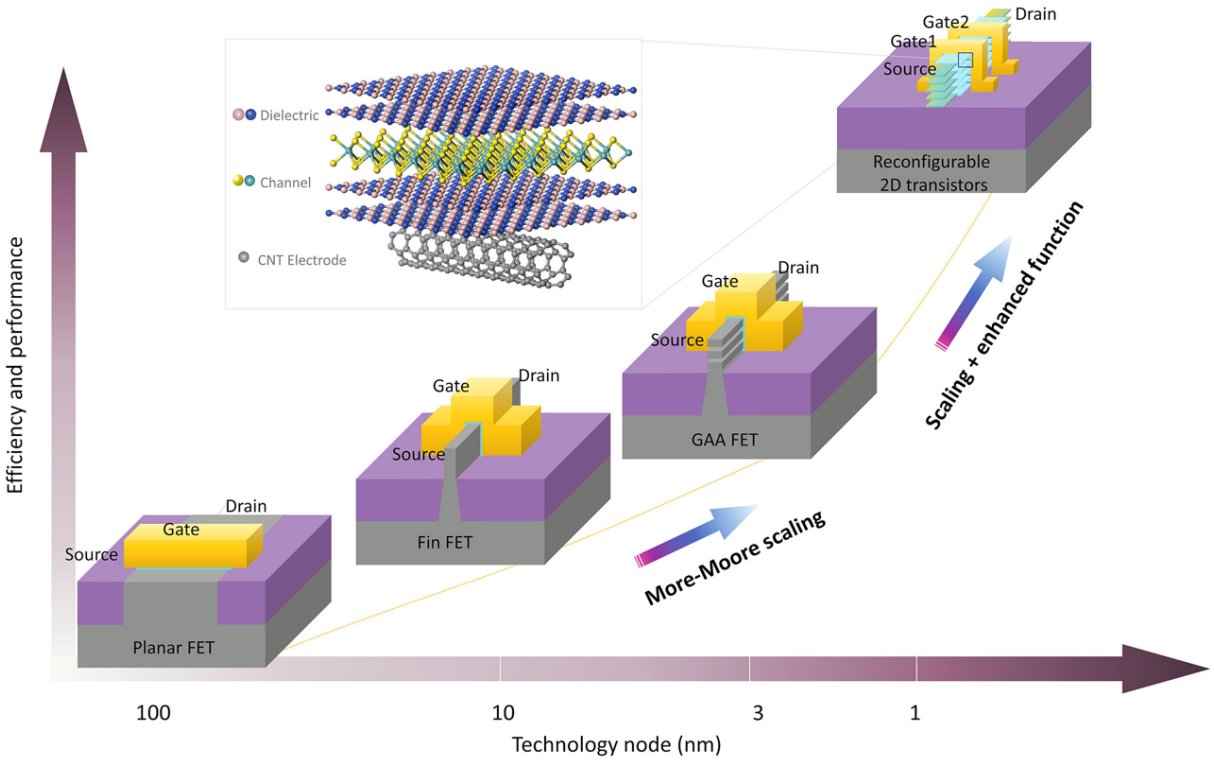

Figure 2.2: Progression of transistor scaling and the transformative potential of reconfigurable electronics with 2D materials [26].

Fig. 2.2 depicts the evolution of transistor technology from planar structures to non-planar designs like FinFETs and gate-all-around (GAA) transistors. These advancements aim to mitigate short-channel effects and improve electrostatic control. However, further scaling is becoming increasingly challenging due to rising costs, fabrication complexities, and diminishing performance gains. Reconfigurable devices built on 2D materials [29] provide a breakthrough in this context. These devices not only scale to atomic dimensions but also enhance device functionality through dynamic reconfiguration.

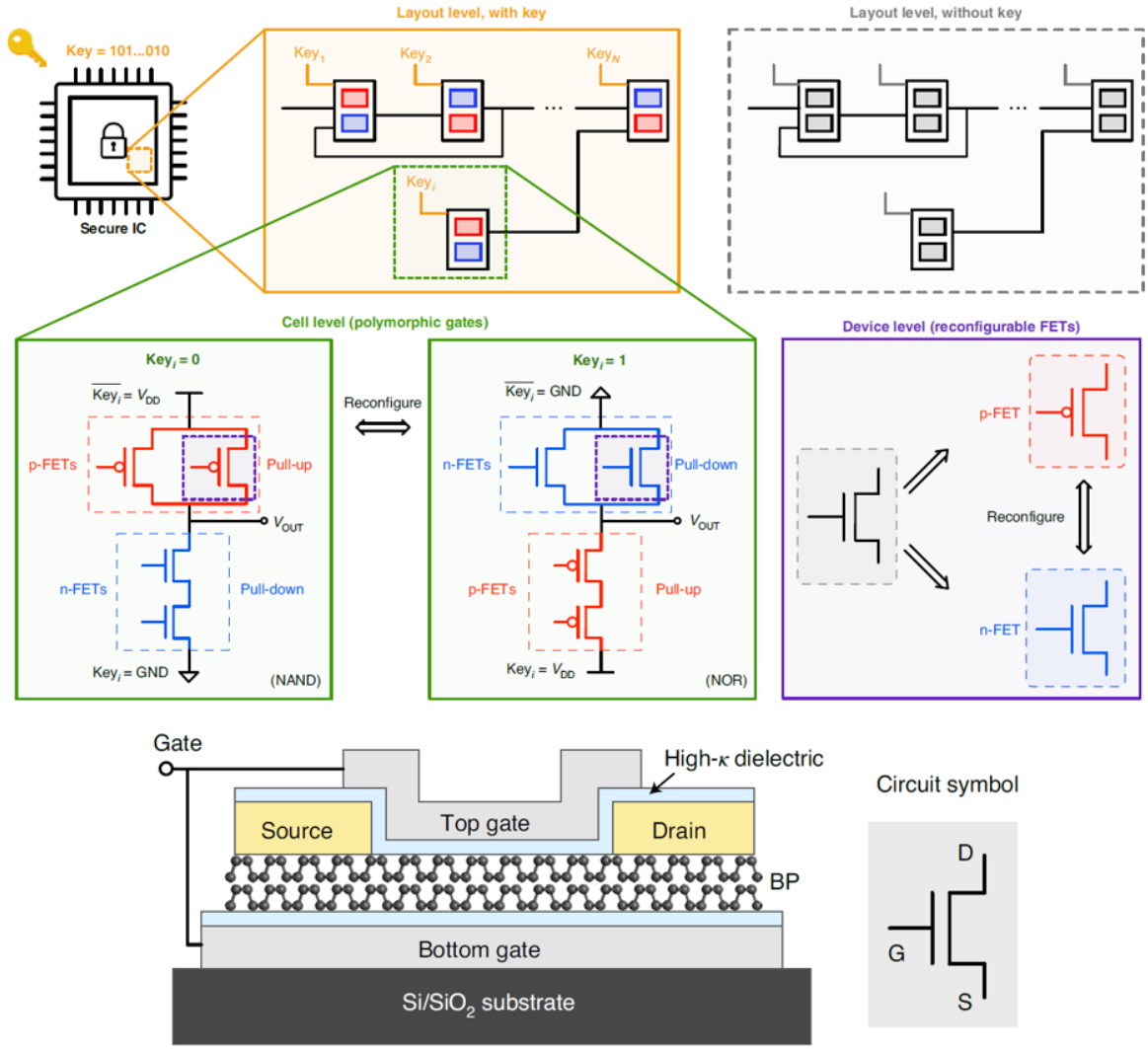

Figure 2.3: Secure chip architecture using polymorphic gates enabled by reconfigurable FETs with a double-gated black phosphorus-based structures [27].

One important application of reconfigurable electronics [26] is in hardware security [27]. By using transistors with reconfigurable polarity, techniques like logic locking and IC camouflaging [30] can be implemented more effectively. This is enabled by polymorphic logic gates, which can switch between different logic functions, such as NAND and NOR, based on control signals or key inputs, allowing the same circuit to behave differently under different conditions.

As shown in Fig. 2.3, a secure chip architecture is built using these polymorphic gates, powered by reconfigurable double-gate black phosphorus-based FETs. The logic function of each gate is controlled by a secret key, which biases the device to operate as either p-type or n-type. This allows the same circuit layout to implement different logic, making the design resilient against reverse engineering and unauthorized access.

2.2. Ferroelectronics

This section is adapted from Jin et al. (2022) [31].

Ferroelectric materials have the unique property of spontaneous electric polarization, which can be reversed by an external electric field. This makes them highly useful for applications such as non-volatile memory, energy-efficient transistors, and neuromorphic computing [32]. Unlike traditional dielectrics, ferroelectrics exhibit a hysteresis loop in their polarization-electric field (P-E) characteristics, meaning they can retain their polarization state without continuous power, making them ideal for low-power electronics.

With the advancement of two-dimensional (2D) ferroelectric materials, these materials are now being integrated into ultra-scaled electronic devices. Their atomically thin structure enables high tunability, compatibility with modern electronic architectures, and enhanced performance in 2D Ferroelectric Field-Effect Transistors (Ferro-FETs). These transistors provide improved gate control, non-volatile switching, and lower power consumption, making them highly promising for next-generation electronics [33].

2.2.1. Ferroelectric Materials and 2D Electronics

Ferroelectrics are being actively explored for integration with 2D materials, such as transition metal dichalcogenides (TMDs) and black phosphorus, to develop advanced electronic devices. Fig. 2.4 illustrates how ferroelectrics combined with 2D materials contribute to 2D electronics. Left part shows a ferroelectric hysteresis loop, demonstrating their ability to retain polarization states. The central part highlights various 2D materials, and the right section presents 2D electronic structures, where these materials are integrated to form high-performance transistors.

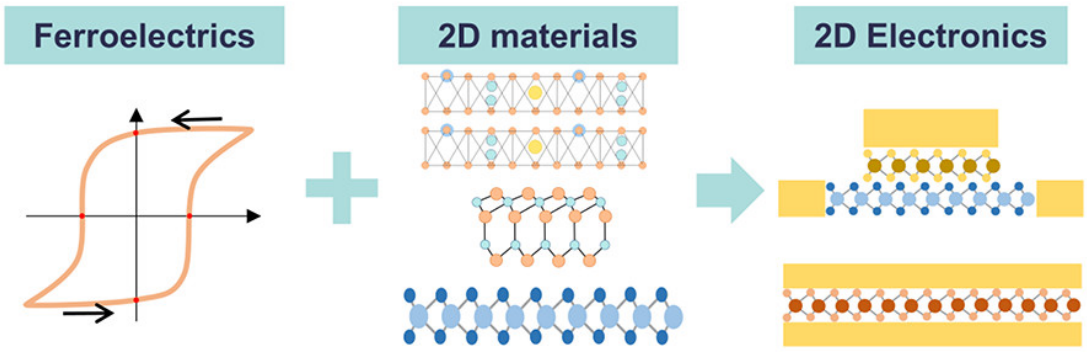

Figure 2.4: Schematic of ferroelectrics combined with 2D materials [31].

2.2.2. Classification and Applications of 2D Ferroelectrics

A major advantage of 2D ferroelectric materials is their van der Waals (vdW) layered structure [31], allowing them to be seamlessly stacked without the interfacial strain issues faced by conventional materials. This makes it possible to create heterostructures that enhance electronic performance, enabling ultra-fast switching and high data retention [34].

Fig. 2.5 categorizes different types of ferroelectric materials, structures, and their applications in 2D electronics. The classification includes thin-film ferroelectrics (such as perovskites and HfO_2) and 2D vdW ferroelectrics (like $CuInP_2S_6$ and α-In_2Se_3). The structural classifications include two-terminal and multi-terminal configurations, crucial for diverse applications. The bottom section of the figure highlights ferroelectric negative capacitance field-effect transistors (NC-FETs) [35] [36], used for reducing power consumption, and neuromorphic computing devices, which mimic brain-like learning behavior.

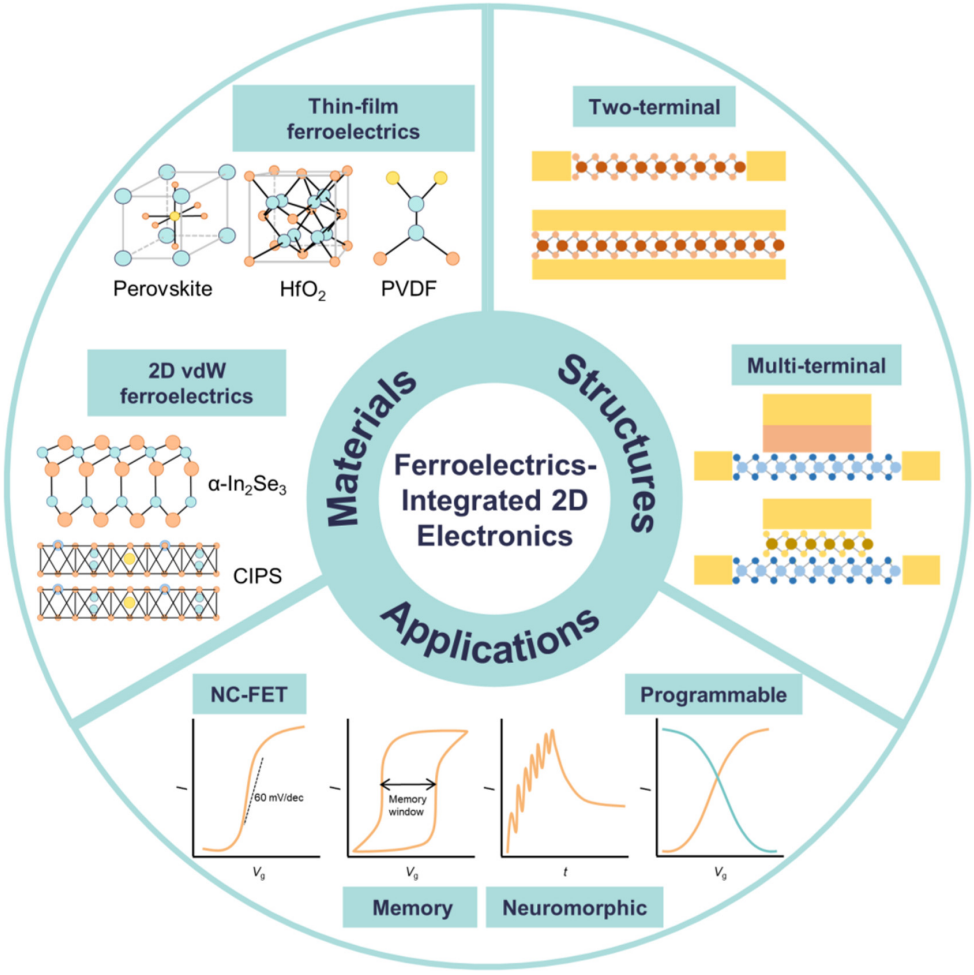

Figure 2.5: Different classifications of ferroelectric materials and their different roles in 2D electronics, including memory devices and neuromorphic applications [31].

2.2.3. 2D Ferroelectric Transistor Architectures

A key application of ferroelectrics in nanoelectronics is their integration into transistor architectures. Fig. 2.6 presents 2D ferroelectric transistors that exploit the polarization-switching properties of these materials. The first set (a-c) showcases ferroelectric field-effect transistors (FeFETs), where a ferroelectric gate dielectric provides superior charge control. vdW FeFETs [33] enhance performance by reducing defect-related scattering. The next set of devices (d-f) focuses on ferroelectric tunnel junctions (FTJs) [37], which modulate quantum tunneling [38] leading to high-speed, non-volatile memory applications.

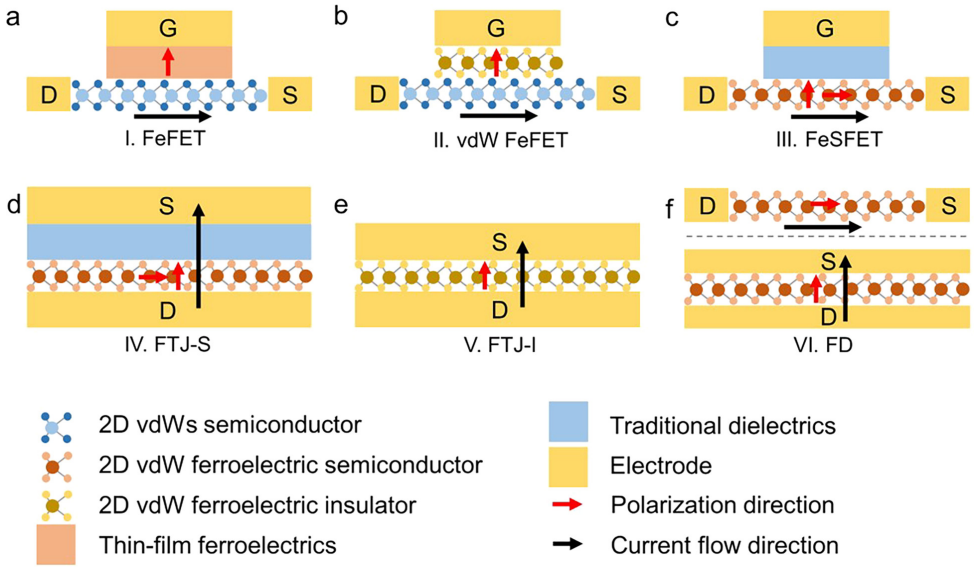

Figure 2.6: Various 2D ferroelectric transistor architectures, including FeFET, vdW FeFET, FeSFET, and ferroelectric tunnel junctions (FTJs), showing their integration for next-generation nanoelectronics [31].

Conclusion

Reconfigurable electronics and ferroelectronics each address critical limitations of CMOS technology in different but complementary ways, one through functional adaptability, the other through non-volatile and low-power switching. When combined, they offer a powerful platform for next-generation device architectures. The concepts introduced in this chapter form the foundation for the device architectures explored in my research. In the following chapters, I build on these ideas and demonstrate how combining reconfigurability with ferroelectric functionality can lead to novel, high-performance devices for next-generation applications.

3 | 2D Materials and Their Electronic Properties

Two-dimensional (2D) materials have revolutionized the field of materials science and condensed matter physics since the isolation of graphene in 2004 [39]. These atomically thin crystals exhibit remarkable electronic properties that often differ significantly from their bulk counterparts. The unique characteristics of 2D materials arise from quantum confinement effects and the reduced dimensionality, which lead to novel phenomena and potential applications in electronics, optoelectronics, and quantum technologies.

The electronic properties of 2D materials span a wide range, from semimetals like graphene to semiconductors such as transition metal dichalcogenides (TMDs) [40, 41] and insulators like hexagonal boron nitride [42]. This diversity allows for the creation of various electronic components within the same atomically thin platform. Moreover, the absence of dangling bonds on their surfaces makes 2D materials less susceptible to interface issues that plague traditional semiconductor devices.

One of the most intriguing aspects of 2D materials is the ability to tune their electronic properties through various methods. These include controlling the number of layers, applying strain, introducing defects or dopants, and manipulating the dielectric environment. Such tunability offers unprecedented flexibility in designing electronic devices with specific characteristics tailored for particular applications.

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3.1. Van der Waals Materials and Heterostructures

Van der Waals (vdW) materials represent a subset of 2D materials characterized by weak interlayer bonding. This weak interaction allows for easy exfoliation of single or few-layer sheets from bulk crystals. The vdW nature of these materials also enables the creation of heterostructures, artificial stacks of different 2D materials, without the constraints of lattice matching that limit traditional epitaxial growth techniques.

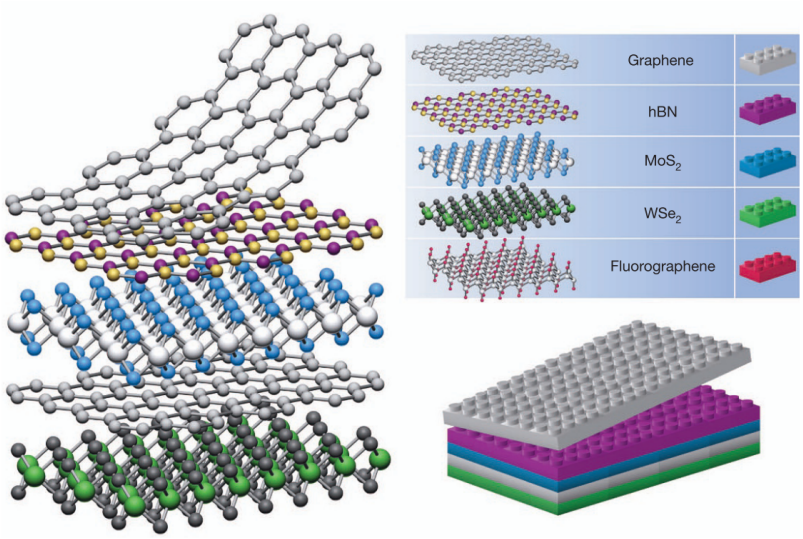

Figure 3.1: Van der Waals heterostructures: A 'Lego-Like' approach to 2D material engineering [29].

As shown in Fig. 3.1(a), van der Waals (vdW) materials [29, 43], characterized by weak interlayer bonding, enable the precise stacking of different two-dimensional (2D) layers to form artificial heterostructures with tailored properties. This modular approach, similar to assembling lego blocks, allows researchers to construct complex layered systems with diverse functionalities. The figure illustrates a multi-layered vdW heterostructure composed of graphene, hexagonal boron nitride (hBN) [44], molybdenum disulfide (MoS_2) [45, 46], tungsten diselenide (WSe_2) [47], and fluorographene [48], demonstrating the versatility of these materials in nanoscale device engineering.

Van der Waals materials have emerged as a transformative platform in condensed matter physics and nanotechnology. Unlike conventional materials, where strong chemical bonds dictate layer arrangements, vdW materials can be exfoliated into atomically thin sheets and restacked in arbitrary sequences without requiring lattice matching. This flexibility has led to the creation of vdW heterostructures (vdWHs) [29, 49–52], where different 2D materials are combined to engineer novel quantum systems with properties unattainable in a single material.

The ability to design vdWHs has enabled groundbreaking advancements in various fields. In electronics, these structures provide ultra-thin, high-mobility semiconducting channels for more efficient transistors and memory devices. In optoelectronics, the combination of materials with different bandgaps allows for highly tunable photodetectors and light-emitting devices applications. With atomic-scale precision, van der Waals heterostructures have revolutionized material design, offering unprecedented control over electronic properties and enabling next-generation applications in nanoelectronics, neuromorphic computing, and photonics. As researchers continue to explore new stacking configurations and interactions, vdW materials are expected to drive further breakthroughs in both fundamental physics and technological innovations.

Highlights of Key Materials in My Research

3.2. Van der Waals Insulator: hBN

Hexagonal boron nitride (hBN) is a two-dimensional material with a structure analogous to graphene, consisting of boron and nitrogen atoms arranged in a honeycomb lattice. Often referred to as "white graphene" due to its appearance, hBN is widely used for its exceptional insulating properties, including a wide bandgap of approximately 6 eV. It plays a crucial role in integrating with other 2D materials, particularly in forming high-quality van der Waals heterostructures (vdWHs). Its atomically smooth surface, free from dangling bonds and charge traps, minimizes impurity states and enhances carrier mobility at the interface with 2D semiconductors. These characteristics make hBN a promising gate dielectric for field-effect transistors (FETs) based on 2D materials, as it meets the key requirements of an ideal insulator, offering excellent gate control, low leakage current, minimal defect density, high breakdown strength, and enhanced carrier mobility.. As such, hBN is indispensable for advancing the performance and reliability of 2D electronic and optoelectronic devices.

Understanding the structural and electronic properties of hBN is essential for its effective utilization in device applications. The atomic arrangement of hBN exhibits a honeycomb structure, where alternating boron and nitrogen atoms form a stable hexagonal pattern, ensuring strong in-plane covalent bonding. This ordered lattice contributes to wide bandgap of hBN, a fundamental characteristic that makes it an excellent insulator (Fig. 3.2(a)).

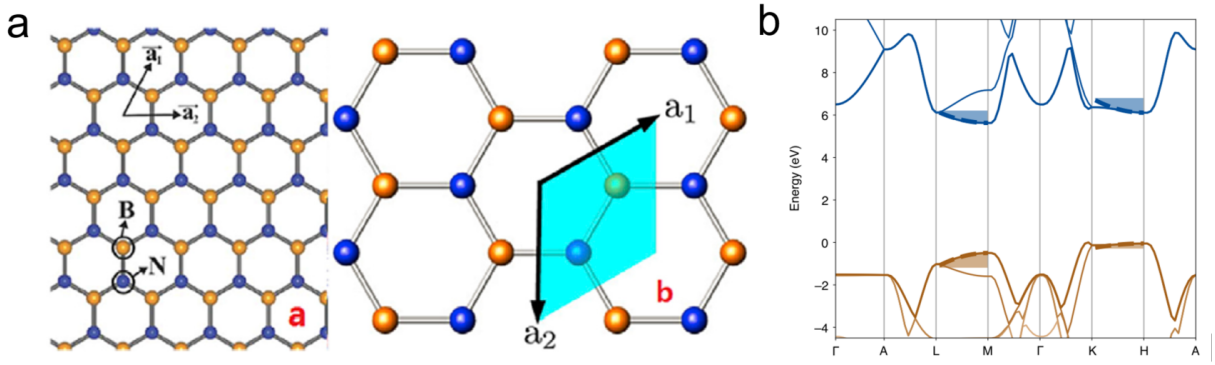

Figure 3.2: (a) Honeycomb structure of 2D hBN with Bravais lattice vectors (left) and a highlighted unit cell (right). (b) Band structure of hBN, illustrating its wide bandgap and electronic properties crucial for its function as an insulator in 2D material-based devices [53].

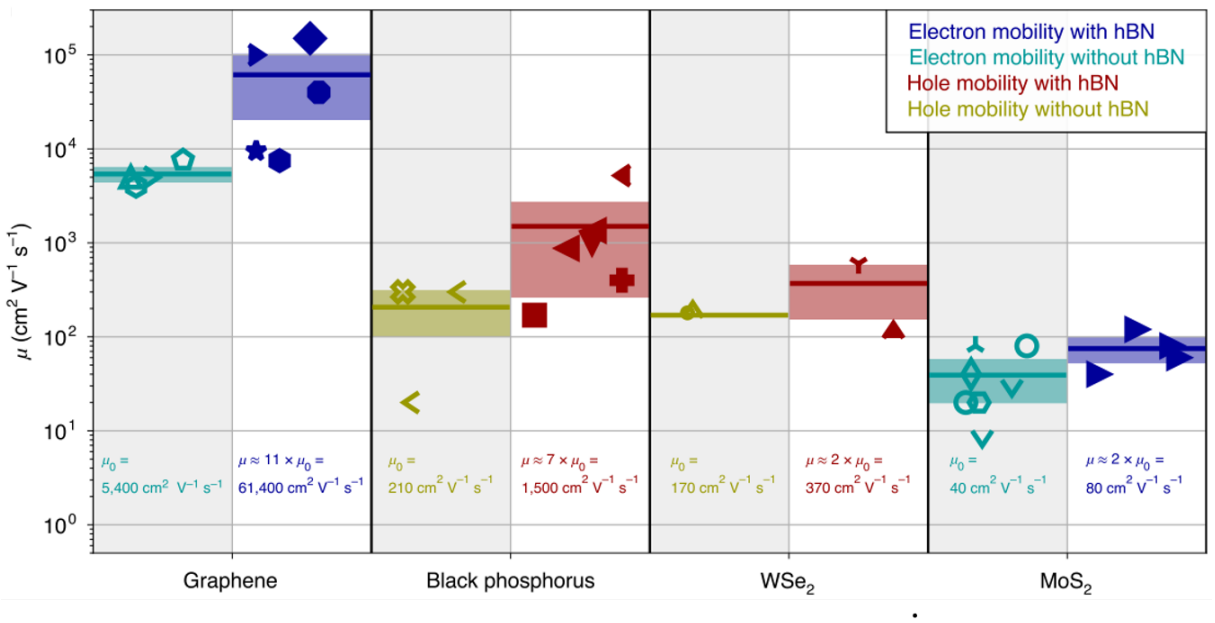

Figure 3.3: Variation in carrier mobility in different 2D semiconductor materials when interfaced with hBN [53].

Carrier mobility is a critical factor in the performance of semiconductor devices. The presence of hBN as an encapsulating layer has demonstrated significant improvements in mobility due to its atomically flat nature and absence of charge traps. These properties help reduce Coulomb scattering and suppress charge impurities, thereby enhancing electronic transport [54–57]. As shown in Fig. 3.3, 2D semiconductors integrated with hBN exhibit notably higher mobility compared to those using conventional oxide-based substrates.

Beyond mobility, another advantage of hBN is its behavior as a gate insulator, particularly in terms of leakage current suppression (Fig. 3.4).

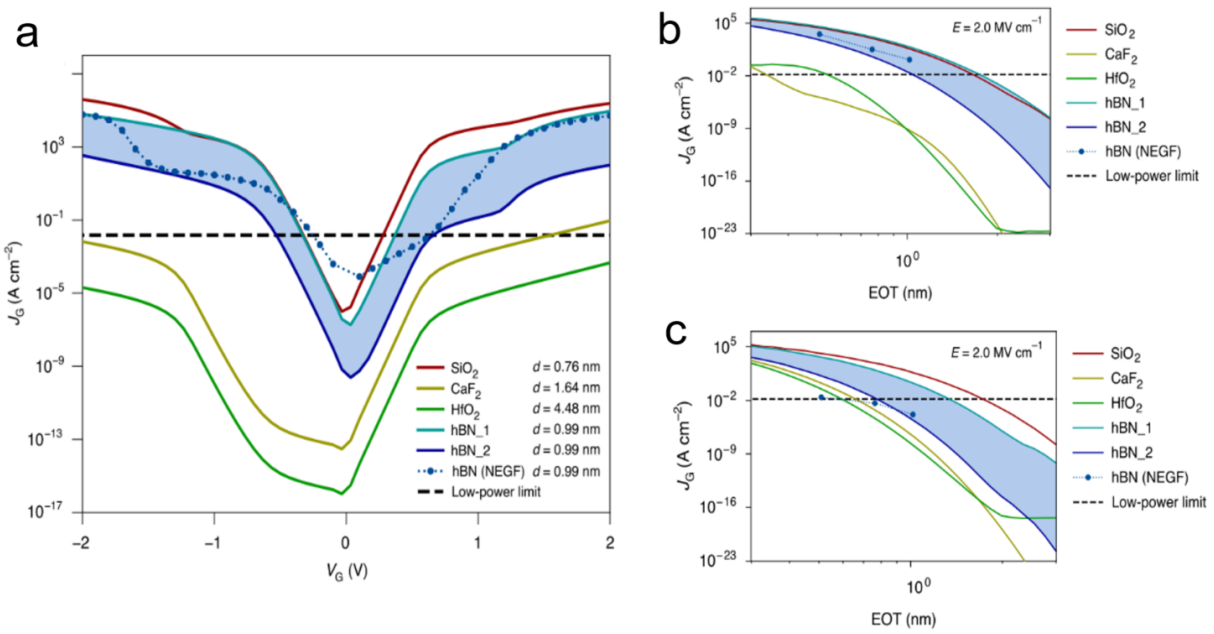

Figure 3.4: Experimental and theoretical tunnel current densities through ultrathin layers of hBN and other dielectrics. The analysis is based on the Tsu–Esaki model for the metal–oxide–semiconductor stack of Au/dielectric/Si. hBN exhibits lower leakage currents than SiO_2, making it a superior alternative for gate insulation in many applications [53].

The results indicate that hBN outperforms SiO_2 in minimizing leakage currents, thereby offering a more effective solution for improving device efficiency in comparison to traditional oxide-based insulators.

3.3. Van der Waals Semiconductor: WSe_2

Tungsten diselenide (WSe_2), a transition metal dichalcogenide (TMD), exhibits remarkable electronic properties, making it a promising material for advanced electronics and optoelectronics. Its layered structure consists of tungsten atoms sandwiched between selenium atoms, held together by weak van der Waals forces. In its monolayer form, WSe_2 transitions from an indirect to a direct bandgap semiconductor, making it highly suitable for optoelectronic applications such as light-emitting diodes (LEDs), solar cells, and photodetectors [58][59].

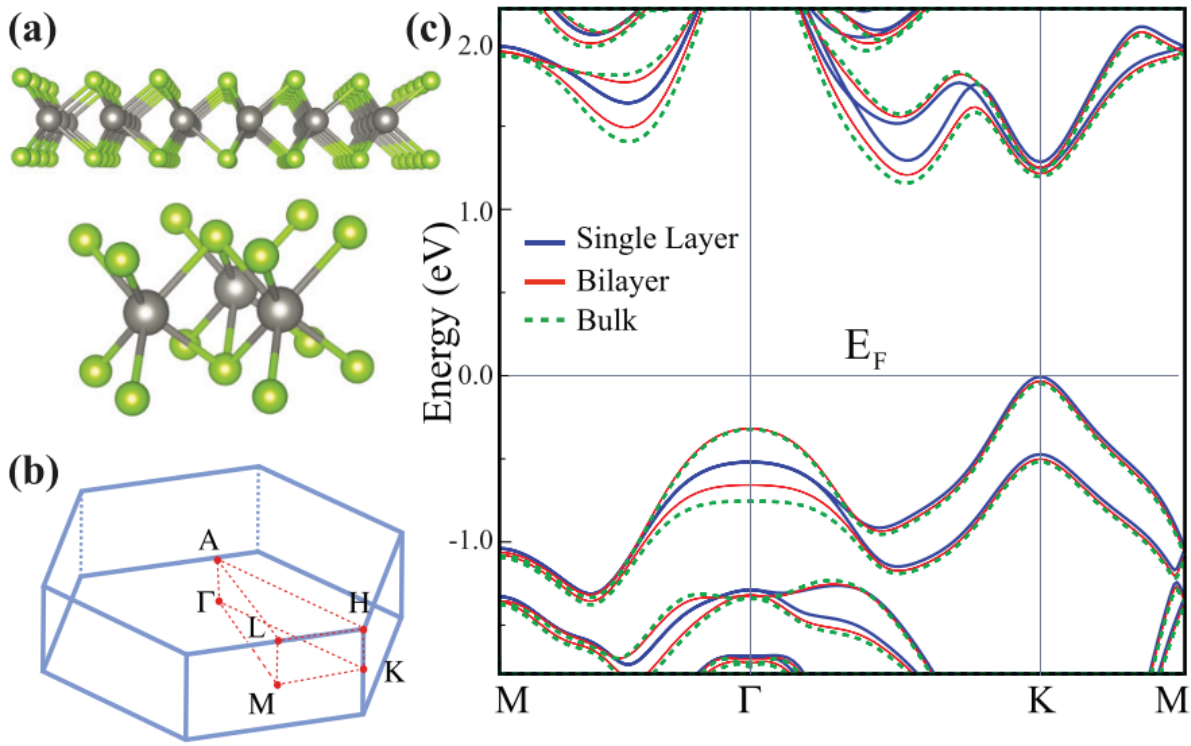

Figure 3.5: (a) Crystal structure of WSe_2 in side and top views. (b) Brillouin zone with high-symmetry points. (c) Electronic band structure evolution from bulk to monolayer. The transition from indirect to direct bandgap enhances optical and electronic properties [59].

A key feature of WSe_2 is its ambipolar semiconducting behavior, allowing it to function as both a p-type and n-type material under appropriate gate voltages. This ambipolarity results from the Fermi level shifting in response to an external electric field, upshifting by approximately 100 meV for n-type behavior and downshifting by approximately 340 meV for p-type behavior [60]. Compared to MoS_2, which exhibits strong Fermi level pinning leading to dominant n-type conduction, WSe_2 provides more balanced electron and hole transport [60].

As shown in Fig. 3.5(c), the band structure of WSe_2 changes significantly with thickness. In bulk form, it exhibits an indirect bandgap, while in monolayer form, it transitions to a direct bandgap, improving its optical absorption and electronic performance.

3.3.1. Electronic Properties

The electronic behavior of WSe_2 is closely tied to its layered structure. As shown in Fig. 3.6, the interlayer spacing is approximately 0.7 nm, and the weak van der Waals interaction between layers provides a clean, atomically flat interface. This structural uniformity helps suppress interfacial impurity scattering, which is critical for improving carrier transport properties.

Moreover, when integrated into a transistor architecture, such as the dual-gate device illustrated in Fig. 3.6(a), an external electric field can modulate the carrier concentration in the WSe_2 channel. This is made possible by the ambipolar nature of the material, allowing it to switch between electron and hole conduction depending on the gate bias. The implications of this field-induced doping tunability will be discussed in detail in the following section.

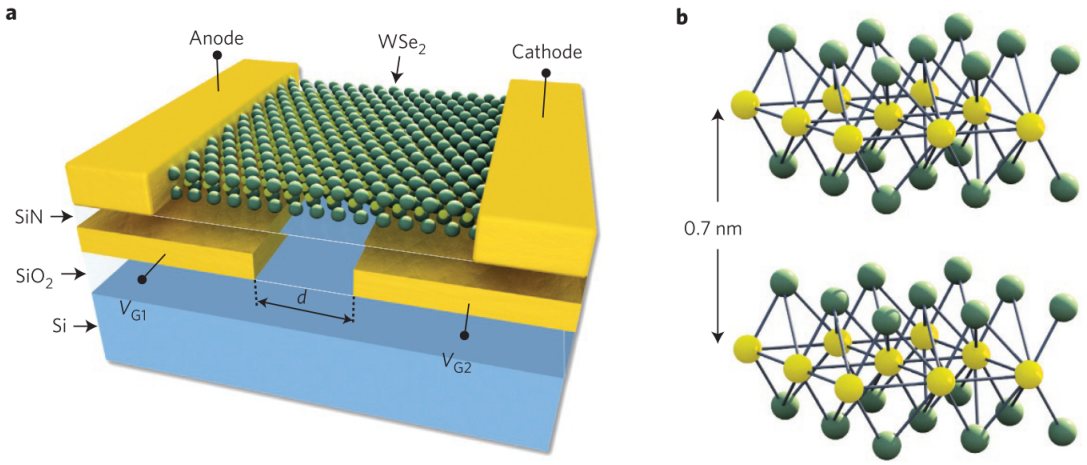

Figure 3.6: (a) WSe_2 transistor device with a dual-gate configuration. (b) Atomic structure showing interlayer spacing of 0.7 nm. The dual-gate architecture enables efficient charge transfer and gate tunability [58].

As illustrated in Fig. 3.6(a), a transistor based on WSe_2 is designed with a dual-gate configuration (V_{G1}, V_{G2}). This structure enables efficient charge transfer and gate-tunable properties, allowing it to switch between p-type and n-type conduction.

3.3.2. Dual-Gate Diode and Photodiode

WSe_2 can function as a diode using a dual backgate architecture, where two separate gate voltages (V_{G1}, V_{G2}) control the formation of the p–n junction within a single material [58]. Due to its ambipolar nature, WSe_2 can exhibit both p-type and n-type conduction depending on the applied gate voltages, enabling a tunable rectifying behavior.

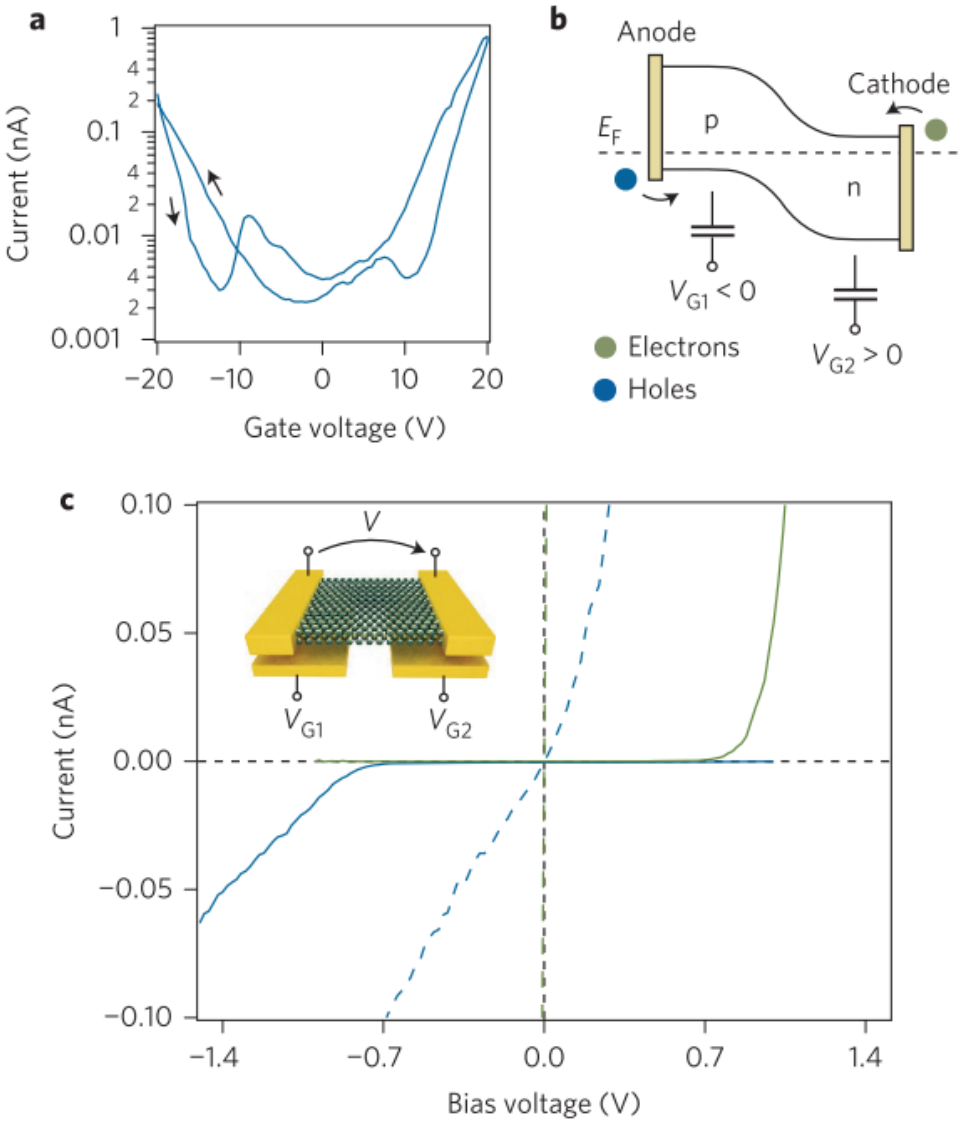

Figure 3.7: (a) Gate-dependent current modulation of WSe_2-based diode. (b) Schematic of p–n junction formation. (c) I–V characteristics showing rectification behavior for different junction configurations: p–n (solid green line), n–p (solid blue line), n–n (dashed green line), p–p (dashed blue line) [58].

As shown in Fig. 3.7(b), the application of $V_{G1} < 0$ induces hole accumulation (p-region), while $V_{G2} > 0$ induces electron accumulation (n-region), forming a p–n junction. The corresponding I–V characteristics in Fig. 3.7(c) confirm the rectification behavior of the WSe_2 diode.

Furthermore, due to its direct bandgap in monolayer form, WSe_2 also functions as a photodiode [61], efficiently converting optical energy into electrical power. The photodiode effect arises from the generation of electron-hole pairs under illumination, leading to a photovoltaic response.

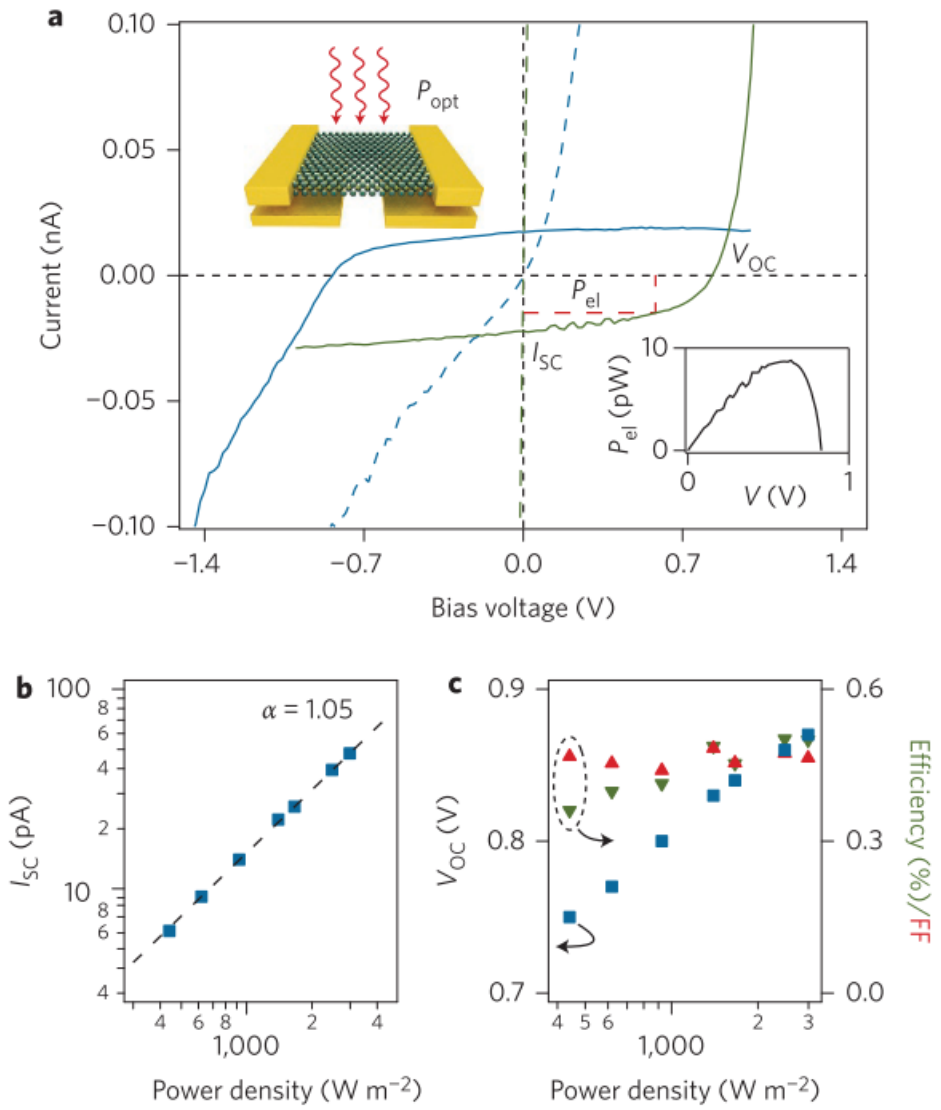

Figure 3.8: (a) I–V characteristics of WSe_2-based photodiode under illumination: p–n (solid green line), n–p (solid blue line), n–n (dashed green line), p–p (dashed blue line). Top inset: Schematic of experiment. Lower inset: electrical power (P_{el}) versus voltage under incident illumination (b) Short-circuit (I_{SC}) current as a function of electrical power density. (c) Open-circuit voltage (V_{OC}) and efficiency variation with electrical power density [58].

Fig. 3.8(a) demonstrates the shift in photocurrent and open-circuit voltage (V_{OC}) under illumination. The short-circuit current (I_{SC}) in Fig. 3.8(b) increases linearly with optical power density, confirming a stable photoresponse. Fig. 3.8(c) further shows the variation of V_{OC} and the efficiency with the power density, indicating the effectiveness of WSe_2 as a photodiode.

3.3.3. Mobility of Electrons and Holes

Carrier mobility in WSe_2 is highly thickness-dependent. In monolayer WSe_2, mobility is lower due to scattering effects from charged impurities at the interface. With increasing thickness, enhanced dielectric screening reduces impurity scattering, improving both electron and hole transport [59, 62]. Furthermore, increased thickness leads to a higher density of states, reduces the Schottky barrier for carrier injection and further enhances mobility [63, 64].

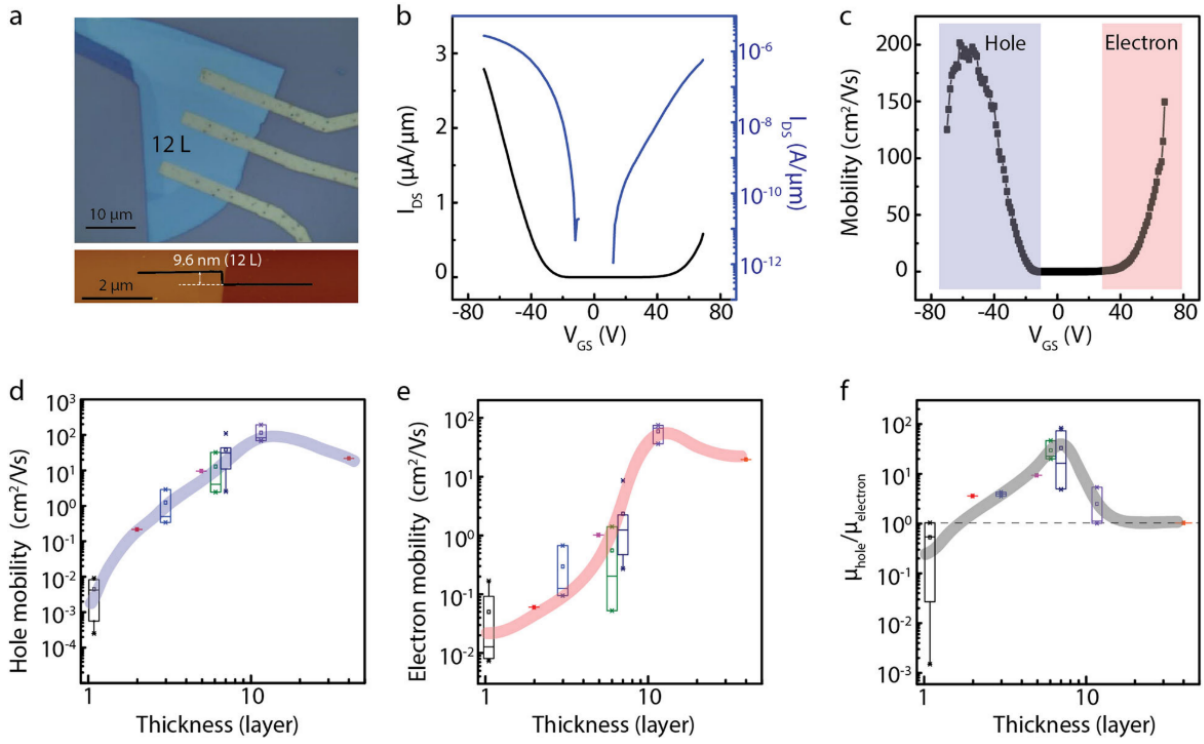

Figure 3.9: (a) Typical optical image of the device. (b), (c) Transfer curve of 12L WSe_2 and the corresponding mobility, respectively. (d),(e) Thickness dependent hole and electron mobility. (f) The ration of electron and hole mobility. [60].

As shown in Fig. 3.9, mobility improves with increasing thickness due to reduced impurity scattering, and, nearly symmetric behavior of hole and electron mobilities confirms balanced ambipolar transport, a key requirement for high-performance ambipolar transistor applications [60].

3.4. Van der Waals Ferroelectric Insulator: $CuInP_2S_6$

Copper indium thiophosphate ($CuInP_2S_6$) is a unique two-dimensional (2D) material that exhibits room-temperature ferroelectricity [65], a rare property among 2D materials. Unlike

conventional bulk ferroelectric oxides such as $PbTiO_3$ and $BaTiO_3$, which require intricate substrate engineering for epitaxial thin-film growth, CIPS belongs to a class of weakly bonded non-oxide ferroelectrics. This characteristic allows mechanical exfoliation into nanometer-thin layers while preserving intrinsic ferroelectric properties.

With distinct electrical, structural, and piezoelectric properties, CIPS is a promising candidate for next-generation nanoelectronics, memory devices, and ferroelectric field-effect transistors (Fe-FETs). Its layered structure, part of the transition metal thiophosphate (TPS) family, enables easy exfoliation, offering stability and scalability for high-efficiency and low-power electronic applications.

3.4.1. Crystal Structure and Ferroelectric Properties

CIPS crystallizes in a monoclinic structure (space group *Cc*), featuring layers weakly bonded by van der Waals interactions. The structure consists of a sulfur framework with Cu, In, and P-P triangular sublattices forming a collinear two-sublattice ferrielectric system. This arrangement enables spontaneous polarization, which can be switched by an external electric field.[65]

CIPS undergoes a first-order phase transition at approximately 320 K, shifting from a ferroelectric to a paraelectric phase due to structural changes from non-centrosymmetric to centrosymmetric symmetry. The spontaneous polarization primarily arises from the off-center displacement of Cu^+ ions, governed by the second-order Jahn-Teller effect [66]. The second-order Jahn–Teller effect refers to the tendency of certain ions, such as Cu^+ in CIPS, to shift from their symmetric position to a slightly off-center one in order to lower the overall energy of the crystal. This distortion breaks inversion symmetry and leads to the formation of a permanent electric dipole, which enables ferroelectric behavior in CIPS.

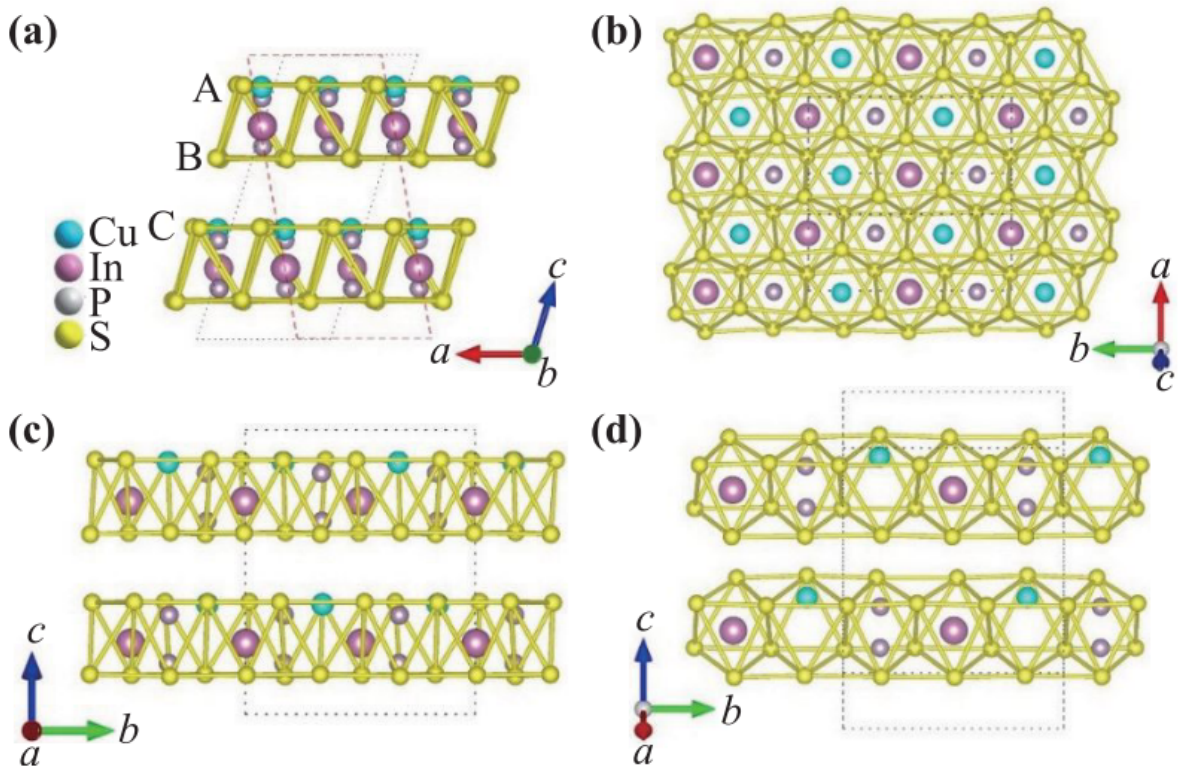

Figure 3.10: Crystal structure of CIPS, showing the sulfur framework with Cu, In, and P-P sublattices. Weak van der Waals interactions enable exfoliation into thin flakes [67].

Fig. 3.11 shows the amplitude and phase curve of the piezorespoce force microscopy (PFM) for different thicknesses of the CIPS layer, this confirms that CIPS retains a stable dipole moment up to a thickness of 4 nm, an extraordinary feature for 2D ferroelectrics, making it highly promising for nanoelectronics and memory applications.

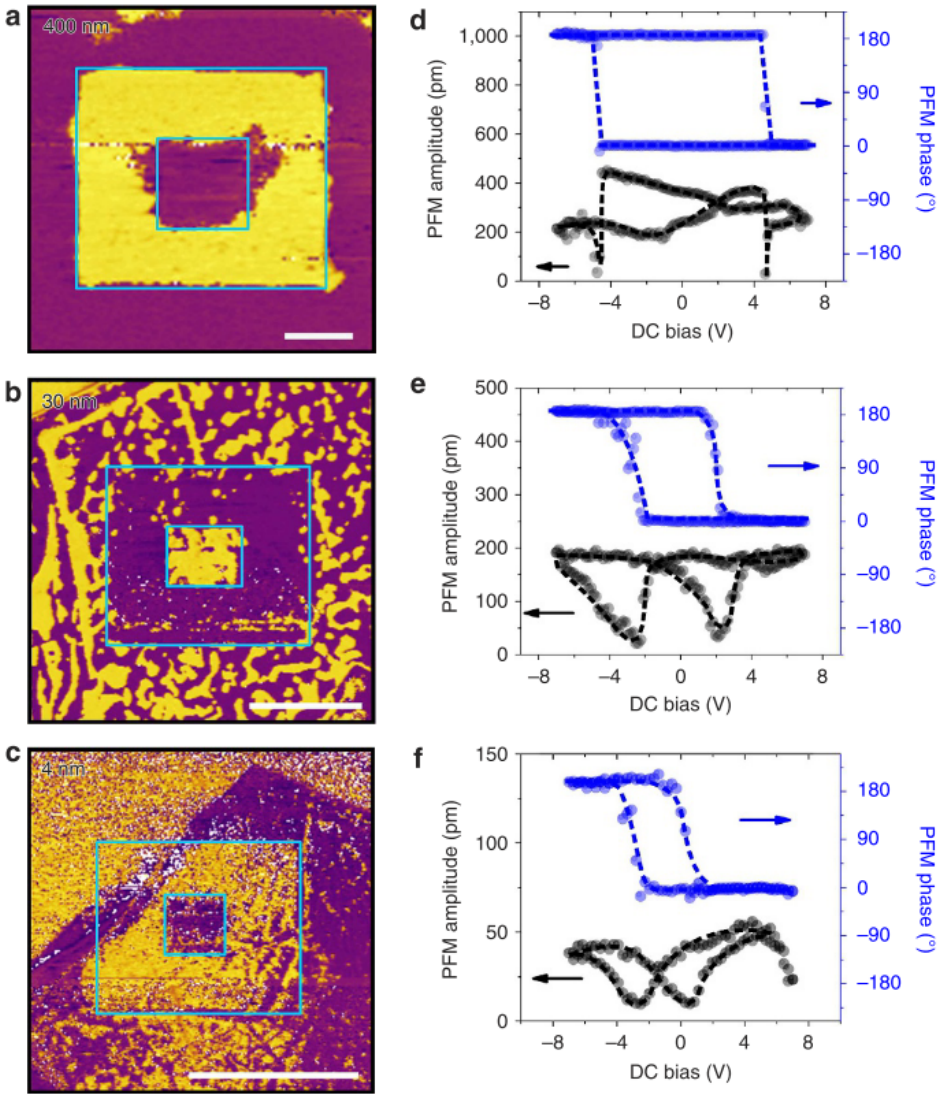

Figure 3.11: (a-c) PFM phase images of 400 nm, 30 nm, 4 nm thick CIPS flake. (d-f) corresponding PFM amplitude and phase hysterisis loop[65]

3.4.2. Electrical Properties

Optimized Ferroelectric Heterostructures

To enhance stability and suppress charge trapping [43, 68], CIPS-based Fe-FETs [67, 69] incorporate hexagonal boron nitride (h-BN) interlayers. These van der Waals (vdW) heterostructures improve endurance, reduce leakage currents, and enhance retention properties.

Insulating Nature of CIPS

CIPS exhibits excellent insulating behavior, making it a suitable gate dielectric for Fe-FETs. Its insulating property allows precise control over the channel conductivity in transistor structures without significant leakage currents (Fig. 3.13). The material's large coercive field (∼300 kV/cm) further enhances its effectiveness as an insulator in electronic devices.

3.4.3. Applications in Emerging Electronics

CIPS-Based Fe-FETs

Fe-FETs are promising for low-power, high-speed memory and logic devices, utilizing ferroelectric materials as gate dielectrics for non-volatile data storage. Recent advancements have demonstrated Fe-FETs based on MoS_2/h-BN/graphene/CIPS vdW heterostructures, where MoS_2 acts as the semiconductor channel and CIPS serves as the ferroelectric top-gate dielectric.

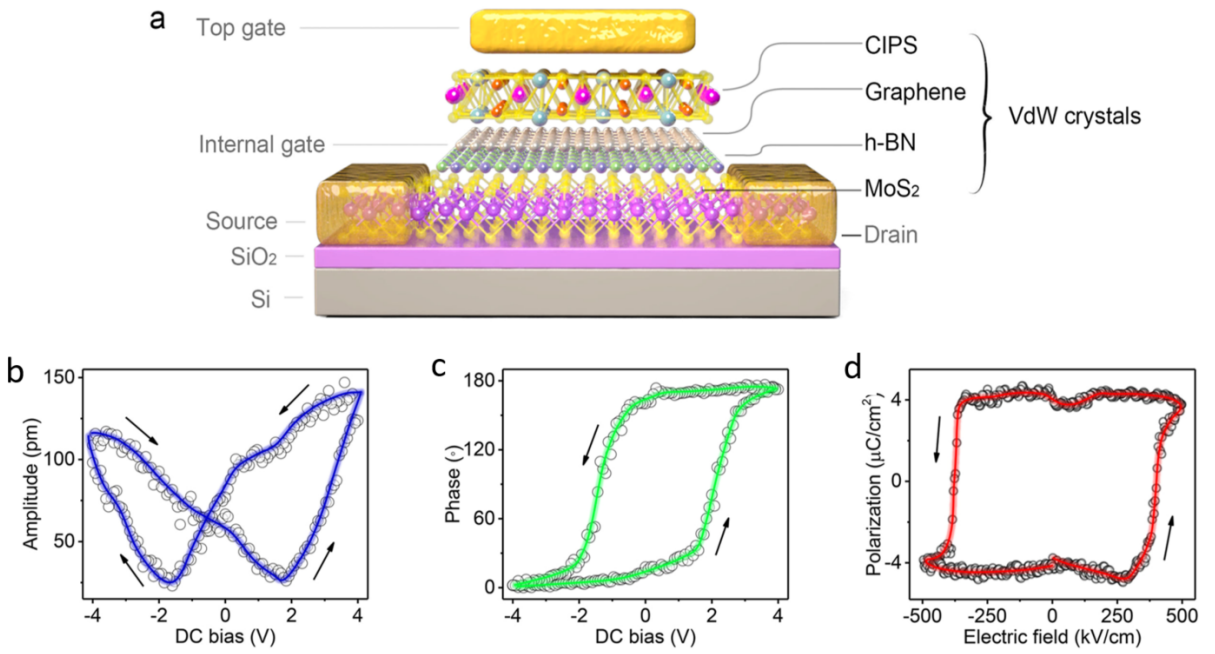

Figure 3.12: (a)Schematic of MoS_2/h-BN/graphene/CIPS vdW Fe-FET. (b)PFM amplitude, (e)phase. (g)P-E hysteresis loop [70].

The van der Waals (vdW) FeFET presented in Fig. 3.12(a) consists of a metal-ferroelectric-metal-insulator-semiconductor (MFMIS) structure, where a CIPS ferroelectric capacitor is integrated onto a 2D field-effect transistor (FET). The stacked heterostructure comprises few-layer MoS_2 as the semiconductor channel, h-BN as the gate dielectric, and graphene as the gate

contact. The ferroelectric polarization in CIPS modulates the surface potential of MoS_2, influencing the source–drain current. The graphene interlayer plays a dual role as an internal gate for baseline 2D FET characterization and as a compensating layer for both upward and downward ferroelectric polarization states.

The piezoresponse hysteresis loops in Figs. 3.12(b) and 3.12(c) exhibit a standard butterfly-shaped amplitude response and a 180° phase shift at coercive voltages, respectively, confirming robust ferroelectric switching. Additionally, the polarization versus electric field (P–E) hysteresis loop in Fig. 3.12(d) demonstrates a nearly square-shaped loop with a high coercive field (∼300 kV/cm) and remnant polarization ∼4 μC/cm^2) , signifying stable and switchable ferroelectric behavior in CIPS.

Counterclockwise hysteresis loops in transfer characteristics confirm the ferroelectric gating effect. High ON/OFF ratios (∼10^6-10^7), large memory windows, and long retention times make these devices suitable for low-power computing applications.

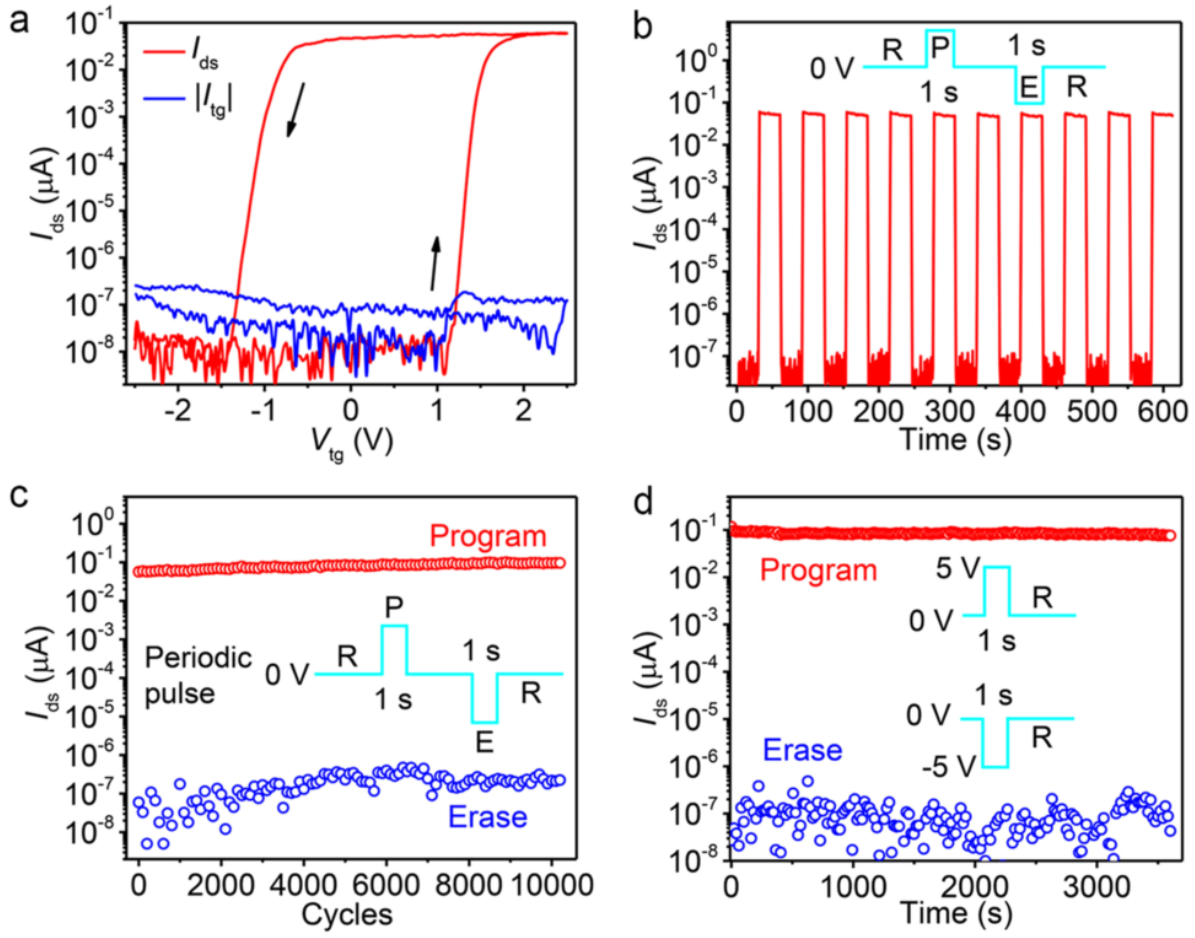

Figure 3.13: Electrical characteristics of a vdW Fe-FET, showing memory retention and endurance performance [70].

These devices exhibit non-volatile memory behavior, where gate voltage switches the polarization state of CIPS, resulting in a stable ON/OFF resistance ratio. Counterclockwise hysteresis loop with a large memory window (MW) and high on/off ratio, confirming stable ferroelectric switching behavior (Fig. 3.13(a)). The top-gate leakage current remains ultra-low (∼0.3 pA), significantly lower than FeFETs with conventional ferroelectrics, ensuring minimal power dissipation. The device achieves a high program/erase (P/E) ratio exceeding 10^7 (Fig.3.13(b)), along with a long retention time (Fig. 3.13(d)).

The endurance performance over 10^4 cycles (Fig. 3.13(c)) confirms fatigue-free operation, with no significant degradation in the P/E ratio. The dynamic switching characteristics further validate stable and reproducible program/erase states, making this vdW FeFET a promising candidate for non-volatile memory applications with high reliability.

Negative Capacitance FETs (NC-FETs)

A significant breakthrough in nanoelectronics is the realization of Negative Capacitance FETs (NC-FETs) using CIPS. In these devices, the negative capacitance effect enhances electrostatic control over the semiconductor channel, leading to sub-60 mV/decade subthreshold swing (SS), breaking the conventional Boltzmann limit of 60 mV/dec. This ultra-low-power operation reduces power dissipation in digital logic applications.

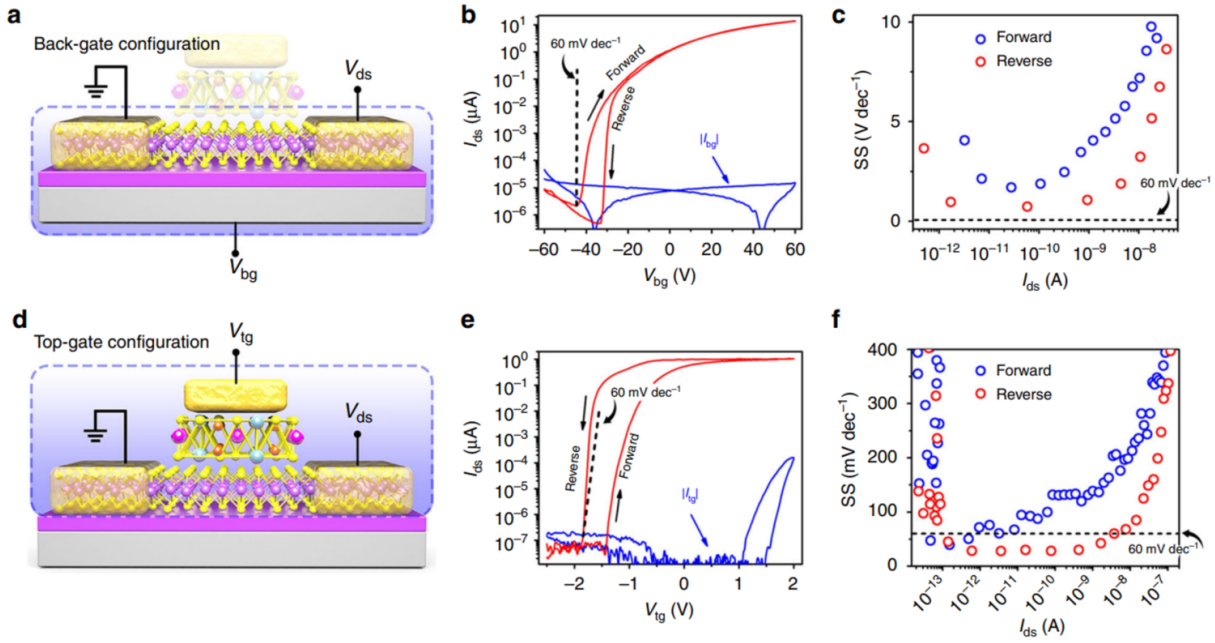

Figure 3.14: Room-temperature electrical characterization of CIPS/MoS_2 vdW NC-FETs, demonstrating subthreshold swing performance [36].

CIPS is an exceptional ferroelectric material with unique properties at the nanoscale. Unlike traditional ferroelectric thin films that require complex deposition techniques, CIPS can be mechanically exfoliated and seamlessly integrated into flexible, low-power devices. Its robust polarization switching, excellent retention, and compatibility with 2D heterostructures make it a strong candidate for next-generation nanoelectronics.

From non-volatile memory and logic circuits to neuromorphic computing and energy-efficient sensors, CIPS holds immense potential for technological advancements. Further research into CIPS-based heterostructures and interface engineering may unlock new applications, making it a key player in the evolution of ferroelectric nanoelectronics and semiconductor technologies.

3.5. Van der Waal Ferroelectric Semiconductor: α-In_2Se_3

Indium selenide (In_2Se_3) is a layered semiconductor with strong ferroelectric and semiconducting properties, making it a promising material for advanced electronic applications. The α-phase, in particular, exhibits stable room-temperature ferroelectricity with coupled in-plane (IP) and out-of-plane (OOP) polarization [71, 72]. This section is adapted from [73, 74].

3.5.1. Crystal Structure and Band Structure of α-In_2Se_3

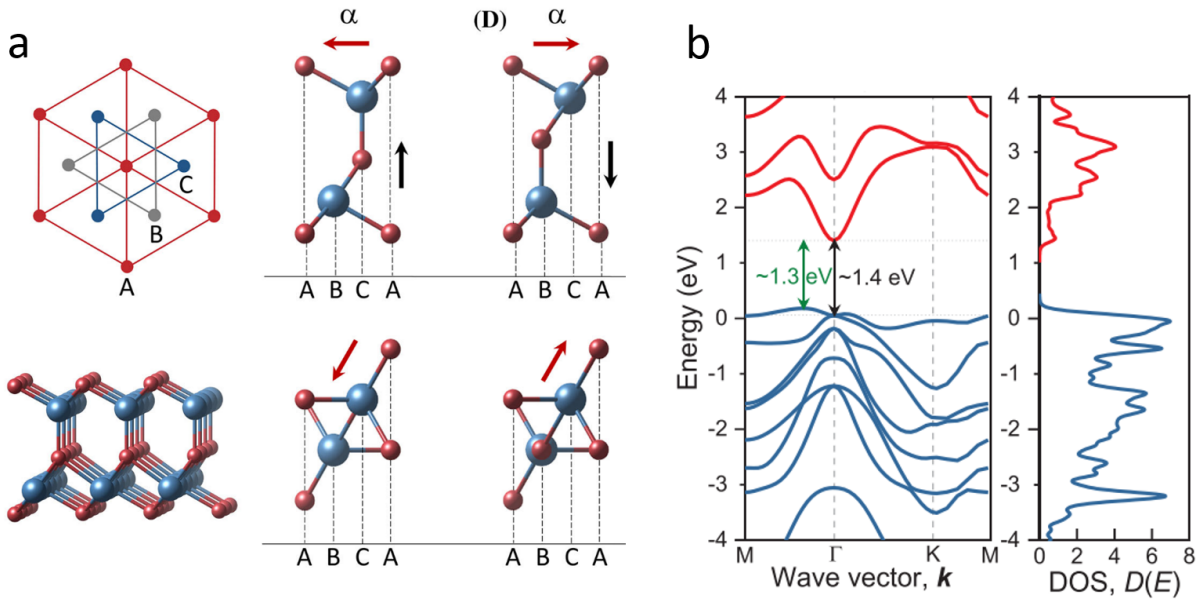

Figure 3.15: (a) Crystal structure and polarization directions of α-In_2Se_3. (b) Density functional theory (DFT)-derived band structure [73, 74].

Fig 3.15(a) illustrates crystal structure of α-In_2Se_3, where the displacement of selenium atoms enables spontaneous ferroelectric polarization [73]. The presence of both IP and OOP polarizations suggests strong coupling between in-plane atomic displacements and the vertical dipole moment, which is a key feature for memory and logic applications [74].

Fig 3.15(b) presents the band structure of α-In_2Se_3 obtained from DFT calculations, confirming a direct bandgap of approximately 1.4 eV [74]. This characteristic is crucial for optoelectronic applications such as photodetectors and transistors. The band alignment and density of states further indicate its potential for use in tunable electronic devices, where electric-field modulation can enable dynamic band engineering [73].

3.5.2. Piezoresponse Force Microscopy (PFM) of α-In_2Se_3

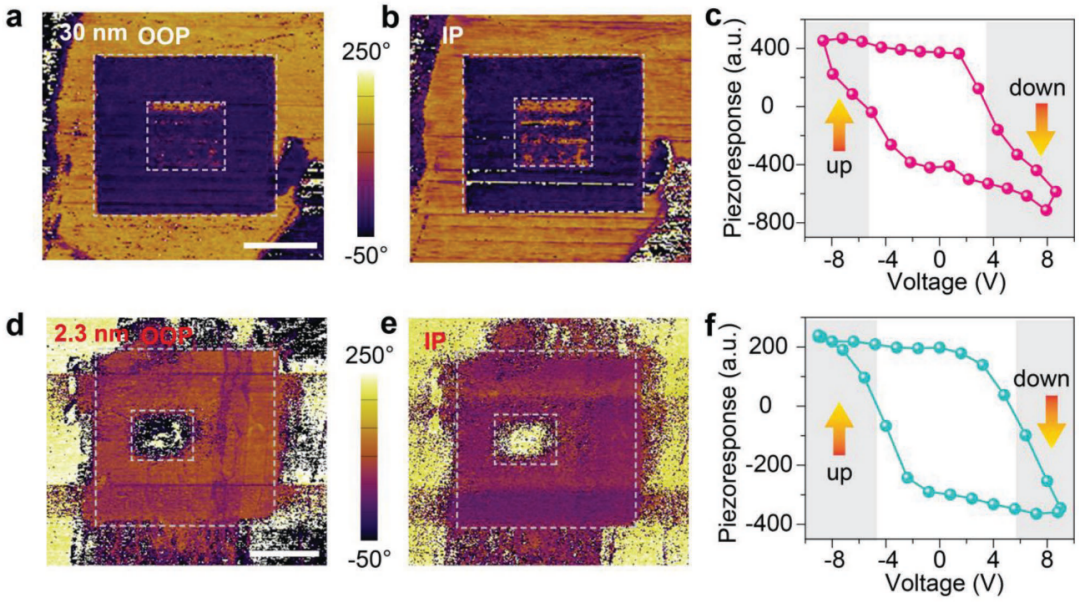

Figure 3.16: (a, b) PFM phase images of 30 nm-thick α-In_2Se_3 flake showing stable out-of-plane (OOP) and in-plane (IP) polarization, respectively. (c) Hysteresis loops confirming ferroelectric switching. (d) and (e) PFM phase images of a 2.3 nm-thick flake, demonstrating robustness of OOP and IP polarization , respectively. (f) Hysteresis loops confirming polarization switching at very thin α-In_2Se_3 [75].

Figs. 3.16(a) and (b) demonstrate PFM phase images capturing the OOP and IP polarization behavior of a 30 nm-thick α-In_2Se_3 flake. The distinct domain contrast indicates that the material exhibits stable ferroelectric switching at this thickness [75]. The corresponding hysteresis loops in Fig 3.16(c) confirm the non-volatile nature of its polarization states.

Figs. 3.16(d, e) highlight the retention of ferroelectricity in ultra-thin (2.3 nm) α-In_2Se_3 flakes, illustrating that its ferroelectric properties persist even at the monolayer limit [75]. This exceptional thin-film stability is advantageous for nanoscale memory devices, where maintaining polarization at reduced dimensions is critical. The observed IP and OOP hysteresis loops in Fig 3.16(f) further validate the bidirectional polarization control, demonstrating the feasibility of α-In_2Se_3 for low-power, non-volatile ferroelectric devices.

The structural and ferroelectric properties of α-In_2Se_3, demonstrated through crystallographic and PFM studies, emphasize its potential for next-generation electronics [73–75]. Its room-temperature ferroelectricity, coupled polarization states, and tunable electronic properties establish α-In_2Se_3 as a leading material for future applications in memory, transistors, and optoelectronic devices.

4 | Fundamental Principles and Device Concepts

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4.1. Physics of Field-Effect Transistors (FETs)

Field-effect transistors (FETs) are foundational components in modern electronics, enabling the control of electrical conductivity using an external electric field. A typical FET includes a gate, source, drain, and a semiconductor channel. By applying a voltage to the gate terminal, the carrier concentration in the semiconductor channel can be modulated, enabling precise control over the current flowing from the source to the drain.

4.1.1. Metal-Insulator-Semiconductor Field-Effect Transistor (MISFET)

One common type of FET is the Metal-Insulator-Semiconductor Field-Effect Transistor (MISFET), as shown in Fig. 4.1(a). A MISFET comprises a metallic gate, a semiconducting layer, and an insulating layer, which electrically separates the gate from the semiconductor. Additionally, source and drain electrodes are used to facilitate current flow.

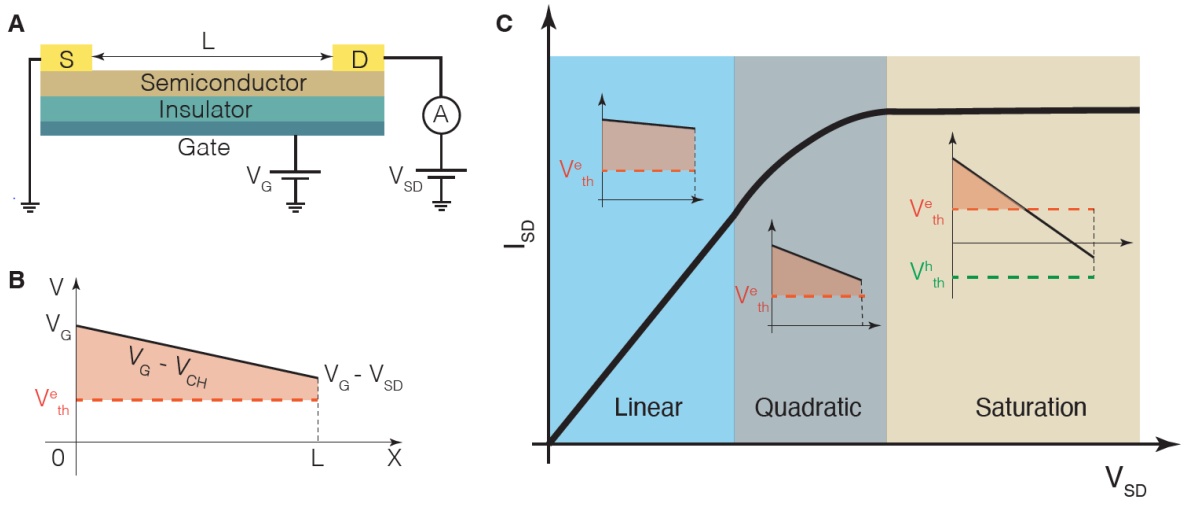


Figure 4.1: Illustration of the operating principles and regimes of a Metal-Insulator-Semiconductor Field-Effect Transistor (MOSFET) under typical biasing conditions. (A) The schematic shows the source (S), drain (D), and gate electrodes along with the semiconductor channel. The gate voltage (V_G) modulates the effective potential of the channel, while the source-drain voltage (V_{SD}) drives the current (I_{SD}). (B) The effective channel potential ($V_{ch}(x)$) transitions from V_G at the source to $V_G - V_{SD}$ at the drain, with the carrier density and potential varying along the channel. (C) Output characteristics depict three key operational regimes: linear (current increasing linearly with V_{SD}), quadratic (transitional region), and saturation (current saturating as V_{SD} approaches $V_G - V_{th}$). These regimes highlight the interplay between V_G, V_{SD}, and the physical properties of the device [76].

In MISFET operation, applying a voltage to the gate creates an electric field that attracts or repels charge carriers (electrons or holes) in the semiconductor channel. This forms a conductive path between the source and drain, enabling current flow.

Apart from the gate voltage (V_G), the source-drain bias voltage (V_{SD}) significantly influences how the transistor operates. This influence becomes particularly evident in the current-voltage (I_{SD}-V_{SD}) characteristics, commonly referred as output curves. These curves are obtained by fixing the gate bias while sweeping the source-drain voltage. The operating behavior of FETs is determined by the interplay of the gate voltage (V_G) and the source-drain voltage (V_{SD}).

At low V_{SD}, the transistor behaves like a resistor, and the current increases linearly with V_{SD}, following Ohm's law. This region is called the **linear** or **ohmic region**. As V_{SD} increases further, the current begins to show a quadratic dependence on V_{SD}, marking the transition towards the **saturation region**. In this regime, as V_{SD} becomes sufficiently high, the current reaches a maximum value and saturates, becoming independent of further increases in V_{SD}.

To describe these operational regimes, the gradual channel approximation[77]and Ohm's law in differential form are applied to analyze the current flow in the transistor channel. Under this approximation, the potential across the channel changes gradually from the source ($V = 0$) to the drain ($V = V_{SD}$). This assumption holds well when the channel geometry is rectangular, and the channel length (L) is much greater than its width (W).

Equations and explanations used in this section are adapted from ref. [76, 78, 79].

Current Density and Charge Density

The current density (j) in the channel is given by Ohm's law in differential form:

$$j = ne\mu E \tag{4.1}$$

where n is the charge carrier density,e is the elementary charge, μ is the carrier mobility, E is the electric field within the channel.

The electric field (E) is defined as the spatial gradient of the potential:

$$E = -\frac{dV_{ch}(x)}{dx} \tag{4.2}$$

Here, $V_{ch}(x)$ represents the potential at a position x along the channel. The charge carrier density (n) is influenced by the gate voltage (V_G), and under the gradual channel approximation,

it can be expressed as:

$$n = \frac{C_G(V_G - V_{ch}(x) - V_{th})}{e} \tag{4.3}$$

where C_G is the gate capacitance per unit area, V_{th} is the threshold voltage, and $V_{ch}(x)$ is the local channel potential.

Deriving the Drain-Source Current (I_{SD})

To determine the total current flowing through the transistor channel, we begin with Ohm's law in differential form. The current density (j) can be expressed as:

$$j = \mu C_G \left(V_G - V_{ch}(x) - V_{th}\right) \frac{dV_{ch}(x)}{dx} \tag{4.4}$$

Integrating the current density over the cross-sectional area of the channel (W) gives the total current (I_{SD}):

$$I_{SD} = W \cdot j = W\mu C_G \left(V_G - V_{ch}(x) - V_{th}\right) \frac{dV_{ch}(x)}{dx} \tag{4.5}$$

Here, I_{SD} is constant and does not depend on the coordinate x along the channel. Solving the first-order differential eq. (4.5) for the channel potential $V_{ch}(x)$ gives:

$$V_{ch}(x) = V_G - V_{th} - \sqrt{(V_G - V_{th})^2 - \frac{2I_{SD}}{W\mu C_G}x} \tag{4.6}$$

The boundary condition $V_{ch}(x = L) = V_{SD}$ (where L is the channel length) allows us to solve for I_{SD} explicitly. Substituting into the expression for I_{SD}, we obtain:

$$I_{SD} = \frac{W}{L}\mu C_G \left[(V_G - V_{th})V_{SD} - \frac{V_{SD}^2}{2}\right] \tag{4.7}$$

This final expression for I_{SD} describes the current as a function of the gate voltage (V_G), the source-drain voltage (V_{SD}), and the physical parameters of the transistor, such as channel width (W), length (L), mobility (μ), and gate capacitance (C_G).

Operational Regimes of FETs

The operational regimes of a FET, as illustrated in Figure 2.1C, are determined by the relationship between V_{SD} and $V_G - V_{th}$:

1. **Linear Region** ($V_{SD} \ll V_G - V_{th}$):
   In the linear or ohmic region, the current increases linearly with V_{SD}. In this regime, the effective potential varies smoothly along the channel, as shown in the blue region of Fig. 4.1C. The current is approximately:

$$I_{SD} \approx \frac{W}{L} \mu C_G (V_G - V_{th}) V_{SD} \tag{4.8}$$

2. **Quadratic/Transition Region** (V_{SD} comparable to $V_G - V_{th}$):
   As V_{SD} increases further, the current begins to exhibit a quadratic dependence on V_{SD}. This region lies between the linear and saturation regions and represents a transition in the device behavior, as seen in the middle region of Fig. 4.1C.

3. **Saturation Region** ($V_{SD} \geq V_G - V_{th}$):
   In this regime, the channel near the drain is "pinched off" and the current saturates at a maximum value, independent of further increases in V_{SD}. This behavior is shown in the red region of Fig. 4.1C, and the saturation current is given by:

$$I_{SD} = \frac{W}{2L} \mu C_G (V_G - V_{th})^2 \tag{4.9}$$

4.2. Ferroelectric Field-Effect Transistor (FeFET)

Ferroelectric Field-Effect Transistors (FeFETs) are an enhanced variation of conventional Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs). The primary distinction is the inclusion of a ferroelectric material within the gate dielectric or insulator stack. This structural modification grants FeFETs with unique properties such as nonvolatile memory storage, tunable threshold voltages, and hysteresis in their current-voltage ($I_{SD} - V_{GS}$) characteristics. These distinctive features originate from the ferroelectric material's ability to retain spontaneous polarization even after the external electric field is removed.

Role of ferroelectric layers in gate control

Key equations and explanations used in this section is adapted from S. Miller et al. 1992 [80].

As shown in Fig. 4.2, the incorporation of a ferroelectric layer, often combined with other dielectric materials, alters the effective capacitance of the gate. This modified capacitor structure can be analyzed using Maxwell's equations, which govern the electrostatic behavior.

The relationship is given by:

$$\nabla \cdot \mathbf{D} = \rho \tag{4.10}$$

Here, ρ represents the free charge density, and the displacement field $\mathbf{D}$ is expressed as:

$$\mathbf{D} = \epsilon_0 \epsilon_r \mathbf{E} + \mathbf{P} \tag{4.11}$$

where ϵ_0 is the permittivity of free space, ϵ_r is the relative permittivity of the material, $\mathbf{E}$ is the electric field, and $\mathbf{P}$ is the polarization in the material. The total polarization includes both linear dielectric contributions and nonlinear components arising from switching dipoles, described as:

$$\mathbf{D} = \epsilon_0 \epsilon \mathbf{E} + \mathbf{P}_d \tag{4.12}$$

In this expression, $\epsilon = 1 + \chi$ is the dielectric constant, and $\mathbf{P}_d$ represents the nonlinear polarization from dipole switching, a phenomenon unique to the ferroelectric layer.

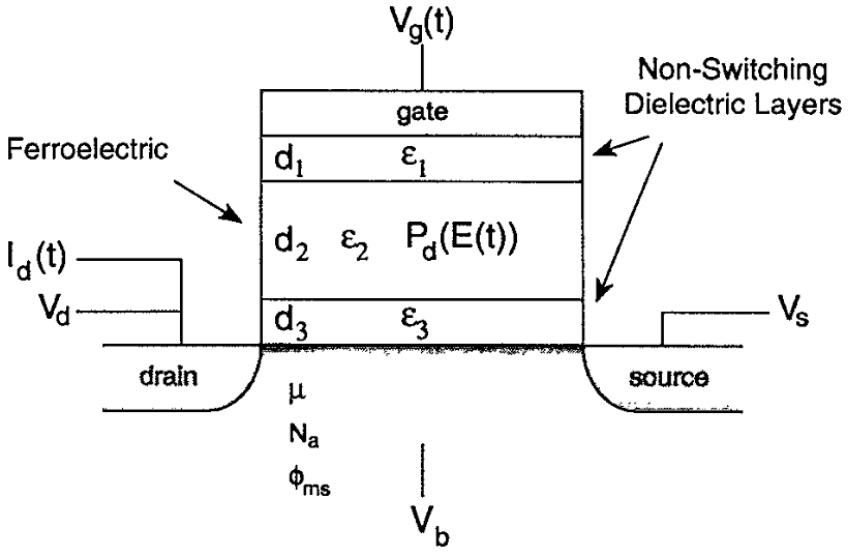


Figure 4.2: Cross-sectional schematic of a Ferroelectric Memory Field-Effect Transistor (FEMFET). The gate dielectric stack consists of a ferroelectric layer (d_2) sandwiched between two non-switching dielectric layers (d_1 and d_3). The ferroelectric layer introduces nonlinear polarization effects that influence the electric field (E) and overall gate control [80].

Electric Field Dynamics

Within the ferroelectric layer, the electric displacement field accounts for linear dielectric responses and nonlinear ferroelectric polarization effects. It is mathematically expressed as:

$$D = \epsilon_0 \epsilon_r E + P_d \tag{4.13}$$

where D is the electric displacement field, ϵ_0 is the permittivity of free space, ϵ_r is the relative permittivity of the ferroelectric material, E is the electric field, and P_d is the polarization resulting from the spontaneous alignment of dipoles in the material. Furthermore, the electric field within the ferroelectric layer, denoted as E_{FE}, depends on the surface charge density σ_s and the ferroelectric polarization P_d. According to Gauss's law, the relationship is given by:

$$E_{\mathsf{FE}} = -\frac{\sigma_s + P_d}{\epsilon_0 \epsilon_{\mathsf{FE}}} \tag{4.14}$$

where ϵ_{FE} is the permittivity of the ferroelectric material. This equation highlights how the surface charge and polarization interact to influence the electric field in a nonlinear manner, a characteristic absent in traditional MOSFETs and critical to FeFET functionality.

Polarization and Hysteresis

Since the dipole polarization depends on the history of the applied electric field, we determine the polarization by integrating $dP_d(E)/dE$ from a specified initial condition. The function $dP_d(E)/dE$ describes the change in polarization with respect to the electric field, capturing the hysteretic behavior of ferroelectric materials. Based on prior studies by S. L. Miller et al. [81] [82], simplified polarization response for the positive-going branch of the hysteresis loop is given by:

$$P^{+}_{\mathsf{sat}}(E) = P_s \cdot \tanh\left(\frac{E - E_c}{\delta}\right) \tag{4.15}$$

where P_s is the spontaneous polarization (the maximum achievable polarization), E_c is the coercive field required to switch the polarization direction, and δ is the saturation constant that governs the sharpness of the transition near E_c. For the negative-going branch, the response is:

$$P^{-}_{\mathsf{sat}}(E) = -P_s \cdot \tanh\left(\frac{E - E_c}{\delta}\right) \tag{4.16}$$

This hysteresis behavior reflects the material's capability to maintain distinct polarization states, which are instrumental in memory storage and nonvolatile operation.

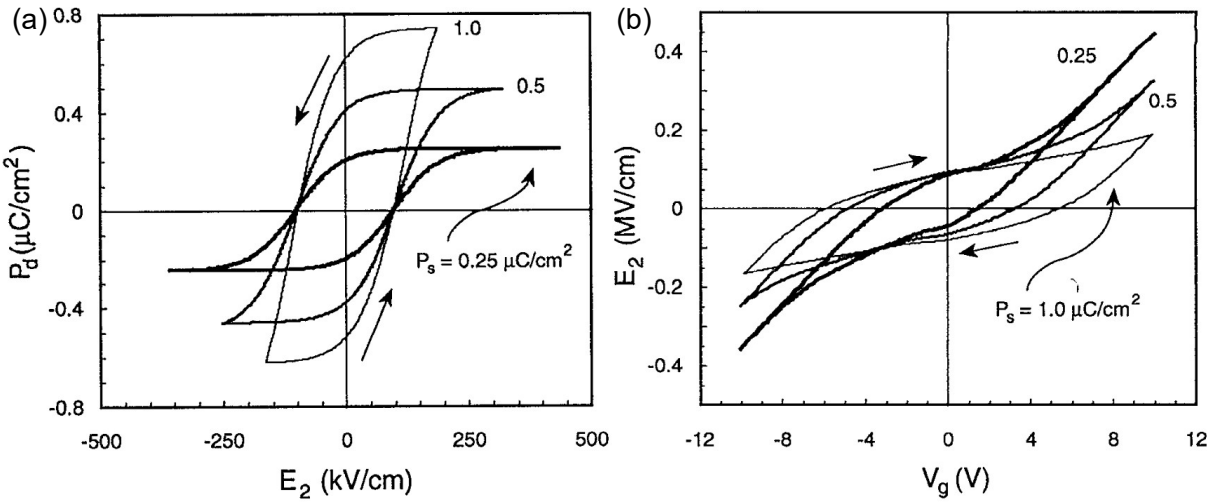


Figure 4.3: (a) The ferroelectric polarization (P_d) as a function of the ferroelectric field (E) exhibits a characteristic hysteresis loop, highlighting the presence of remanent polarization (P_r). (b) The hysteresis behavior of the ferroelectric field (E) versus gate voltage (V_g) follows an opposite trend compared to the polarization, leading to field reversal when the gate bias is reduced to zero. Note that , E_2 in the curve represents the electric field across the ferroelectric layer, which corresponds to E in the equations used [80].

Remanent polarization (P_r) refers to the polarization that remains even after the external electric field is removed ($E = 0$). Unlike spontaneous polarization (P_s), which represents the maximum polarization state, P_r can take two stable values: positive ($+P_r$) or negative ($-P_r$), depending on the direction of the previously applied electric field.

The magnitude of P_r can be derived by setting $E = 0$ in the polarization equation:

$$P_r = P_s \cdot \tanh\left(\frac{-E_c}{\delta}\right) \tag{4.17}$$

Since hysteresis leads to two stable polarization states, FeFETs can store binary information, where $+P_r$ represents logic "1" when the polarization is aligned in one direction, while $-P_r$ represents logic "0" when the polarization is switched to the opposite direction. This bistable nature forms the foundation of FeFET-based nonvolatile memory, ensuring that data remains stored even without power.

Threshold Voltage Modification

The threshold voltage of an FeFET, V_{th}, is directly influenced by the ferroelectric polarization P_d, which introduces an additional voltage drop across the gate stack. This modified threshold voltage is given by:

$$V_{\text{th}}^{(\text{FE})} = \phi_{\text{ms}} + 2\phi_F + \frac{Q_{\text{dep}}}{C_{\text{ox}}} - \frac{P_d}{C_{\text{ox}}} \tag{4.18}$$

In this equation:

- ϕ_{ms} represents the metal-semiconductor work function difference, accounting for the inherent potential offset at the interface.
- $2\phi_F$ corresponds to twice the Fermi potential of the semiconductor, which reflects the required band bending for strong inversion.
- Q_{dep} is the depletion charge per unit area, representing the fixed charge in the depletion region of the semiconductor.
- C_{ox} denotes the gate oxide capacitance per unit area, which incorporates contributions from both the ferroelectric and dielectric layers in the gate stack.
- $-P_d/C_{\text{ox}}$ accounts for the voltage drop due to ferroelectric polarization, effectively modulating the threshold voltage.

Since P_d determines the polarization states, it can take values corresponding to the positive saturation polarization(P_{sat}^{+}) or the negative saturation polarization (P_{sat}^{-}), as described in Equations (4.15) and (4.16).

As a result, the modified threshold voltage (V_{th}^{FE}) will also exhibit bistable states, transitioning between V_{th}^{+} and V_{th}^{-} depending on the polarization state. This behavior is crucial for FeFET-based non-volatile memory, where the two threshold voltage states correspond to distinct logic states, enabling reliable data storage and retrieval.

Current-Voltage Characteristics

The modified threshold voltage directly influences the drain current (I_{DS}) of the FeFET. Substituting $V_{\text{th}}^{(\text{FE})}$ into the MOSFET equation (Eq. 4.7) gives:

$$I_{\text{DS}} = \mu C_{\text{ox}} \frac{W}{L} \left[(V_{\text{GS}} - V_{\text{th}}^{(\text{FE})}) V_{\text{DS}} - \frac{V_{\text{DS}}^2}{2} \right] \tag{4.19}$$

where μ is the carrier mobility, W/L is the channel width-to-length ratio. The $I_{\text{DS}} - V_{\text{GS}}$ characteristics exhibit a counterclockwise hysteresis loop, reflecting the bistable polarization

states.

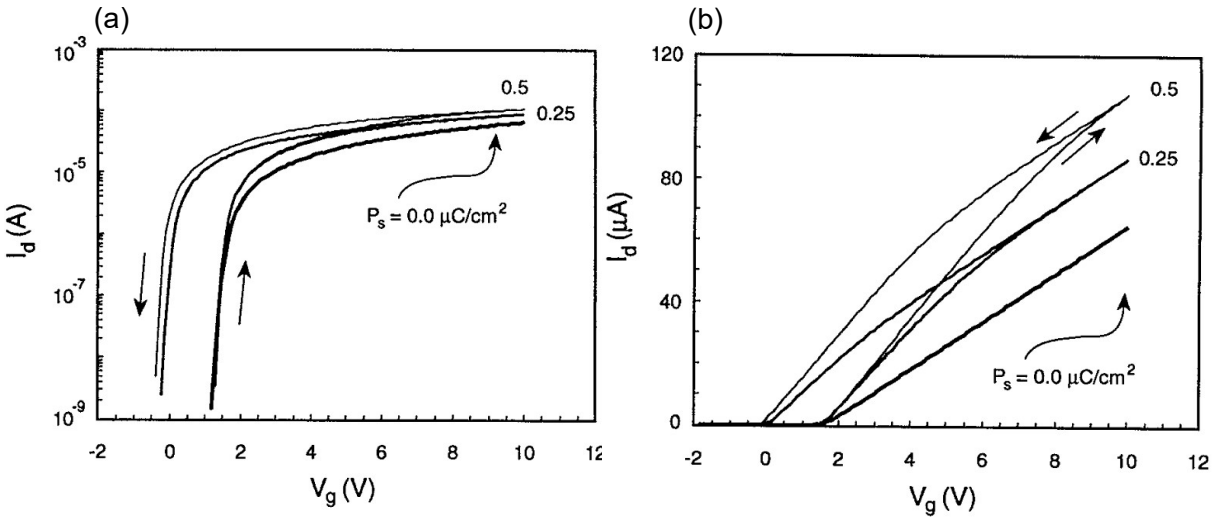


Figure 4.4: Transistor $I_d - V_g$ characteristics presents hysteresis due to ferroelectric switching. (a) and (b) presents the same data but with log and linear current scale, respectively [80].

Since the threshold voltage (V_{th}^{FE}) is influenced by ferroelectric switching, the shift in V_{th} is governed by the coercive field (E_c), while the spontaneous polarization (P_s) determines the current offset at higher voltages. The gate voltage modifies the polarization state, which in turn modulates V_{th}^{FE}. When the gate voltage is increased beyond the coercive voltage, polarization switching occurs, causing a shift in the threshold voltage ($V_{th}^{FE^+}$ and ($V_{th}^{FE^+}$). This behavior is clearly reflected as a hysterisis in the transconductance characteristics of the FeFET, as seen in the $I_{DS} - V_{GS}$ curve in Fig. 4.4.

4.2.1. Negative Capacitance Field-Effect Transistor (NCFET)

Negative Capacitance Field Effect Transistors (NCFETs) [83] [84] are a novel variation of conventional MOSFETs, developed to address critical challenges such as power dissipation, high threshold voltage (V_{TH}), and the limitations of subthreshold swing (SS). NCFETs incorporate a ferroelectric material in the gate stack, which introduces the phenomenon of *negative capacitance*. This unique property enables improved device performance by reducing V_{TH}, enhancing switching efficiency, and achieving a sub-60 mV/decade SS, making NCFETs a promising solution for next-generation low-power electronics. This section and the accompanying equations are adapted from B. Awadhiya et al. 2021 [85]

Subthreshold Swing (SS)

The subthreshold swing (SS) [86] [36] is a key parameter in transistor performance, representing the gate voltage required to increase the drain current by one order of magnitude. In traditional MOSFETs, SS is limited by the Boltzmann thermal limit, as expressed by:

$$SS_{\text{MOSFET}} = 2.3\frac{k_B T}{q}\left(1 + \frac{C_{\text{dep}}}{C_{\text{ox}}}\right) \tag{4.20}$$

In this equation, k_B is the Boltzmann constant, T is the temperature, q is the electronic charge, C_{dep} is the depletion capacitance and C_{ox} is the oxide capacitance. The minimum achievable SS for MOSFETs is 60 mV/decade because the body factor $(1 + C_{\text{dep}}/C_{\text{ox}})$ is always greater than unity. This limitation restricts the scalability and power efficiency MOSFETs.

Ferroelectric materials, which possess negative capacitance, can be incorporated into the gate stack to address this issue [36]. The inclusion of the ferroelectric material modifies the effective oxide capacitance (C'_{ox}) in the device, resulting in a modified SS expression:

$$SS_{\text{NCFET}} = 2.3\frac{k_b T}{q}\left(1 + \frac{C_{\text{dep}}}{C'_{\text{ox}}}\right) \tag{4.21}$$

In NCFETs, the equivalent oxide capacitance (C'_{ox}) is the series combination of dielectric capacitance (C_{ox}) and the ferroelectric capacitance (C_F). The effective oxide capacitance is given by:

$$C'_{\text{ox}} = \frac{C_{\text{ox}}|C_F|}{|C_F| - C_{\text{ox}}} \tag{4.22}$$

When C'_{ox} is negative, which occurs when $C_{\text{ox}} > |C_F|$, the subthreshold swing (SS) can drop below the Boltzmann limit of 60 mV/decade. This reduction in SS improves switching efficiency and reduces power consumption in NCFETs.

Threshold Voltage (V_{TH})

Threshold voltage (V_{TH}) is another critical parameter in transistor operation. It is the minimum gate voltage required to create an inversion layer in the channel. For MOSFETs, V_{TH} is expressed as:

$$V_{TH} = V_{FB} + \phi_f + \frac{eN_a x_{dT}}{C_{\text{ox}}} \tag{4.23}$$

Here, V_{FB} is the flat-band voltage, ϕ_f is the built-in potential determined by the doping concentration (N_a) and intrinsic carrier concentration (n_i), e is the electron charge, x_{dT} is the maximum depletion width, and C_{ox} is the oxide capacitance.

In NCFETs, the oxide capacitance C_{ox} is replaced by the modified capacitance C'_{ox}. Substituting the value of C'_{ox} into Eq. (4.23), the threshold voltage becomes:

$$V'_{TH} = V_{FB} + \phi_{fp} + \frac{eN_a x_{dT}}{C_{\text{ox}}} - \frac{eN_a x_{dT}}{|C_F|} \tag{4.24}$$

Simplifying further, the final threshold voltage expression for NCFETs is:

$$V'_{TH} = V_{TH} - \frac{eN_a x_{dT}}{|C_F|} \tag{4.25}$$

Negative capacitance reduces the subthreshold voltage compared to conventional MOSFETs, enabling efficient operation at lower gate voltages.

Short-Channel effect

Drain-Induced Barrier Lowering (DIBL)

Drain-Induced Barrier Lowering (DIBL) is a short channel effects [87], which describes the sensitivity of threshold voltage to changes in drain voltage (V_D). For MOSFETs, increasing V_D reduces V_{TH}, leading to increased leakage currents. This behavior is expressed as:

$$V_{TH} = V_{TH0} - \eta V_D \tag{4.26}$$

where V_{TH0} is the threshold voltage at zero drain bias, and η is the DIBL factor. DIBL can be computed from the following expression:

$$\text{DIBL} = -\frac{V_{TH}^H - V_{TH}^L}{V_D^H - V_D^L} \tag{4.27}$$

MOSFETs typically exhibit a positive DIBL factor, indicating a decrease in V_{TH} with increasing V_D.

In contrast, NCFETs exhibit a reverse DIBL effect[84] [35]. Due to the influence of negative capacitance, the threshold voltage increases with a higher drain voltage. The internal voltage (V_{MOS}) in NCFETs is influenced by both gate voltage (V_G) and drain voltage (V_D):

$$V_{MOS} = \frac{|C_F|V_G}{|C_F| - C_{\text{MOS}}} - \frac{C_D V_D}{|C_F| - C_{\text{MOS}}} \tag{4.28}$$

Here, C_{MOS} is the combined MOS capacitance, and C_D is the drain capacitance. This leads to a negative DIBL factor, described as:

$$V'_{TH} = V'_{TH0} + |\eta| V_D \tag{4.29}$$

The negative DIBL reduces leakage currents and enhances the robustness of NCFETs against short-channel effects, making them highly suitable for scaled-down transistor technologies.

4.3. Ferroelectric-Semiconductor Field-effect Transistor (FeSFET)

In the previous section (4.2), I discussed ferroelectric field-effect transistors (FeFETs), where the conventional dielectric insulator is replaced by a ferroelectric insulator. In this section, I introduce a different device architecture, the ferroelectric semiconductor field-effect transistor (FeS-FET), in which the ferroelectric insulator is replaced by a ferroelectric semiconductor, fundamentally altering its charge transport mechanisms.

4.3.1. Structural and Operational Differences Between FeFET and FeS-FET

FeFETs and FeS-FETs differ primarily in their use of ferroelectric materials and charge transport behavior. In a FeFET, a traditional ferroelectric insulator is used as the gate dielectric, where only polarization-bound charges exist at the ferroelectric/semiconductor interface. These charges modulate the conductivity of the channel by switching the polarization state in ferroelectric material in response to the applied gate voltage.

In contrast, FeS-FETs [88–90] utilize a ferroelectric semiconductor [71] as the channel material, introducing both polarization-bound charges and mobile carriers within the semiconductor itself. This additional degree of freedom significantly affects the charge accumulation process. When a positive gate voltage is applied, the polarization state is oriented upward, leading to the accumulation of negative mobile charges at the top surface and positive mobile charges at the bottom. Under a negative gate voltage, the polarization reverses, redistributing the mobile charges.

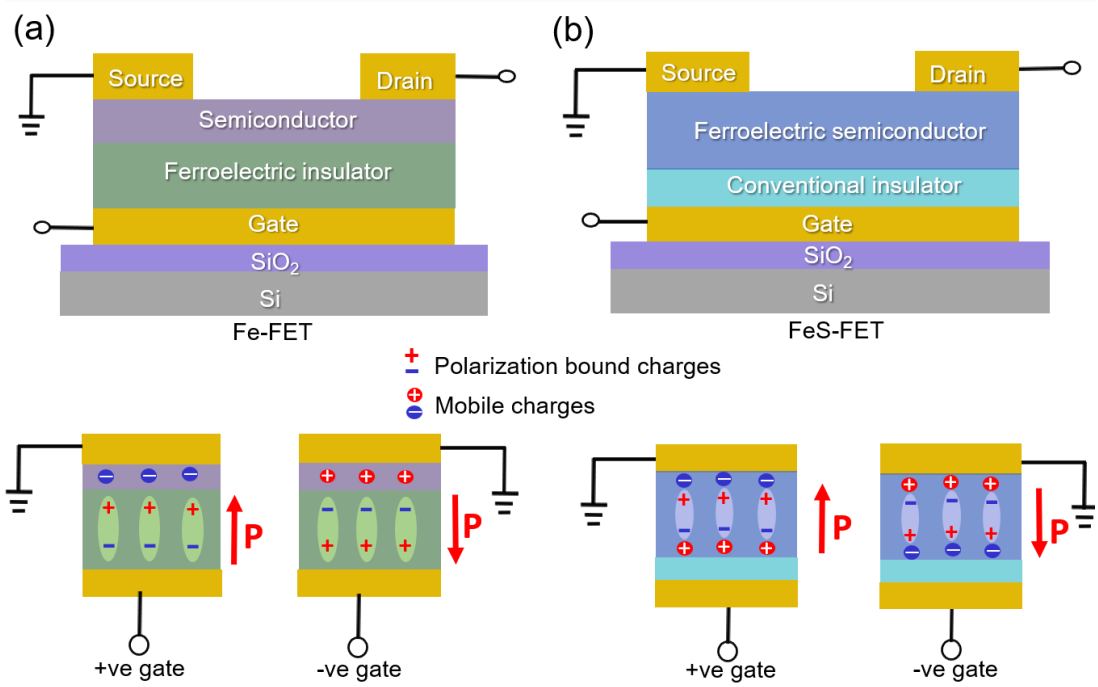


Figure 4.5: Structural Comparison of FeFET and FeS-FET. (a) FeFET structure with a ferroelectric insulator as the gate dielectric, where polarization-bound charges modulate the channel conductance. (b) FeS-FET structure, where a ferroelectric semiconductor replaces the dielectric, leading to both polarization-bound and mobile charge accumulation. The lower panels illustrate charge distributions under different gate voltages, showing the impact of polarization on charge transport.

These structural differences result in unique charge transport behaviors. In FeFETs, the channel conductance is controlled solely by the mobile charges induced by ferroelectric polarization. However, in FeS-FETs, the presence of mobile carriers in addition to polarization-bound charges leads to a built-in electric field that stabilizes polarization states. This makes FeS-FETs promising candidates for memory and logic applications.

4.3.2. Transconductance and Working Mechanism of FeS-FET

The charge transport in FeS-FETs [91] is strongly influenced by the penetration of the gate electric field, which depends on the equivalent oxide thickness (EOT) [87]. EOT represents the thickness of silicon dioxide that would be required to achieve the same capacitance as the actual gate dielectric. The degree of field penetration affects the polarization switching and, consequently, the electrical response of the transistor.

When EOT is low, the gate electric field fully penetrates the semiconductor channel, en-

abling complete polarization switching. In the polarization-down state, positive and negative polarization-bound charges accumulate at the bottom and top surfaces, respectively, preventing electron accumulation at the top surface and resulting in a high channel resistance. Conversely, in the polarization-up state, charge distribution shifts, allowing electron accumulation on the top surface, leading to a low-resistance state. This behavior produces a counterclockwise hysteresis loop in the I_{DS}-V_{GS} curve, similar to FeFETs, where negative voltages below the coercive voltage (V_{FE}^{-}) induce downward polarization and positive voltages above the coercive voltage (V_{FE}^{+}) induce upward polarization.

However, when EOT is high, the gate field is weaker and does not fully penetrate the semiconductor, leading to partial polarization switching confined to the oxide/semiconductor interface. In this case, the polarization-down state results in mobile charge accumulation at the bottom interface, reducing resistance, whereas in the polarization-up state, fewer mobile charges are present at the bottom, increasing the channel resistance. This scenario leads to a clockwise hysteresis loop in the I_{DS}-V_{GS} curve, characteristic of partial polarization switching.

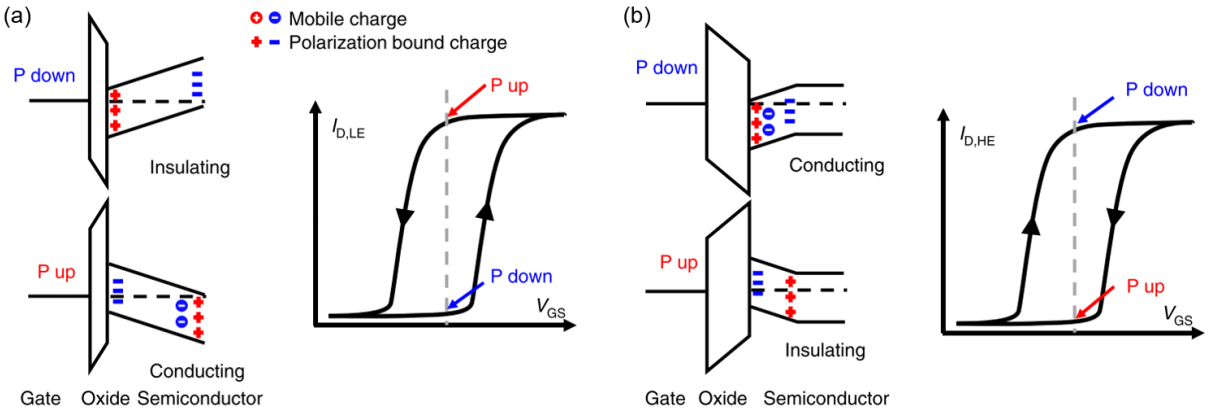


Figure 4.6: Band Diagrams and I_{DS}-V_{GS} Characteristics of FeS-FET. (a) Low EOT condition, where the electric field fully penetrates the semiconductor, enabling complete polarization switching and resulting in a counterclockwise hysteresis loop in the I_{DS}-V_{GS} curve. (b) High EOT condition, where partial polarization switching occurs due to limited field penetration, leading to a clockwise hysteresis loop [92].

These mechanisms highlight the role of EOT in modulating the electrical behavior of FeS-FETs. By carefully tuning EOT, it is possible to optimize the device for specific applications, such as non-volatile memory applications [73].

4.4. Synaptic Devices

The human brain is an efficient and highly parallel computing system, performing complex cognitive tasks such as pattern recognition, learning, and decision-making while consuming minimal power. This capability is attributed to a dense network of biological synapses that dynamically adjust their strength in response to external stimuli. Inspired by this mechanism, artificial synaptic devices aim to mimic these functions in hardware, enabling neuromorphic computing systems with energy-efficient learning and memory capabilities.

Among the various emerging technologies, ferroelectric-based synaptic devices, particularly ferroelectric field-effect transistors (FeFETs), have garnered attention due to their low-power operation, non-volatile storage, and compatibility with existing semiconductor fabrication techniques. FeFETs exploit the remanent polarization of ferroelectric materials such as hafnium oxide and hafnium zirconium oxide to modulate their conductance state, thereby emulating the analog weight updates observed in biological synapses. Utilizing these properties, FeFET-based synapses offer a promising platform for neuromorphic computing, where information is stored and processed within the same physical location, thereby eliminating the von Neumann bottleneck.

4.4.1. Biological and Artificial Synapses

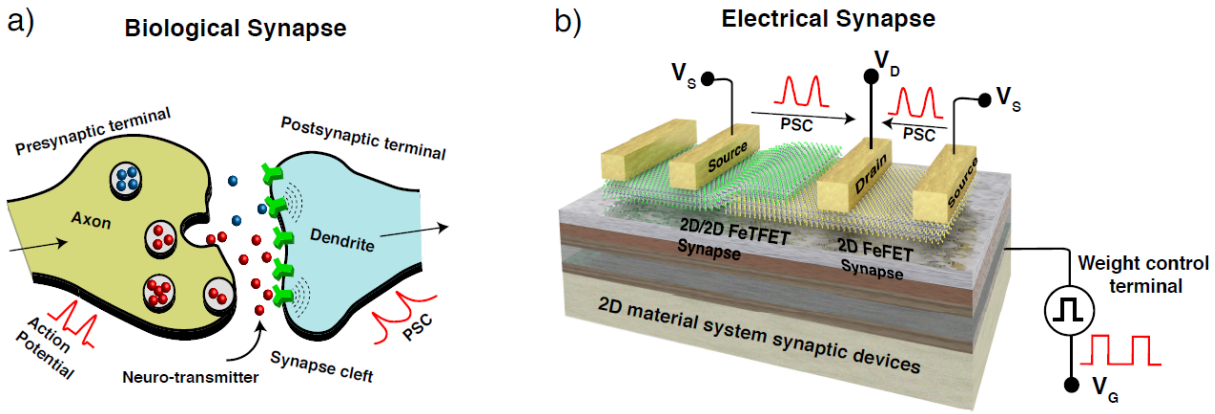


Figure 4.7: (a) Schematic of a biological synapse where neurotransmitters mediate signal transmission, producing a postsynaptic current (PSC) at the postsynaptic terminal. (b) Ferroelectric synaptic devices based on WSe_2 FeFET and $WSe_2/SnSe_2$ FeTFET structures, where gate voltage pulses induce polarization switching to emulate synaptic weight changes. The PSC (postsynaptic current), representing the drain current, is recorded after each pulse to reflect the synaptic response [93].

In biological neural networks [94], synapses mediate communication between neurons by transmitting electrical or chemical signals. When an action potential reaches the presynaptic terminal, neurotransmitters are released into the synaptic cleft and bind to receptors on the postsynaptic membrane, modulating the postsynaptic current. The strength of this connection is dynamically altered through synaptic plasticity, a process that enables learning and the formation of memory. The two fundamental mechanisms underlying synaptic plasticity are long-term potentiation, where the synaptic strength increases, and long-term depression, where synaptic strength decreases.

Artificial synapses [95] based FeFETs replicate key features of biological synapses by modulating the channel conductance through electric-field-induced polarization switching. As shown in Fig.4.7, the biological synapse (Fig.4.7(a)) transmits signals from the presynaptic to the postsynaptic terminal using neurotransmitters, generating a measurable postsynaptic current (PSC) in the receiving neuron. In analogy, the artificial synapse (Fig. 4.7(b)) mimics this behavior by applying gate voltage pulses that switch the polarization of the ferroelectric layer. This results in a controllable change in channel conductance, and the corresponding drain current is measured as the PSC after each pulse is removed.

4.4.2. Working Mechanism of FeFET-Based Synapses

Ferroelectric Polarization and Conductance Modulation

FeFET-based synapses function by modulating the polarization state of a thin ferroelectric layer in response to applied gate voltage pulses. The underlying mechanism relies on the ability of ferroelectric materials to retain their polarization state after the removal of an electric field, allowing for non-volatile conductance tuning. When a positive voltage pulse is applied to the FeFET gate, the polarization aligns in one direction, shifting the threshold voltage and increasing the channel conductance. Conversely, applying a negative voltage pulse reverses the polarization, decreasing the conductance.

FeFET-Based Synapses in Crossbar Arrays

To implement large-scale neuromorphic computing, FeFET synapses are integrated into crossbar arrays, where each device functions as a programmable weight element. Fig. 4.8(a) illustrates such a crossbar architecture, where FeFET synapses are arranged in a matrix format, enabling efficient hardware-based vector-matrix multiplication. A detailed structure of an FeFET synapse is shown in Fig. 4.8(b), where a 10 nm hafnium zirconium oxide ferroelectric layer governs the threshold voltage and conductance state.

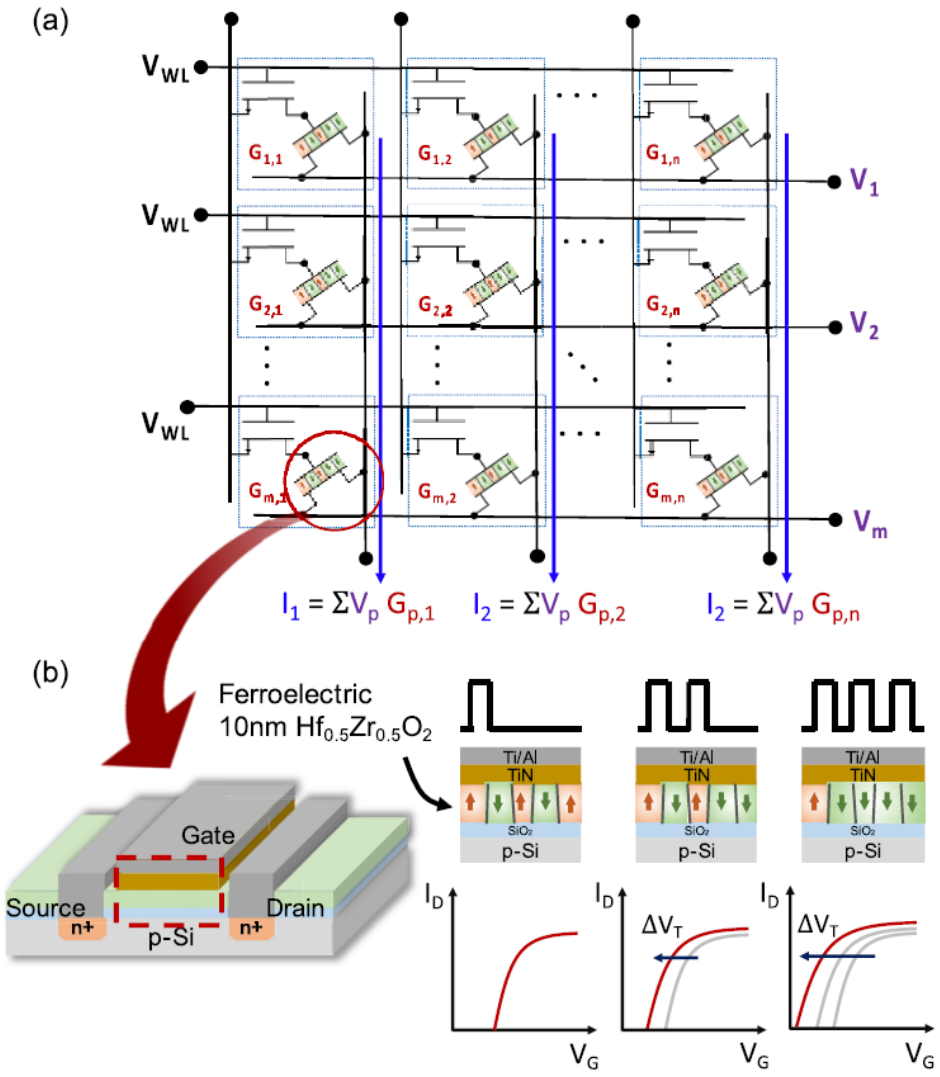


Figure 4.8: (a) Crossbar array where FeFETs store synaptic weights as conductance values. (b) Detailed structure of an FeFET synapse with ferroelectric-based weight modulation [96].

4.4.3. Synaptic Weight Modulation Using Different Pulse Schemes

The effectiveness of FeFET synapses depends on the precision of their conductance modulation. To achieve this, different pulse schemes are employed to control polarization switching. Fig. 4.9 presents experimental data showcasing three distinct programming schemes.

In the identical pulse scheme shown in Fig. 4.9(a), fixed-amplitude pulses are applied to the FeFET gate, resulting in gradual potentiation and abrupt depression. In contrast, variable pulse width scheme in Fig. 4.9(b) uses increasing pulse durations, enabling smoother transitions between conductance states. The most effective approach, shown in Fig. 4.9(c), employs variable pulse amplitudes, achieving symmetric weight updates and a larger dynamic range.

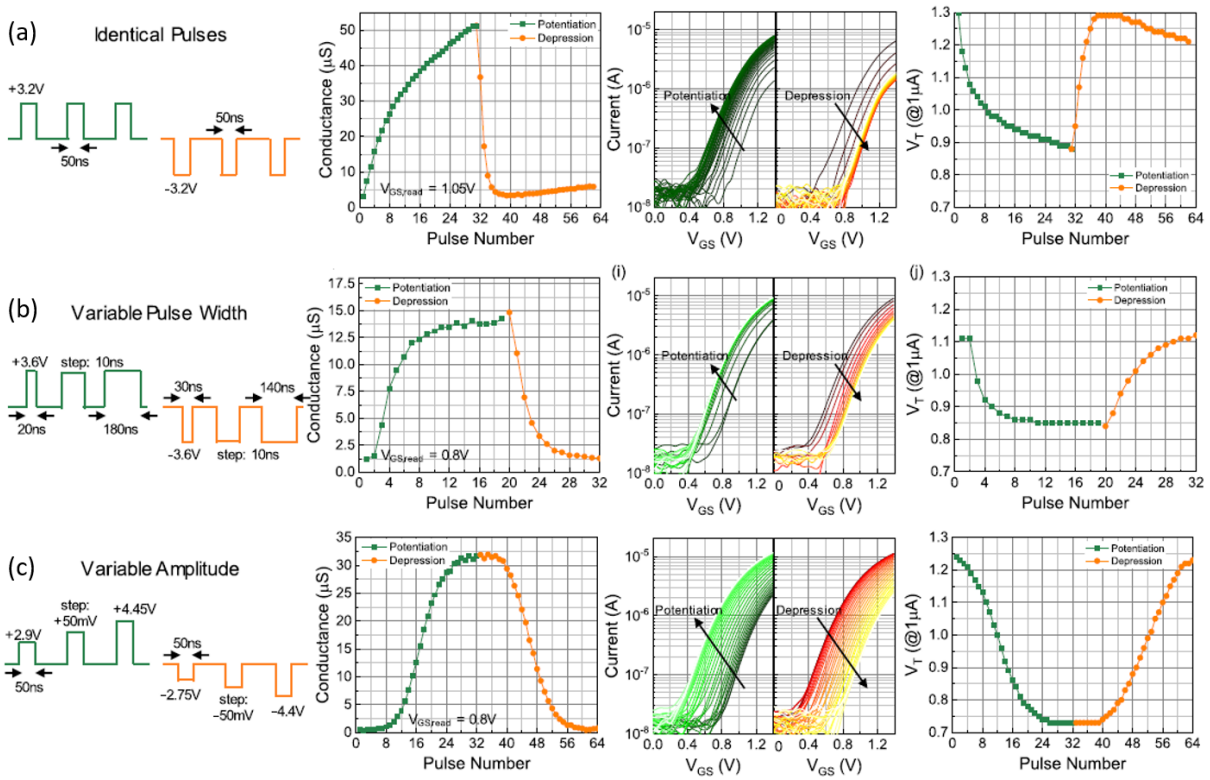


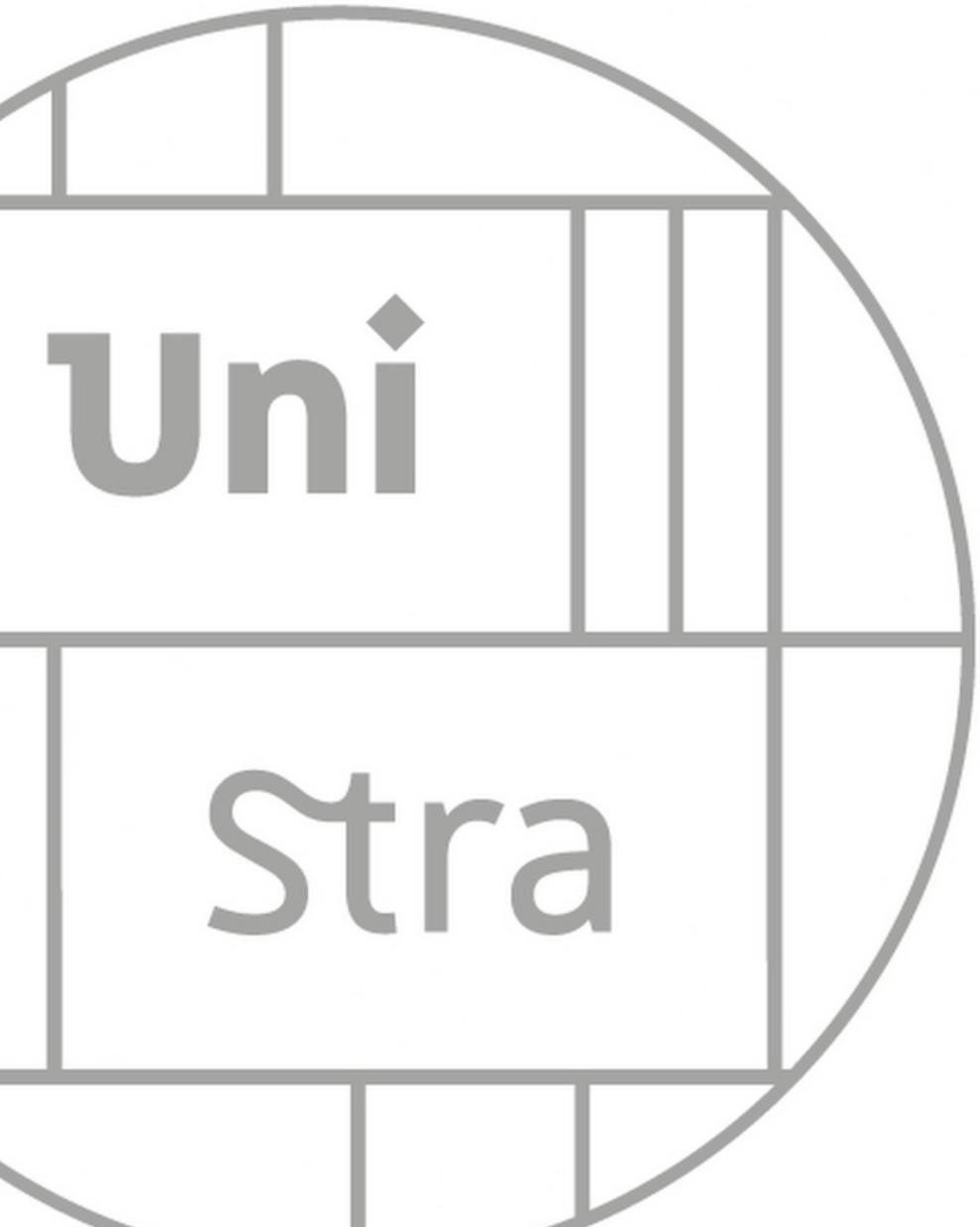
Figure 4.9: (a) Identical pulses result in abrupt potentiation and depression, leading to asymmetry in weight updates. (b) Variable pulse width improves control over conductance modulation. (c) Variable amplitude scheme provides symmetric weight updates and higher precision [96].

FeFET-based synaptic devices offer a promising route toward energy-efficient and scalable neuromorphic computing, bridging the gap between biological and artificial intelligence. By leveraging ferroelectric polarization switching, these devices achieve non-volatile synaptic weight modulation, mimicking key aspects of biological synapses. The integration of FeFET synapses into crossbar arrays enables efficient in-memory computation, reducing energy consumption and enhancing parallel processing capabilities.

Experimental studies demonstrate the feasibility of precise weight tuning using various pulse engineering techniques, with variable amplitude modulation providing the most accurate conductance control. However, challenges such as device variability, endurance constraints, and non-linearity still need to be addressed. Future research will focus on optimizing material properties and fabrication techniques to enhance device stability and scalability. With continued advancements, FeFET-based artificial synapses have the potential to revolutionize neuromorphic computing [97], enabling next-generation AI hardware [98].

PartII

Experimental Work and Results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5 | Device Fabrication and Characterization Techniques

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5.1. Methods

5.1.1. Mechanical Exfoliation

Mechanical exfoliation is a highly efficient technique for obtaining single-crystal 2D materials. This approach is particularly beneficial for producing high-quality 2D materials without introducing defects. By applying mechanical force to van der Waals bulk crystals, the weak interlayer van der Waals bonds break without disrupting the in-plane crystal structure, leading to the formation of atomically thin nanoflakes.

During my PhD research, I used mechanical exfoliation to obtain 2D layers of desired materials. The standard scotch tape method was employed, in which bulk crystals are repeatedly pressed against adhesive tape, causing the layers to separate. The tape containing exfoliated flakes was then pressed onto a substrate, ensuring proper adhesion and removal of air bubbles. I used commercially available viscoelastic PDMS substrates.

Following exfoliation, optical microscope inspection was performed to identify and isolate flakes with optimal characteristics and suitable thickness.

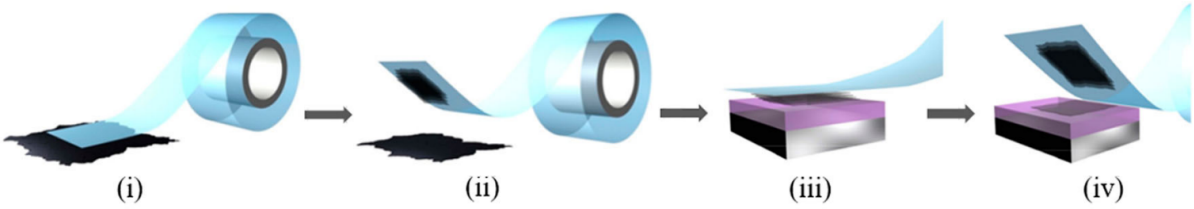

Figure 5.1: Schematic illustration of the mechanical exfoliation process (i) A piece of adhesive tape is pressed onto the surface of a 2D crystal. (ii) Few-layer crystal flakes adhere to the tape. (iii) The tape, carrying the exfoliated flakes, is then pressed onto a target substrate. (iv) The bottom most few-layer flake is transferred on the substrate after the tape is removed[99]

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5.1.2. 2D Stack Assembly

To assemble the desired stack, I used a custom-built micropositioning transfer station to precisely align and transfer/pick up the flakes onto the target substrate.

The following two dry transfer methods were used in this work:

Bottom-Up Method

In this technique, 2D flakes are initially transferred onto a PDMS stamp mounted on a glass slide. After selecting the appropriate flake, the PDMS stamp is carefully cut using a sharp blade to minimize its size while ensuring the flake remains intact. This step is crucial as it reduces unnecessary interactions with the substrate and prevents unwanted flake transfer to unintended areas. This is particularly important when working with pre-patterned electrodes, as it ensures device cleanliness and prevents electrical short circuits.

Once the flake is isolated on the PDMS, the transfer process is executed with controlled adhesion, thanks to the viscoelastic properties of PDMS. The target substrate is heated to approximately $45\,^{\circ}\mathrm{C}$, which allows controlled expansion of the PDMS stamp as it approaches the substrate. The PDMS is then gradually brought into contact with the substrate, with the temperature incrementally increased by $10\,^{\circ}\mathrm{C}$ to facilitate optimal adhesion of the 2D flake. Once the flake has adhered to the substrate, the PDMS is carefully retracted using a combination of mechanical and thermal control to avoid damage or misalignment.

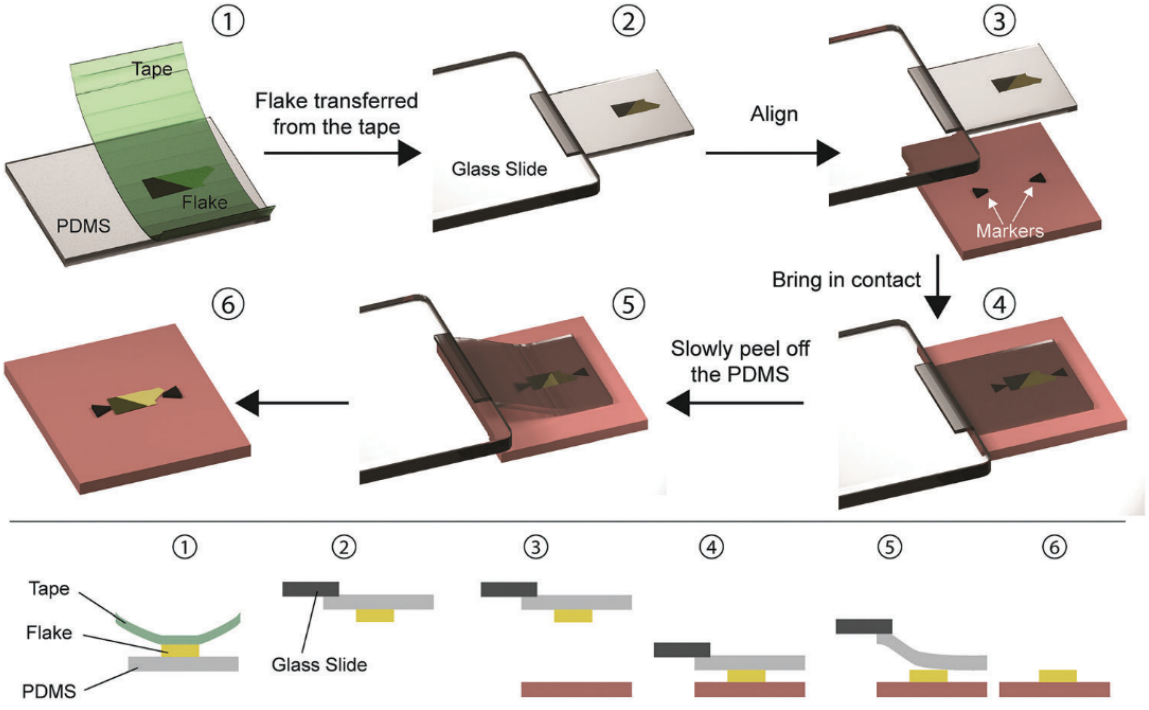


Figure 5.2: PDMS dry transfer method for Bottom-Up 2D stack assembly.[100]

This process is repeated iteratively for each additional 2D material, stacking them one by one to construct the desired 2D stack while ensuring precise alignment and minimal contamination.

Top-Down Method

This method follows a similar exfoliation process on a substrate, such as Si/SiO_2 or PDMS. Here, the first exfoliated layer is transferred onto the substrate, and subsequent flakes are sequentially picked up using a carrier consisting of a PC/PDMS stamp mounted on a glass slide to form the final stack.

The PC/PDMS stamp is prepared by depositing a thin polycarbonate (PC) layer onto a dome-shaped PDMS stamp affixed to a glass slide. In our work, a carrier system was used, comprising a thin PC film carefully placed on top of a small PDMS section ($0.5\,\mathrm{mm} \times 0.5\,\mathrm{mm}$) attached to a glass slide. The small PDMS size allows the PC film to form a slight curvature similar to a dome shape, facilitating selective pickup of target flakes from the substrate.

During the pickup process, the PC/PDMS stamp is brought into contact with the 2D flake on the substrate at around $120\,^{\circ}\mathrm{C}$. At this temperature, PC exhibits ideal viscoelastic properties that enable efficient adhesion and pickup of the flake. This process is repeated for each additional layer to construct a heterostructure consisting of different van der Waals materials on the PC film.

Once the complete stack is assembled on the PC/PDMS stamp, it is transferred onto the final target substrate at approximately $180\,^{\circ}\mathrm{C}$. At this temperature, the PC melts, allowing the release of the 2D material stack onto the substrate along with a thin residual PC layer. The remaining PC layer is subsequently removed by immersing the sample in acetone, followed by a thorough cleaning with isopropanol (IPA) to ensure a clean upper layer.

Both bottom-up and top-down transfer approaches offer precise control over 2D material stacking, enabling the fabrication of high-quality heterostructures for advanced device applications.

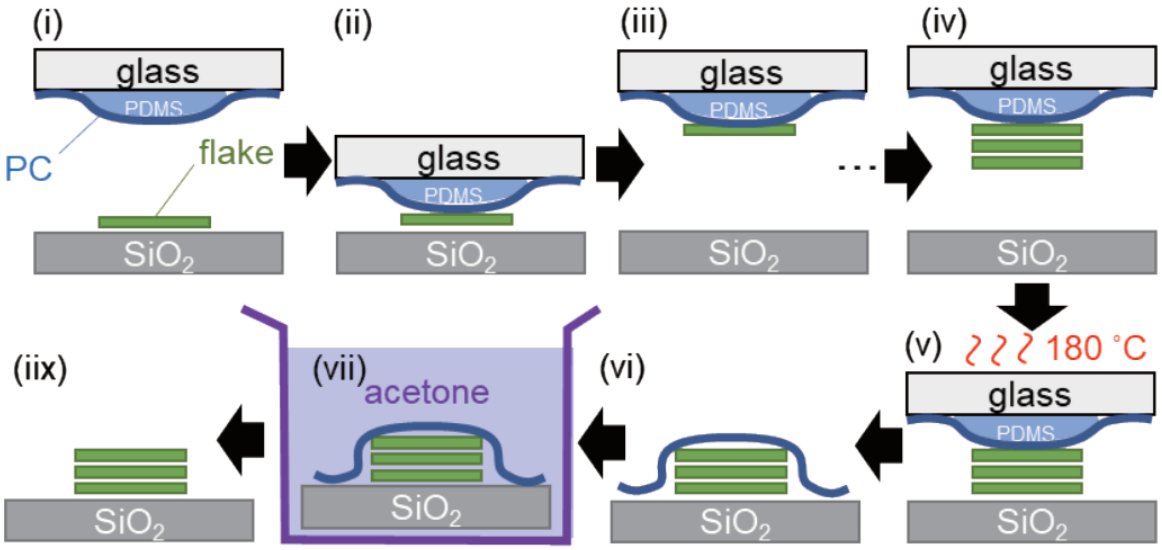


Figure 5.3: Top-Down approach for 2D stack assembly using PC/PDMS stamp [101]

5.1.3. Lithography

Electron Beam Lithography (EBL)

Electron beam lithography (EBL) is a high-precision technique used to create custom nanoscale patterns on surfaces. It employs a focused beam of electrons to draw patterns on a substrate coated with an electron-sensitive resist. The process consists of several key steps:

1. **Sample Preparation:**

   A Si/SiO_2 substrate (280 nm SiO_2) was thoroughly cleaned using acetone, ethanol, and isopropyl alcohol (IPA) in sequence. This was followed by oxygen plasma etching for 10 minutes to remove residual impurities and moisture, ensuring optimal adhesion and surface cleanliness.

2. **Resist Coating**

   The cleaned substrate was spin-coated with an electron-sensitive resist (PMMA) using a bilayer system comprising AR-P 669.04/AR-P 679.02 [102]. Spin coating was performed at 4000 rpm for 60 seconds, achieving a total resist thickness of approximately 270 nm. Each resist layer was subsequently baked at 120°C for 1 minute and 30 seconds to remove residual solvents and enhance structural integrity.

   - **Optimization for Top Electrode Patterning:** When patterning on a thick 2D

material stack (Fig. 5.5), spin-coating was optimized either by incorporating an additional resist layer or by reducing the spin speed (RPM) to achieve the necessary resist thickness. A metal deposition-to-resist thickness ratio of 1:3 was maintained to ensure a successful lift-off process.

- **Optimization for Insulating Surface Patterning:** For patterning on a 2D stack containing an insulating layer, an additional conductive resist layer (AR-PC 5090.02) [103] was incorporated. This conductive layer facilitated charge dissipation during e-beam exposure, thereby preventing charge accumulation and distortion of the pattern.

3. **Exposure**

   Patterning was performed using a Zeiss Supra 40 EBL system. The mask design was created using Raith Elphy Plus software, which is fully compatible with the EBL system. The sample was loaded into the chamber under ultra-high vacuum conditions, followed by advanced calibration procedures. Exposure was performed in a positive tone according to the predefined mask design. For standard designs with feature sizes in the micrometer range, a 30 μm aperture and a 20 kV accelerating voltage were used to optimize resolution and uniformity.

4. **Development**

   Following exposure, the resist was developed in a 1:3 solution of methyl isobutyl ketone (MIBK) and isopropyl alcohol (IPA) for 30 seconds. This was followed by immersion in a stopper solution for 30 seconds and subsequent drying with a nitrogen gun to ensure complete removal of any moisture.

5. **Deposition and Lift-Off**

   The developed pattern underwent a brief 3-second etching step before the deposition of a Ti/Au stack under high-vacuum conditions (10^{-7} mbar). Metal deposition was carried out using an MEB 550-S Plassys e-beam evaporator. Finally, the resist was lifted off in acetone, effectively removing excess material and leaving the well-defined metal pattern.

   - For top electrodes, etching was not performed, as it will direct etch exposed 2D layer.

- **Short-Channel Device Patterning**

The Zeiss Supra 40 EBL system at STNano is capable of achieving extremely high resolutions,

down to ≈ 10 nm. However, achieving such precision necessitates meticulous calibration and multiple processing steps to ensure nanoscale accuracy. Proper dose optimization is critical, as it directly influences resist exposure and ultimately determines the final dimension and quality of the feature.

In Ch. 7, devices with a channel length of 50 nm is discussed. To achieve such small dimensions, various design arrays with different exposure doses were tested under specialized conditions. A 10 μm aperture and a 30 kV accelerating voltage were used for fine-tuning the exposure.

Optical Laser Lithography

Contact pads for the devices were patterned using optical laser lithography. Compared to EBL, optical lithography requires significantly less calibration and optimization. Since large contact pads (e.g. 500 μm $\times$ 500 μm) do not necessitate high resolution, laser lithography was the most efficient approach in terms of effort and processing time.

The laser lithography process followed standard lithographic steps, including resist coating, exposure, and development:

1. **Sample Preparation:** The substrate was cleaned following the standard protocol to ensure surface purity, as described in the EBL section.
2. **Resist Coating:** A positive photoresist, AZ® 1505 resist [104], was spin-coated at 4000 rpm for 50 seconds to achieve a resist thickness of approximately 500 nm. The sample was then baked at 100°C to improve resist adhesion and reduce solvent content.
3. **Exposure:** A Heidelberg μPG101 maskless direct writer was used for exposure, which offers a resolution of approximately 1 μm.
4. **Development:** The exposed sample was developed in AZ® Developer MIC[105] for 20 seconds, followed by a thorough rinse in deionized (DI) water for 1 minute to remove residual developer and prevent overdevelopment.
5. **Deposition and Lift-Off:** The deposition process followed the same methodology as described in the EBL section.

Process Flow of Re-FeFET:

Here, I will outline the stepwise process flow for the device discussed in Ch. (6).

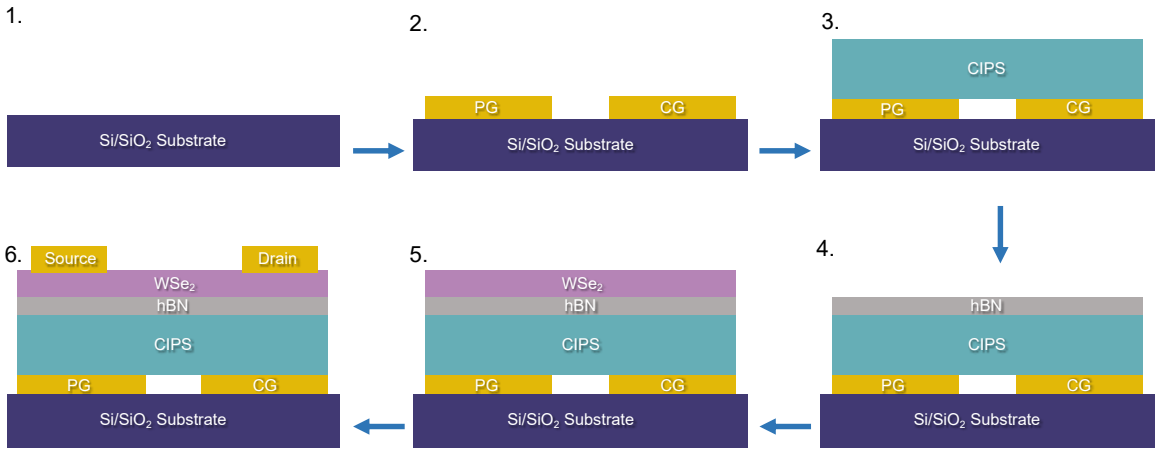


Figure 5.4: Process flow of device fabrication.

Split-gate electrodes were patterned on a silicon/silicon dioxide (Si/SiO_2) substrate using electron beam lithography (EBL). Next, van der Waals materials were exfoliated from their bulk 3D crystals using the Scotch tape exfoliation technique and transferred onto a PDMS polymer fixed on a glass slide. Optical images are provided in Fig. 5.4.

I fabricated three different Re-FeFET samples with typical material thicknesses (see Figure S.1.2.a-d): CIPS (90 nm, 200 nm, 380 nm), hBN (8 nm, 9 nm, 10 nm), and WSe_2 (2 nm, 3.5 nm, 4 nm). The height profile was measured using AFM after the 2D stack assembly step. I estimated the height error, considering surface roughness and possible interlayer water, in the range of ± 1 layer for WSe_2.

The 2D stack assembly was performed using the dry transfer method. This layer stacking process was repeated for each individual layer, leading to the formation of the desired stack. See Fig(5.4.3-5) for the schematic and Fig(5.5.ii-iv) for optical images.

Subsequently, top electrode patterning was accomplished using EBL with enhanced alignment techniques. The top surface of the layered stack was patterned using EBL exposure, followed by the deposition of a 10 nm titanium layer and a 150 nm gold layer via e-gun evaporation. The thicker Ti/Au top contact was designed to prevent cracks that may arise due to the increased thickness of the entire 2D stack.

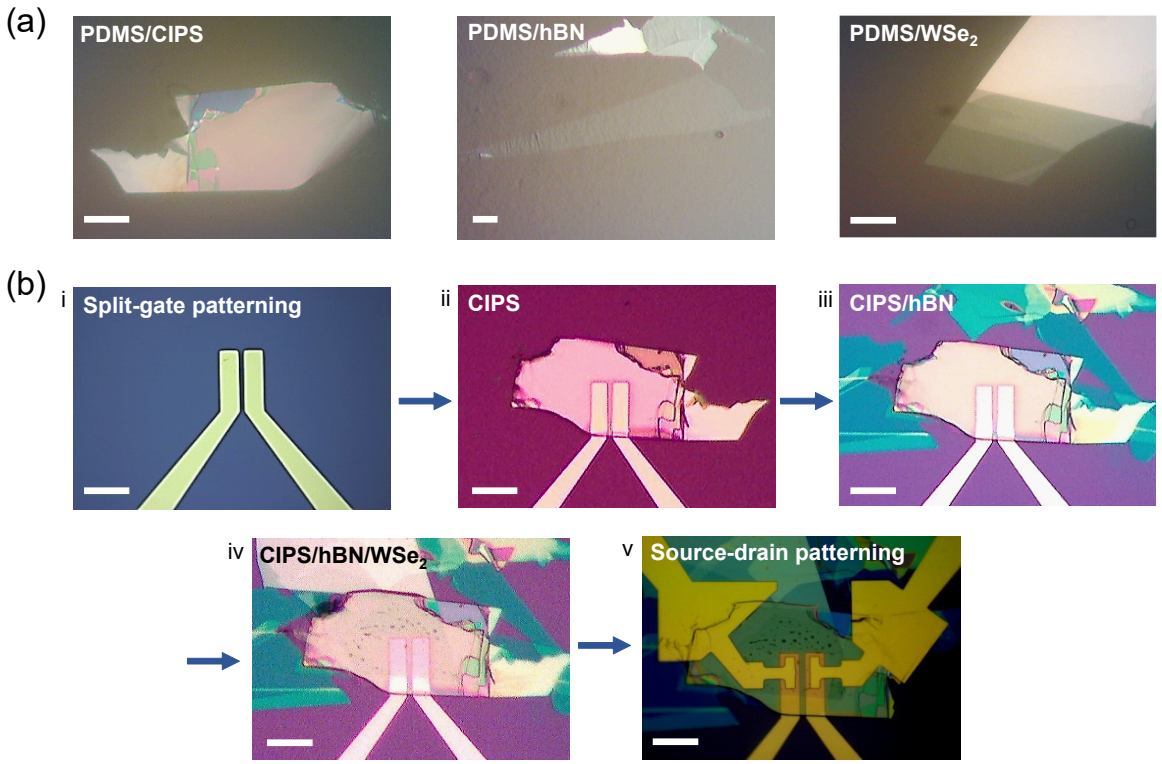


Figure 5.5: Optical microscope images (scale bar = 20 μm) of (a) exfoliated CIPS, hBN and WSe_2 flakes on independent PDMS substrates, (b) different fabrication steps of a typical Re-FeFET (from split-gate patterning, layer-by-layer stacking, to top electrodes pattering

Device fabrication was completed by performing manual bonding using silver paste and epoxy to establish electrical connections with gold wires. This step ensured reliable electrical connections between the device and external measurement equipment. Finally, the bonded device was mounted in a cryostat for further analysis.

5.2. Characterization Techniques

5.2.1. Atomic Force Microscopy (AFM)

The thickness profiles of various materials were measured using a Bruker Dimension Icon atomic force microscope (AFM). Measurements were conducted in tapping mode using a Bruker Si tip (TESPA-V2), ensuring high-resolution surface characterization.

5.2.2. Piezoresponse Force Microscopy (PFM)

PFM measurements were conducted using an atomic force microscope (AFM) (Nanoscope V Multimode, Bruker) equipped with external lock-in amplifiers (SR830, Stanford Research)

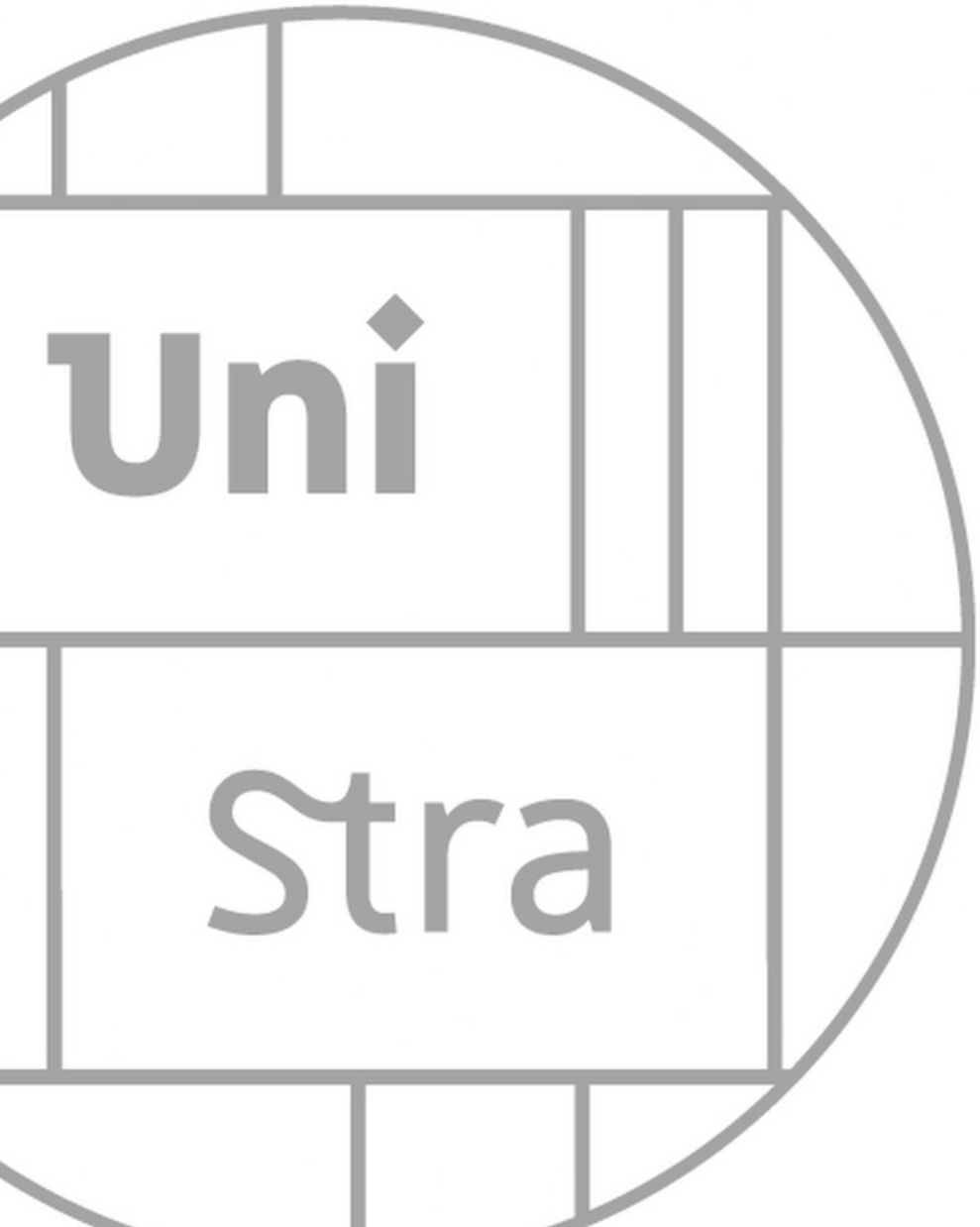
to simultaneously record vertical and lateral piezoresponse signals. In cases where the lateral response was below the noise level, only the out-of-plane component was considered. An AC voltage was applied between a conductive AFM tip and the bottom electrode to generate an electric field across the sample, enabling the detection of piezoelectric and ferroelectric properties. Cantilevers with stiffness values in the range of 7–40 N/m were used to optimize the imaging conditions. The measurement frequency was set to approximately 35 kHz to enhance signal detection while minimizing electrostatic artifacts.

5.2.3. Raman Spectroscopy

Micro-Raman spectroscopy measurements were conducted at room temperature using a commercial confocal Horiba Labram Raman spectrometer operating with a laser of wavelength $\lambda = 532$ nm. The laser beam was focused onto a small spot with a diameter of about 1 μm on the sample and an incident power of about 250 μW. All measurements were acquired at room temperature.

5.2.4. Cryogenic and Photo-Transport Measurements

Devices were measured in helium-flow cryostats, providing a controlled environment for electrical and optoelectrical measurements. High-precision K2634B source meters were used for electrical characterization and gate pulse control. For the ferroelectric logic circuit, a K2182A nanovoltmeter was used to extract the voltage output parameter while measuring the voltage drop across a resistance connected in series with the device. An in situ optical fiber was used for photoexcitation together with a COHERENT OBIS LS/LX 522 nm source in CW-power mode.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6 | Reconfigurable Multifunctional van der Waals Ferroelectric Devices and Logic Circuits

In this chapter, we introduce reconfigurable ferroelectric field-effect transistors (Re-FeFETs) [106], which harness the combined strengths of reconfigurable electronics [26][27] and ferroelectronics. By integrating the programmability of reconfigurable transistors with the nonvolatile memory capabilities of ferroelectric materials, these devices achieve a high degree of multifunctionality and adaptability.

This work advances the state-of-the-art by presenting Re-FeFETs based on van der Waals (vdW) heterostructures composed of $CuInP_2S_6$ (CIPS) [65, 107], hBN [108], and WSe_2 [109, 110]. These devices demonstrate an unprecedented combination of functionalities, including reconfigurable homojunctions, phototransistor modes, and polymorphic nonvolatile logic-in-memory operations. With these innovations, the Re-FeFETs significantly reduce transistor count, enhance design compactness, and provide high energy efficiency. Furthermore, the reconfigurability of these devices introduces new possibilities for in-memory computing and compact logic circuit design, marking a transformative step for beyond-CMOS [23] electronic systems.

The results presented in this chapter have been published in Ram et al. (2023) [106]

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6.1. Device Architecture

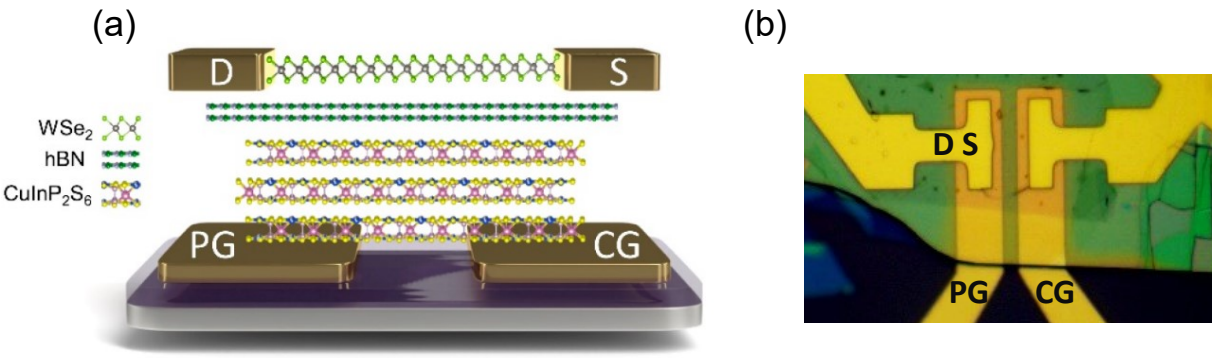


Figure 6.1: (a)Schematic of the device and (b) optical image.

The Re-FeFETs are designed with a split-gate architecture based on a van der Waals heterostructure. The primary components include a WSe_2 semiconducting channel, a $CuInP_2S_6$ (CIPS) ferroelectric layer, and a hexagonal boron nitride (hBN) dielectric spacer, depicted in Fig. 6.1(a). This configuration ensures precise modulation of the energy band profile, enabling reconfigurable functionalities.

The fabrication process begins with the patterning of bottom split-gate electrodes on a silicon/silicon dioxide (Si/SiO_2) substrate using electron beam lithography (EBL). A thin titanium layer (5 nm) followed by a gold layer (45 nm) is deposited to form the gates. Sequentially, mechanically exfoliated layers of WSe_2, hBN, and CIPS are transferred onto the patterned substrate using a PDMS-based dry transfer technique. The layer thicknesses are optimized as follows: WSe_2 (2-4 nm), hBN (8-10 nm), and CIPS (90-380 nm), see the device fabrication chapter (Ch. 5) for more details.

Top electrodes are patterned using EBL and metal deposition techniques, completing the device architecture. The channel length is set to 6 µm, the split-gate separation is 3 µm, and the channel width is 15 µm. Optical image of the fabricated device is presented in Fig. 6.1(b), confirms the precision of the stacking process and alignment of the electrodes.

This architecture enables the independent control of the program and control gates, offering tunability between unipolar (n-n, p-p) and ambipolar (n-p, p-n) configurations. The inclusion of the ferroelectric CIPS layer provides nonvolatile control [111, 112] over the channel properties, making the Re-FeFETs highly versatile for multifunctional applications [26].

6.2. Characterization

6.2.1. Atomic Force Microscopy (AFM)

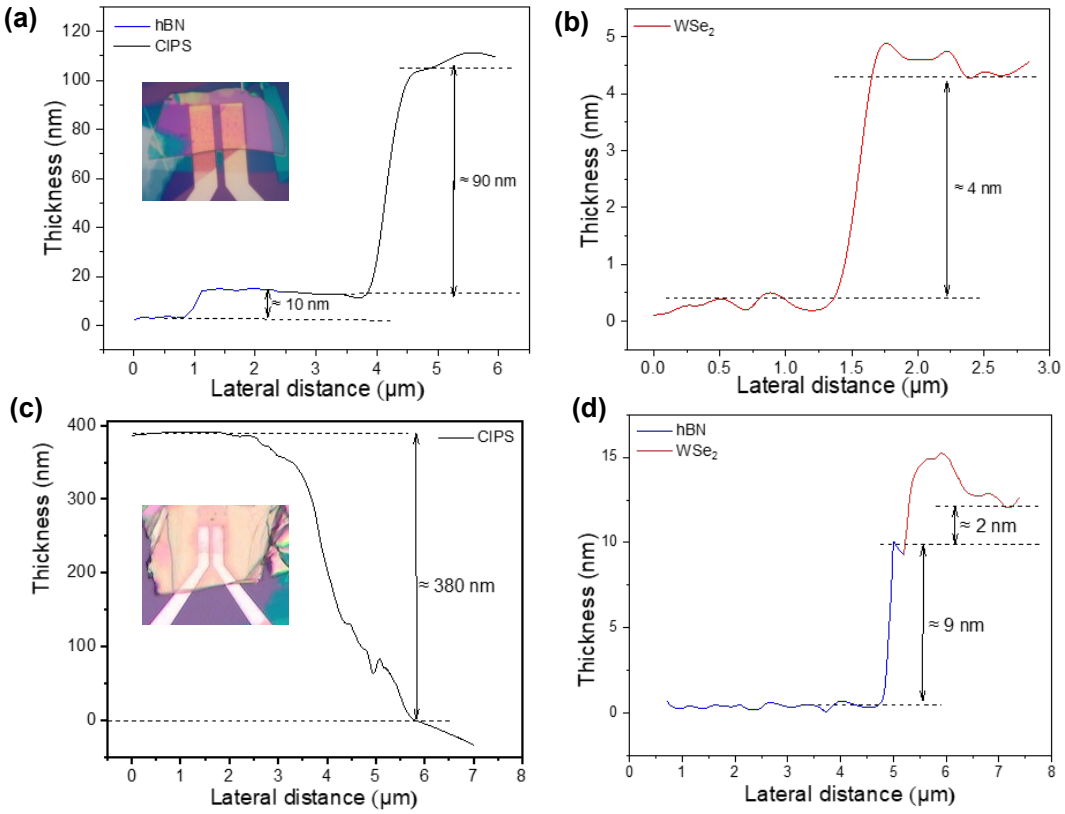


Figure 6.2: (a)-(d), Height profiles of hBN, CIPS and WSe_2 measured on Re-FeFET devices by Atomic Force Microscopy. Inset of a (resp. (c)) shows optical microscope images of sample characterized in (a) and (b) (resp. (c) and (d))

Atomic force microscopy (AFM) was employed to confirm the layer thickness and uniformity of the van der Waals heterostructures. The measured heights of WSe_2, hBN, and CIPS layers were consistent with the design specifications, showing values of 2–4 nm for WSe_2, 8–10 nm for hBN, and 90-380 nm for CIPS. The AFM profiles demonstrated smooth interfaces, indicating high-quality stacking and minimal surface roughness.

6.2.2. Raman Spectroscopy

[Raman analysis was performed in collaboration with PhD student Aymen Mahmoudi under the supervision of Abdelkarim Ouerghi at Université Paris-Saclay, CNRS, Centre de Nanosciences

et de Nanotechnologies.]

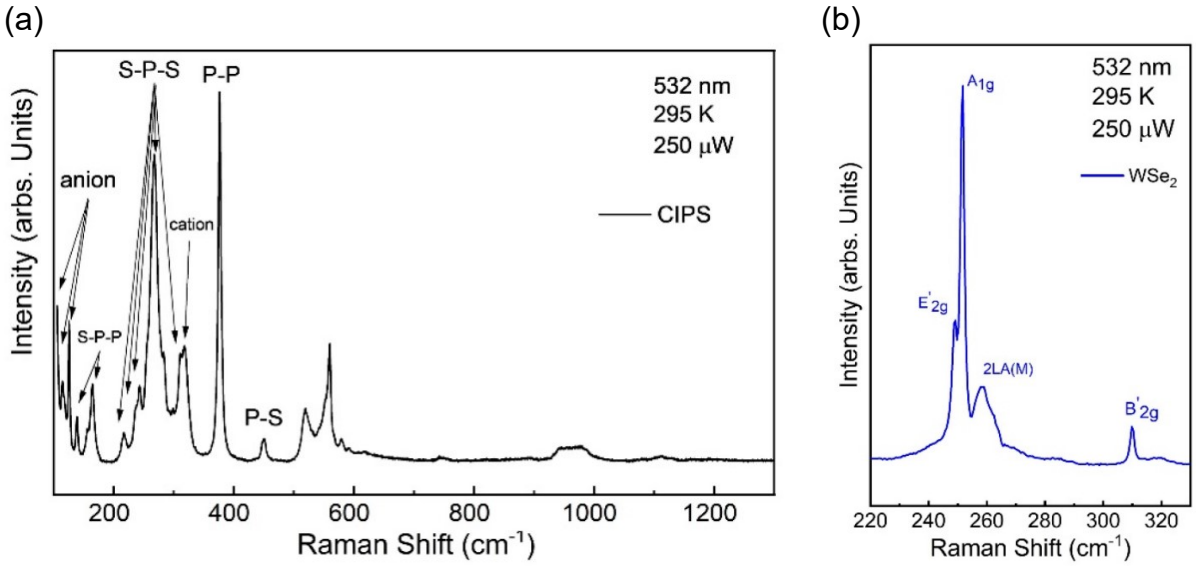


Figure 6.3: (a) Micro-Raman spectrum of $CuInP_2S_6$ taken from a Re-FeFET device. (b) Micro-Raman subtracted spectrum of the WSe_2 channel taken from the WSe_2/hBN/CIPS heterostructure region.

Fig. 6.3 presents the micro-Raman spectrum of the van der Waals heterostructure obtained from a representative Re-FeFET. The spectrum features the first-order in-plane (E'_{2g}) and out-of-plane (A_{1g}) Raman modes of the WSe_2 bilayer, appearing at approximately 249 cm^{-1} and 251 cm^{-1}, respectively. The observed splitting of 2 cm^{-1} between these peaks signifies a suppression of degeneracy, indicative of bilayer stacking. The intensity ratio of the A_{1g} to E'_{2g} peaks, measured to be around 3, further confirms the bilayer configuration.

Additionally, the spectrum reveals a pronounced peak at 308 cm^{-1}, labeled as B'_{2g}, which corresponds to regions with a thickness of two monolayers. This B'_{2g} peak serves as evidence of the bilayer nature of the WSe_2 layer, as supported by prior studies. The splitting between the in-plane and out-of-plane modes, along with the strong B'_{2g} signal, highlights a stacking arrangement characteristic of the 3R phase. This phase contributes significantly to the unique electronic and structural properties of the heterostructure.

The Raman data provide compelling evidence for the high quality and precise fabrication of the van der Waals heterostructure used in the Re-FeFETs, showcasing the successful integration and uniformity of the constituent materials.

6.3. Electrical Characterization

6.3.1. Doping Modulation in WSe_2 via Split-Gate Architecture

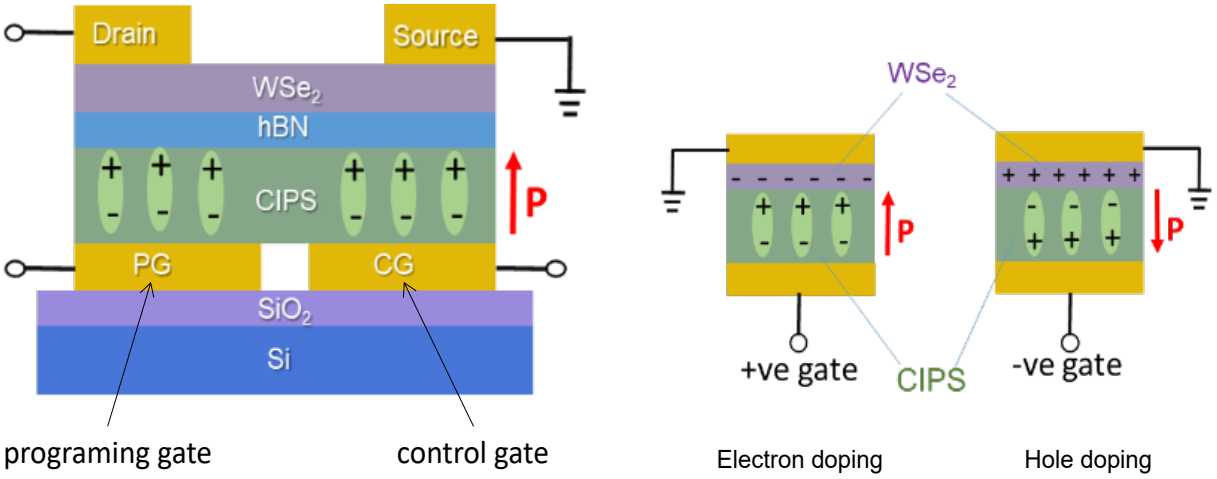


Figure 6.4: Illustration of split-gate doping modulation in the WSe_2 channel via ferroelectric polarization. Positive and negative programming gate voltages induce electron and hole doping, respectively, enabling reconfigurable operation.

We first study how the split-gate architecture [113] enables the emulation of different FeFET operating behaviors by tuning the doping state in the WSe_2 semiconducting channel. This device architecture features two gates: one designated as the program gate (PG) and the other as the control gate (CG).

When a positive voltage is applied at the programming gate, the ferroelectric CIPS layer polarizes upward, inducing electron doping in the WSe_2 channel. Conversely, applying a negative voltage at the programming gate polarizes the CIPS layer downward, resulting in hole doping. The control gate independently modulates the channel conductivity, allowing for dynamic tuning of the device characteristics.

This dual-gate operation provides unprecedented control over the carrier type and density in the semiconducting channel, as illustrated in Fig. 6.4. The schematic demonstrates the doping modulation mechanisms, depicting how ferroelectric polarization governs the electronic properties of the WSe_2 layer. This reconfigurability forms the foundation for the multifunctionality of Re-FeFETs in advanced logic and memory applications.

6.3.2. Transconductance Characteristics of the Re-FeFET

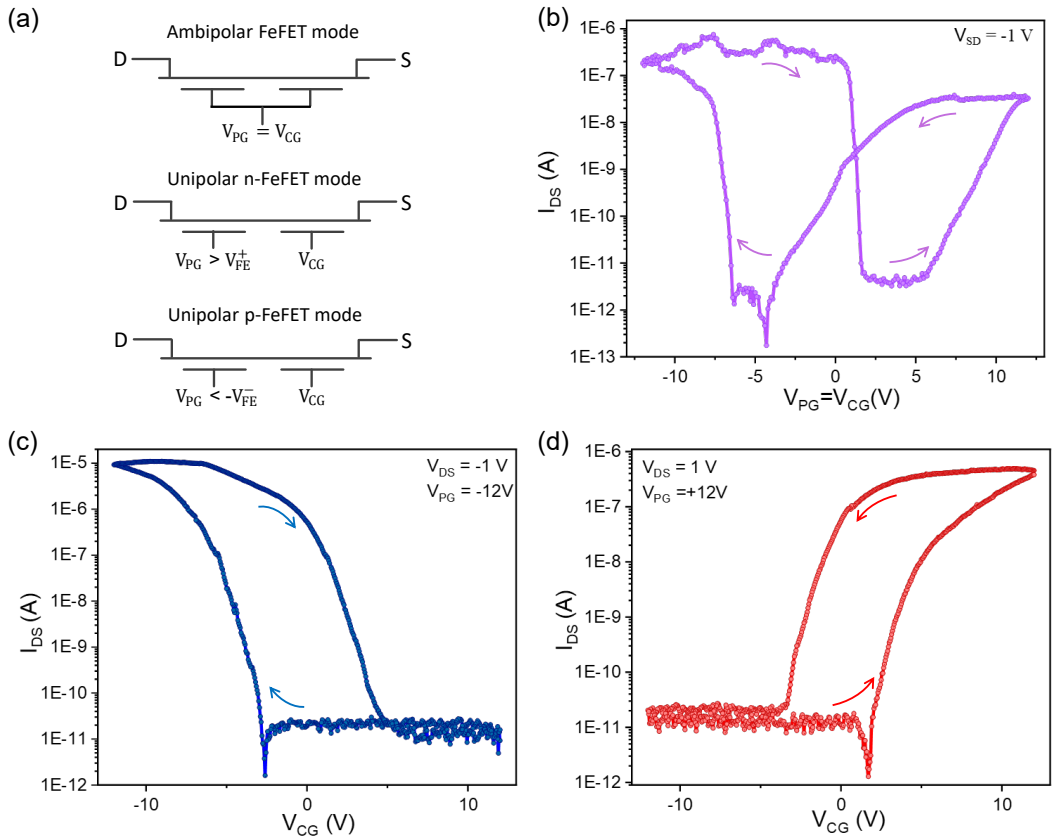


Figure 6.5: Ferroelectric Field Effect Transistor with reconfigurable polarities. (a) Schematic of the various operating modes of the Re-FeFET. In the ambipolar mode, both gates are biased at the same sweeping voltage. In the unipolar n-FeFET (resp. p-FeFET) mode, the program gate V_{PG} is set above (resp. below) the positive (resp. negative) ferroelectric coercive voltage V_{FE}, while the control gate voltage V_{CG} is swept. (b) Transconductance loop of the Re-FeFET operating in the ambipolar mode, demonstrating ambipolar hysteresis with anticlockwise hysteresis in the n-branch and clockwise hysteresis in the p-branch. (c, d) Transconductance loops of the Re-FeFET operating in the p-FeFET and n-FeFET modes, respectively. The ferroelectric polarization switching of the CIPS is responsible for the anticlockwise (resp. clockwise) hysteresis of the n-FeFET (resp. p-FeFET) transconductance.

Fig. 6.5(a) illustrates the schematic representation of the various operating modes of the Re-FeFET. In the ambipolar mode, both gates are subjected to the same sweeping voltage ($V_{\mathrm{PG}} = V_{\mathrm{CG}}$). For the unipolar modes, the program gate (V_{PG}) is set either above the positive ferroelectric coercive voltage (V_{FE}^{+}, e.g., $V_{\mathrm{PG}} = +12$ V) in the *n-FeFET mode* or below the

negative ferroelectric coercive voltage (V_{FE}^{-}, e.g., $V_{PG} = -12$ V) in the *p-FeFET mode*, while the control gate voltage (V_{CG}) is swept.

Fig. 6.5(b) presents the transconductance loop of the Re-FeFET when operating in the ambipolar mode, with both gates biased equally. This configuration closely resembles a single-gate FeFET, a well-documented operational behavior. The remanent polarization state of the $CuInP_2S_6$ (CIPS) layer can be inverted by applying gate voltages exceeding the respective ferroelectric coercive thresholds ($V_{FE}^{+} = +12$ V or $V_{FE}^{-} = -12$ V). Depending on the polarization states, up (P_{up}) or down (P_{down}), negative or positive mobile charges accumulate within the WSe_2 channel, enabling an ambipolar I_{DS}-V_{GS} transfer characteristic. This allows conduction in both the electron and hole accumulation regimes.

The Re-FeFET demonstrates a well-defined hysteresis loop, consisting of an anticlockwise branch for n-type conduction and a clockwise branch for p-type conduction. These hysteresis features directly correspond to ferroelectric polarization switching in the CIPS layer. Performance analysis shows an on/off current ratio exceeding 10^5 for the p-branch and 10^4 for the n-branch, with a ferroelectric memory window approaching 10 V. These features underscore efficient electrostatic coupling between the CIPS and WSe_2 layers, along with a high-quality van der Waals interface, free from detrimental Fermi level pinning or trap states [43, 114].

In Figs. 6.5(a) and (b) 6.5, the reconfigurable properties of the Re-FeFET are explored through its operation in asymmetric configurations. Here, the program gate is polarized to either the upward state ($PG^{\uparrow}$, $V_{PG} = +12$ V $> V_{FE}^{+}$) or the downward state ($PG^{\downarrow}$, $V_{PG} = -12$ V $< V_{FE}^{-}$). This selectively sets the doping state of the WSe_2 channel located over the program gate. Transconductance measurements were then performed by modulating only the control gate voltage (V_{CG}).

In the $PG^{\downarrow}$ state (Fig. 6.5(c)), the device operates as a *p-FeFET* and exhibits a clockwise transconductance hysteresis. The on/off current ratio reaches an impressive six orders of magnitude (10^6). In contrast, when programmed in the $PG^{\uparrow}$ state (Fig. 6.5(d)), the device mimics the behavior of an *n-FeFET*, also displaying a clockwise transconductance hysteresis but with a slightly lower on/off current ratio of four orders of magnitude (10^4). For both unipolar modes, the high-conductance and low-conductance states are achieved when the homojunction is configured as unipolar (p-p or n-n) or ambipolar (p-n or n-p), respectively.

DFT Calculations:

[DFT calculation was done by our collaborator, postdoc Aseem Rajan Kshirsagar, under the supervision of Sven Reichardt at the Department of Physics and Materials Science, University of Luxembourg.]

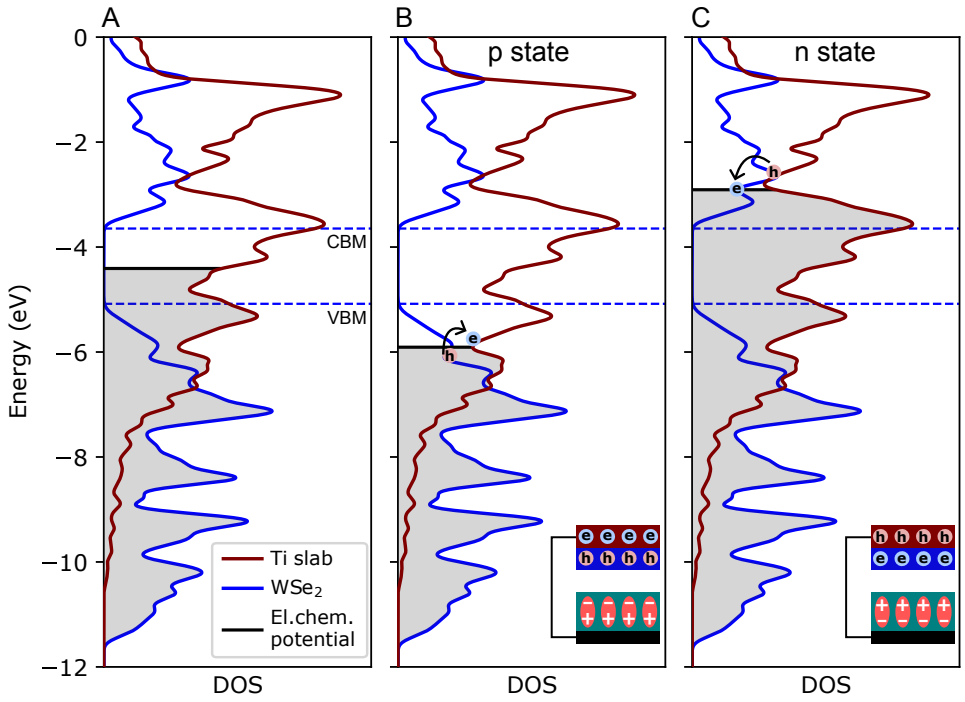


Figure 6.6: Atom-projected density of states (DOS) of the combined system of WSe_2 and Ti metal slab. (left) Electrochemical potential lying within the Ti metallic band within the band gap of WSe_2. (middle) Same as (left) but for the p-doped state, illustrating the electrostatic doping of the WSe_2 layer, with the hole charge carriers supplied by the Ti reservoir. (right) Same as (middle) but for the n-doped state. Inset: sketch of the vertical stacking ofthe Ti contact layer (red), the WSe_2 layer, and the polarized CIPS layer (teal), which is connected to the Ti through a metal contact.

Fig. 6.6 present density functional theory (DFT) simulations which provide deeper insight into the ambipolar behavior of the Re-FeFET. Fig. 6.6 (left graph) shows the density of states (DOS) of a combined WSe_2-Ti system obtained by projecting DFT orbitals onto atomic orbitals. In the absence of surface charge in CIPS, the Fermi level resides near the middle of the WSe_2 bandgap due to the Ti metallic band alignment (left graph). This alignment enables effective doping with both n-type and p-type carriers.

To qualitatively demonstrate the impact of ferroelectric polarization, the middle and right graphs of Fig. 6.6 depict sketches of the effective Fermi level under different surface charge conditions. Upward polarization shifts the conduction band minimum close to the Fermi level, favoring n-type conduction, while downward polarization lowers the valence band maximum, inducing p-type conduction.

The ability of Ti contacts to electrostatically align with WSe_2 bands ensures efficient car-

rier modulation, validating the strong coupling between the polarization of CIPS layer and electronic states of WSe_2. These theoretical insights are consistent with the experimental transconductance characteristics, confirming the reconfigurable multifunctionality of the Re-FeFET.

6.3.3. Reconfigurable Homojunction

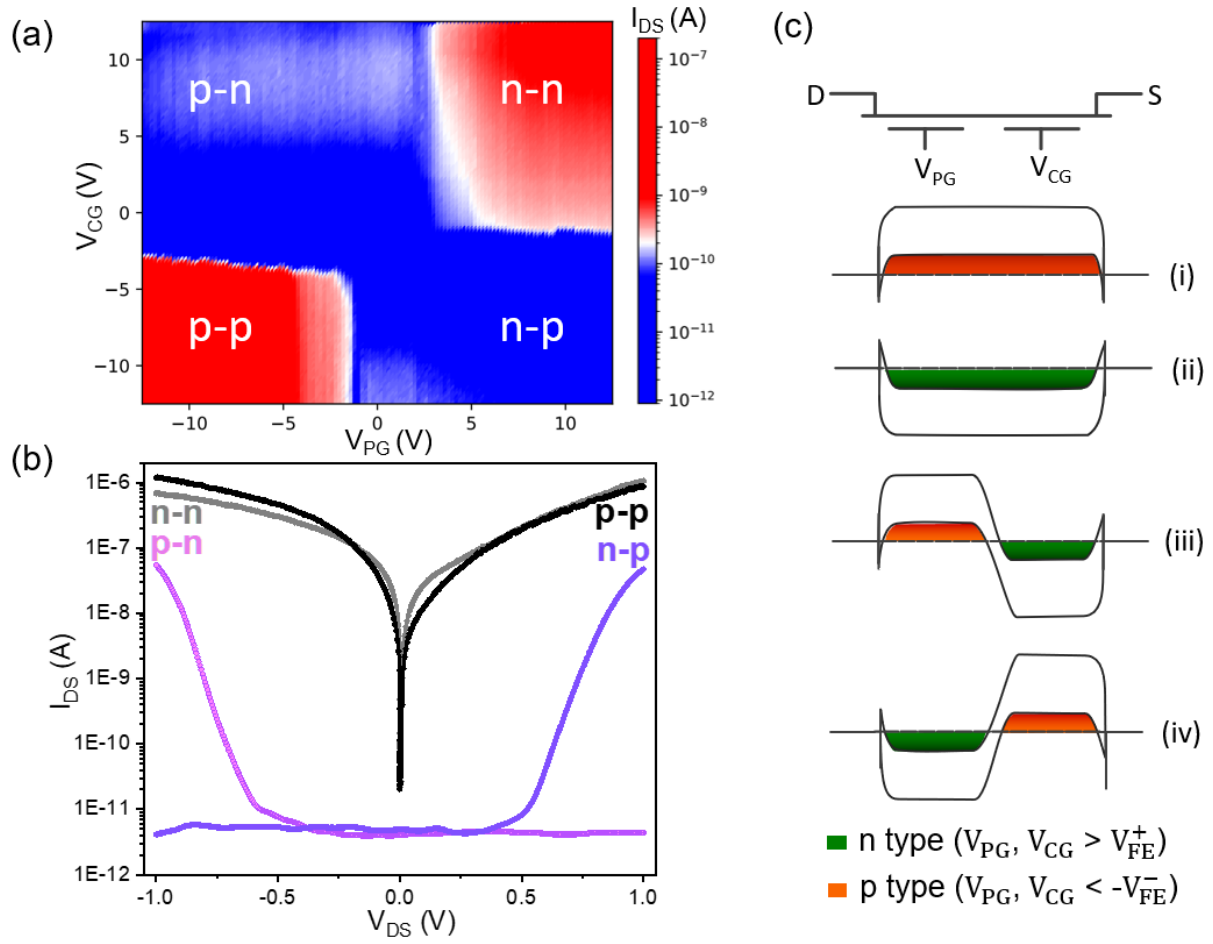


Figure 6.7: Band diagram and electrical modulation characteristics of the device. (a) Contour map of the drain-source current I_{DS} as a function of the voltages applied to the program gate (V_{PG}) and the control gate (V_{CG}). (b) I_{DS}-V_{DS} characteristics of the Re-FeFET programmed in the n-n (grey), p-p (black), p-n (pink), and n-p (purple) states. (c) Band diagrams of the Re-FeFET operated under various (V_{PG}, V_{CG}) settings, respectively in the (i) n-n, (ii) p-p, (iii) p-n, and (iv) n-p modes.

We now fully characterize the tunability of the homojunction while investigating systematically the transport properties of the WSe_2 homojunction as a function of the drain-source (V_{DS}) and gate-source (V_{PG}, V_{CG}) bias voltages. Fig. 6.7(a) shows the transconductance map

$I_{DS}(V_{PG}, V_{CG})$ measured at a fixed drain-source voltage of value 0.5 V under a systematic sweep on the gate bias voltage parameters (V_{PG}, V_{CG}). Four distinct homojunction states can be identified, corresponding to the four quadrants labeled on the transconductance map: the p-p, n-n, p-n, and n-p states. We further characterize the rectifying capability of the homojunction with these four states and report their output characteristics in Fig. 6.7(b). In the unipolar states (n-n or p-p), the $I_{DS}(V_{DS})$ traces show quasi-linear behavior, while in the ambipolar states (n-p or p-n) the $I_{DS}(V_{DS})$ traces demonstrate clear non-linear rectifying characteristics. The rectification ratio (defined as the ratio of the forward current to the reverse current obtained for opposite polarities of V_{DS}) exceeds 10^4 at $V_{DS} = 1$ V in the n-p and p-n states, while it stays close to 1 in the unipolar cases. Such a high rectification ratio indicates the excellent quality of the p-n junction formed in WSe_2 and its efficient coupling with CIPS.

6.4. Optoelectronic Properties

6.4.1. Photodiode and Photovoltaic Functionalities

We then investigate the potential of the Re-FeFET to convert light energy into electricity by the photovoltaic effect, taking advantage of the large built-in electric field of the p-n junction to dissociate photoexcited carriers. Fig. 6.8(a) illustrates the separation of photogenerated electron-hole pairs due to the built-in electric field formed within the WSe_2 bilayer. Upon illumination, the internal built-in electric field dissociates the photogenerated carriers and gives rise to a photocurrent at zero applied voltage (short-circuit photocurrent, I_{SC}) and a photovoltaic voltage with zero current flow (open-circuit voltage, V_{OC}).

Fig. 6.8(b) presents I–V curves under optical illumination ($\lambda = 522$ nm, $P = 0.001$–0.1 mW·mm^{-2}, see Methods for experimental details). When the Re-FeFET is set to a diode configuration p–n (resp. n–p), the I–V characteristics are shifted upward (resp. downward) compared to the dark characteristics. This demonstrates that the Re-FeFET operates as a photodiode.

Fig. 6.8(c) and Fig. 6.8(d) report the color maps of the I_{SC} and the V_{OC} respectively, as a function of the split-gate parameters (V_{PG}, V_{CG}) measured under illumination conditions ($\lambda = 522$ nm, $P = 0.1$ mW·mm^{-2}). The color maps precisely identify the existence of short-circuit photocurrents and open-circuit voltages with the diode states previously pinpointed in dark conditions (Fig. 6.7(a)). When the Re-FeFET is set to a unipolar state (n-n or p-p), no I_{SC} or V_{OC} is detected. Consistently, we observe in the p-n (n-p) configuration the appearance of a large negative (positive) V_{OC} (Fig. 6.8(b) and Fig. 6.8(c) and a positive (negative) I_{SC} (Fig. 6.8(b) and Fig. 6.8(d)). The fact that I_{SC} and V_{OC} change sign while

flipping the diode polarities is a clear indication that the photoresponse does not originate from the Schottky contacts [58, 115, 116]. For an optimally engineered junction profile, the maximum short-circuit photocurrent detected reaches 1.2 nA (resp. -1.3 nA) in p-n (resp. n-p) configuration, while the open-circuit voltage created reaches $+0.7$ V (resp. -0.7 V). The values obtained are among the highest reported so far for WSe_2. This demonstrates that the Re-FeFET can also be used for energy harvesting.

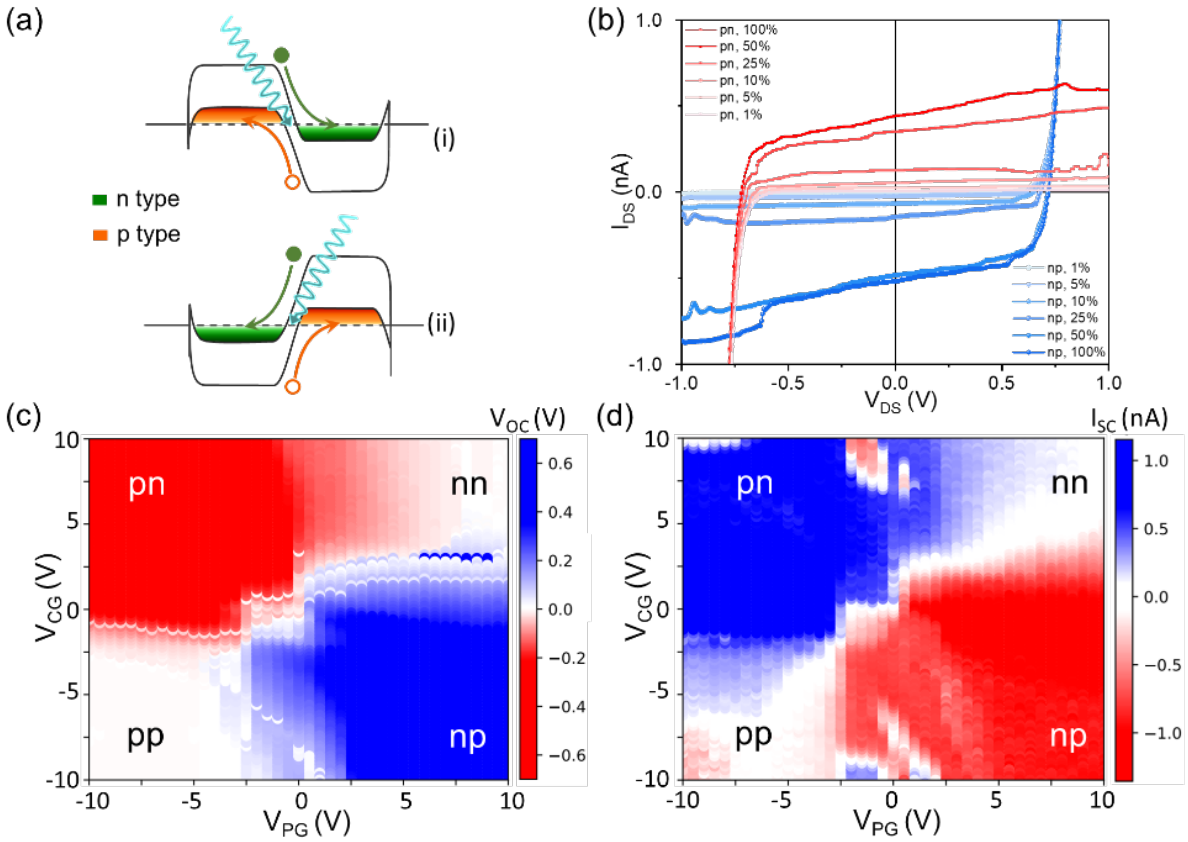


Figure 6.8: Optoelectronics and photovoltaic properties of the Re-FeFET. (a) Energy band diagram illustrating the photovoltaic effect in (i) p-n and (ii) n-p homojunction configuration of the WSe_2 channel. (b) Drain-source current vs voltage characteristics of the Re-FeFET programmed in p-n (red) and n-p (blue) configurations, under various light excitation conditions (Power = 0.1 mW·mm^{-2}, $\lambda = 522$ nm). (c) Color map of the open circuit voltage V_{OC} ($I_{DS} = 0$ A) as the program (V_{PG}) and the control (V_{CG}) gates voltages are tuned independently. (d) Color map of the short circuit photocurrent I_{SC} ($V_{DS} = 0$ V) as the two side-gates are swept independently.

6.4.2. Phototransistor functionality

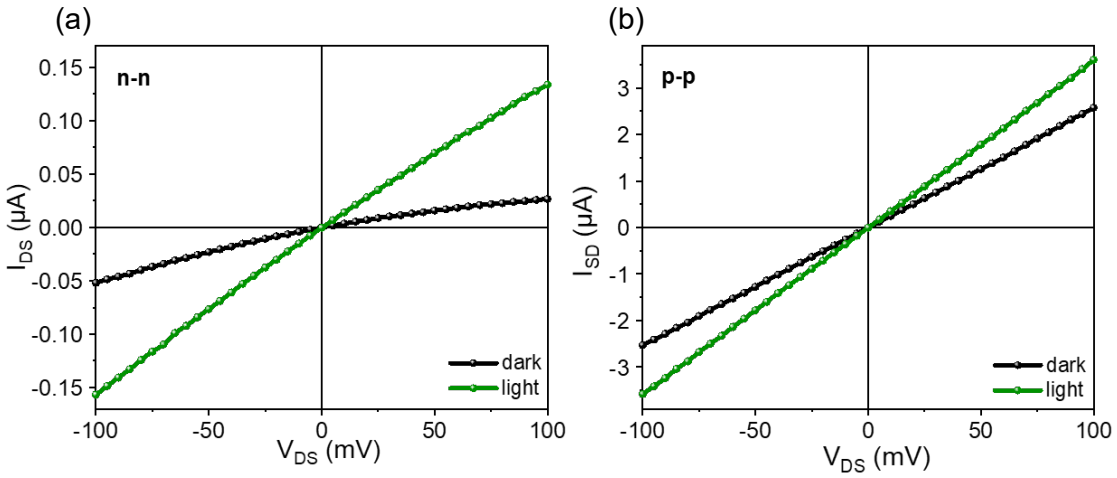


Figure 6.9: I_{DS} vs. V_{DS} characteristics in dark (black) and under illuminated (green) conditions for (a) n-n unipolar state and (b) p-p unipolar state.

In the unipolar states (n-n and p-p), the Re-FeFET exhibits distinct phototransistor behavior, as illustrated in Fig. 6.9. The output characteristics, showing the drain-source current (I_{DS}) as a function of the drain-source voltage (V_{DS}), are presented for both dark and illuminated conditions ($P = 0.1$ mW·mm^{-2}). A key observation is that the I_{DS}–V_{DS} curves for both unipolar states intersect precisely at the origin. This indicates the absence of short-circuit current (I_{SC}) and open-circuit voltage (V_{OC}) in these configurations.

This behavior highlights that, when the Re-FeFET is set to a unipolar homojunction state, it transitions to phototransistor functionality. In this state, the lack of I_{SC} and V_{OC} indicates that photogenerated carriers are not sufficiently separated by an internal electric field, distinguishing it from the photovoltaic response seen in ambipolar states. Instead, the Re-FeFET leverages light to modulate channel conductivity, reinforcing its operation as a phototransistor.

The significance of phototransistors lies in their ability to amplify light-induced signals, making them vital in optoelectronic applications such as imaging sensors, optical communication systems, and environmental monitoring. The Re-FeFET's phototransistor mode underscores its versatility and potential for integration into multifunctional optoelectronic circuits.

6.5. Polymorphic Ferroelectric and Electronic Logic Gates

The Re-FeFET architecture enables programming distinct homojunction states with variable conduction characteristics, providing highly reconfigurable Boolean logic operations [117]. This

flexibility allows the Re-FeFET to function either as an electronic logic gate or a ferroelectric logic gate, depending on the operating mode. This dual capability makes the device a strong candidate for diverse computational tasks, offering adaptability and compactness in circuit design.

6.5.1. Electronic Logic Gate Mode

Fig. 6.10(a) illustrates the Re-FeFET circuit configuration in electronic mode, comprising the device connected in series with a passive load. In this setup, the input variables are defined by the program gate voltage (V_{PG}) and the control gate voltage (V_{CG}), each independently representing logic "1" or "0" A voltage greater than the positive ferroelectric coercive voltage (V_{FE}^{+}) sets the polarization upward, corresponding to logic "1" while a voltage lower than the negative ferroelectric coercive voltage ($-V_{\mathrm{FE}}^{-}$) sets the polarization downward, representing logic "0" Fig. 6.10(b) presents a color map of the output voltage (V_{out}) measured across the passive load. This map visually represents the logic states of the circuit for different combinations of V_{PG} and V_{CG}. The color gradient clearly distinguishes the regions of high and low output voltage: when both inputs (V_{PG} and V_{CG}) are the same (either "1" or "0"), V_{out} is high, corresponding to logic "1" For mismatched inputs, V_{out} is low, corresponding to logic "0" This behavior emulates an XNOR logic gate, where the measured V_{out} values directly correlate with the truth table of the XNOR function, as shown in Fig. 6.10(c).

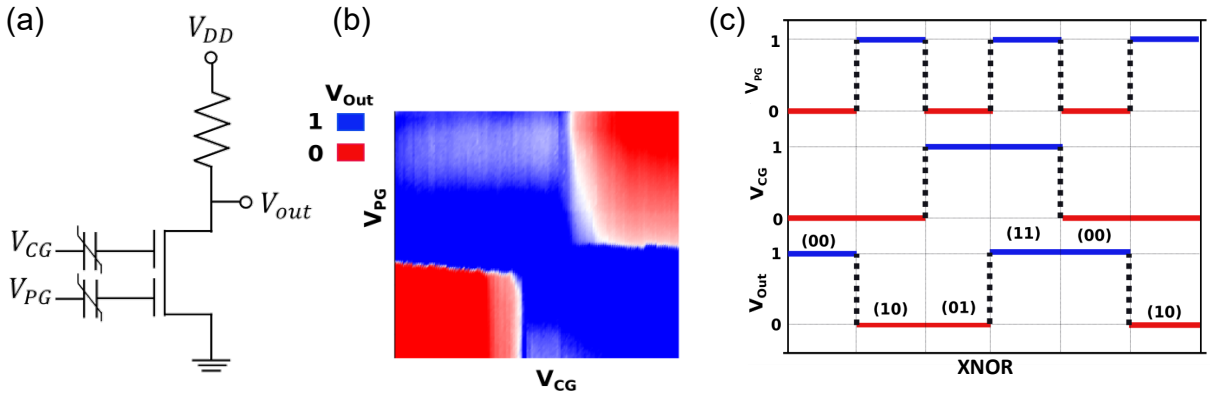


Figure 6.10: (a) Schematic of the Re-FeFET circuit operating in electronic logic mode, showing the device connected in series with a passive load. The input variables V_{PG} and V_{CG} independently control the polarization of the ferroelectric layer; (b) Color map of the measured output voltage (V_{out}) for different combinations of V_{PG} and V_{CG}, demonstrating the operation of the circuit as an XNOR logic gate; (c) Truth table of the XNOR function corresponding to the measured V_{out}, where the high and low output voltages align with the expected logical results.

6.5.2. Ferroelectric Logic Mode

In the case of the ferroelectric logic [118, 119], the logic state is determined by the input pair $(FE_{\text{Branch}}, V_{\text{CG}})$. The program gate ($V_{\text{PG}}$) is preset to a fixed polarized state, either $PG \uparrow$ or $PG \downarrow$, as illustrated in Figs. 6.11 and 6.12. The new input variable FE_{Branch} is unique to ferroelectric logic and is set to the "0" state (or "1" state) when the FeFET operates in the low (or high) threshold voltage branch of the transconductance hysteresis, transitioning at the negative ($-V_{\text{FE}}^{-}$) or positive ($+V_{\text{FE}}^{+}$) coercive field, respectively.

This mode enables the Re-FeFET logic to switch between a ferroelectric NAND (FE-NAND) and a ferroelectric AND (FE-AND) function, depending on the preprogrammed FeFET state (n-type or p-type). This polymorphic logic capability is particularly advantageous for hardware security, custom operations, and advanced circuit designs. Furthermore, the logic gate inputs can be provided via voltage pulses, with the I_{DS} current measured under open-circuit gate conditions. The ferroelectric logic states correspond to remanent states, eliminating the need for a constant supply voltage and enhancing energy efficiency.

Ferroelectric NAND (FE-NAND) Logic Gate

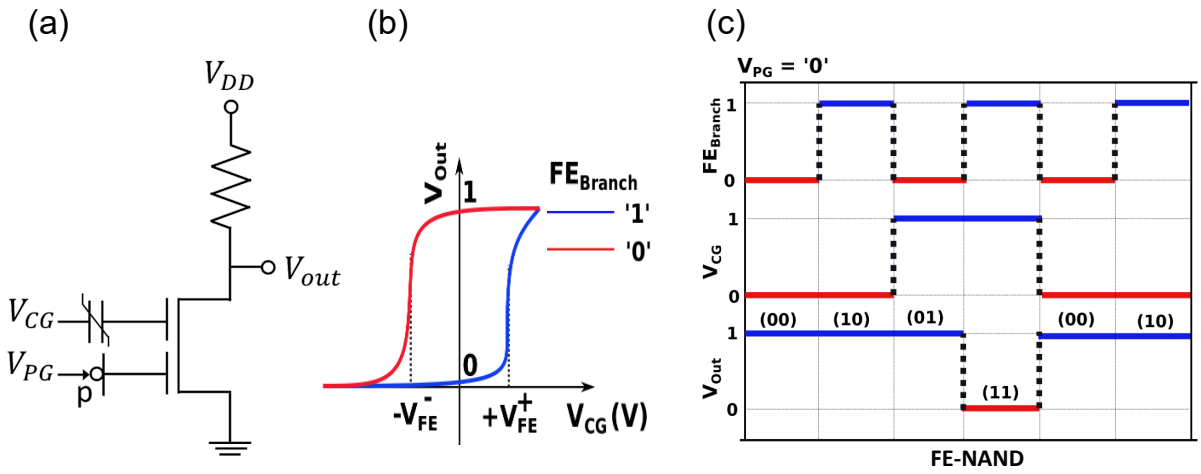


Figure 6.11: Ferroelectric NAND (FE-NAND) logic gate. (a) Circuit schematic showing the Re-FeFET conFig.d for NAND operation with a preset program gate state of '0'. (b) Ferroelectric hysteresis loop showing the threshold voltage branches corresponding to logic '0' and '1'. (c) Truth table demonstrating the FE-NAND logic behavior.

Fig. 6.11(a) shows the setup of a ferroelectric NAND (FE-NAND) logic circuit, where the Re-FeFET has its program gate (V_{PG}) preset to a downward polarization state, representing logic "0" The circuit receives inputs from the control gate voltage (V_{CG}) and a ferroelectric

branch (FE_{Branch}). The output voltage (V_{out}) is governed by the interaction of these two inputs.

Fig. 6.11(b) displays the ferroelectric hysteresis loop, which characterizes the switching behavior of the material. The hysteresis transitions between the low-threshold ($-V_{\text{FE}}^{-}$) and high-threshold ($+V_{\text{FE}}^{+}$) voltage branches, representing logic states '0' and '1' respectively. Fig. 6.11(c) provides the truth table, confirming the FE-NAND functionality: V_{out} is '1' for all input combinations except when both inputs ($FE_{\text{Branch}}, V_{\text{CG}}$) are '1' where the output is '0'

Ferroelectric AND (FE-AND) Logic Gate

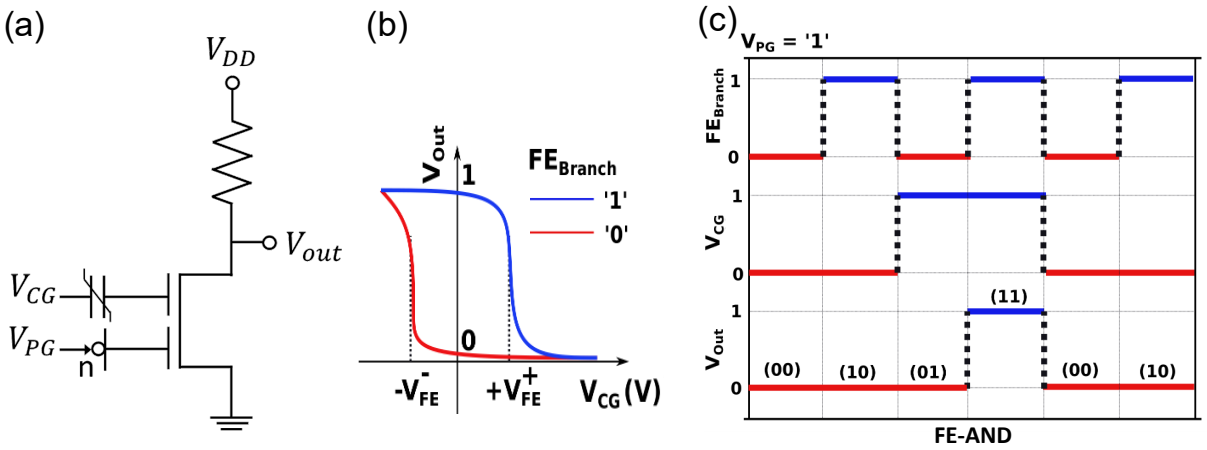


Figure 6.12: Ferroelectric AND (FE-AND) logic gate. (a) Circuit schematic showing the Re-FeFET conFig.d for AND operation with a preset program gate state of '1'. (b) Ferroelectric hysteresis loop showing the threshold voltage branches corresponding to logic '0' and '1'. (c) Truth table demonstrating the FE-AND logic behavior.

Fig. 6.12(a) illustrates the configuration of a ferroelectric AND (FE-AND) logic circuit, which uses the same Re-FeFET architecture. In this case, the program gate (V_{PG}) is preset to an upward polarization state, representing logic '1' The circuit inputs are the ferroelectric branch (FE_{Branch}) and the control gate voltage (V_{CG}).

In Fig. 6.12(b), the ferroelectric hysteresis loop is shown again, similar to the loop in Fig. 6.11(b). However, the preprogrammed polarization state ensures the implementation of AND logic instead of NAND. The transition between the low-threshold ($-V_{\text{FE}}^{-}$) and high-threshold ($+V_{\text{FE}}^{+}$) voltage branches corresponds to the logic states. Fig. 6.12(c) presents the truth table for the FE-AND circuit, verifying its logic behavior: V_{out} is '0' for all input combinations except when both inputs ($FE_{\text{Branch}}, V_{\text{CG}}$) are '1' where the output is '1'.

It is important to underline that the logic gate inputs can be provided by voltage pulses. In this

case, the I_{DS} current is measured after applying the various gate pulses, in open-circuit gate conditions, and the ferroelectric logic states correspond to remanent states. The retention properties of the four homojunction states are reported in Fig. 6.13(a) and Fig. 6.13(b). The Program and Control Gates have been programmed independently either in the up or down state, and subsequently grounded. The output voltage is presented as a function of time, and demonstrates successful retention after more than 10^4 seconds for each state, comparable to the best values reported so far on van der Waals ferroelectric heterostructures [70]. Such remanence is a major added value when compared with traditional CMOS-based circuits that rely on a constant supply of external voltages to maintain the desired doping levels. This represents a paradigm shift with respect to conventional von Neumann architectures, as the information processing and storing are combined in a single device. This demonstrates the promise of van der Waals ferroelectric circuits for Logic-In-Memory hardware [118].

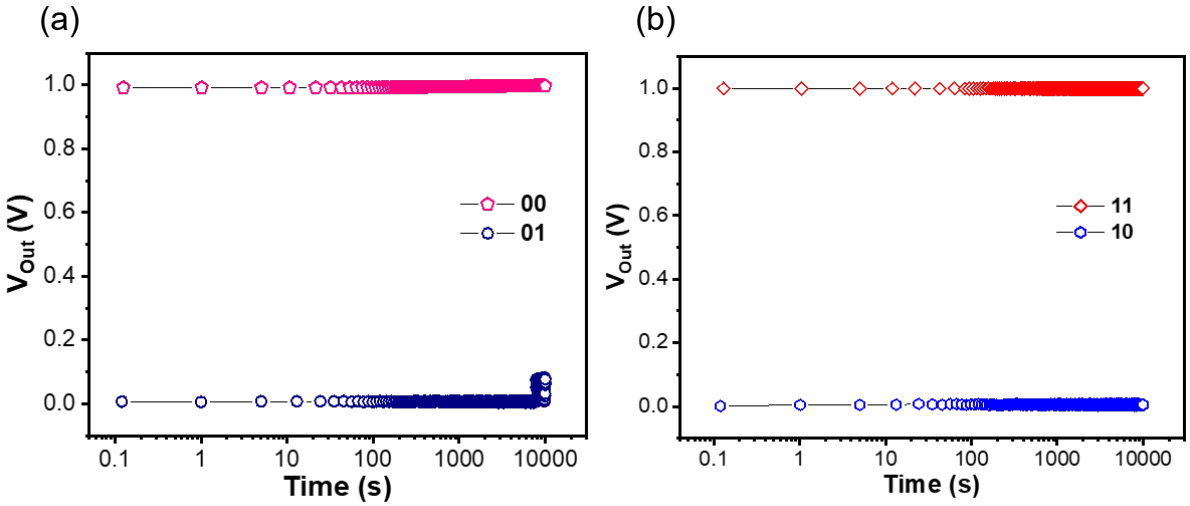


Figure 6.13: Retention properties of the four ferroelectric logic states. The output voltage (normalized with respect to V_{DD} set at 0.5 Volt) was measured after the Program and Control Gates had been programmed independently either in the up or down state, and subsequently grounded.

6.6. Circuit Design Exploration with Re-FeFETs

[Circuit design simulation and analysis presented in this section were carried out in collaboration with Cédric Marchand and Ian O'Connor at École Centrale de Lyon.]

In this section, we assess the potential of ferroelectric reconfigurable logic circuits based on Re-FeFETs through a circuit design exploration and modeling study. To set a framework

and terminology for the analysis, the single device is abstracted into a set of parameters $\{\{t, PG\}, \{X, CG\}\}$, where:

1. t represents the non-volatile conFig.d type of the transistor, where $t = 0$ indicates p-type operation, and $t = 1$ indicates n-type operation.
2. PG represents the volatile voltage applied to the program gate (also referred to as the polarity gate) after type configuration, causing a shift in the threshold voltage.
3. X represents the non-volatile polarization of the second part of the ferroelectric layer within the Re-FeFET. Here, $X = 0$ (resp. 1) corresponds to a negative (resp. positive) polarization.
4. CG represents the volatile voltage applied to the control gate after polarization configuration.

This parameter set for the Re-FeFET allows us to establish conditions that determine when the device is in the On state or the Off state. These conditions are summarized in the conduction table, as presented in Fig. 6.14a.

With this formalization of the Re-FeFET functionality, it becomes possible to explore the diverse logical functionalities achievable with simple circuit structures. Let us consider a specific case where the circuit consists of two series-connected Re-FeFETs (shown in Fig. 6.14c). By leveraging the conduction table, non-volatile logic operations can be implemented using this circuit. The process involves searching for solutions within the table that satisfy the constraints imposed by the truth table of the desired logical operation. Each solution corresponds to a unique parameter set for each Re-FeFET in the circuit (Re-FeFET$_1 = \{\{t_1, PG_1\}, \{X_1, CG_1\}\}$ and Re-FeFET$_2 = \{\{t_2, PG_2\}, \{X_2, CG_2\}\}$).

To create any logical or computing function, six elementary logic gates are needed: NAND, NOR, AND, OR, NOT, and XOR. The conduction table (Fig. 6.14a) provides direct implementations for NAND and NOR functions. However, the XOR function requires a more complex implementation. From the XOR truth table, it is possible to find solutions within the conduction table by setting $n_1 = V_{\text{dd}}$ and $n_2 = gnd$, given by:

$$\text{Re-FeFET}_1 \in \{\{\{\overline{B}, 0\}, \{1, A\}\}, \{\{\overline{B}, A\}, \{0, 1\}\}, \{\{\overline{B}, A\}, \{1, 0\}\}\}$$

$$\text{Re-FeFET}_2 \in \{\{\{B, 0\}, \{1, A\}\}, \{\{B, A\}, \{0, 1\}\}, \{\{B, A\}, \{1, 0\}\}\}.$$

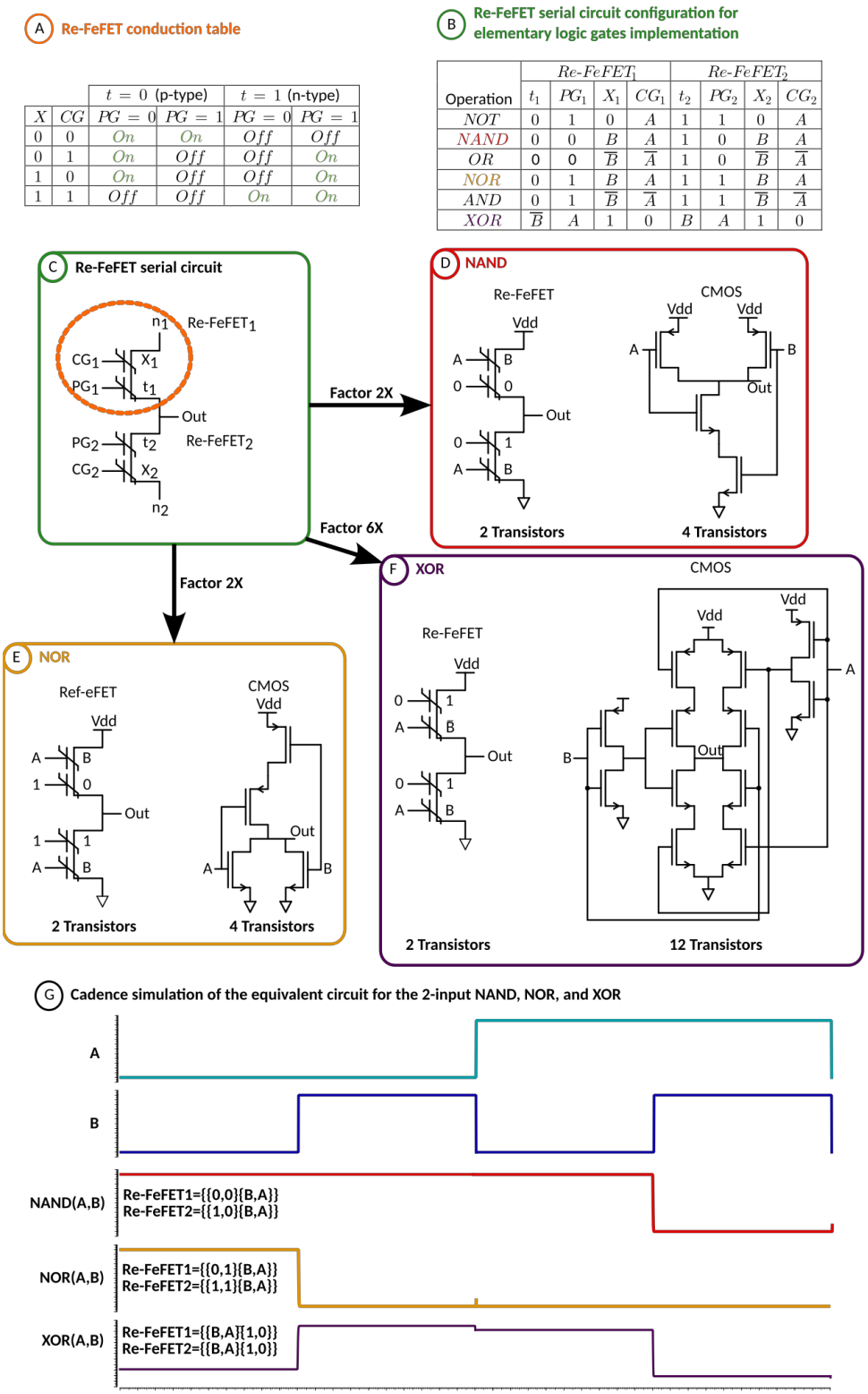
It is worth noting that these solutions only utilize A as the volatile operand. This implies that there is no need for an additional inverter to physically implement this circuit, unlike conventional implementations of 2-input XOR gates. Additionally, the non-volatile operand B

is linked to the type of the Re-FeFET. In some cases, when an n-type device is used to pass V_{dd} to the output, there can be a logic '1' degradation. To mitigate logic degradation, it is common practice to regenerate the output voltage level (usually via an inverter and/or a level restorer), either for each logic gate or for a set of cascaded logic gates.

Finally, it is demonstrated that all six elementary logic gates can be accessed using the single series-connected Re-FeFET (Fig. 6.14c) circuit configuration while keeping $n_1 = V_{dd}$ and $n_2 = gnd$. An example configuration for each logic gate implementation is depicted in Fig. 6.14b. As shown in Fig. 6.14, Re-FeFETs offer the advantage of very compact logic gates compared to CMOS circuits. In the case of the inverter, the same transistor count is required for both Re-FeFET and CMOS implementations. However, Figs. 6.14d and 6.14e show that for NAND and NOR gates, the Re-FeFET-based circuit requires only two devices, while the equivalent CMOS circuits necessitate four transistors. In the case of the XOR operation presented in Fig. 6.14f, the CMOS implementation typically requires 12 transistors, considering the two additional inverters required to convert A and B to their complemented forms ($\overline{A}$ and $\overline{B}$). On the other hand, the Re-FeFET-based XOR can be implemented with just two devices. This results in a significant reduction in transistor count by a factor of 6.

Consequently, Re-FeFET devices offer the potential for compact circuits, which can be beneficial in a wide range of applications such as reconfigurable circuits with systematic and regular structures (such as FPGAs) or obfuscated circuits aimed at preventing reverse engineering, among others. The use of an identical basic circuit element for all logic gates provides additional advantages. Fabrication constraints are alleviated, leading to more compact and reliable chip designs. Furthermore, hardware security can be enhanced as the time-dependent power consumption of each logic gate remains identical, making it more challenging to derive information from power measurements. This inherent resilience to side-channel attacks adds to the appeal of Re-FeFET-based circuits in terms of hardware security.

To facilitate further design considerations and enable device simulation, an equivalent circuit is created in the Cadence software. Using this equivalent circuit, behavioral simulations of the three main logical operations (NAND, NOR, and XOR) are conducted. The simulation results are presented in Fig. 6.14g.



X	CG	$t = 0$ (p-type) $PG = 0$	$t = 0$ (p-type) $PG = 1$	$t = 1$ (n-type) $PG = 0$	$t = 1$ (n-type) $PG = 1$
0	0	*On*	*On*	*Off*	*Off*
0	1	*On*	*Off*	*Off*	*On*
1	0	*On*	*Off*	*Off*	*On*
1	1	*Off*	*Off*	*On*	*On*

Operation	$Re\text{-}FeFET_1$ t_1	PG_1	X_1	CG_1	$Re\text{-}FeFET_2$ t_2	PG_2	X_2	CG_2
NOT	0	1	0	A	1	1	0	A
NAND	0	0	B	A	1	0	B	A
OR	0	0	$\overline{B}$	$\overline{A}$	1	0	$\overline{B}$	$\overline{A}$
NOR	0	1	B	A	1	1	B	A
AND	0	1	$\overline{B}$	$\overline{A}$	1	1	$\overline{B}$	$\overline{A}$
XOR	$\overline{B}$	A	1	0	B	A	1	0

Figure 6.14: Implementation of NAND, NOR, and XOR functions using Re-FeFETs as compared to conventional CMOS circuits.

Fig. 6.14 detailed caption: Implementation of NAND, NOR, and XOR functions using Re-FeFETs as compared to conventional CMOS circuits. (a) Re-FeFET conduction table specifying when the Re-FeFET is conducting ("On") or not ("Off") depending on the set of parameters. (b) Table of series-connected Re-FeFET circuit configurations for six different logic functions (NOT, NAND, OR, NOR, AND, and XOR). (c) Ferroelectric circuit consisting of two series-connected Re-FeFETs and detailed configurations for the logic functions NAND (d), NOR (e), and XOR (f). For each logic function, the ferroelectric logic demonstrates superiority in terms of circuit compactness with a factor between 2 and 6. (f) Behavioral simulations (created with the Cadence software) of the three main logic operations (NAND, NOR, XOR) performed by the in-series Re-FeFET circuit

6.7. Conclusion

- We explored reconfigurable ferroelectric field-effect transistors (Re-FeFETs) based on a WSe_2 semiconducting channel controlled by split gates and a $CuInP_2S_6$ ferroelectric layer. The split-gate architecture enables full electrostatic control, allowing precise tuning of the WSe_2 energy band from unipolar (n-n, p-p) to ambipolar (n-p, p-n) homojunctions. This allows seamless switching between p-type, n-type, and ambipolar FeFET modes, making the device highly adaptable.
- The device achieves a high on/off ratio of 10^6 (p-branch) and 10^4 (n-branch), a wide memory window up to 10 V, and clear ferroelectric hysteresis switching, confirming strong electrostatic coupling. When configured as a diode (p-n or n-p junction), the Re-FeFET exhibits:
    - Strong rectification greater than 10^4 ratio.
    - Photovoltaic capabilities by efficiently converting light into electrical power.
    - High photocurrent with a large open-circuit voltage due to the built-in electric field at the p-n junction, ensuring effective electron-hole separation.
- We demonstrated a reconfigurable logic unit capable of operating in multiple modes:
    - In ferroelectric logic mode, the device can switch between a Fe-NAND gate and a Fe-AND gate, depending on the stored state in the program gate, and exhibits long data retention exceeding 10^4 seconds.
    - In electronic mode, independent control of the program and control gates enables XNOR logic operations.
- Circuit simulations show that two series-connected Re-FeFETs can efficiently implement

NOT, NAND, OR, NOR, AND, and XOR logic functions. The Re-FeFET-based circuit significantly reduces transistor count by up to 80%, making it far more compact compared to traditional CMOS technology.

- Overall, this work highlights the strong potential of van der Waals materials for developing high-performance, beyond-Moore electronics. The Re-FeFET's ability to combine logic, memory, optoelectronic, and photovoltaic functionalities in a single reconfigurable unit presents exciting opportunities for future more-than-Moore and beyond-Moore strategies in advanced electronics.

7 | Scaling Effect in $CuInP_2S_6/WSe_2$ Based van der Waals Ferroelectric Field-Effect Transistors (FeFETs)

In the previous chapter (Ch. 6), we discussed $CuInP_2S_6/WSe_2$ van der Waals heterostructure-based Reconfigurable Ferroelectric Field-Effect Transistors (Re-FeFETs), highlighting their tunable electronic properties and versatile functionality. Building on these findings, we fabricated short-channel FeFETs with a similar device configuration, featuring a single top-gate architecture and systematically varied channel lengths to examine scaling effects.

Our design includes channel lengths reduced by up to a factor of 100 compared to previous configurations [106]. Typically, reducing the channel length in transistors can cause issues such as drain-induced barrier lowering (DIBL) [120] and loss of gate control, leading to performance degradation. However, the negative capacitance [36, 86] property of $CuInP_2S_6$ helps counter these problems, improving device performance. A comparative analysis of long- and short-channel devices reveals a transition in transistor behavior from FeFET-like to MOSFET-like operation, depending on the source-drain bias.

Furthermore, we demonstrate reconfigurability of the device using a ferroelectric floating-gate[121] in combination with a back gate. Leveraging the ambipolar nature of the WSe_2 channel, the device can be dynamically switched between p-FET, n-FET, and ambipolar FET modes.

Our findings offer key insights into the design and operation of short-channel 2D FeFETs, underscoring their potential in beyond-CMOS device architectures [24].

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7.1. Device Architecture and Fabrication Details

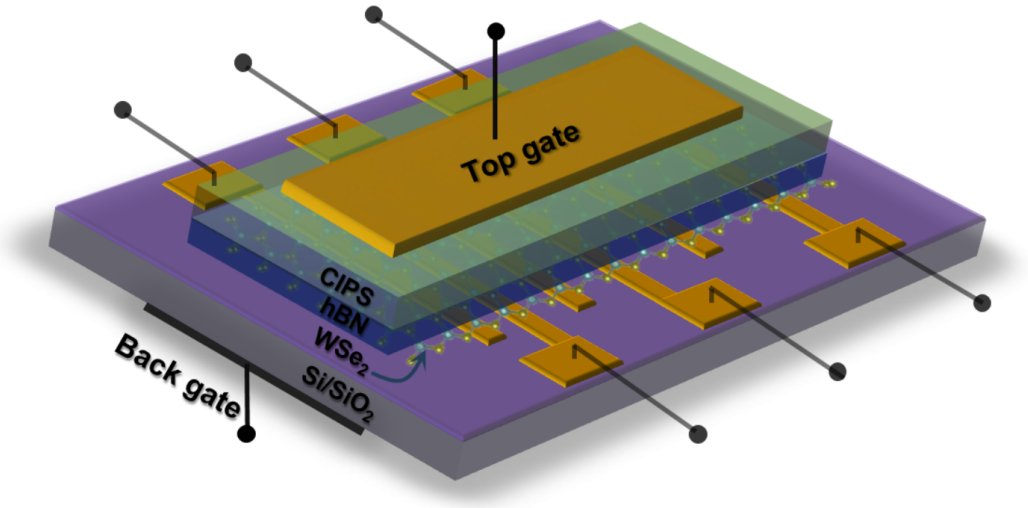


Figure 7.1: Schematic of FeFET with multiple channel lengths.

I successfully fabricated a series of FeFETs with a single top gate while systematically varying the channel length. First, I patterned source-drain electrodes with varying channel lengths using electron beam lithography (EBL). Then, I sequentially transferred exfoliated WSe_2, hBN, and $CuInP_2S_6$ using a dry transfer method. Finally, a top gate was patterned to complete the device structure. Schematic of the device is presented in Fig. 7.1.

To ensure high precision for this challenging fabrication, I implemented multiple optimization steps. For more details, see the fabrication chapter (Ch. 5). The bottom source-drain electrodes were patterned via a 3 nm etching step, followed by the deposition of Ti (3 nm) / Au (20 nm) / Ti (10 nm) onto the Si/SiO_2 substrate. This approach minimized the electrode height, allowing for a smoother transfer of 2D material layers while reducing the likelihood of strain. The 10 nm top Ti layer was specifically incorporated to enhance the ambipolar behavior of WSe_2 [60, 122], as demonstrated by our DFT simulations (discussed in Ch. 6).

Fig. 7.2 illustrates the FeFET fabrication process through SEM and optical images. Fig. 7.2(a) shows an SEM image of the patterned bottom source-drain electrodes, highlighting precisely defined channel lengths of 50 nm, 100 nm, 250 nm, 500 nm, and 1 μm. Fig. 7.2(b) presents optical images of the device at different stages: the left image shows the WSe_2/hBN/CIPS stack transferred onto the electrodes, and the right image depicts the final device after top gate patterning, with a scale bar of 4 μm.

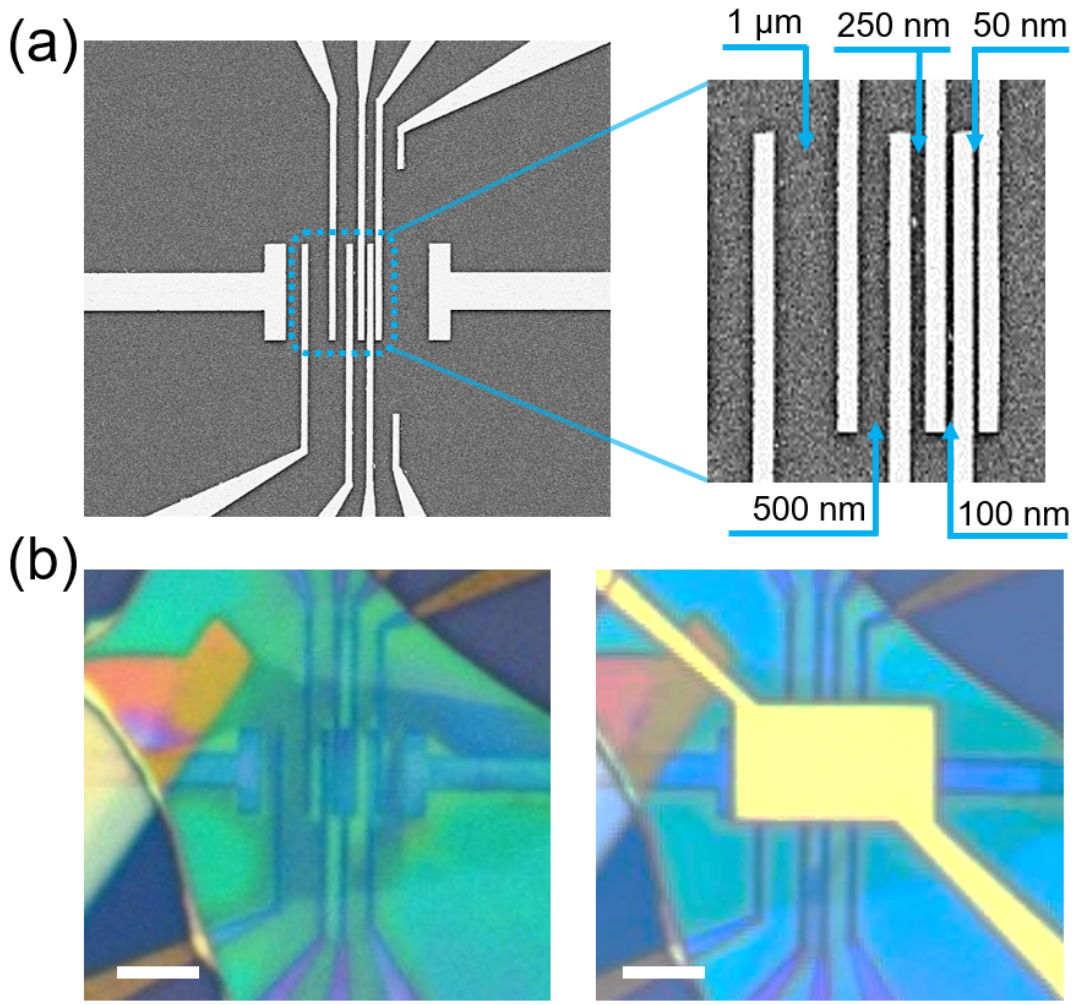


Figure 7.2: (a) SEM and (b) Optical images of the fabricated device.

7.2. Transport Properties

7.2.1. Transfer characteristics

Fig. 7.4(a) presents the transfer characteristics for both short-channel (50 nm) and long-channel (1 µm) devices. The data reveal a distinct ambipolar behavior, where both n-type and p-type conduction are observed as V_{GS} is swept between -6 V and +6 V in both forward and reverse directions, with $V_{DS} = 1$ V. This ambipolar nature arises from the intrinsic properties of WSe_2, enabling both electron and hole [123, 124].

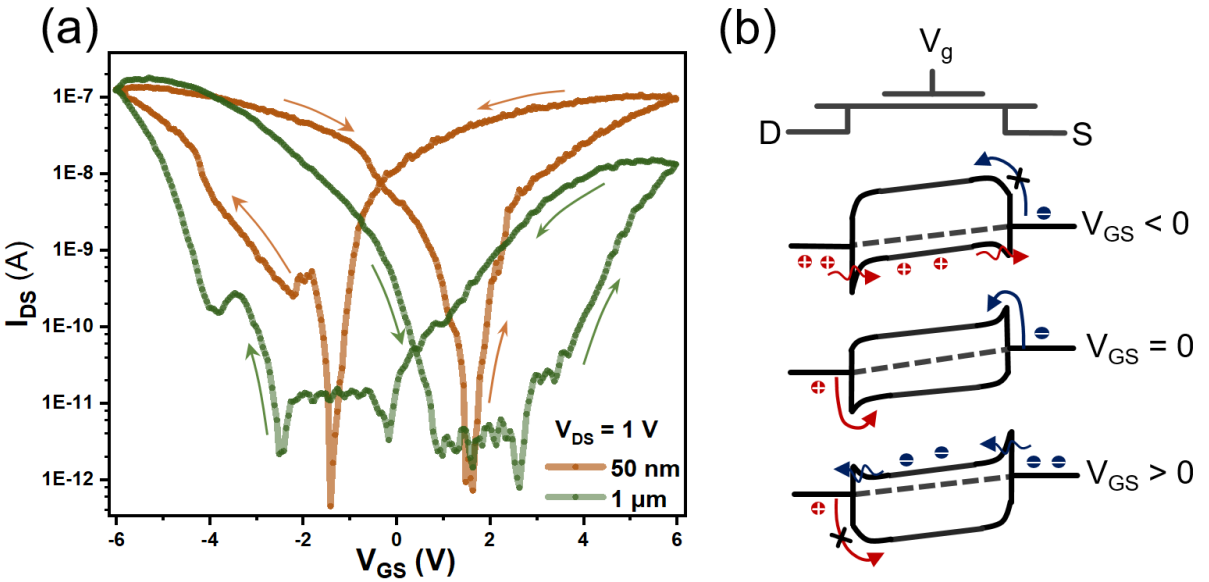


Figure 7.3: Transconductance loop of ambipolar FeFET, exhibiting anticlockwise hysteresis in the n-branch and clockwise hysteresis in the p-branch for both the 50 nm and 1 µm channel devices. (b) Band diagrams illustrating electron and hole accumulation under varying gate voltages.

The mechanism behind this behavior is further illustrated in Fig. 7.3(b), which depicts band diagrams explaining the carrier injection process. Depending on the gate voltage (V_{GS}), the Schottky barriers at the source and drain selectively facilitate either electron or hole conduction, leading to the observed ambipolar transport characteristics.

7.2.2. Impact of Channel length on Carrier Transport

I analyzed the electrical transport characteristics of transistors with channel lengths of 50 nm, 500 nm, and 1 µm. The results in Fig. 7.4(a) indicate that the rate change of I_{DS} with V_{GS} is highest for the shortest channel (50 nm) and decreases as the channel length increases. To explain this behavior, we can consider a simplified band diagram in Fig. 7.4(b) for different channel lengths. The conduction band profile, represented by the solid blue line, illustrates the initial Schottky barrier [63, 125] for an n-type transistor when $V_{GS} < V_T$ (threshold voltage for a 50 nm channel device). As V_{GS} increases beyond V_T, the conduction band shifts downward, reducing both the potential barrier height and tunneling width, as indicated by the orange-colored conduction band profile for the 50 nm channel. For comparison, conduction band profiles for the 500 nm (blue) and 1 µm (green) channels are also presented at the same V_{GS} as the 50 nm device to highlight the differences. For longer channel devices, the potential barrier also reduces with increasing V_{GS}, but the effect is significantly less pronounced.

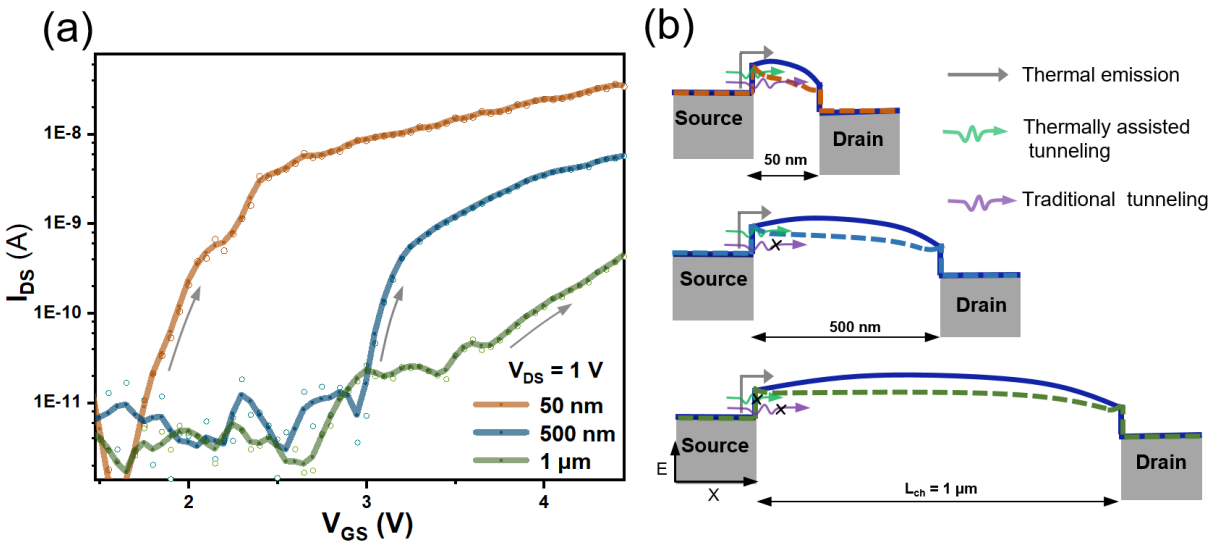


Figure 7.4: (a) Transconductance curve for the n-branch with the channel lengths of 50 nm, 500 nm, and 1 µm at $V_{DS} = 1$ V. (b) Schematic band diagrams illustrating the impact of channel length on carrier transport mechanisms.

Carrier injection from the source to the drain occurs through three primary mechanisms: thermal emission, thermally assisted tunneling, and traditional tunneling [52, 120, 126]. Thermal emission, represented by gray arrows, dominates when the Schottky barrier [127, 128] is wide, making direct tunneling negligible. Thermally assisted tunneling, indicated by green arrows, dominates in carrier transport for WSe_2-based transistors, as demonstrated by A. Prakash et al. (2017) [63]. Traditional tunneling, shown by purple arrows, occurs when the Schottky barrier narrows sufficiently to allow direct carrier injection.

For the 500 nm channel, the wider tunneling width initially suppresses traditional tunneling, requiring a higher V_{GS} to enable significant tunneling transport. In the case of the 1 µm channel, the tunneling width is even larger, further suppressing tunneling effects at lower gate voltages. As the channel length decreases, both the tunneling width and potential barrier across the channel reduce, increasing the probability of tunneling. This enhanced tunneling effect facilitates improved carrier injection through the Schottky barrier, leading to the observed increase in I_{DS} with V_{GS} for shorter channel devices.

The above discussion on thermally assisted tunneling has been analyzed using parameters related to body thickness, which refers to the thickness of the semiconductor. The tunnel barrier width has been considered equal to the semiconductor width instead of the actual tunnel barrier width [63, 120].

The literature survey is not very clear at this stage regarding the charge injection mechanism

concerning channel length. To better understand charge transport through the Schottky barrier for varying channel lengths, dedicated temperature-dependent experiments and a well-defined Schottky barrier model are needed.

7.2.3. Drain-Source Biase (V_{DS}) Influence on Transconductance

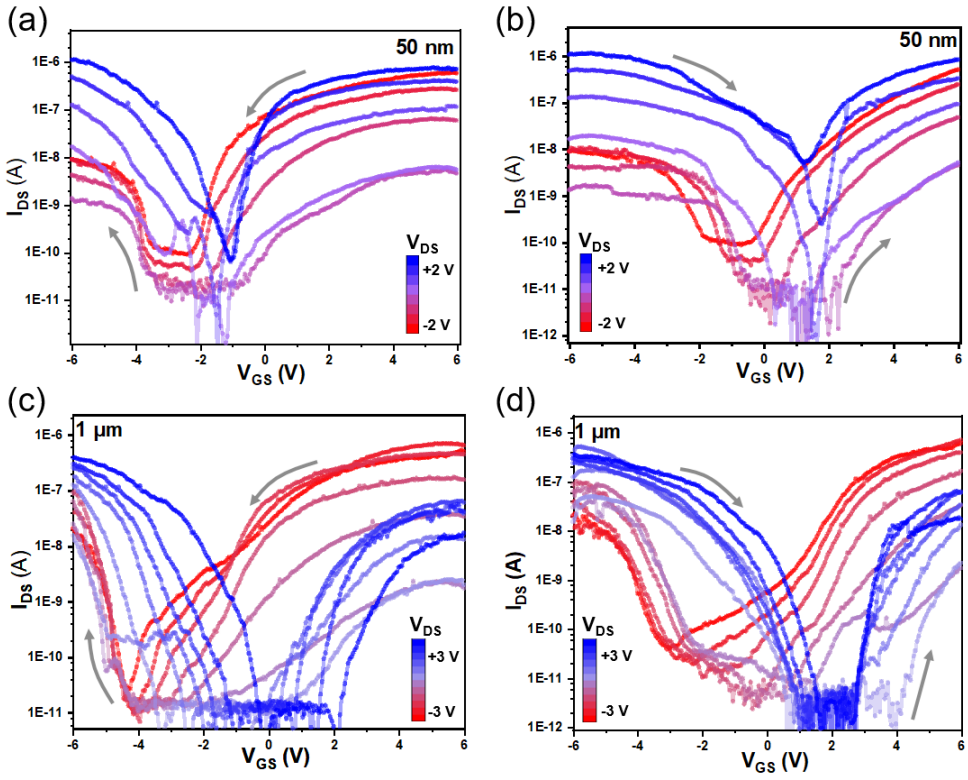


Figure 7.5: Single traces of the transconductance curve (I_{DS} vs. V_{GS}) for both forward (ascending) and reverse (descending) gate voltage sweeps at varying drain-source biases (V_{DS}). The forward sweep corresponds to V_{GS} ranging from -6 V to +6 V, while the reverse sweep follows the opposite direction. (a) Reverse sweep and (b) forward sweep for a 50 nm channel, measured at V_{DS} ranging from -2 V to +2 V. (c) Reverse sweep and (d) forward sweep for a 1 µm channel, measured at V_{DS} ranging from -3 V to +3 V. The color gradient represents different V_{DS} values, with blue indicating positive V_{DS} and red indicating negative V_{DS}.

Fig. 7.5 presents the transconductance characteristics for both 50 nm and 1 µm channel lengths, extracted from the ambipolar transconductance hysteresis curves at varying V_{DS}. The reverse sweep illustrates the transition from n-type to p-type conduction, while the forward sweep presents the transition from p-type to n-type conduction. Specifically, Fig 7.5(a) and (c) emphasize the p-type conduction branches for the 50 nm and 1 µm channels, respectively, whereas Fig 7.5(b) and (d) highlight the n-type conduction branches for the same respective

channels. A noticeable pattern in threshold voltage (V_T) shift is observed as V_{DS} varies, indicating that carrier accumulation, including electron and hole transport, is significantly modulated by the Schottky barrier at the contacts.

7.2.4. Drain-Source (V_{DS}) Induced Polarization Switching

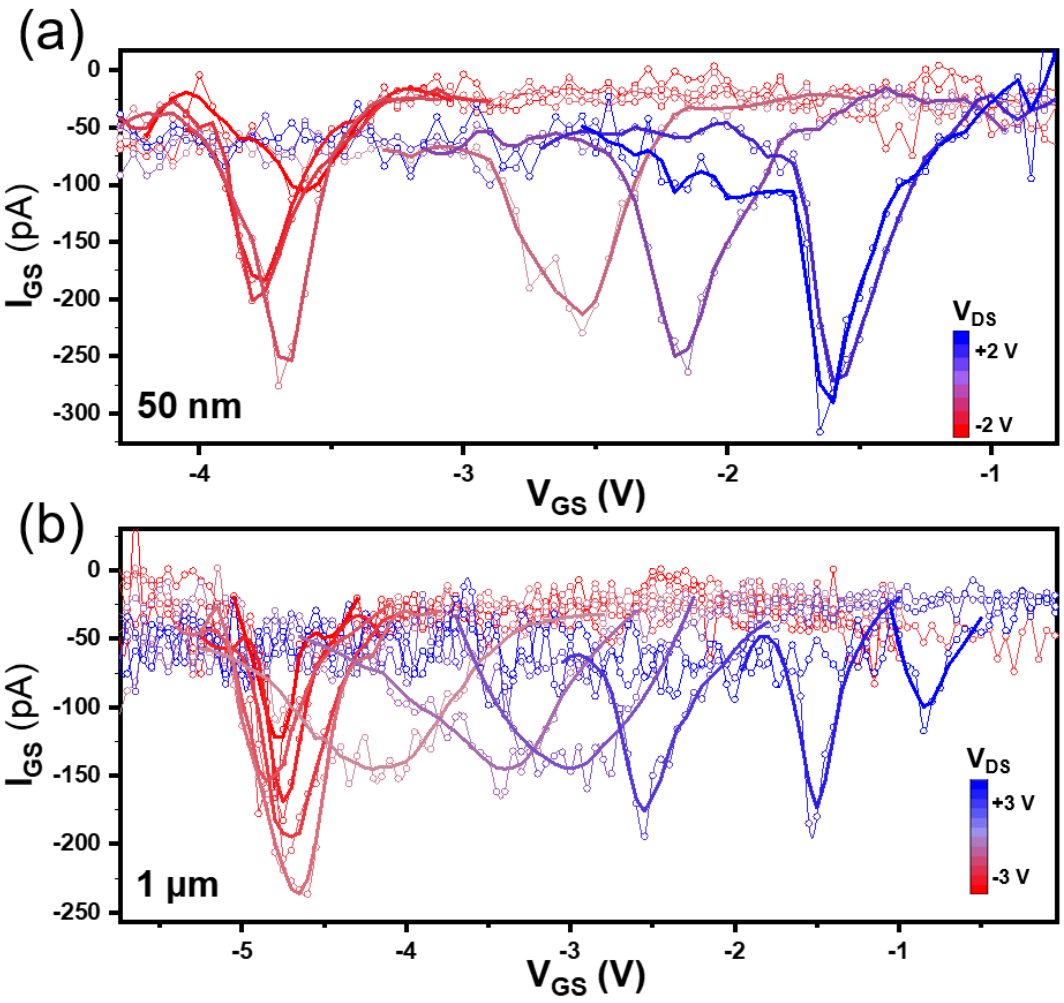


Figure 7.6: I_{GS} vs V_{GS} for the p-branch for (a) 50 nm channel where V_{DS} varies from -2 V to +2 V, and (b) 1 µm channel where V_{DS} varies from -3 V to +3 V.

Figure 7.6 presents the source-gate leakage current (I_{GS}) as a function of gate voltage (V_{GS}). During the reverse sweeping direction, an increase in current in the negative direction followed by a sudden decrease creates a hysteresis loop. The presence of this hysteresis suggests ferroelectric polarization switching behavior in the FeFET, with the abrupt change in current corresponding to the switching gate voltage.

In Figure 7.6(a) and Figure 7.6(b), both channels (50 nm and 1 µm) exhibit switching at

the same position for all negative V_{DS} values. However, for positive V_{DS}, the switching gate voltage increases with increasing V_{DS}.

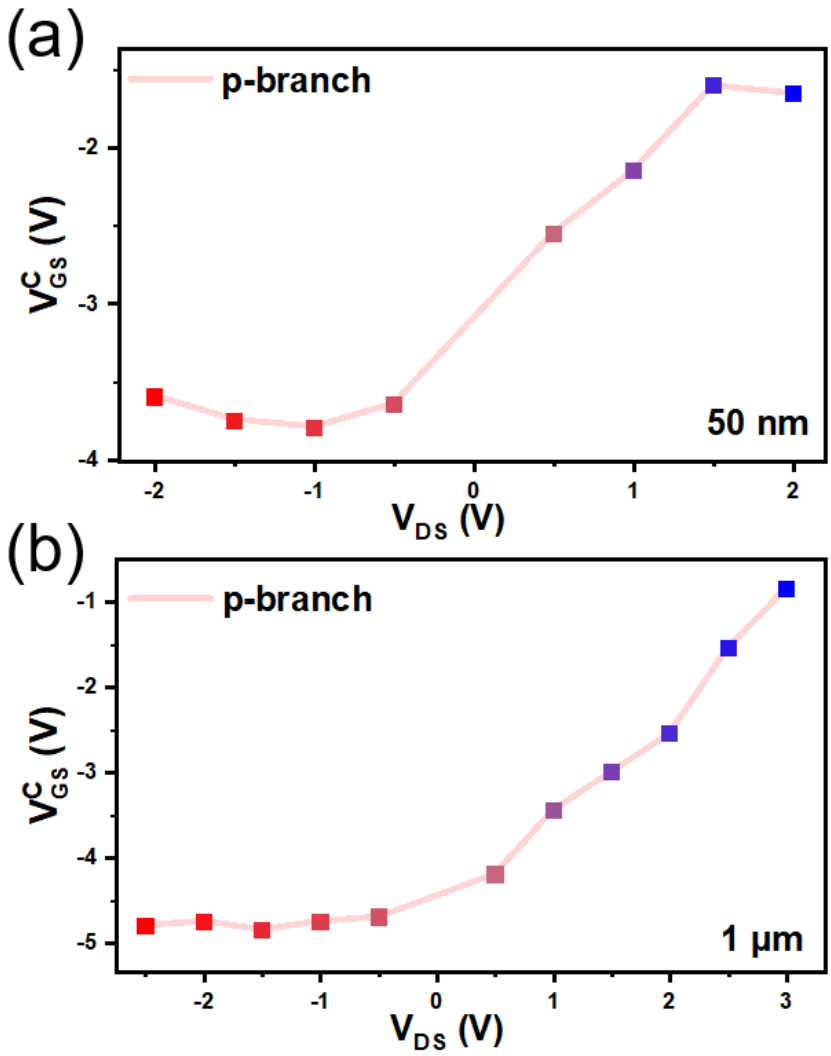


Figure 7.7: Switching gate voltage (V^c_{GS}) vs. drain-source bias (V_{DS}) for the p-branch.

The extracted switching gate voltage as a function of varying drain-source voltage for both 50 nm and 1 µm devices is shown in Figure 7.7.

7.2.5. Influence of V_{DS} on Threshold Voltage (V_T)

Figures 7.8(a) and 7.8(b) show the variation of V_T with respect to V_{DS} for the 50 nm and 1 µm devices, respectively, extracted from the transfer curves shown in Figure 7.5.

For both the channels, the change in V_T remains constant for the p-branch at negative V_{DS} but increases linearly when V_{DS} increases. In contrast, V_T remains constant for the n-branch

at positive V_{DS} but varies linearly with V_{DS} at negative values.

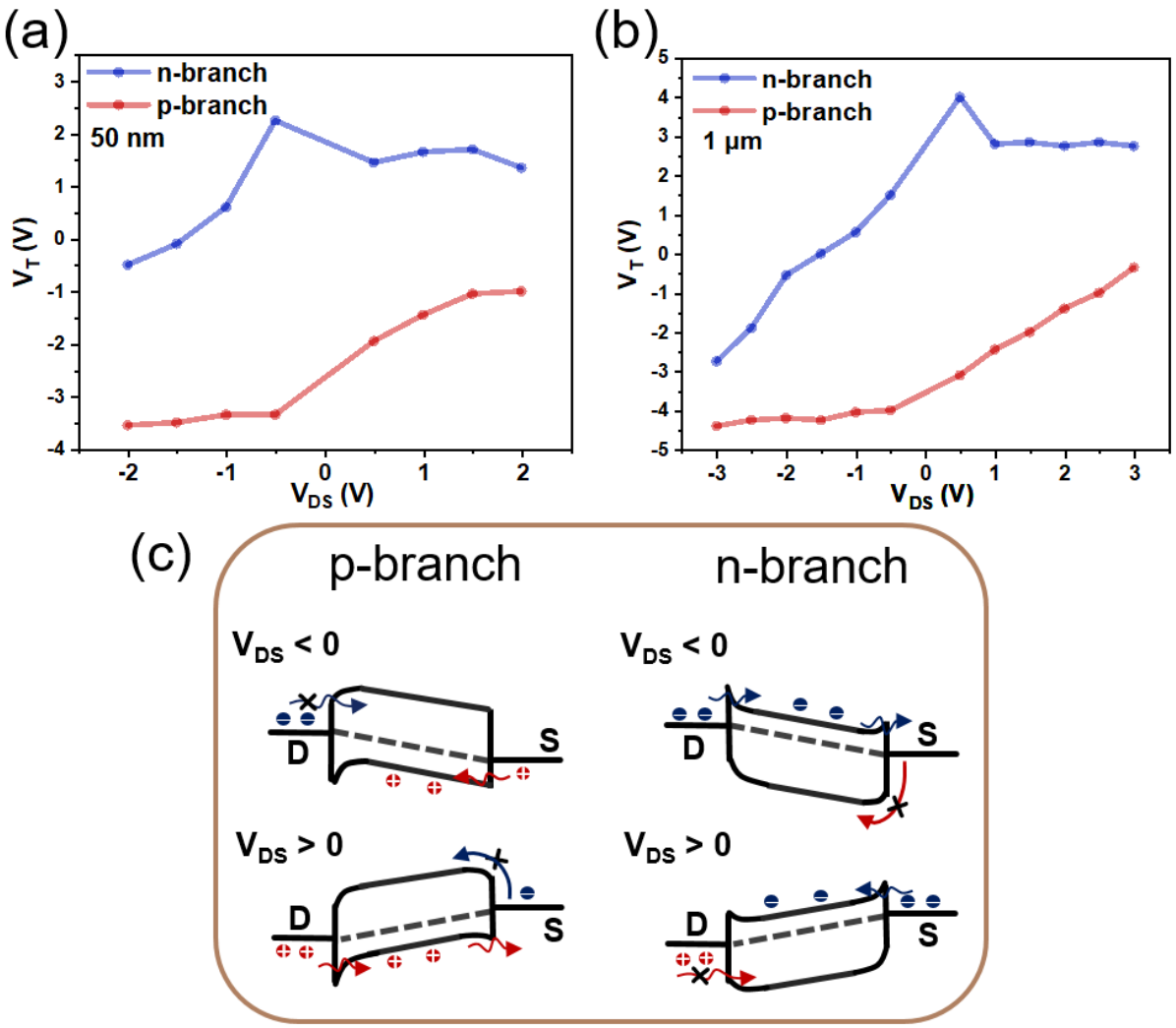


Figure 7.8: Threshold voltage (V_T) variation as a function of V_{DS} for the 50 nm (a) and 1 μm (b) devices. (c) Band diagrams illustrating p-type and n-type transport behaviors under different V_{DS} conditions.

These shifts in V_T suggest that V_{DS} modulates the ferroelectric switching behavior. This is further confirmed by Figure 7.7, which demonstrates a correlation between switching gate voltage and V_{DS}. The similarity between the V_T vs. V_{DS} curve in Figure 7.8(a-b) and the switching gate voltage (V_{GS}^c) vs. V_{DS} curves in Figure 7.7 supports this conclusion, indicating that the threshold voltage shift in transconductance corresponds to ferroelectric polarization switching.

The band diagrams in Figure 7.8(c) explain the transport mechanism under different V_{DS} conditions. When a positive gate voltage is applied to the top gate, the polarization of CIPS

induces hole accumulation in the WSe_2 channel, leading to p-type transport. Conversely, a negative top-gate voltage induces electron doping, enabling n-type transport [129]. The V_{DS}-induced switching mechanism can be understood through the effective gate voltage (V_{eff}), given by:

$$V_{eff(CIPS)} = V_{GS} - V_{DS} \tag{7.1}$$

This effective voltage determines the coercive field required for ferroelectric switching.

For the p-branch, when $V_{DS} < 0$, holes inject from source to drain, making the source potential the limiting factor, and the drain potential does not contribute to V_{eff}. As a result, V_{eff} is determined solely by V_{GS}, leading to no change in V_T with respect to V_{DS}. When $V_{DS} > 0$, holes inject from drain to source, and the drain potential modifies V_{eff}, causing a linear shift in V_T.

Similarly, for the n-branch, when $V_{DS} < 0$, electrons inject from drain to source, and the drain potential modulates V_{eff}, leading to a linear shift in V_T. In contrast, when $V_{DS} > 0$, electrons conduct from source to drain, making the source potential the limiting factor, and V_T remains unchanged with respect to V_{DS}.

These observations align with the transport curves in Figure 7.5, highlighting the role of V_{DS}-induced modulation in the transport characteristics and switching behavior of CIPS/WSe_2-based FeFETs.

7.3. Short Channel Effect analysis

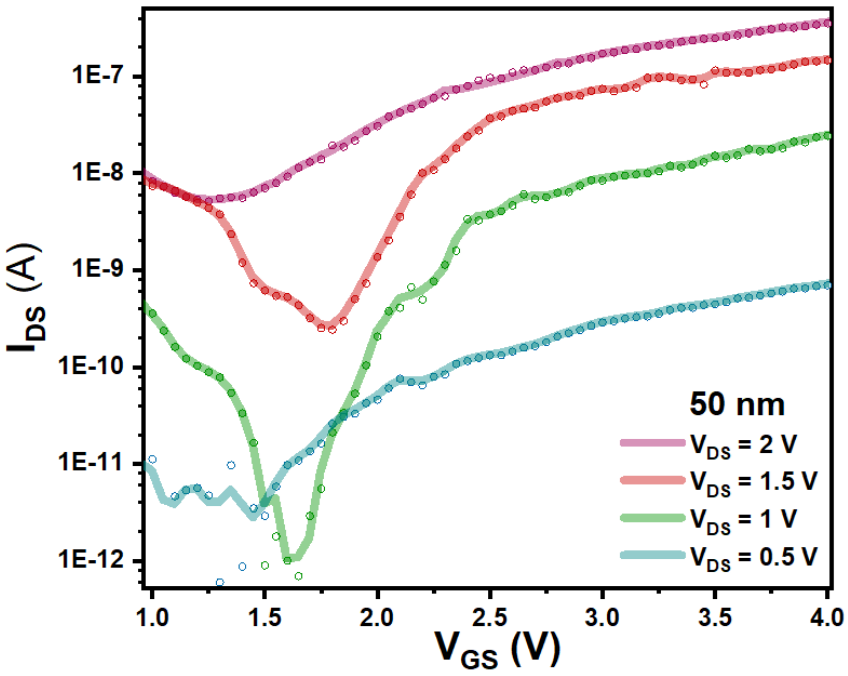


Figure 7.9: Transconductance forward sweep for the 50 nm channel at different V_{DS}.

Figure 7.9 presents the transfer characteristics of the FeFET device at different drain-source voltages (V_{DS}) ranging from 0.5 V to 2 V. Initially, as V_{DS} increases from 0.5 V to 1 V, V_T increases. However, beyond $V_{DS} = 1$ V, V_T begins to decrease, and a significant rise in leakage current is observed.

This behavior corresponds to drain-induced barrier lowering (DIBL) [85], a well-known short-channel effect. DIBL occurs when an increase in V_{DS} reduces the potential barrier at the source-channel junction, leading to threshold voltage reduction and an increase in off-state leakage current. It is quantitatively expressed as:

$$\text{DIBL} = -\frac{\Delta V_T}{\Delta V_{DS}} \tag{7.2}$$

For low $V_{DS} = 0.5$ V and high $V_{DS} = 1$ V, the calculated DIBL value is -0.4 and leakage current is reduced as compared to $V_{DS} = 0.5$ V. This observation supports the presence of reverse DIBL, where an initial increase in V_T is observed However, for V_{DS} values beyond 1V, DIBL becomes positive, and leakage current increases drastically. For longer channel devices, the DIBL effect is negligible, confirming that DIBL is a short-channel effect.

7.3.1. Schematic Representation of DIBL and Reverse DIBL

A schematic representation of DIBL and reverse DIBL is shown in Figure 7.10, illustrating how the potential barrier [130] decreases for higher V_{DS} in DIBL, whereas an opposite trend is observed in reverse DIBL.

In short-channel devices [131, 132], reverse DIBL is commonly associated with negative capacitance field-effect transistors (NC-FETs). The observed increase in V_T as V_{DS} increases, resulting in reverse DIBL furthure confirms negative capacitance properties of 50 nm short-channel FeFET device.

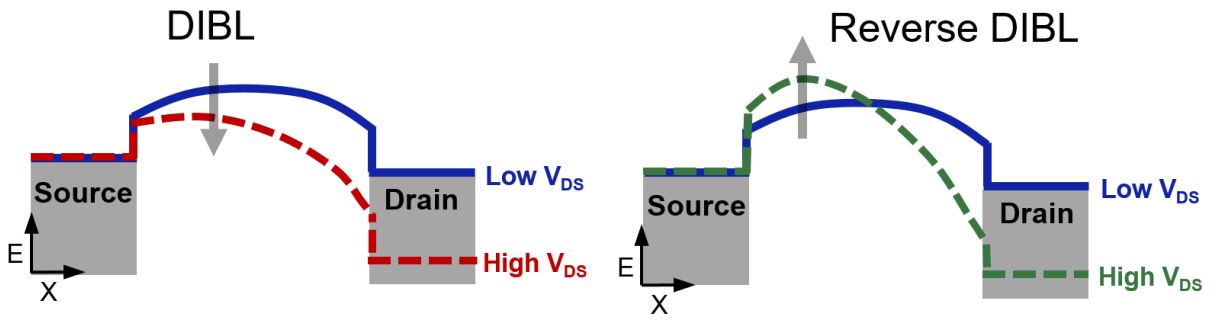


Figure 7.10: Schematic representation of DIBL and reverse DIBL.

7.3.2. Negative Capacitance Effect

Ferroelectric field-effect transistors (FeFETs) are also known as negative capacitance field-effect transistors (NC-FETs), as detailed in Chapter 4. The switching performance of a transistor is often evaluated using the subthreshold swing (SS), which represents the gate voltage (V_G) required to increase the drain current (I_D) by one order of magnitude (10×) in the subthreshold regime. SS can be directly determined by transconductance curve, and its mathematical expression is defined by:

$$SS = \frac{dV_G}{d(\log I_D)} \tag{7.3}$$

The thermionic limit of SS is 60 mV/decade at room temperature. However, in FeFETs, it is possible to achieve SS values below this fundamental limit, enhancing switching speed and energy efficiency. This improvement is attributed to the integration of ferroelectric materials,

which induce an effective negative capacitance. Further theoretical details and equations are discussed in Chapter 4.

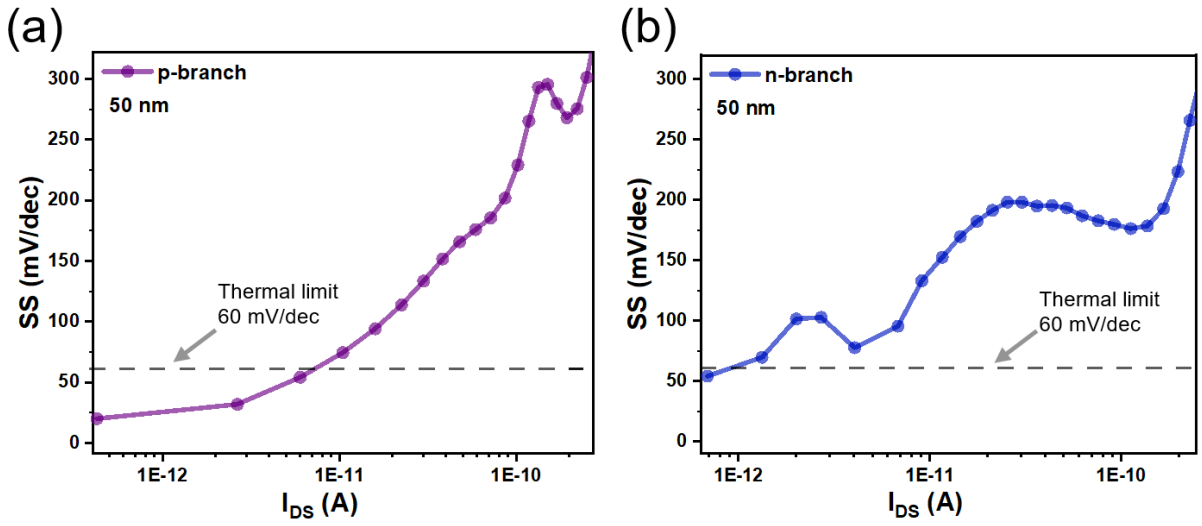


Figure 7.11: Subthreshold swing for the 50 nm channel device. (a) p-branch and (b) n-branch.

Figure 7.11 presents the subthreshold swing for the 50 nm channel device, clearly showing SS values below the thermionic limit. The SS is calculated by differentiating V_{GS} with respect to $\log I_{DS}$, as presented in Eq. (7.3).

We further analyzed SS for devices with channel lengths of 250 nm, 500 nm, and 1 µm, as illustrated in Fig. 7.12. The results confirm that shorter-channel devices exhibit faster switching, characterized by lower SS values. This trend is also evident in the transconductance curves for different channel lengths, as shown in Fig. 7.4.These findings are consistent with previous research [133], highlighting the advantage of NC-FETs with shorter channel lengths in achieving lower SS and better subthreshold performance compared to conventional transistors.

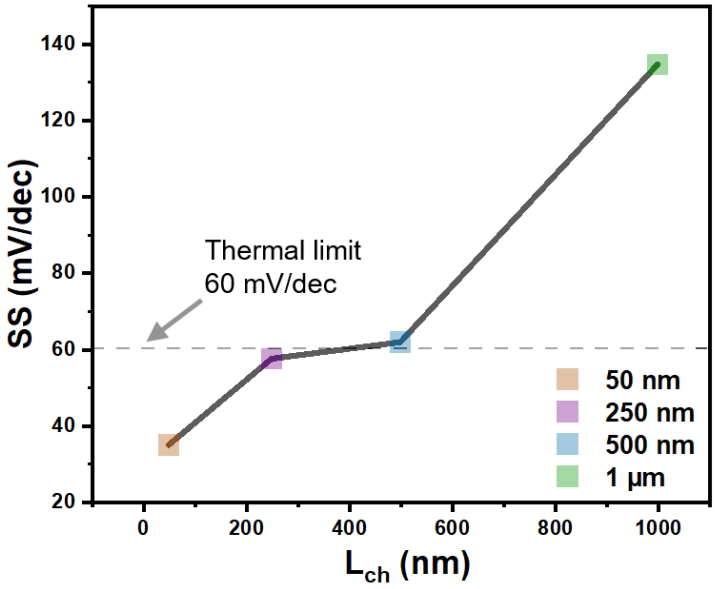


Figure 7.12: Subthreshold swing (SS) vs. channel length (L_{ch}).

These results validate the potential of short-channel FeFETs for achieving enhanced switching efficiency and ultra-low-power applications, making them promising candidates for future semiconductor technology.

7.4. Reconfigurability with Ferroelectric Floating Top Gate and Back Gate

The device demonstrates reconfigurable functionality, enabling operation in n-type FET, p-type FET, and ambipolar FeFET modes. This reconfigurability is achieved through a ferroelectric floating top gate, with readout performed via capacitive coupling to the back gate. The experiment highlights the partial polarization switching mechanism of the ferroelectric domains, which is discussed in detail in Ch. 8. The partial switching characteristics of $CuInP_2S_6$ allow the FeFET to achieve multiple stable doping states.

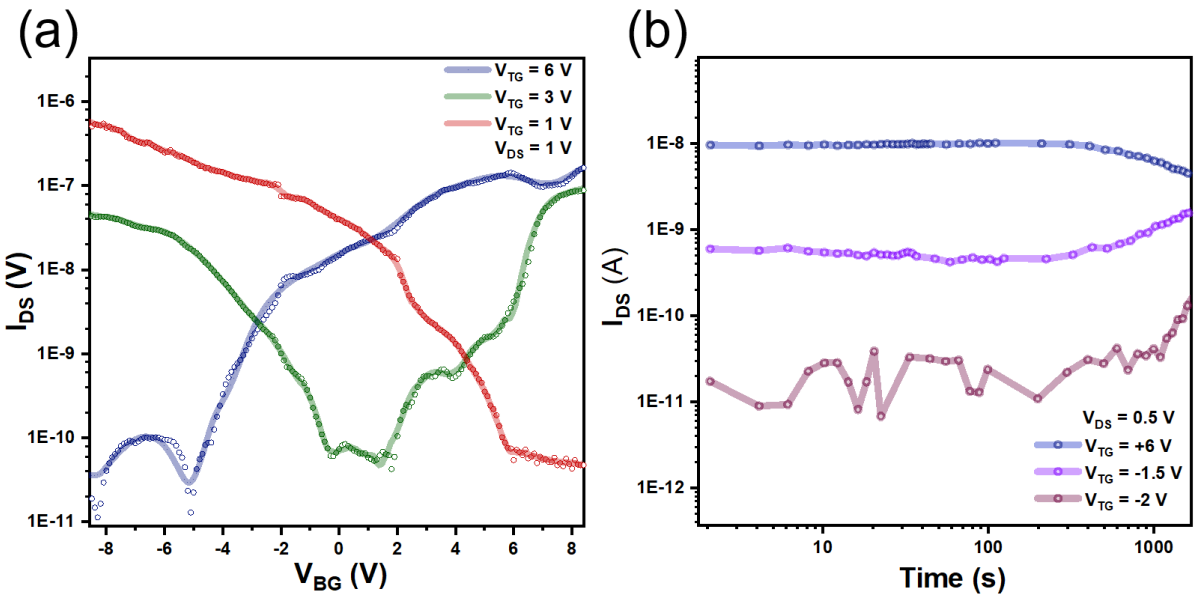


Figure 7.13: (a) Transconductance characteristics of the device measured by sweeping the back gate voltage under different remanent doping states programmed by the ferroelectric floating top gate. (b) Retention characteristics of various doping states, illustrating the stability of the programmed states over time.

Figure 7.13(a) presents the transconductance curves corresponding to distinct doping states programmed by applying single pulses of +6 V, +3 V, and +1 V to the top gate. When a +6 V pulse is applied, the $CuInP_2S_6$ (CIPS) layer polarizes downward, inducing electron doping in the semiconductor channel, resulting in n-type transconductance behavior. A +3 V pulse places CIPS in an intermediate polarization state (not fully upward), reducing electron doping and tuning the device into an ambipolar state that exhibits both n-type and p-type conduction characteristics. When a +1 V pulse is applied, further reversal of the upward polarization state alters the doping state, ultimately shifting the device into a p-type mode.

Notably, these distinct FET modes are observed within the back gate sweeping range of -8.5 V to +8.5 V. Other values of the top gate voltage can further modulate this behavior within different ranges. Intrestingly, these programmed states are achieved and maintained using just a single 1 ms programming pulse, demonstrating efficient and robust programming.

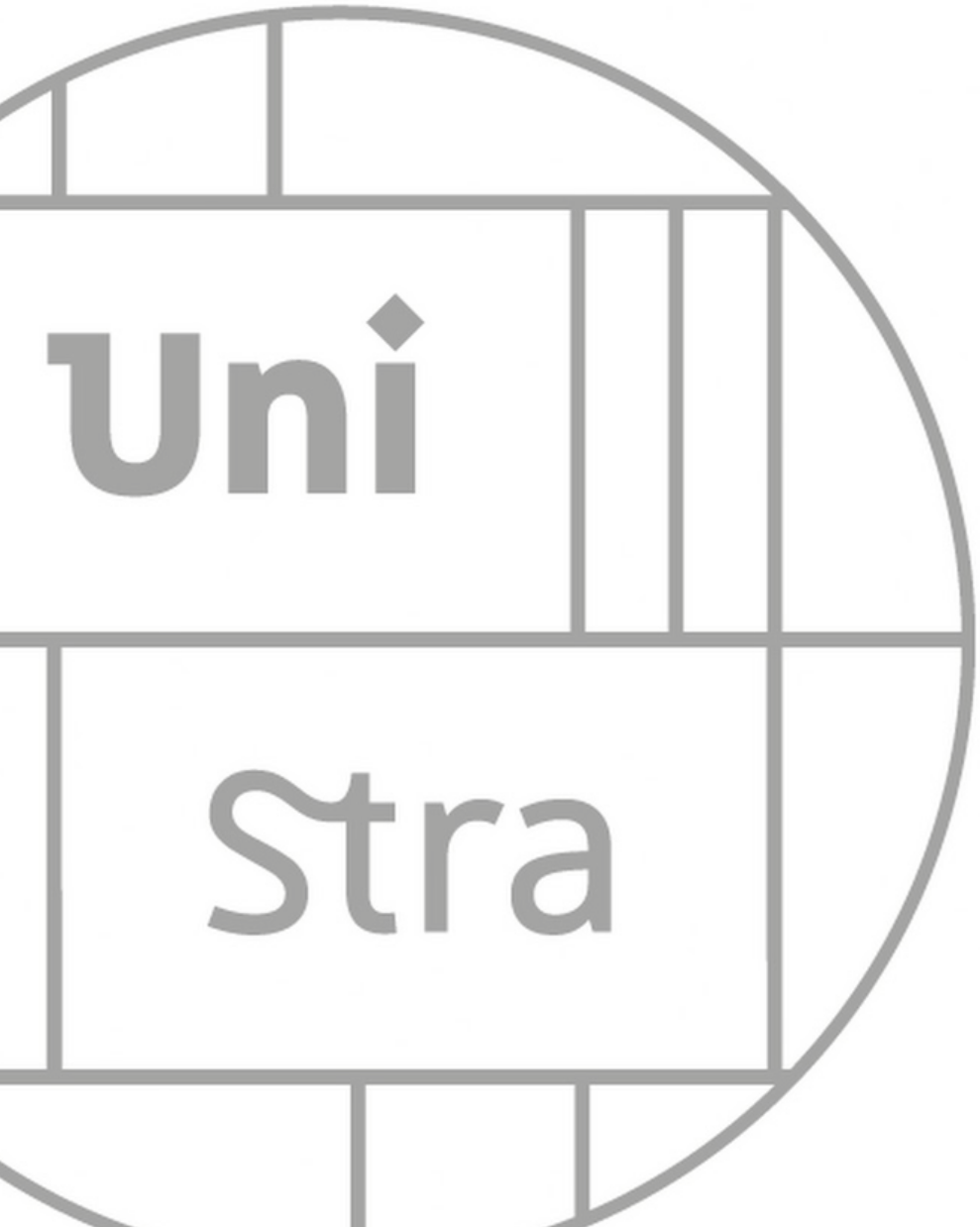
Figure 7.13(b) illustrates the retention properties of the various doping states, demonstrating the long-term stability of the programmed states for top gate pulse values of +6 V, -1.5 V, and -2 V. The +6 V pulse establishes the "on" state, while the -1.5 V pulse results in an intermediate state, and the -2 V pulse corresponds to the "off" state of the device when sweeping in the reverse direction (from +6 V to -6 V). This behavior is reflected in the transconductance curve of the device in Fig. 7.3. The current levels associated with these states remain stable over

extended periods exceeding 10^3 seconds, confirming the nonvolatile nature of the ferroelectric floating gate and its ability to maintain different doping configurations.

This reconfigurability, combined with the stability of the doping states, enables the device to switch between p-type and n-type FET modes, which has significant potential for applications such as high-performance complementary inverters, polymorphic gates, and hardware security implementations [27].

7.5. Conclusion

- I systematically studied the scaling effects in $CuInP_2S_6/WSe_2$-based van der Waals Ferroelectric Field-Effect Transistors (FeFETs) by fabricating short-channel devices with different channel lengths. Our findings show that reducing the channel length significantly affects charge transport and device performance. Shorter channels exhibit a higher rate of current change with respect to the applied gate voltage compared to longer ones.
- The study of transconductance characteristics under varying drain-source biases (V_{DS}) highlights how carrier accumulation and ferroelectric polarization switching are influenced by V_{DS}, directly impacting the threshold voltage (V_T).
- I analyzed short-channel effects such as Drain-Induced Barrier Lowering (DIBL) and reverse DIBL, confirming the presence of negative capacitance effects in these FeFETs. The subthreshold swing (SS) analysis further supports that short-channel FeFETs achieve SS values below the thermionic limit, leading to better switching efficiency and lower power consumption. This makes short-channel negative capacitance FeFETs ideal for ultra-low-power logic applications.
- Another key feature is the device's reconfigurability, made possible by a ferroelectric floating top gate and a back gate. By leveraging the partial polarization switching of $CuInP_2S_6$, the device can dynamically transition between n-type, p-type, and ambipolar FET modes, allowing for nonvolatile multi-state operation.
- The combined insights from scaling effects and reconfigurability offer valuable guidance for designing next-generation 2D FeFETs. These results position short-channel $CuInP_2S_6/WSe_2$ FeFETs as strong candidates for future low-power, high-performance, and reconfigurable electronic applications.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8 | Reconfigurable Exhibitory/Inhibitory Ferroelectric Synapse based on van der Waals Heterostructure

This chapter introduces a reconfigurable synapse based on a $CuInP_2S_6$/hBN/WSe_2 heterostructure, designed to address critical challenges in neuromorphic computing. Through precise electrical modulation of ferroelectric domains in the $CuInP_2S_6$ gate spacer, it is possible to finely tune the WSe_2 channel conductance and the transistor threshold voltage (V_{Th}). This level of control forms the basis for synaptic behavior with tunable weights, opening the door to adaptable and energy-efficient artificial synapses.

The ambipolar nature of WSe_2 plays a crucial role in enabling reconfigurable synaptic properties. By carefully designing voltage pulse sequences, we control the population of ferroelectric domains within the $CuInP_2S_6$ gate and fine-tune its polarization state, directly influencing device conductance. Furthermore, pre-programmed voltage pulses enable FeFET [134, 135] to switch between n-type and p-type conduction modes, allowing it to function as an artificial synapse [136] in two distinct modes, mediated by electron or hole carriers. These modes exhibit opposing synaptic plasticity, allowing the device to operate as either an inhibitory or excitatory synapse[137, 138], with real-time reconfigurability triggered by tailored voltage pulses.

The scalability of the reconfigurable synapse is demonstrated across devices with channel lengths ranging from $1\,\mu m$ to $50\,nm$, 100 times shorter than previous configurations in similar ferroelectric vdW systems. Finally, we benchmark the performance of our reconfigurable synapse by integrating it into Artificial Neural Network simulations, achieving excellent accuracy.

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8.1. Device Architecture

Fig. 8.1(a) presents the schematic of the 2D-FeFET device architecture discussed in this work. The device features a WSe_2 layer as the ambipolar semiconductor channel, deposited onto Ti/Au source and drain electrodes pre-patterned on a Si/SiO_2 substrate. Above the WSe_2 layer, a heterostructure comprising hBN and $CuInP_2S_6$ (CIPS) serves as the dielectric/ferroelectric gate spacer, capped by a Ti/Au top gate electrode. To evaluate device scalability, FeFETs with both $1\,\mu m$ long channel and $50\,nm$ short channel were fabricated. For the sake of meaningful comparison, both the long- and short-channel 2D-FeFET devices were fabricated from the same WSe_2/hBN/CIPS heterostructure. Fig. 8.1(b) presents an optical image of the fabricated device, showing the top view captured via optical microscopy.

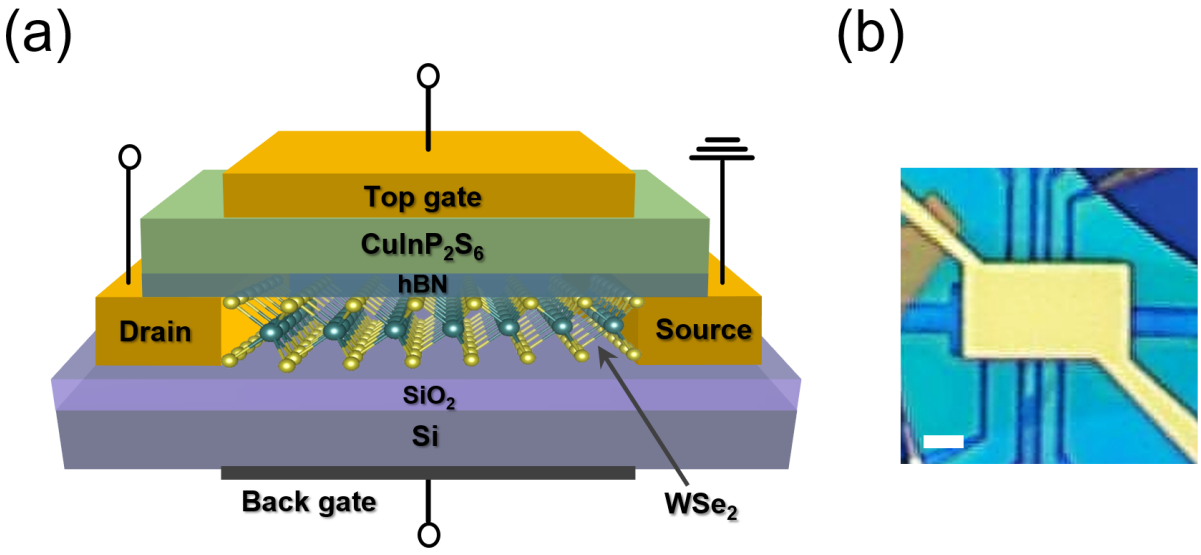


Figure 8.1: (a) Schematic of the Reconfigurable FeFET synaptic device. (b) Optical microscope image with a scale bar of $2\,\mu m$.

8.2. Vertical piezoresponse force microscopy (VPFM)

[This PFM study was conducted in collaboration with postdoc Shehr Bano under the supervision of Alexei Gruverman at the University of Nebraska-Lincoln.]

The ferroelectric properties of the $CuInP_2S_6$ (CIPS) layer (50 nm thick) were characterized after its transfer onto pre-patterned electrodes using vertical piezoresponse force microscopy (VPFM). Fig. 8.2(a) (left) shows the optical image, while Fig. 8.2(a) (right) presents the VPFM topography scan over a $20\,\mu m \times 20\,\mu m$ area, confirming the presence of ferroelectric domains.

In Fig. 8.2(b), a PFM scan over a $2\,\mu m \times 2\,\mu m$ area reveals topography (top), phase (middle), and amplitude (bottom) signals, providing detailed insights into the spatial distribution of the piezoelectric response and polarization orientation. The presence of well-defined ferroelectric domains with opposing polarizations perpendicular to the flake is clearly observed, aligning with previous studies on this material [65].

Additionally, switching spectroscopy was conducted using the PFM tip (Fig. 8.2(c)), revealing well-defined polarization switching characteristics. The phase response (top panel) exhibits a sharp 180° shift, while the amplitude response (bottom panel) presents a characteristic butterfly loop, further confirming the robust ferroelectric nature of the CIPS flakes at room temperature.

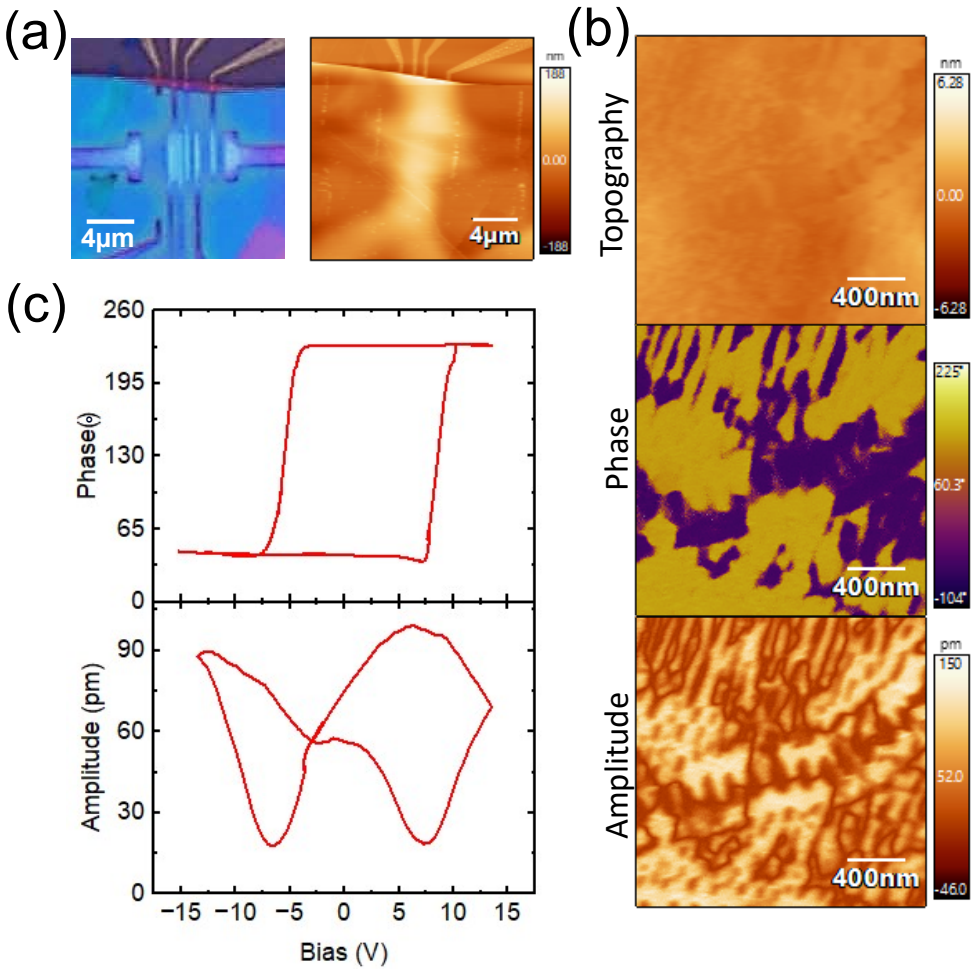


Figure 8.2: (a) Optical image (left) and PFM scan topography (right) on $CuInP_2S_6$, scanned over a $20\,\mu m \times 20\,\mu m$ area. (b) High-resolution $2\,\mu m \times 2\,\mu m$ PFM scan showing topography (top), phase (middle), and amplitude (bottom). (c) Switching spectroscopy was performed using the PFM tip, revealing clear polarization switching signatures in the phase (top) and amplitude (bottom) signals.

PFM analysis on $CuInP_2S_6$ capacitor device:

[PFM characterization on CIPS capacitor device was carried out in collaboration with Stéphane Fusil at Laboratoire Albert Fert, CNRS, Thales, Université Paris-Saclay.]

To further validate the polarization switching of CIPS under an applied gate field, a $CuInP_2S_6$ capacitor device was fabricated (Fig. 8.3(a). The device was structured by transferring exfoliated CIPS onto a pre-patterned substrate, followed by the deposition of metallic electrode arrays for electrical probing.

The PFM phase images in Fig. 8.3(b) and (c) clearly illustrate polarization reversal upon voltage excitation via the top electrodes. After applying $V_{DC} = -10V$, a downward polarization is dominant, showing dark contrast in the PFM phase image. Conversely, applying $V_{DC} = +10V$ results in an upward polarization, appearing as bright contrast. Nearly complete switching is observed, though some minority domains remain pinned in their previous state. The amplitude of the poling voltage was chosen to exceed the coercive field, which was identified from the piezoresponse hysteresis cycle measurement performed locally on CIPS (Fig. 8.3(d)).

This direct insight into the polarization landscape modification at opposite saturation confirms that the transconductance hysteresis measured on the 2D-FeFET arises from the gate-controlled switching of the CIPS polarization.

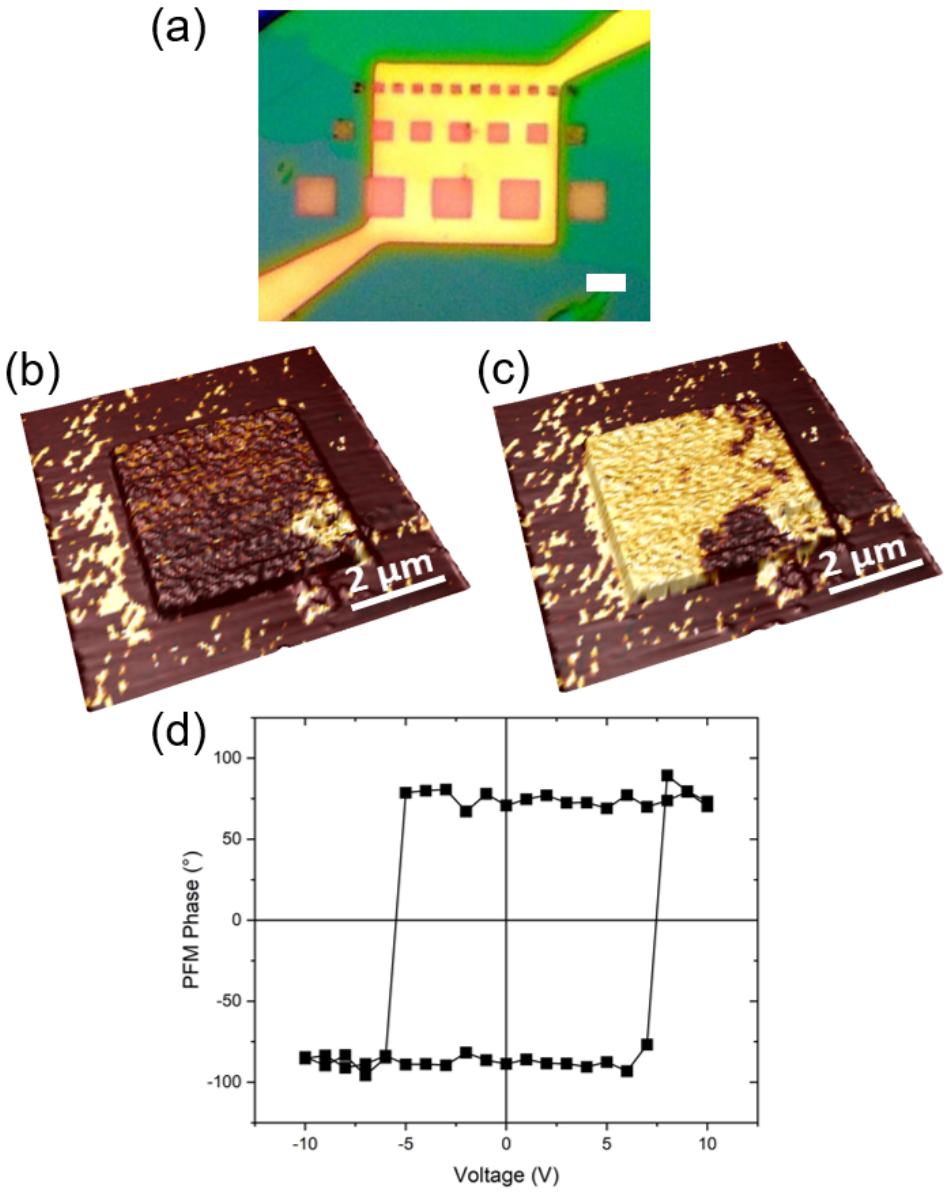


Figure 8.3: (a) Optical image of the $CuInP_2S_6$ capacitor device. (b, c) PFM phase images after poling with $V_{DC} = -10V$ and $+10$ V, respectively, showing polarization switching. Dark contrast in (b) corresponds to downward polarization, while bright contrast in (c) represents upward polarization. (d) PFM phase hysteresis loop measured locally on bare CIPS, with a coercive switching bias of $V_{DC} = \pm 6$ V.

8.3. Transport Characteristics of the Device

I first characterize the transconductance and memory window characteristics of the device, essential for evaluating their synaptic functionality. Fig. 8.4(a) and 8.4(b) show typical I_{SD}-V_{CG} transfer curves, performed respectively on the $1\,\mu\mathrm{m}$ and $50\,\mathrm{nm}$ long channel devices,

measuring the I_{DS} source-drain current under application of a source–drain voltage $V_{DS} = 0.5$ V. Both devices exhibit clear ambipolar behavior, with distinct n-type and p-type conduction branches observed as V_{GS} is swept between ± 6 V in both forward and reverse directions.

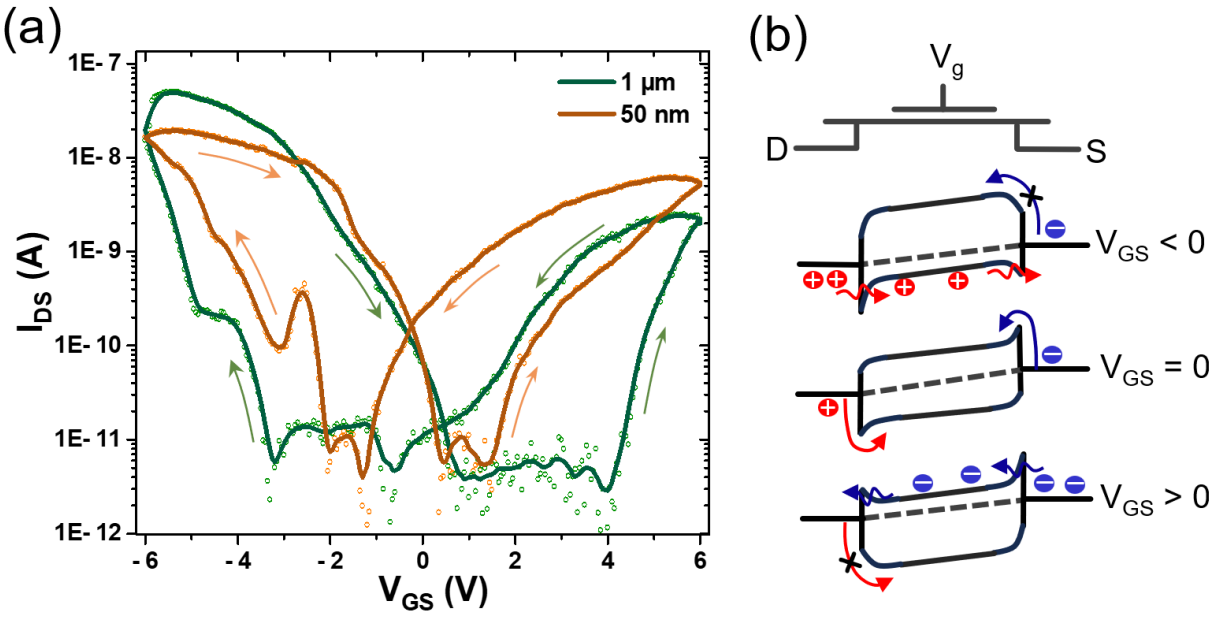


Figure 8.4: (a) Transfer curve of the devices with $50\,\mathrm{nm}$ and $1\,\mu\mathrm{m}$ long channels, demonstrating clear ambipolar behavior and hysteresis characteristics. (b) Band diagrams illustrating electron and hole transport under different gate conditions.

This ambipolarity arises from the intrinsic properties of WSe_2 with small band gap of 1.3 eV enables both electron and hole conduction. The transport mechanism, depicted in Fig. 8.4(b), illustrates how electrons and holes traverse the Schottky barriers at the source and drain under varying gate biases. The gate-controlled modulation of charge carriers enables ambipolar transport, where electron conduction dominates under positive gate bias, while hole conduction is favored under negative gate bias.

This behavior follows the general Schottky barrier injection theory for 2D semiconductors [63, 125, 139], where energy-level alignment at the contacts plays a key role in enabling ambipolar transport. The promotion of n- or p-type charge carriers involved in the electronic transport depends on the cumulative effects of the polarization state of $CuInP_2S_6$ and the electrostatic electric field applied through it, both controlled by the top gate voltage.

The transconductance characteristics in Figure 8.4(a) exhibit a well-defined hysteresis loop, where the *n*-branch follows an anticlockwise path, and the *p*-branch follows a clockwise path. This confirms that the memory window in FeFETs is dictated solely by CIPS ferroelectric polarization switching, without the influence of trap states, which would otherwise produce

opposite traversal directions.

Furthermore, the Fig. 8.5(a) and Fig. 8.5(b) report series of $I_{SD} - V_{GS}$ transfer curves of increasing sweeping range exceeding the ferroelectric coercive field. It is observed that upon increasing the sweeping range, the memory windows of the p and n branch remains unaffected. Moreover, all the curves merge onto the same external envelope beyond the coercive field window. Such signatures are typical of FeFET transconductance and rules out other mechanisms such as floating gate or trap assisted effects that would result in an increase of the memory window.

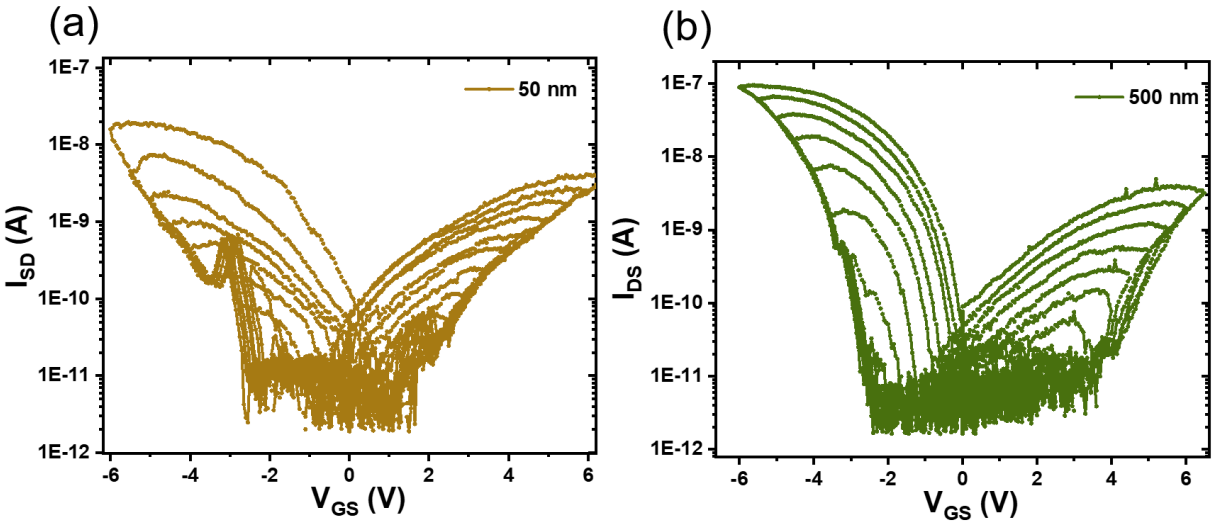


Figure 8.5: Tranfer charecteristic of (a) 50 nm and (b) 500 nm channel devices, under increasing sweeeping range of the gate voltage, at $V_{\mathrm{DS}} = 0.5$ V.

8.4. Switching Kinetics of Ferroelectric Domain

Next, I investigated the electrical control of the multi-domain structure in the van der Waals (vdW) ferroelectric layer and its transduction properties. To achieve this, I design gate voltage pulse sequences that finely tune the ferroelectric domain distribution and the correlated WSe_2 channel conductivity. Furthermore, while analyzing the short-channel 2D-FeFET properties, I aim to provide deeper insights into the scalability of ferroelectric domain control in vdW ferroelectrics, particularly below the technologically strategic sub-100 nm scale.

[PFM characterization presented in Fig. 8.6 was carried out in collaboration with Stéphane Fusil at Laboratoire Albert Fert, CNRS, Thales, Université Paris-Saclay.]

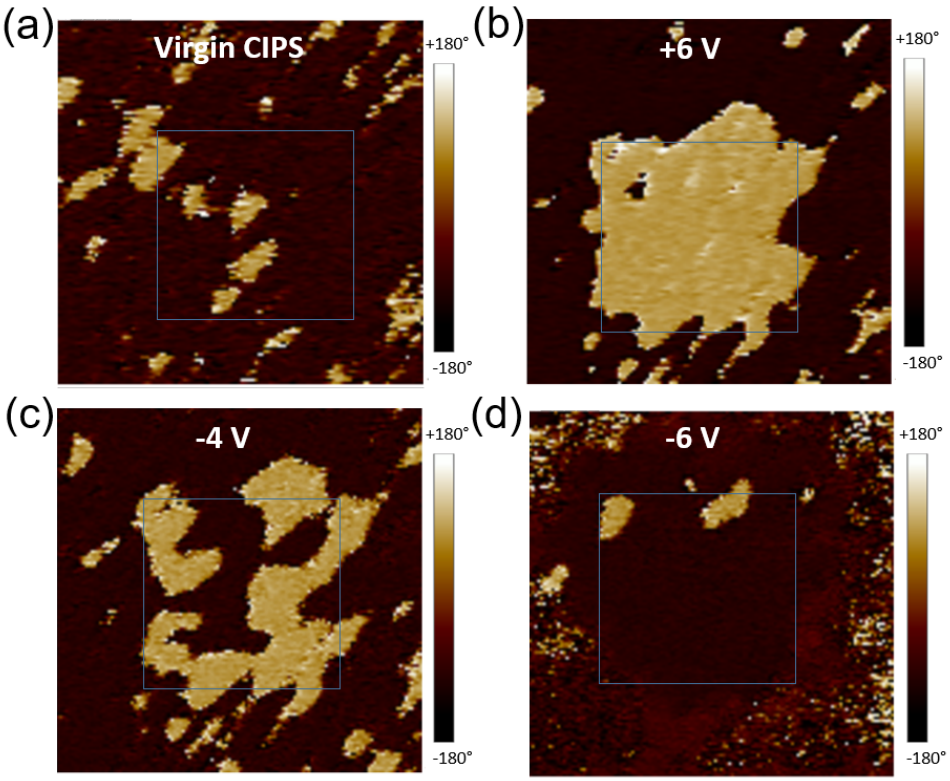


Figure 8.6: PFM phase images illustrating polarization switching in CIPS under different gate voltages. (a) Initial ferroelectric domain landscape with a mix of downward (dark) and upward (bright) polarized regions. (b) PFM image after poling a 1 μm^2 region (blue square) with $V_{DC} = +6$ V while keeping the PFM tip grounded, resulting in a uniformly upward-polarized (bright) region. (c) Partial back-switching of the previously poled region following the application of $V_{DC} = -4$ V, leading to a mixed domain configuration. (d) Near-complete reversal of polarization upon applying $V_{DC} = -6$ V, demonstrating effective ferroelectric domain switching.

Fig. 8.6 presents PFM phase images (1 μm^2 area) of a $CuInP_2S_6$ (CIPS) flake used as a gate spacer after applying different poling voltages. The PFM analysis confirms that the ferroelectric domain configurations can be effectively tailored by adjusting the applied gate voltage. Fig. 8.6(a) shows the initial ferroelectric domain configuration, consisting of a mix of downward (dark) and upward (bright) polarized regions. In Fig. 8.6(b), the blue-marked area highlights a fully upward-polarized region created when a back-gate voltage of $V_{DC} = +6$ V is applied while the Pt-coated PFM tip remains grounded. Conversely, applying a back-gate voltage of $V_{DC} = -6$ V results in an almost complete reversal of polarization, as shown in Fig. 8.6(d). Interestingly, an intermediate domain configuration is achieved with $V_{DC} = -4$ V, leading to partial back-switching and the formation of distinct subpopulations of upward and

downward polarized domains, as seen in Fig. 8.6(c).

We I investigate how such electrical control on ferroelectric domain populations is transduced into fine-tuning of the conduction states of the device. The analysis of partial polarization switching in $CuInP_2S_6/WSe_2$-based FeFETs is conducted using a tailored pulse scheme, systematically applying reference and write pulses to the top gate while monitoring the resulting transconductance characteristics.

Pulse Schemes:

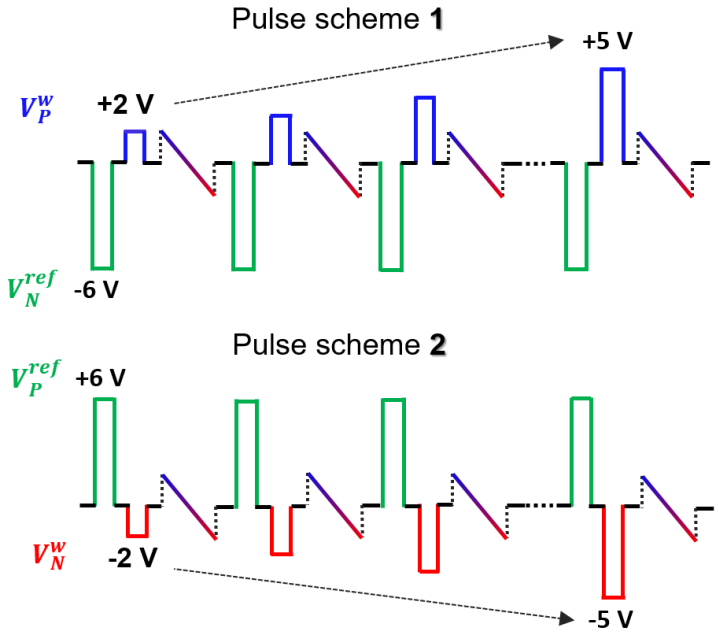


Figure 8.7: Pulse schemes for controlling ferroelectric domain switching in $CuInP_2S_6/WSe_2$-based FeFETs. (Top) Pulse Scheme-**1**: negative reference pulse (V_N^{ref}) followed by positive write pulses (V_P^w). (Bottom) Pulse Scheme-**2**: positive reference pulse (V_P^{ref}) followed by negative write pulses (V_N^w). Blue-red gradient line parents read-out sweeping voltage.

Various pulse schemes have been explored and are represented in Fig. 8.7. In Pulse Scheme-**1**, a positive crescent write pulse (V_P^w), shown in blue, ranges from +2 V to +5 V and is followed by a negative reference pulse (V_N^{ref}) in green at -6 V. Conversely, in Pulse Scheme-**2**, a negative crescent write pulse (V_N^w), presented in red, varies from -2 V to -5 V and is followed by a positive reference pulse (V_P^{ref}) at +6 V. The read-out voltage is applied in the range of ± 2 V after each set of reference and the write pulse, presented through the blue-red gradient line in both pulse schemes.

Now I will discuss how these pulse schemes can be strategically employed to control the

ferroelectric multi-domain behavior. The pulse schemes first apply a reference pulse V_{PorN}^{ref} to the top gate to initialize the ferroelectric polarization state in $CuInP_2S_6$. The reference pulse is designed to exceed the coercive field of $CuInP_2S_6$, ensuring complete polarization of CIPS in a single direction. This initialization allows each trace to start from the same state, facilitating meaningful comparisons. When positive (resp. negative) exceeds, the coercive voltage amplitude polarizes the CIPS downward (resp. upward), increasing electron (resp. hole) concentration in WSe_2.

Next, a write pulse V_{PorN}^{w} of opposite polarity is applied to encode a new remanent ferroelectric state within the CIPS, switching a sub-population of ferroelectric domains in the opposite upward (resp. downward) direction. Compared to the reference state, the write pulse modulates the remanent doping state read at zero gate voltage, shifting it towards a more hole-doped (resp. electron-doped) state. Finally, a transconductance measurement is performed within a restricted gate voltage range to probe the selected carrier polarity (p- or n-branch) while keeping the sweeping gate voltage V_{GS} below the coercive fields.

Modulation of Transconductance Characteristics

Fig. 8.8(a) and Fig. 8.8(b) show the modulation of the transconductance characteristics for the p- and n-branches, respectively, upon applying Pulse Scheme-1. When a subsequent positive write pulse V_P^W is applied, the CIPS domains partially polarize downward, inducing hole doping in the WSe_2 channel. Transconductance measurement is then performed while sweeping the top gate within the range of ± 2 V to remain inside the memory window and below the range of the write pulses. This ensures that only static gating effects occur without influencing the ferroelectric domains.

Comparing the different transfer curves reveals that increasing the amplitude of V_P^W enhances the initial electron doping, as evidenced by a decrease in p-branch current and an increase in n-branch current. This modulation effectively controls the threshold voltage, resulting in an increase in threshold voltage for the n-branch and a decrease for the p-branch. This behavior confirms that ferroelectric domains can be partially switched and that their effects on channel doping can be fine-tuned by varying the pulse amplitude.

Fig. 8.8(c) and Fig. 8.8(d) illustrate the modulation of the p- and n-branches, respectively, of the transfer curves for Pulse Scheme 2. Here, increasing the amplitude of V_N^W enhances the initial hole doping, leading to an increase in p-branch current and a decrease in n-branch current.

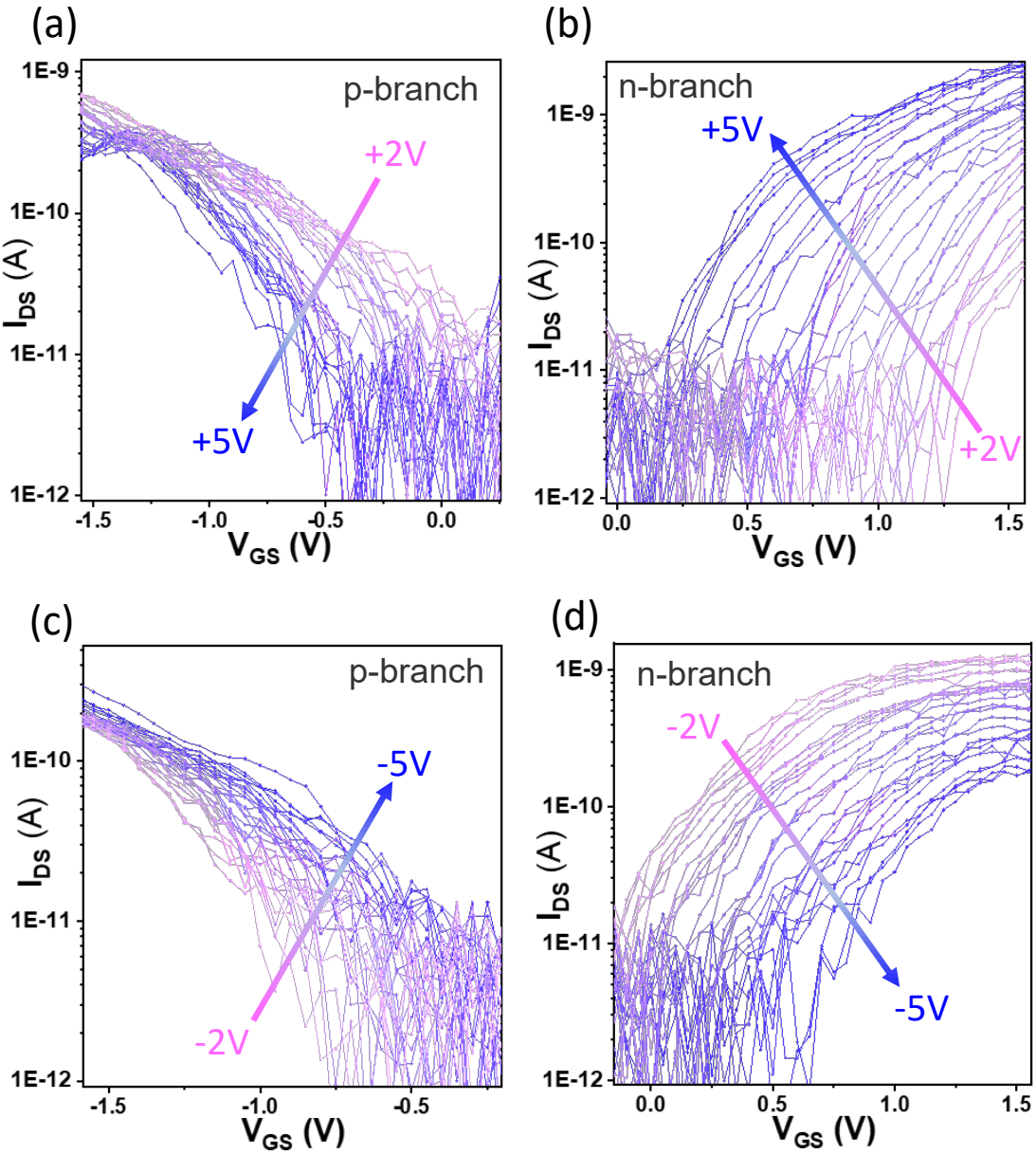


Figure 8.8: Transport measurement study of controlled threshold voltage shift in ambipolar FeFET. (a)-(b) Transfer curve shifts of the p- and n-branches under Pulse Scheme-**1**, followed by continuous sweeping of the V_{GS} read voltage within the range ± 2 V. Data are centered on the respective p- or n-type branches. (c)-(d) Transfer curve shifts of the p- and n-branches under Pulse Scheme-**2**, also followed by continuous V_{GS} sweeping within the range ± 2 V, with data centered accordingly.

Fig. 8.9(a) and (b) details the fine-tuning of the threshold voltage (V_{Th}) as a function of the write gate voltage pulses (either $V_{\mathrm{P}}^{\mathrm{w}}$ or V_N^w), extracted from the systematic measurements of

Fig. 8.8(a)-(e). For simplicity, the threshold voltage was defined as the onset voltage value beyond which the channel passes and $I_{DS} > 10$ pA. The results reveal a linear relationship, indicative of multilevel encoding. The same qualitative trends are observed for the p-branch and for the n-branch under positive or negative write voltage pulses, with opposite shifting directions. This gradual modulation of V_{Th} arises from the partial polarization switching in the ferroelectric CIPS, which is attributed to its multidomain structure as revealed by the PFM analysis (Fig. 8.6). The progressive switching of the ferroelectric domains results in a continuum of intermediate V_{Th} states. This underlines the flexibility in controlling domain switching, offering a pathway for multilevel memory and logic applications. We now explore further the possibilities offered by this functionality for in-memory computing while implementing analog weights in artificial synapses [98, 140, 141].

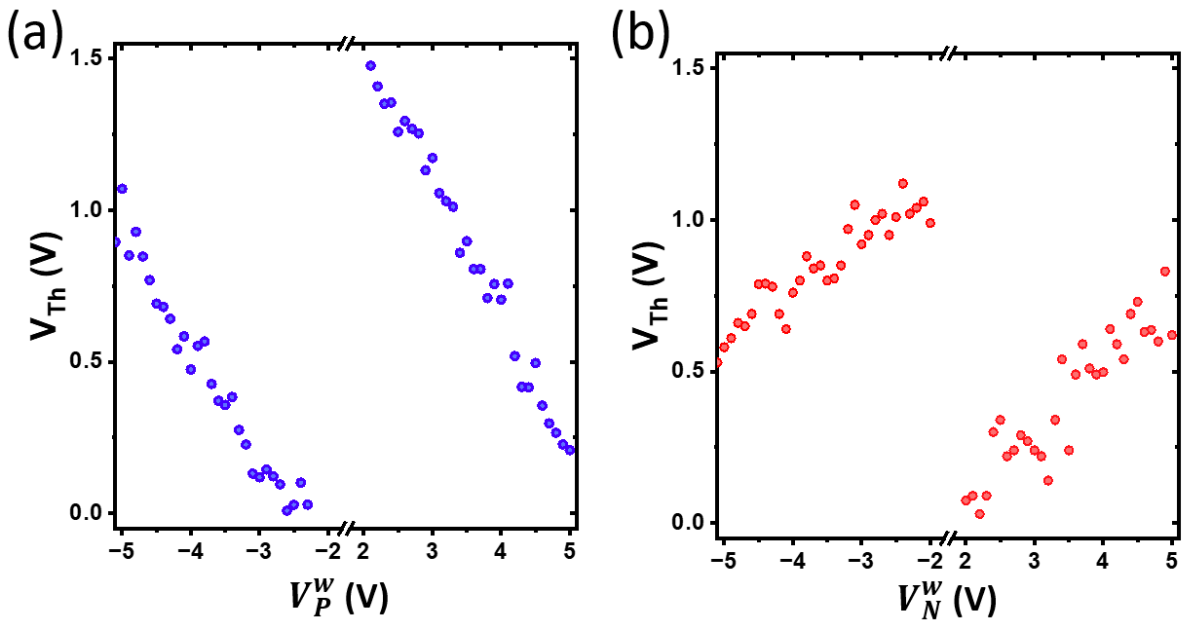


Figure 8.9: Threshold voltage (V_{Th}) as a function of (a) V_P^w for the n-branch and (b) V_N^w for p-branch, illustrating the impact of write gate voltage pulses on the threshold voltage modulation.

8.5. Synaptic Functionality and Performance

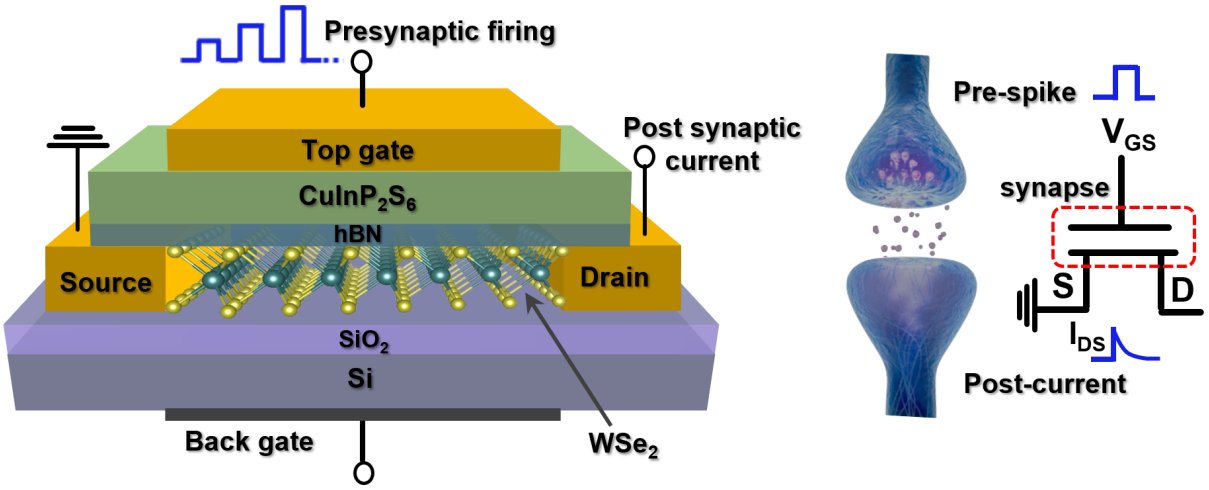


Figure 8.10: Illustration of FeFET as a synaptic device mimicking a biological synapse

The functionality of an artificial synapse in neuromorphic computing [142] is modeled after the ability of biological synapses to adjust the strength of signals transmitted between neurons [97, 143, 144]. Synaptic plasticity, in particular, represents the capacity to maintain stable, long-term potentiation (LTP) and depression (LTD) states in response to external stimuli. This functionality allows the synapse to be tuned across multiple conductance levels, mimicking learning processes in artificial neural networks (ANNs).

Investigating the ferroelectric domain switching kinetics [145, 146] previously suggested that the device can support such multi-level switching. On this note, we now investigate the use of the FeFET device as an artificial synapse in neuromorphic applications. For this, we first characterize the non-volatile modulation of resistance–a.k.a. synaptic plasticity [147] by applying voltage pulses to the control gate. To perform ideally, the resistivity (weight) [148] incrementation of the device (synapse) should be linear for more straightforward and faster optimization (learning). This requires the fine design of the potentiation/depression pulse schemes while considering the specificity of the ferroelectric domain dynamics and its resistive transduction set by the FeFET input characteristics.

8.5.1. LTP/LTD Charecteristics

For this, we compared the LTP/LTD characteristics obtained for optimized crescent pulses (inset of Fig. 8.11(a,b)). With this pulse method, we use voltage pulses of gradually increasing amplitude of positive polarity ($+2$ V to $+6$ V with a 0.05 V step) and negative polarity (-0.01 V

to -0.8 V with a 0.01 V step), as shown in Fig. 8.11(a). This last scheme demonstrates better linearity and a larger dynamic range of resistance states, enabling finer control for representing various synaptic weights, i.e., better synaptic plasticity.

In addition, these states demonstrate remanent properties presented in Ch. 7, confirming the suitability of the device for neuromorphic computing. Moreover, synaptic plasticity can be switched from exhibitory to inhibitory mode depending on the charge type selected to operate the device. When the n-branch is selected, the synapse demonstrates exhibitory plasticity, with potentiation/depression characteristics upon applying positive/negative gate excitations (Fig. 8.11(a)). On the contrary, when the device is operated in the p-type doping mode, it can emulate the elusive complementary inhibitory mode, demonstrating opposite depression/potentiation plasticity (Fig. 8.11(b)), where we used the crescent-pulse method, with voltage pulses of gradually increasing amplitude of positive polarity ($+0.01$ V to $+0.6$ V with a 0.01 V step) and negative polarity (-2 V to -5 V with a 0.05 V step).

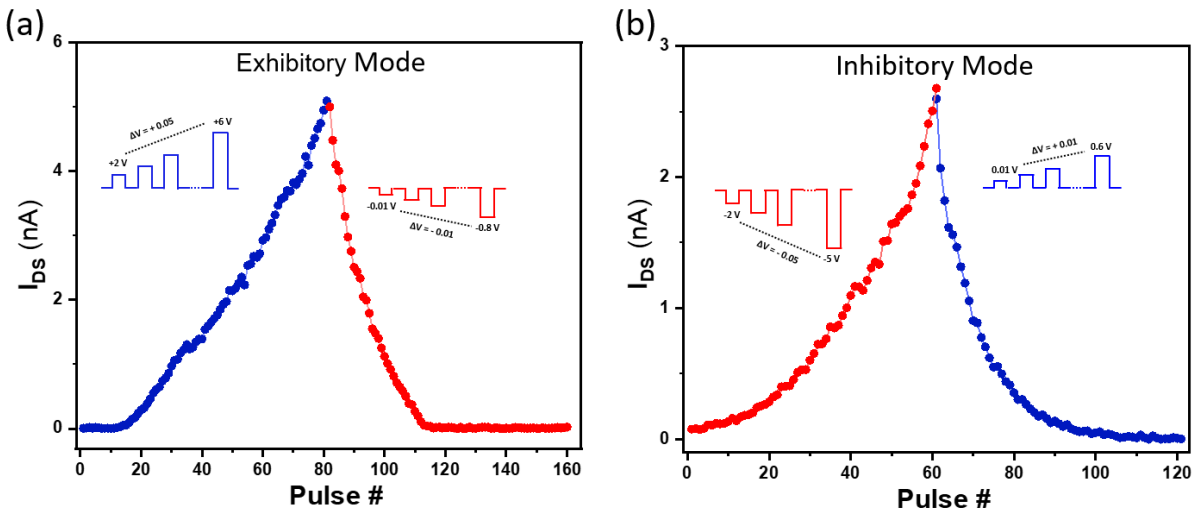


Figure 8.11: Reconfigurable synaptic characteristics. (a-b) Long-term potentiation (LTP) and long-term depression (LTD) responses achieved with the crescent-pulse approach, demonstrating gradual conductance tuning through variable pulse amplitudes. The ferroelectric synapse can be operated either as an exhibitory synapse (a) or inhibitory synapse (b) depending on the branch type and charge carrier selected.

8.5.2. Nonlinearity and Asymmetry

To assess the effectiveness of artificial synapses in neuromorphic computing, two critical performance metrics were considered: nonlinearity (NL) and asymmetry. These properties are crucial for understanding how well these devices function within artificial neural networks (ANNs), influencing learning dynamics and computational efficiency.

Nonlinearity in weight updates represents deviations from an ideal linear relationship between the number of applied pulses and the resulting change in conductance. In practical synaptic devices, conductance changes sharply at first and then gradually saturates as pulses continue to be applied. This behavior can be mathematically modeled as follows:

For long-term potentiation (LTP):

$$G_{LTP} = B \times \left(1 - e^{-P/A_P}\right) + G_{min} \tag{8.1}$$

For long-term depression (LTD):

$$G_{LTD} = -B \times \left(1 - e^{(P-P_{max})/A_D}\right) + G_{max} \tag{8.2}$$

where B is given by:

$$B = \frac{G_{max} - G_{min}}{1 - e^{-P_{max}/A_{P,D}}} \tag{8.3}$$

In these equations, P denotes the number of applied pulses, A determines the extent of nonlinearity in weight adaptation, and B normalizes the conductance range. G_{max} and G_{min} represent the upper and lower conductance limits of the device.

The nonlinearity coefficient A was determined using MATLAB-based computational fitting [149], enabling a precise evaluation of NL across different weight update conditions. The extracted A values were used to calculate nonlinearity. The corresponding nonlinearity index (NL) was computed using the empirical relation:

$$\Phi_{P,D} = 1.726 \times A_{P,D} + 0.162 \tag{8.4}$$

Asymmetry in weight updates can also significantly affect synaptic device performance, impacting the learning efficiency of neuromorphic systems. Asymmetry arises when the rate of conductance increase during LTP differs from the rate of decrease during LTD. This imbalance can introduce biases in network training and degrade overall learning accuracy. Optimizing pulse parameters and device characteristics is crucial for mitigating asymmetry and enhancing stability in neuromorphic processing.

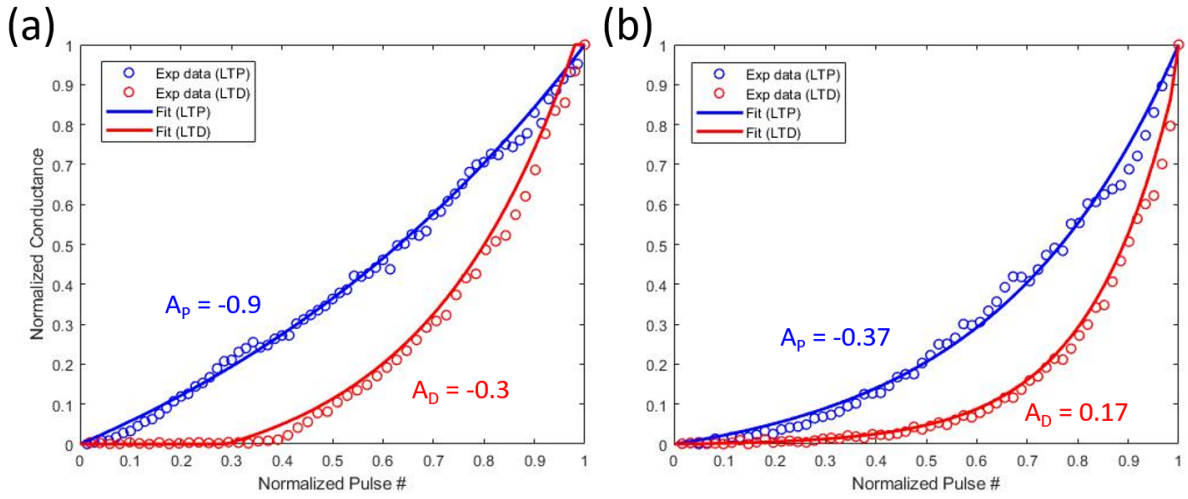


Figure 8.12: Nonlinearity characteristics from LTP/LTD curves in FeFET. (a) Exhibitory mode. (b) Inhibitory mode.

Fig. 8.12 presents fitted LTP and LTD curves for the exhibitory (a) and inhibitory (b) modes, respectively. The extracted A values offer insights into the nonlinearity and corresponding NL values for each mode.

In Fig. 8.12(a), the extracted normalized A values for LTP and LTD are A_P = -0.9 and A_D = -0.3, corresponding to NL values of -1.37 and -3.68. The number of conductance points considered for LTP and LTD are 70 and 60, respectively, indicating some level of asymmetry in weight updates.

Similarly, in Fig. 8.12(b), the extracted values are A_P = -0.37 and A_D = 0.17, resulting in NL values of -3.11 and -5.36. Here, the number of conductance levels is 61 for both LTD and LTP, showing a more symmetric behavior in terms of conductance increase and decrease rates.

8.5.3. Artificial Neural Network (ANN) Performance

To benchmark the short-channel vdW FeFET as an artificial synapse and assess its impact on neuromorphic computing, we simulated its performance in an artificial neural network (ANN) designed for handwritten digit recognition. Figure 8.13(a) illustrates the structure of our ANN model [149], which consists of three layers: an input layer with 400 neurons (representing a 20 $\times$ 20 pixel grayscale image), a hidden layer of 100 neurons, and an output layer with 10 neurons corresponding to digits 0–9. During training, each input passes through weighted connections to the hidden and output layers, emulating synaptic processing in biological neurons.

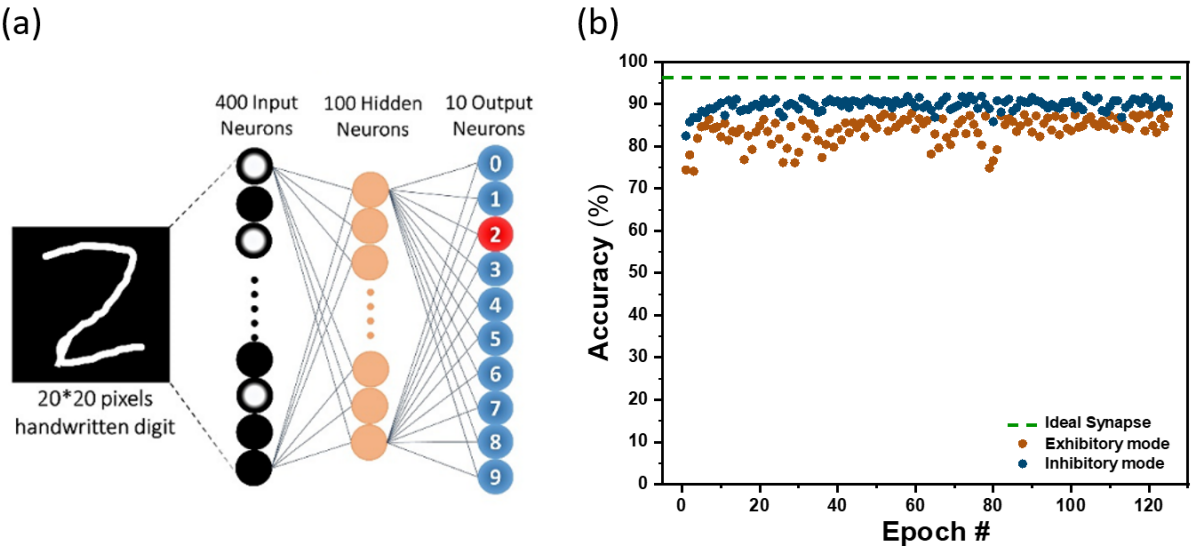


Figure 8.13: (a) Architecture of the artificial neural network (ANN) used for handwritten digit classification, featuring 400 input neurons (for 20 × 20 pixel images), 100 hidden neurons, and 10 output neurons representing digits from 0 to 9. (b) Recognition accuracy comparison for the ANN trained with FeFET-based synaptic weights using crescent-pulse stimulation methods operating in exhibitory (blue) and inhibitory (orange) modes. The ideal synapse accuracy (green) is shown as a reference.

Figure 8.13(b) presents the accuracy trends of the ANN based on the measured LTP/LTD characteristics. The optimized FeFET-based synapse operated in the exhibitory mode using the crescent pulse method achieves an accuracy of approximately 85% after 125 training cycles (epochs), while an accuracy of 75% is obtained using the constant pulse method (see appendix). The significant improvement observed with the crescent-pulse method highlights the importance of precisely controlling domain dynamics and their transduction via the semiconductor channel for optimal synaptic performance.

When the FeFET synapse operates in inhibitory mode, accuracy reaches 92%, attributed to the improved symmetry of LTD and LTP in this mode. For comparison, ideal synapses in the constructed 3-layer ANN achieve a recognition accuracy of approximately 96%. Further theoretical modeling of ferroelectric switching mechanisms in CIPS and FeFET transduction could provide insights for further improving accuracy in next-generation short-channel devices.

8.6. Synaptic Characterization Using a Constant-Pulse Scheme

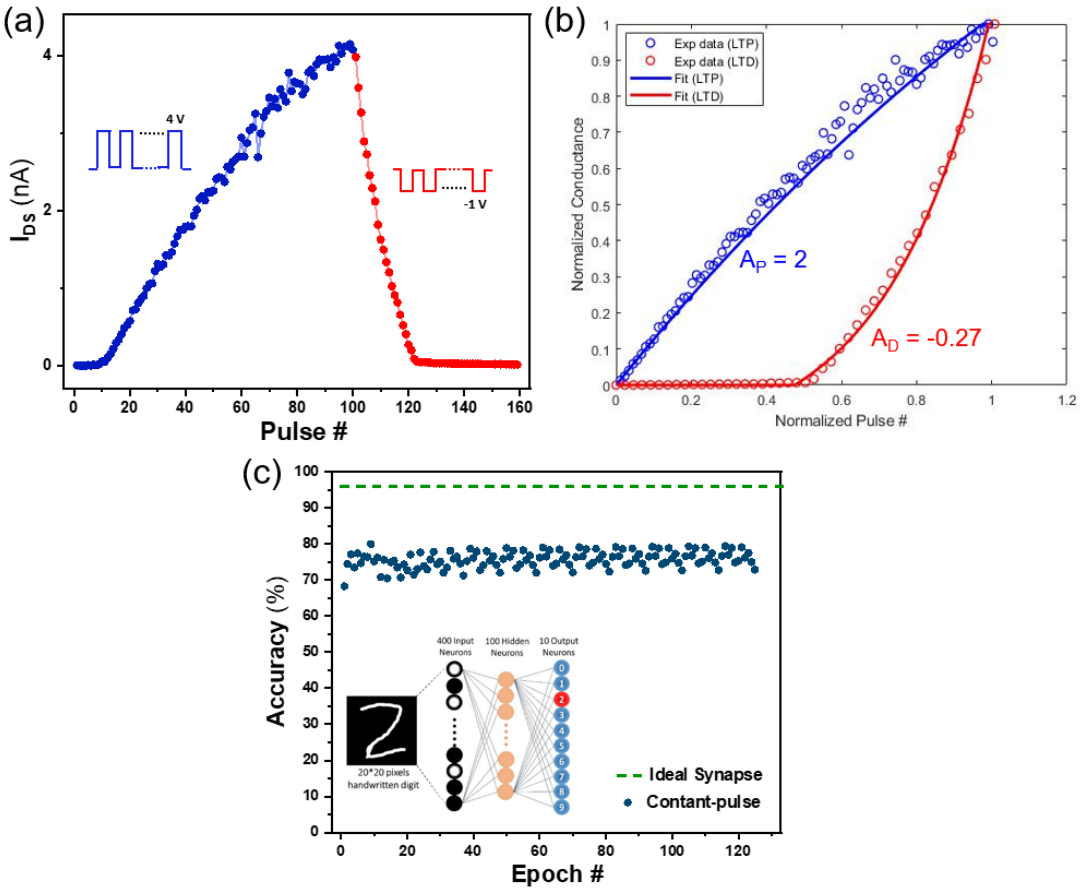


Figure 8.14: (a) Long-Term Potentiation (LTP) and Long-Term Depression (LTD) responses obtained using the constant-pulse approach, demonstrating conductance modulation through pulses of fixed amplitude. (b) Nonlinearity characteristics derived from LTP/LTD curves. (c) Recognition accuracy of an artificial neural network (ANN) (inset) trained with FeFET-based synaptic weights using the constant-pulse scheme (blue), compared to the ideal synapse accuracy (green, for reference).

We investigated the synaptic functionality of our FeFET-based device under a constant-pulse scheme. Figure 8.14(a) illustrates the LTP and LTD behavior of the device, where potentiation is induced using a +4 V pulse and depression using a -1 V pulse. The extracted nonlinearity coefficients for LTP and LTD are A_P = 2 and A_D = -0.27, corresponding to NL values of 6.26 and -3.99, respectively. The number of conductance states used for LTP and LTD are 100 and 50, indicating a higher asymmetry in weight updates compared to the crescent-pulse

scheme.

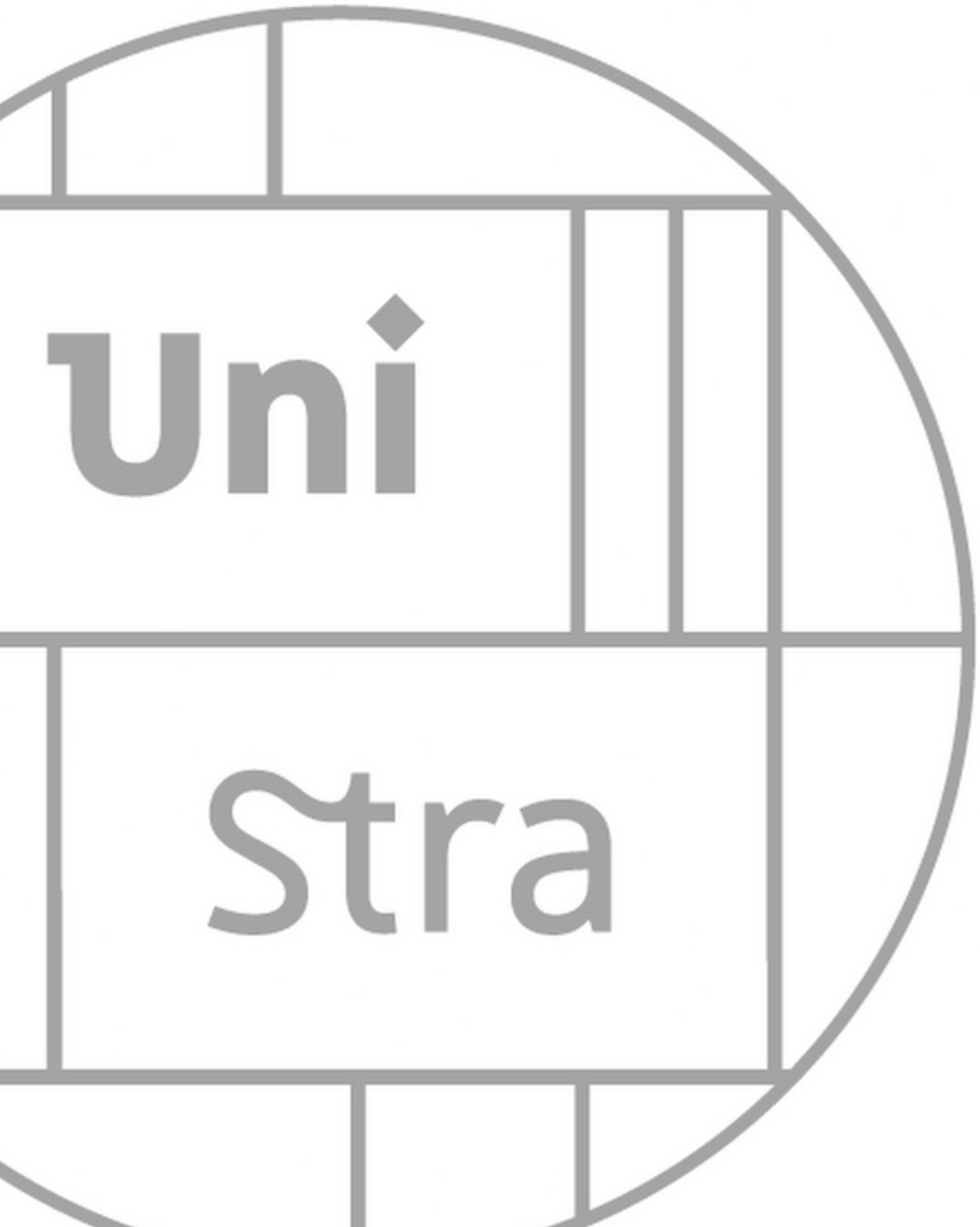
Figure 8.14(c) shows recognition accuracy of ANN, trained with FeFET-based synaptic weights using the constant-pulse scheme. The accuracy achieved is 75%, lower than the cresent pulse method, primarily due to increased asymmetry in the weight update process. Similar synaptic characterization can be conducted for the p-type behavior of the device, where negative pulses induce potentiation and positive pulses induce depression. With the constant-pulse scheme as well, the device can be tuned to operate in both excitatory and inhibitory modes, broadening its applicability.

Theoretical modeling using the Preisach model [150] [96] further supports these findings, indicating that an incremental amplitude approach, as used in the crescent-pulse method, enhances LTP/LTD performance and overall synaptic behavior in neuromorphic circuits. Further exploration of ferroelectric switching mechanisms in CIPS and FeFET transduction could offer additional insights to optimize synaptic performance and enhance accuracy in next-generation devices [151].

8.7. Conclusion

- We conducted transport measurements on a 2D ferroelectric field-effect transistor (2D-FeFET) using the van der Waals ferroelectric material $CuInP_2S_6$ and the ambipolar semiconductor WSe_2. By combining electronic transport analysis with piezoresponse force microscopy (PFM) characterization, we examined how fine-tuning $CuInP_2S_6$ multidomain polarization landscapes influences WSe_2 channel conductance.
- The study showed that the 2D-FeFET provides precise control over charge transport in both n-type and p-type modes, making it highly reconfigurable. By applying tailored voltage pulse schemes, we achieved continuous and reversible threshold voltage tuning, with resistance modulation exceeding two orders of magnitude, which is essential for neuromorphic applications.
- The conductance plasticity of the device qualifies it as a memristive device, allowing it to function as a reconfigurable artificial synapse. Depending on whether the device operates in an n-doped or p-doped regime, it can mimic either excitatory or inhibitory synaptic behavior, expanding its potential for neuromorphic computing.
- The LTP/LTD characteristics exhibited improved linearity and dynamic range, while nonlinearity and asymmetry analysis ensured balanced potentiation and depression, further enhancing the suitability of the device for neuromorphic applications.

- Artificial Neural Network (ANN) simulations confirmed the device's potential as an artificial synapse, up to 92% accuracy for handwritten digit recognition, approaching the ideal synapse performance of 96%.
- These studies were performed on sub-100 nm channel devices, demonstrating the feasibility of high-density neuromorphic circuits based on 2D-FeFET technology.
- Our findings highlight the potential of van der Waals ferroelectrics in next-generation neuromorphic architectures and encourage further research into switching dynamics and hardware integration for advanced brain-inspired computing technologies.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9 | Logic Functionality and Circuit Design of α-In_2Se_3-Based Ferroelectric Field Effect Transistor

This chapter presents the novel ferroelectric properties of semiconductor α-In_2Se_3, and its potential for reconfigurable electronics. To achieve this, I integrated an α-In_2Se_3 channel into a split-gate field-effect transistor (FET) architecture, using an hBN crystal as a van der Waals dielectric spacer. This setup provides two independent gate terminals, allowing precise tuning of the ferroelectric states and conducting properties in different regions of the channel.

I first investigated the transport characteristics of the device and observed hysteresis in both the output (I_{DS}-V_{DS}) and transfer (I_{DS}-V_{GS}) characteristics. This hysteresis serves as a clear indicator of both in-plane and out-of-plane polarization in α-In_2Se_3, confirming its intrinsic ferroelectric nature [152, 153].

The dual-gate design allows independent polarization control, enabling the creation of volatile NAND logic gates. Moreover, by combining ferroelectric properties with this dual-gate setup, a single FeS-FET can function as both Fe-NAND and Fe-NOR logic gates. The device also features tunable threshold voltage and multilevel conductance. Circuit simulations further validate these findings, showing that FeS-FETs can implement all fundamental logic gates when two devices are connected in parallel. These results position the FeS-FET as a strong candidate for future computing systems, particularly in energy-efficient logic and in-memory computing [154].

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9.1. Device Architecture

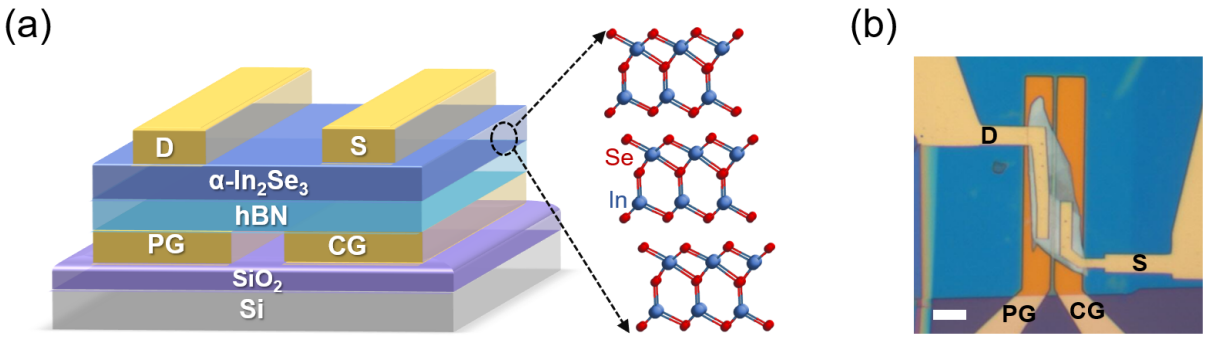


Figure 9.1: (a) Schematic of ferroelectric semiconductor field effect transistor (FeS-FET). (b) Optical microscope image of the fabricated device (scale bar 5 µm).

Fig. 9.1(a) shows a schematic of FeS-FET fabricated with hBN/α-In_2Se_3 heterostructure, where the hBN layer acts as a dielectric layer, while the α-In_2Se_3 serves as a semiconducting channel. The device consists of a Ti (5 nm) / Au (45 nm) split-gate, with a 1 µm spacing, precisely patterned through e-beam lithography. The fabrication process begins with the mechanical exfoliation of hBN and α-In_2Se_3 from bulk crystals using a conventional scotch tape technique. These flakes were transferred onto a pre-patterned metallic split-gate structure on a Si/SiO_2 substrate. Furthermore, source-drain electrodes composed of Ti (10 nm)/Au (60 nm) are deposited, defining a channel length of 3 µm and a channel width of 8 µm. The corresponding optical image is shown in Fig. 9.1(b).

9.2. Characterization:

9.2.1. Atomic Force Microscopy (AFM) Characterization

Atomic force microscopy (AFM) was used to assess the layer thickness and structural uniformity of the van der Waals heterostructures in the FeS-FET. The AFM profiles presented in Fig.s 9.2(a) and 9.2(c) confirm that both the hBN dielectric layer and the α-In_2Se_3 semiconductor exhibit a consistent thickness of approximately 25 nm. The observed step heights indicate uniform material deposition, while the smooth surface morphology highlights high-quality stacking with minimal surface roughness. Additionally, the insets in Fig.s 9.2(a) and 9.2(c) provide AFM scans of the specific areas indicated in the optical image (Fig. 9.2(b)).

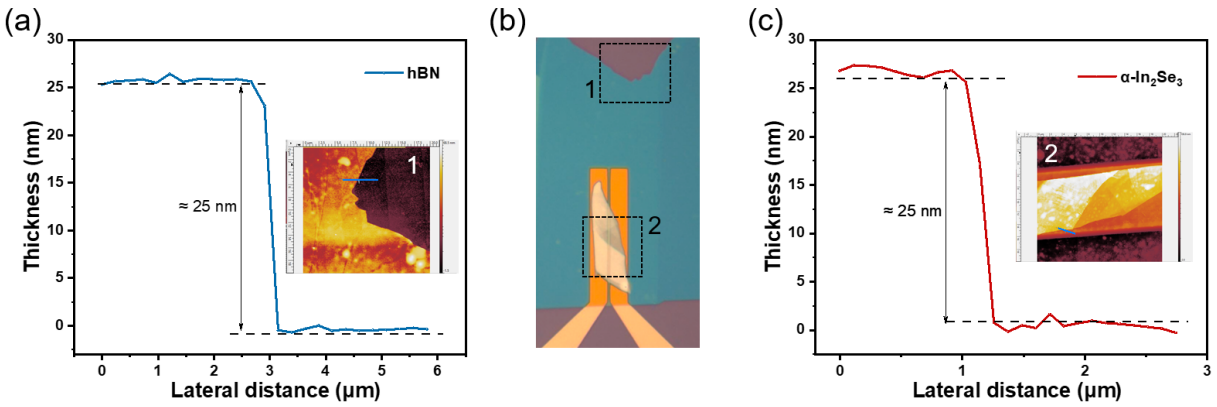


Figure 9.2: (a) Thickness profile of hBN. (b) Optical microscope image of the device. (c) Thickness profile of α-In_2Se_3.

9.2.2. Piezoresponse Force Microscopy (PFM)

(This PFM study was carried in collaboration with postdoc Shehr Bano, under the supervision of Alexei Gruverman at the University of Nebraska-Lincoln.)

The ferroelectric properties of α-In_2Se_3 were characterized on different devices using PFM. Fig. 9.3(a) presents the VPFM scan of the FeS-FET device, with the corresponding optical image shown in Fig. 9.3(b). The switching spectroscopy measurements in Fig. 9.3(c) exhibit a clear polarization switching response, as seen in the phase (top) and amplitude (bottom) curves.

To investigate the local ferroelectric switching [71, 75], a specific region of the device was selected, as marked in Fig. 9.3(d). The PFM scans before and after the application of local switching voltages (8 V and 8.5 V) are displayed in Fig. 9.3(e). Over time, the ferroelectric domain switching becomes more pronounced, as indicated by the dark contrast in the phase and amplitude images. Notably, the topography images remain unchanged, confirming that the observed contrast in the amplitude and phase signals originates from ferroelectric switching rather than morphological changes. These results highlight the robust ferroelectric behavior of α-In_2Se_3.

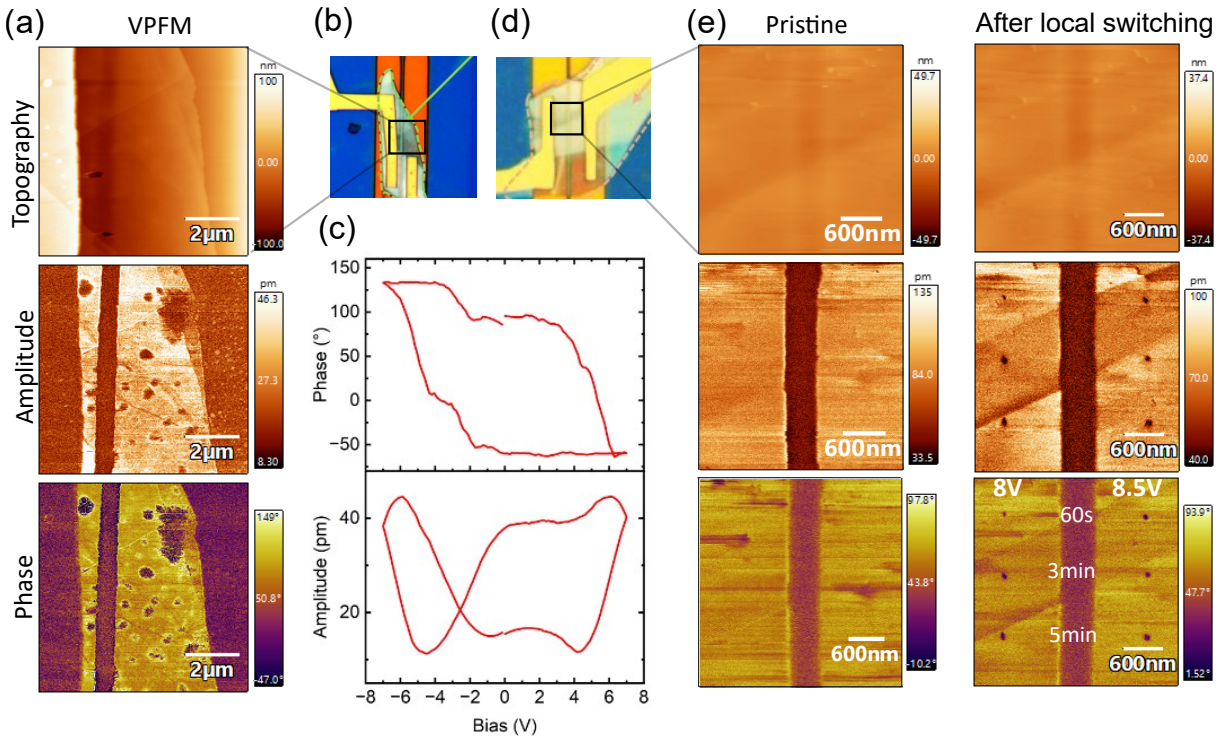


Figure 9.3: (a) Vertical Piezoresponse Force Microscopy (VPFM) analysis of the FeS-FET device. (b) Corresponding optical image of the device, highlighting the region selected for VPFM measurements. (c) Switching spectroscopy measurements displaying phase (top) and amplitude (bottom) responses as a function of applied bias voltage. (d) Optical image of the device with the marked region used for PFM analysis fresented in (e). (e) Local switching charecterization, showing the pristine state (top row) and the evolution of local polarization switching after applying 8 V and 8.5 V biases for different time durations (60 s, 3 min, and 5 min). For all PFM images, the top row represents topography, the middle row corresponds to phase, and the bottom row shows amplitude signals.

9.2.3. Raman Characterization

[Raman analysis was performed in collaboration with PhD student Aymen Mahmoudi under the supervision of Abdelkarim Ouerghi at Université Paris-Saclay, CNRS, Centre de Nanosciences et de Nanotechnologies.]

The phase and crystal quality of the α-In_2Se_3 flakes used in the device channel were analyzed using room-temperature Raman spectroscopy [155] with a 532 nm laser excitation. As shown in Fig. 9.4, the Raman spectrum of α-In_2Se_3 displays distinct peaks at approximately 25, 89, 104, 180, 186, and 194 cm^{-1}, corresponding to the E^1, E^2, A_1^1(LO+TO), E^4, A_1^2(TO), and A_1^3(LO) phonon modes, respectively.

To further characterize the polymorphic nature of α-In_2Se_3, we compared our results with previously reported data by M. Rahimi et al.(2024) [156]. The intensity ratio of the E^2 ($\sim$ 89 cm^{-1}) and A_1^1 modes serves as a key marker for distinguishing between the 3R and 2H polymorphs. Specifically, the E^2 mode is more pronounced in the 2H phase, resulting in a higher E^2/A_1^1 intensity ratio, whereas the opposite trend is observed for the E^1 mode ($\sim$ 25 cm^{-1}). Our findings are consistent with the Raman data reported by Rahimi et al., confirming that the α-In_2Se_3 flakes in this work have the 2H phase.

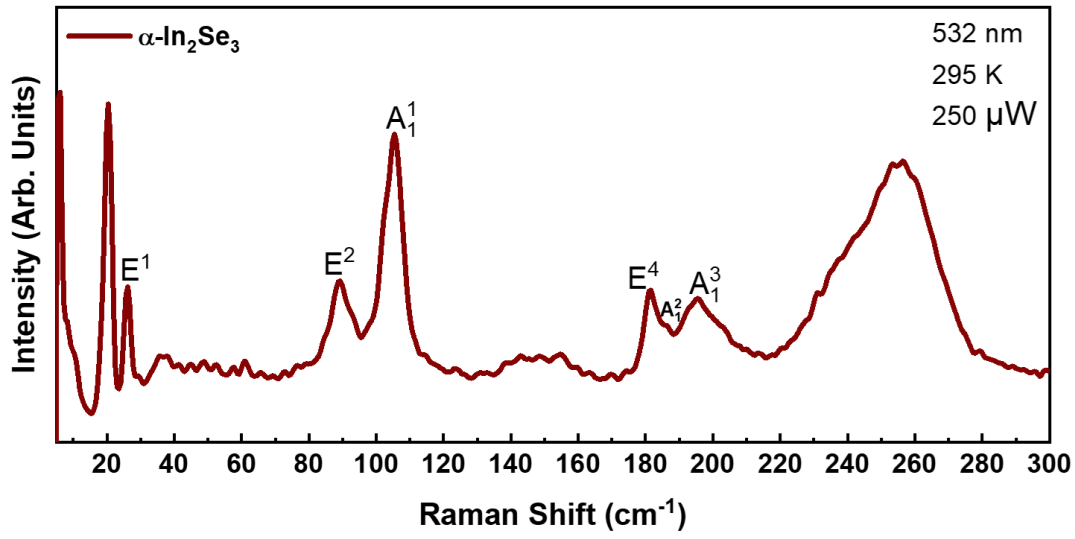


Figure 9.4: Micro-Raman spectrum of α-In_2Se_3 flake taken from the FeS-FET device.

9.3. Electrical Characterisation

Charge Modulation in α-In_2Se_3 Channel via Split-gate

In a ferroelectric semiconductor field-effect transistor (FeS-FET), the ferroelectric semiconductor α-In_2Se_3 itself forms the channel, resulting in the accumulation of both polarization-bound charges and mobile carriers. The split-gate architecture enables independent control of charge accumulation in the channel via the programming gate (PG) and control gate (CG).

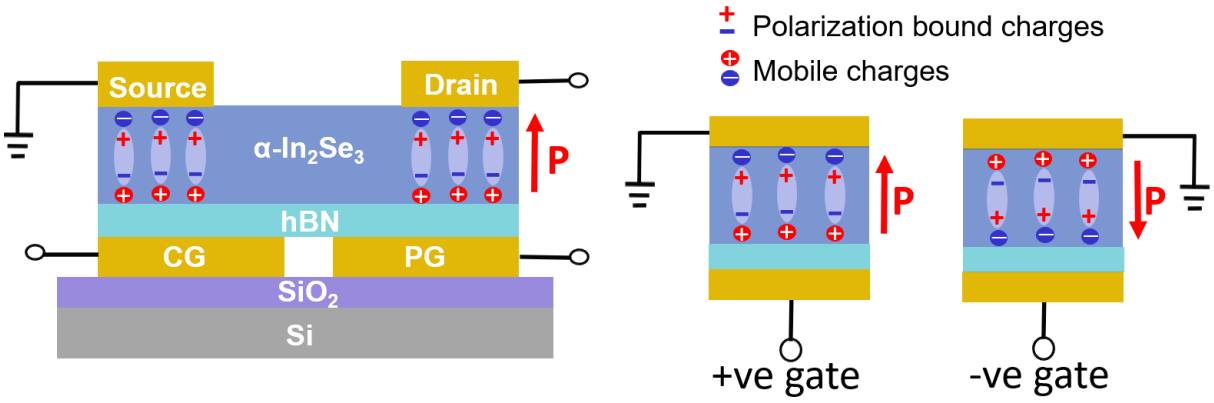


Figure 9.5: Schematic of the FeS-FET, illustrating polarization-bound and mobile charges in the ferroelectric semiconducting channel and charge modulation via the split-gate architecture.

When a positive gate voltage is applied, the ferroelectric polarization aligns upward (P↑), leading to the accumulation of positive bound charges at the top surface (TS) and negative bound charges at the bottom surface (BS). This charge configuration induces electron accumulation at the TS, whereas electrons are depleted at the BS. In contrast, when a negative gate voltage is applied, the ferroelectric polarization reverses downward (P↓). In this case, negative bound charges accumulate at the TS, whereas positive bound charges at the BS. This charge distribution leads to electron depletion at the TS and increased electron accumulation at the BS as shown in Fig. 9.5

9.3.1. Transistor Characteristics and Working Mechanism

Fig. 9.6 presents a comprehensive analysis of the ferroelectric behavior and electrical characteristics of the α-In_2Se_3-based FeS-FET, highlighting both out-of-plane and in-plane polarization mechanisms. Fig. 9.6 shows the transfer characteristics of the split-gate FeS-FET at $V_{DS} = -1\ V$ when both gates are connected and swept in a closed-loop ranging from -10 V to +10 V. The device exhibits a well-defined transconductance hysteresis, with an ON/OFF ratio spanning four decades and a memory window of 12 V. Interestingly, the hysteresis follows a clockwise direction, which has been observed previously in single-gate FeS-FETs made from α-In_2Se_3 or sliding ferroelectric semiconductors [157, 158]. This characteristic may indicate that our device operates in the high Equivalent Oxide Thickness (EOT) regime, where the EOT of the gate dielectric is high enough that the applied electric field lacks the necessary strength to penetrate the entire flake uniformly. Instead, it is concentrated in the vicinity of the gate stack, i.e., in the bottom layers of the α-In_2Se_3 film. Consequently, it is anticipated

that only partial ferroelectric switching will occur during the sweep of the gate voltage, mostly localized in the bottom layers rather than on the top surface.

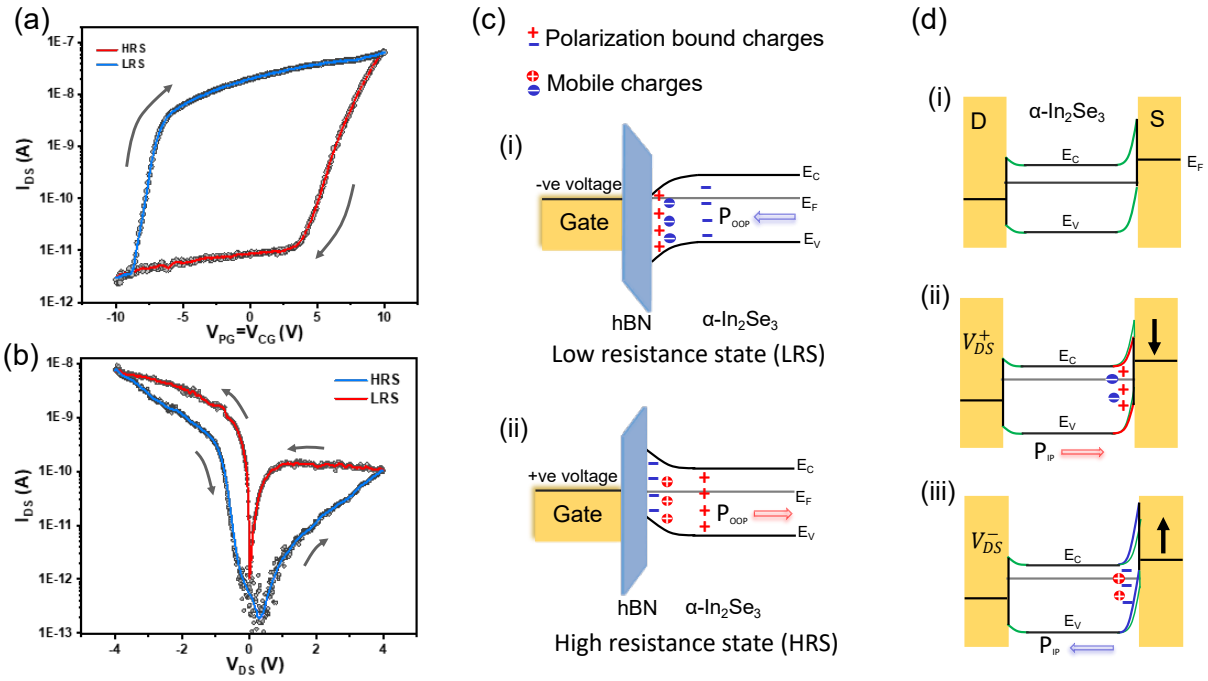


Figure 9.6: (a) Transfer characteristic of the FeS-FET at $V_{DS} = -1V$ when both gates are connected and swept together, exhibiting clockwise hysteresis. (b) I_{DS}-V_{DS} characteristic of the device when $V_{PG} = V_{CG} = 3V$, showing in-plane polarization switching. (c) Band diagrams under negative and positive gate voltages explaining the clockwise hysteresis as a result of partial polarization switching in the high EOT regime. (d) Band diagram depicting the in-plane switching mechanism and its impact on the Schottky barrier, leading to distinct high- and low-resistance states.

In previous discussions (Sec. 4.3), I detailed the working mechanism of FeS-FETs under both low and high EOT conditions. In this work, the EOT is relatively high due to the presence of approximately 25 nm of hBN and 25 nm of α-In_2Se_3, which aligns well with the characteristics of the high-EOT regime. Under these conditions, only the bottom surface of α-In_2Se_3, in close proximity to the hBN layer, becomes partially polarized. When a negative gate voltage is applied, the polarization of the channel layers aligns downward, causing downward band bending and an increase in mobile charge concentration due to electrostatic induction. This leads to an increase in channel conductance and a shift to the low-resistance state (LRS), as illustrated in Fig. 9.6(c)(i). In contrast, when a positive gate voltage is applied, the polarization direction reverses upward, leading to upward band bending, depletion of mobile carriers, and a reduction in channel conductance, thereby placing the device in the high-resistance state

(HRS), as depicted in Fig. 9.6c(ii). Since the LRS and HRS states correspond to low and high threshold voltages (V_{th}), respectively, the transfer characteristic ultimately gives rise to the clockwise hysteresis loop, as shown in Fig. 9.6a. This observation is consistent with findings reported in the literature [91, 92, 158–162].

To further investigate the in-plane ferroelectric properties of the device motivated by the pioneering work of Xue et al. (2021)[91], we examine the I_{DS}-V_{DS} characteristics at $V_{PG} = V_{CG} = 3V$, as shown in Fig. 9.6b. The transport curve obtained by sweeping the source-drain voltage back and forth within the range of -4V to +4V reveals a clear hysteresis effect with an ON/OFF ratio of 1000, even at small reading voltages. Interestingly, the in-plane hysteresis follows an anticlockwise direction, which can be attributed to voltage-driven in-plane polarization switching in α-In_2Se_3. This switching mechanism enables the device to transition between high- and low-resistance states.

The impact of in-plane polarization on the Schottky barrier at the source and drain contacts is significant [163, 164]. When a drain voltage is applied, polarization-bound charges of opposite polarities accumulate at the terminals, resulting in an in-plane polarization field that modifies the Schottky barrier profile [159]. In a standard metal–semiconductor–metal (MSM) device, two Schottky barriers are typically present at the source and drain contacts. When simplified to a single-barrier model [91, 165], the energy band structure appears as illustrated in Fig. 9.6d(i), where the conduction band bends upward due to the difference between the metal work function and the n-type semiconductor. With the source terminal grounded, the initial band alignment presents a barrier between the metal and the semiconductor due to charge transfer from the semiconductor to the metal.

When a positive drain voltage is applied, positive polarization-bound charges accumulate at the source terminal. The built-in potential counteracts polarization, so negative mobile charges accumulate at the Schottky barrier, effectively reducing the barrier height, as indicated by the arrow in Fig. 9.6d(ii). This reduction in barrier height facilitates charge transport, shifting the device to a low-resistance state (LRS), which corresponds to the red I_{DS}-V_{DS} curve in Fig. 9.6b. Conversely, when a negative drain voltage is applied, negative polarization-bound charges accumulate at the source, leading to the depletion of mobile carriers. This depletion increases the Schottky barrier height, making charge transport more difficult and transitioning the device into the high-resistance state (HRS), as represented by the blue I_{DS}-V_{DS} curve in Fig. 9.6b.

It is important to note that α-In_2Se_3 in this study has been confirmed to exist in the 2H phase, where in-plane polarization is relatively weak compared to other ferroelectric phases, as reported in previous studies [156]. Due to this limitation, our further investigations on memory

and logic operations have primarily focused on out-of-plane polarization, where the FeS-FET exhibits robust ferroelectric switching under dual gate control.

9.3.2. Dual-Gate Control

When operated in the symmetric gate mode, where both gates are connected and swept together, the behavior of our device aligns well with single-gate FeFETs based on α-In_2Se_3, as previously reported in the literature [90, 166]. However, unlike single-gate FeFETs, our dual-gate configuration enables additional control over charge transport, allowing for more precise modulation of the channel conductivity. This distinction results in enhanced tunability and the potential for reconfigurable logic applications. By leveraging the dual-gate control in combination with the ferroelectric semiconductor properties of α-In_2Se_3, we unlock exciting possibilities for multifunctional applications, which I will demonstrate in the following sections.

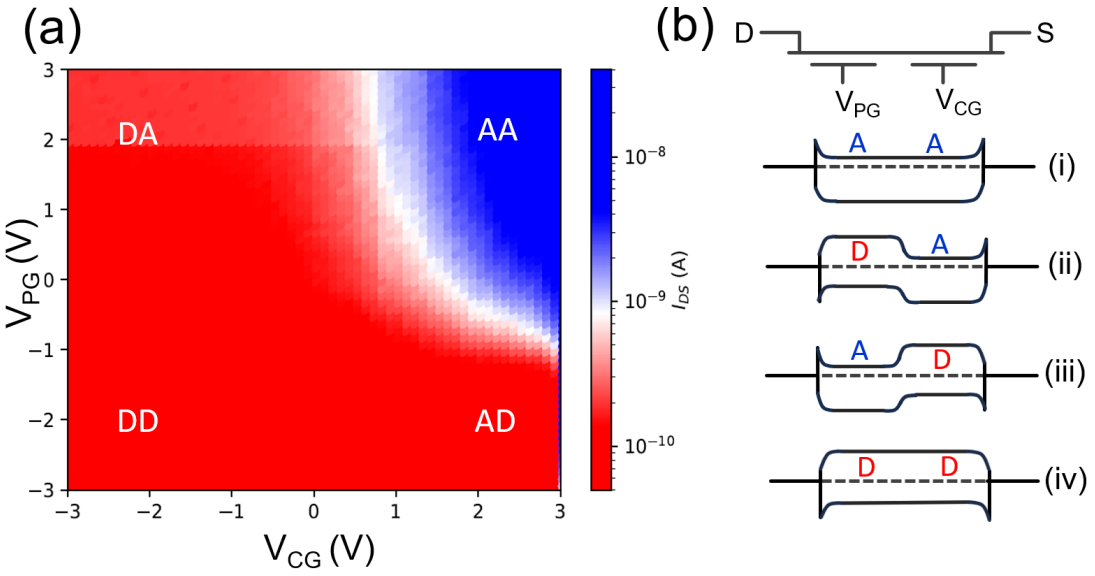


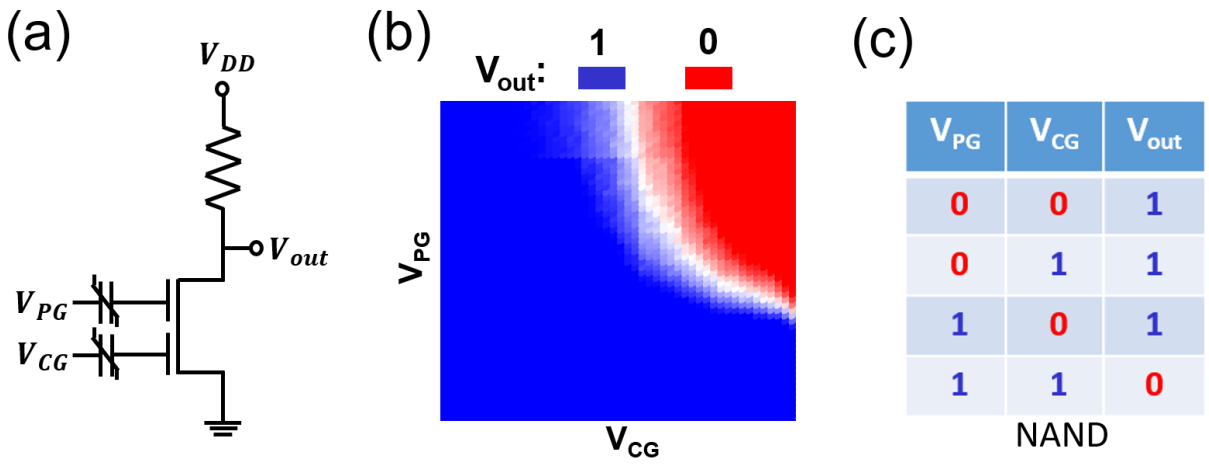
Figure 9.7: (a) Color map of source-drain current (I_{DS}) as a function of program gate (V_{PG}) and control gate (V_{CG}). (b) Energy band structure under different gate voltage conditions.

Fig. 9.7(a) presents a color map depicting the source-drain current (I_{DS}) variation as a function of gate voltages (V_{PG}, V_{CG}). This visualization helps us to understand how different voltage applications influence charge transport. By applying different voltages to each gate, distinct energy band profiles can be imprinted into the channel, significantly impacting carrier dynamics. When both V_{PG} and V_{CG} exceed the threshold voltage (V_{th}), the α-In_2Se_3 channel enters the n-type accumulation regime. The Schottky barriers at the source and drain electrodes are reduced due to an upshift in the electrochemical potential of α-In_2Se_3 towards the Ti level, leading to a highly conductive state [120], as depicted in Fig. 9.7(b)(i).

When one of the gates is biased above the threshold voltage while the other remains below it, carrier transport is blocked due to the depleted side of the homojunction, as shown in Fig. 9.7(b)(ii) and (iii). However, since the Schottky barrier remains small on the accumulated side, residual carrier injection can still occur in the region beyond threshold voltage. When both gate voltages are polarized below the threshold voltage, the channel undergoes complete depletion, increasing the Schottky contact barrier, as shown in Fig. 9.7(b)(iv), and suppressing carrier transport, resulting in an extremely low off-current state. By categorizing the color map into four quadrants, we identify four distinct regimes: AA, AD, DA, and DD, where 'A' represents accumulation ($V_G > V_{th}$) and 'D' signifies depletion ($V_G < V_{th}$). Each quadrant corresponds to a unique combination of these regimes for the two gates.

9.4. Device Functionality

9.4.1. FeS-FET as a Volatile Logic Gate



V_{PG}	V_{CG}	V_{out}
0	0	1
0	1	1
1	0	1
1	1	0

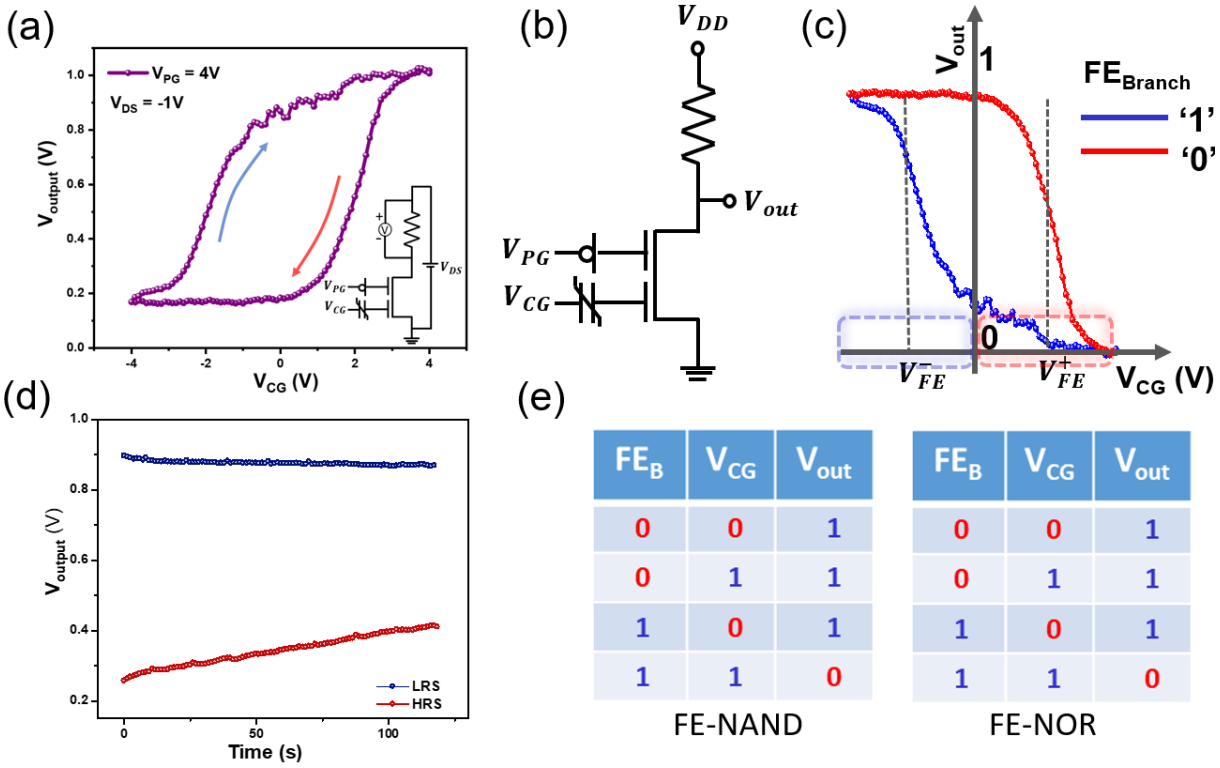
Figure 9.8: (a) Circuit diagram of the FeS-FET-based volatile logic gate. (b) Output voltage across the load demonstrating NAND logic behavior. (c) Truth table for the NAND operation.

Fig. 9.8(a) illustrates the circuit configuration used to demonstrate the functionality of the FeS-FET as a volatile logic gate. When a passive load is connected in series, the device can perform fundamental Boolean logic operations, where V_{PG} and V_{CG} act as input parameters. The output voltage color map in Fig. 9.8(b) demonstrates the device's response when both gates serve as independent input variables, highlighting its potential in logic applications.

This configuration allows the FeS-FET to emulate a volatile NAND logic gate, where the output states are determined by the combined influence of the two gate voltages. Fig. 9.8(c) presents the corresponding truth table, confirming that the device successfully operates in

NAND logic mode.

9.4.2. FeS-FET as a Ferroelectric Logic Gate



FE_B	V_{CG}	V_{out}
0	0	1
0	1	1
1	0	1
1	1	0

FE_B	V_{CG}	V_{out}
0	0	1
0	1	1
1	0	1
1	1	0

Figure 9.9: (a) Voltage drop across a load resistor connected in series with the FeS-FET device while the programming gate voltage (V_{PG}) is fixed at +4V and the control gate voltage (V_{CG}) is swept. The inset shows the corresponding circuit used for this measurement. (b) Circuit diagram of the FeS-FET with a passive load connected in series. (c) Output voltage characteristics illustrating the role of the ferroelectric branch (FE_{Branch}) in determining logic states. The two distinct operational regions, marked by blue and red dotted lines, correspond to Fe-NAND and Fe-NOR functionalities, defined by threshold voltages V_{FE}^{-} and V_{FE}^{+}. (d) Retention properties of the ferroelectric states over time, indicating the stability of logic states. (e) Truth tables for Fe-NAND and Fe-NOR logic operations.

Fig. 9.9 illustrates the functionality of the FeS-FET device as a ferroelectric logic gate. In Fig. 9.9(a), the voltage drop across a load resistor connected in series with the device is shown, where the control gate voltage (V_{CG}) is swept between -4 V and +4 V, while the programming gate voltage (V_{PG}) is fixed at +4 V. The inset schematic provides an overview of the circuit configuration, showing the bias distribution between the ferroelectric transistor and the series-connected load resistor

By leveraging the intrinsic ferroelectric properties of α-In_2Se_3, the FeS-FET device can be employed for logic operations. Fig. 9.9(c) demonstrates how the ferroelectric branch (FE_{Branch}) influences logic states based on the applied control gate voltage V_{CG}. The ferroelectric branch exhibits two distinct resistance states: a high-resistance state (HRS), representing logic $'0'$ and a low-resistance state (LRS), representing logic $'1'$. The transitions between ON and OFF states of the device occurs at threshold voltages V_{FE}^{-} and V_{FE}^{+}. The NAND gate functionality is achieved when the device operates within the region marked by the blue dotted line, where logic $'1'$ is maintained for $V_{FE}^{-} < V_{CG} < 0$ and logic $'0'$ is set for $V_{CG} < V_{FE}^{-}$. In contrast, NOR logic is realized in the red-dotted region, where logic $'1'$ is defined for $V_{CG} > V_{FE}^{+}$, and logic $'0'$ for $0 < V_{CG} < V_{FE}^{+}$. This distinction in operational behavior highlights the ability of FeS-FET to function as both NAND and NOR logic gates through its inherent ferroelectric switching mechanism. Fig. 9.9(e) further validates this capability by providing the corresponding truth tables for Fe-NAND and Fe-NOR operations.

To assess the stability of these logic states, Fig. 9.9(d) presents the retention properties of the device, where the output voltage remains consistent over time for both LRS and HRS states, when V_{CG} is set to 0 V.

9.4.3. Multilevel Logic Behavior of FeS-FET

Previously, we discussed the potential of the device as a ferroelectric logic gate when V_{PG} was fixed at a positive polarity. Now, when V_{PG} is set to a negative polarity, the device exhibits similar characteristics but with reduced conductivity, leading to a lower potential drop across the series resistor, as illustrated in Fig. 9.10(a). For this, we used a similar circuit arrangement as shown in the inset of Fig. 9.9(a). This behavior suggests that the dual-gate configuration of FeS-FET enables the design of multilevel logic circuits [167], which can be advantageous for applications such as reconfigurable logic circuits and side-channel-resistant computing [168, 169].

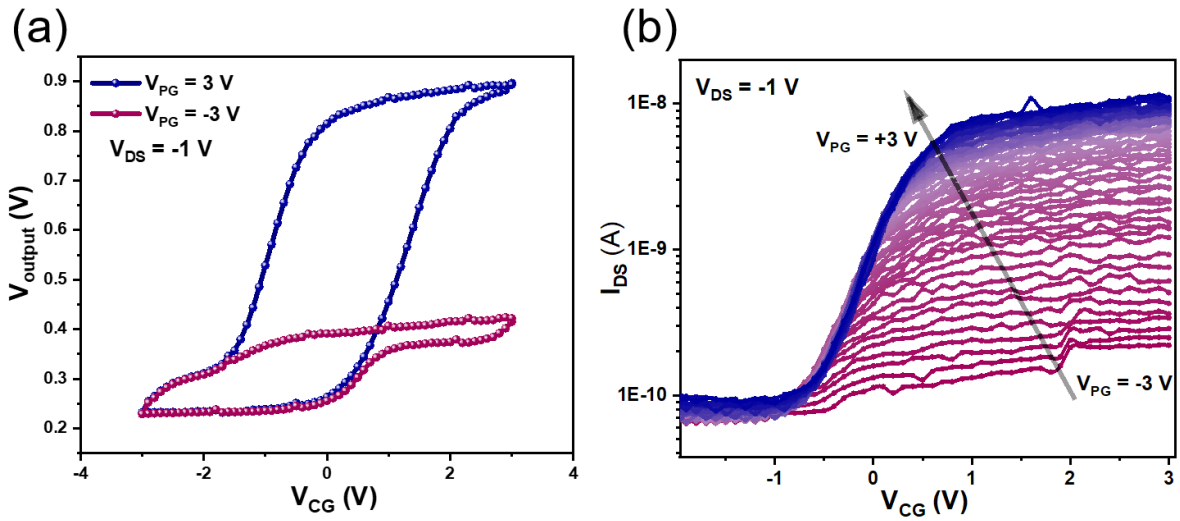


Figure 9.10: (a) Voltage output characteristics for V_{PG} set to opposite polarities with a fixed drain-source voltage ($V_{DS} = -1V$) . (b) Transconductance characteristics with different fixed V_{PG} values while V_{CG} is swept from negative to positive values, showing multiple conductance states.

Additionally, the ability to achieve multilevel states is further validated by the conductance characteristics shown in Fig. 9.10(b). The transconductance trace displays multiple conductance states for different fixed V_{PG} values, ranging from -3 V to +3 V while V_{CG} is swept. This characteristic demonstrates a conductance variation that spans two to three decades, enabling hundreds of distinguishable states, making this FeFET technology particularly suitable for multilevel logic circuits [170].

9.4.4. Device as a Threshold Shift Transistor

Fig. 9.11 illustrates the voltage output characteristics of the ferroelectric transistor under two opposite programming gate voltages. This measurement is similar to that shown in Fig. 9.9(a), but with the drain-source voltage reversed.

The voltage output characteristics of the device for different programming gate voltages (V_{PG}) are depicted in Fig. 9.11(a). This plot illustrates the dependence of the output voltage (V_{output}) on the control gate voltage (V_{CG}) for two opposite polarities of V_{PG}: specifically, at $+3\ V$ and $-3\ V$, where the drain-source voltage (V_{DS}) is maintained at $+1\ V$. A clear threshold voltage (V_{th}) shift is observed for different V_{PG} values, highlighting the tunability of the threshold voltage through ferroelectric polarization and its impact on the switching behavior of the device, enabling it to work as threshold-shift transistor [171]. These experimental findings align with the circuit simulation results discussed in the next section on logic circuit

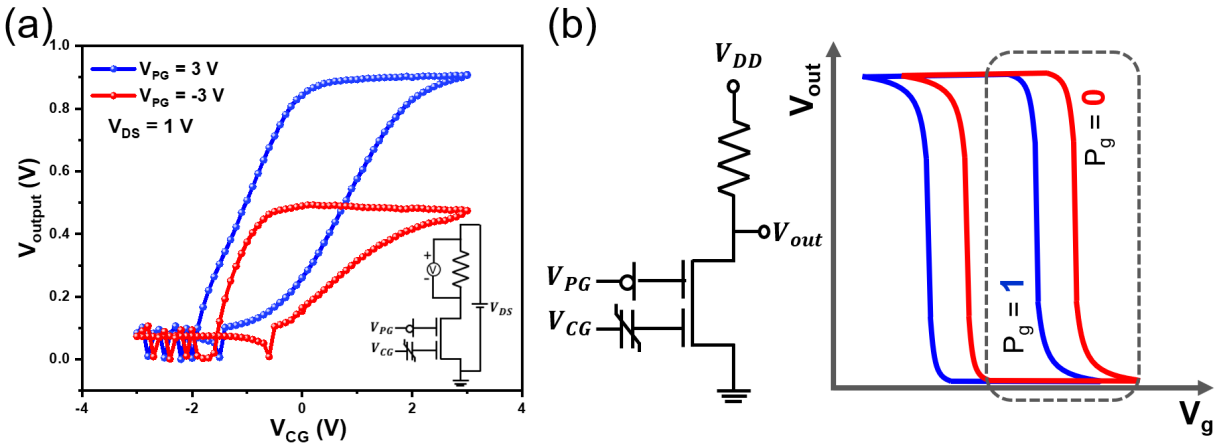


Figure 9.11: (a) Voltage output characteristics of the ferroelectric transistor for two opposite programming gate voltages ($V_{PG} = \pm 3V$) with a fixed drain-source voltage ($V_{DS} = +1V$). The inset shows the circuit configuration, where the device is connected in series with a load resistor. (b) Circuit diagram and corresponding output voltage curves across the passive load resistor.

exploration.

Fig. 9.11(b) presents the circuit diagram alongside the corresponding output voltage characteristics across a passive load resistor. The output curves depict an idealized scenario for a high-conducting device (with current in the milliampere range) and an exceptionally high on/off current ratio ($\sim 10^9$). Under these conditions, a pronounced threshold voltage shift is evident.

To align with the simulation results, the polarization state of the ferroelectric layer is denoted as P_g. When $V_{PG} = -3\ V$, the ferroelectric layer polarizes downward, corresponding to $P_g = 0$. In contrast, applying $V_{PG} = +3\ V$ results in upward polarization, setting $P_g = 1$. In this configuration, the control gate voltage (V_{CG}) is referred to as the volatile gate (V_g).

9.5. Logic Circuit Exploration

[Circuit design simulation and analysis presented in this section were carried out in collaboration with Cédric Marchand and Ian O'Connor at École Centrale de Lyon.]

9.5.1. Simple Circuit Exploration

To show the benefit of the FeS-FET presented in this work in terms of logic functionalities for the targeted application, an exploration of simple logic circuits is done in this section. Here,

two circuits, presented in Fig. 9.12, are analyzed to highlight two different behaviors.

The first one allows storing one operand of the computation inside the polarization of FeFET as a non-volatile operand. This operand will remain stored for the retention time of the technology and disappear afterward. In the case of FeFET presented in this paper, the particularly low retention time makes it possible to store sensitive values in a zero-trust application, for example, ensuring that this information will disappear within minutes.

The second use case is the programmable logic gates, where the polarization of the FeFET is used to program an operation (which can also be sensitive in the case of this technology). The operation can then be performed at the two other gates.

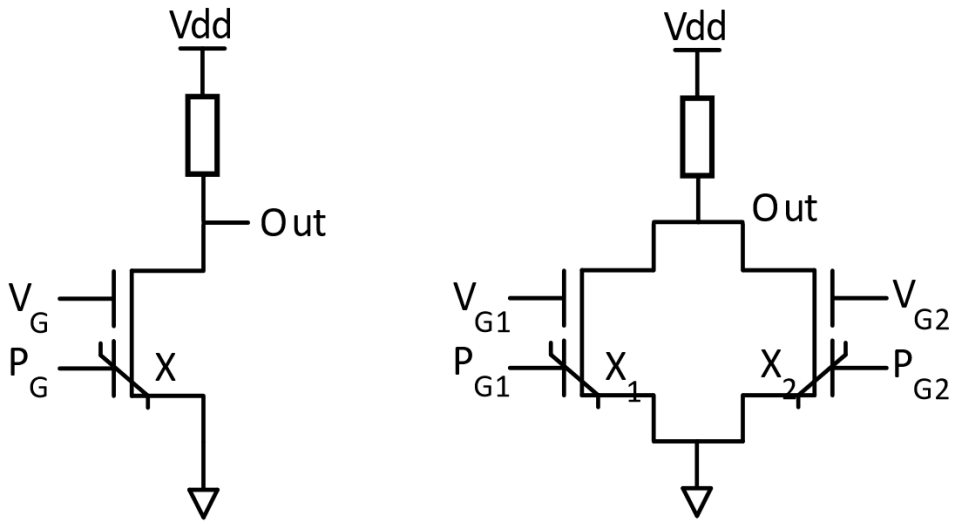


Figure 9.12: logic circuit analyzed for logic exploration on the FeFET technology.

9.5.2. Equivalent Circuit Design

However, before running any simulation, an equivalent circuit is designed based on the behavior of the device. To achieve this equivalent circuit, the so-called RFeFET is formalized using the following notations:

- $X \in \{P^-, P^+\}$: The remanent polarization of the ferroelectric capacitor. P^- corresponds to a higher threshold voltage (V_{th}) and is used as a logical 0, whereas P^+ corresponds to logical 1, meaning a lower V_{th}. To achieve this non-volatile state, a strong negative pulse (-3V) results in High V_{th} (HVT), while a strong positive pulse (+3V) results in Low V_{th} (LVT).
- $PG \in \{0, 1\}$: In addition to the polarization of the ferroelectric layer, it is also possible to slightly shift V_{th} of the RFeFET by applying a constant logical voltage to the polarity

gate. This adjustment enables a "normal behavior" when the RFeFET is set in HVT by slightly decreasing V_{th}, and an "always on" transistor when it is set to LVT.

- $V_G \in \{0, 1\}$: The volatile gate, which functions as the standard transistor gate.

With these notations, the conduction table presented in Table 9.1 is possible. According to Table 9.2, it can be observed that X and PG have a symmetrical role in the device. Since they can be used to shift the V_{th} of the transistor, they can be modeled by voltage sources connected in series to the gates. This modeling approach allows us to propose the equivalent circuit described in Fig. 9.13 to emulate the RFeFET and simulate the simple circuits presented in Fig. 9.12.

X	VG	PG = 0	PG = 1
0	0	Off	Off
0	1	Off	On
1	0	Off	On
1	1	On	On

Table 9.1: Conduction table of the RFeFET.

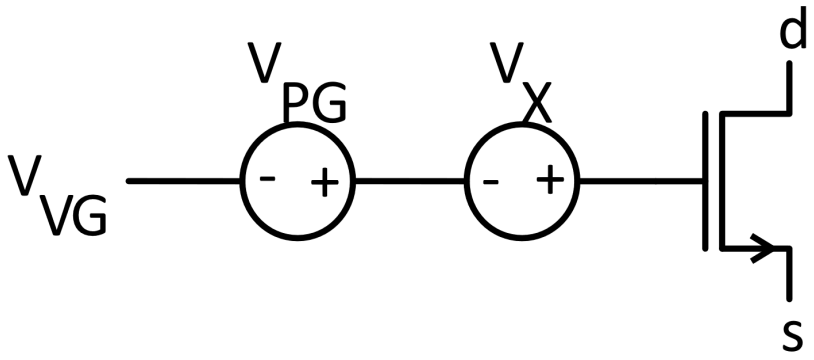


Figure 9.13: Equivalent circuit of the RFeFET.

9.5.3. Simple Circuit Simulation and Results

Concerning non-volatile logic gates, previous publications such as [118] and [172] explore the design of simple logic gates, each assuming a single behavior: NAND or NOR. However, with this device, both behaviors can be achived within a single device.

Exploration based on the simulation of four simple circuits with a resistive pull-up demonstrates all the different 2-input logic gates possible.

Single RFeFET

The first circuit can function as a volatile operation, programmed for a single computation that temporarily remains in the device. This can be seen as a programmable logic gate.

PG (V)	VG	Conduction state
-3	0	Off
-3	1	Off
+3	0	Off
+3	1	On

Table 9.2: Conduction table.

Fig. 9.14 presents NAND/NOR behavior depending on the P_G value. Considering one non-volatile operand inside the FeFET (X) and one volatile operand applied on V_G (A), it is possible to achieve:

- If $P_G = 0$, $S = \overline{A \cdot X}$
- If $P_G = 1$, $S = \overline{A + X}$

Similarly, it is possible to achieve a volatile logic gate considering X as a configuration and two volatile operands on $P_G = A$ and $V_G = B$:

- If $X = 0$, $S = \overline{A \cdot B}$
- If $X = 1$, $S = \overline{A + B}$

This circuit, composed of a single RFeFET with a resistive pull-up for logic exploration, can be seen as two n-type transistors connected in series or in parallel.

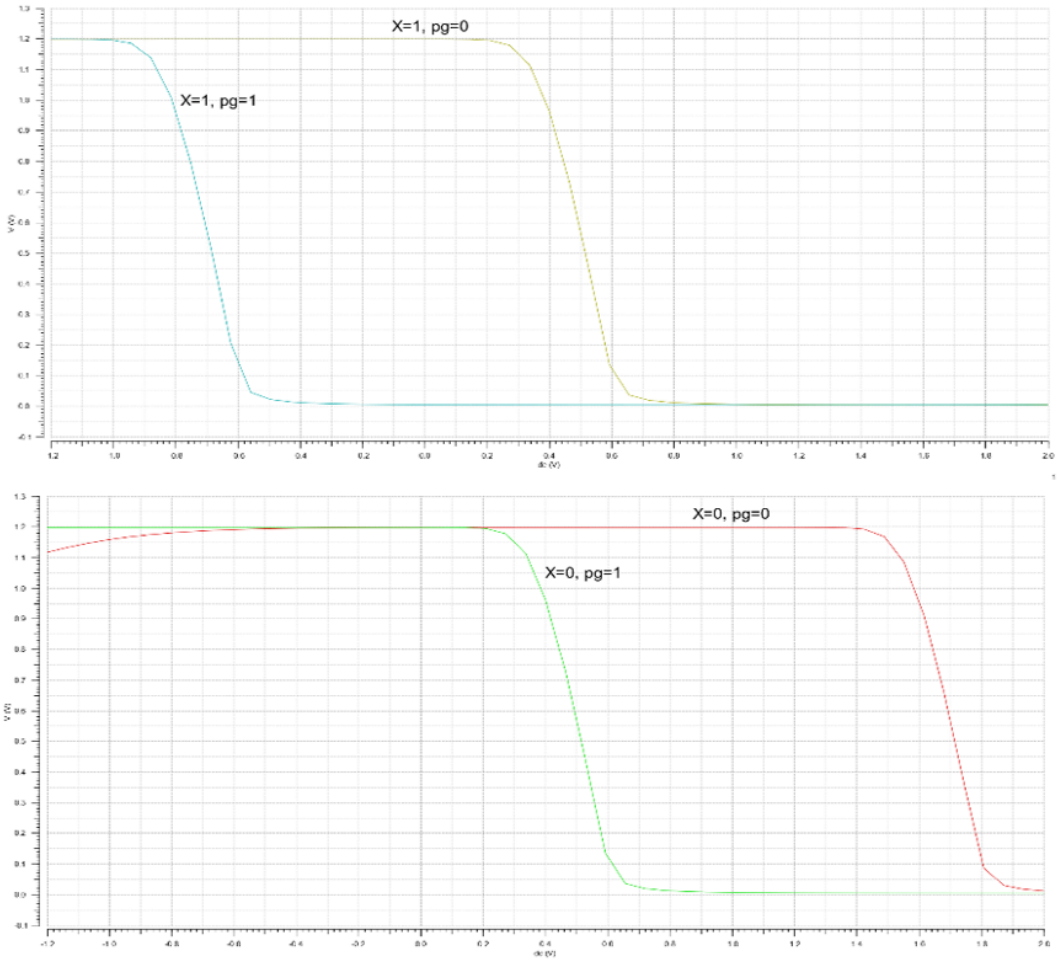


Figure 9.14: Output obtained by circuit used in (Fig. 9.13), presenting shift in threshold voltage.

9.5.4. Parallel Connection Between Two Devices

Based on the conduction table and the simulation of this circuit using the equivalent circuit presented in Fig. 9.13, it is possible to analyze all functionalities that can be achieved using the parallelly connected circuit. The simulations are presented in Fig. 9.14.

Concerning non-volatile logic gates, all functions from Table 9.3 can be executed based on the values of P_{g1} and P_{g2}. However, not all cases are presented because of the symmetrical behavior of the circuit.

P_{g1}	P_{g2}	X_1	X_2	V_{g1}	V_{g2}	S
0	0	B	$\bar{B}$	A	A	$\overline{A \cdot B}$
0	0	B	$\bar{B}$	A	$\bar{A}$	$\bar{B}$
0	0	B	$\bar{B}$	$\bar{A}$	A	$A \oplus B$
0	0	B	$\bar{B}$	$\bar{A}$	$\bar{A}$	$\overline{A \oplus B}$
0	1	B	$\bar{B}$	A	A	$A + B$
0	1	B	$\bar{B}$	A	$\bar{A}$	$\overline{A + B}$
0	1	B	$\bar{B}$	$\bar{A}$	A	0
0	1	B	$\bar{B}$	$\bar{A}$	$\bar{A}$	0
1	1	B	B	A	A	$A \cdot B$
1	1	$\bar{B}$	$\bar{B}$	$\bar{A}$	$\bar{A}$	$A \cdot B$

Table 9.3: Conduction table.

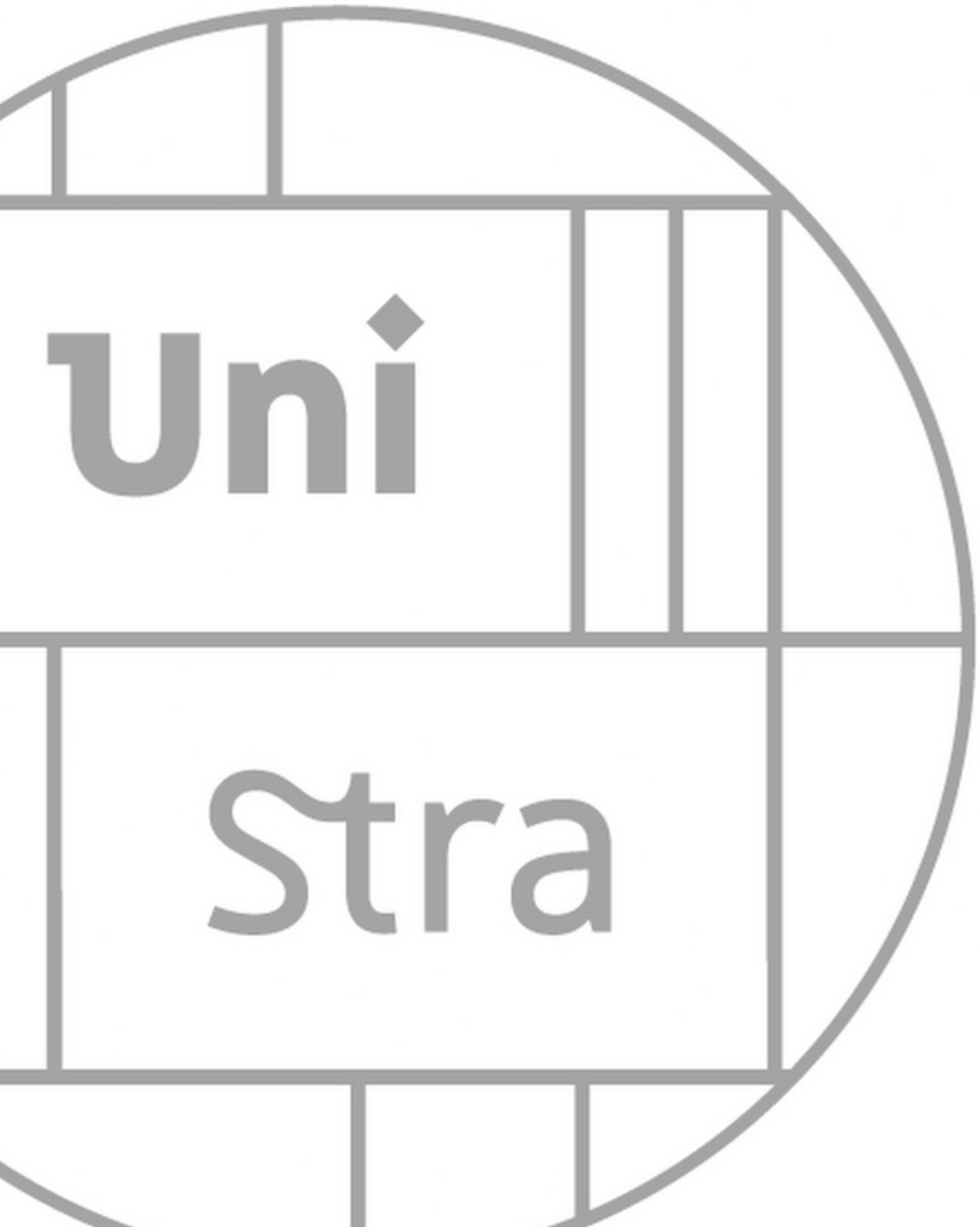
From Table 9.3, it can be observed that all elementary logic gates with two inputs are achievable using this parallel circuit in a non-volatile manner. The same applies when treating the non-volatile polarization as a configuration and applying logic operands to P_{g1}, P_{g2}, V_{g1}, and V_{g2}.

9.6. Conclusion

- In this work, we presented a novel FeS-FET architecture by integrating α-In_2Se_3 with an hBN dielectric layer, harnessing the power of a split-gate design for independent ferroelectric polarization control.
- Through precise fabrication and characterization using AFM, PFM, and Raman spectroscopy, we validated the structural integrity, uniform thickness, and phase purity of α-In_2Se_3.
- We demonstrated the remarkable ferroelectric switching capabilities of α-In_2Se_3, revealing both in-plane and out-of-plane hysteresis effects. With a well-defined memory window of 12 V and an ON/OFF ratio spanning four decades, the device exhibited robust charge transport modulation. The dual-gate configuration further unlocked dynamic

threshold voltage tuning and enhanced reconfigurability, offering an advanced approach to controlling electronic properties.

- By leveraging the dual-gate configuration, we presented the potential of FeS-FETs in logic applications, showcasing their ability to function as volatile NAND gates and reconfigurable Fe-NAND and Fe-NOR logic elements. The multilevel conductance behavior highlighted their adaptability for next-generation computing, where efficient and programmable logic circuits are crucial.
- Through circuit simulations, we confirmed its capability for non-volatile operand storage and threshold shift operation, demonstrating that a tow parallelly connected FeS-FET can be leveraged to implement all elementary logic operations.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10 | Conclusion and Perspectives

Over the period of my PhD research, I explored the immense potential of van der Waals ferroelectric field-effect transistors (FeFETs) and their applications in reconfigurable electronics, optoelectronics, logic circuits, and neuromorphic computing. Our results are divided into four parts in this thesis, which I will conclude here.

First, I introduced a reconfigurable ferroelectric field-effect transistor (Re-FeFET) with a split-gate architecture, fabricated using a $CuInP_2S_6$/hBN/WSe_2 heterostructure. This novel architecture provided complete electrostatic control over the WSe_2 semiconducting channel, enabling precise reconfigurability between p-type, n-type, and ambipolar transport regimes. Next, we explored its optoelectronic properties in diode mode and observed an efficient photovoltaic effect, highlighting the multifunctionality of our devices. Using the split-gate design, we demonstrated the ability to seamlessly switch between ferroelectric logic (Fe-NAND, Fe-AND) and electronic logic (XNOR). Furthermore, circuit simulations confirmed that two Re-FeFETs connected in series could implement all fundamental logic gates, reducing the transistor count by up to 80% compared to CMOS. This work highlights the potential of our approach for both More-than-Moore and Beyond-Moore future of electronics, in particular for an energy-efficient implementation of in-memory computing and machine learning hardware, due to their multifunctionality and design compactness.

Building upon this, I systematically investigated the scaling effects of FeFETs by fabricating devices with different channel lengths, ranging from 1 μm to 50 nm—100 times shorter than previous configurations in similar ferroelectric vdW systems. We analyzed the short-channel effect, where the device showed drain-induced barrier lowering (DIBL) at high voltage. Interestingly, within an optimal voltage range, we also observed reverse DIBL and identified negative capacitance behavior, a crucial feature for ultra-low-power electronic applications. Our subthreshold swing (SS) analysis confirmed that short-channel devices achieved switching below the thermal limit, making them highly energy-efficient. Moreover, we demonstrated dynamic reconfigurability using a ferroelectric floating top gate and a back gate, which allowed us to precisely tune the doping states and switch between n-type, p-type, and ambipolar states. These findings offer valuable insights for the design of future high-performance and scalable

electronics based on FeFETs.

Next, I explored the synaptic functionality of our van der Waals FeFETs, focusing on devices with 50 nm channel lengths. Through electronic transport measurements and piezoresponse force microscopy (PFM) characterization, we demonstrated that multidomain ferroelectric polarization tuning in $CuInP_2S_6$ directly influenced the conductance of the WSe_2 channel. By applying tailored voltage pulse schemes, we achieved continuous, reversible conductance modulation, mimicking the behavior of biological synapses. Our FeFET-based artificial synapse exhibited both excitatory and inhibitory synaptic plasticity, making it a promising candidate for reconfigurable neuromorphic computing. Artificial neural network (ANN) simulations confirmed its potential, achieving up to 90% accuracy in handwritten digit recognition, closely approaching ideal synaptic performance (96%). These results mark a significant step towards reconfigurable neuromorphic circuits, bringing us closer to energy-efficient brain-inspired computing hardware.

Finally, I extended our investigation to ferroelectric semiconducting channels, replacing $CuInP_2S_6$ with α-In_2Se_3 in a split-gate architecture. By integrating hBN as a dielectric gate spacer and α-In_2Se_3 as a ferroelectric-semiconducting channel, we developed a ferroelectric-semiconductor field-effect transistor (FeS-FET). We first analyzed unique in-plane and out-of-plane polarization properties of α-In_2Se_3. Leveraging the out-of-plane polarization and two independent gate configurations, we demonstrated its potential in logic applications where it functions as a volatile NAND gate, as well as reconfigurable Fe-NAND and Fe-NOR elements. Additionally, we explored the device functionality as a multilevel transistor and threshold-shift transistor. Circuit simulations further validated our experimental findings and demonstrated that two FeS-FETs connected in parallel can implement all elementary logic operations, reinforcing their promises for future reconfigurable logic circuits.

By combining the power of van der Waals ferroelectronics with reconfigurable electronics, our research demonstrates a scalable approach for developing adaptive, energy-efficient, and intelligent electronic systems. As computing architectures evolve, our findings offer an approach for developing future ultra-scalable, high-performance devices with promising applications in reconfigurable electronic, in-memory computing, and neuromorphic hardware.

Future Perspectives

- **Investigating device performance with thinner $CuInP_2S_6$ layers:** Our work on reconfigurable ferroelectric field-effect transistor (Re-FeFET) devices with a split-gate architecture has demonstrated their potential for next-generation electronics. These devices were fabricated with van der Waals ferroelectric material ($CuInP_2S_6$) as a gate

insulator, which retain ferroelectricity even at the monolayer level. Future research could focus on integrating thinner insulating gate layers, not necessarily monolayers but thinner than the 100–400 nm range used in our study. Reducing thickness would increase capacitance, enhance switching speed, and enable more compact device designs, optimizing FeFET performance for advanced applications [173].

- **Expanding material choices:** The number of known 2D ferroelectric materials is currently quite limited, making it important to explore new candidates for FeFET applications. A promising approach involves sliding-ferroelectric materials [157, 158, 174], where ferroelectricity arises from atomic layer stacking or sliding, enabling reversible spontaneous polarization. This mechanism significantly expands the family of 2D ferroelectric materials and opens up new possibilities for electronic applications. Additionally, integrating alternative ambipolar semiconductors, such as $MoTe_2$ [175, 176] and black phosphorus (BP) [177–179], could provide further insights into material compatibility and device versatility.

- **Enhancing switching speed and exploring negative capacitance:** Future work should focus on investigating ferroelectric switching kinetics using shorter pulse widths in the nanosecond range, which could provide insights into device speed limitations and response time. Additionally, a focused study on negative capacitance effects in FeFETs is essential for optimizing switching efficiency, which is particularly crucial for ultra-low-power applications. A deeper understanding of these properties could lead to energy-efficient FeFET designs with enhanced performance.

- **Leveraging Hebbian-learning for adaptive computing:** Our study on FeFET switching kinetics has demonstrated that homogeneous partial switching plays a crucial role in tuning the device as a synaptic weight, enabling supervised learning. Alternatively, FeFETs could also implement unsupervised learning by leveraging domain nucleation-based switching, mimicking Hebbian-learning [147, 180] through spike-timing-dependent plasticity (STDP). To fully explore this mechanism, detailed PFM studies on ferroelectric nucleation kinetics are needed, as switching follows a nucleation-limited model, where domains gradually nucleate and expand rather than switching uniformly. Following the work of Boyn et al. (2017) [181], could be a good starting point for further exploration of ferroelectric nucleation dynamics.

- **Investigating FeFETs as neurons for brain-inspired computing:** FeFETs are not only promising for synaptic applications but can also function as neurons, paving the way for fully ferroelectric neuromorphic computing. By exploiting nucleation-limited switching, where small ferroelectric domains gradually switch states until a critical threshold

is reached, FeFETs can process and integrate signals, similar to biological neurons.

Work by Mulaosmanovic et al. (2018) [182] demonstrated that FeFETs can replicate neuron-like behavior through optimized gate voltage pulse shaping, allowing them to exhibit integrate-and-fire dynamics, where signals accumulate over time and trigger an output once a threshold is reached. This enables FeFETs to mimic spike-timing-dependent plasticity (STDP), refractory periods, and exhibit leaky integration, replicating key neuronal behaviors with minimal circuit complexity. Exploring FeFETs as both synaptic and neuronal elements could lead to energy-efficient artificial neural networks, accelerating progress toward brain-inspired computing architectures that function more like the human brain.

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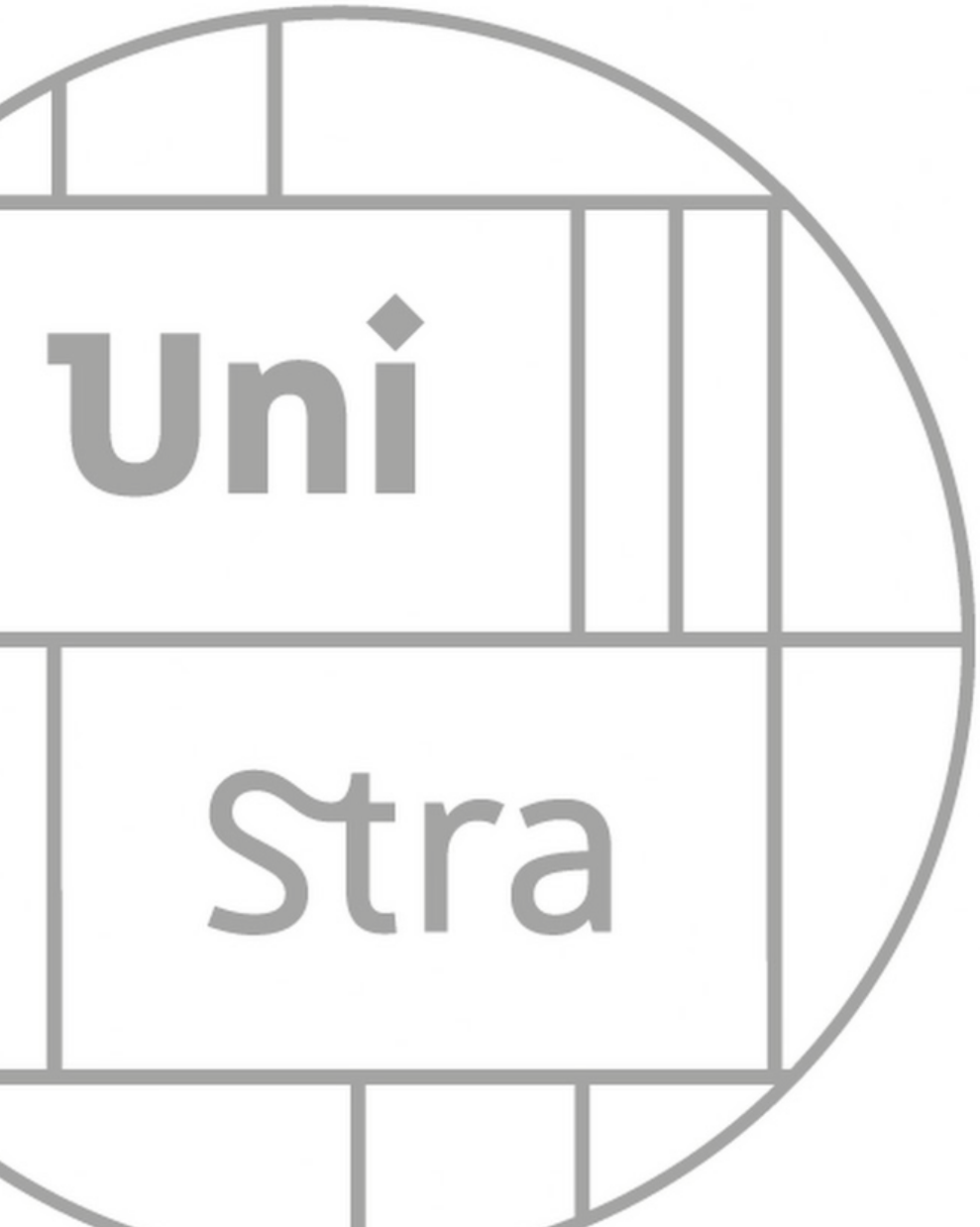
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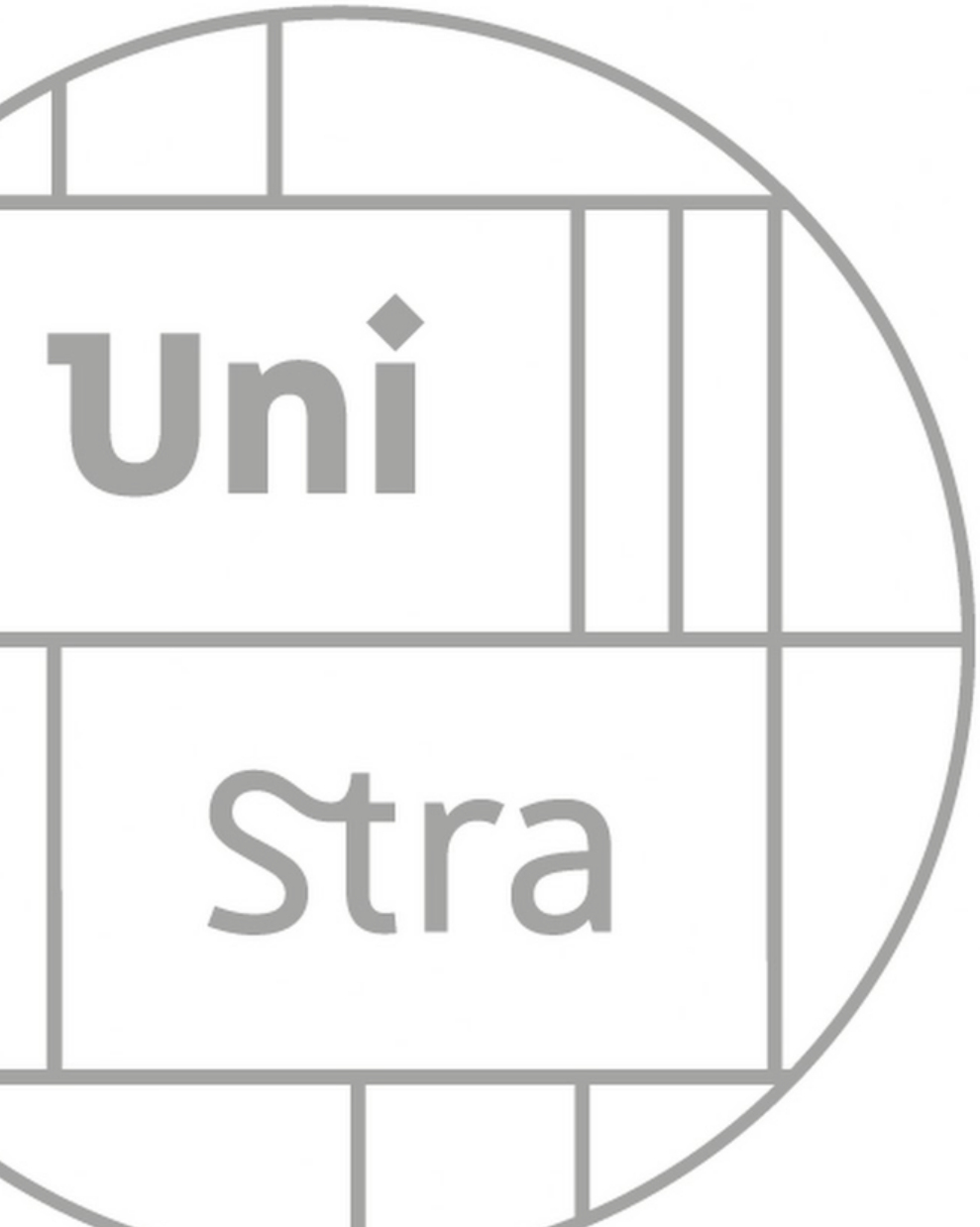
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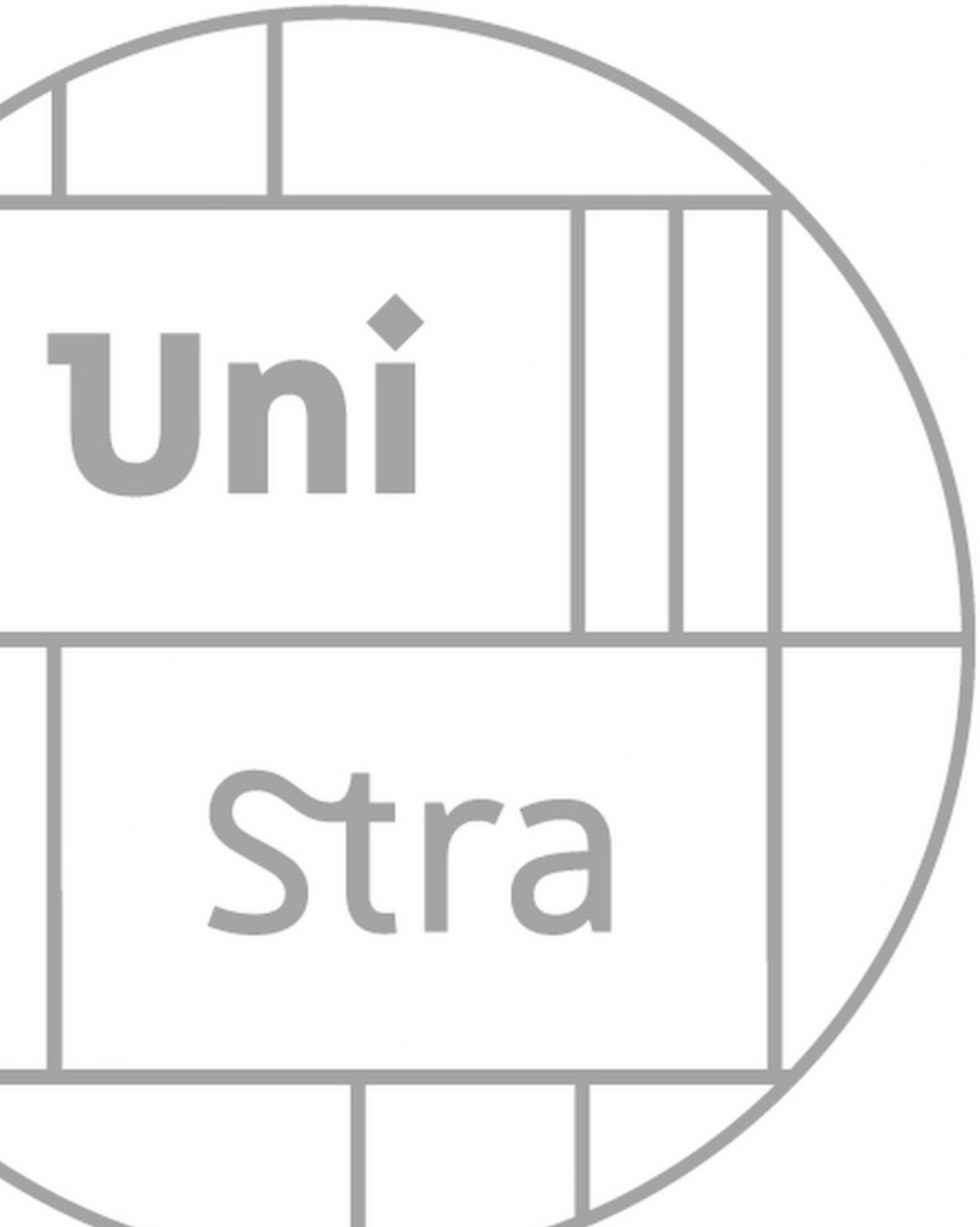
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Emerging Ferroelectric Devices

Résumé

À mesure que la technologie CMOS conventionnelle atteint ses limites physiques de miniaturisation, l'exploration de concepts et de matériaux alternatifs devient essentielle pour maintenir les avancées dans le traitement de l'information à faible consommation d'énergie. Les transistors à effet de champ ferroélectriques (FeFET), en particulier ceux basés sur des matériaux de van der Waals (vdW), apparaissent comme des candidats prometteurs grâce à leur commutation non volatile et à leur compatibilité avec une intégration multifonctionnelle. Cette thèse présente une étude approfondie des dispositifs ferroélectriques émergents, en se concentrant sur leur conception, leur fabrication et leurs applications dans l'électronique reconfigurable, la logique, le calcul en mémoire et l'architecture neuromorphique.

Une contribution clé de ce travail est le développement d'un FeFET à grille divisée reconfigurable (Re-FeFET) basé sur une hétérostructure $CuInP_2S_6$/hBN/WSe_2, permettant une commutation programmable entre conduction de type *p*, *n* et ambipolaire grâce à la modulation électrostatique du canal. Cela permet l'implémentation de fonctions logiques telles que Fe-NAND, Fe-AND et XNOR dans un seul dispositif. Il présente également une réponse photovoltaïque, indiquant un potentiel pour des applications optoélectroniques nanométriques. Le comportement d'échelle est exploré à travers des FeFET à canal court jusqu'à 50 nm, qui montrent une amélioration de la pente sous-seuil et un abaissement réversible de la barrière induit par le drain, dus à la capacitance négative du $CuInP_2S_6$, tout en maintenant la reconfigurabilité via une grille flottante et une grille arrière. Le potentiel neuromorphique est démontré par l'utilisation de la commutation des domaines ferroélectriques pour imiter la plasticité synaptique avec une modulation réversible de la conductance sous impulsions de tension. Enfin, un transistor ferroélectrique-semiconducteur (FeS-FET) utilisant α-In_2Se_3 est étudié, où la coexistence des propriétés semiconductrices et ferroélectriques permet une logique reconfigurable avec fonctionnement multivalué et ajustabilité de la tension de seuil. Dans l'ensemble, ces études mettent en évidence le potentiel des transistors ferroélectriques 2D comme éléments de base pour une électronique future économe en énergie, compacte et multifonctionnelle.

Mots-clés : FeFET, matériaux 2D, $CuInP_2S_6$, WSe_2, α-In_2Se_3, hétérostructures de van der Waals, électronique reconfigurable, logique, calcul neuromorphique, optoélectronique.

Abstract

As conventional CMOS technology approaches its physical scaling limits, exploring alternative device concepts and materials is essential to maintain advances in energy-efficient information processing. Ferroelectric field-effect transistors (FeFETs), particularly those based on van der Waals (vdW) materials, have emerged as promising candidates owing to their non-volatile switching and compatibility with multifunctional integration. This thesis presents a comprehensive investigation of emerging ferroelectric devices, focusing on their design, fabrication, and applications in reconfigurable electronics, logic, in-memory computing, and neuromorphic architecture.

A key contribution of this work is the development of a reconfigurable split-gate FeFET (Re-FeFET) based on a $CuInP_2S_6$/hBN/WSe_2 heterostructure, enabling programmable switching between *p*-type, *n*-type, and ambipolar conduction through electrostatic channel modulation. This supports the implementation of various logic functions, such as Fe-NAND, Fe-AND, and XNOR, within a single device. It also exhibits a photovoltaic response, indicating potential for nanoscale optoelectronic applications. Scaling behavior is explored through short-channel FeFETs down to 50 nm, which show improved subthreshold swing and reversible drain-induced barrier lowering driven by the negative capacitance of $CuInP_2S_6$, while maintaining reconfigurability via a floating gate and back-gate. Neuromorphic potential is demonstrated by using ferroelectric domain switching to emulate synaptic plasticity with reversible conductance modulation under voltage pulses. Finally, a ferroelectric-semiconductor FET (FeS-FET) using α-In_2Se_3 is studied, where the coexistence of semiconducting and ferroelectric properties enables reconfigurable logic with multilevel operation and threshold-voltage tunability. Overall, these studies highlight the potential of 2D ferroelectric transistors as building blocks for future energy-efficient, compact, and multifunctional electronics.

Keywords: FeFET, 2D materials, $CuInP_2S_6$, WSe_2, α-In_2Se_3, van der Waals heterostructures, reconfigurable electronics, logic, neuromorphic computing, optoelectronics.