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Matrices Crossbar basées sur Mémoires à Changement de Phase (PCM) et sélecteur Ovonic Threshold Switching (OTS): un défi de fiabilité vers les nouvelles architectures de calcul 3D

Crossbar Array based on Phase Change Memory (PCM) and Ovonic Threshold Switching (OTS) selector: a challenge for the future of computing

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Abstract (English)

Nowadays, computing systems face an exponential surge in data from AI, IoT, and industrial systems; conventional memories are increasingly inadequate to keep pace. Volatile DRAM/SRAM consumes power for refresh operations and loses its state upon power-off, while Flash is slower, requires higher programming voltages, and wears out over time. The von Neumann architecture is intrinsically liited by energy consumption and latency bottlenecks. Emerging approaches, such as AI accelerators, matrix-vector engines, and in-memory or near-memory computing, require dense, low-power, and reliable non-volatile memories. This work investigates the co-integration of Phase Change Memory (PCM) with Ovonic Threshold Switch (OTS) selectors in crossbar arrays to meet these needs by targeting high-speed, highly scaled standalone memories and reliable, low-power embedded systems. The thesis pursues three goals: validate and characterize the one-selector/one-resistor (1S1R) cell; analyze reliable programming and reading; and demonstrate a functional crossbar array. PCM, built from chalcogenide alloys such as Ge-Sb-Te, switches reversibly between amorphous (high resistance) and crystalline (low resistance) phases, enabling binary and multi-level storage with high scalability potential. Key reliability challenges include resistance drift, endurance limits from atomic migration, and high-temperature retention. OTS devices are two-terminal selectors with volatile threshold switching: they switch from OFF to ON above a threshold voltage and return to OFF below a holding current level. Their strong nonlinearity suppresses sneak currents in dense crossbars while delivering required currents to the selected PCM cell. OTS operation relies on field-induced switching in amorphous chalcogenide materials. Materials such as GeSbSeN are explored for improved stability, endurance, and reduced threshold drift. Co-integration challenges arise from coupling the two chalcogenide technologies. This work investigates the thermal properties of OTS and PCM, presenting a novel Double-Patterned Self-Aligned (DPSA) architecture that advances OTS integration and scaling. We combine device- and array-level analysis to characterize the impact of the OTS+PCM co-integration, providing programming and reading statistics. We propose an empirical read-reliability model to capture the effects of device variability, temperature, and cycling stress on long-term storage behavior. Major failure mechanisms, drift phenomena, and OTS-PCM interactions during extended operation are identified. This

work presents material optimizations of PCM and OTS, with a focus on tuning the Sb/Te ratio in GeSbTe, producing a congruent, high-Sb/Te alloy that achieves sub-100 ns SET pulses, expands the 1S1R memory window to about 2 V, and improves endurance to 10^7 cycles, on par with state-of-the-art. Finally, a functional crossbar array is fabricated and characterized, addressing array-level issues such as sneak path currents, device-to-device variability, threshold constraints, and scaling limitations, and clarifying trade-offs in memory window and subthreshold engineering for large arrays. The study relies on advanced semiconductor processing, electrical characterization, electrothermal simulations, statistical modeling, and physical analyses. We provide an empirical model of read-induced threshold shifts and failure prediction. Remaining challenges include simplifying integration, lowering programming voltages and currents, and further improving data retention and endurance. The thesis outlines concrete development paths focused on voltage reduction and robustness, laying groundwork for reliable, scalable PCM+OTS technology.

Keywords: Phase-Change Memory, Ovonic Threshold Switch, Reliability, Nonvolatile Memory

Résumé (Français)

Le calcul contemporain est confronté à une explosion des données issues de l'IA, de l'IoT et des systèmes industriels, tandis que les mémoires conventionnelles peinent à suivre ce rythme. Les mémoires volatiles DRAM et SRAM necessitent un rafraichîssement constant et perdent leur état hors tension. La mémoire Flash, plus lente, exige des tensions de programmation élevées et se dégrade avec l'usage. L'architecture de Von Neumann, intrinsèquement energivore, souffre d'un gouled d'étranglement lié à la latence de transmission. Les approches émergentes, telles que les accélérateurs d'IA et le calcul *in-memory*, requièrent des mémoires non volatiles à la fois denses et fiables. Ce travail étudie la co-intégration des Mémoires à Changement de Phase (PCM) et des sélecteurs à seuil, où Ovonic Threshold Switch (OTS), pour la réalisation de matrices crossbar destinées à des mémoires autonomes sur des nœuds technologieques avancés, ainsi qu'à des systèmes embarqués fiables et à faible consommation. Cette étude poursuit trois objectifs : valider et caractériser électriquement la cellule sélecteur/résistance (1S1R), analyser la fiabilité en programmation et en lecture, et démontrer une matrice crossbar fonctionnelle. La PCM, à base de matériaux chalcogénures tels que le Ge-Sb-Te, commute de façon réversible entre une phase amorphe (haute résistance) et une cristalline (faible résistance), permettant un stockage binaire où multi-niveaux. Les principaux défis de fiabilité concernent la dérive de l'état résistive, les limites d'endurance dues aux migrations atomiques et la rétention des données à haute température. Les dispositifs OTS, sélecteurs bipolaires à commutation de seuil volatile, basculent entre états OFF et ON au-delà d'une tension seuil, avant de revenir en OFF sous le courant de maintien. Leur forte non-linéarité supprime les courants parasites dans les matrices denses tout en délivrant le courant nécessaire à la programmation de la cellule PCM adressée. La co-integration de deux technologies chalcogénures pose cependant plusieurs défis. Ce travail examine les propriétés thermiques de l'OTS et de la PCM et introduit une nouvelle architecture auto-alignée innovante, dite Double-Patterned Self-Aligned (DPSA). L'impact de la couche PCM sur les performances est évalué par une étude statistique des opérations de programmation et de lecture sur les cellules 1S1R. Un modèle empirique de fiabilité en lecture est proposé, integrant les effets des variations de dispositifs, de la température et du cyclage sur le comportement à long terme. Les mécanismes de défaillance, les phénomènes de dérive et les interactions OTS-

PCM en fonctionnement prolongé sont identifiés. Le travail présente une optimization des matériaux PCM et OTS, en s'appuyant sur l'ajustement du rapport Sb/Te dans l'alliage GeSbTe. Une composition congruente à haut Sb/Te permet d'obtenir des impulsions SET très courtes, d'élargir la fenêtre mémoire 1S1R à 2 V et d'améliorer l'endurance au niveau de l'état de l'art. Enfin, une matrice crossbar fonctionnelle est fabriquée et caractérisée, en prenant en compte les effets des courants de fuite, de la variabilité inter-dispositifs, et des contraintes sur les tensions de seuil. La discussion met en évidence les compromis d'ingénierie entre fenêtre mémoire et courant de sous-seuil pour les matrices de grande taille. L'étude repose sur des procédés avancés de nanofabrication, des caractérisation électrique, des simulations électrothermiques, des modélisation statistiques et des analyses physiques. Les défis restants concernent la simplification de l'intégration, la réduction des tensions et courants de programmation, ainsi que l'amélioration de la rétention et de l'endurance. Cette thèse ouvres des pistes de concrètes développement, jetant les bases d'une technologie PCM+OTS fiable.

Mots clés : Mémoire à changement de phase, Ovonic Threshold Switch, Fiabilité, Memoires Nonvolatiles

List of Acronyms

1S1R One-Selector One-Resistor

AI Artificial Intelligence

ALD Atomic Layer Deposition

BEOL Back End Of Line

C2F Cycles–to–Failure

CD Critical Dimension

CMP Chemical-Mechanical Polishing

CPU Central Processing Unit

CXL Compute Express Link

DPSA Double-Patterned Self-Aligned

DRAM Dynamic Random Access Memory

ECDF Empirical Cumulative Density Function

EDX Energy Dispersive X-ray

FWHM Full-Width Half-Maximum

GPU Graphical Processing Unit

HAADF High-Angle Annular Dark-Field

HDD Hard Disk Drive

IFM Inhibit Fail Margin

IMC In-Memory Computing

IoT Internet-of-Things

IQR Interquartile Range

KDF Kernel Density Function

LLM Large Language Model

MAC Multiply and Accumulate

MAD Memory Advanced Demonstrator

ML Multilayer

MPW Multi-Project Wafer

MRAM Magnetic Random Access Memory

MVM Matrix Vector Multiplication

MW Memory Window

NMC Near-Memory Computing

NVM Non-Volatile Memory

OTS Ovonic Threshold Switching

PCM Phase-Change Memory

PVD Physical Vapor Deposition

ReRAM Resistive Random Access Memory

RIE Reactive Ion Etching

RW Resistance Window

RWM Read Window Margin

SCM Storage Class Memory

SEM Scanning Electron Microscope

SNN Spiking Neural Network

SRAM Static Random Access Memory

SSD Solid-State Drive

TCAD Technology Computer-Aided Design

TEM Transmission Electron Microscope

UL Underlayer

VXP Vertical XPoint

WL Word Line

XRD X-Ray Diffraction

Context and Objectives

Over the last 20 years, technology advancements have dramatically increased the volume of data generated and processed, forecasted to 394 ZB in 2028, a threefold increase from 130 ZB in 2023 (1 ZB = 10^{12} GB) [1]. This *Big Data* encompasses information generated by research, healthcare, industry, and a vast number of end-users, producing a large volume of data of great intrinsic value for multiple applications. How can modern computing systems effectively manage and leverage this exponentially growing amount of data? Over the last two decades, data storage has shifted from the client to the cloud, accelerated by the advent of the AI era in the last five years. The development of complex AI algorithms and Large Language Model (LLM) has permeated our lives and every industrial application, producing an estimated economic growth of more than 30 % across fields ranging from factories, power grid distribution, to hospitals and clinics [2]. The data volume generated each year (**Fig. 1**) must be processed and stored. Temporary data, such as that used for AI inference and computation, is generally stored in fast-access volatile memory close to the processing core, such as SRAM and DRAM, which requires larger and larger working memory, making the system expensive and power-hungry. Processed data coming from the aforementioned sources is stored in Non-volatile Memories (NVM) such as SSD and HDD due to the larger capacity and reduced cost-per-bit ($/bit).

The memory footprint depends on media type, increasing approximately by one order of magnitude from text to images, audio, and videos (**Fig. 2**); when dealing with Large Language Model (LLM), all the computation required to produce the output acounts for about 98% of the total memory footprint, while the final media file is the remaining 2% [1]. Therefore, computing systems must account for data generation and storage, as well as the associated overhead resulting from the movement of data between the processing unit (CPU, GPU) and mass memory. The most critical issues in today's data handling are related to energy consumption, memory access speed, and processing speed. A different type of application, still requiring careful memory consideration, is the constellation of IoT composed of microcontrollers, sensors, and embedded systems requiring reliable and low-power memory.

To perform fast computation, data centers employ a large quantity of off-chip DRAM or integrated SRAM in CPUs and GPUs. DRAM, for instance, accounts for over 40%

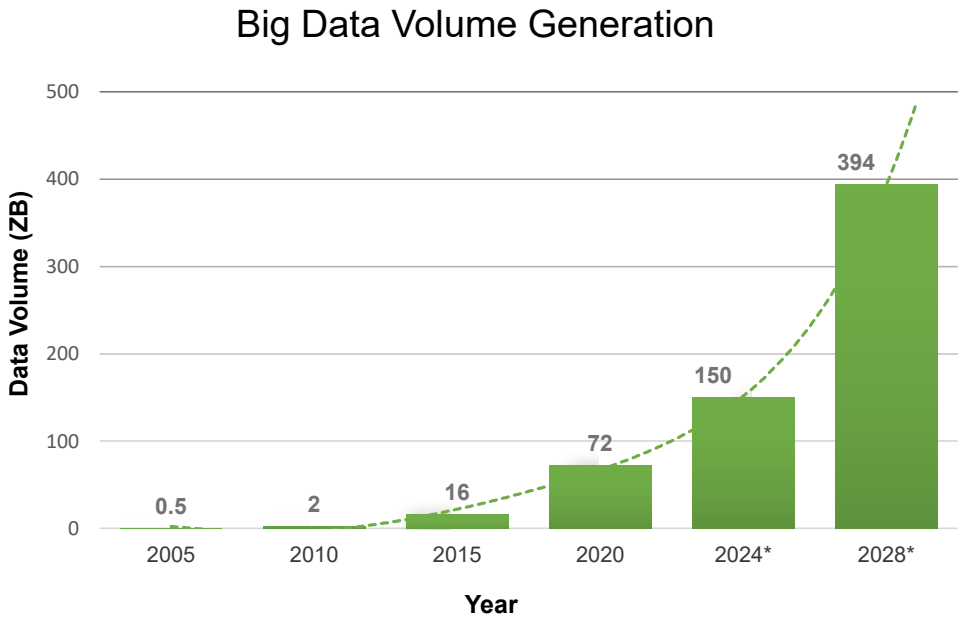


Figure 1: *Big Data* volume generation over the last two decades, forecasting more than 394 ZB in the year 2028. Data from [1, 2].

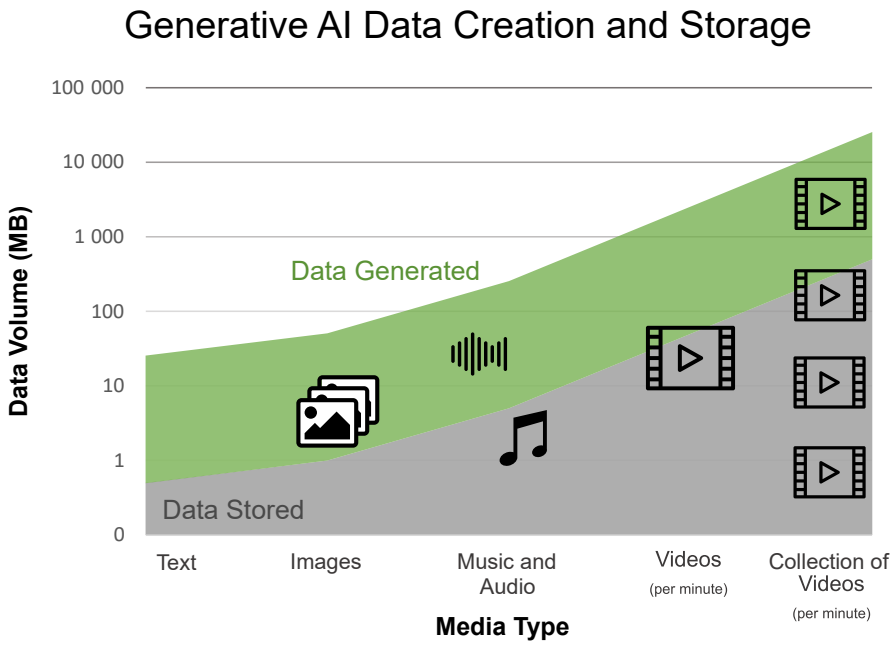


Figure 2: Memory footprint of different media types, in terms of data stored (grey) and data generated by the IA model (green). Assuming the storage of 2% of the generated data [1], with data from [2].

of a system's power consumption [3]. The use of fast (∼GHz) volatile memory not only consumes power but heats up considerably. In server farms, more than 42% of the grid power is used for cooling [4]. The use of Non-Volatile Memory (NVM) in servers has

been proposed as a solution to mitigate the power consumption, as such technology is refresh-free and does not require a continuous power supply. Nevertheless, the most adopted (and cheapest) non-volatile technology is Flash memory, which does not provide the speed required to replace the working memory and has limited endurance [5].

For long-term storage applications, memory speed and access latency are not a problem, and magnetic hard drives (HDD) are still the solution of choice for their large capacity (>10 TB per drive) and reduced cost-per-bit (∼0.015 $/GB) [2]. However, servers need to constantly store and retrieve recent data to process. A *miss* in the DRAM triggers a *fetch* in the slower mass memory, and this data transfer bottleneck is inherent in the Von-Neumann computing system's architecture (**Fig. 3**). A simple example can be seen in the comparison of the clock period of an average CPU (0.25 ns) to the latency of an external DRAM bank (∼20 ns). To mitigate this issue, additional memory technologies were proposed to act as Storage Class Memory (SCM), that is, a buffer between main and working memory [6]. A viable SCM technology should provide low latency, high capacity, reduced cost, and ease of integration into preexisting systems. A well-recognized example of this technology is the Intel 3D XPoint™ accelerator [7], an innovative technical solution that did not succeed in the long run and was subsequently discontinued in 2020, probably due to a lack of competition and the elevated cost for the user (discussed in Chapter 6).

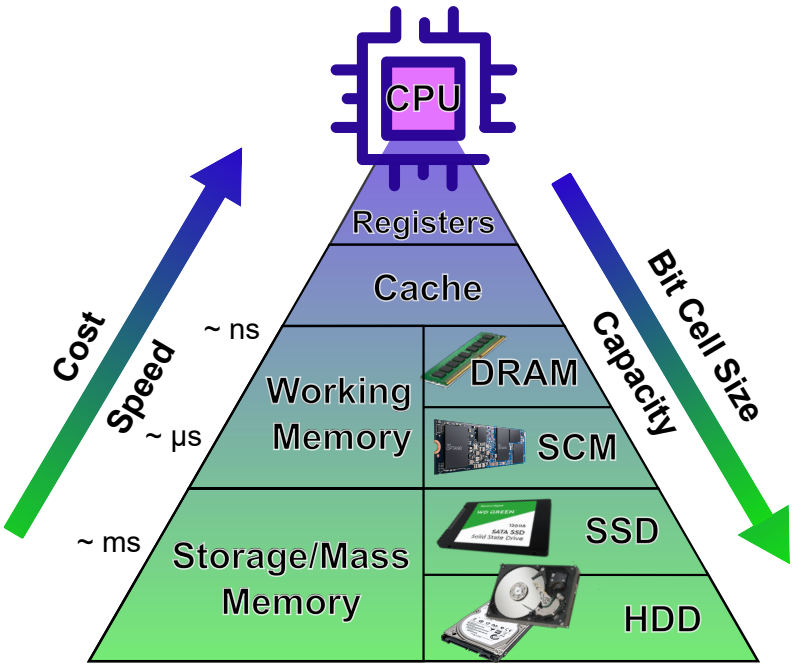


Figure 3: Memory hierarchy in Von-Neumann computing systems. Moving farther away from the CPU, the data transfer latency increases, but so does the capacity, with a corresponding reduction in the cost per bit ($/bit). Both embedded and computing systems share the same architecture; the technology shown on the right side of the pyramid is an example of a personal computer or data center application.

Following the previous discussion, the fast computing speed of processors is unmatched by memory devices or the data transfer bottleneck. To address all these issues simultaneously, considerable research has focused on performing computations directly in memory (In-Memory Computing or IMC) or physically close to it (Near-Memory Computing or NMC). Taking AI as an example, IMC enables performing operations such as updating a model's weights and inference within the memory itself, without the need to transfer information back and forth. Operations like Matrix Vector Multiplication (MVM) or Multiply and Accumulate (MAC) would be performed in parallel on whole memory macro modules, directly updating the bitcell with the new values. While this new paradigm could be applied to existing technologies like SRAM [8], it could benefit from emerging devices and circuits specifically designed for this new approach. Preliminary works on a mixed analog/digital accelerator fabricated with emerging memory devices have shown promising results, with a reduction in latency and energy consumption per operation [9].

Memory is essential in any IoT application, given the constant increase in edge devices generating enormous amounts of data that are essential for further analysis and exploitation. An endpoint device generally transmits raw or slightly processed data to an upper node (e.g., a smartphone, computer, or server) for computations, which increases data transfer, affects energy consumption, and increases latency. Moreover, security is becoming a major concern; depending on the application, the transmitted data should not include sensitive information [10]. Edge computing should be performed with low power and locally within the sensor or microcontroller; emerging memories play a major role, providing nonvolatility and native AI acceleration.

Thesis Objectives

The research presented in this manuscript addresses the critical challenges related to the co-integration of PCM and OTS targeting Crossbar array applications. This research aims to fill the existing literature gap between individual memory and selector elements and OTS+PCM 1S1R cells' reliability and performance. The thesis pursues three interconnected objectives, presented in a sequential progression from fundamental device physics to practical array implementation. The first objective is to validate and characterize a 1S1R OTS+PCM cell with a series transistor, thereby establishing a robust foundation for understanding device behavior at the physical level. The second objective is to conduct a comprehensive reliability and failure analysis for programming and reading operations, thoroughly assessing the factors that affect the long-term stability and performance of the cells. Finally, the third objective focuses on material optimization for both PCM and OTS, so that enhanced device characteristics and overall array performance are achieved through strategic material improvements. The manuscript concludes with a one-selector

one-resistor (1S1R) array demonstration.

The first objective focuses on the fabrication and validation of 1S1R utilizing a novel Double-Patterned Self-Aligned (DPSA) architecture. The details on the device design and fabrication are described in Chapter 2, followed by the electrical and physical characterization methods used throughout this work. Devices with multiple critical dimensions ranging from 40 nm to 300 nm were integrated and evaluated (Section 2.4). The electrical characterization protocols are described, with details of the 16 kb matrix configuration, enabling statistical evaluation of programming and threshold voltage distributions (Section 2.5).

Upon validation, I focus on the electrical performance of 1S1R OTS+PCM cells providing a comprehensive programming optimization using $Ge_2Sb_2Te_5$ PCM with GeSbSeN (GSSN) OTS (Chapter 3). A systematic analysis of SET and RESET programming statistics across multiple device dimensions and operating conditions is presented. The SET and RESET threshold voltages are described in terms of their distributions to justify the use of either Gaussian or Weibull models. The programming reliability is presented, including an endurance test to quantify and model the evolution of the V_{th} to identify the failure mechanisms specific to the DPSA architecture (Section 3.4). The impact of the thermal properties during programming at aggressive scaling dimensions is investigated by means of electrical characterization supported by TEM images and thermoelectric TCAD simulations (Section 3.5).

The reliability and failure analysis of reading operations is carried out in Chapter 4. In this work, for the first time to my knowledge, the effects of switching during reading operation induce a shift of the V_{th} in 1S1R OTS+PCM cells. The impact is attributed to both selector switching and reading current, confirmed by repeating the characterization for 1S and 1R cells individually. An empirical model is developed to describe the reading-induced threshold voltage shifts in 1S1R configurations (Section 4.3.1). The model captures the effects of repeated switching, as well as current and relaxation time. The model, and more generally the protocols, provides a tool for memory array design and optimization, allowing the prediction of bit-flip failures and suggesting possible mitigation paths (Section 4.3.2).

Chapter 5 is devoted to material optimization, with a core focus on the role of the Sb/Te ratio in GeSbTe-based PCM alloys. This investigation enables improvements in device performance, including speed and endurance, thereby overcoming the limitations arising from the thermal confinement described in Chapter 3. The congruent compositions with a higher Sb/Te ratio achieve sub-100 ns SET speed with high endurance and wide resistance window, representing a significant improvement from previously reported solutions, and a starting point for further material engineering (Section 5.1). Additionally, the optimized PCM material is integrated with OTS, providing a larger threshold voltage

window of about 2 V, and achieving a reliable SET operation thanks to the improved PCM crystallization kinetics (Section 5.4). The optimized material combination overcomes the SET speed limitations seen for standard $Ge_2Sb_2Te_5$, providing a clear material-oriented solution for downscaled and high-density applications.

The concluding Chapter 6 culminates in the demonstration of a functional 1 kb Cross-bar array, validating the transition from matrices of individual devices towards a practical array implementation of the OTS+PCM cell, leveraging all the previously reported results. The chapter focuses on the new challenges coming from the architecture, which complexify the analysis and require a new approach to overcome the technology limitations (Section 6.1) This demonstration concludes this work and opens the way for future perspectives and paths for the development of OTS+PCM technology. In particular, I present some preliminary results on the memory effect on OTS selectors, as candidates for Selector-Only Memory (SOM) applications (Section 6.2). This new path offers a perspective to surpass the classical 1S1R cell, aligning well with the direction the scientific community has taken over the last couple of years.

Chapter 1

Phase-Change Memory and Ovonic Threshold Switching Selectors

1.1 Emerging Memory and Selector Technologies

1.1.1 Emerging NVMs

The aforementioned shift in the computing paradigm for both standalone and embedded systems is driving research to develop and improve emerging nonvolatile memory technologies. A few of them are currently deployed in commercial products and are well described in the literature, making the adjective *emerging* not entirely accurate. The three most mature memory technologies are Phase-Change Memory (PCM), Resistive Memory (ReRAM), and Magnetic Memory (STT-MRAM), while other technologies, such as Ferroelectric Memory (FeRAM), are still in early development [11]. Reducing bitcell size is crucial for achieving high-density arrays, while reducing operating voltages makes MRAM and ReRAM particularly suitable for low-power embedded memory applications. Depending on the target application, each technology excels in specific performance metrics; a comparison in **Table 1.1** highlights the differences. All three technologies achieve high programming speeds with reduced energy consumption. For standalone applications that require high data transfer and updates, MRAM offers the best endurance. On the other hand, PCM provides the best data retention at high temperatures, making it suitable for automotive applications that require reliability in harsh environments.

Phase-Change Memory

Phase-Change Memory (PCM or PCRAM) is the most mature among emerging memory technologies and has been deployed in commercial products since the '80s. PCM

	MRAM	ReRAM	PCM
Voltages	**0.8 V**	1.5 V	3.5 V
Bitcell area	**0.019 μm^2**	0.025 μm^2	**0.019 μm^2**
Writing Speed	50 ns	**∼20 ns**	**∼20 ns**
Energy	12 pJ	**∼1 pJ**	∼10 pJ
Retention	10 yrs	10 yrs	**>10 yrs @160 °C**
Multilevels	2	2048	Analog*

Table 1.1: Performance benchmark comparing the three most mature emerging non-volatile memory technologies: MRAM, ReRAM, and PCM. Data from [11, 12]. * PCM provides an analog programming characteristic; an example application used a 12-bit ADC to read the PCM resistance value [9].

is particularly appealing due to its scalability, low power consumption, high speed, and multi-level capabilities. PCM exploits the reversible phase transition between a highly resistive amorphous phase and a low-resistive crystalline phase. A current pulse during programming is used to increase the temperature in the memory cell and induce a controlled phase transition. The most commonly used phase-change materials are based on chalcogenide glasses, typically the GeSbTe ternary compounds.

Resistive Memory

Resistive memories (RRAM or ReRAM) are fabricated with a simple Metal-Insulator-Metal (MIM) structure. The technology offers several compelling advantages, including low operating power, excellent scalability, and reduced fabrication costs associated with its simple CMOS-compatible structure. ReRAM is attractive for high-density applications, but suffers from high intrinsic stochasticity and nonlinearity, which are detrimental for storage applications. However, it could be exploited for neuromorphic computing, cryptography, or random number generation (RNG). The memory operation relies on the controllable formation and dissolution of a conductive filament, achieved through field-induced electrochemical movement of oxygen vacancies in the oxide insulating layer. ReRAM demonstrations based on hafnium oxide (HfO2) showed high-speed operation, large ON/OFF resistance ratios, and endurance compatible with flash memory [13].

Magnetic Memory

Spin-Transfer Torque Magnetic RAM (STT-MRAM) technology is based on a Magnetic Tunnel Junction (MTJ) consisting of two ferromagnetic layers separated by a thin dielectric tunnel barrier. This technology offers exceptional endurance and ultra-fast switching speed [13], but it suffers from high write energy, susceptibility to external magnetic fields, and complex integration, requiring multiple ferromagnetic layers. The memory exploits the Tunnel Magnetoresistance (TMR) effect, in which the stack resistance depends on

the relative alignment of the magnetic induction in the two ferromagnetic layers: low resistance for parallel orientation and high resistance for antiparallel orientation. One of the two layers serves as a reference with a fixed ferromagnetic orientation, while the free layer's magnetic orientation can be programmed by magnetic torque induced by the device's current. Other types of magnetic memories are being investigated, such as the Spin-Orbit Torque MRAM (SOT-MRAM), which involves a more complex device stack and is still under investigation, but has provided promising preliminary results [14].

Ferroelectric Memory

Ferroelectric RAM (FeRAM) uses the polarization of ferroelectric materials to store information. FeRAM offers high-speed operation and low voltages, with promising scalability, making it well-suited for applications that require high speed and endurance, such as DRAM replacement. However, FeRAMs are still struggling with 3D integration compatibility and low-temperature data retention, remaining at an early development stage far from commercial application [15, 16]. Ferroelectric materials, such as the emerging hafnium oxide (HfO2), exhibit ferroelectric polarization that can be programmed by the application of a suitable electric field. A ferroelectric stack can replace the floating gate of a transistor (FeFET) to modulate the threshold voltage, similar to Flash, but without charge trapping. Ferroelectric materials can also be used to fabricate capacitors in 1T1C cells, where the transient current depends on the ferroelectric layer's polarization state.

1.1.2 Selector Devices

The implementation of emerging nonvolatile memories in high-density crosspoint arrays requires selector devices to enable precise addressing while preventing unintended disturbances to non-selected cells. These selector devices must exhibit highly nonlinear current-voltage characteristics to suppress sneak-path currents while delivering sufficient current for memory programming operations. The selector device of choice should also provide significantly higher endurance than the memory itself, as it must withstand prolonged read operations. A CMOS or FinFET transistor is usually the selector of choice, allowing the individual selection of a bitcell in a large array; alternative three-terminal selectors proposed include BJT [17]. A transistor requires a large area, especially to provide the currents required to operate the memory cell. For this reason, research is focusing on two-terminal switching selectors that could be integrated in series with the memory. Among the available selectors, a few are promising for their high current density, selectivity, endurance, and the possibility of integrating them into 3D architectures. A comparison table among silicon-based, oxide, ovonic, and ionic-electronic selectors is presented in **Table 1.2**, highlighting the benefits of each technology.

	Si-based	Ox-based	MIEC	OTS
J_{ON} (MA cm^{-2})	10	<1	10	>10-100
ON/OFF Selectivity	$>10^6$	$>10^4$	$>10^6$	$>10^6$
Bidirectional	No	No, possible by barrier tuning	Yes	Yes
3D Integration	Possible	Yes	Yes	Yes
Endurance	-	-	10^8	$>10^{11}$

Table 1.2: Performance comparison of two-terminal selector elements, data from [18, 19].

Silicon-Based Selector

Silicon-based selectors leverage knowledge of semiconductor manufacturing and well-understood device physics, with perfectly CMOS-compatible integration. However, their implementation with 3D memory is challenging due to the limited thermal budget and vertical integration capabilities, especially in the Back End Of Line (BEOL) of fabrication. In particular, polysilicon diodes often exceed the BEOL thermal budget, and at lower process temperatures, their quality is challenging. Vertical PN junction diodes utilize epitaxial growth techniques to fabricate a stack capable of achieving the high current density required by emerging memories; however, thermal treatment for dopant activation is incompatible with the BEOL [18].

Oxide-Based Selector

Oxide-based selectors can be easily fabricated at low temperatures, which are compatible with the BEOL. However, they often provide limited maximum current densities, which are unable to meet the requirements of ReRAM and PCM. Metal-oxide Schottky barriers can be tuned to produce asymmetric barrier heights with a strongly nonlinear characteristic, resulting in large ON/OFF current ratios [18].

Ovonic Threshold Switching Selector

Two-terminal Ovonic selectors have found their way into multiple applications, combined with ReRAM, PCM, and Ferroelectric memory [20, 21]. They exploit a volatile field-induced resistance change in chalcogenide-based glasses without inducing a phase transition, unlike PCM. The OTS selector has enabled the commercial deployment of PCM on a large-scale manufacturing with the 3D XPoint technology [22]. OTS selectors provide

large current densities (>10-100 MA cm^{-2}), high ON/OFF current ratio ($\geq 10^6$), extended endurance and picosecond switching speed [23, 24].

Mixed Ionic-Electronic Conduction Selector

Mixed Ionic-Electronic Conduction (MIEC) selectors utilize copper-doped materials, where both electron and ion movement contribute to the total conduction, resulting in a highly nonlinear characteristic suitable for memory applications. MIEC selectors demonstrate excellent scalability and functionality in large arrays [18]. However, turn-off times after operation strongly limit the operating speed.

1.1.3 Current State of the Art of PCM and OTS

From the proposed memory and selector technologies presented in Table 1.1 and 1.2, PCM and OTS demonstrated good performance in commercial products and are promising for the future of NVMs. Phase-Change Memory has evolved from a switching chalcogenide material to a compelling memory for storage-class and in-memory computing applications [6]. Since the discovery of the threshold switching phenomenon by Stanford Ovshinsky in 1968 [25], modern understanding frames and models OTS conduction and threshold switching, and provides fundamental insight into the phase-change mechanism in PCM. **Fig. 1.1** provides a timeline of the history of both selector and memory elements [11, 26–28].

Already in 1971, the first PCM array was developed, demonstrating the promising functionality of the technology. Due to Flash memory's faster scaling and development, PCM was primarily investigated and implemented in optical storage media, such as rewritable CDs and DVDs. The optical era of PCM dominated the 90s. During this decade, PCM technology gained widespread use in optical storage media, such as CDs and DVDs, laying the groundwork for subsequent advances in solid-state applications. Over the following two decades, the potential benefits of solid-state, nonvolatile memory to enhance Flash technology came back into focus. This resurgence of interest in PCM coincided with the publication of the first articles on PCM matrices and OTS+PCM Crossbar arrays, which appeared before 2010. This progress laid the groundwork for the 2009 introduction of the OTS+PCM 1S1R Crossbar architecture [22]. This pivotal innovation eventually came to market in 2015 as the 3D XPoint array, marking a significant milestone in the commercial deployment of PCM. Recent years have seen further development of PCM for both embedded and automotive applications on one hand [17, 31, 32], and standalone applications on the other. In particular, PCM has been proposed for in-memory computing or AI applications, with good preliminary demonstrations [9, 33]. Since 2021, a memory effect in the OTS selector has been discovered, sparking significant scientific activity around the concept of a chalcogenide-based Self-Selecting Memory

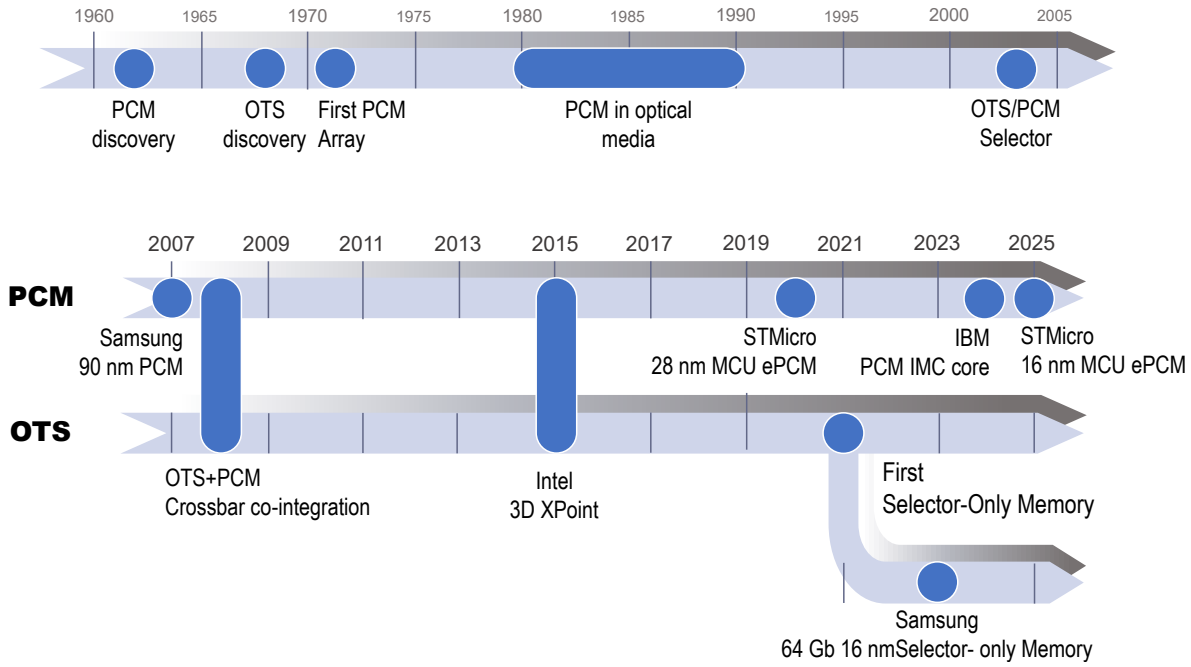


Figure 1.1: History timeline of the major PCM and OTS advancements, from the discovery of the phenomenon to recent commercial products. The second line details the individual evolution of both PCM and OTS, with the recent discovery of the Selector-Only Memory effects in 2021 [11, 26–30].

(SSM) [34]. This memory effect in the OTS selector is characterized by its ability to retain a state even after power is turned off, a phenomenon not typically observed in conventional OTS devices. This discovery introduces potential for OTS devices to be used not only for switching but also for data storage. The implications of this are significant, as it could lead to the development of more compact and energy-efficient non-volatile memory architectures, while also facilitating faster data access speeds and reduced power consumption. While the idea of a memory element with selector capabilities is not new [35], the mechanism behind the OTS-based memory does not exploit a phase change and remains to be fully understood. While the literature on the subject is still limited, some prototypes are currently being investigated [30], as this technology could play a major role in the future, as proposed in the perspectives of this work (Chapter 6).

The current OTS+PCM state of the art features a few key players proposing advanced memory solutions. **Table 1.3** compares the performance of three major crossbar references based on PCM technology. For reference, we report the performance reported by previous studies at CEA-Leti for single devices to situate our work in the current Crossbar landscape. The current trends revolve around reducing device size and latency, and improving endurance and data retention for storage-type applications.

Besides economics and market positioning, the OTS+PCM technology faces several

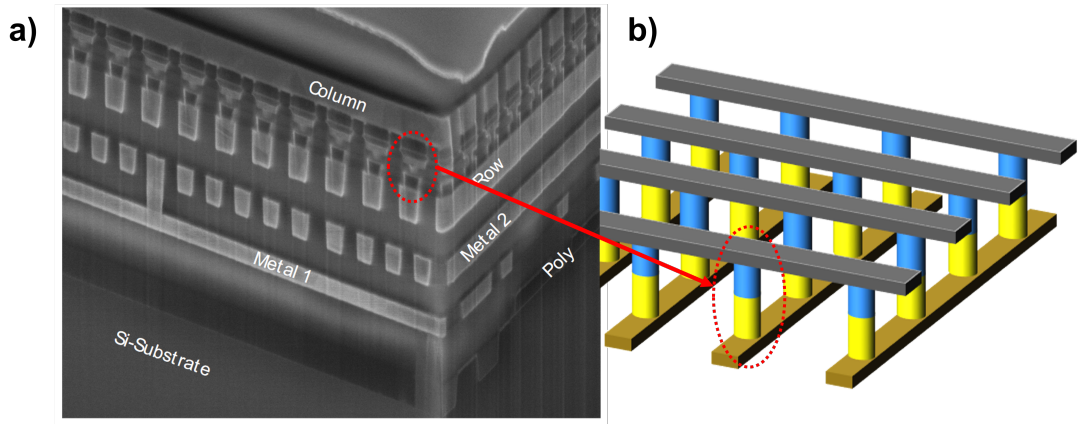


Figure 1.2: a) TEM image of a 3D XPoint array, highlighting one single bit in red. b) schematic representation of the array with perpendicular metal lines with bits at each intersection. Reprinted from [22].

	Intel 3D XPoint™ [22, 36]	IBM/Macronix [12, 37]	TSMC [38]	CEA-Leti * [39]
Array size	64 Gb	N/A	1 Mb	Single device
Selector device	OTS	OTS	Transistor	OTS
Structure type	Pillar	Pillar	Plug	Heater
Switching voltage	N/A	<4 V	<3 V	<4 V
Write speed	500 ns	10 ns	100 ns	2 µs
Read speed	100 ns	10 ns	100 ns	300 ns
Write/read endurance	10^8	10^9	$2{\cdot}10^5$	10^9
Data retention	7 years @40 °C	N/A	10 years @120 °C	N/A

Table 1.3: Current state of the art of PCM-based crossbar array demonstrations, with data from [12, 22, 36–38]. * Previous results obtained at CEA-Leti for OTS-PCM on a single-device level are reported as a reference [39].

roadblocks that hinder development and undermine scalability. The PCM devices require relatively high programming energies (i.e., more than 10 pJ per bit), which could pose an issue for IoT embedded systems. On the other end of the spectrum, standalone memory must keep adequate speed and endurance level at aggressive technology nodes. Novel materials must be investigated to enhance the thermal and electrical properties, thereby overcoming device-level constraints. OTS selector cells suffer from leakage, which limits the maximum macro array size achievable; nonlinearity and drift contribute to global device variability. As for PCM, endurance is a core issue as modern memories must provide extensive cycling capabilities.

Moving to an array and system-level view, classical issues such as IR drop and thermal

crosstalk need to be investigated, accounting for the specificity of this technology. Sensing and driving circuits must be designed with consideration for both application and technology constraints. The inherent variability associated with devices based on amorphous materials can pose significant challenges for digital applications, where precision and predictability are crucial. However, in analog applications, the same stochastic properties may prove advantageous. The variability and randomness inherent in amorphous materials can be harnessed to create adaptive systems that benefit from noise and variability, particularly in applications such as neural networks, random number generation, and other analog computing systems [33, 40].

1.2 Phase-Change Memory Physics

As briefly discussed above, phase-change materials exploit the high resistance and optical contrast between crystalline and amorphous phases to encode information. In solid-state electrical PCM, the phase transition is induced by a suitable current pulse. The high-resistance amorphous phase represents the logical state "0", while the low-resistance crystalline state represents the logical "1". The PCM operation typically involves a reduced active volume within the cell, which is responsible for the phase transition. The PCM device essentially consists of a phase-change material sandwiched between two metal electrodes; the temperature increase generated through Joule heating allows for either melting or quenching of the active region, or induces thermally activated crystallization. The chalcogenide materials used for PCM are compounds containing at least one chalcogen group element (Group VI) of the periodic table, usually alloyed with Groups IV and V elements like As, Sb, and Ge. These materials form peculiar *metavalent* bonds which differ in electron delocalization and resistivity properties between the two phases. Metavalent bonding is characterized by the delocalization of electrons across multiple atoms, resulting in a balance between covalent and metallic characteristics. This is crucial for PCM, as it affects the material's ability to switch between phases rapidly. The study of metavalent bond-forming compositions provides useful insight into candidate phase-change alloys [41, 42].

1.2.1 Devices Physics

The working principle of a PCM cell is depicted in **Fig. 1.3**. The represented cell is composed of a crystalline phase-change chalcogenide layer integrated between a narrow resistive metal electrode and a larger top metal electrode. Applying a suitable voltage pulse induces a current in the device; the heat generated by the resistive electrode (also referred to as the heater) is controlled to program the cell. Depending on the resulting temperature profile, the cell will end up in different states: first, a sharp and short tem-

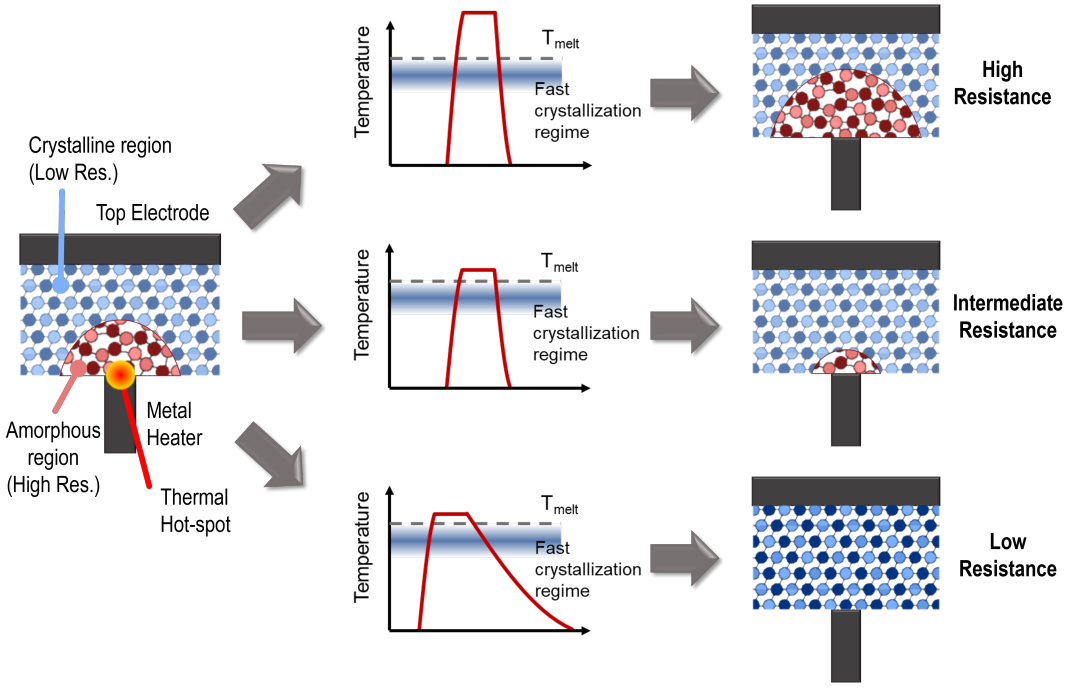


Figure 1.3: The Phase-Change Memory working principle of a cell with a narrow "heater" bottom electrode. Depending on the applied temperature profile, the cell can be reprogrammed under multiple conditions, each characterized by a different resistance value due to the varying amount of amorphous material obtained during the programming. Adapted from [43].

perature spike will melt a portion of the phase-change material; then, the rapid cool down will quench the melted region, freezing the element in an amorphous state (Fig. 1.3 top). By reducing the current (hence the temperature), the size of the amorphous dome close to the heater reduces (Fig. 1.3 middle); if the temperature is kept in the crystallization range, or if the active region is melted and slowly cooled, the device crystallizes (Fig. 1.3 bottom). To achieve programming, the temperature in the active region should exceed T_{melt} (e.g., 630 °C for $Ge_2Sb_2Te_5$); higher temperatures increase the size of the melted dome. The programming curve of a PCM is shown in **Fig. 1.4b** where the resistance measured at low voltage is reported as a function of the pulse programming current. Within a suitable range, the programming current promotes crystallization, resulting in a reduction of resistance; for higher currents, amorphization occurs.

SET State

The crystalline state (SET state) can, in principle, be achieved by heating the cell below its melting temperature but above its crystallization temperature (T_x), inducing a solid-to-solid phase transition [44]. In PCM, this is not usually the case, as the programming current will, in general, melt the active region; crystallization is then achieved by providing a suitable pulse fall time that will help crystal growth [45, R2]. The programming speed

of a PCM is usually determined by the SET speed, which depends on material properties and cell design considerations. Crystallization occurs through crystallite nucleation and growth from existing crystals. In materials like $Ge_2Sb_2Te_5$, growth speed is usually larger, and the crystals propagate from outside the active region down to the heater element [46]. A detailed investigation on the SET speed in relation to material properties is carried out in Chapter 5 while the impact of the cell design and lateral dimension is described in Chapter 3.

In the crystalline SET state, the phase-changing material exhibits quasi-metallic behavior, characterized by relatively low electrical resistivity. In the case of $Ge_2Sb_2Te_5$, the fcc crystalline phase behaves as a p-type semiconductor with a Fermi level close to the valence band, while the most thermodynamically stable hexagonal phase behaves like a degenerate p-type semiconductor with a Fermi level within the valence band [29]. This results in a nearly ohmic behavior under normal operating conditions.

RESET State

The amorphous RESET state exhibits a more complex electrical characteristic, due to the disordered nature of the chalcogenide glass. Counduction in the RESET state is characterized by a highly nonlinear characteristic (**Fig. 1.4a**). The amorphous structure contains numerous structural defects, including dangling bonds and distorted bonds, which arise from the disordered atomic arrangement. These defects create numerous localized states within the bandgap, leading to band tails within the bandgap. Conduction in this type of glass can be well described by the Poole-Frenkel mechanism, in which carriers hop from one localized defect to the next, under the force of the applied electric field. The electrical conduction in the amorphous phase is thermally activated, due to the trap barrier lowering for increasing temperatures, following an Arrhenius-like relationship [47, 48].

Threshold Switching

Threshold switching is a fundamental and critical phenomenon that enables PCM operation by allowing a large current flow, accompanied by a corresponding temperature increase within the device. This electronic switching effect occurs in the amorphous phase-change material upon the application of a critical threshold electric field (E_{th}). Threshold switching is essential for generating the high current densities required for memory switching at sufficiently low voltages in a material that is not highly resistive.

When the voltage applied to the amorphous PCM exceeds a threshold (V_{th}), the PCM exhibits a S-shaped negative differential resistance in the I–V characteristic (Fig. 1.4a). The device rapidly commutes to a low-resistance ON state through a voltage snapback [47, 49]. The large current flowing through the PCM can then induce crystallization, at the point where the two IV curves meet.

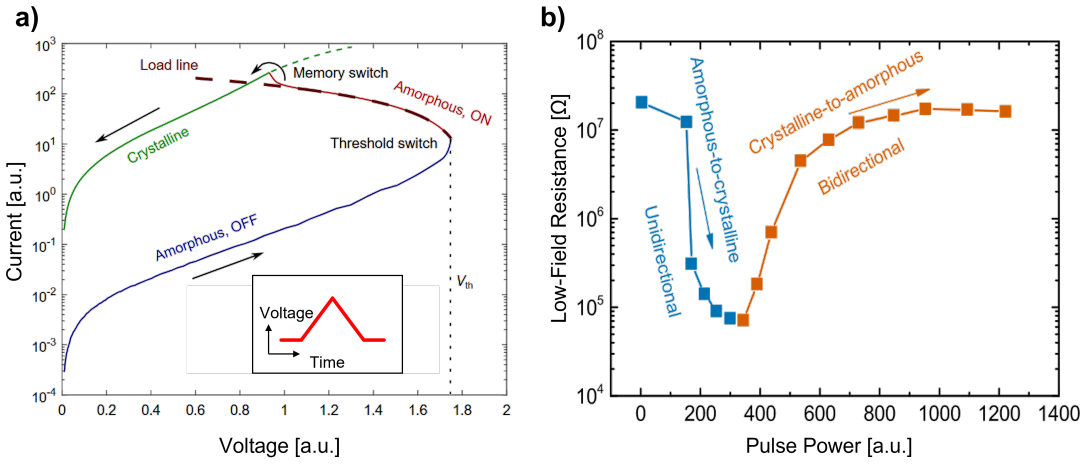


Figure 1.4: Typical quasistatic I–V characteristic of a PCM (a), and corresponding low-field resistance measured for increasing programming power (b). Adapted and reprinted from [43].

The threshold voltage of a standard PCM cell typically ranges from 0.5 to 2 V and increases with layer thickness, depending on the material composition. The threshold switch strongly depends on temperature, with lower V_{th} at higher temperatures.

Over the years, multiple physical explanations for the switching phenomenon were proposed. Thermal models, which attribute switching to a temperature-dependent conductivity and a positive feedback loop, are now being disregarded in favor of electronic models. The consensus today is on field-induced defect delocalization, forming a conductive path allowing current flow in the material layer [50]. This hypothesis fits well with experimental data and bridges the gap between purely electronic models [47] and field-induced nucleation models [49].

1.2.2 Phase-Change Materials

The primary materials used in PCM belong to the chalcogenide family, characterized by containing at least one chalcogen element (S, Se, Te), typically alloyed with elements from Groups IV (Ge, Sn) and V (Sb, As) [29]. The Ge-Sb-Te ternary system represents the most extensively studied and commercially implemented family of phase-change materials. Materials along the GeTe–Sb_2Te_3 pseudo-binary line have attracted particular attention due to the combination of fast programming speed and thermal stability [51].

$Ge_2Sb_2Te_5$ (GST225) is a well-known and explored composition, combining the high melting temperature (∼630 °C) and thermal stability of GeTe with the rapid crystallization kinetics of Sb_2Te_3 [29]. In this work, we will focus on $Ge_2Sb_2Te_5$ PCM for the OTS+PCM co-integration; in Chapter 5 we investigate the role of Sb/Te ratio tuning in GeSbTe alloys to improve the performance of standard $Ge_2Sb_2Te_5$.

An optimized Phase-Change Material must satisfy multiple requirements. They should provide fast crystallization for SET operation, in the order of nanoseconds, requiring materials capable of rapid crystalline growth [52]. Since the amorphous phase is a metastable state, it is essential that it remains highly resistive over long operating periods and at elevated temperatures to satisfy data retention needs for consumer (85°C) and automotive (165°C) applications [31]. If the amorphous phase undergoes unintended crystallization, it results in decreased resistance, leading to data loss as the stored information becomes compromised. Crystallization can occur due to thermal perturbations or prolonged exposure to high temperatures, thereby affecting the PCM's retention limits. As the data is encoded in the resistance state of the PCM, a high contrast between the SET and RESET states is required to achieve a large resistance memory window, with a resistance ratio in the order of 10^3–10^4.

Other requirements include cyclability, as the material should be able to change phase consistently without elemental segregation or loss of functionality. Finally, the material should retain these properties even when scaled down to aggressive lateral dimensions to remain competitive for future technology nodes.

Crystallization Kinetics

The crystallization kinetics of phase-change materials fundamentally determine device switching speed and reliability. Two primary mechanisms govern the crystallization process: crystal nucleation and growth. $Ge_2Sb_2Te_5$ and similar alloys are characterized by growth-dominated crystallization where the crystalline matrix surrounding the active region acts as a seed for homogenous crystallization. When most of the cell volume is amorphised, there are no crystals to grow from, hence nucleation must occur, usually on a longer timescale [53]. Compositions with increased antimony content exhibit a faster growth rate, which allows faster SET operation by rapidly growing a single or large grain crystal structures [51].

1.2.3 Cell Architectures

PCM cell architectures have evolved to address the fundamental challenge of minimizing programming current while maintaining a large window for device scalability and reliability. The primary design objective is to confine the active cell volume, thereby reducing the energy required to melt it. The microtrench cell architecture confines the PCM volume within a trench in the insulating material, which is in contact with the bottom electrode. A variation of this cell is the pillar structure (**Fig. 1.5a**) where the phase-change material is completely confined by a dielectric material; in this architecture, the resistance of the active layer itself provides the necessary heat required for phase transitions; for this reason, the phase-change material of choice should provide a sufficient ON resistance.

The plug architecture (Fig. 1.5b) represents the simplest and most widely implemented PCM cell design, characterized by a narrow bottom electrode constraining the current path, with larger phase-change and top electrode layers. The narrow bottom electrode has a higher current density, leading to an increase in temperature, which causes the cell's active volume to take the classic *mushroom* shape. An evolution of this cell structure is the "Wall" architecture (Fig. 1.5c), where the bottom electrode is thinned down to a few nanometers thick for a vertical contact. Moreover, the electrode resistance is increased to act as a heater element, capable of controlling the hot-spot position and temperature without relying on the phase-change material properties [17]. The "Wall" architecture for PCM is widely adopted throughout this work, and its design and fabrication are described in detail in Chapter 2.

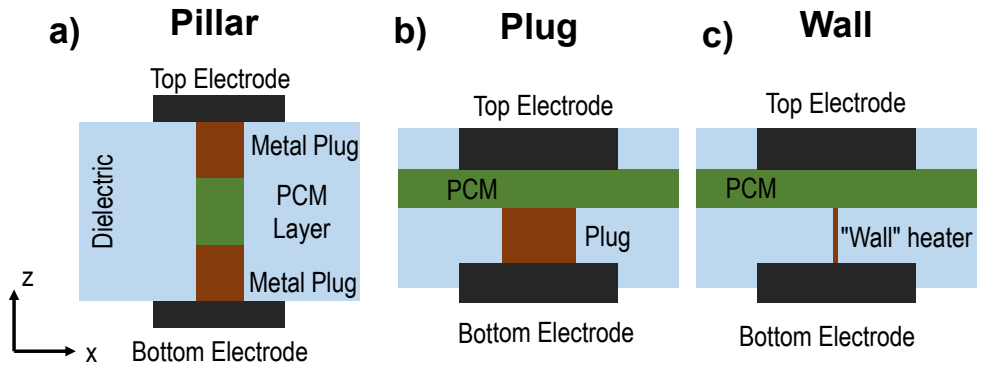


Figure 1.5: Schematic of different PCM cell designs: a) pillar structure; b) plug structure; c) wall structure, similar to the plug but characterized by a narrow resistive metal heater.

1.2.4 PCM Reliability

The reliability of PCM devices encompasses multiple physical mechanisms that can affect how data is stored and for how long. Typical memory reliability performance metrics include endurance, resistance drift, data retention, read and write disturbance, and stochasticity. Endurance refers to the number of program/erase cycles a device can withstand before failure. Resistance drift is an increase in the resistance of the amorphous (and crystalline, depending on the material) phase over time due to structural relaxation in the material. Data retention emphasizes the need for memory to maintain its state for a long time at elevated temperatures. Read and write disturbance involves unintended changes to the stored data during read or write operations. Stochasticity refers to random variations in memory behavior that can impact performance, for example, a large variability in the programmed resistance, which reduces the effective memory window. Understanding the physical origin of the mechanism behind critical reliability issues is essential for commercial viability and deployment of PCM. Some reliability metrics are

inherent in the PCM working principle and crucial to its functionality; they are:

Endurance

Endurance refers to the number of program/erase cycles a device can withstand before failure. This represents a critical reliability parameter to qualify a technology for the target application. In general, an endurance evaluation performs either SET and RESET programming to assess the target resistance throughout the lifetime, or high-energy RESET to induce early failures in accelerated testing.

Typical PCM failures involve either a stuck SET or RESET. A stuck SET is characterized by a gradual loss of RESET capability, in which the device cannot be programmed into the high-resistance amorphous state even with increased programming current. This failure mode is associated with the formation of short-circuit paths between the bottom and top electrodes caused by compositional changes in the layer, as a result of electromigration or elemental segregation that occurs during repeated thermal cycling.

A stuck RESET failure manifests as a sudden, irreversible increase in the device's resistance, typically much higher than in the typical RESET state. This failure mode is associated with void formation at the interfaces, particularly at the narrower bottom electrode, resulting in an electrical open circuit.

Repetitive cycling induces atomic migration driven by the electric field, thermal gradient, and high current density. The asymmetric structure of the pillar or wall architecture is subject to strong temperature and field gradients. Elements with large electronegativity are driven by the high local electric fields during programming, causing preferential migration of some elements. Similarly, the strong thermal gradient near the device hotspot induces thermophoretic motion of species, depending on their Soret coefficients. For instance, antimony in GeSbTe PCM has a strong negative Soret coefficient and tends to move toward the higher temperature points, especially thanks to the high atomic mobility of the liquid phase obtained during programming [54]. Therefore, the direction and magnitude of migration also depend on the programming polarity, as the aforementioned mechanisms can either add or cancel each other out.

Resistance Drift

Resistance drift is an increase in the resistance of the amorphous (and crystalline, depending on the material) phase. Resistance drift originates from structural relaxation in the phase-change material [55]. When the molten material is rapidly quenched during RESET operations, atomic configurations are frozen into a highly stressed non-equilibrium glass. Over time, this structure spontaneously relaxes toward a more stable configuration through local bonding rearrangements, defect annihilation, and reduction of traps.

The resistance drift follows a power-law relationship in time, where the drift exponential coefficients depend on the material [48].

Resistance drift has a strong impact on the memory window as it evolves over time. In multi-level storage, drift can cause separation between the as-programmed levels, potentially leading to read errors. The PCM threshold voltage is related to the amorphous state and exhibits the same drift phenomenon, increasing logarithmically over time. The PCM threshold voltage is extremely important for programming, as it determines the read window margin when co-integrated with a selector in 1S1R configurations.

The approaches developed to address resistance drift aim either to compensate for its impact on the reading operation or to reduce it. Resistance drift can be estimated and compensated using a reference cell or predictive programming [56]. Specific cell architectures aim to reduce the relative impact of the resistance drift, for example, by adding a resistive layer in series with the PCM to provide alternative current paths during reading [57].

Data Retention

The memory must retain the programmed state for a long time, even at temperatures higher than standard room temperature. For automotive applications, these requirements translate into 10 years of data retention at a constant 160 °C [31]. The PCM must remain amorphous, without any crystallization, to prevent data loss. The PCM is tested by measuring the programmed states after multiple baking cycles to accelerate data loss and to identify the technology's minimum viable retention time.

1.3 Ovonic Threshold Switching Selector Physics

Ovonic Threshold Switching (OTS) transition between a highly resistive (OFF) to a low-resistive (ON) state is a reversible electronic phenomenon in chalcogenide glasses, such as PCM [25]. Unlike PCM, Ovonic switching selectors fundamentally differ, as the switching is volatile and occurs without any crystallization process in the material. This is possible thanks to OTS materials, ranging from simple binary compositions to complex multi-element systems, remaining amorphous during operation with adequate thermal stability compatible with the BEOL processing temperatures (∼400 °C). When deployed as a selector, the OTS cell architecture affects its performance, specifically in terms of OFF current and threshold voltage (V_{th}), as well as introducing different reliability issues compared to the memory element.

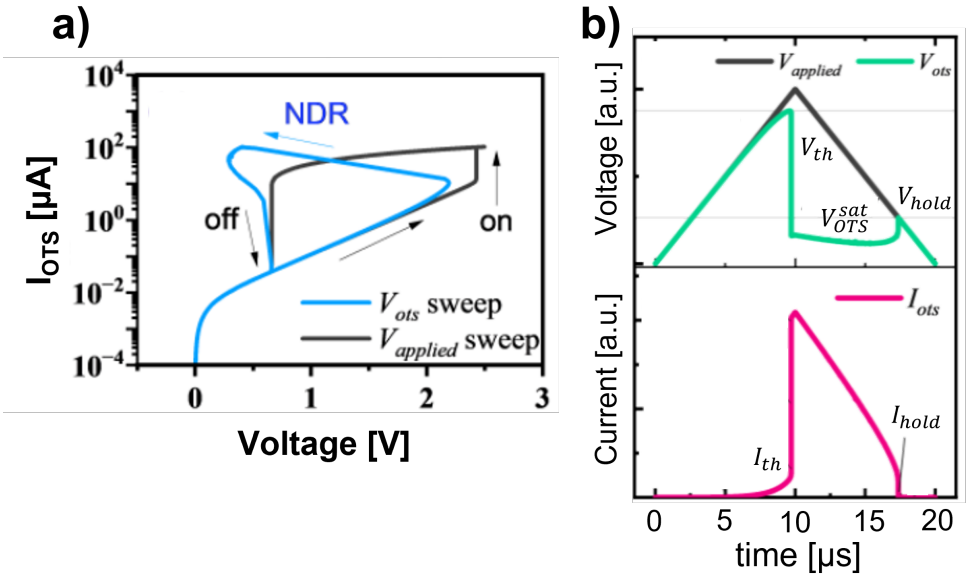


Figure 1.6: a) I–V quasistatic characteristic of an OTS, with the applied voltage in black and the voltage drop on the OTS in blue. b) Voltage and current profile over time, highlighting the applied bias and the voltage and current of the OTS. Reprinted from [58].

1.3.1 Devices Physics

The typical current-voltage (I–V) characteristic of an OTS device exhibits an S-shaped curve during quasistatic current-controlled measurements (**Fig. 1.6a**) [18]. This curve is similar to that observed in PCM (Fig. 1.4a) due to the similar materials and switching mechanisms in these two device categories. Initially, the device is in a highly resistive OFF state, with a low leakage current (typically below the nanoampere). Upon reaching a threshold voltage (V_{th}), the device rapidly transitions to a highly conductive ON state, capable of delivering very high current densities (more than 10 MAcm^{-2}) if not limited by a transistor or a suitable series resistor. The device maintains this conductive state as long as the current remains above a minimum holding current (I_h), below which it returns to the OFF state. Threshold switching is a fast phenomenon that occurs on a nanosecond timescale [24] and decreases with increasing applied voltage [18].

For applied bias above V_{th}, the OTS voltage drop is limited at a saturation voltage (V_{sat}) (Fig. 1.6b). When the current drops below I_h, with a corresponding holding voltage (V_{hold}), the device rapidly recovers its high-resistive state.

Switching Mechanism

The switching mechanism behind OTS is still subject to debate; in recent years, most theoretical models have converged on the hypothesis of an electric field-induced local rearrangement of atomic bonds, creating a temporary conductive path in the amorphous

matrix [50]. As for PCM, electronic transport in amorphous chalcogenide glasses is described by a Poole-Frenkel (PF) model [47]. When the electric fields approach the threshold, it lowers the conduction barrier height between neighbouring localized trap states. As the voltage increases, carriers acquire more energy to tunnel from trap to trap, resulting in an increase in overall mobility. At the same time, local bonds between atoms are distorted and tend to align; the structural change creates a low-resistive path for electrons without the need for atomic diffusion [50]. Both electronic and structural models converge to the same conclusions, the latter being supported by multiple ab initio molecular dynamics simulations [59]. This phenomenon is favored in materials that form metavalent bonds, exhibiting properties between metallic and covalent, with strong electron delocalization upon the application of an electric field [41]. Previous authors suggest a switching through the formation of a conductive crystalline filament within the amorphous matrix [49, 60, 61]. While this field-induced nucleation struggled to explain the volatile nature of the OTS switching and the ultrafast recovery, it provides an intuitive picture of what is happening inside the chalcogenide layer (**Fig. 1.7**). Local bonding rearrangements happen close to the bottom electrode, forming a conductive path (Fig. 1.7a). When a fixed voltage is applied between the two electrodes, the electric field is lower in the conductive region and higher in the amorphous region. This increase in the electric field provides an explosive positive feedback bridging the two electrodes, thus producing a fast switching event (Fig. 1.7b) [47, 58].

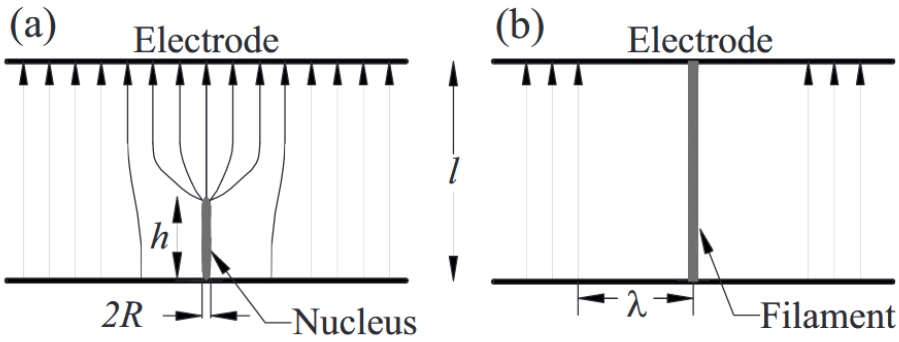


Figure 1.7: Simplified schematic of threshold switching in a chalcogenide layer, highlighting the filament creation (a), reducing the effective layer thickness and causing an increase in the electric field, leading to the fast formation of the conductive filament between the two electrodes (b). Reprinted from [61].

Electroforming

During the first operation, an OTS device requires an electroforming or "firing" step, happening at higher voltages (V_{fire}) than subsequent switching events. This *First Fire* (FF) step permanently modifies the material structure, and it is essential for achieving a

repeatable behavior. After switching at V_{fire}, the threshold voltage decreases back to V_{th} [62]. The forming operation can be understood as creating a network of active conduction paths within the amorphous matrix. During the forming process, traps and dangling bonds are redistributed and annihilated, resulting in slight atomic rearrangements without bulk crystallization. Upon the formation of a preferential conduction path, this will act as the site of further switching of the device, in coherence with the depiction of Fig. 1.7 [63]. The high voltages and currents during FF will also induce rapid heat generation in the active path, further favoring atomic mobility and lowering the bonding energy barrier [62].

Experimental evidence suggests that electroforming involves the formation of an active region characterized by changes in the local composition and structure of the amorphous material. TEM-EDX and X-ray spectroscopy revealed a different bonding distribution within the active region [64].

The first fire voltage is material-dependent as Se-rich compositions usually require higher firing voltages (3–5 V) due to a larger mobility gap distribution, while Te-based OTS forms at lower voltages (1–2 V). The forming, as with threshold switching, is both dependent on layer thickness and activated by temperature, with V_{fire} and V_{th} decreasing at higher temperatures [65].

1.3.2 Ovonic Materials

The development of OTS materials targets the requirement for a stable amorphous phase capable of withstanding repeated switching and generating current spikes at high temperatures within the conductive channel. An OTS material should provide adequate thermal stability for both high-temperature transient spikes and for Back End Of Line (BEOL) thermal budged and soldering reflow (i.e., more than 400 °C for 15 minutes) [66].

Selenium-based OTS materials, like the binary GeSe, represent the most thermally stable OTS category, with crystallization temperatures generally above 300 °C. Se-based OTS shows low leakage currents below the nanoampere and high endurance. However, pure GeSe systems suffer from high threshold voltages (i.e., above 3 V), and early degradation [67]. For this reason, alloying and doping are widely studied to improve device performance. Arsenic incorporation proved extremely effective in slowing down atomic mobility and improving material stability, while simultaneously reducing threshold voltages [68]. Research has focused on investigating safer compositions that avoid the use of hazardous elements. Nitrogen or Silicon doping reduces the number of germanium dangling bonds and widens the mobility gap [69, 70]. In our work, we widely adopt a state-of-the-art GeSbSeN (GSSN) OTS alloy, which demonstrated high endurance, thermal stability, and reduced threshold voltage in previous studies [69, 71, 72].

Pure tellurium exhibits some OTS properties, but has a low crystallization temper-

ature and a high subthreshold current (i.e., leakage) [73]. Binary and ternary Te-based compounds offer lower threshold voltages and high current densities. Systems like GeTe demonstrate fast switching speed and reasonable performance metrics, but still suffer modest thermal stability [74]. Also, for tellurides, multi-element doping proves essential to improve performance. Studies focus on silicon, carbon, or nitrogen doping to improve thermal stability and endurance while maintaining low threshold voltages, with promising demonstrations [24, 74, 75].

Sulfur-based materials exhibit exceptional thermal stability with low leakage currents. As for tellurides and selenides, sulfide compounds like GeS benefit from doping with nitrogen and arsenic to improve device performance, namely, reducing leakage current and improving endurance [76].

1.3.3 Cell Architectures

The OTS selector cell architecture uses a simple metal-insulator-metal (MIM) structure, with the chalcogenide layer sandwiched between inert metal electrodes. Electrode selection critically influences OTS performance through work function matching, interface contacts, and possible intermixing issues. Tungsten and Titanium Nitride (TiN) are the preferred materials due to thermal stability and CMOS compatibility. For our study, we use TiN electrodes with a carbon buffer layer to prevent possible diffusion of Ti into the chalcogenide layer [77].

The MIM cell structure is extremely scalable; downsizing reduces switching current and leakage, though device-to-device variability becomes more challenging at aggressive technology nodes. For memory applications, the OTS is integrated in series with the memresistive element in a one-selector one-resistor (1S1R) configuration. The co-integration requires careful consideration of voltage partitioning between the two. Particularly, the OTS contact area should be patterned and minimized to reduce leakage current and control threshold voltage variability [78]. We provide the details of the co-integration of the OTS and PCM in a novel Double-Patterned Self-Aligned (DPSA) cell in Section 2.4.

1.3.4 OTS Reliability

OTS reliability encompasses multiple degradation mechanisms limiting device performance. Some of these characteristics are unique to chalcogenide glasses and are similar to those reported for Phase-Change Materials. Understanding and mitigating selector-specific reliability issues is crucial for the development and implementation of this technology.

The impact of temperature and thermal stability is essential for devices that must survive the thermal budget of the BEOL and solder reflow. In some scenarios, such as

automotive applications, they should even be able to operate at higher temperatures and in harsh environments. As for memory, endurance is a critical reliability metric, as the selector is supposed to be virtually unaffected by read and write operations to ensure reliable, long-lasting memory. The issue of drift, similarly to what happens to PCM, has to be taken into account, as well as in the 1S1R configuration.

Thermal Stability

The bulk OTS must remain amorphous during device operation, and should withstand the BEOL thermal budget. Crystallization of the chalcogenide selector is the primary failure mechanism, as it becomes conductive without any threshold switching behavior. The material composition strongly influences thermal stability, with Se-based systems exhibiting greater stability [71].

The OTS electrical characteristic depends on temperature: subthreshold conduction is activated by higher temperature, resulting in a corresponding reduction in V_{th}. As leakage current depends on the operating temperature, the leakage current (I_{leak}) must be measured with the target operating temperatures in mind.

Endurance

OTS selectors experience gradual performance degradation over repeated switching cycles. The degradation stems from both the total power dissipated by the selector and the number of switching events. Programming operations are responsible for a high thermal stress induced in the OTS device due to the high power delivered. Therefore, programming will reduce the OTS lifetime, but even less energetic operations can degrade it. Even reading operations can induce early degradation if the current is not properly controlled during threshold switching. The details on the reliability of reading for OTS and OTS+PCM performance are provided in Chapter 4. State-of-the-art OTS materials demonstrate exceptional endurance under optimized conditions, with endurance ranging from 10^8 to 10^{11} cycles [79]. Further testing is still required to evaluate the device's performance in a real scenario, especially when co-integrated with a memory.

Threshold Voltage Drift

Chalcogenide materials evolve over time, leading to an increase in their resistance and threshold voltage. High temperatures or electric fields speed up this relaxation process, which can last from a few microseconds to a few hours. This large time range is critical, depending on the application, because drift must be accounted for when storing data for long periods. Drift is as critical for OTS as it is for PCM, as an increase in the threshold voltage can induce bit-flip soft errors. The impact of the threshold voltage of the OTS on the programming and reading of OTS+PCM is explored in Chapter 3, 4.

1.4 OTS+PCM Devices

WWhen PCM is co-integrated with the OTS, a low-field reading of the memory resistance is more difficult because of the selector's high resistance. In this configuration, the stack's threshold voltage results from the combined contributions of the selector and the memory, with V_{th} not exceeding the sum of the PCM threshold ($V_{th,PCM}$) and the OTS threshold ($V_{th,OTS}$). The actual switching voltage is typically lower because it is influenced by the voltage divider formed by the two series elements. **Fig. 1.8** presents the typical current-voltage (IV) characteristics of a one-transistor one-selector one-resistor (1T1S1R) cell in both SET and RESET states [37].

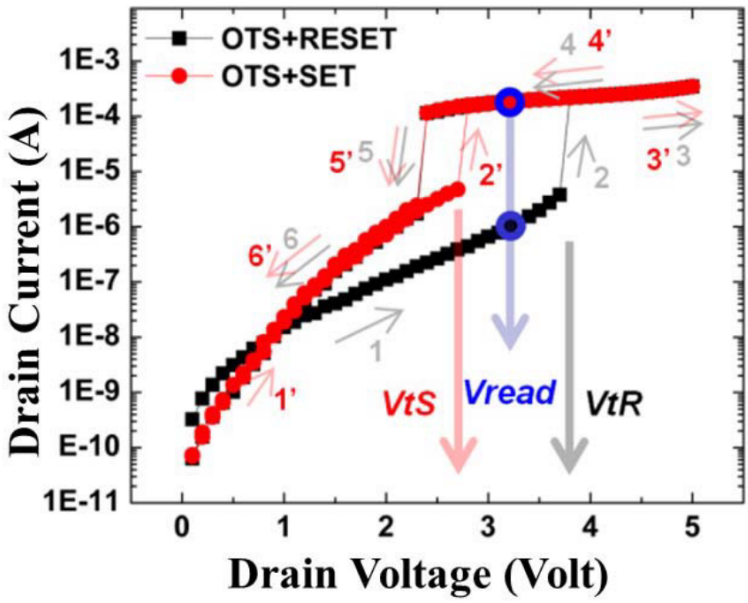


Figure 1.8: Typical IV curve of an OTS+PCM for a voltage ramp up and down: 1) subthreshold conduction for increasing voltage; 2) threshold switching; 3) ON state current saturated at the transistor compliance; 4) decreasing the voltage from the ON state; 5) when the voltage is lowered below holding condition the device switches OFF; 6) the device goes back to subthreshold conduction. Figure reproduced from [37].

The I–V curve is obtained by applying a quasistatic voltage ramp up and down, for both SET (red) and RESET (black) states. In the SET state, the PCM remains crystalline, and the threshold voltage is governed solely by the OTS (V_{SET}). In the RESET state, the PCM exhibits high resistance and contributes to the threshold, thereby increasing the total voltage required to switch the stack (V_{RESET}) [80]. The high current through the device in the ON state crystallizes the PCM, so the RESET curve coincides with the SET curve as the voltage decreases.

The IV curve in Fig. 1.8 illustrates a typical cell incorporating a series transistor for current limitation, as discussed further in Chapter 4. In this configuration, the maximum

current is restricted to a compliance value (i.e., 3 in Fig. 1.8). When the device is OFF, the OTS leakage current becomes the primary contributor to the total current (i.e., 6 in Fig. 1.8). The electrical test protocols for OTS+PCM characterization are detailed in Chapter 2, programming results are presented in Chapter 3, and the description and evaluation of the reading operation are provided in Chapter 4.

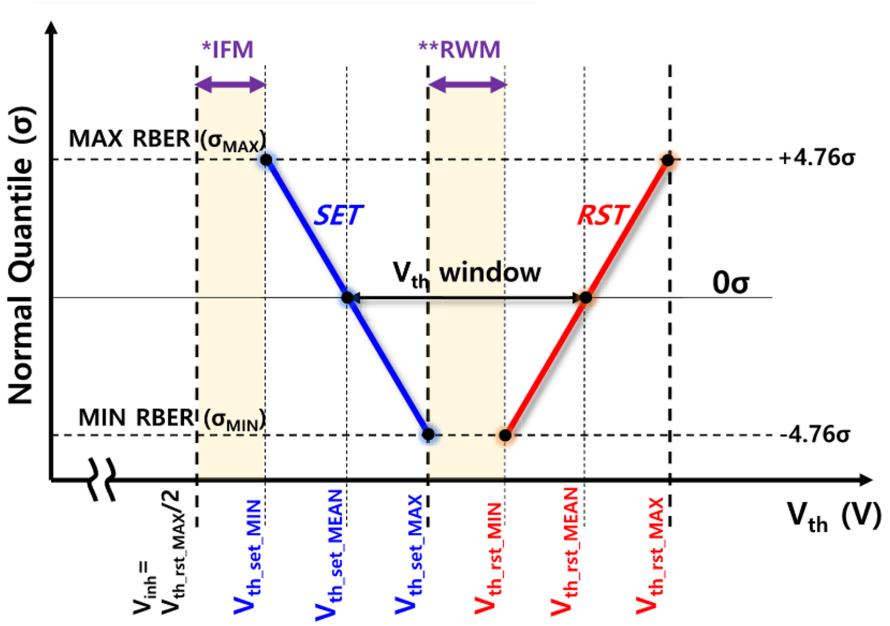


Figure 1.9: Key parameters in OTS+PCM Crossbar array design, the distance between the SET and RESET distribution tails is the Read Window Margin (RWM). In the Crossbar array, the half-selected cells are biased at half of the programming voltage, posing a limit to the maximum RESET V_{th} to obtain an Inhibit Fail Margin (IFM) greater than zero. Figure reproduced from [81].

In the Crossbar architecture, such as the one shown in Fig. 1.2, the selected device is biased to either the reading or programming voltage. To prevent devices on the same word line or bit line from switching unintentionally, a half-selected bias scheme is adopted. A typical bias scheme applies half the programming voltage to the half-selected cells [80]. The proportion between the PCM and OTS resistances and threshold voltages plays a major role in determining the maximum window achievable. **Fig. 1.9** reports the key parameters for Crossbar array design [81]. The SET and RESET distributions will determine the effective Read Window Margin (RWM), that is, the distance between the minimum RESET and maximum SET thresholds (Vth_rst_MIN - Vth_set_MAX), which is smaller than the mean V_{th} window. The programming voltage must exceed the maximum RESET V_{th} (Vth_rst_MAX) to switch and access the devices independently of their state. The application of a high voltage poses a critical issue for the half-selected cell, where an Inhibit Fail Margin (IFM) greater than zero is required. The Inhibit Fail Margin is the distance between the minimum SET voltage and half of the programming

voltage (Vth_set_MIN - Vth_rst_MAX/2). PCM and OTS designs should aim for a suitable combination of a resistive PCM with a large threshold voltage, in the same order of magnitude as the OTS, to maximize both RWM and IFM [82]. A detailed description of the Crossbar array working principle with data obtained by experimental characterization of the OTS+PCM devices is presented in Chapter 6.

Chapter 2

Materials and Characterization Methods

This chapter provides a comprehensive overview of the materials, device architectures, and characterization methodologies employed throughout this work. The chapter begins with a description of Phase-Change and Ovonic materials, comparing our material selection with previous research findings. Subsequently, device cell structures and architectures are presented, including both one-resistor (1R) PCM configurations in the Wall architecture and one-selector one-resistor (1S1R) Double-Patterned Self-Aligned (DPSA) structure combined with an OTS selector. The integration challenges associated with the DPSA architecture are outlined, along with the solutions adopted, supporting the advantages of this cell structure for OTS+PCM co-integration. The electrical characterization methods and test equipment are described, followed by comprehensive explanations of the test protocols developed to extract key PCM and OTS figures of merit and reliability metrics. Finally, a brief description of the TCAD simulation models deployed is provided.

2.1 Phase-Change Materials

The most extensively studied PCM alloy is the stoichiometric $Ge_2Sb_2Te_5$ (GST225), which was successfully adapted for electrical PCM devices, demonstrating wide resistance windows, sub-100 ns crystallization capability, and 10-year data retention at 110°C [83]. GST225 composition is illustrated in the Ge–Sb–Te ternary diagram of **Fig. 2.1**.

GST225 demonstrates nucleation-dominated behavior with a high nucleation rate but a low growth rate, which poses severe limitations to the maximum programming speed achievable, especially for highly scaled devices [46]. To address this fundamental limitation, we explored the role of antimony content in tuning electrical performance, implementing both bulk and multilayer materials.

The limitations of conventional GST225 for automotive and high-temperature appli-

cations drove the development of alternative compositions. Germanium-rich GST (GGST or Ge-rich GST) materials emerged as promising candidates for automotive-grade applications requiring enhanced thermal stability [44]. Systematic investigation revealed that Ge-rich compositions demonstrate higher crystallization temperatures exceeding 250 °C compared to 150 °C of GST225 [84, 85].

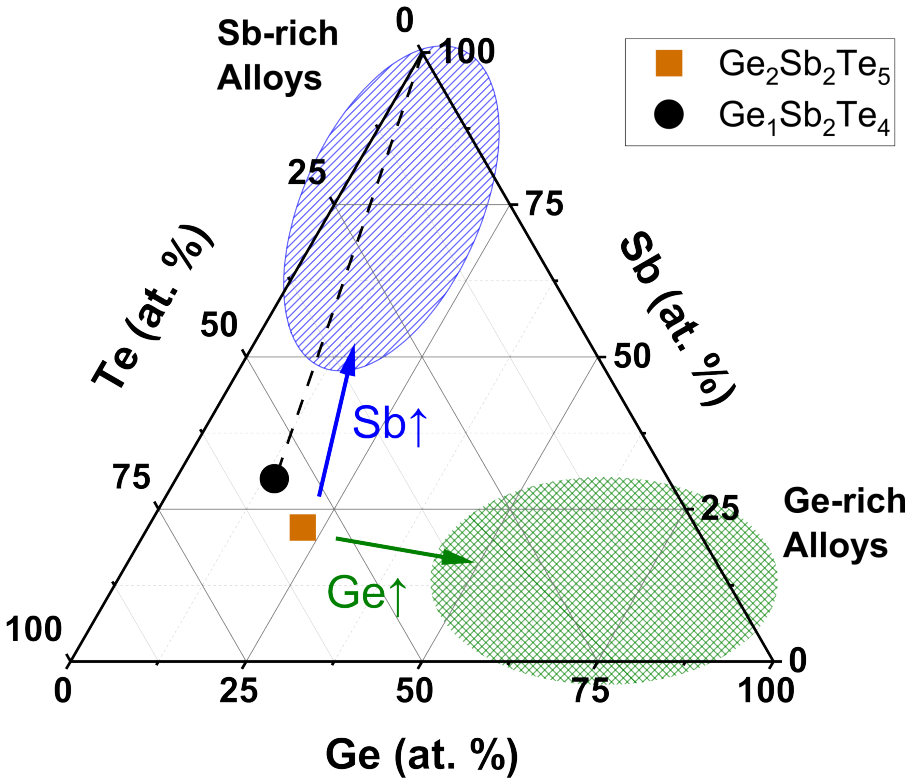


Figure 2.1: Ge–Sb–Te ternary diagram showing the compositions investigated in this work. $Ge_2Sb_2Te_5$ and $Ge_1Sb_2Te_4$ are marked as reference points. The Sb-rich region is highlighted in blue and the Ge-rich region in green, representing the compositional spaces explored.

GST225 Reference Material

Unless otherwise specified, our reference material is standard $Ge_2Sb_2Te_5$ (GST225). We integrate GST225 through monotarget low-temperature Physical Vapor Deposition (PVD) sputtering. The PCM cell is integrated either by itself in the (1T)1R configuration for fundamental characterization of the Phase-Change material, or in combination with an OTS selector in the (1T)1S1R configuration for complete memory cell evaluation. The GST225 stoichiometric composition is positioned within the Ge–Sb–Te ternary diagram as shown in **Fig. 2.1**.

Antimony-Tuned GeSbTe Compositions

In Chapter 5, we systematically investigate the influence of the Sb/Te ratio on the physical and electrical properties of PCM materials. We integrate various GeSbTe alloys with increasing antimony content to achieve Sb/Te ratios ranging from 0.5 to 2.25 (Fig. 2.1). The PVD deposition is performed through co-sputtering of $Ge_1Sb_2Te_4$ (GST124) and elemental Sb targets. Two distinct integration approaches are employed to obtain amorphous bulk materials formed through simultaneous co-sputtering, and multilayer structures created by alternating deposition of GST124 and Sb layers.

Germanium-Rich GST Materials

Section 5.2 presents preliminary electrical characterization of Ge-rich GeSbTe compositions with germanium excess exceeding 50% (Fig. 2.1). These compositions are designed to achieve automotive-grade thermal stability while maintaining acceptable electrical performance characteristics. The devices are fabricated through co-sputtering from GST225 and Ge targets.

2.2 Ovonic Threshold Switching Materials

OTS material selection requires careful balancing of multiple specifications: high thermal stability for fabrication processes (thermal budget of several hours at $\geq$450 °C), low leakage current, high endurance, and tunable threshold voltages compatible with memory integration requirements [23].

This research focuses on selenium-based OTS systems combined with Group V elements, specifically antimony (Sb) or arsenic (As), using SbSe and AsSe alloys as building blocks for advanced OTS materials. The selection of selenium reflects its optimal combination of thermal stability, electrical properties, and processing compatibility [78]. Previous Investigations of GeSbSeN and N-doped SbSe alloys have demonstrated that germanium content and nitrogen doping significantly influence material structure and thermal stability [69]. Optimized GeSbSeN devices demonstrate endurance exceeding 10^9 cycles [77]. Degradation mechanisms involve gradual crystallization initiated by segregation of SbSe and GeN components under cycling and annealing stress conditions [72].

Unless otherwise specified, we integrate an optimized GeSbSeN (GSSN) alloy composition as described in previous works [19].

Multilayer OTS Architecture

The multilayer (ML) approach addresses fundamental questions regarding OTS functionality, parameter optimization, structural stability during operation, and cost-effectiveness

compared to bulk deposition methods. Multilayer deposition reduces crystalline cluster formation probability, delaying OTS material crystallization under thermal and electrical stress conditions [86]. Previous experimental validation demonstrates excellent electrical performance matching standard bulk GSSN up to 160 °C operating temperatures, with capability to withstand Back End Of Line (BEOL) thermal budget [66].

We validate the ML integration approach for GeSbSeN alloy through electrical tests in Chapter 5 and adopt it for the 1S1R Crossbar application presented in Chapter 6. The ML OTS structure is deposited through alternating SbSe and GeN layers, with individual layer thicknesses and overall composition similar to the "MLA" detailed in previous works [19].

Arsenic-based Selenide Materials

Chapter 5 presents the characterization of AsSe-based OTS alloys fabricated with additions of germanium and silicon to prevent crystallization. These alloys are designed to reduce both the forming voltage and the threshold voltage. The optimal composition proposed, particularly the amount of Si and Ge added to the base AsSe system, is the result of previous extensive material characterization upon which this work builds [19].

2.3 Wall-heater PCM Cell Architecture

The heater-based cell architecture represents one of the most widely adopted approaches in PCM technology, offering precise control over the active region position and improved temperature gradient during programming [43, 87]. This architecture is fundamentally based on a chalcogenide layer deposited on top of a resistive thin bottom electrode (BE), commonly referred to as the "heater". Precise control of heater thickness and length allows optimization of the heat generated during programming operations and positioning of the thermal hot-spot, depending on the PCM/heater resistance ratio [88].

We integrated PCM devices with the Wall–heater architecture (**Fig. 2.2**). This architecture derives its name from the heater deposition process, performed by sidewall deposition of TiN on a patterned SiN dielectric layer that partially masks the bottom electrode. The sidewall deposition process, followed by CMP planarization, enables precise control of the heater width with nanometer-scale accuracy. The heater element is subsequently etched to reduce its length along the y-direction, which defines the "Wall" Critical Dimension (CD). The PCM layer extends across multiple devices on the same bit line without issue, as individual device control through word line selection ensures programming of only the selected cell.

The heater thickness and height are 5 nm and 100 nm, respectively. Unless stated otherwise, the PCM layer thickness is 50 nm, with cell CD ranging from 40 nm to 300 nm

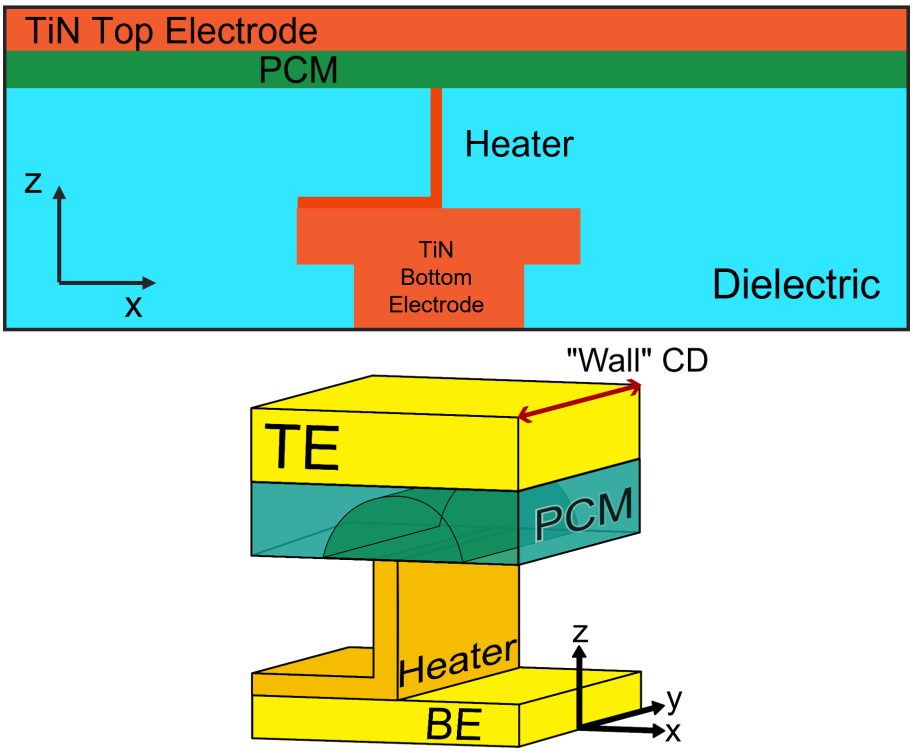


Figure 2.2: Wall–heater cell architecture scheme showing cross-sectional view perpendicular to the TiN heater (top), and 3D cell representation highlighting the key elements of the integration (bottom).

to enable scaling studies.

This architecture is not suitable for direct OTS co-integration, as the presence of a large-area OTS layer increases the OFF-state leakage current (I_{leak}), thereby preventing proper OTS operation [89]. For this reason, a different cell design is mandatory for fabricating devices that successfully co-integrate both OTS and PCM.

2.4 Double-Patterned Self-Aligned Structure for OTS+PCM

This section demonstrates and validates a novel integration approach for PCM devices (1R) combined with OTS selectors (1S) using a "Self-Aligned" technique implemented by two perpendicular patterning steps (i.e., "Double Patterned"). This Double-Patterned Self-Aligned (DPSA) integration simultaneously patterns both memory and selector with independent control along x and y directions. We successfully fabricated devices with Critical Dimension (CD) down to 40×40 nm^2, demonstrating the scalability potential of this integration. The integration is validated using $Ge_2Sb_2Te_5$ PCM and GSSN OTS ma-

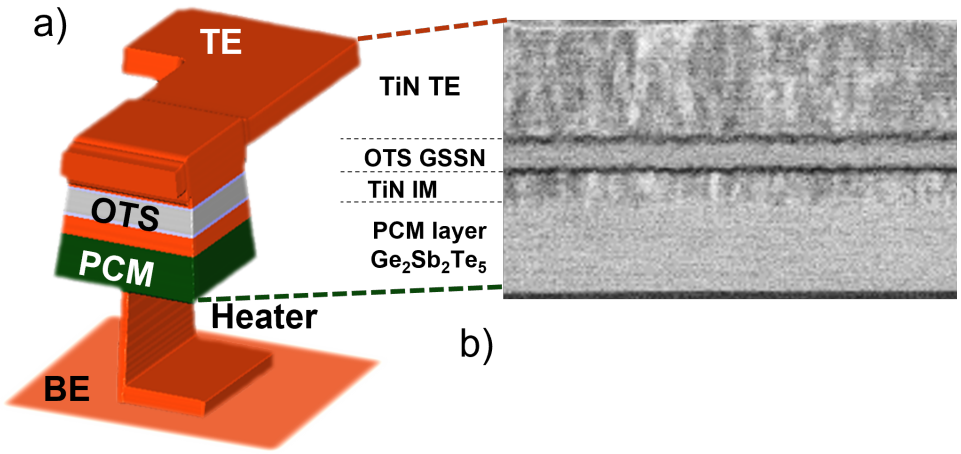


Figure 2.3: DPSA PCM-OTS device architecture a) schematics, and b) Bright Field TEM image of the complete stack. Reproduced from [R10].

terials, and exploited for further material investigations in Chapter 5 [23, 69]. Complete electrical characterization of single devices and array configurations is provided in Chapter 3, as this integration approach allows evaluation of 1S1R Crossbar array functionality (Chapter 6).

The following sections investigate the specific challenges associated with this integration, particularly focusing on the bit line (BL) contact recovery and stringent lithographic alignment requirements for scaled devices. We demonstrate process control through TEM-EDX analysis and provide electrical validation results confirming proper device functionality.

The critical dimension scaling and confinement of the chalcogenide material within an encapsulation material alter the cell's thermal properties, potentially posing a challenge for smaller CDs. The investigation of the thermal properties of the cell is carried out in Chapter 3.

2.4.1 1S1R Cell Fabrication Process

The complete cell architecture is illustrated in **Fig. 2.3a**, featuring a PCM layer deposited on top of a thin TiN metal heater, followed by the OTS layer. To prevent intermixing and elemental migration between PCM and OTS during operation, a TiN Intermediate Metal (IM) layer is incorporated. The fabricated device stack is shown in the TEM of Fig. 2.3b. To improve selector performance and reduce electrical variability, the OTS layer is encapsulated by thin 3 nm carbon layers serving as diffusion barriers and improving interfaces [77]. The heater dimensions are optimized with a height of 100 nm and a thickness of 5 nm, respectively; unless otherwise stated, the PCM and OTS layer heights are 50 nm and 15 nm, respectively.

The 1S1R cells are integrated in both single device and array configurations, with each cell connected in series with an NMOS transistor (1T) fabricated in the BEOL of the LETI Memory Advanced Demonstrator (MAD) based on 130 nm CMOS technology.

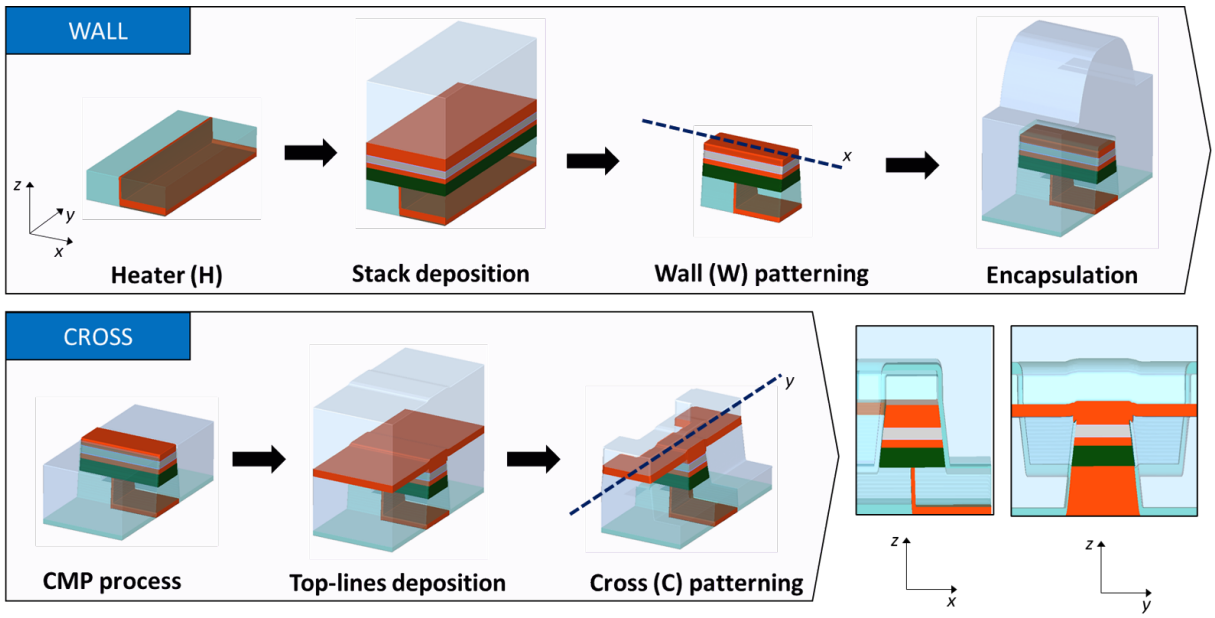


Figure 2.4: DPSA PCM OTS process integration flow highlighting the key "Wall" Self-Aligned patterning (top) and the following "Cross" patterning (bottom). Reproduced from [R10].

The key fabrication steps in the DPSA integration process are illustrated in **Fig. 2.4**, generated using the Coventor SEMulator3D® tool. Following TiN heater deposition, SiN encapsulation, and Chemical-Mechanical Polishing (CMP) planarization, the device stack (PCM, IM, OTS) is deposited. The first patterning step along the Wall (W) x direction etches the memory stack and the heater in a self-aligned fashion, ensuring precise alignment between all active layers. After dielectric encapsulation and CMP planarization, the Top Electrode (TE) metal lines are deposited, followed by the "Cross" perpendicular (C) patterning along the y direction.

The first critical integration challenge is the Top Electrode contact recovery immediately after Wall patterning. We compare two process approaches: dry etch-back performed by RIE (**Fig. 2.5a**), and full CMP planarization (Fig. 2.5). SEM imaging analysis revealed that the etch-back approach exhibits dependence on device pitch, leading to higher variability in the final contact quality. Conversely, the full CMP approach relies on SiO_2 selectivity using the encapsulating SiN as an etch-stop layer, which has been demonstrated to be more reproducible.

The lithography was performed using a Variable Shape Beam VISTEC® SB3054 lithography system, allowing die-to-die correction with high throughput.

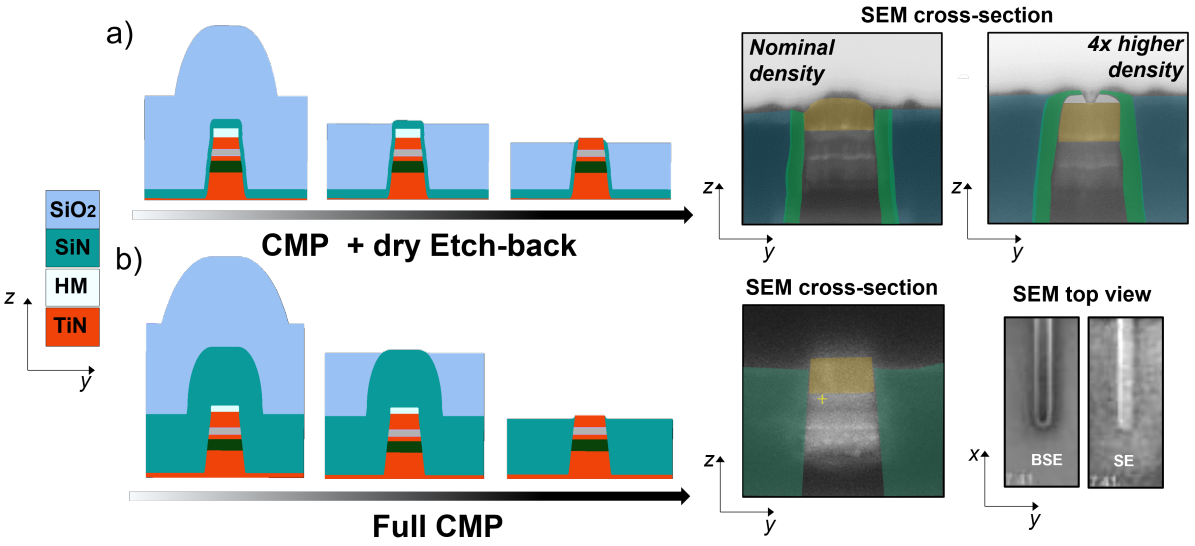


Figure 2.5: Contact recovery approaches after "Wall" patterning and encapsulation: a) "Etch-back" approach showing strong dependency on device density. In the TEM, we compare nominal density to 4× density, demonstrating poorer results. b) "Full CMP" approach demonstrating improved uniformity, confirmed by both SEM cross-section and top view. Reproduced from [R10].

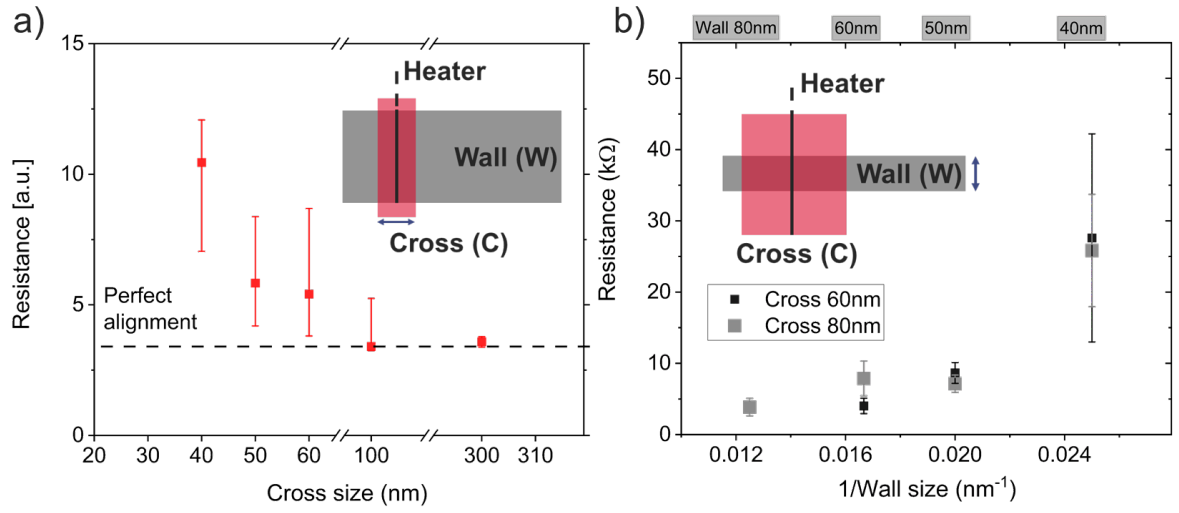


Figure 2.6: Alignment characterization results with a) Median resistance as a function of Cross size on dedicated test structures with variable C for alignment control in 1R devices, and b) Evolution of mean virgin resistance versus reciprocal Wall size in 1R devices. The smallest Wall size of 40 nm shows a higher variability. Reproduced from [R10].

Precise alignment between the "Cross" patterning and the metal heater is crucial for contact recovery and cell functionality, as the active region of the PCM should be centered within the cell volume, requiring the heater to be positioned in the center of the Cross area. To verify the Cross/heater (C/H) alignment, we designed a test structure with varying Cross sizes and enlarged Wall surface, fabricated on wafers with PCM only (i.e., 1R cells)

for contact resistance measurements. The resistance increases for decreasing Cross size due to increasing C/H misalignment (**Fig. 2.6a**), supported by increased resistance dispersion for Cross size below 100 nm. The inset schematically illustrates the test configuration with a wide Wall and varying Cross surface, where misalignment can cause the heater (represented as a black line) to fall outside the Cross contact area, resulting in open circuits.

The "Wall" (W) size represents a less critical but still important parameter. Using the same test vehicle Fig. 2.6b shows device resistance for increasing W with two different Cross sizes of 60 and 80 nm. An approximately linear increase in the pristine resistance with the reciprocal of the Wall size is observed, consistent with expectations based on the total heater surface increase.

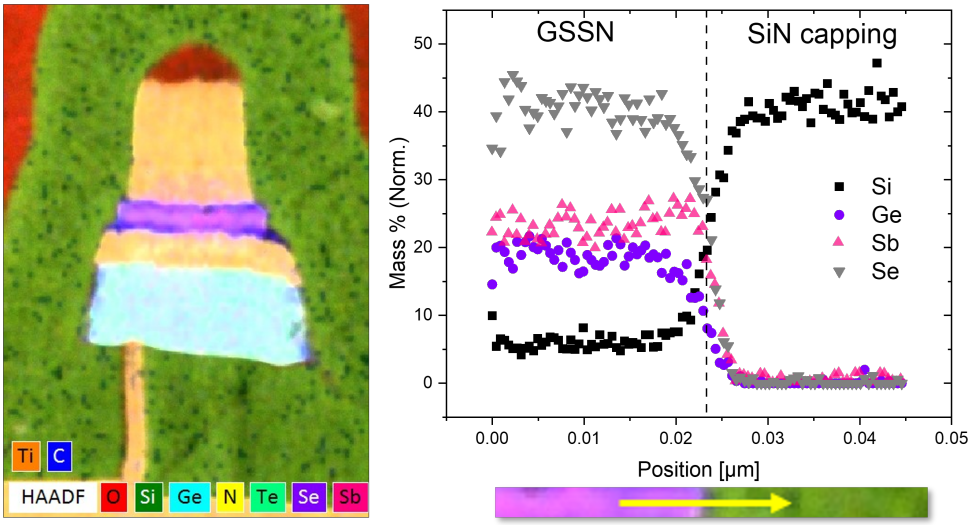


Figure 2.7: HAADF TEM-EDX analysis of a 60×60 device, a) perpendicular to the heater, highlighting C/H misalignment. b) EDX profile performed at the OTS/SiN capping interface showing good device encapsulation. Reproduced from [R10].

By performing High-Angle Annular Dark-Field (HAADF) TEM-EDX analysis on a 60×60 nm^2 device, we obtain an example of the critical Cross alignment issue (**Fig. 2.7a**). In this specific case, the heater (H) is displaced from the Cross center, but still falls within its borders. EDX profiles in Fig. 2.7b confirm the GSSN composition along the OTS/SiN capping interface, validating the encapsulation. To prevent halogen contamination of the chalcogenide layers, which can significantly degrade electrical properties, a customized step-by-step etching strategy was developed and implemented for both Wall and Cross patterning sequences.

The CMP represents a critical step for heater surface planarization before chalcogenide layer deposition. The narrow TiN electrode (5 nm width) and its interface with the PCM play crucial roles during the device operation and lifetime. By TEM-EDX investigation

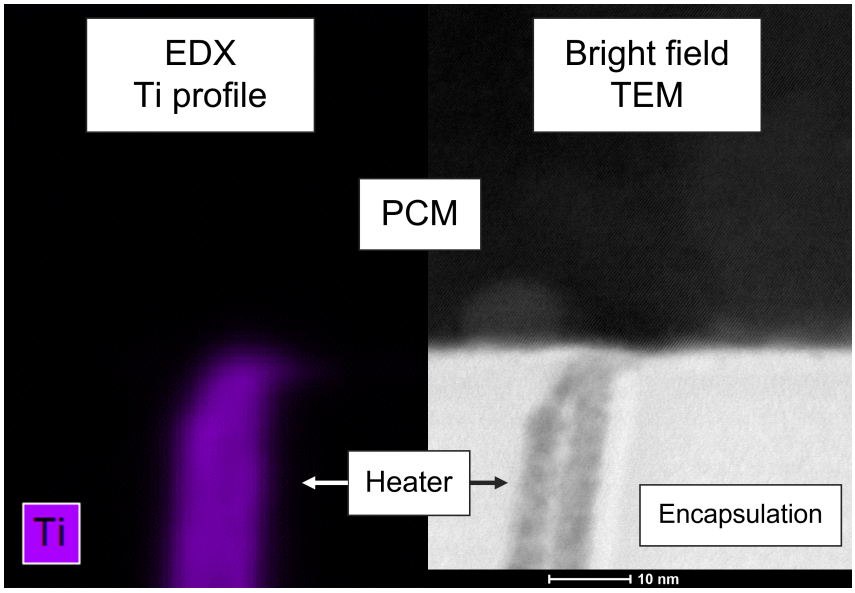


Figure 2.8: TEM-EDX titanium profile (left) and bright field image (right) of the heater/PCM interface showing necking of the heater at the contact interface.

on the heater region of another cell (**Fig. 2.8**), we observe a narrowing of the heater contact, critical for the control of the hot-spot position, confirmed both by a bright-field TEM (right) and Ti profile in the EDX (left). Fine-tuning of CMP parameters and slurry chemical composition plays a major role in this process step and requires careful engineering to maximize yield and uniformity while reducing device-to-device variability [R10]. For instance, a possible solution would be to over-polish the heater surface, exposing the vertical heater sidewall by removing material deposited on the edges, thereby ensuring a consistent contact area.

2.4.2 DPSA 1S1R Electrical Characterization

The electrical characterization of the DPSA cell has provided excellent results, enabling comprehensive characterization of OTS+PCM devices in terms of programming performance (Chapter 3) and reliability assessment (Chapter 4). The electrical characterization methodologies developed for DPSA cells are described in the following section; the integration and evaluation of different PCM and OTS alloys are presented in Chapter 5. The culmination of this work includes electrical results from a 1 kb 1S1R Crossbar array implementation using DPSA OTS+PCM cells, as detailed in Chapter 6.

2.5 Device Electrical Characterization

This section presents the main electrical characterization methods used throughout this work. The device cell and its configurations, either as a single device, matrix, or Crossbar,

are presented. Finally, the test equipment and setup are described.

2.5.1 OTS+PCM Cell circuit

The simplified circuit diagram of a 1T1S1R cell is presented in **Fig. 2.9a**, depicting the series connection of the OTS selector, the PCM, and the NMOS transistor. Due to the high resistance of the amorphous OTS in its OFF state, most of the applied voltage (V_{top}) drops across it, making the NMOS transistor contribution negligible for sufficiently high compliance voltages (V_{comp}). This configuration enables all types of operations, while the access transistor provides essential current limitation that is not intrinsically provided by the selector alone. The resulting I–V characteristic is as presented in Section 1.4, with the amorphous OTS dominating conduction until threshold switching occurs, where the current saturates to the transistor's compliance.

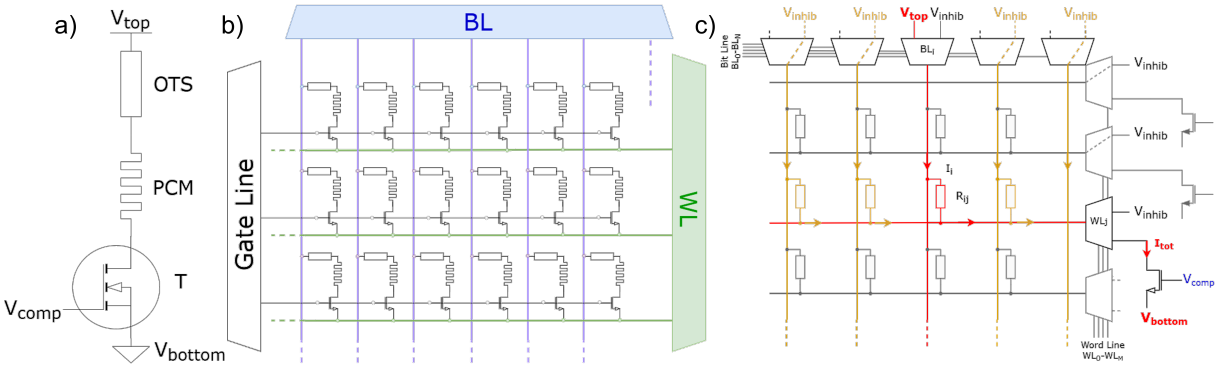


Figure 2.9: Circuit diagram of a) single 1T1S1R cell, b) 16 kb 1T1S1R matrix, c) 1 kb 1S1R Crossbar array.

Upon threshold switching, both the OTS and PCM resistances drop significantly (i.e., to a few kΩ range), causing the voltage drop across the transistor to increase, leading to current saturation at I_{comp} or I_{sat}.

In the final product, the OTS should be considered the sole selector, but the MOSFET selector in series with the 1S1R cell presents some advantages, particularly during preliminary exploration and validation phases. Current limitation capability allows characterization of the impact of different electrical stress conditions and energy levels applied to devices, while also allowing the exclusion of non-functional cells from arrays, without risk of sneaking paths. For these reasons, we integrated a wide range of configurations: 1R PCM, 1S OTS, and 1S1R OTS+PCM, each available with and without series transistors. The transistor drain connects to the PCM Bottom Electrode (BE) while the source is biased at V_{bottom}. Only the Crossbar arrays presented at the conclusion of this work utilize true 1S1R cells without series transistors, representing the target architecture for commercial implementations.

Series NMOS Transistor Specifications

The transistor saturation current (I_{sat}), also referred to as compliance current (I_{comp}), depends on the NMOS transistor dimensions. We integrated three different sizes with channel lengths of 0.6, 3.5, and 5.9 µm, providing maximum currents of approximately 600 µA, 1 mA, and 2 mA, respectively. All devices with Critical Dimension (CD) ranging from 300 nm down to 40 nm are available in series with any of the three transistor sizes. This design flexibility enables the selection of appropriate transistor characteristics depending on device size and desired operating conditions. Initial transistor characterization was performed on short-circuit test structures (i.e., without PCM or OTS layers) to obtain I_D–V_G curves, allowing selection of appropriate device/transistor combinations. When transistor effects are not relevant for intrinsic device property studies, cells are referred to as 1S1R or (1T)1S1R, indicating that while the transistor is present, it does not influence the studied behavior.

(1T)1S1R 16 kb Matrix

We integrated the 1T1S1R cell into a 16 kb matrix configuration (Fig. 2.9b). The matrix comprises 128 bit lines (BL) and 128 source lines (SL) connected to device Top Electrodes (TE) and NMOS sources, respectively. A series of 128 Word Lines (WL) parallel to the SL enable an independent set of transistors gate bias (V_{comp}). During operation, the selected BL is biased to V_{top} while the corresponding SL is polarized to V_{bottom}. Device addressing is accomplished through scan-chain control managed by an external clock signal provided by the measurement equipment. The matrix configuration allows access to individual cells while maintaining isolation from neighbouring devices. Due to the reduced device-to-device fabrication variability of spatially proximate devices, the matrix represents an excellent platform for statistical evaluation of large populations and forms the foundation for most of the studies presented in this work.

A potential concern in large matrices is IR drop due to line resistance, which we evaluated using short-circuit cells (NMOS transistors only without memory devices). The maximum IR drop was determined to be 70 Ω across the entire matrix, which is negligible compared to typical device resistances. This low IR drop is achieved through metal line dimensions that are significantly larger than the device size, with consistent line dimensions across all device critical dimensions.

1S1R 1 kb Crossbar Array

One primary objective of this work is to demonstrate the functionality of a Crossbar array, achieved in Chapter 6. A true 1S1R Crossbar relies on the OTS selector for device access, with current control and limitation delegated to peripheral circuitry acting on multiple

devices. The circuit schematic of a 1S1R Crossbar is shown in Fig. 2.9c, where each BL can connect to either the top electrode voltage (V_{top}) or the inhibit voltage (V_{inhib}), through a multiplexer. Similarly, each WL can connect to V_{inhib} or to a transistor drain providing current limitation shared across the entire line. Crossbar array performance depends critically on the quality of the fabricated OTS selector, as any short circuit in a single device would compromise an entire WL. Therefore, careful material optimization, integration refinement, and programming protocol development must be completed using matrix configurations before transferring the technology to Crossbar architectures.

2.5.2 Test Equipment and Measurement Setup

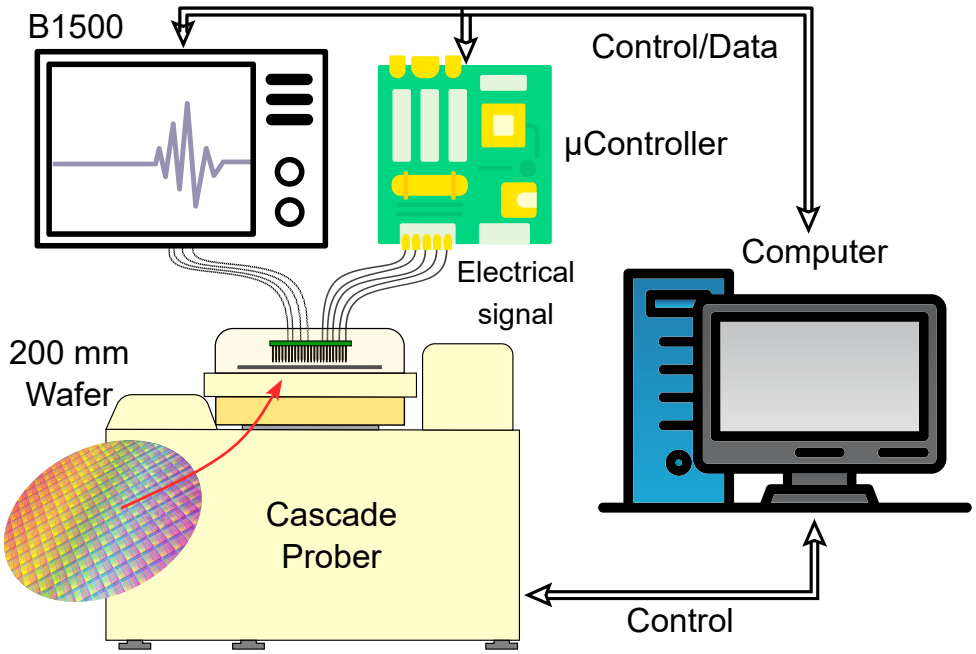


Figure 2.10: Laboratory test environment configuration. The test framework running on the computer controls the semi-automatic prober, the Agilent B1500 analyzer, and a custom microcontroller used for matrix addressing. Measurement data flows back to the computer for storage and analysis.

A comprehensive schematic of the test setup is illustrated in **Fig. 2.10**. Devices are integrated on 200 mm silicon wafers and handled by a semi-automatic Cascade Microtech 200/300 mm wafer prober, offering semi-automatic device selection and wafer alignment capabilities. The prober accommodates both whole wafers and individual dies, as required in sample preparation for TEM analysis. Device access is achieved through metal pads fabricated on the wafer surface, with electrical contact established through a 25-pin custom probe card. The measurement equipment is then connected to the probe card through dedicated connectors. Matrix addressing and DC power supply are provided through a customized microcontroller board specifically designed for this application. AC

signal generation and measurement are performed by means of an Agilent B1500 Semiconductor Analyzer equipped with Waveform Generator Fast Measurement Unit (WGFMU) modules.

A Python-based custom framework running on a dedicated computer synchronizes and manages communication between all instruments. Through coordinated control signals, the framework handles wafer positioning and probe contact, addressing and bias signal, as well as triggering the execution of preloaded waveforms in the B1500 analyzer. Upon measurement completion, the semiconductor analyzer transmits back to the main computer. This framework is designed to handle various structure types, from single devices to matrices, with sufficient flexibility to customize measurement sequences for different characterization requirements. Individual measurement protocols, including pulse types, duration, and sequences, are defined in dedicated Python scripts specific to each waveform and pulse sequence, enabling rapid protocol development and optimization.

Data Analysis and Processing

Raw data output from the Agilent B1500 is analyzed, conditioned, and interpreted using both open-source statistical software and libraries (including Python and R) and commercial software such as Origin Pro™. Statistical analysis includes distribution fitting, reliability modeling, and advanced visualization techniques essential for device characterization and reliability assessment.

2.6 Electrical Characterization Protocols and Methods

This section presents the electrical characterization protocols developed to assess PCM and OTS device performance. The fundamental differences between PCM and OTS reading and programming are presented, followed by the description of reliability metrics extraction procedures.

2.6.1 PCM Characterization Methods

Phase-Change Memory is a resistive device whose state can be assessed through low-voltage resistance measurements. Programming is achieved by providing sufficient current to generate adequate Joule heating for melting the PCM in the active region. Depending on the selected pulse voltage and profile, either crystallization (SET) or amorphization (RESET) can be achieved.

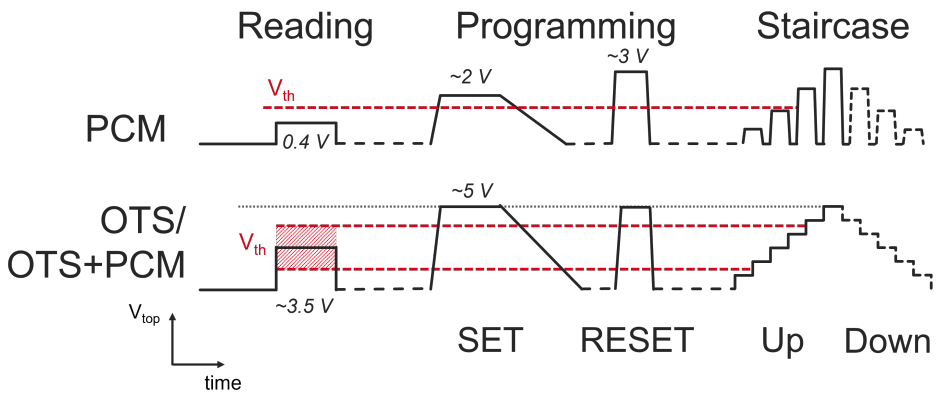


Figure 2.11: PCM and OTS/OTS+PCM main characterization tests. The voltage waveforms as functions of time are shown for reading, programming, and staircase sequence.

Reading and Programming Operations

In (1T)1R devices, reading operations are performed at sufficiently low voltages (e.g., 0.4 V) to measure the PCM resistance, typically in the range from a few kΩ for the SET to a few MΩ for the RESET (**Fig. 2.11**).

The reading voltage (V_{read}) must not exceed the PCM threshold and should drive minimal current to avoid unintentional state changes.

Programming is achieved using higher voltage pulses that exceed the PCM threshold, in the 1 to 2 V range. The current amplitude depends on the Top Electrode voltage (V_{top}) and has to be higher for RESET to increase the size of the melted region. Critical pulse parameters include fall time, which determines the final state; a short fall time (e.g., 5–10 ns) can produce melt-quench amorphization, while longer fall times (e.g., 100 ns to 100 µs) favor crystallization [44].

The series transistor enables favorable programming current control either through top electrode voltage (V_{top}) modulation or by fixing V_{top} and limiting the transistor gate voltage (V_{comp}). While these approaches appear equivalent, subtle differences in programming behavior have been reported between voltage- and current-controlled programming schemes [56].

Pulsed Staircase Sequence

The most important figure of merit for PCM is the resistance-current (R–I) characteristics (As seen in Section 1.2). To establish this relationship, device resistance is measured as the programming pulse current increases (Fig. 2.11). The pulsed staircase UP (SCU) allows for the detection of the crystalline-to-amorphous transition (i.e., RESET current); a pulsed staircase DOWN (SCD) provides information on current and timing requirements for reliable SET operations.

The combination of multiple SCU and SCD sequences is often referred to as a "bathtub" curve and provides a comprehensive representation of key PCM metrics [90].

2.6.2 OTS and OTS+PCM Characterization

Reading and programming operations in (1T)1S OTS or (1T)1S1R OTS+PCM devices are current-controlled, requiring Top Electrode voltage (V_{top}) that exceeds the device threshold voltage (e.g., 5 V in OTS+PCM). Therefore, reading must discriminate between distinct V_{th} states, while programming is performed at a fixed V_{top} by varying the transistor gate voltage.

Reading and Programming Operations

Depending on the PCM state, 1S1R cells exhibit two distinct threshold voltage (V_{th}) states, high (i.e., RESET) and low (i.e., SET) V_{th}. Reading operations are performed by applying voltages within the RESET–SET voltage margin and measuring the resulting current (Fig. 2.11). The impact of reading operations on programmed states is studied in detail in Chapter 4.

For OTS+PCM programming, the same considerations as for PCM apply, with the distinction that SET or RESET programming is performed by applying fixed V_{top} while controlling transistor compliance current (I_{comp}). Similar pulse profile variations enable either SET or RESET operations, as the OTS remains conductive down to its holding voltage (V_{hold}), which is typically much lower than programming voltages (approximately 1 V).

Electroforming Initialization Step

OTS devices require an initialization step called "forming" or "firing" to create a conductive path in the selector, responsible for the subsequent reliable threshold switching [23]. To induce switching in as-deposited amorphous OTS chalcogenides, voltages typically higher than the V_{th} are required (e.g., $V_{fire} \geq 5$ V). This initialization step significantly impacts subsequent device operation characteristics [62]. The forming pulse is similar to a RESET pulse in amplitude and duration, and the forming current level influences long-term device behavior and reliability. The physical implications of the electroforming step are described in Section 1.3.1.

Voltage Staircase Sequence

OTS threshold voltage detection employs staircase sequences with increasing voltage amplitude (Fig. 2.11). A pulsed staircase similar to the one used for PCM could be used to detect the threshold voltage. In this study, we utilize continuous staircases rather than

pulsed sequences for several essential reasons. Depending on the PCM state, devices may switch at different voltages, and pulsed staircases would terminate upon V_{th} detection, causing different devices in different states to experience different current intensities, contributing to increased variability. Moreover, switching events significantly impact OTS state (Section 4.3), and repeated ON/OFF switching may induce early degradation, while continuous staircase on devices only switch once. Additionally, measuring OTS holding voltage (V_{hold}) requires maintaining the device in the ON state while voltage decreases. We employ staircases with discrete steps rather than continuous ramps to ensure well-defined voltage levels at each measurement point while achieving rapid measurement times (300 ns step width).

2.6.3 Reliability Metrics

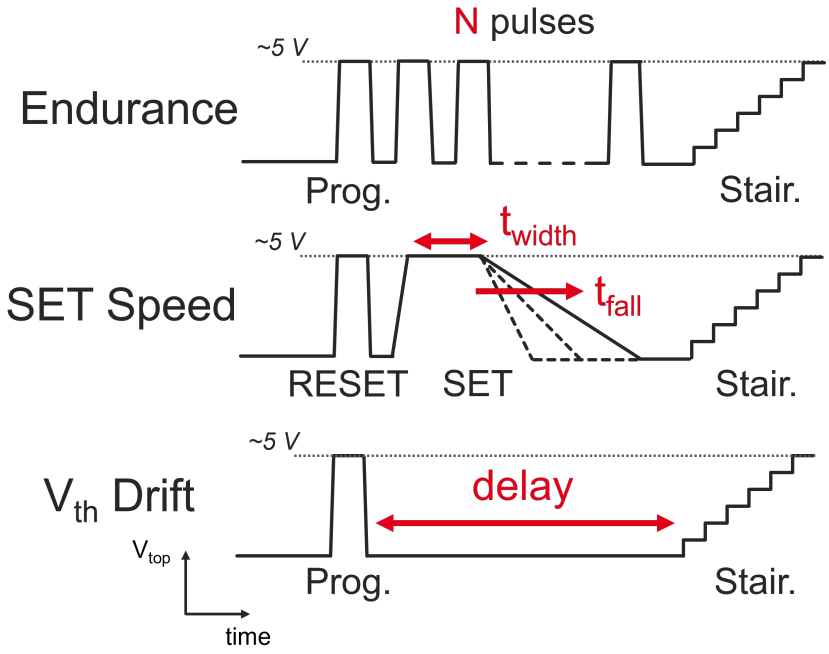


Figure 2.12: Endurance, SET Speed, and V_{th} Drift assessment protocol voltage waveforms.

Beyond standard electrical characterization, additional figures of merit are essential for comprehensive device performance evaluation. These are described for 1S1R OTS+PCM, though similar protocols can be adapted for 1R PCM.

Endurance

Endurance testing involves repeated programming cycles, typically providing large amounts of energy to devices. It allows for evaluating the characteristic after extended electrical

stress to assess the device's lifespan. The endurance test is performed by applying an increasing number of programming cycles interspersed with voltage staircases for V_{th} detection (**Fig. 2.12**). Degradation of V_{th} or subthreshold resistance can be correlated with the number of applied pulses or cumulative energy.

SET Speed

SET speed measurements evaluate the minimum pulse width (t_{width}) and fall (t_{fall}) time required for complete PCM crystallization (Fig. 2.12). The protocol consists of RESET initialization to establish a known starting condition, followed by SET pulses with variable t_{width} and/or t_{fall}. Finally, a voltage staircase measures devices' I–V curve for V_{th} and subthreshold conduction. Similar protocols with reduced voltages are used for evaluating SET speed in 1R PCM devices.

Drift

Threshold voltage drift in OTS devices (and resistance drift in PCM) represents a well-known phenomenon in chalcogenide materials [48, 64]. This temporal evolution of programmed states is evaluated by measuring device conduction after increasing delay times from the programming pulse (Fig. 2.12). Subthreshold conduction as a function of delay time enables extraction of the drift coefficient (ν), which quantifies the rate of resistance or threshold voltage change and is critical for predicting long-term data retention performance.

Data Retention

Data retention represents a critical parameter for evaluating programmed state stability under thermal stress. This metric is crucial for automotive-grade memory validation, where devices must retain information for 10 years at 165 °C [31]. Evaluation involves programming multiple cells in both SET and RESET states, followed by resistance or V_{th} monitoring after baking with increasing temperature and duration.

2.7 Multiphysics TCAD Simulations

To support and interpret the electrical results presented throughout this work, we employ TCAD multiphysics simulations. This section provides details and references for the simulation methods employed.

The thermal response of both "Wall" and DPSA cell architectures during programming operations was simulated using the Synopsys Sentaurus™ Technology Computer-Aided Design (TCAD) suite. The technology design tools enable the simulation of fabrication

steps, accurately recreating cell geometry. While the simulations approach experimentally measured values, they are not fully optimized and primarily provide qualitative evaluation tools to corroborate hypotheses supported by electrical measurements and TEM analysis. The trade-off between model complexity and computational accuracy limits deployment at the current development stage, requiring focused research and engineering efforts to obtain quantitative results. The core simulation model builds upon previous works that have established fundamental approaches to PCM device simulation [91, 92]

Cell Geometry Definition

The integration steps illustrated in Fig. 2.2 were reproduced using the Sentaurus Process suite. The integration assumes ideal conditions, with nominal dimensions, while the top and bottom boundaries are assumed to have Dirichlet boundary conditions (DBC). All interfaces are considered ideal, unaffected by imperfection or roughness effects. PCM/TiN and PCM/SiN thermal boundary resistances (TBR) are selected from literature values [93].

Electrothermal Modeling

The primary simulation objective is to determine the temperature distribution in the PCM hot-spot during programming operations using quasi-stationary analysis for different current conditions. The Sentaurus solver determines potential, current, and temperature distributions throughout the cell by solving coupled partial differential equations (PDEs) for heat transfer, Joule heating, and Poisson conservation equations. The coupled system incorporates model-dependent parameters, including PCM and OTS electrical conductivity, thermal interfaces, heat capacity, and material density values obtained from literature and experimental measurements [94]. Temperature-dependent electrical conductivity of PCM materials is extracted from an Arrhenius model formulation calibrated to experimental data [83]. Thermal conductivity values for chalcogenide materials are based on established literature values with temperature dependencies incorporated where available [45].

OTS Layer Simulation

Electrothermal simulation of the OTS layer presents greater complexity, requiring dynamic models that account for threshold switching events and property differences between conductive filaments and amorphous regions within the selector [58, 95, 96]. To simplify OTS simulation while maintaining physical relevance, we defined an active conductive region compatible with filament dimensions [63]. This region is assumed to exhibit metallic-like electrical and thermal properties, with ON resistance consistent with experimental results [97]. The remaining OTS volume maintains OFF state properties typical

of chalcogenide materials, with thermal and electrical properties similar to PCM in the amorphous state [98]. While this approximation does not capture the complete physics of the threshold switching, it provides valuable insights into PCM behavior at aggressive scaling dimensions, as discussed in Section 3.5.

Chapter 3

Programming Operation in (1T)1S1R OTS+PCM

This chapter examines the impact of programming conditions on 1S1R OTS+PCM cells in comparison with 1R PCM and 1S OTS devices. The basic programming procedures are outlined, investigating the impact of the lateral confinement and the addition of the OTS selector. Devices with dimensions of 40 and 100 nm are compared to assess the impact of scaling on electrical characteristics, providing the parameters for both RESET and SET operations. We examined the variability of the threshold voltage (V_{th}) for both the SET and RESET states, comparing different distribution models to validate the use of mean and standard deviation as viable metrics. The dispersion of V_{th} is tracked under different programming conditions to provide insight into the evolution of device behavior over SET/RESET, in terms of programming speed and endurance cycles. The chapter motivates the adoption of the normal distribution for population description, outlining its limitations when dealing with device failures. The second part of the chapter examines the device's failure modes upon programming, originating from both PCM and OTS elements. Their respective contributions are analyzed, showing that the OTS selector is responsible for limiting endurance. The presence of a co-integrated PCM on the stack may further degrade the cycling performance. Finally, TCAD thermal simulations are carried out to compare 1R and 1S1R cells; the results show higher temperatures in the 1S1R cell with a full volume involved in the phase transition. The simulation results are confirmed by TEM analysis of cells in SET and RESET states.

3.1 OTS+PCM Programming

In this chapter, we analyze the programming characteristics of DPSA 1S1R OTS+PCM devices, including RESET and SET programming performance, the statistics of the corresponding threshold voltage, the programming endurance, and the impact of the integration on the thermal behavior of the cell. As described in Chapter 1, programming enables the selector to be turned ON, thereby applying a suitable current profile to the memory. The heater element, fabricated in both "Wall" and our DPSA architectures, is responsible for the Joule heating of the PCM layer and fixing the hot-spot position [44]. The OTS requires an initialization step with currents similar to those of the RESET. This step forms the conductive path in the OTS device and melts a large portion of the PCM volume [62]. Before performing further electrical characterization, the devices were all initialized with a pulse adapted to the size and material to reliably program the cells. We performed the electrical characterization of the devices using a pulse-based (AC) protocol. The threshold voltage (V_{th}) was systematically measured by a staircase-up sequence (Section 2.6). During the programming and reading operations, we controlled the series NMOS transistor (1T) gate voltage to limit its saturation current (I_{sat}). Unless otherwise specified, the PCM material is standard $Ge_2Sb_2Te_5$ (GST225) and the OTS based on a GeSbSeN (GSSN) alloy as described in Chapter 2.4.

In a (1T)1S1R cell, the programmed state is assessed by a current measurement at high voltage (e.g., 3.5 V) in place of a low voltage (∼0.4 V) resistance measurement in (1T)1R cells. In a (1T)1R PCM cell, the desired current profile is obtained by selecting a suitable Top Electrode voltage, which exceeds the PCM threshold voltage ($V_{th,PCM}$), and a suitable series transistor gate voltage. However, in a (1T)1S1R OTS+PCM cell, the Top Electrode voltage should exceed the highest V_{th} possible (when the PCM is programmed in the RESET state); therefore, the current control relies on the series transistor to perform programming operations (Fig. 2.11). The SET threshold voltage (V_{SET}) of 1S1R devices depends only on the OTS switching voltage, as the PCM acts as a small series resistance [37]. When in the RESET state, the OTS selector and the PCM threshold voltages and their subthreshold resistances affect the final V_{th} distribution. The RESET threshold voltage (V_{RESET}) is reached when one of the two elements switches first; the RESET hence depends on the voltage divider between the two (Fig. 1.8) [99, 100]. The OTS exhibits larger resistance but also greater V_{th} compared to PCM; however, as the subthreshold bias increases, the resistance decreases, following the Poole-Frenkel mechanism, similarly to PCM [47]. The optimal case has the ratio of the resistances (R_{OTS}/R_{PCM}) approaching the ratio of the threshold voltages ($V_{th,OTS}/V_{th,PCM}$). The overall V_{RESET} is then equal to the sum of the two individual thresholds ($V_{th,OTS}+V_{th,PCM}$). This case provides a suitable upper limit for approximating the V_{RESET} in a 1S1R cell.

3.1.1 Electrical characteristic

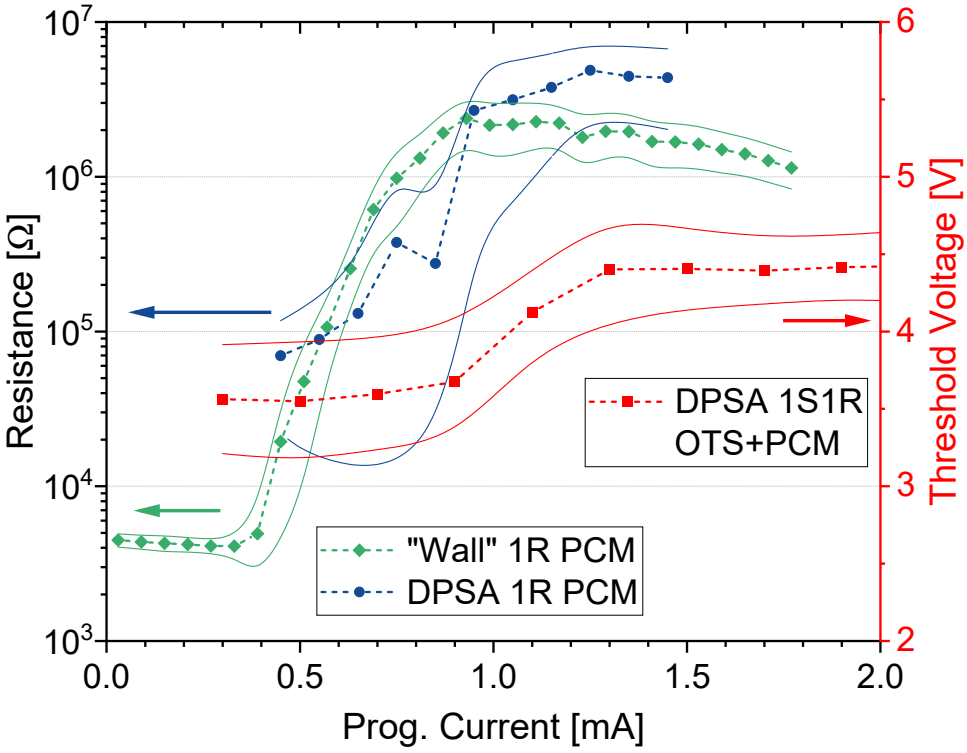


Figure 3.1: Resistance (left axis) and threshold voltage (V_{th}) (right axis) versus programming current comparing 1R "Wall" PCM, 1R DPSA PCM, and 1S1R DPSA OTS+PCM. As the OTS+PCM is highly resistive, its programming is assessed by the detection of the threshold voltage. The graph reports the mean and standard deviation of more than 64 devices with a 100 nm critical dimension (CD).

A sequence of programming pulses is applied to extract the programming characteristic (**Fig. 3.1**). The device is first initialized in the SET state, and a pulse is applied for each programming current. The cell is reinitialized before each iteration, as the cumulative application of pulses can reinforce PCM states, discriminating the effect of an individual pulse. For the 1R PCM, the programming pulse is followed by a low-voltage readout of the resistance value (left axis of Fig. 3.1), for OTS+PCM, a staircase up sequence detects the V_{th} (right axis of Fig. 3.1). The programming characteristic provides the first essential parameters related to devices' behavior, as the RESET current ($I_{prog,RESET}$), and the favorable SET current range ($I_{prog,SET}$) [43]. Comparing 1R and 1S1R devices sharing the DPSA architecture, we find compatible programming current values (I_{prog}) for the SET-to-RESET transition.

Comparing the "Wall" to the DPSA structure reveals similar RESET resistances; however, the SET state differs by more than one order of magnitude between the two, despite expectations of consistency given identical materials and the same heater surface. To

understand why the SET state appears degraded in the 1R DPSA cell, we hypothesize that the applied pulse does not fully crystallize the cell, therefore, only inducing a partial crystallization. The partial crystallization can also be observed in the 1S1R OTS+PCM cell, where the minimum threshold voltage is approximately 3.5 V on average, higher than the expected 2 V of the OTS expected for an effective SET state. Our protocol performs programming with fixed pulse duration (t_{width}) and fall time (t_{fall}), which may not be sufficient to induce a complete crystallization of the PCM. Therefore, the programming characteristic provides a range of I_{prog} that is favorable to the SET operation, which requires further optimization by adapting the pulse shape. In an OTS+PCM, the SET performs a melt and a slow cooling to crystallize the chalcogenide material; the temperature in the active region must be higher than the melting point, T_{melt}. Then, either the cool-down rate should favor the nucleation of new crystallites or the temperature gradient should maximize crystal growth from the cell borders [53, 60].

Care must be taken when comparing different cell architectures in Fig. 3.1 as fabrication differs significantly, which may lead to variations in Critical Dimension (CD) from the nominal one. The DPSA structure is laterally confined, that is, the chalcogenide is patterned with a critical dimension on both x and y directions, and encapsulated by an insulating material (Section 2.4). This lateral confinement may alter the temperature gradient, requiring longer fall times to reach a complete SET [101]. When co-integrating the OTS selector, the PCM layer is isolated from the Top Electrode by approximately 15 nm of amorphous chalcogenide material, further confining the heat generated in the cell, which could be responsible for the differences seen in Fig. 3.1 between 1R and 1S1R. This hypothesis is further supported by the simulations and TEM images presented later in the chapter.

3.1.2 Impact of the Device Size

Device scaling reduces the total volume and the heater surface area while increasing lateral confinement. **Fig. 3.2** compares the programming curves of scaled down devices with 40 nm and 100 nm Critical Dimension (CD). The two sizes exhibit a compatible threshold voltage range, between 3.5 V (V_{SET}) and 5 V (V_{RESET}). The 40 nm cells can be programmed in the RESET state with a current reduction of approximately 50% as expected from the reduced heater size (i.e., critical dimension). 40 nm devices show higher V_{th} than the 100 nm population, with an enlarged voltage window. A resistance increase due to the reduced heater surface is expected; however, it does not justify the corresponding increase in the window. We suggest that the increased lateral confinement leads to an amorphization of the whole cell volume during the RESET operation. Potential elemental segregation upon the first fire operation could partially account for this difference, but further investigation is required.

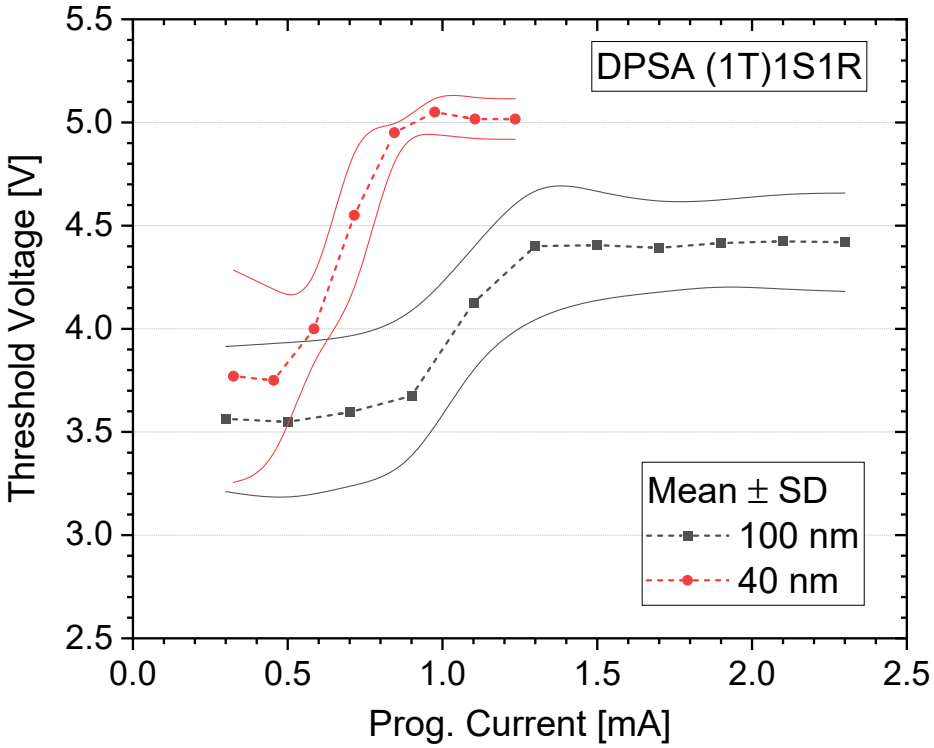


Figure 3.2: Evolution of the V_{th} as a function of the programming pulse current in 1S1R OTS+PCM devices with CD of 40 and 100 nm. The figure reports the mean and standard deviation of 50 devices.

3.2 RESET Operation and Optimization

The RESET V_{th} is maximized by choosing a suitable $I_{prog,RESET}$, keeping it the lowest possible to reduce power and overall energy to the selector. For a reliable melt-quench operation, the pulse fall time should be the shortest possible, given the instrument or line capacitance limits on the programming speed. Unless otherwise specified, typical RESET pulses have the optimized parameters outlined in **Table 3.1**, reported for 40 and 100 nm in $Ge_2Sb_2Te_5$. Our test vehicle is unreliable in achieving current control below 100 µA due to the large NMOS transistor size (3500 nm width).

	t_{rise} [ns]	t_{width} [ns]	t_{fall} [ns]	I_{prog} for GST225	
				40 nm	100 nm
RESET	20	300	20	1 mA	1.2 mA
SET	100	300	10^3	350 µA	500 µA

Table 3.1: SET and RESET programming pulse parameters for 40 and 100 nm CDs.

3.3 SET Operation and Speed

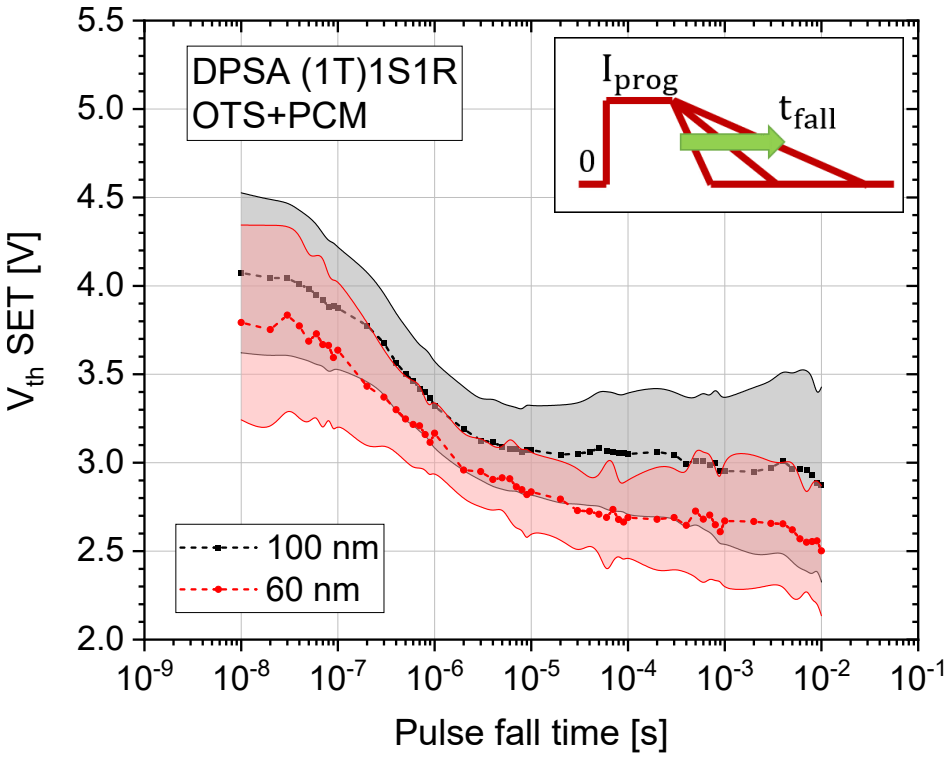


Figure 3.3: V_{SET} as a function of t_{fall} of about 300 devices: 60 nm and 100 nm devices show a similar trend. The inset describes the pulse shape, with fixed current and variable t_{fall}.

The SET current was selected to minimize the V_{SET} from V_{th} vs I curves (Fig. 3.2). To further crystallize the PCM, we investigated the impact of pulse fall-time (**Fig. 3.3**). We observe a reduction in V_{SET} when increasing the t_{fall} value in both device dimensions, which is compatible with an improved SET programming. Remarkably, both 60 and 100 nm devices show a similar evolution, suggesting a negligible impact of the scaling on the device's SET performance for the same DPSA structure. These results suggest a t_{fall} greater than 10 µs to obtain the most reliable SET state in our configuration. Since this would make endurance tests impractical, we selected a reasonable fall time (t_{fall}) of 1 µs. The optimized SET parameters used for this study are reported in Table 3.1.

The duration of the SET pulse represents a latency bottleneck, as the writing frequency cannot attain the MHz range. While our programming speed is slower compared to the state-of-the-art competitive level [46], it provides a comparative insight into the underlying issues. The DPSA architecture suffers from enhanced thermal confinement of the PCM layer, as in our configuration, the OTS selector is deposited between the memory and the Top Electrode. Fast SET exploits the rapid crystalline growth that occurs outside the active region. As the device size is reduced, the active chalcogenide material volume is

smaller and more thermally confined, producing the amorphization of the whole volume during RESET operations. To SET the PCM cell, there is no preexisting crystal left to induce homogeneous crystal growth, and crystal nucleation has to occur to start to crystallize the cell. As the nucleation rate is much slower than the growth rate [53], this could explain our slower SET compared to the DPSA compared to the Wall cell, as SET speed is limited by the formation of new crystals within the cell volume [102].

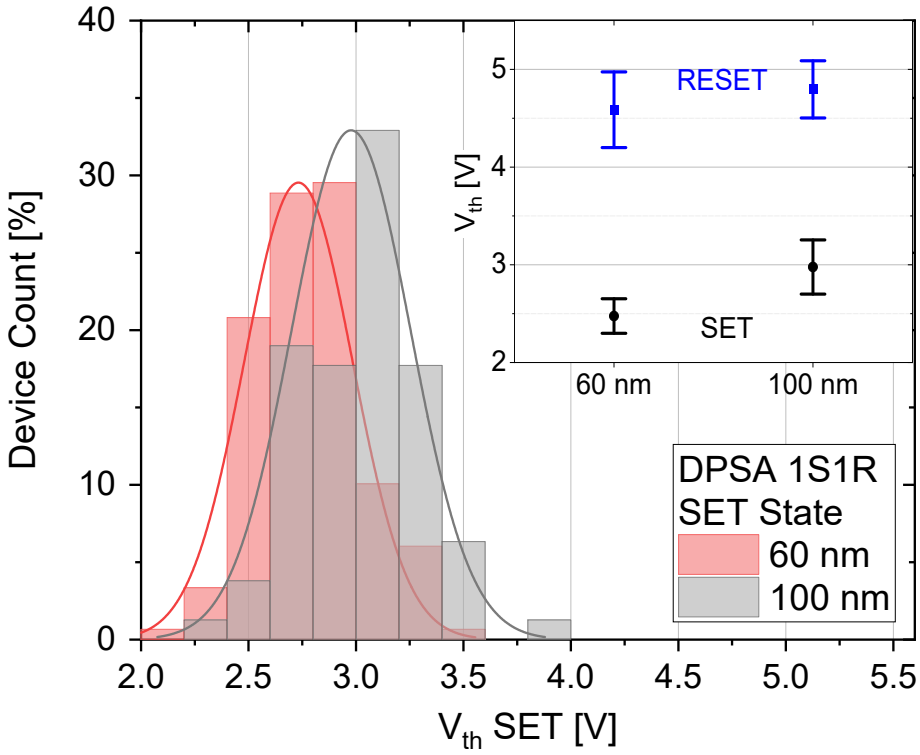


Figure 3.4: V_{SET} distributions of 160 devices, both for 60 nm and 100 nm. In both cases, the SET is achieved with a 1 µs fall time (t_{fall}). The inset shows the achieved V_{SET} and V_{RESET} (with their 1σ deviation).

3.3.1 SET State Statistical Analysis

After the first forming operation, some devices may still not have reached a stationary regime, as the composition of the PCM in the active region [90] or the OTS conduction [62] may still evolve. To obtain reliable and repeatable results, we cycled the devices approximately 100 times, alternating SET and RESET programming operations. **Fig. 3.4** shows the obtained V_{SET} distributions after an optimized SET pulse. The inset in Fig. 3.4 highlights the good separation (at 1σ) of the SET and RESET distributions. Both sizes exhibit a compatible window of more than 2 V for the 60 nm devices. We obtain a good window, comparable with literature standard devices based on pillar structure OTS+PCM

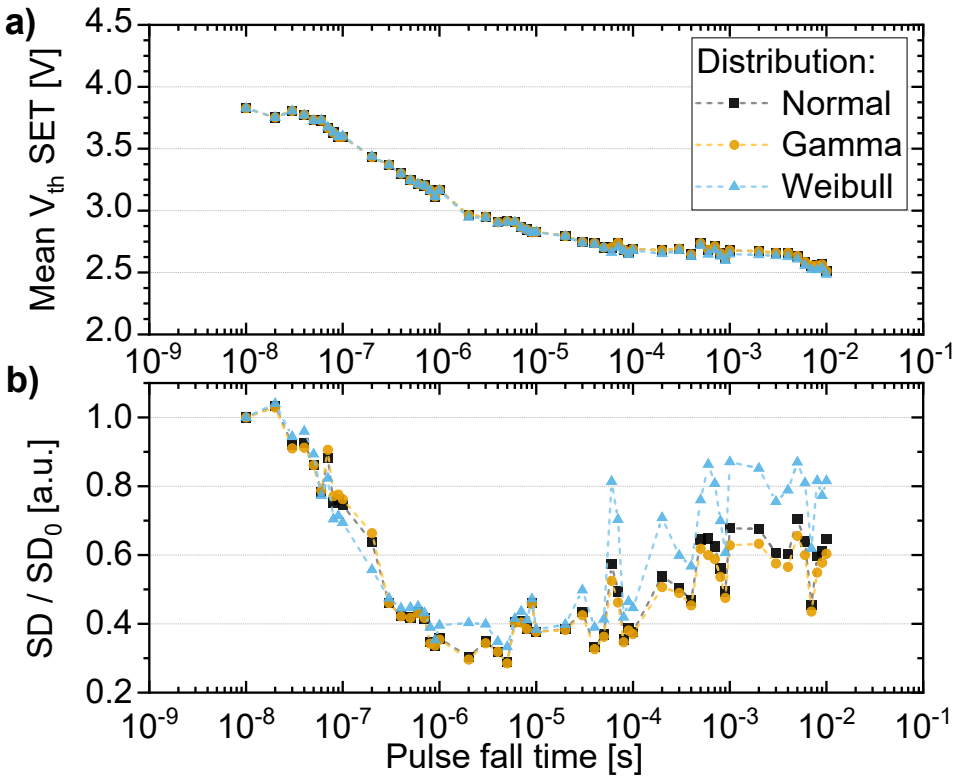


Figure 3.5: (a) Mean and (b) standard deviation values of V_{SET} as a function of t_{fall} extracted using Normal, Weibull, and Gamma distribution models for 60 nm devices (300 samples).

[79, 80], with the additional advantage of using an As-free composition for our OTS selectors [R9].

Normal distribution is commonly used for the analysis of V_{th}, reporting the associated mean and standard deviation (SD) values. However, the stochastic switching mechanism in chalcogenide-based devices has been suggested to better follow a Weibull distribution or a Generalized Gamma function [103]. We compared the three different distribution models by fitting the SET data from Fig. 3.3 with an iterative Maximum-Likelihood method, in particular focusing on 60 nm devices (**Fig. 3.5**), fitting the data for each discrete time step individually. The mean values overlap with no significant differences, while the SD varies slightly depending on the model. Greater Likelihood coefficient corresponds to a better fitting [104], reported in **Table 3.2** for three different time instants corresponding to a low, medium, and high t_{fall}. The Gamma distribution fits best in all cases, followed by the Normal model. The Weibull model typically produces the worst approximation of the data set. Based on these results, the Gamma distribution provides the best fit. However, the Normal distribution still offers a reasonable estimate, and the mean and standard deviation provide a coherent insight into the population's behavior.

All three models present a minimum SD around 2 µs, compatible with a lower variabil-

t_{fall} [s]	Normal	Gamma	Weibull
10^{-8}	0.82	1	0.41
10^{-6}	0.98	1	0.08
10^{-2}	$5.6 \cdot 10^{-4}$	1	$2 \cdot 10^{-11}$

Table 3.2: Normalized Likelihood estimate of the fitting model, a higher number indicates a better fitting (normalized with respect to the results obtained for the Gamma distribution). The analyses were performed using the *fitdistrplus* package of R software [104, 105].

ity of the SET operation in this t_{fall} range. Indeed, a more reliable SET operation thanks to the t_{fall} increase can be easily achieved below 2 µs with a reduction of V_{SET} from about 3.7 V to 3 V, likely suppressing all the amorphous residuals over the heater/chalcogenide interface. While such a pulse width (Table 3.1) is longer than in similar works [80, 102], the role of size, structure, and materials has a substantial impact on the programming dynamics.

3.4 Programming Endurance and Reliability

With the optimized SET and RESET pulses of Table 3.1, we can reliably program the devices. In this section, we investigate programming cycling endurance to assess device lifespan and failure mechanisms. The protocol is applied to 1S1R devices with a 60 nm CD, using a RESET current overdrive of approximately 30% to induce early degradation and reduce test time. The V_{th} for both RESET and SET states as a function of the programming cycle number are reported in **Fig. 3.6**. After 10^3 cycles, the programming window begins to narrow, in particular due to a reduction of V_{RESET}. First, we model the cycled devices by comparing three distribution functions to highlight the limitations of using mean and standard deviation to represent the appearance of different populations. The analysis of the failed devices allows us to recognize the OTS as the critical reliability component, but a degradation of the PCM is not to be excluded, given the higher current density in the layer due to reduced heater surface [106] The following section focuses on the role of the DPSA architecture in device failure, comparing TCAD thermal simulations with TEM imaging, and confirming that the modified OTS conduction is responsible for the lower V_{RESET}.

3.4.1 Endurance Statistical Analysis

For the previous SET state analysis, we could correctly model the SET V_{th} dispersion with a Gaussian distribution. The analysis holds for functional devices but could be

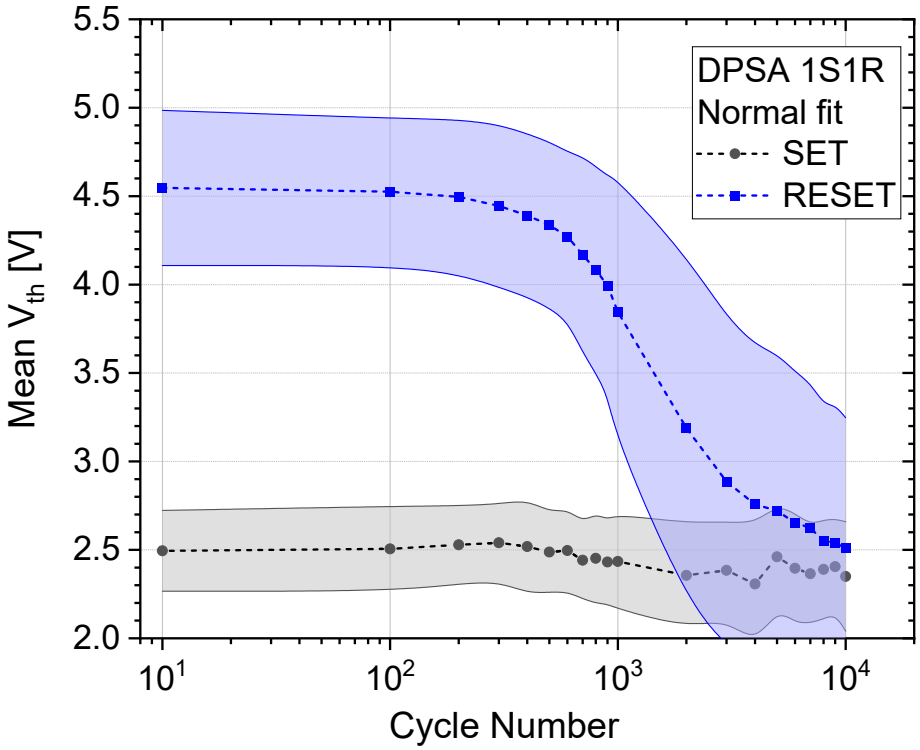


Figure 3.6: Programming endurance for 80 devices with 60 nm Critical Dimension (CD), performed with a current overdrive of + 30% with respect to standard RESET programming current to accelerate device degradation and reduce test time. Both mean and SD values are reported.

misleading when cycle-induced stress alters their electrical behavior. As multiple failure mechanisms may contribute to determining devices' endurance, their threshold voltage distribution may be the outcome of the convolution of multiple populations. By repeating the previous statistical analysis, we report (**Fig. 3.7**) the normalized SD for the SET and RESET distributions along cycling for the corresponding endurance test of Fig. 3.6. Moreover, we could argue that a possible population bias present in early device life disappears with cycling; therefore, the best-fitting model goes from a generalized Gamma to a Gaussian model. One hypothesis to explain this result is that an initial asymmetry of the distribution curve, due to the material composition, disappears along cycling as the devices reach a steady state in the active region, leading to a Normal dispersion. While the SD of V_{SET} is relatively stable, in the RESET it sharply increases when the degradation phenomena start to occur. Comparing Normal, Weibull, and Gamma models, all of them show similar trends. Moreover, starting from 10^3 cycles, we can observe a reduction of the Likelihood estimates for all models (**Table 3.3**). Regarding previous results, the SET state can be well described by a Gamma distribution or accurately approximated as a Normal distribution. This is no longer valid when stress-induced degradation alters device behavior (e.g., in the RESET state), as none of the three proposed models can

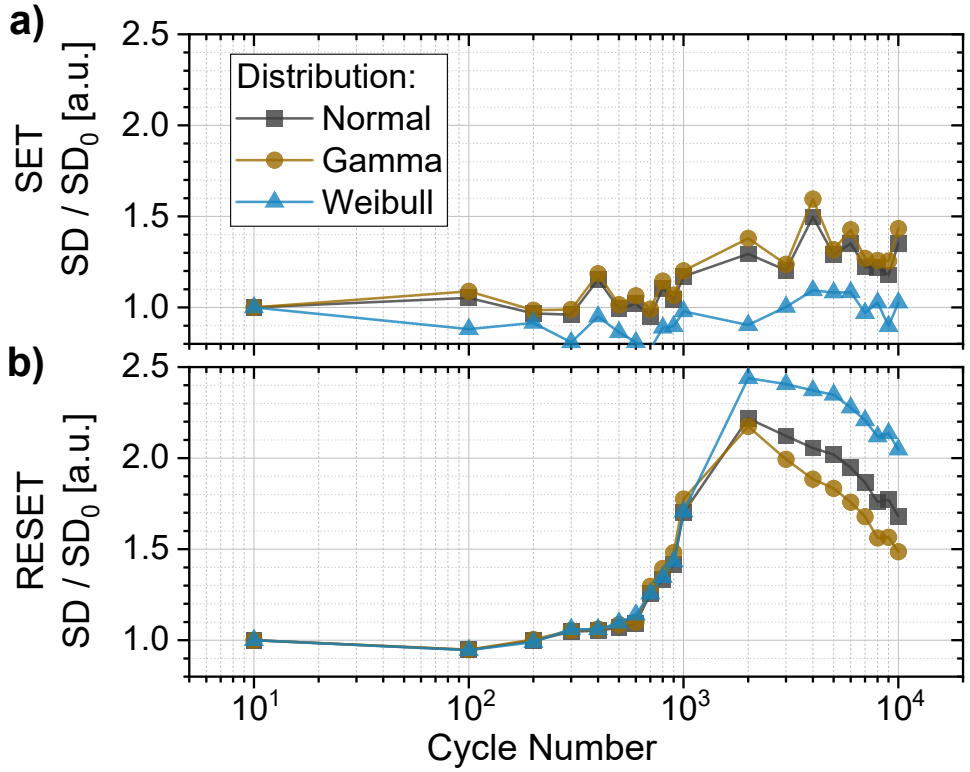


Figure 3.7: (a) Normalized Standard Deviation (SD) for the SET state and (b) for the RESET state of 60 nm devices along cycling. The analysis is performed on a population of 80 devices.

accurately represent the experimental data.

	SET		RESET	
	100 Cycles	10^4 Cycles	100 Cycles	10^4 Cycles
Normal	0.15	1	$3 \cdot 10^{-4}$	$1.6 \cdot 10^{-4}$
Gamma	1	0.8	$3.5 \cdot 10^{-5}$	1
Weibull	$4 \cdot 10^{-7}$	0.5	1	$4 \cdot 10^{-5}$

Table 3.3: Normalized Likelihood estimate coefficients for SET and RESET states for two different cycling conditions (100 and 10^4 Cycles). A higher number indicates a better fitting [104].

However, interpreting the data with a Gaussian fit is misleading, as the data cannot be considered part of a unique population but rather the result of the convolution of two or more different populations (i.e., distributions). The histogram in **Fig. 3.8** reports the RESET threshold voltage after 10^4 programming cycles; there are two main populations at 2 V and 3.6 V, and a third smaller one at 0 V. Devices still preserving a functional RESET state (higher V_{th}) are mixed with failed devices presenting a stuck SET state (lower V_{th}). When the OTS of 1S1R devices crystallizes, it behaves like a resistor, with

no or low residual switching effect. In this case, the V_{th} is missing and is treated as 0 V.

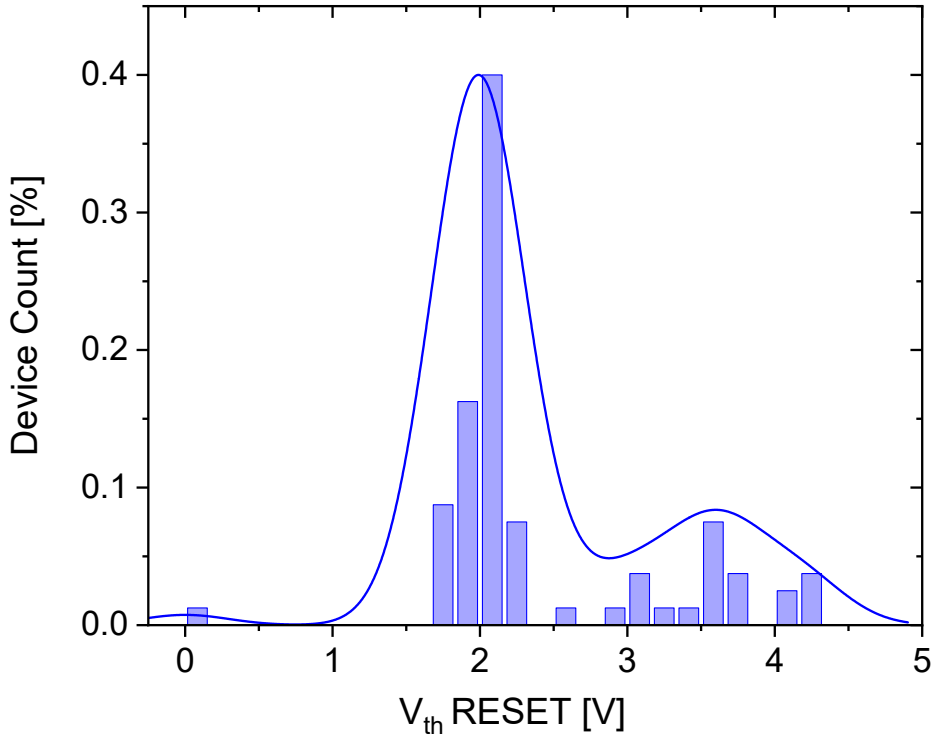


Figure 3.8: RESET V_{th} distribution after 10^4 programming cycles. The blue line represents the smoothed distribution using a Kernel Density Function (KDF) with Gaussian bandwidth. Out of the 80 devices reported, 76% are centered around 2 V, 23% around 3.6 V, and 1% at 0 V.

3.5 DPSA Failure Modes and Thermal Analysis

The V_{th} distribution after failure-inducing stress obtained with 10^4 programming cycles highlights the possible failure modes for 1S1R OTS+PCM devices (Fig. 3.8). Besides the case of a total failure due to excessive current (Open hard fail), which did not occur in our tests, the possible failure modes could be related to:

- (Partial) Crystallization of the OTS selector, leading to higher leakage currents and reduced V_{th} [60];
- PCM SET-stuck condition favored by elemental segregation [107];
- Reduced PCM V_{th} and RESET resistance due to the aforementioned changes in composition.

Other phenomena may further degrade devices' performance, such as interdiffusion of elements from the OTS to the PCM through the intermediate metal [108, 109].

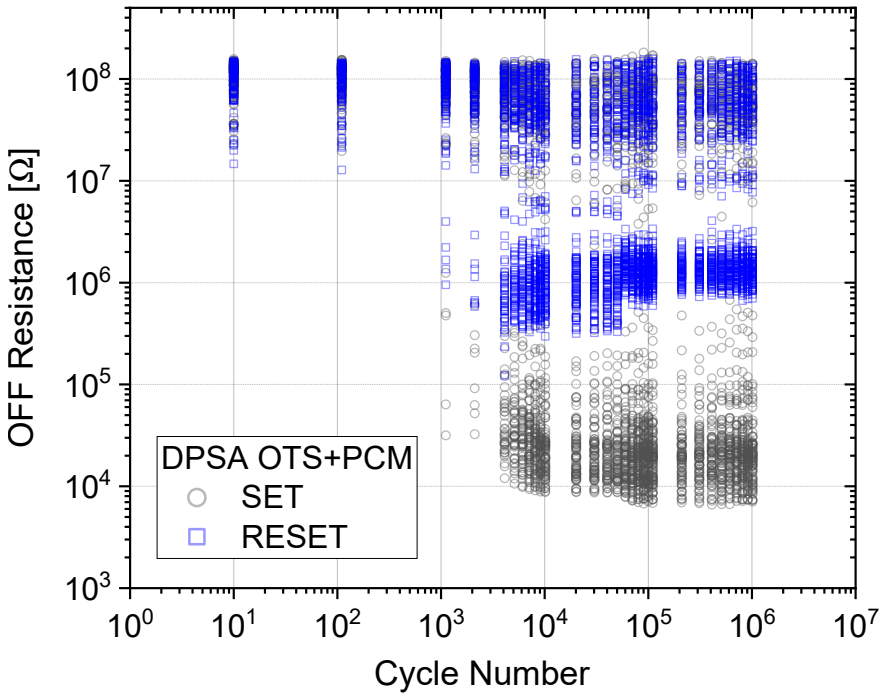


Figure 3.9: OFF Resistance (R_{OFF}) measured at 1 V of OTS+PCM for SET and RESET states along cycling. The results show more than 2000 devices with 100 nm CD.

OTS crystallization appears to be the predominant failure mechanism. **Fig. 3.9** reports the OFF resistance (R_{OFF}) for OTS+PCM devices measured well below threshold (i.e. 1 V). The previously reported reduction of the V_{th} is accompanied by an increased OTS leakage. Two distinct resistance levels appear corresponding to the SET and RESET state of the memory, with resistances compatible with 1R devices (Fig. 3.1). The OTS loses its blocking capabilities, becoming less resistive than the SET PCM. This is not clearly visible from the V_{th} distribution alone (Fig. 3.8), as the threshold voltage of the PCM (i.e., about 2 V) is similar to the one of the OTS and the two populations overlap. Still, a subset of the whole devices is still functional with high OFF resistance and RESET V_{th}.

However, the SET state distribution observed in Fig. 3.6 is incompatible with the hypothesis of a crystallized OTS, as there would be no switching. Indeed, we still detect a V_{th} of about 2 V. We can attribute the presence of a residual threshold switching behavior to a modified OTS subthreshold conduction, with higher I_{leak} making the OTS resistance compatible with the PCM one and unbalancing their ratio (R_{OTS}/R_{PCM}). This partial crystallization of the OTS still exhibits ovonic switching, but with a reduced current window, thus becoming a series resistance to the still functional PCM (Fig. 3.9).

We extracted the device failure rate for increasing programming cycles; establishing a failure event for $V_{RESET} \leq V_{SET}$ or $R_{OFF} \leq$ 10 MΩ conditions (**Fig. 3.10**), that is, the

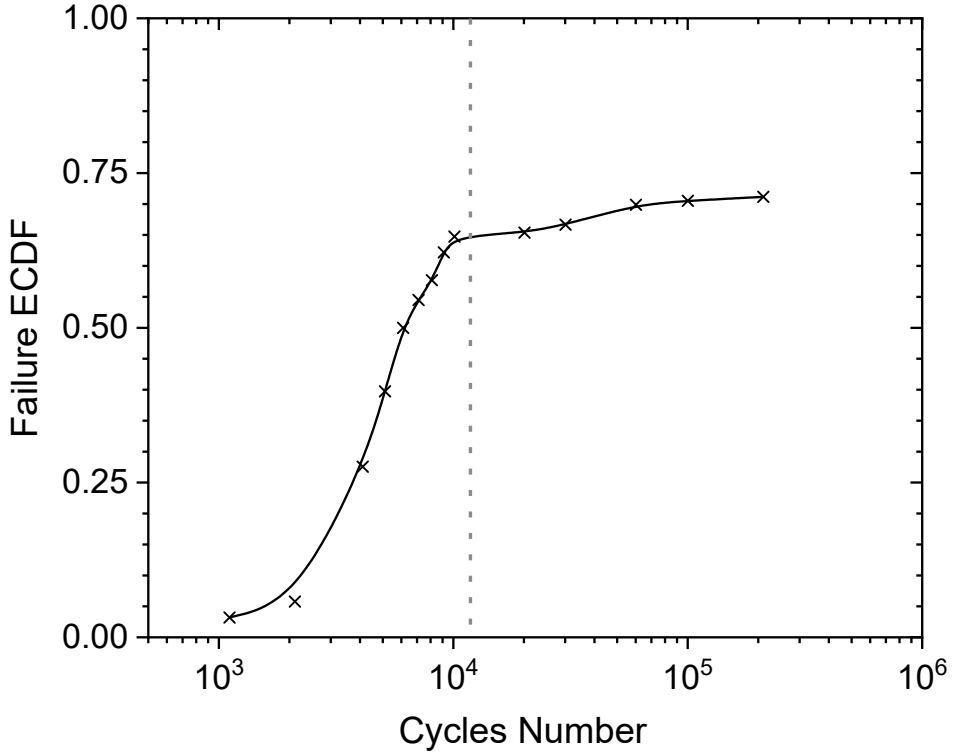


Figure 3.10: Failures Empirical Cumulative Density Function (ECDF) versus programming cycles (SET+RESET). A fail is detected for $V_{RESET} \leq V_{SET}$ or $R_{OFF} \leq 10$ MΩ. The dataset is composed of 156 devices with 100 nm CD.

absence of a voltage window or a crystallized selector. We cycled the devices up to $2{\cdot}10^5$ cycles, discarding the failed ones from further testing to speed up the execution. The failure rate follows approximately a log-normal distribution up to 10^4 cycles, with a cumulative failure rate exceeding 60% of the population. For further programming, the failure rate drastically reduces, suggesting that the first-occurring failures are most likely related to an extrinsic population. As the variability in fabrication may induce early failures, devices that remain functional above 10^4 are more likely to have a longer lifespan. Although not certain, the data presented in Fig. 3.10 suggest that the cell's failure cannot be attributed to a single mechanism. Instead, it likely arises from a combination of several contributing factors from the PCM and the OTS. Optimizing the fabrication steps would introduce a significant improvement in variability and reduce early failures. For example, the uniformity and homogeneity of the chalcogenide layer deposition would strongly impact the device-to-device variability. Nonetheless, optimized programming schemes may delay degradation by preserving the memory and selector material, as done for similar technologies [20]. For instance, the first sequence of cycles could be designed to provide more energy to the system to accelerate the early failures, maintaining only the functional devices.

3.5.1 Co–Integration Reliability Impact

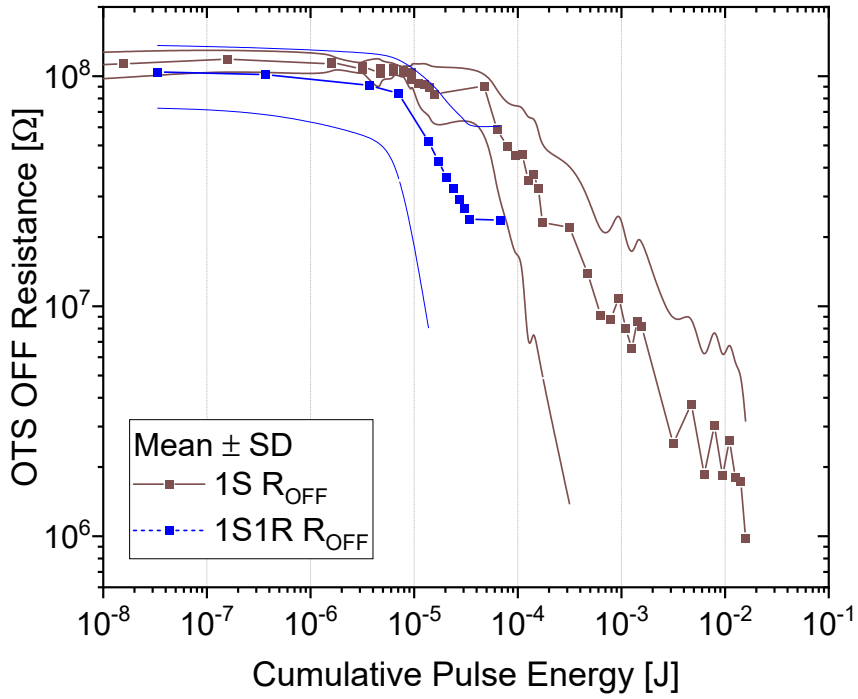


Figure 3.11: Mean and SD R_{OFF} of 1S OTS and 1S1R OTS+PCM versus total pulse energy provided to the OTS.

DPSA architecture and OTS+PCM co-integration have a significant impact on electrical performance (Fig. 3.1), which is more evident for highly scaled nodes [89]. **Fig. 3.11** compares the OFF resistance (R_{OFF}) obtained for 1S1R OTS+PCM cells with 1S OTS for increasing cumulative energy, as cycles cannot be directly compared due to different programming pulses. We consider both cases, where the energy provided only to the OTS is isolated, as shown in **Eq. 3.1**, to exclude the PCM contribution:

$$E_{pulse} = I_{prog}^2 \cdot R_{ON} \cdot (t_{width} + 1/2\ t_{rise} + 1/2\ t_{fall}) \tag{3.1}$$

where I_{prog} is the programming current, R_{ON} is the OTS ON resistance. t_{width}, t_{rise}, and t_{fall} are respectively the pulse width, rise, and fall time. OTS ON resistance is approximated to 300 Ω, extracted from 1S IV curves without a series transistor. The cumulative energy is given in **Eq. 3.2**, where N is the total number of applied cycles:

$$E_{tot} = (E_{pulse,SET} + E_{pulse,RESET}) \cdot N \tag{3.2}$$

The ON resistance depends on the initialization condition of the OTS, on the local temperature, and decreases with increasing bias [97]. Our approximation affects both curves, but does not alter their relative relationship. 1S1R OTS+PCM fails earlier than 1S

OTS, likely due to the increased heat generated by the PCM heater. These results support the role of temperature, suggesting topological and material engineering to improve device longevity.

As a remark, the pulse energy could be calculated using the OTS voltage, which is more difficult to extract in our structure since most of the applied voltage falls on the saturated MOS transistor.

3.5.2 DPSA vs Wall Thermal Behavior

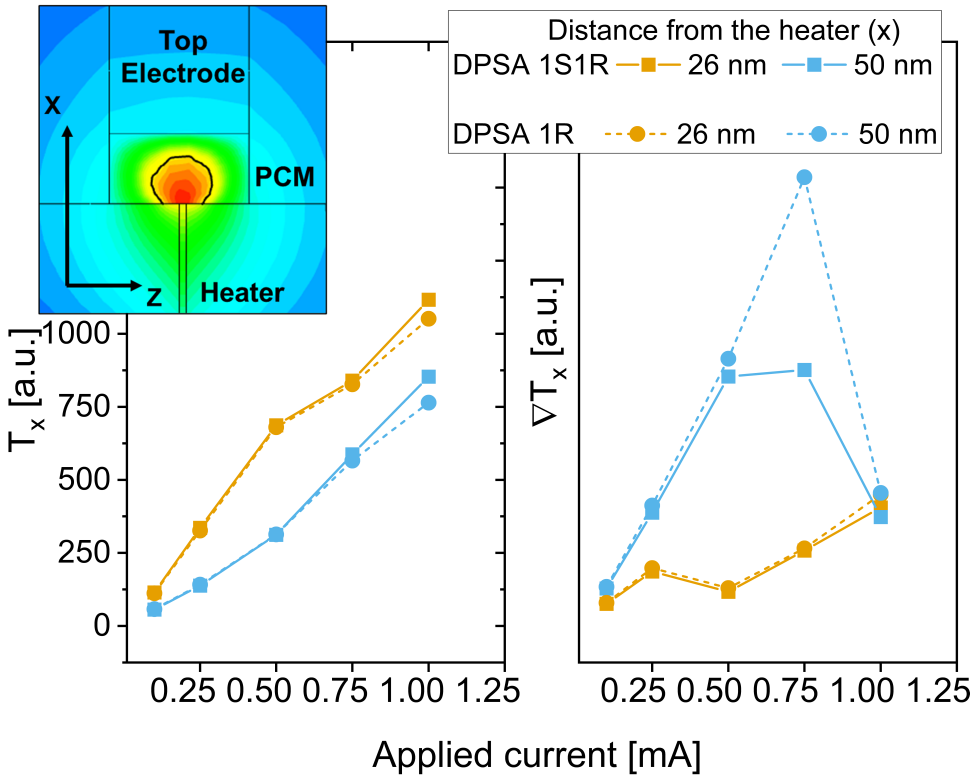


Figure 3.12: Simulated temperature and temperature gradient along the x-axis of the cell for different pulse currents (heater direction shown in the inset). The color scale indicates the data at 26 and 50 nm from the heater/PCM interface.

We conducted TCAD thermal simulation comparing 1R and 1S1R DPSA cells. The temperature and its gradient are reported for increasing pulse current values at different distances from the heater (**Fig. 3.12**). The results show consistently a slightly higher temperature in the 1S1R OTS+PCM cell compared to the PCM alone. The increase in heat confinement has another impact on the cell: it uniformizes the temperature distribution within the cell, reducing the gradient across the cell volume. 1R PCM cells achieve a greater thermal gradient at the limits of the PCM active region, which is responsible for the PCM crystallization [53].

The TEM analysis performed on two cells previously programmed in SET and RESET states showed that almost the whole volume is involved in the phase-change (**Fig. 3.13**). FFT shows crystallinity in a large portion of the SET cell (dashed red line in Fig. 3.13), while the same volume is amorphous in the RESET cell. In light of the previous results, the increased thermal confinement lowers the current required to melt and amorphize the PCM material, which is beneficial for programming performance. On the contrary, the SET operation requires crystal nucleation and growth since there are no crystallites in the cell periphery to grow, explaining the long fall time required to lower the V_{th} in Fig. 3.3.

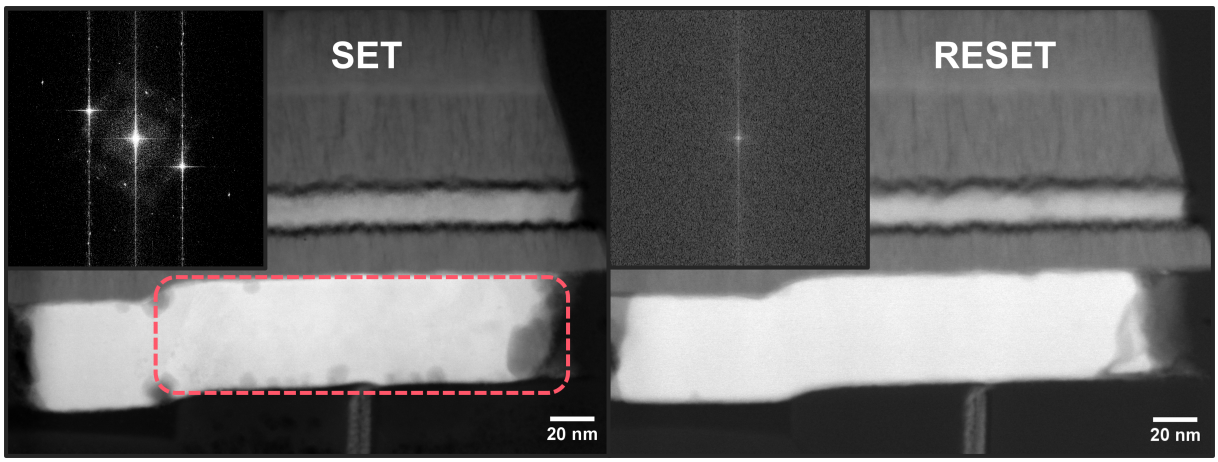


Figure 3.13: TEM images of SET (left) and RESET (right) states of a 1S1R OTS+PCM cell. The inset shows the computed FFT highlighting the crystalline nature of the SET state. The red line bounds the crystallized region.

The TCAD model used does not model phase change in the chalcogenide layer but accounts for changes in thermal and electrical conductivity at the melting temperature via an empirical law [92, 110]. More information on the simulation technique is reported in Section 2.7.

3.6 Conclusions

In this chapter, we examined the programming operation and reliability characteristics of 1S1R OTS+PCM devices based on the Double-Patterned Self-Aligned (DPSA) architecture, comparing their performance with standalone 1R PCM and 1S OTS devices (Fig. 3.1). The integration of GeSbSeN-based OTS selectors with GST-based PCM elements in the DPSA structure demonstrates significant advantages in terms of thermal confinement and programming efficiency. Statistical analysis of threshold voltage distributions reveals that while normal distribution provides an adequate approximation for device characterization, the Gamma distribution offers improved fitting accuracy, particularly for SET states (Table 3.2, 3.3). The analysis validates the use of mean and standard

deviation as reliable metrics for population analysis under normal operating conditions [R9, R7]. However, this approach becomes inadequate when device failures introduce multiple populations and increase dispersion, as demonstrated by the RESET distribution observed after 10^4 programming cycles (Fig. 3.8). The endurance characteristics reveal that programming window degradation occurs primarily through a reduction in the RESET threshold voltage, with the memory window narrowing significantly after 10^3 cycles under accelerated stress conditions (Fig. 3.6). The failure analysis identifies two dominant mechanisms: partial crystallization of the OTS selector, leading to increased leakage currents, and PCM stuck-SET conditions resulting from elemental segregation. The failure rate is increased by the co-integration itself, as evidenced by the earlier failure of 1S1R devices compared to standalone 1S OTS devices when normalized by the cumulative energy delivered to the OTS selector. Devices surviving beyond 10^4 cycles demonstrate significantly improved longevity, indicating that fabrication optimization could substantially enhance device reliability (Fig. 3.10).

The enhanced thermal confinement achieved through the DPSA architecture results in a more uniform temperature distribution within the active volume, as confirmed by TCAD simulations, which show higher peak temperatures but reduced thermal gradients compared to PCM-only devices (Fig. 3.12) [R2]. This thermal behavior directly impacts programming performance: while RESET operations benefit from lower required currents due to improved melting efficiency, SET operations require longer fall times to achieve complete crystallization, as the uniform heating is detrimental for crystal growth. TEM analysis confirms that nearly the entire PCM volume participates in the phase change, with FFT analysis revealing the crystalline nature of the SET states and uniform amorphization in the RESET states (Fig. 3.13). This complete volume switching contributes to the enhanced thermal stress experienced by both PCM and OTS elements during cycling. Due to the amorphization of the whole cell volume during RESET, the SET t_{fall} should allow the formation of new crystallites, as there is no crystal to grow from, significantly reducing the SET speed. The study demonstrates that while the DPSA 1S1R architecture offers promising scalability and programming performance advantages, the co-integration introduces additional reliability challenges that must be addressed through material optimization and refinement of the programming scheme.

Chapter 4

Reading Reliability in (1T)1S1R OTS+PCM

This chapter presents a comprehensive study on the reading reliability of (1T)1S1R memory devices co-integrating PCM and OTS in a DPSA architecture (Chapter 2, 3). The investigation focuses on the impact of repeated read operations, revealing that the SET state experiences a significant threshold voltage (V_{th}) increase — exceeding 20% — as a function of both the read current and the number of applied reading cycles, potentially leading to bit–flip soft failures. Distinct contributions to this voltage shift from the OTS selector and the PCM are isolated and quantified using a dedicated test protocol. An empirical model is developed to describe the evolution of V_{th}, enabling the extraction of key performance metrics such as the Read Window Margin (RWM), the number of read cycles-to-failure, and the maximum feasible Crossbar array size for a given set of specifications. The results highlight that while the RESET state remains stable under read stress, the SET state is susceptible to reliability degradation, especially under higher read currents and frequent switching. The findings provide critical insights for optimizing read operations and device design to enhance the reading endurance and reliability of OTS+PCM Crossbar arrays.

4.1 The Reading Operation Design and Reliability Assessment

As described in chapters 1 and 2, when PCM is co-integrated with a two-terminal nonlinear selector such as the OTS, the read current (I_{read}) depends on both the memory state and the voltage divider between the two components [111]. The typical 1S1R reading principle exploits the device's high ON/OFF current ratio for state discrimination at the reading voltage (V_{read}) (**Fig. 4.1**). When the PCM is programmed in the low resistance

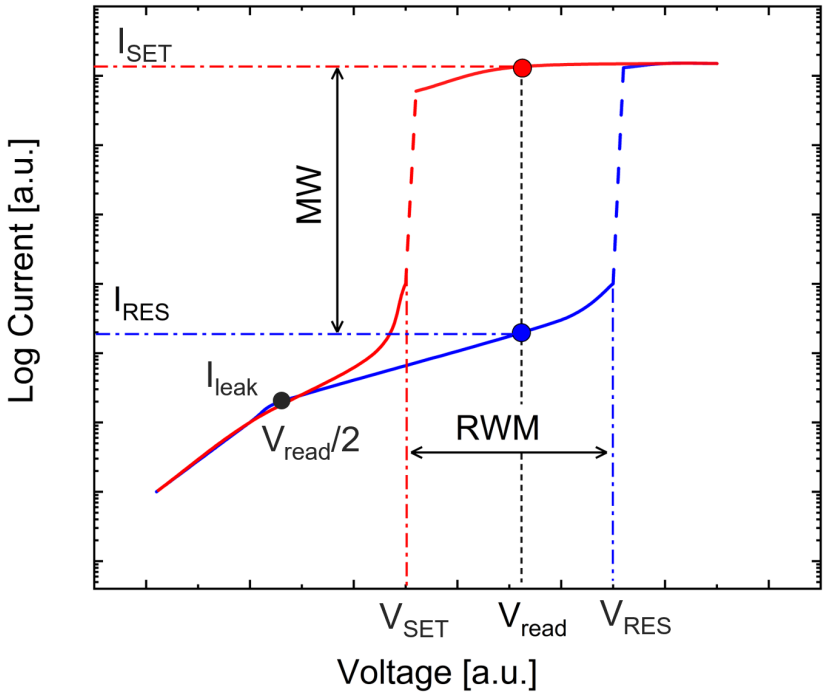


Figure 4.1: Typical IV curve of an OTS+PCM highlighting the key parameters. From left to right: Compliance SET current (I_{SET}); OFF RESET current (I_{RES}); leakage current (I_{leak}); Memory Window (MW); SET threshold voltage (V_{SET}); RESET threshold voltage (V_{RESET}); read voltage (V_{read}), Read Window Margin (RWM).

state (SET), the V_{read} applied within the RWM triggers OTS switching, with a current flow through the device limited by transistor compliance (I_{SET}). Conversely, with PCM in the high resistance state (RESET), neither OTS nor PCM reaches the threshold, preventing switching and resulting in minimal current flow (I_{RES}) determined by the series resistance of both memory and selector.

The reading operation relies on the current Memory Window (MW) defined as the ratio between I_{SET} and I_{RES} (Fig. 4.1). Reading failures (bit-flip) may occur if either when a cell fails to switch at V_{read} due to an unexpected increase in V_{th} from its SET state threshold (V_{SET}) — namely a SET failure — or when a cell incorrectly switches at V_{read} while programmed in the RESET state — a RESET failure. These failures can be either reversible (i.e., "soft failure") or irreversible (i.e., "hard failure") if the cell cannot be reprogrammed in its original state. Ideally, the reading operation should not affect stored information. In conventional PCM, reading is performed at low voltages, with currents sufficiently low to avoid phase changes [44]. However, when in series with an OTS selector, the reading voltage exceeds several Volts. While steady-state current remains limited by the series transistor or the peripheral circuitry, transients during OTS commutation are difficult to estimate and depend on circuit design [112]. Such transients may induce shifts in the programmed threshold voltage state, posing a critical reliability concern.

This chapter supports the hypothesis of a switching-induced threshold voltage shift in OTS+PCM 1S1R cells. We introduce an experimental protocol to isolate the contributions from memory and selector elements (4.1.1) for both RESET (4.2) and SET (4.3) states. We quantify and model the V_{th} increase according to a power law (4.3.1), and extrapolate essential reliability and failure analysis metrics such as the Read Window Margin (RWM) and Cycles–to–Failure (C2F) evolution during repeated cell readings (4.3.2).

4.1.1 Reading Reliability Protocol

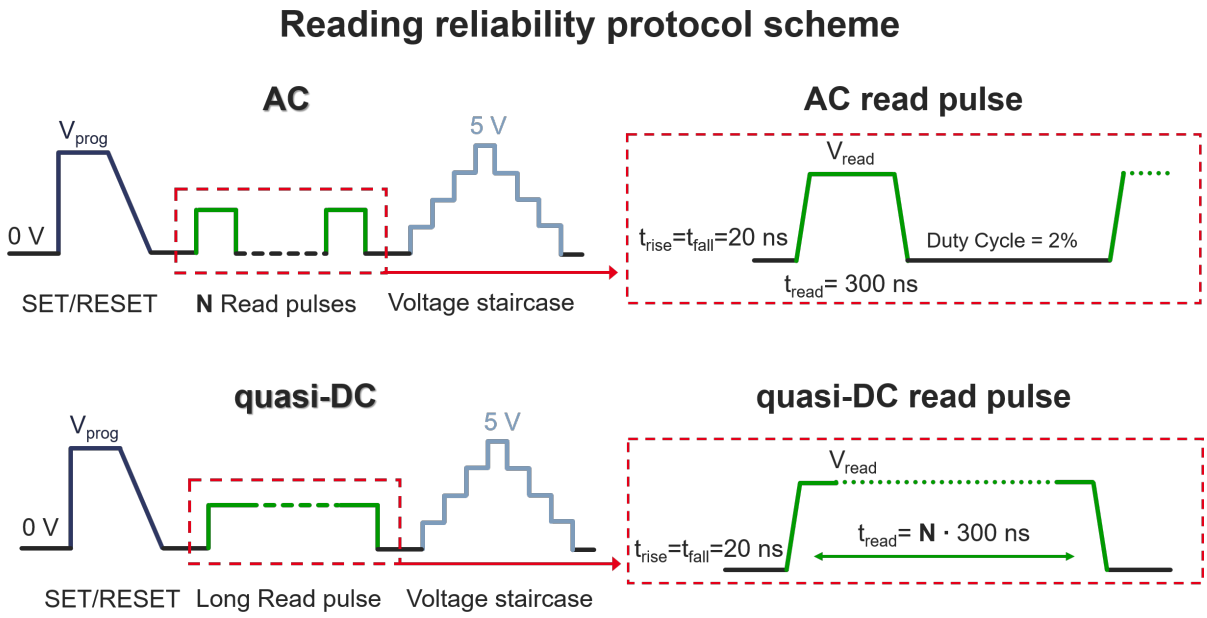


Figure 4.2: *AC* and *quasi-DC* protocols description. The reading pulse for each protocol is detailed on the right. The pulse voltage is applied to the device's top electrode while the current is limited by the 1T series transistor controlling its gate voltage.

We designed a test protocol to investigate reading operation impact and reliability, as illustrated in **Fig. 4.2**. The protocol develops two different approaches — *AC* and *quasi-DC* — differing by the type of reading pulse applied. Both protocols first perform a programming pulse followed by the reading operation itself, and conclude with a staircase up sequence to measure the V_{th}.

The *AC* protocol applies a sequence of N reading pulses, each with duration $t_{read} = 300$ ns and low duty cycle of about 2% (intervals between consecutive pulses of about 1.5 µs). The *quasi-DC* protocol involves a single extended reading pulse (i.e. 100% duty cycle) with duration equivalent to $N \cdot t_{read}$, where N represents the corresponding number of reading cycles in the *AC* protocol.

We selected V_{read} of 3.5 V with I_{SET} ranging from 60 µA up to 400 µA. The device current is controlled by a series transistor through the gate bias voltage, as the OTS provides no intrinsic current limitation. The reading current remains below typical programming currents, which range from 500 µA to 2 mA depending on the device dimensions (Chapter 3).Finally, leakage current (I_{leak}) is measured at $V_{leak} = V_{read} / 2$ to verify the proper OTS recovery of the OFF state.

4.1.2 Materials and Methods

The reading reliability assessment focuses on a $Ge_2Sb_2Te_5$ (GST225) and GeSbSeN (GSSN) Double-Patterned Self-Aligned (DPSA) stack described in detail in Section 2.4, with programming operations for the (1T)1S1R device outlined in Chapter 3. We tested devices from multiple 16 kb arrays, with critical dimensions (CD) ranging from 80 nm up to 300 nm. Each cell in our test vehicle integrates a series transistor (1T), enabling independent control on each device.

4.2 RESET state reading

The PCM in RESET state exhibits high resistivity with V_{th} around 2 V, in series with the OTS featuring a V_{th} of 3 V, resulting in an overall V_{RESET} of approximately 5 V (Chapter 3). When tested with the *quasi-DC* protocol, I_{RES} is sampled during the read pulse, followed by measurement of I_{leak} and V_{th}. **Fig. 4.3a** shows the median V_{th} values across multiple t_{read} intervals. The V_{RESET} remains constant regardless of the reading pulse duration, with no switching observed. The I_{RES} consistently remains below 1 µA (Fig. 4.3b), preserving the programmed PCM state. Moreover, I_{leak} measures more than one order of magnitude lower than I_{read} (limited by instrument resolution), confirming a good preservation of the OTS blocking capabilities. The RESET state demonstrates stability under our reading protocol, with no failure detected. The *AC* protocol produced comparable results (not shown); the equivalent cycle numbers for each corresponding to t_{read} are indicated on the top axis of Fig. 4.3a. The drift phenomenon in amorphous chalcogenides tends to increase the V_{th}, further reducing the risk of unwanted switching [64].

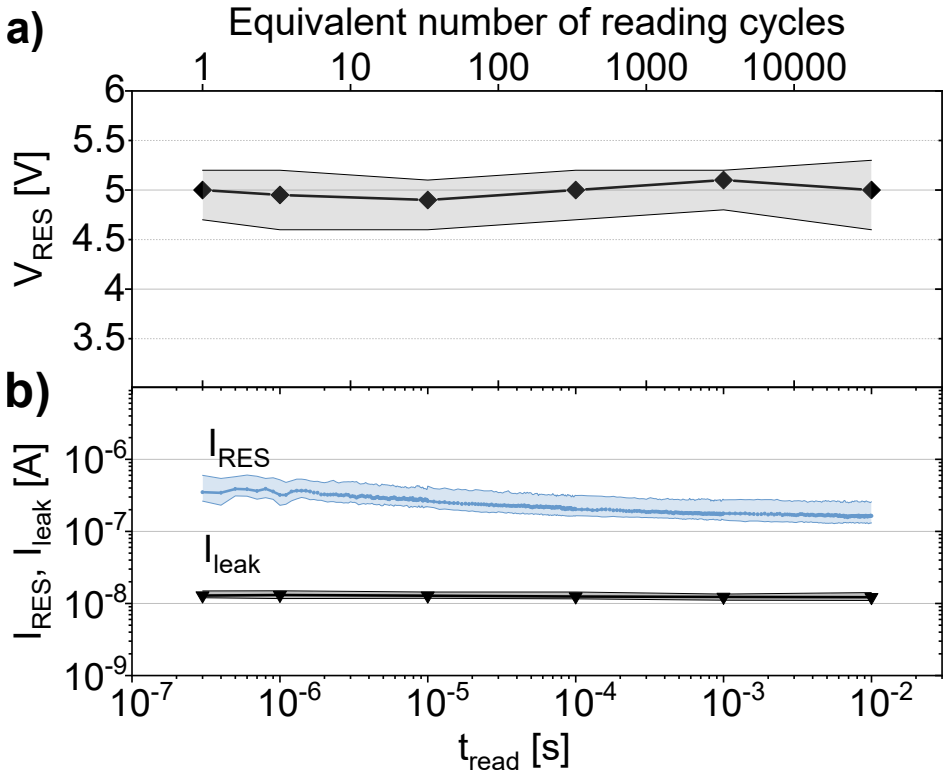


Figure 4.3: V_{RESET} (a), I_{RES} measured at V_{read}=3.5 V and I_{leak} measured at V_{leak}=1.75 V (b) for different read pulse duration t_{read} with the *quasi-DC* protocol (*AC* showed equivalent results, not reported). The graphs report the median values and the Interquartile Ranges (IQR) of about 150 1S1R devices.

4.3 SET state reading

When applying the *AC* protocol to the devices in the SET state, the threshold voltage increases (**Fig. 4.4**) from the as-programmed V_{SET}, by more than 0.4 V on average. This change exhibits clear dependencies on both the number of reading cycles (N) and read current (I_{SET}) applied (represented by color gradient). The original V_{SET} is restored upon the application of the SET programming pulse after each protocol iteration. To correlate this behavior with either memory or selector, we repeated the test on 1R PCM cells (**Fig. 4.5a**). The higher resistance observed at increased I_{SET} demonstrates a direct relationship with SET read current, but the nearly flat slope supports no dependency on the number of reading cycles N. Conversely, when testing 1S OTS selector cells, the threshold voltage increases by more than 200 mV (Fig. 4.5b) with increasing number of reading cycles. In the OTS, no clear correlation with the reading current appears, as all results converge toward the same trend. While the current increase drives gradual PCM amorphization [44], repeated OTS switching triggered by the reading pulses causes a cumulative threshold shift. This switching-induced threshold voltage shift in OTS has not been previously addressed in the literature to our knowledge. In the (1T)1S1R con-

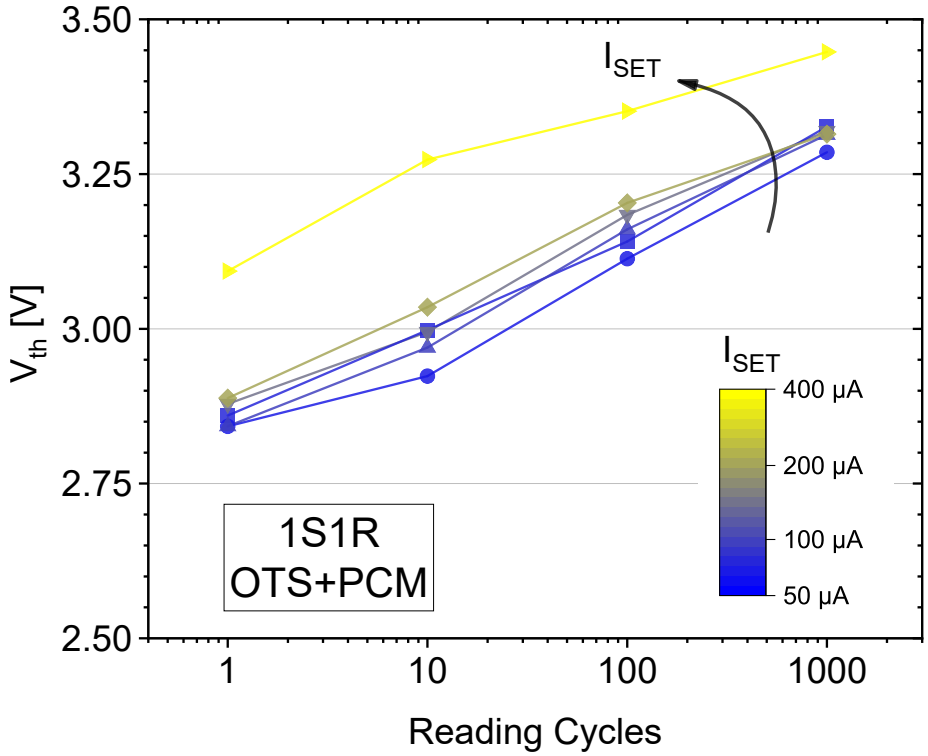


Figure 4.4: V_{th} evolution as a function of the applied N reading cycles. The evolution depends on both the number N of applied reading cycles and the read current I_{SET}. Mean values obtained from a population of about 150 devices.

figuration, the V_{th} shift appears enhanced by the PCM+OTS co-integration, increasing the thermal resistance across the entire stack [113, 114]. The interaction between memory and selector components produces greater V_{th} shifts (Fig. 4.4) than observed in isolated 1S and 1R cells (Fig. 4.5).

Comparing normalized results for both *AC* and *quasi-DC* protocols on (1T)1S1R cell (**Fig. 4.6**), the V_{th} shows a significant impact under *AC* protocol, increasing by more than 20% (approximately 0.4 V). In contrast, during *quasi-DC* protocol, as N increases, we observe a more stable V_{th}, increasing at first but approaching the initial V_{SET} at higher currents. Consistent with the observations in Fig. 4.5, this difference is correlated to the OTS switching count — occurring once per reading pulse in *AC* protocol but only once in *quasi-DC* one. For both protocols, the shift magnitude increases proportionally with I_{SET}.

4.3.1 SET model extraction

We approximated the V_{th} evolution along reading cycles (Fig. 4.6) by the following empirical power law:

$$V_{th}(N) \approx V_{th0} + \log_{10}(N) \cdot \Delta V \tag{4.1}$$

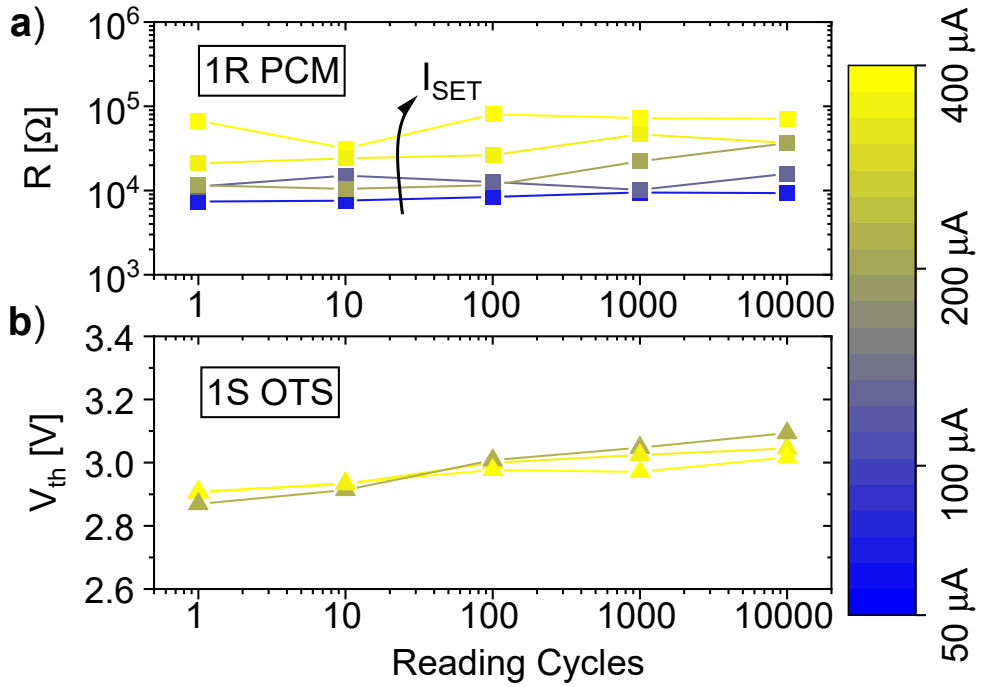


Figure 4.5: 1R PCM resistance (a), and 1S OTS V_{th} (b) for an increasing number N of reading cycles at multiple I_{SET}. Medians extracted from a population of 30 devices each.

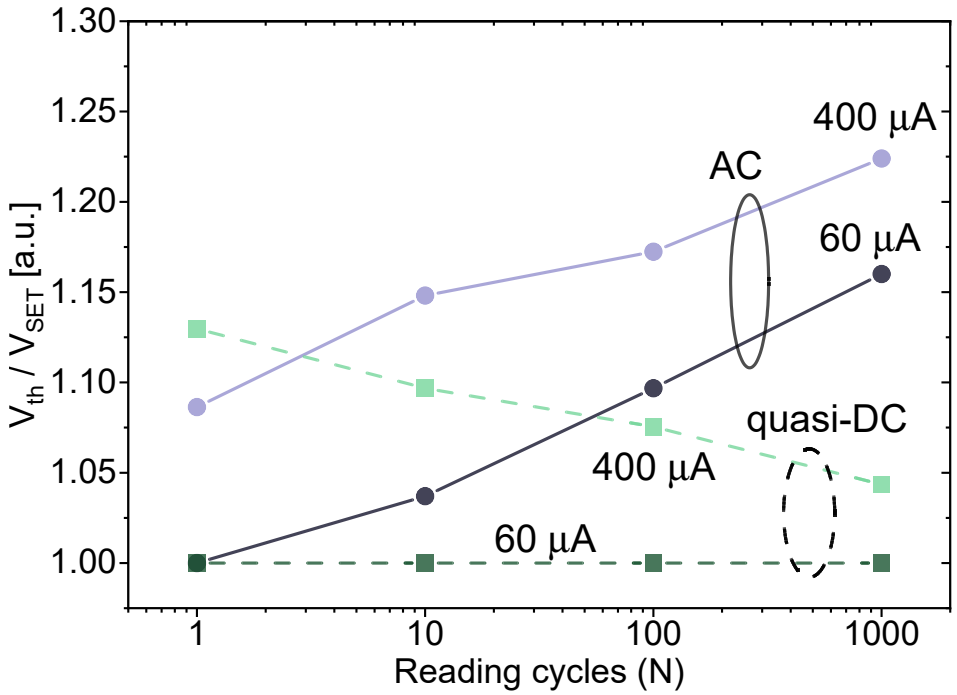


Figure 4.6: Normalized threshold voltage (V_{th}/V_{SET}) as a function of the number of applied reading pulses. The *AC* (solid lines) and *quasi-DC* (dashed lines) protocols at different I_{SET} are shown. The median values are obtained from about 200 1S1R devices.

Where the slope ΔV represents the threshold voltage increase due to the total reading cycles number (i.e. switching events), and V_{th0} is the intercept. We extracted the model

parameters independently for both protocols and each I_{SET} current condition. The empirical model presented in equation (4.1) resembles the one proposed for threshold voltage drift in amorphous PCM [115], with the fundamental distinction that our observed shift arises from accumulated switching rather than aging or structural relaxation.

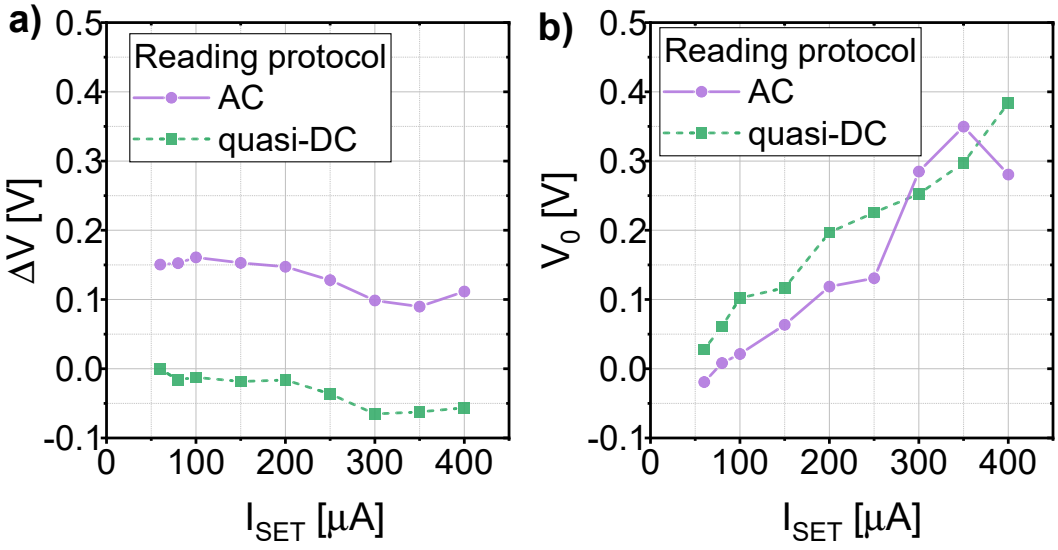


Figure 4.7: The slope ΔV as a function of I_{SET} (a), in accord with equation (4.1). The threshold shift V_0 as a function of I_{SET} (b), in agreement with equation (4.2). The median values are obtained from about 200 1S1R devices.

As shown in **Fig. 4.7**a, the threshold voltage increase ΔV remains nearly independent from the compliance current I_{SET}, maintaining approximately 150 mV for the *AC* protocol while proving almost negligible for *quasi-DC*. This ΔV quantifies the threshold voltage increase per cycle decade. The intercept V_{th0} in equation (4.1) represents the device threshold voltage after a single reading operation at a given I_{SET}. We define it in terms of increase over the as–programmed V_{SET}, namely V_0:

$$V_0 = V_{th0} - V_{SET} \propto I_{SET} \tag{4.2}$$

As shown in **Fig. 4.7b**, V_{th0} varies proportionally with I_{SET} and independently from the protocol. For currents below 100 μA, it corresponds to as–programmed SET threshold voltage, V_{SET}. Our model confirms that ΔV depends solely on selector switching events (as previously shown in Fig. 4.5, 4.6, and 4.7a). This shift is likely due to OTS material evolution induced by current density spikes at the switching event, leading to increased defect localization in the conductive path, thereby increasing the resulting V_{th} [116]. However, the V_0 increase correlates with a partial PCM amorphization resulting from the increased I_{SET}, when approaching current intensities closer to programming rather than reading operations.

The total reading energy of both *AC* and *quasi-DC* protocols is equivalent by design,

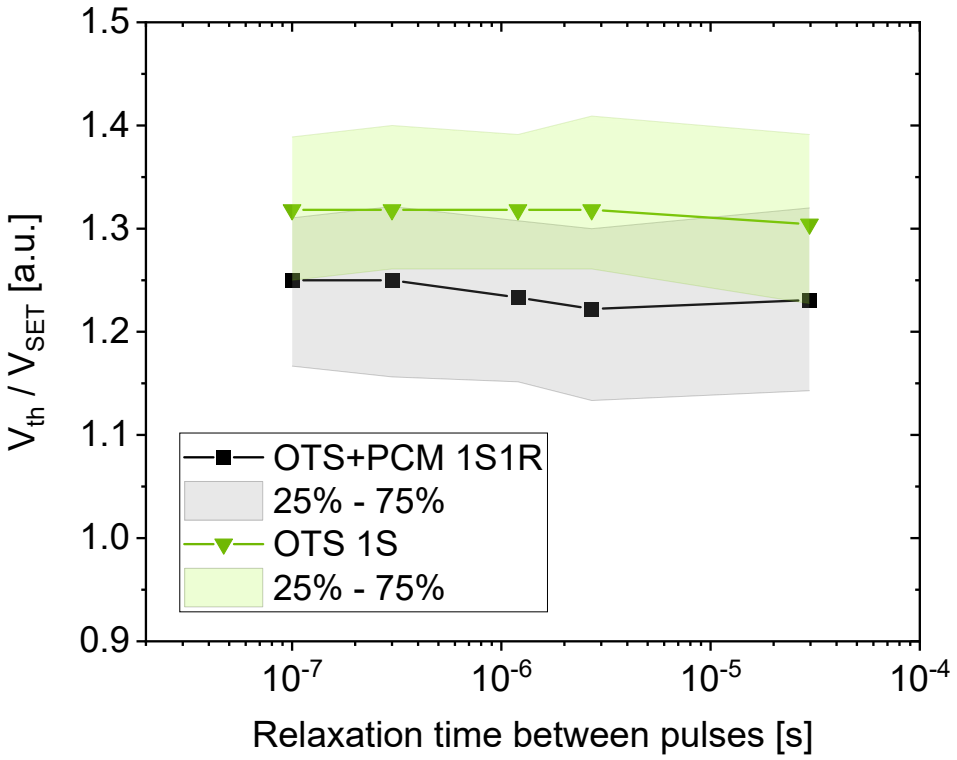


Figure 4.8: Normalized V_{th} for increasing relaxation time between consecutive reading pulses. The devices show limited drift over µs timescale for 1000 applied reading cycles.

given the *quasi-DC* reading duration matching that of N applied *AC* reading pulses (Fig. 4.2). However, the *AC* protocol introduces a relaxation time (a long pulse–free interval) between each pulse. Increasing this relaxation time produced no significant effect on V_{th} for either 1S1R and 1S selector devices (**Fig. 4.8**). This result highlights that the observed threshold voltage shift is not a transient state but a (meta)stable condition persisting over timescales comparable to expected memory reading frequencies, and it is also not related to drift phenomena (Fig. 4.8) at least for the observed timescales [117].

In relaxation time tests (Fig. 4.8), we fixed the single pulse duration to t_{read} = 300 ns. **Fig. 4.9** maintains constant the total pulse period while increasing the duty cycle (i.e., the energy). The figure presents the normalized V_{th} across reading cycles for increasing duty cycles ranging from 30% to 100%, with the latter effectively equivalent to *quasi-DC* protocol. A relatively high I_{SET} of 250 µA was selected to enhance the V_{th} shift.

As the duty cycle increases, the slope decreases, eventually changing sign. Linear regression of data from Fig. 4.9 allows quantification of ΔV shifts under different duty cycles. The extracted slope as a function of the duty cycle is shown in **Fig. 4.10**. Shorter pulse ON times (lower duty cycles) lead to higher threshold increases, while longer reading pulses (higher duty cycles) reduce V_{th} toward the initial V_{SET}. At approximately 50% duty cycle, reading pulses have a minimal effect on V_{th}. This result confirms the

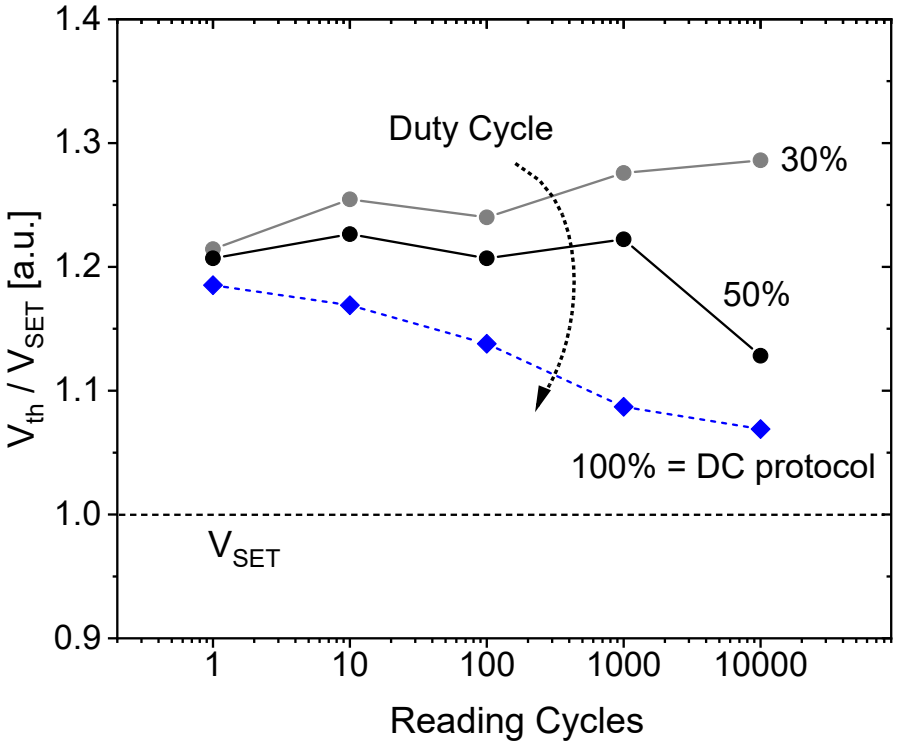


Figure 4.9: Normalized V_{th} evolution as a function of the applied N reading cycles, for different reading duty cycles in the *AC* protocol (solid lines), and for the *quasi-DC* protocol, i.e., 100% duty cycle (dashed line). I_{SET} is fixed at 250 μA.

thermal implication in the observed shift: the shift occurs at the switching event (at the beginning of the reading pulse), and longer pulses promote recovery, reducing the V_{th}, driving it toward the original V_{SET}. This result explains why the V_{SET} is restored upon the application of a programming pulse characterized by a long t_{fall}, in this case, the programming pulse becomes a *quasi-DC* reading pulse (Fig. 4.2).

4.3.2 SET failure analysis

As previously discussed, both I_{SET} and the reading cycles N increase the V_{th}, therefore reducing the RWM (**Fig. 4.11**). Reducing the reading current mitigates the V_0 increase, thus delaying errors to a higher number of reading cycles. The average reading Cycles–to–Failure extracted from the worst 10% extrinsic population is reported in **Fig. 4.12**, clearly demonstrating the correlation between current and bit-flip errors. Bit–flips occur when reading voltage V_{read} fails to produce the expected I_{SET} as the device does not switch ON. With our large sample size (150 devices), reading-induced V_{th} shift first impacts the devices populating distribution tails. **Fig. 4.13** shows the as-programmed SET and RESET distributions before and after 1000 reading pulses: approximately 30% of devices fail with a V_{th} exceeding V_{read}.

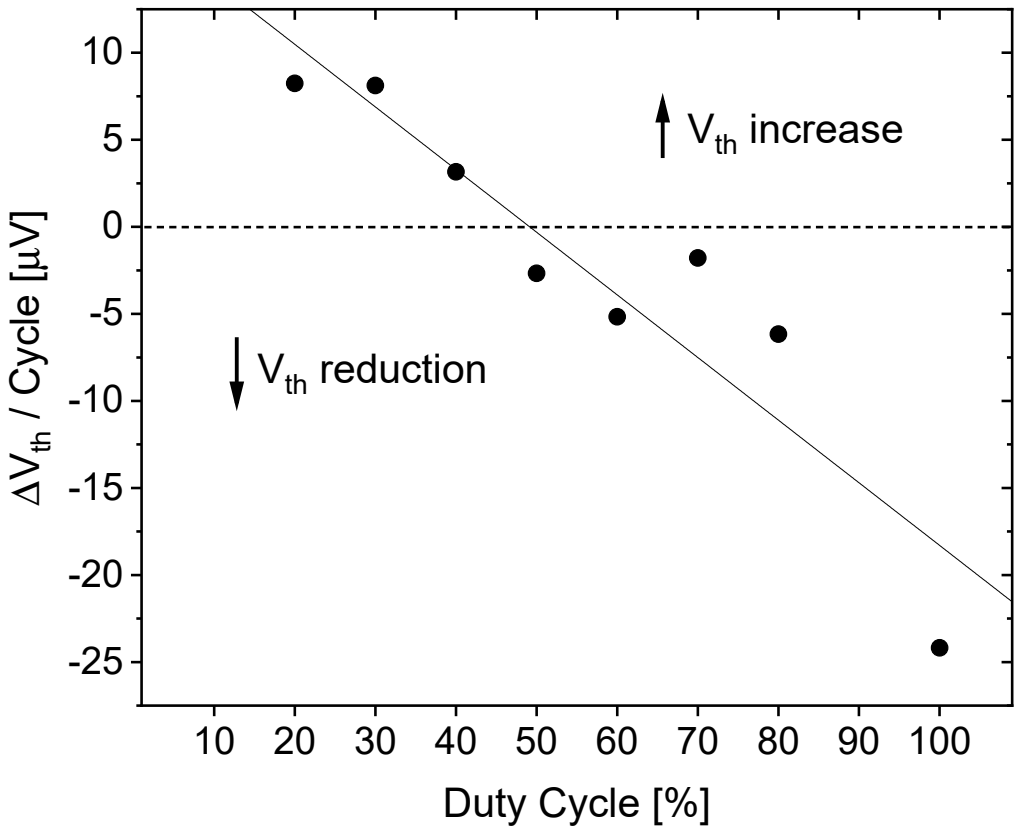


Figure 4.10: Slope extracted from the linear regression of data reported in Fig. 4.9. At a duty cycle of about 50%, the V_{th} is almost constant over cycling. For low duty cycles ($< 50\%$), V_{th} shifts towards higher voltages, while for high duty cycles ($> 50\%$), V_{th} decreases, thereby restoring the V_{SET}.

In Crossbar array design, current Memory Window represents a critical parameter for reading operations due to half-selected devices on the same Word Line (WL), where an I_{leak} increase reduces the MW (Chapter 6). While limiting I_{SET} mitigates RWM impact, it simultaneously reduces the overall current MW (Fig. 4.3). A positive MW ($MW > 0$) remains achievable; however, MW of 10 or greater is typically required to account for extrinsic devices [118]. Based on our results, we can estimate the maximum number of devices achieving optimal RWM and MW, therefore determining the maximum array or sub–array size viable for integration.

Since I_{leak} scales proportionally with the array size, considering M devices in an M×M matrix, we can estimate the Crossbar array current Memory Window as:

$$MW = \frac{I_{SET}}{(M-1) \cdot I_{leak} + I_{RES}} \tag{4.3}$$

Where M-1 devices are half-selected on the same WL. We assume equivalent I_{leak} for both SET and RESET states (a minor approximation), with the selected device pro-

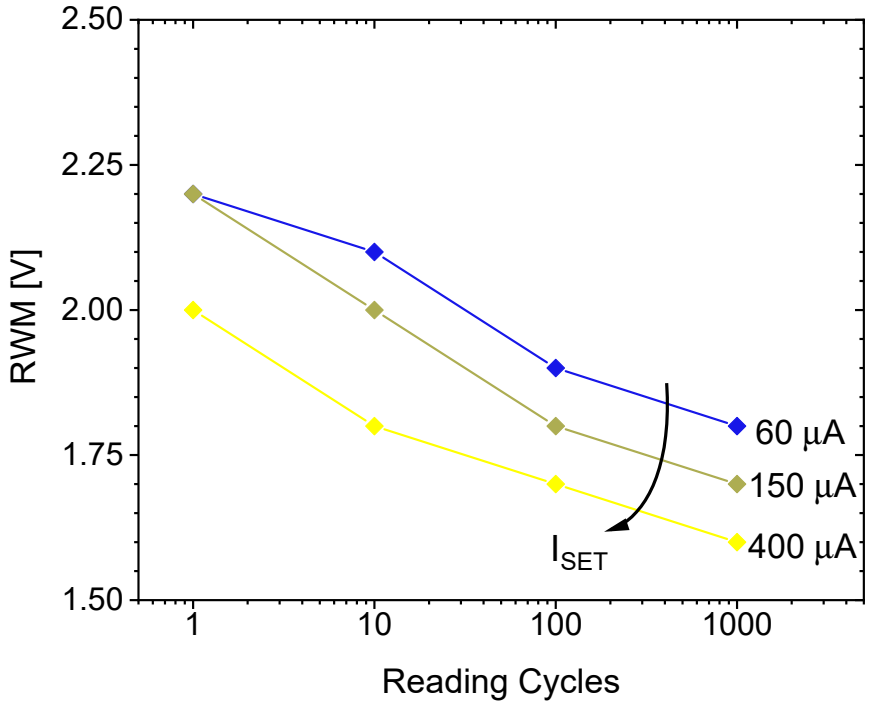


Figure 4.11: Voltage Read Window Margin (RWM) evolution over repeated reading cycles for different I_{SET}.

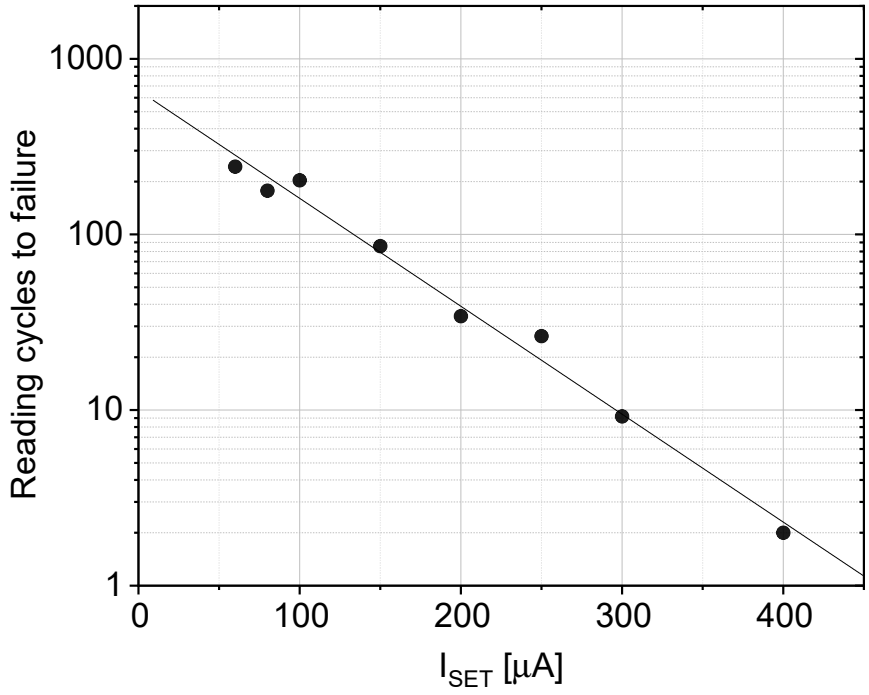


Figure 4.12: Number of reading cycles to reach a soft failure for the extrinsic 10% of the devices. The lower the current, the higher the number of reading operations that can be performed before reaching a soft failure condition.

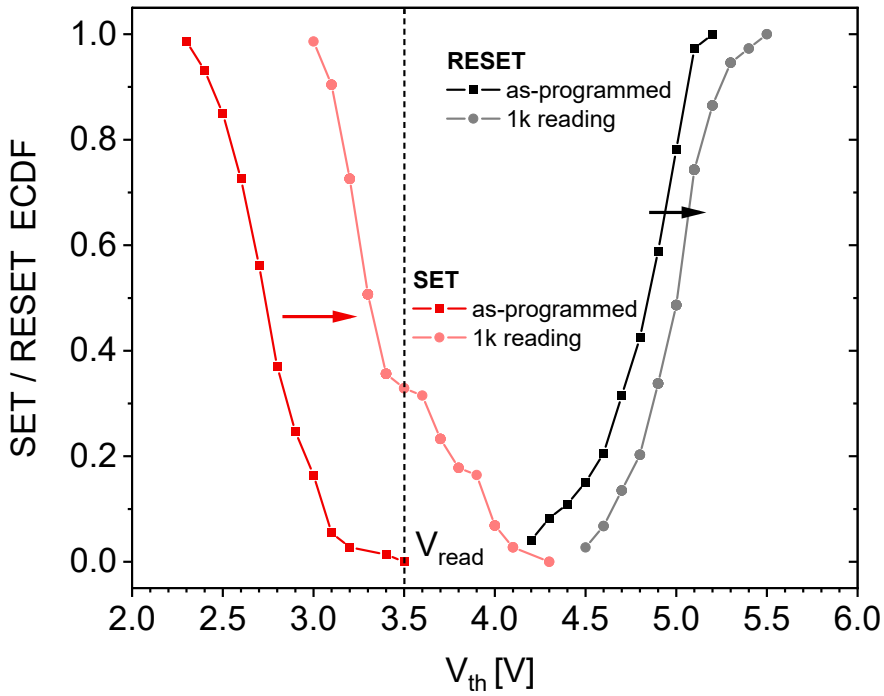


Figure 4.13: Empirical cumulative density function (ECDF) of both V_{SET} and V_{RESET} before and after 1k reading cycles (150 devices, read at 100 µA). After multiple readings, the V_{SET} shifts towards higher threshold voltages, causing both a reduction in the RWM and soft failures for devices whose V_{th} is higher than V_{read}.

grammed in the RESET state (worst-case scenario) [80]. **Fig. 4.14** illustrates the trade-off between I_{SET} and Crossbar array size, where reading current minimization competes with memory window maximisation to achieve the largest possible array size.

We delimited reading and programming regions with a vertical line, and a minimum MW of 10 with a horizontal line. The bounded region provides the limits for the maximum Crossbar Array size. With our device specifications, we could achieve a reliable 64×64 Crossbar array size, but the impact of repeated reading should be taken into account, for example, by implementing an optimized read and verify scheme or a read and reprogram operation.

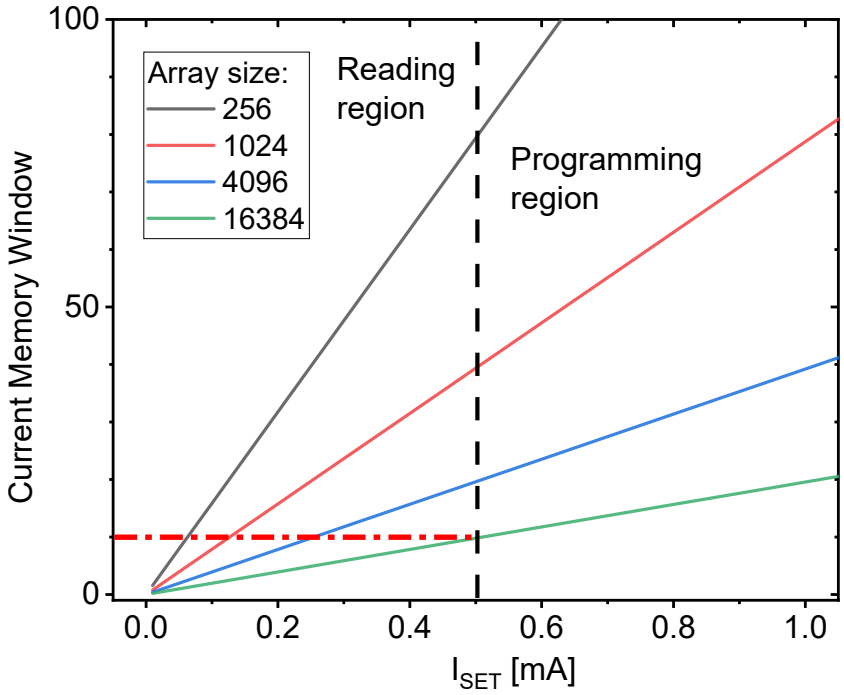


Figure 4.14: Maximum number M of devices (either rows or columns) in an M×M matrix for different MWs, extrapolated from equation (4.3). The vertical dashed line separates the reading (left) and the programming (right) current regions. The red horizontal line defines a minimal MW of 10.

4.4 Results Discussion

In the SET state, the reading operation affects the information stored in 1S1R OTS+PCM devices even when limiting the read current I_{SET} (Fig. 4.4). Prior literature [55] suggests the presence of a threshold voltage drift caused by phase-change structural relaxation, leading to time-dependent resistance evolution (i.e., drift phenomenon). Our observations, however, reveal an OTS V_{th} shift induced by repeated switching (Fig. 4.5 b). Interestingly, the temperature gradient generated by the applied current does not affect the selector material; rather, the repeated switching events drive the observed changes. While V_{th} evolution can occur under extensive cycling or aging [119], these typically operate on timescales longer than our experiment. In our test protocols, V_{th} consistently returns to its initial value after each programming pulse in both 1S and 1S1R devices (Fig. 4.6), confirmed through repeated testing and previous studies [72].

The post-switching V_{th} increase, more pronounced in the 1S1R configuration, likely stems from local structural changes of the selector, possibly through the annealing of shallow defects that broaden the bandgap after each commutation. Additionally, the conductive filament radius during the ON state varies with current [63]. Higher pulse energy during programming involves a greater portion of the material volume, and when

the selector switches off, new defects are "frozen" in place, restoring the initial condition [34].

In the 1S1R device, we observe larger V_{th} shifts under *AC* protocol, which cannot be fully explained by the selector drift hypothesis. We hypothesize a partial amorphization of the PCM-heater interface, a phenomenon not apparent in 1R devices due to stronger thermal confinement in OTS+PCM stacks (Chapter 3). The overall thermal resistance (R_{th}) increases from additional interfaces and amorphous OTS layer thickness, impeding heat dissipation through the top metal line, generating higher local temperatures near the hot-spot.

Both switching events and thermal confinement contribute to the increase of bit-flip soft errors (Fig. 4.12). The persistence of the V_{th} shift over microsecond timescales during intensive read operations presents a significant concern for failure analysis (Fig. 4.8), as maintaining data integrity may require periodic reprogramming of the memory with refresh-like operations. A potential mitigation strategy involves read pulse shaping to reinforce SET states by optimizing current and pulse duration, although this would compromise reading speed.

Reading reliability in 1S1R devices depends on device architecture and dimensions, which affect thermal properties. To reduce energy consumption, I_{SET} should be minimized, improving the Read Window Margin (Fig. 4.11). However, this conflicts with requirements for a large memory window and SET-reinforcing read pulses. Careful cell design and material engineering may reduce this phenomenon, as eventual selector memory effects are related to the composition [R6].

4.5 Conclusions

This chapter evaluates the impact of the reading operation on threshold voltage (V_{th}) reliability in programmed states of DPSA 1S1R OTS+PCM devices, reporting for the first time at our knowledge the switching-induced threshold voltage shift in both OTS and OTS+PCM [R8, R3]. While RESET state demonstrate a high stability during reading operations, SET state experience V_{th} increase exceeding 20% of initial V_{SET} leading to bit errors.

Our SET state V_{th} model evidences the dual nature of the shift: a gradual increase related to OTS switching during reading (ΔV), and a constant increase proportional to the reading current I_{SET} (V_0), likely related to partial PCM amorphization. Reducing I_{SET} increases the number of tolerated reading cycles before a soft failure. Reading pulse duty cycles determine the voltage shift direction, suggesting a possible mitigation path by careful optimization. Reducing I_{SET} is crucial for minimizing the mean reading-cycles-to-failure.

In Crossbar arrays, high I_{SET} remains important for preserving reading current MW.

Therefore, I_{SET} selection requires careful optimization to maximize RWM, MW, and the maximum reading cycles number, providing a comprehensive reading reliability assessment protocol.

In light of our results, we provide practical design estimation specifically addressing the reading reliability issue not investigated by previous studies [120]. Equation (4.3) and Fig. 4.14 highlight several potential improvement pathways:

- Reduction of leakage current through material design and CD downscaling;
- Material optimization to mitigate cumulative switching effects;
- Cell design and encapsulation material engineering to improve thermal behavior during programming and reading;
- Reading scheme and pulse optimization to minimize energy consumption and V_{th}.

Chapter 5

Material Engineering for OTS and PCM Optimization

This chapter presents a comprehensive investigation of material engineering strategies for PCM and OTS optimization. The study focuses mainly on the antimony-tellurium ratio (Sb/Te) optimization. Exploration of Ge-rich PCM, Multilayer OTS, and As-based OTS is also presented. Finally, the best-performing PCM and OTS compositions are co-integrated and evaluated in a DPSA architecture.

Antimony plays a crucial role in GeSbTe alloys, enhancing SET speed and improving cycling endurance stability in Sb-rich compositions [51]. Previous studies highlighted the benefits of an increase in antimony content but focused mostly on Sb-rich alloys, not considering the key role of the antimony–tellurium (Sb/Te) ratio, especially in compositions characterized by a congruent crystalline phase [121]. Our investigation on the Sb/Te ratio aims to improve devices' SET speed and endurance without compromising on the resistance window, targeting threshold voltages compatible with standard materials (Section 5.1). Three congruent GeSbTe alloys with increasing Sb/Te ratio were investigated through physical and electrical characterization (**Fig. 5.1**). The thin film material characterization includes resistivity measurements, X-Ray Diffraction, and Transmission Electron Microscopy. Electrical characterization involves investigating programming speed and reliability. The investigation revealed that increased antimony content suppresses the metastable cubic phase typical of low Sb/Te materials (e.g., $Ge_2Sb_2Te_5$, $Ge_1Sb_2Te_4$), enabling direct amorphous-to-hexagonal crystallization with increased activation energy and fast growth speed. The $Ge_1Sb_4Te_4$ (GST144) alloy with Sb/Te = 1 emerged as the optimal tradeoff, combining the fast sub-100 ns SET speed characteristic of Sb-rich materials with the large resistance memory window typical of lower Sb/Te ratios. Reliability assessment demonstrated high cycling endurance and confirmed device stability, extrapolated to over 10^8 low-energy programming cycles.

Complementary to Sb-rich materials, Ge-rich alloys are particularly interesting for

automotive embedded applications where data retention is the most critical reliability metric [31]. These compounds suffer slower SET speed and present larger variability than common $Ge_2Sb_2Te_5$; for this reason, we perform a preliminary evaluation of Germanium-rich GeSbTe alloys (Section 5.2). The devices showed promising preliminary electrical results, with reasonable programming speed and endurance.

OTS materials, as well as PCM ones, require careful composition tuning and optimization to enhance their electrical performance. In particular, the intrinsic variability of the threshold switching and the high-energy electroforming operations are two critical issues that can be addressed from a material perspective. Targeting variability reduction and reliability improvements, we explored the Multilayer integration of our reference nitrogen-doped GeSbSeN-based OTS material (GSSN) (Section 5.3.1). Multilayer integration showed comparable performance to bulk materials, which could be beneficial for compositional control and reduced variability. We confirmed the variability reduction achieved through the implementation of a carbon underlayer, which improves surface contact and prevents intermixing with the bottom and top electrodes.

To address the electroforming operation, targeting forming-free alloys, we investigate alternative arsenic-based selenides OTS compositions (SAGS and Si-doped As_2Te_3) to achieve forming-free selector operation and to reduce threshold voltages (Section 5.3.2). We present promising preliminary results for applications requiring sub-3.3 V operation.

The chapter concludes with a co-integration assessment of optimized PCM compositions with GSSN multilayer OTS in the DPSA architecture. GST144 PCM confirmed its superior voltage Read Window Margin and programming current advantages over standard $Ge_2Sb_2Te_5$ and Sb-rich alloys (Section 5.4). These findings establish a material engineering basis and validation for next-generation OTS+PCM technologies, suggesting the pathways for further material optimization to improve speed, reliability, and scalability required for advanced memory applications.

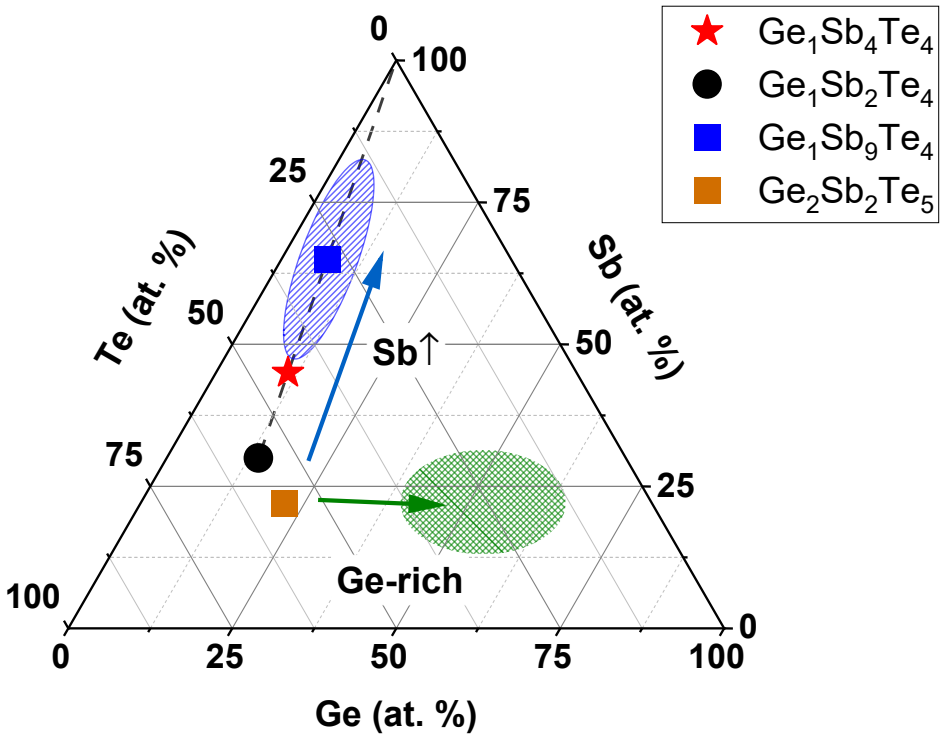


Figure 5.1: Ge–Sb–Te ternary diagram with the studied compositions. The blue region highlights the Sb-rich alloys along the GST124–Sb tie line corresponding to an increase in the Sb/Te ratio. The green region corresponds to the Ge-rich alloys. Standard GST225 reference composition is reported as an orange square.

5.1 Sb/Te ratio tuning in GeSbTe-based PCM

This section investigates the effects of the Sb/Te ratio on the crystallization kinetics, programming characteristics, SET speed, and endurance in GeSbTe-based Phase-Change Memory. Previous studies have highlighted the role of antimony addition in $Ge_2Sb_2Te_5$ (GST225), enabling rapid SET speed due to the enhanced crystallite growth rates facilitated by the abundance of Sb–Te bonds [46, 122]. The Sb in excess can be responsible for partially filling the available structural vacancies of the stoichiometric $Ge_2Sb_2Te_5$, suppressing the metastable cubic phase and leading to a direct transition from amorphous to trigonal (or hex) crystalline phase [123]. Previous works have focused mainly on Sb enrichment in stoichiometric alloys, rather than specifically obtaining congruent compositions.

In this study, we propose the investigation of congruent alloys lying on the pseudo-dash binary tie line connecting $Ge_1Sb_2Te_4$ and Sb (**Fig. 5.1**), exploring the effects of the progressive Sb/Te ratio increase. The three finely tuned GeSbTe (GST) alloys are $Ge_1Sb_2Te_4$ (GST124), $Ge_1Sb_4Te_4$ (GST144), and $Ge_1Sb_9Te_4$ (GST194), with increasing Sb/Te ratio of 0.5, 1, and 2.25.

First, we assess the material stability of the alloys by presenting physical characterization results on thin films, which demonstrate the stability of the antimony-rich crystalline phases and the suppression of the metastable cubic phase. Resistivity as a function of temperature (R–T) measurements and the extraction of the Activation Energy (E_a) for crystallization reveal a progressive increase in the stability of the alloys against nucleation with an increasing Sb/Te ratio. X-Ray Diffraction (XRD) analysis, combined with Transmission Electron Microscope (TEM), confirms the absence of segregation and the congruent nature of the explored compositions, highlighting a fast growth-dominated crystallization in alloys with a higher Sb/Te ratio. When the antimony content is elevated, Sb planes alternate with Sb_2Te_3 planes [121]. Although not homogeneous, these compositions do not segregate [51]; we therefore refer to them as "congruent" for the scope of this work.

The alloys were integrated in a "Wall" self-aligned (1T)1R architecture with Critical Dimension (CD) down to 40 nm (Section 2.3). The increased Sb/Te ratio enables a more reliable and faster SET operation, despite a decrease in the Resistance Window (RW) for large Sb/Te ratios. Reliability assessments yield promising results in terms of cycling endurance, with no apparent material degradation extrapolated up to 10^8 cycles for low-energy programming. Increasing Sb enables improved SET operation reliability; however, a too high Sb/Te ratio reduces the RESET state resistance, affecting the final PCM memory window. For the first time to our knowledge, this work successfully integrates GST144 alloy, which features a high SET programming speed typical of Sb-rich

compositions (e.g., GST194), thanks to the suppression of the cubic metastable phase, and a wide RW typical of standard low Sb/Te ratio compositions (e.g., GST124). Intermediate Sb/Te ratio of $Ge_1Sb_4Te_4$ provides the best trade-off between the high SET speed of $Ge_1Sb_9Te_4$ and the large memory window of $Ge_1Sb_2Te_4$. Therefore, we show how Sb/Te tuning in GST alloys represents a key knob for performance optimization in Phase-Change Memory.

Finally, we propose a multilayer integration approach as a means to further enhance device performance. The studied compositions are then co-integrated with an OTS selector and compared to standard GST225 in the later Section 5.4.

5.1.1 Material Stability Analysis

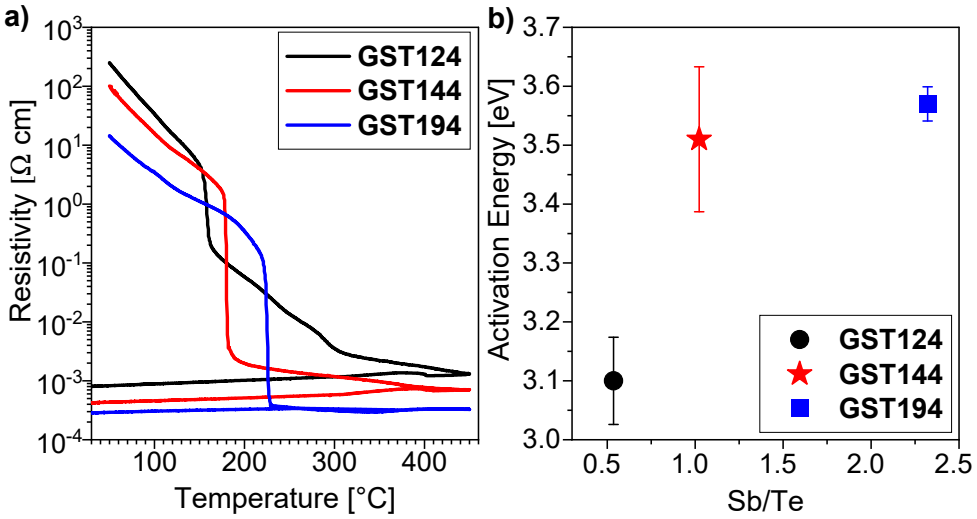
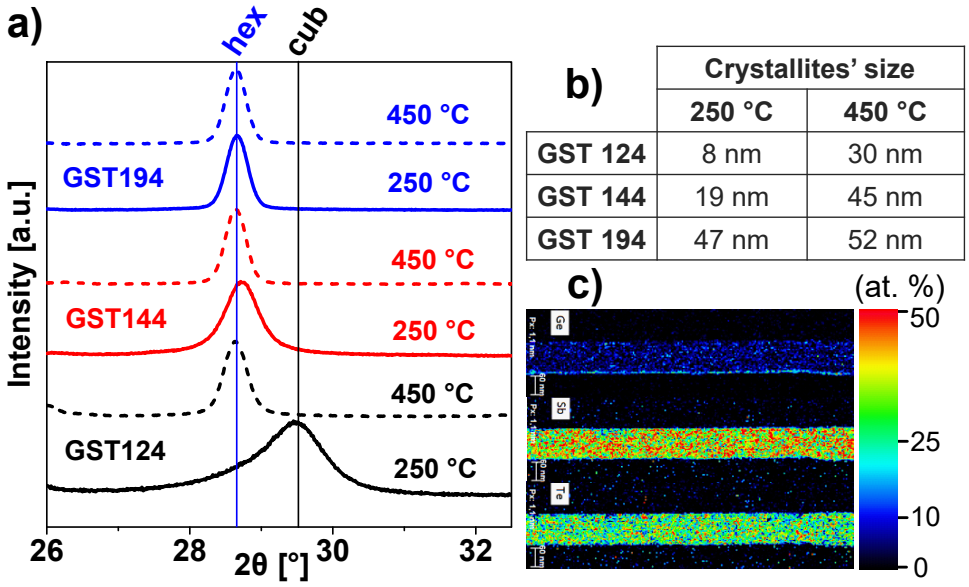


Figure 5.2: a) R-T measurements for amorphous GST thin films. The three compositions stabilize into a stable hex phase, while GST144 and GST194 reach stability directly upon crystallization, and GST124 transitions through an intermediate cubic phase. b) Crystallization activation energy for increasing the Sb/Te ratio, obtained by the Kissinger method.

We deposited GeSbTe films by PVD co-sputtering of GST124 and Sb targets to obtain the desired Sb content. The thin films were analyzed using resistivity measurements, XRD, and TEM [1].

Fig. 5.2a illustrates the sheet resistance of GST thin films as a function of temperature (RvsT) at a fixed heating rate of 10 °C/min. The crystallization temperature of the GST thin films increases with the Sb content. GST124 (Sb/Te = 0.5) first crystallizes into a metastable cubic phase at 157 °C, transitioning to a stable hex phase at 290 °C. In

[1] The physical characterization of full-sheet samples was performed by Oumaima Daoudi. A description of the techniques along with the results were published in [124, 125, R1].



b)	Crystallites' size	
	250 °C	450 °C
GST 124	8 nm	30 nm
GST 144	19 nm	45 nm
GST 194	47 nm	52 nm

Figure 5.3: a) XRD patterns obtained on thin films after annealing at 250 °C and 450 °C. b) Average crystallite size after annealing both at 250 °C and 450 °C, extracted with the Scherrer equation from the FWHM of the Bragg peaks. c) Energy Dispersive X-ray (EDX) spectroscopy of a GST144 film after annealing at 450 °C, showing the uniformity of the layer and no apparent elemental segregation.

contrast, GST144 and GST194 (Sb/Te $\geq$ 1) crystallize directly into a low-resistive hex phase. After crystallization, GST144 continues to exhibit an evolution towards even lower resistance (i.e., crystalline growth), whereas GST194 remains stable. Using Kissinger analysis [126], we extracted the Activation Energy of crystallization (E_a) for the first crystalline transition. Fig. 5.2b shows that E_a increases with the Sb/Te ratio. Samples with Sb/Te $\geq$ 1 require a higher energy for nucleation, as crystallization does not pass through the cubic phase, as observed in GST124.

To confirm the nature of the crystalline phase, we performed XRD measurements on samples annealed respectively at 250 °C and 450 °C (**Fig. 5.3a**). GST124 annealed at 250 °C exhibits a peak corresponding to the cubic (cub) phase, while samples with increased Sb/Te ratio show only the Bragg peaks corresponding to a hex phase, in agreement with previous results [54, 127]. After the annealing at 450 °C, only the hex phase peak is present in all compositions, including GST124, where the cubic phase has been completely replaced. GST144 exhibits an improved crystallinity (sharper peak), while GST194 remains unchanged upon annealing. Using the Scherrer equation, we determined the grain size for the three studied samples (Fig. 5.3b). The crystallites' size increases with the Sb/Te ratio, with GST144 exhibiting intermediate behavior between GST124 and GST194. TEM-EDX analysis of GST144 annealed at 450 °C (Fig. 5.3c) shows a homogeneous phase with no elemental segregation, confirming the congruency of the obtained phase. The phases are composed mainly of Sb_2Te_3 blocks with periodic Sb_2 planes

depending on the antimony content, compatibly with the limited amount of GeTe bonds due to the decreasing Ge at. % for increasing Sb [128].

Crystallites in GST144 grow in size but remain related to the same stable hexagonal phase; in GST194, the crystallite size increase is minimal upon annealing. This result validates the fast growth-dominated crystallization kinetics of Sb-rich compositions, tuned with the Sb/Te ratio [124]. The properties of GST144 show promise for device applications, as they maintain a high resistivity contrast between the amorphous and crystalline phases while facilitating rapid growth-dominated crystallization toward a stable hexagonal phase.

5.1.2 Electrical Performance

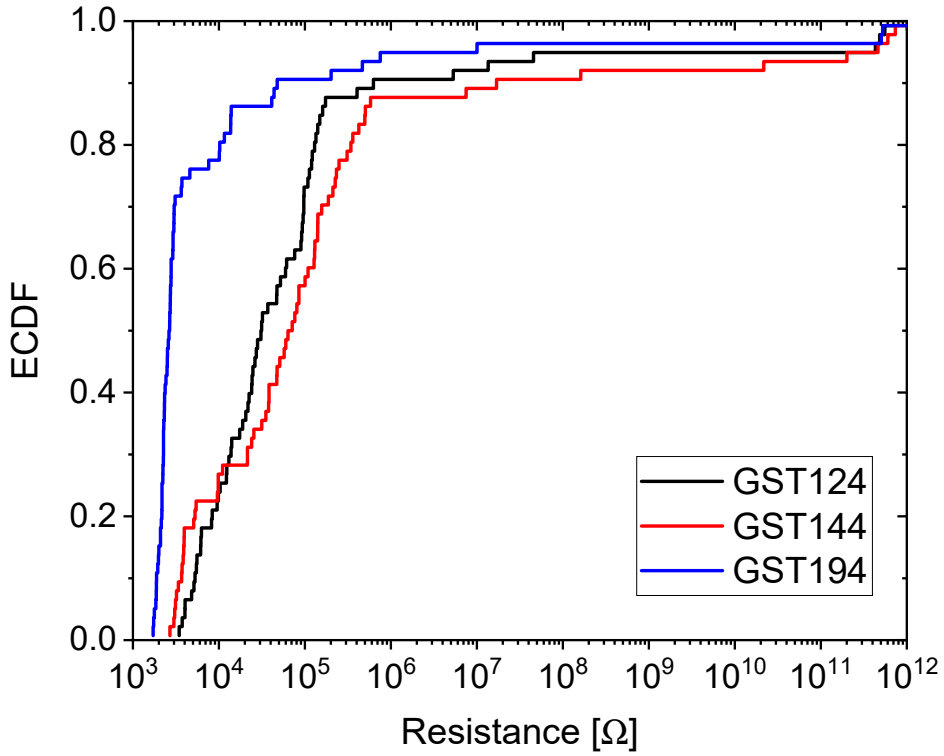


Figure 5.4: Empirical cumulative distribution (ECDF) of the pristine resistance of 40 nm CD "Wall" devices. GST144 and GST194 were integrated in both bulk and multilayer configurations. The distributions represent about 70 devices covering most of the 200 mm wafer surface.

The three alloys with increasing antimony content were integrated in a "Wall" heater structure in the BEOL of the LETI Memory Advanced Demonstrator (MAD) based on 130 nm CMOS (Section 2.3). GST144 and GST194 were deposited by PVD co-sputtering as homogeneous bulk from GST124 and Sb targets. GST124 is obtained by monotarget sputtering. The as-deposited (i.e., pristine) resistance of 40 nm devices across 200 mm

wafers is reported in **Fig. 5.4**. Due to the low-temperature PVD deposition, the resulting layers are amorphous, but undergo crystallization during the final steps of the BEOL fabrication (metal lines, dielectrics, etc.). GST124 and GST144 have similar resistance distributions, with a slight dispersion attributable to a partial crystallization. The enhanced growth speed of GST194 produces a less dispersed distribution with a median resistance of about 2 kΩ. The crystallized pristine resistance provides insight into the achievable SET resistance for the devices. In contrast, GST124 and GST144 may fully crystallize the cell during SET programming, reducing the median resistance.

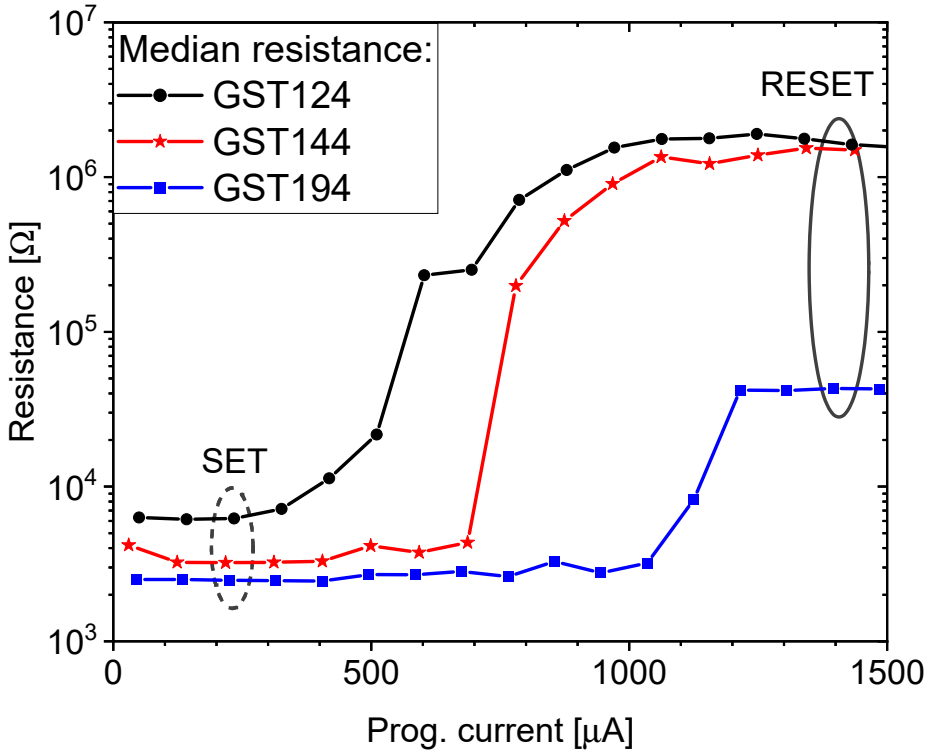


Figure 5.5: Programming curve showing the resistance as a function of the programming current I_{prog}. The transition from SET to RESET states for the three compositions is highlighted. The points are the median extracted from about 100 devices with a nominal CD of 40 nm.

Fig. 5.5 shows the programming characteristics for the three compositions. The programming current (I_{prog}) required to amorphize the material increases with the Sb content, following the increase in the melting temperature. I_{prog} is similar between GST124 and GST144, but it exceeds 1 mA for GST194, likely due to both the fast crystal growth speed, which can overcome the melt-quench amorphization rate at lower currents [122]. The RESET can be effective only if quenching is faster than crystallization; also, due to the lower SET resistance, a higher current is needed to produce sufficient heat. Higher currents produce a higher temperature in the heater. The rapid current variation induced by

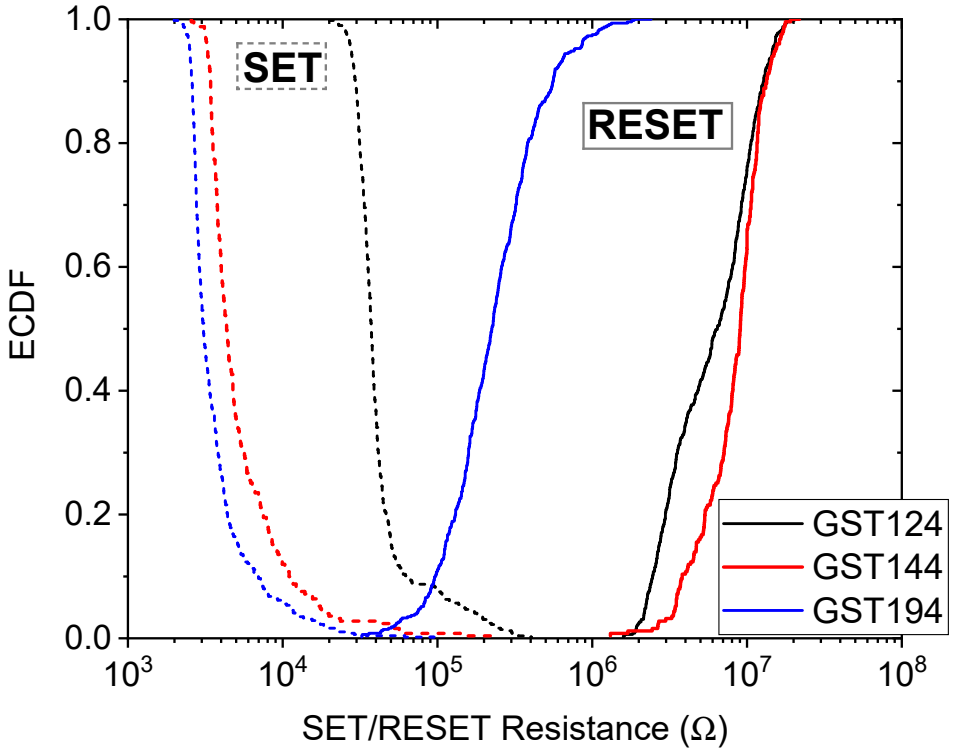


Figure 5.6: ECDF of the SET (dashed line) and RESET (solid line) state resistances. The increase in Sb content results in a more metallic conduction with lower resistance and variability in the SET state. In GST194, this comes at the cost of a reduction in the RW due to the more conductive RESET. The sample size exceeds 256 devices, each with a nominal CD of 40 nm.

programming pulses with a short fall time produces a fast temperature variation (dT/dt). Antimony promotes a more metallic conduction, resulting in a significantly lower RESET resistance in GST194, which is nearly two orders of magnitude lower relative to GST124. **Fig. 5.6** reports the SET and RESET distributions for the three compositions. Both GST124 and GST144 exhibit a large RW, with a RESET/SET resistance ratio of over 170 and 2000, respectively[2]. In GST194, the lower RESET resistance limits the overall window. For high Sb/Te ratios, the SET resistance decreases and becomes less dispersed, and in particular, GST144 presents reduced SET tails with an additional enlargement of the RW.

The PCM threshold voltage (V_{th}) is a critical parameter as it is responsible for the voltage Read Window Margin (RWM) in 1S1R OTS+PCM devices (Chapter 3, 4). GST124 and GST144 have similar V_{th} (of about 1 V) with a significant reduction of the dispersion for the larger Sb/Te composition (**Fig. 5.7**). GST194 presents a similar distribution to GST144 but with a lower mean V_{th} with a value of about 0.6 V.

SET resistance cartographies were performed to investigate the SET programming

[2]The resistance ratio R_{RESET}/R_{SET} is calculated at the median 50% of the distribution.

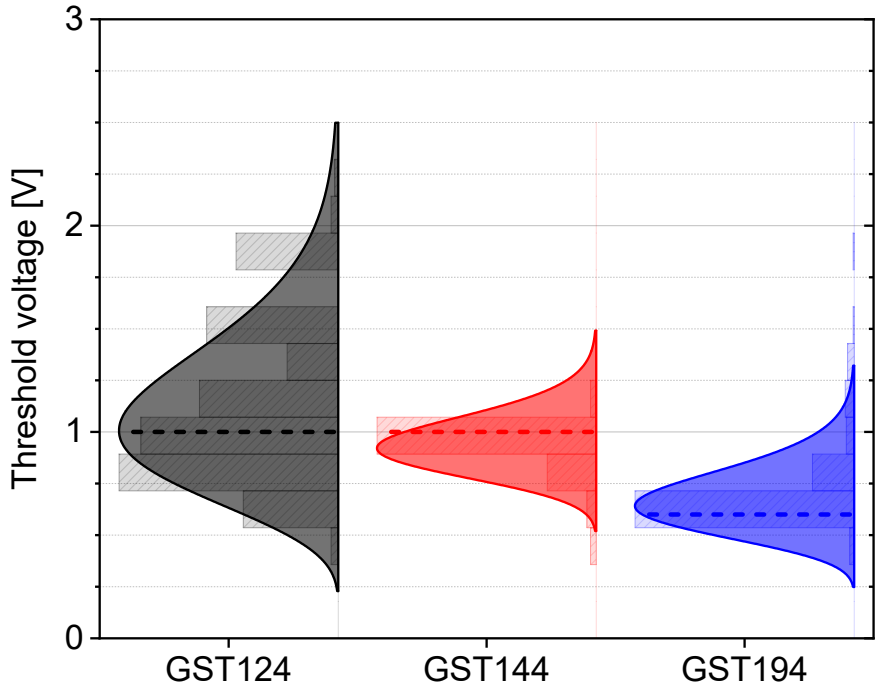


Figure 5.7: PCM threshold voltage distribution of the RESET state comparison for the three alloys. The data is fitted with a Gamma distribution model (Chapter 3), and the dashed line represents the median. The V_{th} is extracted for over 256 devices with a 100 nm lateral dimension.

speed: varying I_{prog}, the programming pulse width (t_{width}), and the pulse fall time (t_{fall}), starting from the RESET state (**Fig. 5.8**). For Sb/Te $\geq$ 1, the SET operation is more reliable and faster ($t_{fall} < 5$ ns) already at low programming currents. Conversely, GST124 requires a higher programming current and a longer fall time to ensure the same programming reliability. The almost time-independent response at different t_{width} in Fig. 5.8a demonstrates the device's capability to crystallize below our minimum pulse duration of 80 ns if a suitable current condition is met. The current-over-time decreasing rate (proportional to the material growth speed [129]) of GST144 to ensure an optimal SET operation, is extracted by linear fitting of the SET-to-RESET iso-resistance curve shown as a dotted line in Fig. 5.8b. It is approximately 1.7 μA/ns, higher than values previously reported for standard $Ge_2Sb_2Te_5$ (1.3 μA/ns) and Ge-rich GeSbTe (0.3 μA/ns) [110, 129] integrated in an equivalent test vehicle for comparable device dimensions. This result aligns with the higher growth speed of GST144 observed through material analyses. The same extraction could not be reliably performed for GST124 due to the slower crystallization speed, which limits the SET capability at low currents. The lateral confinement of the cell also limits the temperature gradient, therefore not promoting the propagation of the crystallites from the borders. In GST194, the crystallization speed is significantly

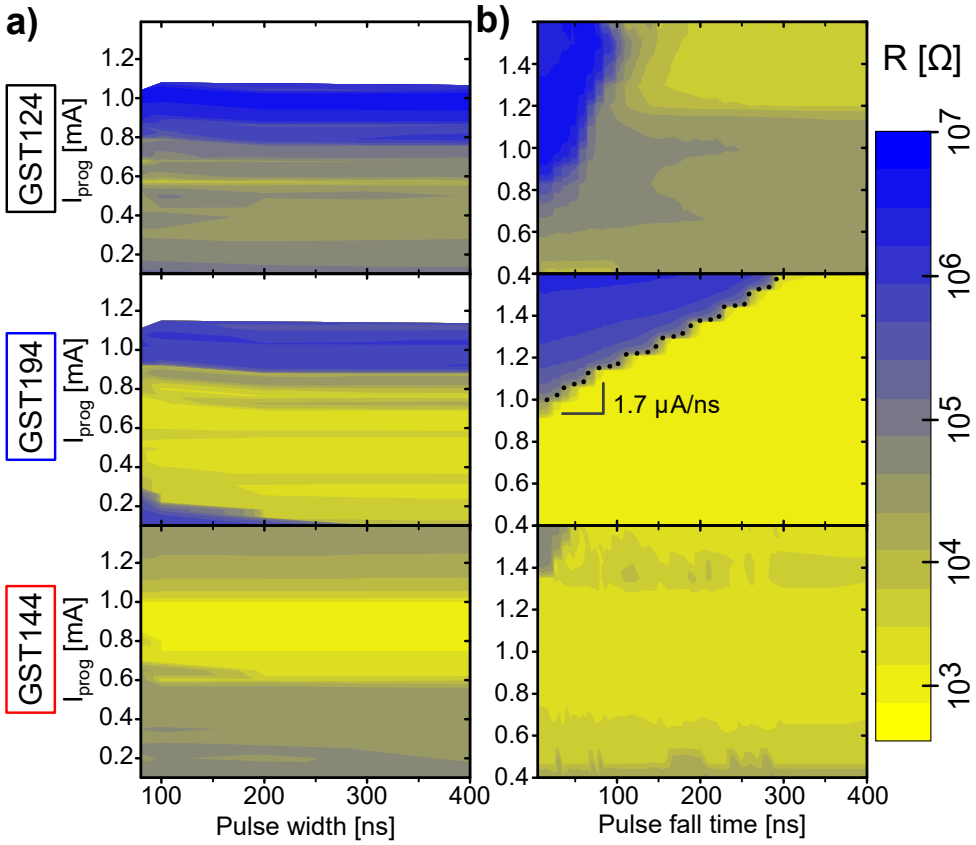


Figure 5.8: Resistance cartographies for increasing I_{prog} (y-axis) and a) t_{fall}, and b) t_{width} (x-axis). The devices are first programmed in the RESET state before the application of the pulse. Each point represents the mean resistance value of a population of approximately 100 to 256 devices. The dotted line in GST144 represents the SET-to-RESET iso-resistive curve used for the current over time (dI/dt) decreasing rate extraction for optimal SET operation.

faster, making RESET operation possible only at high currents, as previously observed in the programming characteristics (Fig. 5.5).

5.1.3 Reliability Analysis

Endurance tests were performed by applying repeated SET and RESET writing pulses (t_{width} = 300 ns), following the evolution of the programmed resistance states. The maximum I_{prog} is equivalent for GST124 and GST144 devices to trigger the material evolution under the same programming conditions (i.e., programming energies). The GST194, however, required a higher current to achieve a reliable RESET. GST124 is stable upon cycling, with both SET and RESET resistances evolving after 10^4 cycles (**Fig. 5.9a**). The devices remain functional and programmable even after 10^5 iterations. GST194 exhibits a higher starting resistance variability that decreases with cycling, likely due to elemental reorganization occurring in the active region. The RW is preserved after 10^5 cycles

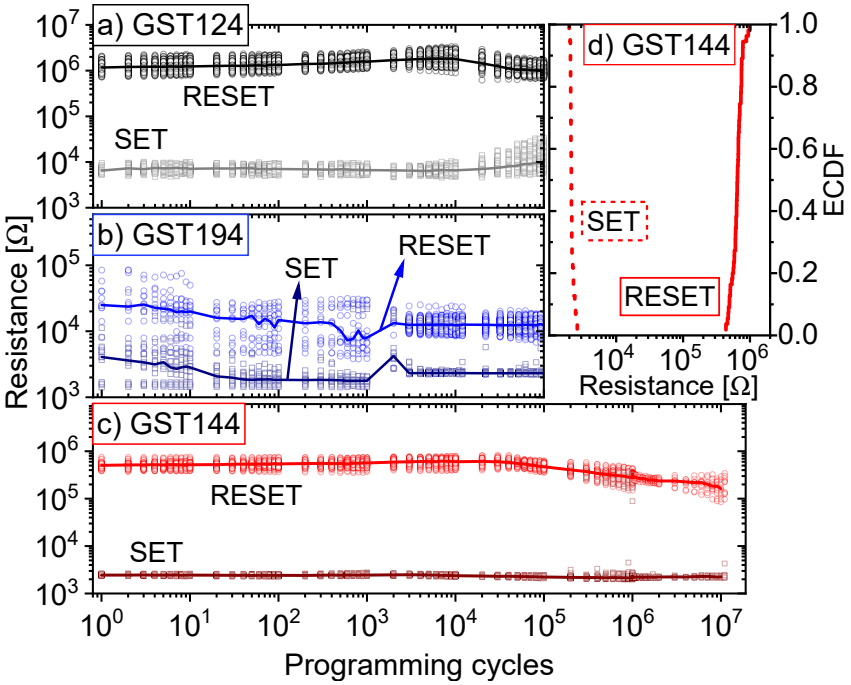


Figure 5.9: SET/RESET Endurance for a) GST124, b) GST194, and c) GST144 performed on at least 10 devices for each composition. d) SET and RESET distributions (55 devices) for GST144 after 10^6 programming cycles. All the devices have 100 nm CD.

(Fig. 5.9b), with the onset of RESET degradation for further programming operations. GST144 exhibits the lowest SET and RESET variability, demonstrating excellent stability upon cycling. The RESET resistance decreases to approximately 100 kΩ after 10^5 cycles. Nevertheless, the devices maintain a reliable RW up to 10^7 cycles, where heater metal degradation is likely the cause of open failures (Fig. 5.9c). The good performance of the GST144 devices after 10^6 writing cycles is confirmed by the distributions in Fig. 5.9d, which remain largely unaffected compared to the not cycled ones (Fig. 5.6).

Material evolution is triggered by the total energy provided to the system during programming, along with the temperature gradient produced by the heater integration (**Fig. 5.10**). For GST144, in the case of fast programming pulses of 5 ns allowed by its high SET speed (Fig. 5.8), the material evolution in the active region is not expected before more than 10^8 cycles. By EDX analyses (not reported), we could appreciate an enrichment of approximately +25% in Sb content and a reduction of -15% in Te content in the active region of the device after cycling (Fig. 5.9c) with almost no Ge evolution, without compromising the cyclability of the device. As mentioned in the chapter's introduction, the congruent phases should not lead to segregation; in the case of a "Wall" heater device, the Phase-Change material is subject to an intense and repeated temperature gradient. The elements, therefore, experience a thermophoretic moving force along this gradient [106, 130]. Antimony, with its significant negative Soret coefficient,

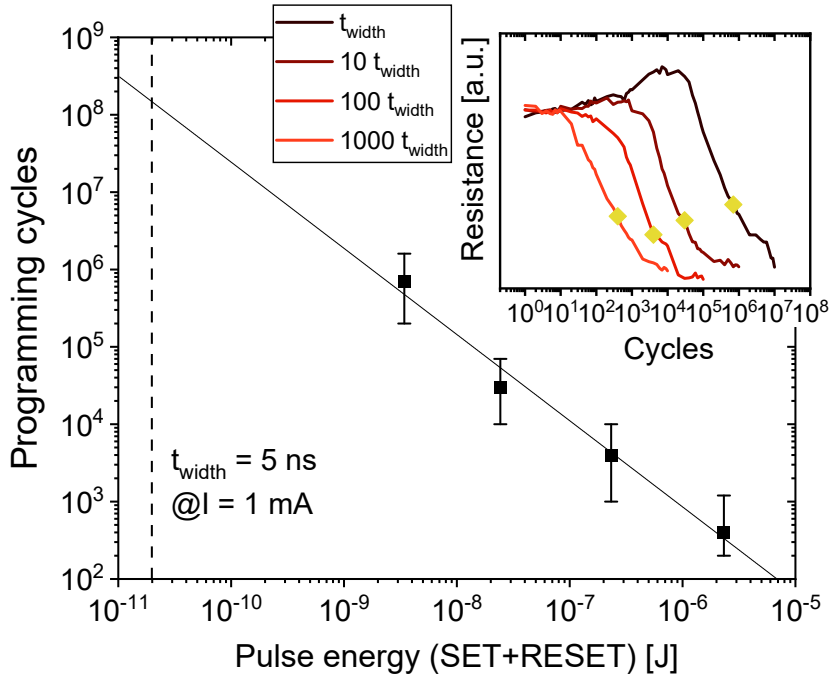


Figure 5.10: Number of max SET/RESET cycles for a given programming energy (SET + RESET energy) before the start of the resistance states evolution in GST144. The dashed vertical line represents the energy of a short 5 ns pulse (e.g., RESET). The inset reports the endurance result performed with increasing pulse width time (t_{width} = 300 ns). The yellow diamonds represent the points of halved resistance, used for estimating material stability.

is driven and accumulates towards the hot spot [54, 131]. Since materials still show good phase transition, a different composition in the active region is probably achieved, balancing out thermophoretic, thermoelectric, and concentration forces, preserving the device's functionality for practical purposes. From these results, it is clear that the antimony concentration plays a crucial role in delaying material evolution, which probably involves only the active region for sufficiently high Sb/Te, where the SET state remains unchanged. Detailed material and device characterization are still required to support these hypotheses and provide quantitative results.

A summary of the electrical results for the three alloys is reported in **Fig. 5.11**, benchmarking the three compositions, where the performance of the GST144 stands out as the best tradeoff, maximizing all metrics.

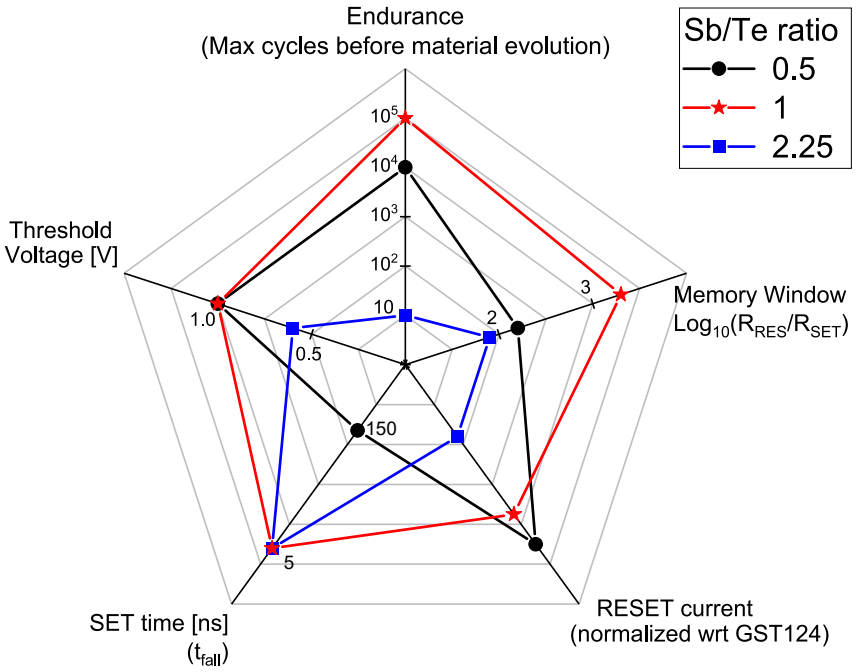


Figure 5.11: Performance metrics comparison among the three compositions. GST144 is the optimal tradeoff, featuring the high programming speed of GST194 and the large Resistance Window (RW) of GST124, as obtained by averaging the results from 256 devices.

5.2 Ge-Rich GeSbTe-based Alloys

Ge-rich GeSbTe alloys are interesting for their improved thermal stability and data retention while keeping low programming currents; they are often proposed as candidates for embedded and automotive applications [31, 32, 132]. Ge content increases inhibit crystallization and stabilize the amorphous phase at higher temperatures compared to GST225 [133]. The higher crystallization temperature is particularly interesting for automotive and aerospace applications, where devices must be capable of withstanding soldering reflow and extreme environments [134]. However, Ge-rich GST presents higher pristine resistance and larger variability, which requires a controlled forming operation to achieve sufficient uniformity [90]. The tendency of germanium to form clusters poses a critical reliability concern, addressed by doping and process optimization [85, 135].

We integrated Ge-rich GST with more than 50% Ge at.% with DPSA architecture. **Fig. 5.12** shows the SET/RESET resistance distributions comparing Ge-rich GST and standard GST225, with the same cell architecture. Ge-rich GST shows a more reliable SET state with lower median resistance and dispersion; on the contrary, the RESET state has lower resistance, due to the abundance of Ge-Ge homopolar bonds [85]. To enhance the resistance window, the programming pulses must be optimized. Following the procedure presented in Chapter 3, we report the R–I in **Fig. 5.13a** and the SET

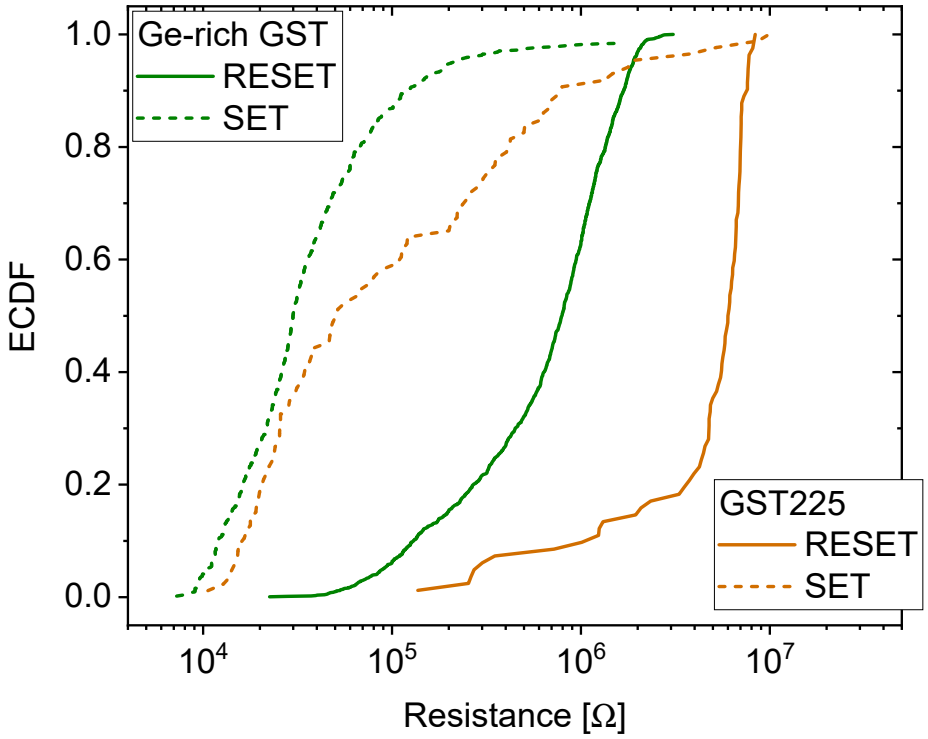


Figure 5.12: SET/RESET resistance distribution of Ge-rich GST compared to the standard GST225. The SET state is compatible between the two, while the RESET is less resistive for the Ge-rich. Eighty devices are considered for GST225 and more than 400 for the Ge-rich GST, all with a CD of 100 nm.

speed in Fig. 5.13b. The Ge-rich PCM can achieve a resistance window compatible with GST225 for lower currents. While we do not have a direct comparison with GST225, the SET speed of the Ge-rich alloy appears slower with respect to literature [135], with long fall times required to achieve complete crystallization. The modified thermal properties of the DPSA cell play a crucial role in increasing the temperature, leading to full volume amorphization with the consequent need for more extended pulse widths (t_{width}) to induce the nucleation of new crystallites (Chapter 3). The impact of the DPSA architecture can justify the much longer t_{fall} required to SET our Ge-rich PCM compared to similar works [110, 135]. This could also be due to the complexity of the DPSA integration, especially challenging during the etching steps (Section 2.4); our variability could be impacted by possible oxidation or by the chemistry used for the fabrication.

Writing endurance tests were conducted (**Fig. 5.14**) to verify the stability and repeatability of the SET and RESET operations. The Ge-rich material can be reliably programmed up to more than 10^3 cycles before degradation begins. The endurance provides a promising preliminary result, considering that the programming pulses were not designed to minimize the energy supplied to the cells. The typical failure mechanism in Ge-rich GST PCM is related to the segregation of Ge clusters, lacking phase-change prop-

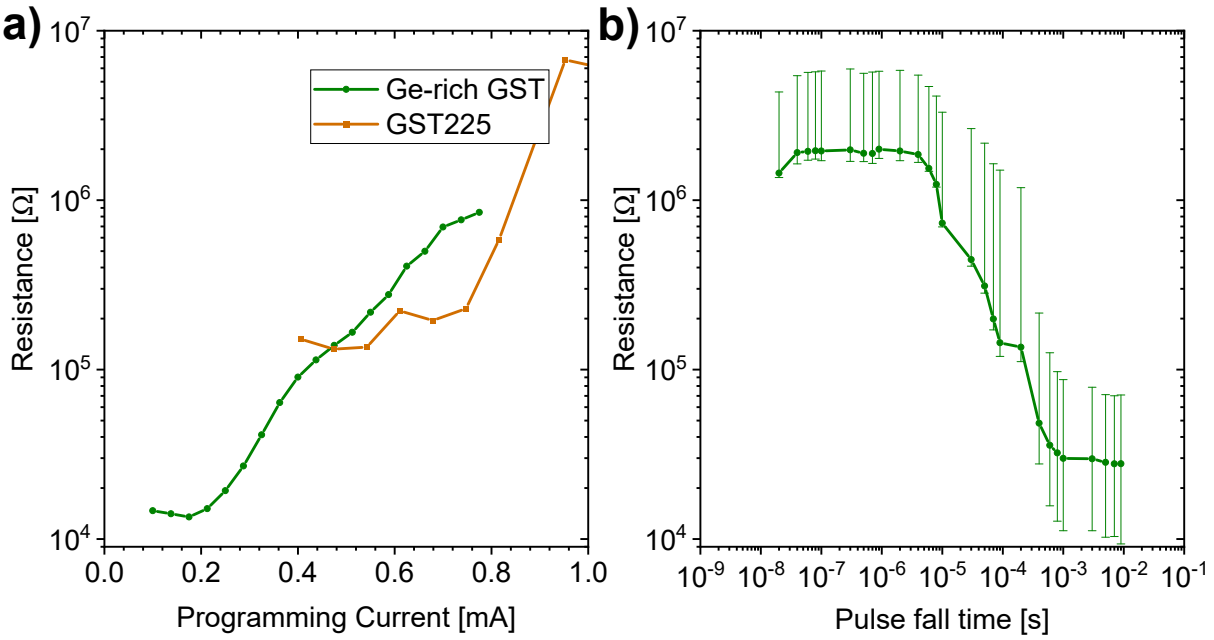


Figure 5.13: Median R-I programming curve of Ge-rich GST (compared to our GST225 reference) on the left, from more than 500 devices. Resistance vs SET pulse fall time of Ge-rich GST on the right, Median and IQR of 512 devices. All the devices have a CD of 100 nm.

erties [106]. The excess germanium is expelled from $Ge_2Sb_2Te_5$ crystals and accumulates, reducing the total active volume of the cell; Ge segregation may eventually form conductive paths between the heater and the Top Electrode, causing a stuck-SET hard failure [136]. Previous studies emphasize the importance of the forming operation to adjust the electrical behavior of the Ge-rich alloy, by limiting the event of Ge cluster formation on top of the heater contact [90]. In this work, we did not focus on this step during programming, meaning that performance could be further optimized. The threshold voltage of the Ge-rich composition is compatible with the one of $Ge_2Sb_2Te_5$.

Ge-rich GST is a promising candidate for automotive PCM applications; however, several critical issues related to fabrication, variability, and reliability remain. The benefits arising from the stabilization of the amorphous phase may not compensate for the inherent segregation phenomena that will inevitably limit the device's lifespan and cause many early failures. A possible approach would be first to optimize the Sb/Te ratio to benefit from a stable and congruent phase (as outlined in Section 5.1), to then trying to stabilize the amorphous phase to improve the data retention by the addition of dopants elements; which could be Ge or In, Ga, and N [137–140].

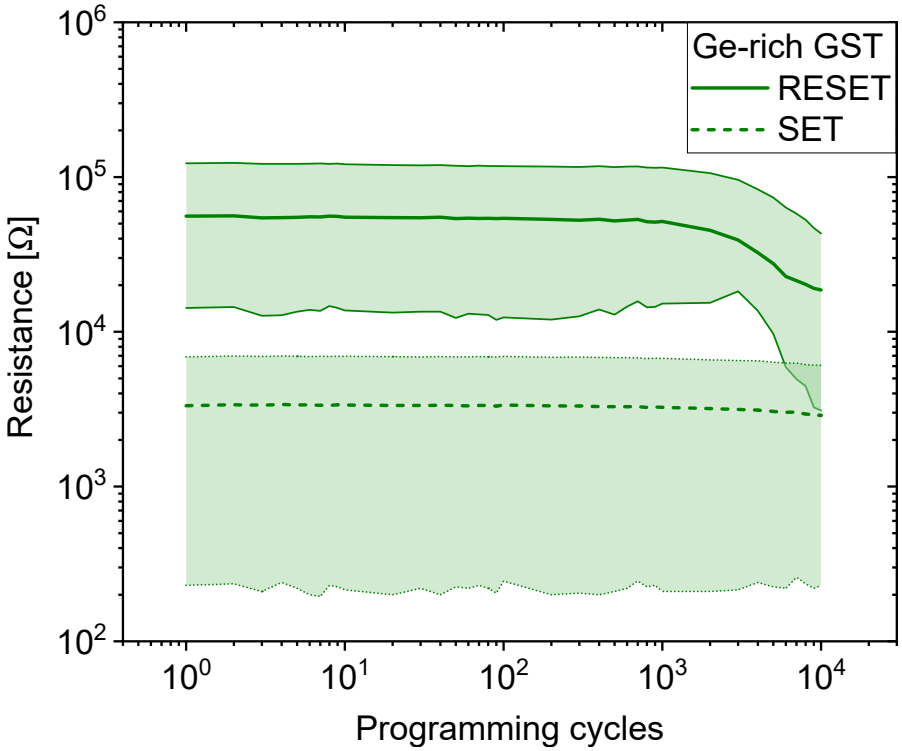


Figure 5.14: SET/RESET cycling endurance of Ge-rich GST showing material stability up to 10^3 cycles. Median values and Interquartile Range (IQR) of 500 devices with 300 nm CD.

5.3 OTS Materials Engineering

Our OTS material of reference is a Nitrogen-doped GeSbSeN alloy (GSSN), whose electrical properties have been validated by previous studies [69, 71]. The GSSN alloy demonstrates good electrical performance and thermal stability up to 400 °C, with low OFF current and leakage. The primary goal of OTS engineering is to improve the reliability for extended operation. In the following, we address the issue of device-to-device variability by a multilayer deposition approach. To improve the OTS/Metal interface, a Carbon Underlayer was introduced [77]. The underlayer reduces the variability of the threshold voltage and inhibits elemental diffusion of Ti from the TiN top electrode. In this section, we present preliminary results comparing the threshold voltage properties of GSSN OTS, which serves as a reference for OTS+PCM co-integration (as discussed in later sections 5.4, Chapter 3, and 4). We integrated the GSSN OTS both as bulk material and as a Multilayer, outlining the effects of carbon underlayers on the firing and threshold voltages. A second reliability challenge is related to the high voltages usually required to electroform an OTS device (e.g., 5 V), which contributes to the electrical stress at the beginning of the device life. To reduce the forming and threshold voltages, we investigate alternative compositions based on As–Se compounds. We demonstrate the potential of these alloys

to reduce switching and forming voltages, as well as control the variability of the V_{th}.

5.3.1 Multilayer GeSe-based OTS alloys

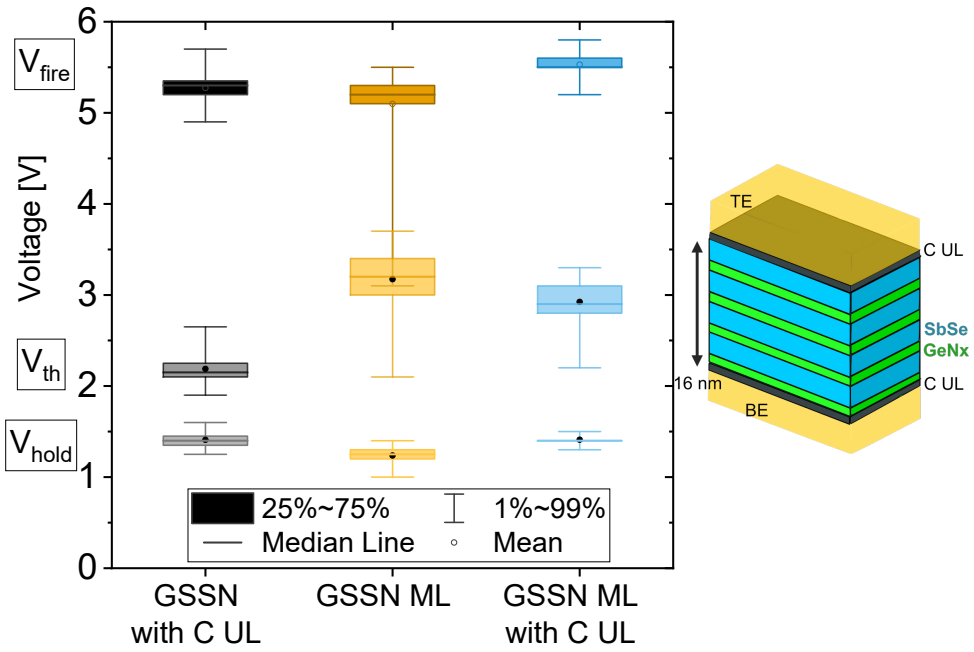


Figure 5.15: Forming (Firing), Threshold and Holding voltages of different GSSN OTS integrations. Bulk GSSN with a carbon Underlayer (UL) has a lower threshold voltage than the Multilayer (ML). Adding the carbon UL to the multilayer structure reduces the variability. The boxplot accounts for over 100 devices with 100 nm CD per alloy type. The inset shows the ML integration with GeNx/SbSe layers.

When depositing bulk GSSN alloy, the presence of the carbon Underlayer is essential for device reliability, whose performance is strongly degraded by Ti interdiffusion from the top and bottom electrodes [77]. The as-deposited OTS requires a single high-voltage forming (also called firing) operation where the conductive path is generated, defining the active region [141]. The forming (V_{fire}), threshold (V_{th}), and holding (V_{hold}) voltages are reported in **Fig. 5.15**. A Multilayer (ML) integration was performed by stacking GeNx/SbSe layers with nm-range thickness for both the GeNx and the SbSe layers. The overall composition is nominally compatible with the bulk GSSN (**Table 5.1**):

Ge	Sb	Se	N
22%	17%	48%	13%

Table 5.1: Global composition of the GSSN ML structure (in at. %).

The Multilayer integration has a similar forming voltage to the bulk one but with

much greater variability, leading to a dispersed V_{th} distribution. A possible increase of dispersion could be caused by variation during fabrication. The introduction of the carbon UL mitigates the variability at the forming step, with a less variable threshold voltage about 1 V higher than the bulk material. One of the advantages of the ML integration is the ease of deposition of layers of controlled thickness by bi-target sputtering, leading to a uniform deposit with precisely controlled global composition. This fabrication method could be beneficial for the Atomic Layer Deposition of chalcogenide materials [142]. A reduced device-to-device variability will greatly reduce the firing operation variability, which is determined by the pristine device conduction, producing more predictable forming conditions.

These preliminary results show the performance compatibility between the Multilayer and bulk integration, with similar V_{fire} and V_{th}. The results highlight the importance of the carbon Underlayer to reduce the forming and threshold voltage variability. Further tests are still required to assess other benefits of this structure, such as endurance and thermal confinement along the stack direction.

5.3.2 AsSe-based OTS Alloys

Operational OTS threshold voltages reported in this work are in the range between 2 and 4 V, adapted for standalone applications but critical when targeting embedded systems. Considering the final application where a PCM is in series, the overall threshold voltage should be below 5 V, or 3.3 V to limit the power consumption and avoid high voltage drivers [31, 129]. For this reason, new OTS materials are explored to identify candidates with reduced threshold voltages and sufficiently low leakage currents. As the electroforming initialization step requires higher voltages ($V_{fire} \geq V_{th}$), it is critical to find a composition with reduced firing voltage as well [141]. The forming operation is responsible for the conductive filament formation in the selector (Section 2.6) and will determine the subsequent V_{th} and impact the device lifespan [62]. The possibility of having a reduced forming or forming-free selector is often sought in literature [143]. Arsenic-based selenides and tellurides are good OTS candidates due to their high endurance and low leakage current [68, 76]. This investigation examines the electrical performance of As-based selenides OTS to reduce the selector threshold voltage and minimize V_{fire}.

Fig. 5.16 reports the firing and threshold voltages of Si-doped As_2Se_3 and SiAsGeSe (SAGS) alloy for decreasing layer thickness. The 15 nm of As_2Se_3 presents a dispersed V_{fire} which stabilizes to a V_{th} of about 3.25 V. The introduction of 6% Silicon in the As_2Se_3 composition aims to inhibit possible crystallization. The SAGS alloy introduces 10% Ge and 17% Si to As_2Se_3 to hinder crystallization, reduce device variability, and lower the threshold voltage. The results show a V_{th} similar to As_2Se_3+Si without any significant

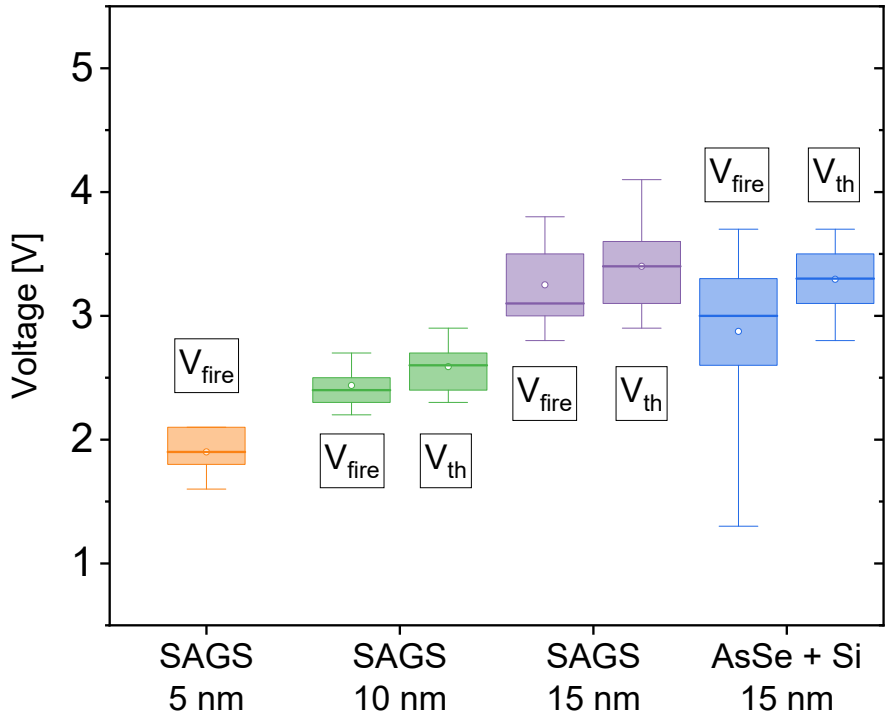


Figure 5.16: As-based SAGS OTS firing and threshold voltages for increasing layer thickness. On the right, a Si-doped As_2Se_3 OTS shows similar metrics to the 15 nm SAGS. The switching voltage does not vary much after firing, showing the potential of such forming-free OTS alloys. The sample size varies with the integrations and ranges from 100 to 500 devices. For the 5 nm SAGS, only 11 devices were functional, but they are sufficient to confirm the threshold voltage scaling trend. All the devices have 100 nm CD.

reduction; we still remark the absence of a firing step as V_{fire}approaches V_{th}. The trend of V_{th} reduction with layer thickness is confirmed by comparing three different sizes, where the forming-free capability of the selector is confirmed. As layer thickness decreases, we face more challenging integration, where a slight variation in the deposition may lead to shorts between the top and bottom electrodes. Moreover, during PVD sputtering, the film presents approximately a constant rugosity, which becomes more impactful on the electrical parameters as the film thickness decreases. For this reason, we identified only a few working devices for the SAGS 5 nm, confirming the scaling trend.

We studied As-based OTS alloys to identify possible forming-free candidates for embedded applications. We found that the forming step is suppressed and the V_{th} variability reduced in As_2Se_3 OTS with the addition of Si and Ge. Still, we face high threshold voltages, especially for larger layer thicknesses above 10 nm. Layer thinning could be a viable approach to reduce the threshold voltage (Fig. 5.16), while the proposed composition still requires tuning to reduce the threshold voltages further. An assessment of the leakage

current and the endurance of these alloys is still lacking and would provide essential information for solving the problem. The environmental issues related to arsenic compounds in the microelectronic industry have been well known for a long time [144]. For this reason, our effort should be oriented toward possible alternative solutions: Our reference OTS material, GSSN, is an arsenic-free solution that showed performance compatible with the ones outlined above (Chapter 2, 5.3), as well as other research groups who report excellent and promising performances not involving arsenic [145].

5.4 Material Perspective on OTS+PCM Co-Integration

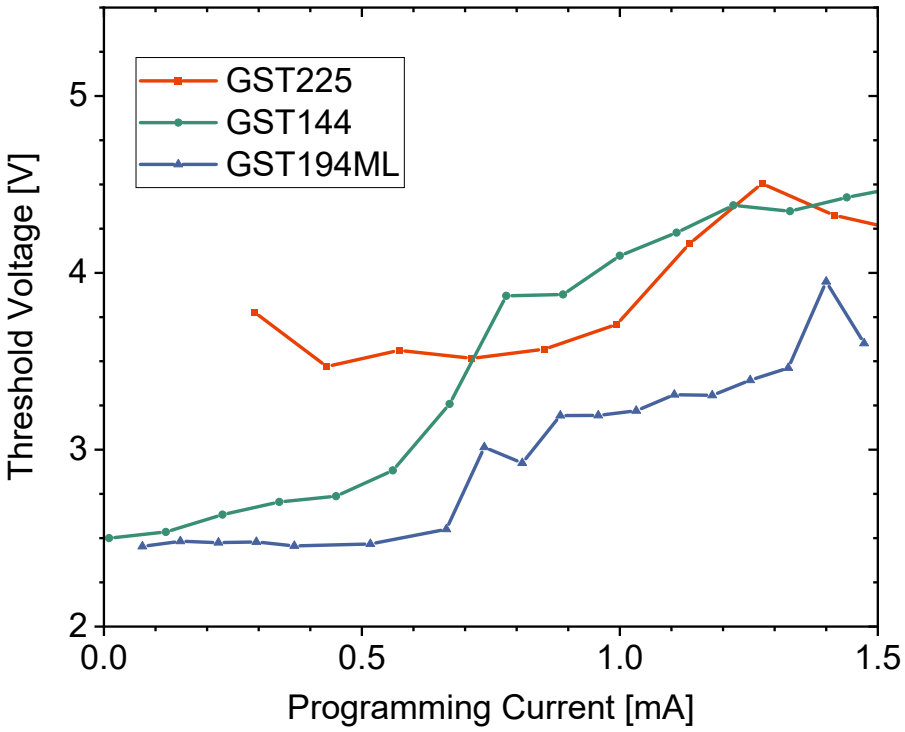


Figure 5.17: SET and RESET threshold voltage comparison between GST225, GST144, and GST194 ML co-integrated with a GSSN ML OTS selector in DPSA architecture. Boxplot of about 50 devices with 100 nm CD for each population.

Following the material optimization previously described in Section 5.1, we co-integrated GST225, GST144, and GST194 PCM alloys with GSSN Multilayer OTS in a DPSA architecture. GST225, widely investigated in previous Chapter 3, 4 is our reference. Due to the limited fabrication availability and test constraints, we only carried out a partial characterization on GST144 + OTS.We still consider that these results provide a comparative insight into the programming performance of tuned Sb/Te PCM when co-integrated in

the laterally confined DPSA structure. **Fig. 5.17** reports a V_{th}–I_{prog} curve for the three compositions. The programming current increases with the Sb/Te ratio for the GST144 and GST194-based PCM layer, confirming the trend observed for in Fig. 5.5. The results for GST225 are not compatible with what was previously observed, as the lowest threshold achieved exceeds 3.5 V. This incognuence can be explained by the short programming pulse applied, which, while providing a suitable current, does not favor a complete SET of the PCM. This can be confirmed by comparing the programming curve presented in Fig. 5.17 with the previous programming analysis carried out in Chapter 3. The thermal confinement of the PCM cell due to the presence of the OTS layer could further uniformize the temperature gradient, hindering the crystallization. This phenomenon, discussed in Section 3.5, is less impactful for faster crystallizing GST144 and GST194, which will crystallize for short pulses as long as the SET current is appropriately selected below 500 µA.

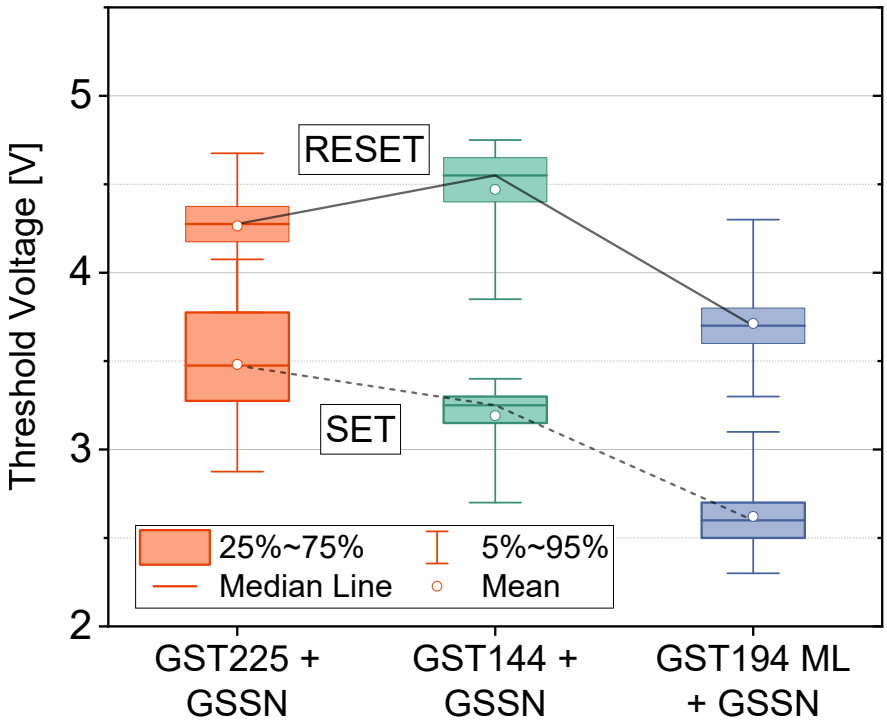


Figure 5.18: Median V_{th} vs I_{prog} for DPSA OTS+PCM comparing GST225, GST144, and GST194. Data from approximately 50 devices with 100 nm CD.

The advantage in terms of programming current is accompanied by an improvement of the voltage Read Window Margin (RWM) for GST144, showing more than 1 V of window (**Fig. 5.18**). GST194 ML still provides a significant window but at a reduced V_{th} due to its lower SET and RESET resistances associated with the large Sb/Te ratio. The SET state monotonically decreasing V_{th} with increasing Sb/Te is confirmed for the three PCM

compositions, while GST144 shows the highest RESET V_{th}.

In this chapter, we analyzed the impact of the Sb/Te ratio on the physical and electrical properties of GeSbTe-based PCM. We identified the GST144 composition as the best tradeoff in terms of Read Window Margin, SET and RESET resistances, and programming current. In this section, we extended the results to the OTS+PCM case by co-integrating a 16 nm Multilayer GSSN OTS following a DPSA architecture. While the change in the architecture and the presence of the OTS alter the thermal properties of the cell, we are still able to recognize the threshold voltage reduction trend of the SET state associated with a resistance decrease related to increasing antimony content. We confirm the advantages of GST144 over other compositions. We propose material optimization (e.g., by doping) to further enhance device performance and address the critical limitation of Sb-rich alloys, namely, data retention. Further characterization is required to isolate the role of the architecture in the device's electrical performance, in terms of current and pulse timing. A complete analysis of the subject will involve conducting repeated programming endurance tests and detailed programming cartographies to fully explore the device's performance.

5.5 Conclusions

This chapter explored material engineering approaches for the optimization of both PCM and OTS devices. The comprehensive investigation encompasses material stability analysis through physical and electrical characterization, reliability assessment, and structure comparison. The focus encompasses the antimony-tellurium ratio (Sb/Te) optimization (Section 5.1), exploration of Ge-rich PCM (Section 5.2), Multilayer OTS (Section 5.3.1), and As-based OTS (Section 5.3.2), concluding on the co-integration of the best-performing PCM and OTS compositions (Section 5.4).

The tuning of the antimony-tellurium ratio (Sb/Te) in GeSbTe-based PCM alloys showed $Ge_1Sb_4Te_4$ composition (Sb/Te = 1) as the optimal candidate reconciling the requirements for high speed operation and large memory window (Fig. 5.11) [R1]. With this composition, and by tuning the Sb/Te ratio, we achieved the suppression of the metastable cubic phase characteristic of conventional $Ge_2Sb_2Te_5$ and $Ge_1Sb_2Te_4$ (low Sb/Te); this enables a direct amorphous-to-hexagonal crystallization (Fig. 5.2). The faster crystallization kinetics allow for improved SET speed and lower programming power. Intermediate Sb/Te grants a wide SET/RESET resistance ratio and SET state stability. This composition showed exceptional reliability exceeding 10^7 programming cycles (Fig. 5.9), with a material stability expected to withstand over 10^8 cycles without material evolution (Fig. 5.10). Material analysis revealed increasing activation energy for higher Sb/Te ratios; crystallite size evolution confirms growth-dominated crystallization kinetics and a stable SET state

(Fig. 5.3), supported by electrical reliability assessments.

The preliminary investigations of Ge-rich GeSbTe compositions revealed a tradeoff between thermal stability and reliability metrics. While beneficial for embedded applications, the high germanium content poses a threat to writing endurance (Fig. 5.13). We present a preliminary characterization of Ge-rich PCM alloys and propose combining the strategies of Sb/Te tuning and doping to achieve both fast speed without compromising data retention. Further tests are still required to confirm our suggestions.

In the studies presented in this manuscript, we mostly adopted the well-established GSSN OTS alloy (a nitrogen-doped GeSbSe composition) as a robust selector material. In this chapter, we present preliminary results on multilayer integration achieved through PVD co-sputtering, highlighting the role of thin carbon underlayers in enhancing the contact interface and preventing intermixing with bottom and top electrodes (Fig. 5.15). Multilayer integration provided compatible performance with bulk materials with reduced device-to-device variability; further results are required to confirm the reliability of the multilayer stack for extended programming. If confirmed, it could represent a viable solution for vertical integration exploiting ALD techniques [146].

We explored arsenic-based OTS compositions (namely As_2Se_3 and SAGS), which showed promising forming-free operation capability, addressing this critical requirement for low-power embedded applications (Fig. 5.16). While the threshold voltage reduction remains challenging, the scaling trend with layer thickness is promising for sub 3.3 V applications. The use of arsenic for chalcogenide device fabrication is subject to debate and must be carefully analyzed.

Finally, we validated the co-integration of optimized GST144 PCM with multilayer GSSN OTS, confirming that material optimization successfully translates to device performance (Fig. 5.17). GST144 PCM maintained its superior characteristic when integrated in the OTS+PCM DPSA structure compared to standard $Ge_2Sb_2Te_5$ and the Sb-rich $Ge_1Sb_9Te_4$ (Fig. 5.18). The Sb/Te ratio optimization improves the SET and RESET characteristics, minimizing the impact of the thermal confinement induced by scaling of the DPSA cell and OTS co-integration; a crucial finding for array-level implementations where thermal cross-talk and programming uniformity are primary concerns.

Further research directions should focus on optimization of the material compositions, with eventual doping. Thermal and electrical coupling of OTS+PCM co-integration is still lacking in the literature, and further experiments are required to highlight the role of the stack and architecture at highly scaled nodes under realistic operating conditions.

Chapter 6

Towards the Crossbar Array

This chapter presents a comprehensive investigation of the transition from individual device characterization to practical Crossbar array implementation in OTS+PCM systems. The work bridges the fundamental gap between device-level studies performed in a 1T1S1R matrix and array-level operation by analyzing a real 1S1R OTS+PCM Crossbar based on Double-Patterned Self-Aligned (DPSA) cell architecture with 60×80 nm dimensions integrated in a 1 kbit configuration.

The investigation examines Crossbar architecture considerations, including critical design decisions for inhibit voltage schemes that balance functionality against power consumption. Two primary biasing approaches are analyzed: the V/2 scheme, which minimizes power consumption, and the 1/3V–2/3V scheme, which reduces voltage stress on half-selected cells at the expense of dramatically increased power. Experimental results demonstrate successful Crossbar operation, with a clear threshold voltage (V_{th}) separation between Low and High V_{th} states, validating material and device consistency across various integration architectures. However, the electrical characterization is challenging due to the large number of half-selected device switching events.

The chapter extends beyond OTS+PCM Crossbars by examining emerging paradigms, including 3D vertical integration architectures and selector-only memory. The overview includes research focusing on atomic layer deposition for high-aspect-ratio structures, as well as novel selector-only memory approaches that combine storage and selection functions in a single chalcogenide layer.

Preliminary experimental results on 1T1S OTS selector-only memory demonstrate a threshold voltage separation of 200 mV, indicating potential for next-generation memory implementations. This work establishes essential design principles for high-density Crossbar, identifying critical areas that require further development, including materials with reduced threshold voltage variability.

6.1 Moving from 1T1S1R Arrays to 1S1R Crossbars

The preceding chapters have systematically investigated the electrical performance and programming characteristics of individual memory devices, specifically those based on one-transistor-one-selector-one-resistor (1T1S1R) architectures. In these configurations, the presence of a dedicated access transistor enables selective addressing of individual memory cells while effectively isolating them from the neighboring ones, thereby preventing unwanted interference.

However, as mentioned in Chapter 1, a true Crossbar array fundamentally relies on the intrinsic selective capabilities of the Ovonic Threshold Switching (OTS) device, eliminating the need for dedicated access transistors. This transition from transistor-controlled matrices to selector 1S1R Crossbar arrays represents a critical paradigm shift, introducing new challenges and considerations that cannot be directly extrapolated from individual device studies.

To bridge the gap between device-level characterization and array-level implementation, this chapter presents a comprehensive analysis of a real 1S1R OTS+PCM Crossbar based on the double-patterned self-aligned (DPSA) cell structure [R10]. The investigation addresses the unique operational challenges inherent to Crossbar architectures and provides insights into the transition toward practical high-density memory implementations.

6.1.1 Crossbar Array Architecture Considerations

The experimental Crossbar array consists of a 1 kbit configuration with aggressive lateral cell dimensions of 60×80 nm, integrated within a Multi-Project Wafer (MPW) using the 200 mm CEA-Leti Memory Advanced Demonstrator (MAD) platform [R10]. The complete system incorporates essential peripheral circuitry, including addressing logic (shift registers and multiplexers), programming control units, and sensing elements (sense amplifiers and series transistors). **Fig. 6.1** presents a simplified schematic diagram that emphasizes only the components relevant to this discussion.

Each crosspoint intersection between bit lines (BL, vertical conductors) and word lines (WL, horizontal conductors) contains a DPSA OTS+PCM cell comprising $Ge_1Sb_4Te_4$ (GST144) PCM and GeSbSeN (GSSN) multilayer OTS selector, as detailed in Section 2.5 and Chapter 5. The symmetric array configuration features N = M = 32 rows and columns.

Each bit line can be polarized either to the programming voltage (V_{top}) or the inhibit voltage (V_{inhib}) through a multiplexer. Similarly, word lines connect to ground (V_{bottom}) through an NMOS transistor or directly to V_{inhib}. The word line NMOS provides current compliance through V_{comp} while enabling current reading at the transistor source. Under typical operating conditions with V_{bottom} = 0 V and sufficient compliance, the

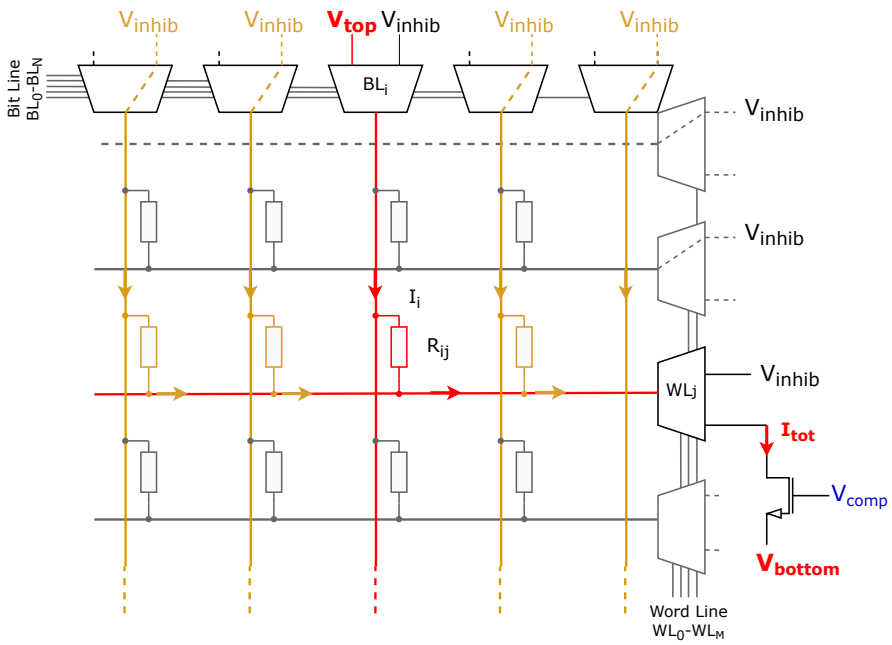


Figure 6.1: Simplified schematic of the 1S1R Crossbar array showing the essential components for Crossbar operation. Each intersection contains a DPSA OTS+PCM cell. Each bit line (vertical) and word line (horizontal) can be individually multiplexed between two voltages; a series transistor on the word line allows current compliance. The selected device at BL_i, WL_j is colored in red, while the half-selected cells on the same WL are colored in yellow.

drain-source saturation voltage becomes negligible compared to the device programming voltages (e.g., 0.2 V$\ll$5 V).

The selection of appropriate inhibit voltage schemes represents a critical design decision impacting both functionality and power consumption. The voltage difference ΔV between unselected lines must be carefully controlled to prevent unwanted switching while minimizing leakage current [18, 22, 80, 100].

The $V_{top}/2$ bias scheme applies $V_{inhib} = V_{top}/2$ to all unselected lines (e.g., 1.75 V when $V_{top} = 3.5$ V). With this approach, the majority of the cells experience zero voltage difference ($\Delta V = 0$) and remain completely unselected. Only half-selected cells (connected to either the selected WL or BL) experience a $\Delta V = V_{top}/2$, with a total leakage current ($I_{leak,tot}$) scaling as:

$$I_{leak,tot} = ((M-1) + (N-1))I_{leak} = (M+N-2)I_{leak}$$

Where M and N are the array dimensions.

Alternative biasing applies $V_{inhib} = V_{top}/3$ to bit lines and $V_{inhib} = 2V_{top}/3$ to word lines. While this reduces voltage stress on all half-selected cells to $V_{top}/3$, it dramatically increases power consumption as the total leakage scales as

$$I_{leak,tot} = (M \cdot N - 1)I_{leak}$$

This is suitable only for applications where preventing unwanted switching takes priority over power efficiency.

6.1.2 Reading Operation in the Crossbar Array

For our experimental validation, we selected the $V_{top}/2$ scheme (e.g., $V_{inhib} = 1.75$ V). During read operations, a moderate voltage V_{top} (typically 3.5 V) is applied while maintaining $V_{bottom} = 0$ V. The total current collected from the selected word line WL_j depends critically on the memory state of the target cell and the cumulative leakage from half-selected elements.

For a cell in the RESET state (high resistance), the device remains OFF, and the measured current consists primarily of leakage contributions:

$$I_{OFF} = (N - 1)I_{leak} + I_{leak,j} \approx N \cdot I_{leak}$$

Where $I_{leak,j}$ represents the leakage through the selected cell, which could be approximated to the leakage of a half-selected cell under similar bias conditions[1].

Conversely, when the selected cell exists in the SET state, threshold switching occurs, producing a current I_{on} related to the ON resistance of the device (R_{ON}) and typically limited by the compliance current (I_{comp}) of the series NMOS transistor (Chapter 2).

The fundamental figure of merit for Crossbar readability is the Memory Window (MW), which must be as wide as possible to discriminate the programmed state correctly, and it is defined as the ratio between ON and OFF currents:

$$MW = I_{ON}/I_{OFF} = \frac{I_{ON}}{(N - 1)I_{leak} + I_{leak,j}} \tag{6.1}$$

This relationship reveals a critical array scaling limitation before the programmed states become indistinguishable from one another. We provided an estimation of possible MW and array size guidelines for our OTS+PCM devices in Section 4.3.2.

[1] In this discussion, we do not account for the voltage dependency of the subthreshold resistance, which produces different leakage depending on the bias voltage [39, 118]. Additionally, as mentioned later, the leakage of each half-selected cell depends on its state.

Modeling Assumptions and Limitations

The focus of our investigation is the device performance within a Crossbar array. To simplify the discussion, we make several approximations, each representing areas for future refinement, which are partially addressed by previous works [80, 81, 147]. All half-selected cells are assumed to exhibit identical leakage currents, though in reality, different memory states produce varying subthreshold conduction levels [39, 118]. Our assumption of half-selected cells in the SET states provides worst-case scenario results with the highest I_{leak}, proving a safe approximation. The model neglects subthreshold voltage dependence and potential threshold voltage shifts under inhibiting bias conditions [120]. For the relatively small array size investigated, line resistance effects are considered negligible compared to OFF-state device resistance, while the IR significantly impacts larger arrays.

6.1.3 Programming Operation in the Crossbar Array

Programming operations require significantly higher voltages ($V_{top} \geq 5$ V) with correspondingly larger inhibit voltages ($V_{inhib} \geq 2.5$ V). This voltage regime introduces a critical challenge: some OTS+PCM devices may exhibit threshold voltages within or below the inhibit voltage range, as demonstrated in the matrix studies presented in Chapter 3. Some of the half-selected devices may switch ON during programming, as this switching is uncontrolled and only clamped by the NMOS for the WL, which erases the cell into an unknown state, losing the information. This problem is especially challenging when trying to program a RESET cell: if a neighbouring cell on the same WL switches ON, it will drive a large current saturating at I_{comp}. This will in turn increase the voltage across the MOS, reducing the ΔV on the devices and preventing the selected cell from switching. The programming failure is challenging to identify since the measured current may appear normal.

An approach to address half-selected cell interference could be to deploy the more energy-demanding $1/3V_{top}$, $2V_{top}/3$ bias scheme. Circuit solutions, such as current mirror configurations, can provide better bias control throughout the array.

6.1.4 Early Experimental Results from 1S1R Crossbar Arrays

Fig. 6.2 presents the experimental threshold voltage distributions for both SET and RESET states measured from a subset of the 1 kbit array using the $V_{top}/2$ inhibit scheme. The measurement methodology requires careful control on V_{top} with an appropriate adjustment of V_{inhib}. The PCM material is our optimized $Ge_1Sb_4Te_4$ (GST144) and the OTS is a GeSbSeN (GSSN) multilayer (ML) alloy, as described in Chapter 5. The results demonstrate promising performance with a clear separation between the SET and RESET state distributions, comparable to the performance achieved in 1T1S1R matrix

configurations that integrate identical materials. This result validates the material co-development approach and confirms that fundamental OTS+PCM electrical performance metrics remain consistent across different integration architectures [R2].

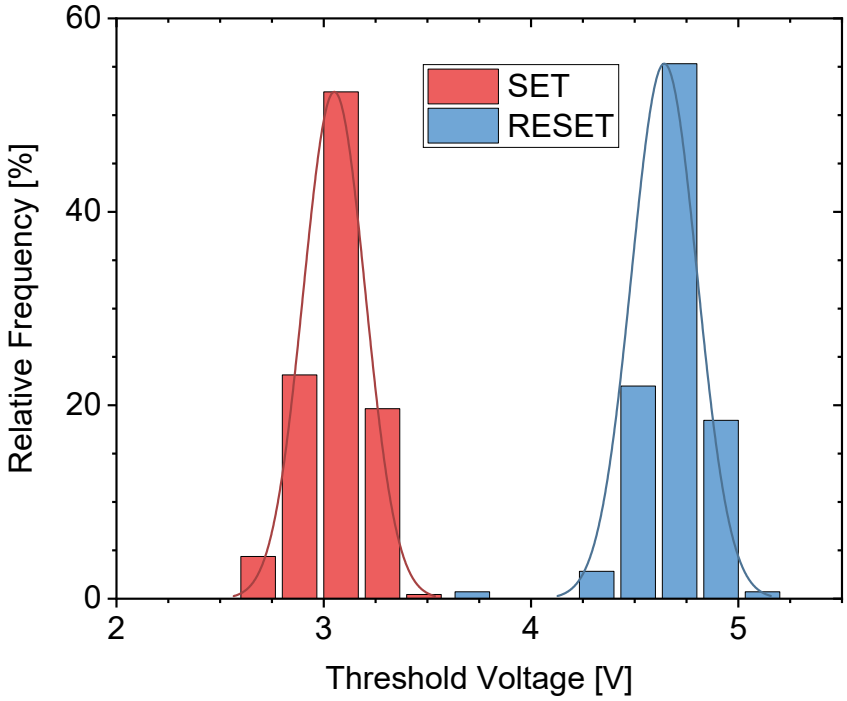


Figure 6.2: Threshold voltage distributions for SET and RESET states measured from a 1 kb 1S1R Crossbar array subset. The clear separation between states demonstrates successful Crossbar operation while highlighting material consistency with matrix implementations. Data from more than 140 60×80 nm DPSA devices.

The I–V curves of 137 devices reveal the complex behavior inherent to Crossbar (**Fig. 6.3**). The population can be categorized into three distinct groups based on the electrical behavior, and can be compared to a standard OTS+PCM electrical characteristic from 1T1S1R matrices (Section 2.5).

About 18 % are functional, exhibiting standard threshold switching behavior with a median value of V_{th} of approximately 3 V, with proper subthreshold conduction. Only a few (6 %) switch at significantly lower voltages ($V_{th} \leq 2$ V), with some showing resistive behavior indicative of partial OTS crystallization compatibility with common device defectivity. The majority, 76 %, show large currents saturating to I_{comp} without any clear switching signature.

Physical mapping of the high-current population suggests that these devices are predominantly located on identical word lines. This spatial correlation indicates that unintentional switching of individual devices due to inhibiting bias creates a cascading effect. Once a single device on a word line becomes conductive, it effectively blocks access to all

other devices on that line. Moreover, the high stress on the activated device may lead to early cell failure, causing a short on the line. This failure mode represents a fundamental reliability concern for Crossbar architectures, as repeated read/write operations increase the cumulative probability of device failure. The stochastic nature of the threshold switching exacerbates this issue, resulting in a progressive loss of accessible memory capacity on a line-by-line basis.

Despite this limitation, the identification of sufficient functional devices enabled the demonstration of threshold voltage distributions presented in Fig. 6.2, validating the Crossbar concept while highlighting areas requiring continued development. A possible mitigation pathway could be the adoption of $1/3V_{top}$, $2/3V_{top}$ bias scheme to reduce the number of unwanted switching events at the expense of larger current and heating.

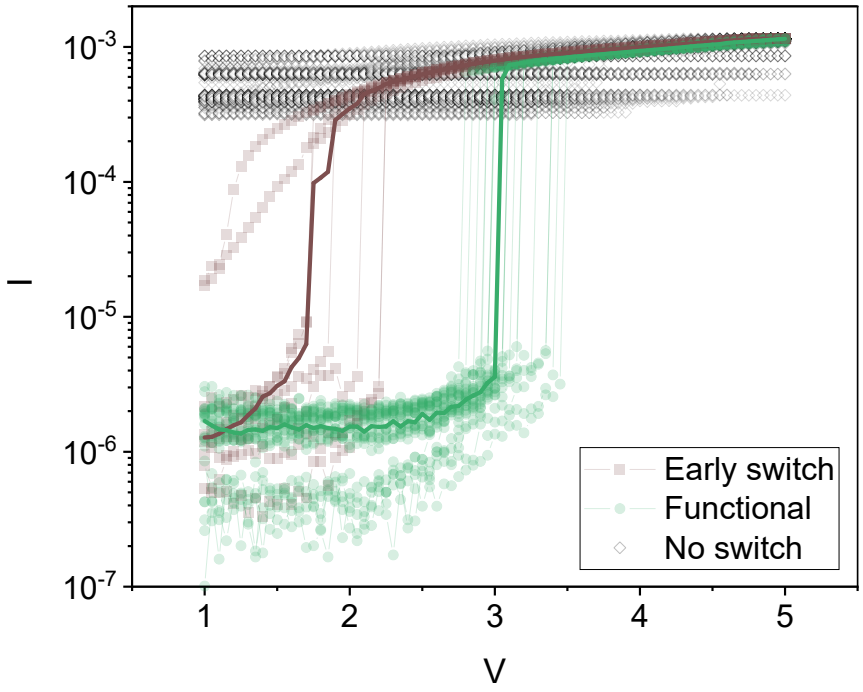


Figure 6.3: I-V characteristics of 137 60×80 nm DPSA Crossbar devices showing three distinct populations: functional devices (green, 18%), early switching devices (brown, 6%), and high-current devices (gray, 76%). The solid green and brown lines represent the median current of functional and early switching devices.

This study successfully demonstrates the feasibility of 1S1R Crossbar arrays based on DPSA cell architecture, achieving correct SET and RESET programming operations. The comprehensive material and device optimization studies presented in earlier chapters provide a crucial foundation for further development of Crossbars. The theoretical framework and experimental results from our arrays establish essential design principles for future high-density implementations. Key areas for continued development include OTS materials with reduced V_{th} variability and enhanced bias control for the half-selected cells.

6.2 Beyond the Crossbar

The 3D XPoint™ memory accelerator, originally proposed by Intel and Micron based on PCM+OTS Crossbar technology, promised fast DRAM-like performance at much larger capacities. Its development, dating back to 2009 [22], led to production in 2015 [7]. The development continued, and in 2020, Intel announced a 4-layer Crossbar implementation [148]. However, the 3D Xpoint technology did not achieve commercial success, suffering from the termination of the Intel–Micron joint venture in 2018 [149] and was finally discontinued by both companies in 2022 [150]. In an attempt to make integration of new memory modules easier, Intel shifted its focus toward software-centric solutions and the Compute Express Link (CXL) standard [151, 152]. Although this product provided good technical performance, it did not fully meet customer requirements, likely due to implementation constraints and integration overhead in existing server applications. The market failure highlighted the gap between promising memory technology and practical business considerations.

Although 3D XPoint was withdrawn, the drive for advanced Crossbar architectures has not diminished. Current industry efforts focus on developing next-generation Crossbar arrays for DRAM replacement applications, with companies such as SanDisk and others actively pursuing similar technologies [153, 154].

Contemporary research focuses on two primary directions: achieving 3D vertical integration, similar to the successful 3D NAND Flash approach, and developing selector-only memory concepts that integrate both memory and selector functions into a single active layer [155].

6.2.1 Advent of Selector-Only Memory

The optimization and development of memory materials with highly nonlinear electrical characteristics could provide intrinsic selecting capabilities, simplifying the device stack architecture. This concept, although not new, was first introduced in 2003 [35] as an early access-transistor-free memory based on highly resistive PCM. It has gained renewed attention with advancements in chalcogenide material engineering [156]. Recent developments in OTS chalcogenide alloys have demonstrated memory properties through controlled doping and tuning of alloy composition [78]. Having only one active material layer simplifies both integration and characterization.

The first significant advancement in OTS for memory applications was reported in 2021 [34], leading to various nomenclature within the research community:

- Self-Rectifying Memory (SRM) [34, 157];
- Self-Selecting Memory (SSM) [158, 159];

- Selector-Only Memory (SOM) [30, 160];
- Single chalcogenide XPoint Memory (SXM) [36];
- Threshold-Changeable Memory (TCM) [R6, R5];

These devices rely on local and reversible changes in the OTS amorphous matrix, leading to V_{th} variations depending on programming conditions such as current amplitude, pulse duration, or polarity. This phenomenon exhibits persistence over extended time scales and provides the foundation for a novel memory technology [64].

6.2.2 Early Experimental Results on Selector-Only Memory

Building upon the threshold voltage variability investigations presented in Chapter 4, where we observed that multiple reading operations could increase selector threshold voltage, we exploit this non-volatile threshold control for selector-only memory applications as a threshold-changeable memory [R6].

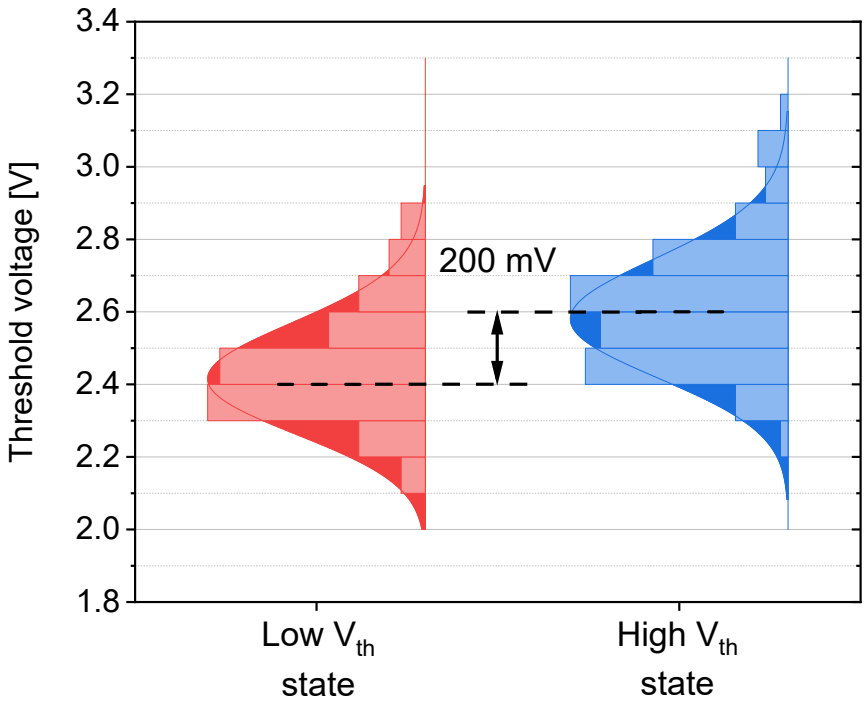


Figure 6.4: Threshold voltage distributions of DPSA OTS devices demonstrating two voltage states: Low and High V_{th}, obtained through positive and negative pulse programming. Data collected from 122 devices with 100×100 nm dimensions.

We systematically applied positive and negative voltage pulses to characterize their impact on the threshold voltage of DPSA 1T1S OTS cells (**Fig. 6.4**). The OTS is a GeSbSeN (GSSN) alloy, already studied in Chapter 3 and 4. The application of short

pulses affects the V_{th} depending on the polarity; while longer positive pulses with sufficient fall time (similar to SET pulses used in PCM) can restore the original lower threshold state.

The extended voltage staircase used for V_{th} detection provides sufficient energy to recover the original state (Low V_{th}). This observation suggests that the memory effect is related to reversible structural modifications rather than permanent material changes.

We identified two distinct voltage states (Fig. 6.4) corresponding to positive (Low V_{th}) and negative (High V_{th}) programming pulses. Through pulse optimization, we achieved approximately 200 mV separation between the median values of the two populations. Notably, the distribution shapes remain consistent between the two states, suggesting that negative pulse application does not modify the global conduction mechanism or material composition. Instead, the phenomenon appears related to local changes in the bonding structure within the chalcogenide matrix [161].

These preliminary results demonstrate the potential of SbSe-based OTS selectors for selector-only memory applications. However, additional electrical characterization is required to identify optimal candidate alloys. Due to the novelty of this technology, the literature remains limited but is rapidly growing due to the significant scaling potential of this technology.

6.3 Conclusions

In this chapter, we provide a comprehensive investigation of Crossbar array implementation, starting from device characterization obtained in a 1T1S1R configuration. We successfully demonstrate a 1 kb 1S1R Crossbar array, featuring significant threshold voltage separation between programmed states and consistent performance across different integration architectures, thereby validating the co-development approach pursued throughout this thesis (Section 6.1).

The experimental results confirm that fundamental OTS+PCM electrical performance metrics remain valid when transitioning from individual device characterization to array-level implementation (Fig. 6.2). However, the investigation reveals critical reliability challenges that must be addressed for practical deployment. In particular, a large part of devices exhibit high-current behavior without switching signatures, posing a serious reliability concern (Fig. 6.3). These findings establish that successful Crossbar deployment demands not only advanced materials but also sophisticated peripheral circuitry and bias control strategies.

Looking beyond limitations, the exploration of emerging paradigms offers promising pathways for transcending conventional Crossbar constraints. The investigation of vertical crosspoint architectures, enabled by atomic layer deposition techniques, and the

preliminary demonstration of selector-only memory concepts indicate potential solutions to current scaling and reliability limitations.

We experimentally validate a selector-only memory by achieving a 200 mV separation in SbSe-based selectors, representing a crucial step toward integrating memory and selectors into a single device (Fig. 6.4). This approach, combined with 3D vertical integration strategies, could address the fundamental challenges observed in conventional Crossbar implementations while enabling new computational paradigms that integrate storage and processing functions.

While current Crossbar architectures faced significant challenges in achieving the desired commercial success, the fundamental physics and materials science foundations are sound. The path forward requires continued innovation in materials engineering to reduce threshold voltage variability, development of advanced bias control circuits to mitigate half-selected cell interference, and exploration of novel architectures that simplify device structures. The insights gained from this Crossbar investigation provide essential guidance for the continued evolution toward practical high-density memory systems that can meet the demanding requirements of next-generation computing applications.

Conclusions and Perspectives

This manuscript proposes a comprehensive foundation for understanding, optimizing, and deploying Phase-Change Memory (PCM) and Ovonic Threshold Switching (OTS) selectors targeting Crossbar array applications for next-generation non-volatile memory applications. The work bridges the gap between individual device characterization and practical array implementation through systematic investigation of programming reliability, reading-induced degradation mechanisms, material optimization strategies, and Crossbar-specific challenges.

Conclusions

This work pursues three core objectives on the study and reliability of the OTS+PCM: a first devices characterization and validation; a complete investigation on programming and reading reliability; and material engineering for performance optimization. The three objectives are interconnected, and the presented results are at the foundation of the one-selector one-resistor (1S1R) Crossbar array demonstration concluding this work (Chapter 6).

The objectives are tackled following a rigorous approach, with the use of techniques and protocols outlined in Chapter 2, in particular with the integration and validation of a Double-Patterned Self-Aligned (DPSA) cell used as the test vehicle throughout the manuscript.

To address the first objective, the integrated devices are characterized to highlight the basic performance metrics such as the SET and RESET threshold voltage (V_{th}) distributions, the cycling endurance, and the effect of scaling of the Critical Dimension (CD) on the electrothermal behavior of the cell (Chapter 3).

In the following, we present the extensive reliability and failure analysis of the reading operation (Chapter 4), presenting for the first time to our knowledge the effect of switching-induced threshold voltage shift of the programmed state. We modeled this phenomenon as a critical reliability concern to understand its causes and suggest possible mitigation strategies.

Finally, we engineer the PCM and OTS materials to improve device performances in

light of the reliability results previously proposed (Chapter 5). We focus our attention on the role of the Sb/Te ratio in GeSbTe PCM as a means of improving the SET speed and the endurance while keeping a large resistance window. Similarly, we propose multilayer integration and new material exploration for OTS compositions to improve the selector reliability. The multilayer deposition approach proves useful to reduce device variability. We propose As-based OTS alloys to reduce and eventually suppress the forming voltage, which is critical for applications requiring lower operating voltage supplies.

We leverage the gained knowledge on devices and materials to fabricate and characterize a 1S1R Crossbar array based on optimized PCM and OTS materials (Chapter 6). This demonstration concludes our work and paves the way for future research aiming to improve the Crossbar functionality.

Devices Programming and Thermal Behavior

The research presented in Chapter 3 establishes a detailed understanding of programming operations and cell thermal behavior in OTS+PCM 1S1R architectures, particularly leveraging the Double-Patterned Self-Aligned (DPSA) structure. Device validation was achieved across critical dimensions down to 40 nm, with statistical analysis justifying Gaussian and Gamma distribution for threshold voltage modeling (Section 3.3). Single-population models are insufficient to capture device wear due to extended cycles; therefore, care must be taken when evaluating the population's failure modes to isolate the contributions from fabrication variability (Section 3.4).

The active layer confinement in the DPSA cell, especially when co-integrated with an OTS, significantly increases the thermal confinement, changing the programming characteristic and impacting the device's performance. We supported the electrical characterization with TCAD electrothermal simulations combined with TEM images, demonstrating that DPSA integration intensifies thermal confinement (Section 3.5). During RESET programming, a complete volume amorphization occurs, which improves energy efficiency by lowering the programming currents. Yet the increased temperature and reduced thermal gradient pose significant challenges for SET operations, which rely on growth-dominated crystallization in GeSbTe alloys. The TEM analysis confirms that the active region of the PCM cells involves nearly the whole volume, reducing the presence of crystallites and requiring nucleation in order to achieve a crystalline state.

Reading Reliability

The discovery and characterization of reading-induced threshold voltage shifts in 1S1R configurations represents a major original contribution (Chapter 4). We developed and applied a dedicated protocol to isolate the contributions to the V_{th} shift coming from PCM

memory elements (1R) and OTS selectors themselves (1S) demonstrating that SET state threshold voltage increases from two distinct mechanisms: a gradual increase correlated with the number of OTS switching events, and a constant increase proprortional to the reading current associated to a partial amorphization of the PCM cell (Section 4.3). We developed an empirical model to capture the V_{th} shift, using it to predict the reading-induced bit-flip failures, correlating them with the number of switching, current, duty-cycle, and relaxation time between pulses. The reading-induced threshold voltage shift poses a significant reliability threat; our investigation suggests a potential mitigation strategy through optimized pulse shape and current, as well as customized read-verify schemes. Moreover, this phenomenon could be beneficial to specific applications, as in the case of Spiking Neural Network (SNN), which could exploit the increase in threshold voltage to implement an artificial neuron.

Material Optimization for PCM and OTS

Material optimization is central to overcoming integration challenges and performance bottlenecks. We target this objective with a systematic exploration of the role of the antimony-tellurium (Sb/Te) ratio in GeSbTe PCM alloys (Chapter 5). We demonstrate that congruent compositions with a higher Sb/Te ratio improve the SET state variability and SET speed thanks to faster crystallization kinetics, crystallizing the material directly into a stable hexagonal phase (Section 5.1). The increase of the Sb/Te ratio comes at the expense of a reduction of the resistance window. We proposed the optimized $Ge_1Sb_4Te_4$ (GST144) composition as the optimal trade-off between high and low Sb/Te compositions. GST144 benefits from a growth-dominated crystallization to achieve sub-100 ns SET speed while maintaining a large resistance window of more than three orders of magnitude. The devices exceeded 10^7 cycles and are expected to work at sub-10 ns speed for over 10^8 programming cycles. The exceptional performance of GST144 is extremely beneficial for OTS+PCM co-integration, addressing the speed limitations encountered with standard $Ge_2Sb_2Te_5$, and overcoming the effects of the thermal confinement of the scaled-down DPSA architecture. The resulting (1T)1S1R cells demonstrate threshold voltage windows of approximately 2 V, with reliable SET and RESET operations.

Complementary research into Ge-rich compositions advances thermal stability for automotive and embedded applications (Section 5.2).

For OTS, the adoption of nitrogen-doped GeSbSeN alloys (GSSN) and multilayer integration addresses reliability and threshold voltage variability, with carbon underlayers aiding interface diffusion management (Section 5.3). Further, arsenic-based forming-free selectors offer low voltage operation potential, but present environmental and process issues.

The co-integration of optimized PCMs and OTS selectors in DPSA structures vali-

dates the feasibility of achieving consistent array-level performance, by benefitting from the memory and selector material optimization (Section 5.4). We achieved the best performance combining the optimized $Ge_1Sb_4Te_4$ PCM alloy with a multilayer GeSbSeN (GSSN) OTS.

Crossbar Array Implementation

Finally, we conclude our work with the demonstration of a functional 1 kb Crossbar array with a 60×80 nm^2 cell critical dimensions to validate the transition from a 1T1S1R cell to an OTS-based array (Chapter 6). This investigation addresses additional array-specific challenges, including the switching of unselected cells, the role of sneak current paths, the bias schemes, and the impact of device-to-device variability. For this preliminary investigation, we adopted a V/2 bias scheme as a trade-off between consumption and half-selected cells stress, reporting the SET and RESET threshold voltage distributions (Section 6.1).

Perspectives

The perspectives outlined encompass near-term optimization opportunities, mid-term material and architectural innovations, and long-term system-level integration strategies. The emergence of Selector-Only Memory concepts and 3D vertical architectures suggests that research in the field remains active, with recent advancements that are potentially transformative. In light of these perspectives, we propose some preliminary results on a bipolar Selector-Only Memory (SOM) based on the GeSbSeN (GSSN) OTS alloy presenting different threshold voltage levels depending on the applied pulse conditions (Section 6.2). Continued fundamental research combined with engineering development targeting specific application requirements will determine the ultimate role of OTS+PCM or SOM technology in future computing systems, addressing the challenges of exponentially growing data volumes and evolving computational paradigms.

The convergence of materials science, device physics, circuit design, and system architecture demonstrated throughout this work exemplifies the multidisciplinary approach essential for advancing emerging memory technologies from laboratory demonstrations to commercial deployment. As the semiconductor industry confronts the limitations of conventional memory hierarchies and seeks solutions for data-centric computing, storage-class memory, and edge intelligence applications, OTS+PCM Crossbar arrays represent a promising technology pathway warranting continued investigation and development.

Materials Perspectives

Future research should prioritize continued material exploration across both PCM and OTS domains. Sb/Te ratio tuning and quaternary alloy design (via C, N, Si, In doping) offers potential for further performance and data retention improvement. The principles exposed in Chapter 5 can guide the exploration of doping optimized Sb/Te alloys to improve data retention and stability at high temperatures.

For OTS, development of arsenic-free forming-free selectors with tailored threshold voltages and enhanced thermal stability is a critical goal, as is long-range investigation into multilayer and interface-engineered stacks compatible with vertical integration techniques. Advanced characterization, such as in-situ TEM and synchrotron-based X-ray analysis, should underpin these developments, enabling real-time observation of cycling-induced changes and defect dynamics, which are expensive or difficult to achieve. The recently discovered memory effect in OTS selectors operating without phase change mechanisms offers the potential for simplified device structures, eliminating the need for separate memory elements. Understanding the physical mechanisms underlying this memory effect, as well as optimizing materials and programming conditions for an enhanced window, are the most pressing research challenges.

Several immediate research directions emerge from the limitations and opportunities proposed in this work. The optimization of programming schemes is a critical priority, particularly for achieving reliable programming, improving endurance, and minimizing energy consumption. Also, reading operation requires careful optimization, and further study has to confirm the nature of the threshold voltage shift in the OTS selector.

Architecture Perspectives

Architectural innovation is essential for scaling OTS+PCM technologies. The promising Selector-Only Memory (SOM) pathway may eliminate the need for separate storage elements. 3D vertical integration of OTS+PCM represents a critical pathway toward achieving extremely high aerial densities for storage applications. As the stacking of multiple conventional Crossbar levels becomes a limiting factor beyond a few layers, multiple innovative 3D architectures have been proposed [162], most notably the Vertical XPoint (VXP) configuration. The vertical architecture employs a *spaghetti-like* structure fabricated with planar word-lines intersecting long vertical bit-lines coated with PCM and OTS materials (**Fig. 6.5**) [52, 163]. This approach fundamentally differs from conventional planar scaling by utilizing the vertical dimension for capacity expansion, rather than reducing lateral feature size.

To achieve successful vertical integration, both materials engineering and advanced fabrication techniques require significant development. In particular, Atomic Layer Deposition (ALD) becomes mandatory when dealing with high aspect ratio structures, as

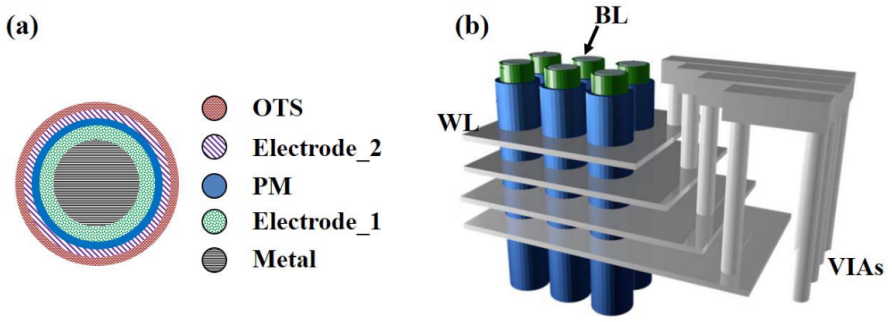


Figure 6.5: a) Vertical XPoint (VXP) cross-section consisting of a metal line coated with Phase-Change, Intermediate Metal, and OTS layers. b) Complete VXP scheme showing vertical bit lines intersecting horizontal word line plates. Reprinted from [52].

conventional PVD deposition techniques cannot provide adequate step coverage or conformality. The development of suitable precursors and deposition techniques for chalcogenide materials remains an active area of investigation [142, 146, 164]. These developments establish the foundation for practical vertical memory implementations.

Long-Term Perspectives

Long-term objectives must address integration into practical systems. This requires robust peripheral circuit design that accounts for device variability, advanced sense amplifiers, and adaptive programming/refresh algorithms. Statistical reliability modeling embedded within memory controllers, possibly leveraging machine learning for prediction, will be essential as manufacturing scales. Industrial qualification should focus on defect tolerance, self-repair, and standardized reliability metrics. The multidisciplinary approaches uniting materials science, device physics, architecture, and systems engineering showcased herein will be crucial for progressing OTS+PCM arrays from laboratory demonstrations to commercial deployment, especially in storage-class memory, embedded, neuromorphic, and automotive applications.

Author's publication list

The thesis work led to different publications in peer-reviewed journals and communications in international conference proceedings:

[R1] Renzo Antonelli. "Sb/Te Ratio Engineering in Phase-Change Memory for High SET Speed and Large Memory Window". *2025 IEEE European Solid-State Electronics Research Conference (ESSERC)*. 2025 IEEE European Solid-State Electronics Research Conference (ESSERC). Munich, Germany, Sept. 2025. URL: https://www.esserc2025.org/.

[R2] Renzo Antonelli et al. "OTS+PCM Material Exploration and Thermal Analysis for Crossbar Arrays". *Proceedings of the 2025 European Phase-Change and Ovonic Symposium (E\PCOS)*. European Phase-Change and Ovonic Symposium (E\PCOS). Marseille, France, Sept. 2025.

[R3] Renzo Antonelli et al. "Reading reliability analysis and modeling in 1S1R devices based on Phase-Change Memory and Ovonic Threshold Switching selector integrated in a double-patterned self-aligned structure". *Microelectronics Reliability* 172 (Sept. 1, 2025), p. 115801. ISSN: 0026-2714. DOI: 10.1016/j.microrel.2025.115801. URL: https://www.sciencedirect.com/science/article/pii/S0026271425002148.

[R4] C. De Camaret et al. "Effects of Carbon Lateral Implantation in Ge-rich GeSbTe Phase-Change Memory". *IEEE Electron Device Letters* 46.3 (Mar. 2025), pp. 385–388. ISSN: 1558-0563. DOI: 10.1109/LED.2025.3531547. URL: https://ieeexplore.ieee.org/abstract/document/10845864.

[R5] Mohamad Kanaan et al. "Innovative Threshold-Changeable Memory (TCM) Based on Amorphous GeSbSeN". *2025 European Phase-Change and Ovonic Symposium (EPCOS)*. 2025 European Phase-Change and Ovonic Symposium (EPCOS). Marseille, France, Sept. 23, 2025.

[R6] Mohamad Kanaan et al. "Threshold-Changeable Memory (TCM) Based on Amorphous GeSbSeN". *2025 International Conference on Solid State Devices and Materials*. 2025 International Conference on Solid State Devices and Materials (SSDM). Yokohama, Japan, Sept. 15, 2025.

[R7] Renzo Antonelli et al. "Programming Operations Analysis and Statistics in One Selector and One Memory Ovonic Threshold Switching + Phase-Change Memory Double-Patterned Self-Aligned Structure". *physica status solidi (RRL) - Rapid Research Letters* (Feb. 2024), p. 2300429. ISSN: 1862-6270. DOI: 10.1002/pssr.202300429. URL: https://onlinelibrary.wiley.com/doi/10.1002/pssr.202300429.

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[R10] G. Bourgeois et al. "Crossbar Arrays based on "Wall" Phase-Change Memory (PCM) and Ovonic-Threshold Switching (OTS) Selector: a Device Integration Challenge Towards New Computing Paradigms in Embedded Applications". *2023 7th IEEE Electron Devices Technology & Manufacturing Conference (EDTM)*. 2023 7th IEEE Electron Devices Technology & Manufacturing Conference (EDTM). Mar. 2023, pp. 1–3. DOI: 10.1109/EDTM55494.2023.10102961.

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