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Développement d'un pixel de type "temps de vol indirect" pour un capteur d'image 3D

Development of an indirect time-of-flight pixel for 3D imaging

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Summary

General introduction **4**
Working context . . . 4
Economical context . . . 5
Thesis work . . . 7
References . . . 8

1 Imaging techniques for distance measurement **8**
Introduction . . . 8
1.1 Broad overview of different techniques . . . 8
1.2 Time-of-flight measurement techniques . . . 10
1.2.1 Global versus rolling shutter sensors . . . 11
1.2.2 Direct time-of-flight . . . 12
1.2.3 Indirect time-of-flight . . . 13
Continuous modulated signal iToF . . . 13
Pulsed light iToF . . . 16
1.3 Time-of-flight pixels . . . 18
1.3.1 Near infra-red light detection . . . 18
1.3.2 Photodiode for infrared sensing . . . 20
PN junction . . . 20
Pinned photodiode . . . 23
1.3.3 Indirect time-of-flight pixels . . . 24
The CAPD iToF pixel . . . 24
The PPD iToF pixel . . . 26
1.3.4 2D imaging vertical gate pixel . . . 27
1.4 Indirect time-of-flight sensor architecture . . . 29
1.4.1 iToF image sensor on chip . . . 29
1.4.2 Charge and voltage domain pixel architecture . . . 30
1.4.3 Rolling and global shutter pixel architecture . . . 31
1.4.4 Indirect time-of-flight pixel architecture . . . 32
1.5 Figures of merit . . . 34
1.5.1 Demodulation contrast: DMC . . . 34
1.5.2 Parasitic light sensitivity: PLS . . . 35
1.5.3 Transit time: TrT . . . 35
1.5.4 Quantum efficiency: QE . . . 36
1.5.5 Power consumption: P_{Mod} . . . 36

1.5.6 Fullwell . . . 37
1.6 State-of-the-art of iToF pixel: performances & technology . . . 39
Conclusion . . . 41
Synthesis . . . 41
Goal of this work . . . 42
References . . . 44

2 TCAD simulation methodology iToF 45
Introduction . . . 45
2.1 Simulation tools benchmark . . . 45
2.1.1 Optical FDTD simulation . . . 45
2.1.2 TCAD electrical simulation & modeling . . . 49
Poisson . . . 49
Recombination/Generation . . . 50
Continuity . . . 50
Mobility . . . 51
2.2 Pinned photodiode modeling . . . 52
2.2.1 Electric potential distribution simulation . . . 52
(1.) Reset . . . 54
(2.) Integration . . . 54
(3.) Readout . . . 56
2.2.2 Fullwell computation . . . 59
2.3 Indirect time-of-flight pixel simulation . . . 62
2.3.1 Pixel modeling . . . 62
2.3.2 Electrostatic potential analysis . . . 63
2.3.3 Optical generation . . . 67
2.3.4 Transfer efficiency . . . 68
2.4 TCAD versus measurements . . . 70
Conclusion . . . 71
References . . . 72

3 MC simulation methodology iToF 77
Introduction . . . 77
3.1 MC modeling . . . 78
3.2 MC versus TCAD . . . 80
3.3 MC & TCAD versus measurements . . . 84
3.4 Statistical impact to the iToF technique . . . 88
3.4.1 Pixel response non-uniformity . . . 88
3.4.2 Depth non-uniformity . . . 89
3.4.3 MC simulation results . . . 90
3.4.4 MC simulation versus measurement . . . 93
Conclusion . . . 96
References . . . 97

4 Current assisted photonic demodulor: silicon & germanium 99
Introduction . . . 99
4.1 The current assisted photonic demodulator . . . 100
4.2 Reverse engineering of the CAPD pixel . . . 101
4.2.1 Optical simulation . . . 104
4.2.2 Electrical simulation . . . 107
4.2.3 Proposition of improvements . . . 112
Substrate doping concentration . . . 112
4.2.4 Limitations . . . 115
Biasing versus transfer efficiency . . . 115
Pitch reduction . . . 116
4.3 Ge CAPD state-of-the-art . . . 119
4.4 Fabrication: Ge CAPD . . . 120
4.4.1 Different design simulation results . . . 122
4.4.2 Comparison with measured results . . . 125
Conclusion . . . 128
References . . . 129

5 Trench vertical gate iToF pixel development 131
Introduction . . . 131
5.1 Devices with deep trench isolation . . . 134
5.1.1 Capacitive deep trench isolation CDTI . . . 135
Electrical behaviour . . . 135
Optical behaviour . . . 139
5.1.2 Passive DTI . . . 141
5.2 Planar gate iToF pixel: improvements & limitations . . . 143
5.3 Vertical gate 2D imaging pixel . . . 147
5.3.1 Trench vertical gates fabrication . . . 148
5.3.2 Sensing node trench insulation . . . 149
5.3.3 Photogate . . . 150
5.4 Vertical gate iToF pixel . . . 154
5.4.1 Fast photogate pixel schematic . . . 154
5.4.2 Pixel electrical response simulation . . . 156
5.4.3 Pixel biasing and consumption . . . 158
5.4.4 2D mode biasing optimization . . . 160
5.5 Fast photogate proposed designs . . . 161
5.5.1 Design variants . . . 163
5.5.2 Optical simulation of the reference pixel . . . 165
5.5.3 Process splits . . . 167
SNTI depth & N+ optimization . . . 167
TVG depth & P-Well optimization . . . 168
Epitaxy doping optimization . . . 170
5.6 Comparison with prior state-of-the-Art . . . 171
5.7 Fabrication & process validation . . . 173
5.7.1 Epitaxy doping . . . 173

5.7.2 TVG & SNTI morphology 174
5.8 Perspectives 177
Conclusion 178
References 180

General conclusion **183**
Abstract 183
Distance measurement techniques 185
Multiphysics simulation methodology 187
3D Monte Carlo simulation 187
Studies on CAPD Pixels 188
New solution using trench vertical gates 188
Perspectives 189

Annex **191**
6.1 Direct time-of-flight pixels 191
6.2 Optimization study using MC 193
6.3 Other materials for infrared detection 196
6.4 Germanium CAPD additional results 198
6.4.1 CAPD Ge-P+ sole fabrication flow 198
6.4.2 Sole accumulation of wholes 200
6.4.3 Different process alternatives table 200

Résumé en français **202**
Introduction et contexte 202
Synthèse des principaux résultats 203
Chapitre 1 : Techniques de mesure de distance 203
Chapitre 2 : Méthodologie de simulation multiphysique 203
Chapitre 3 : Simulation Monte Carlo 3D 205
Chapitre 4 : Études sur les pixels CAPD 205
Chapitre 5 : Nouvelle solution avec grilles verticales 206
Perspectives 207

Lexic and mathematical terminology:

i.e. *id est*

e.g. *exempli gratia*

$<,>$ Dot product

$||$ Absolute value

$\frac{\delta}{\delta t}$ Partial differentiation versus time

$Re\{\}$ Real part

$fft[]$ Fast Fourier transform

MC Monte Carlo

General pixel terminology:

iToF Indirect time-of-flight

pToF Pulsed indirect time-of-flight

SPAD Single photon avalanche diode

CAPD Current Assisted Photonic Demodulator

GS Global shutter

PD Photodiode

PPD Pinned photodiode

PG Photogate

FPG Fast-photogate

Physics constants and terms:

ϕ Phase.

ϵ Permittivity

ϵ_0 Permittivity of the void

ϵ_R Relative permittivity

ϵ_{Si} Silicon permittivity

μ_0 Permeability of the void

μ_R Relative Permeability

h Plank's constant

q Elementary charge

c Light speed in free space

$\mathscr{E}$, $\vec{\mathscr{E}}$ Electrostatic field vector

$\mathscr{B}$ Magnetic field

$\mathscr{P}$ Poynting vector

E_C, E_V Conduction and valence energy level

E_i Ionization energy level

E_F Fermi energy level

E_{gap} Band gap energy

E_{ph} Energy of a photon

V_{bi} Built-in voltage

V_T Threshold voltage

V_{fb} Flat band voltage

C_{ox} Gate oxide capacitance

C_D Depletion capacitance

C_{inv} Inversion layer capacitance

μ free carrier mobility

$\mathscr{A}$ Absorption coefficient

$\mathscr{T}$ Transmission coefficient

P_{ph} Optical power of the incident light

$\mathscr{G}_{ph}$ Optical generation rate

SRH Shockley-Read-Hall

Electrical, optical and design terminology

NIR Near infrared

$SWIR$ Short infrared

SN Sensing node

TG Transfer gate

C_{TG} Transfer gate capacitance

$\widehat{C}_{TG}$ Average transfer gate capacitance in a biasing interval

GND Ground

RST Reset

V_{BD} Breakdown voltage

DMC Demodulation contrast

PLS Parasitic light sensitivity

TrT Transit time

QE Quantum efficiency

$PRNU$ Pixel response non-uniformity

DNU Depth non-uniformity

Technology terminology:

TCAD echnology Computer-Aided Design

MC Monte Carlo

BSI Back-side illumination

FSI Front-side illumination

VIA Vertical interconnect assembly

AR layer Anti-reflective layer

Ge-on-Si Germanium-on-Silicon technology

General introduction

Working context

An image sensor is a device that captures a scene by transforming it into an electrical signal, which is then transmitted, processed and stored in the sensor circuits.

The history of image sensors dates back to the invention of the photography, with the development of silver-based photography techniques in the early 19th century. The first image sensors were based on Charge-Coupled Devices (CCD) [1], which replaced photographic film with an electronic sensor that could capture and store images. Today, Complementary Metal-Oxide-Semiconductor (CMOS) image sensors have replaced CCDs and are used in a wide range of applications [2], from scientific and medical imaging to consumer photography[3]. The rise of smartphones has led to an explosion in the number of photos taken each year, making it accessible to anyone with a smartphone and allowing to capture and share moments from their daily lives in ways previously unconcieved.

Additionally to 2D image sensors used for taking family and dog pictures, 3D image sensors have been conceived to provide depth information [3]. They are capable of measuring the distance between the camera and a point in the scene for each pixel.

The popularity of 3D imaging is growing, and the potential applications are vast. For example, the automotive industry is interested in this type of sensor to increase safety in vehicles. For smartphones or computers, this type of sensor could be used for facial recognition, providing a secure payment method or simply a new way to unlock these devices.

The thesis work is part of the development of digital image sensors using CMOS technology at STMicroelectronics, with the aim of producing increasingly high performance and innovating image sensors for consumer applications. In the R&D team for the technology for optical sensors, the work involved developing a new pixel for acquiring 3D images, combining the company existing expertise with new insights in imaging technology.

Economical context

CMOS image sensors are widely used in digital cameras and other imaging devices. They are a significant player in the semiconductor market with various applications, ranging from consumer mobile and automotive to security and medical applications. In 2022, the market reached a total of 21.3 billion dollars (Fig. 1).

A significant share of this market is the 3D imaging market, accounting for up to 8.2 billion dollars of the total market share (Fig. 2). Unlike 2D CMOS image sensors, 3D image sensors are required to provide depth information for every pixel. The projected growth for the 3D imaging market is much more significant, with more than double of the volume expected by 2028. The rise of the importance of the 3D imaging sector has its roots in the increasing number of applications using such technology. This includes spatial recognition in autonomous vehicles, facial recognition in smartphones and security applications, as well as various medical, industrial, and defense applications. STMicroelectronics is a leading actor in this market, accounting for more than 9% of the total revenue (Fig. 3).

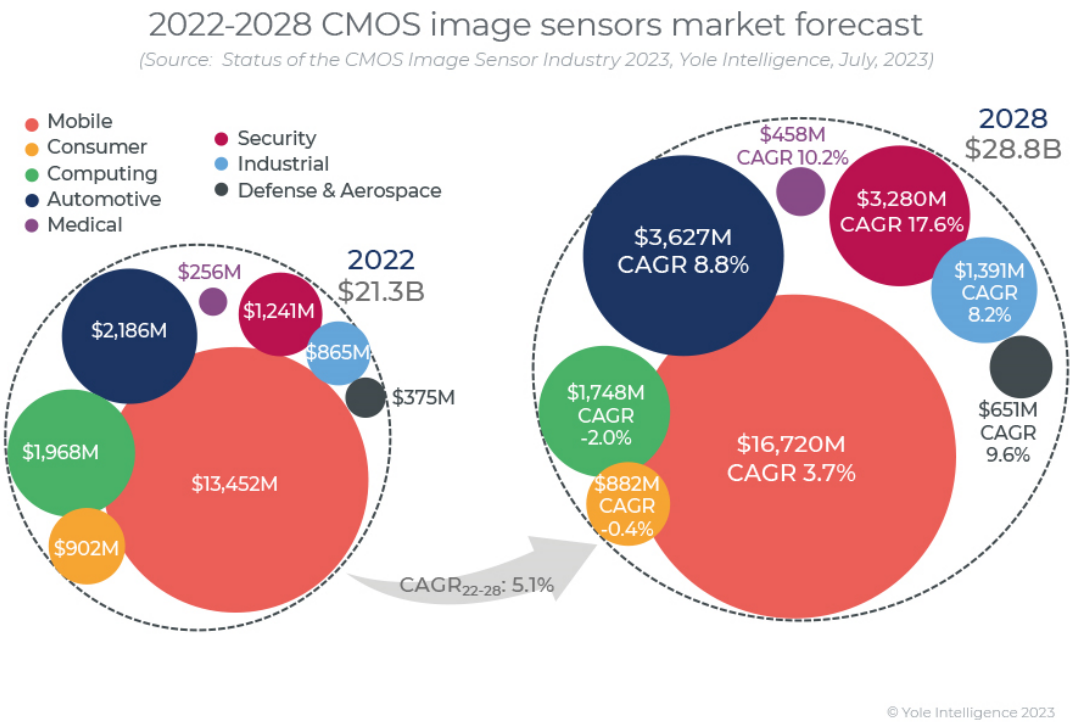


Figure 1: CMOS imaging market forecast [4].

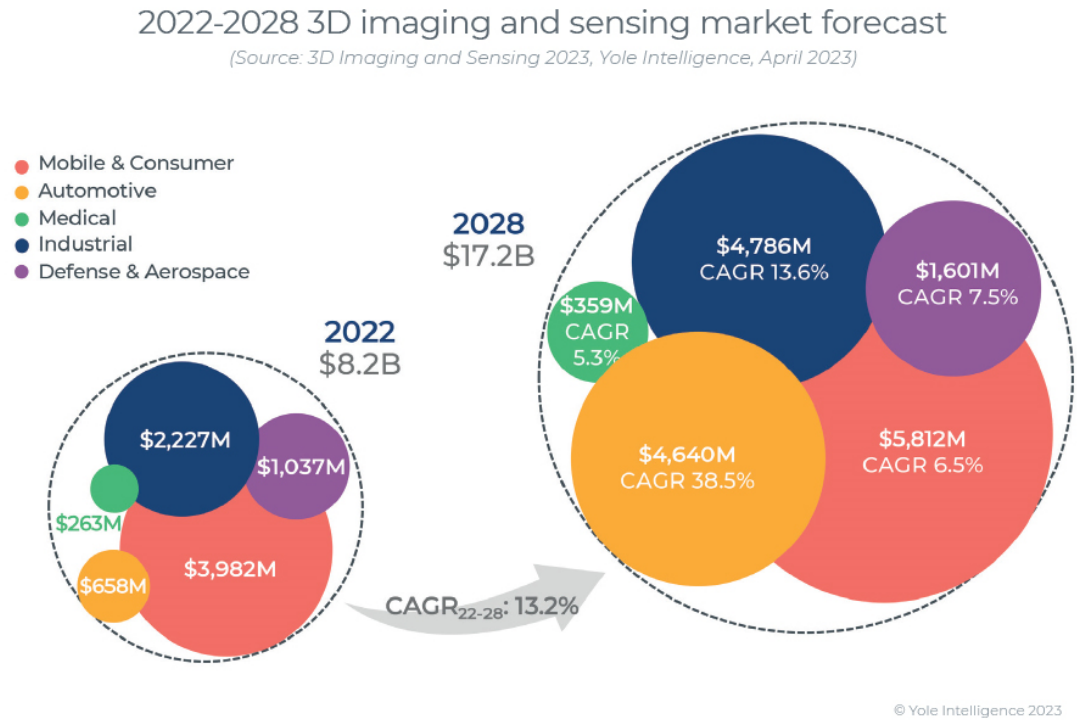


Figure 2: 3D imaging market forecast [5].



Figure 3: Leaders in mobile and consumer 3D cameras market [5].

Thesis work

The measurement of distance is a fundamental task in many applications, including robotics, automotive, and industrial automation. Optical techniques have been widely used for distance measurement due to their high accuracy and non-contact nature. This thesis focuses on the design and optimization of intensity-modulated time-of-flight (iToF) image sensors, which are widely used for distance measurement.

Chapter 1 provides an overview of the optical techniques used for distance measurement. The principles of time-of-flight (ToF) and continuous wave (CW) modulation methods are discussed. The different types of optical sensors used for distance measurement, including 2D and 3D image sensors, are also described.

Chapter 2 presents the simulation methodology used for the design and optimization of iToF image sensors. The TCAD (Technology Computer-Aided Design) simulation tools used for the analysis of the iToF pixel architecture are described. Complementarily, in chapter 3, a Monte Carlo methodology for simulating iToF pixels is presented. This new methodology allows the simulation of statistical quantities giving a better understanding of noise figures of merit.

Chapter 4 and 5 present the studies done to develop new pixels using this methodology. Chapter 4 focuses on the design and optimization of "fast integration" CMOS compatible architectures for iToF image sensors. The different presented architectures and technologies are used in current assisted photonic demodulators (CAPD). The advantages and disadvantages of each architecture and technology are discussed. In chapter 5, the design and optimization of "sophisticated integration" CMOS compatible architectures for iToF image sensors are presented. The different types of sophisticated integration techniques used for iToF image sensors are described, including stacked pixel architectures and various other key process developments used in high performance devices. The optimization of technological and geometric parameters for the sophisticated integration CMOS compatible architectures for iToF image sensors is also discussed.

This thesis aims to design and optimize innovating iToF solutions for 3D image sensors. The different chapters cover the various aspects of the work done in the research and development of iToF image sensors. It includes the modeling, simulation, design and fabrication of the proposed iToF solutions.

1 - Imaging techniques for distance measurement

Introduction

This chapter introduces the state-of-the-art 3D imaging techniques, with a special focus on the indirect time-of-flight technique (iToF) and iToF 3D imaging complementary metal oxide semiconductor (CMOS) pixels. A broad overview of different optical depth sensing techniques is given in the first section. After that, a special focus is given for the various time-of-flight (ToF) techniques: a broad overview of ToF techniques is provided, it is followed by an overview of pixels used for ToF detection, with an in-depth description of the indirect ToF pixel. The following section on the sensor architecture and the pixel circuits focuses on iToF. Finally, a detailed description of the main figures of merit is given.

1.1 Broad overview of different techniques

Distance measuring techniques can be classified into three groups: (i) interferometry [6, 7], (ii) triangulation [8, 9] and (iii) time-of-flight [10, 11]. Fig. 1.1 provides a visual representation of these techniques. The main difference between them lies in the light path from emitter to receiver.

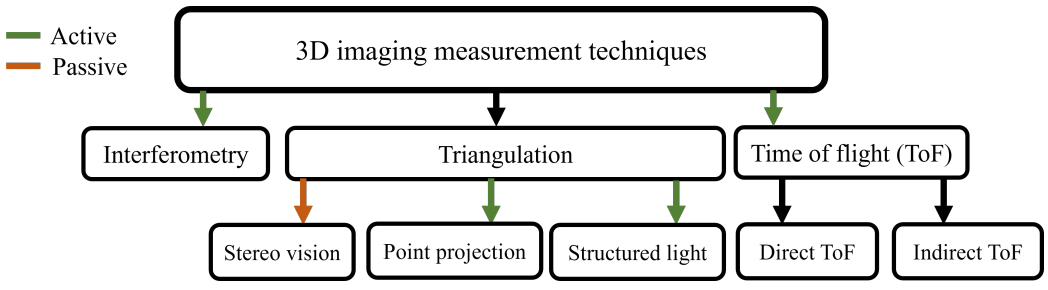


Figure 1.1: 3D imaging measurement techniques.

[(i)]Interferometry involves computing the distance from the interference of two coherent waves. The emitted wave is split into two beams, with one directed at a target that reflects it back, while the other serves as a reference. The interference between the two beams changes with the distance to the target, and the light intensity

provides an image of the phase difference between them. This method is commonly used for high-precision short distance range measurements of less than 1 mm [10, 12].

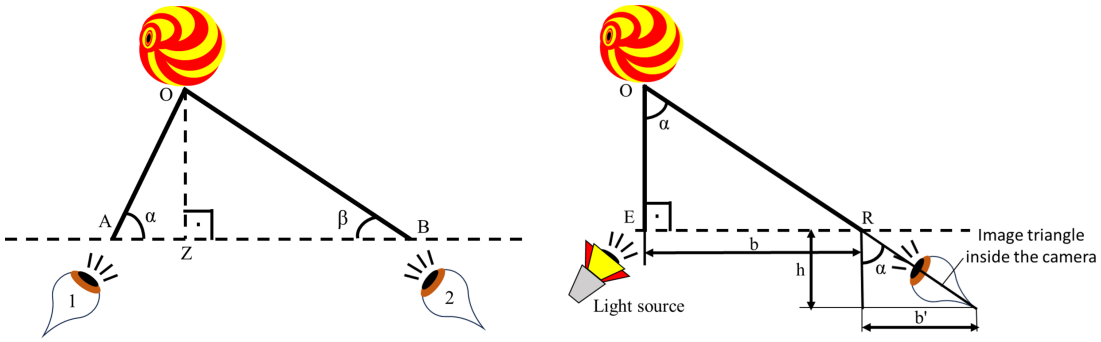
$^{(ii)}$Triangulation-based techniques are geometrical approaches. Passive triangulation, such as stereo vision, involves observing a scene from two different perspectives, A and B. Fig. 1.2(a) shows a schematic of a triangle used to measure the distance represented by the section $\overline{OZ}$ using two cameras 1 and 2. The trigonometric relation for $\overline{OZ}$ is given in equation (1.1) versus the angles α ($O\widehat{A}B$) and β ($O\widehat{B}A$).

$$\overline{OZ} = \frac{\overline{AB}}{\frac{1}{tan\alpha} + \frac{1}{tan\beta}} \tag{1.1}$$

Active triangulation, on the other hand, only uses a single camera. A trigonometric relation is drawn from the distances between the emitter (E, a light source), the receiver (R, a camera sensor), and the target object (O). The schematic of this method is shown in Fig. 1.2(b). The measured distance $\overline{OE}$ can be computed as indicated by equation (1.2), where h is the focal distance of the camera, b the distance between the emitter and the receiver and b' the distance of the point projection inside the camera.

$$\overline{OE} = h\frac{b}{b'} \tag{1.2}$$

The precision of triangulation-based techniques highly depends on the distance between the cameras or the emitter and receiver. For example, structured illumination is an active triangulation technique that significantly looses precision for longer distances [13]. The structured illumination technique consists in illuminating the scene with 2D spatially varying intensity patterns. The schematics for such a technique is similar to the one in Fig 1.2(b), only the light source intensity is modulated. An image sensor measures the light intensity reflected by the object. From the 2D image with the spatial variation of light intensity, it is possible to extract depth information [14]. This technique can have a significant computational load [13]. However for the acquisition, it only requires a standard 2D image sensors.



(a) Stereo vision (b) Point projection

Figure 1.2: (a) Passive and (b) active triangulation techniques for distance measurement.

1.2 Time-of-flight measurement techniques

The time-of flight technique consists of measuring the time taken for a wave to travel from an emitter to an object and after the signal is reflected, from the object to a receiver. A schematic of the technique is shown in Fig. 1.3. The time the received signal is detected is t_{dist} and the stored reference time of the emitted signal is t_0. The delay $\Delta t = t_{dist} - t_0$ between the emitted and the received signal is computed. This Δt time difference is proportional to the distance from the sensor to the object d. Knowing the propagation velocity v_p of the emitted signal, the traveled distance d is computed as in equation (1.3).

$$d = \frac{v_p \Delta t}{2} \tag{1.3}$$

The propagating wave can vary significantly in wavelength, being sound (sonar), radio (radar), or light (lidar) [13]. Commonly, lidar applications with direct and indirect time-of-flight use wavelengths from 850nm to 940nm at Near Infra-Red (NIR) spectrum [15–18], which is mostly invisible to the human eye [19].

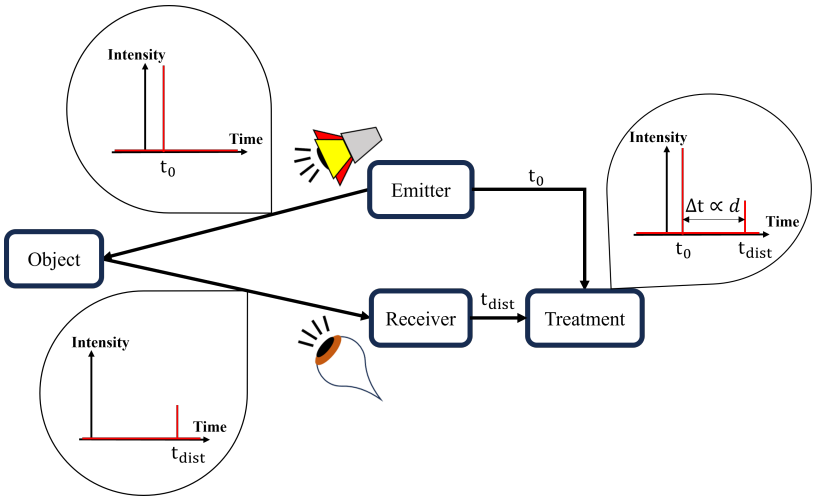


Figure 1.3: Direct time-of-flight scheme.

An overview of different technique advantages and disadvantages is given in Table 1.1. Time-of-flight technique is a performant competitor in terms of short range measurement. Despite its consequent system size, it is a good candidate for low consumption and high precision distance measurement.

In addition to the imaging technique, the sensor architecture may change depending on the application. For example, if the objective is to capture images of moving targets, a suitable architecture may be required for the sensor. Otherwise, the image may be degraded by motion blur. An alternative to avoid this issue is to separate the light detection and conversion phase from the readout phase by using a global shutter type architecture.

Table 1.1: Comparison of different depth sensing techniques [13].

3D optical measurement technique				
	Stereo vision	**Structured light**	**Interfero-metry**	**Time of flight**
System size	-	-	-	+
Short distance	+	++	+++	++
Long distance	-	-	–	++
Outdoor performance	++	++	-	+
Computational load	+	++	+++	++
Triangulation based	Yes	Yes	No	No
Range adaptability	-	-	–	++

1.2.1 Global versus rolling shutter sensors

There are two distinct phases in the process of capturing an image: the integration phase and the readout phase. During the integration phase, the sensor is exposed to a light source and the optical signal is detected and converted to an electrical signal inside the pixel. There are two types of image sensor exposure mechanisms: rolling shutter and global shutter [3, 20]. In rolling shutter, each line of the image is exposed sequentially. This exposition technique produces motion blur in images of moving objects due to the time difference between the exposure of the top and bottom of the image. In contrast, global shutter exposes the entire image at once, eliminating the distortion caused by rolling shutter delayed readout (Fig. 1.4) [21]. Nonetheless, the readout of the signal stored at each pixel for the global shutter sensor is also done sequentially in a rolling manner. As the exposure and the readout can be done simultaneously in the case of the rolling shutter sensor, they are often much faster than global shutter sensors. The choice between rolling and global shutter depends on specific application requirements, such as the high-speed imaging, favoring the use of rolling shutter type sensors or the presence of moving objects in the scene, favoring the use of global shutter type sensors [3, 21–23].

Fig. 1.5 shows the schematics for such a global shutter sensor. The two steps for the acquisition of an image with the global shutter sensor (i.e. integration and readout) are identified in Fig. 1.5. The change between each step is done by changing the state of the global shutter switch in Fig. 1.5, namely S_{GS}, This shutter is responsible for transferring the signal stored inside the pixel to the global shutter capacitor when activated (S_{GS}) and for separating the storage node inside the pixel from the global shutter capacitor (C_{GS}) when deactivated ($\overline{S}_{GS}$). During the integration phase, if

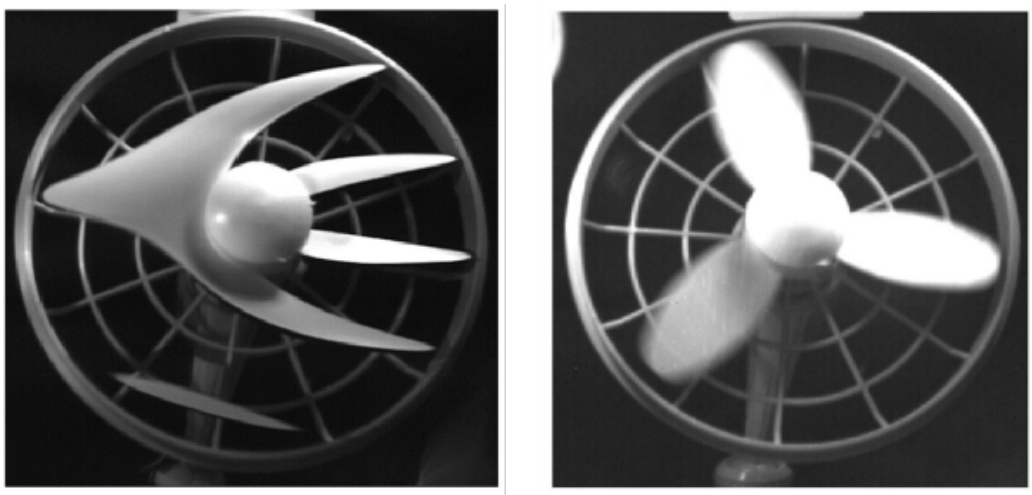


Figure 1.4: Rolling shutter and global shutter image of a moving target [21].

the photogenerated signal is transferred and stored directly in the form of a charge signal inside of the semiconductor, the pixel operates in the charge domain. Hence, it is called a charge domain pixel. In contrast, if the charge signal is first converted to a voltage signal when charges are transferred to a storage capacitor, it is called a voltage domain pixel. The case in Fig. 1.5 depicts the storage of the charge signal directly in the photodiode during integration, i.e. the shutter switch for transfer is deactivated ($\overline{S}_{GS}$). During readout, the signal of each pixel is transferred to a reading node, the shutter switch for transfer is activated (S_{GS}). Another integration can be started simultaneously to the treatment and reset of the readout signal.

Because of the complexity of 3D imaging operations such as structured light, discussed in section 1.1 and time-of-flight, the use of rolling shutter is limiting. Global shutter does not have the same fast readout requirements of rolling shutter, consequently it is more robust when detecting moving objects. Global shutter is often preferred for 3D imaging techniques due to high readout rates required for the matrix of pixel [13].

1.2.2 Direct time-of-flight

When a light pulse is emitted, the technique is called direct time-of-flight (dToF). It is the case of the schematic shown in Fig. 1.3. Measuring an optical signal requires a device sensible to the number of absorbed photons. With an impulse, this number is small. Because of that, single photon avalanche diodes (SPAD) are an alternative for 3D imaging [24–26]. They operate with the detection of the avalanche generated by a single charge carrier from the absorption of at least a photon. However, to be submitted to the avalanche, these sensors require high inverse biasing voltages, and they deliver high picks of current when activated. For more information see Annex 6.1.

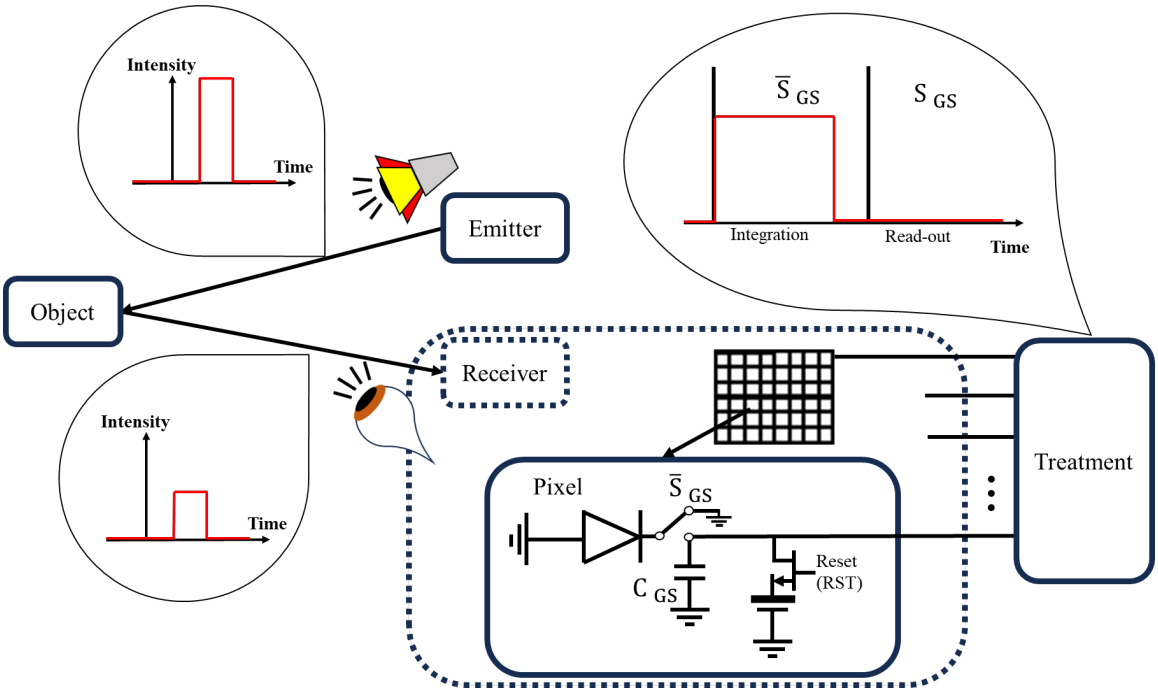


Figure 1.5: Global shutter scheme. The shutter that separates the signal in the pixel from the signal in the global shutter storage capacitor is identified by S_{GS} when activated and by $\overline{S}_{GS}$ when deactivated. C_{GS} is the global shutter capacitor.

1.2.3 Indirect time-of-flight

Continuous modulated signal iToF

A different technique is the indirect time-of-flight (iToF) measurement. The emitted optical signal can be a pulse or a continuous wave modulated in intensity, for example a sinus wave with frequencies from 10MHz to 250MHz [18, 27, 28]. The intensity of the signal is varied in accordance with the characteristic of the modulating sine wave. Hence, the signal is modulated in intensity. The time-of-flight is the time delay between the emitted and the received signal that is proportional to the distance traveled by the light signal. The distance measurement inside of the same period T, without time ambiguity caused by the periodicity of the light signal, is limited to D. For a given frequency, a maximum distance measurement proportional to the period of the signal is allowed with no ambiguity as shown in equation (1.4) [10]. The modulation frequency f_{Mod} is the frequency of the emitted signal with modulated intensity, the peeks of intensity are spaced in time by the period T and c is the light speed. Operating at different frequencies allows a more accurate measurement in larger distance ranges, eliminating this ambiguity. After measuring the phase shift ($d\phi$), the distance (dz) is computed with equation (1.5).

$$D = \frac{c \cdot T}{2} = \frac{c}{2 \cdot f_{Mod}} \tag{1.4}$$

$$dz = \frac{1}{2} D \frac{d\phi}{360^\circ} \tag{1.5}$$

For a continuous modulated light signal, a schematic of a sensor is shown in Fig. 1.6. The received signal photogenerates charges inside the photodiode of each pixel inside the matrix. For each pixel, the photogenerated signal is sampled into different collection sites. The sampled signal will later be used for the computation of the light signal phase shift. The pixel schematics in Fig. 1.6 illustrates a pixel with two separated collection sites, they are called sensing nodes (SN_1 and SN_2). The sampling of charges in time is done by alternating the activation of switches Sc_1 and Sc_2. The alternating activation of the switches guides charges that are transferred from the photodiode to the storage capacitors C_1 or C_2. When the Sc_1 and Sc_2 switches are deactivated, i.e. $\overline{Sc_1}$ and $\overline{Sc_2}$ the charge transfer from the photodiode to storage capacitors C_1 and C_2 is blocked. Indeed, during the readout, these switches are at the state $\overline{Sc_1}$ or $\overline{Sc_2}$ and the signal in capacitors C_1 and C_2 is transferred to the readout circuit by activating the global shutter switch S_{GS}. By doing so, the signal of the capacitors is copied in the pixel circuit. After this, the global shutter switch is deactivated again $\overline{S}_{GS}$ and both capacitors are reset before a new measurement is done. As in the previous global shutter schematic in Fig. 1.5, with the closed shutter, another acquisition can be done in parallel to the treatment of the previous acquisition.

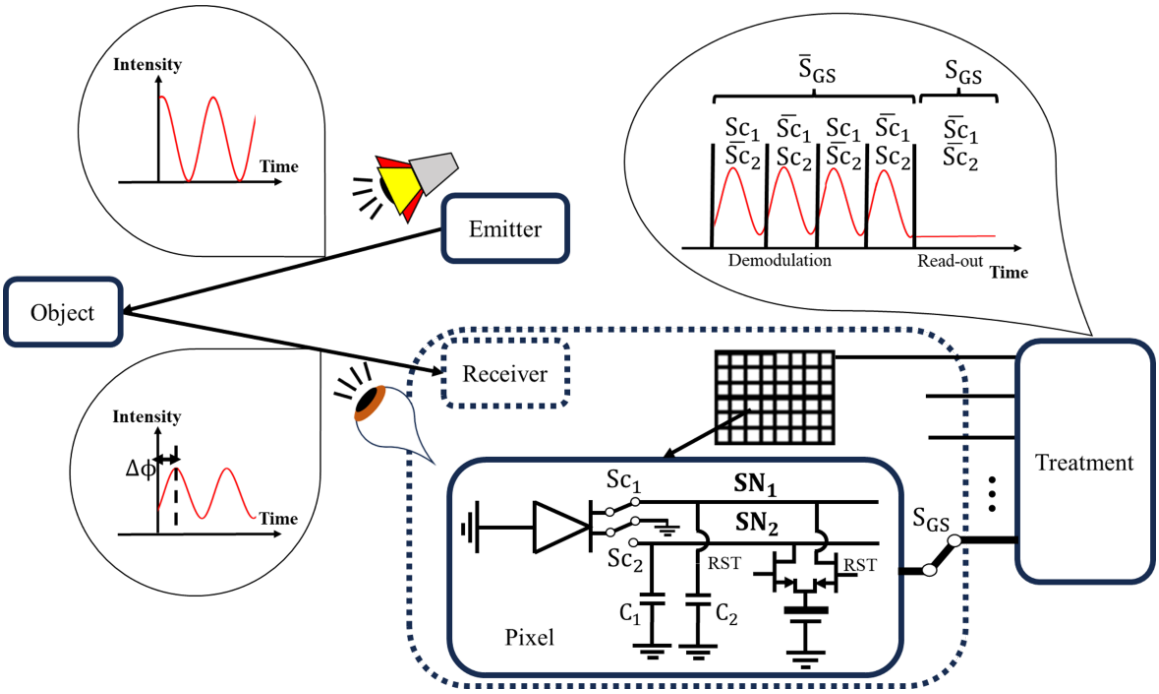


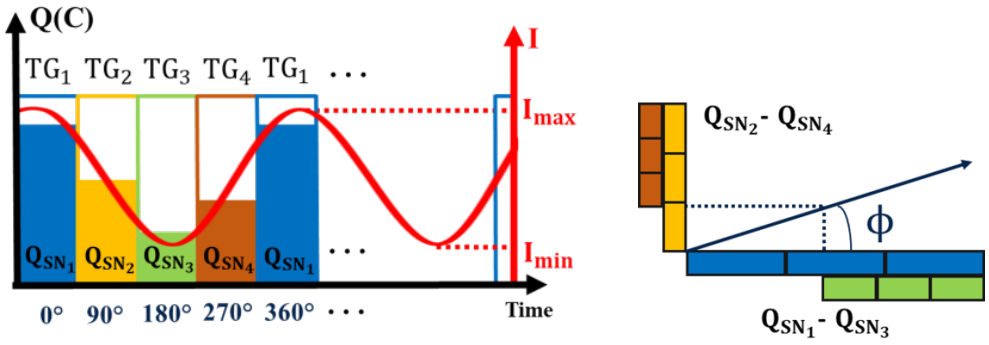
Figure 1.6: Indirect time-of-flight scheme with two sensing nodes (SN_1 and SN_2) operating with a global shutter exposure. The switches S_{C_1} and S_{C_2} are alternatively activated during the demodulation and are simultaneously deactivated during the readout. While the global shutter switch S_{GS} is activated.

The treatment consists of computing the phase value of the recieved signal. The light signal reflected by the object and received at the sensor photogenerates charges in each pixel. In turn, charges are sampled to different sensing nodes (SN) and are stored in different collection sites. The number of samples per period of the modulated light signal is the number of taps. For a 4-tap per period operation, the phase value can be extracted as the operation depicted in Fig 1.7a [13, 29]. Sampling happens at the frequency $N_{tap} \cdot f_{Mod}$ where N_{tap} is the number of taps and f_{Mod} the light modulation frequency. The role of the switches inside of the pixel is taken by the transfer gates (TG). When activating TG, TG_1 to TG_4 at each demodulation cycle, respective charge values, Q_{SN_1} to Q_{SN_4} are measured. Then, the phase value is computed as shown in Fig 1.7b and with equation (1.6).

$$\Delta\phi = arctan(\frac{Q_{SN_4} - Q_{SN_2}}{Q_{SN_3} - Q_{SN_1}}) \tag{1.6}$$

To avoid under sampling, Shannon-Nyquist's theorem must be respected. For that, various techniques can be used. (α) The sampling frequency can be set higher than the laser modulation frequency to validate the strict conditional $f_{sampling} > 2f_{Mod}$. (β) The pixel can operate with multiple taps. The relation with N_{tap} taps and the same number of sensing nodes is shown in equation (1.7) [13].

$$\phi = -arctan(\frac{\sum_{n=1}^{N_{tap}} Q_{SN_n} sin(2\pi \frac{n}{N_{tap}})}{\sum_{n=1}^{N_{tap}} Q_{SN_n} cos(2\pi \frac{n}{N_{tap}})}) \tag{1.7}$$



(a) (b)

Figure 1.7: 4-tap (a) demodulation schematic and (b) phase computation schematic.

(γ) Another alternative is to shift the demodulation phase for successive acquisitions or frames. In practice, iToF pixels operate more often with 2-tap or 1-tap cycles [13, 18]. When this operation is accumulated between successive frames, it is possible to overcome the sampling limitations of a single simpler pixel with fewer sensing nodes [30, 31]. Yorikado et al. [30] compare a 2-tap pixel operation using two and four frames. Fig. 1.8 shows a schematic for the phase shift between frames. By

superposing images with different phase shift, it is possible to construct a multiple tap phase value as in equation (1.7) only operating in 2-tap mode.

(δ) A final solution is to couple neighbor pixels for the reconstruction of the same phase value at the same time [32]. The *binning* technique used in 2D image sensors consists in combining the signal of multiple pixels into one, aiming to increase the sensor sensitivity. For iToF pixels, *binning* may be used. However, a more complex combination of the neightboor pixels is also possible. The demodulation signal of neighbor pixels can be phase shifted to coordinate the acquisition with different pixels. The shift in the operation of each pixel may allow for example, to compute a single distance value from a 1-tap operation by using four pixel. If each pixel has a single TG and sensing node, the TG may be operated with differently shifted signal by a fourth of the period of the demodulation signals. In that case, multiple pixels operate artificially as one with fewer taps to give a more precise depth measurement. Nevertheless, the effective resolution is reduced [13, 31].

Often a combination of these techniques is used to obtain a precise distance measurement. However, electronics for the detection in each sensing node inside a pixel require space. More often, to obtain a smaller pixel, fewer sensing nodes are designed per pixel and image reconstruction techniques coupling neighbor pixels are implemented.

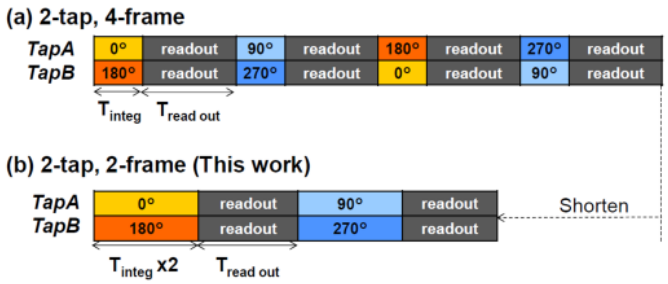


Figure 1.8: Yorikado et al. [30] 2-tap operation over multiple frames with different phase shifts. The conventional four frames operation is compared to the proposed two frames operation. T_{integ} is the integration period and $T_{read\ out}$ is the readout period.

Pulsed light iToF

An similar technique to continuous wave modulated iToF is pulse light iToF, also called pToF. It consists of measuring the phase shift between an emitted periodic pulse wave and the one reflected by the object. The advantage of pToF compared to iToF is the simplicity of the light source used. Continuous wave modulation iToF requires a light wave modulator, complexifying significantly the device. Nevertheless, the precision of the latter remains higher and it is more reliable for applications requiring exposure to ambient illumination [13]. For instance, it is the case of facial and spatial recognition. This is due to the amount of light signal of an impulse that can be very small. The number of emitted photons will depend on the intensity and the width of the emitted light pulse. For a short impulse width required for the

implementation of the pToF technique and for intensity values in accordance with eye safety regulations, the sensor will often be impacted by background noise [13].

For noise suppression, a 3-tap configuration with three different collection sites is envisaged. The phase value can be estimated as in equation (1.8) [33]. Fig. 1.9 gives an example of time diagram for pToF operation. By increasing sampling frequency relative to light modulation frequency, it is possible to reconstruct the phase shift value $\Delta\phi$ from measured charge values Q_1, Q_2 and the background charge Q_b, i.e. the signal collected in the third collection site.

$$\phi = arctan(\frac{Q_2 - Q_b}{Q_1 - Q_b}) \tag{1.8}$$

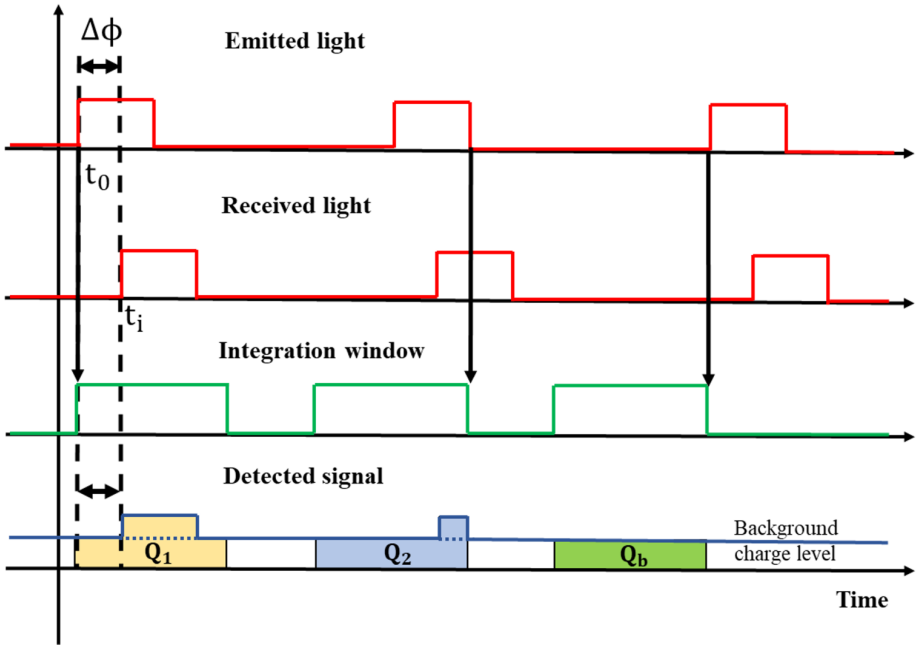


Figure 1.9: Pulsed light indirect time-of-flight scheme.

1.3 Time-of-flight pixels

1.3.1 Near infra-red light detection

Photodiodes are commonly used to absorb light, but they require a material with a suitable band gap. When an incident light wave has enough energy to ionize an electron/hole pair, light absorption occurs. The energy required for this process is determined by the band gap of the material, which is the difference between the conduction and valence band energies (Fig. 1.10). The energy of the photon can be calculated using equation (1.9), where E_{ph} is the energy of a photon in electron volts (eV), h is Planck's constant and ν is the frequency of the incident wave, given by $\frac{c}{\lambda}$, where c is the speed of light and λ is the wavelength.

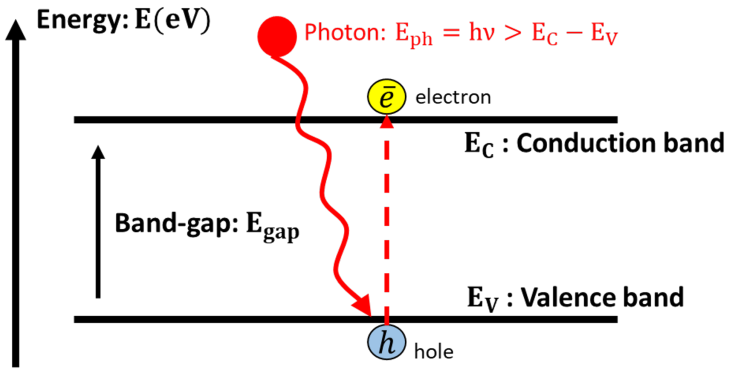


Figure 1.10: Absorption of a photon of energy E_{ph} higher than the band gap energy E_{gap} and photogeneration of an electron hole pair.

$$E_{ph}(eV) = h\nu = \frac{hc}{\lambda} \tag{1.9}$$

In addition to the band gap, the nature of the gap is also important. Two different types of gaps are distinguished for various band structures: direct and indirect gaps. The nature of the band structure is intrinsically linked to the dual nature of electrons, which display both wave-like and particle-like behaviors [34]. For the absorption of a photon to occur, there must be conservation of the energy value E and of the wave vector k. In some materials, such as silicon or germanium, the local maximum of the valence band and the local minimum of the conduction band do not occur at the same value of k in the band diagram. This results in a mismatch of the wave vector k, which can be compensated by a phonon, which is a quantum of lattice vibration. This process is known as phonon-assisted indirect absorption and is crucial for the operation of many semiconductor devices, including photodiodes [34]. The phonon-assisted absorption in an indirect band gap material is illustrated in Fig. 1.11.

Silicon has an indirect band gap of $1.12eV$, which makes it transparent to wavelengths above $1100nm$. However, it is still extensively used for detecting near-infrared light with wavelengths up to $940nm$ [15–18]. Germanium, on the other hand, has a

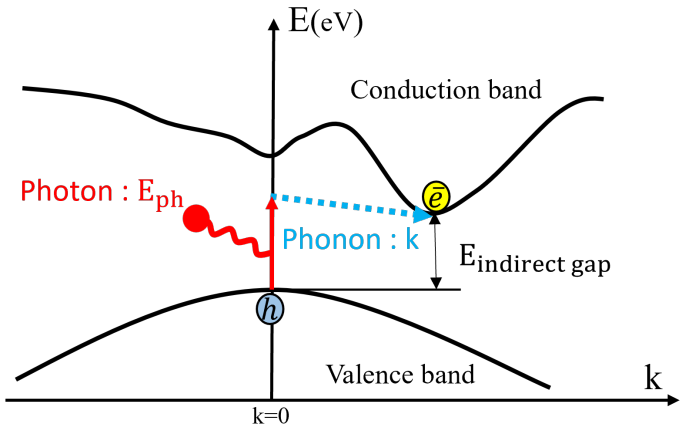


Figure 1.11: Schematic representation of the absorption of a photon of energy E_{ph} higher than the band gap energy $E_{indirect\,gap}$ in an indirect band-gap material. The energy value E is given by the abscissa axis and the wave value k is given by the ordinate axis. The absorption of the photon requires the absorption or the emission of a phonon to compensate for the mismatch in the k value between the conduction and the valance bands.

smaller indirect band gap of $0.66eV$ and a direct band gap of $0.8eV$ [35]. These smaller band gaps allow germanium to detect larger wavelengths, but it is also more susceptible to high ionization rates. This means that the minimum energy required to generate a pair of free carriers in germanium is significantly low. A high ionization rate can lead to the generation of parasitic charges, which can impact the noise and reduce the sensitivity of germanium photodetectors. Hence, the choice of material for a photodetector depends on the specific application and the desired trade-off between sensitivity and noise.

To increase the NIR light sensitivity of silicon sensors, thick layers are fabricated. The absorption of light inside a material is given by Beer-Lambert's law in equation (1.10), where P_{abs} is the absorbed light power, P_{inc} is the incident light power, α is the absorption coefficient in the material and l is the propagation length.

$$P_{abs} = P_{inc} \cdot e^{-\alpha l} \tag{1.10}$$

Besides the absorption length, the concentrations of electrons (n) or holes (p) in the sensitive volume is also important. If absorption occurs in a zone with a high p value, the probability of recombination of a photogenerated electron with available holes is higher than in a zone deserted of holes.

To maintain equilibrium, excess photogenerated minority carriers tend to recombine with majority available carriers in a doped substrate [36].

1.3.2 Photodiode for infrared sensing

PN junction

The photodiode is a device that is commonly used to collect photogenerated free charges. 1D TCAD simulations were carried out to illustrate a PN junction photodiode with the anode doped with P-type species and the cathode with N-type species. The simulated structure is shown in Fig. 1.12 and the differently doped zones are identified by the different background colors and the net active concentration, i.e. the total donor ions concentration N_D minus the total acceptor ions concentration N_A. The free carriers diffuse to locations where they are less concentrated inside of the junction at the interface between both zones to attain an equilibrium. This causes a desertion of free carriers at the interface between both zones.

In the depletion region, the concentration of free charge carriers is very low, and the electric field dominates, causing the electrons and holes to move towards the opposite sides of the junction. This creates a region depleted of free carriers, which acts as a barrier to the flow of current and causes a voltage drop across the junction. The length of the deserted region at the interface between the P-type and N-type zones for the simulated values of N_D and N_A is identified at Fig. 1.12 by $W_{D_{bi}}$.

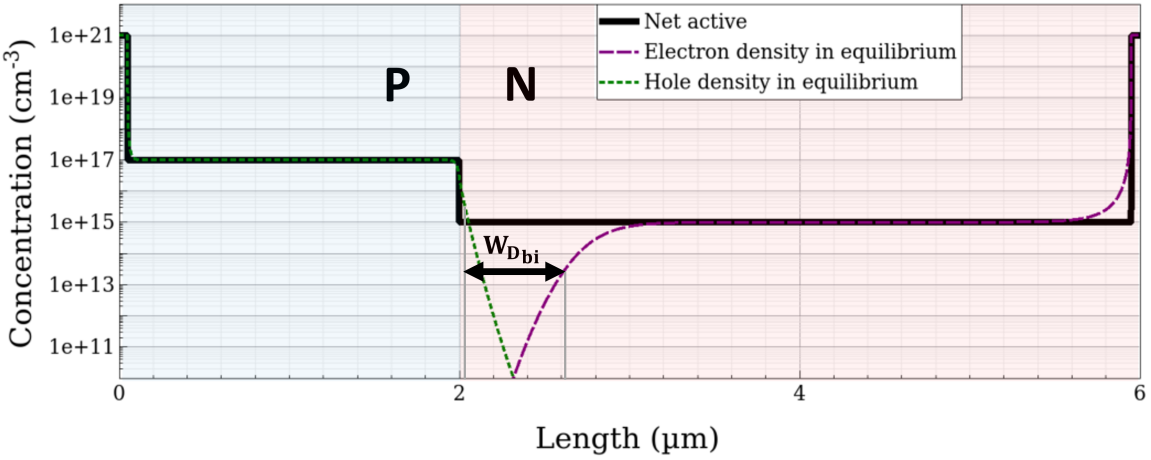


Figure 1.12: Thick PN junction electron and hole densities in equilibrium. The threshold concentration of free carriers corresponding to the depleted region is defined as 5% of the original doping concentration [37].

The photodiode previously simulated in equilibrium is also simulated in zero bias and with a reverse 5V biasing, meaning the anode is biased at the ground voltage and the cathode at 5V. The depletion region created by the interface of the different doping zones is extended, as shown in Fig. 1.13. The energy built in barrier can be observed with a simulated band diagram in Fig. 1.14 for the zero bias case. The drift field in the photodiode is responsible for the transport of photogenerated electrons and holes, which move towards the cathode and the anode, respectively, under the influence of the electric field. The photogenerated electrons and holes movement creates a photocurrent in the photodiode.

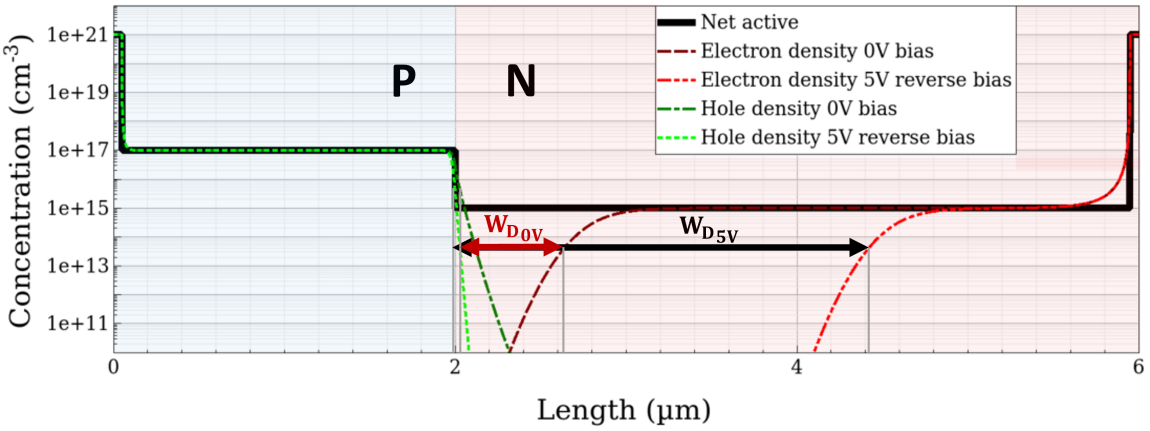


Figure 1.13: Thick PN junction electron and hole densities at $0V$ biasing and at $5V$ reverse biasing.

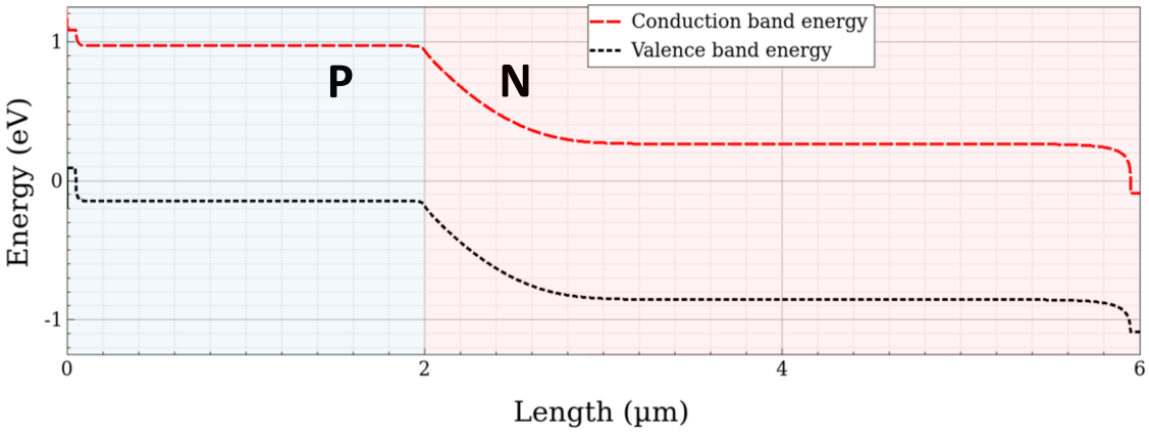


Figure 1.14: Thick PN junction $0V$ biasing.

A stronger reverse bias increases the depletion width $W_{D_{5V}}$ compared to $W_{D_{0V}}$ (Fig. 1.13). Equation (1.11) [34] describes the depletion width for a reverse biased PN junction.

$$W = \sqrt{\frac{2 \cdot \epsilon_0 \cdot \epsilon_r \cdot (N_A + N_D) \cdot (V_{bi} - U)}{q \cdot N_A \cdot N_D}} \tag{1.11}$$

N_A and N_D are respectively the doping concentrations of the acceptor (N-type) and the donor (P-type) atoms, ϵ_0 is the vacuum permittivity, ϵ_r is the relative permittivity of the semiconductor material, i.e. in the simulated case silicon, q is the elementary charge value, U is the reverse biasing or the difference between cathode and anode biasing and V_{bi} is the built in potential.

For a biasing U corresponding to a lower potential on the cathode compared to the anode, the PN junction changes its regime and becomes conducting. For a forward

bias with, e.g. the cathode biased at −1V, the direct current increases exponentially [34]. Fig. 1.15 shows the voltage drop in the photodiode length for different cathode biasing. For a strong reverse biasing on the cathode compared to the anode, the difference of potential observed in the depleted region increases. This increase in the difference of potential may reduce the transit time of free carriers inside of the photodiode.

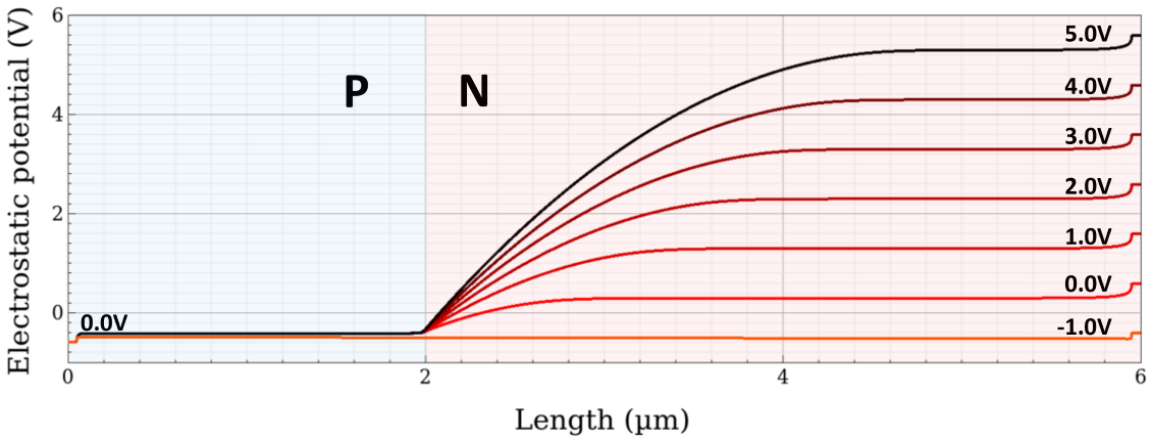


Figure 1.15: Long PN junction potential distribution for different biasing of the cathode (N) relative to the anode (P).

In equilibrium, when there is no carrier injection, the electron quasi-Fermi energy level E_{F_n} and hole quasi-Fermi energy level E_{F_p} are equal to the Fermi energy level E_F (equation (1.12)). However, with carrier injection, E_{F_n} and E_{F_p} are split. The new quasi-Fermi energy values take into consideration the excess carrier concentrations Δn and Δp (equation (1.13) for the electrons). The electrostatic potential for electrons is given by V_n. In turn, the computation of quasi-Fermi levels will allow the computation of a current value J for a point vector, $\vec{r}$ and mobility values, μ_n and μ_p respectively for electrons and holes as in the drift current equation (1.14) and by solving the continuity equation [34]. The gradient of the quasi-Fermi energy of electrons in equation (1.14) will force the free negative charge in the direction of the gradient.

In TCAD electrical simulation, the electrostatic potential is computed from the intrinsic energy level E_i (equation (1.15)) [37]. When computing the Poisson equation in TCAD, the external bias V will force the quasi-Fermi energy level to its value at the contact, which will remain an image of the intrinsic energy level E_i. Hence, the potential V in equation (1.15) will fix the energy levels E_{F_n} and E_{F_p} in equation (1.13) that in turn will be the reference for electrons and holes transport computation.

$$E_F = E_{F_n} = E_{F_p} \tag{1.12}$$

$$qV_n = E_{F_n} + qV = kTln(\frac{n}{n_i}) \tag{1.13}$$

$$\vec{J}(\vec{r}) = \mu_n n\vec{\nabla} \cdot E_{F_n} + \mu_p p\vec{\nabla} \cdot E_{F_p} \tag{1.14}$$

$$E_i = -qV \tag{1.15}$$

Pinned photodiode

To acquire an accurate image, a high signal-to-noise ratio is necessary. Pinned photodiodes are a type of photodiode that provides several advantages over traditional photodiodes [38]. A simple schematic of a pinned photodiode is identified in Fig. 1.16a with the equivalent circuit depicted by the three elements of Fig. 1.16b : (i) the photodiode, (ii) the transistor and (iii) capacitor [38].

(i) The pinned photodiode is constructed by doing a deep N-type implanted zone at the center of the pixel, followed by a P+ implantation on the surface over the first implant. The P+ implant is the pinning implant, that when biased with a low biasing will extend a depletion region inside the N doped implanted volume.

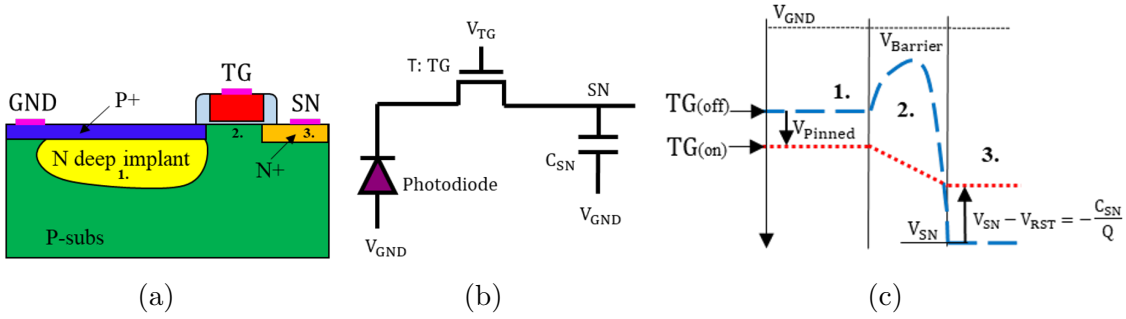
(ii) The transfer gate is responsible for the transfer of charges in the N doped volume. I.e. for the collection of photogenerated signal, but also for the depletion of the pinned region during a reset of the pixel.

(iii) The sensing node (SN) is where charges are collected when the TG is activated. It has a storage capacitance C_{SN} that is reset at a high potential V_{RST} and left floating for the collection of charges photogenerated in the pinned photodiode.

As shown in the schematic in figure 1.16c, (1.), the pinned potential, in the N-type deep implanted region, is attained by activating the TG. The on state (TG_{on}) is represented by the red doted line. For the measurement of the optical signal, the TG is mantained in the off state (TG_{off}) represented by the dashed blue line. The photogenerated charges are firstly directed to the depleted implanted photodiode. The maximum potential V_{PD} inside of the N deep implant region, is equal the pinned potential V_{pinned}, when the N doped region is fully depleted of electrons. V_{pinned} decreases with the increase of the electron concentration in the volume according to equation (1.16). C_{PD} is the pinned photodiode capacitance and Q_{PD} is the total charges inside of the pinned photodiode. The photogenerated holes are evacuated at the reference ground node GND biased at V_{GND}. (2.) The strong low $V_{Barrier}$ potential, in the P-doped region, between the SN and the photodiode when the TG is on the off state, impedes the transfer of charges to the floating SN. At a second moment the transfer gate is activated (TG_{on}) and the photogenerated electrons are transfered to the SN. (3.) The potential of the sensing node V_{SN} decreases as the total collected charges (Q) increases [39].

$$V_{PD} = V_{pinned} - \frac{Q_{PD}}{C_{PD}} \tag{1.16}$$

One of the primary benefits of pinned photodiodes is their ability to reduce dark current [40, 41], which is the current that flows through a biased photodiode even when no light is present. This is particularly useful for applications where low light levels must be detected.



(a) (b) (c)

Figure 1.16: Schematic of (a) pinned photodiode pixel and (b) pixel circuit. (c) The electric potential of the two operating modes are identified depending on the activation of the TG (i.e. TG(on) and TG(off)) [38]. During TG_{off}, the charges stored in the sensing node capacitor C_{SN} are transferred to the readout circuit, and the sensing node is reset to the V_{RST} potential.

1.3.3 Indirect time-of-flight pixels

There are two main alternatives when developing an indirect time-of-flight (iToF) pixel. The first alternative is the current assisted photonic demodulator (CAPD) [16, 42–44]. The CAPD solution has been demonstrated both in silicon [16] and germanium [44]. A back-side illumination silicon integration of the CAPD with $5\mu m$ pixels is currently commercially available [45]. The second alternative is the pinned photodiode (PPD) iToF pixel. It consists of a PPD pixel with multiple TGs and as many SNs. Both alternatives will be shortly described in this section.

The CAPD iToF pixel

The CAPD pixel is shown in Fig. 1.17 and it is composed of four electrodes. Two of them are doped N+ to create the sensing nodes and two are doped P+ to create the demodulators. The demodulators are responsible for orienting the charges photogenerated by the NIR light signal continuously modulated in intensity to the sensing node, where they are collected. A difference of potential is applied between the P+ demodulators electrodes (D_1 and D_2) situated on each side of lightly P-type doped substrate, this creates an electric field between the demodulators. The sensing nodes are biased at an electric potential higher than the demodulators and are left floating during demodulation. When illuminated by a photon with a given wavelength, an electron hole pair is generated inside the pixel substrate. The electric field ($\vec{\mathscr{E}}$) inside the pixel causes the hole to drift in the direction of the hole current ($\vec{J}_h$) and is collected by the P+ demodulator electrode polarized by the lower biasing D_2. The electron is oriented in the opposite direction of the electric field and is collected at the opposite N+ electrode, i.e. SN_1.

A germanium on silicon (Ge-on-Si) alternative integration has been envisaged and demonstrated [44]. The silicon circuit required for the interface of the detected photogenerated signal and the readout circuit may be deported to the front side.

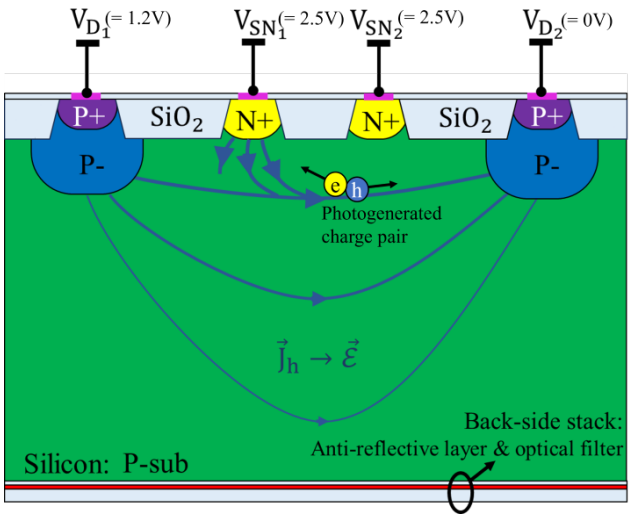


Figure 1.17: State-of-the-art current assisted photonic demodulator (CAPD) pixel schematics. The pixel has two demodulators (D_1 and D_2) and two sensing nodes (SN_1 and SN_2). The substrate is lightly doped with a P-type doping, i.e. P-subs. The different implants (N+, P+ and P-) are depicted for the case where the sensing nodes collect the electrons and the demodulators the holes. The back-side stack is depicted with different unspecified layers consisting of the anti-reflective layer and the optical filter. Shallow trench insulation done with silicon oxide (SiO_2) is integrated between the sensing nodes and the demodulators for isolation purposes. The electrical field ($\vec{\mathscr{E}}$) lines follow the hole current ($\vec{J}_h$) orientation caused by the difference of potential between the demodulator and represented by the blue arrow lines.

While the pixels are integrated with back-side illumination germanium integration, the front-side integrates the pixel circuits.

The PPD iToF pixel

A PPD iToF pixel can be understood with the schematics in Fig. 1.18a and Fig. 1.18b. Two separated photodiodes with respective sensing nodes SN_1 and SN_2 are illustrated. The differently doped zones are depicted in Fig. 1.18a. A substrate doped with a low P-type concentration in green referenced at a ground biasing GND through a $P+$ implanted zone. A N-type zone in yellow is created at the center of the device through ion implantation, a $N+$ implanted zone is created for the drain and an oxide-polysilicon gate is deposited. The transfer gates TG_1 and TG_2 are intended to modulate the barrier between the deep implanted N-type zone and the $N+$ drain. Fig. 1.18(a) illustrates the case where the TG is activated by biasing it with a high electric potential and electrons are collected in SN_1. In contrast, Fig. 1.18b illustrates the case where the TG is deactivated by biasing it with a low electric potential. An electrostatic potential barrier is created between the SN_2 drain and the N-type doped yellow zone. Electrons are stoped by the potential barrier created by TG_2.

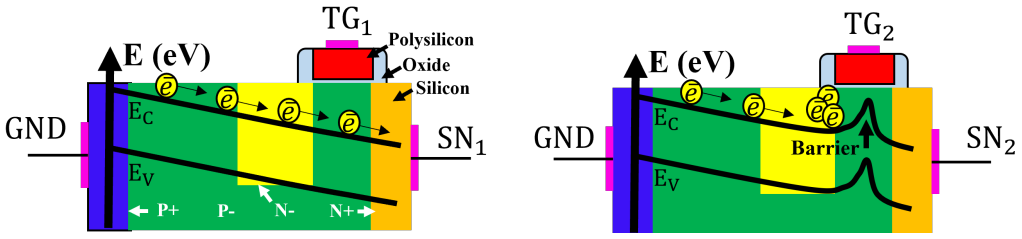
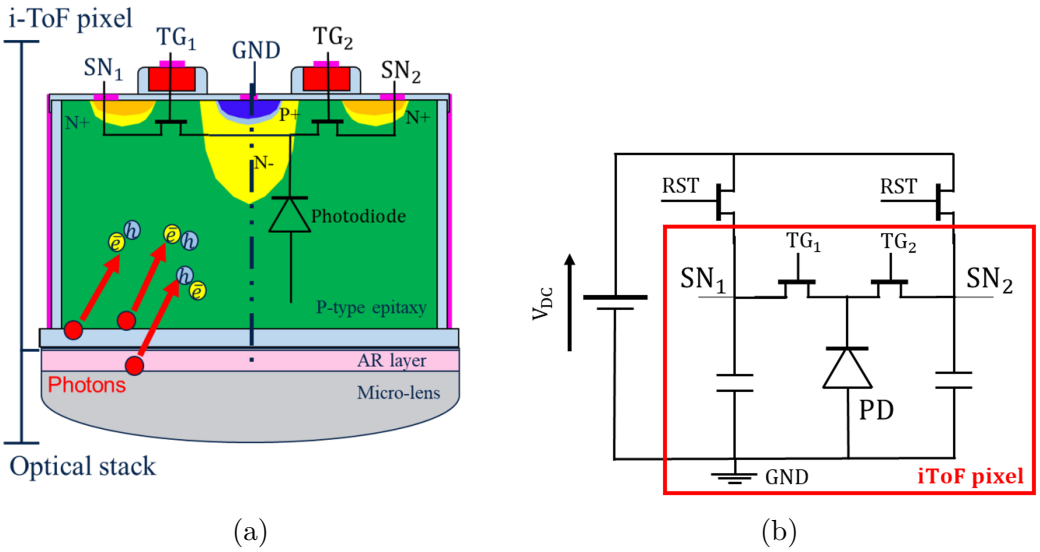


Figure 1.18: A pinned photodiode with a TG to (a) allow the transfer of electrons to the sensing node when activated (i.e. TG is biased with a high electric potential) or (b) block electrons path with a potential barrier when deactivated (i.e. TG is biased with a low electric potential). The moving electrons ($\overline{e}$) are illustrated in the conduction band (E_C). The valence band (E_V) is also identified.

In a standard state-of-the-art iToF, these two operations happen simultaneously as illustrated in Fig. 1.19a. The deep implanted photodiode created by the deep N-implant in the center of the pixel is shared between TG_1 and TG_2.

An equivalent circuit for the iToF pixel can be understood as the one in Fig. 1.19b. In addition, sensing nodes are connected to a treatment circuit. The iToF pixel and the iToF circuit together form the pixel architecture. Often, an iToF pixel has a global shutter five transistors (5T) architecture per sensing node and an additional transistor for pixel selection [13].

However, it can be simplified for cost reduction purposes in the case of lower cost devices [16] or complexified to add functionalities [18, 46]. In addition to these components, the iToF pixel can also include other elements such as antiblooming, dedicated reset transistors, and deep trench isolations. It is worth noting that deep trench isolations can be biased electrically or they can have an integrated layer with a high concentration of fixed charges for the same effect [47], allowing them to operate both electrically and optically.

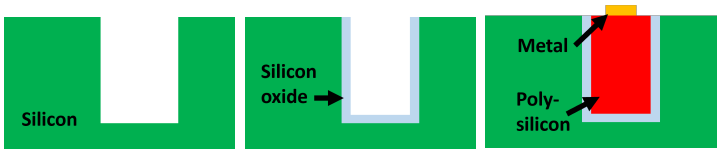


(a) (b)

Figure 1.19: (a) iToF pixel and (b) equivalent electronic circuit [13, 18].

1.3.4 2D imaging vertical gate pixel

In the latest visible light 2D imaging technology, the previously used planar gates have been replaced by trench vertical gates (TVG). These TVG are operated as MOS capacitors that can modulate the potential at the volume of the pixel. The TVG used as transfer gates allows an efficient charge transfer in the pixel collection volume. For a low DC biasing, closed TVG allow the storage of a significant number of charges in the volume of the pixel while having a low dark current [48]. A simplified flow for the TVG is depicted in Fig. 1.20, i.e. the trench etching, followed by the liner deposition, the polysilicon filling and the metallic contact deposition.



(a) (b) (c)

Figure 1.20: The TVG simplified process flow: (a) trench etching in the silicon, (b) silicon oxide liner deposition and (c) polysilicon trench filling followed by the metal contact deposition.

A schematic of a pixel using the TVG is depicted in Fig. 1.21 [48]. Additionally, it has three implants (N+, P+ and P-Well) and the capacitive deep trench isolation (CDTI), for electrical and optical isolation. Furthermore, the deep photodiode implants used in a PPD pixel are no longer required. They are entirely replaced by the TVG and CDTI that are capable of entirely depleting the volume of the pixel creating a favorable potential distribution in the volume of the photogate [48].

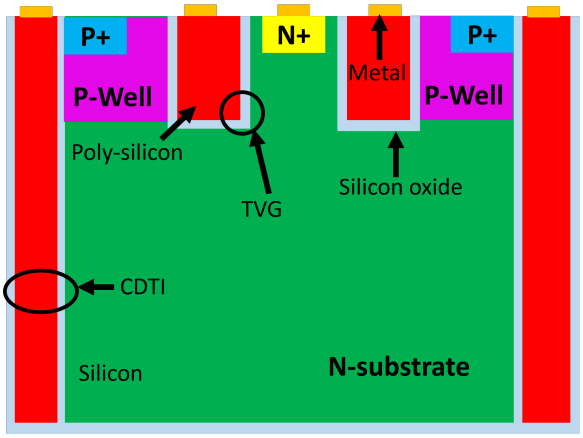


Figure 1.21: A schematic of the photogate pixel using the TVG as TG. Additionaly, it has three implants (N+, P+ and P-Well) and capacitive deep trench isolation (CDTI), for electrical and optical pixel isolation.

TVG has been identified as a key element for pixel shrinking and the state-of-the-art of 2D imaging color pixels integrates this technology [49]. The key figure of merit of a 2D pixel is the fullwell capacity. That is the maximum charges a pixel can collect per acquisition. The challenge in developing a competitive visible 2D image sensor is to maintain a high fullwell capacity while reducing the pitch, aiming to increase the resolution. The state-of-the-art of visible light pixels integrating the TVG as TG are pixels of pitch as small as $0.56\mu m$, in a matrix of 200Mpix (ie. 200,000,000 pixel or 200 mega pixels). For these pixels, the attained performances are synthesized in Table 1.2, they are a fullwell capacity close to 10,000 electrons and a low dark current value of less than $1\overline{e}/s$ (i.e. one unity of electron $\overline{e}/s$ or hole per second h/s) [48, 50–52]. It must be mentioned that to attain such small pixels, the 3D stacking is indispensable.

Table 1.2: State-of-the-art 2D imaging color pixel

	TVG 2D image sensors			
	Choi [50] (2023)	***Yun [51] (2022)***	***Park [52] (2022)***	***Roy [48] (2020)***
Pixel pitch (μm)	0.56	0.6	0.56	2.0
Pixel array	200Mpix	200Mpix	64Mpix	0.1Mpix
Fullwell capacity ($\overline{e}$ or h)	4,700	10,000	6,000	13,000
Dark current ($\overline{e}/s$ or h/s)	—	0.8	0.75	5.3

1.4 Indirect time-of-flight sensor architecture

In the previous section 1.3.3, the different pixel structures for the iToF operation have been described. In this section, a broader overview will be given for the sensor into which this pixel is integrated. Combined with each pixel structure, there is a circuit for the readout of the detected signal at each pixel. These two conjoined elements are called the pixel architecture. This unified element, called the pixel architecture, is integrated into a matrix of pixels. The pixel matrix is then incorporated with other elements that are required for the operation of the pixels and this combination composes the sensor. The different building blocks that compose the iToF sensor are referred to as the sensor architecture.

1.4.1 iToF image sensor on chip

A block diagram of the iToF sensor on chip architecture is depicted in Fig. 1.22. This section will detail the main building blocks of the sensor as well as the architecture of the circuit of a pixel [13, 18, 53].

1. **The pixel matrix:** It is responsible for capturing the light that enters the sensor and converting it into an electrical signal. This matrix is made up of a large number of individual pixels, each of which can detect the distance to a specific point in the scene.

2. **The alternate phase driver:** For an iToF pixel operating with 4-taps, i.e. four measured samples per light signal modulation period, drivers will generate the command signal for each transfer gates operating with phase shifts of 0, $\frac{\pi}{2}$, π and $\frac{3\pi}{2}$.

3. **The phase locked loop:** The phase locked loop (PLL) is responsible for synchronizing the modulated light signal with the internal clock of the sensor and the driver demodulation signal. This ensures that the sensor is able to synchronously reconstruct the phase difference between the emitted light signal and the received light signal.

4. **The analog to digital converters:** The analog to digital converters (ADC) are used to convert the analog electrical signal generated by the pixel matrix into a digital signal that can be processed by the image signal processor.

5. **The image signal processor:** This processor is responsible for processing the digital signals generated by the analog to digital converters and producing an output. The output is not the final image and it will be interfaced to another processor that will have the suitable software to process the measured data.

There are two approaches to measure the photogenerated signal, they are: (1) to measure directly a charge value, i.e. a charge domain pixel or (2) to first convert the charge signal into a voltage measured signal, that is a voltage domain pixel.

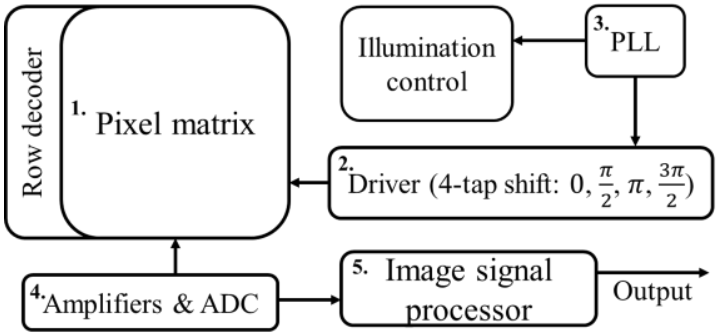


Figure 1.22: Indirect time-of-flight sensor architecture comprising: [1.] the pixel matrix, [2.] the alternate phase driver, [3.] the phase locked loop (PLL) responsible for generating the demodulation signal, [4.] the analog to digital converters (ADC) and [5.] the image signal processor that gives the output of the sensor [13, 18, 53].

This subsection discussed the architecture of the iToF sensor on a chip and its main building blocks. The following subsection will focus on the pixel architecture, i.e. how photogenerated charges are measured in the pixel level and the corresponding circuit.

1.4.2 Charge and voltage domain pixel architecture

A charge domain pixel measures the photogenerated signal directly in the form of a charge signal. The charges are transferred to memories inside the pixel and during the readout they are converted into a voltage signal [18, 54]. The charge domain pixels have two main issues:

(i) The memories integrated directly on the pixel level constrains the miniaturization of the pixel. It imposes pixel reduction design constraints and reduces the effective pitch of the pixel. I.e. the total surface of the pixel exposed to incident light, also called the fill factor [55].

(ii) Charge domain pixels suffer from parasitic light reaching storage memories, this reduces the efficiency of light photogeneration and collection [55, 56].

An alternative to these issues is the voltage domain pixel. Differently than the charge domain alternative, in voltage domain, the photogenerated signal is collected directly as a voltage signal. Floating diffusions or high density capacitors are used. They are engineered to have a suitable conversion factor, to convert and store charges as a voltage value [23, 55, 56]. The floating diffusion storage capacitance will correspond to the sensing node capacitance that will be left floating and change with the charge collection. On the other hand, the high density capacitor consists in additional capacitors connected to the sensing nodes. They are much larger in size allowing for a high charge storage capacity.

However, integrating the high density capacitors to the pixel architecture can cause a significant fill factor reduction, impacting the pixel optical performances. Because of that, the added high density capacitors require 3D sequential stacking to be competitive when compared to the more elementary floating diffusion alternative.

1.4.3 Rolling and global shutter pixel architecture

The rolling and global shutter pixels have been described and compared earlier in subsection 1.2.1. This section intends to illustrate the corresponding pixel circuits composing the rolling and global shutter pixel architecture.

Fig. 1.23 is an example of a four transistor (4T) rolling shutter pixel architecture operating in voltage domain [21, 22]. A transistor is used as a transfer gate (TG) that separates the photodiode from the sensing node (SN). This node is often a floating diffusion that can be connected to a high density capacitor [55]. The node can be reset by activating the reset transistor (RST) whose drain is connected to the circuit DC reference voltage source V_{ref}. The output impedance of the SN is adjusted by integrating a supplementary transistor as a source follower (SF). The voltage at the SN is replicated by the SF to the output node (OUT). The replicated voltage can be readout by activating the readout transistor (READ). A supplementary transistor can be added to the circuit to reset the photodiode [22, 57]. This can avoid the leakage of charges in the pixel in case the sensing node is saturated, i.e. when the sensing node has reached the maximum capacity for total stored charges.

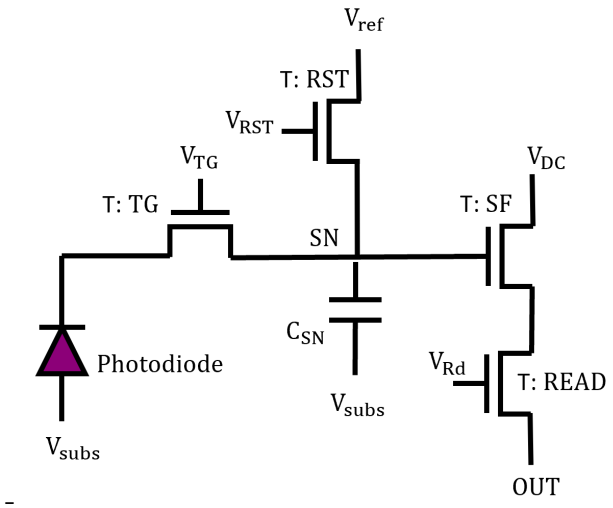


Figure 1.23: Four transistor (4T) rolling shutter pixel architecture.

A global shutter can be designed from the circuit previously depicted in Fig. 1.23, by adding a transistor that will work as a shutter between the SN and the capacitor node (C_{SN}). The obtained circuit is depicted in Fig. 1.24 with an added transistor as a source follower, to adapt the impedance of the SN and correctly replicate the voltage value at SN to the CN. The shutter allows the pixel to simultaneously acquire the photogenerated charges in SN at the current picture frame, while the charges stored in C_{SN} from the previous frame are readout.

The readout of the voltage signal stored in CN is done with a rolling readout that resembles a rolling shutter operation. Furthermore, there are circuit designs where the pixel could operate both in rolling shutter and global shutter modes [23]. This can allow either an operation at a higher speed using the rolling shutter mode or with

a lower consumption using the global shutter mode. However, having this hybrid operation mode will require a larger circuit and consequently it will be a limitation for pixel pitch reduction.

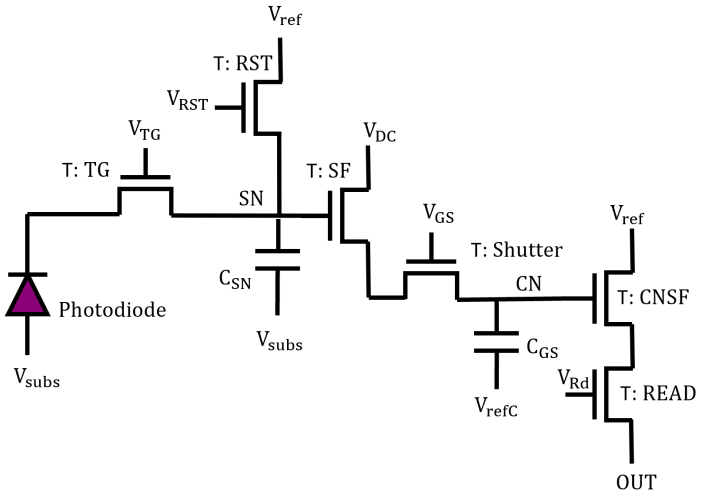


Figure 1.24: Six transistor (6T) global shutter pixel architecture.

1.4.4 Indirect time-of-flight pixel architecture

One of the main challenges of iToF is the motion aberrations, which can cause distortions in the image [13]. To address this issue, synchronization of acquisitions is required, and a global shutter pixel is necessary to capture the image accurately.

Further more, the equivalent global shutter circuit is required for each sensing node. For example, a 2-tap pixel means a circuit that is twice the size of the global shutter circuit. The corresponding design is depicted for one sensing node in Fig. 1.25 [13, 18, 58]. Compared to the elements previously depicted in the global shutter circuit Fig. 1.24, the presented iToF circuit has an additional transistor for binning (BIN) and two additional transistors for memory selection (S_1 and S_2).

When the binning option is selected, multiple pixels operate simultaneously and their measured signal is collected in a common storage node (SN_{BIN}). Binning can be used to suppress mismatches between pixels [32]. However, a global shutter is still required to avoid phase computation issues that may arise due to motion at multiple frames. Additionally, it increases the sensor sensitivity while reducing its effective resolution [13, 31, 32].

Similarly, memory capacitors C_{11} and C_{21} can be selected by activating respectively S_1 or S_2 at successive frames to suppress the low frequency thermal noise (i.e. the RMS noise). By doing the mirror acquisition at successive frames, the noise proportional to the capacitance can be reduced [59].

Additionally, in Fig. 1.25, an antiblooming transistor is added (TG_{AB}) to complete the pixel circuit schematic. The antiblooming, as its name indicates, is intended to evacuate the exceeding generated charges before they overflow to the neighbor pixels

or to the read-out circuit. It may also be added to the previously presented pixel circuits. In the iToF pixel architecture, while the signal collected in SN is transferred to CN by activating the shutter transistor, the TGs are deactivated. During that time, to avoid the leakage of the charges generated at the volume of the pixel, the antiblooming transistor (TG_{AB}) is activated and the exceeding signal is evacuated to the antiblooming node (AB) [13].

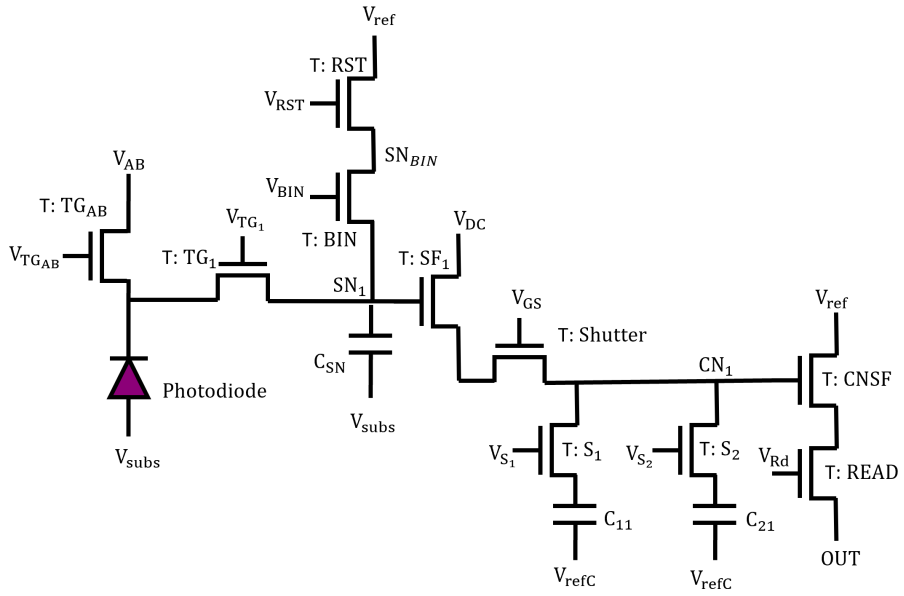


Figure 1.25: Nine transistors (6T+3T) iToF pixel architecture. A six transistors (6T) global shutter pixel architecture is designed for each sensing node. The three additional transistors are: (BIN) a transistor to activate the binning option and (S_1 and S_2) options for access to different storage nodes or capacitors.

1.5 Figures of merit

For the efficient operation of an iToF sensor three main aspects are taken into consideration. They are (*i*) the signal, (*ii*) the noise and (*iii*) the power consumption.

(*i*) For the signal the main elements are the demodulation contrast (DMC), the parasitic light sensitivity (PLS) and the quantum efficiency (QE). (*ii*) The noise signal can be understood as an offset to the continuous modulated sinusoidal signal. (*iii*) The consumption for a 3D image acquisition is largely dependent of demodulation operation consumption.

1.5.1 Demodulation contrast: DMC

Demodulation contrast can be approached in low frequency as a steady state figure of merit, as the demodulation duration in low frequency is much longer than the expected transit time of the photogenerated charges. When time tends to infinity and all charges are supposed collected, the distribution of charges gives the demodulation contrast in DC. It is defined as the difference between the maximum (I_{max}) and the minimum signal intensity (I_{min}), normalized by their sum (equation (1.17) [13]). It can be estimated by computing the difference between the charge signal collected at each sensing nodes (Q_{SN_1} and Q_{SN_2}) for a given biasing condition where one TG is activated and the other TG is deactivated.

$$DMC_{DC} = \frac{I_{max} - I_{min}}{I_{max} + I_{min}} = \frac{Q_{SN_1} - Q_{SN_2}}{Q_{SN_1} + Q_{SN_2}} \tag{1.17}$$

In state-of-the-art applications, iToF pixels operate in frequencies up to 250MHz [18]. During a high frequency operation, the charge transfer speed may not be sufficient to transfer all the photogenerated charges [31]. This imposes a demodulation contrast definition depending on the frequency (equation (1.18)). The remaining charges cause an additional offset to the pixel that will be observed in subsequent demodulation steps.

Often the light signal is continuously modulated in the form of a cosine wave. Due to the nature of cosine signal, by using a single harmonic for detection, only a maximum contrast of $\frac{2}{\pi}$ can be achieved [13]. A coefficient of $\frac{\pi}{2}$ is multiplied to the signal partitioning when using a sinusoidal continuous modulated wave to obtain a DMC value from 0 to 1 [13].

$$DMC(f_{Mod}) = \frac{\pi}{2} \cdot \frac{Q_{SN_1}(1/f_{Mod}) - Q_{SN_2}(1/f_{Mod})}{Q_{SN_1}(1/f_{Mod}) + Q_{SN_2}(1/f_{Mod})} \tag{1.18}$$

Assuming that all charges are collected in SN_1, the intended sensing node, the DMC response can be computed from an impulse stimulus, and it is computed, in the context of this work, with equation (1.19). In simulation, the demodulation contrast can be estimated by computing the current impulse response versus the frequency of the demodulation signal. This is computed by doing the fast-Fourier-transform of the current response ($fft[i_{SN_1}(N_{tap} \cdot t)](f_{Mod})$). The fast-Fourier-transform is computed

with equation (1.20) [60]. The corresponding frequency of operation (f) depends on the number of taps (N_{tap}), and it is accounted for by multiplying the time value (t) by the number of taps ($N_{tap} \cdot t$). N is the total number of points of the simulated current response vector (i_{SN_1}).

$$DMC(f_{Mod}) = Re\left\{\frac{fft[i_{SN_1}(N_{tap} \cdot t)](f_{Mod})}{fft[i_{SN_1}(N_{tap} \cdot t)](0)}\right\} \tag{1.19}$$

$$fft[i_{SN_1}(N_{tap} \cdot t)](f) = \sum_{n=0}^{N-1} i_{SN_1}(N_{tap} \cdot t) \cdot e^{-i \cdot 2 \cdot \pi \cdot f \cdot \frac{n}{N}} \tag{1.20}$$

DMC is intimately bound to the transfer efficiency of photogenerated charges. Differently than the DC operation, where DMC_{DC} is dependent only on how the charge collection is distributed between sensing nodes. In AC and with frequency dependency, it depends on the transit time (TrT).

1.5.2 Parasitic light sensitivity: PLS

The DMC_{DC} depends on the parasitic light sensitivity (PLS), that is the total charges measured in the deactivated electrode also in DC. During demodulation, one transfer gate is active while the other is not, similarly to Fig. 1.7 but here, the particular case of a 2-tap pixel is considered. The PLS is the percentage of signal collected in the sensing node whose gate is not active. Supposing collection is intended in SN_1, then PLS is defined as in equation (1.21).

$$PLS = \frac{Q_{SN_2}}{Q_{SN_1} + Q_{SN_2}} \tag{1.21}$$

Ideally, all photogenerated charges are collected, which means that no charges are lost through recombination mechanisms inside the pixel, as it was shown with equation (1.21). The total charges Q_{Total} is the sum of all charges collected in SN_1 and SN_2, respectively denoted as Q_{SN_1} and Q_{SN_2}. It may be the case that a few charges are lost or that some charges are collected by other electrodes inside of the pixel. In the particular case where all charges are collected by either sensing nodes the PLS is given by equation (1.22).

$$PLS = \frac{Q_{SN_2}}{Q_{Total}} \tag{1.22}$$

1.5.3 Transit time: TrT

TrT is defined as in equation (1.23) and it is the average transfer time of measured charges normalized by the total charges. A pixel with transfer time much smaller than the demodulation period gives a higher DMC close to 1.

$$TrT = \int_0^{+\infty} \frac{t \cdot i(t)}{Q_{Total}} \cdot dt \tag{1.23}$$

The integration of the current expression introduced in equation (1.23) can be decomposed into an expression depending directly on the charge value in time ($q(t)$) in equation (1.24). It depends on the maximum simulation time ($T_{+\infty}$), that is sufficient to the collection of all photogenerated charges and it is normalized by the total charges (Q_{Total}).

$$TrT = \frac{Q_{Total} \cdot T_{+\infty} - \int_0^{T_{+\infty}} q(t)dt}{Q_{Total}} \tag{1.24}$$

1.5.4 Quantum efficiency: QE

Finally, the key sensitivity figure of merit is quantum efficiency. That is the total measured charges over incident photons. It is defined in equation (1.25) as the ratio between the current of photogenerated charges (I_{ph}) and the photon flux through the illuminated pixel Φ_{ph}. This relation is normalized by the elementary charge q in Coulombs so QE is a ratio.

$$QE = \frac{I_{ph}}{q \cdot \Phi_{ph}} \tag{1.25}$$

The charges that are directly photogenerated into sensing node diffusion zones can result in a loss of QE. As only one TG is activated at once, the charges photogenerated directly into the other sensing nodes are promptly collected and contribute to the total parasitic light sensitivity, i.e. the optical PLS. This inefficient distribution of signal can impact the measured signal offset. Additionally, the photogenerated charge signal can be lost through recombination. Especially if they are photogenerated in highly defective zones, such as highly doped zones or near different materials interfaces, the charges may recombine before they are collected.

1.5.5 Power consumption: P_{Mod}

The consumption for a 3D image acquisition is dependent on the power delivered by the high frequency drivers. The consumption scheme can be simplified as in Fig. 1.26. Between S_1 and S_2 states, C_{Gate} is charged and discharged. Supposing an operating frequency f_{Mod} for the operation of the switch between these two states. The total power consumed with demodulation (P_{Mod}) can be estimated as in equation (1.26) [61, 62]. The term I is the average current consumed for charging or discharging the capacitor during the voltage excursion ΔV and U_{ref} is the reference DC voltage source used for the drivers. It can be decomposed in an expression depending on the number of taps (N_{tap}), the demodulation frequency (f_{Mod}), the average capacitor charged and discharged during the voltage excursion ($\widehat{C}_{TG}$), the difference of potential ΔV and the reference DC voltage U_{ref}.

$$P_{Mod} = N_{tap} \cdot I \cdot U_{ref} = N_{tap} \cdot f_{Mod} \cdot \widehat{C}_{TG} \cdot \Delta V \cdot U_{ref} \tag{1.26}$$

The consumed current is given by the charging and discharging of the equivalent capacitance between cycles ($f_{Mod} \cdot \widehat{C}_{TG} \cdot \Delta V$). N_{tap} is the number of taps, i.e. the

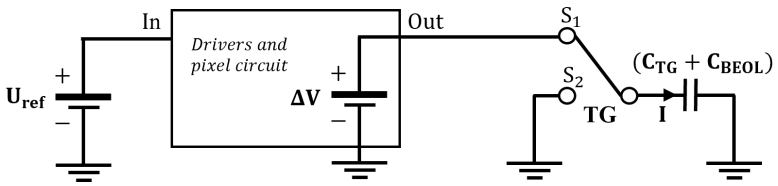


Figure 1.26: Equivalent consumption schematic for a transfer gate consumption capacitance. The schematic box represents the drivers and pixel circuit that take as the input the DC voltage source U_{ref} and deliver as the output the voltage ΔV, proportional to the current I.

number of the capacitance charging and discharging cycles. Reducing the difference of potential ΔV between TGs can contribute to decreasing U_{ref}. If U_{ref} equals to ΔV, the power consumption is reduced to the square of ΔV, while it depends linearly on capacitance value.

Depending on the gate biasing V_{TG}, the equivalent capacitance C_{TG} can be impacted significantly (equation (1.27)). By operating the TGs close to the interval between the flat band voltage, V_{fb} and the threshold voltage, V_T, the inversion layer capacitance C_{inv} is negligible. The gate capacitance C_{ox} is then reduced by the depletion capacitance C_D, thanks to the depletion of the semiconductor surrounding the gate.

$$C_{TG} = \left(\frac{1}{C_D + C_{inv}} + \frac{1}{C_{ox}} \right)^{-1} \tag{1.27}$$

Because of that for a precise estimation of the consumed power, an average capacitance value is estimated in the voltage interval ΔV. It is defined as in equation (1.28).

$$\widehat{C}_{TG} = \frac{\int_{V_{TG_{Off}}}^{V_{TG_{On}}} C_{TG}(V) dV}{\Delta V} \tag{1.28}$$

The external voltage reference U_{ref} and the difference of potential between states ΔV are distinguished in equation (1.26). For a same value between these two quantities (i.e. U_{ref} and ΔV), it is observed that consumption is proportional to the average capacitance and it is proportional to the square of the voltage excursion ΔV.

1.5.6 Fullwell

The fullwell capacity is the total measured charge per pixel during a single sensor acquisition. The fullwell is computed in simulation from the evolution of the minority carriers in the volume of the pixel in time for a complete operation cycle. This computation is done by integrating the electron concentration in the volume of the pixel in time. The detailed methodology will be described in section 2.2.2.

The pixel is illuminated with an uniform optical generation for a fixed duration. In Fig. 1.27 two moments are identified during the pixel operation. (i) During the first moment, after the illumination, the pixel is filled with minority carriers. For

a constant value of the biasing of the SN (V_{SN}), the TG toggles from the off-state ($TG(off)$) with a low biasing to the on-state ($TG(on)$) with a high biasing. The voltage ramp is depicted in Fig. 1.27a. (ii) In a second time, after the readout of charges in the SN, the TG changes again from the state $TG(on)$ to $TG(off)$ as shown in Fig. 1.27c.

The fullwell value is computed from the difference of electrons in the volume after displaced charges stabilize and before the activation of the TG. These values correspond to the ending and starting times of Fig. 1.27d and Fig. 1.27b. The fullwell obtained for this non-optimized pixel is 1600 electrons.

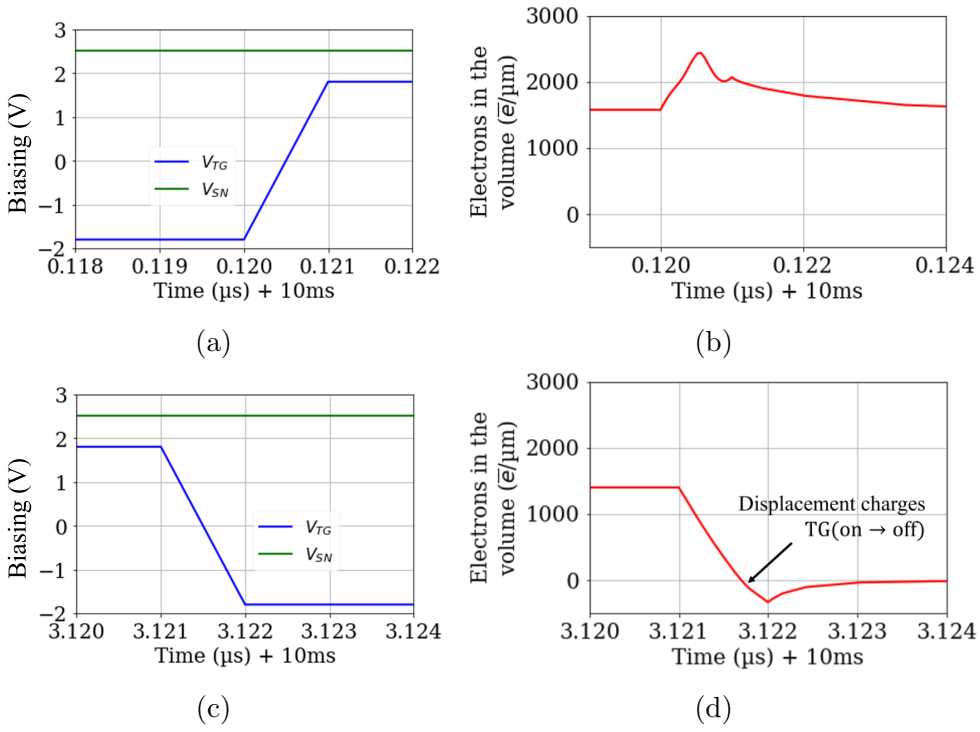


Figure 1.27: (a) Chronograph of the biasing applied to TG and SN during the first simulated toggling of the TG from the TG(off) state to the TG(on) state and (b) the corresponding charges integrated in the volume of the PPD in time. Followed by the (c) chronograph of the biasing applied to TG and SN during the second simulated toggling of the TG from the TG(on) state to the TG(off) state and (d) the corresponding charges integrated in the volume of the PPD in time.

1.6 State-of-the-art of iToF pixel: performances & technology

Table 1.3 is a synthesis of different iToF sensor technology performances. The PPD iToF pixel alternative allows for lower consumption pixels when compared to the CAPD pixel alternative, consequently allowing larger pixel arrays. The transfer efficiency in terms of DMC is higher for the PPD iToF when compared to the silicon CAPD. However, the germanium CAPD shows even higher DMC values regardless of an increase of the demodulation frequency (f_{mod}). This happens for two reasons: firstly, because of the higher mobility of free carriers in germanium when compared to silicon. Secondly, because of the use of thinner substrates for the absorption layer, causing carriers to be photogenerated closer to the sensing nodes. Despite the thinner absorption layers the germanium CAPD shows a much higher quantum efficiency at higher wavelengths (λ). Being capable of operating in SWIR at 1400nm [53] or even 1550nm [44]. Even with the attractive performances in terms of DMC and QE, little information is available for the dark signal of germanium CAPD sensors. Indeed, because of germanium band gap properties, theses devices may suffer from high leakage.

In general, PPD iToF outperform the silicon CAPD. However, due to the fabrication advantages of the CAPD sensor, lower fabrication costs can be achieved. Because of that, this solution is commercially pertinent [45].

Table 1.3: State-of-the-art iToF performances.

	PPD iToF			**CAPD**	
	Keel [17] (2021)	***Tubert [18] (2021)***	***Ebiko [58] (2020)***	***Chen [53] (2020)***	***Jang [63] (2021)***
Process	3D-stacked 65nm/40nm	3D-stacked 65nm/65nm	3D-stacked 90nm/65nm	Ge-on-Si	3D-stacked 90nm/65nm
Pixel pitch (μm)	3.5	4.6	3.5	10	5
Taps	4	2	2	2	2
Pixel array	1280x960	672x804	1280x960	240x960	640x480
DMC @f_{Mod}	80% @200MHz	88.5% @200MHz	79% @200MHz	70% to 90% @500MHz	80% —
QE @$\lambda(nm)$	38% @940	18.5% @940	32% @940	46.3% @1310	—
Power Consumption	290mW (sensor) @30fps	300mW (system) @30fps	300mW (sensor)	200mW (sensor)	140mW (sensor)
Depth range	0.3 to 3.0m	0.4 to 4.0m	0.4 to 4.2m	—	0.3 to 3.0m
Depth noise	$< 1.52\%$ @—	$< 1.0\%$ @dark	$< 0.7\%$ @25kLux	$< 0.55\%$ @Outdoor at $1.0m$	$< 0.47\%$ @at $3.0m$

A solution analog to the TVG, described in section 1.3.4, called "Dual VG" has been integrated to an iToF pixel [30]. Significantly high performances are obtained in terms of DMC. Table 1.4 compares the available results of the TVG solution found in literature with the state-of-the-art PPD planar gate iToF. However, Yorikado et al. [30] indicate that using the vertical gates increases consumption, making this solution less competitive compared to the planar gate option. Despite the observations on consumption, no values were given.

Table 1.4: The latest solution analog to TVG ("Dual VG") iToF versus existing state-of-the-art using planar gates

	"Dual VG" iToF	**PPD iToF**		
	***Yorikado [30]* (2023)**	***Keel [17]* (2021)**	***Tubert [18]* (2021)**	***Ebiko [58]* (2020)**
Process	3D-stacked 90nm/65nm	3D-stacked 65nm/40nm	3D-stacked 65nm/65nm	3D-stacked 90nm/65nm
Pixel pitch (μm)	3.0	3.5	4.6	3.5
Taps	2	4	2	2
Pixel array	640x480	1280x960	672x804	1280x960
DMC @f_{Mod}	88% @200MHz	80% @200MHz	88.5% @200MHz	79% @200MHz
QE @$\lambda(nm)$	38% @940	38% @940	18.5% @940	32% @940
Power Consumption	—	290mW (sensor) @30fps	300mW (system) @30fps	300mW (sensor)
Depth noise	$< 0.8\%$ @Outdoor 10kLux	$< 1.52\%$ @—	$< 1.0\%$ @dark	$< 0.7\%$ @Outdoor 25kLux

Conclusion

Synthesis

Distance measuring techniques can be classified into three groups: interferometry, triangulation, and time-of-flight. Interferometry is commonly used for high-precision short distance range measurements of less than 1mm, while triangulation-based techniques accuracy depends on the distance between the emitter and the receiver. Currently, the structured light technique, that uses a triangulation-based computation, is a strong competitor for 3D imaging.

The structured light technique reconstructs a 3D image from a 2D spatially varying intensity patterns. The computation for the reconstruction of the 3D image from a 2D image may have a significant computational load. The time-of-flight technique, the alternative competitive technique, measures the time it takes for a wave to travel from a laser source to an object and back to the sensor. Despite its consequent system size, it is a good candidate for low consumption and high precision distance measurement, especially for a use in both long and short range measurements. A synthesis of the different techniques with a performances balance sheet is shown in Table 1.5.

Table 1.5: Comparison of structured light and time of flight depth sensing techniques [13].

3D optical measurement technique		
	Structured light	**Time of flight**
System size	-	+
Short distance	++	++
Long distance	-	++
Outdoor performance	++	+
Computational load	++	++
Triangulation based	Yes	No
Range adaptability	-	++

The indirect time-of-flight (iToF) measurement technique involves measuring the phase difference between the emitted reference signal and the received measured signal, with the time delay proportional to the traveled distance. For a continuous modulated light signal, the received phase shifted signal photogenerates charges inside each pixel, which are sampled into different collection sites and transferred to storage capacitors for readout. The phase value is computed by measuring the charge values at each demodulation cycle and using equation (1.6). This technique allows for precise distance measurements. However, it requires more complex circuitry and can have a higher computational load.

In addition to the indirect time-of-flight (iToF) measurement technique using a continuous wave modulated light, there is also the pulse light iToF (pToF) technique. This involves measuring the phase shift between an emitted periodic pulse wave and the one reflected by the object. While pToF and direct ToF are simpler in terms of the

light source used, iToF remains more precise and reliable for applications requiring exposure to ambient illumination, such as facial and spatial recognition. To obtain a smaller pixel size, often only two collection sites are designed per pixel and image reconstruction techniques such as phase shifting between frames or coupling neighbor pixels are prioritized.

The choice between rolling and global shutter image sensors is also an important consideration for 3D imaging applications. Rolling shutter exposes each line of the image at a slightly different time, which can result in motion blur in images of moving objects. In contrast, global shutter exposes the entire image at once, making it more suitable for 3D imaging techniques such as structured light and time-of-flight. In addition to rolling and global shutter pixels, there is another distinction for pixel architectures, i.e. voltage domain or charge domain pixel. The latter measures the photogenerated signal directly in the form of a charge signal and transfers the charges to memories inside the pixel. However, charge domain pixels have two main issues: the memories integrated directly on the pixel level constrain the miniaturization of the pixel, reducing the effective pitch of the pixel, and parasitic light reaching storage memories reduces the efficiency of light photogeneration and collection. An alternative to charge domain pixels is voltage domain pixels, where the photogenerated signal is collected directly as a voltage signal. Floating diffusions combined with high density capacitors are used to convert and store charges as a voltage value.

Additionally, different pixel structures are found in literature. They can be compared through the key figures of merits shown in Table 1.6, e.g. demodulation contrast (DMC), quantum efficiency (QE) and power consumption. Two different pixel strucatures have been distinguished, they are the current assisted photonic demodulator (CAPD) [16] and the pinned photodiode (PPD) iToF pixels [17, 18, 58]. Furthermore, a third new type of pixels has been demonstrated. These pixels replace the state-of-the-art PPD implant and planar gates by vertical gates [30].

Goal of this work

For the different distance measuring techniques, iToF is an elaborated and accurate technique. The various figures of merit available (section 1.5), allow the comparison of different pixel and sensor solutions. To be able to integrate an iToF pixel to a sensor with high resolution and low consumption, various challenges can be identified.

The goals of this work are (i) to construct a complete simulation methodology for the study of the iToF pixels, (ii) to apply this complete methodology to exploit the existing and new pixel solutions. The study of the existing solutions will then help accomplish the next main goal, that is (iii) to propose innovating iToF pixel solutions exceeding the state of the art performances, to be fabricated and tested.

The following chapters concern in a first moment the benchmark of the different simulation methodology. In chapter 2, a complete multiphysics methodology is described for the simulation and computation of the figures of merit related to the performances of an iToF pixel. After that, in chapter 3, the classical TCAD simulator is compared to an in house Monte Carlo simulator capable of completing the analysis of iToF pixel. Finally a complete simulation methodology was developed, for the

Table 1.6: The latest solution analog to TVG ("Dual VG") iToF versus existing state-of-the-art using planar gates

	"Dual VG" iToF	**PPD iToF**		
	***Yorikado [30]* (2023)**	***Keel [17]* (2021)**	***Tubert [18]* (2021)**	***Ebiko [58]* (2020)**
Pixel pitch (μm)	3.0	3.5	4.6	3.5
Pixel array	640x480	1280x960	672x804	1280x960
DMC @f_{Mod}	88% @200MHz	80% @200MHz	88.5% @200MHz	79% @200MHz
QE @940nm	38%	38%	18.5%	32%
Power Consumption	—	290mW (sensor)	300mW (system)	300mW (sensor)

computation of all the figures of merit related to an iToF pixel.

This complete methodology is then applied in chapter 4, to the benchmark of the CAPD pixel. Firstly, a commercially available silicon CAPD pixel is reverse engineered and its limitations are identified in detail. Secondly, a germanium CAPD pixel is simulated and in partnership with CEA LETI, the sensor using these pixels is fabricated in a germanium-on-silicon technology.

Finally, in chapter 5, a new solution is proposed for iToF pixels in silicon using TVGs. A complete 3D stack of the proposed innovating solution is simulated optically and electrically. The obtained performances of the new pixel are compared to and exceed those of the state-of-the-art of iToF pixels. The realization and proof of concept are demonstrated through the use of transmission electron microscopy (TEM) cut measurements and preliminary electrical characterization results.

References

[1] W. S. Boyle and G. E. Smith. "Charge Coupled Semiconductor Devices". In: *Bell System Technical Journal* 49.4 (1970), pp. 587–593. DOI: https://doi.org/10.1002/j.1538-7305.1970.tb01790.x.

[2] S. Mendis, S.E. Kemeny, and E.R. Fossum. "CMOS active pixel image sensor". In: *IEEE Transactions on Electron Devices* 41.3 (1994), pp. 452–453. DOI: 10.1109/16.275235.

[3] M. Bigas, E. Cabruja, J. Forest, and J. Salvi. "Review of CMOS image sensors". In: *Microelectronics Journal* 37.5 (2006), pp. 433–451. DOI: https://doi.org/10.1016/j.mejo.2005.07.002.

[4] Yole. *Statu of the CMOS image sensor industry 2023*. https://www.yolegroup.com/product/report/status-of-the-cmos-image-sensor-industry-2023/. Accessed: November 14, 2023. 2023.

[5] Yole. *3D imaging sensing 2023*. https://www.yolegroup.com/product/report/3d-imaging--sensing-2023/. Accessed: November 14, 2023. 2023.

2 - TCAD simulation methodology

Introduction

Powerful tools are available for the simulation of semi-conductors devices and phenomena. It is the case of Sentaurus TCAD (Technology Computer-Aided Design) process & device simulation tools [37, 64]. A full 3D iToF pixel fabrication process is simulated. The pixel structure is decomposed in a finite number of nodes and the studied solutions are reproduced numerically. This process reduces resources used and fabrication cost significantly.

In this chapter, a synthesis of the different used models will be presented for the different used simulation tools. They are the TCAD finite element method electrical simulation tools and the optical simulation tools. These tools were used to develop a complete and accurate simulation methodology for the computation of the key iToF figures of merit. All figures of merit computed in this chapter were described in detail in section 1.5.

2.1 Simulation tools benchmark

The simulation methodology can be decomposed as in the schematic shown in Fig. 2.1. Firstly, the key process steps are simulated, such as implantation and annealing already validated on an existing process flow. In another simulator the optical behavior of this same structure is simulated. The results of the optical simulation are then imported to an electrical simulation in the form of a photogeneration map. The electrical simulation gives, as an output, the pixel electrical response to the previously simulated optical stimuli. This combined multiphysical approach was used in the developed opto-electrical simulation methodology. In this section, the computation technique used in the optical and electrical simulators will be briefly described.

2.1.1 Optical FDTD simulation

Optical finite-difference time-domain (FDTD) simulations are a powerful tool for simulating the behavior of light in complex optical systems, including the optical stack and transmission equations. FDTD simulations use numerical methods to solve Maxwell's equations (2.1) and (2.2), which describe the behavior of electromagnetic waves, in three-dimensional space and time [65]. The terms $\mathscr{E}$ and $\mathscr{B}$ are respectively

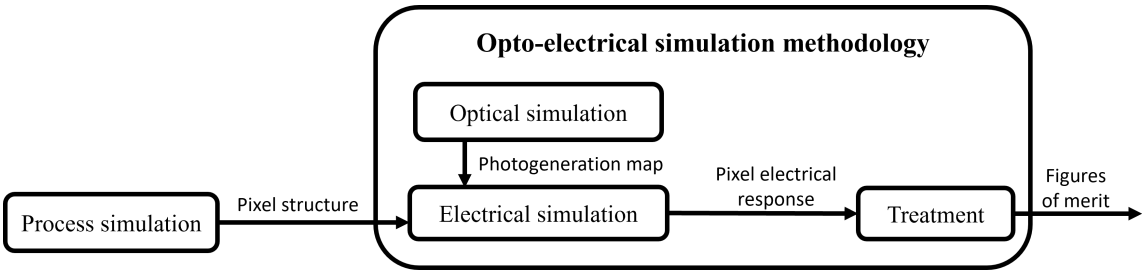


Figure 2.1: Schematic with the different simulation steps used in the developed opto-electrical simulation methodology.

the electrical and magnetic fields, μ_0 is the magnetic permeability of free space, and ϵ_0 is the electric permittivity of free space. The terms μ_R and ϵ_R are the relative permeability and permittivity of the propagation medium. The vector product is represented by the symbol $\wedge$, the vector partial difference in space by nabla ∇ and the partial difference in time by $\frac{\partial}{\partial t}$.

$$\nabla \wedge \mathscr{E} = -\frac{\partial \mathscr{B}}{\partial t} \tag{2.1}$$

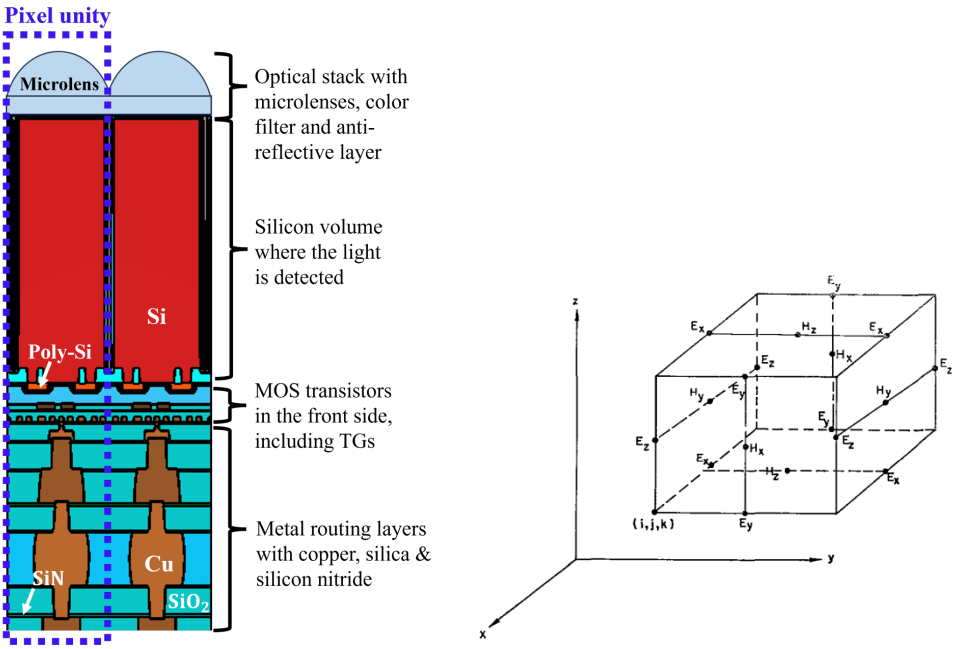
$$\nabla \wedge \mathscr{B} = \mu_0 \cdot \mu_R \cdot \epsilon_0 \cdot \epsilon_R \cdot \frac{\partial \mathscr{E}}{\partial t} \tag{2.2}$$

To dimension a pixel, the various layers that make up the optical stack are considered. A back-side illuminated stack is depicted in Fig. 2.2a. The layers of the stack include the color filter, the microlens, the metal layers and the photodiode. The thickness of each layer needs to be carefully chosen to ensure that the pixel can accurately capture the intended light wavelength. The thickness of the color filter, for example, will determine the amount of light that is allowed to pass through to the photodiode. The microlens, on the other hand, helps to focus the light onto the photodiode, while also reducing the amount of crosstalk between neighboring pixels. Finally, the thickness of the photodiode needs to be optimized to ensure that it can absorb as much light as possible.

To simulate the optical stack, FDTD simulations can be used to model the interaction of light with each layer of the optical stack with different thicknesses and optical properties. The device is decomposed into elementary 3D cells as the one depicted in Fig. 2.2b [65] with different electrical field (E) and magnetic excitation (H) values in each direction.

To model a device using FDTD simulations, the required parameters are described below.

1. **Refractive index:** The refractive index n of each layer is a critical parameter that determines how light interacts with the material. The refractive index describes how much the speed of light is reduced when it passes through a material.



(a) (b)

Figure 2.2: (a) The schematic back-side illumination optical stack layers and (b) the schematic representation of an elementary cell used in 3D FDTD simulation depicted by Yee et al. [65].

2. **Extinction coefficient:** The extinction coefficient k is related to the absorption coefficient and the scattering coefficient [66]. It measures how much light is absorbed by the material versus the wavelength as it passes through the layer. This parameter is important for modeling the Beer-Lambert law, which describes the absorption of light by a material.

Both n and k coefficients are well known for most materials used in the fabrication of semiconductor devices. It is the case for intrinsic silicon and silica [67, 68]. However, for materials with a specific composition, measured n and k coefficient values are imported for different light wavelength (λ) values. For instance, Al_2O_3 and HfO_2 coefficients used in simulation were extracted from ellipsometry measurements for the in-house process at STMicroelectronics. The simulation interpolated the values of n and k coefficients for different λ values.

3. **Polarization:** The polarization of light can also affect how the optical signal interacts with the material. In some cases, it may be necessary to model the polarization of light to accurately simulate the behavior of the optical stack. In simulation, to obtain the response of an optical device, two simulations can be done at different polarization angles of 0° and 90°. By performing a linear combination of these perpendicular responses, any polarization of the incident light beam can be described.

4. **Thickness:** The thickness of each layer is also an important parameter that affects the behavior of light. The thickness of the layer determines the distance that light travels through the material, which can affect the amount of light that is transmitted, reflected or absorbed.

These properties are critical for accurately modeling the behavior of light in different layers of an optical stack using FDTD simulations. The simulated electric and magnetic fields are used to compute the Poynting vector in time domain or in frequency domain.

The Poynting vector, denoted by $\mathscr{P}$, indicates the direction of propagation of the electromagnetic wave in an isotropic medium. The magnitude of the Poynting vector corresponds to the electromagnetic wave power per unity area, expressed in W/m^2, which is also known as the wave intensity. It is defined by the equation (2.3). The terms $\mathscr{E}$ and $\mathscr{B}$ are respectively the electrical and magnetic fields. The magnetic permeability of free space and the relative permeability are respectively μ_0 and μ_R. The vector product is represented by the symbol $\wedge$. $\mathscr{P}$ implicitly depends on the wavelength (λ).

$$\mathscr{P} = \mathscr{E} \wedge \frac{\mathscr{B}}{\mu_0 \cdot \mu_R} \tag{2.3}$$

The power transmission coefficient is computed using equation (2.4) [69, 70]. This equation is the ratio between the power flux of the transmitted wave, given by the flux of the real part of the Poynting vector ($Re\{\mathscr{P}\}$) and the power flux of the optical incident wave ($\int\int p_{ph} \cdot dx \cdot dy$). At the boundaries, the power transmission coefficient ($\mathscr{T}$) is computed, i.e. the parameter that determines the amount of light that is transmitted through the device.

$$\mathscr{T} = \frac{\int\int -0.5 \cdot Re\{\mathscr{P}\} \cdot dx \cdot dy}{\int\int p_{ph} \cdot dx \cdot dy} \tag{2.4}$$

To obtain the power absorption coefficient, the optical generation rate ($\mathscr{G}_{ph}$) is computed with equation (2.5) versus the wavelength (λ). This equation computes the optical generation rate through the inner product ($<,>$). The real part of the dot product between the ∇ operator and the Poynting vector ($\mathscr{P}$) can be decomposed in a function of the material conductivity (σ), the electric field ($\mathscr{E}$), the wavelength of the incident light (λ), Plank's constant (h) and the light speed in free space (c).

$$\mathscr{G}_{ph}(\lambda) = -Re\{<\nabla, \mathscr{P}>\} = \frac{\sigma \cdot |<\mathscr{E}, \mathscr{E}>|}{h \cdot \frac{c}{\lambda}} \tag{2.5}$$

The power absorption coefficient ($\mathscr{A}$) is computed through equation (2.6). This equation is the ratio between the power absorbed in the volume of the material, given by the volume integral of the optical generation rate ($\mathscr{G}_{ph}$) and the total optical power (P_{ph}) of the simulated light.

$$\mathscr{A} = \frac{\int\int\int -0.5 \cdot \mathscr{G}_{ph}(\lambda) \cdot dx \cdot dy \cdot dz}{P_{ph}} \tag{2.6}$$

The FDTD simulation meshing grid spacing must be chosen such that there is no significant change in the electromagnetic field between two calculation nodes. This means that the grid spacing must be smaller than a fraction of the wavelength of the source to ensure the accuracy of the simulation results.

Finally, the frequency information on the simulation results is computed from the Fourier transform of the temporal signal. This allows to compute the light reflection and transmission, or the Poynting vector as a function of wavelength in a single simulation. The frequency information is necessary to be able to replicate the real laser source. Lasers are typically characterized by their ability to emit light at a specific wavelength, which corresponds to a specific light color. However, no laser emits light at a perfectly unique wavelength; there is always a range or *span* of wavelengths around the targeted wavelength where the laser also emits light. This span is non ideal, meaning it is broader than the ideally narrow wavelength that would be expected from a perfect laser source. Hence, the non ideal span in wavelength is replicated in simulation to compute the correct temporal pulse.

2.1.2 TCAD electrical simulation & modeling

From a process simulated structure [64], the obtained pixel can be operated electrically in simulation, as it will be characterized when fabricated. Through finite element method, Poisson equation is computed for potential estimation and continuity equations is computed for transport simulation. Various mobility degradation phenomena can be considered depending on the device and device operation. Furthermore, various recombination mechanisms can be selected based on device expected behavior. From selected external biasing, the pixel can be tested electrically and an in depth understanding of full 3D pixels is enabled.

The coupling of optical simulation can be done to electrical simulation to have a complete view of the device operation. A full 3D optical stack is simulated with commercial FDTD simulator [71]. Light transmission and absorption for a light source can be observed in time. The simulated photogeneration can then be imported during electrical simulation.

Poisson

The 1D Poisson simplified equation (2.7) derived from Maxwell-Gauss equation shows that the electrostatic field gradient, equivalent to the electrostatic potential is dependent on electron and hole concentrations. It is given as a function of the concentration of holes p and electrons n function of the distance x and the acceptor and donor ions respectively N_A^- and N_D^+. The elementary charge constant is q and ϵ is the permitivity of the silicon.

$$\frac{dE}{dx} = \frac{q}{\epsilon} \cdot (p(x) - n(x) - N_A^- + N_D^+) \tag{2.7}$$

Recombination/Generation

Shockley-Read-Hall (SRH) recombination is considered as it can impact pixel performances in two ways. First, it impacts the generated carrier collection by recombination. Second, SRH is a mechanism of generation of electron and hole pairs through recombination centers. The carriers generated by the SRH mechanisms are counted and may impact the accuracy of the measurement [40]. These measured carriers are called dark current and they are considered as noise when computing the signal to noise ratio. The SRH effective recombination rate given in equation (2.8) [72] is computed from the free electron and hole concentrations (respectively n and p), the electron and hole lifetimes (respectively τ_n and τ_p), the intrinsic carrier concentration (n_i), the auxiliar variables n_1 and p_1. For a trap energy level located in the middle of the band gap the relation $n_1 = p_1 = n_i$ is obtained. Otherwise, n_1 and p_1 depend on the effective densities of states and the lattice temperature [34].

$$R^{SRH} = \frac{n \cdot p - n_i^2}{\tau_p \cdot (n + n_1) + \tau_n \cdot (p + p_1)} \tag{2.8}$$

The doping and temperature have a significant contribution to SRH free carriers lifetime (τ_{SRH}). For the simulated cases, SRH doping dependence lifetime degradation is computed with Scharfetter's empirical equation shown in equation (2.9) [72]. The terms N_D and N_A are respectively the donor and acceptor ion concentrations. The terms τ_{max}, τ_{min} and N_{SRH} are empirical fitting parameters. This contribution is simulated with the possibility of being activated and deactivated for comparison. The leakage current was plotted versus the biasing for a case with and without SRH recombination and lifetime degradation shown in equations (2.8) and (2.9).

$$\tau_{SRH}(N_D + N_A) = \tau_{min} + \frac{\tau_{max} - \tau_{min}}{1 + (\frac{N_D + N_A}{N_{SRH}})} \tag{2.9}$$

Continuity

The resolution of the resulting drift-diffusion equation using the finite element method is the current deterministic computation method used by Sentaurus TCAD SDevice [37]. The simple formulation of the continuity equation (2.10) describes the variation in time of the amount of charges ρ due to the charge flux variation Φ and the generation and recombination of charges $(G - R)$ [34].

$$\frac{1}{q} \cdot \frac{\partial \rho}{\partial t} = \nabla \Phi + (G - R) \tag{2.10}$$

Equation (2.10) can be developed in 1D for electrons n giving equation (2.11). The gradient of the flux of charges, i.e. the gradient of the current density gives a drift component $\frac{\partial j_{Drift}}{\partial x}$ (2.12) and a diffusion component $\frac{\partial j_{Diff}}{\partial x}$ (2.12). $\frac{\partial j_{Drift}}{\partial x}$ is proportional to the mobility μ_n and depends on the electrostatic field E. $\frac{\partial j_{Diff}}{\partial x}$ on the other hand is proportional to the diffusion coefficient D_n. The resolution of this

equation using finite element method is the deterministic computation method used by Sentaurus TCAD SDevice [37].

$$\frac{\partial n(x,t)}{\partial t} = \frac{1}{q} \cdot \frac{\partial}{\partial x} j_{Drift}(x,t) + \frac{1}{q} \cdot \frac{\partial}{\partial x} j_{Diff}(x,t) + (G-R)(x,t) \tag{2.11}$$

$$\frac{1}{q} \cdot \frac{\partial}{\partial x} j_{Drift}(x,t) = \frac{\partial}{\partial x}(n(x,t) \cdot \mu_n \cdot \mathscr{E}(x,t)) \tag{2.12}$$

$$\frac{1}{q} \cdot \frac{\partial}{\partial x} j_{Diff}(x,t) = \frac{\partial}{\partial x}(D_n(x,t) \cdot \frac{\partial n(x,t)}{\partial x}) \tag{2.13}$$

Mobility

For the computation of the continuity equation, two models for mobility degradation are considered. They are complementary.

Firstly, the high field saturation model computes the degraded mobility ($\mu_{High-\mathscr{E}}$) due to the saturation of free carrier velocity under high field [73] from the low electric field mobility ($\mu_{Low-\mathscr{E}}$). The relation used to compute the high field degradation is given in equation (2.14). It depends on the saturation velocity (v_{sat}) and the temperature (T). Herein for most simulation results, temperature is fixed at $333K$. This value corresponds to the temperature of the sensor device during operation.

$$\mu_{High-\mathscr{E}}(\mathscr{E}) = \frac{\mu_{Low-\mathscr{E}}}{((1 + (\frac{\mu_{Low-\mathscr{E}} \cdot \mathscr{E}}{v_{sat}})^{1.188}))}, for\ T = 333K\ (60°C) \tag{2.14}$$

Secondly, the inversion and accumulation layer mobility model (IALMob) is used. IALMob model also takes into consideration the mobility degradation components due to acoustic phonon scattering and surface roughness scattering [74, 75]. In the iToF pixel, this model is necessary for two reasons: to consider the free carriers mobility degradation (i) in zones with high free carriers concentration due to a high photogeneration and (ii) in zones close different material interfaces, such the silicon under the tranfer gates, close to the interface between the silicon and silice. The mobility is computed with the relation shown in equation (2.15). Where $\mu_{Coulumb}$, μ_{Phonon} and $\mu_{Surface}$ are respectively coulomb impurity scattering, phonon scattering and surface roughness scattering. The latter has a weight ($\mathscr{D}$), whose corresponding relation is given in equation (2.16). It is a function of the shortest distance between an interface and the computed coordinate (x) divided by the critical distance (l_{crit}), depending on the interface materials.

$$\frac{1}{\mu} = \frac{1}{\mu_{Coulumb}} + \frac{1}{\mu_{Phonon}} + \frac{\mathscr{D}}{\mu_{Surface}} \tag{2.15}$$

$$\mathscr{D} = e^{-(\frac{x}{l_{crit}})} \tag{2.16}$$

2.2 Pinned photodiode modeling

To understand the different physical mechanisms impacting the transfer of free charges in an iToF pixel the selected approach is first to model a more elementary device, that is the pinned photo diode (PPD). The electrical modeling and the computation of Poisson and the continuity equation described in the previous section are used within the FEM Sentaurus TCAD to discribe the operation of the PPD [37].

The PPD is the state-of-the-art 2D pixel solution and it resembles significantly the state-of-the-art iToF pixel, as it was described in section 1.3.3. For a 2D image, the factors that impact the quality of the acquisition are dependent on both signal and noise. The sensitivity of devices is also determined by QE. The detected charges in 2D imaging are collected in two separated steps: integration and readout. The performance of 2D imaging, is mainly estimated by simulating the maximum charges that can be stored in the pixel volume and measured in the sensing nodes, known as the fullwell capacity. Unlike iToF pixels, 2D pixels have longer operation times (e.g. transfer times higher than 0.1ms) and because of that, they have lower transfer speed requirements.

The PPD was previously introduced in subsection 1.3.2. The schematic previously depicted in chapter 1 at Fig. 1.16a is simulated and the non-optimized pixel structure is depicted in Fig. 2.3a. It has various implants: (i) a P-type doping silicon substrate, doped with a Boron concentration of $1 \cdot 10^{15} cm^{-3}$, (ii) a deep N-type implant for the photodiode creation, (iii) a shallow P+ implant for the pinning of the photodiode, (iv) the P-Well implant for the creation of isolated zone for N-MOS inside the pixel and (v) N+ implant with Phosphorus and Arsenic for the creation of the floating diffusion SN. Furthermore, the pixel has a polysilicon transistor doped N-type used as a TG, the back-side passivation stack and shallow trench insulator (STI) depicted at the left and right top sides in Fig. 2.3a. The uncharged insulators like silicon oxide are depicted in grey.

The developed methodology consists in operating the simulated pixel in time and reproducing the different steps depicted in Fig. 2.3c. The different operation steps are: (1.) the reset, (2.) the integration and (3.) the read-out steps.

2.2.1 Electric potential distribution simulation

The main simulated steps are represented with TCAD 2D simulation plots in Fig. 2.4, Fig. 2.5 and Fig. 2.6. They are respectively (1.) the reset, (2.) the integration and (3.) the read-out steps. These three steps are depicted with electrical simulations in this section. Here it is done for a 2D simulated pixel, but it can also be applied to 3D simulated pixels.

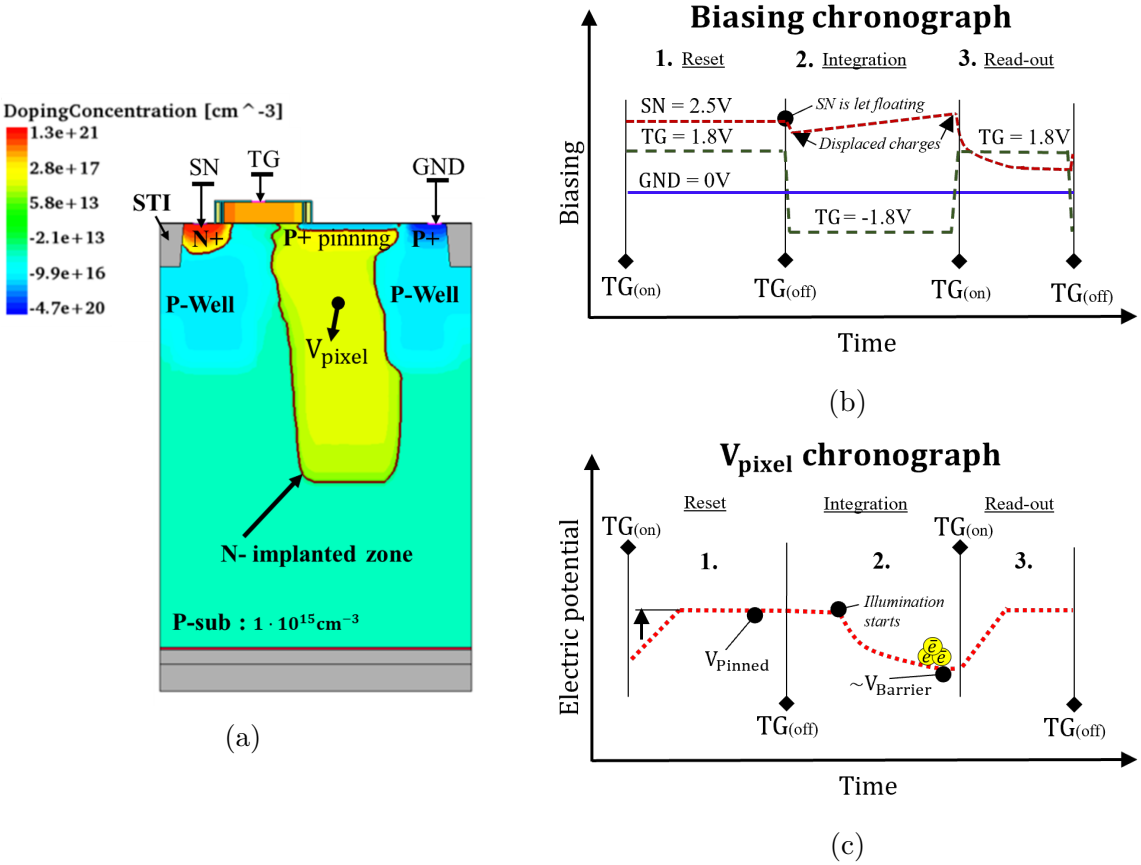
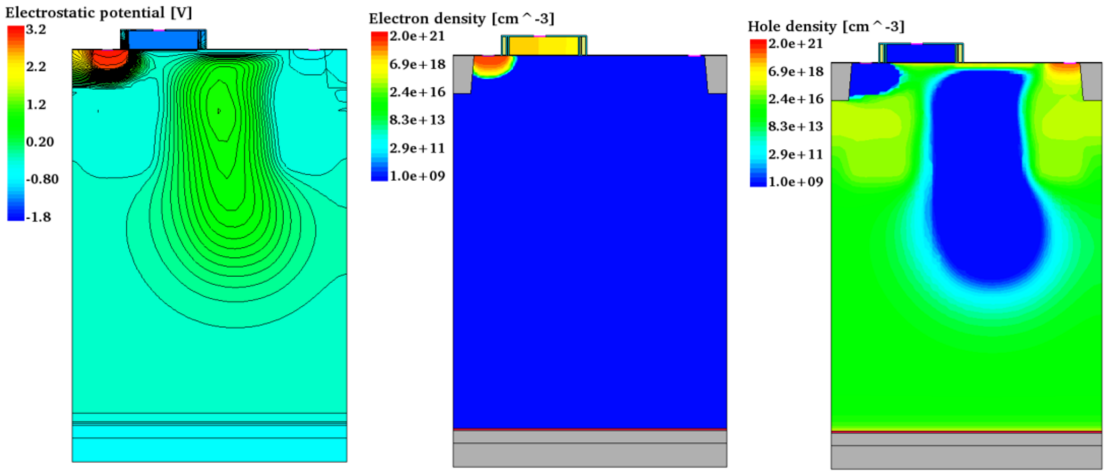


Figure 2.3: (a) The non-optimized simulated PPD pixel with its various implants: $^{(i)}$a P-type doping silicon substrate (*P-subs*), doped with a Boron concentration of $1 \cdot 10^{15} cm^{-3}$, $^{(ii)}$a deep N-type implant for the photodiode creation, $^{(iii)}$a shallow P+ implant for the pinning of the photodiode and the creation of the ground reference for the holes (GND), $^{(iv)}$the P-Well implant for the creation of isolated zone for N-MOS inside the pixel and $^{(v)}$N+ implant with Phosphorus and Arsenic for the creation of the floating diffusion SN. Furthermore, the pixel has a polysilicon transistor doped N-type used as a TG, the back-side passivation stack and shallow trench insulator (STI) on the top side. (b) The pixel operates in three different steps illustrated in the chronograph. They are (1.) the reset, (2.) the integration and (3.) the read-out steps. TG(on) and TG(off) are respectively the TG activation and deactivation states. (c) The maximum electrostatic potential (V_{pixel}) evolution at the center of the PPD pixel during the different operation steps is illustrated by another chronograph. V_{pinned} is the maximum depletion potential of V_{pixel} and $V_{Barrier}$ is the electric potential barrier caused by the deactivation of the TG between the PPD and the SN during the integration step.

(1.) Reset

In the reset step, the pinned potential is attained by activating the TG at the on-state ($TG(on) = 1.8V$) and maintaining the sensing node (SN) at a high potential of $2.5V$ (Fig. 2.3b). The maximum potential inside the photodiode identified by V_{pixel} in Fig. 2.3a is represented in time by the red doted line in Fig. 2.3c. The activated transfer gate, actively deserts the volume implanted with N-type doping shown in Fig. 2.3a. Fig. 2.4a illustrates the electrostatic potential distribution for the depleted pixel after the TG is deactivated ($TG(off)$). The potential at the center of the photodiode V_{pixel} is equal the pinned potential V_{pinned} when the implanted zone is fully depleted. While the TG remains at the off-state the pinned photodiode (PPD) remains depleted, maintaining the depletion potential in the volume of the pixel. The electron and hole concentrations are depicted respectively in Fig. 2.4b and Fig. 2.4c. The maximum depletion potential value can be used as a figure of merit for 2D pixels, here called V_{pixel}.



(a) (b) (c)

Figure 2.4: 2D simulation of the PPD structure depicted in Fig. 2.3a. The SN biased at $2.5V$ and the GND biased at $0V$. (a) The electrostatic potential distribution, (b) the electron density and (c) the hole density of the pixel is plotted just after reset with TG biased at TG(off)= $-1.8V$.

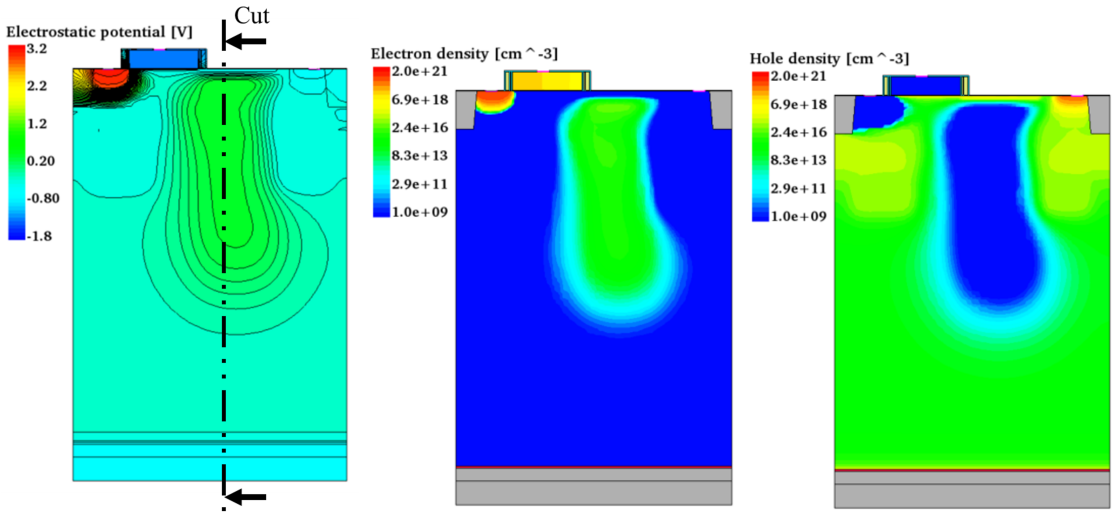
(2.) Integration

During the integration step, for the measurement of the optical signal, the TG is maintained in the off-state ($TG(off)$). The photogenerated charges are firstly directed to the depleted implanted photodiode. The potential at the center of the photodiode V_{pixel} decreases with the increase of the electron concentration in the volume (Fig. 2.3c). The photogenerated holes are evacuated at the reference ground node GND biased at V_{GND}. The value of the potential at the center of the photodiode

V_{pixel} becomes closer to the strong low $V_{Barrier}$ potential between the SN and the photodiode during illumination. During the off-state, the TG impedes the transfer of charges to the floating diffusion.

Before the toggling of the TG between the on- and the off-states, the sensing node is left floating. Hence, the TG voltage excursion causes the potential of the sensing node to change. This is a result of the displaced charges caused by the TG voltage swing.

The charges photogenerated within the pixel are transferred to the center of the pixel, leading to a change in the depletion potential level. This behavior is simulated by importing an optical generation map for a short duration throughout the state $TG(off)$. The photogeneration used in this part is a normalized uniform distribution map, that is a 3D map with a normalized constant photogeneration value in the silicon volume and a null photogeneration value elsewhere. The pixel is maintained in this state for a duration corresponding to the integration time (10ms). During this time, there is the leakage of charges due to diverse mechanisms, i.e. diffusion and recombination. The potential distribution for the pixel filled with photogenerated electrons stored in its volume is depicted in Fig. 2.5a. The electron and hole concentrations are respectively depicted in Fig. 2.5b and Fig. 2.5c.



(a) (b) (c)

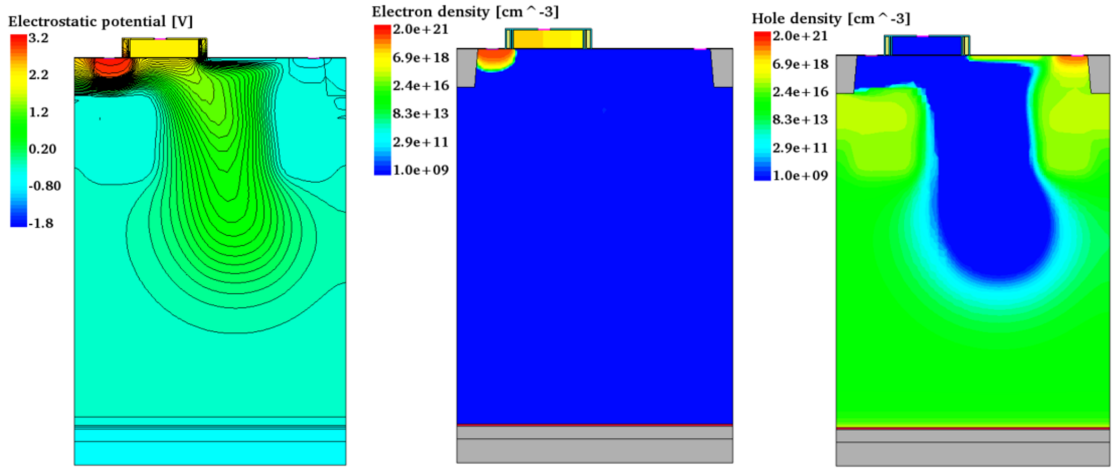
Figure 2.5: 2D simulation of the PPD structure depicted in Fig. 2.3a. The SN biased at $2.5V$ and the GND biased at $0V$. (a) The electrostatic potential distribution, (b) the electron density and (c) the hole density of the pixel is plotted after illumination with TG biased at TG(off).

(3.) Readout

At the readout step, the transfer gate is activated ($TG(on)$) and the photogenerated electrons are transferred to the SN. The potential of the sensing node V_{SN} decreases as the number collected electrons increases [39]. Indeed, the studied pixel is a voltage domain pixel. The fullwell capacity is the total measurable charge for this operation. The detailed description of the computation method for fullwell will be done in the next section 1.5.6.

The maximum value of minority carries, i.e. electrons that can be stored in the volume is an important figure of merit and it is used to compute the fullwell capacity of the pixel. The maximum of electrons that can be stored in the volume is different than the maximum of electrons that can be stored at the sensing nodes. When the transfer gate is activated, not all the electrons at the center may be detected if the sensing node storage capacity is lower than the photodiode charge storage capacity. Hence, the fullwell capacity will depend on both the potential distribution within the pixel photodiode and the sensing nodes.

The readout potential distribution, when the transfer gate is on the $TG(on)$ state, is depicted in Fig. 2.6a. In the simulated case, the sensing node is not left floating. Indeed, it is often simpler to bias the sensing node at a lower biasing to evaluate the transfer limitations of the pixel. A simulation with a floating sensing node will have much higher computation cost, due to the constantly changing electrostatic potential values in different simulation meshing points. In the case of the presented simulated structure, all charges are collected in the SN biased at 2.5V



(a) (b) (c)

Figure 2.6: 2D simulation of the PPD structure depicted in Fig. 2.3a. The SN biased at $2.5V$ and the GND biased at $0V$. (a) The electrostatic potential distribution, (b) the electron density and (c) the hole density of the pixel is plotted during read-out with TG biased at TG(on)= $1.8V$.

The electron and hole concentrations are respectively depicted in Fig. 2.6b and Fig. 2.6c. A 1D cross-section, identified by the cut in Fig. 2.5a, is done over the 2D simulated electrostatic potential distribution (Fig. 2.7a) and electron density (Fig. 2.7b) distribution. V_{pixel} is identified by the maximum of the potential 1D distribution after reset. During readout this maximum of potential increases. This is caused by the much higher biasing potential of the SN than V_{pixel}. In this case, the SN potential sets the potential in the volume.

Differently from a biased sensing node, a sensing node floating diffusion electric potential would decrease with the collection of charges according to equation (1.16). When the SN electric potential becomes too low, the readout of charges remaining in the volume is not possible. To ensure the best trade-off between the measured contrast, i.e. dependent on the sensing node excursion voltage and the detection of all charges, the floating diffusion SN capacitance is designed considering the application.

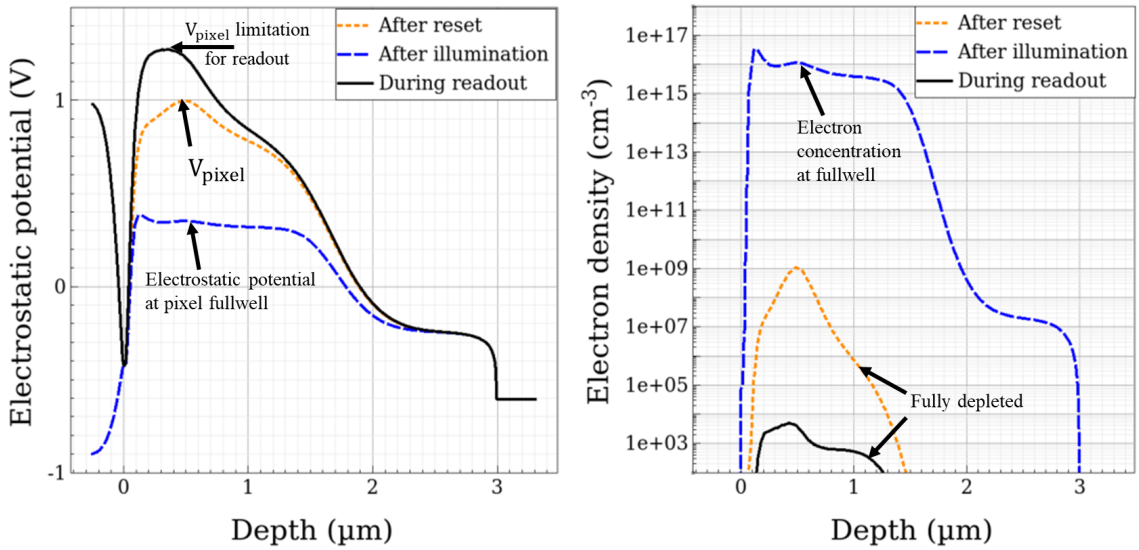


Figure 2.7: 1D cut depicted in Fig. 2.5a at the maximum of potential (V_{pixel}) inside the PPD for three different cases: (Fig. 2.3c(1.)) just after reset, (Fig. 2.3c(2.)) after illumination and (Fig. 2.3c(3.)) during read-out. (a) The electrostatic potential distribution and (b) the electron density are plotted in the direction of the 1D cut versus the depth of the pixel.

Furthermore, the difference of potential between the SN and the PPD should be considered. Fig. 2.8 illustrates the potential evolution of two different cases, they are a high and low conversion factor PPD pixels. The sensing node is reset at V_{RST} and during the read-out the electric potential of the floating diffusion decreases. To avoid possible transfer issues due to a low electric potential of the sensing node (V_{SN}), the electric potential V_{pinned} is optimized lower than the maximum allowed excursion of V_{SN}. That way, the PPD may be entirely depleted and V_{pixel} is equal V_{Pinned}. Furthermore, all the photogenerated charges may be collected by the sensing node without transfer issues due to a lack of electric field or a potential barrier between the photodiode and the sensing node. Besides this optimization, other developments have allowed to facilitate the transfer between the photodiode and the SN by optimizing the channel of the TG, it is the case of the buried channel TG [57].

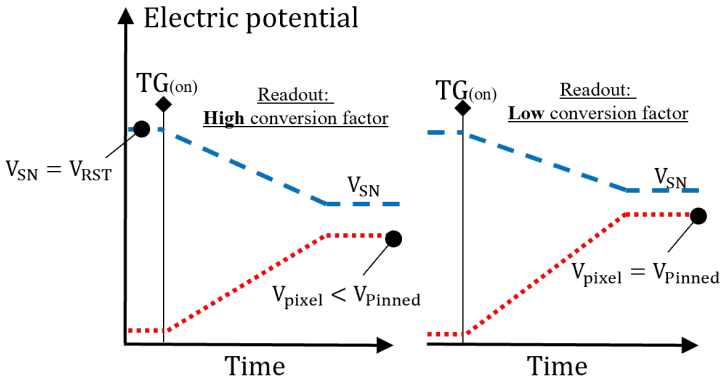


Figure 2.8: Schematic representation of the floating electric potentials in the sensing node (V_{SN}) and in the center of the photodiode (V_{pixel}) in time for two different values of the sensing node conversion gain. Firstly, to the left, the schematic for a high conversion factor, not allowing the full depletion of the pixel with the initialization of the sensing node at the value of the reset biasing (V_{RST}). Secondly, at the center, a low conversion gain, allowing the full depletion of the center of the photodiode reaching the pinning potential (V_{Pinned}).

2.2.2 Fullwell computation

The computation of minority carriers in the volume of the pixel in time is a key element of the methodology used for computing the fullwell. In this section, the fullwell is simulated for the PPD presented in the previous section 2.2.1.

The fullwell capacity, introduced in section 1.5.6, is the total measured charge per pixel for a single sensor acquisition. This is done by integrating the electron concentration in the volume of the PPD in time. At the same time, it is also possible to track the evolution of V_{pixel} by plotting the maximum electrostatic potential value in the volume of the pixel. The methodology for computing the fullwell capacity is depicted with the time diagrams in Fig. 2.9.

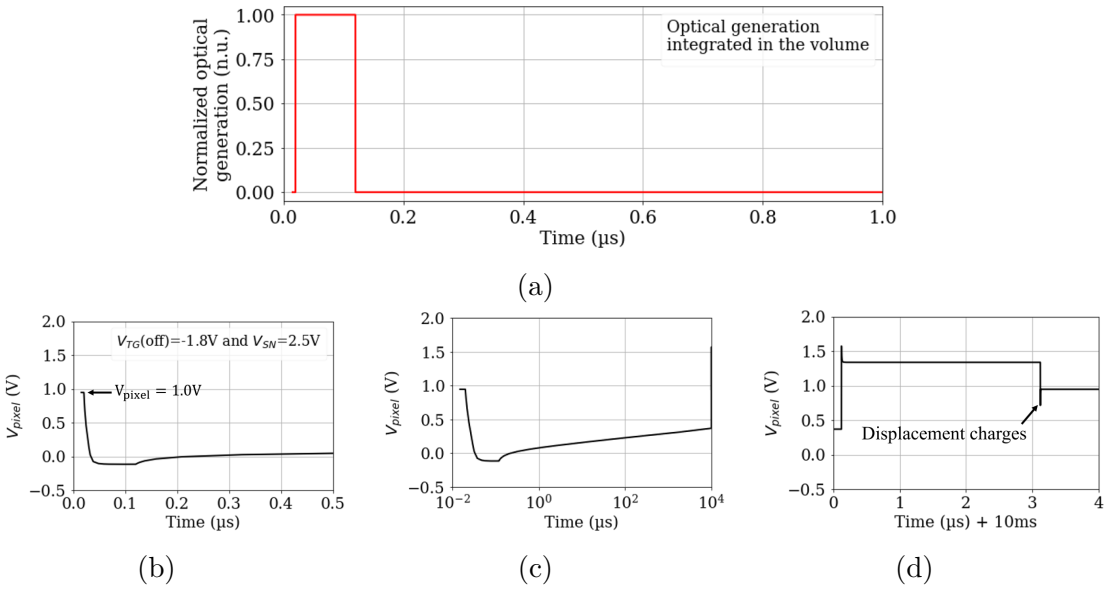


Figure 2.9: The complete fullwell simulation methodology with (a) the imported photogeneration time diagram, (b) the corresponding evolution of the potential at the center of the pixel (V_{pixel}). (c) V_{pixel} is also plotted for the whole duration of the simulation versus the time abscissa in the logarithmic scale. Finally, (d) a zoom is done at the abscissa at the time zone of the toggling of the TG from the TG(off) state to the TG(on) and back to the TG(off) state. The displaced charges in the volume of the PPD, caused by the toggling of the TG, impact the value of V_{pixel}.

The simulation starts with a reset pixel with V_{pixel} equals 1.0V (Fig. 2.9b). The pixel is illuminated with an uniform optical generation for the duration depicted in Fig. 2.9a. After the illumination, the previously depleted PPD in the center of the pixel is filled with minority carriers and it is left to leak for the duration depicted in Fig. 2.9c, V_{pixel} changes with the change of the electrons concentrated in the volume. For a constant value of the biasing of the SN (V_{SN}), the TG toggles from the off-state ($TG(off)$) with a low biasing of -1.8V to the on-state ($TG(on)$) with a high biasing of 1.8V. The voltage ramp is depicted in Fig. 2.10a. After the readout of charges in the SN, the TG changes again from the state $TG(on)$ to $TG(off)$ as shown in

Fig. 2.10c. Fig. 2.9d depicts the evolution of V_{pixel} with the changes of state of the TG. The significant increase in V_{pixel} is caused by the displaced charges originated from the toggling of TG between states, observed in Fig. 2.9d .

Fig. 2.10 shows not only the biasing of the TG changing between the $TG(on)$ to $TG(off)$ states, but it also shows the zoomed plot of electrons integrated in the volume of the photodiode. Fig. 2.10b is an image of the charge increase due to the activation of the TG but also of the charge decrease due to the collection of photogenerated charges. In contrast, for the time duration shown in Fig. 2.10d, all charges have already been collected. Hence, the change of the electrons in the volume of the pixel depicted Fig. 2.10d is only due to the displaced charges. The total number of electrons inside the pixel returns to the initial reference value of nearly zero charges. This shows that all photogenerated electrons have been collected. Furthermore, it shows that the displaced charges from the activation of the TG are compensated with the displaced charges due to the deactivation of the TG.

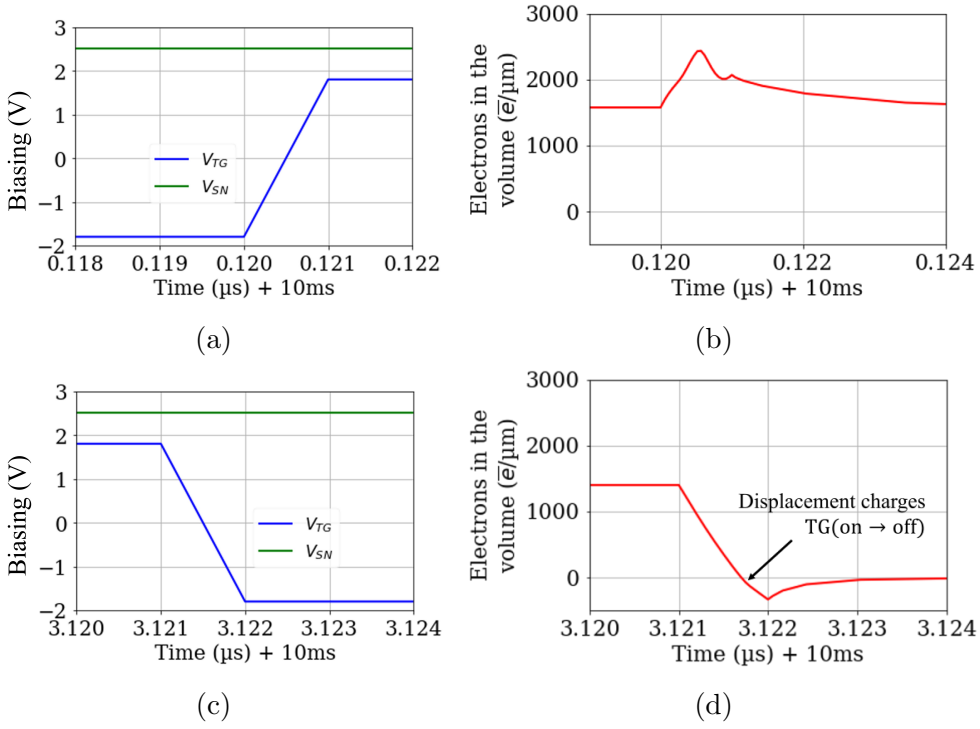


Figure 2.10: (a) Chronograph of the biasing applied to TG and SN during the first simulated toggling of the TG from the TG(off) state to the TG(on) state and (b) the corresponding charges integrated in the volume of the PPD in time. Followed by the (c) chronograph of the biasing applied to TG and SN during the second simulated toggling of the TG from the TG(on) state to the TG(off) state and (d) the corresponding charges integrated in the volume of the PPD in time.

The duration of the computations during the simulation is different depending on the time step. To achieve suitable computation times, adaptable time steps are used. Fig. 2.11 shows how larger steps can be used in simulations of the same duration of $10ms$. These larger steps converge to the same value of leaked charges. However, the duration of the computations during the simulations is much shorter.

The fullwell value is computed from the difference of electrons in the volume after displaced charges stabilize and before the activation of the TG. These values correspond to the ending and starting times of Fig. 2.9d. The fullwell obtained for this non-optimized pixel is 1600 electrons.

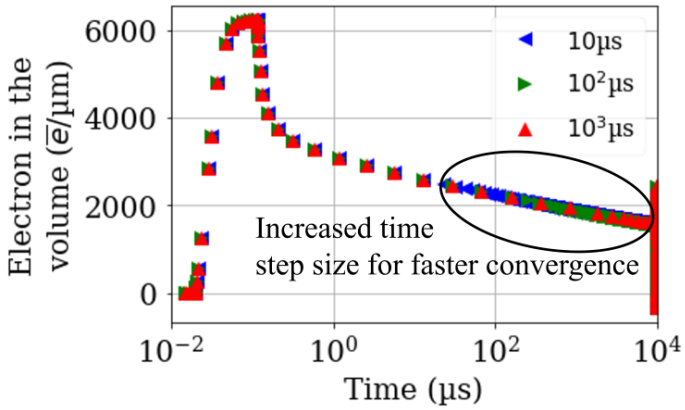


Figure 2.11: Integrated electron concentration in the volume of the 2D simulated PPD in time for different simulation time steps.

2.3 Indirect time-of-flight pixel simulation

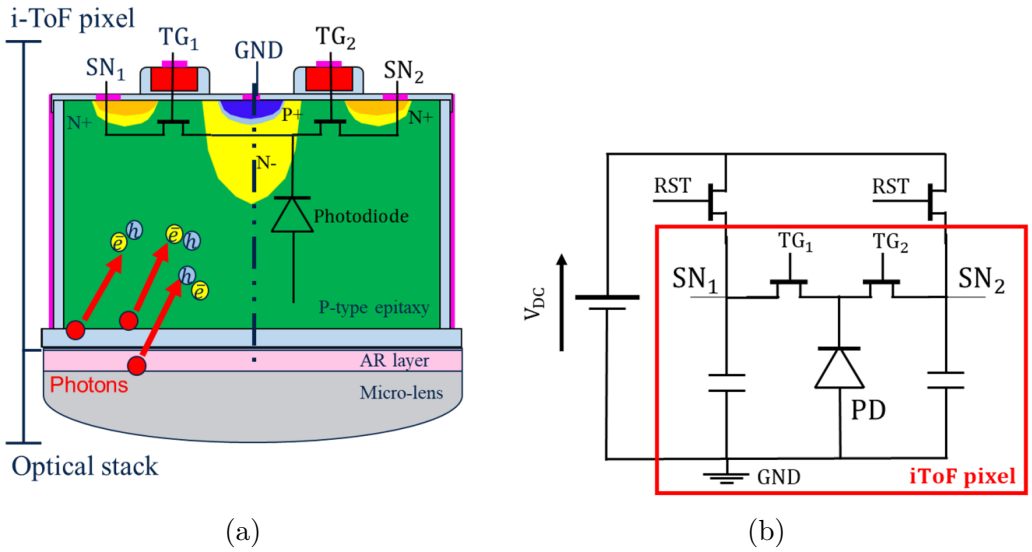
Aiming to develop and optimize new iToF pixel solutions, a complete methodology has been developed to simulate iToF pixels. The approach consists of, firstly, qualitatively analyzing the electric potential distributions inside of the pixel and secondly, computing the key figures of merit described in section 1.5.

Indeed, as a mean of comparing different 3D iToF image acquisition solutions, figures of merit are defined. These figures can simplify the interpretation of the performance of one solution against another. In this section, two types of figures of merit are presented. The first type includes the transfer efficiency figures, namely: parasitic light sensitivity (PLS), transit time (TrT) and demodulation contrast (DMC). Routines for simulating these figures of merit will be defined. The second type includes the signal and noise figures of merit, namely: the signal figure i.e. quantum efficiency (QE).

Additionally in the second type, there are the noise figures of merit that will not be discussed in this chapter. They are the pixel response non-uniformity (PRNU) and the depth non uniformity (DNU). Monte Carlo simulations can be used to help quantify these noise figures and improve the understanding of simulated devices, this will be the subject of the next chapter.

2.3.1 Pixel modeling

An example of iToF pixel with two collection sites is shown in Fig. 2.12a [17, 18]. Each of the two collection sites, the sensing nodes SN_1 and SN_2, have a corresponding transfer gate TG_1 and TG_2. They guide the sampled charges to the storage nodes or capacitors which are depicted in the iToF pixel equivalent circuit in Fig. 2.12b. A deep N-type doped zone in yellow is implanted at the center of the device. It is a deep photodiode implant which creates a central depletion region with an electric field that favors carrier drift until they reach the sensing nodes. Additionally, the full pixel architecture incorporates the optical stack with microlenses and anti-reflective (AR) layers, the read-out MOS circuit and metal layers for the contact routings [76]. These elements of the architecture do not impact the electrical behavior of the iToF pixel and will not be incorporated in this simulation study. In the case depicted in Fig. 2.12a, the silicon volume is an epitaxied layer doped with a low P-type concentration and is referenced at a ground biasing GND through a $P+$ implanted zone. Furthermore, the pixel is surrounded with deep trench isolation (DTI). They can be biased, allowing DTI to operate both electrically and optically [18].



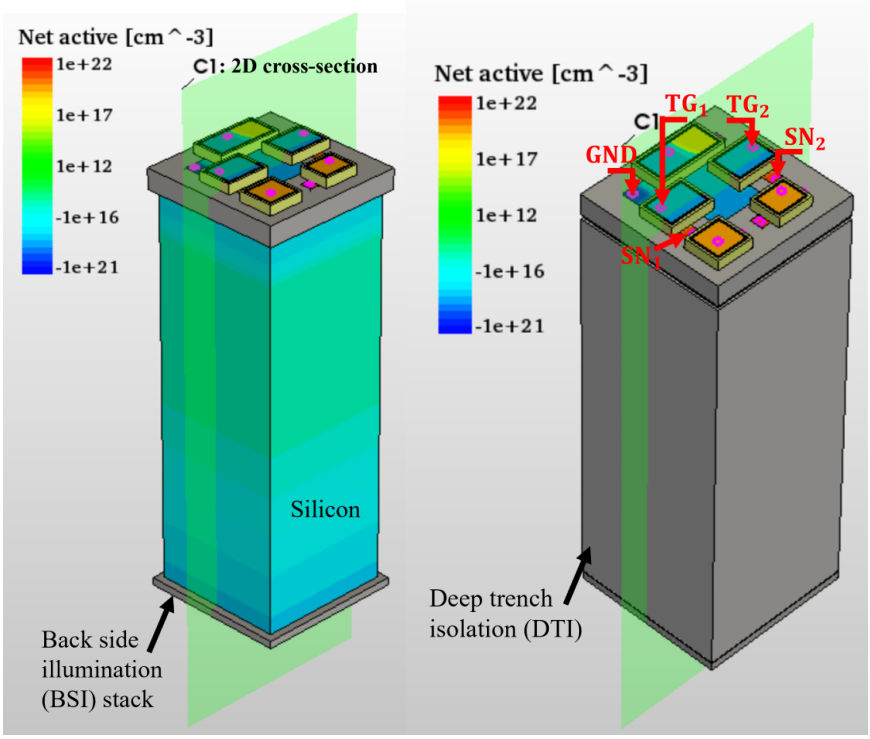
(a) (b)

Figure 2.12: (a) An iToF pixel structure cross-section with two transfer gates (TG_1 and TG_2), two sensing nodes (SN_1 and SN_2), a deep N-type implant for the creation of the photodiode, the DTI and the optical stack. (b) The pixel equivalent electronic circuit for the given structure is highlighted with a red square.

2.3.2 Electrostatic potential analysis

A non optimized iToF pixel has been selected for the simulation methodology benchmark. The 2D cross section of the 3D simulated pixel depicted in Fig. 2.13 is used for analyzing the transfer efficiency. The cut plane is transversal to both sensing nodes and TGs.

The obtained net active concentration of the 2D cross section of the pixel is shown in Fig. 2.14. A dark line is used for the separation of differently doped regions. The white line shows the depletion region when the pixel is biased, i.e. a zone with a majority carrier concentration lower than 5% of the net active concentration. This is the default percentage threshold set by the simulator for the definition of the depleted regions. The pixel is biased and from Poisson's equation computation the electrostatic potential distribution in Fig. 2.14b is obtained. The equipotential lines are plotted for each 100mV for a better understanding of the potential distribution. To attain the potential distribution shown in Fig. 2.14b, first the pixel is reset. This is done by activating both TGs. The photodiode is fully depleted and the sensing nodes are initialized at $2.5V$, the hole and electron concentrations are shown respectively in Fig. 2.14c and Fig. 2.14d. After that, by closing one of the TGs, it is possible to analyze the potential distribution inside the pixel when TG_1 is activated and TG_2 is deactivated, similarly to the operation of the pixel. This scenario of TG activation corresponds to the polarization during one of the demodulation operations shown in Fig. 2.14b, where the transfer gates are toggled between the TG(on) and TG(off) states alternatively.



(a) (b)

Figure 2.13: 3D simulated structure with plotted net active concentration. Two different illustrations are used to (a) expose the silicon volume and identify the BSI stack as well as to (b) illustrate the pixel DTI and the various pixel contacts. The sensing nodes (SN_1 and SN_2 at $2.2V$), transfer gates (TG_1 and TG_2, respectively at $1.2V$ and $0V$) and grounds (GND at $0V$) contacts are identified. Additionally, the shown 2D cross-section plan will be used to analyzing the transfer efficiency of the simulated pixel.

When optimizing an iToF pixel, the goal is to facilitate the transfer. To obtain an efficient transfer, the distribution of the electrostatic potential is optimized. An ideal electric potential distribution favors the collection of all charges while forcing a strong electric field to drive the charges that are photogenerated distant from the sensing nodes. At the same time, a sufficiently low barrier between the sensing node and the PPD is optimized to avoid that charges may be collected by the sensing node where the collection is not intended. Hence, for the comparison of the different potential distributions, the 2D cross section of 3D electrical simulation of photodiode implants with different implantation doses are depicted in Fig. 2.15. If the dose is higher, the obtained higher doping values cause the pinning potential ($V_{pinning}$) to increase. However, if it is too high, an electric potential barrier may appear between the sensing node and the active trasfer gate (TG_1). This issue is observed in Fig. 2.16 from the 1D cut identified in Fig. 2.15. On the contrary, if the implant dose is too low, the distribution of electrostatic potential in the volume of the pixel does not favor the transfer of charges that are photogenerated far from the sensing nodes (e.g. the green line in Fig. 2.16).

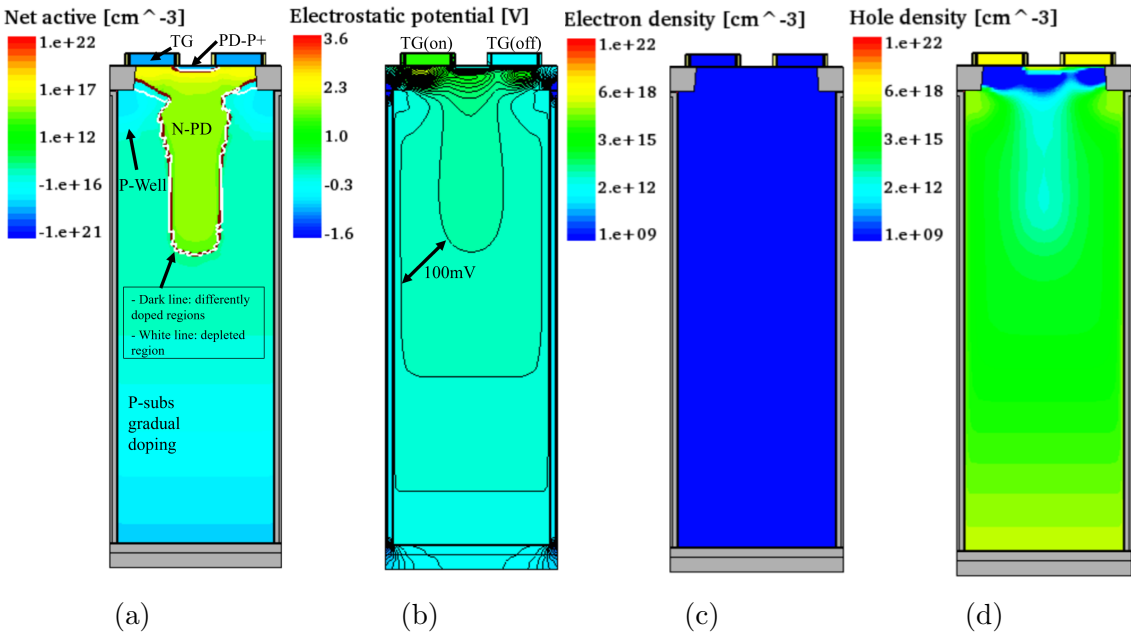


Figure 2.14: 2D cross-section of the 3D simulated PPD iToF pixel introduced in Fig. 2.13. (a) The different implants are identified in the net active concentration cross-section. Additionally a brown line is plotted for the separation of the differently doped zones and a white line is plotted for the delimitation of the depleted region. (b) The electrostatic potential distribution is plotted with equipotential lines at each 100mV. The sensing nodes SN_1 and SN_2 are biased at $2.2V$, the transfer gates TG_1 and TG_2 are biased respectively at $1.2V$ and $0V$ and grounds GND is biased at $0V$. Furthermore, (c) the 2D electron and (d) concentration distributions are also plotted. The electron and the hole concentration low limit is set to $10^9 cm^{-3}$. At this threshold the silicon is already significantly depleted for the doping concentration values used in the simulation.

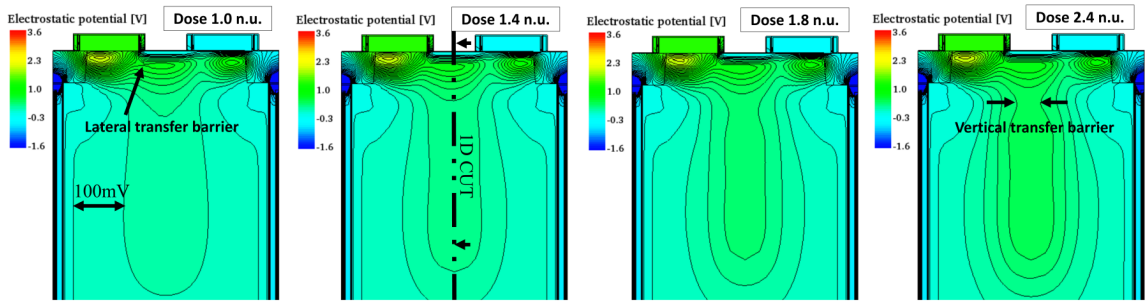


Figure 2.15: 2D cross-section over the 3D simulated structure depicted in Fig. 2.13 showing the electrostatic potential distribution for different N-PD implant doses. A 1D cut is identified at the center of the PD.

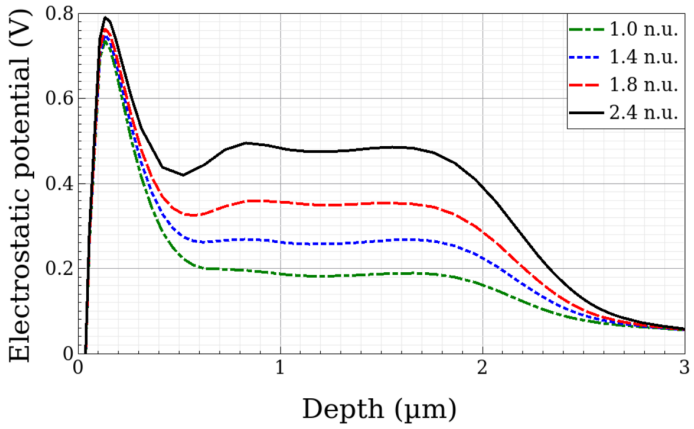


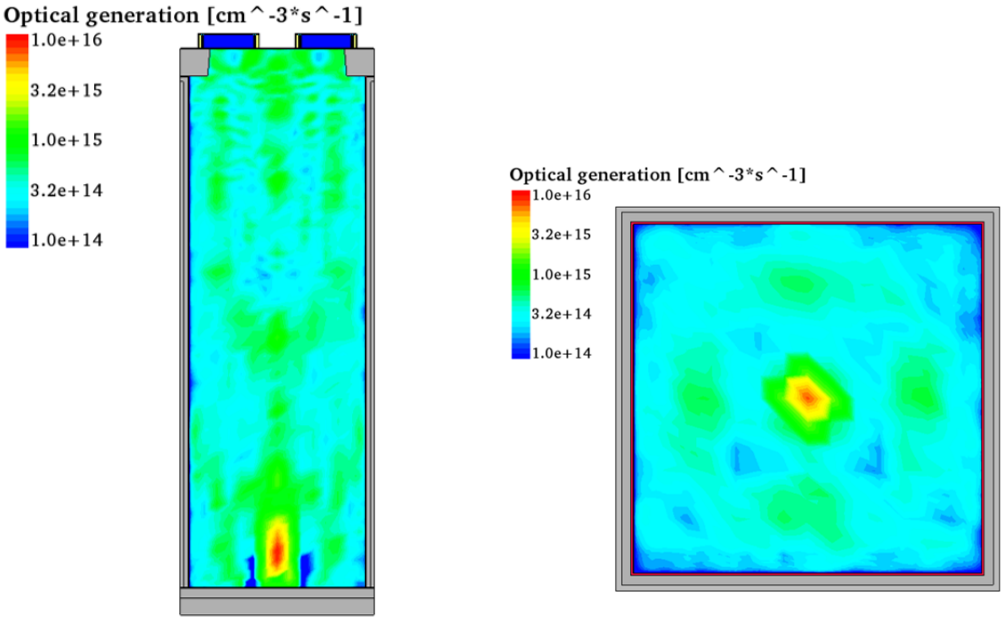
Figure 2.16: 1D cross-section over the different simulated structures with a sweep of the N-PD implant dose. The corresponding 1D cut line is depicted in Fig. 2.15.

In conclusion, the electrostatic potential distribution analysis is an important tool in the optimization of iToF pixel process and electrical parameters, such as implant doses and pixel biasing potentials. The computation requirements for solving Poisson's equation are much lower than the requirements for computing the continuity equation. Hence, the potential distribution computation is a fast method for a preliminary evaluation of the transfer efficiency. However, to model iToF pixels and to obtain predictive simulation results that can be compared to measured results, the computation of the electric potential distribution is not sufficient. Indeed, it is not possible to measure the electrostatic potential value at all points of a fabricated device the same way it is done in simulation. Because of that, a drift-diffusion-based-TCAD simulator combined with the modeling of the iToF pixel was used to simulate the key figures of merit of iToF pixels. This is the chosen approach to study new iToF solutions and the complete TCAD simulation methodology developed is described in the following sections.

2.3.3 Optical generation

The key figure of merit for the optical generation is the quantum efficiency, i.e. the total measured charges over incident photons [77].

It can be simulated with available commercial optical simulation FDTD tools [71]. Thicker absorption layers are used to increase sensitivity in near infra red (NIR). However, with a thicker layer, light is absorbed farther from sensing nodes, increasing their path before collection. To obtain an accurate simulation of carrier transfer times in a drift-diffusion-based-TCAD, the photogeneration map is first computed using an optical FDTD simulator. This map is then imported to the TCAD. As the electron transfer time will depend on where they are photogenerated, by using this method, an accurate DMC simulation can be obtained [77]. Fig. 2.17 shows a cut of the photogeneration distribution in the volume of the pixel interpolated with a structure simulated in drift-diffusion-based-TCAD.



(a) (b)

Figure 2.17: Lumerical generation imported at drift-diffusion-based-TCAD simulated pixel structure (a) cutting plane transversal to the transfer gates and (b) cutting plane parallel to transfer gates.

The percentage of collected charges in electrical simulation multiplied by the absorbed light power in FDTD simulation gives the QE value. It will be often the case that all the photogenerated charges imported in the electrical simulation will be collected by the sensing nodes. Because of that, the percentage of light power absortion computed in optical simulatied may give an estimation of QE.

It must be noted that in the optical simulation, silicon is considered to be intrinsic. The impact of doping defects on the scattering of light in the NIR at 940nm is small

for doping values inferior to 10^{19} $cm^{-}3$ [67, 78]. Furthermore, only an insignificant part of light reaches the highly doped zones on the top of the pixel, where SN N+ and ground P+ implanted zones are situated. This is observed in the cross-section in Fig. 2.17a. Hence, the doping concentration has no significant impact on QE, as well as on the photogeneration distribution map. The simulated impulsion signal imported in the electrical simulation is plotted in Fig. 2.18a.

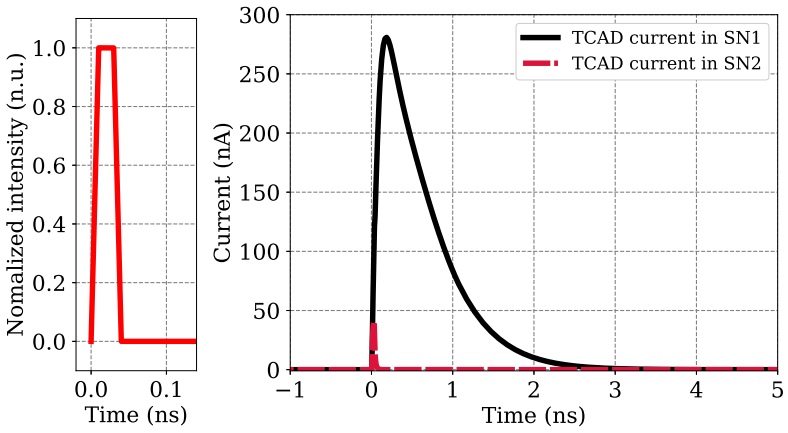
2.3.4 Transfer efficiency

Demodulation contrast (DMC) is a metric used to quantify the transfer efficiency of photogenerated charges inside a pixel. In DC operation, it depends only on how the charges are distributed between the sensing nodes. More often, another figure of merit similar to the DMC_{DC} is used to quantify the transfer efficiency. That is the parasitic light sensitivity (PLS) and it refers to the percentage of the photogenerated charges that are unintentionally collected in sensing nodes. Alternatively, the percentage of the signal that is detected in a sensing node whose respective TG is deactivated.

An efficient transfer implies that the electrostatic barrier of a closed TG, is significant enough to prevent the collection of any charges during transfer. Charge distribution as well as charge transfer in time can be observed by studying the impulse response of the pixel under biasing [77]. The methodology used consists of simulating the pixel response to a short light pulse. In simulation it corresponds to an impulse of optical generation applied to the volume of the pixel (Fig.2.18a). The actual distribution of photogenerated charges is imported in drift-diffusion-based technology computed-aided design (TCAD) simulation (Fig. 2.17). This is done for a biasing condition where the TG_1 is on and the TG_2 is off. The obtained current response is shown in Fig. 2.18b. A small percentage of the signal is collected in SN_2 immediately after the impulse. This PLS value is solely due to charges that are photogenerated directly in the collection site.

In AC and with frequency dependency, DMC is dependent on the transit time (TrT). TrT is defined by equation (1.24) and it represents the expected transfer time value or average transfer time of the measured charges. The collected charge flux in time corresponds to the current versus time ($i(t)$).

A value ranging from 0% to 100% can be obtained, which reflects the capability of a pixel to reproduce the received light signal with modulation frequency f_{Mod}. A DMC of 100% indicates that a pixel illuminated with a sinus of A_{pp} peak-to-peak amplitude and B offset will be able to reconstruct a sinus with optimum amplitude and offset. The corresponding DMC computed curve for the simulated response in Fig. 2.18 is plotted versus the frequency in Fig. 2.19.



(a) (b)

Figure 2.18: (a) Drift-diffusion-based-TCAD impulse light generation with normalized intensity. The photogeneration probability map is a, constant in time, 3D map with the light power absorbed in the volume of the pixel. It is computed with the FDTD optical simulator and it is imported in TCAD for the duration of the impulsion. The impulsion magnitude is a result of the photogeneration density integrated in the volume of the pixel. (b) The current response is obtained from the photogenerated charge distribution between sensing nodes SN_1 and SN_2.

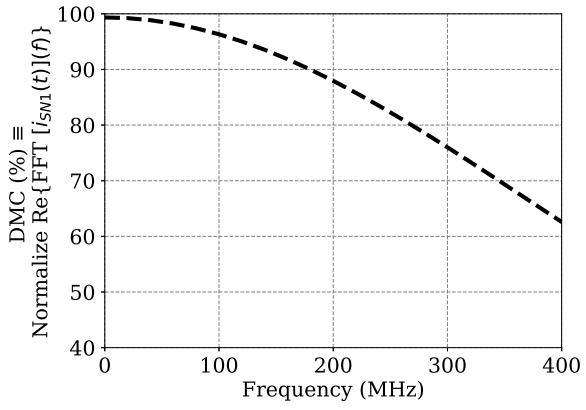


Figure 2.19: Normalized fast-Fourier-transform of current impulse response simulated with drift-diffusion-based-TCAD versus frequency. The obtained response is the DMC computed as described in section 1.5.1

2.4 TCAD versus measurements

Fabricated iToF pixels were simulated using commercial Poisson equation and transient drift-diffusion TCAD simulators. The transfer efficiency figures of merit computation methodology was depicted in section 2.3.4. The obtained value of PLS in simulation is equals to 0.4% and it matches the measured PLS value. The PLS is the charge percentage measured in SN_2 for time $t \to +\infty$. However, here it also corresponds to the percentage of charges that are directly photogenerated in the zone of the sensing node.

The current signal in SN_1 can then be exploited to extract the demodulation contrast in frequency as described in section 1.5.1.

In Fig 2.20 it is shown that, after calibration, the drift-diffusion-based-TCAD results match significantly with the measured results versus temperature. It is important to note that TCAD simulated process has been calibrated to match drift-diffusion-based-TCAD DMC values with measured results. The non-calibrated process results are also presented in Fig. 2.20. The calibration consists in a factor applied to the dose used in the simulated photodiode implants.

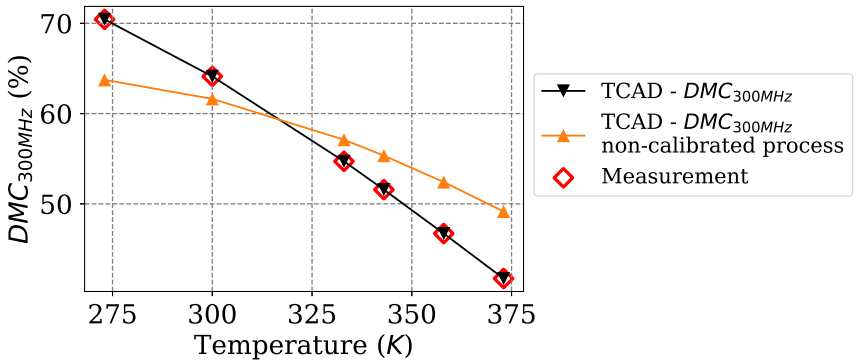


Figure 2.20: DMC at $300MHz$ versus temperature for drift-diffusion-based-TCAD simulations comparison with measured results.

Conclusion

A complete multiphysics methodology was developed for the simulation of iToF pixels. The simulation methodology uses TCAD process, drift-diffusion-based-TCAD electrical simulation and lumerical FDTD optical simulation to compute the key iToF figures of merit.

The key simulated figures of merit are power consumption, DMC, PLS and QE. Power consumption can be simulated by using AC-analysis TCAD simulation to compute the equivalent capacitor that is charged and discharged between cycles (see section 1.5). As all charges photogenerated inside the pixel are collected by the sensing nodes, QE can be computed by simulating the light power absorption inside of the pixel silicon volume with lumerical FDTD. In contrast, DMC and PLS require the development of dedicated simulation routines.

Firstly, a qualitative evaluation can be done with the electric potential distribution computation. 2D cross-sections where depicted to illustrate the transfer efficiency relation to the electric potential distribution inside of the pixel volume. Finally, transient drift-diffusion-based-TCAD simulations are used for the computation of DMC. Through the coupling of TCAD electrical simulation with lumerical FDTD light absorption maps, the pixel current response is simulated. From the obtained current response, predictive DMC values can be computed. The DMC values were extensively compared to measurements. The methodology reproduces significantly the DMC measured results after process simulation calibration.

The used methodology is limited to the simulation of deterministic figures of merit. The non deterministic figures of merit such pixel non-uniformity and depth non-uniformity are approached in the next chapter through the use of a MC simulator.

References

[3] M. Bigas, E. Cabruja, J. Forest, and J. Salvi. "Review of CMOS image sensors". In: *Microelectronics Journal* 37.5 (2006), pp. 433–451. DOI: https://doi.org/10.1016/j.mejo.2005.07.002.

[6] Brett E. Bouma and Guillermo J. Tearney. *Handbook of Optical Coherence Tomotraphy*. 2002.

[7] Bahaa Saleh and Malvin Teich. *Fundamentals of Photonics*. 2007.

[8] Fabrizio De Nisi. "A novel CMOS sensor for position detection". In: *Proceedings of IEEE Sensors* 2 (2003), pp. 1277–1282.

[9] Fabrizio De Nisi. "A CMOS sensor optimized for laser spot-position detection". In: *Proceedings of IEEE Sensors* 5 (2005), pp. 1296–1304.

[10] Robert Lange. "3D Time-of-Flight Distance Measurement with Custom Solid-State Image Sensors in CMOS/CCD-Technology". In: *Sensors Peterborough NH* 222 (2000), p. 223.

[11] Robert Lange and Peter Seitz. "Solid-state time-of-flight range camera". In: *IEEE Journal of Quantum Electronics* 37.3 (2001), pp. 390–397. DOI: 10.1109/3.910448.

[12] Boris Rodrigues. "Développement d ' un pixel innovant de type temps de vol pour des capteurs d ' image 3D-CMOS". In: *THESE de DOCTORAT DE L'UNIVERSITE DE LYON* (2018).

[13] R. Lange, S. Böhmer, and B. Buxbaum. "11 - CMOS-based optical time-of-flight 3D imaging and ranging". In: *High Performance Silicon Imaging (Second Edition)*. Ed. by Daniel Durini. Second Edition. Woodhead Publishing Series in Electronic and Optical Materials. Woodhead Publishing, 2020, pp. 319–375. DOI: https://doi.org/10.1016/B978-0-08-102434-8.00011-8.

[14] Jason Geng. "Structured-light 3D surface imaging: a tutorial". In: *Advances in Optics and Photonics* 3 (2011), pp. 128–160. DOI: 10.1364/AOP.3.000128.

[15] Kota Ito. "A Back Illuminated 10um SPAD Pixel Array Comprising Full Trench Isolation and Cu-Cu Bonding with Over 14% PDE at 940nm". In: (2020), pp. 16.6.1–16.6.4. DOI: 10.1109/iedm13553.2020.9371944.

[16] Yuichi Kato. "320x240 Back-Illuminated 10-um CAPD Pixels for High-Speed Modulation Time-of-Flight CMOS Image Sensor". In: *IEEE Journal of Solid-State Circuits* 53.4 (2018), pp. 1071–1078. DOI: 10.1109/JSSC.2018.2789403.

[17] Min-Sun Keel. "A 4-tap 3.5um 1.2Mpixel indirect time-of-flight CMOS image sensor with peak current mitigation and multi-user interference cancellation". In: *IEEE International Solid-State Circuits Conference, ISSCC* (2021), pp. 106–108. DOI: 10.1109/ISSCC42613.2021.9365854.

[18] Cedric Tubert. "4.6um Low Power Indirect Time-of-Flight Pixel Achieving 88.5% Demodulation Contrast at 200MHz for 0.54MPix Depth Camera". In: *ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference, Proceedings* (2021), pp. 135–138. DOI: 10.1109/ESSCIRC53450.2021.9567878.

[19] American National Standard for Safe Use of Lasers. *Laser Institute of America*. Version ANSI Z136.1-2014 revision of ANSI Z136.1-2007. 2014.

[20] Sergey Velichko. "Overview of CMOS Global Shutter Pixels". In: *IEEE Transactions on Electron Devices* 69.6 (2022), pp. 2806–2814. DOI: 10.1109/TED.2021.3136148.

[21] M. Wany and G.P. Israel. "CMOS image sensor with NMOS-only global shutter and enhanced responsivity". In: *IEEE Transactions on Electron Devices* 50.1 (2003), pp. 57–62. DOI: 10.1109/TED.2002.807253.

[22] Qian Zhang and Zhongjie Guo. "An 8T global shutter pixel with extended output range for CMOS image sensor". In: *2019 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*. 2019, pp. 1–3. DOI: 10.1109/EDSSC.2019.8754501.

[23] Chen Xu. "5.1 A Stacked Global-Shutter CMOS Imager with SC-Type Hybrid-GS Pixel and Self-Knee Point Calibration Single Frame HDR and On-Chip Binarization Algorithm for Smart Vision Applications". In: *2019 IEEE International Solid-State Circuits Conference - (ISSCC)*. 2019, pp. 94–96. DOI: 10.1109/ISSCC.2019.8662441.

[24] K. Ito. "A Back Illuminated 10µm SPAD Pixel Array Comprising Full Trench Isolation and Cu-Cu Bonding with Over 14% PDE at 940nm". In: *2020 IEEE International Electron Devices Meeting (IEDM)*. 2020, pp. 16.6.1–16.6.4. DOI: 10.1109/IEDM13553.2020.9371944.

[25] Edward Van Sieleghem. "A Backside-Illuminated Charge-Focusing Silicon SPAD With Enhanced Near-Infrared Sensitivity". In: *IEEE Transactions on Electron Devices* 69.3 (2022), pp. 1129–1136. DOI: 10.1109/TED.2022.3143487.

[26] Henna Ruokamo, Lauri W. Hallman, and Juha Kostamovaara. "An 80x25 Pixel CMOS Single-Photon Sensor With Flexible On-Chip Time Gating of 40 Subarrays for Solid-State 3-D Range Imaging". In: *IEEE Journal of Solid-State Circuits* 54.2 (2019), pp. 501–510. DOI: 10.1109/JSSC.2018.2878816.

[27] Ward Van Der Tempel. "A 1k-pixel 3D CMOS sensor". In: *Proceedings of IEEE Sensors* (2008), pp. 1000–1003. DOI: 10.1109/ICSENS.2008.4716611.

[28] Andreas Süss. "Benchmarking time-of-flight based depth measurement techniques". In: *Smart Photonic and Optoelectronic Integrated Circuits XVIII*. Ed. by Sailing He, El-Hang Lee, and Louay A. Eldada. Vol. 9751. International Society for Optics and Photonics. SPIE, 2016, p. 975118. DOI: 10.1117/12.2212478.

[29] Donguk Kim. "Indirect Time-of-Flight CMOS Image Sensor With On-Chip Background Light Cancelling and Pseudo-Four-Tap/Two-Tap Hybrid Imaging for Motion Artifact Suppression". In: *IEEE Journal of Solid-State Circuits* 55.11 (2020), pp. 2849–2865. DOI: 10.1109/JSSC.2020.3021246.

[30] Yuhi Yorikado. "Tap mismatch mitigation of 3 um 2-tap pixels of indirect Time-of-Flight image sensor for high-speed depth mapping". In: *Proceedings of the 2023 International Image Sensor Workshop (IISW)* (2023).

[31] Congzhen Hu. "Compact Numerical Modeling of Indirect Time-of-Flight CMOS Image Sensors". In: *IEEE Transactions on Electron Devices* 69 (2022), pp. 6897–6903.

[32] Donguk Kim. "5.4 A Dynamic Pseudo 4-Tap CMOS Time-of-Flight Image Sensor with Motion Artifact Suppression and Background Light Cancelling Over 120klux". In: *2020 IEEE International Solid-State Circuits Conference - (ISSCC)*. 2020, pp. 100–102. DOI: 10.1109/ISSCC19947.2020.9063101.

[33] Simone Bellisai. "Single-photon pulsed-light indirect time-of-flight 3D ranging". In: *Optics Express* 21 (2013), pp. 5086–5098. DOI: 10.1364/OE.21.005086.

[34] Simon Sze. *Physics of Semiconductor Devices*. ser. Wiley-Interscience publication. John Wiley and Sons, 1981.

[35] Moustafa El Kurdi, Guy Fishman, Sébastien Sauvage, and Philippe Boucaud. "Band structure and optical gain of tensile-strained germanium based on a 30 band k·p formalism". In: *Journal of Applied Physics* 107.1 (2010).

[36] Chenming Calvin Hu. 2009.

[37] SDevice. *Sentaurus Device User Guide*. Version S-2021.06. 2021.

[38] Eric R. Fossum and Donald B. Hondongwa. "A Review of the Pinned Photodiode for CCD and CMOS Image Sensors". In: *IEEE Journal of the Electron Devices Society* 2.3 (2014), pp. 33–43. DOI: 10.1109/JEDS.2014.2306412.

[39] M. Furumiya. "High sensitivity and no-cross-talk pixel technology for embedded CMOS image sensor". In: *International Electron Devices Meeting 2000. Technical Digest. IEDM (Cat. No.00CH37138)*. 2000, pp. 701–704. DOI: 10.1109/IEDM.2000.904415.

[40] Y. Hagiwara. "High-density and high-quality frame transfer CCD imager with very low smear, low dark current, and very high blue sensitivity". In: *IEEE Transactions on Electron Devices* 43.12 (1996), pp. 2122–2130. DOI: 10.1109/16.544383.

[41] Li Weiping. "Collection efficiency and charge transfer optimization for a 4-T pixel with multi n-type implants". In: *Journal of Semiconductors* 32.12 (2011), p. 124008. DOI: 10.1088/1674-4926/32/12/124008.

[42] Danil Van Nieuwenhove. "Photonic Demodulator With Sensitivity Control". In: *IEEE Sensors Journal* 7.3 (2007), pp. 317–318. DOI: 10.1109/JSEN.2006.890164.

[43] Cristine Jin Estrada. "Physical Model of Current-Assisted Photonic Demodulator (CAPD) for Time-of-Flight CMOS Image Sensor". In: *IEEE Transactions on Electron Devices* 67.7 (2020), pp. 2825–2830. DOI: 10.1109/TED.2020.2995349.

[44] N Na, S-L Cheng, H-D Liu, M-J Yang, C-Y Chen, K-C Chu, H-W Chen, Y-T Chou, C-T Lin, W-H Liu, et al. "Proposal and demonstration of germanium-on-silicon lock-in pixels for indirect time-of-flight based three-dimensional sensing". In: *arXiv preprint arXiv:1806.07972* (2018).

[45] Edge AI Vision. *Why the Sony IMX570 is the Leading iTOF Sensor*. 2023. URL: https://www.edge-ai-vision.com/2023/04/why-the-sony-imx570-is-the-leading-itof-sensor/ (visited on 04/15/2023).

[46] Markus Dielacher. "Advancements in indirect Time of Flight image sensors in front side illuminated CMOS". In: *European Solid-State Device Research Conference* 2021-Septe.1 (2021), pp. 139–142. DOI: 10.1109/ESSDERC53440.2021.9631809.

[47] Tampon Inventor. "Tampon patent to be replaced with BDTI if i can mention it". Pat. mzeltkazntest.

[48] François Roy. "Fully Depleted, Trench-Pinned Photo Gate for CMOS Image Sensor Applications". In: *Proceedings of IEEE Sensors* (2020).

[49] John Scott-Thomas. "Trends and Developments in State-of-the-Art CMOS Image Sensors". In: *Proceedings of the Int'l Image Sensor Workshop (IISW), Crieff, UK*. 2023.

[50] Sungsoo Choi. "World smallest 200Mp CMOS image sensor with 0.56 μm pixel equipped with novel deep trench isolation structure for better sensitivity and higher CG". In: *Proceedings of the Int'l Image Sensor Workshop (IISW), Crieff, UK*. 2023, pp. 22–25.

[51] Jungbin Yun. "A 0.6 µm Small Pixel for High Resolution CMOS Image Sensor with Full Well Capacity of 10,000e- by Dual Vertical Transfer Gate Technology". In: *2022 IEEE Symposium on VLSI Technology and Circuits*. 2022, pp. 351–352. DOI: 10.1109/VLSITechnologyandCir46769.2022.9830254.

[52] Sungbong Park. "A 64Mpixel CMOS Image Sensor with 0.56µm Unit Pixels Separated by Front Deep-Trench Isolation". In: *2022 IEEE International Solid-State Circuits Conference (ISSCC)*. Vol. 65. 2022, pp. 1–3. DOI: 10.1109/ISSCC42614.2022.9731750.

[53] C.-L. Chen. "5.3 An Up-to-1400nm 500MHz Demodulated Time-of-Flight Image Sensor on a Ge-on-Si Platform". In: *2020 IEEE International Solid-State Circuits Conference - (ISSCC)*. 2020, pp. 98–100. DOI: 10.1109/ISSCC19947.2020.9063107.

[54] Y. Kumagai. "Back-Illuminated 2.74 µm-Pixel-Pitch Global Shutter CMOS Image Sensor with Charge-Domain Memory Achieving 10k e-Saturation Signal". In: *2018 IEEE International Electron Devices Meeting (IEDM)*. 2018, pp. 10.6.1–10.6.4. DOI: 10.1109/IEDM.2018.8614676.

[55] Seung-Sik Kim. "3-Layer Stacked Voltage-Domain Global Shutter CMOS Image Sensor with 1.8µm-Pixel-Pitch". In: *2022 International Electron Devices Meeting (IEDM)*. 2022, pp. 37.5.1–37.5.4. DOI: 10.1109/IEDM45625.2022.10019515.

[56] Geunsook Park. "A 2.2µm stacked back side illuminated voltage domain global shutter CMOS image sensor". In: *2019 IEEE International Electron Devices Meeting (IEDM)*. 2019, pp. 16.4.1–16.4.4. DOI: 10.1109/IEDM19573.2019.8993606.

[57] Boris Rodrigues. "Indirect ToF pixel integrating fast buried-channel transfer gates and gradual epitaxy and enabling CDS". In: *Proc. IISW* (2017), pp. 266–269.

[58] Yoshiki Ebiko. "Low power consumption and high resolution 1280X960 Gate Assisted Photonic Demodulator pixel for indirect Time of flight". In: *International Electron Devices Meeting, IEDM* (2020). DOI: 10.1109/IEDM13553.2020.9372109.

[59] Xiaolin Shi, Jiangtao Xu, Kaiming Nie, and Zhiyuan Gao. "A Low kTC Noise and Low FPN Reset Method for Pixel in ToF Image Sensor". In: *IEEE Sensors Journal* 22.3 (2022), pp. 2053–2061. DOI: 10.1109/JSEN.2021.3135348.

[60] E Oran Brigham. "The Fast Fourier Transform Prentice-Hall". In: *Englewood Cliffs, NJ* 19742 (1974).

[61] Texas Instruments. *CMOS Power Consumption and C pd Calculation*. Version SCAA035B, June, 1997, [Online]. 1997.

[62] Ramjee Prasad. *Analog and Digital Electronic Circuits: Fundamentals, Analysis, and Applications*. Springer Nature, 2021.

[63] Jaehyung Jang. "An Ultra-low current operating 5-µm Vertical Field Modulator Pixel for in-direct Time of Flight 3D Sensor". In: *2020 International Image Sensor Workshop (IISW)*. 2020.

3 - Monte Carlo simulation methodology

Introduction

Standard TCAD modeling offers an efficient, accurate, and well-tested method for extracting the various figures of merit of the iToF pixel [77]. A simulation methodology similar to the one presented by Mugny et al. [77] was developed in Chapter 2. However, this method is fully deterministic and cannot provide access to statistical quantities. Although iToF pixels are not single-event detectors like SPAD devices, their operation relies on a limited number of events. These events are the different charge trajectories, starting at the position where the charges are photogenerated in the volume of the pixel and ending at the position of the sensing node where they are collected. Therefore, a statistical simulation of iToF can provide insights into the device stochastic behavior.

The statistical treatment of carrier transport in semiconductor devices has mostly been studied through Monte Carlo (MC) methods. In such methods, charge particles are treated individually. The particle trajectories are determined by a stochastic selection of events, based on their occurrence probabilities. The events probabilities can be derived from physical or empirical models and may allow to reproduce on average the bulk mobility of the material studied. The reference method relies on the semi-classical approach, where the particle motion is solved in both real and momentum spaces, with a classical treatment of the real space and a quantum treatment of the momentum space [79]. The real space describes the position of the particles and the reciprocal momentum space their phase. Although accurate, these approaches are usually of extensive numerical computation, especially when the electronic structure is described with full-band models over the entire Brillouin zone. Hence, they are not suitable for long simulations that require a large number of statistical data.

Different approaches have been proposed to reduce the computation time of the standard methods [80, 81]. The "Advection-Diffusion Monte Carlo" (ADMC) approach has been used in this work [81]. This method interprets the standard drift-diffusion-based-TCAD equations as Fokker-Planck equations applied to spatial probability density of electrons. The Fokker-Planck equations are partial differential equations that describe the time evolution of the probability density function of a particle velocity. These equations are solved with a particle MC approach, providing a new stochastic method to compute the particle trajectory [79, 81].

The random dynamic of the drift-diffusion equation, can be described by the random movement of a particle as Fokker-Planck equations. In equation (3.1), the position of the particle becomes a probability state function X in time t. In the algorithm the successive positions are given by the increment of i with the corresponding time t_i. The position $X(t_i)$ is the sum of two components. (i) $X(t_i)$ has a drift component, that is the velocity of the particle. The velocity depends on the mobility of the particle μ_n, here an electron, times the electric field $\mathscr{E}$. (ii) $X(t_i)$ also has a diffusion factor $\mathscr{D}_n$, that depend on the electronic diffusion coefficient D through the equation $\mathscr{D}_n(X(t_i), t_i) = \sqrt{2 \cdot D(X(t_i), t_i)}$. $B(t_i)$ is a random variable describing the Brownian motion, i.e. random process describing a succession of infinitesimal random steps [79]. This random process follows a Gaussian law with variance t and may be described by a Fokker-Planck differential equation. Hence, $dB(t_i)$ also follows a Gaussian distribution and $Var\{dB(t_i)\} = dt$ [82].

$$dX(t_i) = \mu_n \cdot \mathscr{E}(X(t_i), t_i) \cdot dt + \mathscr{D}_n(X(t_i), t_i) \cdot dB(t_i) \tag{3.1}$$

3.1 MC modeling

The 3D MC code diagram is represented in Fig. 3.1. The main three blocks are identified and they are: (i) The initialization of the particle positions. (ii) ADMC in the form of a Markov chain algorithm for the resolution of the continuity equation. Each iteration of the Markov chain algorithm solves equation (3.1) for the step $i+1$ at the time t_{i+1} from the values of the step i at the time t_i. (iii) Finally, the counting of particles taking place at each iteration of the algorithm.

(i) The optical generation map simulated with lumerical FDTD is a four dimension map with three of the dimensions being the space coordinates (x, y and z) and the fourth dimension being the normalized power absorption. The optical generation is proportional to the light power absorption. Two dimension cross-sections of the photogeneration map are shown in Fig. 2.17. In the MC simulation, this photogeneration map is used as a probability density function (PDF). The total volume under a PDF, that is the total measure, is the total probability of all possible results of a trial. A result of a trial is called an outcome and all possible outcomes are called the measure of the PDF. In the case of the power absorption map, the volume under the PDF may be computed with the integral of the PDF over the three space coordinates (x, y and z). The integral of the simulated light power absorption in the pixel volume gives a normalization coefficient for a PDF optical generation to obtain a PDF with a measure equals one. After this normalization, four random numbers are generated. Three of them are coordinates for the position of the particle (r_{x_i}, r_{y_i} and r_{z_i}) and the fourth number is a probability value going from 0 to 1 (r_{ph_i}). This random probability value (r_{ph_i}) is compared with the PDF value at the corresponding coordinate of photogeneration $PDF(r_{x_i}, r_{y_i}, r_{z_i})$. If the r_{ph_i} is higher than the corresponding PDF value, a free electron is photogenerated. Else, the random numbers are regenerated until the condition for probability is satisfied. An image of statistical finite number of events of photogeneration is obtained in the volume of the

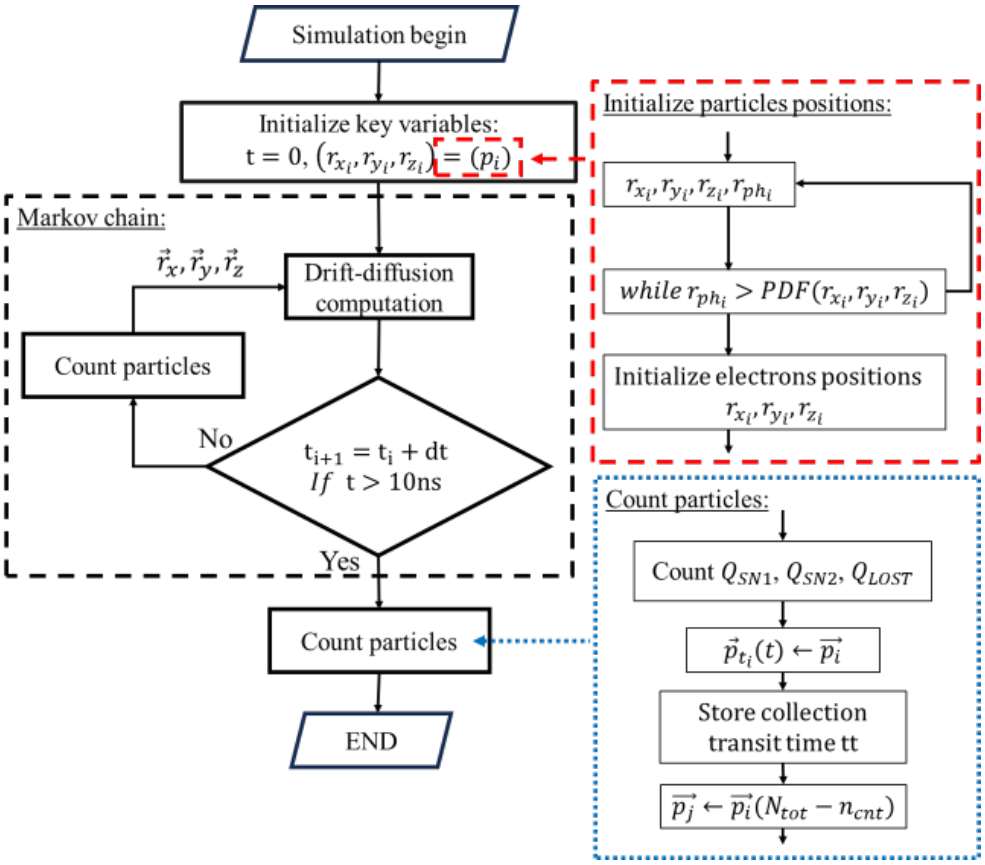


Figure 3.1: The diagram of the ADMC code for simulating the studied iToF pixel. Three main blocks are identified, they are: (i) the initialization of position of particle with photogeneration accounted for by a probability density function (PDF), (ii) the ADMC algorithm in the form of a Markov chain for the computation of the drift-diffusion equation and (iii) the counting particles function that identifies collected particles and their position.

pixel.

(ii) The stochastic transport of the electrons is computed through the "Advection-Diffusion Monte Carlo" (ADMC) method. This is an in-house code at STMicroelectronics solving equation (3.1) as presented by Helleboid et al. [81]. The doping concentration and electric field at the particle positions are interpolated to a 3D squared meshing grid using the data from the initial Poisson TCAD simulation. This meshing grid has a fixed distance meshing step in 3D equal δm. These data at the particle position may be used to compute the drift velocity and the random diffusion at each time step. However, a more accurate approach is to use the mobility map also obtained with TCAD, taking advantage of the different mobility degradation models available in the commercial simulator [37, 74].

(iii) At each iteration, particles are counted. The particle counting function identifies if one of the electrons is inside one of the designated areas with high N-type

doping concentration. If a charge reaches a zone with high N-type doping concentration it is collected. The total charge values Q_{SN_1}, Q_{SN_2} or Q_{LOST} increase with the charge collection, for free charges that are collected respectively in SN_1, SN_2 or zones where particles are lost. The particles that are lost, are electrons that are collected in the other different N+ diffusion zones inside of the pixel that happen to intercept a part of the photogenerated signal. Further information is stored during the counting of the particles in each iteration, such as the position of the particle for a given time.

Convergence studies have been carried out for the MC study of iToF pixels and they are shown in Fig. 3.2. The minimum time steps Δt and the spatial squared meshing Δm steps have been identified to obtain the convergence of the charge response obtained with the MC simulator. The time step convergence is obtained for a time step of $0.1ps$. Comparatively, the impulse of optical-generation used in time-resolved drift-diffusion TCAD simulation is of $40ps$.

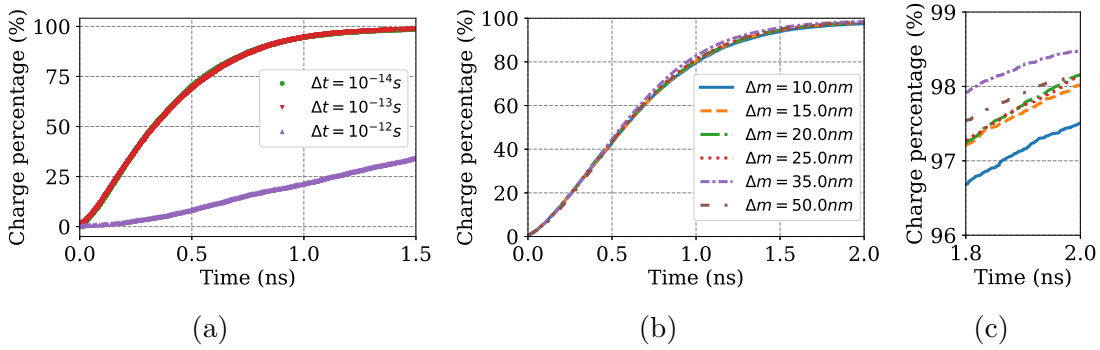
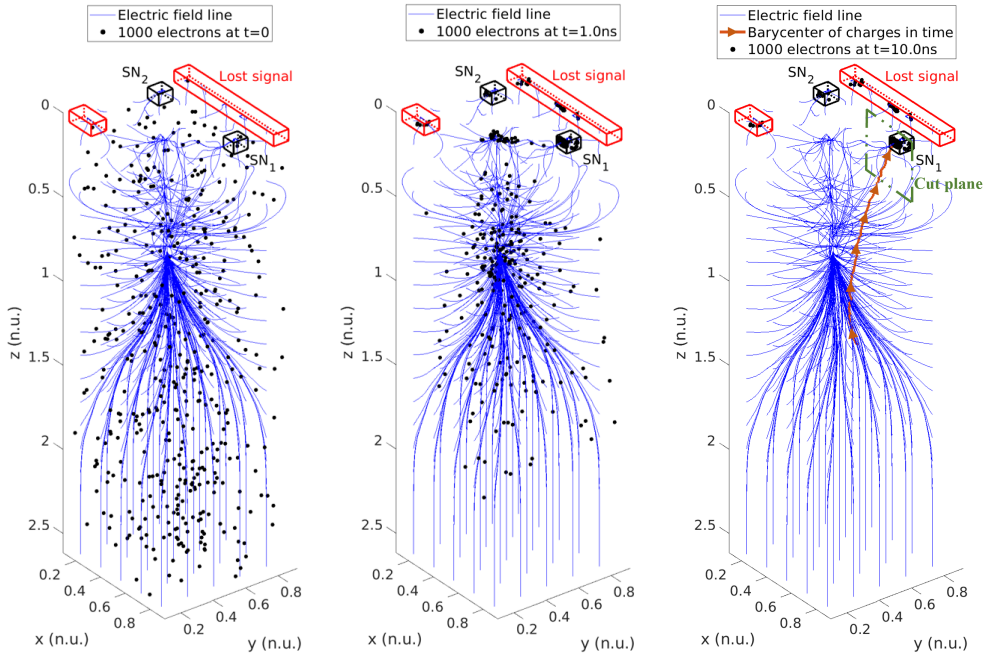


Figure 3.2: SN_1 charge response (a) time step Δt convergence, (b) 3D meshing step Δm convergence and (c) zoom different Δm curves showing the spatial meshing fast convergence.

3.2 MC versus TCAD

Comparison studies have been carried out to validate the MC modeling on the iToF pixel. An impulse of electrons was generated using an uniform probability density function of photogeneration in the silicon volume of the pixel. Fig. 3.3 shows the distribution of charges at three different times respectively at (a) 0s, (b) 1.0ns and (c) 10.0ns. This complete visualization allows to identify zones where the electrons drift or diffuse. The transport by the diffusion mechanism, often unwanted, can be caused by potential barriers or by smaller electric field regions, which affects the efficiency of the transfer. At Fig. 3.3c, a line is drawn with the barycenter of charges in time following the direction of the arrows. That is the average position of photogenerated charges in the volume. It starts in the center of the pixel just after photogeneration and reaches the top after all charges are collected.

To simplify the 3D mobility in the volume of the pixel, uniform mobility maps with constant values have been used. The simulated results for TCAD and MC

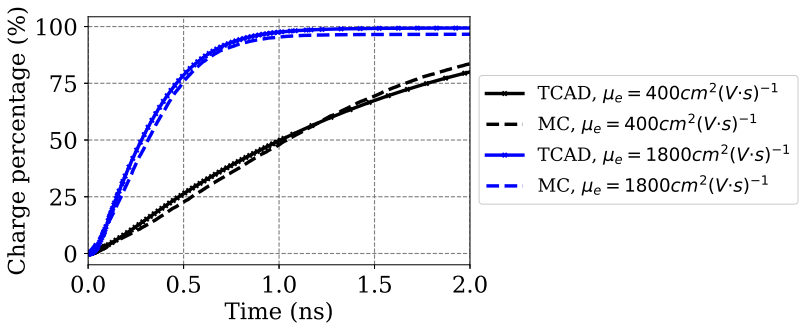


(a) (b) (c)

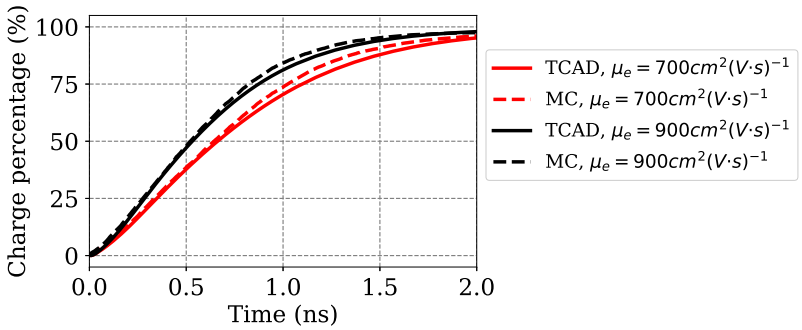
Figure 3.3: 3D plot of MC simulated particles in the volume of the pixel at different times: (a) 0, (b) 1.0ns and (c) 10.0ns. The electric field stream lines are plotted in blue. They are a result of the gradient of electrostatic potential obtained with TCAD Poisson equation computation. The collection zones for SN_1 and SN_2 are identified with black boxes and other N+ diffusion zones where signal is lost are identified with red boxes. Additionally in (c), the red line is the barycenter of charges at all times during the MC simulation. It starts at the center of the pixel and follows the direction of the arrow to end at the top off the pixels where charges are finally collected. Furthermore, a cut plane is identified in (c), it will be used for later plots.

are compared in Fig. 3.4. The obtained MC charge responses are for an impulse of 10,000 photogenerated electrons. A significant match is obtained for different constant mobility values.

A significant match is also obtained for TrT plotted versus the uniform mobility value shown in Fig. 3.5. The TrT is computed as described previously by equation (1.24) using the TCAD current impulse responses and the MC charge impulse responses. The transit time offset observed between MC and TCAD simulation is due to the difference in the time width of the light impulsion stimulus used in each one of the simulators. In MC, this impulsion stimulus is ideal, meaning that it is instantaneous and it has a time width equals zero. In contrast, for TCAD, the light impulsion signal has a time width larger than zero. The impulsion used in the TCAD simulator is depicted in Fig. 2.18a and it has a width of $40ps$. Furthermore, this larger width corresponds to the actual pulse width of the laser that will be used in the characterization of the sensor in the next section.



(a)



(b)

Figure 3.4: Charge transfer into SN_1 computed with MC versus TCAD with constant mobility.

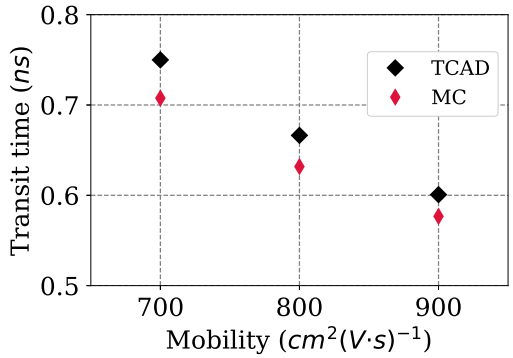


Figure 3.5: TCAD and MC obtained TrT for simulations with different uniform mobility values. TrT is computed with equation (1.24).

For the case of an electron mobility of $800cm^2 \cdot (V \cdot s)^{-1}$, different optical generation uniform distribution densities are compared in TCAD. The uniform distribution density is proportional to the photogeneration density in the volume of the pixel, changing the density of the uniform distribution consists in multiplying the uniform photo-generation value by a constant value. The obtained charge response is plotted in Fig. 3.6 for the different multiplication constant values. A change in the response is observed with increasing illumination intensity. This happens because when the illumination intensity density (I_{max}) is too strong, as in the case of the $10^2 n.u.$ (normalized unity) density response, a significant quantity of free charges are photogenerated, changing significantly the electrostatic potential in the volume of the pixel. The change in the electrostatic potential causes the response of the pixel to change as well. The difference in the electrostatic potential distribution is caused by the increase of the free electrons density according to the Maxwell-Gauss equation (2.7). For a smaller density of $10^{-2} n.u.$, the change to the free electron density distribution is irrelevant and the solution converges to a case where the photogenerated charges do not impact the electrostatic potential distribution of the system. A total of 19 electrons are photogenerated for the case with the I_{max} equals $10^{-}2 n.u.$. The TCAD response converges to the MC simulated charge response for the cases with a lower illumination coefficient. Indeed, the MC simulation electrostatic potential does not change with photogenerated electrons. The electrostatic potential distribution is simulated in TCAD and imported at the beginning of the MC simulation, it than remains constant for the remainder of the simulation. That way, it is possible to isolate a single phenomenum to identify the ideal response of the pixel to a photogenerated stimulus. For an example of a optimization study using MC see Annex 6.2.

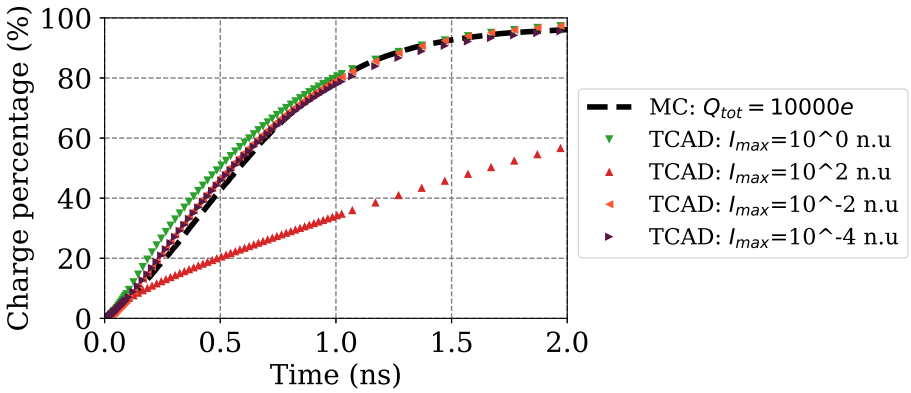


Figure 3.6: Charge response in SN_1 for different normalized illumination intensity density values (I_{max}) given in a normalized unity (n.u.). The convergence of TrT is observed for lower illumination, as there is no change in the electrical behavior of the low illumination intensity cases. Simulations are done with a constant mobility of $800cm^2(V \cdot s)^{-1}$.

3.3 MC & TCAD versus measurements

Fabricated iToF pixels were simulated using commercial Poisson equation and time-resolved drift-diffusion TCAD simulators (see section 2.1.2). The simulated 3D pixel maps for electrostatic potential, doping concentration and electron mobility were extracted and used as input to the ADMC simulator. A significant match is obtained between the integrated current response of TCAD and the charge response of MC. This response is plotted for SN_1 in Fig. 3.7a and for SN_2 in Fig. 3.7b. The simulation of the parasitic light sensitivity (PLS), that is the charge percentage measured in SN_2 for time $t \to +\infty$, is higher with the MC simulation. The difference in PLS between both simulation techniques remains unexplained but it is considered at the margin of the methodology precision.

The current detected in the sensing nodes is the time derivative of the charge collected in the sensing nodes. The obtained current curve is interpolated with a new time domain to reduce the number of points in time. The MC computed current signal is shown in Fig. 3.8 and it is compared with the TCAD simulated current signal. The current signal can then be exploited to extract the demodulation contrast versus the frequency as in section 1.5.1.

The result obtained with MC presented in Fig. 3.9 shows a slightly increasing mismatch with frequency when compared to the TCAD simulated results.

Nonetheless, when isolating DMC to a single frequency, MC simulator reproduces the tendency observed with TCAD. Fig. 3.10 shows the DMC versus temperature obtained with measurements, calibrated TCAD and MC simulation. A shift of 6% in DMC_{300MHz} is observed between measured and MC curves. It is important to note that TCAD simulated process has been calibrated to match the TCAD DMC values with measured results. The non-calibrated process results are also presented in Fig. 3.10. The mismatch of the DMC_{300MHz} of 6% corresponds to a transit time of $200ps$. This is higher than the previously depicted offset in Fig. 3.5 of the pulse width of $40ps$.

Another cause is identified for this increased mismatch in the transit time between the two simulators. Different electron mobility values are observed in TCAD depending on the concentration of free electron carriers. The electron density under the active transfer gate for a pixel just after reset in Fig. 3.11a is different from the electron density of the transfer gate during the photogeneration impulse in Fig. 3.11b.

The increase in the transit time happens because in simulation, the photogeneration impulse increases the density of free carriers significantly. Zones with higher electron density suffer from mobility degradation due to scattering of free ionized charges, which is considered by the IALMob mobility model [74]. The mobility cross-section over the transfer gate is shown in Fig. 3.11c for the lower electron concentration just after reset and in Fig. 3.11d for the higher electron concentration during the photogeneration impulse. Contrarily to the TCAD impulse response methodology, the electron mobility distribution in the pixel imported in MC is simulated with TCAD just after reset.

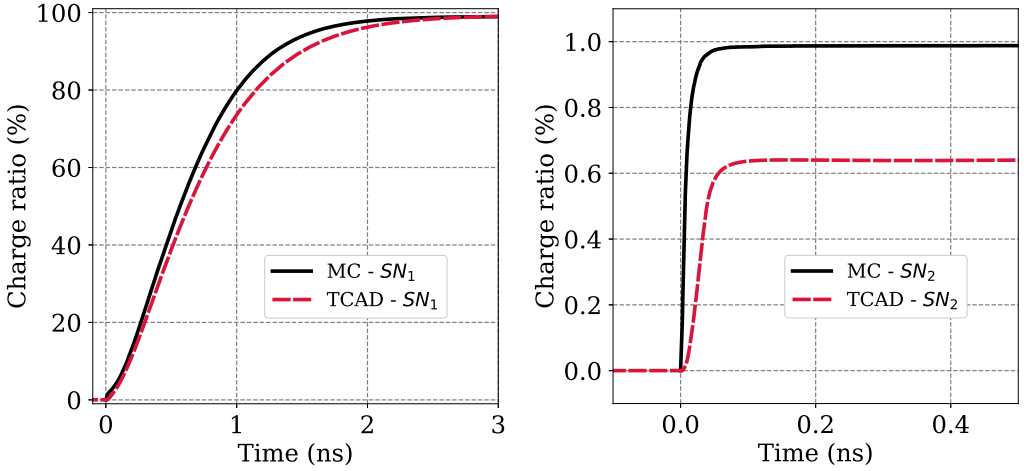


Figure 3.7: MC and TCAD simulated charge responses for (a) SN_1 and (b) SN_2.

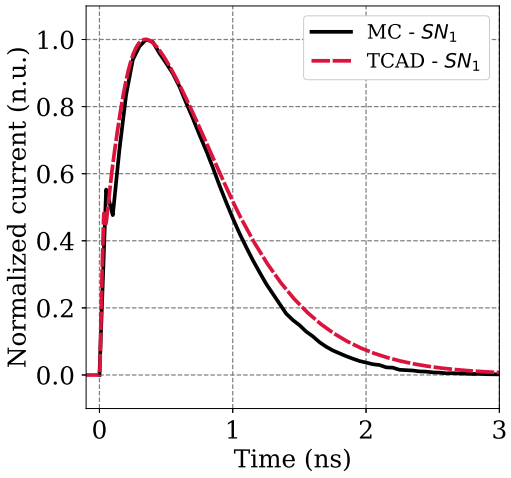


Figure 3.8: Current response at SN_1 obtained by differentiating the MC charge data in Fig. 3.7 compared with the current response simulated in TCAD.

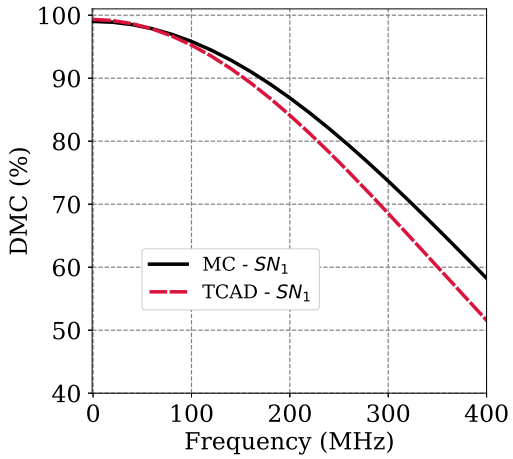


Figure 3.9: MC and TCAD computed DMC using the FFT of the current responses at SN_1 in Fig. 3.8.

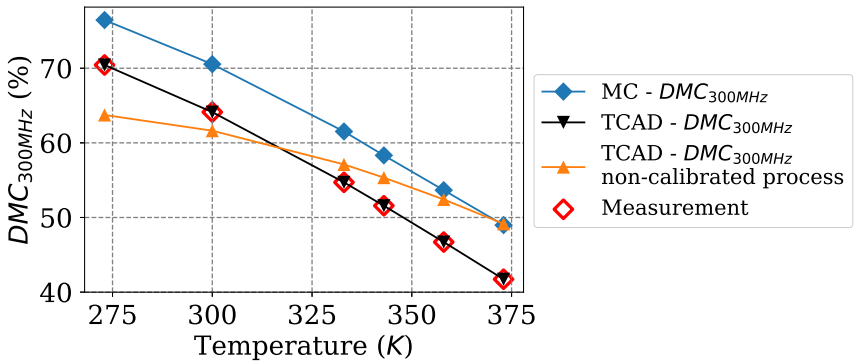


Figure 3.10: DMC at $300MHz$ versus temperature for MC and TCAD simulations comparison with measured results.

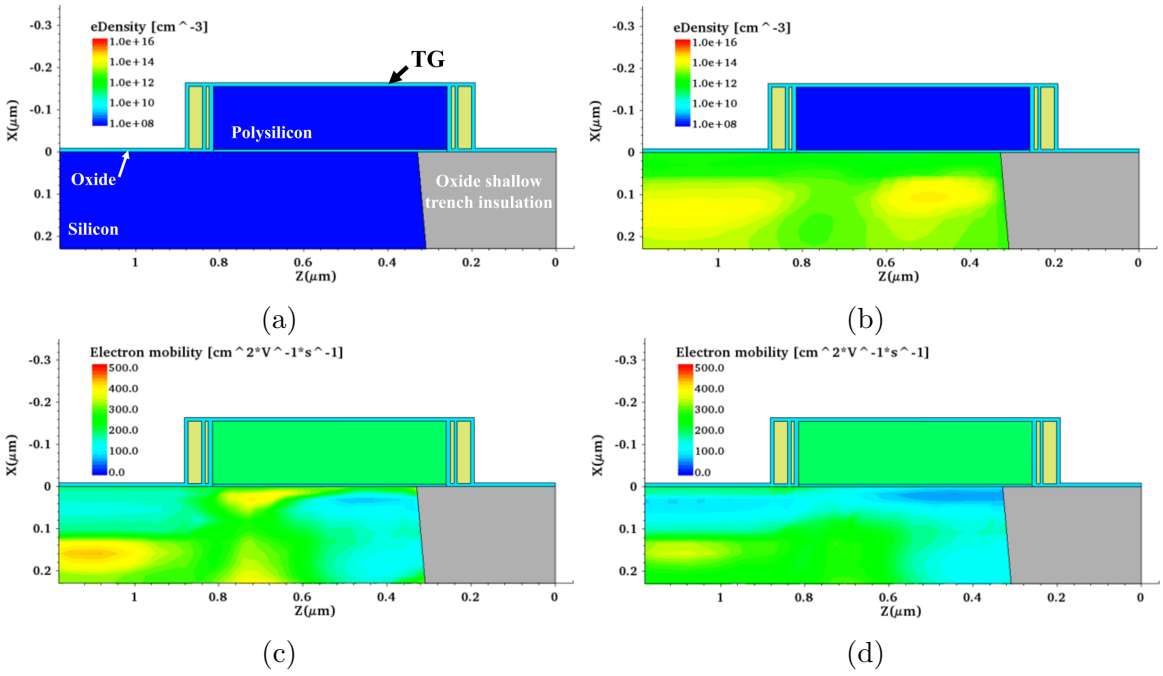


Figure 3.11: The cut plane depicted in Fig. 3.3c is used in TCAD to generate these images. The generated images are (a) the electron density under the active transfer gate for a pixel just after reset, (b) the electron density under the transfer gate during the photogeneration impulse, (c) the electron mobility under the transfer gate for the lower electron concentration just after reset and (d) the electron mobility for the higher electron concentration during the photogeneration impulse.

3.4 Statistical impact to the iToF technique

Non-uniformity in pixel response can be caused by various factors that can be either temporal or spatial [10]. The non-uniformity is related to statistical figures of merit such a pixel response non-uniformity (PRNU), that is intrinsically spatial and depth non-uniformity (DNU), that has a spatial and a temporal component. Spatial non-uniformity can be caused by the variability in the pixel matrix due to mismatches between each pixel, e.g. process and design variability. Temporal non-uniformity can occur due to changes in the pixel characteristics over time, such as changes in the sensitivity or the noise.

The total measurement error, σ_ϕ, is a function f of a time-related error, σ_t and a spatial error, σ_s, as indicated by equation (3.3) [30].

$$\sigma_\phi = \sqrt{\frac{\sum_{i=1}^{n}(\phi_i - \bar{\phi})^2}{n-1}} \tag{3.2}$$

$$\sigma_\phi = f(\sigma_t, \sigma_s) \tag{3.3}$$

3.4.1 Pixel response non-uniformity

PRNU is defined as the standard deviation of the measured signal in percentage [10, 83]. The different pixels inside a matrix are not identical. The variability is a consequence of (i) process and (ii) electrical aspects. (i) Namely process variations are differences in physical properties across surfaces, such as variations in the thickness or composition of the pixel layers. (ii) Examples of electrical variations are mismatches in the transfer gate threshold voltages or the biasing between pixels [31, 76]. Other factors that can contribute to non-uniformity include temperature variations, manufacturing defects, and variations in the illumination or viewing angle of the pixel.

PRNU is a DC figure of merit. That means it is intrinsically spatial and mainly dependent on the photogeneration dispersion. It is computed from the measured variance of the percentage of total collected signal ($\sigma^2_{\%}$) minus the variance of the charge signal in the dark (s^2_{dark}) [84]. Three independent contributions are distinguished in equation (3.4): (i) the variation due to the quantity and location of the photogenation of charges σ_{charge}, (ii) the variation due to the efficiency of transfer $\sigma_{transfer}$ and (iii) the variation due to the measurement artifacts σ_{offset}. This last value can be caused by the measurement conditions.

Despite the existing dark current compensation techniques to correct the response of the pixel with reference noise bias, the second order dark current variability σ_{dark} may also contributes to the measurement error [84, 85]. This value is mainly dependent on measurement condition parameters, such as the number of frames used for the acquisition, the illumination and the integration times.

$$PRNU = \sqrt{\sigma^2_{\%} - s^2_{dark}} = \sqrt{\sigma^2_{charge} + \sigma^2_{transfer} + \sigma^2_{offset}} \tag{3.4}$$

Even for a case where pixels are identical, the statistical variability of the charges photogeneration, transfer and collection is expected during operation. Supposing two identical pixels operating with the same conditions and consequently having the same number of photogenerated charges. The location of photogeneration or the charge distribution in SN_1 and SN_2 may be different. Hence, for iToF pixels, PRNU is strongly related to the standard deviation of PLS (σ_{PLS}).

It is shown in Fig. 2.18b that all charges reaching SN_2 (i.e. PLS) are collected directly after the optical generation impulse. Because of that, PLS in the studied pixel is considered to be entirely due to the charges photogenerated directly in the sensing node.

3.4.2 Depth non-uniformity

DNU on the other hand, takes into account the time measurement variance. There are two contributions to the depth error, the temporal error σ_t and the spatial error σ_s as described in equation (3.5). The correlation between the temporal and spatial errors is added to the expression $\rho_{t,s}$, despite being often neglected [30, 85]. The spatial variation is a consequence of mismatches in the matrix of pixels, i.e. doping and morphology variability between pixels. The time variation is due to the variance between measurements. It may occur if only a limited number of charges are transferred or a limited number of acquisitions, i.e. frames are averaged.

$$DNU(f_{Mod}) = \sqrt{\sigma_t^2 + \sigma_s^2 + \rho_{t,s}} \tag{3.5}$$

The measurement technique of DNU consists of computing the phase variance ($\sigma^2(\Delta\phi)$) in a matrix with a total of N pixels. From the phase variance, the time variance is computed as described in equation (3.6). The expression is divided by the modulation frequency (f_{Mod}) to change the phase value into a time value.

$$DNU_{meas}(f_{Mod}) = \sqrt{\frac{\sigma^2(\Delta\phi_i)}{2\pi f_{Mod}}} \tag{3.6}$$

The classical drift-diffusion-based TCAD simulators have limitations when considering the detection variability. To be able to extract further information that relies on statistical uncertainties such as PRNU and DNU, other approaches are envisaged. It is the case of MC simulation for the transport computation [79, 86].

The mobility map computed by the TCAD simulator can be imported in the MC simulation. Additionally, at the specific simulation time and position p_i, the particle (i.e. the free electron) will be subject to the electric field and the charge concentration, both values are computed with the TCAD Poisson simulator. However, the mobility map imported in the MC simulation will no longer evolve with a change in the charge concentration. The mobility change due to the charge concentration change in time, is only computed in TCAD.

3.4.3 MC simulation results

As discussed previously in Sec. 3.4.1, PRNU is a figure of merit that is intrinsically spatial. However, it is impacted by the magnitude of the measured signal [10, 83]. For a small quantity of the detected charges, the measurement error may not be neglected.

The 3D MC results were used to compute the charge percentage variability and the charge transfer expected transit time variability. The simulated particles were randomly partitioned in groups of the same size as shown schematically in Fig. 3.12. For each group the PLS and TrT values are computed. A distribution can be drawn by considering each group as a sample. For all samples of the same size the standard deviation of PLS and TrT values, respectively σ_{PLS} and σ_{TrT}, are computed.

In Fig. 3.13, the standard deviation of PLS (σ_{PLS}) is plotted versus the number of particles per sample. As the PLS is collected directly after photogeneration, $\sigma_{transfer} = 0$ and σ_{PLS} equals σ_{charge}.

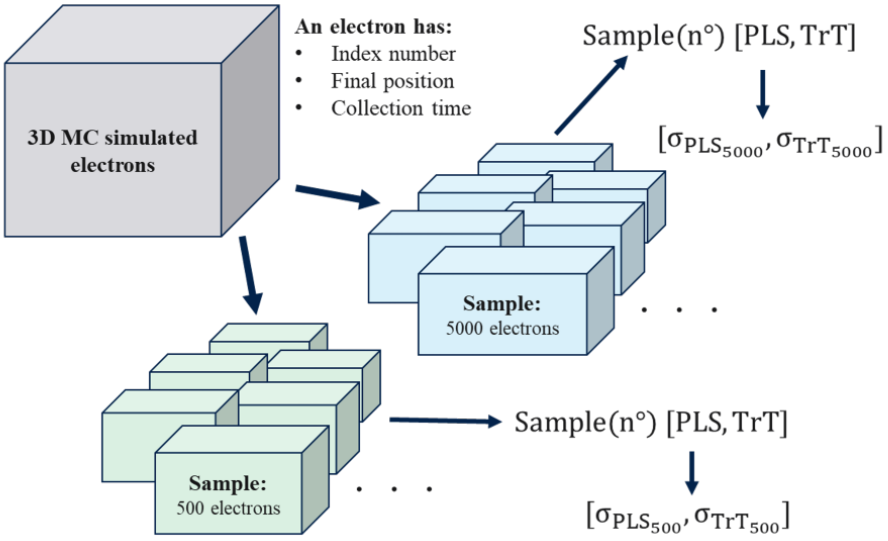


Figure 3.12: All electrons simulated with 3D MC are partitioned in smaller samples. This is done by randomizing the index number of simulated particles. PLS and TrT values are computed for each sample with a smaller number of particles. They are computed respectively from the final position and collection time of all electrons in each sample. Different standard deviation values σ_{PLS_n} and σ_{TrT_n} can be computed for a different total number of particles per sample n . The standard deviation values will decrease if the value of n increases.

The obtained curve shows a decreasing value of PLS standard deviation with an increase of the number of charges per package. As the signal stored at the sensing node increases closer to the sensing node maximum storage capacity, i.e. fullwell, an increase of the measured PRNU values is expected [83]. This non-linear behavior of

PRNU due to the saturation of sensing nodes is not taken into consideration in this analysis. The maximum storage capacity of the studied pixel is of 5,500 electrons. This is important to be noted because an increase to measured PRNU close to the maximum storage value would be due to a non-linear increase of σ_{charge}. Furthermore for the case with a sample size much smaller than the pixel capacity, σ_{PLS} is expected to match more significantly PRNU measured results. Additionally, as PLS is solely optical, no further contribution of $\sigma_{transfer}$ is expected.

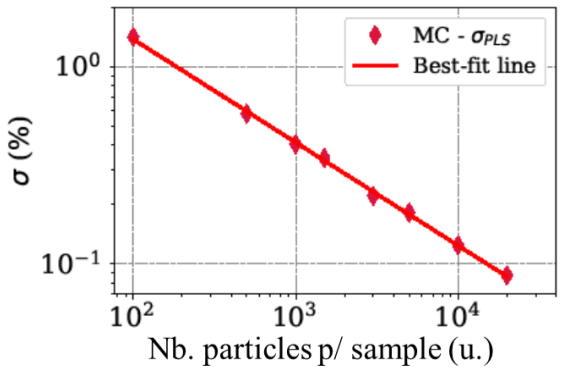


Figure 3.13: Simulated electrons were random partitioned in samples with different sizes. Computed σ_{PLS} value is plotted versus the number of particles per sample. At a 1,500 electrons operation, the computed σ_{PLS} value is 0.3% versus 0.82% measured PRNU.

The simulated contribution of the charge statistical error σ_{charge} to the PRNU is 0.3% compared to the measured PRNU value of 0.82%, both values are obtained for the charge amount of 1,500 electrons. This difference indicates that there are mismatches in the pixel matrix. It is also the case for depth non-uniformity (DNU).

The standard deviation of TrT (σ_{TrT}) is plotted versus the number of particles per sample. The obtained curve is shown in Fig. 3.14. DNU measurement is done at 40% of the total storage node capacity to reduce the charge variability to a standard operating value. The measured DNU is of 20.0ps versus a simulated time error of 10.4ps. There is not enough information to conclude on the main contributor of DNU as a study of dark current and pixel process mismatches would be required. However, the results seem to indicate that the deterministic limitation is still far of the measured value. This deterministic limitation is the value of DNU obtained from the MC simulation using samples with a number of charges corresponding to those collected during the pixel operation.

Equation (3.7) identifies the main temporal and spatial contributions of DNU. The previous elements introduced in equation (3.5) are decomposed in more precise elements to interpret and understand the main contributors of the depth error. They are the temporal (t) and spatial (s) contributions caused by:

(i) The dark variability ($\sigma^2_{dark_{t,s}}$): that is the variability of the dark current in time for a same pixel corresponding mainly to the low frequency noise in the pixel; and

the dark spatial variation inside of the pixel matrix.

(ii) The ambient illumination variability ($\sigma^2_{amb.\ illum._{t,s}}$) : the ambient light variation will depend on the quantity of photons emitted by the ambient light source. It can be understood as a variation to the percentage of the total signal for the spatial contribution and a variation of the ambient photogenerated charges for the temporal contribution. If the ambient illumination can be considered constant during the integration step, no impact of the temporal contribution will be observed, as the ambient response will remain in a quasi-permanent regime.

(iii) The transfer efficiency variability figures are:

(iii.1) The signal transfer variability composed by the temporal error of transit time (σ_{TrT}).

(iii.2) The spatial error of transfer ($\sigma_{transf._s}$) due to process mismatches between pixels inside the matrix.

$$DNU = \sqrt{\sigma^2_{dark_{t,s}} + \sigma^2_{amb.\ illum._{t,s}} + (\sigma_{TrT} + \sigma_{transf._s})^2} \tag{3.7}$$

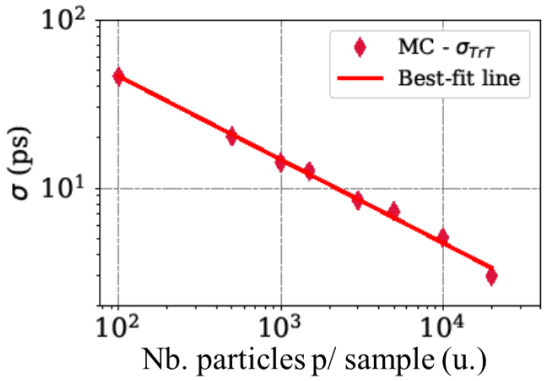


Figure 3.14: Computed σ_{TrT} is plotted as a function of sample size. The simulated electrons were random partitioned in samples with different sizes. At a 2,000 electrons operation i.e. 40% of the total storage node capacity, the computed σ_{TrT} value is 10.4ns versus 20ns measured DNU.

If the ambient illumination of the sensor during DNU measurement is much lower than the detected light signal, the ambient light variance contribution may be neglected ($\sigma^2_{amb.\ illum._{t,s}}$). The same happens to the variance of the charge signal in the dark contribution ($\sigma^2_{dark_{t,s}}$). Because it is of the order of one electron per second, the standard deviation of the dark signal is much lower than the total signal of 2,000 for an acquisition of a duration of $0.1ms$. Hence, the spatial and temporal transfer errors, i.e. $\sigma_{transf._s}$ and σ_{TrT} are inferred to be the biggest contributors of DNU. 3D MC gives an estimation of σ_{TrT}, that is the minimum measurement error attainable by the pixel when all other elements are neglected. Results indicate that PRNU and DNU is reduced by increasing pixel storage capacity and the amount of detected signals. However, specifically for DNU, $\sigma_{transf._s}$ remain the main contributor.

3.4.4 MC simulation versus measurement

PRNU measurements have been carried-out to compare with the simulated results. The measurement consists of biasing the iToF sensor as it is done during a demodulation phase and while biased, the sensor pixel matrix is exposed to a constant laser illumination for a long integration time of $5ms$. This operation is done over 4 successive frames. (i) Firstly, the 4 frames are stacked together (pixel-by-pixel) to compute the averaged between the frames. (ii) Then, the standard deviation of all pixel is done for the obtained averaged array image. Hence, the standard deviation of the charge signal percentage ($\sigma_{\%}$) is obtained.

To compare with the simulated results of PRNU versus the number of charges per acquisition, the laser intensity is modulated. In Fig. 3.15, $\sigma_{\%}$ is plotted versus the total photogenerated charges by frame. To compute the value of the PRNU also shown in the previous graph, the value of the dark standard deviation (s_{dark}) must be measured (equation (3.4)). This value is obtained by doing an acquisition without illumination. The measured PRNU value increases with signal decrease as expected [83, 84].

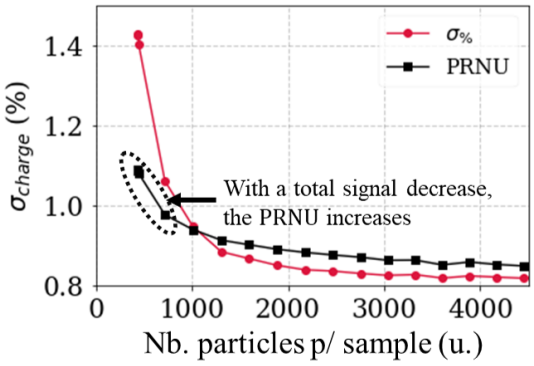


Figure 3.15: Measured $\sigma_{\%}$ and PRNU versus the total measured signal per frame. The measurements are done with a constant exposure time of $5ms$

Despite the reproduction of the expected tendency of PRNU, to have a reliable comparison with the simulated results, much lower signal intensities are required. To attain the lower signal values with the used laser, the exposure time must be reduced. Fig. 3.16 shows the PRNU versus the total measured charges per frame for two different measurement conditions. They are the previous condition with a constant integration time of 5ms and a new condition with a variable integration time. For the second case, it is possible to reach much lower signal values.

To be able to compare the measured results with simulation, σ_{charge} is computed from the measured values (equation (3.4)). As the PLS is collected directly after generation, $\sigma_{transfer}$ is neglected. The same may be considered for the charges collected in the other zones of the pixel where collection is not intended, causing a part of the signal to be lost. The computation of σ_{charge} is done by suppressing the σ^2_{offset} component of each one of the measured sets. The obtained results are shown in Fig. 3.17a.

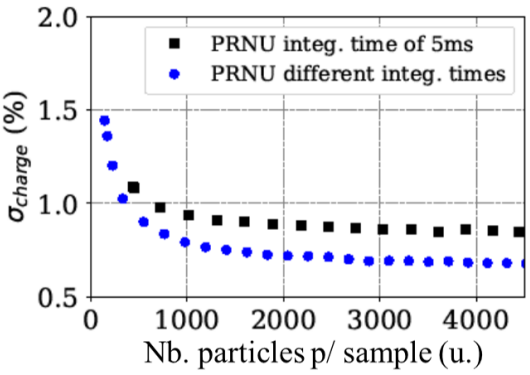


Figure 3.16: PRNU versus the total measured charges per frame for two different measurement conditions. They are a condition with constant integration time of 5ms and a condition with variable integration.

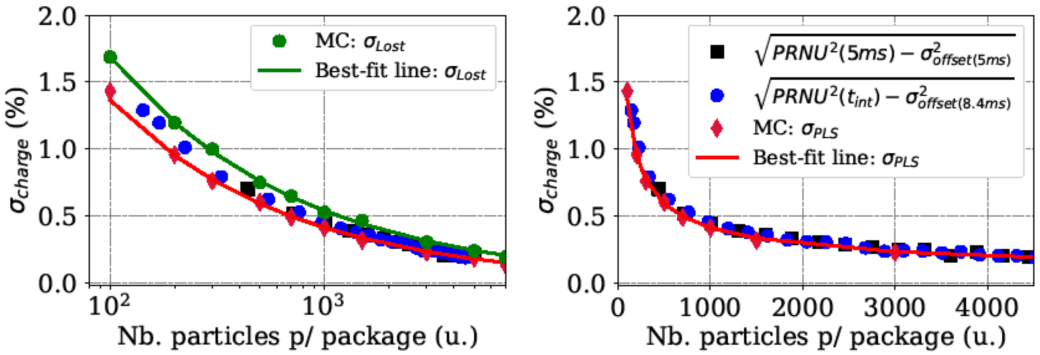
The σ_{offset} value is taken from the difference between the measured PRNU and the simulated σ_{PLS} for a case with high signal (e.g. 4000 electrons) and for each data set. Indeed, a different offset is observed between both configuration and the origin of the offset is unclear. The obtained result match significantly with the σ_{PLS} for the different amount of charge measurements, the same tendency is obtained with a linear correlation of 0.99.

Despite being unclear, the origin of the σ_{offset} may be caused by the following two reasons. The first one is a change to the second order of standard deviation of the dark signal (σ_{dark}), caused by the use of the different integration durations between the measurements. The different exposure times may cause σ_{dark} to change, i.e. the standard deviation of the spatial dark standard deviation (s_{dark}). The second possible reason, is a variation of QE. Indeed, the measured values represent only the collected electrons. Therefore the spatial mismatch of photogenerated electrons may be caused by a variability of the photons that reach and generate charges inside of the pixel. The QE is a figure of merit that is normalized by the incident photons. Hence, a variation of the QE is observed as an offset contribution to $\sigma_{\%}$ (i.e. σ_{offset}). This offset is not simulated with MC, as the approach used for the amount of photogenerated charges is deterministic and only the reparation of those charges is statistical. Additionally, there may be other non identified artifacts related to the different measurement conditions.

Finally, the computed standard deviation percentage of $\sqrt{\sigma^2_{charge} + \sigma^2_{transfer}}$ is compared using a logarithm scale for the abscissa in Fig. 3.17b. An additional simulation result is plotted versus the number of particles, that is the standard deviation of the lost signal (σ_{Lost}). Both σ_{Lost} and σ_{PLS} correspond significantly to the analyzed measured results. Additionally, the simulated standard deviation of the lost signal correspond to the standard deviation of charges collected in SN_1 and SN_2, as described by equation (3.8), where $\sigma_{SN_1\%}$ is the standard deviation of the percentage of signal collected in SN_1.

$$\sigma_{Lost} = \sqrt{\sigma^2_{SN_1\%} + \sigma^2_{PLS}} \tag{3.8}$$

Contrarily to PRNU, DNU measurement requires a laser source capable of being modulated in intensity and in frequency. The in situ available laser source has a restricted sine wave effective intensity while operating at a 200MHz frequency and because of that it is not possible to control the number of charges at a high frequency measurement. Hence, it is not possible with the currently available material and test bench to carry on DNU measurements versus the number of charges collected.



(a) (b)

Figure 3.17: Simulated electrons were randomly partitioned in samples with different sizes. Computed σ_{PLS} value is plotted versus the number of particles per sample. The percentage variation $\sigma_{\%}$ of signal was measured and, as in the MC the dark signal is not simulated, it corresponds to the PRNU. A constant value of σ^2_{offset} equals to 0.42% is obtained for measurements from 1000 electrons up to 5000 electrons. This value is used to compute the measured contribution of $\sigma_{charge} = \sqrt{PRNU^2 - \sigma^2_{offset}}$ versus the number of particles for the measurement. The obtained σ_{charge} has a linear correlation of 0.99 when compared to the best-fit line obtained with abscissa and ordinate logarithmic scales.

Conclusion

The developed iToF 3D MC simulation methodology presents the same tendencies for DMC observed with the TCAD methodology. They both match significantly with the measured DMC tendencies in temperature. However, an offset is observed between the DMC values obtained with the 3D MC simulation and the measurements. This offset has two reasons: (i) the degradation of mobility representative of the real behavior of the pixel. This mobility degradation is caused by the coulomb scattering with the increase of free carriers concentration during illumination. This mobility degradation mechanism is included in the IALMob mobility model. (ii) The increase in transit time due to the real pulse width used in TCAD. This offset of $40ps$ is not considered in the MC simulation, as in this simulator the photogeneration is instantaneous. The pulse widths corresponds to that of the laser used during the DMC measurements.

Despite these mismatches, the tendencies match measured results significantly. Additionally, the interest of the 3D MC simulation is the possibility of obtaining information complementary the drift-diffusion-based-TCAD deterministic approach. Indeed, the statistical variability obtained with the 3D MC methodology points to the different contributions of PRNU and DNU.

To exploit the statistical properties of the simulated data, the simulated particles were randomly partitioned over different samples. Each sample has a different outcome for PLS and TrT. The standard deviations of PLS and TrT (σ_{PLS} and σ_{TrT}) for all outcomes can be computed versus the number of particles per sample. The σ_{PLS} corresponds to the σ_{charge} contribution of the PRNU value. Similarly, the σ_{TrT} is a contribution of the DNU value.

With the obtained 3D MC results, it is possible to conclude that to reduce the PRNU and DNU values, the QE and the fullwell capacity must be increased. The obtained 3D MC results represent a minimum attainable standard deviation with the given quantity of charges.

Despite the promising results, complementary measurements are required for a deeper understanding of the PRNU and DNU contributions. New test structures could be envisaged to estimate the spatial contributions of DNU. Additionally, a dedicated test bench is required to measure the evolution of DNU versus the number of charges.

References

[17] Min-Sun Keel. "A 4-tap 3.5um 1.2Mpixel indirect time-of-flight CMOS image sensor with peak current mitigation and multi-user interference cancellation". In: *IEEE International Solid-State Circuits Conference, ISSCC* (2021), pp. 106–108. DOI: 10.1109/ISSCC42613.2021.9365854.

[18] Cedric Tubert. "4.6um Low Power Indirect Time-of-Flight Pixel Achieving 88.5% Demodulation Contrast at 200MHz for 0.54MPix Depth Camera". In: *ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference, Proceedings* (2021), pp. 135–138. DOI: 10.1109/ESSCIRC53450.2021.9567878.

[34] Simon Sze. *Physics of Semiconductor Devices*. ser. Wiley-Interscience publication. John Wiley and Sons, 1981.

[37] SDevice. *Sentaurus Device User Guide*. Version S-2021.06. 2021.

[39] M. Furumiya. "High sensitivity and no-cross-talk pixel technology for embedded CMOS image sensor". In: *International Electron Devices Meeting 2000. Technical Digest. IEDM (Cat. No.00CH37138)*. 2000, pp. 701–704. DOI: 10.1109/IEDM.2000.904415.

[40] Y. Hagiwara. "High-density and high-quality frame transfer CCD imager with very low smear, low dark current, and very high blue sensitivity". In: *IEEE Transactions on Electron Devices* 43.12 (1996), pp. 2122–2130. DOI: 10.1109/16.544383.

[57] Boris Rodrigues. "Indirect ToF pixel integrating fast buried-channel transfer gates and gradual epitaxy and enabling CDS". In: *Proc. IISW* (2017), pp. 266–269.

[64] SProcess. *Sentaurus Process User Guide*. Version S-2021.06. 2021.

[65] Kane Yee. "Numerical solution of initial boundary value problems involving Maxwell's equations in isotropic media". In: *Transactions on Antennas and Propagation IEEE* 14 (3 1988), pp. 302–307. DOI: 10.1109/TAP.1966.1138693.

[66] A. R. Forouhi and I. Bloomer. "Optical properties of crystalline semiconductors and dielectrics". In: *Phys. Rev. B* 38 (3 1988), pp. 1865–1874. DOI: 10.1103/PhysRevB.38.1865.

[67] David F. Edwards. "- Silicon (Si)". In: *Handbook of Optical Constants of Solids*. Ed. by Edward D. Palik. Burlington: Academic Press, 1997, pp. 547–569. DOI: https://doi.org/10.1016/B978-012544415-6.50027-3.

[68] H.R. Philipp. "- Silicon Dioxide (SiO2) (Glass)". In: *Handbook of Optical Constants of Solids*. Ed. by Edward D. Palik. Burlington: Academic Press, 1997, pp. 749–763. DOI: https://doi.org/10.1016/B978-012544415-6.50038-8.

[69] Axel Crocherie. "From photons to electrons: a complete 3D simulation flow for CMOS image sensor". In: *Proceedings of the 2009 International Image Sensor Workshop (IISW)* 1 (2009), pp. 1–4.

[70] Jerome Michallon. "Etude et optimisation de l ' absorption optique et du transport électronique dans les cellules photovoltaiques à base de nanofils". In: *'PhD manuscript, HAL Id: tel-01171003'* (2015).

[71] Lumerical. *Inc., FDTD: 3D Electromagnetic Simulator*. Version version 2022-r6. 2022.

[72] Andreas Schenk. "A Model for the Field and Temperature Dependence of Shockley-Read-Hall Lifetimes in Silicon". In: *Solid-State Electronics* 35 (1992), pp. 1585–1596.

[73] W Hänsch and M Miura-Mattausch. "The hot-electron problem in small semiconductor devices". In: *Journal of applied physics* 60.2 (1986), pp. 650–656.

[74] Syed Aon Mujtaba. "Advanced Mobility Models for Design and Simulation of Deep Submicrometer MOSFETs". PhD thesis. Stanford, CA, USA: Stanford University, 1995.

[75] M.N. Darwish, J.L. Lentz, M.R. Pinto, P.M. Zeitzoff, T.J. Krutsick, and Hong Ha Vuong. "An improved electron and hole mobility model for general purpose device simulation". In: *IEEE Transactions on Electron Devices* 44.9 (1997), pp. 1529–1538. DOI: 10.1109/16.622611.

[76] Cyrus Bamji. "A Review of Indirect Time-of-Flight Technologies". In: *IEEE Transactions on Electron Devices* 69.6 (2022), pp. 2779–2793. DOI: 10.1109/TED.2022.3145762.

[77] Gabriel Mugny. "Demodulation Contrast simulation for indirect Time-of-Flight sensors based on Fast Photo-Diode". In: *Proceedings of the 2021 International Image Sensor Workshop (IISW), Online* (2021).

[78] L. Viña and M. Cardona. "Effect of heavy doping on the optical properties and the band structure of silicon". In: *Phys. Rev. B* 29 (12 1984), pp. 6739–6751. DOI: 10.1103/PhysRevB.29.6739.

4 - Current assisted photonic demodulor: silicon & germanium

Introduction

Although a thicker silicon absorption layer can increase the quantum efficiency, it may also reduce the transfer efficiency and degrade the depth measurement accuracy. This trade-off makes it challenging to engineer a high-performing indirect time-of-flight pixel. Additionally, in the SWIR wavelength range between $1.0\mu m$ and $2.5\mu m$, silicon is quasi-transparent. This means that to detect a SWIR photon, silicon must be replaced by a more suitable material. Photodiodes of different materials have been proposed for NIR and SWIR sensing. The main candidates are PbS quantum dots in quantum films [87, 88], InGaAs [89, 90], and germanium on silicon (Ge-on-Si) [91–93] (see Annex 6.3).

The integration of these photodiodes into a 3D device depends on three main factors. The fabricated sensors require (i) to be compatible with CMOS integration, (ii) to have a low response time and (iii) a low noise level. Among the CMOS compatible alternatives, two different types of iToF pixels can be distinguished. The first one is a pixel with fast integration, as it has less fabrication steps, called the current assisted photonic demodulator (CAPD), i.e. the focus of this chapter. This solution has been demonstrated both in silicon and germanium on silicon technologies [16, 53]. In contrast, the second pixel type relies on more sophisticated integration. These pixels have state-of-the-art performances and they will be the focus of the last chapter 5.

This chapter is divided into four parts. Firstly, in sections 4.1, the state-of-the-art of the CAPD technology is reviewed. In section 4.2, the silicon CAPD pixel is studied using a reverse engineering methodology of a commercially available device [45]. In the next two parts (section 4.3 and 4.4) the germanium CAPD is investigated. In section 4.3 the state-of-the-art of the germanium CAPD is reviewed. Finally in section 4.4 the simulation investigation of a germanium CAPD pixel is presented. The work developed in this last part proposes and optimizes a CAPD pixel design to be later fabricated in partnership with CEA LETI in Grenoble. The simulation methodology developed in chapiter 2 is used for the study of the CAPD devices.

4.1 The current assisted photonic demodulator

The principle of the current assisted photonic demodulator (CAPD) sensor was first published by van der Temple et al. [94]. The first reported pixel evolved in the following years to the structure shown in Fig. 4.1 [42]. Since then, the CAPD structure was extensively reported in literature as a promising candidate for indirect time-of-flight (iToF) pixels [16, 43].

The CAPD shown in Fig. 4.1, previously introduced in subsection 1.3.3, is composed of four electrodes. Two of them are doped N+ (SN_1 and SN_2) to create the sensing nodes and two are doped P+ (D_1 and D_2) to create the demodulators. By polarizing the demodulators electrodes (D_1 and D_2) at different voltage (e.g. respectively $1.2V$ and $0V$), an electric field can be generated in the depth of the P- doped substrate. When illuminated by a photon with a given wavelength, an electron hole pair is generated deep inside the substrate. The hole drifts with the electric field ($\vec{\mathscr{E}}$) in the direction of the hole current ($\vec{J_h}$) and is collected by the P+ demodulator electrode polarized by the lower biasing D_2. The electron is oriented on the opposite direction of the electric field $\vec{\mathscr{E}}$ and is measured at the opposite electrode, SN_1.

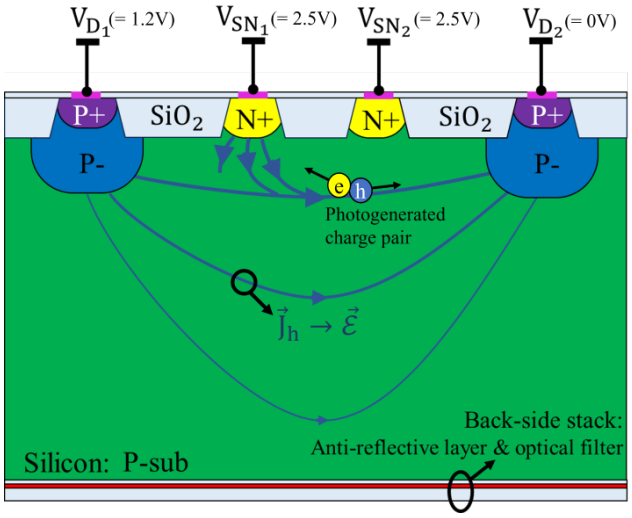


Figure 4.1: State-of-the-art current assisted photonic demodulator (CAPD) pixel schematics. The pixel has two demodulators (D_1 and D_2) and two sensing nodes (SN_1 and SN_2). The substrate is lightly doped with a P-type doping, i.e. P-subs. The back-side stack is depicted with different unspecified layers consisting of the anti-reflective layer and the optical filter. These layers are specific to the back-side illumination (BSI) and may change significantly in the case a front-side illumination is intended. Shallow trench insulation fabricated in silicon oxide (SiO_2) is integrated between the sensing nodes and the demodulators for isolation purposes. For more information, see subsection 1.3.3

Pancheri et al. [95] studied a similar structure to the one in Fig. 4.1 where the substrate was lightly doped with an N-type doping and the collected minority carriers

were the holes. This configuration is not optimal, because collecting free electrons may allow smaller transfer times [95].

Dalla Betta et al. [96] continued studying a similar structure to the one presented by Pancheri et al. [95] with the implementation of a gradually doped P-type silicon layer. The gradual doping creates an improved electric potential distribution in the depth of the silicon layer used for light detection. Higher electric field values are observed deeper inside the silicon absorbing layer, improving photogenerated charge collection. Additionally, improving the electrostatic potential gradient with the doping decrease, causes a reduction in the electron collection time.

Furthermore, the P+ demodulators integrated by Dalla Betta et al. [96] placed inside of P- implanted zones, have an increased driven current. Additionally, by decreasing the distance between D_1 and D_2, and consequently between SN_1 and SN_2, the transfer speed of photogenerated charges can be increased.

The CAPD pixel solution has been previously demonstrated in a Ge-on-Si platform [44, 53]. The germanium CAPD study and solution proposition will be the subject of the last two sections of this chapter. In the next section, a commercially available CAPD sensor is studied with a reverse engineering approach.

4.2 Reverse engineering of the CAPD pixel

The studied sensor is integrated to operate with back-side illumination (BSI) to improve its QE performance. A camera sensor requires wiring and other electronic components which may occupy a significant part of the pixel total surface. This part of the sensor drives the photogenerated signal to the treatment circuit. If the sensor electronics are designed on the illuminated side of the sensor, it becomes difficult to design smaller pixels without losing sensitivity.

Hence, by using the BSI integration, the commercially available CAPD achieves $5\mu m$ pitch pixels which are smaller than those found in other CAPD camera sensors [16, 27, 45]. However, the sensor has a resolution of 644 by 488 pixels, which is low compared to other iToF camera sensors [17, 18].

The commercially available solution is reverse-engineered in three steps:

1. Morphological reconstruction of the layout and the optical stack through physical analysis using scanning electron microscope and transmission electron microscopy data.

2. Optical simulation of the reconstructed stack (section 4.2.1).

3. Electrical simulation of the reverse-engineered solution (section 4.2.2), aiming to obtain an estimation of the key figures of merit and compare to the existing CAPD literature.

The morphological reconstruction of the pixel is not explained in detail. Nevertheless, a description of the layout is provided in the following paragraph and the optical stack is illustrated schematically in section 4.2.1.

The scanning electron microscope (SEM) images of the CAPD sensor, were used for the reconstruction of the TCAD simulated pixel. The reconstructed layout and the designed matrix are depicted in Fig. 4.2, where the pixel motif is identified. This is the unitary motif replicated inside of the pixel matrix. The masks, depicted in Fig. 4.2, are the (i) active region mask ("Active"), a negative mask for the shallow trench insulator fabrication, (ii) the gate mask ("Gate") for the fabrication of polysilicon MOS gates and (iii) the contact ("Contact"), metalization routing layers (M1, M2 and M3) and vertical interconnect assembly (VIA) layers (VIA1 and VIA2). For other important layers, such as (iv) implantation layers (P-Well, P-, PD, N+ and P+), the design was approached using standard drawing techniques available at STMicroelectronics.

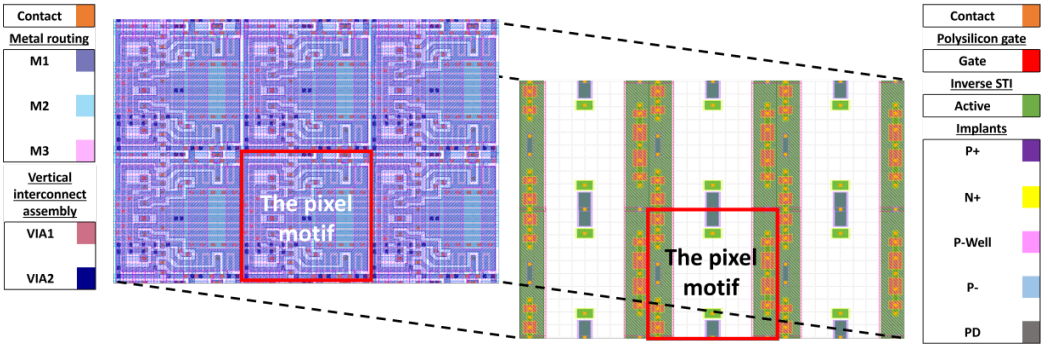


Figure 4.2: Reverse engineered layout from SEM imaging of the commercially available imager pixel.

Fig. 4.3a shows the complete coverage of the surface of the pixel by the metal layers used for the routing of the contacts in the pixel. The detailed labeling of each contact is done in Fig. 4.3b. In the case of the simulated layout, each transistor function will not be specified as it does not impact significantly the operation at the pixel level.

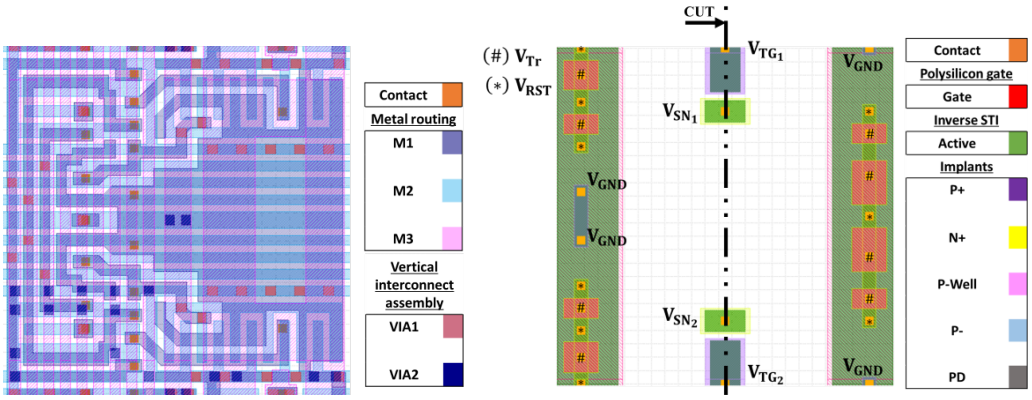


Figure 4.3: The simulated pixel layout (a) BEOL metal layers and (b) FEOL pixel layer. A cut line is identified in the sense of the demodulators. Cross-sections over this cut line will be used later on to illustrate the sense of the charge transfer inside the pixel.

4.2.1 Optical simulation

Kato et al. [16] previously opted for a pixel operating at the NIR wavelength of $850nm$ and a thinner device of $1.2\mu m$ thickness. Consequently, the pixel had a lower quantum efficiency but a faster charge transfer. Transmission electron microscopy measurements allowed to determine the thickness of the optical stack layer as well as the thickness of the silicon used for the absorption of infrared light.

Optical simulation have been carried out on the optical stack of the pixel layout depicted in Fig. 4.3. A simplified schematic of the optical stack is depicted in Fig. 4.4. The pixel is back side illuminated and the optical stack is composed of different elements such as the micro-lens, an anti-reflective layer and the BSI stack for the passivation of the silicon back-side. Additionally, the different implants are depicted although the doping concentration is not considered in optical simulation. As the substrate is lightly P-doped and only a negligible part of the light reaches the highly doped zones at the top of the pixel, the doping concentration plays no significant role in the optical simulation. However, during the electrical simulation studies, the doping concentration will be optimized. This structure simulated in 3D is displayed in Fig. 4.5.

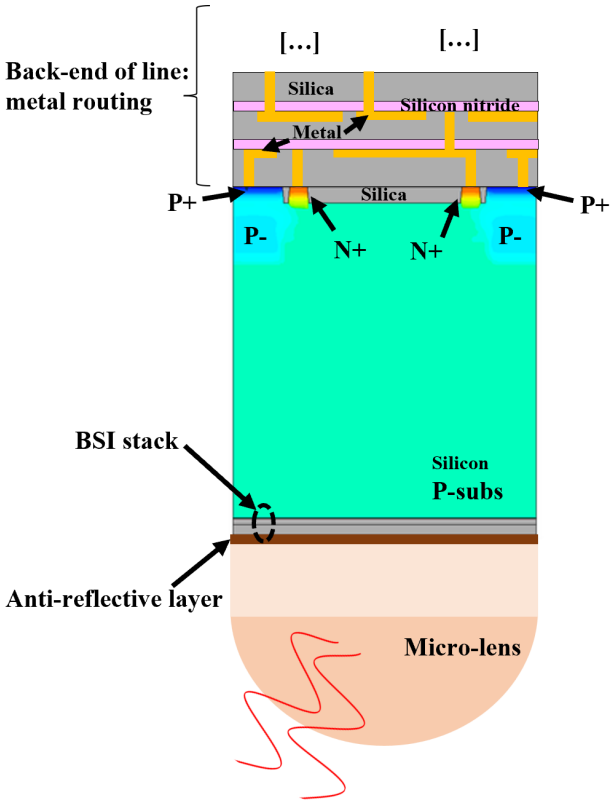


Figure 4.4: Simplified 2D schematic of the studied CAPD optical stack.

Metal layers cover all the surface of the pixel as shown in Fig. 4.3a. This is important because as the device uses BSI, the metal layers situated on the front side will behave as an internal reflector. The light that enters through the BSI stack and

crosses the pixel a first time, reaches the metal layers, where it is reflected back to the silicon absorbing volume. The increased light path causes a QE increase.

Simulations carried out with lumerical FDTD [71] show a light power absorption of 38% of the total incident light power, at a wavelength of 940nm with an epitaxial layer thickness of 6.6μm. A 2D cross-section of the simulated 3D pixel in Fig. 4.5 is presented in Fig. 4.6 with the different refractive indexes of the structure.

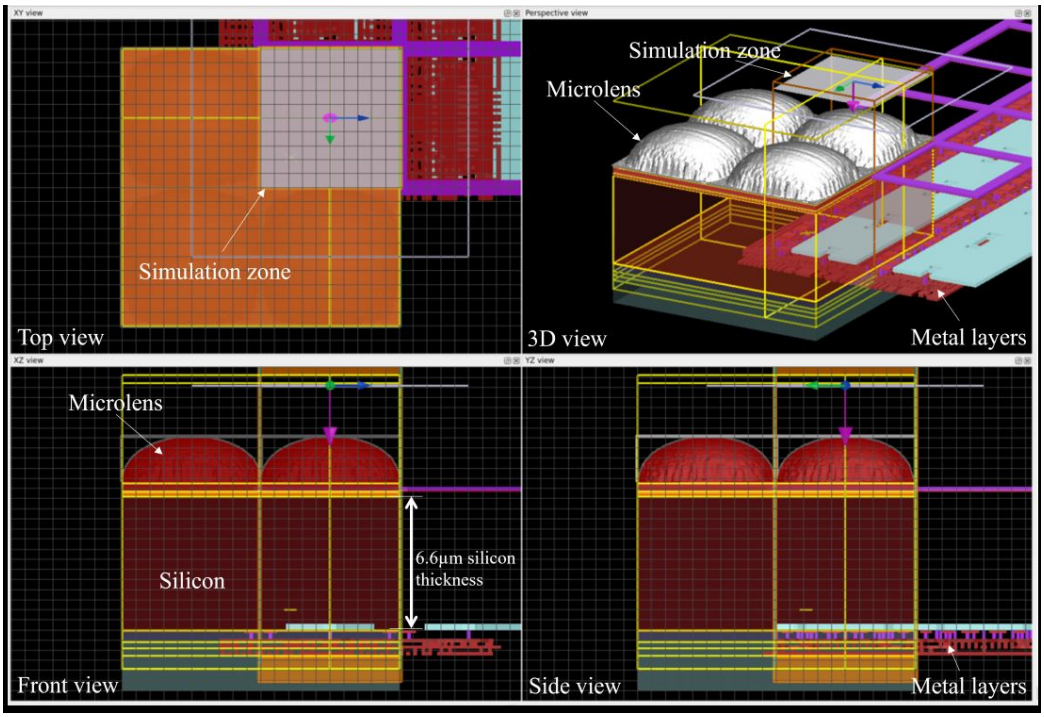


Figure 4.5: Lumerical 3D simulation of the reconstructed optical stack from the reverse engineered layout, whose dimensions were obtained with third parties TEM cuts.

The map of absorption in the volume of the pixel is computed in time and then used as a 3D map of photogenerated charges. The simulated photogeneration distribution is imported in Sentaurus TCAD electrical simulation [37]. The interpolated map of photogeneration is depicted in Fig. 4.7 with cross-sections in each direction. The photogenerated free carriers distribution is mostly central thanks mainly to the optimized microlenses. Additionally, the reflection of light by the metallic layers is maximized by covering the whole pixel surface with the metal routing. All the photogenerated charges imported in TCAD electrical simulation are collected by the sensing nodes in the pixel. Hence, the percentage of absorbed light power is equivalent to the quantum efficiency and is equals 38%.

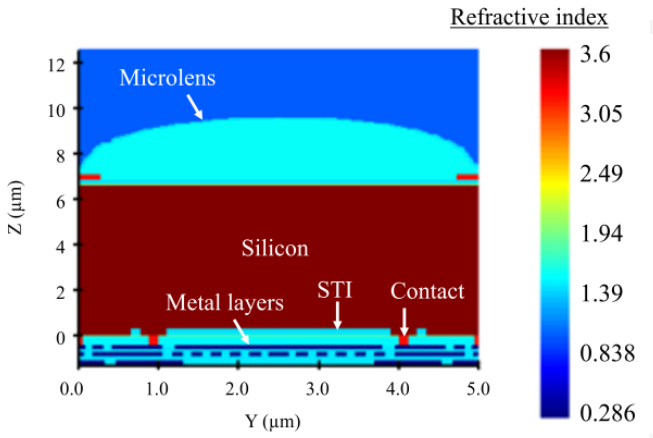
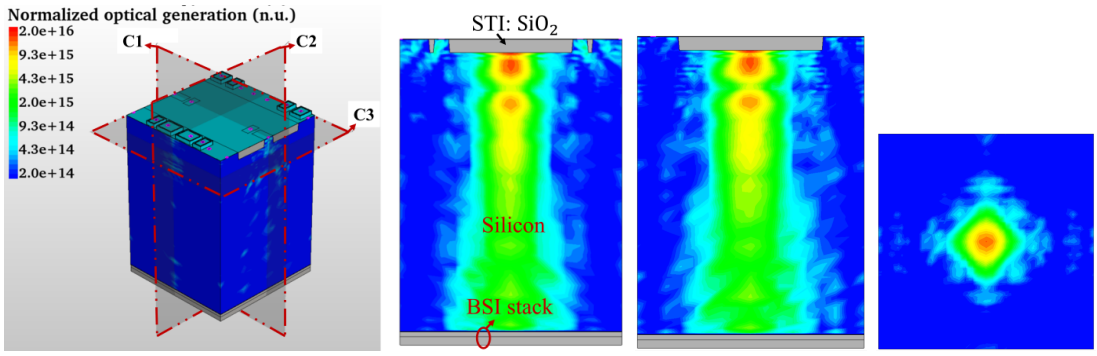


Figure 4.6: 2D cross-section of lumerical 3D simulation of reverse engineered lyaout.



(a) 3D CAPD. (b) Cut C1. (c) Cut C2. (d) Cut C3.

Figure 4.7: Optical generation simulated using lumerical FDTD and imported in (a) 3D TCAD simulated pixel, the cross-sections of the 3D structure are plotted in (b) the direction of demodulators and SNs, (c) in the transversal direction of SNs and (c) in the depth of the pixel at $1.0\mu m$.

4.2.2 Electrical simulation

In this part, the commercially available solution is simulated and compared to the literature. In the following parts, the goal is to evaluate the possible improvements to the CAPD and to identify its limitations.

An additional mask designs is simulated, it is depicted in Fig. 4.8. A second P-type implant is designed over the P+ demodulators. This implant, done with much higher energies than the P+ implants. Despite the limited information on the doping concentration of implanted zones, this implant was likely implemented in the commercially available solution, as it is expected to improve the photogenerated charge transfer [96].

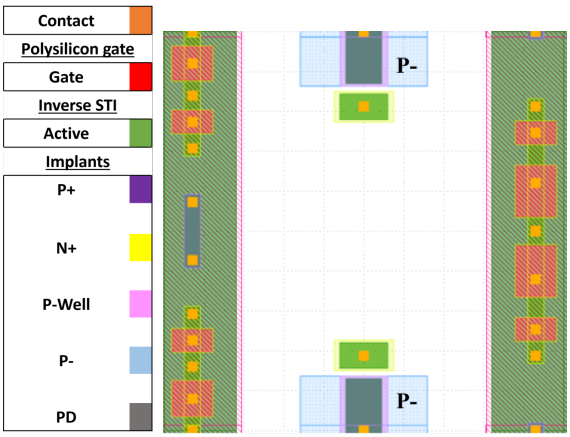


Figure 4.8: A second P-type (i.e. P-) implant designed over the P+ demodulators, done with much higher energies than the P+ implants.

The reverse engineering of the energy dose and tilt conditions of the implants is limited due to the absence of information on the doping values of the structure. The doping values of silicon volume is chosen to be $5{\cdot}10^{14}cm^{-3}$ as it was the value achieved for previous solutions demonstrated by Sony [16].

An accurate demodulation is when most photogenerated charges are collected by the sensing node where collection is intended. To achieve an accurate demodulation, with a thicker pixel, an alternative is to implant the demodulators with higher energy implants [96, 97]. To study this effect, the complete 3D pixel is simulated and displayed in Fig. 4.9. In Fig. 4.10, 2D cross-sections of 3D simulated structure (Fig. 4.9) are presented for the cases where the designed demodulators are fabricated only with the shallow P+ implant and the case where the designed demodulators have an additional P- implant.

The obtained electric potential distribution for a structure with an activated demodulator (i.e. $(D_1(on) = 1.2V)$) on the left and a deactivated demodulator (i.e. $(D_2(off) = 0V)$) on the right are depicted in Fig. 4.11a and Fig. 4.11b. Fig. 4.11a shows the electric potential distribution for a pixel with designed demodulators fabricated only with the shallow P+ implant and Fig. 4.11b has a demodulator designed with an additional P- implant. Because the electric field in the volume of the pixel is

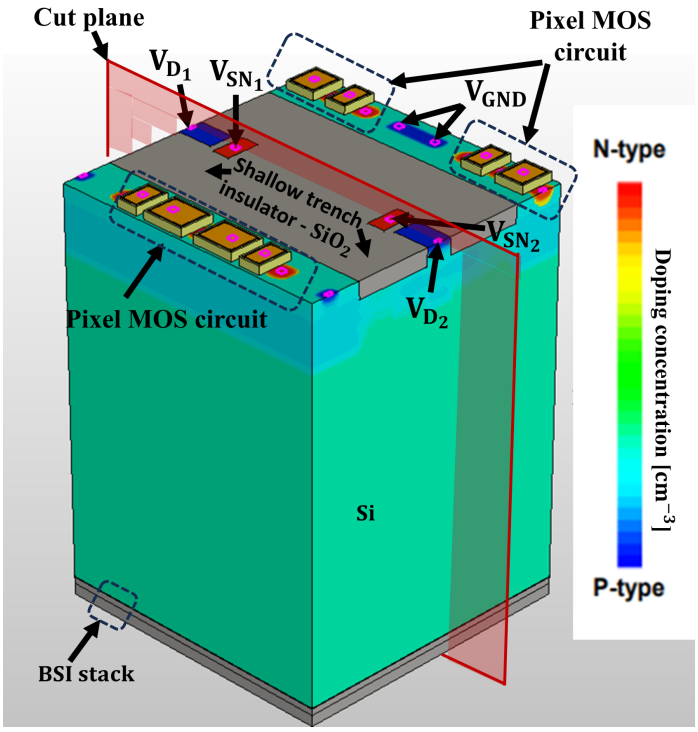


Figure 4.9: Complete 3D simulated pixel with the identified cut plane used in Fig. 4.10.

higher, the photogenerated charges may be collected much faster.

The transient response for a light impulse of photogeneration shown in Fig. 4.12a is simulated for the structures presented in Fig. 4.10. The obtained current response at SN_1 is compared with a deeper and shallow P-type demodulators in Fig. 4.12b. The slower transfer for the case with shallow implants is due to the longer transit times of charges photogenerated inside of the pixel volume. This is caused by the much weaker electric field in the pixel volume shown by the degraded electrostatic potential distribution of the shallow demodulator case Fig. 4.11a when compared to deeper demodulator Fig. 4.11b. The photogenerated charge collection efficiency is increased by increasing the depth of the demodulators. The current response to the light impulse of photogeneration obtained for both SNs is shown in Fig. 4.13.

The computed FFT response provides an estimation of the DMC versus the frequency (see section 1.5.1). In Fig. 4.14, it is compared with the results measured by Kato et al. [16] for a $10\mu m$ pitch CAPD with a thinner silicon layer used for light absorption. The similar DMC values of the two different solutions demonstrate that the use of deeper P-type demodulators increases the charge transfer efficiency despite the increased pixel substrate thickness. The stronger electric field, created by the additional P-type implant, compensates for the larger traveled distances of the charges photogenerated further away from the SNs. The deeper P-type demodulators were likely implemented in the commercially available sensor with a thicker substrate. Hence, the demodulation transfer efficiency of the previous $10\mu m$ pitch CAPD was maintained, while increasing QE at $940nm$ wavelength.

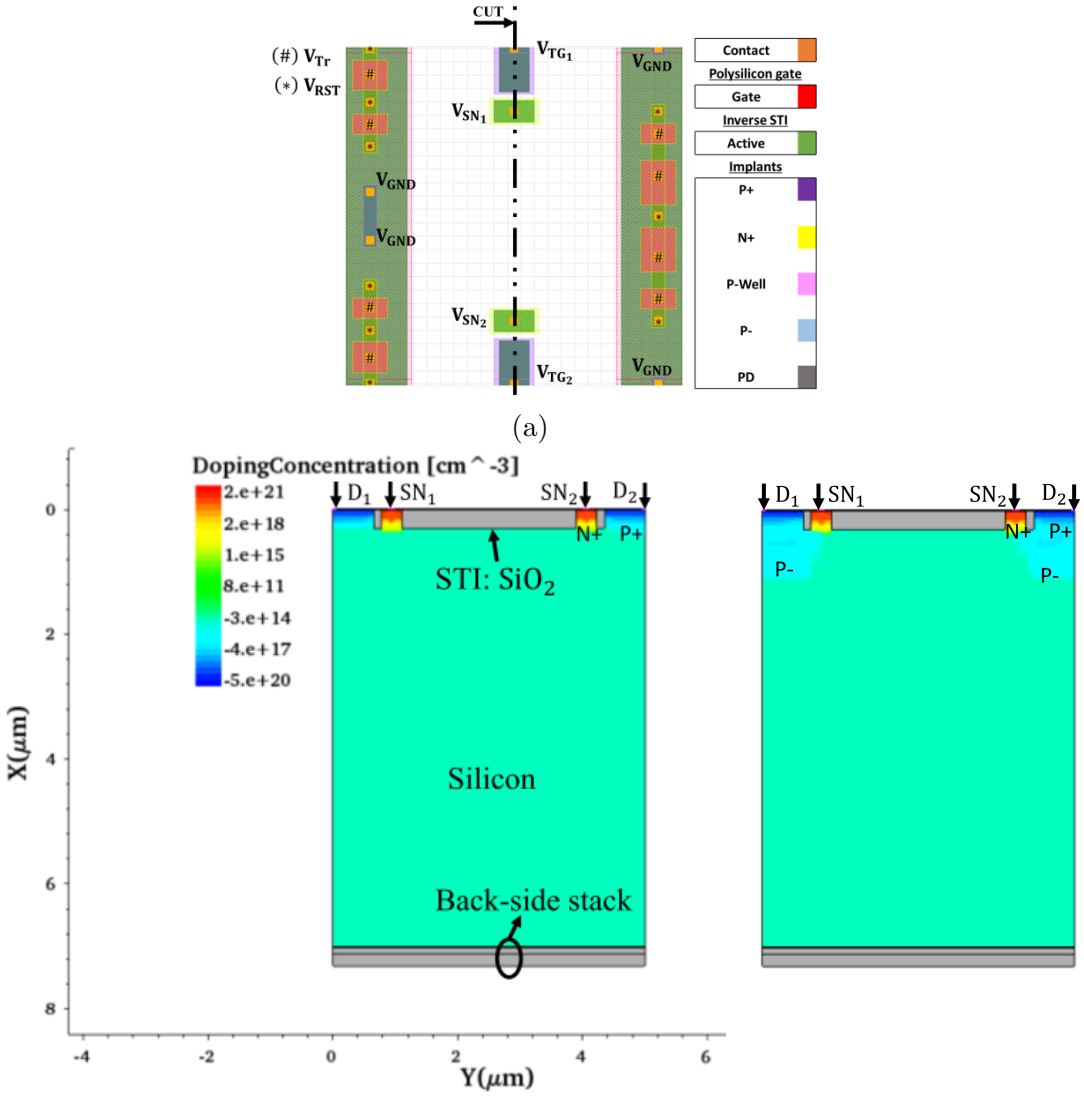
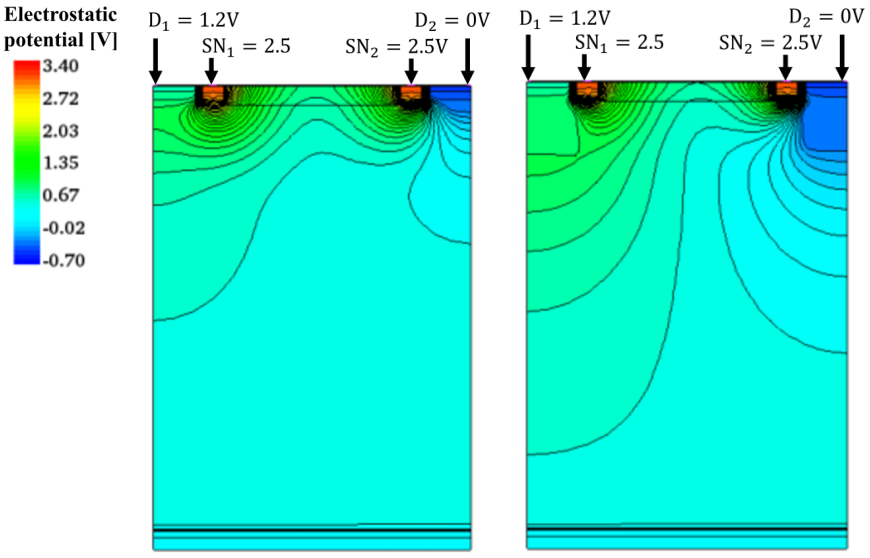
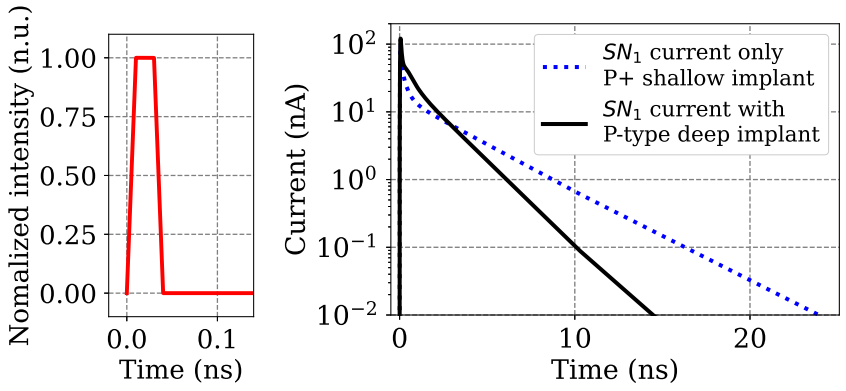


Figure 4.10: 2D cross-section in the sense of the demodulators over a 3D simulated structure. (a) The cut line is depicted over the previous presented layout. (b) A design with shallow P+ demodulator junction is compared against (c) a design with P+ and deep P implanted demodulator junctions. The P implant is done at $150eV$ with a dose of $1e12cm^{-3}$ and a tilt of $0°$.



(a) (b)

Figure 4.11: 2D cross-section of 3D CAPD simulated structures electrostatic potential distribution corresponding to the simulated pixels in Fig. 4.10. Respectively, the electrostatic potential is plotted for (a) the variant with shallow P+ demodulator junction and (b) the variant with P+ and deep P- implanted demodulator junctions. The equipotential lines are spaced by 100mV.



(a) (b)

Figure 4.12: (a) Normalized photogeneration integrated in the volume of the simulated 3D CAPD pixel. The photogeneration impulse is used to simulate the transfer of generated charges in time. The charges that are transferred and collected in the sensing nodes are measured in the form of (b) the current responses to the photogeneration impulse. This is done for shallow and deeper implanted P-type demodulators.

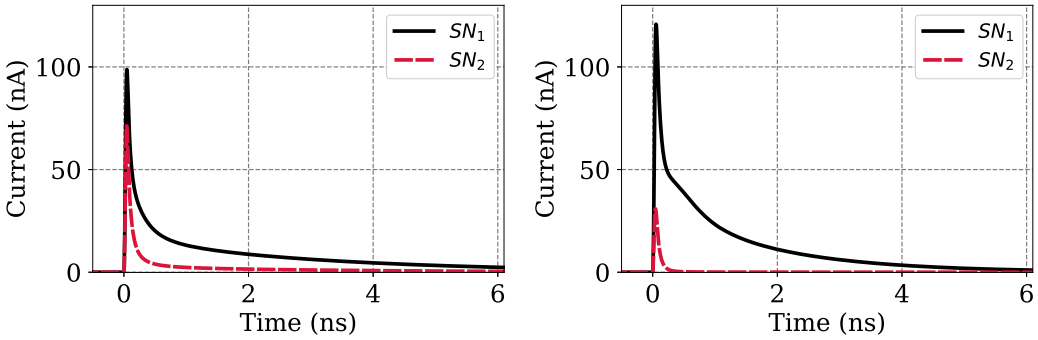


Figure 4.13: The current impulse response detected in SN_1 and SN_2 for a photogeneration impulse stimulus. The photogeneration map was simulated using FDTD optical simulation and imported in the TCAD-drift-diffusion-based simulator for the duration of the impulsion. (a) The response of the case where only the $P+$ implant is done, show a significantly high current correntions in SN_2. On the other hand, (b) by using the $P-$ deep implant, the current collected in SN_2 is much lower. The addition of the deep $P-$ implants improoves PLS significantly.

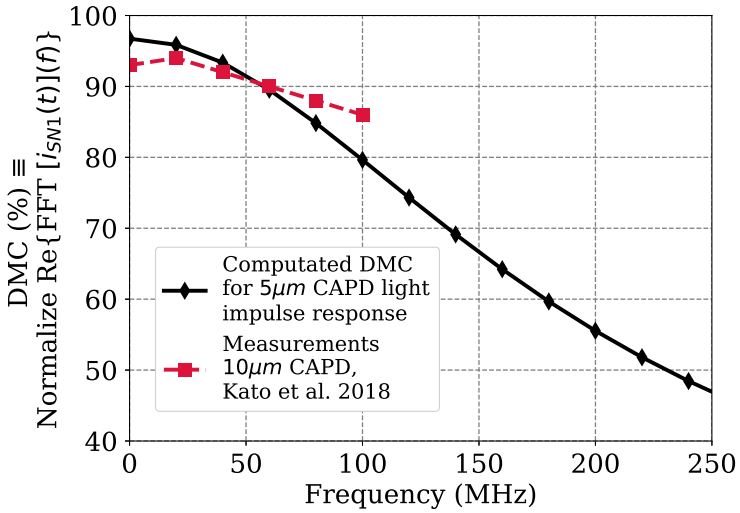


Figure 4.14: The simulated DMC versus the operating frequency f_{Mod}, (i) for the $5\mu m$ pitch CAPD pixel with high quantum efficiency, is compared to the measured data presented by Kato et al. [16], (ii) for a $10\mu m$ pitch CAPD with a thinner silicon. In simulation, the $5\mu m$ pitch CAPD current impulse response collected in SN_1 and SN_2 for a photogeneration impulse stimulus is transformed with an FFT and compared with the published data for the $10\mu m$ pitch CAPD [16].

4.2.3 Proposition of improvements

Substrate doping concentration

In CAPD sensors, the consumption is mainly due to the voltage drop between demodulators D_1 and D_2. Fig. 4.15 depicts the consumed current versus the voltage drop between demodulators, for two different doping values of the P-type substrate. Indeed, with an increase in the high biasing D(on) applied to D_1, the current increases linearly versus D(on). Consequently, when the doping of the substrate increases, the current consumption increases. Hence, a clear axis of improvement for the CAPD pixel is to decrease the substrate doping. A decrease of substrate doping increases the resistivity between D_1 and D_2 demodulators consequently reducing the current consumption.

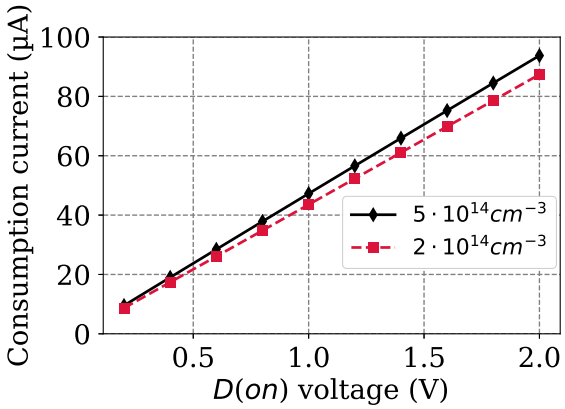
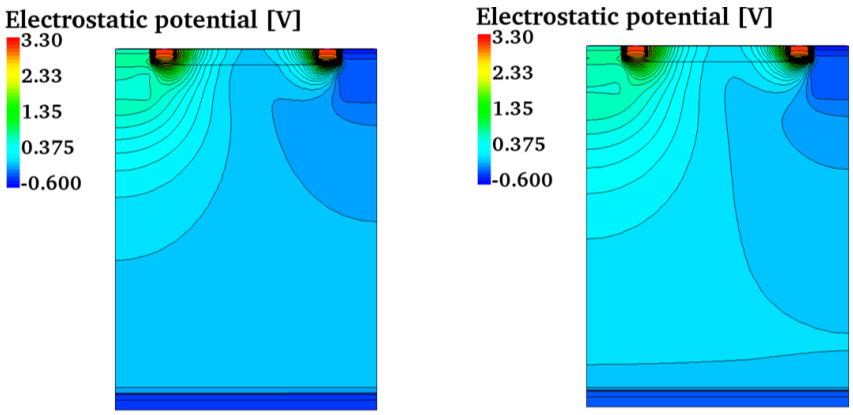


Figure 4.15: The consumed current in the demodulator biased with D(on) for different doping values of the P-type substrate.

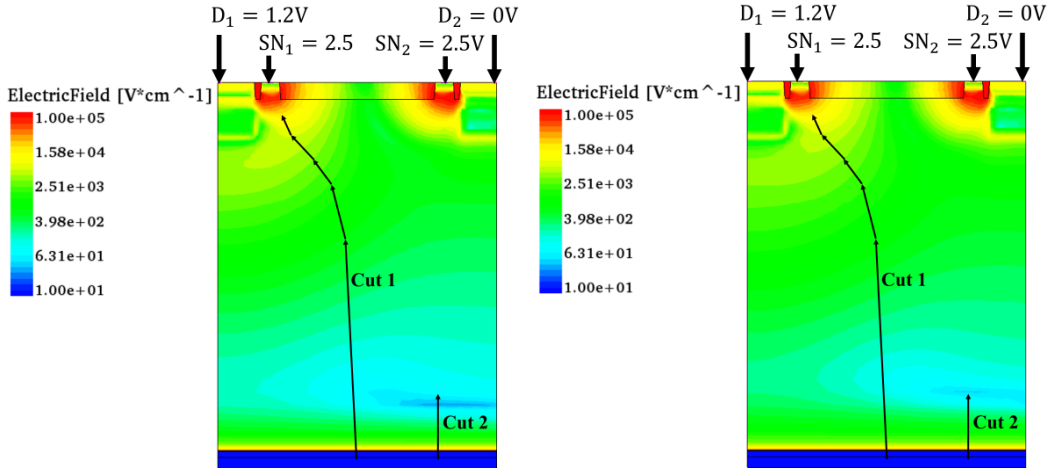
The 2D cut of 3D simulated pixels, also show different electrostatic potential distributions in the depth of the pixel for different substrate doping concentration, i.e. $5 \cdot 10^{14} cm^{-3}$ (Fig. 4.16a) and of $2 \cdot 10^{14} cm^{-3}$ (Fig. 4.16b). With a lower doping concentration of the substrate, a more homogeneous distribution of equipotential lines in the volume of the pixel is observed. Consequently, an increased electric field value at the bottom of the pixel is observed in Fig. 4.17. The increased electric field is clearly observed in the 1D cuts in Fig. 4.18 over the structures presented in Fig. 4.17.

In Fig. 4.19, the performance of a CAPD in terms of transfer efficiency figures of merit is plotted versus its P-type doping. When the doping concentration of the P-type substrate decreases, the improvement is mainly observed by an increase of DMC_{100MHz} shown in Fig. 4.19a. In conclusion, the increase in DMC_{100MHz} is a consequence of a reduction of the transit time of photogenerated charges (section 1.5.1). The transit time is reduced thanks to an improved distribution of the electrostatic potential and consequently a higher electric field deep inside the pixel volume (Fig. 4.16 and Fig. 4.17).



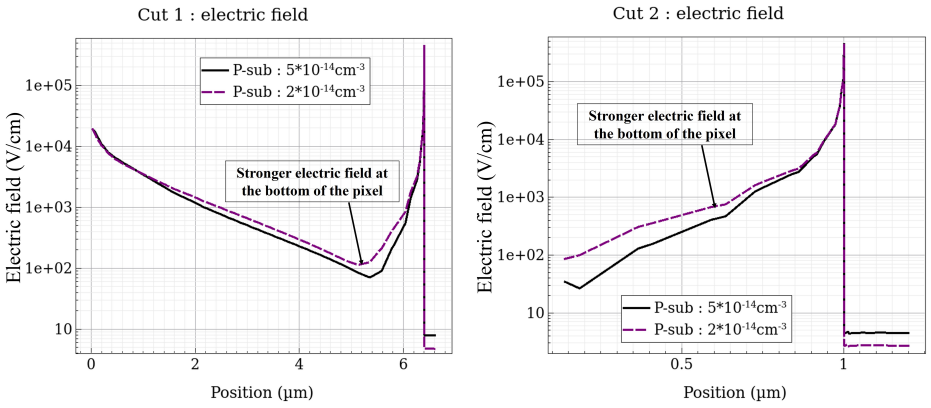
(a) (b)

Figure 4.16: A 2D cross-section of the electrostatic potential distribution in the 3D CAPD simulated pixel for a substrate of P-type doping concentration of (a) $5 \cdot 10^{14} cm^{-3}$ and of (b) $2 \cdot 10^{14} cm^{-3}$. The equipotential lines are spaced by 100mV.



(a) (b)

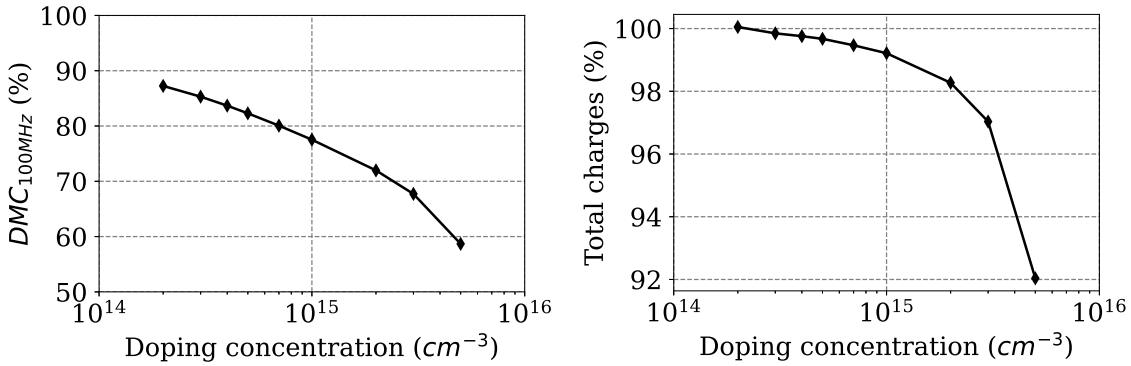
Figure 4.17: A 2D cross-section of the electric field distribution in the 3D CAPD simulated pixel for a substrate of P-type doping concentration of (a) $5 \cdot 10^{14} cm^{-3}$ and of (b) $2 \cdot 10^{14} cm^{-3}$.



(a) (b)

Figure 4.18: 1D cross-sections over the 2D cross-sections of the electric field distribution in the pixel volume, for a substrate of P-type doping concentration of $5 \cdot 10^{14} cm^{-3}$ (Fig. 4.17a) and of $2 \cdot 10^{14} cm^{-3}$ (Fig. 4.17b). (a) "Cut 1" displays a larger length of the pixel volume and (b) "cut 2" focuses on the electric field at the bottom part of the pixel.

The highly doped substrate scenarios may also be susceptible to other transfer accuracy issues. The charges photogenerated at the low electric field zones at the pixel bottom may not be collected. These low field zones may results in electrostatic potential pockets where charges will diffuse without ever reaching any of the two sensing nodes. The total photogenerated measured charges versus the substrate doping is observed in Fig. 4.19b.



(a) (b)

Figure 4.19: (a) DMC_{100MHz} and (b) the percentage of the total collected charges normalized by the total photogenerated charges versus the substrate doping concentration.

4.2.4 Limitations

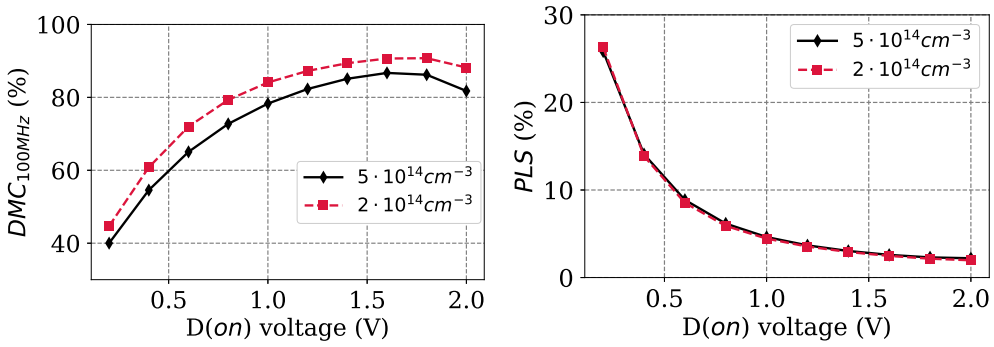
Biasing versus transfer efficiency

The consumption decrease is not the only advantage of the doping decrease, it may also improve the photogenerated charges transfer efficiency. In Fig. 4.20 the computed values of the DMC_{100MHz} and PLS are plotted versus the high biasing D(on) applied to D_1 for a 3D simulated CAPD with a substrate with $5 \cdot 10^{14} cm^{-3}$ and $2 \cdot 10^{14} cm^{-3}$ P-type doping concentrations.

When the biasing of D_1 increases (i.e. D(on) increases) the DMC_{100MHz} increases and the PLS decreases. The photogenerated charges are transferred more efficiently for two reasons:

(i) The increase in DMC is a consequence of a higher electric field in the volume of the pixel that is in turn caused by the higher potential differential between D_1 and D_2 causing a fast transfer.

(ii) The reduction of PLS is due to the distribution of electrostatic potential surrounding the sensing nodes causing charges to correctly drift and be collected by SN_1 instead of being collected by SN_2.



(a) (b)

Figure 4.20: (a) DMC_{100MHz} and (b) PLS versus the D(on) biasing applied to D_1 for a 3D simulated CAPD with a substrate with $5 \cdot 10^{14} cm^{-3}$ and $2 \cdot 10^{14} cm^{-3}$ P-type doping concentrations.

The increase in the DMC_{100MHz} reaches a maximum value at D(on) equals $1.8V$ (Fig. 4.20a). After this value it starts decreasing. This is a consequence of the PLS decrease. With the biasing increase, the charges photogenerated further from SN_1 are collected by the sensing node where the collection is intended. However, as they are generated at a longer distance, they take much longer to be collected and may not be collected in a demodulation period (i.e. N_{tap}/f_{Mod} with the number of taps $N_{tap} = 2$ and the demodulation frequency $f_{Mod} = 100MHz$). Because of that, the decreasing PLS corresponding to the charges taking longer than N_{tap}/f_{Mod} to reach the sensing node, causes a decrease of DMC_{100MHz}.

Furthermore, the PLS is limited for two reasons: (i) despite the increase in the biasing D(on), some of the charges may be directly photogenerated in the sensing node

zone. These charges are directly collected by the sensing node where the collection is not intended. (ii) The maximum biasing allowed to activate the demodulators (D(on)) must be much smaller than the sensing node biasing. If D(on) is selected too close to the biasing of the sensing nodes, the PN junction composed by D_1 and SN_1 may be foward biased. A direct current in the PN junction renders the device nonfunctional. Due to the required reverse bias, to maintain a pertinent contrast between the sensing nodes, the operating bias must ensure a large excursion of at least 1 V (i.e. $max(V_{SN_1}) - min(V_{SN_2}) > 1.0V$). Therefore, D($on$) is chosen as $1.2V$ and $max(V_{SN_1})$ as $2.5V$.

Pitch reduction

The key limitation of the CAPD pixel is the pitch reduction. Ebiko et al. [58] identifies this issue for CAPD pixels below $5\mu m$ that will suffer from a significant consumption increase. To improve the understanding of the pitch reduction limitation, different CAPD pitches were attempted in simulation. The 2D TCAD-drift-diffusion-based simulation is used to compute the current consumed during the activation of one of the demodulator D_1 with a biasing of D(on) equals $1.2V$. The obtained results are shown in Fig. 4.21. The 2D simulation focuses on the demodulator current consumption, neglecting the impact of the other pixel elements. Hence, for pixels with the same demodulator size, the consumed current obtained in $\mu A \cdot \mu m^{-1}$) in 2D simulation is directly compared between the different pixel pitches. In Fig. 4.21, a significant increase in consumption is observed between the pitch of $5\mu m$ and $2.5\mu m$. Fig. 4.22 shows electrical 2D simulation results for different pitches. With the pitch decrease, the hole current between the demodulators increases (e.g. Fig. 4.22i at a $3\mu m$ pitch shows a higher hole current density than Fig. 4.22c at a $5\mu m$ pitch).

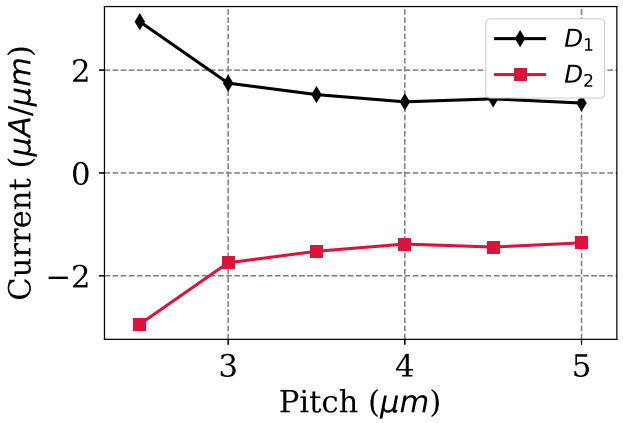


Figure 4.21: 2D CAPD current consumption versus the pixel pitch. The structure is biased as during operation. One of the demodulators (D_1) is activated with a biasing of D(on) equals $1.2V$. D_2 is biased at $0V$ and the sensing nodes SN_1 and SN_2 are biased at $2.5V$.

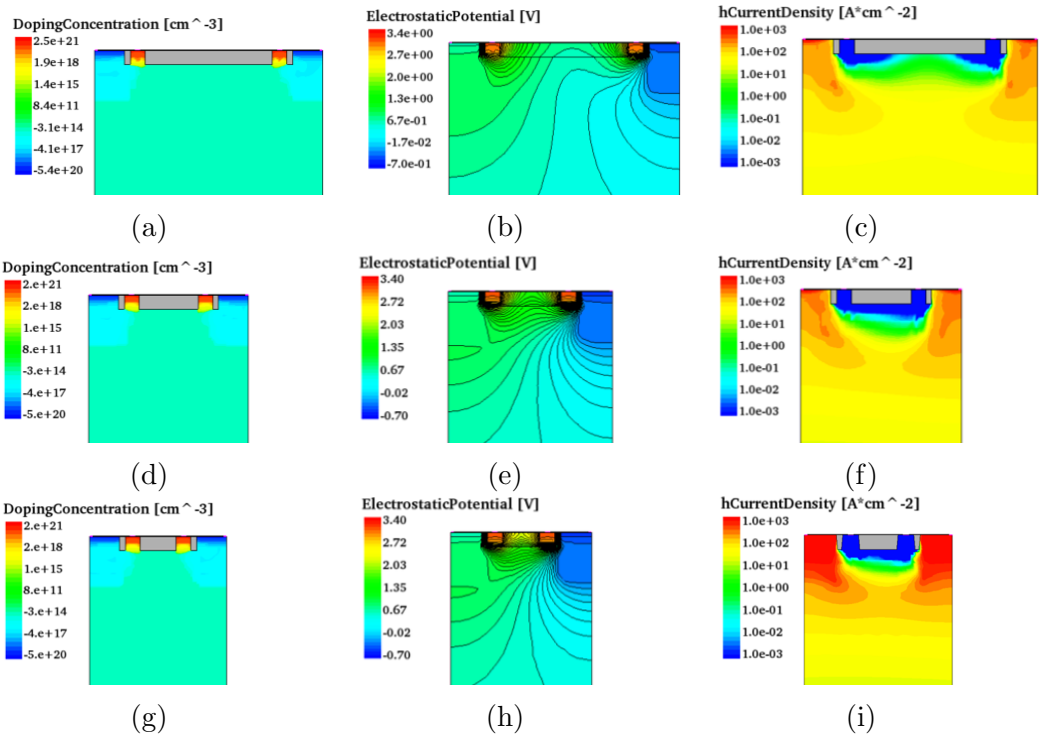
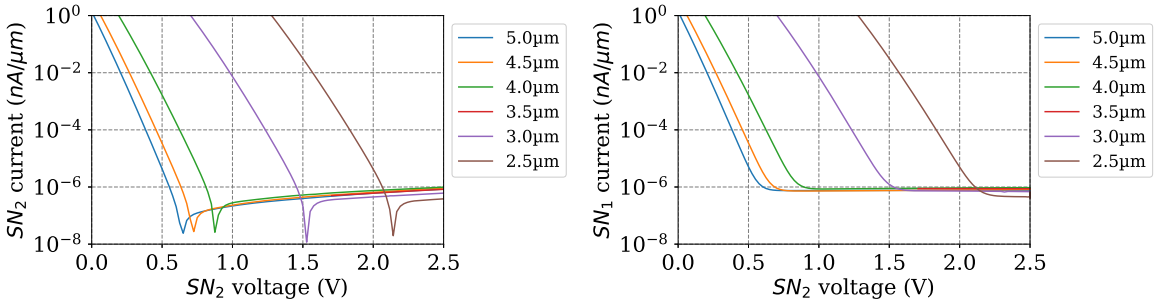


Figure 4.22: 2D simulation of the CAPD pixel of different pitches. The doping concentration distribution is plotted for the pitches of (a) $5\mu m$, (d) $3.5\mu m$ and (g) $3\mu m$. The structure is biased as during operation with the activation of one of the demodulator D_1 with a biasing of D(on) equals $1.2V$. D_2 is biased at $0V$ and the sensing nodes SN_1 and SN_2 are biased at $2.5V$. The electrostatic potential and hole current densities are plotted respectively for the pitches of (b,c) $5\mu m$, (e,f) $3.5\mu m$ and (h,i) $3\mu m$.

The potential of the sensing nodes (SN_1 and SN_2) decreases, as photogenerated electrons are collected (section 1.3.3). Another consequence of the pitch reduction is the leakage increase between SN_1 and SN_2 during charge collection with the floating potential change. In Fig. 4.23, the leakage current is computed in 2D simulation for both sensing nodes during a sweep of the SN_2 biasing from $2.5V$ to $0V$. D_1 is maintained at $1.2V$ and D_2 at $0V$. From a certain biasing of SN_2, a leakage current is observed between SN_1 and SN_2. To avoid leakage, a maximum potential differential between the sensing nodes is identified and this value decreases as the pitch decreases. The indicator of leakage is considered to be an increase of two times the leakage current when the sensing nodes are at the same biasing of 2.5V.

For a pixel of $3\mu m$, a floating diffusion sensing node would not allow a voltage excursion that decreases the sensing node potential lower than $1.5V$. This limited voltage excursion of the sensing nodes impacts the contrast of the pixel significantly. The minimum pitch for a CAPD pixel is $3.5\mu m$. This is the limit of pitch for a CAPD with a suitable consumption current and a floating diffusion with an acceptable maximum contrast without leakage. At this pitch an excursion of a sensing node bias

between $2.5V$ and $0.8V$ has a leakage increase of less than twice the value of the leakage current at $2.5V$.



(a) (b)

Figure 4.23: 2D CAPD absolute leakage current in (a) SN_2 and (b) SN_1 are plotted for a sweep of the biasing of SN_2 for different pitches. The structure is biased as during operation with the activation of one of the demodulator D_1 with a biasing of D(on) equals $1.2V$. D_2 is biased at $0V$ and the sensing nodes SN_1 and SN_2 are biased at $2.5V$. The sensing node SN_2 is swept from $2.5V$ to $0V$.

In conclusion, the silicon CAPD is a suitable iToF pixel solution with competitive low cost integration. However, it shows a clear limitation in terms of miniaturization and high resolution matrix integration. To extend the application of the CAPD solution to the detection of wavelengths higher than $1\mu m$ and maintain its competitiveness, an alternative integration has been envisaged by using a germanium-on-silicon technology.

4.3 Ge CAPD state-of-the-art

The use of silicon as an absorbing material limits the illumination wavelength to the near infrared region. There have been attempts to develop CAPD devices using germanium as the absorbing material, that are sensitive at wavelengths beyond $1\mu m$ [44, 53]. Recently, Ge-based CAPD sensors were able to obtain a depth image operating at $1310nm$ with a demodulation contrast between 70% and 90% at $500MHz$ [53].

The obtained QE for the germanium CAPD pixel presented by Chen et al. [53] is higher than 64.6% at $940nm$ and higher than 46.3% at $1310nm$. No silicon iToF sensor has been published with a QE as high as the one obtained with the germanium CAPD. The challenge of using germanium is the noise caused by significant dark current values at ambient temperature due to the small band gap of the material [91, 98].

Aiming to study the Ge-based CAPD, the solution was integrated to a LETI Ge-on-Si fabrication process. Previous to fabrication, the devices have been extensively simulated. The proposed devices and their electro-optical characterizations under illumination were carried out by CEA LETI in Grenoble. All measurements are done at a wavelength of $1310nm$ and at $30°C$.

4.4 Fabrication: Ge CAPD

The Ge layer used in this study was grown in a reduced-pressure chemical-vapor-deposition reactor on silicon substrates that were oriented in the $< 100 >$ direction and had a diameter of $200mm$. The growth process is described in detail by Durlin et al. [91]. The epitaxial growth is a process done at high temperatures from $400°C$ up to $750°C$, where germanium and silicon lattice mismatch is small. When exposed to ambient temperatures, lattice relaxation takes place. Due to mismatches in the lattice sizes between silicon and germanium, the epitaxial layer contains dislocations.

Fig. 4.24 shows a schematic of the final complete device with all available process options, i.e. the Ge-P+ epitaxial interface layer, P+ and N+ implants and P+ doped polysilicon trench isolation. The high boron doping germanium interface layer (Ge-P+) is intended to passivate the defects created by the dislocations. The germanium epitaxy layer is fabricated over a Si(001) substrate lightly P-type doped, i.e. with a boron concentration of $1 \cdot 10^{15} cm^{-3}$. For additional information on the fabrication of the germanium epitaxial layer over silicon, please refer to annex 6.4.1.

N-type and P-type contact areas were created through ion implantations of phosphorus and boron, respectively. A rapid thermal annealing step was performed at $600°C$ to activate the dopants, resulting in a specific resistivity of $1.4 \cdot 10^{-6}$ and $6.8 \cdot 10^{-6} \Omega \cdot cm$ for N-type and P-type, respectively. These implant and annealing conditions are aligned with the fabrication process used in LETI and were used as such in TCAD process simulation.

The sensing nodes (SN_1 and SN_2) and demodulators (D_1 and D_2) are defined respectively by N-type and P-type areas with dimensions of $1.0\mu m$ by $1.0\mu m$. The four tungsten metal electrodes contacting the detectors and guides are $0.4\mu m$ by $0.4\mu m$.

The CAPD was front-side illuminated, through a metal layer containing an opening at the center. The metal opening, illustrated with the device top view in Fig. 4.25, is designed over the center of the pixel to limit the illuminated surface to the area between the demodulators.

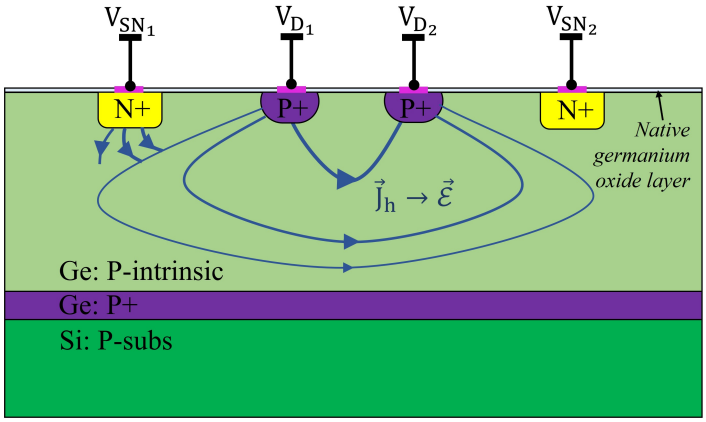


Figure 4.24: Ge-on-Si CAPD schematic.

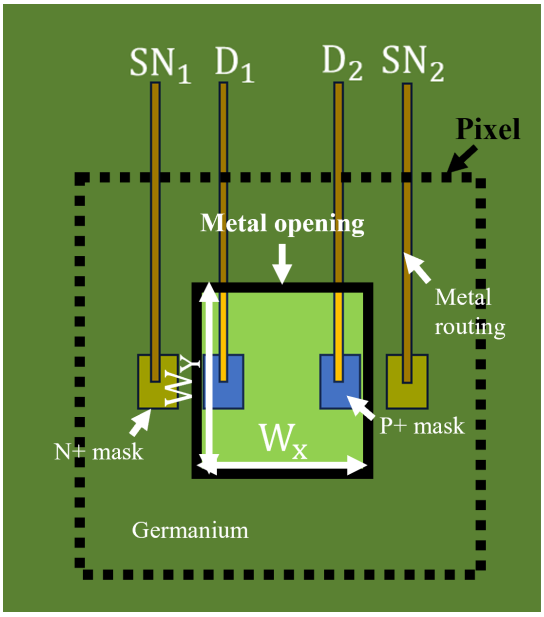


Figure 4.25: Top view of the germanium CAPD pixel with the different routing for the demodulators (D_1 and D_2) and the sensing nodes (SN_1 and SN_2). The retangular metal opening fabricated at the top of the pixel has respective length and width values of W_x and W_y.

4.4.1 Different design simulation results

The optical generation rate was computed analytically and imported into the electrically simulated device. The computation considers the metal opening. This opening is depicted in the top view of the pixel shown in Fig. 4.25. The illumination through this metallic optical window changes when the dimensions of the opening change. In this zone the generation is considered to follow Beer-Lambert's Law for light absorption. The absorption coefficient versus wavelength were measured at the CEA LETI.

2D simulations were carried out to compare different pixel elements impact, i.e. (i) the highly doped Ge-P+ passivation layer and (ii) the silicon at the bottom of the structure. The later (ii) is always present when fabricating the device. However, when the highly doped germanium layer is biased, the intrinsic germanium is electrically isolated from the silicon at the bottom. In this part, it will be demonstrated that the silicon at the bottom of the pixel has no impact to the electrostatic potential distribution when the germanium is biased. This is an important simplification for 3D simulation, as a smaller structure can reduce the total simulation time.

The obtained results for DMC_{300MHz}, PLS without dark (i.e. $PLS_{w/o}$) and leakage current are presented in Table 4.1. The charges leaked per second are computed from the simulated leakage current (I_{dark}) given in Table 4.1. The PLS without dark current, i.e. $PLS_{w/o\ dark}$ is computed with equation (4.1) by subtracting the percentage of the leaked charges ($\frac{Q_{dark}}{Q_{Total}}$) relative to the total number of charges collected in both sensing nodes (Q_{Total}). In equation (4.1) q is the elementary charge value and t is the total simulation time.

$$PLS_{w/o\ dark} = PLS - \frac{Q_{dark}}{Q_{Total}} = PLS - \frac{I_{dark} \cdot t}{q \cdot Q_{Total}} \tag{4.1}$$

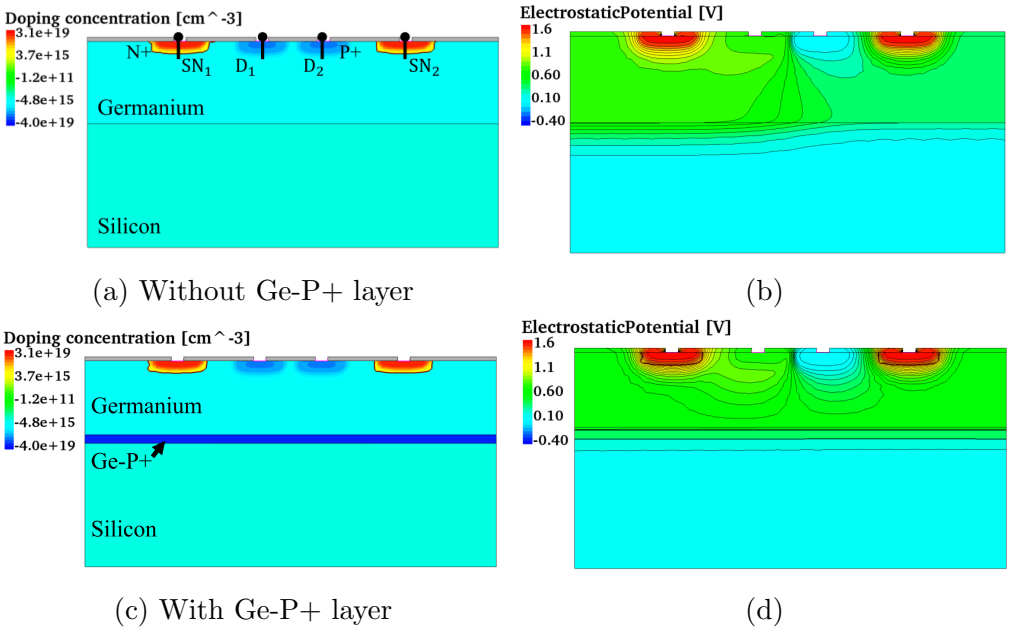
The case without the Ge-P+ interface layer is not functional (Fig. 4.26a,b). It has a significantly high PLS value and a degraded DMC value. This happens because the electric potential distribution in the silicon bulk participates in the electrostatic distribution inside the germanium layer and it depends on the sensing node and demodulator biasing. The simulated potential distribution is shown in Fig. 4.26b. It is not possible the determine the reason for the high PLS from the interpretation of the electrostatic potential in Fig. 4.26b. For the study of the pixel, the PLS and DMC computation from the current response to a light impulse is required.

For a functional fabricated device, the Ge-P+ interface layer is necessary shown in Fig. 4.26c,d, as it reduces the high leakage currents. The reason for this layer is the passivation of the high defect density on the germanium close to the interface with silicon. These defects are generated during the fabrication, as the epitaxial layer close to the interface between both materials suffers from dislocations due to the lattice size mismatches. For more information on the electric behavior of this sole and the different envisaged process alternatives results see annex 6.4.

The Ge-P+ also has a significant importance in simulation. The use of this layer allows to simplify the silicon bulk in simulation. Fig. 4.27 illustrates a case where the silicon bulk is not simulated. DMC_{300MHz} and $PLS_{w/o}$ for the case depicted in Fig. 4.27a show similar values in Table 4.1 than the corresponding cases with a silicon bulk in Fig. 4.26c,d because they have the Ge-P+ interface layer. This highly doped layer isolated electrically the germanium from the silicon bulk.

Table 4.1: DMC_{300MHz}, PLS without dark (i.e. $PLS_{w/o}$) and leakage current in SN_1 for different combination of significant parameter for different process alternatives of a germanium CAPD obtained in 2D simulation.

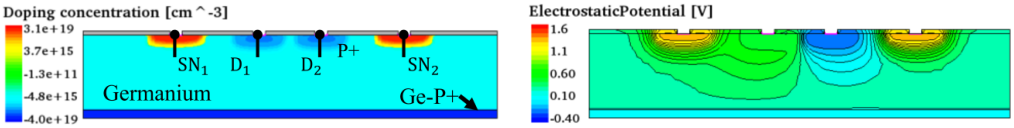
Ge-P+ layer	**Added Si-bottom**	DMC_{300MHz} (%)	$PLS_{w/o}$ (%)	I_{dark} **in** SN_1 $(pA/\mu m)$
No	Yes	19.0	14.4	282.3
Yes	Yes	94.8	6.9	2.39
	No	94.7	6.9	2.36



(a) Without Ge-P+ layer (b)

(c) With Ge-P+ layer (d)

Figure 4.26: 2D simulation of the germanium CAPD pixel with different process options. The doping concentration and electrostatic potential distributions are plotted respectively for the cases (a,b) without the Ge-P+ interface layer and (c,d) with the Ge-P+ seed layer.



(a) (b)

Figure 4.27: 2D simulation of the germanium CAPD pixel with different process options without the added silicon bottom part of the structure. (a) The doping concentration and (b) electrostatic potential distributions are plotted for the design with the Ge-P+ interface layer.

4.4.2 Comparison with measured results

In this section a measured $7\mu m$ pitch CAPD pixel is compared to 3D simulation results.

The measurement set-up has a single-mode optical fiber aligned above a pixel. The optical fiber is centered over a squared metal layer opening fabricated at the top of the pixel. This squared opening serves as an optical window to focus the light beam and it was previously depicted in Fig. 4.25. The pixel is symmetrical. If D_1 and D_2 are biased at the same voltage, the collected photocurrent at SN_1 and SN_2 are identical. Hence, the photocurrent response will be symmetrical, when the light beam is centered over the pixel. The charge-transfer efficiency is determined through the analysis of the DMC_{DC} versus the potential difference applied between the demodulators (Fig. 4.28). Symmetric experimental results are obtained when D_1 or D_2 is kept at zero bias, and when photogenerated charges are swept towards detecting junctions SN_1 or SN_2, respectively.

A light impulse of $200ps$ is generated at the wave-length of $1310nm$ and used as the incident light for the characterization of the fabricated CAPD pixel. The transient currents on both sensing nodes are measured for different applied biases between the demodulators (Fig. 4.28). During illumination and at zero bias, the same photocurrent is collected in SN_1 and SN_2. In the schematic in Fig. 4.24, as V_{D_1} increases while V_{D_2} remains at zero bias, more photogenerated charges are transferred the sensing node SN_1 instead of SN_2. Notice that restraining the optical window may increase DMC and reduce PLS, but the improvement is in detriment of QE. This is due to the reduction of fill factor of the pixel, i.e. the effective surface exposed to the incident light.

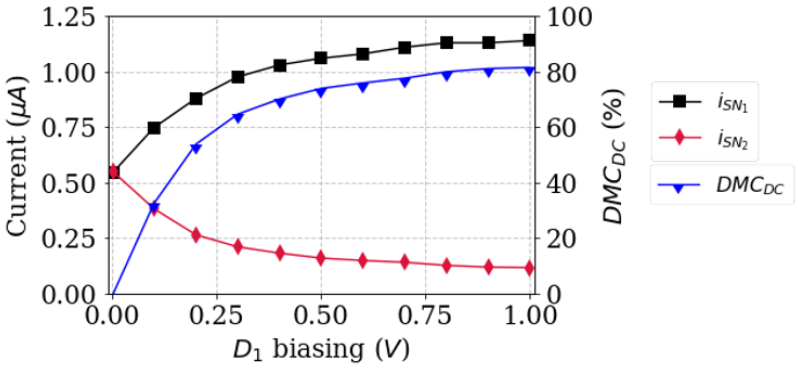


Figure 4.28: Measured DC current response and computed DMC_{DC} value versus the biasing D(on) applied to the demodulator D_1. D_2 is biased at $0V$ and the sensing nodes are biased at $1.0V$. The illumination window is a square centered over the pixel with an oppeneing of $W_x = W_y = 5\mu m$.

In Fig. 4.29 the DMC_{DC} measured results are compared to the obtained 3D simulation results for a device of an equivalent optical window. The simulation methodology reproduces significantly the DMC_{DC} measurements. An extrapolation is done

for an operation with a demodulation frequency (f_{Mod}) of $300MHz$. The DMC at $300MHz$ (DMC_{300MHz}), is computed by using equation 4.2 and the developed methodology described in section 2.3.4. This computation is done for a case of two taps per period ($N_{tap} = 2$). Because only the photocurrent collected in SN_1 is considered (i_{SN_1}), the PLS is substracted from the obtained DMC_{300MHz} simulation results. This explains partially the difference between DMC_{DC} and DMC_{300MHz}, as PLS equals 9%. The additional offset is due to the large transit time of charges that are photogenerated distant from SN_1. Additionally, no improvement on the collection time of these charges is observed for a biasing higher than $0.7V$, as the difference between DMC_{DC} and DMC_{300MHz} remains constant up to $1.0V$.

$$DMC(f_{Mod}) = Re\left\{\frac{fft[i_{SN_1}(N_{tap}\cdot t)](f_{Mod})}{fft[i_{SN_1}(N_{tap}\cdot t)](0)}\right\} \tag{4.2}$$

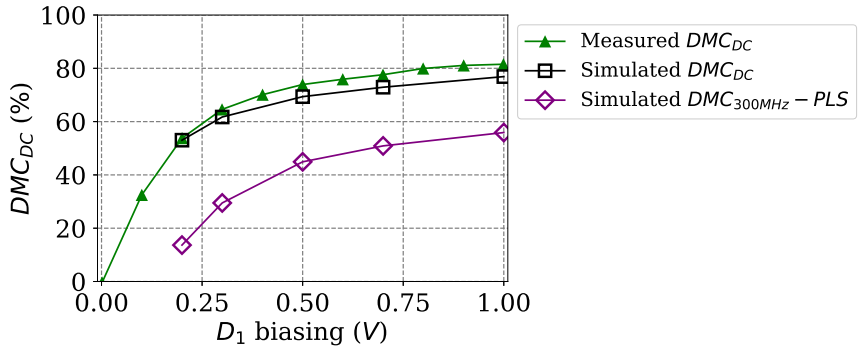


Figure 4.29: Measured DMC_{DC} and 3D simulated DMC_{DC} and DMC_{300MHz} values versus the biasing D(on) applied to the demodulator D_1. D_2 is biased at $0V$ and the sensing nodes (SN_1 and SN_2) are biased at $1.0V$. The illumination window is a square centered over the pixel with an opening of $W_x = W_y = 5\mu m$ for the measured result and for the simulated results. However, for the simulation results, only the Beer-Lambert law is considered for the distribution of light absorption. No diffraction is taken into consideration.

The current characteristic of the PN junction, formed by the sensing nodes and demodulators, is shown in Fig. 4.30. The current is plotted versus sensing node voltage for dark and illuminated measurements when demodulators D_1 and D_2 are maintained at 0.0V and the sensing nodes SN_1 and SN_2 are swept at the same time from $1.0V$ to $-0.5V$. Both sensing nodes have the same dark current characteristics as the device is symmetrical. The measurements are performed at ambient temperature.

A significant improvement is still possible for the germanium CAPD device. Fig. 4.31 shows the 3D simulated performances in terms of low and high frequency DMC values versus the pitch of the CAPD pixel. The size of the sensing nodes and demodulators were shrinked to that of available dimensions in silicon technology and the doping concentration is selected at $1 \cdot 10^{16} cm^{-3}$. A small window of $2\mu m$ is applied for the illumination with a wavelength of $1310nm$. A significant increase is observed in

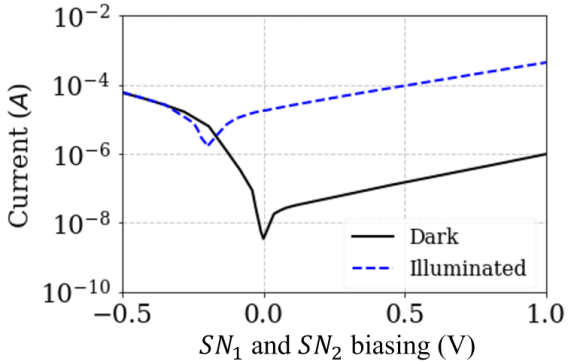
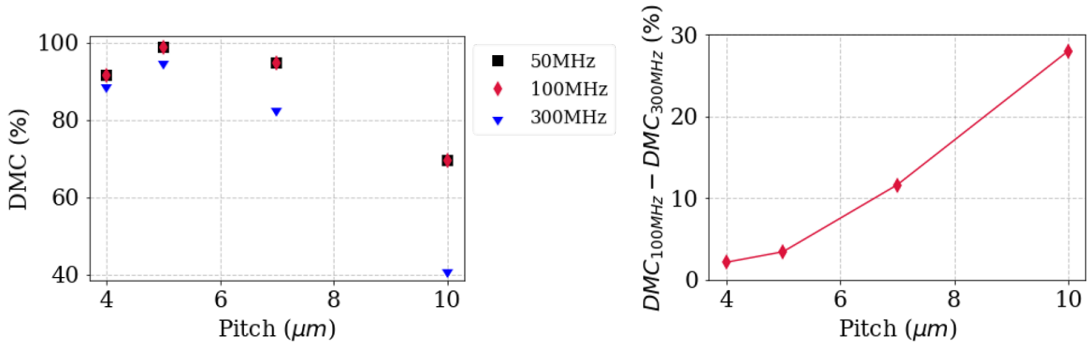


Figure 4.30: Dark and illuminated measured current response of the germanium CAPD reference pixel versus the sensing nodes biasing. During the sensing nodes sweep, both demodulators D_1 and D_2 are biased at 0.0V.

Fig. 4.31a for the DMC values with the pixel pitch decrease. The improvement is even higher for the high frequency DMC_{300MHz}, as for smaller pitches, carriers have to travel small distances before being collected in the sensing nodes. This is illustrated by the difference between low frequency and high frequency demodulation contrast in Fig. 4.31a. This is also seen in Fig. 4.31b, as the charges that are not collected during the high frequency demodulation period, increase the PLS value. Hence, the higher PLS for the larger pitch pixels.



(a) (b)

Figure 4.31: (a) 3D simulated performances in terms of low ($50MHz$ and $100MHz$) and high frequencies ($300MHz$) DMC values versus the pitch of the CAPD pixel. The size of the sensing nodes and demodulators were shrinked to that of available dimensions in silicon technology and the doping concentration is selected at $1 \cdot 10^{16} cm^{-3}$, that is a non-optimized epitaxy doping concentration. A small window of $2\mu m$ is applied for the illumination with a wavelength of $1310nm$. (b) The difference between low frequency ($100MHz$) and high frequency ($300MHz$) demodulation illustrates the advantage of the pitch reduction from $10\mu m$ down to $4\mu m$.

Conclusion

Two different possibilities were envisaged when studying the CAPD pixel integration to a commential iToF pixel. (i) Silicon CAPD and (ii) germanium CAPD.

(i) The silicon CAPD was studied from the reverse engineering of a commercially available sensor [45].

A functional solution was demonstrated in simulation. It is compatible with the reverse engineered available solution. After the demonstration, improvements were envisaged to the silicon CAPD by reducing the substrate doping concentration. With a lower doping, an improved distribution of the electric potential is expected in the volume of the device due to an improved voltage drop of the biasing applied between the demodulators. Additionally, the reduction of the doping concentration may reduce consumption. However, this reduction is not significative at the already used low doping values of the order of $10^{14} cm^{-3}$. Indeed, these low values reach the fabrication limitations.

The studied device is intended to operate at 100MHz and no isolation is integrated in the studied CAPD pixel [16, 45]. Because of that, this solution may be vulnerable to electrical and optical cross-talk. However, the key limitation is the pitch reduction. A pitch limitation of $3.5\mu m$ is identified to the CAPD pixel. This limitation is due to the increased leakage between sensing node with the reductions of the pitch. Furthermore, for smaller pitches an increase current is expected between the demodulators if they have the same implantation dimensions. This is due to the increase in hole current between the demodulators.

(ii) The germanium CAPD solution previously demonstrated in literature was envisaged [44]. This alternative can have benefits for SWIR application.

The goal was to develop a functional device in a germanium-on-silicon platform. The simulation methodology was used to identify the best design alternatives. They are front-side illumination alternatives with a highly doped germanium layer between the silicon and germanium to passivate the highly defective interface.

The limitation of the germanium CAPD is the dark signal. This is due to the nature of germanium, i.e. it is a material with a small band gap and consequently a high ionization rate. Additionally the solution may also suffer from the pixel pitch reduction limitations. This was not put into evidence with the attempted pitches as low as $4\mu m$. On the contrary the transfer efficiency was improved with the pitch reduction. Indeed, as the germanium thicknesses required for an accurate pixel are much lower, pitch limitation may firstly come from the technological limitations than from the previous leakage issue observed in silicon. The technological limitations of germanium are due to the available fabrication process which is less developed when compared to the silicon devices fabrication.

References

[10] Robert Lange. "3D Time-of-Flight Distance Measurement with Custom Solid-State Image Sensors in CMOS/CCD-Technology". In: *Sensors Peterborough NH* 222 (2000), p. 223.

[30] Yuhi Yorikado. "Tap mismatch mitigation of 3 um 2-tap pixels of indirect Time-of-Flight image sensor for high-speed depth mapping". In: *Proceedings of the 2023 International Image Sensor Workshop (IISW)* (2023).

[31] Congzhen Hu. "Compact Numerical Modeling of Indirect Time-of-Flight CMOS Image Sensors". In: *IEEE Transactions on Electron Devices* 69 (2022), pp. 6897–6903.

[37] SDevice. *Sentaurus Device User Guide*. Version S-2021.06. 2021.

[74] Syed Aon Mujtaba. "Advanced Mobility Models for Design and Simulation of Deep Submicrometer MOSFETs". PhD thesis. Stanford, CA, USA: Stanford University, 1995.

[76] Cyrus Bamji. "A Review of Indirect Time-of-Flight Technologies". In: *IEEE Transactions on Electron Devices* 69.6 (2022), pp. 2779–2793. DOI: 10.1109/TED.2022.3145762.

[77] Gabriel Mugny. "Demodulation Contrast simulation for indirect Time-of-Flight sensors based on Fast Photo-Diode". In: *Proceedings of the 2021 International Image Sensor Workshop (IISW), Online* (2021).

[79] C Jacoboni and P Lugli. "The Monte Carlo Method for Semiconductor Device Simulation". In: *Computational Microelectronics* (1989).

[80] F Rosset and A Pilotto. "A model for the jitter of avalanche photodiodes with separate absorption and multiplication regions". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 977 (2020). DOI: https://doi.org/10.1016/j.nima.2020.164346.

[81] Remi Helleboid. "A Fokker-Planck-based Monte Carlo method for electronic transport and avalanche simulation in single-photon avalanche diodes". In: *Journal of Physics D: Applied Physics* 55.50 (2022). DOI: 10.1088/1361-6463/ac9b6a.

[82] Grigorios A. Pavliotis. *Stochastic Processes and Applications*. Springer-Verlag New York Inc., 2014. Chap. Diffusion Processes, the Fokker-Planck and Langevin Equations.

[83] Andrej Suler. "Développement d ' un pixel photogate éclairé par la face arrière". In: *'PhD manuscript, HAL Id : tel-03632251'* (2022).

[84] EMVA. "Standard for Characterization of Image Sensors and Cameras". In: *European Machine Vision Association (EMVA) Standard 1288* (2021), pp. 26–31.

[85] Keita Yasutomi. “A Sub-100µm-Range-Resolution Time-of-Flight Range Image Sensor With Three-Tap Lock-In Pixels, Non-Overlapping Gate Clock, and Reference Plane Sampling”. In: *IEEE Journal of Solid-State Circuits* (2019), pp. 2291–2303.

[86] F Sun. “A Simple Analytic Modeling Method for SPAD Timing Jitter Prediction”. In: *IEEE Journal of the Electron Devices Society* 7 (2019), pp. 261–267.

5 - Trench vertical gate iToF pixel development

Introduction

The demand for high accuracy depth sensing devices with low consumption requires sophisticated pixel solutions. These solutions aim to reduce pixel pitch, sensors power consumption and continually increase sensors accuracy both for 2D and 3D imaging. One such solution is 3D sequential stacking, which involves stacking multiple wafers with different functions to fabricate complex semiconductor devices such as imagers. The 3D sequential stacking has been shown to improve pixel efficiency in terms of sensitivity and pixel pitch reduction. In addition, the read-out circuit can be relocated to a secondary stack, resulting in improved read-out performance. State-of-the-art 3D sequential stacking, integrates up to three wafers for the fabrication of the same device [99].

A schematic example of such integration is shown in Fig. 5.1. The obtained device is back side illuminated (BSI). An optical stack is integrated with anti-reflective layers for light filtering and light transmission and micro-lenses for light focusing. The full schematics is depicted in Fig. 5.2.

As semiconductor technology continues to evolve, the demand for higher resolution and more advanced imaging capabilities is increasing. This has led to the development of various pixel architectures that utilize 3D stacking technology.

The existing iToF state-of-the-art pixel has its own unique advantages and challenges and they will be discussed in detail, in this chapter, to provide a comprehensive understanding of their capabilities and limitations. Firstly, section 5.1 introduces the different deep trench isolation fabricated in the state-of-the-art pixels. Secondly, the planar gate state-of-the-art iToF pixel is studied in section 5.2. Improvement solutions are proposed in simulation for the existing planar gate iToF. Next, in section 5.3 the STMicroelectronics 2D imaging pixel is presented. To introduce this pixel, first the trench vertical gates process flow is presented and than the simulation results for the preliminary understanding of the pixel are shown [48].

Finally, sections 5.4 a new solution is proposed for an iToF pixel using trench vertical gates (TVGs). The designed pixel is named the fast photogate (FPG), after its 2D imager counterpart [48]. 2D simulation results are used for a preliminary evaluation of the FPG pixel. During this evaluation, the pixel biasing is optimized in depth and areas are identified for the studies of the next section. Then, section 5.5

presents an in-depth electrical and optical 3D simulation study of different designs. The main proposed designs are presented, and the different process alternatives and optimizations are examined. Section 5.6 compares the performance of the new solution obtained in simulation to the state-of-the-art alternatives, which it exceeds. The chapter ends with the on-going fabrication results in section 5.7 and the perspectives in section 5.8.

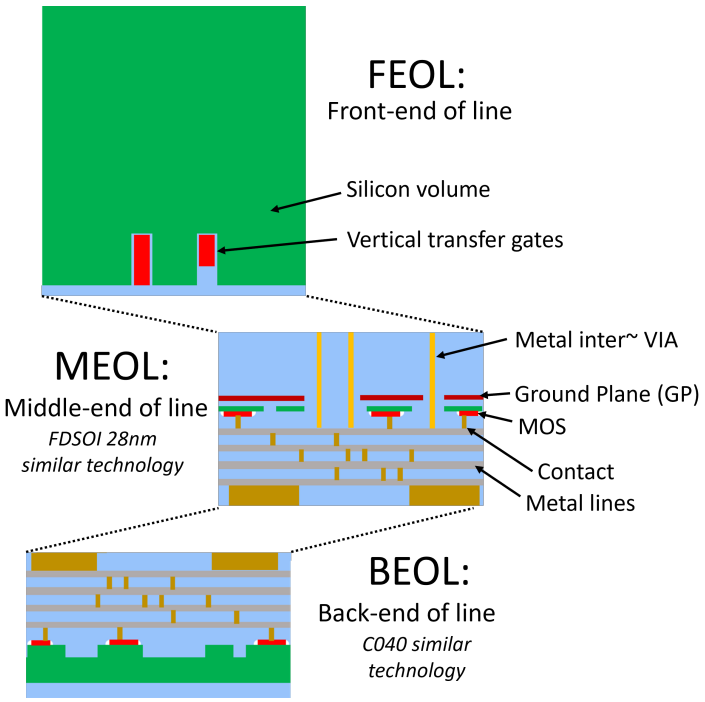


Figure 5.1: Full 3D sequential stacking with front-end of line (FEOL) imaging technology stacked to analogical circuits in a technology similar to FDSOI 28nm in middle-end of line (MEOL), stacked to back-end of line (BEOL) digital circuits [99].

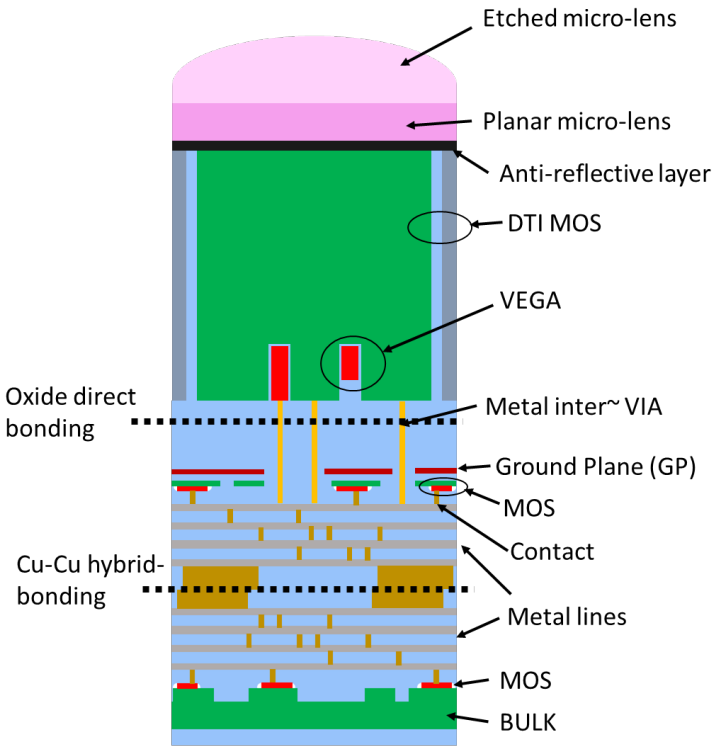


Figure 5.2: Schematic of 3D sequential stacking after back side illumination integration. The schematic includes metal-on-insulator (MOS) transistors, deep trench insulator (DTI) MOS, trench vertical gate (TVG), antireflective layer and microlenses.

5.1 Devices with deep trench isolation

Pixel matrixing makes imaging devices subject to optical and electrical crosstalk. Two types of crosstalk are distinguished. Firstly the electrical crosstalk is the percentage of charges photogenerated inside the pixel that is collected in the neighboring pixels. Secondly the optical crosstalk is the percentage of light that photogenerate collected charges in the neighboor pixel from the total incident photons over one pixel.

A solution is to use pixel trenches [76, 100]. The deep trench isolation (DTI), illustrated in a complete pixel in Fig. 5.2, is depicted schematically in Fig. 5.3. These trenches can isolate the pixel electrically or optically. Additionally, different physical mechanisms are depicted in Fig. 5.3 for the utility of these trenches. DTI efficiency against optical and electrical crosstalk will depend on how these trenches are fabricated. Simple oxide trenches can isolate pixels electrically avoiding electrical crosstalk as depicted in Fig. 5.3b. However optical crosstalk is only partially avoided (Fig. 5.3c). A part of the incident light may not be reflected by DTI only filled with silica as shown in Fig. 5.3a and can photogenerate electric carriers inside a neighbor pixel. Furthermore, the surface of the etched deep trench covered with oxide could be a source of defects. These interfaces could be a source of dark current through mechanisms of defect assisted generation and recombination (Fig. 5.3d). Indeed, an alternative to simple DTI, is the charged deep trench isolation (CDTI), that works as a deep trench metal on insulator capacitor and can remedy the dark current caused by the added defects [101–103].

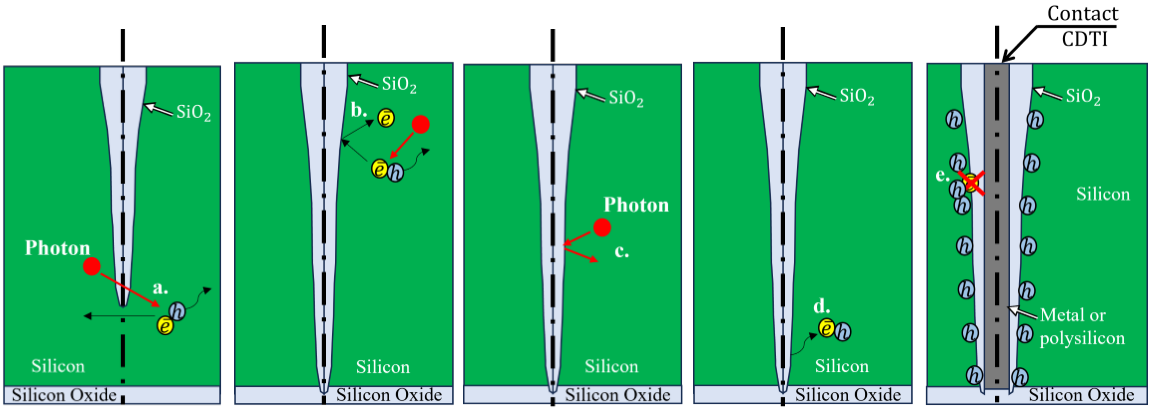


Figure 5.3: Deep trenches illustrations for (a) the optical and electrical crosstalk, (b) the DTI electric crosstalk isolation, (c) the DTI optical crosstalk isolation, (d) the electron/hole pair generation of dark charges through defects and (e) the recombination of generated electron with a hole in the CDTI passivated trench isolation.

5.1.1 Capacitive deep trench isolation CDTI

In a N-type or P-type doping silicon, the charged deep trench isolation (CDTI) is fabricated by etching trenches of a few micrometers and depositing an oxide liner. The remaining empty space can then be filled with a material that is biased, such as N-type, P-type doping polysilicon or metal, to provide different electrical and optical properties. In this section, the electrical behavior of the filing material will be covered first and then the optical behavior will be discussed.

The change to the electrical properties are due to a change to the work function depending on the filling material [34, 36]. Indeed, the CDTI behavior is similar to a deep trench MOS gate [18, 36].

The change to the optical properties are due to the change to the reflective index and absorption coefficient of the filling material. A part of the light will be reflected by the filling material and the other part will be transmitted inside of the material. For instance, a metal layer will optically isolate the pixels reducing the optical crosstalk significantly thanks to the absorption of the light transmitted to the metal layer [66, 67].

Electrical behaviour

A simplified sketch is provided in Fig. 5.4. For the collection of photogenerated electrons, the chosen doping of the silicon volume is of N-type. It will be shown in section 5.7.1 that the N-type doping will have an increased electrical field when the pixel silicon volume is fully depleted. The chosen doping for the polysilicon is of P-type, to facilitate the operation of the CDTI in strong inversion. The P-type polysilicon enables the use of lower absolute potentials, for the negative bias required for the strong hole inversion inside of the silicon N-type doping volume [34].

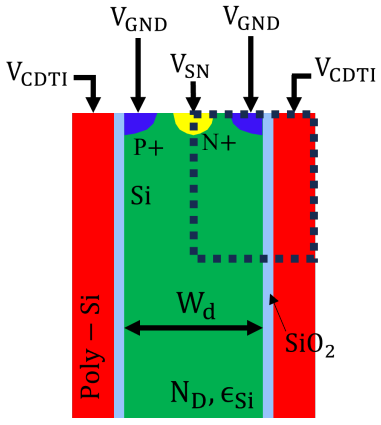


Figure 5.4: Schematic with biasing conditions of 2D TCAD simulation of CDTI with a 1D confinement. The reference biasing values used in the simulation presented later on are $2.5V$ for V_{SN}, 0.0 for V_{GND} and $-2.0V$ for V_{CDTI}.

For a device such as the one shown in Fig. 5.4 with a N-type silicon doping and P-type polysilicon, a hole inversion layer occurs in the silicon near the CDTI interface when a negative bias voltage is applied to the trench, depleting the substrate surrounding the trench. This creates a positive depleted region in the substrate, attracting holes at the interface between the substrate and the oxide liner. The entire pixel region confined by the CDTI is depleted as free carriers are swept away through electron and hole collection respectively by V_{SN} and V_{GND} contacts in the substrate. The depleted volume reaches a potential well and a low free carrier density.

Once the entire volume is depleted, V_{pixel} represents the maximum potential in the 1D cross-section of the surrounded volume. This potential depends on the potential at the interface between the silicon and the silica (V_{ox}) and the charges in the volume of the pixel. In turn, the charge concentration in the volume depends on the depleted length (W_d) and the donor concentration (N_D) in the case of a N-type doped substrate.

In Fig. 5.4, the reference bias for the electrons V_{SN} is applied to the contact over a $N+$ implanted zone in yellow and the reference bias for the holes V_{GND} is applied to the contact over a $P+$ implanted zone in blue. The 2D simulated structure doping profile is given in Fig. 5.5a. In Fig. 5.5b the electrostatic potential distribution is computed for the applied voltages of $2.5V$ to V_{SN}, 0.0 to V_{GND} and $-2.0V$ to V_{CDTI}.

The gradient of potential caused by the pinning of the volume can be useful for creating a positive electric field in the silicon substrate. Electrons will follow the potential gradient up to the $N+$ SN zone and will be collected. Fig. 5.5c,d show the volume fully depleted of electrons and holes. This leads to higher mobility values depicted in 5.5f due to the reduced coulomb scattering of charge carriers in the depleted volume. This effect can improve the photogenerated charge transfer speed inside of the imaging devices such as photodiodes.

A cross-section of Fig. 5.5c for the different substrate donor doping values N_D is shown in Fig. 5.6. The depletion potential increases with the doping concentration increase. ΔV_{pixel} is obtained with the computation of the difference of potential inside the silicon between the maximum of the depletion potential (V_{pixel}) and the potential at the silicon and silica interface (V_{ox}). For the length of confined silicon of $0.83\mu m$ with a doping concentration of $10^{16} cm^{-3}$ the obtained value is of $1.33V$. The difference between the computed values using equation (5.1) and the simulated values using TCAD comes from additional electrons and holes existing in simulation. Indeed, in a complete pixel, the electrostatic potential in the volume of the substrate will depend on multiple elements added for the fabrication of the whole device [83, 104].

$$V_{pixel} = V_{ox} + \Delta V_{pixel} = V_{ox} - \frac{W_d^2 q N_D}{8\epsilon_0 \epsilon_{Si}} \tag{5.1}$$

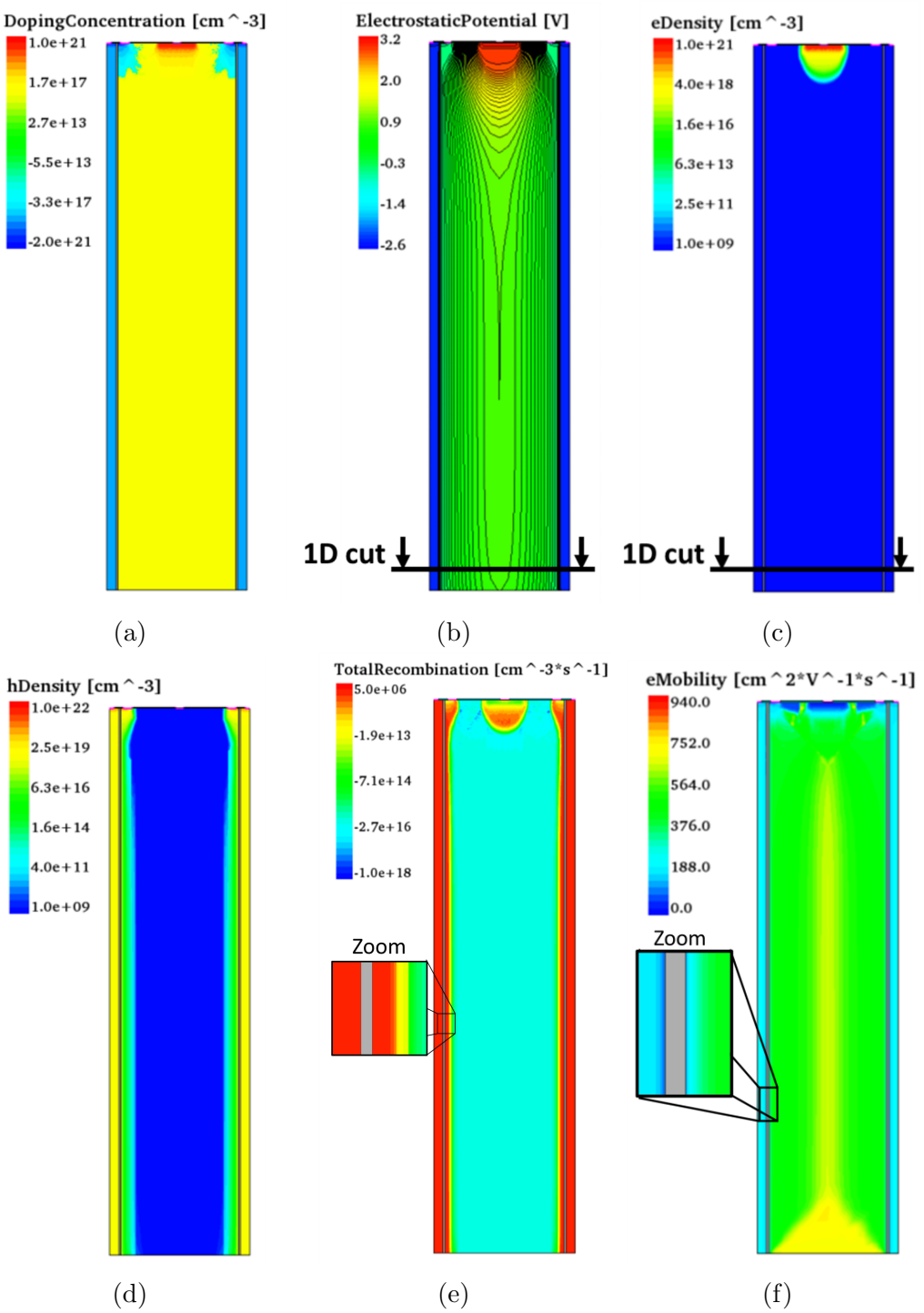


Figure 5.5: 2D TCAD electrical simulation of CDTI with a 1D confinement. The structure corresponds to the schematic given in Fig. 5.4a with the same biasing conditions.(a) The silicon volume of the simulated structure has a N-type doping concentration of a $1 \cdot 10^{16} cm^{-3}$. (b) The electrostatic potential is computed for a structure, (c) fully depleted of electrons and (d) hole inversion is observed for a negative biasing of CDTI polysilicon. (e) The total recombination show a higher recombination rate (positive values) on the field-effect passivated zone and a high generation rate (negative values) elsewhere. (f) A high mobility is observed in the volume of the device depleted of electrons and holes.

In a N-type substrate, the hole inversion from negative CDTI biasing reduces the leakage current through field-effect passivation. This process is depicted schematically in Fig. 5.3e and illustrated with simulation results in Fig. 5.5d. The high hole density, at the highly defective interface, reduces the SRH generation rate of electron and hole pairs locally in Fig. 5.5e.

The potential well created by CDTI can also help to reduce the effects of parasitic capacitance and other unwanted effects that can arise in high-density integrated circuits. By isolating adjacent circuit elements from each other, CDTI can help to minimize cross-talk and other forms of interference that can degrade the circuit performance [18].

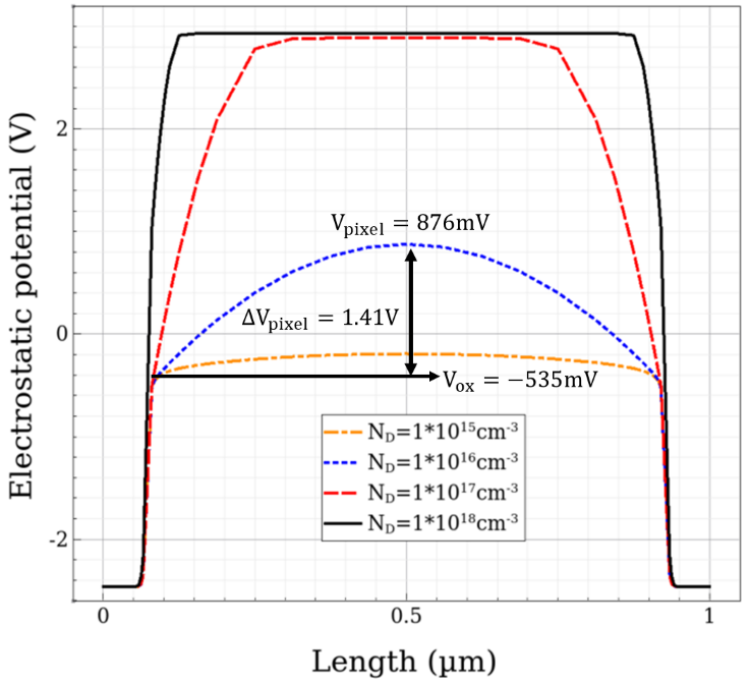


Figure 5.6: 1D cross-section over 2D TCAD simulation results shown in Fig. 5.5b with 1D substrate confinement. (a) A pinning potential is obtained in the center of the substrate depending on the substrate doping concentration N_D. The cross-section of electron concentration shows that for higher doping values the substrate is not depleted of electrons.

Optical behaviour

For a multi-layer structure between two pixels such as CDTI, the incident, transmitted and reflected optical wave powers are depicted in the schematic in Fig. 5.7. The thicknes of the oxide is identified by l_{ox} and the thickness of the filling material by l_r. The transmitted and reflected light power can be described by equation (5.2) [105]. For a wave signal of power 1, T is the transmitted power and R is the reflected power. $\tilde{H}$ is the the matrix relating the entering and exiting light power and for the depicted case it is given as in equation (5.3). The transmission and reflection of each interface is given by $T_{r,ox}$, $T_{ox,r}$, $R_{r,ox}$, $R_{ox,r}$, $T_{ox,Si}$, $T_{Si,ox}$, $R_{ox,Si}$ and $R_{Si,ox}$. The absorption coefficient in the oxide α_{ox} depends on the oxide properties and on the wavelength of the light signal,

$$\begin{vmatrix} 1 \\ R \end{vmatrix} = \tilde{H} \begin{vmatrix} T \\ 0 \end{vmatrix} \tag{5.2}$$

$$\tilde{H} = \frac{1}{T_{ox,Si}} \begin{vmatrix} 1 & -R_{ox_1,Si_1} \\ R_{Si_1,ox_1} & T_{ox_1,Si_1} \cdot T_{Si_1,ox_1} - R_{ox_1,Si_1} \cdot R_{Si_1,ox_1} \end{vmatrix} \cdot H_{ox_1} \cdot H_r \cdot H_{ox_2} \tag{5.3}$$

$$H_{ox_1} = \frac{1}{T_{r,ox_1}} \begin{vmatrix} e^{-\alpha_{ox} l_{ox}} & 0 \\ 0 & e^{\alpha_{ox} l_{ox}} \end{vmatrix} \begin{vmatrix} 1 & R_{r,ox} \\ R_{r,ox_1} & T_{r,ox_1} \cdot T_{ox_1,r} - R_{r,ox_1} \cdot R_{ox_1,r} \end{vmatrix} \tag{5.4}$$

If the filling is metallic, optical isolation is much more efficient. However, as CDTI is integrated in the front end of line (FEOL), the filling with a metal is not possible because high temperature annealing is required later on during the remaining fabrication flow. To solve this issue, an alternative to CDTI is deep trench isolation metal on insulator capacitor (DTIMOSCap) [106]. Process constraints are different from those of polysilicon CDTI. Indeed, there are process limitations on annealing when aluminum is used. The melting point of aluminum is $660°C$ [107], making it unsuitable to sustain annealing at high temperatures such as annealing higher than $1000°C$ required for the activation of dopants. Other limitations are observed for this new solution. Passivation of deep trenches through implantation or dopant diffusion is limited [101, 102, 108]

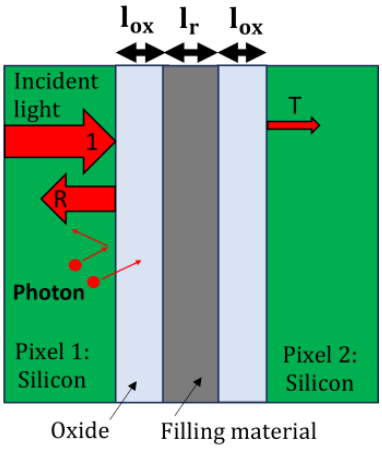
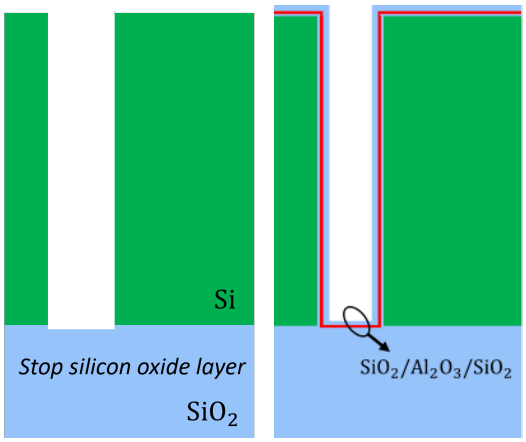


Figure 5.7: 1D optical schematic of charged deep trench isolation.

5.1.2 Passive DTI

An alternative to the polysilicon trench gates for the isolation between pixels is the use of a charged oxide layer. The solution consists of using a layer of a high-k material such as HfO_2 or Al_2O_3. By increasing the ratio of oxygen in the deposition of these oxides it is possible to increase the fixed charges concentration in the liner oxide of the DTI [109]. A thin layer of silica appears at the interface between the Al_2O_3 and the silicon. The process flow of the passive DTI is illustrated in Fig. 5.8.



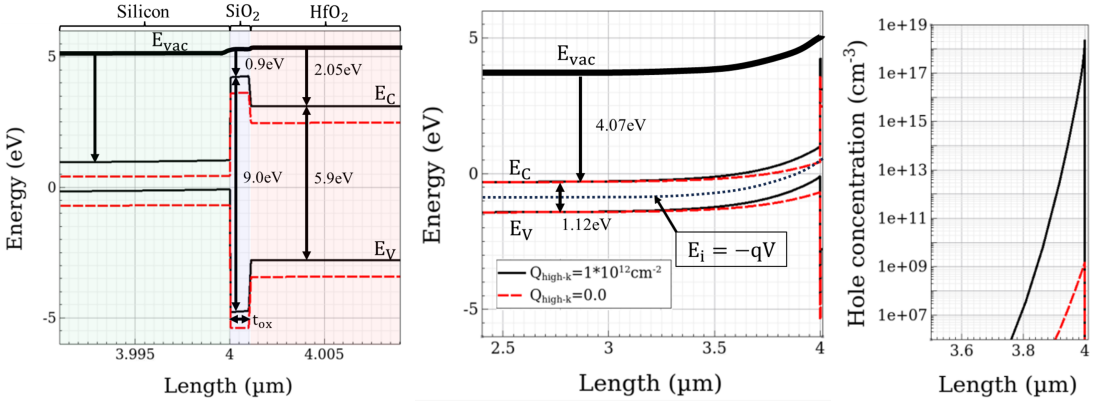
(a) Etching (b) Liner deposition

Figure 5.8: DTI flow with (a) dry and wet etching of deep trench with silicon oxide stop layer, (b) deposition of liner composed of a charged high-k oxide (Al_2O_3) and silicon oxide (SiO_2) layer in cyan, deposited in the respective order. The interface between the Al_2O_3 and the silicon has the appearance of a thin layer of silica.

Negative fixed charges from highly electronegative bonds in high-k materials will attract positive charges in the silicon. Fig. 5.9a-b shows the evolution of the conduction band with fixed charges concentration in the high-k oxide. Fixed charges concentration is computed in TCAD 2D simulation homogeneous to cm^{-2}. The fixed charge concentration is multiplied by the elementary charge q to obtain a total charge value in $C \cdot cm^{-2}$. The charge concentration Q_{high-k} per surface area in the high-k oxide causes an electrostatic field $\mathscr{E}_{ox}$ at the interface of the silicon oxide of permitivitty $\epsilon_0 \epsilon_{ox}$ as in equation (5.5) [36]. The decreasing gradient of the electrostatic field in the oxide is described by (5.6) [36], where ΔV_{ox} is the potential at the silicon substrate and t_{ox} is the silicon oxide thickness.

$$\mathscr{E}_{ox} = -\frac{Q_{high-k}}{\epsilon_0 \cdot \epsilon_{ox}} \tag{5.5}$$

$$\Delta V_{ox} = E_{ox} \cdot t_{ox} \tag{5.6}$$



(a) (b) (c)

Figure 5.9: (a) A zoom is done at the back side interface of the pixel showing the band structure of the silicon interface with SiO_2 and HfO_2. The energy level of vacuum E_{vac} is plotted with electron affinity energies for each material for two cases. In the black full lines, negative fixed charges are added to SiO_2 and HfO_2 interface, in the dashed red lines case, no fixed charges are added. (b) A broader view of the band diagrams on the silicon side show the band structure change for the cases with and without negative fixed charges added to the SiO_2 and HfO_2 interface. The electrostatic potential in the TCAD electrical simulation is relative to E_i, depicted at the silicon mid gap. (c) A strong inversion layer with high hole concentration appears on the silicon side of the interface between silicon and silicon oxide.

5.2 Planar gate iToF pixel: improvements & limitations

As seen previously, various deep trench isolation types may be used in pixels to decrease optical and electrical crosstalk and improve the transfer efficiency of photogenerated charges. The state-of-the art indirect Time-of-Flight (iToF) pixels also integrate various alternatives of deep trench isolation [17, 18].

The existing iToF imaging technology is shown in Fig. 5.10 was extensively discussed in section 1.3.3 of chapter 1 and the pixel was modeled in section 2.3 of chapter 2. The planar gate iToF pixel, utilizing a pinned photodiode and CDTI for pixel structure, exhibits certain limitations that can affect its performance. Improvements have been made in simulation to an existing pixel design. The thickness of the absorbing layer has been significantly increased to enhance quantum efficiency (QE) and the doping level of the epitaxial layer has been optimized. An optimal gradient of N-type and P-type doping has been employed. The detailed optimization of the epitaxial profile will be realized later in a new proposed solution and a comparison with an equivalent planar gate solution will be conducted. This section focuses on the limitations of the existing technology.

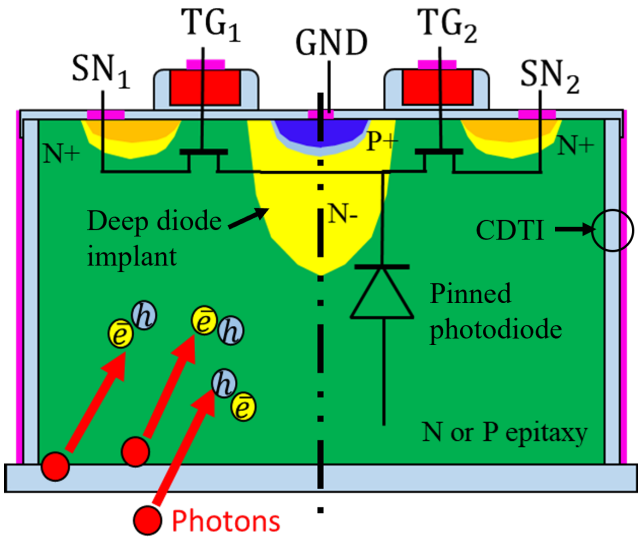


Figure 5.10: Schematic of the iToF pixel integrating a charged deep trench isolation, a pinned photodiode and the planar gates [13, 18].

One of the primary challenges is the limited capability of planar gates to effectively modulate the electrostatic potential within the pixel. 2D cross-sections of simulations of an improved existing iToF pixel are given in Fig. 5.11 to illustrate these limitations. The transfer of photogenerated charges is limited at low bias voltages, where the planar gates struggle to create a sufficiently strong potential gradient to facilitate efficient charge transfer. The pixel, previously simulated in section 2.3, was improved by replacing the P-type substrate by a gradual N-type doping concentration profile .

The final substrate doping profile with the N-type doping gradient obtained in simulation is depicted in Fig. 5.12 with a vertical 1D cross-section of the structure simulated in Fig. 5.11. The P+ and N- photodiode implants are identified. The optimization of the doping profile is limited by the minimum N-type doping concentration achieved with the in situ doping process. Additionally, a P-type gradient is integrated at the bottom of the pixel to further increase the electric potential gradient at the bottom of the device without increasing V_{pixel}. Indeed, the trade-off for this optimization is to increase the gradient of dopants to a maximum while maintaining a V_{pixel} lower than $1.2V$.

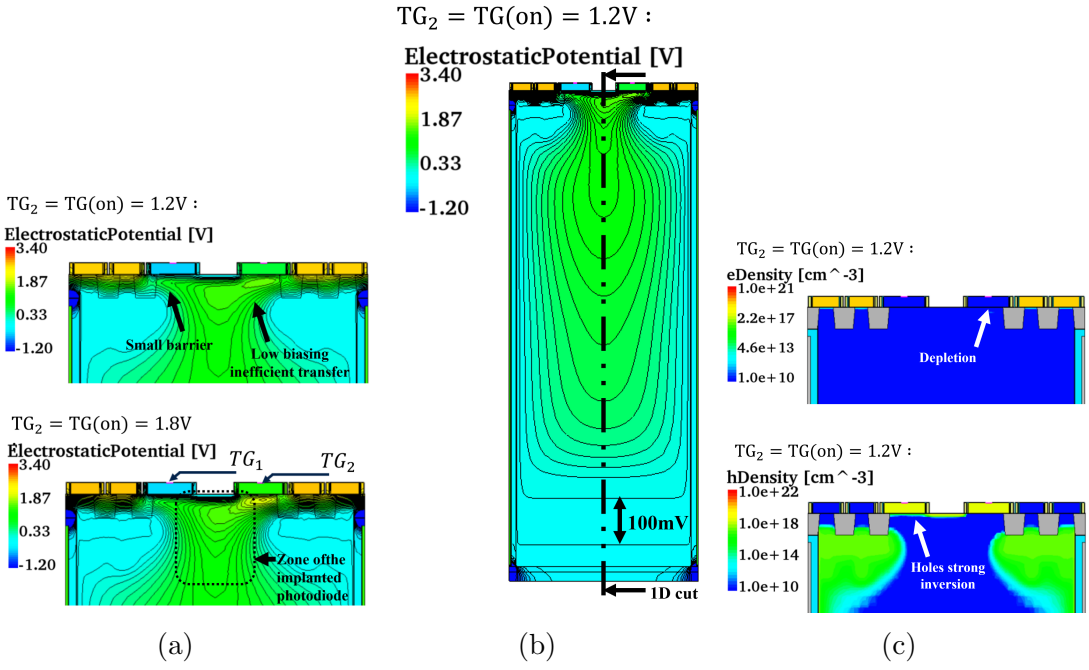


Figure 5.11: (a) A view of the top is displayed for the electric potential distribution of two different biasing (TG(on) of 1.2V & 1.8V). (b) The volume distribution of the electric potential is displayed for the TG(on) of 1.2V. (c) A view of the top of the hole and electron concentration is displayed for the TG(on) of 1.2V.

Fig. 5.11a compares two transfer gate (TG) biasing cases. The simulations demonstrate that the potential distribution can be inadequate for a lower biasing of $1.2V$, as shown when plotting the DMC value versus the biasing TG(on) in Fig. 5.13. Additionally, the potential barrier created by the low-biasing gate is insufficient, rendering the pixel susceptible to erroneous transfer of charges, which can lead to high PLS values.

Furthermore, the variability introduced by the deep diode implants depicted in Fig. 5.10, which are used to construct the pinned photodiodes, can further degrade the performance of iToF pixels. These implants are essential for defining the photodiode doping profile and are critical for its functionality. However, variations in the implant process can cause inconsistencies in the electric field distribution within the photo-

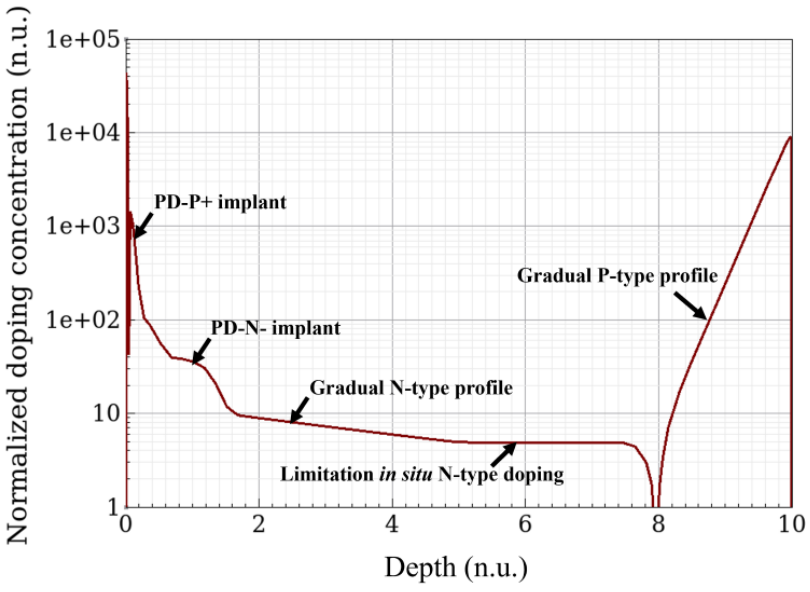


Figure 5.12: 1D cross-section of the simulated doping profile imported for the structure in Fig. 5.11b. The doping concentration and depth are presented in normalized units (n.u.) in the implanted photodiode (PD) and in the epitaxied pixel volume.

diode, leading to non-uniform charge collection efficiency across the pixel matrix. This variability can compromise the image quality and the reliability of depth information captured by the iToF system. Addressing these limitations requires careful design optimizations and advanced manufacturing techniques to improve the control over electrostatic potentials and to minimize the variability induced by the implant processes.

A novel solution presented in the next section has been developed to address the three main limitations associated with the use of planar gates in the iToF pixel technology. This innovative approach successfully overcomes the following challenges:

(i) QE versus DMC trade-off: The new design enhances QE while maintaining a significantly high DMC at low biasing.

(ii) Low barrier limitation: The solution introduces a more robust control over the electrostatic potential, effectively creating a higher potential barrier during charge transfer reducing PLS.

(iii) Variability of deep implantation: The new design does not use a deep diode. This may results in a more uniform electric field distribution and consistent charge collection efficiency across the pixel array, thereby reducing Dark Non-Uniformity (DNU) and Photo-Response Non-Uniformity (PRNU).

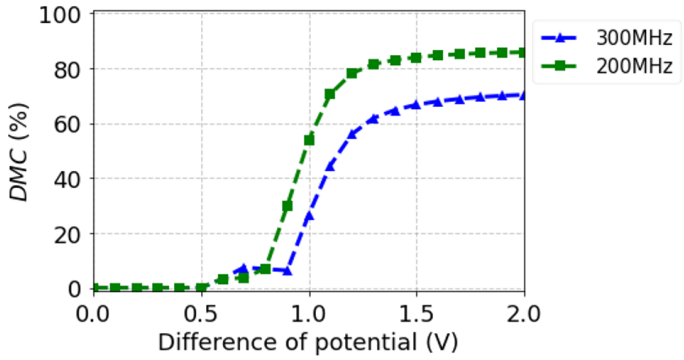


Figure 5.13: High frequency DMC versus TG(*on*) biasing.

5.3 Vertical gate 2D imaging pixel

In section 1.3.3 of chapter 1, a 2D imaging pixel using the trench vertical gates (TVGs) was briefly discussed. The pixel schematic is depicted in Fig. 5.14. The use of the TVG as transfer gate allow an efficient charge transfer in the pixel collection volume. Additionally, for a negative DC biasing, closed TVG allow the storage of a significant number of charges in the pixel sensing zone while having a low dark current [48].

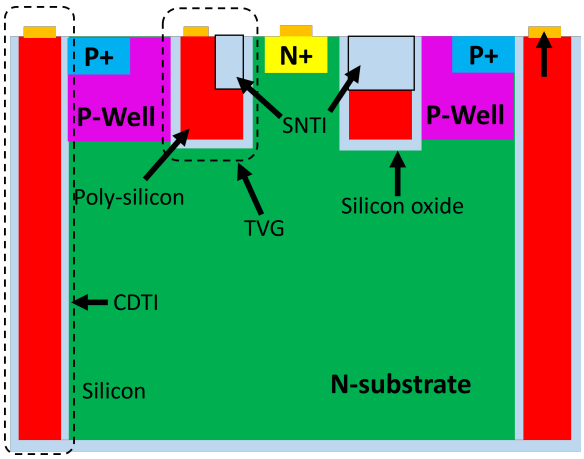


Figure 5.14: A schematic of the photogate pixel using the TVG as TG. Additionaly, it has three implants (N+, P+ and P-Well), capacitive deep trench isolation (CDTI), for electrical and optical pixel isolation and sensing node trench insulation (SNTI).

This section is decomposed in three subsections. Firstly, two key elements of the existing pixel solution will be presented. A brief section explains the detailed process flow of the TVG fabricated in STMicroelectronic. After that, a second subsection is dedicated to the sensing node trench insulation (SNTI) description. The SNTI, an alternative to shallow trench isolation in small pitch pixel, is a key fabrication step for the isolation of the top part of the TVG [48]. The third and last subsection will present a simulation study of the photogate pixel (Fig. 5.14).

5.3.1 Trench vertical gates fabrication

A trench vertical gate is a buried MOS. By filling a trench with a liner oxide and polysilicon, it is possible to create a MOS of different properties than a classical planar MOS. TVGs have shown great performance when integrated with silicon pixels for visible light detection. The state-of-the-art pixels for visible light detection integrate trench vertical gates as transfer gates (TG) due to their pinning capability [48–50, 106, 110].

The fabrication flow of the trench vertical gates is illustrated in Fig. 5.15. (i) A trench is etched in the silicon using a SiN stop layer and a amorphous carbon hard-mask. The etching of a trench is done with reactive ion etching [111] (Fig. 5.15a). (ii) The next step is the liner deposition shown in Fig. 5.15b. (iii) A step of nitruration is done to the liner oxide nitruration (Fig. 5.15c). (iv) The trench is filled with polysilicon as illustrated in Fig. 5.15d. The exceeding polysilicon is chemicaly mechanicaly polished.

To avoid electrical parasitic behaviors such as high gate contact resistance and poly-depletion, polysilicon is highly doped. However, doping the polysilicon requires successive anneals that can cause the diffusion of dopants from polysilicon through the liner oxide into silicon. To address this issue, a charge nitruration layer is integrated to create a diffusion barrier for polysilicon dopants [112].

The morphology of the trench vertical gates is constrained by the fabrication process. These fabrication limitations are translated into design rules. To achieve the specification given by the design rule manual, a large enough critical dimension must be drawn. These limitations were critical for the choice of the shape and the disposition of the vertical gates inside of the pixels.

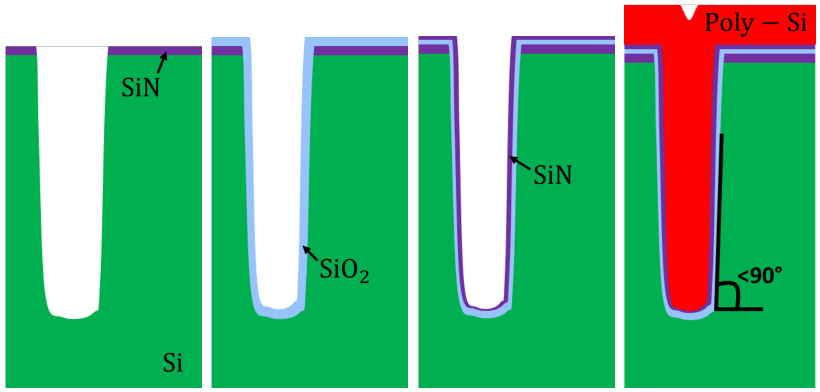


Figure 5.15: TVG flow with (a) dry RIE etching of trench, (b) deposition of liner composed of silicon oxide in cyan and (c) nitruration of oxide liner in violet, (d) polysilicon trench filling.

5.3.2 Sensing node trench insulation

Shallow trench insulators (STIs) are trenches etched into the substrate which are filled with silicon oxide. These trenches serve to isolate different devices or zones by creating a dielectric barrier to prevent electrical charges from flowing between different parts of the semiconductor. They can be used to isolate high electrostatic field zones or differently doped zones and have been of significant importance for the reduction of MOS transistor pitch [113].

In denser circuits, the decrease in device pitch has forced the transition from STI to other alternatives. The STI process is not auto-aligned to gates and implantations, causing variability when fabricating semiconductor devices with such a process. Furthermore, the use of high density STI can create stress, as silicon oxide has a different thermal expansion coefficient than silicon. An alternative to STI is sensing node trench insulation (SNTI) [83].

SNTI is created from selectively etched trenches, as shown in Fig. 5.16. The trenches are created only in zones of high interest, by selectively etching polysilicon. These zones are situated close to high dose implants and they are illustrated in Fig. 5.16d. SNTI can be auto-aligned and the selectivity of the process could allow for the integration of the process step without the use of photolithography. The polysilicon could then be contacted through vertical interconnect accesses (VIAs) etched through the SNTI. However, this could increase the complexity of the process to achieve good contacts with polysilicon, as SNTI can be thick.

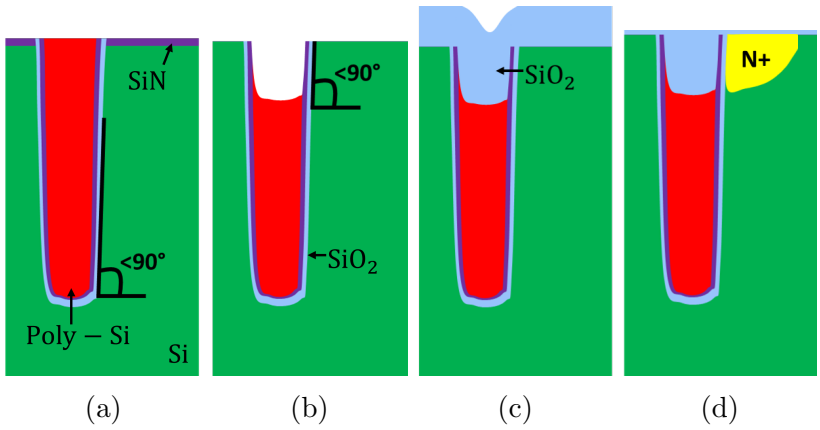


Figure 5.16: SNTI flow with (a) polished TVG after polishing, (b) selective polysilicon etched trench inside TVG, (c) silicon oxide filled trench and (e) the device after polishing and $N+$ sensing node implantation.

5.3.3 Photogate

Fig. 5.17 shows a 2D TCAD simulated structure of a pixel that integrates TVG as transfer gates. This pixel is called photogate (PG) [48]. It has a N-type doped substrate with a low arsenic concentration of $10^{16} cm^{-3}$ and CDTI for pixel isolation. In Fig. 5.17 the *P-Well* box implant serves as a hole source for the inversion of CDTI and TVG, which operates in strong inversion. A *P+* contact over *P-Well* box implants is biased at V_{GRND}. A sensing node for the collection of electrons is created between both vertical gates and is biased at V_{SN}. The CDTI polysilicon is contacted and biased at a negative DC biasing (V_{CDTI}). The TVGs are biased at V_{TG}. For global shutter operation, V_{TG} is a low biasing during the integration step as illustrated in section 2.2.1, or a high biasing during the readout (section 2.2.1).

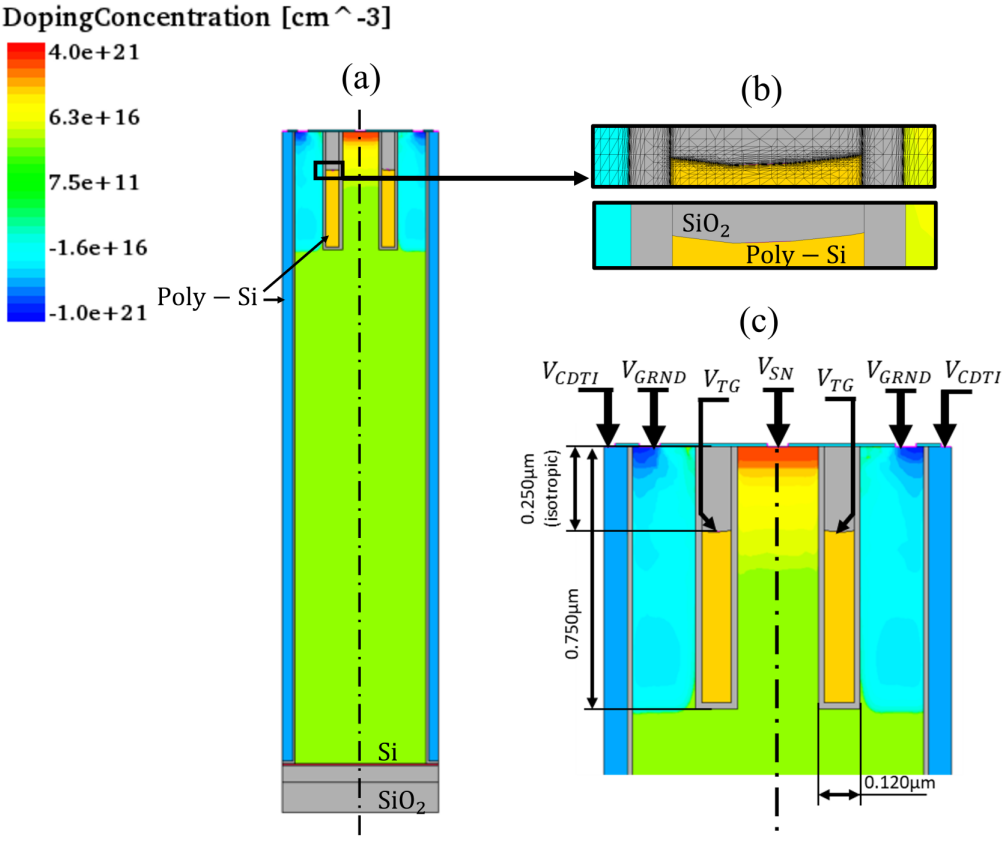
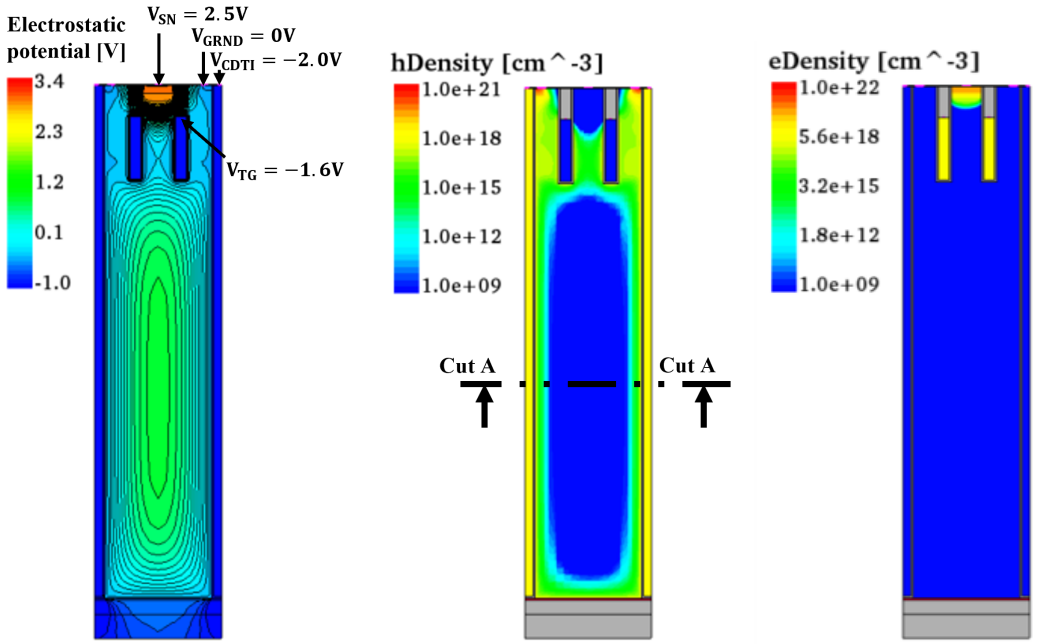


Figure 5.17: PG 2D TCAD simulated doping concentration (a) entire structure of $1.0\mu m$ pitch. (b) A zoom over the isotropic etched SNTI is shown with the used finite elements simulation meshing and (c) a zoom of the top part of the device with contacts for CDTI (V_{CDTI}), ground (V_{GRND}), TG (V_{TG}) and SN (V_{SN}) biasing.

In section 2.2.1 the different operation steps of a 2D imaging pixel have been described in detail. Fig. 5.18 and Fig. 5.19 illustrate the electrical behavior of the photogate (PG) pixel during two of these steps. Fig. 5.18 displays the obtained simulation results during the integration phase, just after reset and Fig. 5.19 displays simulation results obtained during the readout phase. The 2D TCAD simulation in Fig. 5.18a shows the electrostatic potential distribution in the volume.

Fig. 5.18b show the hole density distribution during the integration phase. The strong inversion is observed around the CDTI and TVG. Operating the TVGs in strong inversion creates a device with low dark current during integration, as the hole concentration in the interface between silicon and silicon oxide is significant and the interfaces defects are passivated. Fig. 5.20 shows the 1D cross-sections of the 2D simulated structure hole density. A hole concentration higher than $10^{18} cm^{-3}$ is attained close to the silicon oxide interface.

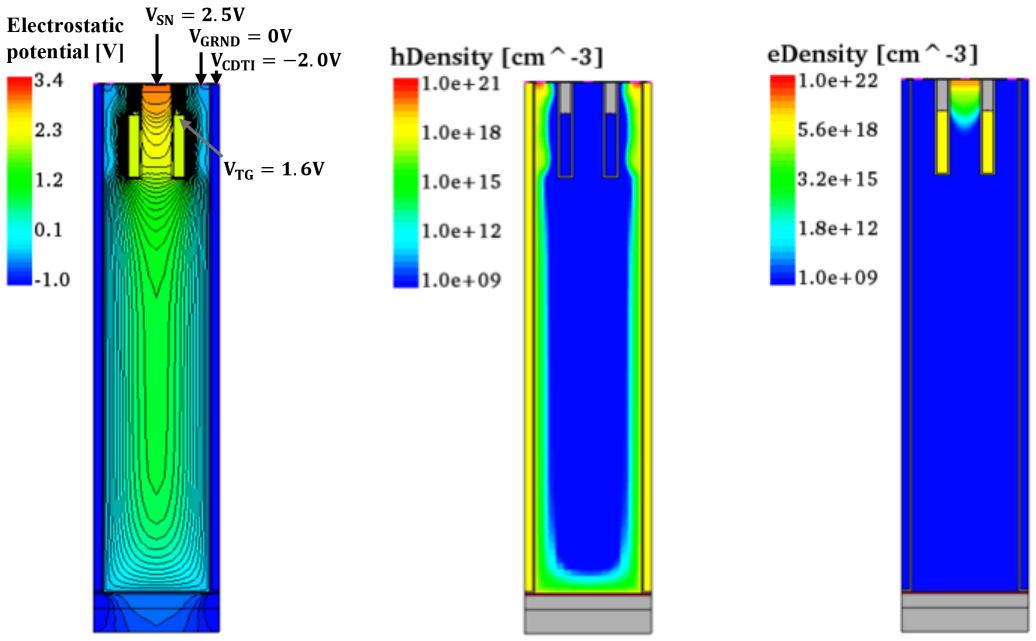


(a) (b) (c)

Figure 5.18: PG 2D TCAD simulation with structure illustrated in Fig. 5.17 with V_{CDTI} biased at -2.0V, V_{SN} at 2.5V, V_{GRND} at 0.0V. For TG off, just after reset, during integration with a V_{TG} biasing of -1.6V (a) electrostatic potential distribution, (b) hole concentration and (c) electron concentration.

It is important to note that 2D simulation has limitations. For example, it does not consider the pinning of a 3D constraint volume, which will reduce not only the pixel depletion potential (V_{pixel}), but also the absorption volume [83]. However, 2D simulation can still help in understanding complex devices and show relevant trends. With the correct approach, the values obtained from 2D simulation can be adjusted to match the measured values. This is demonstrated in Fig. 5.22, where the TVG 2D simulation AC-analysis results are compared to the capacitance measurement results.

A photogate TG capacitance value is measured and compared to a 2D simulated



(a) (b) (c)

Figure 5.19: PG 2D TCAD simulation with structure illustrated in Fig. 5.17 with V_{CDTI} biased at -2.0V, V_{SN} at 2.5V, V_{GRND} at 0.0V. For TG on, during readout, with a V_{TG} biasing of 1.6V (a) electrostatic potential, (b) hole concentration and (c) electron concentration.

structure. The schematic of structure that illustrates the measured device is depicted in Fig. 5.21. The 2D capacitances obtained for the presented 2D structure is compared to capacitance values measured in a 3D fabricated device. Fig. 5.22 displays the normalized capacitance simulated and measured results versus the voltage $-V_{in}$. Despite the differences between the simulation and the measurement, a reasonable match of the depletion capacitance (C_D) is obtained by adjusting the simulated capacitance versus voltage curve to match the gate oxide capacitance (C_{ox}). The match obtained for C_D is explained by the depletion volume around the TVG. As the silicon substrat is confined, the total silicon volume is depleted of free carrier. Hence, no change is expected for the depletion length between the 2D and the 3D simulation cases. Because of that, the surface normalization that allow to obtain a normalized C_{ox} is also applicable to the value of C_D when the whole confined silicon volume is depleted. The volume fully depleted of electrons is simulated and presented in Fig. 5.18c and Fig. 5.19c.

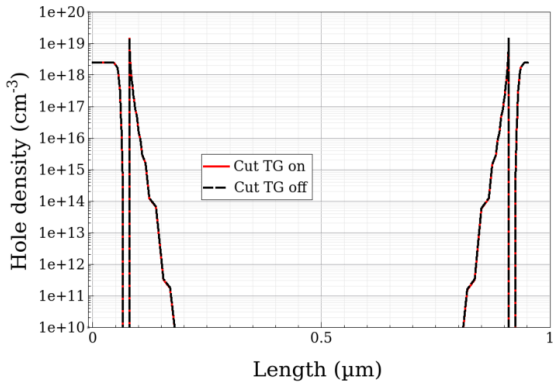


Figure 5.20: 1D cross-sections of 2D TCAD hole density simulation in Cut A at Fig. 5.18b.

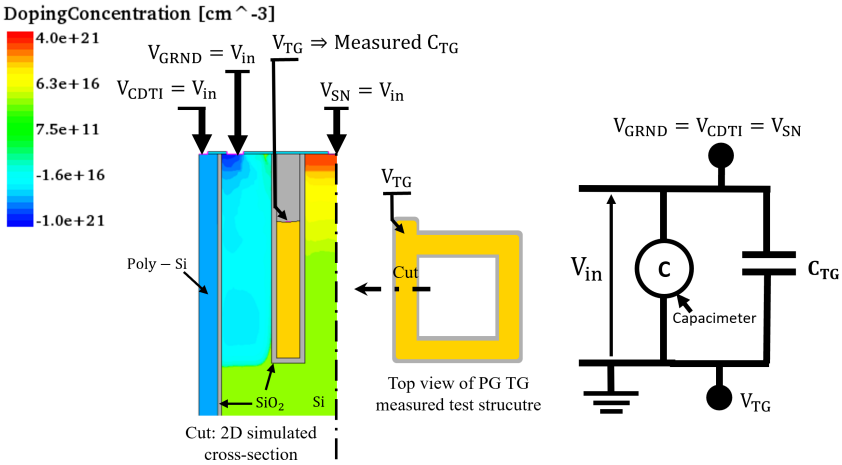


Figure 5.21: Schematic representation of the measured PG pixel. A simulated cross-section of the top view of the fabrication TVG device illustrates how the device is biased. The measurement set-up is illustrated with a simplified circuit, where the input voltage V_{in} is applied to the CDTI, GRND and TG nodes.

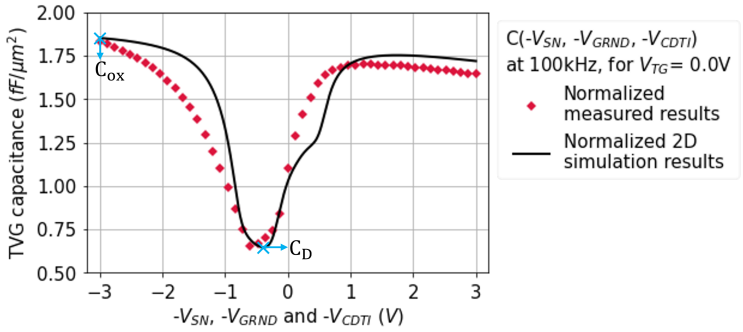


Figure 5.22: Comparison of the 2D simulated capacitance with the measured capacitance of the TVG in a PG test matrix structure at 100 MHz. The TVG has N-type polysilicon. The measured capacitance is normalized by the total gate liner oxide surface. The 2D simulated capacitance is normalized by a constant factor that aligns the value of the simulated curve with the C_{ox} value indicated in the graph.

5.4 Vertical gate iToF pixel

In the previous section, an example of an existing 2D imaging pixel with trench vertical gates, known as the photogate, was presented. The pixel was simulated, and the advantages of the TVG, the key element of the photogate structure, were discussed. This section proposes a new solution that integrates the TVG for iToF pixels, referred to as the fast photogate pixel (FPG). To introduce and understand the FPG pixel, this section is divided in four parts. Firstly, in subsection 5.4.1, an illustration of the pixel is provided with a simplified cross-section schematic. It is accompanied by an equivalent 2D simulated structure. Secondly, in section 5.4.2, a preliminary simulation study of the pixel impulse response is presented to qualitatively evaluate the charge transfer efficiency. In section 5.4.3 the choice of the N-type polysilicon doping is explained through the FPG pixel biasing and consumption study. Finally in section 5.4.4 the pixel biasing is optimized for a 2D image acquisition.

5.4.1 Fast photogate pixel schematic

A cross-section of the simulated structure is presented in Fig. 5.23. A small pitch FPG iToF pixel using the TVGs is proposed for increased efficiency in charge transfer. Three implants are necessary: $^{(i)}$sensing nodes SN_1 and SN_2 N+ implant, $^{(ii)}$ground GND P+ implant and $^{(iii)}$deeper P- box implant. Later, in section 5.5, pixel structures will be shown in which the 3D shape of the TVGs differs from the 2D cross-section presented in this section. The polysilicon composing the TVGs is of N-type doping. The reason behind this choice will be elaborated in detail in section 5.4.3. The pixel is surrounded by deep trench isolation biased at V_{DT}. Deep trench MOS operates with negative DC biasing in strong hole inversion regime and fully depletes the pixel volume [48].

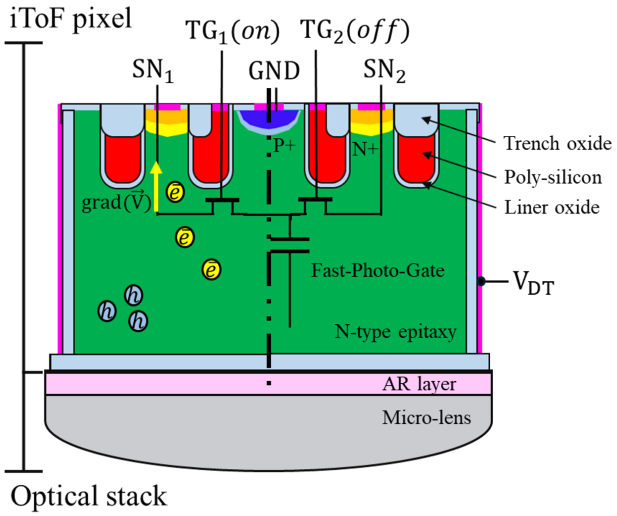


Figure 5.23: FPG iToF pixel schematic cross-section of the simulated structure with trench gates, contacts and pixel deep trench isolation biased at V_{DT}.

In this section, to introduce the operation of the the FPG pixel, a 2D structure is simulated. It is depicted in Fig. 5.24. In Fig. 5.24a a zoom at the top of the structure is done to facilitate the comparison with the reference schematic described previously in this section.

An optimal potential gradient is achieved by combining a gradual N-type and P-type doping profile. The detailed optimization of the epitaxial profile will be realized later in 3D simulation of the new pixel. For the introduction of the FPG pixel, a reference doping profile is selected. The simulated absolute net active concentration is present in the complete 2D structure given in Fig. 5.24b. A 1D cross-section in the expected charge transfer direction is shown in Fig. 5.24c. The gradual net active concentration is strictly increasing to favor the charge transfer.

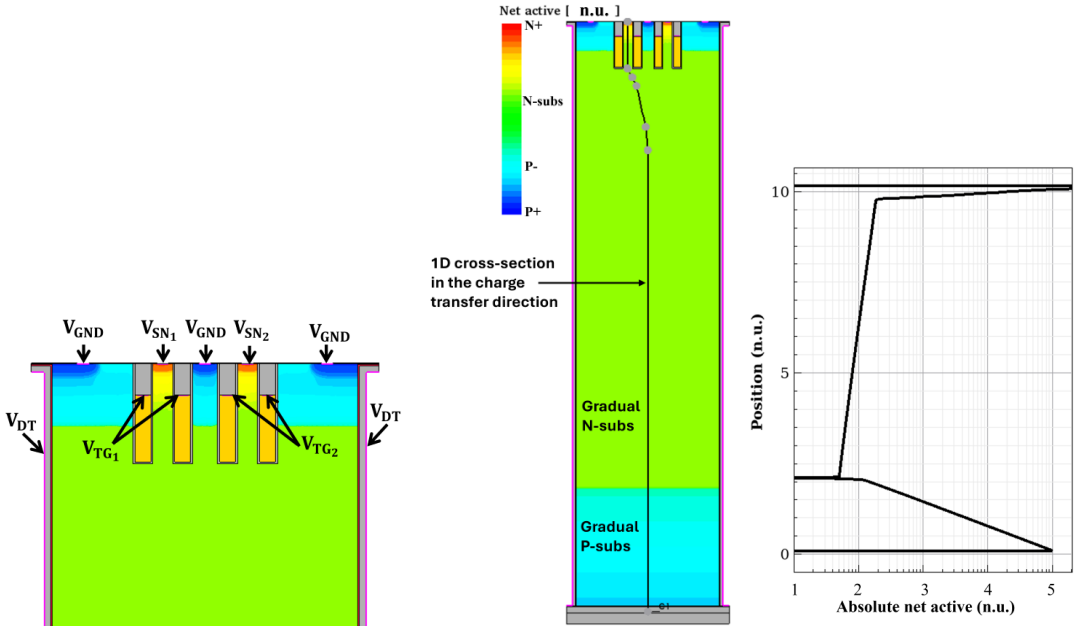


Figure 5.24: 2D simulated FPG pixel structure. (a) A structure top view is presented to facilitate the comparison with the reference schematic given in Fig. 5.23. (b) A complete view of the whole pixel shows a combined N-type and P-type gradual net active profile. (c) A 1D cut is realized in the expected charge transfer direction to illustrate the gradual absolute net active concentration in normalized unities (n.u.).

5.4.2 Pixel electrical response simulation

The pixel presented in the previous section is simulated and an overview of the electrical TCAD results is presented in Fig. 5.25. The simulated biasing is illustrated in Fig. 5.25a. The electrostatic potential distribution obtained in the pixel volume is shown in Fig. 5.25b. A 1D cut over the 2D simulated structure, in Fig. 5.25c, shows the strictly increasing potential in the charge transfer direction. Consequently, the electric field is strictly positive, favoring an optimal and fast charge transfer.

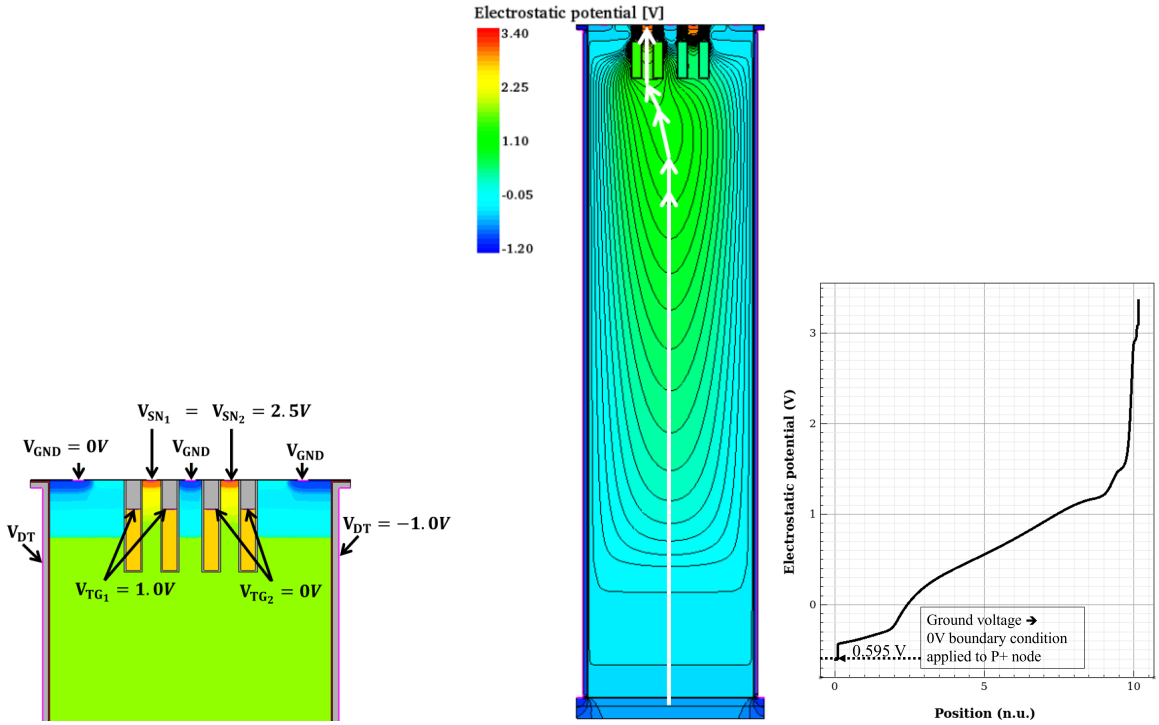


Figure 5.25: 2D simulated FPG pixel structure. (a) A structure top view is presented to illustrate the pixel simulation biasing. (b) A complete view of the entire pixel shows the electrostatic distribution within the pixel volume. (c) A 1D cut is made in the expected direction of charge transfer, with strictly increasing potential.

In the electrical simulation, a light impulse stimulus is used to extract the current response, which is measured in the sensing nodes SN_1 and SN_2 for the bias condition illustrated in Fig. 5.25a. The photogeneration impulse integrated in the volume and the corresponding response in both sensing nodes are depicted in Fig. 5.26. The used illumination has a uniform distribution in the volume of the pixel. The integration of the measured current values gives the collected charges in time for each sensing node. Fig. 5.27 shows the percentage of charges collected in SN_1 and SN_2. Despite the non-optimized uniform distribution of photogenerated charges, they are collected almost entirely in SN_1.

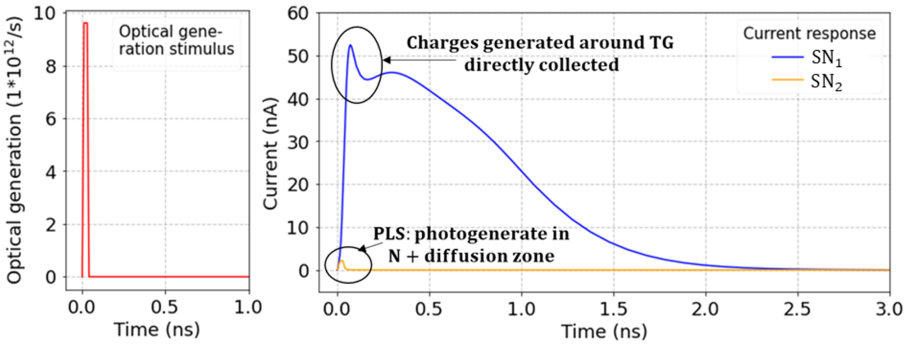


Figure 5.26: Simulated photogeneration pulse and impulse response for a uniform photogeneration distribution in the volume of the pixel.

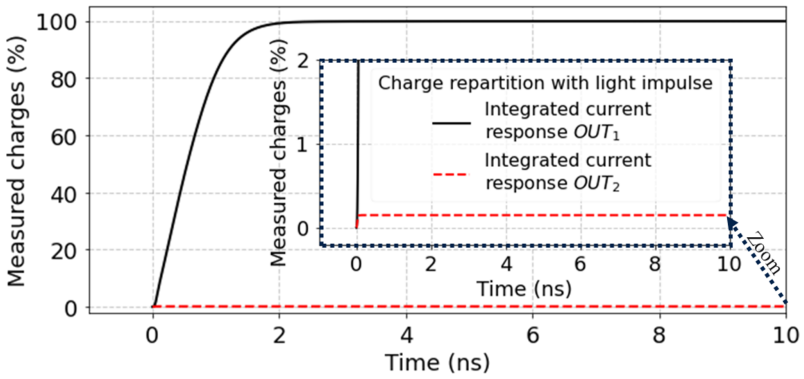


Figure 5.27: Simulated charge percentage in time. The charge response is obtained by integrating current response for a light impulsion stimulus.

5.4.3 Pixel biasing and consumption

TVGs with polysilicon doped phosphorus (N-type), were compared with boron (P-type) doping. Fig. 5.28 shows the evolution of capacitance versus the biasing of TVG. The capacitance values are computed from small signal AC-analysis simulation in 2D TCAD. The shift in V_T with the use of N-type doped polysilicon can reduce capacitance up to 30% in the interval of 0.0V to 1.0V. The capacitance with real application is also simulated by applying 2.5V to sensing nodes SN_1 and SN_2. The simulation is performed at low and high frequencies. As the pixel is already fully depleted, no high frequency change with C_D is observed. $\widehat{C}_{TG}$ is computed to 1.0fF per gate and C_{par} is approximated to 0.5fF per gate. Simulated structures in Fig. 5.29(c,d) illustrate, using hole and electron densities, the depletion regime between $V_{TG}(on)$ 1.0V and $V_{TG}(off)$ 0.0V.

For the same biasing, electrostatic potential lines are homogeneous from bottom to sensing nodes with no barrier observed for TVG high biasing of 1.0V, Fig. 5.29a-b. The barrier observed with gates biased at 0.0V is significant and sufficient to prevent parasitic signal collection in SN_2, fig. 5.27. It is observed with Fig. 5.29 that the polysilicon doping choice is suitable for iToF operation and that an accurate demodulation with TVG can be achieved while operating entirely in the depletion regime.

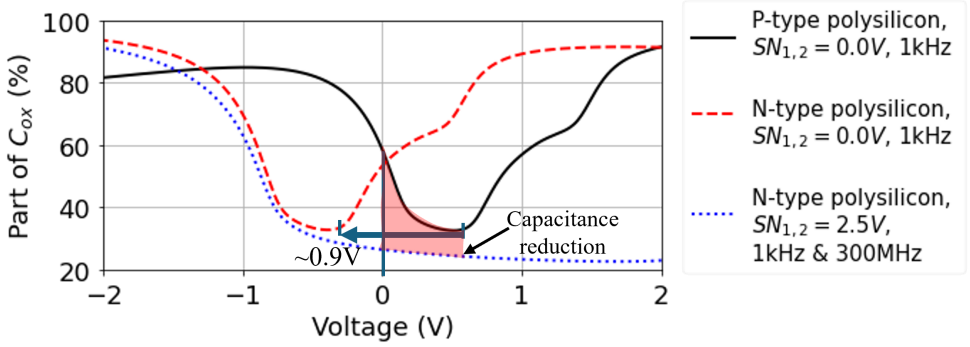


Figure 5.28: Capacitance function of gate biasing for polysilicon different doping types. A different reference potential for electrons is attempted for SN_1 and SN_2 for low and high frequencies. GND reference biasing for holes is 0.0V.

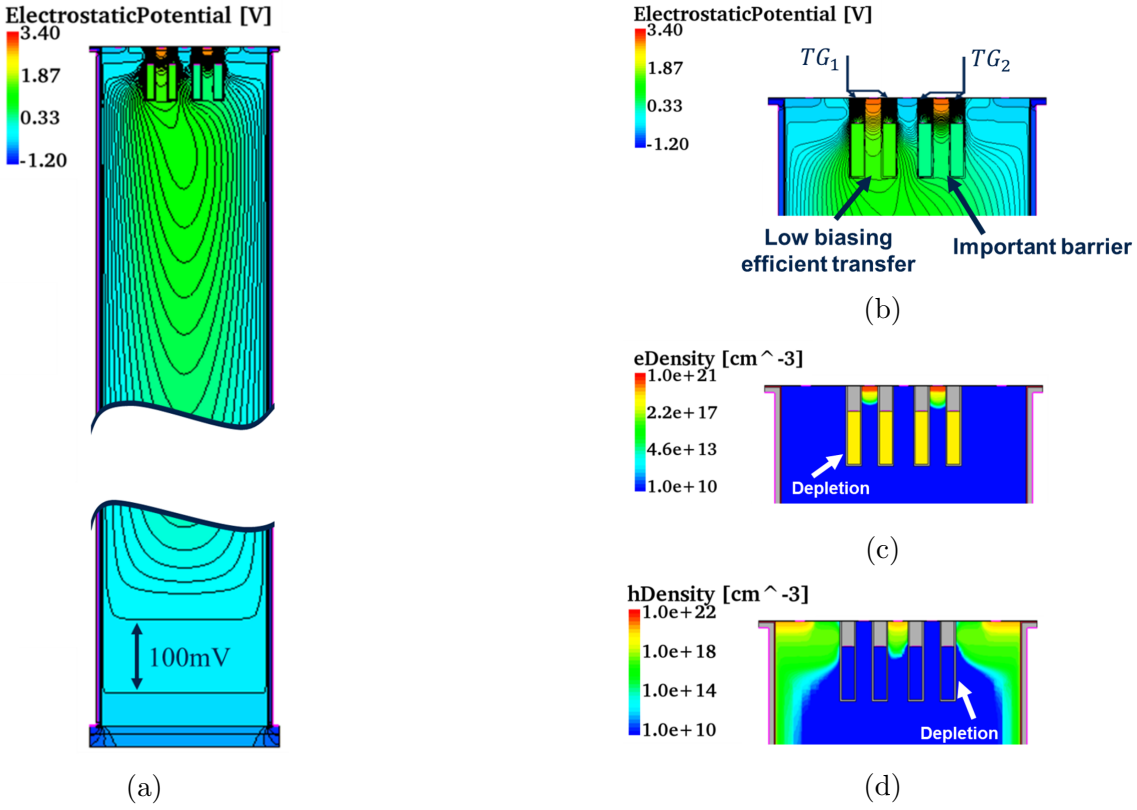


Figure 5.29: FPG pixel electrical simulation operating in 3D mode. TG_1 is biased *on* with 1.0V and TG_2 is biased off with 0.0V. Cross-section (a) a view of the sensing volume electrostatic potential with equipotential lines each 100mV, (b) TVG transfer and potential barrier, (c) electron density for high TG biasing depletion regime and (d) hole density for low TG biasing depletion region.

5.4.4 2D mode biasing optimization

The proposed FPG iToF pixel can also be used to acquire a 2D intensity image. Although optimization focuses on 3D depth imaging, a complementary simulation study evaluates the fullwell capacity of the proposed pixel. The methodology presented in section 2.2.2 is used.

Strong hole inversion is expected for a biasing lower than -1.0V when using the N-type polysilicon doping shown in Fig. 5.28. For a lower negative bias e.g. TVG at –1.6V, a significantly high potential barrier is achieved, Fig. 5.30. When this low bias is applied to the TVG, the photogenerated electrons are stored in the depleted pixel volume. This high potential barrier prevents the free charges in the volume from leaking to the output nodes. At a later time, transfer gates are activated for the readout of electrons stored in the pixel volume.

Fullwell capacity is estimated over 16,000 electrons in the studied case and it increases as the barrier height increases. Fig. 5.30 shows that a trade-off exists between 2D and 3D metrics, namely fullwell capacity and DMC versus $TG(off)$ bias value. A $TG(off)$ bias value of 0V is chosen here for iToF operation. This is the ground voltage for the TG driver power supply.

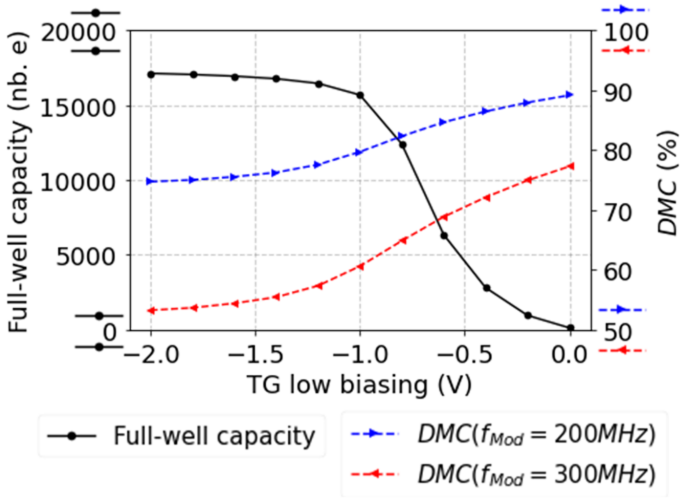


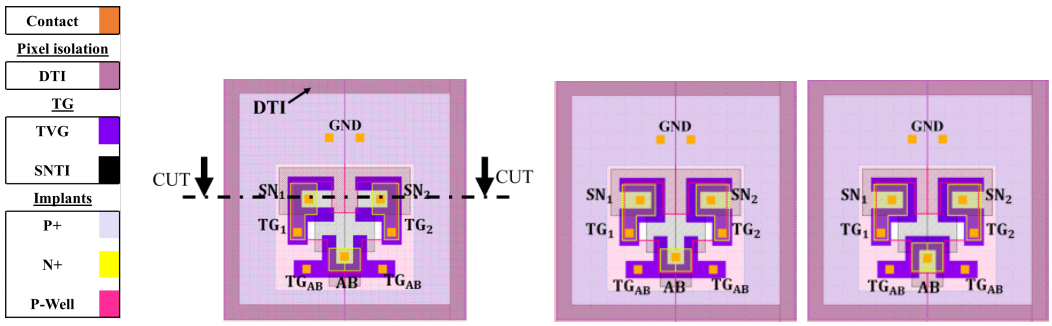
Figure 5.30: Electrical simulation fullwell and DMC results for FPG operating in 2D and 3D modes versus TG(off) biasing for 1.0V *on* biasing.

5.5 Fast photogate proposed designs

Multiple designs are proposed for the fabrication of the FPG solution. The proposed solution aims to maximize the FPG pixel accuracy, while being a feasable solution to integrate to a 300mm fabrication line at STMicroelectronics.

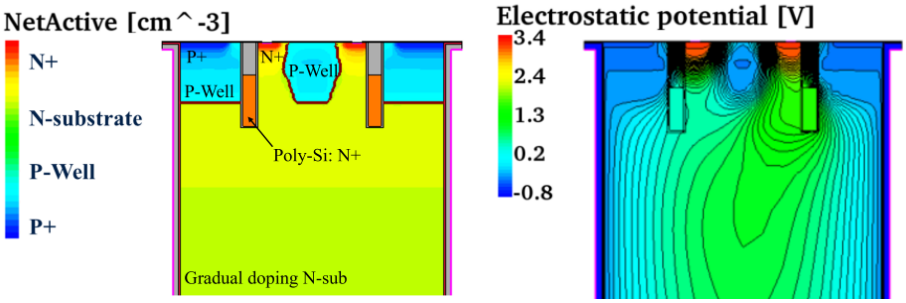
The proposed designs are 3-wafer stacked sensors. Hence, the designs must be compatible with the used technology fabrication process [99]. That means that the pixel is constraint to the design rules of the used technology. To be capable of integrating all required MOS transistors and the vertical gates a pitch of $2.79\mu m$ was selected. Additionally, the realization of TVGs with SNTI and suitable contacts impose a limited number of shapes for TVGs. A few of the envisaged variants are depicted in Fig. 5.31. The depicted designs have two TVG TGs (TG_1 and TG_2), two SNs (SN_1 and SN_2), an antiblooming node (AB) and a TVG antiblooming TG (TG_{AB}). In chapter 1, section 1.4.4, the iToF pixel circuit and the antiblooming use where briefly explained. 3D simulation are carried out for the designed variants with this three key TVGs.

Fig. 5.32 shows a 2D cross-section of the process and electrical simulation of the reference variant (V1) shown in Fig. 5.31a. Aiming to facilitate the transfer of charges photogenerated at the center of the pixel, the shape of TVG in the reference layout is opened at the center. To avoid a possible leakage between the sensing nodes, the *P-Well* implant is prolonged at the center of the pixel. However, this implant could impede the correct transfer of charges depending of mismatches between the fabrication flow and the simulation flow. Because of that, other designs were integrated where the *P-Well* implant does not cover the center of the pixel. One of these other designs is illustrated in the following section.



(a) (b) (c)

Figure 5.31: Different pixel designs with different TVG mask shapes are proposed. (a) The pixel of reference (V1) has TVG drawing opening oriented towards the center of the pixel. (b) The design V2 has TG_1 and TG_2 TVG drawing variations with the opening oriented towards the edge of the pixel and TG_{AB} TVG drawing oriented towards the center of the pixel. (c) The design V3 has TG_1, TG_2 and TG_{AB} TVG drawing variations with the opening oriented towards the edge of the pixel.



(a) (b)

Figure 5.32: 2D cross-sections of the 3D simulation of the pixel of reference (V1). The corresponding cut line and design are illustrated in Fig. 5.31a. (a) The doping concentration top view of the pixel is used to identify the differently doped zones with each of the used implants (i.e. N+, P+ and P-Well). (b) The electrostatic potential top view, show an efficient transfer for a TG_1 biasing of 1.0V, TG_0 at 0V and sensing nodes (SN_1 and SN_2) at 2.5V. TG_{AB}, AB and GND are also biased but can not be seen in this same 2D cross-section. They are biased respectively at -1.6V, 2.5V and 0V.

5.5.1 Design variants

To identify the limitation of one of the variants without the *P-Well* implant at the center of the pixel, different pixels were simulated in 3D. The simulated layouts are shown in Fig. 5.33. They have different distances between the drawings of the N+ sensing node implants.

The pixel is biased entirely in DC. TG_1 is biased at TG(on) equals $1.0V$ and TG_2 is biased at TG(off) equals $0V$. TG_{AB} is biased at TG(off) equals $-1.6V$, at strong inversion (Fig. 5.28). V_{GND} is biased at $0V$, SN_2 and AB are biased at $2.5V$ and SN_1 is swept from $2.5V$ to $0.5V$. While sweeping the biasing of SN_1 (V_{SN_1}) the current collected at SN_1 is also measured. From the total current at each biasing configuration it is possible to compute the corresponding dark signal, i.e. the unity (u.) of parasitic electrons. The obtained value of normalized dark charge signal versus the biasing of SN_1 is depicted in Fig. 5.34.

To maintain a suitable contrast value, a difference of potential between sensing nodes higher than $1.5V$ is a safe choice, i.e. no leakage from SN_1 to SN_2, for V_{SN_1} equals $1.0V$ while V_{SN_2}, the biasing of SN_2 equals $2.5V$. The variants with a distance higher than $550nm$ between the SN N+ implant mask are the suitable choices. Hence, an additional variant is selected from Fig. 5.33, it is labeled V4 and it corresponds to the layout with a distance of 550nm between the sensing node N+ implant drawings shown in Fig. 5.33b.

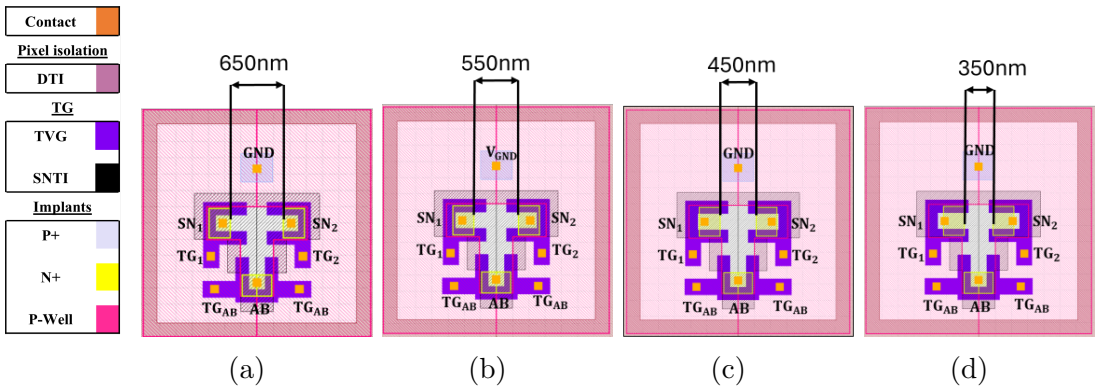


Figure 5.33: An additional design is envisaged to validate that the P-Well implant in the center of the pixel may not be needed. In simulation different distances between the N+ implants of the sensing nodes are attempted and the design (V4) is identified as having the optimal dimensions.

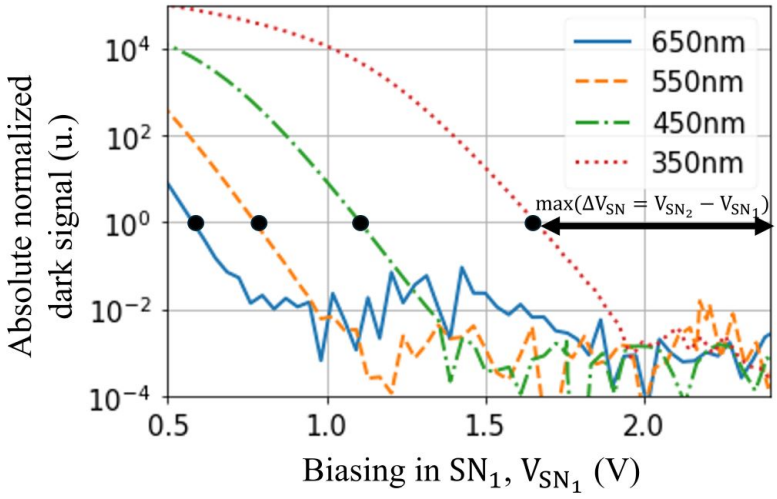


Figure 5.34: Dark signal in unity of charges versus the biasing applied to SN_1 for a DC biasing of SN_2 equals $2.5V$. A line is drawn for the leakage limitation at 1 electron per second. This dark signal limitation gives a corresponding maximum voltage different between the sensing nodes during the operation of the pixel.

5.5.2 Optical simulation of the reference pixel

In optical simulations, a complete stack was built, integrating micro-lens, antireflective layer, light structuration, metallic routing layers and deep trench insulator between pixels. The pixel is intended to detect NIR light of 940nm wavelength. The light power traveling inside of the pixel at different moments during the optical simulation is depicted in Fig. 5.35. The silicon volume, where the absorption of the light occurs is identified with a yellow dotted square line.

Optical stack optimization is required for each variant. For this reason, optical simulations were primarily used to simulate QE for the best pixel cases. The light absorption map obtained with FDTD was imported into the electrical simulations, which confirmed that all photogenerated charges in the pixel volume were collected in the sensing nodes. Since all charges were collected, the simulated percentage of light absorption corresponded to the QE value. In contrast, the DMC values presented later in this chapter were simulated using a uniform optical generation distribution in the pixel volume. This allows for the comparison of different designs without optimizing the optical stack for each individual design variant. A QE of 40% can be obtained with a thick collection volume, and the parasitic light signal (PLS) measured in SN_2 is close to 0%.

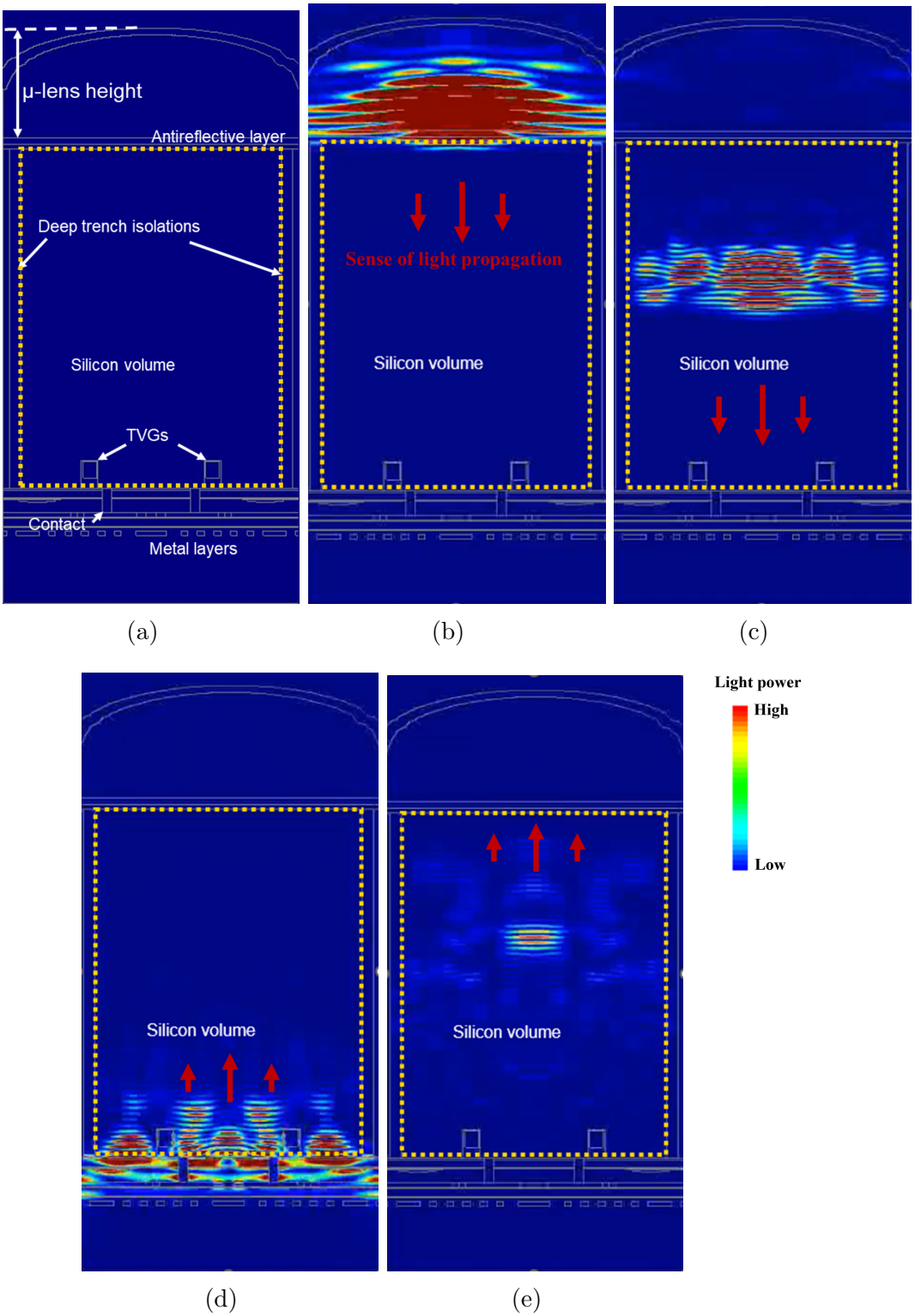


Figure 5.35: 2D cross-sections of 3D lumerical simulation of the FPG pixel. (a) The entire optical stack is label and (b, c, d & e) the different moments in time are presented during the light propagation inside the pixel. The silicon absorbing volume is identified with the yellow dotted square line.

5.5.3 Process splits

The reference pixel design (V1), presented in the previous sections, is used in this section to study multiple process splits.

SNTI depth & N+ optimization

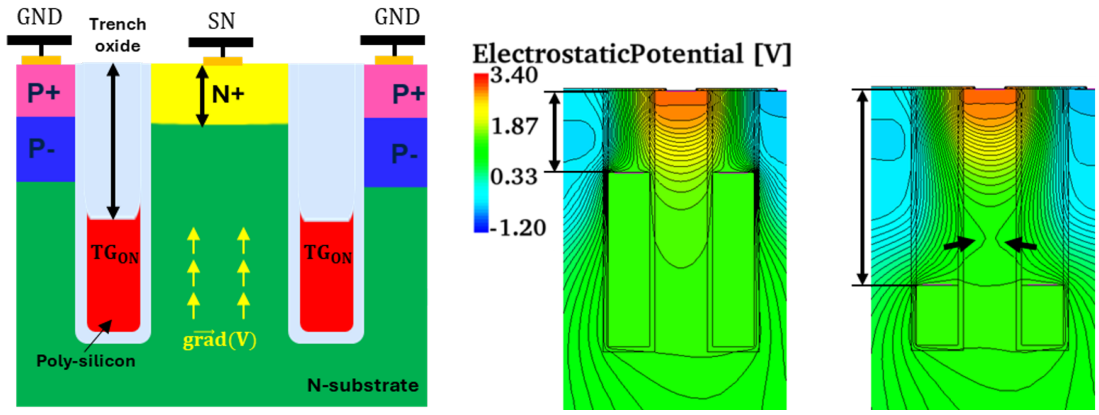
Sensing node trench insulator (SNTI) depth is identified as a crucial process parameter for the improvement of the pixel. Originally, the SNTI brick is intended to avoid leakage due to high electric field between TVG from highly doped zones [83]. Herein, aiming to reduce TVG oxide capacitor C_{TG}, deeper SNTI is proposed. With SNTI depth increase, shallow N+ sensing nodes can present transfer issues. Fig. 5.36 illustrates the problem identifying in Fig. 5.36c a zone where potential pockets preventing proper charge transfer can appear between N+ diffusion zones and TGs for deeper SNTI.

An optimum depth of SNTI is identified by the maximum of the figure of merit (FoM) presented in Fig. 5.37. The FoM relation is given in eq. (5.7). It consists in the ratio between DMC and power consumption for one TVG. Fig. 5.37 shows that a DMC at 200MHz over 80% can be maintained while increasing SNTI depth to 50% of VTG depth. C_{TG} depending on the gate surface decreases significantly as shown by equation (5.8) [36] and equation (1.27). In equation (5.8) the term C_{ox} is the gate oxide capacitance, S_{ox} is the total oxide surface covered by the doped polysilicon, T_{ox} is the oxide thickness, ϵ_0 the permittivity in free space and ϵ_{ox} the relative permitivitty of the oxide. The best trade-off is identified around 45% SNTI depth for the studied shallow N+ implant and TVG depth. By implanting sensing nodes deeper a better transfer can be attained.

$$FoM = \frac{DMC(\%)}{Power(\frac{\mu W}{gate})} \tag{5.7}$$

$$C_{ox} = \frac{S_{ox} \cdot \epsilon_0 \cdot \epsilon_{ox}}{T_{ox}} \tag{5.8}$$

Furthermore for the V4 variant presented in Fig. 5.33b, the presence of the SNTI can have an effect over the leakage between sensing nodes. In Fig. 5.38, the difference of potential allowed between the sensing nodes SN_1 and SN_2 is plotted versus the distance between the N+ implantation masks. A difference is observed between the case with and without SNTI. The effect is attributed to other elements that change the electrostatic potential distribution inside the pixel depending if the SNTI is present or not. For instance, two regimes are identified. Firstly, a case where the distance between the N+ implantation masks is lower and the leakage is mainly determined by the distance between the N+ SN implant design. Secondly, a case were the distance between the sensing nodes is much higher. For that case, the *P-Well* is predominant for the distribution of the electrostatic potential reparation. Contrarily, if there is no SNTI, the potential fixed by the gate on the top of the pixel causes sensing nodes to leak sooner.



(a) (b) (c)

Figure 5.36: Schematic representation of N+ implantation depth and SNTI depth impact on charge transfer. Shallow N+ implantation with (b) shallow SNTI and (c) deeper SNTI.

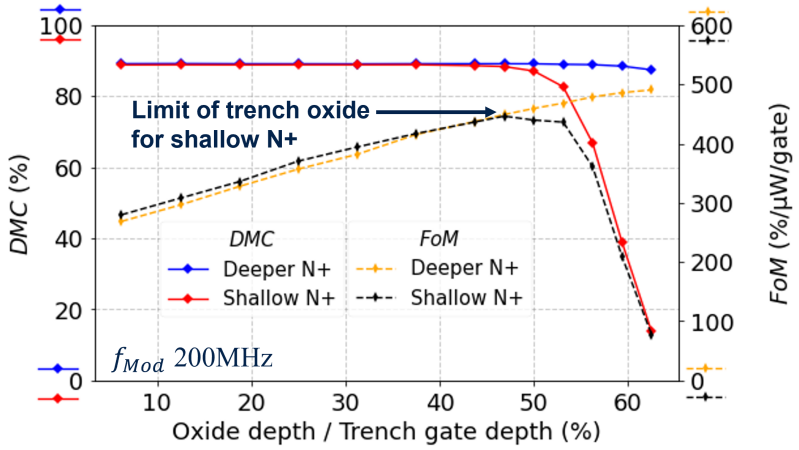


Figure 5.37: DMC and FoM at 200MHz versus SNTI depth and TVG depth ratio.

It is possible to conclude that, because most of the surface of the pixel is covered by the P-Well implant, no significant difference in DMC is observed between the case with SNTI and the case without.

TVG depth & P-Well optimization

A TVG depth change impacts the distribution of the electrostatic potential in the volume of the pixel. This is shown in Fig. 5.39, where the DMC_{200MHz} is plotted versus the TVG depth. With the increase of the depth of the TVG the transfer efficiency increases. However, the consumption will also increase. To minimize the consumption and maximize the transfer efficiency, the critical TVG depth values are identified. These are the optimum depth values to obtain the best trade-off between transfer efficiency and consumption. Further more, for different $P\text{-}Well$ implantation

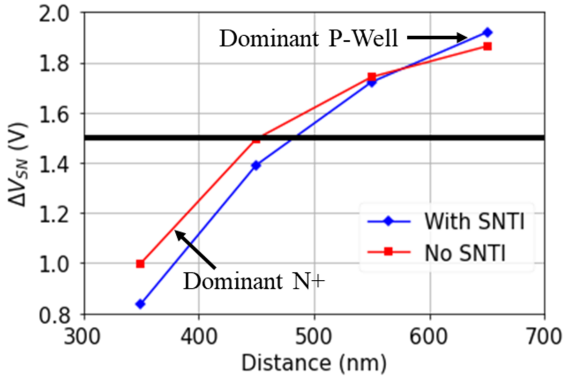
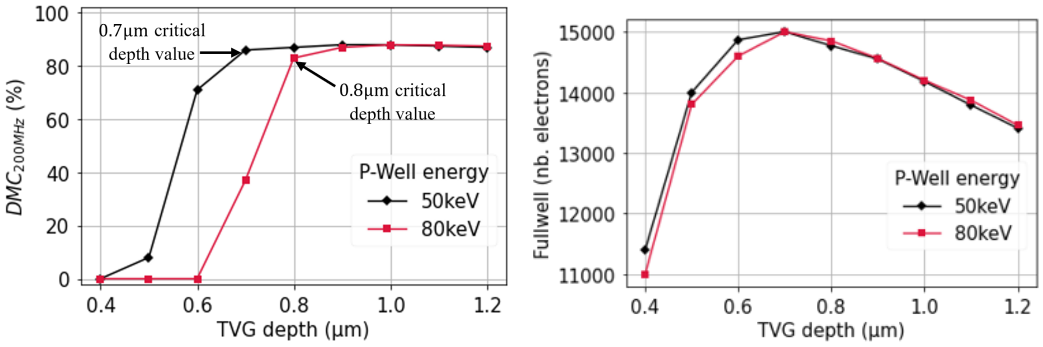


Figure 5.38: The maximum voltage excursion while maintaining a dark signal lower than an electron per second is computed for the sweep of N+ mask distance depicted in Fig. 5.33. A case with SNTI and the case without are compared and no significant difference is observed between the two alternatives.

energies, the critical TVG depth changes. A deeper *P-Well* box implant surrounding the TVGs require deeper MOS gates. This happens because, if the implants are done deeper than the TVG, they create a transfer barrier between the TVGs and the center of the FPG.

On the contrary, the fullwell capacity decreases from a certain value of TVG depth. This happens because the total pinned volume is reduced. The maximum of potential is situated lower in the volume of the FPG. As the N-type epitaxied zone has a gradual doping profile, the maximum depletion potential decreases if it is located lower inside the pixel epitaxy, further away from the TVGs.



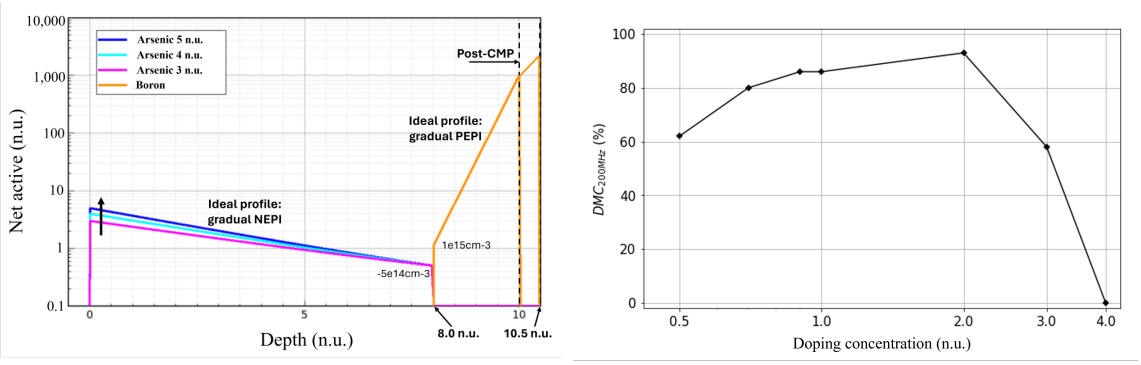
(a) (b)

Figure 5.39: (a) DMC_{200MHz} versus TVG depth with identified critical functioning depths for different *P-Well* implantation energies. (b) Fullwell at 2D operation versus TVG depth for different *P-Well* implantation energies. No significant difference is observed between the two different values of P-Well implantation energy.

Epitaxy doping optimization

Different gradual epitaxy N- and P-type doping profiles are used in simulation. Fig. 5.40a shows the net active of three variants integrated in silicon, plotted versus the depth of the epitaxy. The consequence of the change of the slope of the N-type doping profile by increasing the top doping value at $0\mu m$ depth to the transfer efficiency is depicted in Fig. 5.40b. The DMC_{200MHz} is plotted versus the top value of the N-type doping profile showing how the transfer is sensitive to a difference change of $1.0n.u.$ to the doping value.

The optimal value is identified at $2n.u.$ for the doping concentration, where the obtained maximum DMC is observed in Fig. 5.40b. To avoid the risk off process variability, that may decrease DMC with the doping concentration change, different doping splits will be investigated fabricated. They are presented in section 5.7.1.



(a) (b)

Figure 5.40: The simulation results of different complex gradual N and P-type doping epitaxy profiles are illustrated. (a) The net active is plotted versus the depth of the epitaxy. (b) DMC_{200MHz} is plotted versus the top value of the N-type doping profile showing how transfer is sensitive to a difference change of $10^{15}cm^{-3}$ to the doping value.

5.6 Comparison with prior state-of-the-Art

3D simulation of planar gate solution have been carried out with same pixel thickness and pitch than TVG proposed solution. Fig. 5.41 presents the evolution of DMC at 200MHz and 300MHz between both solutions in simulation with same sensing zone depth. For the FPG pixel, the difference of potential could be as low as 0.8V, while maintaining better than state-of-the-art DMC performances over 88%. When compared to planar gate solution, the TVG iToF pixel shows significantly higher performances in term of DMC.

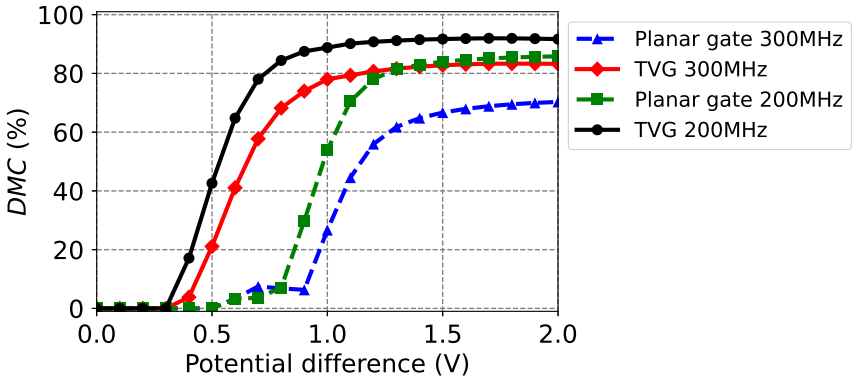


Figure 5.41: Trench against planar gate iToF pixels best case, DMC at 200MHz and 300MHz function of difference of potential, ΔV between TGs.

The FPG pixel has performant DMC values at 200MHz while operating at very low biasing. Indeed, to reduce TVG power consumption lower than planar TG consumption, TVGs drivers could operate with low reference voltage. Table 5.1 compares state-of-the-art solutions with simulated solution.

Table 5.1: Trench against planar gates iToF

iToF pixel	**TVGs**	**Planar gates**		
	This work	***Keel [17] (2021)***	***Tubert [18] (2021)***	***Ebiko [58] (2020)***
DMC @f_{Mod}	89% @200MHz	80% @200MHz	88.5% @200MHz	79% @200MHz
QE@940nm	40%	38%	18.5%	32%
Consumption p/ pixel eq. (5.7) @f_{Mod} @ΔV	$1.2\mu W$ (2-taps) @200MHz @1.0V	— @200MHz @1.05V	$1.4\mu W$ (2-taps) @200MHz @1.2V	— @200MHz @1.2V

In conclusion, the small pitch trench vertical gate iToF pixel is validated using 3D TCAD simulations. The fast photogate solution shows in general better performances

than state-of-the-art. Demodulation contrast (DMC) values of 89% are obtained at 200MHz and of 77% at 300MHz, while transfer gates operate at a 1.0V difference of potential. Such a low biasing operation allows a lower consumption per pixel than planar gates. Moreover, 3D optical FDTD simulations give a high quantum efficiency (QE) of 40%. Fig. 5.42 shows transmission electron microscopy (TEM) cuts of the trench vertical gates in promising fast photogate pixel design on-going fabrication.

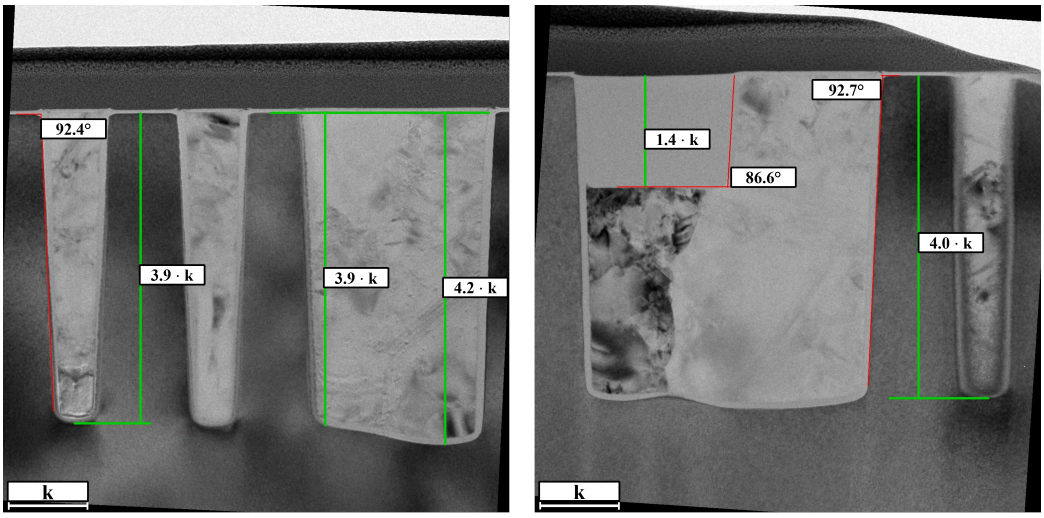


Figure 5.42: TEM cut images of fabricated TVG in a designed reference FPG pixel. The targeted depth of TVGs is indicated by k. TVG and trench oxide etching profiles are slightly flared to avoid the creation of filling voids during the fabrication process.

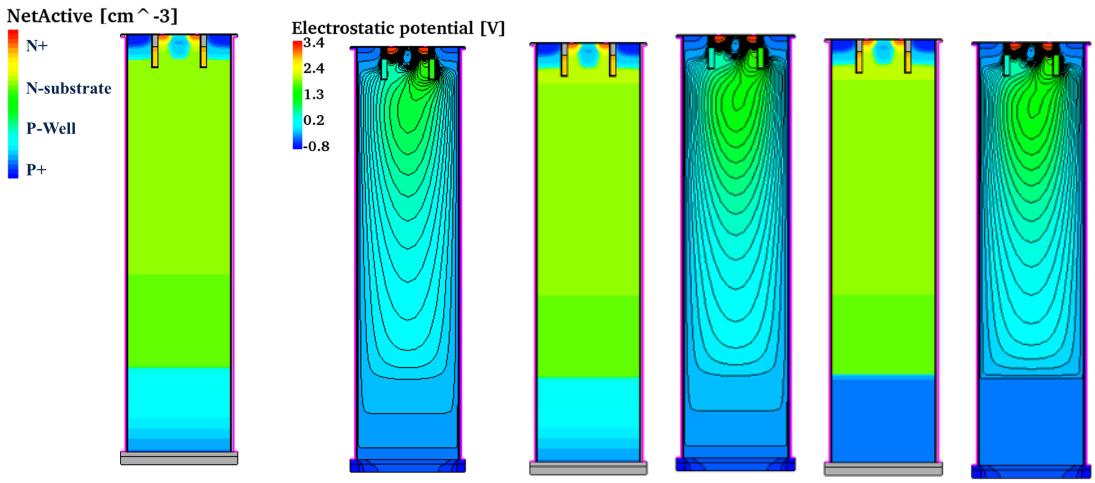
5.7 Fabrication & process validation

From the previous different simulation studies, the main elements impacting pixel performance have been identified. The key parameters to be challenged and optimized are (i) TVG morphology, i.e. (i.a) TVG etching depth, (i.b) SNTI etching depth and; (ii) doping values of the (ii.a) epitaxy, (ii.b) TVG polysilicon (ii.c) of the *P-Well* box implant and (ii.d) energy values of P-Well and N+ sensing node implants.

In this section, the approach to the fabrication of test structures will be discussed. It must be mentioned that the fabrication did not reach the final step. That impedes the complete analysis of performances of the devices using TVG. However the morphological validation of TVG has been achieved.

5.7.1 Epitaxy doping

Different epitaxy profiles have been attempted in simulation to optimize the N- and P-type gradual dopings. Fig. 5.43 shows two things. Firstly, it shows that for the given pixel pitch, the depletion potential at the center of the pixel V_{pixel} is very sensitive to small changes in the doping value of the N-type profile. Sencondly, when the pixel is fully depleted the potential V_{pixel} depends only on the doping of the N-type epitaxy part.



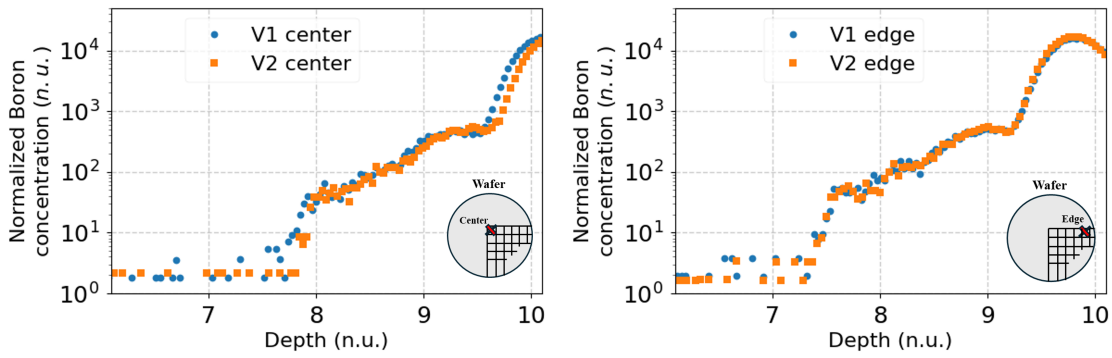
(a) $1 \cdot N_D$ (b) (c) $1.2 \cdot N_D$ (d) (e) $1.2 \cdot N_D$ (f)

Figure 5.43: Simulation of the epitaxy with different gradual N- and P-type doping values. (a) A gradual N- and P-type epitaxy is attempted with a maximum value of donor doping N_D with (b) the corresponding electric potential distribution. (c) The maximum doping value is increased by 1.2 times, hence giving a steeper gradual profile and (b) the corresponding electric potential distribution. Finally, (e) the P-type gradual potential is replaced by a flat P-type doping profile and the N_D value is maintained, (f) the corresponding electric potential distribution is obtained.

As the pixel operation is sensitive to the epitaxy doping values, it is important to

have a strong control of this parameter during the fabrication. Indeed, the realization of a commercial device relies on the capability of reproducing the epitaxy profile with a change of the doping value much inferior than 20% and with a strong uniformity. That is, the same epitaxy doping values for devices at the center and the edge of a 300mm wafer.

In the order of the flow, the P-type doping profile is epitaxied over a light P-type doping substrate. Fig. 5.44 shows the secondary ion mass spectroscopy (SIMS) results of the fabricated test samples with normalized doping values. The epitaxied layer doping results at the center of the pixel (Fig. 5.44a) is compared with a zone at the edge of the wafer (Fig. 5.44b). The P-type epitaxy is done in a chamber filled with Borine and the N-type gradual epitaxy is done in a chamber filled with Arsine, both at temperatures of up to $1200°C$. Because of the high temperature epitaxial process, the epitaxy doping profile is considered significantly stable. Hence, the epitaxy doping profile is expected not to change during the other successive annealing in the remaining fabrication process. However, that may not be the case with boron P-type species and the profile is selected to compensate for possible further deformations to the doping gradient. A stronger gradient is selected for the boron doping concentration slope at the bottom of the device, as shown in Fig. 5.44a, close to 10 $n.u.$. This higher doping gradient may fix the direction of the gradient of diffusion and may avoid the creation of potential barrier due to doping gaps.



(a) (b)

Figure 5.44: Epitaxy SIMS results of the boron gradual doping concentration profile at (a) the center and (b) the edge of the 300mm wafer.

As doping values are much lower, the process requires a more precise control of the gas flow inside the chamber. The SIMS results are presented in Fig. 5.45 with SIMS normalized measured doping values. A significant difference is observed between the values of the border and the center of the wafer. This profile would not be considered reliable for a commercial application.

5.7.2 TVG & SNTI morphology

Different TVG depth have been targeted aiming to improve the trade-off between the transfer efficiency and the consumption. The flow of the TVG has been shown

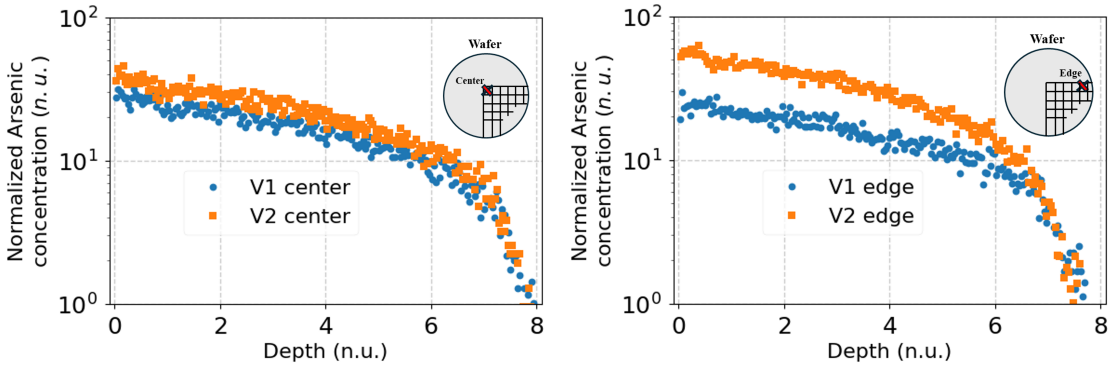
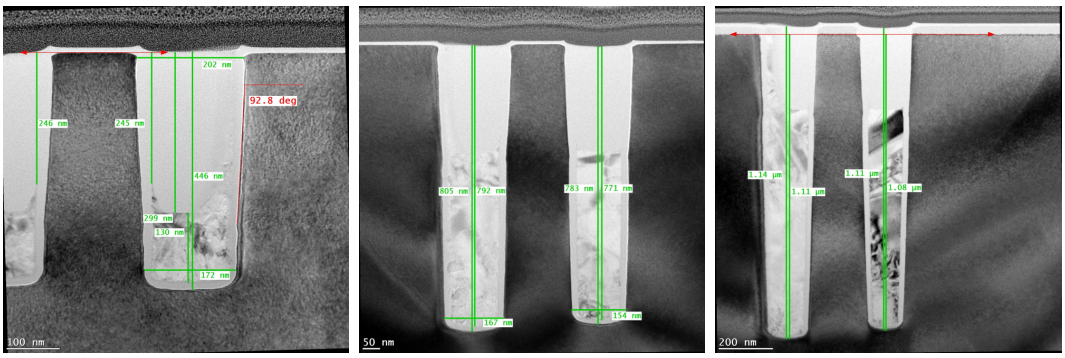


Figure 5.45: Epitaxy SIMS results of the arsenic gradual doping concentration profile at (a) the center and (b) the edge of the 300mm wafer.

previously in section 5.3. The actual depth of the trench depends on the tool parameters but also on the design. Indeed, the first validation in the process of the trench gate etching is the lithophotography step. To identify the suitable conditions responding to the critical dimensions (CD), a sweep of the photolithography conditions in terms of dose and focus has been done with the focus exposure matrix (FEM) technique.

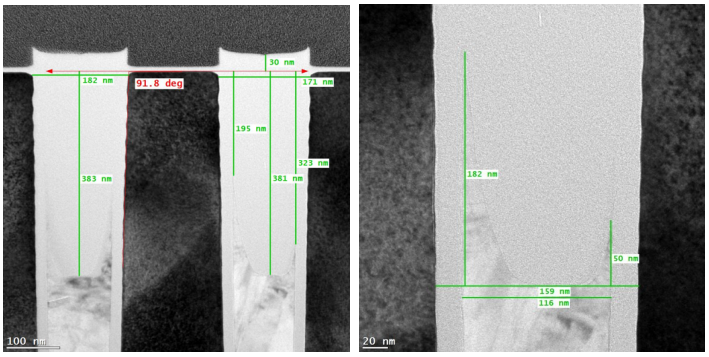
A TEM cut is required for the validation of the TVG morphology and depth. However, to reduce the fabrication time, the TEM cuts were done only later on during the fabrication flow and they are shown in Fig. 5.46. Initially the targeted depths were $400nm$, $800nm$ and $1200nm$. By adjusting the RIE etching process, the average depth values obtained are $450nm$, $790nm$ and $1100nm$. The polysilicon filling step shows no voids and the SNTI is correctly etched down to an effective depth of $250nm$. The strong anisotropic behavior of the SNTI process causes the effective depth of SNTI ($245nm$ in Fig. 5.46a) to be much lower than the maximum depth ($290nm$ in Fig. 5.46a). The remaining unetched polysilicon around the SNTI etched trench is called a polysilicon fence.

An attempt was made at a process variation to increase the SNTI depth. The TEM cuts of the targetted $400nm$ SNTI are shown in Fig. 5.47. In the preliminary depicted morphological analysis, the trial was not successful because of the increasingly higher polysilicon fences. Indeed the effective SNTI depth is significantly close to the reference SNTI process depicted in Fig. 5.46. Electrical confirmation is required, but the deeper SNTI process variation may give the same capacitance values as the reference process.



(a) (b) (c)

Figure 5.46: TEM cuts of the TVG process fabrication with different targeted depths of (a) 400nm, (b) 800nm and (c) 1200 nm. Respectively, the average depth values obtained are 450nm, 790nm and 1100nm.



(a) (b)

Figure 5.47: TEM cuts of the SNTI process fabrication a targeted depth of (a) 400nm overview and (b) with a zoom on fences.

5.8 Perspectives

The fabrication of the designed devices is on-going. The fabricated devices are required for the validation of the promising results obtained in simulation. Additionally, the comparison of simulation and measurements is required for the validation of the simulation methodology never used in a TVG iToF pixel. The calibration of simulation parameters may be required to obtain a predictive simulation methodology.

Different test structures were designed for the validation of the major process steps such as the TVG functionality.

Additionally the TVG iToF pixels were integrated to complete sensors inside of a test chip that may pursue the fabrication completely, i.e. up to the fabrication of the microlenses at the end of the fabrication flow of a sensors.

This is the first fabrication loop that was carried out for TVG iToF inside of STMicroelectronics. Because of that, a second fabrication iteration may be required to understand the major issues that may be found with the technology, to validate major choices and apply other improvements

Finally, a complementary simulation study of PRNU and DNU computed for a TVG iToF pixel using MC is intended. The reduction of the variations related to the mismatch between pixels is expected as no photodiode implants are used.

Conclusion

The novel solution for iToF pixel technology, the fast photogate (FPG), using trench vertical gates (TVGs) effectively addresses the critical limitations of planar gates.

TVGs, which are buried MOS structures created by filling a trench with liner oxide and polysilicon, show great performance when integrated with silicon pixels for visible light detection. The state-of-the-art pixel for visible light detection, the photogate (PG), integrates TVGs as transfer gates due to their pinning capability.

The morphology of TVGs is constrained by the fabrication process. The etching of a trench is done with reactive ion etching (RIE). Sensing node trench insulation (SNTI) is created by etching trenches inside of the polysilicon close to high dose implants.

Simulations were used for the understanding of the existing PG pixels used in 2D imaging. By adjusting simulated curves to match measured values, relevant trends are extracted and a simulation set-up is built for the simulation of other innovative pixels. For instance, a reasonable match of depletion capacitance is obtained between the simulation and the measured results.

The proposed small pitch FPG iToF pixel using TVG, operating with 940nm wavelength light detection, shows increased efficiency in charge transfer. This innovative approach enhances quantum efficiency (QE) while maintaining high demodulation contrast (DMC) at low biasing conditions, introduces robust electrostatic potential control and ensures consistent charge collection efficiency, thereby reducing parasitic light sensitivity (PLS).

Key advancements include:

- **QE vs. DMC Trade-off:** The new FPG design has enhanced QE for the detection of 940nm light wavelength, while maintaining a significantly high DMC, even at low biasing conditions.

- **Low barrier limitation:** The solution introduces a more robust control over the electrostatic potential, creating a higher potential barrier during charge transfer. This advancement ensures efficient and precise transfer of photogenerated charges, significantly facilitating parasitic light signal (PLS) reduction.

- **Variability of Deep Implantation:** By avoiding deep diode implantation, the design achieves a more uniform electric field distribution and consistent charge collection efficiency across the pixel array. This could reduce depth non-uniformity (DNU) and pixel-response non-uniformity (PRNU).

Simulations show that an efficient charge transfer is achieved and the use of TVGs provides a good trade-off between QE and DMC. Parasitic light signal (PLS) measured in SN_2 is close to 0%. Optical simulation carried out with a commercial finite-difference time-domain (FDTD) solver shows a high QE of 40%.

The designed iToF pixel could also acquire a performant 2D image, with two identified operation modes optimized for both. The total measurable charges for this operation, known as the fullwell capacity, is estimated over 16,000 electrons and increases as the barrier height increases.

SNTI depth is identified as a crucial process parameter for improving the pixel. Deeper SNTI is proposed to reduce TVG oxide capacitor C_{TG}, but shallow N+ sensing nodes can present transfer issues. An optimum depth of SNTI is identified by the maximum of the figure of merit (FoM), maintaining DMC at 200MHz over 80% while increasing SNTI depth to 50% of VTG depth.

Different TVG depths impact the distribution of the electrostatic potential in the pixel volume. The critical TVG depth values are identified to minimize consumption and maximize transfer efficiency. The fullwell capacity decreases from a certain value of TVG depth due to the reduction of the total pinned volume.

Different gradual epitaxy N- and P-type doping profiles are used in simulation, showing that the transfer is sensitive to changes in the doping value. The realization of a commercial device relies on the capability of reproducing the epitaxy profile with minimal changes in doping value.

The fabrication of the designed devices is currently ongoing. These fabricated devices are essential for validating the promising simulation results obtained and for comparing simulation and measurement data to validate the novel simulation methodology used for TVG iToF pixels. Calibration of simulation parameters may be necessary to achieve a predictive simulation methodology. Various test structures were designed to validate major process steps, including TVG functionality. Additionally, the TVG iToF pixels were integrated into complete sensors within a test chip, potentially including the fabrication of microlenses at the end of the process. This marks the first fabrication loop for TVG iToF within STMicroelectronics and a second iteration may be needed to address any issues, validate key choices and implement improvements. A complementary simulation study of PRNU and DNU using Monte Carlo (MC) methods is also planned, with the expectation of reduced variations due to the absence of photodiode implants.

References

[16] Yuichi Kato. "320x240 Back-Illuminated 10-um CAPD Pixels for High-Speed Modulation Time-of-Flight CMOS Image Sensor". In: *IEEE Journal of Solid-State Circuits* 53.4 (2018), pp. 1071–1078. DOI: 10.1109/JSSC.2018.2789403.

[17] Min-Sun Keel. "A 4-tap 3.5um 1.2Mpixel indirect time-of-flight CMOS image sensor with peak current mitigation and multi-user interference cancellation". In: *IEEE International Solid-State Circuits Conference, ISSCC* (2021), pp. 106–108. DOI: 10.1109/ISSCC42613.2021.9365854.

[18] Cedric Tubert. "4.6um Low Power Indirect Time-of-Flight Pixel Achieving 88.5% Demodulation Contrast at 200MHz for 0.54MPix Depth Camera". In: *ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference, Proceedings* (2021), pp. 135–138. DOI: 10.1109/ESSCIRC53450.2021.9567878.

[27] Ward Van Der Tempel. "A 1k-pixel 3D CMOS sensor". In: *Proceedings of IEEE Sensors* (2008), pp. 1000–1003. DOI: 10.1109/ICSENS.2008.4716611.

[37] SDevice. *Sentaurus Device User Guide*. Version S-2021.06. 2021.

[42] Danil Van Nieuwenhove. "Photonic Demodulator With Sensitivity Control". In: *IEEE Sensors Journal* 7.3 (2007), pp. 317–318. DOI: 10.1109/JSEN.2006.890164.

[43] Cristine Jin Estrada. "Physical Model of Current-Assisted Photonic Demodulator (CAPD) for Time-of-Flight CMOS Image Sensor". In: *IEEE Transactions on Electron Devices* 67.7 (2020), pp. 2825–2830. DOI: 10.1109/TED.2020.2995349.

[44] N Na, S-L Cheng, H-D Liu, M-J Yang, C-Y Chen, K-C Chu, H-W Chen, Y-T Chou, C-T Lin, W-H Liu, et al. "Proposal and demonstration of germanium-on-silicon lock-in pixels for indirect time-of-flight based three-dimensional sensing". In: *arXiv preprint arXiv:1806.07972* (2018).

[45] Edge AI Vision. *Why the Sony IMX570 is the Leading iTOF Sensor*. 2023. URL: https://www.edge-ai-vision.com/2023/04/why-the-sony-imx570-is-the-leading-itof-sensor/ (visited on 04/15/2023).

[53] C.-L. Chen. "5.3 An Up-to-1400nm 500MHz Demodulated Time-of-Flight Image Sensor on a Ge-on-Si Platform". In: *2020 IEEE International Solid-State Circuits Conference - (ISSCC)*. 2020, pp. 98–100. DOI: 10.1109/ISSCC19947.2020.9063107.

[58] Yoshiki Ebiko. "Low power consumption and high resolution 1280X960 Gate Assisted Photonic Demodulator pixel for indirect Time of flight". In: *International Electron Devices Meeting, IEDM* (2020). DOI: 10.1109/IEDM13553.2020.9372109.

[71] Lumerical. *Inc., FDTD: 3D Electromagnetic Simulator*. Version version 2022-r6. 2022.

[87] Jonathan S Steckel. "High resolution quantum dot global shutter imagers". In: *SID Symposium Digest of Technical Papers*. Vol. 52. 1. Wiley Online Library. 2021, pp. 975–977.

[88] Jiwon Lee. "Imaging in short-wave infrared with 1.82 µm pixel pitch quantum dot image sensor". In: *2020 IEEE International Electron Devices Meeting (IEDM)*. IEEE. 2020, pp. 16–5.

[89] S. Manda. "High-definition Visible-SWIR InGaAs Image Sensor using Cu-Cu Bonding of III-V to Silicon Wafer". In: *2019 IEEE International Electron Devices Meeting (IEDM)*. 2019, pp. 16.7.1–16.7.4. DOI: 10.1109/IEDM19573.2019.8993432.

[90] R. Fraenkel. "Development of low-SWaP and low-noise InGaAs detectors". In: *Infrared Technology and Applications XLIII*. Ed. by Bjørn F. Andresen, Gabor F. Fulop, Charles M. Hanson, John Lester Miller, and Paul R. Norton. Vol. 10177. International Society for Optics and Photonics. SPIE, 2017, p. 1017703. DOI: 10.1117/12.2262112.

[91] Quentin Durlin. "Fabrication and characterisation of the PiN Ge photodiode with poly-crystalline Si: P as n-type region". In: *Opto-Electronics Review* 31.Special Issue (2023).

[92] Caitlin Rouse. "Development of low dark current SiGe near-infrared PIN photodetectors on 300 mm silicon wafers". In: *Optics and Photonics Journal* 6.05 (2016), p. 61.

[93] Jurgen Michel, Jifeng Liu, and Lionel C Kimerling. "High-performance Ge-on-Si photodetectors". In: *Nature photonics* 4.8 (2010), pp. 527–534.

[94] Daniel Van Nieuwenhove, Ward Van Der Tempel, and Maarten Kuijk. "Novel Standard CMOS Detector using Majority Current for guiding Photo-Generated Electrons towards Detecting Junctions". In: *2005 IEEE/LEOS Symposium Benelux Chapter*. Annual IEEE/LEOS Symposium Benelux Chapter. Annual IEEE/LEOS Symposium Benelux Chapter, 2005.

[95] L. Pancheri. "Current assisted photonic mixing devices fabricated on high resistivity silicon". In: *SENSORS, 2008 IEEE*. 2008, pp. 981–983. DOI: 10.1109/ICSENS.2008.4716606.

[96] Gian-Franco Dalla Betta. "Design and Characterization of Current-Assisted Photonic Demodulators in 0.18- µm CMOS Technology". In: *IEEE Transactions on Electron Devices* 58.6 (2011), pp. 1702–1709. DOI: 10.1109/TED.2011.2126578.

[97] Quazi Delwar Hossain, Gian-Franco Dalla Betta, Lucio Pancheri, and David Stoppa. "Current assisted photonic mixing demodulator implemented in 0.18µm standard CMOS technology". In: *2009 Ph.D. Research in Microelectronics and Electronics*. 2009, pp. 212–215. DOI: 10.1109/RME.2009.5201367.

[98] Chong Li, Chunlai Xue, Zhi Liu, Buwen Cheng, Chuanbo Li, and Qiming Wang. "High-Bandwidth and High-Responsivity Top-Illuminated Germanium Photodiodes for Optical Interconnection". In: *IEEE Transactions on Electron Devices* 60.3 (2013), pp. 1183–1187. DOI: 10.1109/TED.2013.2241066.

General conclusion

Abstract

Beyond the conventional 2D sensors used for photography, 3D sensors have been developed to provide depth information. They measure the distance between the camera and a point in the scene for each pixel. The popularity of 3D imaging is growing, and it has vast potential applications. For example, the automotive industry is interested in using it to improve safety. Additionally, these sensors can be used for facial recognition to secure payments or offer new unlocking methods for smartphones or computers.

This doctoral work contributes to the development of CMOS digital image sensors at STMicroelectronics with the goal of producing innovative sensors for consumer applications. Within the STMicroelectronics R&D team dedicated to optical sensor technologies, the focus is on developing a new pixel for 3D image acquisition that combines the existing company expertise with new technological advances. This thesis concentrates on the design and optimization of indirect time-of-flight (iToF) image sensors, which are widely used for distance measurement. The overall objective is to design and optimize innovative iToF solutions, covering modeling, simulation, design, and fabrication. The thesis is divided into five chapters.

Chapter 1 provides an overview of optical distance measurement techniques, explaining the principles of time-of-flight (ToF) and the specific case of iToF methods with intensity-modulated waves. It also describes different types of optical sensors, including 2D and 3D sensors.

Chapter 2 describes the simulation methodology used for the design and optimization of iToF pixels, notably the TCAD (Technology Computer-Aided Design) tools for pixel architecture analysis. The key simulated figures of merit include power consumption, demodulation contrast (DMC), parasitic light sensitivity (PLS) and quantum efficiency (QE). Predictive DMC and PLS values can be computed from the obtained pixel current response. Chapter 3 complements this approach with a Monte Carlo methodology, enabling the extraction of statistical quantities and improves the understanding of noise figures in iToF pixels, such as pixel response non-uniformity (PRNU) and depth non-uniformity (DNU).

Chapters 4 and 5 describe the development of new pixels using the methodologies presented in previous chapters. Chapter 4 addresses CMOS architectures compatible with “fast integration” for iToF, focusing on CAPD (current assisted photonic demodulator) pixels, analyzing their advantages and limitations. Two avenues were

explored: (i) silicon CAPD, (ii) germanium CAPD. (i) A pitch limitation was identified for the silicon CAPD pixel. This limitation is due to the increased leakage between sensing nodes as the pitch decreases. (ii) Germanium CAPD, interesting for SWIR applications [44], was simulated and fabricated in partnership with CEA LETI on a germanium-on-silicon platform. The main drawback of this solution is the high dark signal resulting from the narrow bandgap of germanium.

Chapter 5 focuses on "sophisticated integration" architectures, including stacked pixels and deep trench isolation, as well as other developments for high-performance devices. It also covers the optimization of technological and geometrical parameters. A new iToF pixel technology is proposed. This, the fast photogate (FPG) using vertical gates (TVG), overcomes the limitations of planar gates. Simulations show an improved QE/DMC trade-off, with high QE (40%) at 940nm, DMC above 80% at 200MHz, and near-zero parasitic light sensitivity. The simulated DMC values obtained with this new pixel exceed state-of-the-art specifications. Higher DMC values are achieved at reduced bias voltages for the FPG. The low bias voltages used, necessary for photogenerated charge transfer, result in lower pixel power consumption.

The following sections provide more detail on the main ideas presented in this abstract and present the obtained key results.

Distance measurement techniques

Distance measurement techniques are varied. One such technique is indirect time-of-flight (iToF). This measures the phase difference between an intensity-modulated emitted signal and the received signal, allowing precise distance measurement. This is achieved through different transfer gates (TG) that bring photogenerated charges to sensitive nodes (SN). The various TGs are operated alternately with a phase-shifted signal to sample the photogenerated signal. Equation 1 describes the computation of the phase value (ϕ) from the amount of charge collected on the different SNs (Q_{SN_1}, Q_{SN_2}, Q_{SN_3} & Q_{SN_4}), for a pixel with four SNs and four TGs.

$$\Delta\phi = arctan\left(\frac{Q_{SN_4} - Q_{SN_2}}{Q_{SN_3} - Q_{SN_1}}\right) \tag{1}$$

Three types of iToF pixels are identified: (i) the "current assisted photonic demodulator" (CAPD) [16], (ii) the "pinned photodiode" (PPD) [17, 18, 58], and (iii) a new approach using vertical gates ("dual VG") [30]. An overview of the performance for these different sensors is presented in Table 1. The performances of the different alternatives are compared through figures of merit.

1. Power consumption: This is closely related to current call for driving the TG at a certain frequency.

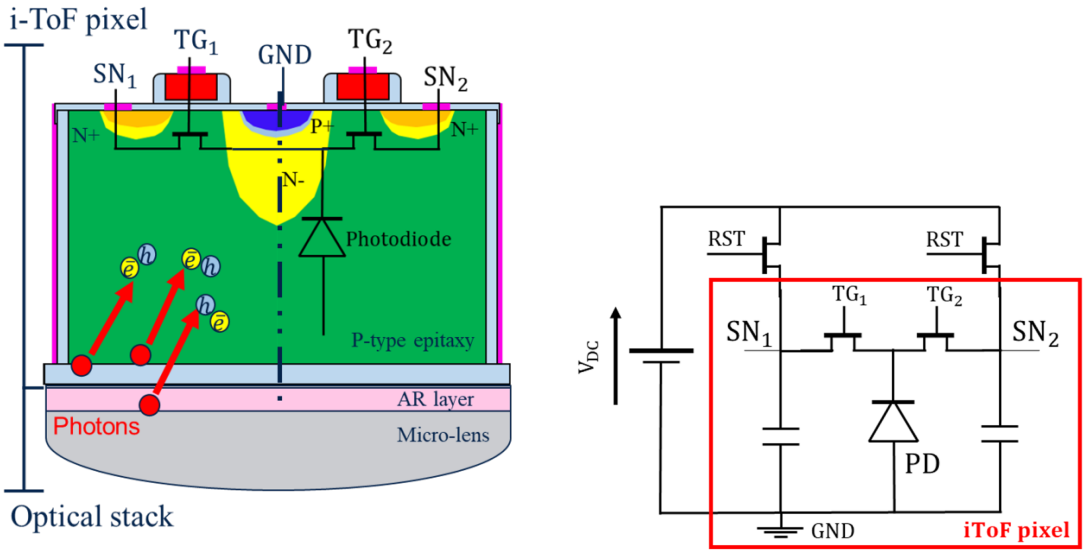
2. Demodulation contrast (DMC): It indicates the efficiency of photogenerated charge transfer and is correlated with the transit time of photogenerated charges and sensitivity to parasitic light (PLS).

3. Quantum efficiency (QE): It is computed from the ratio between the collected electrical signal in charge quantity and the number of incident photons.

A schematic example of a state-of-the-art PPD iToF pixel is illustrated in Fig. 4.

Table 1: State-of-the-art iToF performances.

	"Dual VG" iToF	**PPD iToF**		**CAPD**	
	Yorikado [30] (2023)	***Keel [17] (2021)***	***Tubert [18] (2021)***	***Chen [53] (2020)***	***Jang [63] (2021)***
Process	3D-stacked 90nm/65nm	3D-stacked 65nm/40nm	3D-stacked 65nm/65nm	Ge-on-Si	3D-stacked 90nm/65nm
Pixel pitch (μm)	3.0	3.5	4.6	10.0	5.0
Taps	2	4	2	2	2
Pixel array	640x480	1280x960	672x804	240x960	640x480
DMC @f_{Mod}	88% @200MHz	80% @200MHz	88.5% @200MHz	70% to 90% @500MHz	80% —
QE @$\lambda(nm)$	38% @940	38% @940	18.5% @940	46.3% @1310	—
Power consumption	—	290mW (sensor)	300mW (system)	200mW (sensor)	140mW (sensor)



(a) (b)

Figure 4: (a) Cross-sectional view of the structure of an iToF pixel with two transfer gates (TG_1 and TG_2), two sensing nodes (SN_1 and SN_2), a deep N-type implant for photodiode creation, deep trench isolation (DTI), and optical stacking. (b) The equivalent electronic circuit of the pixel for the given structure is highlighted by a red square.

Multiphysics simulation methodology

A comprehensive methodology combining TCAD simulations (process and electrical) with optical simulation by Lumerical FDTD was developed to compute key figures of merit for iToF pixels: power consumption, demodulation contrast (DMC), parasitic light sensitivity (PLS), and quantum efficiency (QE).

The simulation faithfully reproduces the measured results after calibration, notably for DMC. These results are presented in the summary of Chapter 3, where the Monte Carlo simulation methodology is performed and compared with the multiphysics TCAD & FDTD methodology. This methodology allows qualitative and quantitative evaluation of performance.

3D Monte Carlo simulation

Classical TCAD simulators based on drift-diffusion have limitations when it comes to considering detection variability. Examples of such information include statistical figures of merit such as pixel response non-uniformity (PRNU) and depth non-uniformity (DNU). To extract additional information based on statistical uncertainties, other approaches are considered. To accomplish this, a Monte Carlo method has been developed to simulate the transfer of photogenerated charges within a pixel to the readout nodes.

A comparison of the methodology developed in Chapter 2 with the Monte Carlo methodology is shown in Fig. 5. The 3D Monte Carlo simulation confirms the DMC trends that were observed with TCAD and measured experimentally. The slight shift is explained by the degraded mobility and the fact that the actual light pulse width was not modeled in the Monte Carlo approach.

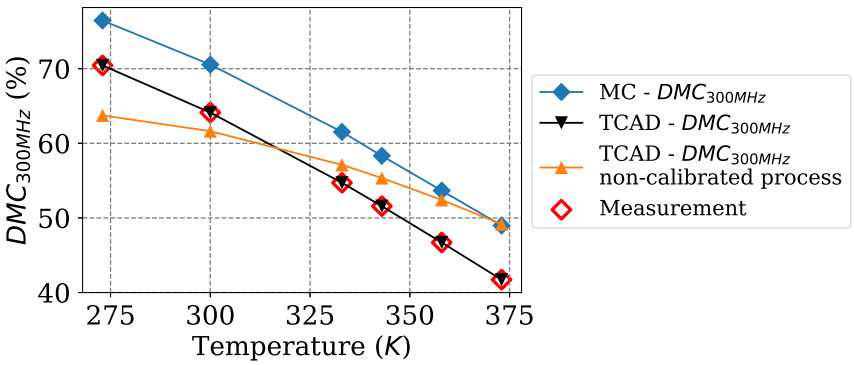


Figure 5: DMC at $300MHz$ as a function of temperature comparing MC and TCAD simulations with measured results.

This approach allows studying statistical variations related to pixel response non-uniformity (PRNU) and depth non-uniformity (DNU). To reduce these variations, it is necessary to increase QE and the total collected charge.

Additional measurements and new test benches are planned to deepen the understanding of PRNU and DNU contributions.

Studies on CAPD pixels

The limitations of the silicon CAPD were identified, and it was concluded that it is less accurate than its PPD iToF counterpart, for the targeted consumer applications. The studied device is designed to operate at 100 MHz [16, 45], whereas the PPD iToF can operate at frequencies up to 250 MHz [18]. The lower transfer efficiency of the CAPD when compared to its counterpart originates from the improved vertical electric potential gradient of the PPD iToF device. Technological solutions, such as charged deep trench isolation, are indispensable to overcoming the performance gap. Notably, the studied CAPD pixel lacks any isolation. Such a solution may also be vulnerable to electrical and optical crosstalk.

Two avenues were explored: (i) silicon CAPD, (ii) germanium CAPD.

(i) Silicon CAPD was studied by reverse engineering a commercial sensor [45]. A functional compatible solution was simulated, with possible improvements by reducing the substrate doping concentration to optimize the electric potential and reduce power consumption. However, this was limited by manufacturing constraints. A $3.5\mu m$ pitch limitation is identified for the CAPD pixel. This limitation is due to the increased leakage between sensing nodes as the pitch decreases.

(ii) Germanium CAPD, interesting for SWIR applications [44], was simulated and fabricated in partnership with CEA LETI on a germanium-on-silicon platform. The main drawback is the high dark signal due to the narrow bandgap of germanium. Pitch reduction seems less problematic than for silicon, but technological limitations remain significant.

New solution using trench vertical gates

A new iToF pixel technology is proposed. This, the fast photogate (FPG) using vertical gates (TVG), overcomes the limitations of planar gates. The pixel is schematically illustrated in Fig. 6.

TVGs are buried MOS structures formed by trench filling, offering an improved electrostatic control and enhanced charge transfer efficiency. Simulations show an improved QE/DMC trade-off, with high QE (40%) at 940nm, DMC above 80% at 200MHz, and near-zero parasitic light sensitivity. The DMC values obtained with this new pixel are compared with those of the previous planar gate pixel in Fig. 7. Higher DMC values are obtained at lower bias voltages for the FPG.

Table 2 summarizes and compares the figures of merit obtained with this new pixel relative to existing technologies. The low bias voltages used, necessary for photogenerated charge transfer, result in lower pixel power consumption. Additionally, the absence of a deep implant is expected to improve electric field uniformity, reducing DNU and PRNU. Future Monte Carlo simulation work is planned to study the

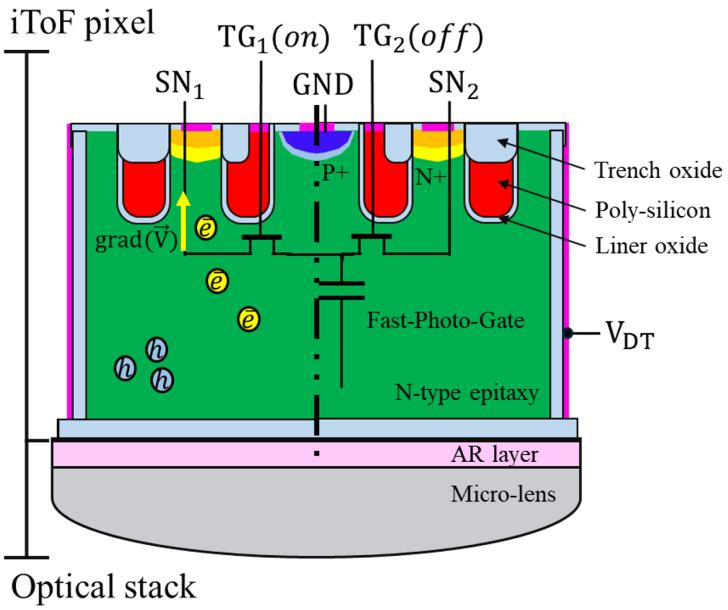


Figure 6: Cross-sectional schematic of the simulated FPG iToF pixel structure with trench gates, contacts, and deep pixel isolation (DTI) biased at V_{DT}.

reduction of PRNU and DNU variations

Table 2: iToF with trench gates versus planar gates

iToF pixel	**TVGs**	**Planar gates**		
	This work	***Keel [17] (2021)***	***Tubert [18] (2021)***	***Ebiko [58] (2020)***
DMC @f_{Mod}	89% @200MHz	80% @200MHz	88.5% @200MHz	79% @200MHz
QE@940nm	40%	38%	18.5%	32%
Power consumption per pixel @f_{Mod} @ΔV	1.2μW (2-taps) @200MHz @1.0V	— @200MHz @1.05V	1.4μW (2-taps) @200MHz @1.2V	— @200MHz @1.2V

Various fabrication parameters, such as SNTI and TVG depths and epitaxy profiles, have been optimized through simulation. The fabrication of devices is currently underway, with their incorporation into complete sensors.

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Perspectives

Experimental validation of the fabricated devices is crucial to confirm the promising simulation results and validate the innovative methodology developed for TVG

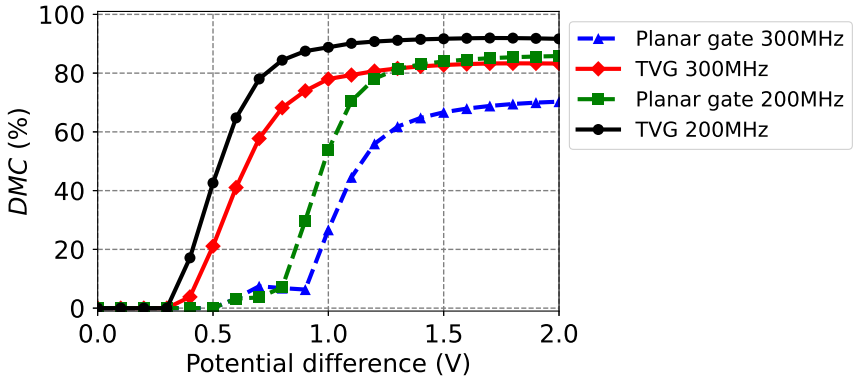


Figure 7: Comparison between trench gate and planar gate iToF pixels, best case, DMC at 200MHz and 300MHz as a function of the potential difference, ΔV, between the transfer gates (TG).

iToF pixels.

Test structures have been designed to validate major process steps, notably the functionality of the TVGs. The integration of TVG pixels into complete sensors marks the first TVG iToF fabrication loop at STMicroelectronics. A second iteration will likely be necessary to resolve potential issues, validate technological choices and implement improvements.

Finally, a complementary Monte Carlo simulation study is planned to further understand and reduce PRNU and DNU, with the hope of further improving the pixel performance.

Annex

6.1 Direct time-of-flight pixels

For the complex operation of measuring a distance that is the time-of-flight technique, elaborated semiconductor devices are integrated in silicon. It is the case both for direct time-of-flight (dToF) and indirect time-of-flight (iToF). For instance, dToF state-of-the-art devices integrate single photon avalanche diodes (SPAD).

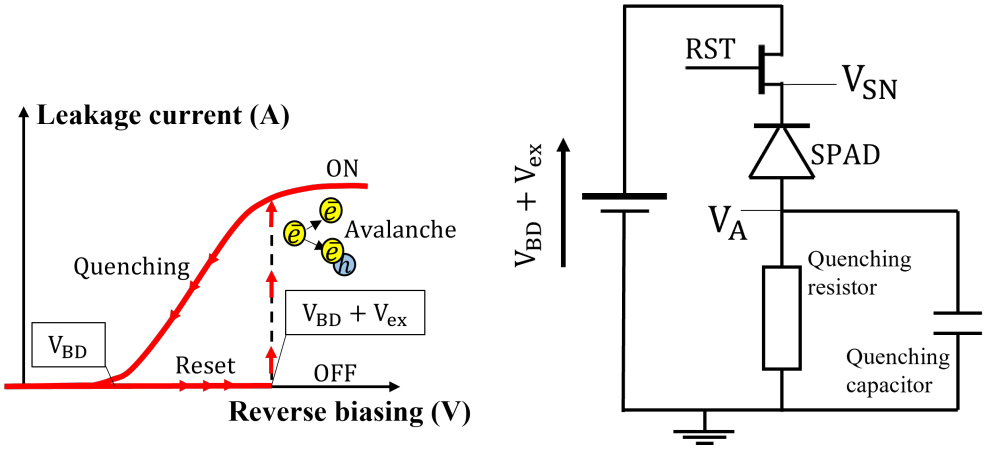
The SPAD pixels are sensitive to small light signal and have the fastest reaction time in between time-of-flight devices [13, 15, 25]. A SPAD is a photodiode that is reverse biased higher than breakdown voltage. Fig. 6.1a illustrates the activation of a SPAD pixel through an I(V) curve. In principle, SPAD devices are discrete, having binary ON and OFF states. In reset, while the quenching capacitor is discharged, the SPAD is reverse biased further than the breakdown voltage V_{BD} with the excess biasing V_{ex}. A photogenerated free carrier, in this case an electron, is accelerated and through impact ionization can trigger an avalanche. The exponential increase in current is seen by the resistor depicted in Fig. 6.1b and causes a change in the electric potential of the floating SPAD anode node V_A. When it is sufficiently high, the difference of potential between V_A and the sensing node electric potential V_{SN} decreases lower than V_{BD}. This causes the electric field inside the SPAD to decrease. With the reduced electric field, the remaining free electrons stop generating other free carriers through impact ionization. The remaining free electrons are evacuated and the avalanche is interrupted. This outrigger of the SPAD avalanche is called quench.

After quenching and for another acquisition, the SPAD is reset beyond breakdown. Fig 6.2 illustrates a $1D$ representation of a SPAD. When the difference of potential between the anode node A and the cathode represented by the sensing node SN is higher than the breakdown voltage, the corresponding band digagram is as represented in Fig 6.2(b). The photogenerated electrons ($\overline{e}$) and holes (h) in Fig 6.2(a)(b), are oriented according to the electrostatic potential gradient. Holes are evacuated in the anode and electrons are accelerated towards the cathode.

When an electron exits the transfer zone and enters the impact ionization zone with a high electrostatic field, it can trigger the ionization of another electron through impact ionization. This newly generated electron can then continue the same interaction and energize another electron, leading to a chain reaction called an avalanche effect.

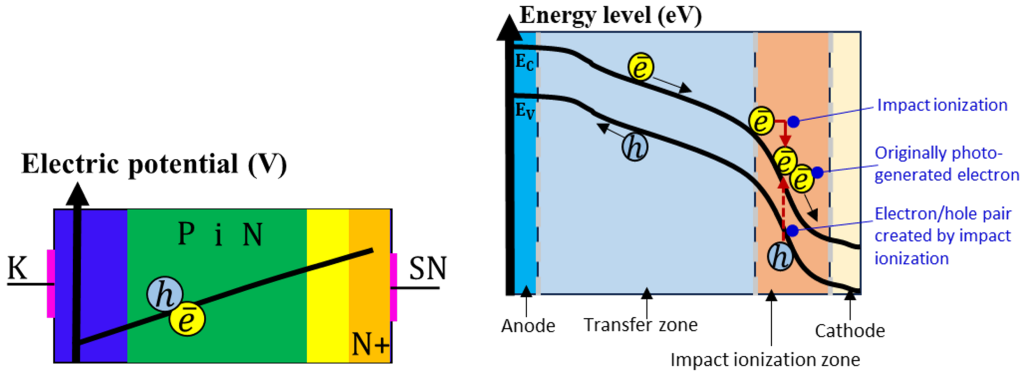
However, for this to occur, certain conditions must be met. Firstly, the electrostatic field must exceed the breakdown field, which is approximately 10^6V/cm.

Secondly, it is crucial that photogenerated carriers do not recombine with carriers present in the pixel volume, as this can result in signal loss. To prevent such recombination, the transfer zone is intrinsic or fully depleted [25]. Finally, the electrons must possess sufficient kinetic energy to trigger the impact ionization chain reaction.



(a) (b)

Figure 6.1: SPAD activation and reset (a) I(V) quenching diagram and (b) example of a passive quenching circuit.



(a) (b)

Figure 6.2: (a) Equivalent SPAD PiN junction and (b) band diagram with different zones representation. The impact ionization is represented, it is the mechanism responsible of the multiplication of photogenerated carriers.

6.2 Optimization study using MC

After the validation of MC simulations for iToF pixels, an optimization study has been carried out isolating two parameters: (i) the dose of photodiode deep implantation and (ii) the epitaxy doping profile. Two types of epitaxy profiles were attempted, both with different doping. In Fig. 6.4 at the left column in orange the attempted doping profiles are strictly exponentially increasing from top to bottom. The top doping value is $10^0 n.u.$ while the bottom value is given by the abscissa. Fig. 6.4b,d,f shows results obtained for a profile with a flat doping of $10^0 n.u.$ down to a depth of more than a micrometer where a doping gradient starts and finishes in the value represented in the abscissa.

Fig. 6.4a-b shows the lost signal for all simulated combinations of implantation dose and epitaxy doping. A line is drawn at 1% lost signal for functional choices. To study the device in DC, the PLS is plotted in Fig. 6.4c-d and to study the device in AC the transit time (TrT) is plotted in Fig. 6.4e-f. An increase in PLS is observed for sample implantation with an increase in gradient for the first column of epitaxy (Fig. 6.4c). This is due to the degraded electrostatic potential distribution inside the pixel between the sensing nodes and the implanted photodiode. The difficulty is to implant a N-type zone that can be appropriately driven by the transfer gates despite the epitaxy high doping gradient. The barrier in the opposite sensing node leaks into the faulty sensing node in that cycle. This issue is corrected by fabrication a zone with constant doping, deeper than a micrometer. Flat PLS curves are shown in Fig. 6.4d for those profiles.

The AC study with TrT shows how the increase in doping gradient favors a fast transfer. The best simulated case results are obtained for the strongest doping gradient and implantation dose.

This optimization could also be done with the drift-diffusion-based-TCAD simulator, as it only concern the transfer efficiency figures of merit. This section only serves as a demonstrator of the MC simulator.

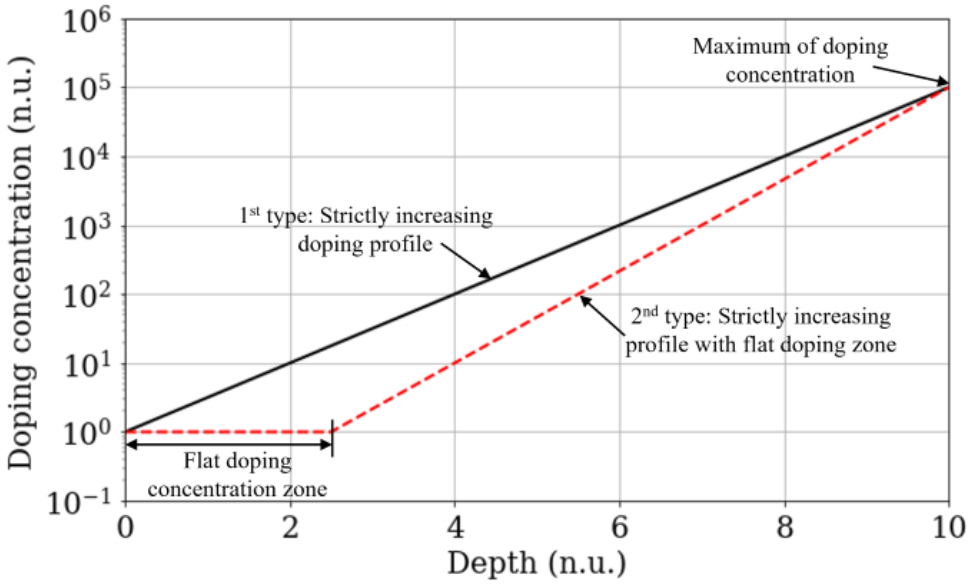


Figure 6.3: Two types of epitaxy doping profiles are simulated. The first type is a strictly increasing doping profile while the second type has a flat doping concentration at the top of the profile. The linear slope reaches a maximum value that is used as the abscissa in the following plots in Fig. 6.4. The profiles are imported in the direction of the z-axis, perpendicular to the (x,y) plan of the structure depicted in Fig. 3.3. Both the depth and the doping concentration are plotted in normalized unities (n.u.).

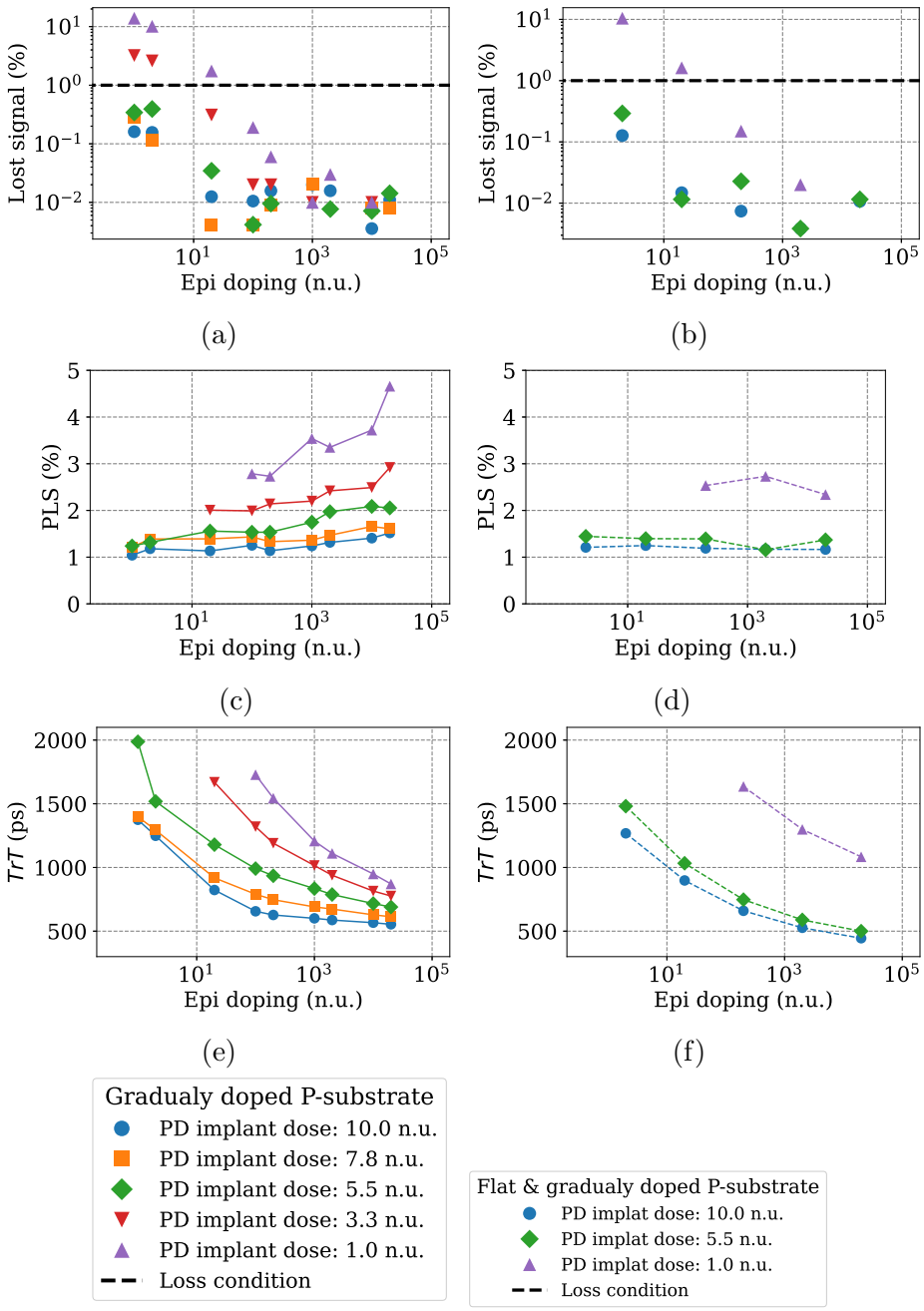


Figure 6.4: Doping optimization results using MC simulator for different PD implantation dose and epitaxy profile maximum doping values. Two types of epitaxy are studied. The strictly exponential doping profiles results are compared against the doping profiles with a light doping value plateau down to a micrometer depth. (a) The lost signal percentage for the first type and (b) for the second type of doping profiles is used as a metric to select functional process conditions and it is plotted versus the maxinum epitaxy doping value. For the cases satisfying lost signal conditions, (c, d) PLS percentage and (e, f) TrT are plotted versus the epitaxy maximum doping values for the respective epitaxy types.

6.3 Other materials for infrared detection

The use of longer than visible wavelengths for 3D imaging has three main motivations. (1.)First the ambient illumination drops at NIR wavelength due to the attenuation of these wavelength in the atmosphere, (2.)secondly these wavelengths suffer less from the scattering caused by fog and rain drops during extreme operation conditions [114]. (3.)Finally, the increase in wavelength reduces eye safety optical power requirement, down to the eye safe wavelength of $1400nm$ [115]. Recently, there has been a trend to shift the near-infrared (NIR) operation wavelength from $850nm$ to $940nm$ to take advantage of the solar spectrum dip at $940nm$. However, silicon features weaker absorption at longer NIR wavelengths, which degrades the quantum efficiency as the wavelength increases. Although a thicker silicon absorption layer can increase the quantum efficiency, it may also reduce the transfer efficiency and degrade the depth measurement accuracy. This trade-off makes it challenging to engineer a high-performing indirect time-of-flight pixel.

In the SWIR range between $1.0\mu m$ and $2.5\mu m$, silicon is quasi-transparent. This means that to detect a SWIR photon, silicon must be replaced by a more suitable material. Photodiodes of different materials have been proposed for NIR and SWIR sensing. The main candidates are PbS quantum dots in quantum films [87, 88], InGaAs [89, 90], and germanium on silicon (Ge-on-Si) [91–93].

In section 1.1 the structured light technique was introduced as an alternative to 3D imaging. This technique consists of using an elementary global shutter pixel to acquire a 2D image. From this 2D image and the information on the illumination a 3D image (i.e. a depth value per pixel) can be computed for each pixel [14]. Such a technique can be an alternative for the integration of the much more elementary pixels fabricated with these different materials.

The integration of these photodiode to a 3D device depends on three main factors. The pixel fabricated with these materials require (i) to be compatible with CMOS integration, to have (ii) a low response time and (iii) a low noise. A time-of-flight pixel has been demonstrated using InGaAs single photon avalanche diode [116]. Furthermore, recently an InGaAs image sensor with small pixel size has been developed by using Cu-Cu pixel level connections [89]. Despite these new developments, the fabrication of InGaAs image sensor remains expensive and pixels remain large for commercial applications. The solution is not suitable for high-resolution compact 3D camera systems.

Ge-on-Si and PbS quantum dots sensors are more adapted for a cost efficient and NIR and SWIR pixel. However, they suffer respectively from high leakage current at ambient temperature [91] and low free carrier mobility [117, 118].

Finally, among the CMOS compatible alternatives, two different types of pixels can be distinguished. The first one is a pixel with fast integration, as it has less fabrication steps, called the current assisted photonic demodulator (CAPD), i.e. the focus of this chapter. This solution has been demonstrated in silicon and germanium on silicon technology [16, 53]. In contrast, the second are pixels with sophisticated integration. These pixels integrate state-of-the-art fabrication techniques and consequently have

state-of-the-art performances. They will be the focus of the last chapter 4.

Ge-on-Si technology has been widely adopted for making optical receivers on Si photonics platform, especially for high-speed optical communication applications, making it a suitable candidate for high speed operations. Ge features a strong absorption at NIR wavelengths. A CAPD indirect time-of-flight pixel has been demonstrated with a high quantum efficiency from $850nm$ to $1400nm$ wavelengths [53] and $1550nm$ [44] operating at frequencies up to 500MHz. Moreover, Ge-on-Si technology is a CMOS compatible fabrication process, which can be incorporated with the existing front-side illumination (FSI) and back-side illumination (BSI) CMOS image sensor processes [44]. Despite these demonstrated first solutions using other materials than silicon, the state-of-the-art of indirect time-of-flight remains a silicon pixel solution. Indeed, its silicon counterpart is a much more suitable alternative for commercial applications as the germanium CAPD suffers from high leakage current value.

6.4 Germanium CAPD additional results

The germanium CAPD was fabricated in LETI.

6.4.1 CAPD Ge-P+ sole fabrication flow

The germanium epitaxial layer over silicon for the germanium CAPD fabrication is done in three steps ((i.), (ii.) and (iii.)) [91]. These three steps are illustrated in Fig. 6.5.

(i.) In the first step, a $50nm$ thick Ge seed layer is grown at $400°C$ and $100Torr$ using GeH_4.

(ii.) In the second step, two types of Ge-on-Si substrates are investigated for the fabrication of CAPDs:

(A.) For the first type of substrate, an intrinsic Ge layer with a thickness of $200nm$ is deposited at $400°C$ and $100Torr$.

(B.) For the second type of substrate, a high boron doping germanium (Ge-P+) passivation layer with a boron concentration of $4 \cdot 10^{19} cm^{-3}$ is deposited with a thickness of $200nm$ at $400°C$ and $100Torr$. The high boron doping germanium interface layer (Ge-P+) is intended to passivate the defects created by the dislocations.

(iii.) Finally, a $1.8\mu m$ thick Ge layer is grown using GeH_4 at $750°C$ and $20Torr$ on both types of substrates. A short duration thermal cycling under H_2 is used afterwards to reduce the threading dislocation density in the germanium down to values close to $10^7 cm^{-2}$ while keeping a smooth Ge surface [91].

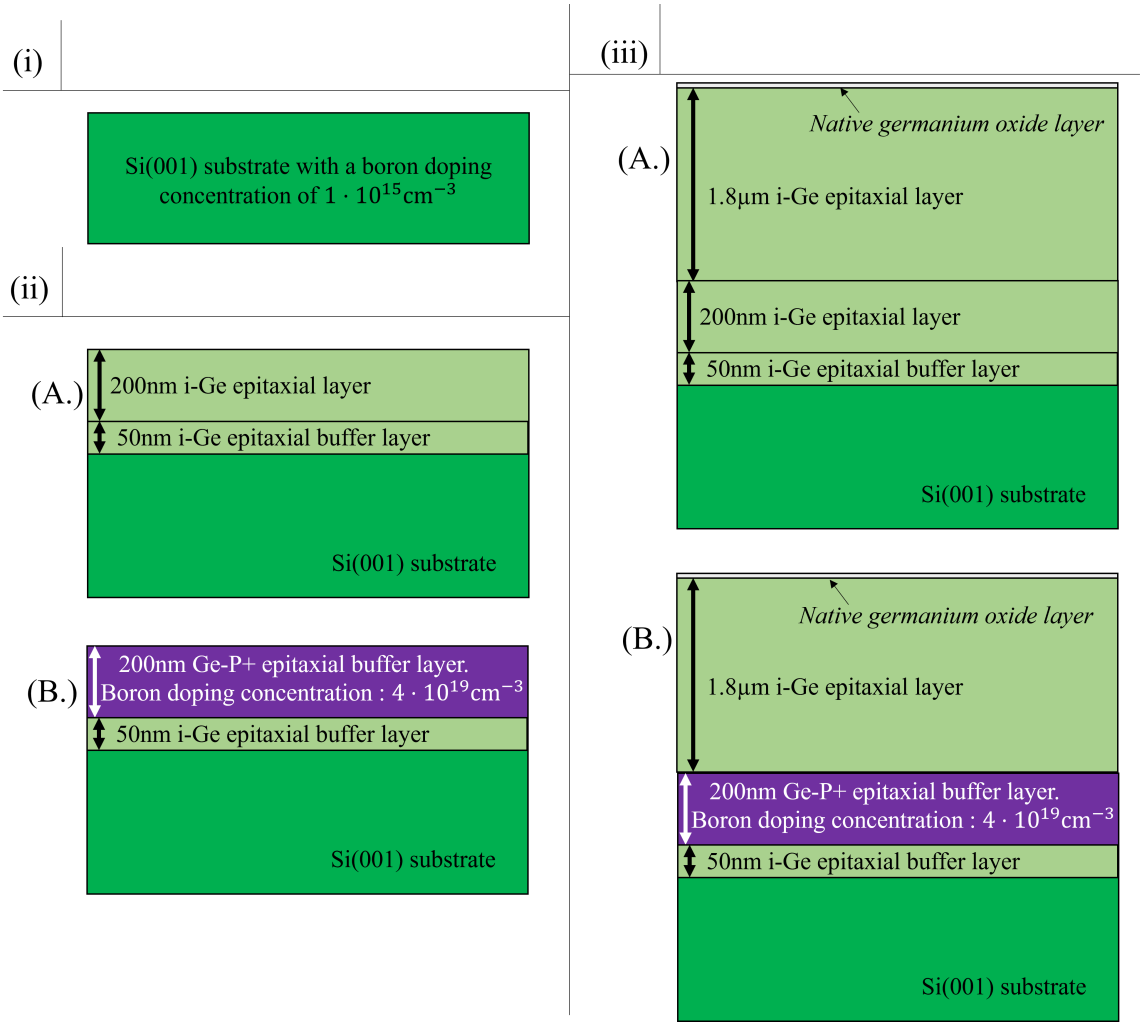
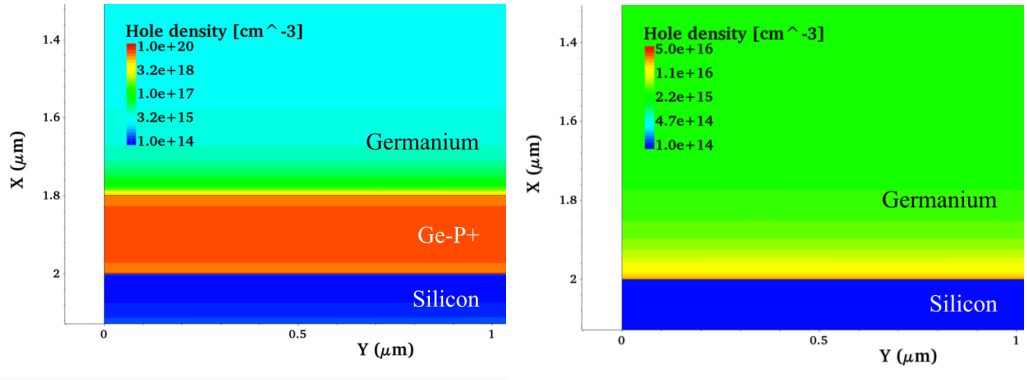


Figure 6.5: Ge-on-Si epitaxi process flow presented in three steps ((i.), (ii.) and (iii.)) with two process alternatives (A.) and (B.).

6.4.2 Sole accumulation of wholes

Fig. 6.6 shows the hole density compared between the case with highly doped germanium layer at the interface of both materials (Fig. 6.6a) and the case with $3 \cdot 10^{15} cm^{-3}$ P-type doped germanium directly epitaxied over the silicon bulk (Fig. 6.6b). During the operation the demodulators are biased at $0.7V$ and $0V$ respectively for D_1 and D_2, the sensing nodes are biased at $1.0V$ and the BULK is floating. The accumulation of holes at the order of $10^{16} cm^{-3}$ for the case without the highly doped germanium layer is not sufficient to passivate the interface defects and a three decade higher concentration of $4 \cdot 10^{19} cm^{-3}$ can be attained with the germanium doping using Boron.



(a) (b)

Figure 6.6: Hole density at the bottom of the 2D CAPD pixel simulation (a) with the Ge-P+ interface layer and (b) with the direct epitaxy of the lighly doped germanium layer. During the operation the demodulators are biased at $0.7V$ and $0V$ respectively for D_1 and D_2, the sensing nodes are biased at $1.0V$ and the bulk is floating

6.4.3 Different process alternatives table

In equation (6.1), this current value is multiplied by the simulation time (T_{int}) and divided by the elementary charge of the electron (q) to obtain the corresponding dark (Q_{dark}). The PLS without dark, i.e. $PLS_{w/o\ dark}$ is computed as equation (6.2) by subtracting the percentage of the total charges collected in the sensing nodes (Q_{Total}).

$$Q_{dark} = \frac{I_{dark} \cdot T_{int}}{q} \tag{6.1}$$

$$PLS_{w/o\ dark} = PLS - \frac{I_{dark} \cdot Q_{dark}}{Q_{Total}} \tag{6.2}$$

Table 6.1: DMC_{300MHz} and PLS for different combination of significant parameter for different process alternatives of a germanium CAPD obtained in 2D simulation.

Ge-P+ layer	**Added Si-bottom**	DMC_{300MHz} (%)	PLS (%)
No	Yes	19.0	18.2
Yes	No	94.7	8.4
	Yes	94.8	8.4

Table 6.2: PLS without dark (i.e. $PLS_{w/o}$) and leakage current in SN_1 for different combination of significant parameter for different process alternatives of a germanium CAPD obtained in 2D simulation.

Ge-P+ Layer	**Added Si-bottom**	$PLS_{w/o}$ (%)	I_{dark} **in** SN_1 $(pA/\mu m)$)
No	Yes	14.4	282.3
Yes	No	6.9	2.36
	Yes	6.9	2.39

Résumé en français

Introduction et contexte

Outre les capteurs 2D classiques utilisés pour les photos, des capteurs 3D ont été développés afin de fournir une information de profondeur [3]. Ils mesurent la distance entre la caméra et un point de la scène pour chaque pixel. La popularité de l'imagerie 3D est croissante, avec des applications potentielles vastes : l'industrie automobile s'y intéresse pour améliorer la sécurité, tandis que pour les smartphones ou les ordinateurs, ces capteurs peuvent servir à la reconnaissance faciale pour sécuriser les paiements ou offrir de nouvelles méthodes de déverrouillage.

Le travail de thèse s'inscrit dans le développement de capteurs d'image numériques CMOS chez STMicroelectronics, visant à produire des capteurs innovants pour les applications grand public. Dans l'équipe R&D de STMicroelectronics dédiée aux technologies des capteurs optiques, ce travail a porté sur le développement d'un nouveau pixel pour l'acquisition d'images 3D, combinant l'expertise existante de l'entreprise avec de nouvelles avancées technologiques. Cette thèse se concentre sur la conception et l'optimisation de capteurs d'image à temps de vol indirect (iToF), très répandus pour la mesure de distance. L'objectif global est de concevoir et optimiser des solutions iToF innovantes, couvrant la modélisation, la simulation, la conception et la fabrication. Le travail de thèse est décomposé en 5 chapitres.

Le chapitre 1 présente un panorama des techniques optiques de mesure de distance, expliquant les principes du temps de vol (ToF) et le cas particulier des méthodes iToF avec une onde modulée en intensité. Les différents types de capteurs optiques, incluant capteurs 2D et 3D, sont décrits. Le chapitre 2 détaille la méthodologie de simulation utilisée pour la conception et l'optimisation des pixels iToF, notamment les outils TCAD (Technology Computer-Aided Design) pour l'analyse de l'architecture pixel. Le chapitre 3 complète cette approche avec une méthodologie Monte Carlo pour simuler les pixels iToF, permettant d'obtenir des grandeurs statistiques et une meilleure compréhension des figures de bruit.

Les chapitres 4 et 5 présentent les études de développement de nouveaux pixels à partir des méthodologies décrites dans les chapitres précédents. Le chapitre 4 traite des architectures CMOS compatibles à "intégration rapide" pour iToF, notamment les pixels CAPD (current assisted photonic demodulators), en analysant leurs avantages et limites. Le chapitre 5 s'intéresse à celles à "intégration sophistiquée", incluant les pixels empilés et autres développements pour des dispositifs haute performance, avec l'optimisation des paramètres technologiques et géométriques.

Synthèse des principaux résultats par chapitre

Chapitre 1 : Techniques de mesure de distance

Les techniques de mesure de distance sont variées. L'une de ces techniques est le temps de vol indirect (iToF). Celle-ci mesure la différence de phase entre un signal émis modulé en intensité et le signal reçu, permettant une mesure précise de la distance. Ceci est réalisé par l'intermédiaire des différents grilles de transfert (TG) qui ramènent les charges photogénérées à des noeuds sensibles (SN). Les différents TG sont opérés en alternance avec un signal déphasé pour faire l'échantillonnage du signal photogenéré. L'équation 2 décrit le calcul de la valeur de phase (ϕ) à partir de la quantité de charges collectées sur les différents SN (Q_{SN_1}, Q_{SN_2}, Q_{SN_3} & Q_{SN_4}), pour un pixel avec quatre SNs et quatre TGs.

$$\Delta\phi = arctan(\frac{Q_{SN_4} - Q_{SN_2}}{Q_{SN_3} - Q_{SN_1}}) \tag{2}$$

Trois types de pixels iToF sont identifiés : (i) le "current assisted photonique demodulator" (CAPD) [16] et (ii) la "photodiode pinnée" (PPD) [17, 18, 58], (iii) ainsi qu'une nouvelle approche utilisant des grilles verticales ("dual VG") [30]. Une vue d'ensemble des performances pour ces différents capteurs est présentée au tableau 3. Les performances des différentes alternatives sont comparées par l'intermediaire de figures de mérite.

1. Puissance consommée: Intimement liée aux forts courants pour le pilotage de TG en fréquence.

2. Contraste de demodulation (DMC): Indique l'efficacité de transfert des charges photogénérées et est corrélé au temps de transit des charges photogénérées et à la sensibilité à la lumière parasite (PLS).

3. Efficacité quantique (QE): Le ratio entre le signal électrique collecté en quantité de charges et le nombre de photons incidents.

Un exemple schématique d'un pixel PPD iToF à l'état de l'art est illustré en figure 8.

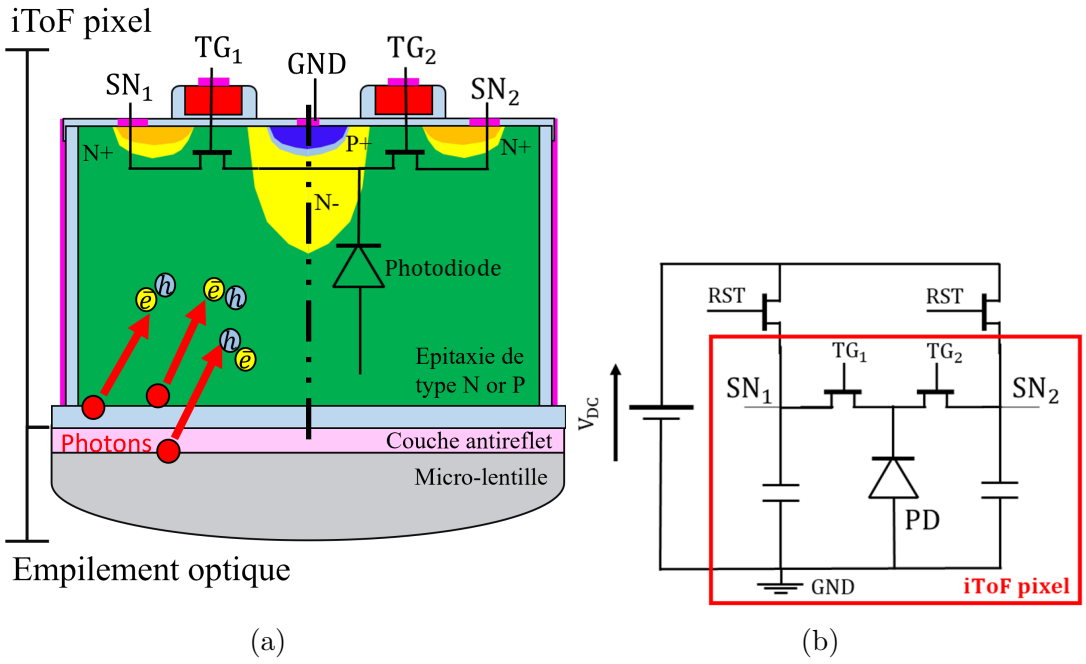
Chapitre 2 : Méthodologie de simulation multiphysique

Une méthodologie complète combinant des simulations TCAD (process, électrique) avec simulation optique par FDTD lumerical a été développée pour calculer les figures de mérite clés des pixels iToF : consommation, contraste de démodulation (DMC), sensibilité à la lumière parasite (PLS) et efficacité quantique (QE).

Les simulations reproduisent fidèlement les résultats mesurés après calibrage, notamment pour la DMC. La présentation de ces résultats est faite pour le résumé du chapitre 3, où la méthode avec la simulation Monte Carlo est réalisée et comparée avec la méthologie multiphysique en TCAD & FDTD. Cette méthodologie permet une évaluation qualitative et quantitative des performances.

Table 3: Performances iToF à l'état de l'art.

	"Dual VG" iToF	**PPD iToF**		**CAPD**	
	Yorikado [30] (2023)	***Keel [17] (2021)***	***Tubert [18] (2021)***	***Chen [53] (2020)***	***Jang [63] (2021)***
Process	Empilement 90nm/65nm	Empilement 65nm/40nm	Empilement 65nm/65nm	Ge-sur-Si	Empilement 90nm/65nm
Taille du pixel (μm)	3.0	3.5	4.6	10.0	5.0
Taps	2	4	2	2	2
Matrice de pixels	640x480	1280x960	672x804	240x960	640x480
DMC @f_{Mod}	88% @200MHz	80% @200MHz	88.5% @200MHz	70% to 90% @500MHz	80% —
QE @$\lambda(nm)$	38% @940	38% @940	18.5% @940	46.3% @1310	—
Puissance consommé	—	290mW (capteur)	300mW (sistème)	200mW (capteur)	140mW (capteur)



(a) (b)

Figure 8: (a) Coupe transversale de la structure d'un pixel iToF avec deux grilles de transfert (TG_1 et TG_2), deux nœuds de détection (SN_1 et SN_2), un implant profond de type N pour la création de la photodiode, l'isolation de tranchée profonde (DTI) et la superposition optique. (b) Le circuit électronique équivalent du pixel pour la structure donnée est mis en évidence par un carré rouge.

Chapitre 3 : Simulation Monte Carlo 3D

Les simulateurs TCAD classiques basés sur la dérive-diffusion présentent des limites lorsqu'il s'agit de prendre en compte la variabilité de détection. Pour pouvoir extraire des informations supplémentaires reposant sur des incertitudes statistiques, d'autres approches sont envisagées. Des exemples de telles informations sont les figures de mérite statistiques comme la non-uniformité de réponse des pixels (PRNU) et la non-uniformité de profondeur (DNU). Pour cela, une méthode Monte Carlo a été dévéloppée pour simuler le transfert des charges photogénérées au sein d'un pixel vers les noeuds de lecture.

Un comparatif de la méthodologie développée au chapitre 2 avec la méthodologie Monte Carlo est montré en figure 9. La simulation Monte Carlo 3D confirme les tendances du DMC observées avec TCAD et mesurées expérimentalement, avec un léger décalage expliqué par la mobilité dégradée et la largeur d'impulsion réelle non modélisée.

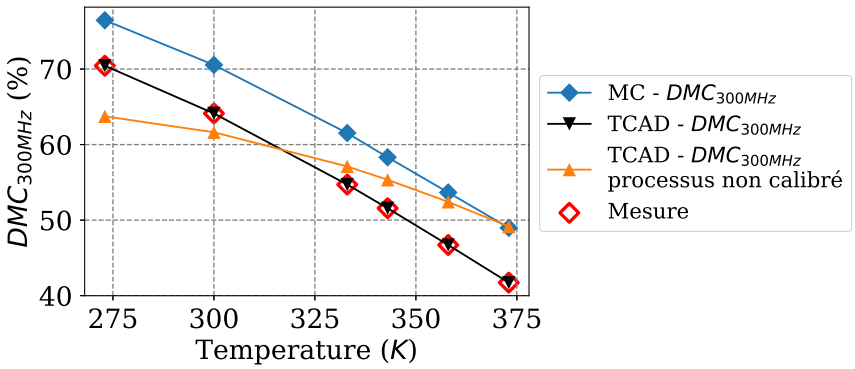


Figure 9: DMC à $300MHz$ en fonction de la température pour la comparaison entre simulations MC et TCAD avec les résultats mesurés.

Cette approche permet d'étudier les variations statistiques liées à la non-uniformité de réponse des pixels (PRNU) et à la non-uniformité en profondeur (DNU). Pour réduire ces variations, il est nécessaire d'augmenter la QE et la totalité des charges collectés.

Des mesures complémentaires et de nouveaux bancs de test sont envisagés pour approfondir la compréhension des contributions PRNU et DNU.

Chapitre 4 : Études sur les pixels CAPD

Deux pistes ont été explorées : (i) CAPD en silicium, (ii) CAPD en germanium.

(i) Le CAPD silicium a été étudié par rétro-ingénierie d'un capteur commercial [45]. Une solution fonctionnelle compatible a été simulée, avec des améliorations possibles par réduction de la concentration en dopage du substrat pour optimiser le potentiel électrique et réduire la consommation, limitée cependant par les contraintes de fabrication.

Le principal frein est la réduction du pitch, limitée à environ $3.5\mu m$ à cause des fuites entre nœuds de détection.

(ii) Le CAPD germanium, intéressant pour les applications SWIR [44], a été simulé et fabriqué en partenariat avec le CEA LETI sur plateforme germanium-sur-silicium. Le principal inconvénient est le signal d'obscurité élevé lié à la faible largeur de bande interdite du germanium. La réduction du pitch semble moins problématique que pour le silicium, mais les limitations technologiques restent importantes.

Chapitre 5 : Nouvelle solution avec grilles verticales

Une nouvelle technologie de pixel iToF est proposée. Celle-ci, le fast photogate (FPG) utilisant des grilles verticales (TVG), surmonte les limites des grilles planaires. Le pixel est illustré schématiquement en figure 10.

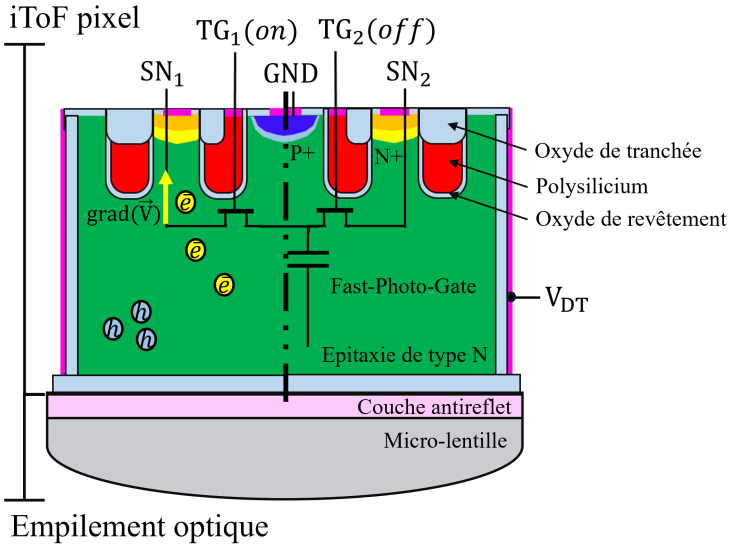


Figure 10: Schéma en coupe transversale du pixel FPG iToF de la structure simulée avec grilles en tranchée, contacts et isolation profonde de pixel (DTI) polarisée à V_{DT}.

Les TVG sont des structures MOS enfouies, formées par remplissage de tranchées, offrant un excellent contrôle électrostatique et une meilleure efficacité de transfert de charges. Les simulations montrent une amélioration du compromis QE/DMC, avec une QE élevée (40%) à 940nm, un DMC supérieur à 80% à 200MHz, et une sensibilité à la lumière parasite quasi nulle. Les valeurs de DMC obtenues avec ce nouveau pixel sont comparées avec celles du précédent pixel aux grilles planaires en figure 11. Des valeurs plus élevées de DMC sont obtenues à des tensions de polarisation plus faibles pour la FPG.

Le tableau 4 synthétise et compare les figures de mérite obtenues avec ce nouveau pixel par rapport aux technologies existantes. Les faibles tensions de polarisation utilisées, nécessaires aux transferts des charges photogénérées, ont pour conséquence la baisse de la consommation du pixel. En plus, il est attendu que l'absence d'implant profond améliore l'uniformité du champ électrique, réduisant DNU et PRNU.

Différents paramètres de fabrication (profondeur SNTI, profondeur TVG, profils d'épitaxie) ont été optimisés par simulation. La fabrication des dispositifs est en cours, avec l'intégration dans des capteurs complets.

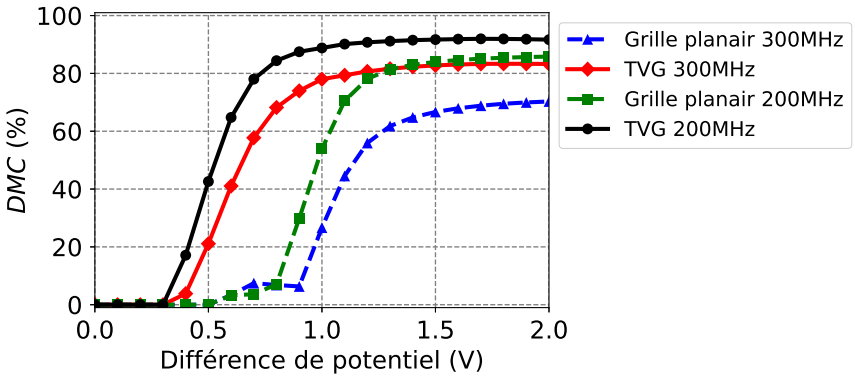


Figure 11: Comparaison entre pixels iToF à grille en tranchée et grille plane, meilleur cas, DMC à 200MHz et 300MHz en fonction de la différence de potentiel, ΔV, entre les grilles de transfert (TG).

Table 4: iToF à grilles en tranchée versus grilles planes

iToF pixel	**TVGs**	**Grilles planaires**		
	Ce travail	***Keel [17] (2021)***	***Tubert [18] (2021)***	***Ebiko [58] (2020)***
DMC @f_{Mod}	89% @200MHz	80% @200MHz	88.5% @200MHz	79% @200MHz
QE@940nm	40%	38%	18.5%	32%
Puissance consommé p/ pixel @f_{Mod} @ΔV	$1.2\mu W$ (2-taps) @200MHz @1.0V	— @200MHz @1.05V	$1.4\mu W$ (2-taps) @200MHz @1.2V	— @200MHz @1.2V

Un futur travail de simulation Monte Carlo est prévu pour étudier la réduction des variations PRNU et DNU.

Perspectives

La validation expérimentale des dispositifs fabriqués est cruciale pour confirmer les résultats prometteurs des simulations et valider la méthodologie innovante développée pour les pixels TVG iToF.

Des structures tests ont été conçues pour valider les étapes majeures du procédé, notamment la fonctionnalité des TVG. L'intégration des pixels TVG dans des capteurs complets, marque la première boucle de fabrication TVG iToF chez STMicroelectronics. Une deuxième itération sera probablement nécessaire pour résoudre les problèmes éventuels, valider les choix technologiques et apporter des améliorations.

Enfin, une étude complémentaire par simulation Monte Carlo est prévue pour approfondir la compréhension et la réduction des non-uniformités PRNU et DNU, avec l'espoir d'améliorer encore la performance des pixels.

References

[1] W. S. Boyle and G. E. Smith. "Charge Coupled Semiconductor Devices". In: *Bell System Technical Journal* 49.4 (1970), pp. 587–593. DOI: https://doi.org/10.1002/j.1538-7305.1970.tb01790.x.

[2] S. Mendis, S.E. Kemeny, and E.R. Fossum. "CMOS active pixel image sensor". In: *IEEE Transactions on Electron Devices* 41.3 (1994), pp. 452–453. DOI: 10.1109/16.275235.

[3] M. Bigas, E. Cabruja, J. Forest, and J. Salvi. "Review of CMOS image sensors". In: *Microelectronics Journal* 37.5 (2006), pp. 433–451. DOI: https://doi.org/10.1016/j.mejo.2005.07.002.

[4] Yole. *Statu of the CMOS image sensor industry 2023*. https://www.yolegroup.com/product/report/status-of-the-cmos-image-sensor-industry-2023/. Accessed: November 14, 2023. 2023.

[5] Yole. *3D imaging sensing 2023*. https://www.yolegroup.com/product/report/3d-imaging--sensing-2023/. Accessed: November 14, 2023. 2023.

[6] Brett E. Bouma and Guillermo J. Tearney. *Handbook of Optical Coherence Tomotraphy*. 2002.

[7] Bahaa Saleh and Malvin Teich. *Fundamentals of Photonics*. 2007.

[8] Fabrizio De Nisi. "A novel CMOS sensor for position detection". In: *Proceedings of IEEE Sensors* 2 (2003), pp. 1277–1282.

[9] Fabrizio De Nisi. "A CMOS sensor optimized for laser spot-position detection". In: *Proceedings of IEEE Sensors* 5 (2005), pp. 1296–1304.

[10] Robert Lange. "3D Time-of-Flight Distance Measurement with Custom Solid-State Image Sensors in CMOS/CCD-Technology". In: *Sensors Peterborough NH* 222 (2000), p. 223.

[11] Robert Lange and Peter Seitz. "Solid-state time-of-flight range camera". In: *IEEE Journal of Quantum Electronics* 37.3 (2001), pp. 390–397. DOI: 10.1109/3.910448.

[12] Boris Rodrigues. "Développement d ' un pixel innovant de type temps de vol pour des capteurs d ' image 3D-CMOS". In: *THESE de DOCTORAT DE L'UNIVERSITE DE LYON* (2018).

[13] R. Lange, S. Böhmer, and B. Buxbaum. "11 - CMOS-based optical time-of-flight 3D imaging and ranging". In: *High Performance Silicon Imaging (Second Edition)*. Ed. by Daniel Durini. Second Edition. Woodhead Publishing Series in Electronic and Optical Materials. Woodhead Publishing, 2020, pp. 319–375. DOI: https://doi.org/10.1016/B978-0-08-102434-8.00011-8.

[14] Jason Geng. "Structured-light 3D surface imaging: a tutorial". In: *Advances in Optics and Photonics* 3 (2011), pp. 128–160. DOI: 10.1364/AOP.3.000128.

[15] Kota Ito. "A Back Illuminated 10um SPAD Pixel Array Comprising Full Trench Isolation and Cu-Cu Bonding with Over 14% PDE at 940nm". In: (2020), pp. 16.6.1–16.6.4. DOI: 10.1109/iedm13553.2020.9371944.

[16] Yuichi Kato. "320x240 Back-Illuminated 10-um CAPD Pixels for High-Speed Modulation Time-of-Flight CMOS Image Sensor". In: *IEEE Journal of Solid-State Circuits* 53.4 (2018), pp. 1071–1078. DOI: 10.1109/JSSC.2018.2789403.

[17] Min-Sun Keel. "A 4-tap 3.5um 1.2Mpixel indirect time-of-flight CMOS image sensor with peak current mitigation and multi-user interference cancellation". In: *IEEE International Solid-State Circuits Conference, ISSCC* (2021), pp. 106–108. DOI: 10.1109/ISSCC42613.2021.9365854.

[18] Cedric Tubert. "4.6um Low Power Indirect Time-of-Flight Pixel Achieving 88.5% Demodulation Contrast at 200MHz for 0.54MPix Depth Camera". In: *ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference, Proceedings* (2021), pp. 135–138. DOI: 10.1109/ESSCIRC53450.2021.9567878.

[19] American National Standard for Safe Use of Lasers. *Laser Institute of America*. Version ANSI Z136.1-2014 revision of ANSI Z136.1-2007. 2014.

[20] Sergey Velichko. "Overview of CMOS Global Shutter Pixels". In: *IEEE Transactions on Electron Devices* 69.6 (2022), pp. 2806–2814. DOI: 10.1109/TED.2021.3136148.

[21] M. Wany and G.P. Israel. "CMOS image sensor with NMOS-only global shutter and enhanced responsivity". In: *IEEE Transactions on Electron Devices* 50.1 (2003), pp. 57–62. DOI: 10.1109/TED.2002.807253.

[22] Qian Zhang and Zhongjie Guo. "An 8T global shutter pixel with extended output range for CMOS image sensor". In: *2019 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*. 2019, pp. 1–3. DOI: 10.1109/EDSSC.2019.8754501.

[23] Chen Xu. "5.1 A Stacked Global-Shutter CMOS Imager with SC-Type Hybrid-GS Pixel and Self-Knee Point Calibration Single Frame HDR and On-Chip Binarization Algorithm for Smart Vision Applications". In: *2019 IEEE International Solid-State Circuits Conference - (ISSCC)*. 2019, pp. 94–96. DOI: 10.1109/ISSCC.2019.8662441.

[24] K. Ito. "A Back Illuminated 10µm SPAD Pixel Array Comprising Full Trench Isolation and Cu-Cu Bonding with Over 14% PDE at 940nm". In: *2020 IEEE International Electron Devices Meeting (IEDM)*. 2020, pp. 16.6.1–16.6.4. DOI: 10.1109/IEDM13553.2020.9371944.

[25] Edward Van Sieleghem. "A Backside-Illuminated Charge-Focusing Silicon SPAD With Enhanced Near-Infrared Sensitivity". In: *IEEE Transactions on Electron Devices* 69.3 (2022), pp. 1129–1136. DOI: 10.1109/TED.2022.3143487.

[26] Henna Ruokamo, Lauri W. Hallman, and Juha Kostamovaara. "An 80x25 Pixel CMOS Single-Photon Sensor With Flexible On-Chip Time Gating of 40 Subarrays for Solid-State 3-D Range Imaging". In: *IEEE Journal of Solid-State Circuits* 54.2 (2019), pp. 501–510. DOI: 10.1109/JSSC.2018.2878816.

[27] Ward Van Der Tempel. "A 1k-pixel 3D CMOS sensor". In: *Proceedings of IEEE Sensors* (2008), pp. 1000–1003. DOI: 10.1109/ICSENS.2008.4716611.

[28] Andreas Süss. "Benchmarking time-of-flight based depth measurement techniques". In: *Smart Photonic and Optoelectronic Integrated Circuits XVIII*. Ed. by Sailing He, El-Hang Lee, and Louay A. Eldada. Vol. 9751. International Society for Optics and Photonics. SPIE, 2016, p. 975118. DOI: 10.1117/12.2212478.

[29] Donguk Kim. "Indirect Time-of-Flight CMOS Image Sensor With On-Chip Background Light Cancelling and Pseudo-Four-Tap/Two-Tap Hybrid Imaging for Motion Artifact Suppression". In: *IEEE Journal of Solid-State Circuits* 55.11 (2020), pp. 2849–2865. DOI: 10.1109/JSSC.2020.3021246.

[30] Yuhi Yorikado. "Tap mismatch mitigation of 3 um 2-tap pixels of indirect Time-of-Flight image sensor for high-speed depth mapping". In: *Proceedings of the 2023 International Image Sensor Workshop (IISW)* (2023).

[31] Congzhen Hu. "Compact Numerical Modeling of Indirect Time-of-Flight CMOS Image Sensors". In: *IEEE Transactions on Electron Devices* 69 (2022), pp. 6897–6903.

[32] Donguk Kim. "5.4 A Dynamic Pseudo 4-Tap CMOS Time-of-Flight Image Sensor with Motion Artifact Suppression and Background Light Cancelling Over 120klux". In: *2020 IEEE International Solid-State Circuits Conference - (ISSCC)*. 2020, pp. 100–102. DOI: 10.1109/ISSCC19947.2020.9063101.

[33] Simone Bellisai. "Single-photon pulsed-light indirect time-of-flight 3D ranging". In: *Optics Express* 21 (2013), pp. 5086–5098. DOI: 10.1364/OE.21.005086.

[34] Simon Sze. *Physics of Semiconductor Devices*. ser. Wiley-Interscience publication. John Wiley and Sons, 1981.

[35] Moustafa El Kurdi, Guy Fishman, Sébastien Sauvage, and Philippe Boucaud. "Band structure and optical gain of tensile-strained germanium based on a 30 band k·p formalism". In: *Journal of Applied Physics* 107.1 (2010).

[36] Chenming Calvin Hu. 2009.

[37] SDevice. *Sentaurus Device User Guide*. Version S-2021.06. 2021.

[38] Eric R. Fossum and Donald B. Hondongwa. "A Review of the Pinned Photodiode for CCD and CMOS Image Sensors". In: *IEEE Journal of the Electron Devices Society* 2.3 (2014), pp. 33–43. DOI: 10.1109/JEDS.2014.2306412.

[39] M. Furumiya. "High sensitivity and no-cross-talk pixel technology for embedded CMOS image sensor". In: *International Electron Devices Meeting 2000. Technical Digest. IEDM (Cat. No.00CH37138)*. 2000, pp. 701–704. DOI: 10.1109/IEDM.2000.904415.

[40] Y. Hagiwara. "High-density and high-quality frame transfer CCD imager with very low smear, low dark current, and very high blue sensitivity". In: *IEEE Transactions on Electron Devices* 43.12 (1996), pp. 2122–2130. DOI: 10.1109/16.544383.

[41] Li Weiping. "Collection efficiency and charge transfer optimization for a 4-T pixel with multi n-type implants". In: *Journal of Semiconductors* 32.12 (2011), p. 124008. DOI: 10.1088/1674-4926/32/12/124008.

[42] Danil Van Nieuwenhove. "Photonic Demodulator With Sensitivity Control". In: *IEEE Sensors Journal* 7.3 (2007), pp. 317–318. DOI: 10.1109/JSEN.2006.890164.

[43] Cristine Jin Estrada. "Physical Model of Current-Assisted Photonic Demodulator (CAPD) for Time-of-Flight CMOS Image Sensor". In: *IEEE Transactions on Electron Devices* 67.7 (2020), pp. 2825–2830. DOI: 10.1109/TED.2020.2995349.

[44] N Na, S-L Cheng, H-D Liu, M-J Yang, C-Y Chen, K-C Chu, H-W Chen, Y-T Chou, C-T Lin, W-H Liu, et al. "Proposal and demonstration of germanium-on-silicon lock-in pixels for indirect time-of-flight based three-dimensional sensing". In: *arXiv preprint arXiv:1806.07972* (2018).

[45] Edge AI Vision. *Why the Sony IMX570 is the Leading iTOF Sensor*. 2023. URL: https://www.edge-ai-vision.com/2023/04/why-the-sony-imx570-is-the-leading-itof-sensor/ (visited on 04/15/2023).

[46] Markus Dielacher. "Advancements in indirect Time of Flight image sensors in front side illuminated CMOS". In: *European Solid-State Device Research Conference* 2021-Septe.1 (2021), pp. 139–142. DOI: 10.1109/ESSDERC53440.2021.9631809.

[47] Tampon Inventor. "Tampon patent to be replaced with BDTI if i can mention it". Pat. mzeltkazntest.

[48] François Roy. "Fully Depleted, Trench-Pinned Photo Gate for CMOS Image Sensor Applications". In: *Proceedings of IEEE Sensors* (2020).

[49] John Scott-Thomas. "Trends and Developments in State-of-the-Art CMOS Image Sensors". In: *Proceedings of the Int'l Image Sensor Workshop (IISW), Crieff, UK*. 2023.

[50] Sungsoo Choi. "World smallest 200Mp CMOS image sensor with 0.56 μm pixel equipped with novel deep trench isolation structure for better sensitivity and higher CG". In: *Proceedings of the Int'l Image Sensor Workshop (IISW), Crieff, UK*. 2023, pp. 22–25.

[51] Jungbin Yun. "A 0.6 µm Small Pixel for High Resolution CMOS Image Sensor with Full Well Capacity of 10,000e- by Dual Vertical Transfer Gate Technology". In: *2022 IEEE Symposium on VLSI Technology and Circuits*. 2022, pp. 351–352. DOI: 10.1109/VLSITechnologyandCir46769.2022.9830254.

[52] Sungbong Park. "A 64Mpixel CMOS Image Sensor with 0.56µm Unit Pixels Separated by Front Deep-Trench Isolation". In: *2022 IEEE International Solid-State Circuits Conference (ISSCC)*. Vol. 65. 2022, pp. 1–3. DOI: 10.1109/ISSCC42614.2022.9731750.

[53] C.-L. Chen. "5.3 An Up-to-1400nm 500MHz Demodulated Time-of-Flight Image Sensor on a Ge-on-Si Platform". In: *2020 IEEE International Solid-State Circuits Conference - (ISSCC)*. 2020, pp. 98–100. DOI: 10.1109/ISSCC19947.2020.9063107.

[54] Y. Kumagai. "Back-Illuminated 2.74 µm-Pixel-Pitch Global Shutter CMOS Image Sensor with Charge-Domain Memory Achieving 10k e-Saturation Signal". In: *2018 IEEE International Electron Devices Meeting (IEDM)*. 2018, pp. 10.6.1–10.6.4. DOI: 10.1109/IEDM.2018.8614676.

[55] Seung-Sik Kim. "3-Layer Stacked Voltage-Domain Global Shutter CMOS Image Sensor with 1.8µm-Pixel-Pitch". In: *2022 International Electron Devices Meeting (IEDM)*. 2022, pp. 37.5.1–37.5.4. DOI: 10.1109/IEDM45625.2022.10019515.

[56] Geunsook Park. "A 2.2µm stacked back side illuminated voltage domain global shutter CMOS image sensor". In: *2019 IEEE International Electron Devices Meeting (IEDM)*. 2019, pp. 16.4.1–16.4.4. DOI: 10.1109/IEDM19573.2019.8993606.

[57] Boris Rodrigues. "Indirect ToF pixel integrating fast buried-channel transfer gates and gradual epitaxy and enabling CDS". In: *Proc. IISW* (2017), pp. 266–269.

[58] Yoshiki Ebiko. "Low power consumption and high resolution 1280X960 Gate Assisted Photonic Demodulator pixel for indirect Time of flight". In: *International Electron Devices Meeting, IEDM* (2020). DOI: 10.1109/IEDM13553.2020.9372109.

[59] Xiaolin Shi, Jiangtao Xu, Kaiming Nie, and Zhiyuan Gao. "A Low kTC Noise and Low FPN Reset Method for Pixel in ToF Image Sensor". In: *IEEE Sensors Journal* 22.3 (2022), pp. 2053–2061. DOI: 10.1109/JSEN.2021.3135348.

[60] E Oran Brigham. "The Fast Fourier Transform Prentice-Hall". In: *Englewood Cliffs, NJ* 19742 (1974).

[61] Texas Instruments. *CMOS Power Consumption and C pd Calculation*. Version SCAA035B, June, 1997, [Online]. 1997.

[62] Ramjee Prasad. *Analog and Digital Electronic Circuits: Fundamentals, Analysis, and Applications*. Springer Nature, 2021.

[63] Jaehyung Jang. "An Ultra-low current operating 5-µm Vertical Field Modulator Pixel for in-direct Time of Flight 3D Sensor". In: *2020 International Image Sensor Workshop (IISW)*. 2020.

[64] SProcess. *Sentaurus Process User Guide*. Version S-2021.06. 2021.

[65] Kane Yee. "Numerical solution of initial boundary value problems involving Maxwell's equations in isotropic media". In: *Transactions on Antennas and Propagation IEEE* 14 (3 1988), pp. 302–307. DOI: 10.1109/TAP.1966.1138693.

[66] A. R. Forouhi and I. Bloomer. "Optical properties of crystalline semiconductors and dielectrics". In: *Phys. Rev. B* 38 (3 1988), pp. 1865–1874. DOI: 10.1103/PhysRevB.38.1865.

[67] David F. Edwards. "- Silicon (Si)". In: *Handbook of Optical Constants of Solids*. Ed. by Edward D. Palik. Burlington: Academic Press, 1997, pp. 547–569. DOI: https://doi.org/10.1016/B978-012544415-6.50027-3.

[68] H.R. Philipp. "- Silicon Dioxide (SiO2) (Glass)". In: *Handbook of Optical Constants of Solids*. Ed. by Edward D. Palik. Burlington: Academic Press, 1997, pp. 749–763. DOI: https://doi.org/10.1016/B978-012544415-6.50038-8.

[69] Axel Crocherie. "From photons to electrons: a complete 3D simulation flow for CMOS image sensor". In: *Proceedings of the 2009 International Image Sensor Workshop (IISW)* 1 (2009), pp. 1–4.

[70] Jerome Michallon. "Etude et optimisation de l ' absorption optique et du transport électronique dans les cellules photovoltaiques à base de nanofils". In: *'PhD manuscript, HAL Id: tel-01171003'* (2015).

[71] Lumerical. *Inc., FDTD: 3D Electromagnetic Simulator*. Version version 2022-r6. 2022.

[72] Andreas Schenk. "A Model for the Field and Temperature Dependence of Shockley-Read-Hall Lifetimes in Silicon". In: *Solid-State Electronics* 35 (1992), pp. 1585–1596.

[73] W Hänsch and M Miura-Mattausch. "The hot-electron problem in small semiconductor devices". In: *Journal of applied physics* 60.2 (1986), pp. 650–656.

[74] Syed Aon Mujtaba. "Advanced Mobility Models for Design and Simulation of Deep Submicrometer MOSFETs". PhD thesis. Stanford, CA, USA: Stanford University, 1995.

[75] M.N. Darwish, J.L. Lentz, M.R. Pinto, P.M. Zeitzoff, T.J. Krutsick, and Hong Ha Vuong. "An improved electron and hole mobility model for general purpose device simulation". In: *IEEE Transactions on Electron Devices* 44.9 (1997), pp. 1529–1538. DOI: 10.1109/16.622611.

[76] Cyrus Bamji. "A Review of Indirect Time-of-Flight Technologies". In: *IEEE Transactions on Electron Devices* 69.6 (2022), pp. 2779–2793. DOI: 10.1109/TED.2022.3145762.

[77] Gabriel Mugny. "Demodulation Contrast simulation for indirect Time-of-Flight sensors based on Fast Photo-Diode". In: *Proceedings of the 2021 International Image Sensor Workshop (IISW), Online* (2021).

[78] L. Viña and M. Cardona. "Effect of heavy doping on the optical properties and the band structure of silicon". In: *Phys. Rev. B* 29 (12 1984), pp. 6739–6751. DOI: 10.1103/PhysRevB.29.6739.

[79] C Jacoboni and P Lugli. "The Monte Carlo Method for Semiconductor Device Simulation". In: *Computational Microelectronics* (1989).

[80] F Rosset and A Pilotto. "A model for the jitter of avalanche photodiodes with separate absorption and multiplication regions". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 977 (2020). DOI: https://doi.org/10.1016/j.nima.2020.164346.

[81] Remi Helleboid. "A Fokker-Planck-based Monte Carlo method for electronic transport and avalanche simulation in single-photon avalanche diodes". In: *Journal of Physics D: Applied Physics* 55.50 (2022). DOI: 10.1088/1361-6463/ac9b6a.

[82] Grigorios A. Pavliotis. *Stochastic Processes and Applications*. Springer-Verlag New York Inc., 2014. Chap. Diffusion Processes, the Fokker-Planck and Langevin Equations.

[83] Andrej Suler. "Développement d ' un pixel photogate éclairé par la face arrière". In: *'PhD manuscript, HAL Id : tel-03632251'* (2022).

[84] EMVA. "Standard for Characterization of Image Sensors and Cameras". In: *European Machine Vision Association (EMVA) Standard 1288* (2021), pp. 26–31.

[85] Keita Yasutomi. "A Sub-100µm-Range-Resolution Time-of-Flight Range Image Sensor With Three-Tap Lock-In Pixels, Non-Overlapping Gate Clock, and Reference Plane Sampling". In: *IEEE Journal of Solid-State Circuits* (2019), pp. 2291–2303.

[86] F Sun. "A Simple Analytic Modeling Method for SPAD Timing Jitter Prediction". In: *IEEE Journal of the Electron Devices Society* 7 (2019), pp. 261–267.

[87] Jonathan S Steckel. "High resolution quantum dot global shutter imagers". In: *SID Symposium Digest of Technical Papers*. Vol. 52. 1. Wiley Online Library. 2021, pp. 975–977.

[88] Jiwon Lee. "Imaging in short-wave infrared with 1.82 µm pixel pitch quantum dot image sensor". In: *2020 IEEE International Electron Devices Meeting (IEDM)*. IEEE. 2020, pp. 16–5.

[89] S. Manda. "High-definition Visible-SWIR InGaAs Image Sensor using Cu-Cu Bonding of III-V to Silicon Wafer". In: *2019 IEEE International Electron Devices Meeting (IEDM)*. 2019, pp. 16.7.1–16.7.4. DOI: 10.1109/IEDM19573.2019.8993432.

[90] R. Fraenkel. "Development of low-SWaP and low-noise InGaAs detectors". In: *Infrared Technology and Applications XLIII*. Ed. by Bjørn F. Andresen, Gabor F. Fulop, Charles M. Hanson, John Lester Miller, and Paul R. Norton. Vol. 10177. International Society for Optics and Photonics. SPIE, 2017, p. 1017703. DOI: 10.1117/12.2262112.

[91] Quentin Durlin. "Fabrication and characterisation of the PiN Ge photodiode with poly-crystalline Si: P as n-type region". In: *Opto-Electronics Review* 31.Special Issue (2023).

[92] Caitlin Rouse. "Development of low dark current SiGe near-infrared PIN photodetectors on 300 mm silicon wafers". In: *Optics and Photonics Journal* 6.05 (2016), p. 61.

[93] Jurgen Michel, Jifeng Liu, and Lionel C Kimerling. "High-performance Ge-on-Si photodetectors". In: *Nature photonics* 4.8 (2010), pp. 527–534.

[94] Daniel Van Nieuwenhove, Ward Van Der Tempel, and Maarten Kuijk. "Novel Standard CMOS Detector using Majority Current for guiding Photo-Generated Electrons towards Detecting Junctions". In: *2005 IEEE/LEOS Symposium Benelux Chapter*. Annual IEEE/LEOS Symposium Benelux Chapter. Annual IEEE/LEOS Symposium Benelux Chapter, 2005.

[95] L. Pancheri. "Current assisted photonic mixing devices fabricated on high resistivity silicon". In: *SENSORS, 2008 IEEE*. 2008, pp. 981–983. DOI: 10.1109/ICSENS.2008.4716606.

[96] Gian-Franco Dalla Betta. "Design and Characterization of Current-Assisted Photonic Demodulators in 0.18- µm CMOS Technology". In: *IEEE Transactions on Electron Devices* 58.6 (2011), pp. 1702–1709. DOI: 10.1109/TED.2011.2126578.

[97] Quazi Delwar Hossain, Gian-Franco Dalla Betta, Lucio Pancheri, and David Stoppa. "Current assisted photonic mixing demodulator implemented in 0.18µm standard CMOS technology". In: *2009 Ph.D. Research in Microelectronics and Electronics*. 2009, pp. 212–215. DOI: 10.1109/RME.2009.5201367.

[98] Chong Li, Chunlai Xue, Zhi Liu, Buwen Cheng, Chuanbo Li, and Qiming Wang. "High-Bandwidth and High-Responsivity Top-Illuminated Germanium Photodiodes for Optical Interconnection". In: *IEEE Transactions on Electron Devices* 60.3 (2013), pp. 1183–1187. DOI: 10.1109/TED.2013.2241066.

[99] François Guyader. "3-Tier BSI CIS with 3D Sequential and Hybrid Bonding Enabling a1 . 4um pitch , 106dB HDR Flicker Free Pixel". In: *International Electron Devices Meeting, IEDM* (2022), pp. 898–901.

[100] Taesub Jung. "A 4-tap global shutter pixel with enhanced IR sensitivity for VGA time-of-flight CMOS image sensors". In: *IS&T International Symposium on Electronic Imaging Science and Technology* 103.7 (2020), pp. 1–6. DOI: 10.2352/ISSN.2470-1173.2020.7.ISS-103.

[101] Nayera Ahmed. "MOS Capacitor Deep Trench Isolation for CMOS image sensors". In: (2014), pp. 4.1.1–4.1.4. DOI: 10.1109/IEDM.2014.7046979.

[102] Paul Stampfer, Gerald Meinhardt, Tibor Grasser, and Michael Waltl. "Simulating and modeling the influence of deep trench interface recombination on Si photodiodes". In: *2022 IEEE International Integrated Reliability Workshop (IIRW)*. IEEE. 2022, pp. 1–5.

[103] Junsik Lee. "0.6 μm F-DTI based quad-cell with advanced optic technology for all-pixel PDAF and high sensitivity/SNR performance". In: *Proceedings of the Int'l Image Sensor Workshop (IISW), Crieff, UK*. 2023, pp. 22–25.

[104] Thomas Dalleau. "Etude et optimisation d ' un capteur d ' images à collection de trous". In: *THESE de DOCTORAT DE L'UNIVERSITE DE LYON* (2022).

[105] Charalambos C. Katsidis and Dimitrios I. Siapkas. "General transfer-matrix method for optical multilayer systems with coherent, partially coherent, and incoherent interference". In: *Appl. Opt.* 41.19 (2002), pp. 3978–3987. DOI: 10.1364/AO.41.003978.

[106] Chun Yung Ai. "0.56 μm-pitch CMOS image sensor for high resolution application". In: *Proceedings of the Int'l Image Sensor Workshop (IISW), Crieff, UK*. 2023, pp. 22–25.

[107] OnlyMetals.com. *Melting Point*. https://www.onlinemetals.com/en/melting-points. Accessed: November 17, 2023. 2022.

[108] Celestin Doyen. "Caractérisations électriques innovantes de capteurs d ' image CMOS à l'aide de structures de test". In: *DOCTORAT DE L'UNIVERSITE DE TOULOUSE* (2021).

[109] Samuel Tlemsani. "Analysis methodology of Deep Trench Isolation Field-Effect Passivation techniques for Image Sensors through dedicated test structures". In: *2024 IEEE International Conference on Microelectronic Test Structures*. 2024.

[110] Shota Kitamura. "Low-Noise Multi-Gate Pixel Transistor for Sub-Micron Pixel CMOS Image Sensors". In: *2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*. IEEE. 2022, pp. 347–348.

[111] Rimantas Knizikevičius and Vitoldas Kopustinskas. "Anisotropic etching of silicon in SF 6 plasma". In: *Vacuum* 77 (2004), pp. 1–4. DOI: 10.1016/j.vacuum.2004.07.063.

[112] K. A. Ellis and R. A. Buhrman. "Phosphorus Diffusion in Silicon Oxide and Oxynitride Gate Dielectrics". In: *Electrochemical and Solid-State Letters* 2.10 (1999), p. 516. DOI: 10.1149/1.1390888.

[113] C. -P. Chang. Ed. by K.H. Jürgen Buschow, Robert W. Cahn, Merton C. Flemings, Bernhard Ilschner, Edward J. Kramer, Subhash Mahajan, and Patrick Veyssière. Oxford: Elsevier, 2001. Chap. Shallow Trench Isolation, pp. 8437–8444. DOI: https://doi.org/10.1016/B0-08-043152-6/01508-4.

[114] Kelsey M Judd, Michael P Thornton, and Austin A Richards. "Automotive sensing: Assessing the impact of fog on LWIR, MWIR, SWIR, visible, and lidar performance". In: *Infrared Technology and Applications XLV*. Vol. 11002. SPIE. 2019, pp. 322–334.

[115] Scott M Spuler and Shane D Mayor. "Scanning eye-safe elastic backscatter lidar at 1.54 μm". In: *Journal of Atmospheric and Oceanic Technology* 22.6 (2005), pp. 696–703.

[116] C Osorio Quero. "Evaluation of a 3D imaging vision system based on a single-pixel InGaAs detector and the time-of-flight principle for drones". In: *Three-Dimensional Imaging, Visualization, and Display 2020*. Vol. 11402. SPIE. 2020, pp. 63–72.

[117] Qiwei Xu. "Ultrafast colloidal quantum dot infrared photodiode". In: *ACS Photonics* 7.5 (2020), pp. 1297–1303.

[118] Dima Bederak. "PbS colloidal quantum dots for near-infrared optoelectronics". English. PhD thesis. University of Groningen, 2021. DOI: 10.33612/diss.172171198.