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Design of a multi-standard IR-UWB transmitter with pulse shaping capabilities based on frequency transposition synthesis

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Résumé et mots clés

Les communications dites radio-impulsionnelles ultra large bande (IR-UWB) reposent sur des transmissions à faible rapport cyclique réalisées à l'aide d'impulsions brèves (de l'ordre de la ns) envoyées à des débits modérés (de l'ordre de la dizaine de Mbps). Elles sont particulièrement pertinentes pour des applications courte portée (de l'ordre de la dizaine de mètres) où elles autorisent une localisation à 5 cm près des dispositifs compatibles.

Les communications IR-UWB ont principalement été normalisées par les standards IEEE dédiés aux réseaux personnels sans fil (WPAN ; standard IEEE 802.15.4) et aux réseaux corporels sans fil (WBAN ; standard IEEE 802.15.6). Dans ce contexte, un axe important de recherche est la conception d'émetteurs multistandard capables de couvrir l'intégralité des canaux standardisés qui d'une part, s'étalent de 3,1 GHz à 10,6 GHz et d'autre part, sont associés à des masques d'émissions radio-féquence différents à respecter.

Pour répondre à cette problématique, une architecture d'émetteur IR-UWB à transposition de fréquence permettant le réglage de la fréquence porteuse et de l'enveloppe des impulsions générées est proposée dans ce manuscrit. Elle présente également l'avantage de compenser les variations de process, de tension et de température (PVT), ainsi que d'optimiser la réjection des lobes secondaires et donc de limiter les interférences avec les canaux adjacents et les autres technologies de communication sans-fil fonctionnant à des fréquences voisines.

Ce travail de thèse présente tout d'abord les contraintes spectrales induites par la réglementation et par les standards IEEE. Puis, les formes d'enveloppes permettant de les respecter tout en étant synthétisables électroniquement parlant sont investiguées. Ensuite, une étude bibliographique sur les émetteurs IR-UWB est réalisée et la conception de deux émetteurs IR-UWB multistandard est proposée en technologie CMOS 28 nm. Même si l'un comme l'autre transposent en fréquence les oscillations provenant d'un oscillateur en anneau, la mise en forme des impulsions se fait pour le premier émetteur à l'aide d'un générateur d'enveloppes externe alors que pour le deuxième, celle-ci est faite par l'intermédiaire d'un générateur d'enveloppes intégré développé au cours de la thèse. Enfin, les résultats de mesure ont démontré la capacité du premier émetteur à synthétiser des impulsions pour l'ensemble des canaux IEEE compris dans la bande de fréquences 3,1-10,6 GHz. Les résultats de mesure du second émetteur ont quant à eux prouvé que les canaux les plus larges, canaux qui sont les plus difficiles à respecter du fait de la brièveté des impulsions associées, pouvaient être adressés grâce au générateur d'enveloppe intégré. Toutefois, l'intégralité des canaux IEEE compris entre 3,1 GHz et 10,6 GHz semble tout-à-fait accessible moyennant un ajustement de son dimensionnement.

Mots clés : Ultra-large bande; Emetteur; Multistandard; Générateur d'impulsions; Mise en forme d'enveloppe

Abstract and keywords

Ultra-wideband impulse Radio (IR-UWB) is a wireless communication technology well-suited for short-range communications (about 10 meters) and allows real-time location with a precision of 5 cm. Its use has been standardized in some standards, especially in the IEEE 802.15.4, dedicated to Wireless Personal Area Networks (WPAN), and the IEEE 802.15.6, dedicated to Wireless Body Area Networks (WBAN).

Although research on IR-UWB communications has been extensively conducted, the design of a multi-standard IR-UWB transmitter remains a significant topic. This is not an easy task since both the WPAN and WBAN IEEE standards introduce 499.2 MHz channels having distinct spectral masks, which must be respected in addition to local regulations. Additionally, the WPAN standard specifies several different bandwidths for the standardized channels.

To respect these constraints, a strategy consists of designing an IR-UWB transmitter based on frequency transposition able to tune the central frequency and envelope of generated pulses. Additionally, this versatility should equally allow the compensation of the Process, Voltage, and Temperature (PVT) variations, and a high enough rejection of side-lobe to protect adjacent channels and neighboring wireless communications.

After presenting the spectral requirements of each standard and some regulations, the modeling and characterization of pulse envelopes are presented. The objective is to find an envelope that can be easily synthesized while achieving a high side-lobe rejection and respecting the WPAN and WBAN spectral masks.

Next, based on the envelope shape study and a literature survey on the IR-UWB transmitter, the design of two multi-standard IR-UWB transmitters based on frequency transposition synthesis is proposed in 28 nm technology. The first circuit has pulse shaping controlled by an external arbitrary waveform generator, whereas the second integrates a shaping circuit of the pulse envelope.

A physical validation of the proposed designs has been done. The measurement results show that the first circuit with an external pulse shaping circuit can synthesize pulse addressing all IEEE standards channels in the 3-10.6 GHz frequency band.

However, the measurement results indicate that the second circuit with an integrated pulse shaping circuit generates pulse addressing only large-bandwidth IEEE channels in the 1-8.7 GHz frequency band with a side-lobe rejection of 26.7 dB. Nevertheless, issues have been identified and can be corrected.

Keywords: Ultra-wideband; Transmitter; Multi-standard; Pulse Generator; Envelope Shaping

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List of acronyms

AC

Alternating Current. 108, 135

AM

Amplitude Modulation. 117

AWG

Arbitrary Waveform Generator. 107–109, 117, 118, 123, 125, 133, 159

BLE

Bluetooth Low Energy. 29

BPM

Burst Position Modulation. 36

BPSK

Binary Phase-Shift Keying. 11, 36, 38, 89, 90, 95, 100, 102, 106, 110, 111, 133, 159

CCSI

Integrated Circuits and Systems Design. 25

CDR

Clock Data Recovery. 30

CML

Current Mode Logic. 14, 98, 99, 108, 110–112, 114–118, 124, 139, 150

CMOS

Complementary Metal Oxide Semiconductor. 25, 83–86, 89, 91–93, 95, 99–102, 108, 114, 121, 132, 135, 141, 147, 157, 161

DA

Driving Amplifier. 89

DAC

Digital-to-Analog Converter. 91

DB-BPSK

Delay-Based Binary Phase-Shift Keying. 84, 106, 133, 159

DBPSK

Differential Binary Phase-Shift Keying. 36

DC

Direct Current. 39, 108, 110, 135

DCA

Digitally-Controlled Amplifier. 15, 17, 135–139, 141, 144, 145, 147, 152, 155, 156

DCDL

Digitally Controlled delay line. 14, 15, 79, 89, 103, 104, 135, 137, 139, 141–145, 147, 150–152, 154, 156, 157, 161

DCO

Digitally Controlled Oscillator. 14, 78, 99–102

DCRO

Digitally Controlled Ring Oscillator. 103

DesSer

Deserialization-Serialization. 92

DPA

Digital Power Amplifier. 89, 95, 101–103

DQPSK

Differential Quadrature Phase-Shift Keying. 36

EIRP

Equivalent Isotropically Radiated Power. 31

ESD

Energy Spectral Density. 43, 173, 179

ETSI

European Telecommunications Standards Institute. 11, 15, 24, 25, 31, 32, 39–42, 82, 85, 95, 97, 105, 106, 127, 129, 133, 159

FCC

Federal Communication Commission of the United States. 11, 15, 16, 24, 25, 30–33, 39–42, 44, 57–64, 66–69, 72, 78–82, 86, 88, 97, 101, 103–108, 113, 115, 119, 124, 127, 129, 130, 132–135, 150, 152, 154, 155, 159–161

FD-SOI

Fully Depleted Silicon on Insulator. 101, 106, 133, 159

FFT

Fast Fourier Transform. 123

FIFO

First In First Out. 15, 139–143

GPS

Global Positioning System. 28

HRP

High Rate Pulse repetition frequency. 11, 17, 32–36, 38, 44

IEEE

Institute of Electrical and Electronics Engineers. 11–13, 15, 17, 24, 25, 27, 28, 30–42, 44, 57–69, 74, 76–88, 90–97, 100–108, 110, 112, 119, 124, 127–130, 132–134, 136, 139, 141, 144, 150, 152–155, 157, 159–161

IM2NP

Institut Matériaux Microélectronique et Nanosciences de Provence. 25

IoT

Internet of Things. 27

IR

Impulse-Radio. 24

IR-UWB

Impulse-Radio Ultra-Wideband. 11–17, 24–27, 29–31, 33, 35, 37–41, 43, 44, 57–60, 62, 63, 65, 67–69, 72–74, 81–85, 87–93, 95–98, 101–109, 112, 113, 115, 117, 121–124, 127, 130–137, 145, 147–153, 155–157, 159–161

ISI

Intersymbol Interference. 92

LNA

Low Noise Amplifier. 30

LO

Local Oscillator. 106, 133, 159

LP-WPAN

Low-Power Wireless Personal Area Network. 32

LRP

Low Rate Pulse repetition frequency. 17, 32–34, 36, 37

LSB

Least Significant Bit. 91, 140, 142, 152

LUT

Look-Up Table. 89, 91, 106, 133, 159

MOS

Metal Oxide Semiconductor. 25, 87, 98, 143

MSB

Most Significant Bit. 91, 140, 142

NFC

Near Field Communications. 29

NMOS

N-channel Metal Oxide Semiconductor. 84, 119, 121, 142, 147

OOK

On-Off Keying. 11, 36, 37, 84, 88, 90, 106, 133, 159

PA

Power Amplifier. 85

PA-FLL

Phase-Aligned Frequency-Locked Loop. 14, 100, 101, 106, 133, 159

PAM

Pulse Amplitude Modulation. 36

PCB

Printed Circuit Board. 14, 122, 148

PHY

physical layer. 11, 17, 27, 32–38, 44

PLL

Phase-Locked Loop. 14, 91, 92, 95–97

PMOS

P-channel Metal Oxide Semiconductor. 103, 111–113, 118, 119, 121, 137, 147

PPM

Pulse Position Modulation. 11, 36–38, 106, 133, 159

PRF

Pulse Repetition Frequency. 15, 37, 39, 82, 93, 97, 109, 130, 136, 138, 139, 144, 145, 155

PSD

Power Spectral Density. 29, 31, 43, 82, 171

PSK

Phase-Shift Keying. 36, 38

PSU

Puls-Shaping Unit. 101

PVT

Process, Voltage and Temperature. 24, 91, 95, 96, 98, 102, 117, 136

QFN

Quad Flat No-leads. 121, 122, 147, 148

QPSK

Quadrature Phase-Shift Keying. 38

QVCO

Quadrature Voltage-Controlled Oscillator. 14, 95–97

RF

Radio Frequency. 89, 101, 102, 113, 121–124

SNR

Signal-to-Noise Ratio. 29, 30

SoC

System-on-Chip. 101

SPI

Serial Peripheral Interface. 139, 148, 157

TPSC

True Single-Phase-Clock. 96

UMTS

Universal Mobile Telecommunications System. 28

UWB

Ultra-wideband. 11, 13, 14, 17, 24, 25, 28–39, 42, 44, 79, 86, 87, 89, 92, 93, 98, 100, 101

VCA

Voltage-Controlled Amplifier. 14, 17, 108, 109, 114, 116–121, 124–126, 130–132, 134, 135, 137, 161

VCDL

Voltage-Controlled Delay Line. 81, 84, 105, 161

VCO

Voltage-Controlled Oscillator. 14, 15, 17, 81, 88, 89, 98, 99, 104, 108–114, 116, 117, 119–121, 124, 125, 130–132, 134–136, 138, 139, 144, 147, 150, 151, 155–157, 160

VCRO

Voltage-Controlled Ring Oscillator. 14, 110, 111

WBAN

Wireless Body Area Network. 24, 25, 27, 34, 83, 160

WLAN

Wireless Local Area Network. 28

WPAN

Wireless Personal Area Network. 24, 25, 27, 160

Introduction

Since the decade of 1960s, the generation and exploitation of short pulses applied to radio communications have been a research topic [1]. The shorter the pulse, the greater the spectrum bandwidth. Nevertheless, the term Ultra-wideband (UWB) was only introduced 3 decades later, in the decade of 1990s. The name Impulse-Radio (IR) arose in 1992 from the utilization of these pulses in the telecommunications field. This corresponds to the starting point of several research works [2]. In 1997, the terms UWB and IR were merged into the acronym Impulse-Radio Ultra-Wideband (IR-UWB), which is used to nominate impulse radio communications in high frequency [3, 4]. Due to extensive research work done within UWB communications, the Federal Communication Commission of the United States (FCC) evaluated from 1998 to 2002 the feasibility of authorizing the exploitation of the UWB systems [5]. As a result, in 2002, the 3.1-10.6 GHz frequency band was authorized to be exploited by non-licensed applications in the United States [6]. Next, in Europe, the European Telecommunications Standards Institute (ETSI) authorized in 2006 the use of the 6-8.5 GHz frequency band dedicated to UWB applications [7].

Since the beginning of the last decade, many short-range communications standards for Wireless Personal Area Network (WPAN) and Wireless Body Area Network (WBAN) have been defined [8, 9]. Consequently, this has enabled the emergence of innovative physical layers that allow a transmitter power consumption from 1 mW to 10 µW. For instance, the UWB enables the exploitation of the properties of the IR, such as a 5 cm accurate real-time location, in addition to data transmission with a bit rate of several tens of Mbps [10]. Nowadays, it should be noticed that UWB technology has been massively deployed since September 2019 thanks to Apple's iPhone 11 launch. The UWB is available on Apple's iPhone 11 models and later [11]. These devices are equipped with a UWB chip, enabling high-accuracy indoor positioning.

Context

IR-UWB communications have been largely studied in the literature. Nevertheless, the design of a multi-standard IR-UWB transmitter remains an important research topic [12–14]. Indeed, WPAN and WBAN IEEE standards introduced different radio-frequency spectral masks to comply with. Moreover, the WPAN one defines several different bandwidths for the standardized channels. Since an IR-UWB transmitter is a pulse generator, it is also necessary to design pulse generators with envelope shaping and central frequency tuning capabilities to achieve a multi-standard design. Besides, this versatility must be fine enough to compensate for the Process, Voltage and Temperature (PVT) variations to which pulse generators are very sensitive. For these reasons, IR-UWB transmitters are, in fact, more pulse synthesizers than pulse generators, as can be seen in the literature.

Since 2004, the Integrated Circuits and Systems Design (CCSI) team of Institut Matériaux Microélectronique et Nanosciences de Provence (IM2NP) has carried out UWB research activities. They are focused on the realization of non-coherent impulse receivers and UWB transmitters based on pulse generators [15, 16]. These are the core of the transmitters. The CCSI team has studied several architectures of pulse generators and later architectures of pulse synthesizers.

Firstly, between 2004 and 2008, a pulse generator based on an impulse response filter was the first developed UWB transmitter. It was implemented in 130 nm CMOS technology [12, 17–19]. This transmitter was able to comply with American and European regulations. Nevertheless, this transmitter could not achieve bandwidth restricted to a few hundred MHz required by the IEEE standards.

Secondly, between 2008 and 2018, the research has focused on architectures of pulse synthesizers, which only use Metal Oxide Semiconductor (MOS) transistors [13, 20]. One is based on a gated oscillator, and the other is on a delay line. The pulse synthesizers based on gated oscillators can address IEEE standardized channels having distinct bandwidths by adjusting the turn-on time of the oscillator. However, a pulse shaping of the generated oscillations is required to comply at the same time with the spectral requirements imposed by the IEEE standards and regional regulations, like FCC or ETSI. On the other hand, the pulse synthesizers based on a delay line can perform a UWB pulse synthesis having a fine pulse shaping. However, this architecture is more suitable for the generation of pulses whose bandwidth is greater than 1 GHz. Consequently, it does not allow a feasible circuit that is completely compliant with IEEE standards. Therefore, since 2011 the UWB transmitter research focus has been only on pulse synthesizer architecture based on a gated oscillator.

Thus, the objective of this PhD manuscript is to develop, test, and validate a IR-UWB transmitter employing an architecture based on a gated oscillator with pulse shaping capabilities. The synthesizer design targets covering the 3.1-10.6 GHz frequency band while addressing the WPAN and WBAN IEEE standard channels. In other words, a multi-standard and multi-channel transmitter design. The pulse shaping capabilities are essential because the circuit must respect the spectral requirements imposed by regional regulations (FCC and ETSI), in addition to WPAN and WBAN IEEE standards. The circuit is implemented in 28 nm bulk CMOS technology.

Manuscript Structure

Chapter 1 addresses an overview of UWB communications. It presents the FCC and ETSI regulations, in addition to an overview of IEEE 802.15.4 (WPAN) and 802.15.6 (WBAN) standards. Chapter 2 addresses pulse envelope modeling and characterization. It addresses continuous envelopes like rectangular, triangular, and trapezoidal. On the other hand, it addresses sample and hold envelopes, which are a combination of shifted rectangular pulses. Chapter 3 addresses the state of the art of IR-UWB pulse transmitters. It presents two pulse synthesis methods reported in the literature: direct synthesis and synthesis by frequency transposition. Chapter 4 addresses the design, simulation, and physical validation of an IR-UWB transmitter based on a gated oscillator with pulse shaping controlled by an external arbitrary signal gener-

ator. First, a system overview is addressed. Next, the IR-UWB transmitter top-down design is presented. Lastly, the transmitter's global layout and measurements are addressed, in addition to a comparison with state-of-the-art transmitters. Likewise, Chapter 5 addresses the design, simulation, and physical validation of an IR-UWB transmitter based on a gated oscillator with a pulse shaping digital circuit. The circuit of Chapter 5 is an extension of the circuit addressed in Chapter 4. Similar to Chapter 4, a system overview, top-down design, global layout, and measurements of the transmitter are presented.

1. Ultra-wideband Communications Overview

Summary

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1.5. Conclusion 39

1.1. Introduction

The Wireless Personal Area Network (WPAN) and Wireless Body Area Network (WBAN) are wireless networks well-suited for communications between devices placed close to the human body which require a transmission rate of up to 10 Mbps. The WPAN and WBAN have been standardized by the IEEE 802.15.4 standard (10 m range) and the IEEE 802.15.6 (2 m range) [8, 9]. This standardization has focused on the 3.1-10.6 GHz frequency band. Both standards seek the optimization of the power consumption according to their own targeted range [21]. Both standards have several applications, such as wellness, safety, sports, the Internet of Things (IoT), and healthcare [22, 23]. Figure 1.1 shows an example of an application regarding healthcare. The network sensors (in red) placed on the human body transmit to a smartphone data relative to the heart rate, blood pressure, and oxygen rate. This smartphone, connected to the internet, sends healthcare data to a healthcare worker. Meanwhile, the network actuator (in green) can be a pacemaker whose finality is to generate electrical pulses to maintain the heartbeat at a normal rate. Nowadays, both sensors and actuators can be wearable [24, 25]. For example, there are the smartwatches produced by Apple [26] and activity trackers produced by Google Fitbit [27], both being worn on the wrist.

For the implementation of WPAN and WBAN, these standards exploit 2 types of physical layer (PHY): Narrowband and IR-UWB. Their spectrum shape is displayed in Figure 1.2.

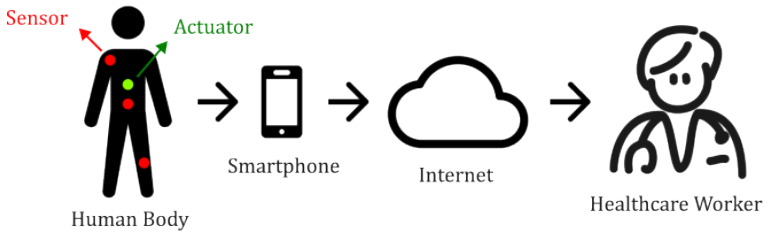


Figure 1.1.: Healthcare Application Diagram

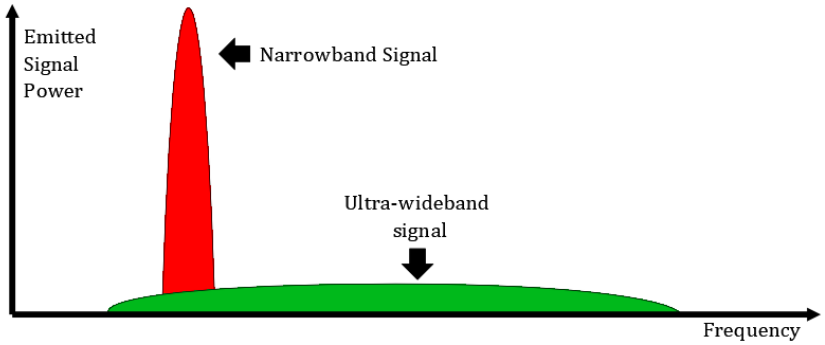


Figure 1.2.: Radio-frequency signals spectrum

Conventional narrowband devices are widely used for short-range wireless communications between nearby devices. A well-known narrowband radio technology is Bluetooth, which operates at 2.4 GHz. Bluetooth is employed in wireless communications between smartphones, computers, and peripherals (headset, mouse, keyboard). Moreover, narrowband devices have tracking capabilities with 100 cm accuracy. Narrowband uses a modulated carrier to perform data transmission and has a power consumption independent of the data rate. In addition to Bluetooth, there are lots of narrowband systems such as Global Positioning System (GPS), Universal Mobile Telecommunications System (UMTS), Wireless Local Area Network (WLAN) (Fig. 1.3).

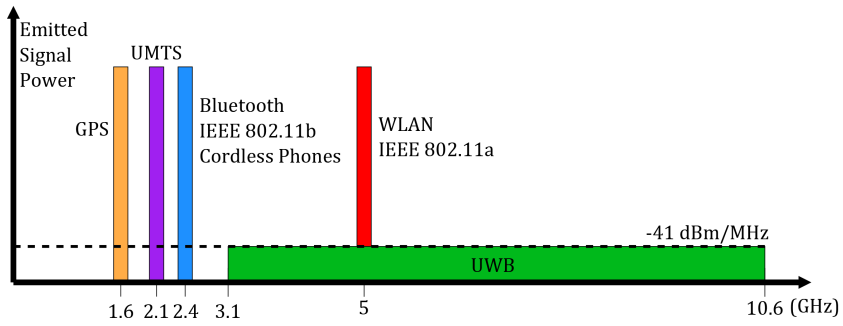


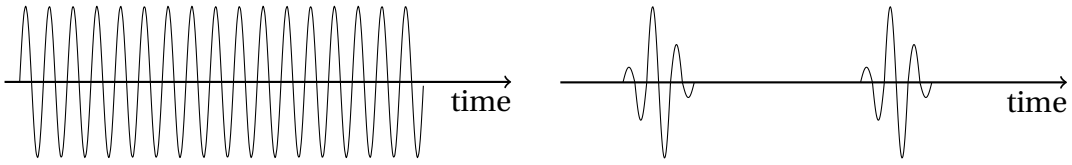
Figure 1.3.: Several technologies spectrum.

On the contrary, UWB devices can use low-duty cycle short pulses. To exploit the frequency band between 3.1 GHz and 10.6 GHz, the IEEE 802.15.4 and IEEE 802.15.6 standards have chosen the impulse radio instead of the usual carrier modulations, as shown in Figure 1.4.

An IR-UWB pulse typically has a duration lower than 5 ns (nanosecond order), which leads to a large bandwidth greater than 500 MHz. Thereby, the IR-UWB signal has the particularity to spread the signal energy on a frequency bandwidth of GHz order. This signal has an emitted Power Spectral Density (PSD) that is directly proportional to the squared modulus of the emitted pulse spectrum. This short duration allows IR-UWB pulses to have distinguishable multi-path interferences and also to be robust to multi-path fading [28]. The use of UWB improves the capacity of a channel within which the signal is transmitted [29]. Indeed, the Shannon's limit equation is expressed below:

$$C = BW \cdot log_2(1 + SNR) \tag{1.1}$$

where C is the channel capacity (bit/s), BW is the channel bandwidth, and SNR is the Signal-to-Noise Ratio. From expression 1.1, the greater the channel bandwidth, the greater the channel capacity for a given SNR.



(a) Narrowband waveform (b) IR-UWB waveform

Figure 1.4.: Traditional narrowband and IR-UWB signals comparison.

In addition, the short duration of IR-UWB pulses allows a real-time location with an accuracy of 5 cm [10], being more precise than narrowband devices. Thus, an interesting application of IR-UWB devices that can be highlighted is tracking luggage using an AirTag. AirTag is a keychain-sized tracking device developed by Apple [30]. It is designed to help people find personal belongings, in particular keys and bags. AirTag employs not only IR-UWB but also Bluetooth Low Energy (BLE) and Near Field Communications (NFC) [31]. For instance, a passenger during his travel can place an AirTag inside his luggage to locate it using his smartphone (iPhone). Figure 1.5 shows the process of luggage tracking. The Airtag can communicate with any nearby iPhone through IR-UWB communications. After, this iPhone transmits the AirTag position to the passenger's iPhone through the mobile network.

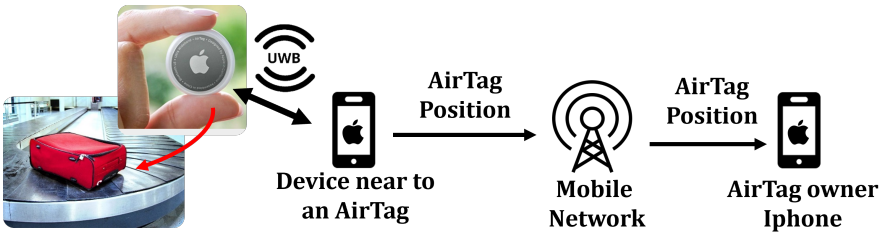


Figure 1.5.: Luggage Tracking Application Diagram.

Despite the UWB signal transmission's positive features, it is important to pay attention to some issues. Regardless of the low complexity of short pulse processing, the receiver

design is challenging, considering that the receiver front-end is power-hungry and both low transmitted power and wide-band noise lead to a low SNR of received signal [32]. This can be explained by the fact that the Low Noise Amplifier (LNA) often cannot be turned off since the LNA itself does not know precisely when the UWB pulses are transmitted. To overcome this, a pulse detector and a synchronizer block composed of a Clock Data Recovery (CDR) and window generation block are implemented to shut down the power-hungry LNA between the generation of consecutive pulses [33, 34]. Consequently, this reduces the receiver power consumption. Besides, the LNA drains more power when working in higher frequencies.

Finally, Figure 1.6 summarizes the comparison of the narrowband and IR-UWB device applications. In addition to the real-time location application of Figure 1.5, two other real-time location IR-UWB applications can be cited: in logistics, where an IR-UWB device can track an object in a warehouse, and in sports, where a player's real-time location is extracted to improve his performance.

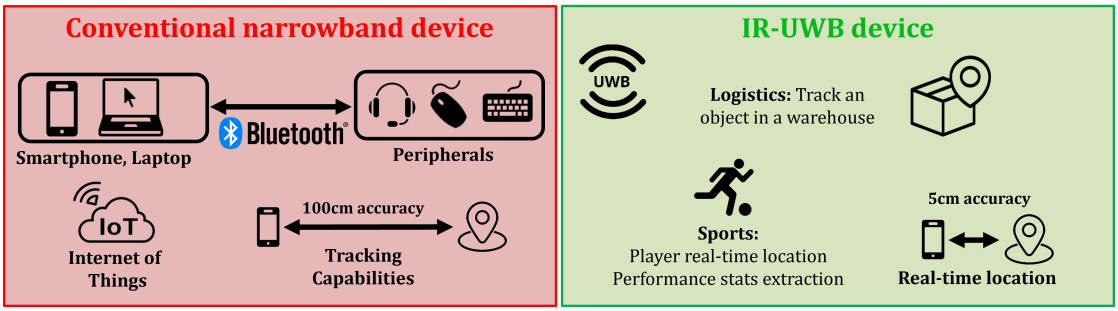


Figure 1.6.: Comparison of narrowband and IR-UWB devices applications.

1.2. Spectral Requirements Overview

First of all, the Federal Communication Commission of the United States (FCC) in 2002 defined the UWB frequency as the frequency band comprised between 3.1 GHz and 10.6 GHz [6, 35]. Since then, several standards exploiting this frequency have been defined like IEEE 802.15.4 and IEEE 802.15.6.

The signal bandwidth BW_{-XdB} can be expressed as a function of an attenuation value X_{dB}, being bounded by both upper frequency f_H and lower frequency f_L, such that (1.2):

$$BW_{-XdB} = f_H - f_L \tag{1.2}$$

The central frequency of the signal can be computed as:

$$f_c = \frac{f_H + f_L}{2} \tag{1.3}$$

Its fractional bandwidth can also be calculated as follows:

$$B_{frac} = \frac{BW_{-XdB}}{f_c} \tag{1.4}$$

Applying (1.2) and (1.3) on (1.4), the fractional bandwidth can be expressed as:

$$B_{frac} = 2\frac{f_H - f_L}{f_H + f_L} \tag{1.5}$$

1.2.1. FCC Regulations (United States)

According to FCC, an UWB signal must have a minimal absolute bandwidth of 500 MHz or a minimal fractional bandwidth of 20%, for an attenuation of 10 dB (Fig. 1.7). This means that for a UWB signal with a particular shape, the FCC restricts the signal's maximum duration.

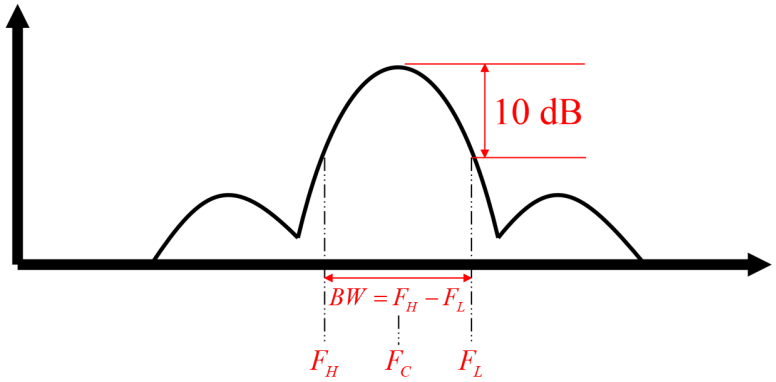


Figure 1.7.: IR-UWB Signal Spectrum.

Moreover, the UWB signal is authorized to be transmitted within the frequency band of 3.1 - 10.6 GHz with a maximum Equivalent Isotropically Radiated Power (EIRP) of -41.3 dBm/MHz [6, 36]. Figure 1.8 shows the indoor and handheld spectral masks defined by FCC regulations, delimiting the PSD of the UWB signal to be transmitted.

1.2.2. ETSI Regulations (Europe)

The European Telecommunications Standards Institute (ETSI) authorized in 2007 the use of UWB communications and radar systems [7, 37]. Figure 1.8 displays the spectral mask defined by European regulations and the comparison with the FCC indoor mask. The European mask authorizes a maximum EIRP of -41.3 dBm/MHz for the frequency band between 6-8.5 GHz. The IR-UWB emitted signal must be attenuated by 28.7 dB for the frequency band between 3.8-6 GHz, 43.7 dB for the frequency band between 1.6-3.8 GHz, and 23.7 dB for the frequency band between 8.5-10.6 GHz.

1.2.3. IEEE 802.15.4 Standard

IR-UWB devices should not only respect regional regulations but also IEEE standards spectral masks. Indeed, the IR-UWB emitted signal spectrum must fit into IEEE radio-frequency spectral masks. To clarify, an analogy is shown in Figure 1.9. The radio-frequency mask is the hole of a shape-matching box, whereas the emitted signal spectrum is the geometric shape.

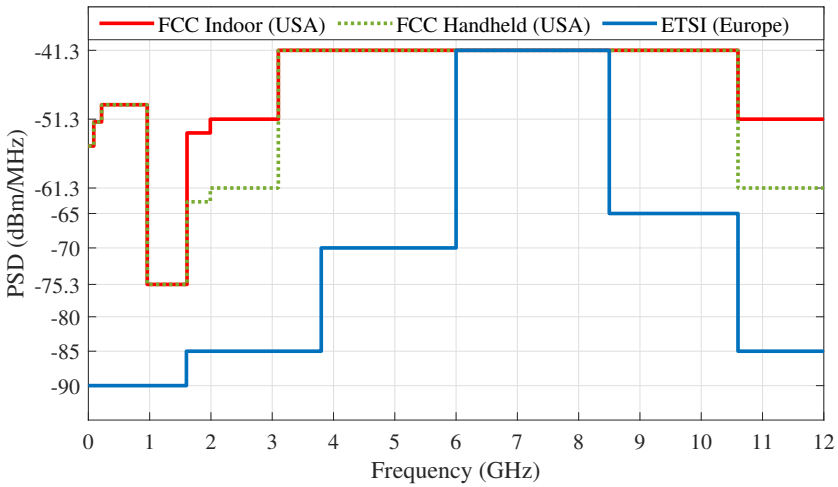


Figure 1.8.: FCC and ETSI spectral masks

Like the geometric shape must fit properly into the box hole, the signal spectrum must fit into the radio-frequency mask.

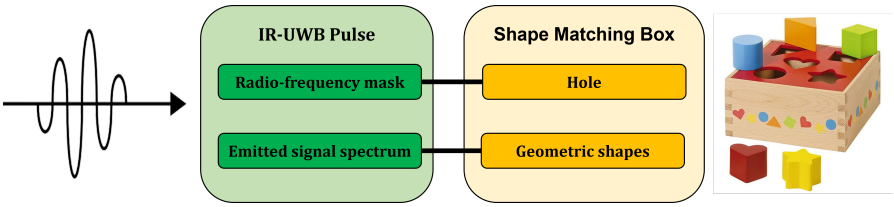


Figure 1.9.: Analogy to clarify radio-frequency masks.

In this sub-section, the IEEE 802.15.4 standard is addressed. This standard was introduced in 2011 and is dedicated to Low-Power Wireless Personal Area Network (LP-WPAN) applications [8]. This standard introduces two PHYs: High Rate Pulse repetition frequency (HRP) UWB PHY and Low Rate Pulse repetition frequency (LRP) UWB PHY.

The frequency band plan of IEEE 802.15.4 standard HRP UWB PHY is indicated in Figure 1.10. It defines 15 channels distributed in 3 groups: the sub-GHz band, low band, and high band. From Figure 1.10, every channel has a central frequency band and a bandwidth. This bandwidth is either 499.2 MHz, 1081 MHz, 1331 MHz, or 1355 MHz. A channel having a bandwidth greater than 1 GHz is considered a large-bandwidth channel. For a particular group, the UWB device must cover one channel in particular, indicated in red in Figure 1.10. The first group, the sub-GHz, has only one channel of 499.2 MHz. The second group, the low band, presents 3 channels of 499.2 MHz and one of 1331 MHz within the frequency band of 3.1-4.8 GHz. The third and last group, the high band, presents 9 channels of 499.2 MHz, one of 1081 MHz, one of 1331 MHz, and one of 1355 MHz within the frequency band of 6-10.6 GHz.

Table 1.1 summarizes the IEEE 802.15.4 15 channels specifications concerning the HRP UWB PHY. The center frequencies of all channels are integer multiples of 499.2 MHz. Thus, the 499.2 MHz adjacent channel centers are spaced at 499.2 MHz.

Figure 1.11 presents the IEEE 802.15.4 standard spectral masks displayed in Table 1.1, in addition to the 500 MHz minimal bandwidth imposed by FCC. The signal spectrum should not be much narrower than this minimal bandwidth. Namely, an IR-UWB signal spectrum with 500 MHz bandwidth respects all the four spectral masks of Figure 1.11. Nevertheless, this UWB spectrum only fits properly the spectral mask of Figure 1.11a. The interest is to exploit as maximum as possible the limits of the radio-frequency spectral masks. In other words, achieve a better spectrum occupancy. From Figure 1.11, it can be seen that larger pulses have a narrower spectrum, and shorter pulses wider spectrum. From this, it can be inferred that a pulse addressing channel 15 will be the shortest one.

On the other hand, the IEEE 802.15.4 standard LRP UWB PHY defines 3 channels between 6.5 GHz and 8 GHz. Each channel has a different frequency band and bandwidth. Table 1.2

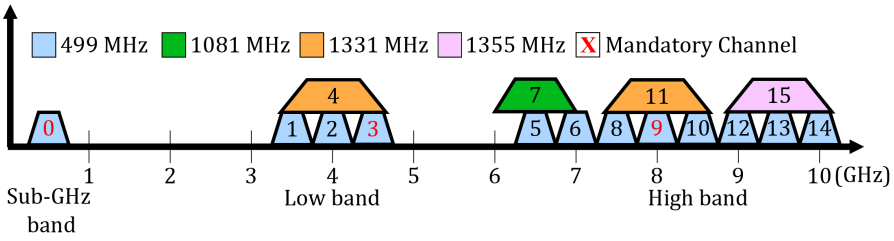
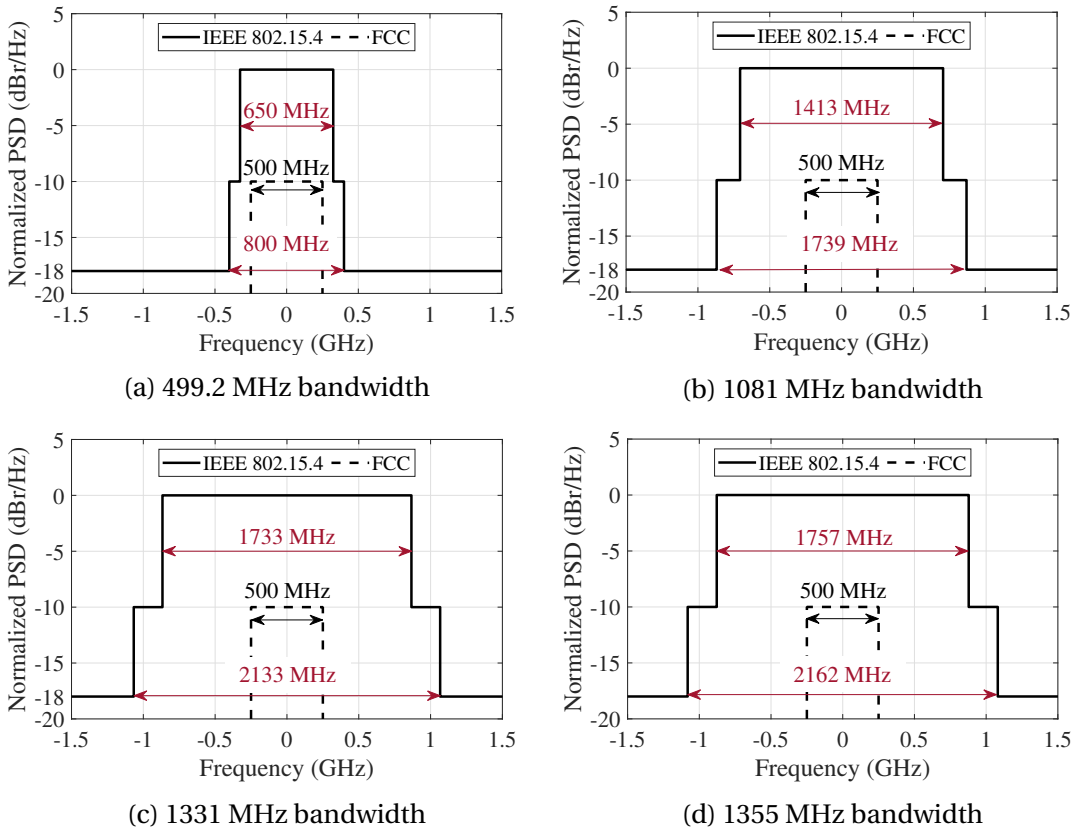


Figure 1.10.: IEEE 802.15.4 standard HRP UWB PHY frequency plan.

Table 1.1.: IEEE 802.15.4 Standard HRP UWB PHY channels specifications (Mandatory indicated in red).

Group	Channel	f_c (MHz)	BW (MHz)	BW_{-10dB} (MHz)	BW_{-18dB} (MHz)
0 Sub-GHz Band	0	499.2	499.2	650	800
1 Low Band	1	3494.4			
	2	3993.6	499.2	650	800
	3	4492.8			
	4	3993.6	1331.2	1733.33	2133.33
2 High Band	5	6489.6	499.2	650	800
	6	6988.8			
	7	6489.6	1081.2	1413.04	1739.13
	8	7488.0			
	9	7987.2	499.2	650	800
	10	8486.4			
	11	7987.2	1331.2	1733.33	2133.33
	12	8985.6			
	13	9484.8	499.2	650	800
	14	9984.0			
	15	9484.8	1355	1757.76	2162.16



(a) 499.2 MHz bandwidth

(b) 1081 MHz bandwidth

(c) 1331 MHz bandwidth

(d) 1355 MHz bandwidth

Figure 1.11.: IEEE 802.15.4 HRP UWB PHY channels spectral masks.

summarizes the IEEE 802.15.4 3 channels specifications concerning the physical layer LRP UWB PHY.

Table 1.2.: IEEE 802.15.4 Standard LRP UWB PHY channels specifications

Channel	f_c (MHz)	BW_{-10dB} (MHz)	BW_{-18dB} (MHz)
0	6489.6	1406.08	1730.56
1	6988.8	2146.56	2296.32
2	7987.2	1730.56	2129.92

1.2.4. IEEE 802.15.6 Standard

In this sub-section, the IEEE 802.15.6 standard is addressed. This standard was introduced in 2012 and is dedicated to WBAN applications. Its frequency band plan is indicated in Figure 1.12. This IEEE standard defines 11 channels distributed in 2 groups: low band and high band. For a particular group, the UWB device must cover one channel in particular, indicated in red in Figure 1.12. The first group, the low band one, contains 3 channels of 499.2 MHz within the

frequency band of 3.1-4.8 GHz. The other group, the high band one, presents 8 channels of 499.2 MHz within the frequency band of 6-10.6 GHz.

Table 1.3 summarizes the 11 channels, indicating which are mandatory and which are optional. Like IEEE 802.15.4 standard, the center frequencies of all channels are integer multiples of 499.2 MHz. Consequently, the 499.2 MHz adjacent channel centers are spaced at 499.2 MHz. Figure 1.13 presents the IEEE 802.15.6 standard spectral mask displayed in Table 1.3, in addition to the IEEE 802.15.4 (HRP) standard mask having a bandwidth of 499.2 MHz.

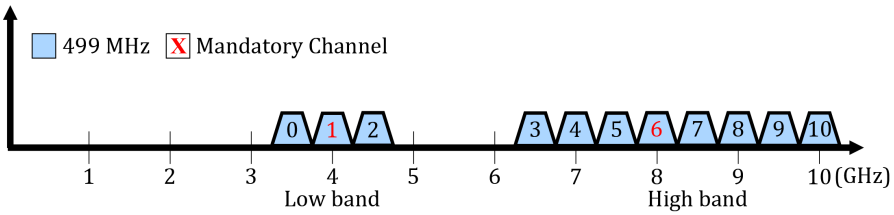


Figure 1.12.: IEEE 802.15.6 standard UWB PHY channels frequency plan

Table 1.3.: IEEE 802.15.6 Standard UWB PHY channels specifications (Mandatory indicated in red)

Group	Channel	f_c (MHz)	BW (MHz)	$BW_{-10\,dB}$ (MHz)	$BW_{-18\,dB}$ (MHz)	$BW_{-20\,dB}$ (MHz)
1 Low Band	0	3494.4	499.2	665.6	797.72	998.4
	1	3993.6				
	2	4492.8				
2 High Band	3	6489.6	499.2	665.6	797.72	998.4
	4	6988.8				
	5	7488.0				
	6	7987.2				
	7	8486.4				
	8	8985.6				
	9	9484.8				
	10	9984.0				

1.3. Modulation

The physical layers of a particular IEEE standard have not only specifications for radio-frequency masks but also specifications for modulations and data rates of the transmitters and receivers, as indicated in Table 1.4. For an IR-UWB pulse transmission, the data can be transmitted using different values of the emitted pulse parameters like amplitude, position, or polarity [12, 13].

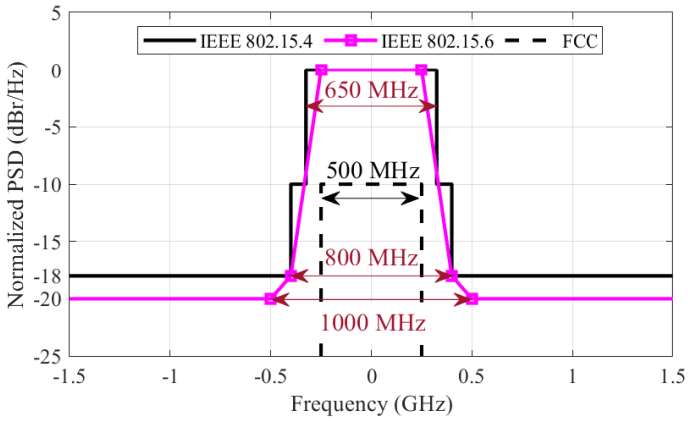


Figure 1.13.: IEEE 802.15.4 (HRP) and 802.15.6 standards spectral mask (BW = 499.2 MHz).

From Table 1.4, different pulse modulations are specified. To summarize them, they are divided into groups such as :

- Pulse Amplitude Modulation (PAM) in 2 levels, namely On-Off Keying (OOK) modulation
- Pulse Position Modulation (PPM) in 2 levels
- Phase-Shift Keying (PSK) modulation that can be Differential Binary Phase-Shift Keying (DBPSK), Differential Quadrature Phase-Shift Keying (DQPSK), or the combination of Burst Position Modulation (BPM) with Binary Phase-Shift Keying (BPSK) modulation (BPM-BPSK)

Table 1.4.: Pulse modulations and data rates associated with the physical layer of IEEE standard 802.15.4 and 802.15.6

Standard	IEEE 802.15.4		IEEE 802.15.6
PHY	HRP UWB	LRP UWB	UWB
Pulse Modulations	BPM-BPSK	PPM, OOK	OOK, DBPSK, DQPSK
Data rate associated Min. - Max.	0.11 Mbps - 27.24 Mbps	32.25 kbps - 1 Mbps	0.243 Mbps - 12.636 Mbps

To clarify, the BPSK modulation has 2 levels. The following sub-sections address the pulse modulations introduced in Table 1.4.

1.3.1. On-Off Keying Pulse Modulation (OOK)

From Table 1.4, the OOK pulse modulation is exploited by the physical layers LRP UWB of the standard IEEE 802.15.4 and UWB of the IEEE standard 802.15.6. The OOK pulse modulation is a simple pulse amplitude modulation in 2 levels. Each symbol corresponds to 1 bit. Figure 1.14

shows an OOK pulse modulation coding and waveform. T_p corresponds to a pulse duration, which is lower than a symbol period T_{Sb}. The transmitted symbols can be either '0' or '1'. They are coded according to the absence or presence of a pulse during a time interval of T_{Sb}. The signal emitted by the UWB antenna can be expressed as a combination of single pulses, such that:

$$s(t) = \sum_{k=0}^{\infty} d_k \cdot p\left(t - \left[k + \frac{1}{2}\right] T_S\right) \tag{1.6}$$

where $p(t)$ is the elementary generated pulse waveform centered at $t = 0$, and d_k is the kth emitted symbol taken from alphabet D, such that:

$$D : \{d_k\} = \{0, 1\} \tag{1.7}$$

To implement this pulse modulation, an IR-UWB transmitter only has to generate a pulse whose Pulse Repetition Frequency (PRF) is equal to the maximal symbol rate $1/T_{Sb}$ established by the physical layer of interest.

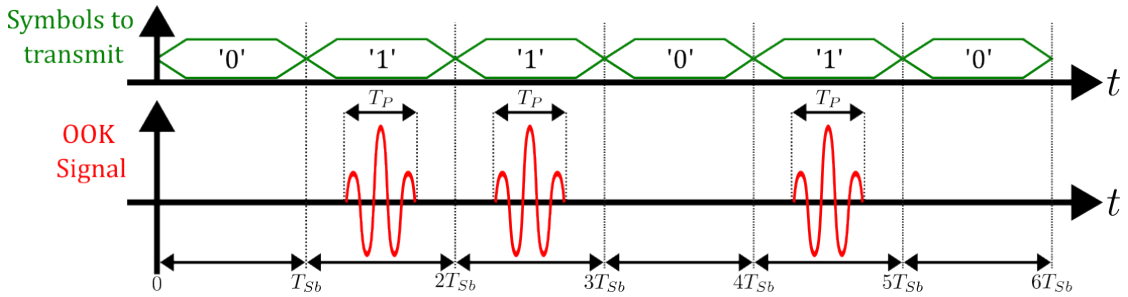


Figure 1.14.: OOK pulse modulation coding and waveform.

1.3.2. Pulse Position Modulation (PPM)

From Table 1.4, the PPM modulation is exploited by the physical layer LRP UWB of the standard IEEE 802.15.4. The principle of an M-PPM modulation in M levels consists of splitting the symbol period T_{Sb} into M uniform time intervals T_{PPM} such as:

$$T_{PPM} = \frac{T_S}{M} \tag{1.8}$$

$$M = 2^N \tag{1.9}$$

where N is the number of bits that represent one level of the M-PPM modulation. Each time interval T_{PPM} is associated with one of M symbols. To transmit this, the IR-UWB transmitter should just transmit one or several pulses during the time interval T_{PPM}. For instance, Figure 1.15 shows a PPM pulse modulation coding and waveform for a M = 4. In this Figure, only one pulse was generated within the 4 time intervals.

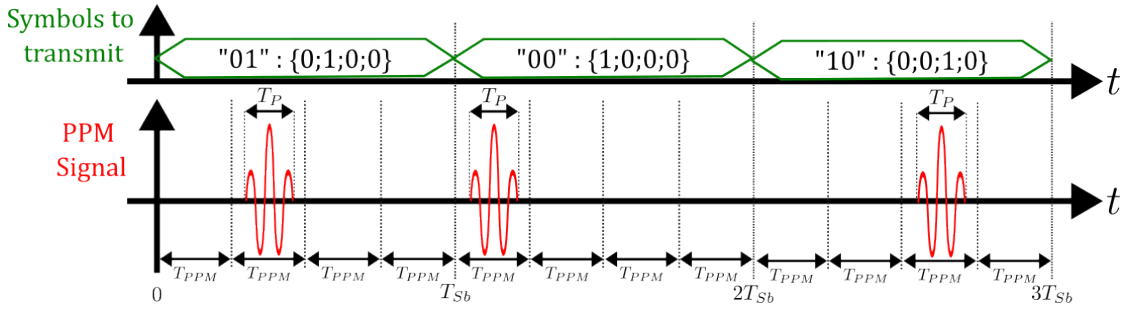


Figure 1.15.: PPM pulse modulation coding and waveform.

1.3.3. Phase-shift Keying Pulse Modulation (PSK)

From Table 1.4, the BPSK modulation is exploited by the physical layers HRP UWB of the IEEE standard IEEE 802.15.4 and UWB PHY of the IEEE standard 802.15.6. On the other hand, the Quadrature Phase-Shift Keying (QPSK) modulation is exploited only by the physical layer UWB of the IEEE standard 802.15.6. Among the PSK modulations, the BPSK modulation is the simplest one. Indeed, the BPSK modulation is a PSK pulse modulation in 2 levels, where each symbol transmitted corresponds to a single bit. Since a symbol is represented by a single pulse, this modulation consists of modifying the pulse polarity according to the symbol to transmit. For instance, Figure 1.16 shows a BPSK pulse modulation coding and waveform. The transmitted symbols can be either '0' or '1'. They are coded according to the pulse polarity during a time interval of T_{Sb}. The signal emitted by the UWB antenna is expressed in expression (1.6), where the alphabet D is given as follows:

$$D : \{d_k\} = \{-1, 1\} \tag{1.10}$$

To implement this pulse modulation, an IR-UWB transmitter must be able to switch the pulse polarity.

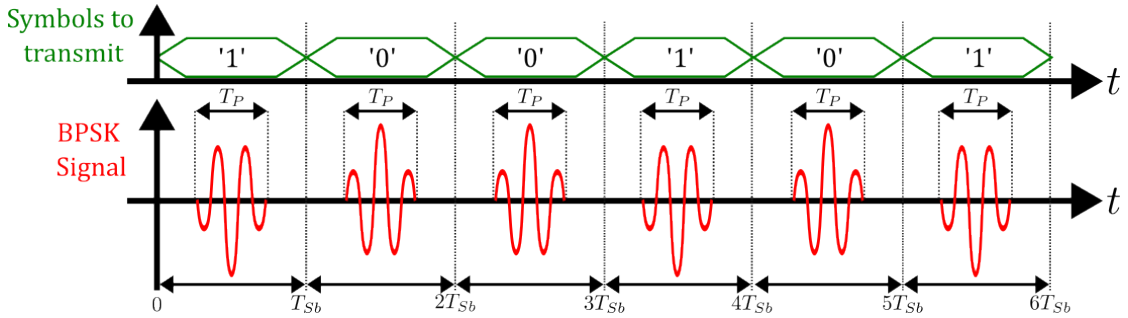


Figure 1.16.: BPSK pulse modulation coding and waveform.

1.4. Power Consumption

IR-UWB allows duty-cycle transceiver power at the bit scale and presents a power consumption proportional to the data rate [20]. In fact, the power consumption of an IR-UWB transmitter P_c can be expressed as a function of the PRF as follows:

$$P_c = P_{0Hz} + E_{ac} \cdot PRF \tag{1.11}$$

where E_{ac} is the energy drained per IR-UWB pulse and P_{0Hz} the static power of the IR-UWB transmitter [12, 13]. Static power corresponds to the DC power consumed when no pulse is generated. Therefore, for a low data rate transmission, a low power consumption can be achieved, which is interesting for low-power applications [14, 38].

1.5. Conclusion

This chapter presents an overview of UWB communications. It compares traditional narrowband and UWB communications. Narrowband uses a modulated carrier and has a power consumption independent of the data rate. On the other hand, UWB uses low-duty cycle short pulses, which enables a precise real-time location (5 cm). Besides, the IR-UWB signal has a power consumption proportional to the data rate and an emitted power spectrum density that is directly proportional to the squared modulus of the emitted pulse spectrum.

The spectral requirements imposed by FCC, ETSI, IEEE 802.15.4, and IEEE 802.15.6 standards have been presented. Table 1.5 displays a summary of the main parameters specified by regional regulations and IEEE standards for an IR-UWB signal synthesis. FCC imposes a minimum 10 dB bandwidth of 500 MHz. IEEE 802.15.4 standard radio-frequency mask delimits a maximum 10 dB bandwidth and 18 dB bandwidth. On the other hand, the radio-frequency mask of IEEE 802.15.4 delimits a maximum 20 dB bandwidth. The generated IR-UWB pulse must fit into these spectral masks. Controlling the IR-UWB pulse amplitude, duration, and, most importantly, envelope shape is important for respecting these spectral requirements. Therefore, a pulse envelope shaping is required. This can modify the pulse shape, which can improve the side-lobe rejection and pulse energy emission.

Table 1.5.: Summary of the main parameters specified by regional regulations and IEEE standards for IR-UWB signal synthesis

Parameter	Value or Interval (min. - max.)
Central frequency f_c (GHz)	3.1 - 10.6
Minimal pulse bandwidth BW_{-10dB} (MHz)	500 (FCC)
Maximal pulse bandwidth BW_{-10dB} (MHz)	650 - 2146.56
Maximal pulse bandwidth BW_{-18dB} (MHz)	798.72 - 2296.32
Minimal side-lode rejection (dB)	10 - 20 (FCC) 23.7 - 28.7 (ETSI)

The IR-UWB transmitter design should be multi-band and multi-standard to generate pulse addressing the IEEE 802.15.4 and 802.15.6 standardized channels in the FCC band (3.1-10.6

GHz). The IR-UWB transmitter should be able to tune the pulse central frequency, covering the FCC band. Besides, it should have pulse shaping capabilities to generate nanosecond short pulses that respect the radio-frequency masks imposed by IEEE standards and regulatory commissions (FCC,ETSI), in addition to the minimum 10 dB bandwidth of 500 MHz.

2. Pulses Envelope Modeling and Characterization

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2.1. Introduction

In the IR-UWB pulse generation scheme, a critical point is the pulse envelope shaping. Indeed, the IR-UWB pulse envelope has a major effect on the frequency response, side-lobes rejection, and energy of the pulse [13, 39].

As indicated in Chapter 1, the generated IR-UWB pulse main lobe and side-lobes must fit into spectral masks established by regional regulations (FCC or ETSI), and IEEE standards (802.15.4 and 802.15.6). Thus, to disturb the least as possible neighboring channels or other wireless systems, a minimum level of side-lobe rejection is fixed. For example, FCC imposes a

side-lobe rejection outside the 3.1-10.6 GHz band of 10 dB or 20 dB according to the targeted applications. In this case, it is not a major concern because the frequency response of the UWB antenna can help to filter the emitted signal (the antenna is not studied in this thesis work).

However, the FCC requires a minimal bandwidth of 500 MHz, and the IEEE 802.15.4 and IEEE 802.15.6 standards require a side-lobe rejection of 18 dB and 20 dB, respectively [8, 9]. For instance, the ETSI frequency mask imposes a side-lobe rejection of 28.7 dB below 6 GHz and 23.7 dB over 8.5 [7]. Envelope shaping can also help to respect these spectral requirements.

Several works reported in the literature have chosen to synthesize the Gaussian truncated envelope to achieve high side-lobe suppression [21, 40, 41]. The Gaussian truncated envelope corresponds to a Gaussian envelope with rectangular windowing since the ideal Gaussian function has an infinite width [12, 13, 41]. The greater the truncation level of the Gaussian envelope is, the greater the side-lode rejection loss is. Despite that, the Gaussian truncated envelope can achieve high side-lobe rejection [12, 13]. However, the generation of this envelope can not be easily done with conventional analog electronic circuits. Thus, linear piece-wise envelopes such as triangular or trapezoidal are detailed here in a first time and used in Chapter 4. But, in a second time, the approximation of any envelope in continuous time by an envelope in discrete time is proposed. Indeed, envelopes in discrete time can be more easily generated using digital electronic circuits, as proposed in Chapter 5, while equivalent side-lobe rejection levels can be obtained.

This chapter is divided into three parts. In a first time, the main envelope's characteristics are introduced. In a second time, the modeling and the characterization of continuous envelopes are detailed. Then, the modeling and characterization of sample and hold envelopes are studied. It is important to note that MATLAB software has been utilized in the envelopes study.

The first part of this chapter introduces the main envelope's characteristics, which serve as a basis for the next two parts. These characteristics are basically the envelope waveform and its Fourier Transform, in addition to the bandwidth, the side-lobe rejection, and the energy.

The second part of this chapter addresses the modeling and characterization of continuous envelopes. Five continuous shapes are studied: Rectangular, Symmetrical triangular, Asymmetrical triangular, Symmetrical trapezoidal, and Asymmetrical trapezoidal. Their performance in terms of side-lobe rejection and energy are compared.

Finally, the third part of this chapter addresses the modeling and characterization of sample and hold envelopes. They are a combination of shifted rectangular pulses [13], which are easier to synthesize than the continuous one from an electrical point of view [13, 41].

Initially, a uniform sampling of the studied continuous envelopes is presented. The performance of the sampled envelopes is analyzed in terms of side-lobe rejection. Indeed, the fewer samples there are, the less complex the sample and hold envelope synthesis is, but the higher the side-lobe rejection.

Finally, the optimization of an arbitrary sample and hold envelope is proposed to achieve a better side-lobe rejection. These parameters are the amplitude and width of each shifted rectangular pulse. This optimization takes into account the spectral requirements presented in Chapter 1.

2.2. Envelope general characteristics

A pulse $p(t)$ can be described with a modulated sine-wave as follows:

$$p(t) = x(t)\cos\left(2\pi f_c t - \varphi\right) \tag{2.1}$$

where $x(t)$ is the pulse envelope, f_c is the frequency at which the pulse power spectral density reaches its maximum value, and φ is the sine-wave phase. The pulse Fourier transform can be computed as:

$$P(f) = \frac{\exp(-j\varphi)}{2}\left[X(f+f_c) + X(f-f_c)\right] \tag{2.2}$$

where $X(f)$ is the envelope Fourier transform. Since the IR-UWB signal PSD is directly proportional to the Fourier transform magnitude of the emitted pulses [40], it is possible to conclude that the IR-UWB signal PSD magnitude is given by the Fourier transform magnitude of the envelope of the pulse [20]. Thereby, this highlights the importance of pulse shaping and so the pulse shaping should be done according to the targeted spectral mask.

If the envelope is a real and even function, the pulse spectrum presents a symmetry around the 0 Hz [42]. Considering this and a central frequency f_c greater than the half value of the emitted pulse bandwidth, the mono-lateral Fourier transform of the pulse can be expressed as [13]:

$$P^{+}(f) = \frac{1}{\sqrt{2}}\left[X(f-f_c)\right]\exp(-j\varphi) \tag{2.3}$$

The pulse bandwidth BW for a certain X_{dB} attenuation can be expressed as [13]:

$$X_{dB} = 10\log\left(\frac{\left|P(f=f_c)\right|^2}{\left|P(f=f_c+\frac{BW}{2})\right|^2}\right) \tag{2.4}$$

where $\left|P(f)\right|^2$ corresponds to the Energy Spectral Density (ESD) of the IR-UWB pulse. Alternatively, the relation between BW and X_{dB} can be expressed using the pulse envelope centered at $f = 0$, such that:

$$X_{dB} = 10\log\left(\frac{\left|X(f=0)\right|^2}{\left|X(f=\frac{BW}{2})\right|^2}\right) \tag{2.5}$$

where $\left|X(f)\right|^2$ corresponds to the ESD of the pulse envelope. Concerning the side-lobe rejection, it can be estimated with the following equation [13]:

$$X_{dB-Side-Lobe} = 10\log\left(\frac{\left|X(f=0)\right|^2}{\left|X(f=f_{Side-Lobe})\right|^2}\right) \tag{2.6}$$

where $f_{Side-Lobe}$ corresponds to the side-lobe frequency.

The energy E_p associated to a pulse $p(t)$ can be computed by calculating the pulse energy drained by the load Z_L to which the pulse is applied, such that [12]:

$$E_p = \frac{1}{Z_L}\int_{-\infty}^{\infty}\left|p(t)\right|^2 dt \tag{2.7}$$

Alternatively, from Parseval's relation, the expression (2.7) can be written as follows [42]:

$$E_p = \frac{1}{Z_L}\int_{-\infty}^{\infty} \left|P\left(f\right)\right|^2 df \tag{2.8}$$

Applying expression (2.1) on energy expression (2.7), the pulse energy E_p can be approximated as follows:

$$E_p = \frac{1}{2Z_L}\int_{-\infty}^{\infty} \left|x\left(t\right)\right|^2 dt \;\Leftrightarrow\; E_p = \frac{1}{2Z_L}\int_{-\infty}^{\infty} \left|X\left(f\right)\right|^2 df \tag{2.9}$$

2.3. Continuous Envelope

In this section, two study cases are presented: a general case (1) and a particular one targeting FCC regulations and IEEE 802.15.4 and 802.15.6 standards (2). Regarding the IEEE 802.15.4 standard, only the HRP UWB PHY is concerned in this chapter. Besides, there is a focus on the 499.2 MHz IEEE channels.

The general case introduces the mathematical modeling of typical continuous envelopes. On the other hand, the particular case submits the introduced envelopes to spectral constraints, which are the IEEE standards masks and the minimal 500 MHz bandwidth established by the FCC. The goal of these study cases is to analyze the envelope shapes' performance in terms of side-lobe rejection and energy to find the most suitable for the IR-UWB pulse synthesis.

2.3.1. Case Study 1: General case

The objective of this part is to study the potential of the envelope's shapes in terms of side-lobe rejection and energy. For convenience, the envelope width τ is constant and equals $\tau = 1$ s. In fact, from the time and frequency scaling Fourier Transform property, the side-lobe rejection can be determined for any width [42, 43].

2.3.1.1. Rectangular

The rectangular envelope is the simplest envelope to generate. It is based on a rectangular function, thereby written as follows:

$$x_R\left(t\right) = A \cdot \Pi\left(\frac{t}{\tau}\right) \tag{2.10}$$

where A and τ are the envelope amplitude and width, respectively [13]. Shifting to the frequency domain, the rectangular envelope Fourier transform can be computed as [44, 45]:

$$X_R\left(f\right) = A\tau \cdot \mathrm{sinc}\left(f\tau\right) \tag{2.11}$$

where:

$$\mathrm{sinc}\left(f\right) = \frac{\sin\left(\pi f\right)}{\pi f} \tag{2.12}$$

Applying expression (2.11) on equation (2.5), the relation between rectangular envelope bandwidth BW and X_{dB} attenuation can be expressed as follows:

$$10^{\frac{-X_{dB}}{10}} = \text{sinc}^2\left(\frac{BW \cdot \tau}{2}\right) \tag{2.13}$$

The mathematical manipulations to obtain this last expression are presented in the Appendix A.1. From equation (2.13), Table 2.1 shows the rectangular envelope bandwidth BW as a function of the X_{dB} attenuation , for τ = 1 s.

Table 2.1.: Rectangular envelope bandwidth as a function of attenuation (τ = 1 s).

XdB	$BW_{X_{dB}}$ (Hz)
3	0.88
10	1.47
18	5.05
20	5.36

Applying expression (2.11) on equation (2.6), and assuming τ = 1 s the side-lobe rejection for a rectangular envelope can be estimated as follows:

$$X_{dB-Side-Lobe} = -10\log\left[\text{sinc}^2\left(f_{Side-Lobe}\right)\right] \tag{2.14}$$

The side-lobe frequency is at f = 1.43 Hz as presented in Appendix A.1. Thus, from equation (2.14) and the calculated value of side-lobe frequency, the side-lobe rejection is estimated at 13.26 dB.

From energy expression (2.9), the pulse energy expression can be written as follows:

$$E_{p-R} = \frac{A^2\tau}{2Z_L} \tag{2.15}$$

For an impedance load of 50 Ω, and an amplitude A = 1 V, the pulse energy can be estimated at 10 mJ. Finally, Figure 2.1 presents a rectangular envelope waveform and spectrum. From this, it can be noticed that the side-lobes, located at 1.43 Hz, have a rejection of 13.26 dB, as calculated earlier. Despite the simplicity of the envelope, it presents a weak side-lobe rejection.

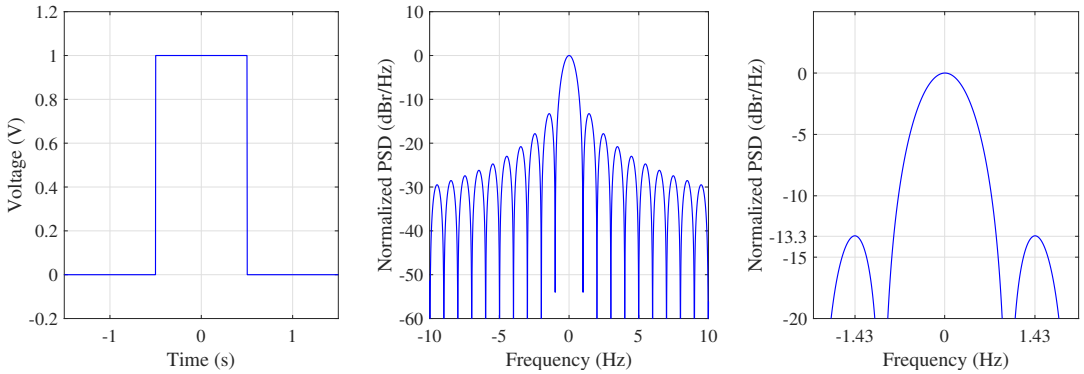
2.3.1.2. Symmetrical Triangular

The second addressed continuous envelope in this chapter is the symmetrical triangular envelope. It is more complex to synthesize than the rectangular envelope. The symmetrical triangular envelope can be expressed as follows [13]:

$$x_{ST}(t) = \begin{cases} A\left(1 - \frac{2|t|}{\tau}\right) & if \quad 0 < |t| < \frac{\tau}{2} \\ 0 & otherwise \end{cases} \tag{2.16}$$

where A is the pulse amplitude, and τ the pulse duration. Shifting to the frequency domain, the symmetrical triangular envelope Fourier transform can be computed as:

$$X_{ST}(f) = \frac{A\tau}{2}\text{sinc}^2\left(\frac{f\tau}{2}\right) \tag{2.17}$$



(a) Waveform (b) Spectrum (c) Spectrum (Zoomed)

Figure 2.1.: Rectangular envelope waveform and spectrum (τ = 1 s).

Applying expression (2.17) on equation (2.5), the relation between symmetrical triangular envelope bandwidth BW and X_{dB} attenuation can be written as follows:

$$10^{\frac{-X_{dB}}{10}} = \text{sinc}^4\left(\frac{BW \cdot \tau}{4}\right) \tag{2.18}$$

The mathematical manipulations to obtain this last expression are presented in the Appendix A.2. From equation (2.18), Table 2.2 shows the symmetrical triangular envelope bandwidth BW as a function of the X_{dB} attenuation for τ = 1 s. Comparing Tables 2.1 and 2.2, it can be noticed that for an attenuation greater or equal to 18 dB, the symmetrical triangular envelope spectrum is wider than the rectangular. On the other hand, for an attenuation smaller or equal to 10 dB, the symmetrical triangular envelope spectrum is narrower than the rectangular.

Table 2.2.: Symmetrical triangular envelope bandwidth as a function of attenuation (τ = 1 s).

X_{dB}	$BW_{X_{dB}}$ (Hz)
3	1.27
10	2.22
18	2.83
20	2.95

Applying expression (2.17) on equation (2.6), and assuming τ = 1 s, the side-lobe rejection for a symmetrical triangular envelope can be estimated as follows:

$$X_{dB-Side-Lobe} = -10\log\left(\text{sinc}^4\left(\frac{f_{Side-Lobe}}{2}\right)\right) \tag{2.19}$$

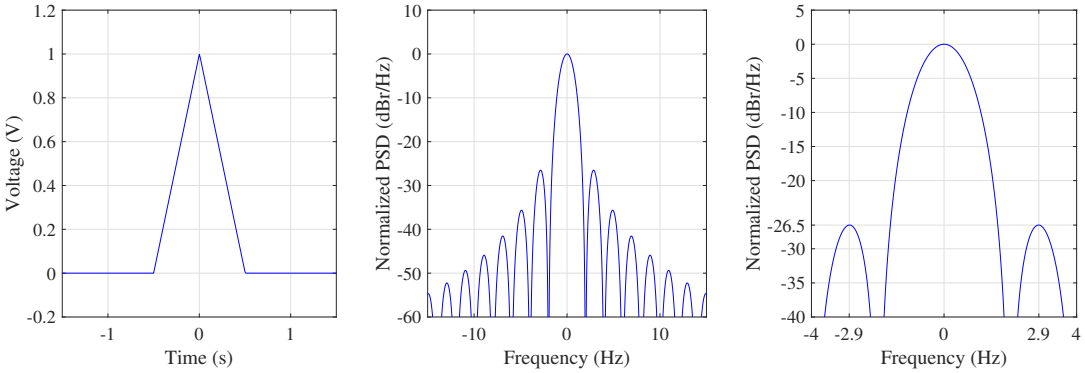
The side-lobe frequency is calculated at f = 2.86 Hz as demonstrated in Appendix A.2. Thereby, from expression (2.19) and the calculated value of side-lobe frequency, the side-lobe rejection is estimated at 26.52 dB.

From energy expression (2.9), its energy expression is given as follows:

$$E_{p-T} = \frac{A^2\tau}{6Z_L} \tag{2.20}$$

For an impedance load of 50 Ω, and an amplitude A = 1 s, the pulse energy can be estimated at 3.4 mJ. This value is 3 times lower than the pulse energy for a rectangular envelope.

Finally, Figure 2.2 presents a symmetrical triangular envelope waveform and spectrum. From this Figure, it can be observed that the side-lobes, located at 2.86 Hz, have a rejection of 26.52 dB, as calculated earlier. Therefore, between rectangular and symmetrical triangular envelopes, the last one presents a stronger side-lobe rejection but a weaker pulse emitted energy.



(a) Waveform (b) Spectrum (c) Spectrum (Zoomed)

Figure 2.2.: Symmetrical triangular envelope waveform and spectrum (τ = 1 s).

2.3.1.3. Asymmetrical Triangular

The third addressed continuous envelope in this chapter is the asymmetrical triangular. It is a more versatile envelope than the symmetrical triangular one. The asymmetrical triangular envelope can be described as follows:

$$x_{AT}(t) = \begin{cases} A\left(1+\frac{t}{\alpha\tau}\right) & if \quad -\alpha\tau < t \leq 0 \\ A\left(1-\frac{t}{\alpha_c\tau}\right) & if \quad 0 < t < \alpha_c\tau \\ 0 & otherwise \end{cases} \tag{2.21}$$

where A is the envelope amplitude, τ the envelope width, and α a parameter. The α parameter is defined as a symmetry factor, whose numerical value is within a closed interval between 0 and 1, such that:

$$0 \leq \alpha \leq 1 \tag{2.22}$$

Alternatively, the α_c parameter is defined as a complementary symmetry factor and expressed as follows:

$$\alpha_c = 1 - \alpha \tag{2.23}$$

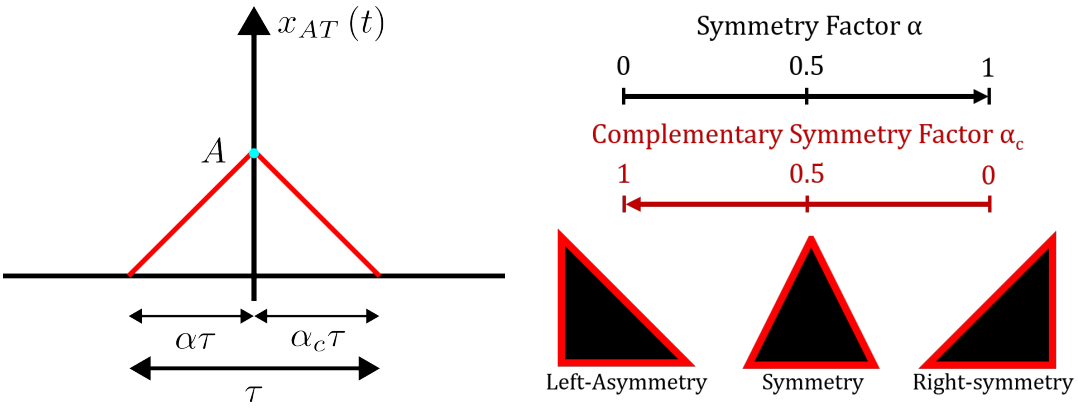
where:

$$0 \leq \alpha_c \leq 1 \tag{2.24}$$

Therefore, the relation between α and α_c is:

$$\alpha + \alpha_c = 1 \tag{2.25}$$

Figure 2.3 displays the asymmetrical triangular envelope, in addition to indicating the effect of the symmetry factor on the continuous envelope shape. From Figure 2.3, it can be noticed that the symmetry factor α influences the rise time of the triangular envelope, whereas the complementary symmetry factor α influences the fall time. From Figure 2.3, it can be observed that an α higher than 0.5 implies a rise time faster than the fall time and conversely. Obviously, the symmetrical triangular envelope is obtained when α is equal to 0.5. Moreover, an envelope with a saw-tooth shape is obtained when α is equal to 0 or 1.



(a) Waveform.

(b) Symmetry factor α influence.

Figure 2.3.: Asymmetrical triangular envelope.

Shifting to the frequency domain, the asymmetrical triangular envelope Fourier transform can be computed as :

$$\begin{aligned} X_{AT}(f) = \frac{A\tau}{2}\left[\alpha \text{sinc}^2(\alpha f\tau) + \alpha_c \text{sinc}^2(\alpha_c f\tau)\right] \\ + j\frac{A}{2\pi f}\left[\text{sinc}(2\alpha_c f\tau) - \text{sinc}(2\alpha f\tau)\right] \end{aligned} \tag{2.26}$$

where a mathematical demonstration is given in Appendix A.3. Comparing the expression of Fourier Transform of the asymmetrical triangular envelope (2.26) with the symmetrical one (2.17), it can be observed that the last has a null imaginary part. In the other words :

$$\alpha = 0.5 \Rightarrow \text{Im}\{X_{AT}(f)\} = 0 \tag{2.27}$$

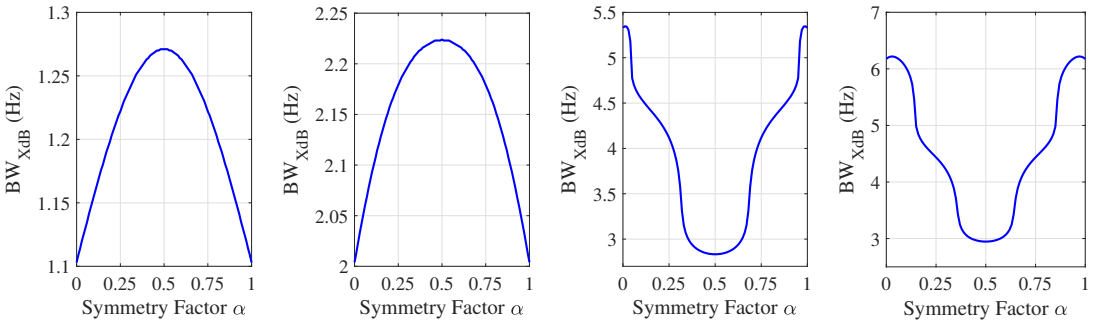
Indeed, from continuous Fourier Transform theory, a non-periodic real and even signal has a Fourier Transform real and even [42].

Figure 2.4 shows the asymmetrical triangular envelope bandwidth BW as a function of symmetry factor α, for several values of X_{dB} attenuation. The mathematical expressions

for the asymmetrical triangular envelope bandwidth BW are given in Appendix A.3. From Figure 2.4, it can be noticed that the more asymmetrical the triangular envelope becomes, the narrower the bandwidth is for low attenuations (X = 3 dB and X = 10 dB), but the wider the bandwidth is for high attenuation (X = 18 dB and X = 20 dB). Moreover, it can be noted that the curves of Figure 2.4 are symmetric around $\alpha = 0.5$. This can be explained by the time reversal property of Fourier transform [42, 44].

Figure 2.5 shows both level and frequency of the strongest side-lobe of the asymmetrical triangular envelope as a function of symmetry factor α. As observed in Figure 2.4, the curves of Figure 2.5 are symmetric around $\alpha = 0.5$. From Figure 2.5, it can be observed that the symmetric triangular envelope ($\alpha = 0.5$) has the weakest side-lobe rejection and the lowest frequency of side-lobe rejection. Meanwhile, a more asymmetrical triangular envelope results in a stronger side-lobe rejection and a side-lobe further away from the main lobe. In particular, when α approaches 0, the side-lobe frequency approaches infinity (vertical asymptote). Consequently, it can be stated that the side-lobe rejection approaches infinity (vertical asymptote). A mathematical demonstration is given in Appendix A.3.1.

Finally, the highest side-lobe rejection (83.9 dB) and frequency (1392 Hz) are achieved for a saw-tooth envelope (either $\alpha \approx 0$ or $\alpha \approx 1$).



(a) X = 3 dB (b) X = 10 dB (c) X = 18 dB (d) X = 20 dB

Figure 2.4.: Asymmetrical triangular envelope bandwidth BW as a function of symmetry factor α.

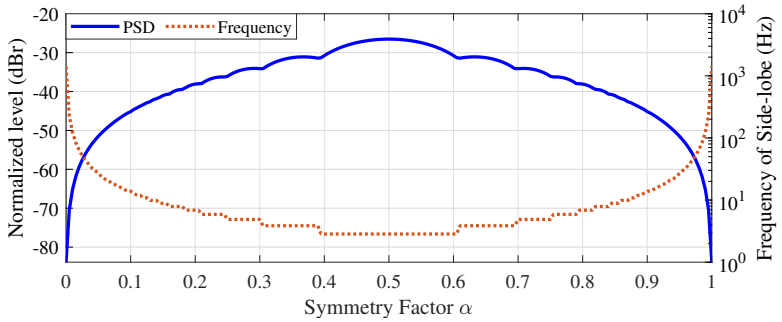
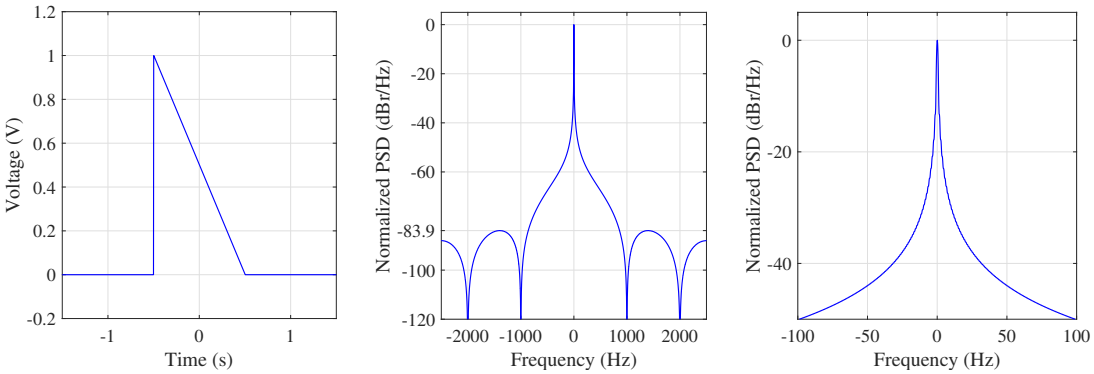


Figure 2.5.: Level and frequency of the strongest side-lobe of the asymmetrical triangular envelope as a function of symmetry factor α.

From the energy expression (2.9), the pulse energy expression is the same than the one given in the expression (2.20). Indeed, since the symmetry factor does not impact the envelope surface, the pulse energy is independent of the symmetry factor.

Finally, Figure 2.6 presents an asymmetrical triangular envelope waveform and spectrum for $\alpha \approx 0$. From this Figure, it can be observed that the side-lobes, located at 1397 Hz, have a rejection of 83.9 dB. Between triangular envelopes, the one with the shape of a saw-tooth presents a stronger side-lobe rejection thanks to the asymmetry. The pulse emitted energy is constant at 3.4 mJ. Consequently, it is feasible to achieve stronger side-lobe rejection for the same pulse transmitted energy by tuning the symmetry factor.



(a) Waveform (b) Spectrum (c) Spectrum (Zoomed)

Figure 2.6.: Asymmetrical triangular envelope waveform and spectrum ($\alpha \approx 0$, $\tau = 1$ s)

2.3.1.4. Symmetrical Trapezoidal

The fourth addressed continuous envelope in this chapter is the symmetrical trapezoidal. This is also more versatile than the symmetrical triangular. The symmetrical trapezoidal envelope can be written as follows [39, 46, 47]:

$$x_{SZ}(t) = \begin{cases} A & if \quad 0 \leq |t| < \frac{\beta\tau}{2} \\ A\left(1 - \frac{2|t|-\beta\tau}{\beta_c\tau}\right) & if \quad \frac{\beta\tau}{2} \leq |t| < \frac{\tau}{2} \\ 0 & otherwise \end{cases} \tag{2.28}$$

where A is the envelope amplitude, and τ is the envelope width. The β parameter is defined here as a surface factor whose numerical value is within a closed interval between 0 and 1, such that:

$$0 \leq \beta \leq 1 \tag{2.29}$$

Alternatively, the β_c parameter is defined as a complementary surface factor and expressed as follows:

$$\beta_c = 1 - \beta \tag{2.30}$$

where :

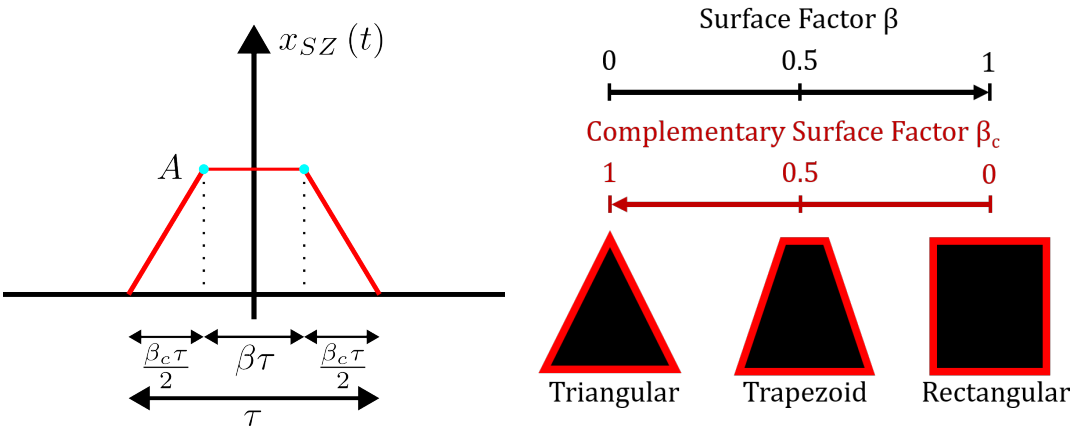
$$0 \leq \beta_c \leq 1 \tag{2.31}$$

Accordingly, from the equation (2.30), the relation between β and β_c parameters can be explained in the following equation:

$$\beta + \beta_c = 1 \tag{2.32}$$

Figure 2.7 displays the symmetrical trapezoidal envelope, in addition to pointing out the effect of the surface factor on the continuous envelope shape. From Figure 2.7, the surface factor establishes the time interval $\beta\tau$, which the envelope is at its maximum value (amplitude A). The complementary surface factor defines the time interval $\beta_c\tau$ corresponding to the sum of rising and falling time.

From Figure 2.7, it can be observed that a higher β increases time interval $\beta\tau$ until the trapezoid becomes a rectangle ($\beta = 1$). Conversely, a lower β reduces the time interval $\beta\tau$ until the trapezoid turns into a triangle ($\beta = 0$). Therefore, the symmetrical trapezoidal envelope can be considered as an extension version of symmetrical triangular and rectangular envelopes.



(a) Waveform

(b) Surface factor β influence.

Figure 2.7.: Symmetrical trapezoidal envelope.

Shifting to the frequency domain, the symmetrical trapezoidal envelope Fourier transform can be computed as :

$$X_{SZ}(f) = \frac{A\tau(1+\beta)}{2}\text{sinc}\left[\frac{f\tau(1-\beta)}{2}\right]\text{sinc}\left[\frac{f\tau(1+\beta)}{2}\right] \tag{2.33}$$

where a mathematical demonstration is given in Appendix A.4. Applying expression (2.33) on equation (2.5), the relation between symmetrical triangular envelope bandwidth BW and X_{dB} attenuation can be expressed as follows:

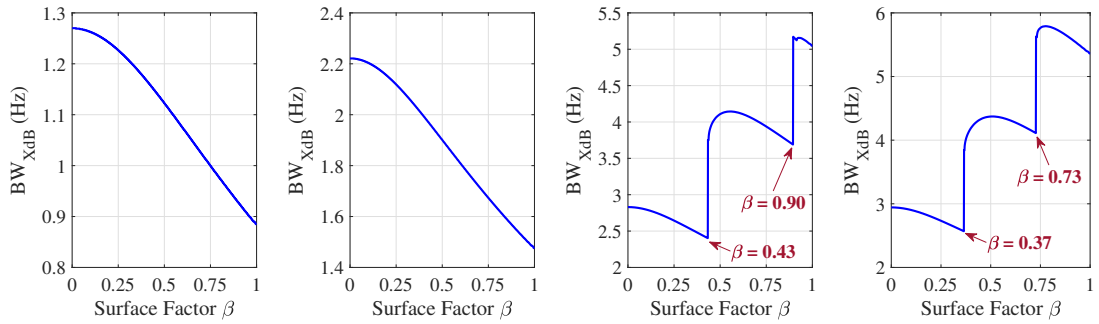
$$10^{\frac{-X_{dB}}{10}} = \text{sinc}\left[\frac{BW(1-\beta)}{4}\right]^2 \cdot \text{sinc}\left[\frac{BW(1+\beta)}{4}\right]^2 \tag{2.34}$$

From expression (2.34), Figure 2.8 shows the symmetrical trapezoidal envelope bandwidth BW as a function of surface factor β, for several values of X_{dB} attenuation. The mathematical expressions for the symmetrical trapezoidal envelope bandwidth BW are given in Appendix A.4.

From Figure 2.8, it can be seen that the more rectangular the symmetric trapezoidal envelope becomes, the spectrum is narrower for low attenuation (X_{dB} = 3 and X_{dB} = 10). The bandwidth for both X = 18 dB and X = 20 dB presents a particular behavior. In fact, the curves of Figures 2.8c and 2.8d have two steep rises. The first one occurs for a β = 0.43 and β = 0.37 for $BW_{X=18dB}$ and $BW_{X=20dB}$ respectively. The second one occurs for a β = 0.73 and β = 0.90 for $BW_{X=18dB}$ and $BW_{X=20dB}$, respectively. Each steep rise corresponds to the inclusion of an adjacent side-lobe into the envelope bandwidth. A graphical demonstration is given in appendix B.

Figure 2.9 displays both level and frequency of the strongest side-lobe of the symmetrical trapezoidal envelope as a function of surface factor β. From figure 2.9, it can be noticed that the optimal side-lobe rejection of 31.88 dB is achieved for a β = 0.164. Thus, a symmetrical trapezoidal envelope can reach a stronger side-lobe rejection than a symmetrical triangular envelope (26.52 dB@β = 0) and than a rectangular envelope (13.26 dB@β = 1). However, an asymmetrical triangular envelope can reach higher side-lobes rejection.

Regarding the side-lobe frequency, from Figure 2.9, a particular behavior can be observed. For a surface factor greater than 0.164, the frequency decreases when β rises. Otherwise, if the surface factor is lower than 0.164, the frequency remains approximately at 2.86 Hz. Regarding this, a graphical demonstration is given in appendix B.



(a) X = 3 dB (b) X = 10 dB (c) X = 18 dB (d) X = 20 dB

Figure 2.8.: Symmetrical trapezoidal envelope bandwidth BW as a function of surface factor β.

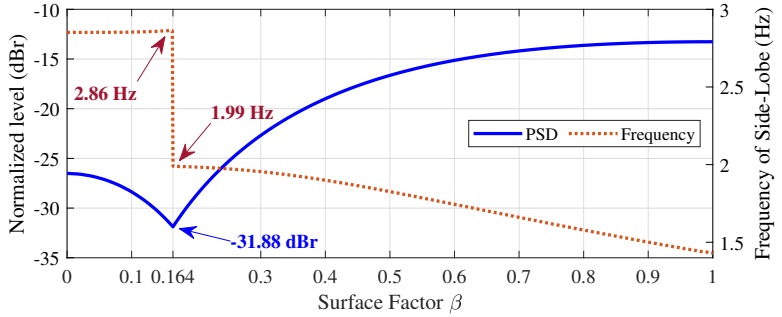


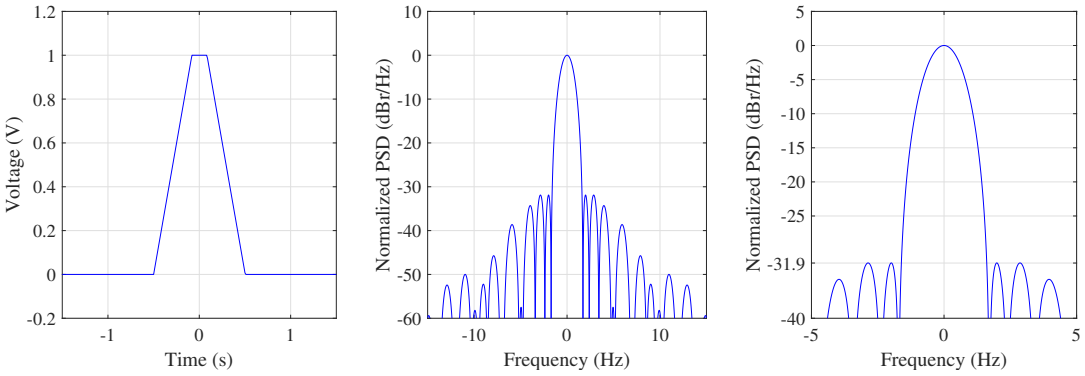
Figure 2.9.: Level and frequency of the strongest side-lobe of the symmetrical trapezoidal envelope as a function of surface factor β.

From expression (2.9), the associated pulse energy expression is given as follows:

$$E_{p-Z} = \frac{A^2\tau}{6Z_L}\left(2\beta+1\right) \tag{2.35}$$

which is linearly dependent of the surface factor. Indeed, an envelope with a bigger surface presents higher energy. If $\beta = 0$, the energy expression (2.35) is the same as triangular envelope pulse energy (2.20). Meanwhile, if $\beta = 1$, the energy expression (2.35) is the same as the rectangular envelope pulse energy expression (2.15).

Finally, Figure 2.10 presents a symmetrical trapezoidal envelope waveform and spectrum for $\beta = 0.164$. From this Figure, it can be noted that the side-lobes, located at 1.99 Hz, present a rejection of 31.88 dB. The envelope presented in Figure 2.10 has a shape close to a triangle. The pulse emitted energy is at 4.4 mJ, for an impedance load of 50 Ω and an amplitude $A = 1$ V. Therefore, tuning the surface factor enables a higher side-lobe rejection, and with a higher pulse energy.



(a) Waveform (b) Spectrum (c) Spectrum (Zoomed)

Figure 2.10.: Symmetrical trapezoidal envelope waveform and spectrum ($\beta = 0.164$, $\tau = 1$ s)

2.3.1.5. Asymmetrical Trapezoidal

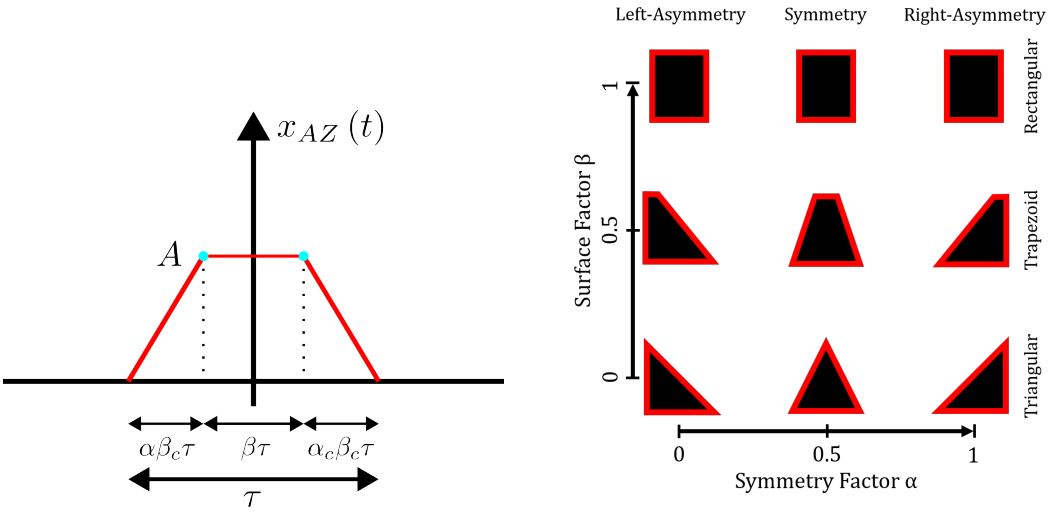
The fifth and last addressed continuous envelope in this chapter is the asymmetrical trapezoidal. Among the addressed continuous envelopes, it is the most versatile. The asymmetrical envelope can be described as follows:

$$x_{AZ}(t) = \begin{cases} A\left(1+\frac{2t+\beta\tau}{2\alpha\beta_c\tau}\right) & if \quad -\left(\alpha\beta_c\tau+\frac{\beta\tau}{2}\right) \le t < -\frac{\beta\tau}{2} \\ A & if \quad -\frac{\beta\tau}{2} \le t < \frac{\beta\tau}{2} \\ A\left(1-\frac{2t-\beta\tau}{2\alpha_c\beta_c\tau}\right) & if \quad \frac{\beta\tau}{2} \le t < \left(\alpha_c\beta_c\tau+\frac{\beta\tau}{2}\right) \\ 0 & otherwise \end{cases} \tag{2.36}$$

where A is the envelope amplitude, and τ is the envelope width. α and α_c are symmetry and complementary symmetry factors, respectively. β and β_c are surface and complementary surface factors, respectively. The expression (2.36) is an extension of the symmetrical trapezoidal

envelope expression (2.28), where the asymmetry is considered.

Figure 2.11 displays the asymmetrical trapezoidal envelope. The envelope of 2.11a encompasses all the 4 addressed continuous envelopes in earlier this chapter. This can be seen in Figure 2.11b, which shows the continuous envelope shape according to the symmetry and surface factors.



(a) Waveform

(b) Symmetry α and surface β factors influence.

Figure 2.11.: Asymmetrical trapezoidal envelope.

Shifting to the frequency domain, the symmetrical trapezoidal envelope Fourier transform can be computed as :

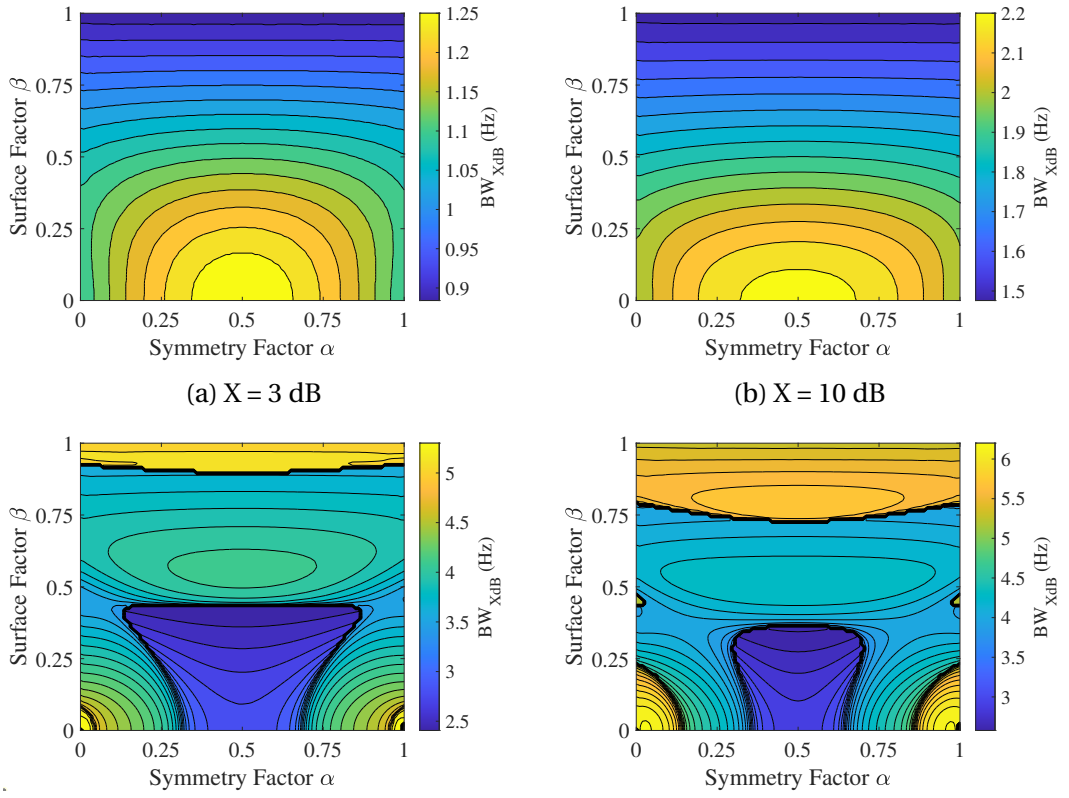
$$\begin{aligned}\mathrm{Re}\left(X_{AZ}(f)\right) = &\frac{A\tau\left(\alpha+\beta-\alpha\beta\right)}{2}\,\mathrm{sinc}\left(\alpha\beta_c f\tau\right)\mathrm{sinc}\left(f\tau\left(\alpha+\beta-\alpha\beta\right)\right)\\ &+\frac{A\tau\left(\alpha_c+\beta-\alpha_c\beta\right)}{2}\,\mathrm{sinc}\left(\alpha_c\beta_c f\tau\right)\mathrm{sinc}\left(f\tau\left(\alpha_c+\beta-\alpha_c\beta\right)\right)\end{aligned} \tag{2.37}$$

$$\begin{aligned}\mathrm{Im}\left(X_{AZ}(f)\right) = &-\frac{A}{2\pi f}\,\mathrm{sinc}\left(\alpha\beta_c f\tau\right)\cos\left(\pi f\tau\left(\alpha+\beta-\alpha\beta\right)\right)\\ &+\frac{A}{2\pi f}\,\mathrm{sinc}\left(\alpha_c\beta_c f\tau\right)\cos\left(\pi f\tau\left(\alpha_c+\beta-\alpha_c\beta\right)\right)\end{aligned} \tag{2.38}$$

where a mathematical demonstration is given in Appendix A.5. As observed from the triangular envelope, the asymmetry gave rise to an imaginary part of the envelope Fourier Transform. The expression (2.38) has null value when $\alpha = 0.5$, like the expression (2.27)

Figure 2.12 shows the asymmetrical trapezoidal envelope bandwidth BW as a function of symmetry and surface factors, for several values of X_{dB} attenuation. The mathematical expressions for the asymmetrical trapezoidal envelope bandwidth BW are given in Appendix A.5. From Figure 2.12, it can be observed the more symmetrical and triangular the envelope becomes, the spectrum tends to be wider for lower attenuation (X = 3 dB and X = 10 dB). In other words, the more symmetrical and triangular the envelope becomes, the main lobe is broader. Otherwise, the spectrum is narrower when raising the asymmetry, and mostly

when raising the surface factor. Meanwhile, for higher attenuation (X = 18 and X = 20 dB), the spectrum is narrower when the envelope becomes more symmetrical and triangular (α = 0.5 and β = 0). For a surface factor lower than 0.4, the asymmetry implies a larger bandwidth. Moreover, in Figure 2.12c ellipses can be observed. This can be explained by the two steep rises that were observed in Figure 2.8c.



(a) X = 3 dB

(b) X = 10 dB

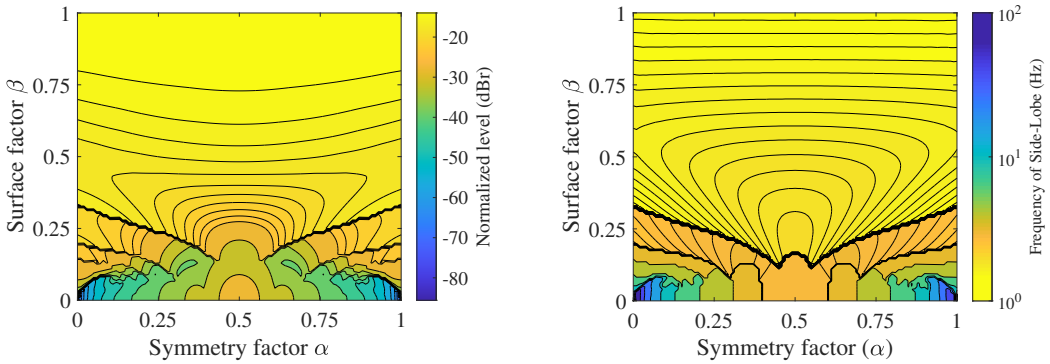
(c) X = 18 dB

(d) X = 20 dB

Figure 2.12.: Asymmetrical trapezoidal envelope bandwidth BW as a function of symmetry α and surface β factors.

Figure 2.13 shows the level and frequency of the strongest side-lobe of the asymmetrical trapezoidal envelope as a function of symmetry and surface factors. From figure 2.13a, it can be seen that the side-lobes rejection is higher when the envelope is more asymmetrical and triangular. Inversely, the side-lobes rejection is weaker when the envelope is more symmetrical, and mostly when it is more rectangular. Hence, a saw-tooth envelope (α = 0, β = 0, or α = 1, β = 0) presents the greatest rejection at 83.89 dB (Fig. 2.6), whereas a rectangular envelope (β = 0) presents the weakest rejection at 13.26 dB (Fig. 2.1). From figures 2.13a and 2.13b, it can perceived that the regions with higher side-lobe rejection correspond to the areas with higher side-lobe frequency. A side-lobe further away from the main lobe tends to have a lower level.

For the asymmetrical trapezoidal envelope, from expression (2.9), the pulse energy expression is given in the expression (2.35). As observed with the triangular envelope, the pulse energy is independent of the symmetry factor since this does not affect the envelope's surface.



(a) Level (b) Frequency

Figure 2.13.: Level and frequency of the strongest side-lobe of the asymmetrical trapezoidal envelope as a function of symmetry α and surface β factors.

2.3.1.6. Summary

Finally, Table 2.3 summarizes the performance of the addressed continuous envelopes. From this Table, the envelope shape is controlled by tuning two parameters: the symmetry factor α and the surface factor β. These strongly influence the side-lobe rejection and the envelope bandwidth. Besides, these parameters can change the side-lobe frequency, especially the symmetry factor. Regarding the pulse energy, it increases linearly with the envelope width and the surface factor. Since the symmetry factor only affects the envelope shape, it has no impact on the pulse energy.

Table 2.3.: Continuous envelopes summary

Continuous Envelope	Rectangular	Symmetrical Triangular	Symmetrical Trapezoidal	Approximated Saw-tooth
Symmetry Factor α	0 to 1	0.5	0.5	$\approx$ 0 or 1
Surface Factor β	1	0	0.164	0
Side-Lobe Rejection (dB)	13.26	26.51	31.88	83.89
Side-Lobe Frequency (Hz)	1.43	2.85	1.98	1397
BW_{-3dB} (Hz)	0.88	1.27	1.25	1.2
BW_{-10dB} (Hz)	1.47	2.20	2.17	2.0
BW_{-18dB} (Hz)	5.04	2.83	2.74	5.3
BW_{-20dB} (Hz)	5.36	2.94	2.87	6.2
Energy (mJ) @Z_L = 50 Ω	10	3.4	4.4	3.4

From Table 2.3, the approximated saw-tooth envelope has the greatest side-lobe rejection of 85.6 dB, but the lowest energy of 3.4 mJ, considering an impedance load of 50 Ω and an amplitude A = 1 V. For a constant envelope width, a higher energy can be achieved by increasing the surface factor. However, this increases side-lobe.

Therefore, the asymmetry is interesting because it increases the side-lobe rejection. Besides, the asymmetrical trapezoidal envelope presents better potential for dealing with spectral

constraints because of its superior flexibility.

2.3.2. Case Study 2: Considering spectral requirements imposed by FCC regulations and IEEE standards

The second case study approaches a particular case. The aim is to study the feasibility of the introduced continuous envelopes in compliance with spectral constraints imposed by the FCC regulations and IEEE 802.15.4 and 802.15.6 standards. For this particular case, the envelope is in the order of a few nanoseconds, which means the envelope bandwidth will be in the order of GHz. It is worth pointing out that from time and frequency scaling Fourier Transform property, the side-lobe rejection is the same for any envelope width τ. However, the envelope width is critical to satisfy the introduced spectral requirements.

2.3.2.1. Rectangular

First of all, it is necessary to calculate the envelope width τ taking into account the channel bandwidth of the IEEE 802.15.4 and IEEE 802.15.6 standards. From the equation (2.13), for a fixed level of attenuation XdB, it is possible to write the following equation:

$$\frac{BW_{-XdB} \cdot \tau}{2} = c_{R_{-XdB}} \tag{2.39}$$

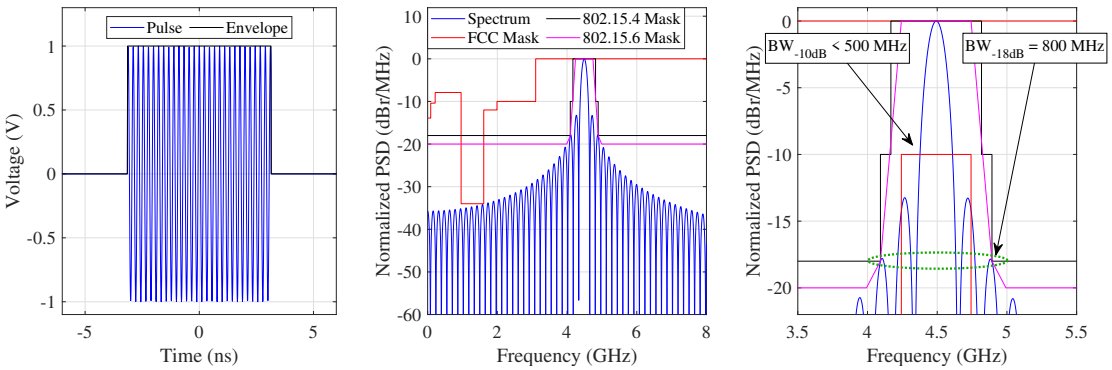
where $c_{R_{-XdB}}$ is the coefficient for a particular level of attenuation. From Table 2.1 of case study 1, it is possible to determine a value of this coefficient. Hence, the coefficient $c_{R_{-XdB}}$ values for the attenuation levels of 3 dB, 10 dB, 18 dB, and 20 dB are 0.44, 0.735, 2.52, and 2.68, respectively. From equation (2.39), the rectangular envelope's minimal width τ is 6.3 ns to address the narrowest channels of IEEE 802.15.4 standard (BW = 499.2 MHz).

Figure 2.14 presents an IR-UWB pulse waveform and spectrum with a rectangular envelope and a duration of 6.3 ns. This pulse addresses channel 3 of IEEE 802.15.4 and channel 2 of IEEE 802.15.6. From this Figure, the spectrum of pulse with a duration of 6.30 ns fits into IEEE spectral masks. However, the rectangular pulse of Figure 2.14 does not satisfy the minimum 10 dB bandwidth of 500 MHz imposed by FCC. The rectangular pulse is not short enough. To comply with the FCC minimum bandwidth, the rectangular pulse must be shorter. But in this case, the side-lobes having a rejection of 13.3 dB will move to adjacent channels. Therefore, the rectangular envelope is not able to comply simultaneously with the spectral requirements imposed by both FCC regulations and IEEE standards.

Concerning the pulse energy, considering an impedance load of 50 Ω and an amplitude A = 1 V, the pulse of Figure 2.14 has 23.04 pJ.

2.3.2.2. Symmetrical Triangular

As for the rectangular envelope, it is first necessary to calculate the symmetrical triangular envelope width taking into account the channel bandwidth of the addressed IEEE standards. From equation (2.18), for a fixed level of attenuation XdB, the following equation can be written:



(a) Waveform (b) Spectrum (c) Spectrum (Zoomed)

Figure 2.14.: IR-UWB pulse with rectangular envelope compliant with channel 3 of IEEE 802.15.4 and channel 2 of IEEE 802.15.6 (BW = 499.2 MHz and τ = 6.30 ns)

$$\frac{BW_{-XdB} \cdot \tau}{2} = c_{ST_{-XdB}} \tag{2.40}$$

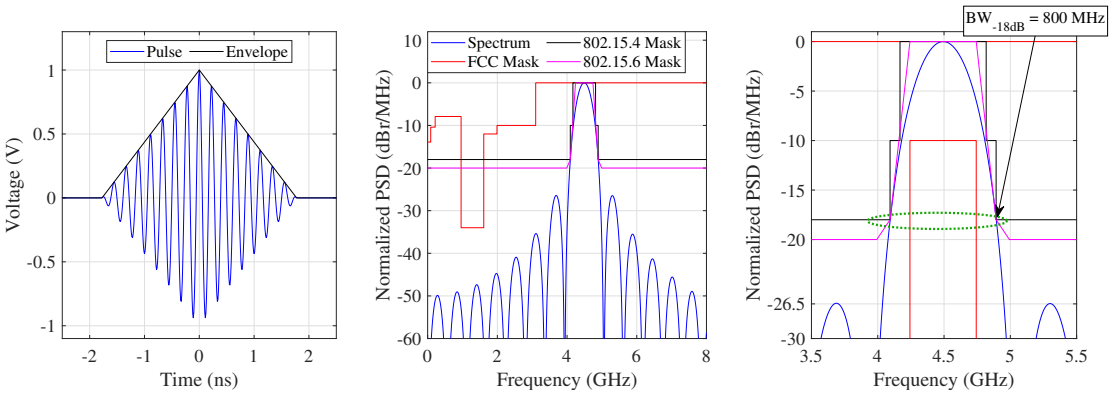
where $c_{ST_{-XdB}}$ is the coefficient for a particular level of attenuation, but valid for symmetrical triangular envelopes. From Table 2.2 of case study 1, it is possible to determine a value of this coefficient. Thereby, the coefficient $c_{R_{-XdB}}$ values for the attenuation levels of 3 dB, 10 dB, 18 dB, and 20 dB are 0.635, 1.11, 1.415, and 1.475, respectively. From equation (2.40), the symmetrical triangular envelope's minimal width is 3.55 ns to address the narrowest channels of IEEE 802.15.4 standard. A shorter pulse can address the 499.2 MHz IEEE channel, but it will present a lower energy and a narrower bandwidth.

Figure 2.15 shows an IR-UWB pulse waveform and spectrum with a symmetrical triangular envelope and a duration of 3.55 ns. This pulse addresses channel 3 of IEEE 802.15.4 and channel 2 of IEEE 802.15.6. From this Figure, it can be observed that the spectrum of this triangular pulse fits into IEEE spectral masks. Compared to the rectangular pulse, the symmetrical triangular pulse can achieve the required side-lobes rejection level (26.5 dB versus 18 or 20 dB required) while having a 10 dB bandwidth greater than 500 MHz.

Concerning the pulse energy, considering an impedance load of 50 Ω and an amplitude A = 1 V, the triangular pulse of Figure 2.15 has 11.84 pJ. Compared with the rectangular pulse of Figure 2.14, the displayed triangular pulse has an energy emitted approximately equivalent to half of the rectangular pulse (23.04 pJ). Thus, a symmetrical triangular envelope allows FCC and IEEE requirements to be respected simultaneously, in addition to achieving a lower pulse energy emission.

2.3.2.3. Asymmetrical Triangular

Compared to the symmetrical triangular envelope, the asymmetrical triangular envelope (Fig. 2.3a) has an additional degree of freedom, which is the symmetry factor α. As observed in study case 1, from Figure 2.5, the asymmetry can improve the side-lobe rejection, reaching

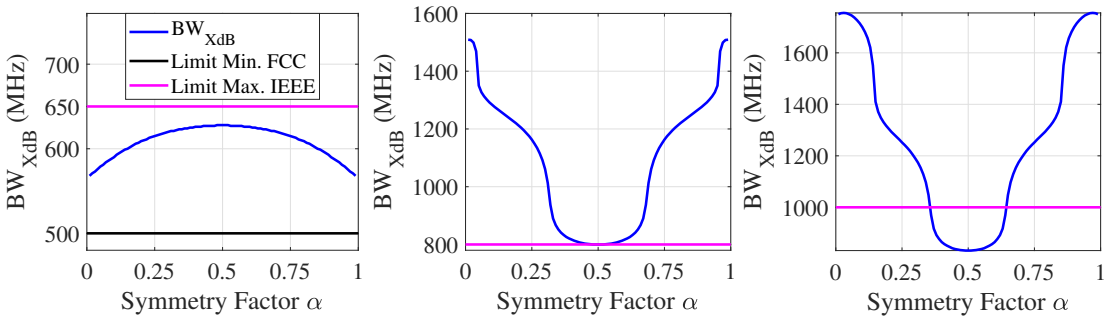


(a) Waveform (b) Spectrum (c) Spectrum (Zoomed)

Figure 2.15.: IR-UWB pulse with symmetrical triangular envelope compliant with channel 3 of IEEE 802.15.4 and channel 2 of IEEE 802.15.6 (BW = 499.2 MHz and τ = 3.55 ns)

83.9 dB for a saw-tooth envelope (2.6).

Figure 2.16 shows the asymmetrical triangular envelope bandwidth BW as a function of symmetry factor for several values of X_{dB} attenuation. In this Figure, the envelope width τ is at 3.55 ns, which is the minimal width of the symmetrical envelope. Figure 2.17 shows the available level of the strongest side-lobe of the asymmetrical triangular envelope as a function of symmetry factor α.



(a) X = 10 dB (b) X = 18 dB (c) X = 20 dB

Figure 2.16.: Asymmetrical triangular envelope bandwidth BW as a function of symmetry factor α compliant with IEEE 802.15.6 standard (BW = 499.2 MHz and τ = 3.55 ns)

From Figure 2.16a, it can be noticed that for all values of symmetry factor, the triangular envelope satisfies the minimum 10 dB bandwidth of 500 MHz required by FCC. However, from Figure 2.16b, it can be perceived that there is a small range of α (0.48 to 0.52) that allows the triangular envelope respect the IEEE spectral masks. From this range of α and Figure 2.17, the side-lobe lobe optimal rejection is 26.66 dB. The optimal rejection is at the borders of the symmetrical factor available range. The reason for this small range is the low envelope width.

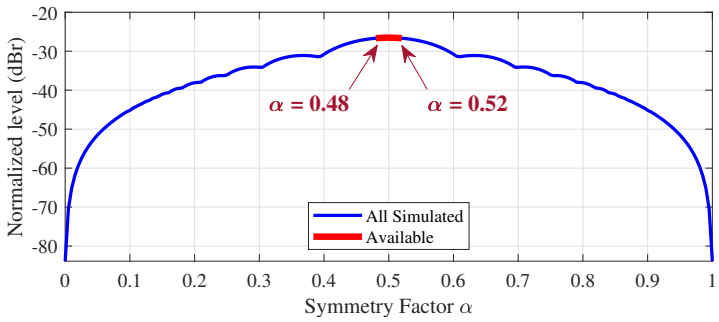


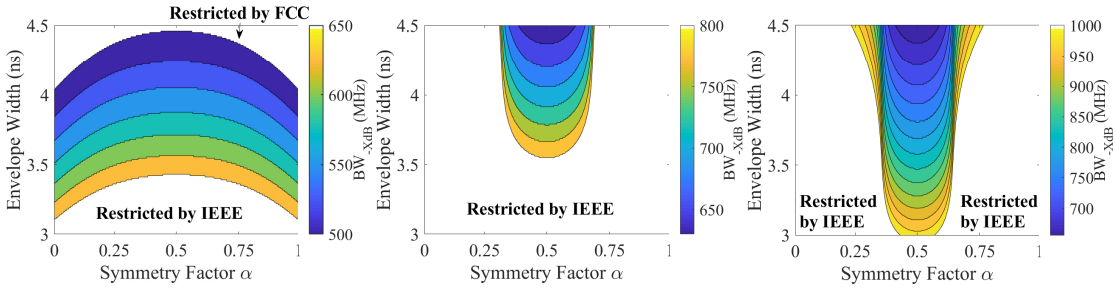
Figure 2.17.: Level of the strongest side-lobe of the asymmetrical triangular envelope as a function of symmetry factor α compliant with IEEE 802.15.6 standard (BW = 499.2 MHz and τ = 3.55 ns).

A solution for this consists of increasing the envelope width, but not much. Otherwise, the minimum 10 dB bandwidth of 500 MHz required by the FCC will not be respected anymore. Accordingly, there is a limited set of values of envelope width and symmetry factor that satisfies the spectral requirements. The set that enables the greatest side-lobe rejection is sought. This can be done by searching the envelope width that enables the largest range of symmetry factors. It is worth pointing out that the envelope width has no impact on the level of the envelope but has on the available α.

Figures 2.18 and 2.19 show the asymmetrical triangular envelope bandwidth BW and level as a function of symmetry factor α and envelope width, respectively. The envelope width is swept from 3 ns to 4.5 ns. For Figure 2.18, the white region corresponds to the region in which the spectral requirements imposed by FCC and IEEE are not satisfied. On the other hand, Figure 2.19a does not consider any spectral requirements. Otherwise, Figures 2.19b, 2.19c, and 2.19d take into account, respectively, only the FCC constraints, only the IEEE constraints, and both FCC and IEEE constraints. Therefore, the white region will be defined here as the forbidden zone and the colored region as the exploitable zone.

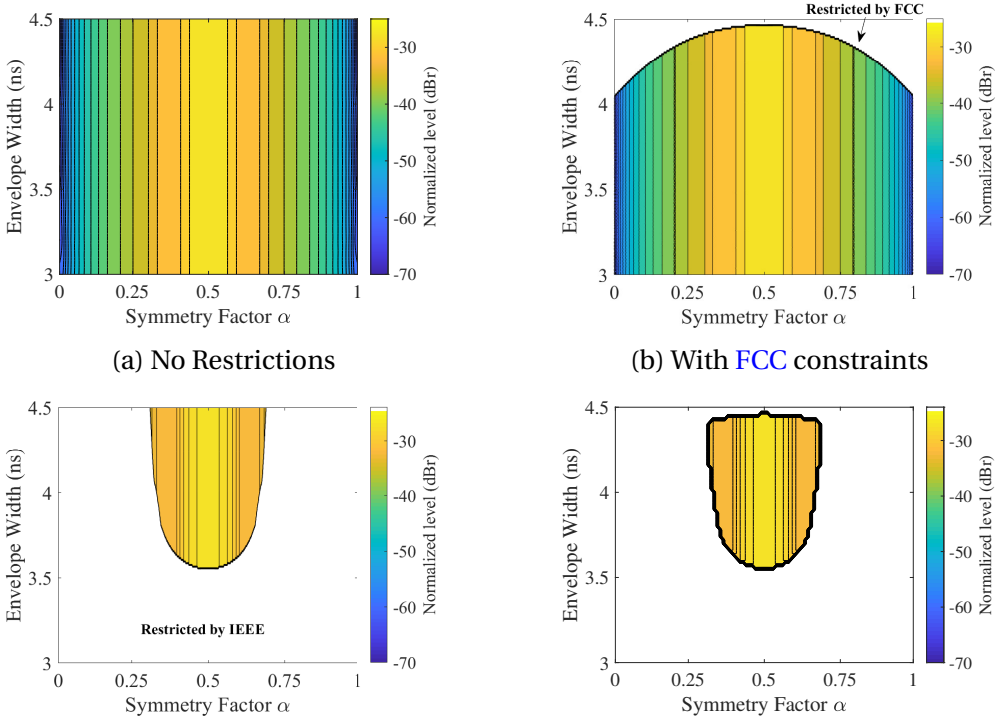
From Figure 2.18a, it can be seen that the FCC spectral requirements delimit the maximal values of envelope width, whereas the IEEE delimits the minimal values of envelope width. From Figure 2.18b, the maximum α range allowed is from 0.31 to 0.69. The maximal 18 dB bandwidth of 800 MHz imposed by the IEEE is the most restrictive among the addressed spectral requirements. The white region at the top of Figure 2.18a corresponds to the white region of Figure 2.19b. In addition, the white region of Figure 2.18b corresponds to the white region of Figure 2.19c. In Figure 2.19d, the side-lobe rejection is greater at the border with the forbidden zone. The envelope width of 4.41 ns enables the maximal range of α (0.31 to 0.69). Since, for a fixed envelope width, the highest side-lobe rejection is at the borders of the symmetrical factor available range, an optimal side-lobe rejection of 33.3 dB can be obtained.

Finally, Figure 2.20 shows an IR-UWB pulse waveform and spectrum with an asymmetrical triangular envelope (α = 0.31) and a duration of 4.40 ns. This pulse addresses channel 3 of IEEE 802.15.4 and channel 2 of IEEE 802.15.6. From this Figure, it can observed that the spectrum of this asymmetrical triangular pulse fits into IEEE spectral masks. Besides, this pulse presents a side-lobe rejection of 33.3 dB. Compared to the symmetrical triangular pulse, the asymmetrical



(a) X = 10dB (b) X = 18dB (c) X = 20dB

Figure 2.18.: Asymmetrical triangular envelope bandwidth BW as a function of symmetry factor α and envelope width compliant with IEEE 802.15.6 standard (BW = 499.2 MHz)



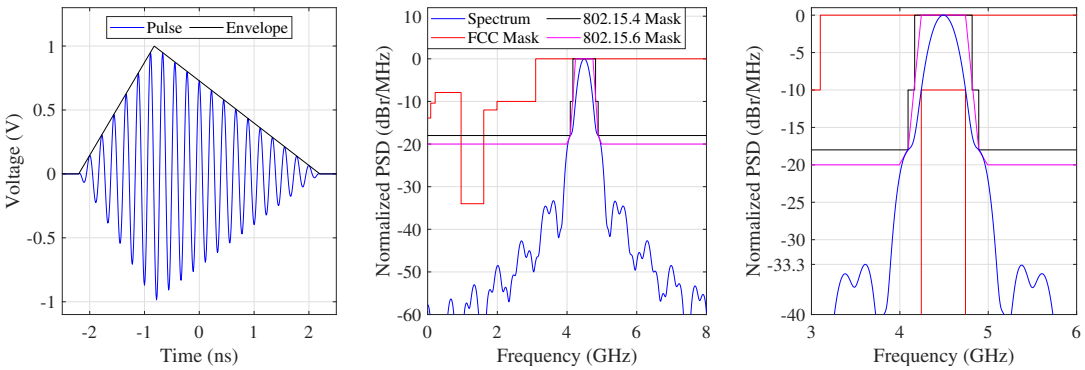
(a) No Restrictions (b) With FCC constraints

(c) With IEEE constraints (d) With both FCC and IEEE constraints

Figure 2.19.: Level of the strongest side-lobe of the asymmetrical triangular envelope as a function of symmetry factor α and envelope width compliant with IEEE 802.15.6 standard (BW = 499.2 MHz).

triangular pulse can achieve a stronger rejection level (33.3 dB versus 26.5 dB).

Regarding the pulse energy, considering an impedance load of 50 Ω and an amplitude $A = 1$ V, the asymmetrical triangular pulse of Figure 2.20 has 14.60 pJ. The asymmetrical triangular pulse has energy emitted 19% greater than the one of the symmetrical triangular pulse of Figure 2.15 (11.84 pJ). Even though the symmetry factor does not change the pulse energy, the



(a) Waveform (b) Spectrum (c) Spectrum (Zoomed)

Figure 2.20.: IR-UWB pulse with asymmetrical triangular envelope compliant with channel 3 of IEEE 802.15.4 and channel 2 of IEEE 802.15.6 (BW = 499.2 MHz, $\alpha = 0.31$ and $\tau = 4.40$ ns)

asymmetrical triangular pulse of Figure 2.20 has a greater energy emitted because of its larger width.

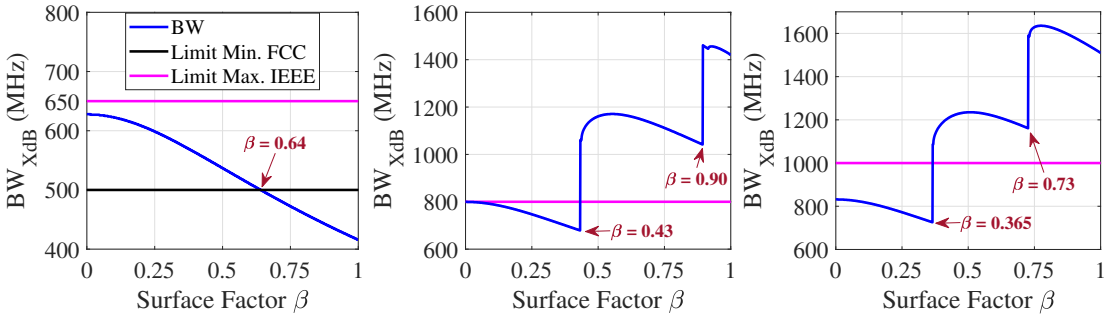
2.3.2.4. Symmetrical Trapezoidal

Like the asymmetrical triangular envelope, the symmetrical trapezoidal envelope (Fig. 2.7a) has the same amount of degree of freedom, but it has the surface factor β instead of the symmetry factor α. It is worth highlighting that for a surface factor of 0 and 1, the trapezoidal envelope will be triangular and rectangular, respectively (Fig. 2.7b). As observed in the general study case, from Figure 2.9, the trapezoidal envelope can reach an side-lobe rejection of 31.88 dB for $\beta = 0.164$.

Figure 2.21 shows the symmetrical trapezoidal envelope bandwidth as a function of the surface factor β, for several values of X_{dB} attenuation. In this Figure, the envelope width τ is at 3.55 ns, which is the minimal width of the symmetrical triangular envelope. On the other hand, Figure 2.22 shows the available level of the strongest side-lobe of the symmetrical trapezoidal envelope as a function of surface factor β.

From Figure 2.21a, it can be observed that for surface factor lower or equal to 0.64, the trapezoidal envelope satisfies the minimum 10 dB bandwidth of 500 MHz required by FCC. In other words, the FCC requirements are no longer fulfilled when the envelope becomes too rectangular. In addition, Figures 2.21b and 2.21c indicate the maximal available value of β is 0.365. This value is right before the steep rise. The steep rise delimits the maximal value of the surface factor accepted by the IEEE 802.15.6 standard. A more triangular envelope can respect FCC and IEEE simultaneously. Besides, as can be seen in Figure 2.22, the optimal side-lobe rejection (31.88 dB) is reached when $\beta = 0.164$. Meanwhile, the worst side-lobe rejection (20.1 dB) is achieved when $\beta = 0.365$.

Figures 2.23 and 2.24 display the symmetrical trapezoidal envelope bandwidth and level of the strongest side-lobe as a function of surface factor β and envelope width, respectively. The envelope width is swept from 3 ns to 4.5 ns. Concerning the white zones, it is worth pointing



(a) X = 10 dB (b) X = 18 dB (c) X = 20 dB

Figure 2.21.: Symmetrical trapezoidal envelope bandwidth BW as a function of surface factor β compliant with IEEE 802.15.6 standard (BW = 499.2 MHz and τ = 3.55 ns)

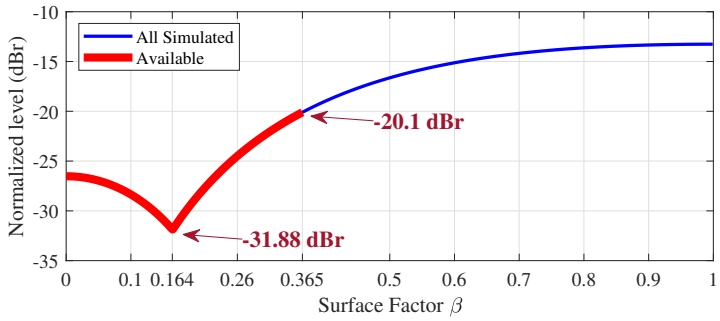


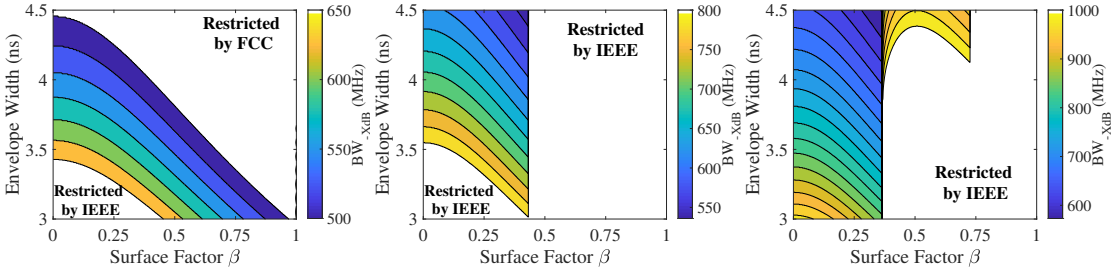
Figure 2.22.: Level of the strongest side-lobe of the symmetrical trapezoidal envelope as a function of surface factor β compliant with IEEE 802.15.6 standard (BW = 499.2 MHz and τ = 3.55 ns).

out the guidelines described in Figures 2.18 and 2.19.

From Figures 2.23b and 2.23c, a β greater than 0.43 is not allowed. For envelope widths shorter than 3.5 ns, the IEEE imposes a minimum value of β. From Figure 2.24d, the maximum surface factor allowed is 0.365, and the minimal envelope width is 3.15 ns. Besides, the highest side-lobe rejection (31.9 dB) is at β = 0.164. Considering the optimal surface factor, the range of available envelope width is from 3.45 ns to 4.35 ns. Therefore, the FCC and IEEE spectral constraints do not affect the optimal side-lobe rejection, but they restrict the envelope width.

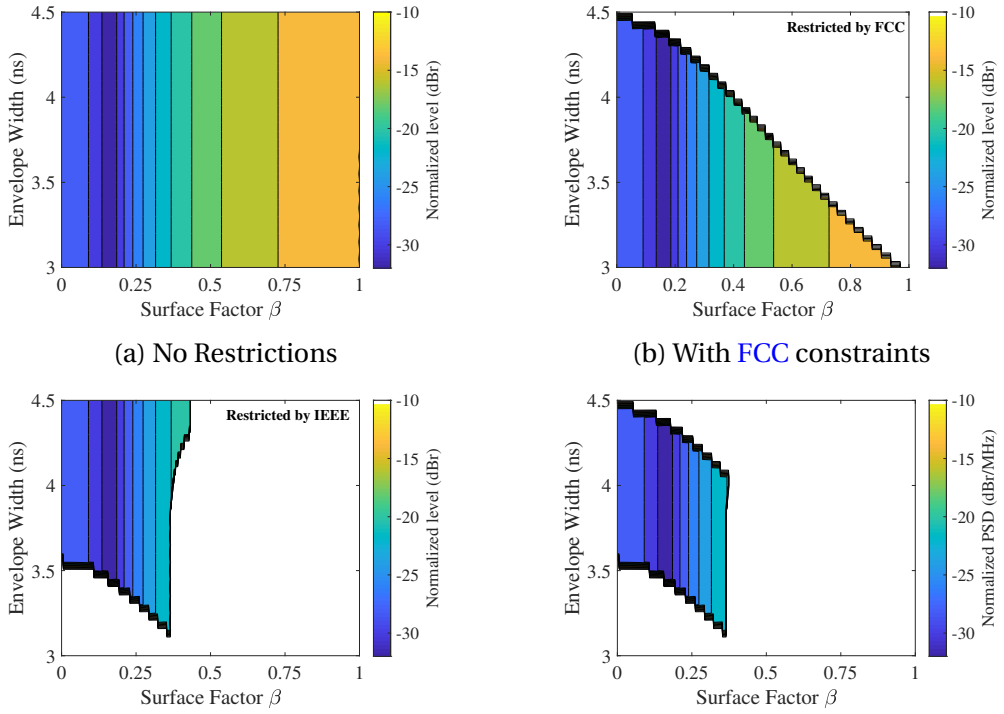
Finally, Figure 2.25 displays an IR-UWB pulse waveform and spectrum with a symmetrical trapezoidal envelope (β = 0.164) and a duration of 3.45 ns. This pulse addresses channel 3 of IEEE 802.15.4 and channel 2 of IEEE 802.15.6. The spectrum of this trapezoidal pulse fits into IEEE spectral masks and features a side-lobe rejection of 31.9 dB. Compared to the symmetrical triangular pulse, the symmetrical trapezoidal pulse can reach a stronger rejection level (31.9 dB versus 26.5 dB). Nevertheless, compared to the asymmetrical triangular pulse, the symmetrical trapezoidal pulse cannot achieve a stronger rejection level (31.9 dB versus 33.3 dB).

Concerning the pulse energy, considering an impedance load of 50 Ω and an amplitude A =



(a) X = 10 dB (b) X = 18 dB (c) X = 20 dB

Figure 2.23.: Symmetrical trapezoidal envelope bandwidth BW as a function of surface factor β and envelope width compliant with IEEE 802.15.6 standard (BW = 499.2 MHz)

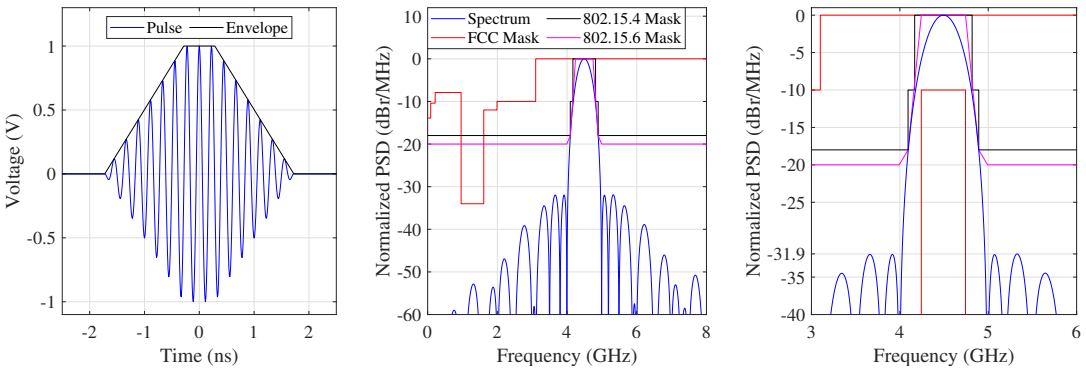


(a) No Restrictions (b) With FCC constraints

(c) With IEEE constraints (d) With both FCC and IEEE constraints

Figure 2.24.: Level of the strongest side-lobe of the symmetrical trapezoidal envelope as a function of surface factor β and envelope width compliant with IEEE 802.15.6 standard (BW = 499.2 MHz).

1 V, the symmetrical trapezoidal pulse of Figure 2.25 has 15.2 pJ. The symmetrical trapezoidal pulse has an energy 4.1% greater than the one of the symmetrical triangular pulse of Figure 2.15 (14.6 pJ). The reason for this is because the pulse energy is linearly dependent of the surface factor β. Therefore, the trapezoidal envelope enables better side-lobe rejection and higher pulse energy.



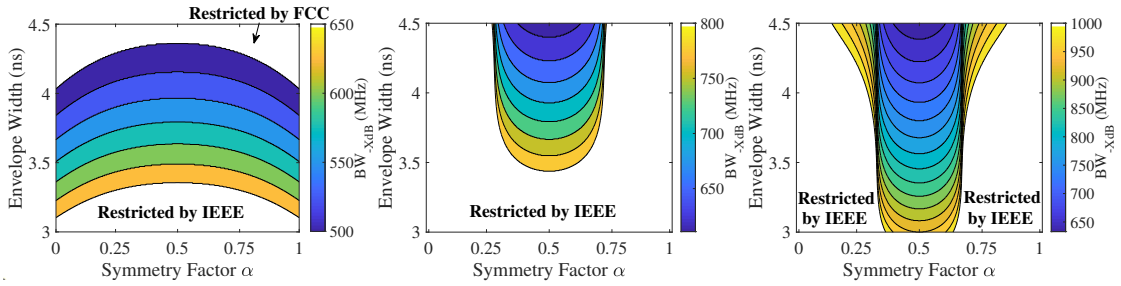
(a) Waveform (b) Spectrum (c) Spectrum (Zoomed)

Figure 2.25.: IR-UWB pulse with symmetrical trapezoidal envelope compliant with channel 3 of IEEE 802.15.4 and channel 2 of IEEE 802.15.6 (BW = 499.2 MHz, $\beta = 0.164$ and $\tau = 3.45$ ns)

2.3.2.5. Asymmetrical Trapezoidal

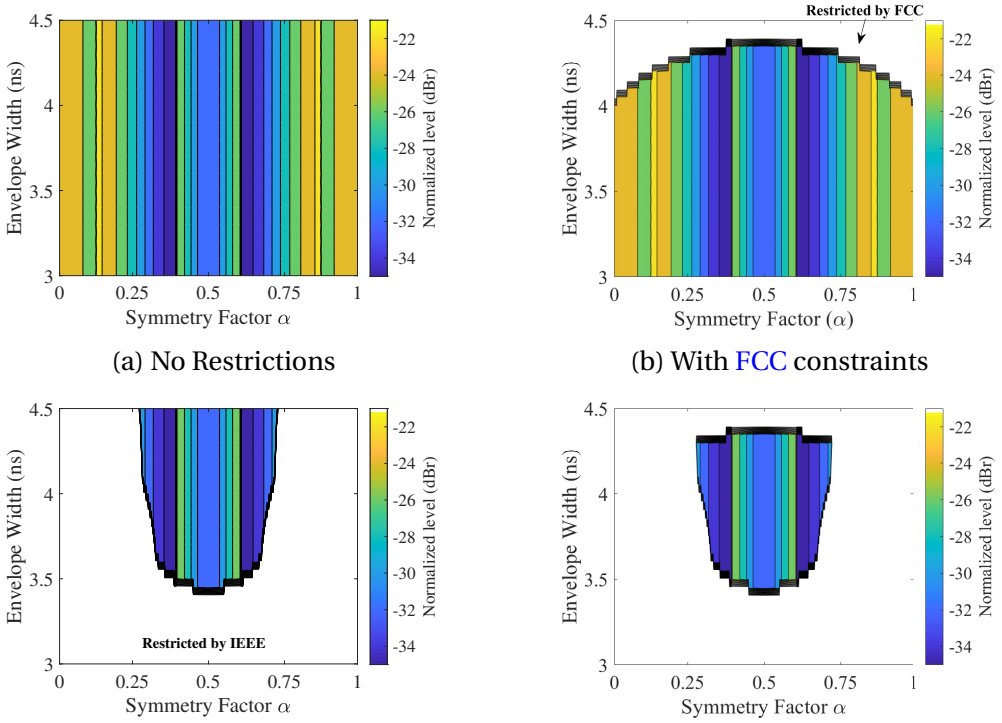
Compared to the symmetrical trapezoidal envelope, the asymmetrical trapezoidal envelope (Fig. 2.11a) has an additional degree of freedom, which is the symmetry factor α. The most versatile continuous envelope has degrees of freedom in terms of the envelope width, symmetry factor, and surface factor. This suggests that this envelope can achieve the highest available side-lobe rejection.

Figures 2.26 and 2.27 show the asymmetrical trapezoidal envelope bandwidth and level of the strongest side-lobe as a function of the symmetry factor α and envelope width, respectively. The surface factor is fixed at 0.164. The envelope width is swept from 3 ns to 4.5 ns. Concerning the white zones, it is worth highlighting the guidelines described in Figures 2.18 and 2.19. Figure 2.26 is similar to Figure 2.18. Figure 2.26 suggests that the maximum α range allowed is from 0.27 to 0.73.



(a) X = 10 dB (b) X = 18 dB (c) X = 20 dB

Figure 2.26.: Asymmetrical trapezoidal envelope bandwidth BW as a function of symmetry factor α and envelope width compliant with IEEE 802.15.6 standard (BW = 499.2 MHz and $\beta = 0.164$)



(a) No Restrictions

(b) With FCC constraints

(c) With IEEE constraints

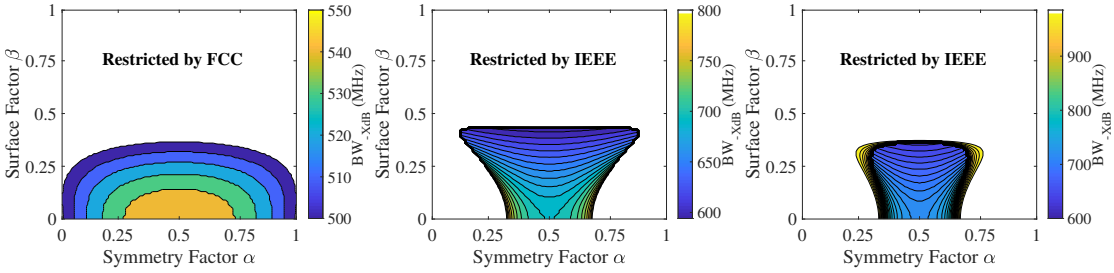
(d) With both FCC and IEEE constraints

Figure 2.27.: Level of the strongest side-lobe of the asymmetrical trapezoidal envelope as a function of symmetry factor α and envelope width compliant with IEEE 802.15.6 standard (BW = 499.2 MHz and $\beta = 0.164$).

However, between Figure 2.27 and 2.19, there are differences to be highlighted. In Figure 2.19, the side-lobe rejection is higher when the envelope is more asymmetrical. On the other hand, in figure 2.27, the side-lobe rejection is higher at $\alpha = 0.38$ or $\alpha = 0.62$. The side-lobe rejection is lower when α is outside the range from 0.25 to 0.75, as shown in Figure 2.27a. Thus, the highest side-lobe rejection is not necessarily at the borders of the forbidden zone in Figure 2.27d. For this Figure, the highest side-lobe rejection achieved is 34.45 dB for an envelope width of 4.06 ns and a symmetry factor of 0.378 or 0.618.

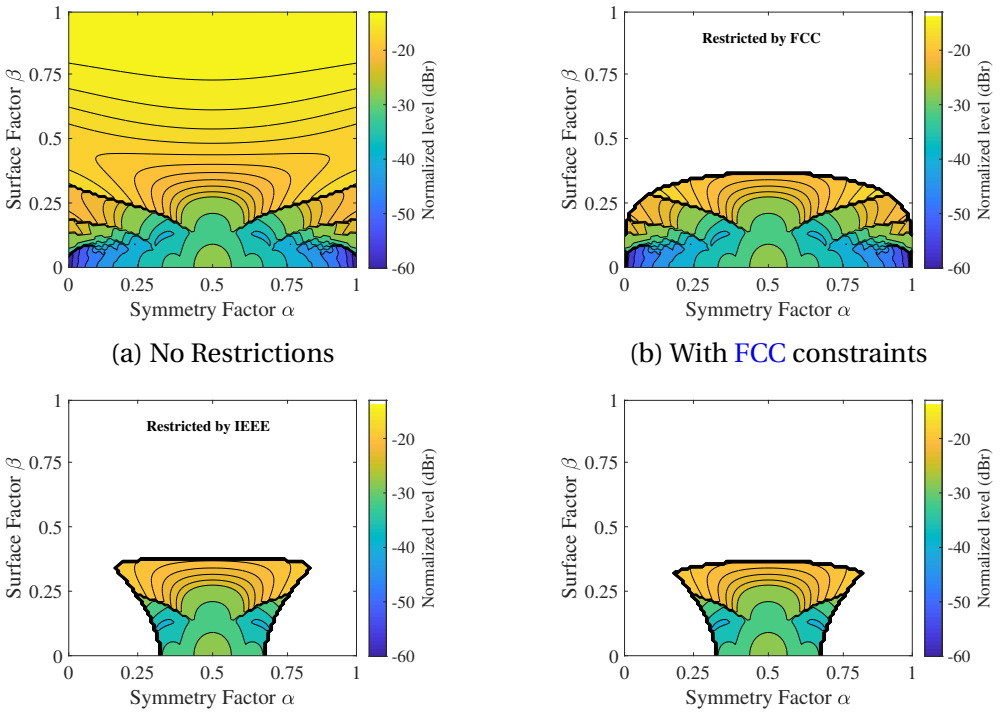
Figures 2.28 and 2.29 show the asymmetrical trapezoidal envelope bandwidth and level of the strongest side-lobe as a function of the symmetry α and surface β factors. The envelope width is fixed at 4.06 ns.

From Figure 2.28, it can be observed that the FCC restricts rectangular envelopes, while the IEEE 802.15.4 and 802.15.6 restricts envelopes with rectangular or saw-tooth shapes. From Figure 2.29d, it can be observed that for lower available values of β, the range of available values of α becomes shorter. Indeed, a more triangular and asymmetric envelope has a wider bandwidth for high attenuation (10 dB and 18 dB). As a result, the spectral masks are no longer respected. From Figure 2.29d, the highest side-lobe rejection achieved is 37.22 dB for a surface factor of 0.12 and a symmetry factor of 0.33 or 0.67. Therefore, the asymmetrical trapezoidal has shown great flexibility in handling the spectral constraints, reaching better side-lobe rejection.



(a) X = 10dB (b) X = 18 dB (c) X = 20 dB

Figure 2.28.: Asymmetrical trapezoidal envelope bandwidth BW as a function of symmetry α and surface β factors compliant with IEEE 802.15.6 standard (BW = 499.2 MHz and τ = 4.06 ns)



(a) No Restrictions (b) With FCC constraints

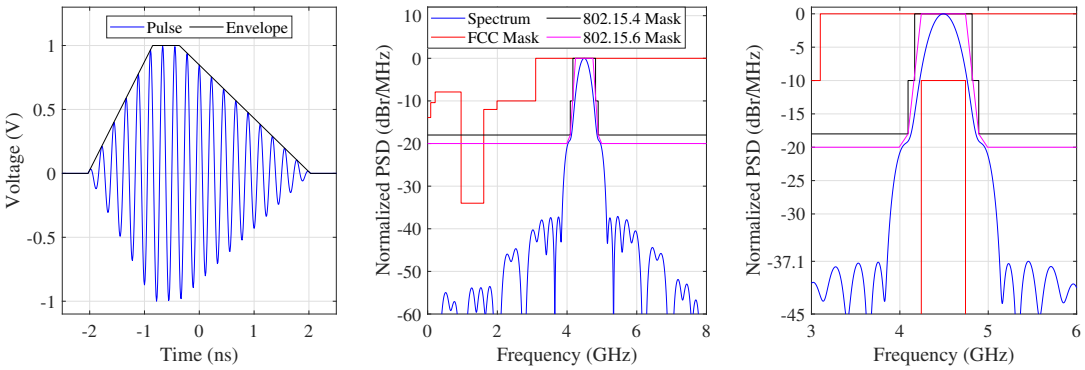
(c) With IEEE constraints (d) With both FCC and IEEE constraints

Figure 2.29.: Level of the strongest side-lobe of the asymmetrical trapezoidal envelope as a function of symmetry α and surface β factors compliant with IEEE 802.15.6 standard (BW = 499 MHz and τ = 4.06 ns).

Figure 2.30 displays an IR-UWB pulse waveform and spectrum with an asymmetrical trapezoidal envelope (α = 0.33, β = 0.12) and a duration of 4.06 ns. This pulse addresses channel 3 of IEEE 802.15.4 and channel 2 of IEEE 802.15.6. The spectrum of this asymmetrical trapezoidal pulse fits into IEEE spectral masks. This pulse has an side-lobe rejection of 37.10 dB. Compared to the asymmetrical triangular pulse, the symmetrical trapezoidal pulse can reach a stronger

rejection level (37.1 dB versus 33.3 dB).

Concerning the pulse energy, considering an impedance load of 50 Ω and an amplitude A = 1 V, the symmetrical trapezoidal pulse of Figure 2.30 has 16.8 pJ. The symmetrical trapezoidal pulse has energy emitted 15.1% greater than the one of the asymmetrical triangular pulse of 2.20 (14.6 pJ). Thus, between the asymmetrical envelopes, the trapezoidal one achieves better side-lobe rejection and greater emitted pulse energy thanks to a slight increase in the envelope surface area.



(a) Waveform (b) Spectrum (c) Spectrum (Zoomed)

Figure 2.30.: IR-UWB pulse with asymmetrical trapezoidal envelope compliant with channel 3 of IEEE 802.15.4 and channel 2 of IEEE 802.15.6 (BW = 499.2 MHz, α = 0.33, β = 0.12 and τ = 4.06 ns)

2.3.2.6. Summary

Finally, Table 2.4 summarizes the performance of the addressed continuous envelopes considering the spectral requirements imposed by FCC and IEEE standards. The minimum 10 dB bandwidth of 500 MHz imposed by FCC delimits the maximum values of pulse width. On the other hand, the IEEE spectral masks delimit the minimum values of pulse width. There is a limited available range of symmetry and surface factors associated with a single value of pulse width. In general, the spectral requirements, mostly the ones imposed by IEEE standards, restrict higher values of symmetry and surface factors. An envelope too asymmetric (higher α) or too rectangular (higher β) does not fit into the IEEE spectral masks.

From Table 2.4, among the pulses that can respect FCC and IEEE spectral requirements, it can be perceived that the asymmetrical trapezoidal pulse has the highest side-lobe rejection (37.1 dB), and the symmetrical triangular has the lowest one (26.5 dB). Besides, the asymmetrical trapezoidal has the highest pulse energy emitted (16.8 pJ), whereas the symmetrical triangular has the lowest one (11.8 pJ). Consequently, the asymmetrical trapezoidal shape has demonstrated significant flexibility in addressing spectral constraints, achieving improved side-lobe rejection and increased emitted pulse energy.

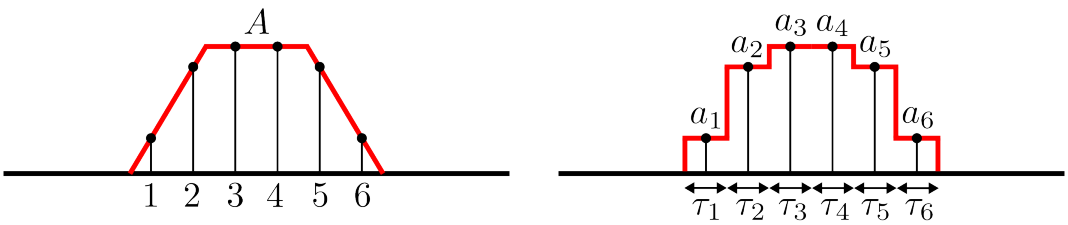
Table 2.4.: IR-UWB pulses summary addressing channel 3 of IEEE 802.15.4 and channel 2 of IEEE 802.15.6 (BW = 499 MHz)

continuous Envelope	Rectangular	Sym. Triangular	Asym. Triangular	Sym. Trapezoidal	Asym. Trapezoidal
Symmetry Factor α	0 to 1	0.5	0.313	0.5	0.33
Surface Factor β	1	0	0	0.164	0.12
Pulse Width τ (ns)	6.30	3.55	4.4	3.45	4.06
Can respect FCC and IEEE?	No	Yes	Yes	Yes	Yes
Side-Lobe Rejection (dB)	13.3	26.5	33.3	31.9	37.10
BW_{-3dB} (MHz)	139	359	283	363	306
BW_{-10dB} (MHz)	232	628	501	632	538
BW_{-18dB} (MHz)	790	800	798	797	734
BW_{-20dB} (MHz)	842	832	940	826	934
Energy (pJ) @Z_L = 50 Ω	23	11.8	14.6	15.2	16.8

2.4. Sample and Hold Envelope

In the previous section, it has been possible to notice that the generation of IR-UWB triangular and trapezoidal pulses can comply with the spectral requirements imposed by FCC regulations and IEEE 802.15.4 and 802.15.6 standards. In particular, the asymmetrical pulses can achieve higher side-lobe rejection, which is searched in this thesis work. Nevertheless, these continuous envelopes are not easy to synthesize using analog electronic circuits [13, 41].

To simplify the generation of trapezoidal or similar envelopes, the sample and hold envelope is proposed. It corresponds to an approximation of a continuous envelope, as indicated in Figure 2.31, where a_n and τ_n are the amplitude and the duration of the nth envelope sample, respectively. For instance, the sample and hold envelope can be obtained from continuous envelope sampling and fabricated using a digital architecture [13, 41].



(a) Continuous envelope.

(b) Sample and hold envelope.

Figure 2.31.: Principle of a continuous envelope approximation via sample and hold the envelope.

In general, the sample and hold envelope can be represented as a combination of rectangular time-shifted functions with different amplitudes and different sample times, which can be written as follows:

$$x_{SH}(t) = \sum_{n=1}^{N} a_n \cdot \Pi_{\tau_n}(t - \sigma_n) \tag{2.41}$$

where N is the total number of samples. $\Pi_\tau(t)$ is the gate function of width τ, and σ_n are the time shifts allowing the generated pulse to be centered around $t = 0$. This last parameter can be expressed as:

$$\sigma_n = \left(\sum_{m=1}^{n} \tau_m\right) - \frac{T_E}{2} - \frac{\tau_n}{2} \tag{2.42}$$

where T_E represents the total duration during which the envelope is not null and can be expressed as the sum of sample durations, as follows:

$$T_E = \sum_{n=1}^{N} \tau_n \tag{2.43}$$

The Fourier Transform of the sample and hold envelope can be expressed as follows:

$$X_{SH}(f) = \sum_{n=1}^{N} a_n \cdot \tau_n \cdot \mathrm{sinc}(f\tau_n) \exp(-j2\pi f \sigma_n) \tag{2.44}$$

From the pulse emitted expression (2.9), the energy associated with this sample and hold can be estimated as follows:

$$E_{p-SH} = \frac{1}{2Z_L} \cdot \sum_{n=1}^{N} a_n^2 \cdot \tau_n \tag{2.45}$$

This section also considers sample and hold envelope and is divided into two parts. In a first time, a uniform sampling of the studied continuous envelopes, particularly the triangular and trapezoidal envelopes, is presented. The impact of the uniform sampling on the side-lobe rejection is analyzed. In a second time, an optimization of an arbitrary sample and hold envelope in terms of side-lobe rejection is addressed. The optimizable variables are the amplitude a_n and the duration τ_n of each envelope sample.

2.4.1. Uniform Sampling

A particular case is the uniform sample and hold envelope, whose sample times are fixed to a single value defined as τ_S. Hence, this envelope, in particular, is a combination of rectangular uniform time-shifted functions. In this case, the envelope total duration T_E can be rewritten as [13, 41]:

$$T_E = N \cdot \tau_S \tag{2.46}$$

where τ_S is the sampling period. Hence, the envelope sampling frequency F_S can be described as:

$$F_S = \frac{1}{\tau_S} \tag{2.47}$$

Alternatively, from equation (2.46), the sampling frequency can expressed as follows:

$$F_S = \frac{N}{T_E} \tag{2.48}$$

where the number of samples is proportional to the sampling frequency. For this particular case, σ_n and a_n can be expressed as follows:

$$\sigma_n = n\tau_S - \sigma_0 \tag{2.49}$$

$$a_n = x_C(t) \cdot \delta(t - n\tau_S + \sigma_0) \tag{2.50}$$

$$a_n = x_C(n\tau_S - \sigma_0) \tag{2.51}$$

where:

$$\sigma_0 = \frac{N\tau_S}{2} - \frac{\tau_S}{2} \tag{2.52}$$

and $x_C(t)$ is the considered continuous envelope to be sampled. When applying the expressions (2.49) and (2.50) on function (2.41), the uniform sample and hold envelope expression can be written as follows [13, 41]:

$$x_{USH}(t) = \sum_{n=1}^{N} x_C(t) \cdot \delta(t - n\tau_S + \sigma_0) \cdot \Pi_{\tau_n}(t - (n\tau_S - \sigma_0)) \tag{2.53}$$

Shifting to the frequency domain, the Fourier transform of the uniform sample and hold envelope is given as follows:

$$X_{USH}(f) = \text{sinc}\left(\frac{f}{F_S}\right) \exp(j2\pi\sigma_0) \cdot \sum_{n=1}^{N} X_C(f - nF_S) \tag{2.54}$$

where a mathematical demonstration is given in Appendix C. Figure 2.32 shows the principle of aliasing caused by sampling $x_C(t)$. This Figure mostly highlights the first replicas of the spectrum main lobe. The red curve corresponds to the spectrum's main lobe, whereas the green and magenta curves represent the spectrum's replicas. Each spectrum's replica is spaced in an integer multiple of F_s from the spectrum centered at $f = 0$ (red curve). These replicas are attenuated by the $\text{sinc}(f/F_S)$ (gray dashed curve). Concerning the spectrum of uniform sample and hold envelope, all replicas are combined. In particular, the first replicas may degrade the side-lobe rejection, mostly for a lower number of samples.

Since the frequency sampling is proportional to the number of samples, one solution to mitigate the side-lobe loss is to increase the number of samples. This solution can be justified by the fact that the higher the number of samples is, the further the first replicas are from the main original lobe. Consequently, the attenuation on the replicas will be greater.

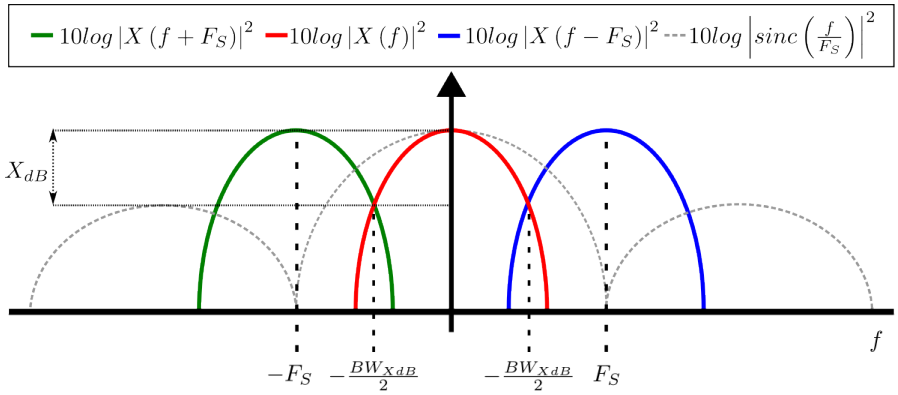


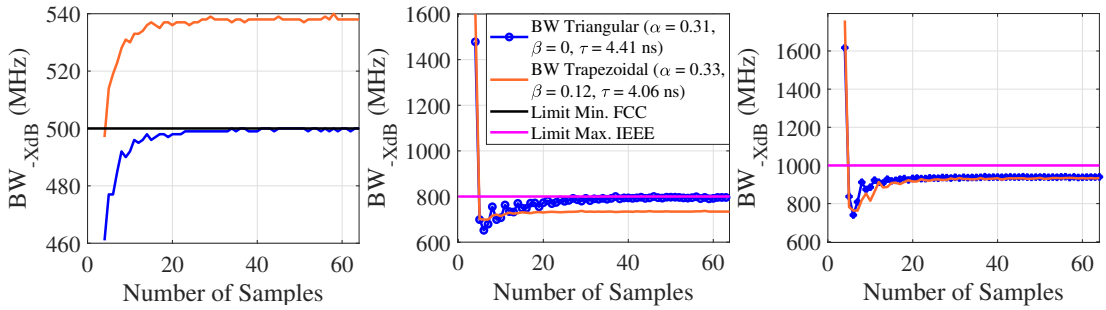
Figure 2.32.: Principle of aliasing caused by sampling the continuous envelope.

From expression (2.45), the energy associated with the uniform sample and hold can be estimated as follows:

$$E_{p-USH} = \frac{\tau_S}{2Z_L} \cdot \sum_{n=1}^{N} x_C^2\,(n\tau_S - \sigma_0) \tag{2.55}$$

It is intended to observe the effects of uniform sampling on the best IR-UWB triangular and trapezoidal pulses of Figures 2.20 and 2.30 in terms of side-lobes rejection. Figures 2.33 and 2.34 show the uniform sample and hold envelope bandwidth and level of the strongest side as a function of the number of samples, respectively. The number of samples is between 4 and 64.

Figure 2.33 suggests that a low number of samples leads to a shorter envelope bandwidth for an attenuation of 10 dB. The lower the number of samples, the more similar the sample and hold envelope is to a rectangular envelope. In particular, for the triangular envelope, to satisfy the minimum 10 dB bandwidth of 500 MHz imposed by FCC, a minimal number of samples required is 24. Another solution consists of increasing the continuous envelope width, which allows a lower number of samples. The steep rises in Figures 2.33b and 2.33c can be attributed to the low side-lobe rejection.



(a) X = 10 dB (b) X = 18 dB (c) X = 20 dB

Figure 2.33.: Uniform sample and hold envelope bandwidth BW as a function of number of samples

From Figure 2.34, it can be perceived that is necessary at least 24 samples to achieve the

side-lobe rejection (33.3 dB) of the triangular envelope. On the other hand, it is necessary at least 35 samples to reach the side-lobe rejection (37.2 dB) of the trapezoidal envelope. The greater the side-lobe rejection of the continuous envelope, the more samples are required. For a low number of samples, both curves (blue and orange) present the same value. The reason for these lower adjacent rejections comes from the aliasing.

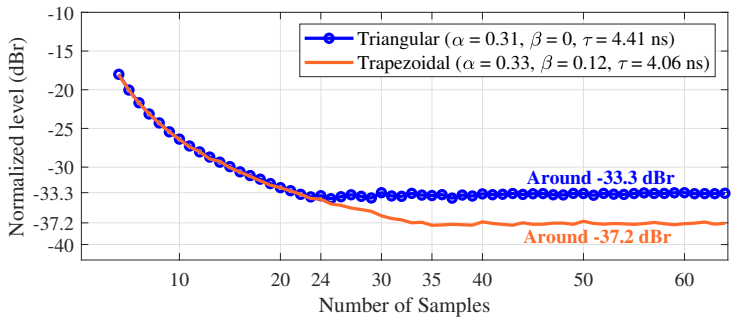


Figure 2.34.: Level of the strongest side-lobe of uniform sample and hold envelope as a function of the number of samples

To clarify, Figures 2.35 and 2.36 show some uniform sample and hold envelopes waveforms and spectra for several numbers of samples. For these Figures, the triangular envelope of Figure 2.20 was sampled. In Figure 2.36, it can be noticed the presence of the side-lobes coming from aliasing. In particular, for $N = 13$, the side-lobe from aliasing has a lower rejection than the side-lobe of the continuous envelope. On the contrary, for $N = 23$, the side-lobe from aliasing and the one of the continuous envelope have approximately the same rejection. Lastly, for $N = 33$, the side-lobe from aliasing has a stronger rejection than the side-lobe of the continuous envelope. A higher sampling frequency results in weaker side-lobes, which are further away from the main lobe.

Therefore, to mitigate the reduction of adjacent side-lobe caused by aliasing, a solution is to increase the number of samples. Nevertheless, a high number of uniform samples will result in lower sample time, requiring a faster digital circuit and a more complex architecture.

Finally, Figure 2.37 shows an IR-UWB pulse waveform and spectrum with a uniform sample and hold envelope ($N = 8$) and a duration of 4.06 ns. For this Figure, the trapezoidal envelope

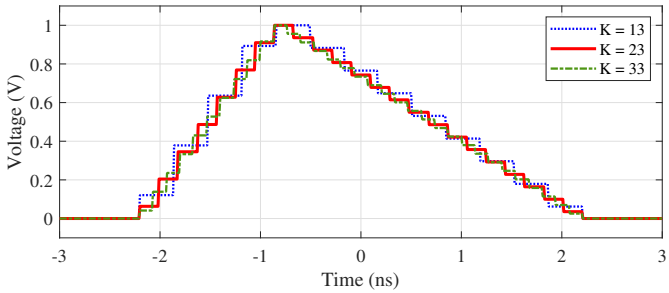
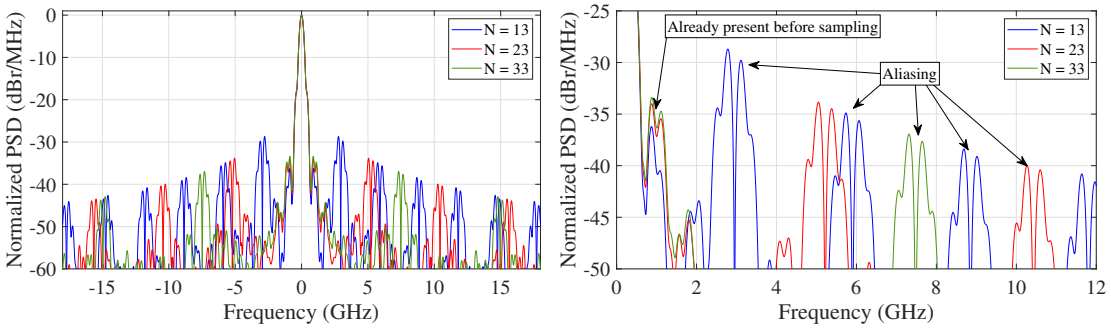


Figure 2.35.: Uniform sample and hold envelope waveforms for several numbers of samples ($T_E = 4.41$ ns)



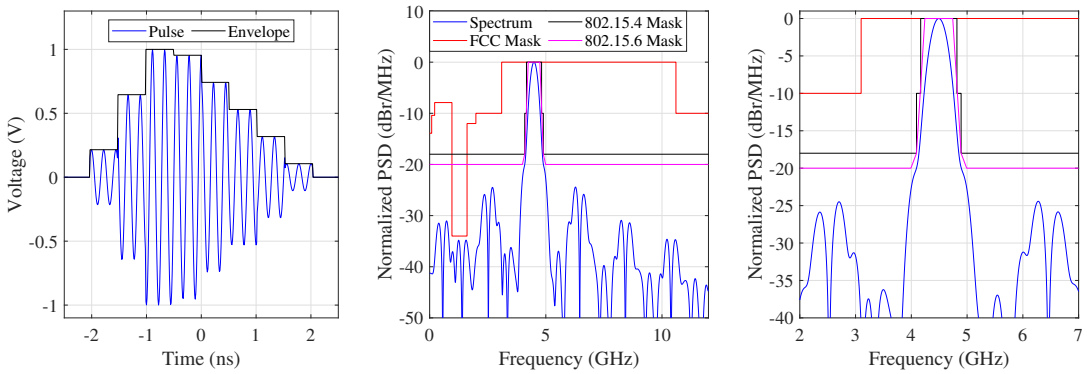
(a) Spectra (b) Spectra (Zoomed)

Figure 2.36.: Uniform sample and hold envelope spectra for several numbers of samples (T_E = 4.41 ns)

of 2.30 has been sampled. This pulse addresses channel 3 of IEEE 802.15.4 and channel 2 of IEEE 802.15.6. The spectrum of this pulse fits into IEEE spectral masks. This pulse has a side-lobe rejection of 24.42 dB.

Concerning the pulse energy, considering an impedance load of 50 Ω and an amplitude A = 1 V, the pulse of Figure 2.37 has 16.8 pJ, like the pulse energy of the continuous pulse.

Two solutions exist to achieve a higher side-lobe rejection. One involves increasing the number of samples, and another involves optimizing the sample and hold envelope. The second seems to be more efficient since it can improve side-lobe rejection even with a smaller number of samples.



(a) Waveform (b) Spectrum (c) Spectrum (Zoomed)

Figure 2.37.: IR-UWB pulse with uniform sample and hold compliant with channel 3 of IEEE 802.15.4 and channel 2 of IEEE 802.15.6 (BW = 499.2 MHz, N = 8 and T_E = 4.06 ns).

2.4.2. Optimization

The previous sub-section presents uniform sampling of a given continuous envelope, where a higher number of samples is required to achieve the same side-lobe rejection of the continuous

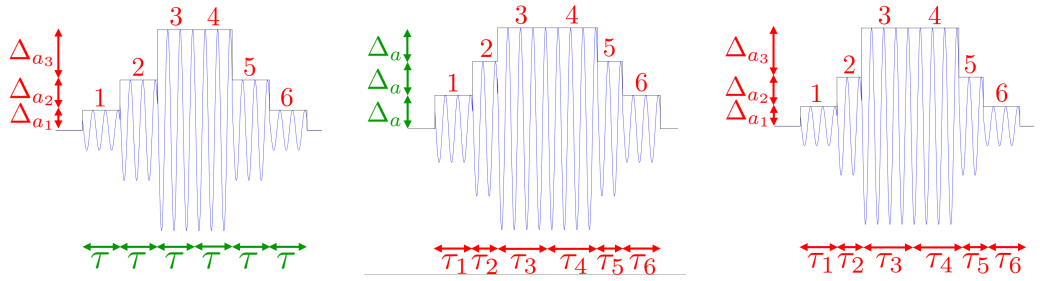
envelope. Alternatively, instead of sampling the continuous envelope with more samples, an optimization of an arbitrary sample and hold envelope is proposed to achieve a high side-lobe rejection with fewer envelope samples. The optimizable variables are the amplitude a_n and the duration τ_n of each envelope sample.

Three different approaches are tested to implement an efficient sample and hold envelope generator with a low number of degrees of freedom and a low design complexity. The first approach sets all values of sample duration τ_n to one fixed value (approach A - uniform sampling). The second one sets all values of sample amplitude a_n such that $\Delta_{a_n} = |a_{n+1} - a_n|$ is constant, and either positive for $t < 0$ or negative for $t > 0$ (approach B – non-uniform sampling). Finally, the third and last approach allows control of every a_n and τ_n (approach C - envelope fully arbitrary).

For each approach, either a symmetrical or an asymmetrical envelope is exploited. The asymmetrical envelope enables a higher number of degrees of freedom. For example, for an even N, the asymmetrical envelope requires to optimize a number of variables two times greater than the one of the symmetrical envelope. These approaches are resumed in Table 2.5 and shown in Figure 2.38. In this Figure, the parameters in red are variable, whereas the green ones are constant.

Table 2.5.: Constraints on τ_n and Δ_{a_n} for every approach of sample and hold envelope generation.

Approach	A Uniform Sampling	B Non-uniform Sampling	C Fully Arbitrary
τ_n	Constant	Variable	Variable
Δ_{a_n}	Variable	Constant	Variable



(a) Approach A (b) Approach B (c) Approach C

Figure 2.38.: Principle of sample and hold envelope optimization approaches.

These approaches have been tested in Matlab environment for several numbers of samples. For this test, scripts have been developed sweeping the set of a_n and τ_n values with the constraints associated with each approach. For convenience, the optimization works with normalized values of a_n and τ_n, which must be always greater than zero. The maximum authorized amplitude of the envelope normalizes a_n. Here, the maximum allowed amplitude of the envelope is set to 1. On the other hand, τ_n is normalized by T_E.

Regarding approach A, there are two constraints: the value of the envelope duration T_E and the range of allowed values of normalized a_n. The authorized range is from a minimal normalized amplitude greater than zero to 1. In other words:

$$\gamma_i = [\gamma_{min}, 1] \quad ; \quad 1 \leq i \leq N \tag{2.56}$$

where γ_i corresponds to the normalized amplitude, and γ_{min} is the minimal normalized amplitude, which is typically 0.1 or 0.2 in this thesis work.

Concerning approach B, there are essentially two constraints: the value of the envelope duration T_E and the sum of τ_n, such that:

$$\sum_{i=1}^{N} \tau_i = T_E \tag{2.57}$$

$$\sum_{i=1}^{N} \rho_i = 1 \tag{2.58}$$

where ρ_i corresponds to the normalized sample duration. An explanation of the constraints of approach B is given in Appendix C. Lastly, approach C encompasses the constraints of approaches A and B. The value of the envelope duration T_E is the common constraint among the presented approaches.

An optimization of arbitrary sample and hold envelope is performed considering the three approaches of Table 2.5. For each approach, the symmetrical and asymmetrical envelopes are tested.

Table 2.6 displays the optimization results in terms of side-lobes rejection associated with the test approaches. The value of the envelope T_E is fixed to 3.5 ns to target the standard 499.2 MHz IEEE channels. The maximum amplitude has been set as 1. In addition, Figure 2.39 shows the maximum rejection as a function of the number of samples for different approaches.

Table 2.6 shows that a greater number of samples enables a higher maximum rejection. It is

Table 2.6.: Maximum side-lobe rejection as a function of the number of samples and the followed approach for a 499.2 MHz IEEE Channel (T_E = 3.5 ns)

N	Rejection as a function of approach (dB)					
	Symmetrical			Asymmetrical		
	A	B	C	A	B	C
4	19.31	20.84	20.96	19.31	21.88	23.40
5	21.41	25.01	25.08	21.58	26.64	26.64
6	23.11	25.01	25.08	23.19	26.64	27.12
7	24.41	28.56	28.61	24.41	29.41	29.41
8	25.55	28.56	28.61	25.55	29.41	29.74
9	26.63	30.65	30.91	26.63	31.94	31.95
10	27.61	30.65	30.91	27.61	32.09	32.09
11	27.98	33.08	33.08	27.98	33.15	33.15
12	28.82	33.08	33.08	28.82	34.43	34.43

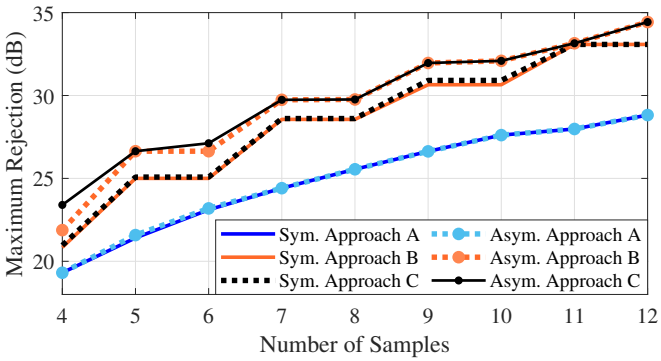


Figure 2.39.: Maximum rejection as a function of the number of samples and the followed approach for a 499.2 MHz IEEE Channel (T_E = 3.5 ns).

worth highlighting that the greater the number of samples, the greater the number of degrees of freedom. Moreover, this Table suggests that asymmetrical arbitrary envelopes can achieve higher rejection than symmetrical arbitrary envelopes for approaches B and C. However, for approach A, the asymmetry could not provide higher rejection despite the greater number of degrees of freedom (an asymmetric envelope involves twice as many parameters to optimize compared to a symmetric envelope).

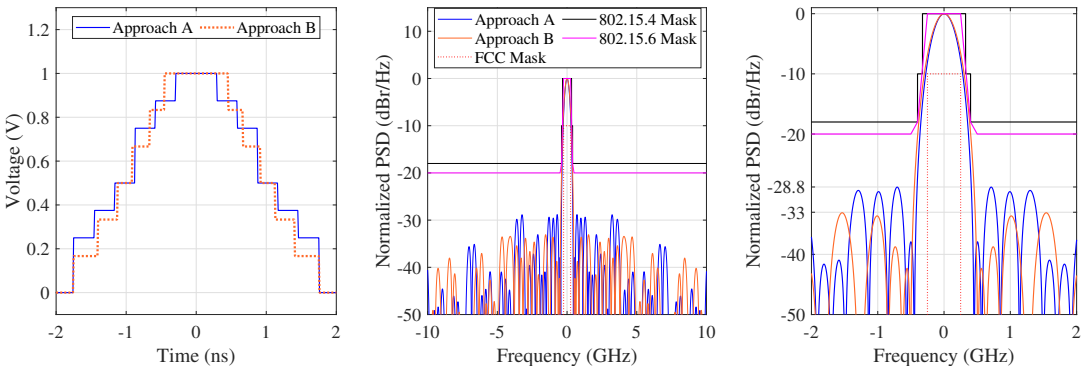
For two consecutive numbers of samples having the same value of rounded half N (for example 7 and 8), the difference between the maximum achieved rejection can be small, regarding approaches B and C. The reason for this is that for two consecutive values of N, where even N is greater, the shapes of the envelope can be strongly alike. They cannot be distinguishable in terms of N. For instance, for $N = 7$, the fourth sample can correspond to the combination of the fourth and fifth samples for $N = 8$. In other words, these samples present the same amplitude and duration.

Between approaches A and B, the second one can reach a higher rejection. The greater the number of samples, the greater the difference between the maximum rejection of these approaches. For instance, Figure 2.40 shows optimal symmetrical envelopes obtained using the approach A and B for $N = 12$ addressing a 499.2 MHz IEEE MHz channel. The duration and amplitude associated with each sample are displayed in Table 2.7.

From Figure 2.40, it can be observed that the envelope spectra fit into the IEEE standards

Table 2.7.: Duration and amplitude of uniform and non-uniform sampled envelopes for a 499.2 MHz IEEE Channel and $N = 12$ (T_E = 3.5 ns, approach A and B)

	n	1 and 12	2 and 11	3 and 10	4 and 9	5 and 8	6 and 7
Approach A	ρ_n	0.083	0.083	0.083	0.083	0.083	0.083
	τ_n (ns)	0.29	0.29	0.29	0.29	0.29	0.29
	a_n (V)	0.25	0.375	0.5	0.75	0.875	1.0
Approach B	ρ_n	0.1	0.08	0.06	0.07	0.06	0.13
	τ_n (ns)	0.35	0.28	0.21	0.245	0.21	0.455
	a_n (V)	0.167	0.333	0.5	0.667	0.833	1.0



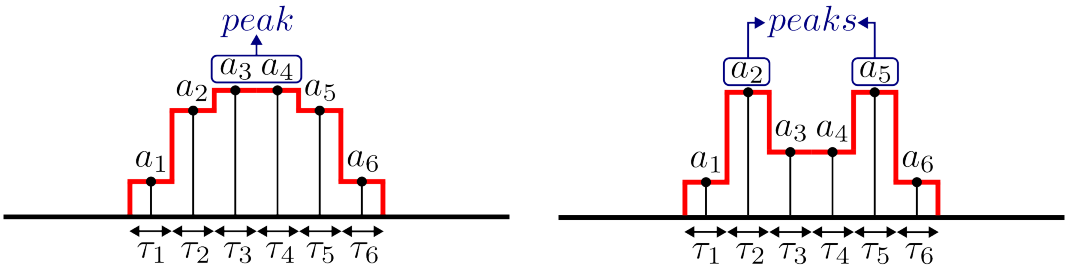
(a) Waveform (b) Spectrum (c) Spectrum (Zoomed)

Figure 2.40.: Uniform and Non-uniform sampled symmetrical envelopes optimal in terms of side-lobe rejection for a 499.2 MHz IEEE channel and N = 12 (T_E = 3.5 ns, approach A and B).

masks, in addition to comply with the minimal BW_{-10dB} of 500 MHz imposed by FCC.

There is little difference in the maximum rejection between approaches B and C. This suggests that between these approaches, approach B is more efficient given its lower number of degrees of freedom. The lower the degrees of freedom is, the lower the complexity of the envelope generator architecture is. Therefore, it is more efficient to optimize only the sample durations.

Although approach C enables a fully arbitrary sample and hold envelope, approach B can also obtain the envelope shapes that optimize side-lobe rejection. For instance, approach B can only obtain envelope shapes with one positive peak (Fig. 2.41a), while approach C can produce envelope shapes with more than one positive peak (Fig. 2.41b). However, it appears that envelope shapes with a single peak are better suited for optimizing side-lobe rejection.



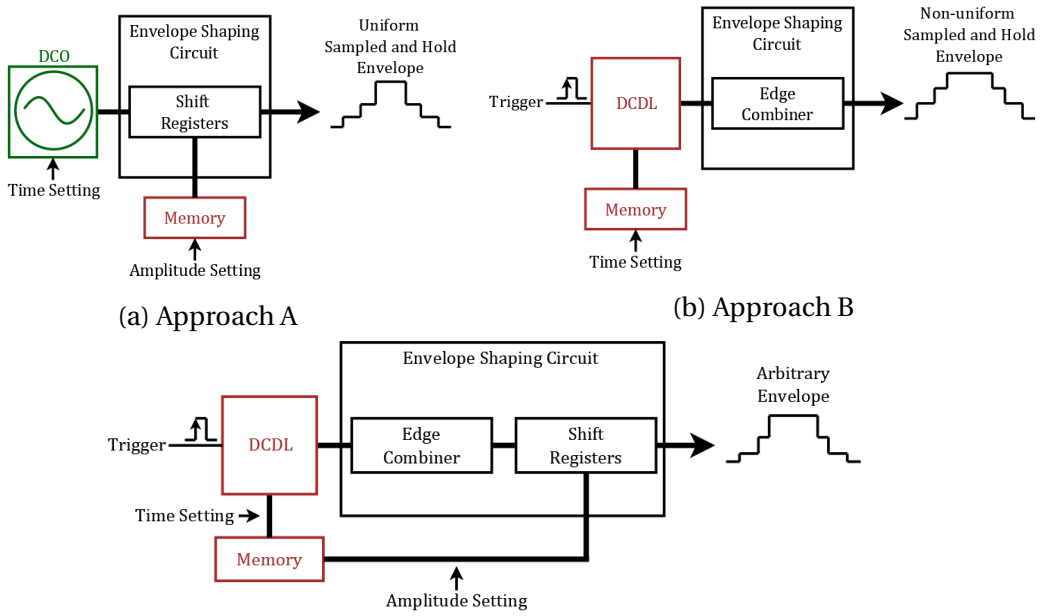
(a) Single positive peak. (b) Multiple positive peaks.

Figure 2.41.: Examples of sample and hold envelopes.

Figure 2.42 displays proposed architectures for the implementation of each sample and hold envelope approach. All architectures present only digital circuits. Concerning approach A, the envelope shaping circuit can be mainly composed of shift registers. The sample amplitude tuning is performed through a memory, whereas the sample duration is controlled by a Digitally Controlled Oscillator (DCO). Concerning approach B, the envelope shaping circuit can be

composed of an edge combiner. The sample duration is controlled by a memory followed by a Digitally Controlled delay line (DCDL). The sample amplitude is controlled by a further circuit. Finally, concerning approach C, the envelope shaping circuit can be composed of an edge combiner and shift registers. The architecture of Figure 2.42c encompasses the architecture of Figures 2.42a and 2.42b. The memory stores the data relative to sample amplitude and duration.

From an electrical point of view, the architecture of 2.42c is the most complex. Indeed, there are more blocks and more data to store in the memory. However, as observed earlier, approach B is more efficient than approach C. Hence, the architecture of Figure 2.42b is more suitable because of its greater simplicity. The time setting is critical to address all the IEEE 802.15.4 and 802.15.6 standard channels, mostly because the IEEE 802.15.4 standard has some channels whose bandwidth BW is greater than 1000 MHz.



(a) Approach A

(b) Approach B

(c) Approach C

Figure 2.42.: Proposed architectures for implementation of sample and hold approaches.

2.5. Conclusion

This chapter presents the modeling and characterization of continuous envelopes and sample and hold envelopes. The continuous envelopes addressed are rectangular, symmetrical triangular, asymmetrical triangular, symmetrical trapezoidal, and asymmetrical trapezoidal. Two study cases have been addressed: one where no UWB spectral requirements are considered, and another one where spectral requirements imposed by FCC and IEEE 802.15.4 and IEEE 802.15.6 standards are considered.

Concerning the first study case, the different considered shapes can be obtained by tuning two parameters: the symmetry factor α and the surface factor β. It can be noted that the pulse energy increases linearly with the envelope width and the surface factor. However, the symmetry factor does not influence the pulse energy since α does not change the envelope surface. Thus, from Table 2.3, the saw-tooth envelope presents the highest side-lobe rejection but presents the weakest pulse energy since the triangular envelopes have the lowest surface factor β. For a fixed envelope width, the surface factor should also be increased to increase the energy, which reduces the side-lobe rejection.

Concerning the second study case, the envelope width, symmetry, and surface factors are subjected to the spectral constraints imposed by FCC, IEEE 802.15.4, and IEEE 802.15.6 and the minimum 10 dB bandwidth of 500 MHz imposed by FCC delimits the maximum value of pulses width. On the other hand, the IEEE spectral masks delimit the minimum value of pulses width. Thus, there is a limited available range of symmetry and surface factors associated with a single value of pulse width. From Table 2.4, the asymmetrical trapezoidal envelope achieved the greatest side-lobe rejection (37.1 dB).

Since continuous envelope generation is not easy from the electronic point of view, an approximation of the continuous envelope by a sample and hold envelope which can be generated using a digital architecture is proposed. When the envelopes are uniformly sampled from the continuous ones, aliasing degrades the side-lobe rejection. However, aliasing degrades less the side-lobe rejection when the sampling frequency is higher, or in other words, when the number of samples is higher. To approximately achieve the same level of side-lobe rejection of a continuous envelope, the number of samples should be high enough. Indeed, the higher the required number of samples is, the greater the rejection level of side-lobe is.

Further, a sample and hold envelope optimization is presented. Three approaches were addressed: uniform sample and hold (A), non-uniform sample and hold (B), and fully arbitrary (C) (Fig. 2.38). Approach B can reach higher side-lobes rejection having fewer degrees of freedom, being the most efficient. This enables a less complex architecture. Therefore, it is more efficient to optimize the sample durations rather than the sample amplitudes.

In addition, a sample and hold with a minimum of 8 samples is required to achieve a good side-lobe rejection, providing a sufficient margin to cover the IEEE channels and respecting the spectral requirements imposed by FCC. Regarding the timing specifications of the sample and hold envelope with 8 samples, the sample duration range is from 100 ps to 700 ps to address the IEEE channels. Specifically, the sample duration should range from 300 ps to 700 ps to address the 499.2 MHz IEEE channels. On the other hand, the sample duration should range from 100 ps to 300 ps to cover the large-bandwidth IEEE channels (1081 MHz, 1331 MHz, and 1355 MHz).

3. IR-UWB Transmitters Literature Survey

Summary

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3.1. Introduction

From the previous chapter, the IR-UWB pulse envelope shaping is important to ensure that the generated pulse complies with spectral masks established by FCC and IEEE standards. These spectral masks restrict the pulse bandwidth in addition to imposing a minimal adjacent rejection of 18 dB (IEEE 802.15.4) and 20 dB (IEEE 802.15.6). To control the pulse envelope, reported works in literature often propose a pulse synthesizer as IR-UWB transmitter compatible with IEEE. It is more interesting than a pulse generator since this typically generates a signal with fixed parameters. To address the IEEE channels in the FCC band (3.1-10.6 GHz), it is necessary to control some parameters, mostly the pulse central frequency and bandwidth. Thus, it is hence essential to design a multi-band and multi-standard pulse synthesizer capable of covering the FCC band.

In the literature, two main pulse synthesis methods are reported: the pulse direct synthesis and the frequency transposition pulse synthesis. Considering the first method, the pulse is directly synthesized within the targeted frequency band employing a delay line such as a Voltage-Controlled Delay Line (VCDL) [48]. On the other hand, considering the second method, the pulse is a baseband pulse transposed to the targeted frequency by modulating oscillations coming from an oscillator such as a Voltage-Controlled Oscillator (VCO) whose architecture can be based on an LC-tank or a ring oscillator [13].

This chapter is divided into four parts. First, the multi-standard IR-UWB transmitter design metrics and comparison criteria are introduced. Second, IR-UWB transmitter based on direct pulse synthesis is presented. Third, IR-UWB transmitter based on frequency transposition synthesis is presented. Last, a comparison with the state-of-the-art IR-UWB transmitters is addressed.

3.2. Metrics and comparison criteria

Concerning the multi-standard IR-UWB transmitters design, its main metrics are given below:

- Central frequency (F_c) range
- Pulse bandwidth (BW_{-XdB}) range
- Side-lobe rejection
- Number of IEEE 802.15.4 standard channels addressed
- Number of IEEE 802.15.6 standard channels addressed
- Pulse maximum magnitude
- Emitted Energy (E_p)
- Dynamic Energy (E_{ac})
- Static Power (P_{0Hz})
- PRF range
- Power consumption in relation to PRF

This survey prioritizes the central frequency range, pulse bandwidth range, and side-lobe rejection, which are relevant to the multi-standard design. The number of IEEE standard channels addressed depends on these metrics. It is worth pointing out that some of these channels are mandatory, where these have a bandwidth of 499.2 MHz.

The comparison criteria of the IR-UWB transmitters are the modulation scheme and spectral compliance (FCC, ETSI). For every reported work, it is evaluated if the addressed pulses comply with the IEEE spectral masks and with the 500 MHz minimal bandwidth imposed by FCC.

Besides, to compare the IR-UWB transmitters, spectral efficiency for an attenuation of 10 dB is proposed as a criterion. To clarify, figure 3.1 shows the spectral efficiency estimation principle. The spectral efficiency is defined as the ratio between the surface occupied by the spectrum (red-hatched gray) and the available surface (gray). The spectral efficiency (SF_{-10dB}) can be expressed as follows:

$$SF_{-10dB} = \frac{E_{p\,-10dB}}{BW_{-10dB} \cdot 0.9 PSD_{peak}} \tag{3.1}$$

where $E_{p\,-10dB}$ is the pulse energy confined in a -10 dB bandwidth (occupied surface of Figure 3.1). The available surface is delimited by an attenuation of 10 dB and a -10 dB bandwidth of reference. For instance, it can be used the specifications of the IEEE 802.15.4 standard spectral masks. Despite Figure 3.1 has a logarithmic scale, the SF_{-10dB} expression should be calculated using a linear scale. The expression $0.9PSD_{peak}$ corresponds to the height of the gray rectangle displayed in Figure 3.1 in linear scale. To clarify, a short mathematical demonstration is given as follows :

$$10log\left(\frac{PSD_{peak}}{PSD_{-10dB}}\right) = 10dB \Leftrightarrow PSD_{peak} = 10PSD_{-10dB} \tag{3.2}$$

$$PSD_{peak} - PSD_{-10dB} = 0.9PSD_{peak} \tag{3.3}$$

where PSD_{-10dB} corresponds to the PSD with an attenuation of 10 dB. Besides, the pulse energy $E_{p\,-10dB}$ can be estimated using a technique for numerical integration such as the trapezoid rule [49]. In this literature survey, the spectrum data are obtained using WebPlot-

Digitizer, which is an assisted software capable of extracting numerical data from images [50].

In this thesis work, there is a condition to estimate the spectrum efficiency using the expression (3.1): the spectrum must fit into the IEEE radio-frequency masks. In addition, it is worth highlighting that for a specific IEEE channel, a higher spectral efficiency enables a more accurate real-time location and an increased data transmission rate.

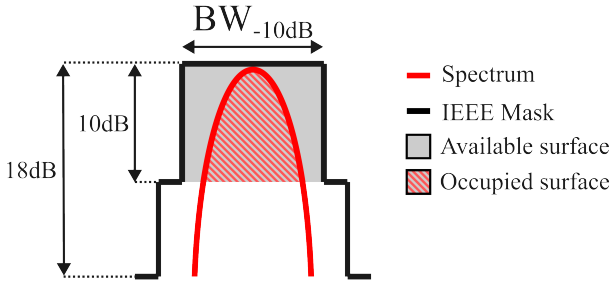


Figure 3.1.: Spectral efficiency estimation principle

3.3. Direct pulse synthesis

The first pulse synthesis method approached in this chapter is direct pulse synthesis, which is performed with a circuit composed of delay cells. Local oscillators are not employed. The IR-UWB pulse is generated directly in the targeted frequency using voltage-controlled delay cells (baseband pulse generator) and an edge combiner (baseband pulse combiner), as indicated in Figure 3.2 [21].

For instance, Figure 3.3 shows an IR-UWB emitter based on direct pulse synthesis reported in [21]. A set of delay cells, tuned by voltages, generates time-shifted baseband pulses, which are combined in an edge combiner circuit. This architecture is capable of generating pulses with arbitrary shapes. A larger number of delay cells can improve the pulse shaping capability. However, it becomes increasingly difficult to maintain a uniform behavior of delay cells, and more complex to design a pulse combiner circuit [21]. There will be a higher influence from parasitic capacitance, which impacts the central frequency range. The minimum delay delimits the highest central frequency, whereas the maximum delay delimits the lowest central frequency. In addition, the narrower the targeted channel and the higher the central frequency, the higher the required number of delay cells is. To clarify, a narrower channel implies a longer pulse, which requires more delay cells. Likewise, considering the same pulse width, a higher central frequency implies a larger number of delay cells with a smaller delay. Therefore, this pulse synthesis method is commonly used for a frequency bandwidth greater than 1 GHz, targeting a central frequency below 5 GHz.

In particular, in [21], it is reported an IR-UWB transceiver implemented in a 130 nm bulk CMOS technology for WBAN applications within the 3.1-4.9 GHz frequency band. The transmitter design is based on a pulse synthesizer based on an architecture composed of a delay line (baseband pulse generator) and baseband combiner (Fig. 3.3). This transmitter can tune

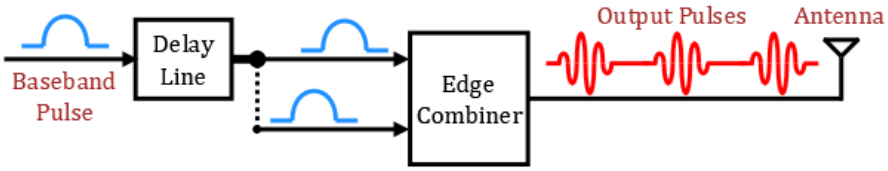


Figure 3.2.: Pulse direct synthesis principle

the amplitude and duration of the generated baseband pulses. Figures 3.4a and 3.4b display baseband pulse generator and baseband pulses combiner architecture, respectively.

The baseband pulse generator comprises two parts: a VCDL and a fast logic stage. Concerning the first part of the baseband pulse generator, the VCDL is a delay line where a rising edge signal is propagated through adjustable delay cells. These delay cells are composed of two buffered stages whose architecture is based on CMOS logic inverters loaded by a capacitor (D-C1) in series with an NMOS transistor that implements an analog switch, such that it is possible to achieve a wide delay tuning range. Each baseband pulse duration depends mainly on the propagation delay of the different stages of VCDL.

The baseband pulse combiner architecture is based on 8 H-bridges paths going into the load (Fig. 3.4b), where each H-bridge path design was done implementing transmission gates (S-M1 and S-M2 of Figure 3.4b). The combined baseband pulse amplitude is controlled through different control voltages (Va-n) applied at each H-bridge path. This IR-UWB transceiver can perform OOK modulation and Delay-Based Binary Phase-Shift Keying (DB-BPSK) modulation. Besides, this transceiver presents a side-lobe rejection of 18 dB, which is enough to comply with IEEE 802.15.4 standard masks. It can generate pulses with a larger bandwidth, more than 1 GHz, addressing channel 4 of the IEEE 802.15.4 standard. The transceiver of [21] has a dynamic energy consumption of 146 pJ/pulse and a static power of 100 µW.

Regarding the multi-standard design, the circuit of [21] proposes the implementation of VCDL combined with 8 H-bridges. This circuit is unsuitable because of its limited frequency tuning range and inability to address the 499.2 MHz IEEE channels. This inability can be attributed to the restricted bandwidth range. Moreover, the reported side-lobe rejection (18

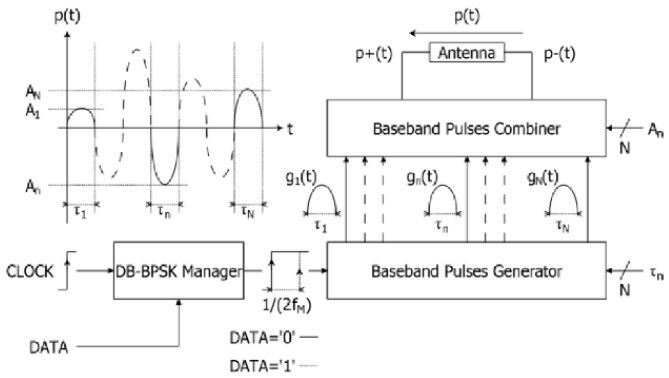
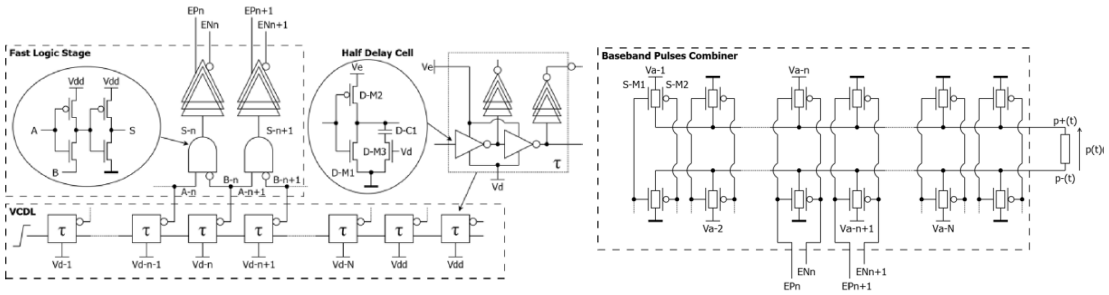


Figure 3.3.: Reported IR-UWB emitter global architecture based on pulse direct synthesis [21].



(a) Baseband pulses generator. (b) Baseband pulse combiner.

Figure 3.4.: Design of IR-UWB emitter based pulse direct synthesis [21].

dB) is compliant with the IEEE 802.15.4 standard but not with the IEEE 802.15.6. The spectral efficiency is not estimated because the reported IR-UWB pulses do not fit into IEEE spectral masks.

An IR-UWB transmitter front-end in 65 nm bulk CMOS technology for energy-harvesting devices, with pulse shaping capabilities and integrated output matching network, is reported in [51]. This IR-UWB transmitter can generate signals with a central frequency between 6 GHz and 8.5 GHz. Its architecture is displayed in Figure 3.5. It requires lots of delay cells, as expected (32 delay cells). The main blocks of this transmitter are delay cells (δ), routers (R), combiners (C), a Power Amplifier (PA), and a matching network (MN). Figure 3.6 shows the delay cell, router, and combiner designs. The delay line, composed of 32 delay cells, generates a pulse whose central frequency is controlled by the propagation delay t_Δ, such that:

$$f_c = \frac{1}{t_\Delta} \tag{3.4}$$

This delay is digitally controlled using a 9-bit word. Each delay cell generates an impulse at router input. Next, the routers propagate the input to up to 4 parallel outputs based on a 4-bit tuning word. The generated signals from routers are then combined into the combiners, and finally, the combined pulses are sent to the PA and the matching network.

The main advantage of this architecture is that it requires only one PA instead of 32 sub-PAs. However, addressing low bandwidth channels implies a larger number of delay cells, as explained earlier, which increases the complexity of the pulse combiner circuit layout due to larger parasitic capacitances, in addition to the impact on the central frequency range itself. Nevertheless, this transmitter presents a high side-lobes rejection (30 dB), better than [21].

The transmitter of [51] can generate pulses addressing 4 low bandwidth channels (499.2 MHz) of the IEEE 802.15.4 standard. One of them is the mandatory channel 8. Nevertheless, it cannot generate pulses addressing the large-bandwidth IEEE channels. From [51], the estimated spectral efficiency is from 49.4% to 55.5%. The generated pulses have an amplitude of 0.46 Vpp and an emitted pulse energy of 0.83 pJ. Finally, the transmitter of [51] presents a dynamic energy consumption of 63 pJ/pulse and a static power of 0.38 µW.

The transmitter of [51] is a good choice for a design targeting the ETSI band (6-8.5 GHz). It covers the IEEE channels in this frequency band and achieves a great side-lobe rejection. In addition, it presents a good spectral efficiency for the 499.2 MHz IEEE channels. The great

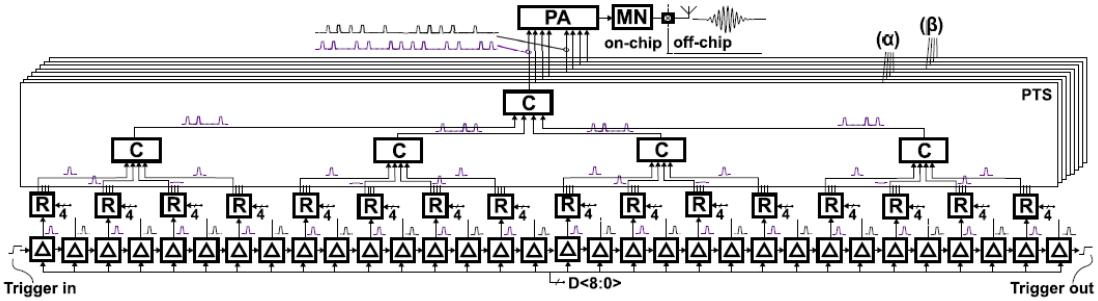
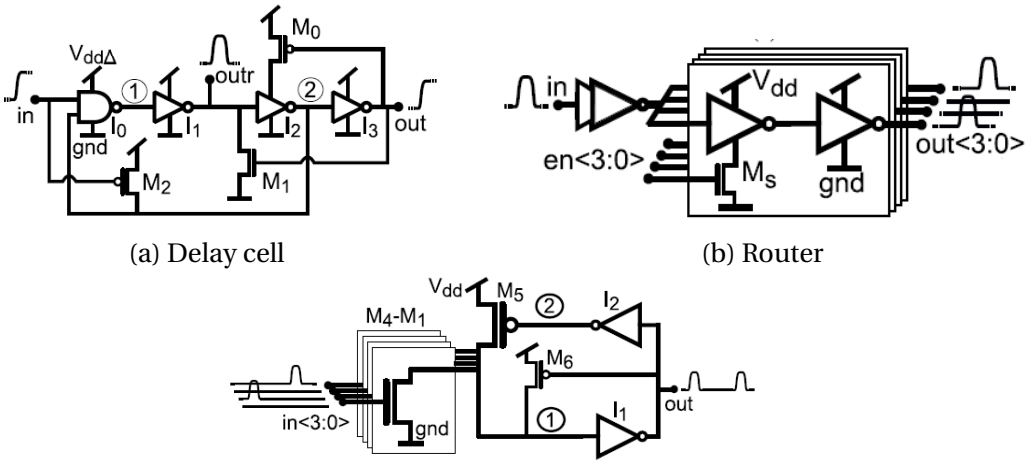


Figure 3.5.: Transmitter front-end architecture based on a delay line [51].



(a) Delay cell

(b) Router

(c) Combiner

Figure 3.6.: Impulse propagation blocks schematics [51].

side-lobe rejection can be attributed to the delay line and recombination circuit. The 32 delay cells enable effective envelope reprogramming. Nevertheless, a disadvantage of using 32 delay cells is the incapacity of generating a pulse short enough to address large-bandwidth IEEE channels. Consequently, the transmitter of [51] has a limited pulse bandwidth.

Regarding the FCC band, this transmitter offers a limited oscillation frequency tuning range. A solution to improve this is, according to expression 3.4, to improve the delay cell tuning range.

Finally, in [52], a UWB pulse transmitter in 65 nm bulk CMOS based on a programmable delay line cell is reported. Its schematic is shown in Figure 3.7. The transmitter of Figure 3.7 can program digitally the amplitude and duration of every UWB pulse, which makes feasible a flexible shaping of the pulse spectrum. This UWB transmitter architecture is mainly based on 10 programmable delay cells in cascade that are capable of generating signals whose bandwidth is greater than 1 GHz.

The delay cell (Fig. 3.8) controls the duration of each cycle of the UWB pulse, where the delays are configured separately. The total number of cycles is 10. The delay cell of Figure 3.8 presents a 3-bit programmable delay cell between input and output, where the delay time

value results from MOS capacitor discharge rate control done by three digitally controlled binary weighted parallel branches. Therefore, the MOS capacitor is charged at a fixed rate through the p-channel MOS transistor when the inverter circuit comes back to its initial state. The interesting feature of this delay control mechanism is an approximate linear dependency of frequency on the delay control numbers.

The transmitter of [52] is capable of generating UWB signal with a central frequency within 3.6-7.5 GHz with an output voltage of 1 Vpp, an emitted energy of 2.4 pJ, and a side-lobe rejection of 23.8 dB. This transmitter can generate pulses addressing 2 high bandwidth channels of the IEEE 802.15.4 standard. The transmitter of [52] presents an energy consumption of 8.5 pJ/pulse and a power static of 13 µW.

The transmitter of [52] presents a quite good oscillation frequency range, better than [21, 51] because of the 3-bit programmable delay cell that has better delay tuning range. Nevertheless, the delay tuning has a low precision, making it difficult to generate the correct pulse central frequency to address the IEEE channels properly In addition, the circuit of [52] is incapable of addressing 499.2 MHz IEEE channels, similar to [21]. Therefore, this circuit is not a good candidate for multi-standard design.

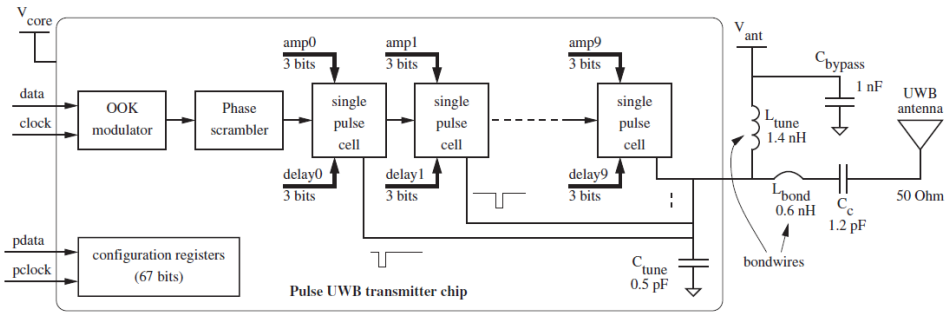


Figure 3.7.: Block diagram of the reported UWB pulse transmitter architecture [52].

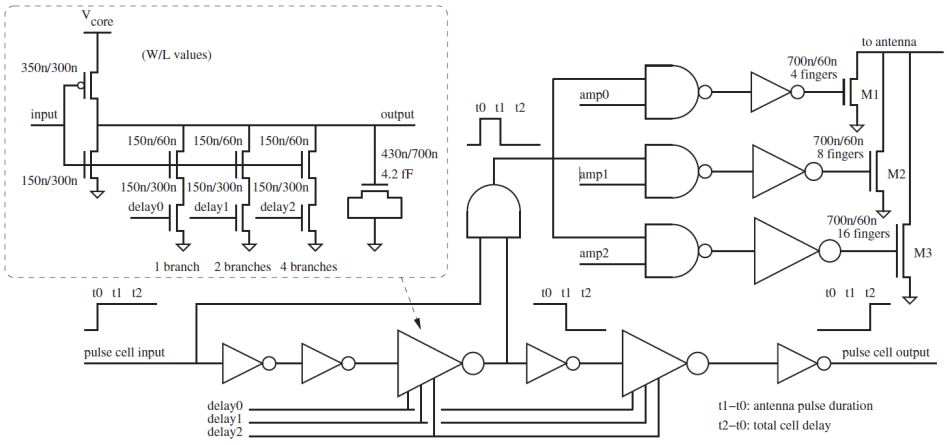


Figure 3.8.: Schematic of the programmable delay line cell [52].

From the presented IR-UWB transmitters based on direct pulse synthesis, the architecture of the delay line and edge combiner have a central frequency range strongly dependent on the delay cell tuning capabilities. This enables a central frequency range high enough to cover

either the low band or the high band of the IEEE standard. Consequently, this frequency range is not enough to cover entirely the FCC band (3.1-10.6 GHz).

Besides, it follows that the delay line architecture has limitations in terms of bandwidth tuning range. For instance, the transmitter of [51] is the only one able to address the narrowest IEEE channels (499 MHz) since [51] has implemented a large number of delay cells (32). On the other hand, [21] and [52] can only address large-bandwidth IEEE channels. The pulse bandwidth range depends on the number of implemented delay cells.

A disadvantage of these transmitters' architecture is that modifying the number of delay cells is not enough to deal with the inability to cover a good pulse bandwidth range (499.2-1355 MHz). An alternative is a programmable edge combiner which is capable of combining a different number of delayed edges according to the target pulse bandwidth. However, this will complicate the recombination of delayed edges even further. Therefore, an IR-UWB transmitter based on direct synthesis appears unsuitable for the multi-standard design covering the FCC band.

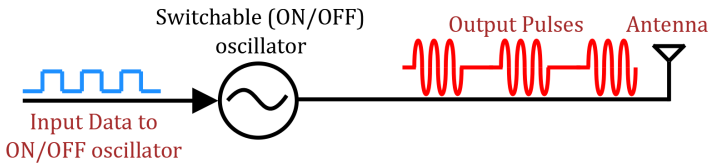
3.4. Frequency transposition pulse synthesis

Concerning the second pulse synthesis method approached in this chapter, the frequency transposition pulse synthesis requires a local oscillator, which must generate oscillations with the targeted central frequency. For instance, a modulated oscillator (switchable on-off) can generate a pulse with a rectangular envelope, as indicated in Figure 3.9a. In this case, the oscillator is called a gated oscillator. A baseband signal can be employed to perform a OOK modulation. However, Chapter 2 has shown that the rectangular IR-UWB pulse does not satisfy simultaneously the minimum 10 dB bandwidth of 500 MHz imposed by FCC and the IEEE minimal side-lobes rejection. Thereby, these oscillations generated by the oscillator must be modulated by a baseband pulse whose envelope depends on the targeted spectral mask, as shown in Figure 3.9b. This synthesis technique hence requires a pulse shaping circuit able to apply on the oscillations an envelope compliant with FCC and IEEE standards spectral requirements.

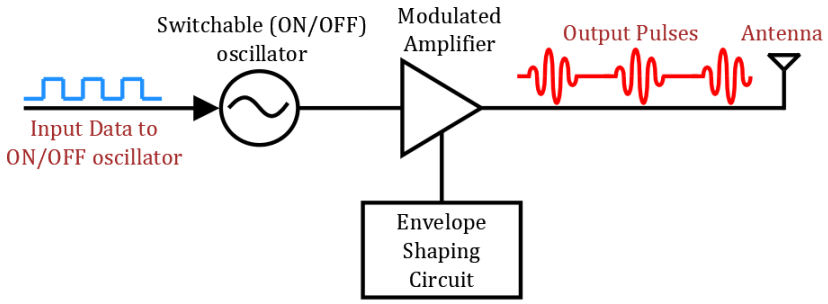
Since a modulated oscillator is used, this synthesis method is capable of offering better tuning of the pulse frequency bandwidth [13, 53–55]. To realize a frequency transposition pulse synthesis, among reported strategies, one consists of employing mixers [47, 56, 57]. However, to reach 499.2 MHz bandwidth or higher as expected for channels 4 (1331 MHz), 7 (1081 MHz), 11 (1331 MHz), and 15 (1355 MHz) of the IEEE 802.15.4, the bandwidth of the mixing circuit shall be very large which generally increases the circuit complexity and the power consumption [57].

Alternatively, to avoid the use of a mixing circuit, another strategy consists of modulating the VCO, leading to the so-called gated VCO [58, 59]. The oscillator settling time and the extinction time, in addition to the start and stop signal shape, are then critical to cover channels that require pulses having a duration of some nanoseconds. From the literature, the VCO architectures are often based on an LC-tank oscillator [60–63] or a ring oscillator [64–69].

In particular, in [54, 55], it is reported IR-UWB digital transmitter with a reconfigurable pulse shaping, whose architecture is shown in Figure 3.10. It has been implemented using 28 nm



(a) Based on gated oscillator



(b) Based on gated oscillator and shaping circuit

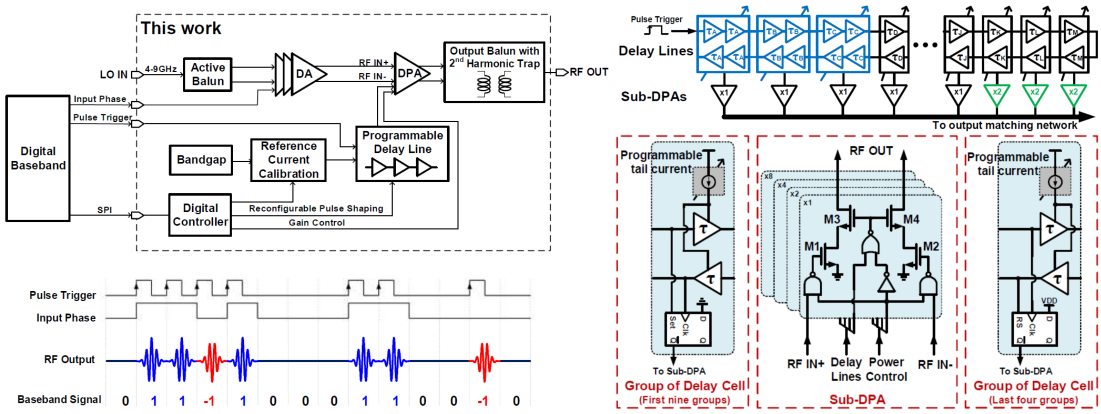
Figure 3.9.: Frequency transposition pulse synthesis principle

bulk CMOS technology. The proposed reconfigurable pulse shaping exploits a programmable delay line, as depicted in Figure 3.11. It seeks to achieve high spectral efficiency and significant side-lobe suppression. From Figure 3.10, the reported IR-UWB digital transmitter design is based on a Digital Power Amplifier (DPA) and a programmable delay line, with an external VCO. A digital baseband provides a pulse trigger and an input phase signal that performs a BPSK modulation. An external VCO generates the oscillation between 4 and 9 GHz, which drives an active balun. This balun generates differential oscillation signals. A multi-stage Driving Amplifier (DA) realizes an up-conversion of the baseband input phase to the carrier frequency. The differential DPA combines the RF carrier with the baseband signals generated by the delay line. In other words, the DPA up-converts the delay line output signal.

The programmable delay line presented in Figure 3.10b enables control of the pulse envelope. Hence, the proposed delay line can be defined as a Digitally Controlled delay line (DCDL). It has an independent delay-time control for each delay cell to obtain a reconfigurable pulse template, as pointed out in Figure 3.11a. Therefore, the envelope pointed out in Figure 3.11a can be defined as a non-uniform sample and hold. The strategy of [54, 55] is to generate a UWB pulse with a step delay time programmable targeting to achieve higher side-lobe rejection than the one from UWB pulse with a delay time constant (uniform sample and hold).

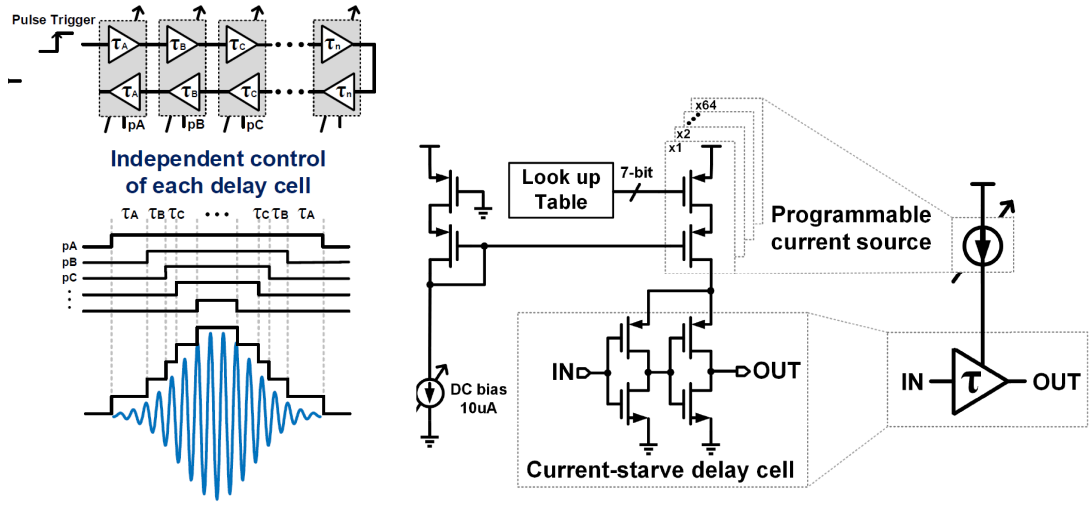
The proposed delay line is composed of 26 current-starve delay cells. As shown in Figure 3.10b, two delay cells drive D flip-flops, generating a control signal for the sub-DPAs. The control signals (pA, pB, pC, etc.) are indicated in Figure 3.11a. Besides, the set of D flip-flops can be seen as an edge combiner. The outputs of the D flip-flops are combined to drive a single sub-DPAs such that a symmetrical pulse is achieved. From Figure 3.11b, a programmable current source can tune the delay time of a current-starved delay cell. The delay time digital control is performed by a 7-bit word supplied by a Look-Up Table (LUT). The pulse width can

be controlled to be between 1.2 and 6 ns, thus covering the 499.2-1331 MHz signal bandwidth.



(a) IR-UWB transmitter architecture [54] (b) Schematic of delay-line and DPA [55]

Figure 3.10.: IR-UWB digital transmitter with external oscillator and reconfigurable pulse shaping [54, 55].



(a) Principle (b) Schematic of the programmable delay cell circuit

Figure 3.11.: Reconfigurable pulse shaping based on programmable delay lines [54].

The proposed IR-UWB transmitter achieves a frequency range of 4-9 GHz and a side-lobe rejection of 31 dB. It can generate pulses addressing 11 channels of the IEEE 802.15.4 standard, where of the 11 addressed channels, 3 have high bandwidth. The IR-UWB transmitter of [54, 55] can perform OOK modulation and BPSK modulation. From [54], the estimated spectral efficiency is from 44.2% to 55.5% for a channel bandwidth of 499.2 MHz, 47.9% for a channel bandwidth of 1081 MHz, and from 45.2% to 45.8% for a channel bandwidth of 1331 MHz. The generated pulses have an amplitude of 0.6 Vpp and an emitted pulse energy of 0.82 pJ. The transmitter of [54] presents an energy consumption of 660 pJ/pulse.

Regarding the multi-standard design, the circuit of [54] is a good candidate because of its good frequency tuning range and ability to address multi-band channels. It has a good pulse bandwidth tuning range and great side-lobe rejection thanks to the programmable delay lines that offer independent control of each delay cell. This control enables the pulse reconfiguration targeting different IEEE bands and standards. Therefore, a programmable delay line is a relevant choice for IR-UWB pulse shaping.

In [57], the reported IR-UWB transceiver has been implemented in 28 nm bulk CMOS technology. The transmitter design is based on a mixing stage and digital pulse shaper, as shown in Figure 3.12. Two Phase-Locked Loops (PLLs) (RFPLL and CLKPLL) generate local oscillator frequencies and clocks for the Digital-to-Analog Converter (DAC), respectively. Figure 3.13 presents the operating principle and circuit implementation of the IR-UWB pulse transmitter. In this work, a LUT is implemented to save all the possible output values. This enables the generation of a uniform sample and hold envelope of 12 samples. The pulse generation is pre-defined by a LUT rather than a real-time calculation, which can save significant power. The LUT is programmable, which enables a PVT variation compensation. The LUT output is a 32-bit word that is serialized at a 2 GHz clock rate to drive an 8-bit mixing DAC, which is introduced in [70].

The DAC cells design combines a 3-bit thermometer Most Significant Bit (MSB) and a 5-bit binary Least Significant Bit (LSB). Besides, the mixing DAC of Figure 3.12 has a sampling rate at 4 GHz and supports a signal bandwidth of up to 1355 MHz.

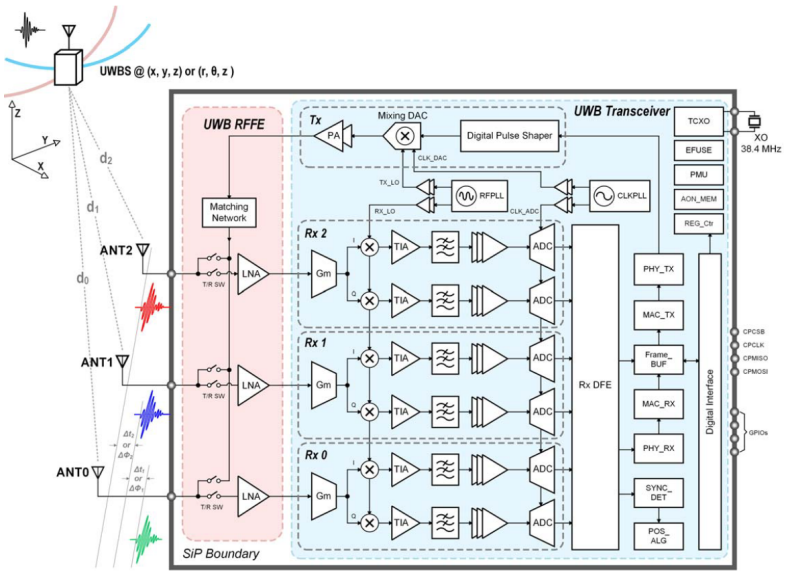


Figure 3.12.: IR-UWB transceiver architecture [57].

The transceiver of [57] covers a frequency range from 6.5 to 10 GHz with a programmable signal bandwidth of 499.2 MHz up to 1355 MHz. Hence, the proposed circuit can address the IEEE 802.15.4 channels 5 to 15, which are the high-band channels. From the transceiver of [57], the estimated spectral efficiency is from 40.2% to 61.6% for a channel bandwidth of 499 MHz and 46.5% for a channel bandwidth of 1081 MHz. It presents a side-lobe suppression of 25 dB,

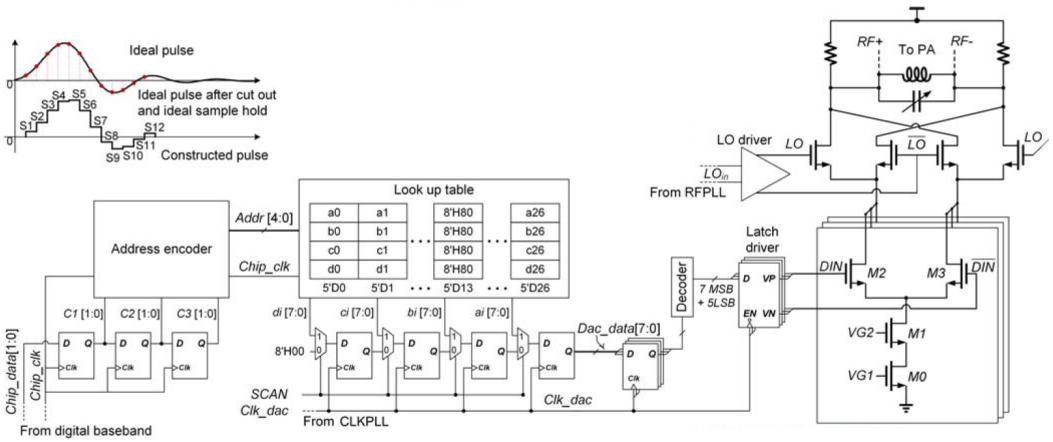


Figure 3.13.: The circuit implementation and operating principle of IR-UWB pulse generation [57].

which is reasonable. The transceiver of [57] presents an energy emission and consumption of 0.86 pJ/pulse and 3940 pJ/pulse, respectively.

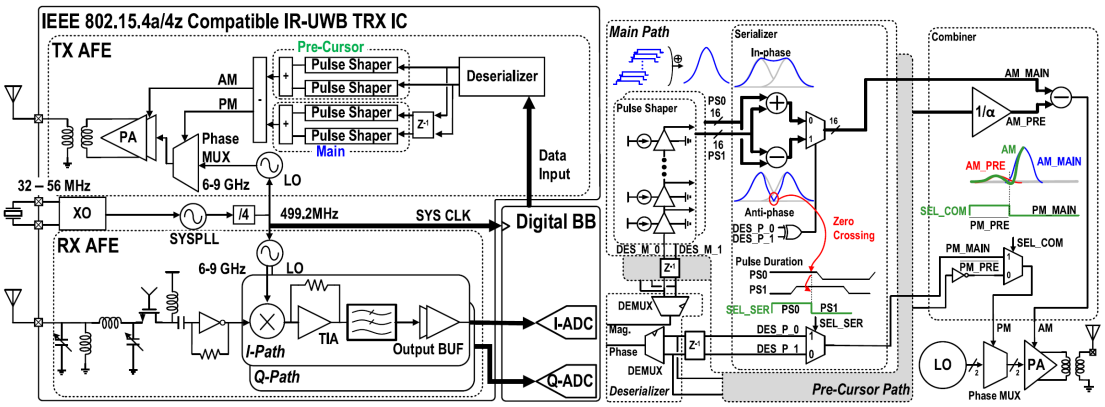
The circuit of [57] is a reasonable candidate for a multi-standard design because of its ability to address multi-band channels. It has a good pulse bandwidth tuning range as a result of the mixing circuit's large bandwidth and the generation of uniform sample and hold envelope composed of 12 samples. This last one is the main responsible for a reasonable side-lobe rejection. Nevertheless, the circuit described in [57] provides a limited frequency oscillation range, confined to the IEEE high-band channels (6.5-10 GHz). Besides, the cost of employing a mixing circuit with a large bandwidth is a significant increase in energy consumption. Therefore, for the architecture of [57], there is a trade-off between pulse bandwidth tuning range and power consumption.

Alternatively, to reduce the oscillator power consumption, one reported strategy is to power up and down the oscillator directly and control the oscillation start through a power management circuit. Turning on and turning off the oscillator during consecutive generated IR-UWB pulses can reduce the oscillator power consumption.

In [58, 59], it is reported a coherent IR-UWB transceiver with pulse pre-emphasis for high-precision ranging. Its architecture is depicted in Figure 3.14. It has been implemented using 28 nm bulk CMOS technology. Concerning the transmitter block (Fig. 3.14b), the pulse shaper exploits a programmable delay line, like [54, 55]. Moreover, a cascaded PLL topology with a crystal oscillator (XO) has been chosen to generate a 6-9 GHz local oscillator frequency for both transmitter and receiver blocks. A digital Deserialization-Serialization (DesSer) is implemented to reduce the Intersymbol Interference (ISI). A 2-bit word corresponding to the amplitude and phase code is deserialized into two parallel paths. This 2-bit word drives a pulse shaper, which is a controlled delay line composed of 16 delay cells. Hence, the pulse shaper provides 16 delayed pulses. These pulses combined form an approximated Hamming envelope, targeting the maximization of the spectrum occupation while respecting the UWB spectrum requirements, like the IEEE 802.15.4 standard. It follows that the proposed IR-UWB transmitter can generate a non-uniform sample and hold envelope with 16 samples. Finally,

the pulse shaper output pulses are serialized through a digital serializer. These pulses are either summed or subtracted according to the polarity supplied by the phase code.

The proposed IR-UWB transceiver achieves a frequency range of 6-9 GHz and a side-lobe rejection of 31 dB. Besides, it can generate pulses addressing 6 IEEE 802.15.4 channels having a bandwidth of 499.2 MHz. From the transceiver of [58, 59], the estimated spectral efficiency is from 49.8% to 51% for a channel bandwidth of 499.2 MHz. This transceiver generates pulses having an amplitude of 0.55 Vpp and an emitted energy of 0.836 pJ. Finally, the transmitter presents an average power consumption of 8.7 mW for a PRF of 124.8 MHz.



(a) Transceiver architecture (b) Transmitter block diagram

Figure 3.14.: IR-UWB transceiver for high-precision ranging [58, 59].

Regarding the multi-standard design, the transceiver of [58, 59] implemented a programmable delay line composed of 16 delay cells to obtain a great side-lobe suppression, similar to the transmitter of [54, 55]. As a result, this ratifies the programmable delay line as a good choice for the envelope shaping circuit. However, the circuit of [58, 59] presents a limited frequency oscillation tuning and an inability to address the 499.2 MHz IEEE channels. The reason for this inability is due to the deserializer single clock frequency (499.2 MHz), as indicated in Figure 3.14b.

3.4.1. Based on LC-tank oscillators

Concerning UWB transmitter design based on gated oscillators, some reported works in literature implemented an LC-tank oscillator. This oscillator is less susceptible to noise but consumes considerably more chip area compared to the ring oscillator [71].

In [61], it is reported pulse generator based on an oscillator composed of an LC resonator integrated into 180 nm CMOS technology (Figs. 3.15 and 3.16). A disadvantage of the LC-tank oscillator with power gating can be the long settling time. Nevertheless, the pulse generator of Figure 3.15 exploits this long settling time, controlling the LC oscillator start-up and shutdown. As a result, this enables a generation of a pulse with particular shapes, like triangular, for example, that is indicated in Figure 3.16. To address the target standardized channels, like IEEE 802.15.4, a bank of switched capacitors can be employed to control the oscillation's central

frequency along with varicap diodes that can be implemented to have a central frequency fine-tuning.

The pulse generator of [61] can achieve a frequency range of 3-5 GHz and a side-lobe rejection of 18 dB. The pulse generator can only address 3 IEEE 802.15.4 channels whose bandwidth is 499.2 MHz. From the measurement results presented in [61], the estimated spectral efficiency is from 53.1% to 54.3%. The pulse generator of Figure 3.15 can generate a pulse of 0.16 Vpp, which is the lowest among the reported transmitters. In addition, it presents a pulse emitted energy of 0.11 pJ. Finally, the pulse generator of [61] has an energy consumption of 16.8 pJ/pulse, a static power of 390 µW.

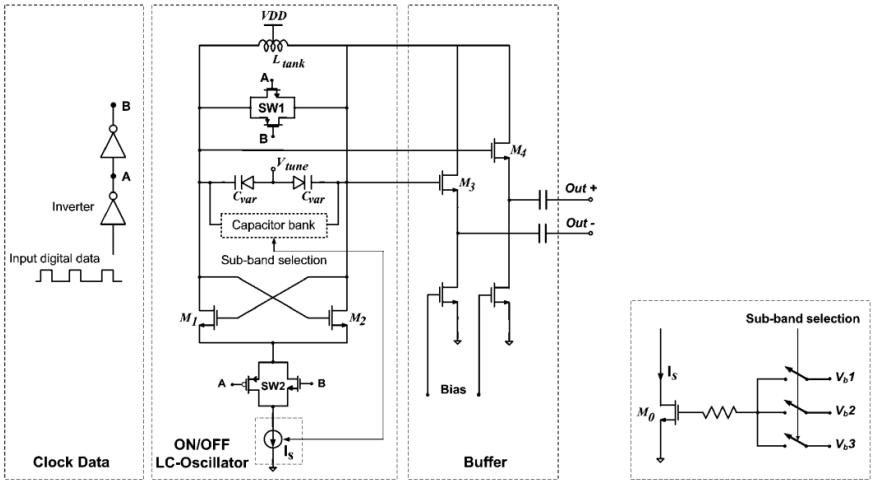


Figure 3.15.: Reported pulse generator based on LC-tank oscillator schematic [61].

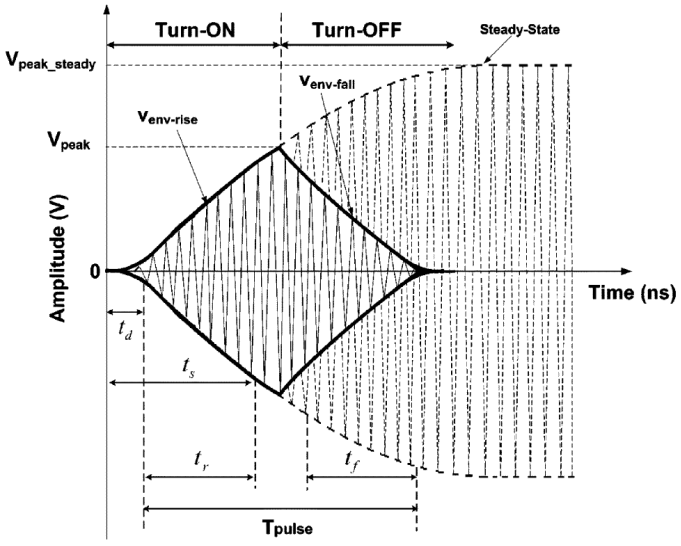


Figure 3.16.: Illustration of oscillator output waveforms. (Confined with solid line) Turn-on and turn-off transients. (Dashed part) Steady-state output [61].

Regarding the multi-standard design, the circuit of [61] proposes as novelty an ON/OFF LC oscillator with sub-band selection. This circuit is unsuitable because of its limited frequency oscillation range and inability to address large-bandwidth IEEE channels. The first can be attributed to the capacitor bank. The second can be attributed to the difficulty of the proposed circuit in generating ultra-short pulses (less than 3 ns). Therefore, to address the large-bandwidth IEEE channels, the LC oscillator settling time should be lower. Besides, this circuit achieves a weak side-lobe rejection, not complying with the IEEE 802.15.6 standard masks (20 dB required).

In [62], it is reported an IR-UWB transmitter front-end, which is powered by a radio frequency energy harvester (Fig.3.17). It has been designed in a 180 nm CMOS technology and seeks to comply with ETSI frequency masks (IEEE channels between 6 GHz and 8.5 GHz). The transmitter architecture is based on a duty-cycled cross-couple-pair LC oscillator (oscillator core) that generates a single pulse for every rising edge event at V_{trig} signal node. This transmitter enables the pulse bandwidth, central frequency, and amplitude to be tuned according to the targeted channel, in addition to compensating PVT variations.

The LC oscillator initializes with an initial voltage on the source-capacitor C_S, and it has a time delay of around 0.25 ns. The central frequency can be tuned between 5.98 GHz and 8.80 GHz using a 6-bit capacitors bank (C). This is a central frequency range larger than the one of the transmitter of [51]. The pulse duration can be controlled through the delay stage. This generates from the input signal V_{trig} two delayed control signals for the n-channel transistors M3 and M4. This delay and also the pulse duration are then controlled by a 6-bit capacitor bank (CBW). The pulse magnitude is controlled in the output stage using a programmable current source (bottom part) with a 4-bit gain control word. Finally, an external output balun is driven by a matching circuit controlled by a 6-bit bank capacitor (CMP). This tunes the generated pulse central frequency but with a lower influence than a 6-bit bank of switched capacitors (C).

The transmitter of [62] can address 4 IEEE channels having a bandwidth of 499.2 MHz and achieve a side-lobe rejection of 18 dB. From the results presented in [62], the estimated spectral efficiency is 48.2%. It presents an output amplitude of 1.0 Vpp, which is the highest among the reported works. Besides, it has a pulse emitted energy of 0.25 pJ. Finally, the transmitter of [62] presents an energy consumption of 6.2 pJ/pulse.

The transmitter of [62] implemented a cross-couple-pair LC oscillator with gain-control targeting the ETSI band. A 6-bit capacitor bank offers a good oscillation frequency covering the ETSI band. However, it presents an unsatisfactory performance because of its weak side-lobe rejection, which does not comply with the ETSI and IEEE 802.15.16 standard spectral requirements. Indeed, ETSI requires a minimum of 23.7 dB. Besides, this transmitter is not capable of addressing high bandwidth IEEE channels like the transmitter of [61]. Both cannot generate pulses short enough to have a large bandwidth.

In [63], it is reported an IR-UWB coherent transmitter that supports all IEEE 802.15.4 high-band channels, that are from 6.5 to 10 GHz. This transmitter is based on a PLL with dual LC Quadrature Voltage-Controlled Oscillator (QVCO) and a digital pulse shaping, as shown in Figure 3.18. It has been implemented in 28 nm bulk technology. It presents a BPSK modulation. The digital pulse shaping method exploits a configurable ring counter and parallel DPA stages.

From Figure 3.18a, the IR-UWB transmitter data and configuration are stored in registers

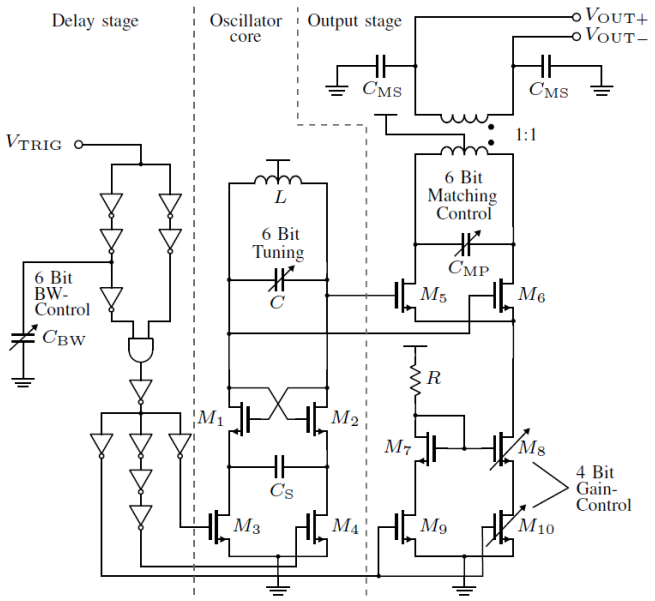
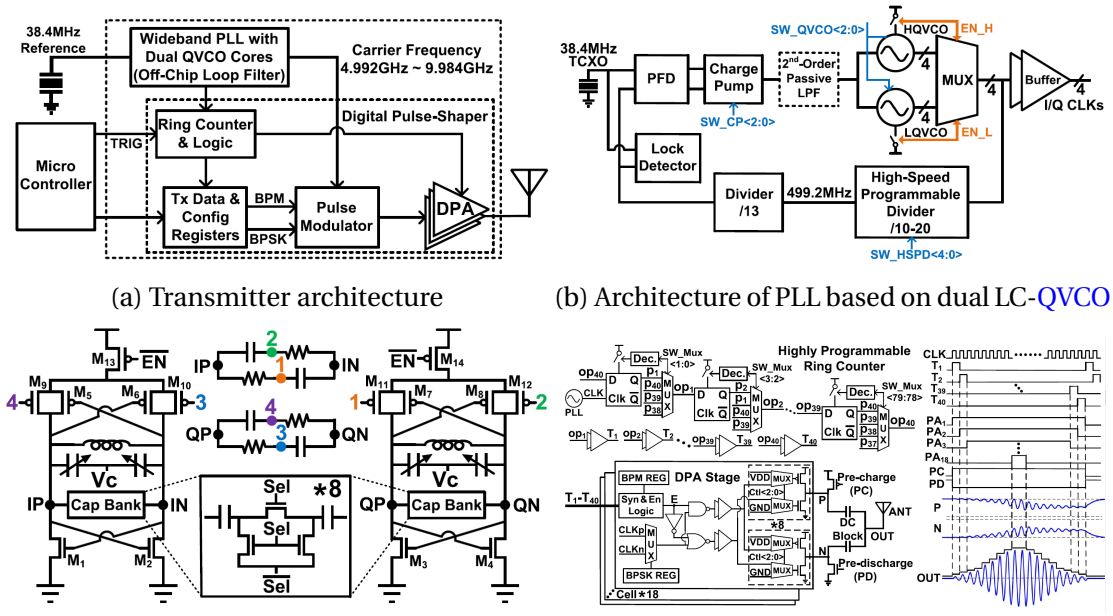


Figure 3.17.: IR-UWB transmitter architecture based on cross-couple-pair LC oscillator [62].

using a microcontroller. The register is loaded before the pulse generation. The PLL architecture is presented in Figure 3.18b. It generates a carrier frequency from 4992 MHz to 9984 MHz, with an external 38.4 MHz reference. Besides, the carrier frequencies provided by the PLL are integer multiples of 499.2 MHz from 10 to 20. The frequencies of 4992 MHz and 9984 MHz are multiple integers of 38.4 MHz. It is worth pointing out that all IEEE 802.15.4 standard channels have central frequencies, which are integer multiples of 38.4 MHz. The PLL is composed of two LC-QVCO, which schematic is displayed in Figure 3.18c. It supplies a continuous frequency range that covers the IEEE 802.15.4 high-band channels, in addition to providing a sufficient margin to compensate for PVT variations and modeling inaccuracies. The quadrature clocks are generated through a direct current coupling between two LC-QVCOs. The PLL output is applied, driving the ring counter and the pulse modulator.

Figure 3.18d displays the digital pulse shaping method. The symmetric ring counter is composed of 40 True Single-Phase-Clock (TPSC) flip-flops and transmission gates based on 4:1 multiplexers. The ring counter can bypass up to 30 TPSC flip-flops. Indeed, the bypassed TPSC flip-flops are disabled to save power. Consequently, the ring counter can generate from 10 to 40 shifted rectangular pulse windows, as shown in Figure 3.18d. The greater the bypassed TPSC flip-flops, the wider the generated pulse bandwidth. It follows that this digital pulse shaping method provides a uniform sample and hold envelope of 10 to 40 samples.

The proposed IR-UWB transmitter in [63] achieves a maximum amplitude of 0.43 Vpp and a side-lobe rejection of 21 dB. This can address the IEEE 802.15.4 standard channels 5 to 15 (high band group). The digital pulse shaping enables the generation of pulses addressing the 499.2 MHz IEEE channels and the high bandwidth IEEE channels (1081 MHz, 1331 MHz, and 1355 MHz). From the results presented in [63], the estimated spectral efficiency is 63.5%, 44.7%, 48.3%, and 44.3% for a channel bandwidth of 499.2 MHz, 1081 MHz, 1331 MHz, and 1355 MHz,



(a) Transmitter architecture

(b) Architecture of PLL based on dual LC-QVCO

(c) Schematic of QVCO

(d) Digital pulse shaping

Figure 3.18.: Configurable IR-UWB coherent transmitter based on PLL with dual QVCO and digital pulse shaping [63].

respectively. The transmitter of [63] has a pulse emitted energy of 0.98 pJ and an total energy consumption of 1300 pJ/pulse for a PRF of 15.6 MHz.

The transmitter of [63] features a highly programmable ring counter enabling reasonable pulse shaping. It provides a great pulse bandwidth range thanks to the proposed ring counter's ability to bypass a programmed number of flip-flops. Indeed, it can generate a uniform sample and hold an envelope with a controlled number of samples, but with the cost of having a high power consumption. However, it presents a weak side-lobe rejection. In addition, the proposed PLL based on dual LC-QVCO offers a quite good central frequency range.

From the presented IR-UWB transmitters based frequency transposition and on LC-tank oscillators, it follows that the LC-tank oscillator exploitation achieves a limited central frequency range. Indeed, this is high enough to cover either the low band or the high band of the IEEE standard, similar to the IR-UWB transmitters based on delay line and edge combiner (direct pulse synthesis). Therefore, the LC-tank oscillator implementation is unsuitable to cover the FCC band. Besides, this implementation is an inappropriate choice regarding the ETSI regulation because of insufficient side-lobe rejection to comply with ETSI spectral masks.

Implementing a highly programmable ring counter is a better choice for pulse shaping than exploiting the long settling time of the LC oscillator. The first one results in a better pulse bandwidth range with the cost of having a high power consumption. Therefore, this highlights the relevance of a pulse-shaping circuit for the multi-standard design.

3.4.2. Based on ring oscillators

Concerning UWB transmitter design based on gated oscillators, it is also possible to implement a ring oscillator. A ring oscillator is composed of an odd number of inverter cells, that provide an instability condition to boot the oscillation. The number of inverters implemented depends on the target frequency. These oscillators are capable of fast start-up and shutdown, which enables the generation of ultra-short pulses (less than 1 ns) with a good output voltage dynamic. The use of ring oscillators has also been reported for the design of IR-UWB transmitters in [53, 72, 73]. The ring oscillator is an interesting architecture since it does not require either a capacitor or an inductor, unlike the LC oscillator. In other words, only MOS transistors are required, providing a more compact design. In addition, it can provide high-frequency oscillations. These can be evaluated by estimating the number of internal switches during an oscillation period. The frequency oscillation depends on the delay time of the delay cells, such that:

$$f_{osc} = \frac{1}{2N_d \cdot T_{delay}} \tag{3.5}$$

where N_d is the number of delay cells within the ring oscillator and T_{delay} is the delay time of the delay cell. The number of oscillator stages is very often 3. This is because a greater number of inverters increases the signal's total delay and reduces the oscillator frequency. From equation (3.5), a ring oscillator frequency depends on the average switching time of ring cells and of the technology process. However, this switching time is susceptible to PVT variations. In addition, another disadvantage of the ring oscillators is that they present worse phase noise and jitter than LC oscillators [71].

To control the frequency oscillation or the inverter time delay, there is the current starving technique that is based on inverter transistor current control, which influences on delay, rise time, and fall time of inverters or delay cells. From [72], Figure 3.19 displays an example where the voltage V_c controls the current that flows into the source current that does the inverter transistor biasing.

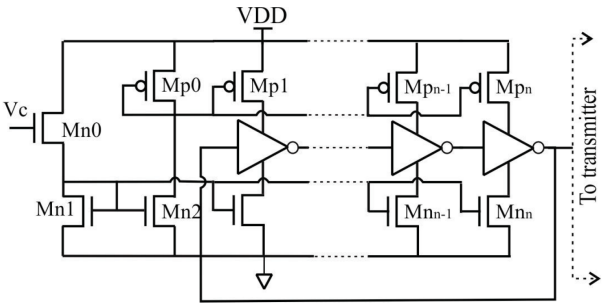
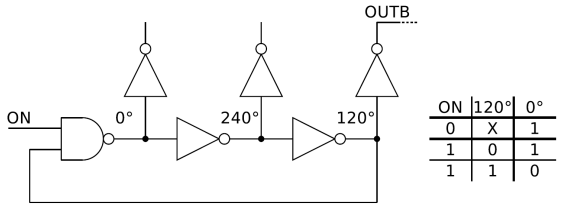


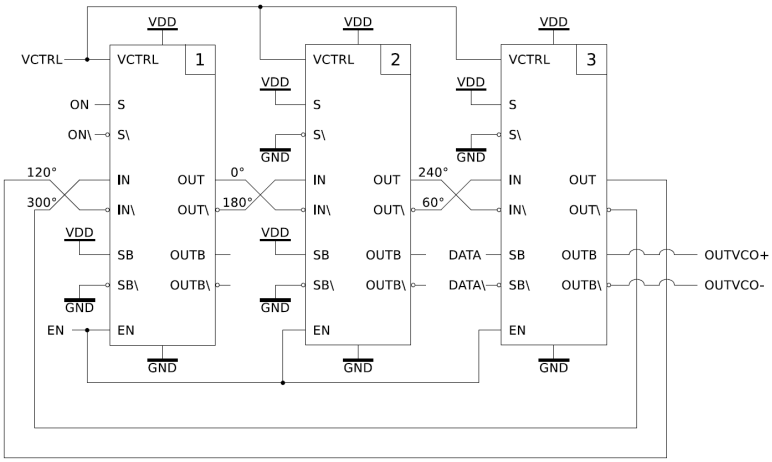
Figure 3.19.: Example of VCO architecture based on ring oscillator [72].

Alternatively, ring oscillators with differential output, using Current Mode Logic (CML), have been reported in [13, 53, 74, 75]. For instance, from [53], the CML logic is used for each stage of the ring oscillator, shown in Figure 3.20. In Figure 3.20b, "VCTRL" controls the oscillation frequency, and the complementary ON input is employed to fix the duration of the oscillations.

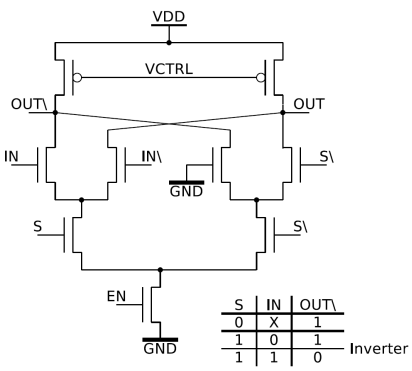
The "EN" input enables the standby mode (switch off). This ring oscillator is composed of 3 CML stages. Each stage has two CML gates, which are a tunable delay cell (Fig. 3.20c), and an output buffer (Fig. 3.20d). These two gates are based on the same CML XOR gate which presents the advantages of being strictly balanced and being turned off when "EN" has a low voltage level. CML cells are faster than CMOS cells. Nevertheless, the leakage power of CML cells is higher [13].



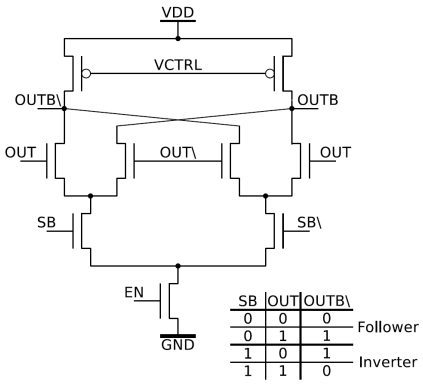
(a) Simplified diagram block.



(b) VCO architecture with 3 CML stages



(c) Tunable delay cell



(d) Output XOR Buffer

Figure 3.20.: Example of VCO architecture based on CML oscillator [53].

Moreover, it is possible to tune the frequency oscillation in a digital manner, where the oscillator is called a Digitally Controlled Oscillator (DCO). From [73], in Figure 3.21, the oscillation frequency is controlled through a set of tri-state buffer inverters placed in parallel,

where the maximal frequency is reached when all inverters are turned on. Since the boot time of the gated ring oscillator is fast, the oscillations present the shape of a rectangular windowed sine wave.

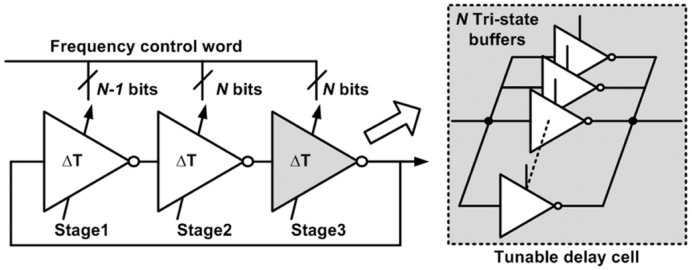


Figure 3.21.: Example of DCO architecture based on ring oscillator [73].

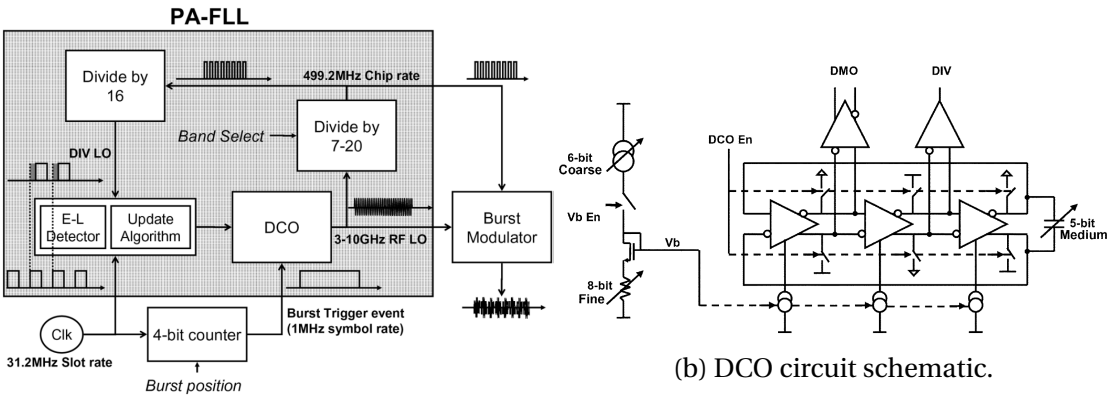
In [65], it is proposed an all-digital UWB transmitter architecture, in 90 nm bulk CMOS technology, based on a DCO that produces oscillations between 3 and 10 GHz. The proposed transmitter targets addressing the 499.2 MHz bandwidth channels of the IEEE 802.15.4 standard. Figure 3.22 displays the proposed UWB transmitter general architecture, where is proposed a Phase-Aligned Frequency-Locked Loop (PA-FLL) for the frequency synthesis. One of the advantages of the PA-FLL system is that it is possible to turn on the DCO and all dividers only during the burst transmission, hence saving power during two consecutive pulses.

Figure 3.22b displays the DCO of the proposed UWB transmitter, where it is proposed 3 methods to control the DCO frequency: coarse-range tuning achieved by a variable current source programmed by a 6-bit code to the biasing, medium-range tuning achieved by a variable capacitor programmed by a 5-bit code to have a short settling time, and finally a fine-range tuning obtained by a variable degeneration resistor programmed by an 8-bit code on the biasing current mirror.

The burst modulator of Figure 3.22a combines the signal generated by the DCO and a signal with a frequency of 499.2 MHz, in addition to performing a BPSK modulation.

The transmitter of Figure 3.22 can generate pulses addressing the 499.2 MHz bandwidth channels of the IEEE standard between 3 and 10 GHz, with a side-lobe suppression of 24 dB. This suggests the ring oscillator can achieve a fast-transient response to fabricate a short pulse. From the measurement results of [65], the estimated spectral efficiency is 56%. The generated pulses have an emitted energy of 1 pJ. Finally, the transmitter of [65] presents an energy consumption of 40 pJ/pulse and static power of 640 µW.

Regarding the multi-standard design, the transmitter of [65] is interesting because of the implementation of the ring oscillator featuring an extensive oscillation frequency range. As a result, this circuit can address all the 499.2 MHz IEEE channels. However, this circuit cannot address large-bandwidth IEEE channels because of the 499.2 MHz signal that drives the burst modulator. Consequently, this circuit cannot generate pulses shorter than 2 ns, having a limited pulse bandwidth range.



(a) General Architecture

(b) DCO circuit schematic.

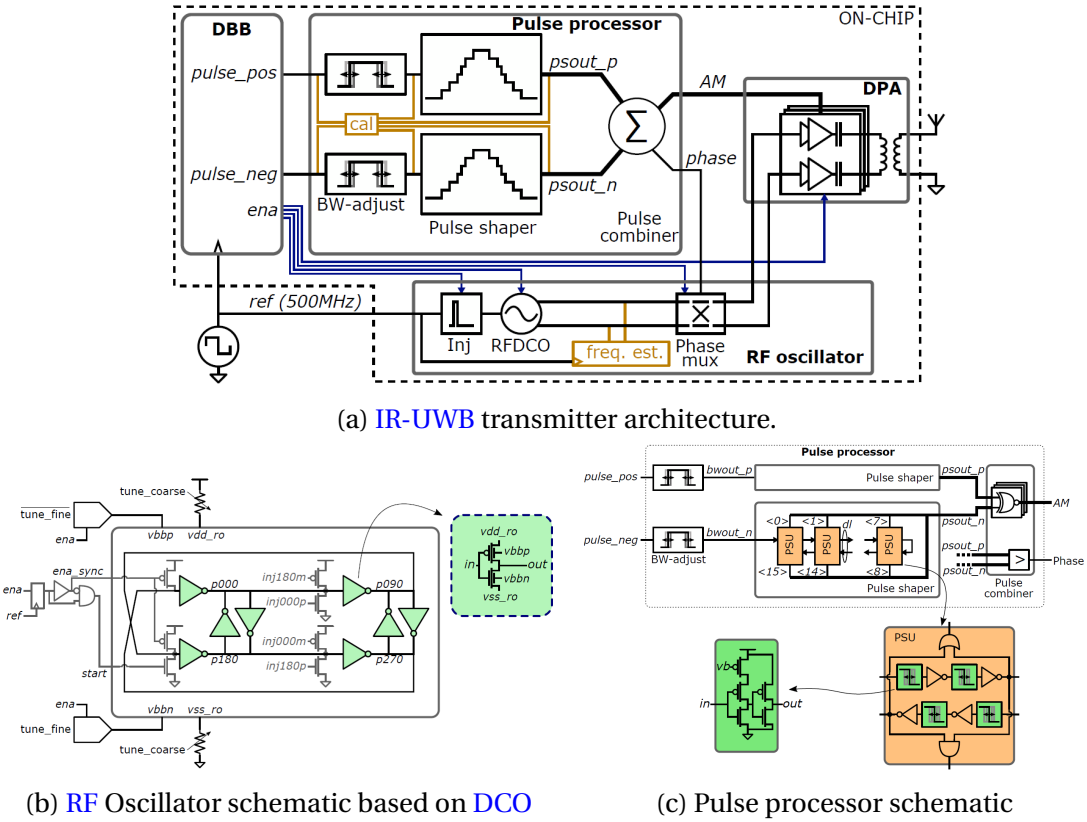
Figure 3.22.: UWB transmitter based on PA-FLL [65].

In [67], the use of a ring oscillator is also considered to design an IR-UWB transmitter based on an enable-locking DCO and pulse mixing. It proposes extensive duty-cycling enabling low power consumption. It has been implemented in 22 nm Fully Depleted Silicon on Insulator (FD-SOI) technology. To clarify, the FD-SOI is a planar process capable of exploiting the reduced silicon geometries advantages. It presents two main attractive advantages: better electrostatic characteristics and reduced leakage current [76–78]. The transmitter architecture is displayed in Figure 3.23. This architecture presents a digital baseband, pulse processor, RF oscillator, and DPA. The digital baseband provides pulse data corresponding to IEEE 802.15.4 packets. The oscillator block generates the carrier frequency. The reference clock for the digital baseband and oscillator blocks is supplied by an external 500 MHz clock signal. Finally, the pulse processor converts the input pulse to a 16-bit control signal for the DPA.

The RF oscillator schematic is displayed in Figure 3.23a. It is composed of a DCO, injection generator, and phase multiplexer. As shown in Figure 3.23b, the DCO core is a ring oscillator whose fine frequency tuning is done through the back-gate biasing (vbbp and vbbn signals). On the other hand, the frequency coarse tuning is done through the current starving technique a configurable resistor.

The back-gate biasing is only suitable for frequency fine-tuning. For instance, [66] proposes an IR-UWB transmitter System-on-Chip (SoC) using a 28 nm FD-SOI CMOS, featuring ring oscillator. It proposes a frequency tuning via back-gate biasing that enables a poor range (3.5-4.5 GHz) since the FCC band range is targeted.

The pulse processor schematic is shown in Figure 3.23c. It performs the pulse shaping. The pulse processor is designed to limit the pulse bandwidth and suppress the adjacent side lobes. The pulse processor inputs correspond to 2 ns pulses. Firstly, the bandwidth adjustment block (BW-adjust) changes the pulse width. Secondly, the pulse shaper transforms the single input pulse to a 16-bit unary-weighed amplitude-modulated signal. From Figure 3.23c, the pulse shaper consists of a controlled delay line. It has 8 stages, each corresponding to a Puls-Shaping Unit (PSU). Every delay line stage has 2 signal outputs, thereby the delay line has an output of 16-bit. The delay time of the PSUs can be controlled separately. Finally, the pulse combiner combines the delay line output using logic gates. It follows that the envelope generated by the circuit of 3.23c corresponds to a non-uniform sample and hold envelope having 16 samples.



(a) IR-UWB transmitter architecture.

(b) RF Oscillator schematic based on DCO

(c) Pulse processor schematic

Figure 3.23.: IR-UWB transmitter based on enable-locking DCO and pulse mixing [67].

The target pulse shape is a trade-off between main-lobe bandwidth, side-lobe rejection, and pulse time span, because of the limited output resolution. The DPA consists of a phase multiplexer and differential switched-capacitor class-D output stage with a balun.

The transmitter of Figure 3.23 allows an output central frequency between 3 GHz and 9 GHz, in addition to a BPSK modulation. The transmitter of [67] can only generate pulses with a bandwidth of 499.2 MHz, with a side-lobe rejection of 29 dB. From the measurement results shown in [67], the estimated spectral efficiency is from 47.8% to 52.7%. The reported pulses have an amplitude of 0.18 Vpp and an emitted energy of 0.87 pJ. Lastly, the transmitter of [67] has an energy consumption of 96 pJ/pulse. This low power consumption can be attributed to the extensive duty cycling of the RF oscillator.

To achieve a good oscillation frequency range, the transmitter of [67] features a frequency coarse tuning using a configurable resistor combined with fine-tuning using back-gate biasing. This last one is useful for compensating PVT variations and making the output waveform rail-to-rail. Besides, this transmitter obtained a great side-lobe rejection to the controlled delay line that features an independent delay tuning, leading to a non-uniform sample and hold the envelope. Nevertheless, a limited pulse bandwidth range is obtained because the digital baseband circuit is clocked at 500 MHz, as pointed out in Figure 3.23a. As a consequence, the transmitter [67] is incapable of addressing the large-bandwidth IEEE channels.

In [68, 69], an IR-UWB transmitter in 28 nm CMOS technology compliant with IEEE 802.15.4

is presented. Its architecture is based on a ring oscillator and a pulse shaping, as shown in Fig. 3.24. The architecture of the transmitter of [68, 69] is similar to the one of [67]. A digital baseband provides phase and amplitude signals clocked at 499.2 GHz to the analog transmitter chain. From Figure 3.24a, the analog transmitter chain consists of an injection-locked ring oscillator, bandwidth controller, pulse shaper, and DPA. The injection-locked ring oscillator consists of a pseudo-differential Digitally Controlled Ring Oscillator (DCRO). It is composed of 4 current-starved inverters whose frequency is controlled digitally.

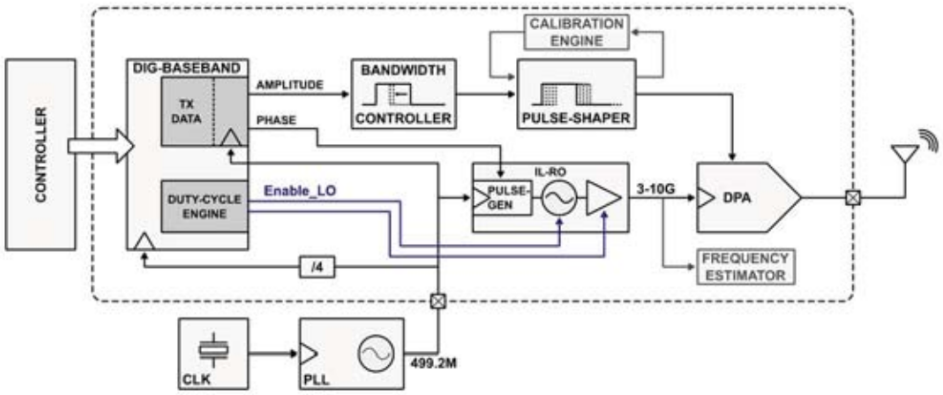
The bandwidth controller controls the pulse width of the generated pulse (nominally 2 ns). The pulse shaper provides an 8-bit word in one-hot coding to the DPA. The pulse shaper block is based on a DCDL line with 8 delay stages. The delay cells of the pulse shaper have been implemented using current-starved buffers whose unit delay is controlled digitally by a 4-bit word, as shown in Figure 3.24b. This 4-bit word corresponds to the bias current control. The employed current-starving technique uses a PMOS current mirror with a programmable current source, similar to the pulse shaping proposed in [54, 55]. Thereby, the proposed transmitter in [68, 69] can generate IR-UWB pulses with a non-uniform sample and hold envelope having 8 steps. The delay line output signals are then combined to obtain the targeted envelope, which can approximate a trapezoidal or triangular envelope. The 8 output signals of the pulse shaper are applied into the switched-capacitor DPA cells.

The transmitter of [68, 69] achieves a central frequency between 3 GHz and 10 GHz, with side-lobe rejection of 32 dB. Besides, this transmitter can address addresses 14 IEEE 802.15.4 channels, especially all the 499.2 MHz channels of the IEEE 802.15.4 standard. The spectral efficiency is estimated at 41.2-51.9% for an IEEE channel bandwidth of 499.2 MHz The spectral efficiency for large-bandwidth IEEE channels is estimated at 40.93% and 33.6-35.1% for an IEEE channel bandwidth of 1081 MHz and 1331 MHz, respectively. The generated pulses have an amplitude of 0.2 Vpp in addition to an emitted energy of 1.7 pJ. Finally, regarding energy consumption, the transmitter of [68, 69] has an energy consumption of 27 pJ/pulse.

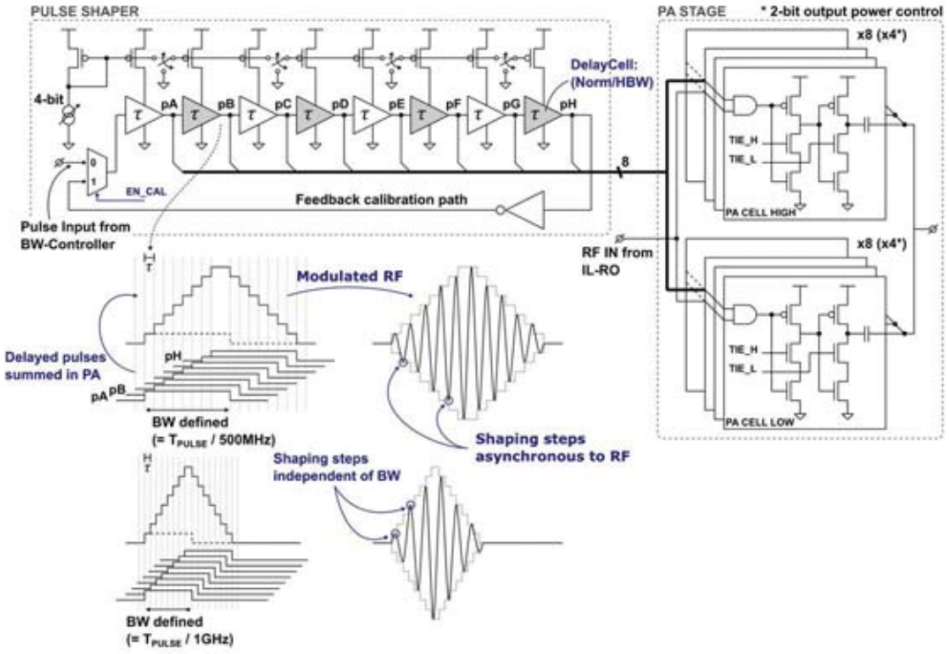
Regarding the multi-standard design, the transmitter of [68, 69] is great because it presented a great frequency oscillation tuning, the best side-lobe rejection and the best highest number of addressed IEEE channels. A great frequency range is achieved by implementing a ring oscillator based on current-starved inverters that are capable of offering a fast startup. The best performance in terms of side-lobe rejection and the number of addressed IEEE channels comes from the pulse shaper based on DCDL featuring an independent delay control. However, it presents a low spectral efficiency for large-bandwidth IEEE. This suggests that this pulse shaper has difficulty generating ultra-short pulses having a bandwidth larger than 1 GHz.

From the presented IR-UWB transmitters based on ring oscillators, it follows that the main advantage of using ring oscillators is the great central frequency range, which is high enough to cover the IEEE channels in FCC band.

To achieve the multi-standard design with a better side-lobe rejection, the ring oscillator is combined with an envelope shaping circuit based on a DCDL composed of current-starved buffers and a pulse combiner. The independent and digital control of the delay cells makes feasible the generation of a IR-UWB pulse having an adjustable duration and non-uniform sample and hold. As a result, this enables a good pulse bandwidth and great side-lobe suppression. Therefore, the implementation of a ring oscillator combined with a DCDL is a pertinent choice for a multi-standard design targeting the FCC band.



(a) IR-UWB transmitter architecture.



(b) Asynchronous pulse shaping based on a controlled delay line.

Figure 3.24.: IR-UWB transmitter based on a ring VCO and DCDL [68, 69].

3.5. Conclusion

In this chapter, the IR-UWB transmitters literature survey was presented. Reported works have chosen to implement pulse synthesizers rather than pulse generators because this generates a signal with fixed parameters, having a limited pulse shaping. It is worth highlighting the importance of a multi-band and multi-standard pulse synthesizer design. It should be able to generate pulses addressing the IEEE 802.15.4 and 802.15.6 channels distributed over the FCC band (3.1-10.6 GHz). Hence, the central frequency and bandwidth are two important pulse parameters to be controlled. Besides, the IR-UWB pulse shaping is crucial to generate pulses with high side-lobe rejection addressing the IEEE channels of different bandwidths, in

addition to with the spectral requirements imposed by the FCC, ETSI and IEEE standards.

This survey reported two main pulse synthesis methods: pulse direct synthesis and frequency transposition pulse synthesis. The first method employs a delay line to synthesize the pulse directly into the targeted frequency. On the other hand, the second method uses a VCO whose architecture is based on an LC tank or a ring oscillator. This oscillator generates the oscillation frequency to which a baseband pulse is transposed.

In Table 3.1, a comparison between the presented IR-UWB transmitters is done. All introduced transmitters presented measurement results. More generally, the transmitters based on ring oscillators are the most interesting regarding the pulse central frequency range. Indeed, the transmitters of [65, 68] cover the frequency band of 3-10 GHz. On the other hand, transmitters based on LC-tank oscillators or delay lines can cover the frequency band corresponding to the IEEE standard low band group (3.1-4.5 GHz) or the high band group (6.5-10 GHz).

The transmitters with a pulse shaping based on a VCDL achieved better side-lobe rejection (29-32 dB). For instance, the transmitters of [68] and [54] achieved a side-lode suppression of 32 dB and 31 dB, respectively. This suggests that the use of a VCDL associated with a recombination circuit for the pulse shaping is interesting to reach better side-lobe rejection. This allows the synthesis of a pulse having a non-uniform sample and hold envelope. However, it should be pointed out that the transmitter [54] does not integrate a local oscillator.

The transmitters based on direct pulse synthesis showed a limitation regarding pulse bandwidth tuning range. They are not able to generate pulses having a bandwidth between 499.2 MHz and 1355 MHz. Meanwhile, some reported transmitters based on frequency transposition pulse synthesis managed to have a pulse bandwidth tuning range capable of covering 499.2-1355 MHz. For instance, the transmitter of [63] is the best in terms of bandwidth tuning range. It can generate signals with bandwidth between 499.2 MHz and 1355 MHz. Nevertheless, this transmitter is not the one that addresses the highest number of IEEE 802.15.4 channels because of its central frequency range of 5-10 GHz. The transmitter of [68] is the one that addresses the highest number of IEEE 802.15.4 channels. It can address 14 IEEE 802.15.4 channels, where 2 of them have a high bandwidth (1081 MHz, 1331 MHz).

The transmitter of [63] is the best in the estimated spectral efficiency criterion. It achieved 63.4% and 48.3% for low and large-bandwidth IEEE channels, respectively. The second best in this criterion is the transceiver of [57]. These circuits have in common a pulse shaping based on the generation of an uniform sample and hold envelope and a reasonable side-lobe (up to 25 dB). This suggests that an envelope having a uniform step time can offer good spectral efficiency with the cost of a lower side-lobe rejection. On the other hand, the transmitter of [68] has the worst estimated spectral efficiency for high bandwidth IEEE channels (33.6-40.9%), despite addressing the highest number of IEEE channels. The reason for this is that the [68] has difficulties in generating ultra-short pulses, which have higher bandwidth.

In conclusion, for a multi-standard IR-UWB pulse synthesizer design with the target of covering the FCC band and achieving better side-lobe suppression, it follows that an architecture based on a ring oscillator and a pulse shaping circuit composed of a VCDL and recombination circuit seems to be the best choice. Regarding the VCDL design, the delay tuning should be wide enough to cover a good pulse bandwidth and independent to achieve better side-lobe rejection. Besides, the frequency transposition pulse synthesis is a better choice to generate pulses with a sufficient bandwidth tuning range to address all the IEEE 802.15.4 channels.

Table 3.1.: Performance comparison with state-of-the-art IR-UWB transmitters

	Vauché TCSI'17 [21]†	Haapala JSSC'20 [51]	Miranda CICC'20 [52]	Chen RFIC'22 [54]&	Chen ISSCC'22 [57]†	Song VLSI'23 [58]†	Phan TCSI'08 [61]	Schmickl TCSI'20 [62]	Zhang LMWT'22 [63]	Ryckaert JSSC'07 [65]	Streel JSCC'17 [66]	Bechthum ESSCIRC'23 [67]	Singh JSSC'21 [68]
Process (nm)	130	65	65	28	40	28	180	180	28	90	28 (FD-SOI)	22 (FD-SOI)	28
Supply Voltage (V)	1.2	1.2	1.2	0.9	1.25	0.9	1.5	1	0.9	1	0.9	0.8	0.9
Core Area (mm²)	0.11	0.22	N/A	0.25	N/A	1.33	0.3	0.25	0.21	0.07	0.55	0.09	0.15
Die Area (mm²)	1.31	1.1	0.7	N/A	8.8	N/A	0.66	3.91	N/A	N/A	0.93	1.0	2.37
Architecture	Delay Line	Delay Line	Delay Line	LO (External)	LO (Mixer)	LO	LO (LC Tank)	LO (LC Tank)	LO (LC Tank)	LO (Ring)	LO (Ring)	LO (Ring)	LO (Ring)
Pulse Shaping	Delay Line	Delay Line	Delay Line	Delay Line	LUT Flip-flop	Delay Line	LO Modulation	LO Modulation	Counter	PA-FLL	Counter	Delay Line	Delay Line
Modulation	OOK DB-BPSK	OOK	OOK	OOK BPSK	N/A	BPSK	OOK	N/A	BPSK	BPSK	2-PPM BPSK	BPSK	BPSK
Spectral compliance	FCC	ETSI	FCC	FCC	FCC	FCC	FCC	ETSI	FCC	FCC	FCC	FCC	FCC
Freq. Range (GHz)	3.1-4.9	6-8.5	3.6-7.5	4-9	6.5-10	6-9	3-5	6-8.8	5-10	3-10	3.5-4.5	3-9	3-10
Mod. BW (GHz)	1/1.3	0.5	1/1.3	0.5/1/1.3	0.5/1	0.5	0.5	0.5	0.5/1/1.3	0.5	0.5	0.5	0.5/1
Side-lobe rejection (dB)	18	30	23.8*	31	25*	31	18	18	21*	24*	23*	29	32
IEEE 802.15.4 Addressed Channels (Total)	4 (1)	5,6,8,9 (4)	4,7 (2)	2-12 (11)	5-15 (11)	5,6,8,9 10,12 (6)	1-3 (3)	5,6,8,9 (4)	5-15 (11)	1-3,5,6 8-10,12-14 (11)	1-3 (3)	1-3,5,6 8-10,12 (9)	1-14 (14)
IEEE 802.15.6 Addressed Channels (Total)	None (0)	3-6 (4)	None (0)	1-8 (8)	3-10 (8)	3-8 (6)	0-2 (3)	3-6 (4)	3-10 (8)	0-10 (11)	0-2 (3)	0-8 (9)	0-10 (11)
Spectral Eff. (%)* @BW = 499.2 MHz	-	[49.5-55.5]	-	[44.2-55.5]	[40.2-61.6]	[49.8-51]	[53.1-54.3]	48.2	63.5	56.3	-	[47.8-52.7]	[41.2-51.9]
Spectral Eff. (%)* @BW = 1081 MHz	-	-	-	47.9	46.5	-	-	-	44.7	-	-	-	40.93
Spectral Eff. (%)* @BW = 1331 MHz	-	-	-	[45.2-45.8]	-	-	-	-	48.3	-	-	-	[33.6-35.1]
Spectral Eff. (%)* @BW = 1355 MHz	-	-	-	-	-	-	-	-	44.3	-	-	-	-
Do the pulses fit into IEEE masks?*	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	No	Yes	Yes
Do the pulses have a BW-$_{-10dB}$ greater than 500 MHz?*	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	No
Amplitude (Vpp)	0.9	0.46	0.91	0.6*	N/A	0.55*	0.16	1	0.43	N/A	0.9	0.18	0.2
Emitted Energy E_p (pJ/pulse)	0.48	0.83	2.4	0.82*	0.86*	0.84*	0.11	0.25	0.98*	1*	0.41	0.87*	1.7
Dynamic Energy E_{ac} (pJ/pulse)	146	63	8.5	660	N/A	N/A	16.8	6.2	N/A	40	158◇	96	27
Efficiency E_p/E_{ac} (%)	0.32	1.28	15.3	0.07*	0.02*	1.2*	0.63	7.5	0.07	2.5*	0.26	1*	6.2
Static power (µW)	100	0.38	13	N/A	N/A	N/A	390	N/A	N/A	640	14.4	N/A	N/A
P_C (mW) @PRF = 3.9 MHz	0.67◇	0.25◇	0.05◇	4.49◇	15.4◇	0.27◇	0.46◇	0.03◇	5.1	0.80◇	0.63◇	0.38◇	0.11◇
P_C (mW) @PRF = 15.6 MHz	2.38◇	0.98◇	0.15◇	17.97◇	61.6	1.09◇	0.65◇	0.10◇	20.3	1.26◇	2.47◇	1.5◇	0.42◇

† Paper includes a receiver, & Carrier input from an external signal generator, * Estimated from reported pulse spectrum, ◇ Estimated power consumption.

4. Design of IR-UWB transmitter based on gated ring oscillator

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4.1. Introduction

From the literature survey, an IR-UWB transmitter based on frequency transposition pulse synthesis and also a local oscillator seems to be the best choice to address every IEEE 802.15.4 and 802.15.6 channels. The required local oscillator should cover the FCC frequency band (3.1-10.6 GHz) while being able to turn on and turn off quickly to minimize the power consumption when no pulse is generated. Indeed, it is necessary to generate short pulses of a few ns to fit into IEEE spectral masks. Therefore, a ring oscillator should be a relevant choice because of its extensive oscillation frequency range. In this Chapter, the design of a multi-standard IR-UWB transmitter based on the frequency transposition of a continuous envelope and implementing a ring oscillator is proposed. The continuous envelope is generated here by an external Arbitrary Waveform Generator (AWG) generator. Therefore, this transmitter design does not include an envelope shaping circuit. However, an envelope shaping circuit is proposed in the next chapter.

The proposed IR-UWB transmitter is designed to synthesize pulses addressing the IEEE channels in the FCC band between 3.1 and 10.6 GHz while respecting the spectral requirements imposed by FCC and IEEE standards. For instance, the FCC requires a minimum 10 dB pulse

bandwidth of 500 MHz, whereas the IEEE standards 802.15.4 and 802.15.4 a minimal side-lobe rejection of 18 dB and 20 dB, respectively.

To meet these spectral constraints, the proposed transmitter should be able to properly control the pulse shape and also the emitted spectrum. Therefore, the design targets the generation of a signal with tunable parameters, which are its central frequency, in addition to its amplitude and duration, as illustrated in Figure 4.1. From these specifications, the proposed IR-UWB transmitter can be labeled as a pulse synthesizer.

The pulse shape can also be controlled through an AWG, which can deliver all continuous envelopes addressed in Chapter 2 (rectangular, symmetrical triangular, asymmetrical triangular, symmetrical trapezoidal, and asymmetrical trapezoidal; from the study introduced in this chapter, the asymmetrical envelopes are the best in terms of side-lobe rejection, especially the trapezoidal).

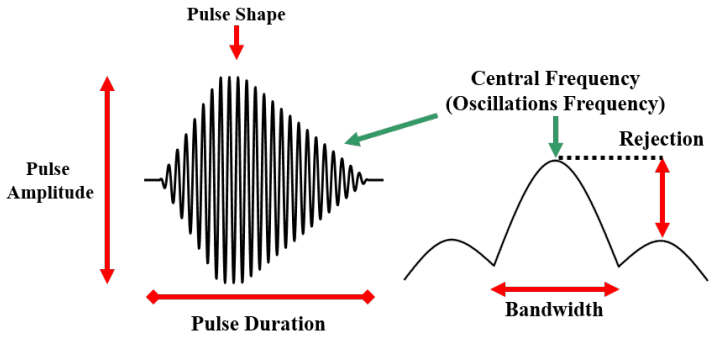


Figure 4.1.: Tunable parameters of an IR-UWB pulse with continuous envelope.

The transmitter architecture, which consists of 3 main blocks, is shown in Figure 4.2. The block (a) is a Voltage-Controlled Oscillator (VCO) with fast start and stop ability. This VCO must be able to generate a pulse with a central frequency covering FCC frequency band (3.1-10.6 GHz). The block (b) is a buffer circuit that must guarantee a good transmission of the oscillations from VCO to the next block, which is the Voltage-Controlled Amplifier (VCA) (c). This block is an amplifier whose gain is controlled to modulate the amplitude of the oscillations coming from the oscillator. However, from Chapter 2, the continuous envelope generated should have a width from 1 ns to 5 ns to address all IEEE channels. The VCA gain input "In RF" must also have a large enough bandwidth. Finally, it can be noticed that there are coupling capacitors of 2 pF, between the VCA and the load, which let pass the AC signal and block the DC signal.

To cover entirely the targeted frequency band, Current Mode Logic (CML) has been chosen to implement the blocks (a), (b), and (c). Indeed, CML logic is a differential logic family, commonly used in high-data rate integrated systems. It has the advantage of being less susceptible to noise, but the drawback is a higher power consumption (but quasi-constant).

The full circuit has been implemented in Cadence Virtuoso and fabricated in a 28 nm CMOS process from TSMC for a supply voltage of 0.9 V. This design kit was chosen because it allows the design of an IR-UWB transmitter capable of covering the FCC band (3.1-10.6 GHz).

In this chapter, an overview of the proposed architecture is first introduced. Next, the design

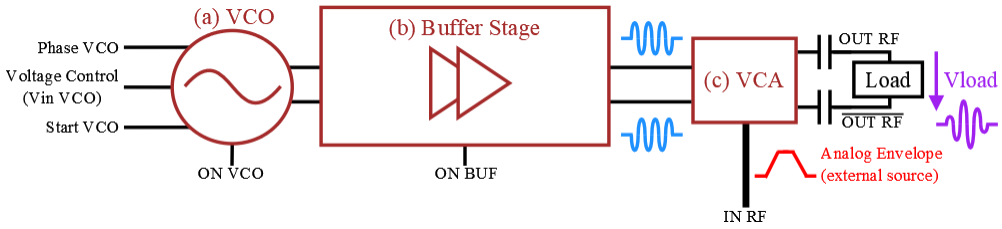


Figure 4.2.: Proposed IR-UWB transmitter architecture.

of the three blocks (a) to (c) is presented. Post-layout simulations are shown all along the design. Finally, the global layout and measurement results are presented.

4.2. Architecture overview

Figure 4.3 displays the proposed transmitter signals chronogram. The signal "ON VCO" turns on and turns off the VCO, while the signal "Start VCO" commands the VCO oscillations' start. The signal "ON BUF" turns on and turns off the buffer stage block. The signal "IN RF" (generated by an AWG) controls the VCA gain. It can be noted that the frequency of "IN RF" corresponds to the Pulse Repetition Frequency (PRF). Finally, the signals "OUT VCO dif" and "OUT RF dif" correspond to the VCO and transmitter differential outputs, respectively.

According to Figure 4.2, the pulse generation process begins by turning on the VCO ("ON VCO" at a high level). The VCO is next started ("Start VCO" at a high level). The VCO frequency should be stabilized before turning on the remaining blocks. Next, the buffer stage is turned on ("ON BUF" at a high level), while the signal "IN RF" modulates the IR-UWB pulse. After the IR-UWB pulse transmission, the transmitter blocks should be turned off, according to the chronogram of Figure 4.3.

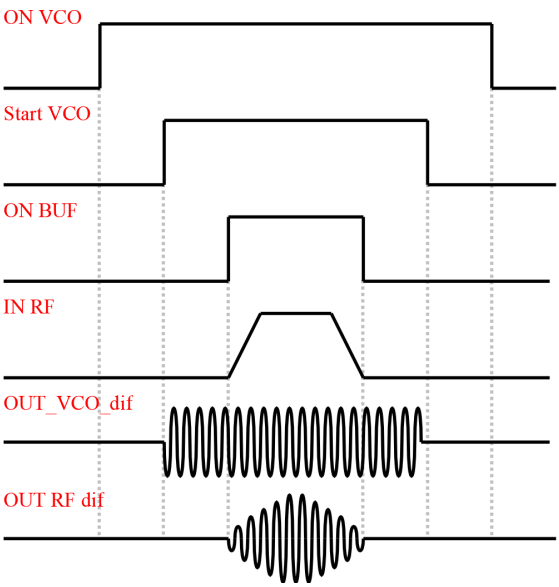


Figure 4.3.: Proposed IR-UWB transmitter signals chronogram.

4.3. Voltage-Controlled Oscillator

The Voltage-Controlled Oscillator (VCO), which is block (a), generates oscillations having a frequency equal to the targeted central frequency. It is based on Voltage-Controlled Ring Oscillator (VCRO) architecture, as indicated in Figure 4.4. Its principle is to propagate an edge in a closed loop chain composed of delay cells but having a negative open-loop gain. From Chapter 3, the oscillation frequency depends on the delay time of the delay cells. In Figure 4.4, the delay time controlled by the "Vin_{VCO}" through the current starving technique to achieve a great VCO gain, and also a good oscillation frequency range.

The number of cascaded delay cells, where the minimum is three if CMOS inverters are used and two for CML inverters, provides an instability condition required for the oscillation start (a ring with one delay cell is not feasible because the transistor will be self-biased, presenting only a DC component current).

NAND gates have been here implemented instead of inverters, enabling fast oscillations start and stop, in addition to requiring the design of only one delay cell since NAND gates can act as an inverter if one of the two inputs is set to V_{DD}. For instance, when the signal “Start VCO” is at a high level, the NAND gate works as an inverter. On the other hand, when the signal “Start VCO” is at a low level, the NAND gate imposes a logic state stabilizing the oscillator.

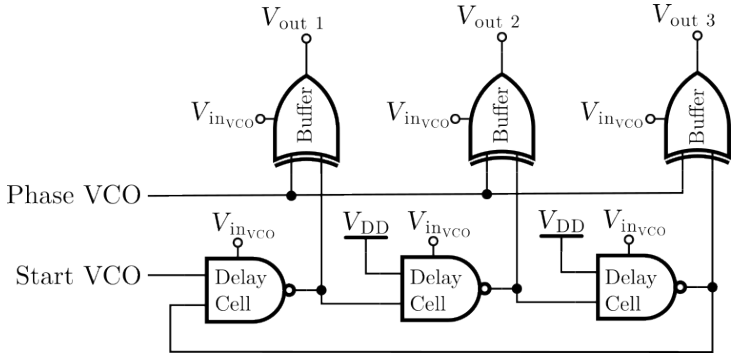
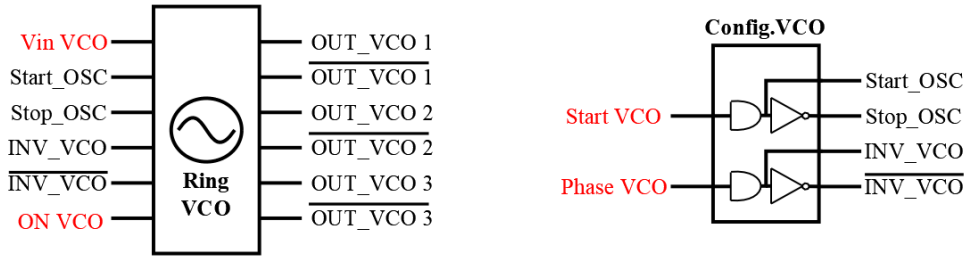


Figure 4.4.: VCRO topology.

Furthermore, a buffer cell based on an XOR gate allows a 180° phase-shift of the emitted pulse as needed to implement the BPSK impulse modulation introduced, for example, in the IEEE 802.15.4 standard. For instance, if the signal “Phase VCO” is at a high level, the buffer stage acts as an inverter. Otherwise, if the signal “Phase VCO” is at a low level, the buffer stage acts as a voltage follower.

In addition, the buffer cell provides better signal integrity of the oscillator output signal, minimizing the effect of frequency instantaneous variation. This variation is caused by modification of the load at the oscillator output through the addition of an element such as a mixer or a filter. There is a buffer cell for every delay cell, so they have the same output load, consequently ensuring that each delay cell has the same behavior.

The proposed VCO architecture is displayed in Figure 4.5. Since the CML VCRO requires input differential signals to control its start-up and phase, the circuit of Figure 4.5b is implemented to generate them.



(a) CML VCRO. (b) Start-stop and Phase Configuration.

Figure 4.5.: VCO architecture.

The proposed CML VCRO architecture is shown in Figure 4.6 and Figure 4.7 shows the delay cell and buffer cell transistor level schematics.

The delay cell and buffer cell are based on an architecture similar to a CML XOR gate [79]. It has the interesting feature of being perfectly balanced. From the CML XOR gate, the input wiring of the tunable delay cell (Fig. 4.7a) is adapted to realize the function of the NAND gate [13, 53].

Regarding the buffer cell (Fig. 4.7b), the wiring has not been modified because this gate is used to implement BPSK modulations. The complementary input signal "INV" enables the positive and negative paths of the differential VCO output to be commuted (the positive VCO output becomes negative VCO output, and the negative VCO output becomes positive VCO output).

From Figure 4.7, the signal "Vctrl" drives the PMOS transistors gate of the tunable delay cell and buffer cell to ensure an identical biasing. This signal controls also the VCO frequency oscillation because it can modify the active loads biasing, thereby tuning the ring VCO stages delay.

Therefore, the proposed ring oscillator has identical delay cells realizing the delay function, but the first stage equally realizes the oscillation activation.

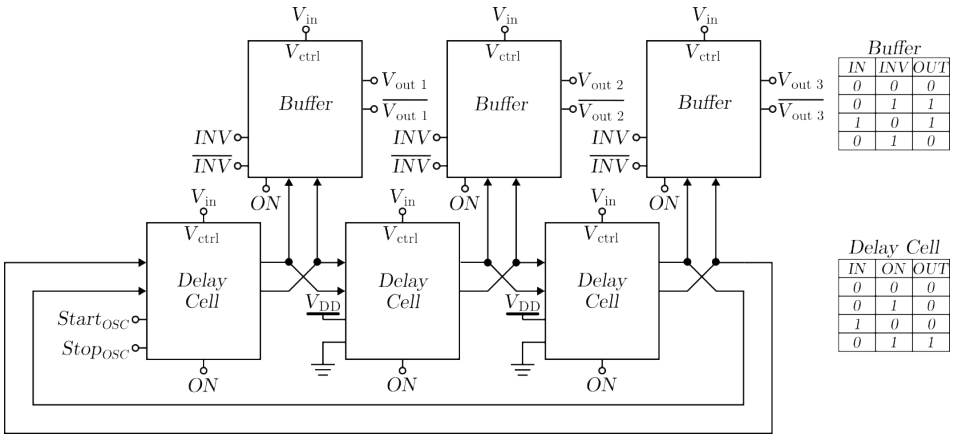
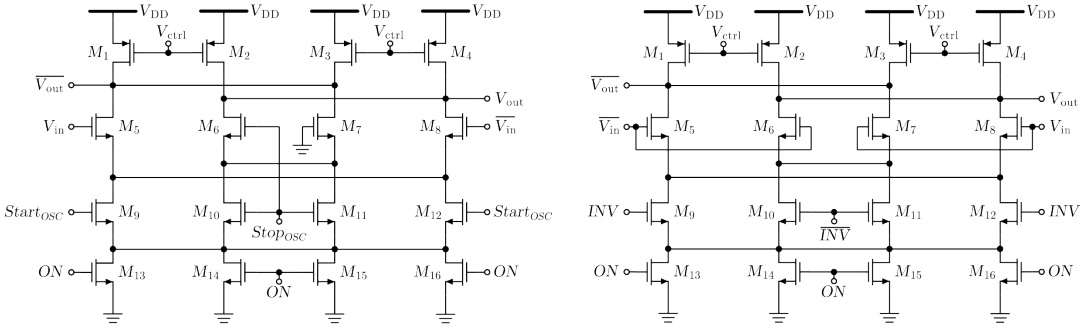


Figure 4.6.: CML gated ring VCO architecture.



(a) Tunable delay Cell. (b) Buffer.

Figure 4.7.: CML gated ring VCO blocs transistor level schematics.

The tunable delay cell and buffer cell transistor sizing are indicated in Table 4.1. The transistor sizing has been done to cover an oscillation frequency of 10.6 GHz considering the parasite's effects related to circuit layout. Moreover, the PMOS transistors composing the active load have been sized to obtain an oscillation frequency range of 3.1-10.6 GHz. The transistors of the tunable delay cell have a width-length ratio (W/L) 3.67 times higher than the one of transistors of the buffer cell. This difference avoids the buffer cell to overload the VCO and also to slow down the VCO, but allows to properly transfer the output voltage to the next IR-UWB transmitter block (buffer stage). The transistor's length is longer than the minimum allowed by the design kit (30 nm) to reduce the VCO power leakage.

Table 4.1.: Ring VCO transistor sizing

Circuit	Width (µm)				Length (nm)
	M1 to M4	M5 to M8	M9 to M12	M13 to M16	M1 to M16
Delay Cell	12.1	48.4	96.8	48.4	60
Buffer	4.4	17.6	35.2	17.6	80

Figure 4.8 shows the layout of the VCO. Since the ring oscillator architecture is differential (CML), the layout of the ring oscillator (black rectangle), delay cells (magenta rectangle), and buffers (blue rectangle) should be balanced. The interconnections between the delay cells have the same metal layers and length to guarantee that the differential signals have the same delay propagation inside the delay cell loop. This condition ensures that the differential signals are in phase opposition. If these signals are not in phase opposition, oscillation harmonics can arise in the transmitter output spectrum, which makes it more difficult to comply with IEEE spectral masks.

To achieve higher oscillation frequencies, the interconnections between delay cells are wide and have 2 stacked metal layers, which these layers are the thickest among the available metal layers. Indeed, the wider the interconnection metal line is, the stronger the parasitic capacitance is. On the other hand, the narrower the interconnection metal line is, the stronger the parasitic resistance is. This can be explained by the second Ohm's Law, where the resistance is directly proportional to the width of the conductor but inversely proportional to the area

of the transversal section [80]. Thus, in RF layout designs, it is more efficient to use thicker and wider metal lines in addition to stacked metal layers to reduce the metal line parasitic resistances of long interconnections. Moreover, it can be noted that buffers have been placed next to the associated delay because the longer the interconnection metal line length is, the greater the metal line resistance is.

Finally, the ground and supply voltage metal layers are distributed all around the VCO layout to ensure a good supply voltage level all along the layout, especially in the PMOS transistor source terminal. The electric current throttling should be avoided because it can limit the maximum VCO frequency.

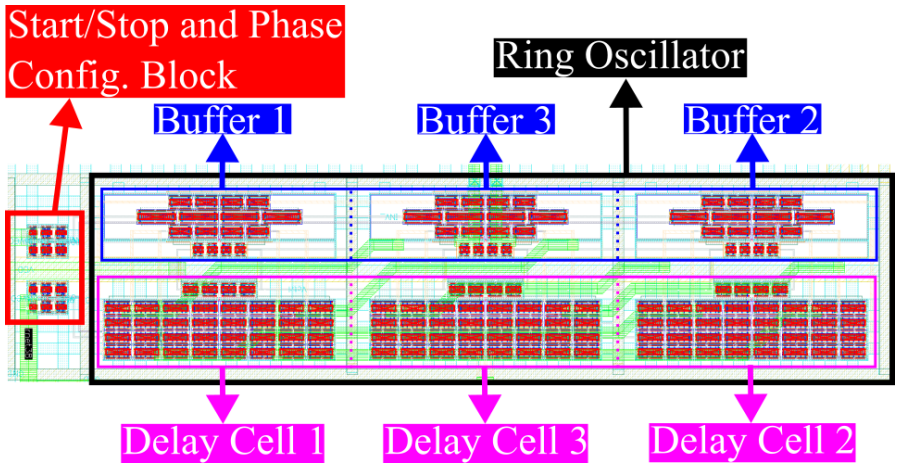


Figure 4.8.: VCO layout.

Figure 4.9 displays the post-layout simulation of VCO frequency as a function of the VCO input voltage ("Vin VCO"). Figure 4.10 shows the post-layout simulation of VCO output voltage and its always-on power consumption as a function of the frequency oscillation. It can be noted that all blocks of the proposed IR-UWB transmitter (Fig. 4.2) were considered to obtain these results. Wire bonding models are not included in the post-layout simulations.

From Figure 4.9, it can be observed that the proposed VCO can cover all the 3.1-10.6 GHz frequency band as required since its minimum and maximum oscillation frequencies are 1 GHz and 10.7 GHz, respectively. The average VCO gain is around -23.4 GHz/V. Therefore, the choice of implementing a differential ring oscillator combined with the layout design strategies seems well satisfactory for a design targeting a wide frequency band, such as the FCC band.

From Figure 4.10a, it can be noticed that the VCO output voltage (indicated in the buffer output in Figure 4.6) decreases non-linearly with an increasing oscillation frequency. The reason for this is the frequency-tuning through the PMOS active loads (Fig. 4.7), which makes unfeasible the output waveform rail-to-rail for all oscillation frequencies. Besides, the maximum frequency oscillation is mostly limited by the parasitic capacitances, which reduce the tunable delay cells' output voltages. Indeed, the ring oscillator requires that oscillations have a peak-to-peak voltage higher than 0.7 to maintain them.

Alternatively, from Figure 4.10b, the VCO always-on mean power consumption is approximately proportional to the oscillation frequency. Hence, a higher frequency oscillation implies a higher power consumption despite the lower output voltage.

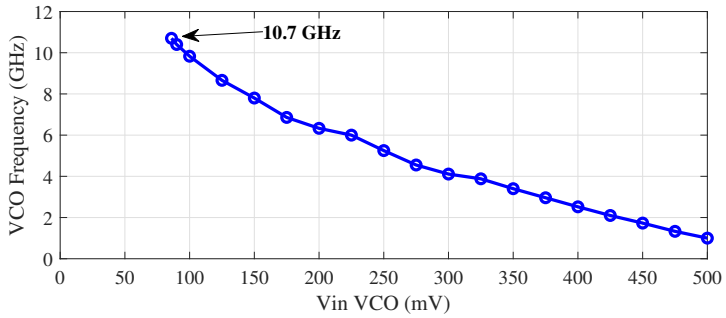
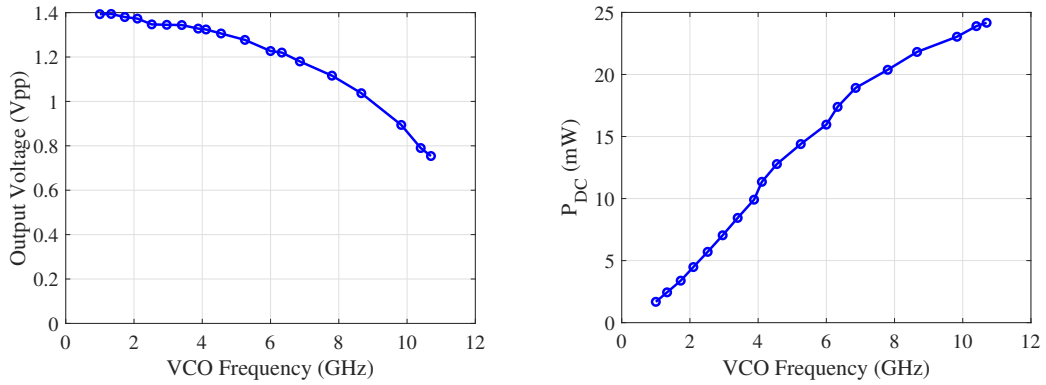


Figure 4.9.: VCO frequency as a function of the VCO input voltage.



(a) Output voltage.

(b) Always-on power consumption.

Figure 4.10.: VCO output voltage and always-on power consumption as a function of the frequency oscillation.

4.4. Buffer Stage

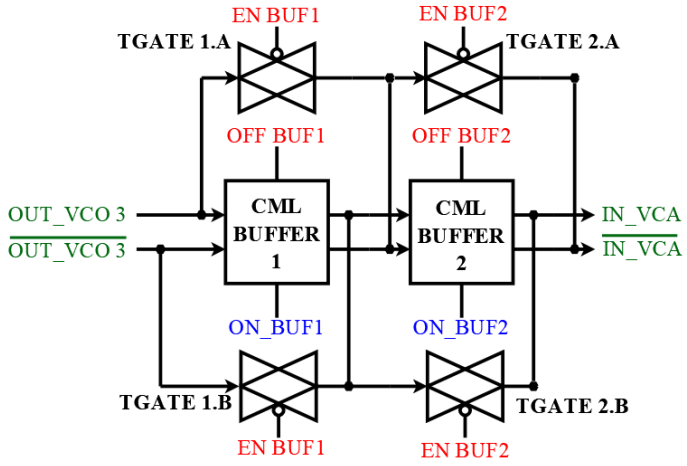
Regarding the transmitter block (b), the buffer stage is employed to transfer properly the VCO output voltage to the VCA. Figure 4.11 displays the buffer stage architecture. The buffer stage is composed of CML buffers, transmission gates (Tgate), push-pull, and AND logic gates. The CML buffers and push-pull are implemented using CML logic. Alternatively, the AND logic gate and transmission gate are implemented using classic CMOS logic. This buffer stage is reconfigurable to adapt its gain according to the central frequency of the targeted channel and also avoid the rise of odd harmonic for low central frequencies (3-6 GHz).

The signals "EN BUF1" and "EN BUF2" control if the CML buffers 1 and 2 are turned on, respectively. The signals "ON BUF", "OFF PP", "OFF BUF1" and "OFF BUF2" perform power management. In general, the signal "ON BUF" can power on all the CML circuits of the buffer stage.

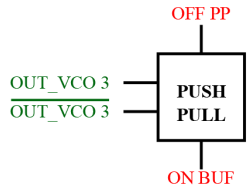
Since at least one CML buffer must be powered on ("ON BUF" must be enabled to active the push-pull), the architecture of the buffer stage allows 3 operating modes: one in which both CML buffers are turned on (mode A), one in which only the first CML buffer is turned on (mode B), and a last one in which only the second CML buffer is turned on (mode C). When a

CML buffer is set off, a pair of transmission gates is turned on, which enables the voltage signal to pass by them. Either the CML buffer is turned on, or the transmission gate is turned on.

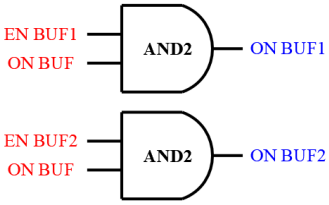
For instance, the signals "EN BUF1" and "EN BUF2" have high logic levels for mode A. CML buffers 1 and 2 are turned on in this case, while all four transmission gates are deactivated. Hence, the voltage signal passes by the two buffers. On the other hand, for mode C, the signal "EN BUF1" has a low logic level, unlike the signal "EN BUF2". In this case, the transmission gates 1.A and 1.B are activated, and the CML buffer 2 is turned on. Hence, the voltage signal passes by the first pair of transmission gates (1.A and 1.B) and then by the CML buffer 2. Table 4.2 summarizes the operation modes of the buffer stage.



(a) Core.



(b) Push-pull.



(c) Mode Manager.

Figure 4.11.: Buffer Stage architecture.

Table 4.2.: Buffer stage operation modes

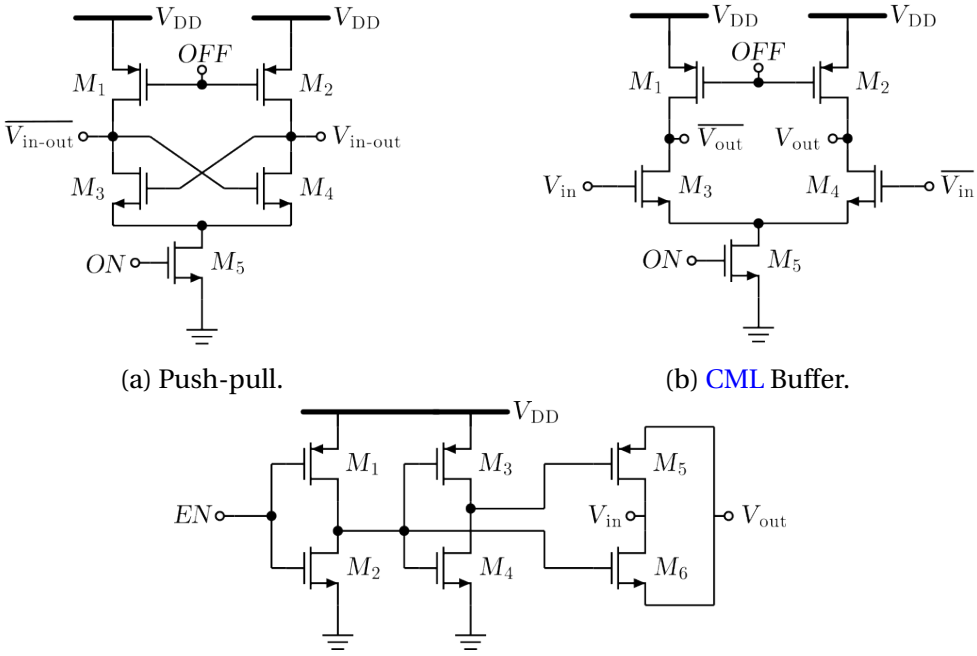
Mode	A	B	C
CML Buffer 1	On	On	Off
CML Buffer 2	On	Off	On
Transmission Gates 1.A and 1.B	Off	Off	On
Transmission Gates 2.A and 2.B	Off	On	Off

These operating modes allow the buffer stage to achieve performance for all FCC band (3.1-10.6 GHz). The mode A is more suitable for higher frequencies (6-10 GHz) or when a higher output amplitude is targeted. However, for lower frequencies (3-6 GHz), mode A may present a stronger third-harmonic, which can make the IR-UWB signal not meet the spectral requirements imposed by FCC. Modes B and C are more suitable for lower frequencies (3-6 GHz), especially because of their lower gain.

The two AND gates of Figure 4.11c enable and disable the CML buffers. The condition for enabling the CML buffer is that the input signals of the AND gate that drives the CML buffer should be at a high logic level.

The push-pull, placed between the VCO and the first CML buffer, has the goal of amplifying the VCO output current, thereby providing improved signal dynamics and driving capability. The push-pull is important and necessary because it allows the VCO output signal to drive properly the buffer stage and the VCA, mostly for lower oscillation frequencies. Otherwise, the transmitter output voltage levels will be very weak.

The transistor-level schematics of push-pull, CML buffer, and transmission gate are shown in Figure 4.12. Table 4.3 presents the transistor sizing of the circuits shown in Figure 4.12. All four transmission gates have the same transistor sizing. The transistors of the CML buffers are designed to achieve good transmission of the oscillations, especially for higher frequencies (10 GHz), where the output voltage of VCO is lower.



(a) Push-pull.

(b) CML Buffer.

(c) Transmission Gate.

Figure 4.12.: Buffer Stage transistor level Schematics.

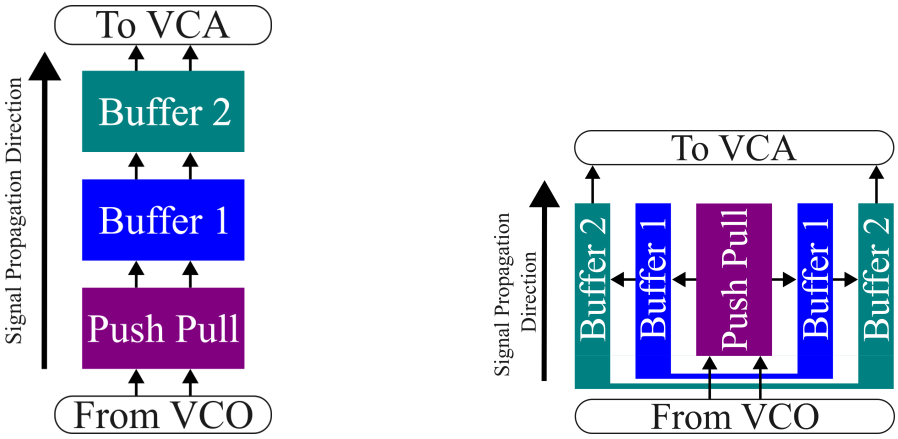
Table 4.3.: Buffer stage transistor sizing

Circuit	Width (µm)						Length (nm)
	M1	M2	M3	M4	M5	M6	All
Push-pull	1.2	1.2	6	6	6	-	30
CML Buffer 1	5	5	20	20	20	-	30
CML Buffer 2	10	10	40	40	40	-	30
Transmission Gate	2.4	1.2	2.4	1.2	2	2	30

Figure 4.13 shows two possible buffer stage layout floorplans. These floorplans focus on the CML circuits of the buffer stage. Firstly, the proposed layout floorplan (A) of Figure 4.13a has a strategy of chaining directly the push-pull, buffer 1, and buffer 2. This suggests that this

strategy is simple from a routing point of view. Meanwhile, to shorten the distance between the VCO and the VCA, thus shortening the metal connection length, a more compact layout floorplan is proposed in Figure 4.13b. Indeed, a shorter distance makes generating IR-UWB pulses with higher central frequency feasible.

The proposed layout floorplan (B) of Figure 4.13b has a strategy of splitting the buffers 1 and 2 layouts into 2 parts. The strategy of floorplan B is chosen because it is more compact despite being more complex from a routing point of view.



(a) Floorplan A. (b) Floorplan B.

Figure 4.13.: Possible buffer stage layout floorplans.

Figure 4.14 shows the layout of the buffer stage. The transmission gates (brown) are placed at the top of Figure 4.14 and closer to the CML buffers to reduce the interconnection length. Since the buffer stage is composed of CML circuits, the layout of the core of the buffer stage is balanced. Moreover, the interconnections within the core of the buffer stage use the thickest metal layer available to achieve a lower propagation delay time. Finally, the ground and supply voltage metal layers are distributed over the buffer stage layout to guarantee a good supply voltage level all along the layout.

4.5. Voltage-Controlled Amplifier

Finally, the Voltage-Controlled Amplifier (VCA), which is block (c), modulates the amplitude of oscillations coming from the output of the buffer stage to achieve the targeted continuous envelope. Figure 4.15 shows the architecture and transistor level schematic of the VCA.

As indicated earlier, the VCA gain is controlled here by an external source through "IN RF", such as an AWG. Thus, the VCA can perform an Amplitude Modulation (AM) on the VCA input oscillations. Besides, this architecture allows the compensation of PVT variations by modifying the envelope gain generated by the Arbitrary Waveform Generator (AWG).

Moreover, the signal "OFF VCA" performs power management of the VCA. It can be noticed that the architecture displayed in Figure 4.15b is the same architecture than the CML buffer (Fig. 4.12b). The difference is in the nature of the signal that drives the transistor gate M5. Indeed, the signal "ON" of Figure 4.12b is digital, while the signal "IN RF" is analog.

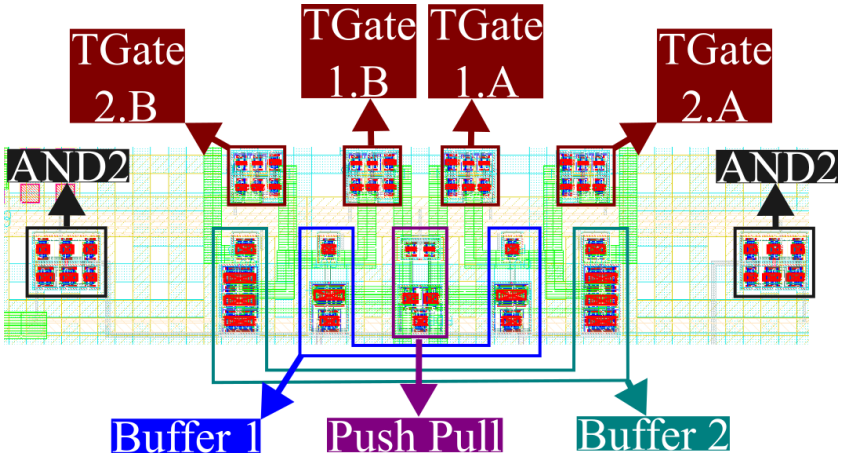
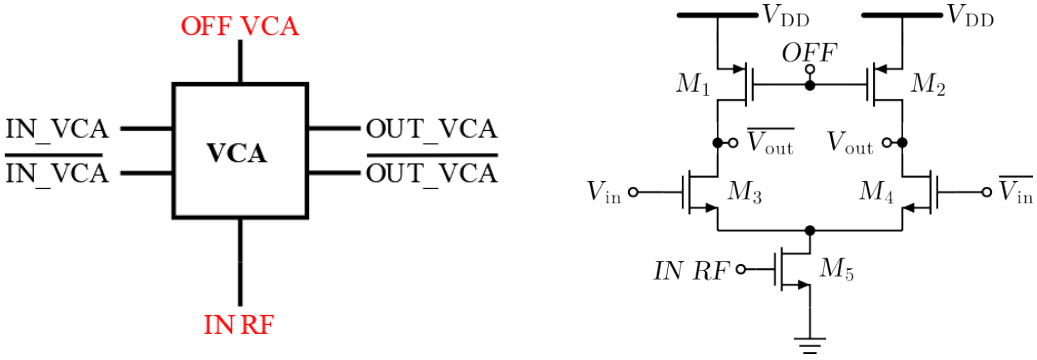


Figure 4.14.: Buffer stage layout.



(a) Architecture.

(b) Transistor level schematic.

Figure 4.15.: VCA architecture and transistor level schematic.

Table 4.4 shows the transistor sizing of the VCA. The amplifier gain is tuned through the transistor M5 which is the current source. The transistor sizing has been done to reach a good voltage level at the output of the VCA, mostly in higher frequencies, with the available AWG. For instance, the available AWG for measurement is the AWG70001 of Tektronix [81]. It provides a maximum peak voltage of 0.5 V on a high impedance (0.25 V on a 50 Ω). Given the AWG output voltage specifications, the transistors M3, M4, and M5 have also a larger width compared to the transistors of the buffer stage.

Table 4.4.: VCA transistor sizing

Width (µm)					Length (nm)
M1	M2	M3	M4	M5	All
32	32	160	160	320	30

Figure 4.16 shows the layout of the VCA followed by the coupling capacitor. Since the VCA has been implemented using CML logic, the layout of the VCA should be balanced. The 2 PMOS transistors are placed next to the coupling capacitor. The interconnection between

the VCA and the coupling capacitor has been implemented using 2 stacked metal layers to has been implemented using 2 stacked metal layers to reduce the parasitic resistance of interconnection lines (these layers are the thickest among the available metal layers).

Besides, since the input "IN RF" is a radio-frequency input, the gate of transistor M5 is connected via a large and thick metal layer to mitigate the parasitic resistance. The ground and supply voltage metal layers are distributed over the VCA layout to ensure a good supply voltage level all along the layout, especially in the PMOS transistor source terminal.

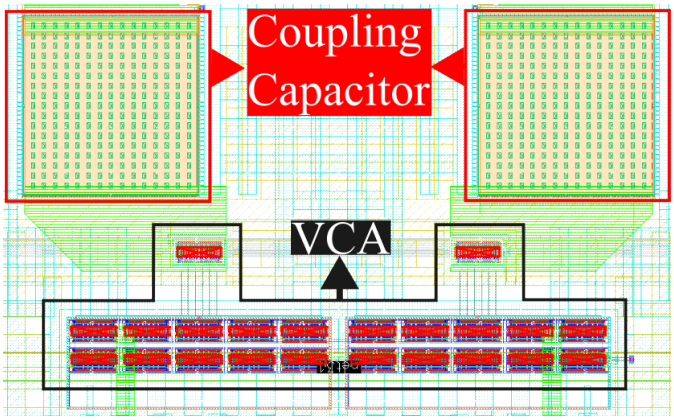


Figure 4.16.: VCA layout.

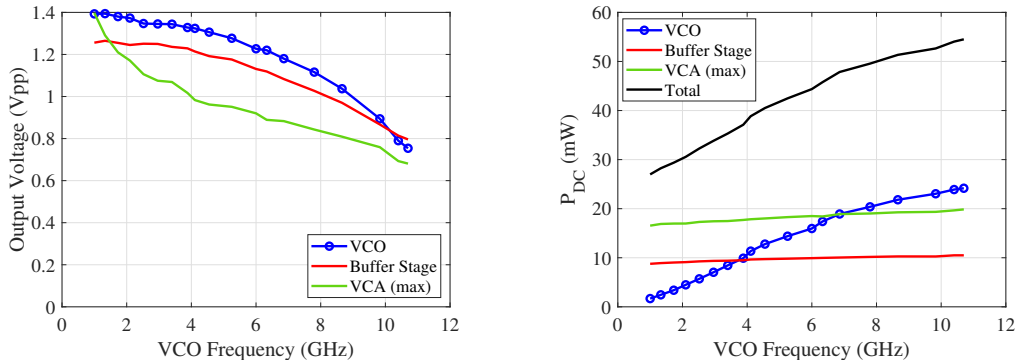
Figure 4.17 shows the post-layout simulation of both VCO, buffer stage, and VCA output voltage and always-on power consumption as a function of the frequency oscillation. It can be noted that Figure 4.17b also displays the total always-on power consumption (VCO, buffer stage, and VCA combined) and the VCO one. In this work, the buffer stage mode A is chosen because it enables better output voltage dynamics and higher side-lobe rejection. Buffer stage mode B or C is used when the minimum side-lobe rejection required by IEEE standards is not accomplished in buffer stage mode A.

From Figure 4.17a, it can be observed that VCA maximum output voltage decreases non-linearly when the oscillation frequency increases. The VCA has a minimum output level of 0.7 Vpp (78% of the supply voltage). This is a good performance, especially in higher frequencies where the parasitic effects are more present and imply a low-pass filter behavior.

From Figure 4.17b, the VCA maximum always-on power consumption is slightly dependent on the frequency oscillation. The VCA power consumption relies on the current source transistor biasing (M5 of Figure 4.15b).

Figure 4.18 gives the post-layout simulation of VCA output voltage, gain, and always-on power consumption as a function of the voltage signal "IN RF" for several values of oscillation frequencies. The simulated VCO frequencies correspond approximately to extremities (3.1 and 10.6 GHz) and the center (6.85 GHz) of the FCC band.

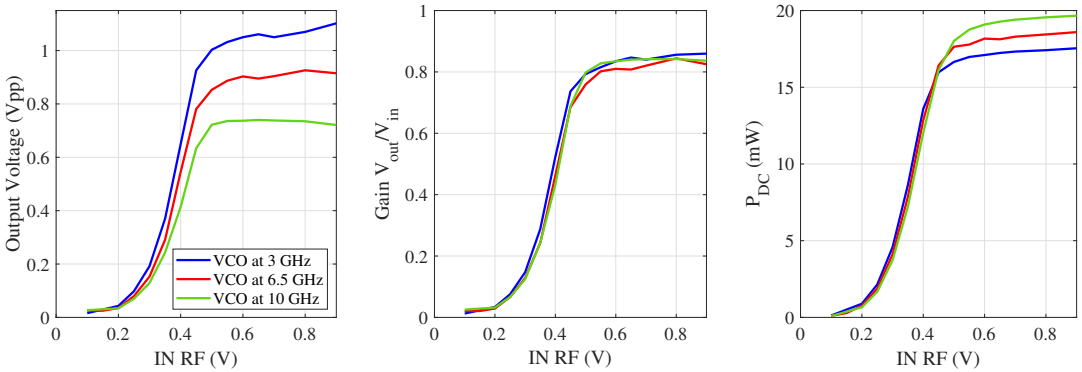
From Figure 4.18a, there is a saturation of the VCA output voltage when "IN RF" is greater than 0.5 V and a linear behavior when "IN RF" is between 0.3 V and 0.5 V. When "IN RF" is lower than 0.25 V, the VCA output voltage is too low (lower than 100 mVpp) because the signal "IN RF" applied in NMOS transistor M5 gate of Figure 4.15b is lower than its threshold voltage and so is not high enough to make the NMOS transistor work outside the cut-off region.



(a) Output voltage. (b) Mean Power consumption.

Figure 4.17.: VCA output voltage and always-on power consumption as a function of the frequency oscillation (Buffer Stage Mode A, IN RF = 0.9 V.).

Thanks to its constant gain according to the frequency (figure 4.18b), the maximum VCA output voltage is around 1.1 Vpp, 0.93 Vpp, and 0.74 Vpp for VCO frequencies of 3 GHz, 6.5 GHz, and 10 GHz, respectively.



(a) Output voltage. (b) Gain. (c) Mean Power Consumption.

Figure 4.18.: VCA output voltage, gain, and always-on power consumption as a function of the signal IN RF (Buffer Stage Mode A).

From Figure 4.18c, the VCA always-on power consumption have closer values for different VCO frequencies. However, within the saturation region, the VCA always-on power consumption is slightly greater when the oscillation frequency is greater within the linear region. The maximum VCA always-on power consumption is around 17.54 mW, 18.59 mW, and 19.67 mW for VCO frequencies of 3 GHz, 6.5 GHz, and 10 GHz, respectively. Therefore, the VCA performance depends more on the voltage levels applied into VCA inputs rather than the oscillation frequency.

4.6. Global Layout

As indicated earlier, the IR-UWB transmitter has been implemented and fabricated in a 28-nm CMOS process of TSMC, with a supply voltage of 0.9 V. All NMOS transistors bulk terminals are connected to the ground, while all PMOS transistors bulk terminals are connected to the positive supply voltage. Figure 4.19 displays the IR-UWB transmitter's global layout with the 29 required pads. Its surface without pads after the 10% shrink is 738 µm x 198 µm (i.e. 0.146 mm²), whereas its surface with pads the surface with pads is 1 mm x 0.45 µm (i.e. 0.45 mm²).

In addition, there are 3 dedicated power supplies: one for VCO, one for the buffer stage, and one for VCA. Thereby, 3 matrixes of power supply decoupling capacitors have been implemented on the core surface that is not occupied by the IR-UWB transmitter. Regarding post-layout simulations or measures, the circuit load is composed of an impedance of 2 × 50 Ω.

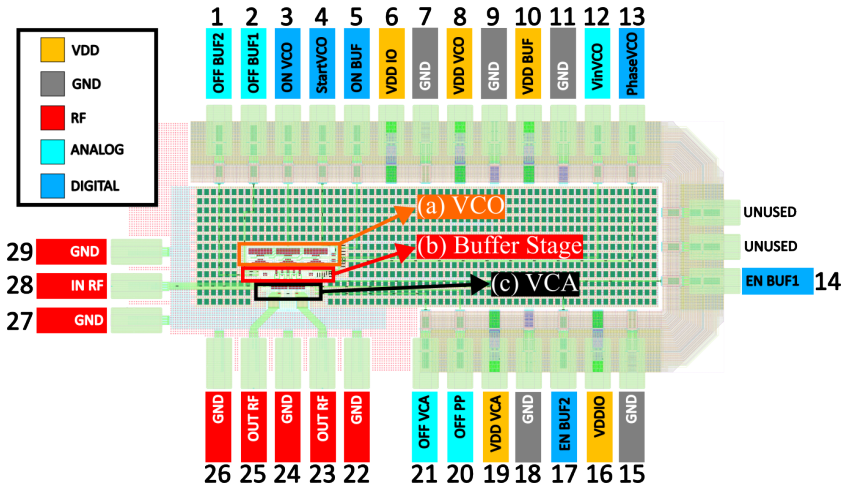


Figure 4.19.: IR-UWB Transmitter layout displaying the bond pad pins.

The fabricated chip was encapsulated in a QFN-40 package, which has 40 pins. Figure 4.20 depicts the wire bonding plan of the IR-UWB transmitter. The IR-UWB transmitter layout is placed at a corner of the QFN-40 package to reduce the wire bonding length of the RF input and output (red pads). The reason for this is because the longer the bonding wires are, the higher their parasitic elements values are, and also, the higher their attenuation is.

Besides, the IR-UWB transmitter layout is placed such that the differential "OUT RF" bonding wires have the same length. Consequently, the RF output differential signals have the same propagation time. This has to be done to ensure that these RF signals present a phase opposition. It is worth highlighting that ensuring a phase opposition for these signals is important for the differential output frequency response, mostly regarding even harmonic and also side-lobe rejection.

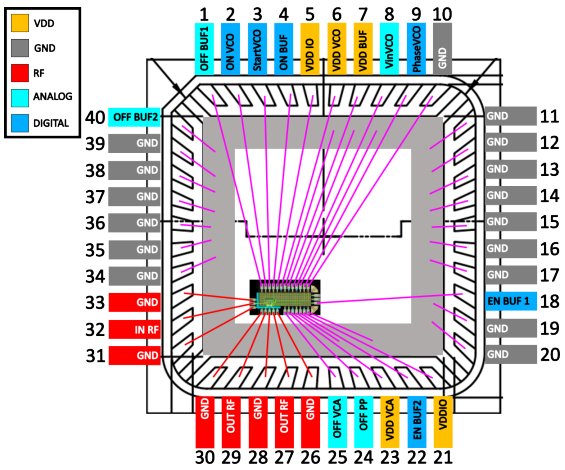


Figure 4.20.: Wire bonding plan of the proposed IR-UWB Transmitter.

4.7. Test Setup and Measurements Results

4.7.1. Test board design

To test the prototype chip, a two-layer Rogers equivalent Printed Circuit Board (PCB) has been designed. Figure 4.21 depicts photos of the assembled test PCB. The PCB substrate is ZYF255DA. All three transmitter blocks (a to c) use a common ground plane. The TSMC 28 nm chip packaged in a QFN-40 is connected to the PCB using an appropriate socket. The use of a socket QFN-40 allows to easily change the chip to be tested.

The ground plane has been implemented in the bottom layer of the PCB, and capacitors were placed as close as possible to the chip to provide low- and high-frequency decoupling. The lines connecting the RF input and output signals to the chip are the most critical. For this reason, these signal lines are 50 Ω microstrip transmission lines.

From Figure 4.21, it can be noticed that multiple switches were implemented. This has been done to reduce the number of voltage supplies required during the chip measurements and also make it easier. Two types of switches are employed. One allows a switch between the ground, the positive supply voltage, and an external signal. This signal can also be supplied

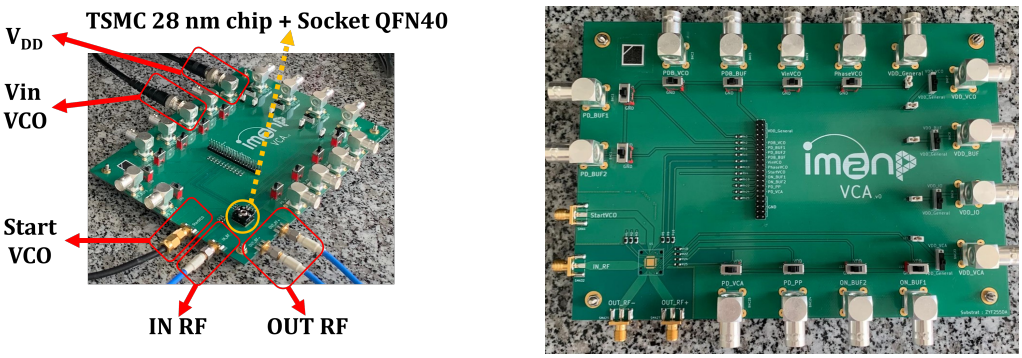


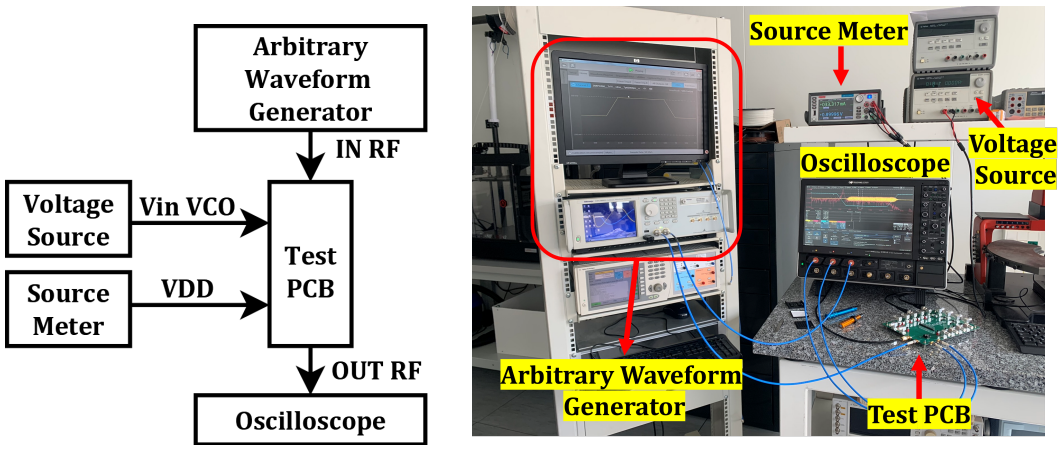
Figure 4.21.: Test PCB of the of the proposed IR-UWB Transmitter.

by a voltage source or a microcontroller combined with a voltage level shifter. This is valid for all analog and digital input signals (Fig. 4.20), except for the "Start VCO," which requires a periodic signal. On the other hand, the other type of switch enables a switch between the common power supply and a dedicated power supply. The dedicated power supply is useful to separately measure the power consumption of a circuit block.

4.7.2. Test Setup

Figure 4.22 displays the test bench of the chip prototype. The "IN RF" signal is provided by the Arbitrary Waveform Generator AWG70001 of Tektronix [81]. This AWG can generate periodic waveforms with a sample rate of 50 GS/s and a maximum amplitude of 0.5 V following a data file. The generation of the data files has been done using MATLAB scripts. Thus, scripts have been developed to generate the appropriate IR-UWB pulse in terms of duration and shape (Fig. 4.1; the pulse shape can be controlled through the symmetry and surface factors). Therefore, the AWG enables the generation of nanosecond order pulses with the shape of the addressed envelopes in Chapter 2.

The supply voltage of 0.9 V is provided by the source meter 2450 of Keithley [82], which allows the power consumption to be precisely measured, whereas a standard voltage source provides the "Vin VCO" signal. Finally, the RF output signals have been measured using the Teledyne LeCroy Wavemaster 813Zi-B oscilloscope [83]. It has 4 port channels, bandwidth up to 13 GHz, a sample rate of 40 GS/s, and can obviously perform the Fast Fourier Transform (FFT) of the differential RF output pulses.



(a) Diagram. (b) Photo.

Figure 4.22.: Test bench of the measured IR-UWB transmitter.

4.7.3. Measurement Results

This sub-section presents the measurement results of the proposed multi-standard IR-UWB transmitter. It is divided into two parts. In a first time, the implemented IR-UWB transmitter characterization is addressed. The circuit tuning capabilities are analyzed as a function of

the VCO input frequency control voltage ("Vin VCO") and VCA RF input gain control voltage ("IN RF"). A comparison between the measurement and post-layout results is also performed. In a second time, pulse examples compliant with IEEE channels are addressed. For each pulse example, it is verified if the generated pulse is compliant with the spectral requirements imposed by FCC (minimal bandwidth of 500 MHz and mask) and IEEE 802.15.4 and 802.15.6 standards (minimal side-lobe rejection of 18 and 20 dB, respectively).

During the measurements, the VCO is always on. It is worth highlighting that the buffer stage mode is set to A (all CML buffers are turned on) to achieve a better output voltage dynamic. Besides, the measured cable attenuation of 1 dB has been taken into account.

4.7.3.1. Characterization

Figure 4.23 displays the post-layout simulated and measured VCO frequency as a function of the VCO input ("Vin VCO"). Figure 4.24 depicts the measurement and post-layout simulation of the pulse synthesizer output voltage and always-on power consumption as a function of the oscillation frequency.

From Figure 4.23, it can be observed that the measured oscillation frequencies are between 0.7 GHz and 10.6 GHz. Hence, the prototype chip can cover all the FCC band (3.1-10.6 GHz). This wide tuning range ratifies the great choice of implementing a ring oscillator in a multi-band design. Comparing the measurement and post-layout simulation results, it can be noticed that they are very similar and also that simulations and measurements match. Indeed, the average measured VCO gain is around -22.5 GHz/V. Meanwhile, the average simulated VCO gain is around -23.4 GHz/V. Thereby, the layout design strategy of the VCO seems good.

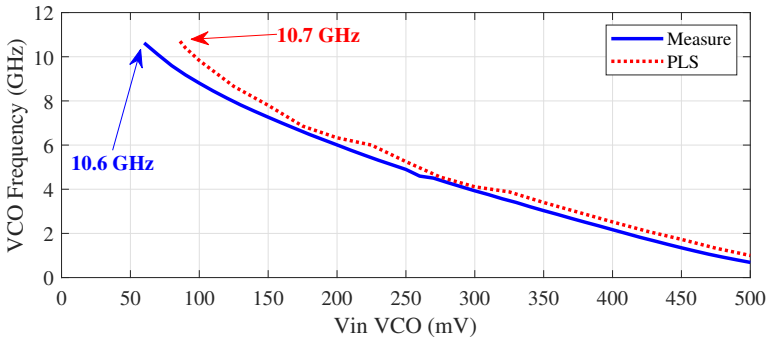
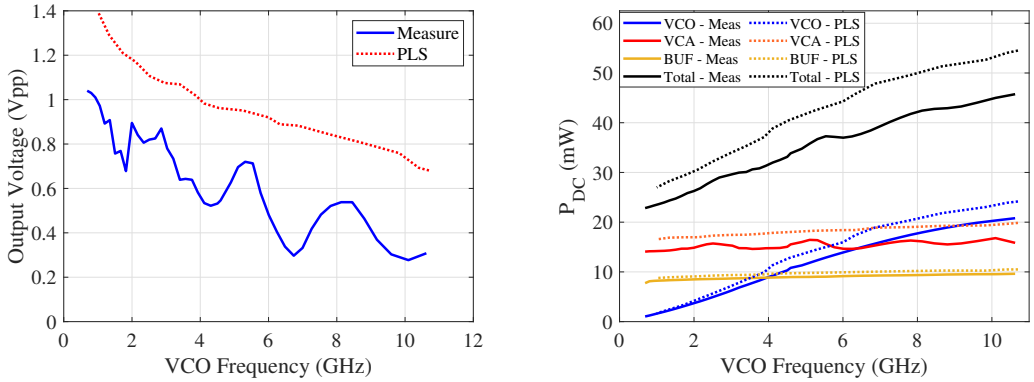


Figure 4.23.: Measured and simulated VCO frequency as a function of the VCO input voltage (Buffer Stage Mode A, IN RF = 0.9 V.).

From Figure 4.24a, it can be observed that the measured output voltage is between 0.3 Vpp and 1 Vpp. It tends to decrease with an increasing oscillation frequency. Comparing the measurement and post-layout simulation results, it can be noticed that the measured output voltage is weaker. Despite the lower level, the measured output voltage is high enough for the generation of IR-UWB pulses addressing the IEEE standards.

From Figure 4.24b, the total always-on power consumption stays approximately proportional to the oscillation frequency. As expected, the VCO power consumption is the most dependent on the oscillation frequency, while the blocks (b) to (c) have a power consumption

weakly sensitive to the oscillation frequency. Comparing the measurement and post-layout simulation results, it can be seen that the measured power consumption is lower for all oscillation frequencies, mostly regarding the VCO. This must be due to the lower dynamic of every RF signal during measurement compared to simulations.



(a) Output voltage.

(b) Always-on power consumption.

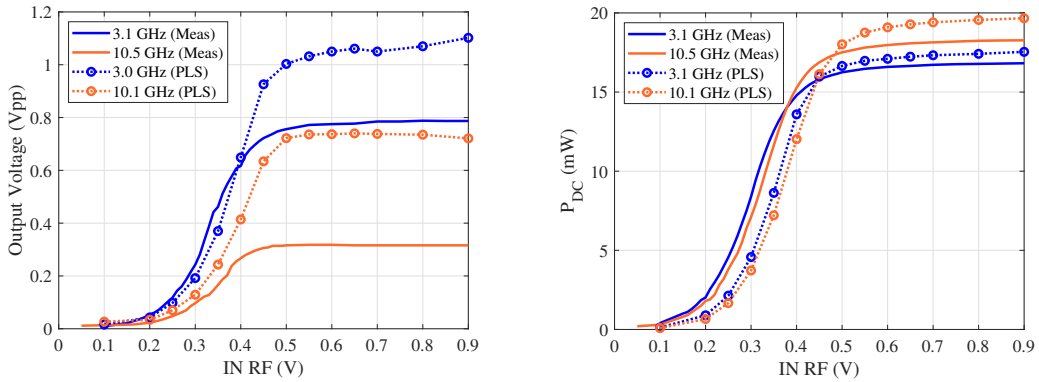
Figure 4.24.: Measured and simulated output voltage and always-on power consumption as a function of the oscillation frequency (Buffer Stage Mode A, IN RF = 0.9 V.)

Figure 4.25 gives the measured and post-layout simulated VCA output voltage and always-on power consumption as a function of the voltage "IN RF" for two values of oscillation frequencies. A saturation when "IN RF" is greater than 0.5 V can be observed as expected. However, comparing the measurement and post-layout simulation results, the measured output voltage is lower, mostly in higher frequencies. For instance, the maximum VCA measured output voltage is around 0.78 Vpp and 0.32 Vpp for VCO frequencies of 3.1 GHz and 10.5 GHz, respectively. Meanwhile, the maximum VCA simulated output voltage is around 1.1 Vpp and 0.74 Vpp for the VCO frequencies of 3 GHz and 10.1 GHz.

From Figure 4.25b, the measured and post-layout simulated power consumption are quite close to the results displayed in Figure 4.25. The measured VCA always-on power consumption is 16.82 mW and 18.27 mW for VCO frequencies of 3.1 GHz and 10.5 GHz, respectively. Meanwhile, the maximum simulated VCA always-on power consumption is 17.54 mW and 19.67 mW for VCO frequencies of 3 GHz and 10.1 GHz, respectively.

Since Figure 4.25a shows a VCO output voltage with a non-linear behavior regarding the applied input signal "IN RF", a linearization of VCA gain control should be done. The objective is to achieve a matching between the targeted continuous envelope and the measured pulse envelope. This linearization is based on the pre-distortion of the AWG output signal. It is performed for the "IN RF" values between 0 V and 0.5 V since this voltage level range can be exploited by the Tektronix AWG70001 [81].

Figure 4.26 depicts the VCA gain pre-distortion diagram block. The generation of the data files for AWG and the pre-distortion are done in the MATLAB environment. The block Pre-distorter $g(x)$ should correspond to the reciprocal function of the VCA $f(z)$. To obtain the function $g(x)$, a non-linear interpolation of the reciprocal function of $f(z)$ has been



(a) Output voltage. (b) Always-on power consumption.

Figure 4.25.: Measured and simulated VCA output voltage and always-on power consumption as a function of the signal IN RF (Buffer Stage Mode A).

performed, where a 6th-order polynomial interpolation was employed. Therefore, the pre-distorter function $g(x)$ can be written as follows:

$$g(x) = -99.92x^6 + 264.54x^5 - 269.9x^4 + 134.35x^3 - 33.93x^2 + 4.33x + 0.048 \tag{4.1}$$

Figure 4.27 depicts the VCA gain control linearization process based on pre-distortion. From Figure 4.27c, it can be observed a predominant linear behavior. Hence, a pre-distortion using a 6th-order polynomial interpolation of the reciprocal function of the VCA $g(x)$ achieves satisfactory results here.

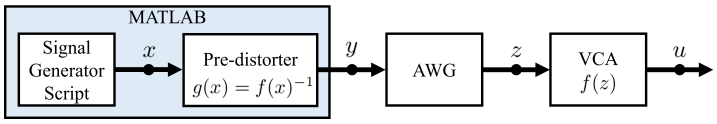
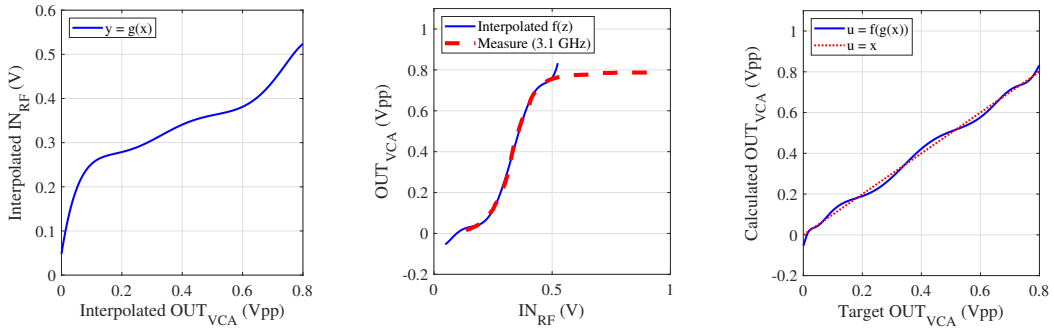


Figure 4.26.: VCA gain pre-distortion diagram block.



(a) Pre-distortion $g(x)$ (b) VCA $f(z)$ (c) Pre-distortion+VCA $f\left(g(x)\right)$

Figure 4.27.: VCA gain control linearization process based on pre-distortion

4.7.3.2. Pulse synthesis

Regarding the IR-UWB pulse synthesis, Figure 4.28 shows the IR-UWB measured pulse waveforms which try to address IEEE 802.15.4 channels 1 to 15, in addition to the signals "IN RF" generated by the Tektronix AWG70001. Table 4.5 shows the IR-UWB measured pulse parameters, in addition to measured output voltage, emitted energy, and estimated spectral efficiency.

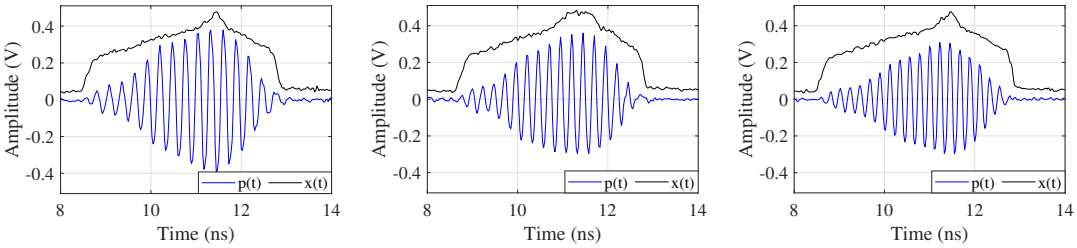
Figure 4.29 and 4.30 display the measured IR-UWB pulses for all the 499.2 MHz channels of the IEEE standard 802.15.4 within the FCC band and ETSI band, respectively. Figure 4.31 shows the measured IR-UWB pulses for all the large-bandwidth channels of the IEEE standard 802.15.4.

From Figure 4.28 and Table 4.5, the measured IR-UWB pulses addressing the 499.2 MHz IEEE channels have a duration between 4 ns and 4.4 ns, while the IR-UWB pulses addressing the large-bandwidth IEEE channels have a duration between 1.7 ns and 2.5 ns. The pulse duration choice is done considering the IEEE spectral masks and the minimal bandwidth BW_{-10dB} of 500 MHz imposed by FCC. About the symmetry, the measured IR-UWB pulse envelopes are generally asymmetrical to optimize side-lobes rejection as demonstrated in Chapter 2.

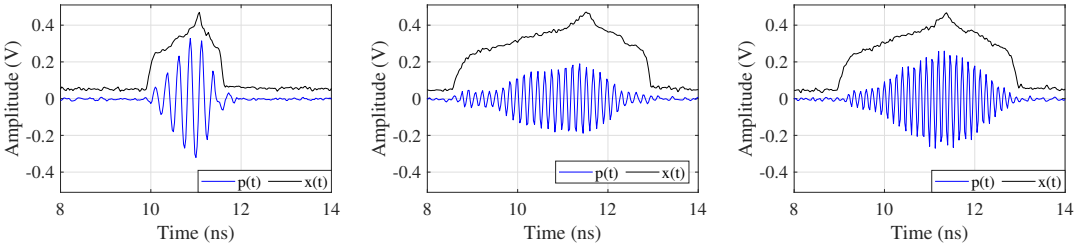
Finally, the measured pulse output voltage is between 0.34 Vpp and 0.76 Vpp, and the peak-to-peak voltage tends to be lower when the pulse central frequency increases. The measured pulse emitted energy is also between 0.11 pJ and 1.58 pJ (the pulse emitted energy is higher when the output voltage is greater, when the pulse duration is longer, and when the surface factor β is greater).

Table 4.5.: IR-UWB measured pulse parameters and performance.

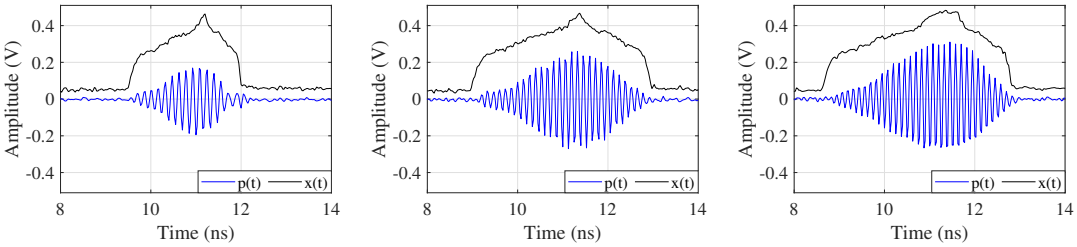
Ch.	f_c (MHz)	BW (MHz)	Buffer Stage Mode	τ (ns)	α	β	Vpp (V)	E_p (pJ)	Side-Lobe Rejection (dB)	Spectral Efficiency (%)
1	3494.4			4.4	0.68	0	0.78	1.50	30.39	54.71
2	3993.6	499.2	A	4.2	0.68	0.12	0.66	1.04	29.39	56.4
3	4492.8			4.4	0.68	0	0.61	0.81	29.98	52.7
4	3993.6	1331	A	1.7	0.68	0	0.65	0.38	24.46	48.0
5	6489.6	499.2	A	4.4	0.68	0	0.38	0.32	25.35	55.1
6	6988.8			4.4	0.68	0	0.36	0.30	28.49	52.3
7	6489.6	1081	A	2.5	0.68	0	0.36	0.17	22.53	46.3
8	7488			4.0	0.60	0	0.53	0.56	29.90	56.7
9	7987.2	499.2	A	4.2	0.68	0.12	0.58	0.87	31.78	53.5
10	8496.4			4.2	0.68	0.12	0.61	0.83	29.58	54.6
11	7987.2	1331	A	1.7	0.68	0	0.52	0.26	25.89	48.6
12	8985.6			4.4	0.68	0	0.46	0.44	30.36	52.0
13	9484.8	499.2	A	4.0	0.60	0	0.35	0.25	25.73	59.2
14	9984			4.4	0.68	0	0.26	0.20	25.43	56.2
15	9484.8	1355	A	1.7	0.68	0	0.34	0.11	21.36	49.3



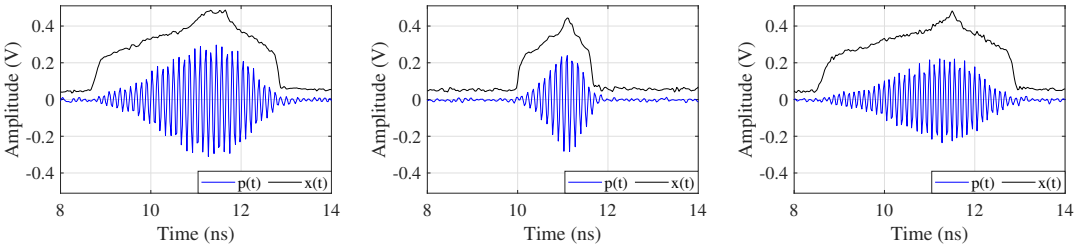
(a) Channel 1 (b) Channel 2 (c) Channel 3



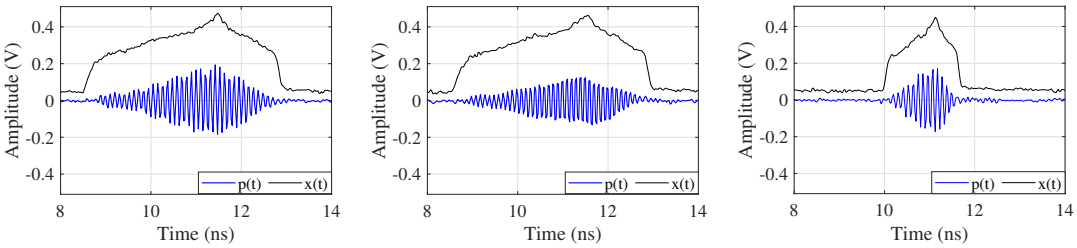
(d) Channel 4 (e) Channel 5 (f) Channel 6



(g) Channel 7 (h) Channel 8 (i) Channel 9



(j) Channel 10 (k) Channel 11 (l) Channel 12



(m) Channel 13 (n) Channel 14 (o) Channel 15

Figure 4.28.: Measured output voltage and signal "IN RF" for IEEE 802.15.4 channels (Buffer Stage Mode A)

From Figure 4.29, it can be observed that the 11 measured output spectra are compliant with the IEEE 802.15.4 standard and FCC handheld mask. Moreover, they meet the minimal bandwidth BW_{-10dB} of 500 MHz required by FCC. From Figure 4.30, it can be noticed that the measured output spectra addressing IEEE channels 6, 8, and 9 fit into the ETSI spectral mask. Nevertheless, the measured output spectrum addressing IEEE channel 5 overlaps a little the ETSI spectral mask (below 6.5 GHz). Indeed, the ETSI mask requires a side-lobe suppression of 28.7 dB below 6.5 GHz, whereas the measured rejection is 25.35 dB.

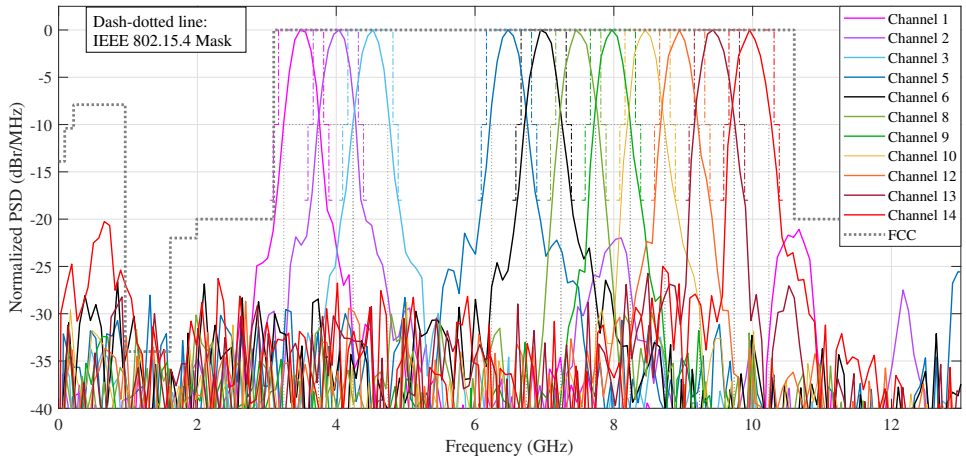


Figure 4.29.: Measured output spectrum for 499.2 MHz Channels with FCC regulatory mask (Buffer Stage Mode A).

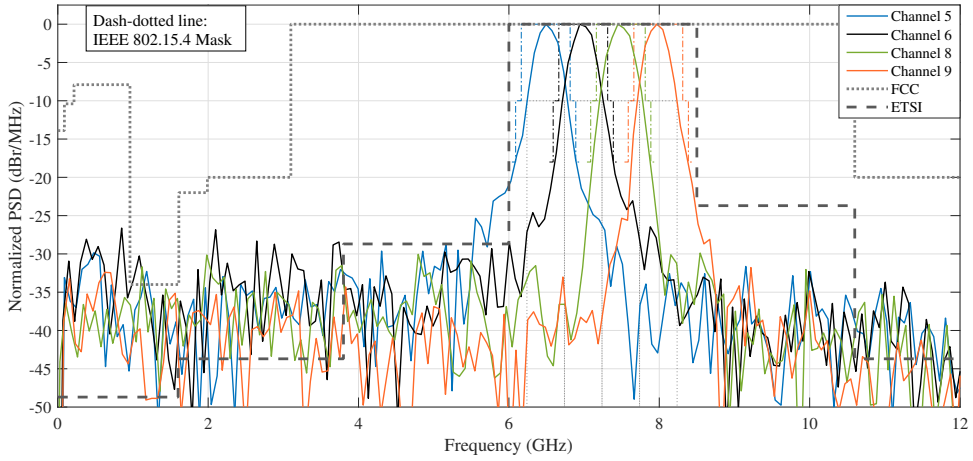


Figure 4.30.: Measured output spectrum for 499.2 MHz Channels with FCC and ETSI regulatory masks (Buffer Stage Mode A).

According to Table 4.5, the output spectra depicted in Figure 4.29 achieve a side-lobe rejection ranging from 25.35 dB to 31.78 dB and an estimated spectral efficiency between

51.9% and 59.2%. It must be highlighted that the measured trapezoidal pulse addressing IEEE channel 9 achieved the best side-lobe rejection and channel 13 the best spectral efficiency.

From Figure 4.31, it can be seen that the 4 measured output spectra are compliant with the masks of the IEEE 802.15.4 standard wide channels and the minimal bandwidth BW_{-10dB} of 500 MHz imposed by FCC. As shown in Table 4.5, the output spectra in Figure 4.31 exhibit a side-lobe rejection of 21.36-24.46 dB and a spectral efficiency of 46.3-49.3%. These values of spectral efficiency are lower than the ones of spectra of Figure4.29.

Therefore, the asymmetrical envelope (triangular or trapezoidal) is an excellent choice for pulse shaping because it achieves great side-lobe rejection and good spectral efficiency. Moreover, the combination of the ring oscillator with an asymmetrical envelope has also proven to be a relevant architecture for a multi-standard and multi-band design.

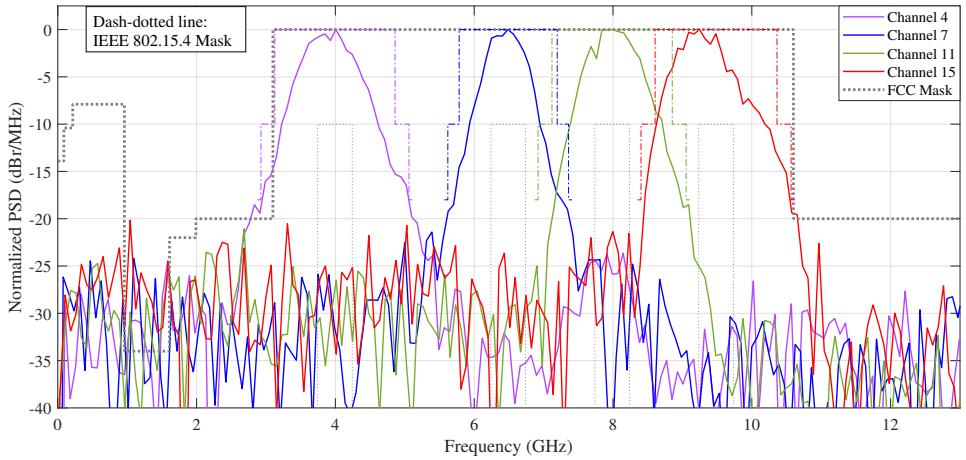


Figure 4.31.: Measured output spectrum for large-bandwidth Channels with FCC regulatory mask (Buffer Stage Mode A).

Table 4.6 presents the measured power consumptions for a PRF of 10 MHz and 100 MHz. This Table shows the power consumption of every block (VCO, buffer stage, and VCA). In addition, the energy consumption per pulse is given. The measured power consumption P_c of the circuit can be expressed as function of the Pulse Repetition Frequency (PRF) as follows :

$$P_c = E_{ac} \cdot PRF + P_{0Hz} + P_{DC-AlwaysOn} \tag{4.2}$$

where $P_{DC-AlwaysOn}$ is the always-on power consumption, E_{ac} the energy consumption per pulse, P_{0Hz} the static power.

From Table 4.6, it can be observed that the VCO and buffer stage always-on power consumption are higher when increasing the pulse central frequency, as shown in Figure 4.24b. Meanwhile, the VCA power consumption is slightly sensitive to the oscillation frequency. The VCA power consumption is lower when the pulse duration τ and the surface factor β are decreased. For lower frequencies, the major part of the IR-UWB power consumption comes from the Buffer Stage, whereas for higher frequencies, the major part comes from the VCO. Among the three circuit blocks, the VCA is the one having the lowest power consumption thanks to the power gating due to the gate voltage modulation.

Finally, the measured static power P_{0Hz} for the VCO, buffer stage, and VCA are 22.68 µW, 5.13 µW, and 3.88 µW. As a result, the total measured static power is 30.69 µW (Fig. 4.32).

Table 4.6.: IR-UWB transmitter performance in terms of the power consumption

Ch.	f_c (MHz)	BW (MHz)	P_{DC} (mW) Always-on		P_c (mW) @PRF = 10 MHz		P_c (mW) @PRF = 100 MHz		E_{AC} (pJ/pulse)
			VCO	Buffer Stage	VCA	Total	VCA	Total	Total
1	3494.4	499.2	7.28	8.67	0.50	16.16	3.93	19.49	197.7
2	3993.6		14.46	9.00	0.45	23.80	3.58	26.87	211.0
3	4492.8		9.80	8.78	0.49	18.77	3.85	22.01	223.3
4	3993.6	1331	8.58	8.72	0.26	17.26	1.59	18.54	187.8
5	6489.6	499.2	14.46	9.00	0.45	23.80	3.58	26.87	269.4
6	6988.8		15.30	9.05	0.47	24.59	3.77	27.66	280.15
7	6489.6	1081	14.46	9.00	0.31	23.47	2.16	25.15	255.23
8	7488		16.24	9.10	0.42	25.61	3.42	28.49	286.65
9	7987.2	499.2	17.05	9.14	0.47	26.38	3.90	29.66	300.0
10	8496.4		17.86	9.20	0.45	27.23	3.81	30.48	307.3
11	7987.2	1331	17.05	9.14	0.23	26.13	1.43	27.25	275.3
12	8985.6		18.51	9.25	0.45	27.91	3.65	31.02	313.3
13	9484.8	499.2	19.06	9.30	0.44	28.50	3.69	31.59	319.7
14	9984		19.52	9.34	0.44	28.99	3.74	32.09	325.3
15	9484.8	1355	19.06	9.30	0.23	28.25	1.52	29.50	297.9

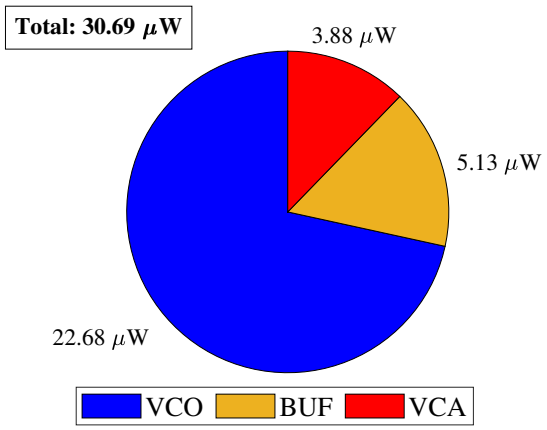


Figure 4.32.: Measured static power P_{0Hz} of the proposed IR-UWB transmitter.

4.8. Conclusion

In this chapter, it was presented the design of a multi-standard IR-UWB transmitter based on the frequency transposition pulse synthesis employing a ring oscillator. It has been implemented and fabricated in a 28 nm CMOS technology of TSMC, with a supply voltage of 0.9 V. The proposed circuit has been designed to generate pulses addressing the IEEE channels in the 3.1-10.6 GHz frequency band while complying with the spectral requirements imposed by FCC and IEEE standards. The proposed transmitter has three main blocks: a VCO, a buffer stage, and a VCA.

The ring oscillator architecture has been chosen because it has a larger frequency tuning range and, consequently, can address a higher number of addressed IEEE channels. The proposed transmitter has pulse shaping capabilities through the designed VCA combined with a pre-distortion technique. This allows the control of the emitted spectrum, making it fit into the spectral masks imposed by the IEEE standard, in addition to improving the side-lobe rejection and spectral efficiency.

In Table 4.7, a comparison between the proposed IR-UWB transmitter and the IR-UWB transmitters addressed in Chapter 3 is done. From this Table and the addressed measurements results presented in this section, the proposed IR-UWB transmitter achieved the largest central frequency (1-10.6 GHz) and the largest number of addressed IEEE 802.15.14 channels. To the best of our knowledge, it is the only one capable of addressing all the 15 IEEE 802.15.14 channels within the FCC band. Indeed, the proposed circuit can synthesize pulse addressing the 499.2 MHz IEEE channels, in addition to all large-bandwidth IEEE channels.

Moreover, the proposed circuit achieves a side-lobe rejection of 31.8 dB. This offers an excellent side-lobe rejection compared to the state-of-the-art IR-UWB transmitters. The proposed circuit has higher spectral efficiency regarding the large-bandwidth IEEE channels than all IR-UWB transmitters of the state-of-art capable of addressing large-bandwidth IEEE channels, except for the transmitter of [52]. It follows that the asymmetrical envelope can give a higher side-lobe rejection in addition to a higher spectral efficiency for large-bandwidth pulses. Regarding power consumption, the proposed circuit presents, in general, a higher power consumption than the transmitters reported in Chapter 3. The main reason for this is that the VCO and buffer stage were set always on during the measurements. Only the VCA has a power gating.

In conclusion, the proposed IR-UWB transmitter provides the best solution in terms of central frequency range and number of addressed channels, adhering to both IEEE 802.15.4 and IEEE 802.15.6 standards. Furthermore, it achieves excellent side-lobe rejection compared to existing solutions. This improvement is obtained thanks to the use of asymmetrical envelopes associated with the compensation of the non-linear VCA gain (pre-distortion).

Table 4.7.: Performance comparison with state-of-the-art IR-UWB transmitters

	Vauché TCSI'17 [21]†	Haapala JSSC'20 [51]	Miranda CICC'20 [52]	Chen RFIC'22 [54]&	Chen ISSCC'22 [57]†	Song VLSI'23 [58]†	Phan TCSI'08 [61]	Schmickl TCSI'20 [62]	Zhang LMWT'22 [63]	Ryckaert JSSC'07 [65]	Streel JSCC'17 [66]	Bechthum ESSCIRC'23 [67]	Singh JSSC'21 [68]	This Work
Process (nm)	130	65	65	28	40	28	180	180	28	90	28 (FD-SOI)	22 (FD-SOI)	28	28
Supply Voltage (V)	1.2	1.2	1.2	0.9	1.25	0.9	1.5	1	0.9	1	0.9	0.8	0.9	0.9
Core Area (mm²)	0.11	0.22	N/A	0.25	N/A	1.33	0.3	0.25	0.21	0.07	0.55	0.09	0.15	0.15
Die Area (mm²)	1.31	1.1	0.7	N/A	8.8	N/A	0.66	3.91	N/A	N/A	0.93	1.0	2.37	0.45
Architecture	Delay Line	Delay Line	Delay Line	LO (External)	LO (Mixer)	LO	LO (LC Tank)	LO (LC Tank)	LO (LC Tank)	LO (Ring)	LO (Ring)	LO (Ring)	LO (Ring)	LO (Ring)
Pulse Shaping	Delay Line	Delay Line	Delay Line	Delay Line	LUT Flip-flop	Delay Line	LO Modulation	LO Modulation	Counter	PA-FLL	Counter	Delay Line	Delay Line	AWG♠
Modulation	OOK DB-BPSK	OOK	OOK	OOK BPSK	N/A	BPSK	OOK	N/A	BPSK	BPSK	2-PPM BPSK	BPSK	BPSK	BPSK
Spectral compliance	FCC	ETSI	FCC	FCC	FCC	FCC	FCC	ETSI	FCC	FCC	FCC	FCC	FCC	FCC
Freq. Range (GHz)	3.1-4.9	6-8.5	3.6-7.5	4-9	6.5-10	6-9	3-5	6-8.8	5-10	3-10	3.5-4.5	3-9	3-10	1-10.6
Mod. BW (GHz)	1/1.3	0.5	1/1.3	0.5/1/1.3	0.5/1	0.5	0.5	0.5	0.5/1/1.3	0.5	0.5	0.5	0.5/1	0.5/1/1.3
Side-lobe rejection (dB)	18	30	23.8*	31	25*	31	18	18	21*	24*	23*	29	32	31.8
IEEE 802.15.4 Addressed Channels (Total)	4 (1)	5,6,8,9 (4)	4,7 (2)	2-12 (11)	5-15 (11)	5,6,8,9 10,12 (6)	1-3 (3)	5,6,8,9 (4)	5-15 (11)	1-3,5,6 8-10,12-14 (11)	1-3 (3)	1-3,5,6 8-10,12 (9)	1-14 (14)	1-15 (15)
IEEE 802.15.6 Addressed Channels (Total)	None (0)	3-6 (4)	None (0)	1-8 (8)	3-10 (8)	3-8 (6)	0-2 (3)	3-6 (4)	3-10 (8)	0-10 (11)	0-2 (3)	0-8 (9)	0-10 (11)	0-10 (11)
Spectral Eff. (%)* @BW = 499.2 MHz	-	[49.5-55.5]	-	[44.2-55.5]	[40.2-61.6]	[49.8-51]	[53.1-54.3]	48.2	63.5	56.3	-	[47.8-52.7]	[41.2-51.9]	[51.9-59.5]
Spectral Eff. (%)* @BW = 1081 MHz	-	-	62.8	47.9	46.5	-	-	-	44.7	-	-	-	40.93	47.9
Spectral Eff. (%)* @BW = 1331 MHz	-	-	-	[45.2-45.8]	-	-	-	-	48.3	-	-	-	[33.6-35.1]	[48.6-52.7]
Spectral Eff. (%)* @BW = 1355 MHz	-	-	-	-	-	-	-	-	44.3	-	-	-	-	49.3
Do the pulses fit into IEEE masks?*	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	No	Yes	Yes	Yes
Do the pulses have a BW_{-10dB} greater than 500 MHz?*	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	No	Yes
Amplitude (Vpp)	0.9	0.46	0.91	0.6*	N/A	0.55*	0.16	1	0.43	N/A	0.9	0.18	0.2	0.79
Emitted Energy E_p (pJ/pulse)	0.48	0.83	2.4	0.82*	0.86*	0.84*	0.11	0.25	0.98*	1*	0.41	0.87*	1.7	1.58
Dynamic Energy E_{ac} (pJ/pulse)	146	63	8.5	660	N/A	N/A	16.8	6.2	N/A	40	158◇	96	27	325.3
Efficiency E_p/E_{ac} (%)	0.32	1.28	15.3	0.07*	0.02*	1.2*	0.63	7.5	0.07	2.5*	0.26	1*	6.2	0.75
Static power (µW)	100	0.38	13	N/A	N/A	N/A	390	N/A	N/A	640	14.4	N/A	N/A	30.69
P_C (mW) @PRF = 3.9 MHz	0.67◇	0.25◇	0.05◇	4.49◇	15.4◇	0.27◇	0.46◇	0.03◇	5.1	0.80◇	0.63◇	0.38◇	0.11◇	16.0
P_C (mW) @PRF = 15.6 MHz	2.38◇	0.98◇	0.15◇	17.97◇	61.6	1.09◇	0.65◇	0.10◇	20.3	1.26◇	2.47◇	1.5◇	0.42◇	16.2

† Paper includes a receiver. & Carrier input from an external signal generator. * Estimated from reported pulse spectrum. ◇ Estimated power consumption. ♠ Combined with a pre-distortion technique.

5. Design of IR-UWB transmitter with envelope shaping circuit

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5.1. Introduction

From the previous chapter, the proposed IR-UWB transmitter composed of VCO, buffer stage, and VCA has shown its capacity to address every IEEE 802.15.4 and 802.15.6 standard channel inside the FCC band (3.1 GHz - 10.6 GHz). However, pulse envelope shaping is done using an external source. In this chapter, it is proposed to design an integrated envelope shaping circuit and to associate it to the previous IR-UWB transmitter. The obtained IR-UWB transmitter can also be seen as an extension of the IR-UWB transmitter presented in Chapter 4.

The envelope shaping circuit is designed here to generate a non-uniform sample and hold (approach B) instead of a continuous one. Indeed, from Chapter 2, the sample and hold envelope is easier to fabricate from an electrical point of view. Hence, there is no need for an external source. Besides, approach B has been the most efficient in increasing the side-lobe rejection.

The proposed IR-UWB transmitter, having an envelope shaping circuit, is designed to generate pulses compliant with every standardized IEEE channel between 3.1 GHz and 10.6 GHz. As mentioned earlier, the generated pulses must also comply with the radio frequency masks imposed by IEEE standards and the 10 dB bandwidth of 500 MHz established by the

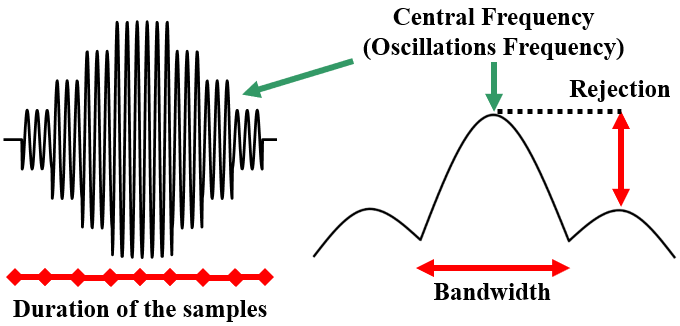


Figure 5.1.: Tunable parameters of IR-UWB pulse with sample and hold envelope.

FCC. Besides, to control the pulse shape and the emitted spectrum (mostly bandwidth and adjacent lobes rejections), the proposed circuit allows the tuning of the central frequency in addition to the duration of every pulse sample, as indicated in Figure 5.1. Thus, the envelope shaping circuit can provide exactly 8 pulse samples with a constant sample amplitude step because the number of 8 samples enables it to achieve a sufficient adjacent lobe rejection without making the circuit design too complex. Indeed, although a higher number of samples can allow a higher adjacent lobe rejection, it will make the envelope shaping circuit bigger and more complex to design.

The new transmitter architecture, which consists of 6 main blocks, is shown in Figure 5.2. This architecture has 2 blocks in common with the IR-UWB transmitter of Chapter 4. These blocks are block (a), which is a VCO with a fast start and stop ability, and block (b), which is a buffer circuit that should ensure good transmission of the oscillations from the VCO to the block (c) which is the amplification stage. The VCA used previously as the amplification stage, whose gain is controlled through an analog signal, is replaced here by an amplifier whose gain is digitally controlled (DCA). Its role is also to modulate the envelope of the rectangular pulse generated by the oscillator according to a 4-bit word applied on its gain control inputs. These binary words are supplied by the set of blocks (d) to (f) which form the envelope shaping circuit whose design is presented in this chapter.

The fourth block (d) is a memory that stores the binary words that control the value of delays between each edge generated by the Digitally Controlled delay line (DCDL), which is the fifth block (e). This DCDL also synchronizes the process of sending the binary word sequence that must be sent to the DCA. Finally, the sixth block (f) is an edge combiner allowing the generation of the binary words sequence which must be sent to the DCA to have a constant amplitude step. Finally, it can be noticed that there are coupling capacitors of 2 pF between the DCA and the load, which lets pass the AC signal and block the DC signal.

In this chapter, an overview of the proposed architecture is first introduced. Next, the design of the new four blocks (c to f) of the proposed IR-UWB transmitter is presented. Some post-layout simulations are shown along the design of these four blocks. Finally, the full circuit has been implemented in Cadence Virtuoso and fabricated in a 28 nm CMOS process from TSMC for a supply voltage of 0.9 V. The global layout and measurement results are also presented.

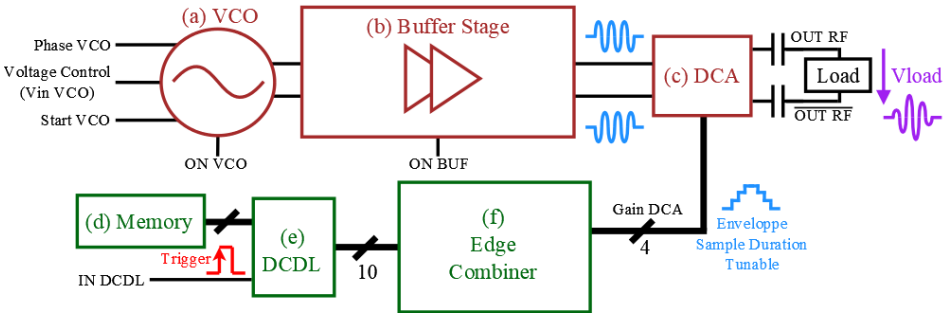


Figure 5.2.: Proposed IR-UWB transmitter architecture.

5.2. Architecture Overview

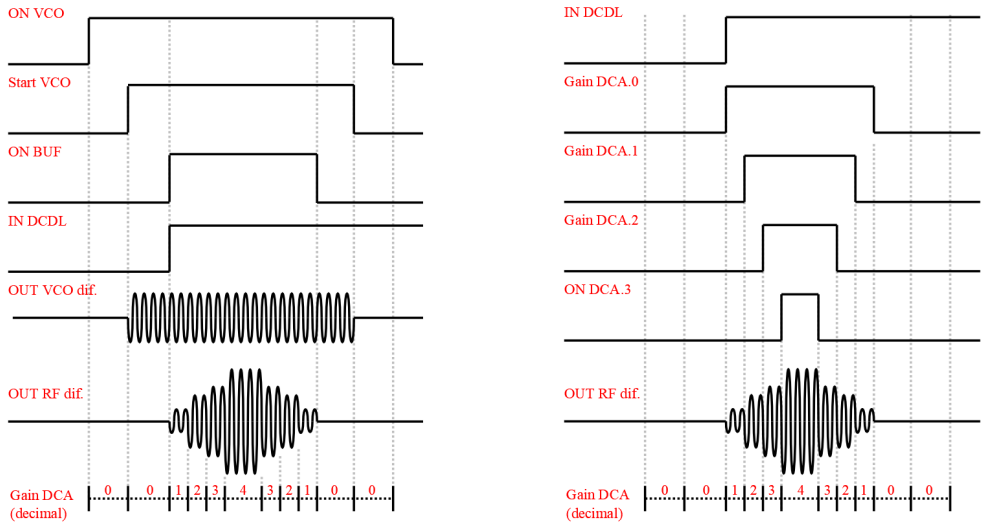
Figure 5.3 displays the proposed transmitter signals chronogram. The signal "ON VCO" turns on and off the VCO, while the signal "Start VCO" commands the oscillations start. The signal "IN DCDL" corresponds to the DCDL trigger input. It can be noted that the frequency of "IN DCDL" corresponds to the Pulse Repetition Frequency (PRF). The signals "OUT VCO dif" and "OUT RF dif" correspond to VCO differential output and transmitter differential output, respectively. Finally, the signals "Gain DCA" correspond to the 4-bit binary word that controls the DCA gain.

Regarding the IR-UWB pulse generation from the transmitter of Figure 5.2, first of all, the VCO is turned on ("ON VCO" at a high level). The VCO is next started ("Start VCO" at a high level"). The VCO frequency should be stabilized before turning on the remaining blocs. Next, the buffer stage is turned on ("ON BUF" at a high level"). The positive edge of signal "IN DCDL" triggers the generation of the IR-UWB pulse. After the IR-UWB pulse transmission, the transmitter blocs are turned off, according to the chronogram of Figure 5.3a.

Besides, to generate an envelope composed of 8 samples (N=8), the DCA has been designed to have a gain that can be tuned using a 4-bit binary word employing the unary coding, also called thermometric coding. In this coding, there are as many '1' in the binary word as the whole number to be coded. Thus, for the proposed architecture, the bit numbers of the word controlling the DCA gain must be equal to the first integer greater than N/2, where N is the total number of samples.

The 8 non-programmable amplitudes a_n are chosen here to increase during the first half of the pulse and decrease during the second half. In this case, the sequence sent to DCA during the pulse generation is constituted by numbers in unary format going from 0 ("0000"; null gain) to 4 ("1111"; maximum gain), and then from 4 to 0, as shown in Figure 5.3b. In other words, the sequence is: "0000"; "0001"; "0011"; "1111"; "1111"; "0111"; "0011"; "0001"; "0000". Therefore, there are 4 amplitude levels.

From Chapter 2, the 8 programmable durations τ_n to generate should have a range from 100 ps to 700 ps to address all IEEE channels. Specifically, τ_n should be set to range from 300 ps to 700 ps to address the 499.2 MHz IEEE channels, while it should be adjusted to range from 100 ps to 300 ps for the large-bandwidth IEEE channels (1081 MHz, 1331 MHz, and 1355 MHz). In addition, it is necessary to have a sufficient resolution to compensate PVT variations. For this reason, each τ_n is programmed employing an 8-bit binary word using the standard



(a) Pulse generation setting.

(b) Envelope shaping.

Figure 5.3.: Proposed IR-UWB transmitter signals chronogram.

binary code, which leads to a resolution of approximating 2 ps supposing a linear distribution. To generate the N=8 delays τ_n, the DCDL is composed of N+3=11 delay cells. Therefore, the memory storing the programming word of every delay cell on 8 bits must store 8 x 11 = 88 bits.

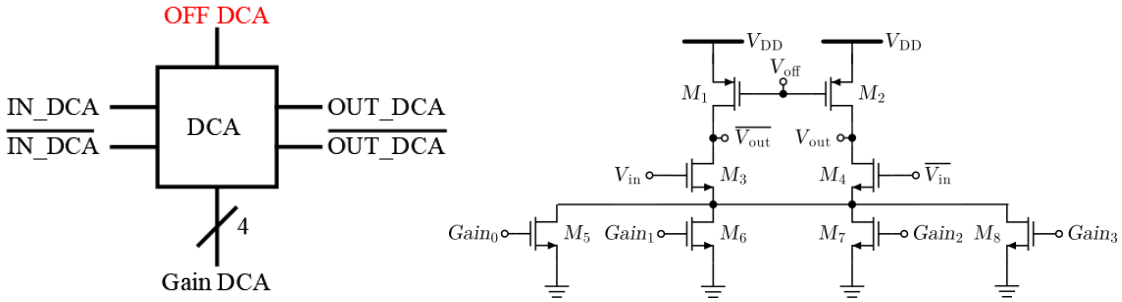
5.3. Digitally Controlled Amplifier

The Digitally-Controlled Amplifier (DCA), which is block (c), modulates the oscillation amplitude to achieve the targeted sample and hold the envelope. Figure 5.4 shows its architecture and transistor-level schematic.

From Figure 5.2, the DCA gain is controlled through a 4-bit word supplied by the envelope shaping circuit. This 4-bit word, which employs thermometric coding, enables the generation of the non-uniform sample and hold envelope composed of 8 samples. Thereby, the DCA can modulate the amplitude of the DCA input oscillations, which come from the buffer stage. It can be perceived that between DCA and VCA architectures, the DCA has 4 current source transistors digitally controlled while the VCA has only one source current transistor controlled by an analog voltage.

The signal "OFF VCA" of Figure 5.4 power off the DCA to execute a power management. Table 5.1 displays the transistor sizing of the DCA. The amplifier gain is also tuned through the transistors M5 to M8, which are the current source. The 4 current source transistors allow obtaining a sample and hold envelope having 4 amplitude levels, as displayed in Figure 5.3. The transistor sizing has been done to make the DCA achieve a high output voltage level dynamic and a constant amplitude step when the thermometric coding is used.

Figure 5.5 displays the layout of the DCA followed by its output coupling capacitor. The layout of the DCA must be as symmetrical as possible, given the DCA has been implemented using CML logic. The 2 PMOS transistors of the differential pair are placed next to the coupling



(a) Architecture. (b) Transistor-level schematic.

Figure 5.4.: DCA architecture and transistor-level schematic.

Table 5.1.: DCA transistor sizing

Width (µm)								Length (nm)	
M1	M2	M3	M4	M5	M6	M7	M8	M1 to M4	M5 to M8
32	32	160	160	15.2	28.8	25.6	130.56	30	60

capacitor. The interconnection between the DCA and coupling capacitor has been implemented using 2 stacked metal layers to reduce the parasitic resistance of interconnection lines (these layers are the thickest among the available metal layers). Moreover, the gates of transistors M5 to M8 are connected via a large and thick metal layer. The reason for this is to reduce the rising and falling times of the output signals from the envelope shaping circuit (Gain DCA). The ground and supply voltage metal layers are distributed over the DCA layout to ensure a good supply voltage level everywhere on the layout.

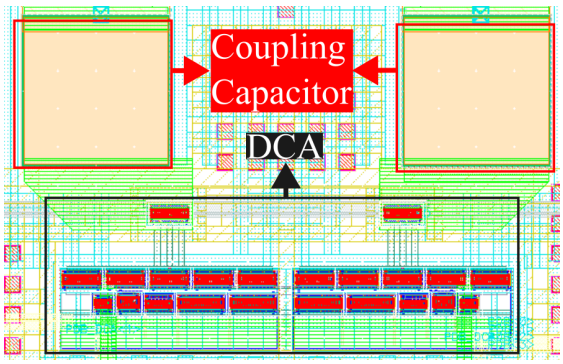


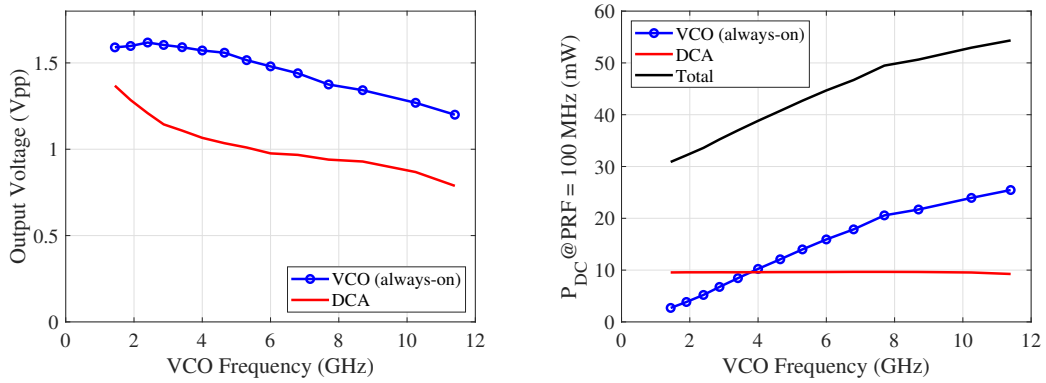
Figure 5.5.: DCA layout.

Figure 5.6 shows the post-layout simulation of VCO and DCA output voltage and power consumption as a function of the oscillation frequency. The VCO is set in always-on mode, contrary to the DCA that generates a pulse with a τ = 6.2 ns with a PRF of 100 MHz (6.2 ns corresponds to the maximum pulse duration enabled by the envelope shaping circuit). However, the post-layout simulation of Figure 5.6 has not considered parasitic associated with power supply decoupling capacitors. The reason for this is that the single post-layout simulation of the complete circuit usually takes at least 2 days.

Figure 5.6b displays the total power consumption of blocks (a) to (f) for a PRF of 100 MHz. From Chapter 4, the buffer stage mode A means that all CML buffers are turned on.

From Figure 5.6a, it can be noticed that the DCA maximum output voltage decreases non-linearly when the oscillation frequency increases, like the VCO output voltage. A reason for this is the parasitic resistance of interconnection lines that is greater for an increasing frequency. An output voltage of at least 0.8 Vpp is promising to generate pulses targeting address the IEEE channels.

From Figure 5.6b, the DCA power consumption for a PRF of 100 MHz is between 9.52 mW and 9.66 mW, with an average of 9.57 mW. Hence, DCA power consumption is weakly sensible to the oscillation frequency. The power consumption relies on the current source transistors' configuration.



(a) Output voltage.

(b) Mean Power consumption.

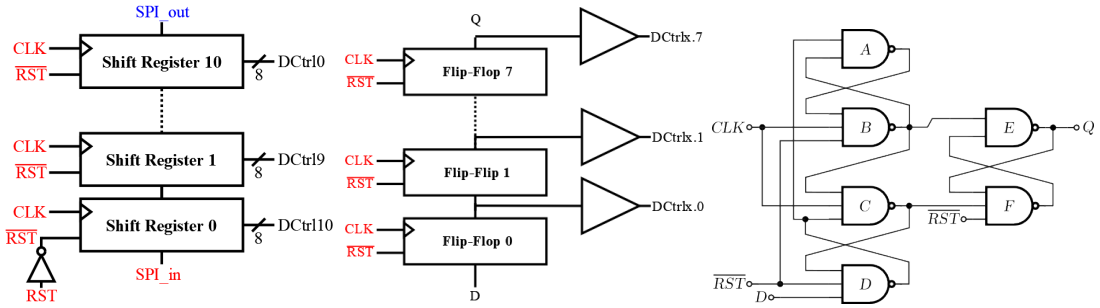
Figure 5.6.: DCA output voltage and power consumption as a function of the oscillation frequency (τ = 6.2 ns, PRF = 100 MHz, Buffer Stage Mode A).

5.4. FIFO Memory

The block (d), which is a First In First Out (FIFO) memory, stores and provides the 11 bytes that drive the DCDL, controlling the value of the delays between edges of the DCDL and also the duration of each envelope sample. This memory loads an 11-byte data bus from a Serial Peripheral Interface (SPI) interface using a frequency of around a few MHz.

The FIFO memory architecture is an 11-byte shift register with serial input and parallel output, as displayed in Figure 5.7, and is activated by a positive rising clock edge. The first byte is loaded in the last shift register (10), while the last byte is loaded in the first shift register (0). The clock signal is "CLK" and the high level asynchronous reset which clears the memory is "RST".

The architecture of each byte (or 8-bit) shift register is based on 8 flip-flops D whose outputs are followed by a buffer, as shown in Figure 5.7b. The 8 flip-flops are activated by a positive rising clock edge and have a high asynchronous reset. The 8 buffered signals control one delay cell of the DCDL, while the flip-flop 7 output signal "Q" drives the following 8-bit shift register input "D".



(a) 11-byte shift register. (b) 8-bit shift register. (c) D flip-flop schematic.

Figure 5.7.: FIFO memory architecture based on serial-in parallel-out shift registers.

It has been chosen that the first loaded bit "Dctrlx.7" is the Most Significant Bit (MSB), while the last loaded bit "Dctrlx.0" is the Least Significant Bit (LSB). The implemented D flip-flop is composed of 6 NAND gates, as indicated in Figure 5.7c (2 NAND gates of 2 inputs and 4 NAND gates of 3 inputs).

Figure 5.8 shows the layout of the FIFO Memory based on an 11-byte shift register. The ground and supply voltage metal layers are distributed over the FIFO memory layout to ensure a good supply voltage level all along the supply lines. The 8-bit shift registers are placed from right to left, and they are equally spaced. Moreover, Figure 5.9 depicts the 8-bit serial-in parallel-out shift register layout proposed floorplan. From Figure 5.8 and Figure 5.9, the directions of data propagation and clock propagation are opposite to guarantee that input data is properly transferred.

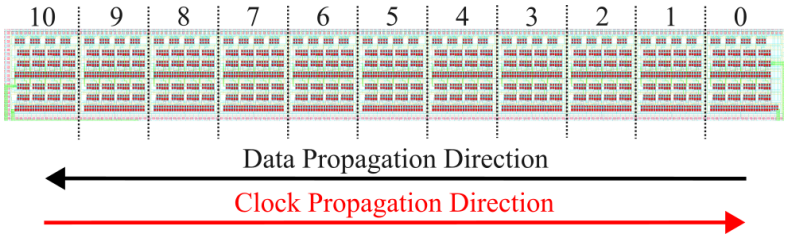


Figure 5.8.: FIFO memory layout.

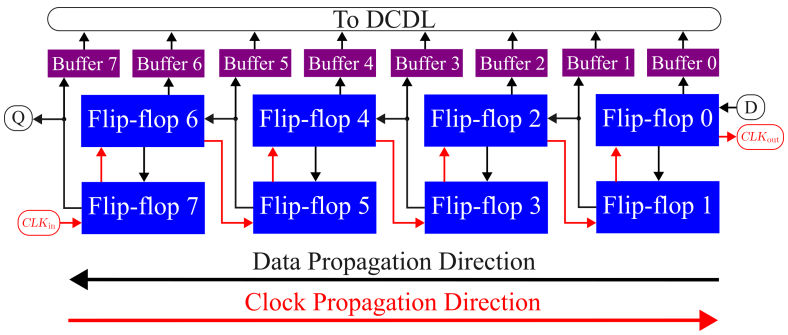
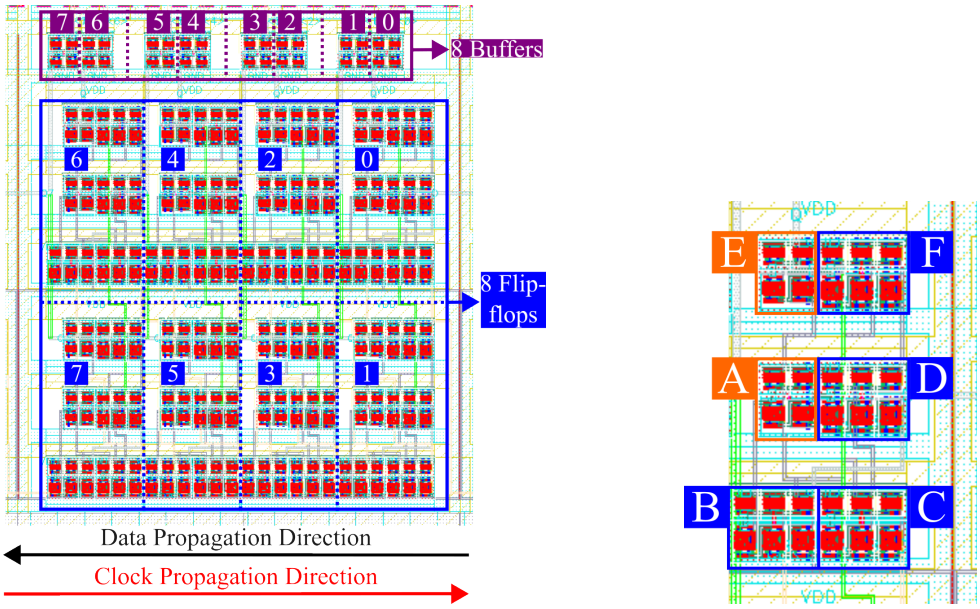


Figure 5.9.: 8-bit serial-in parallel-out shift register layout proposed floorplan.

As shown in Figure 5.9, the flip-flops D of 8-bit shift registers are arranged in a 2x4 matrix to obtain a compact design, and the buffers are placed next to the DCDL. According to the proposed floorplan, the Figure 5.10 displays the 8-bit serial-in parallel-out shift register layout, in addition to the CMOS high asynchronous reset D flip-flop layout. The ground and supply voltage metal layers are distributed over the 8-bit shift register. The interconnection between the flip-flops D has been implemented using thicker metal layers. From Figure 5.10b, the NAND gates layout placement has been done to minimize the metal mine crossing. The D flip-flop input signal "D" arrives from the right of Figure 5.10b, while the D flip-flop output signal "Q" is at the top, being closer to the buffer and DCDL. Besides, the NAND gates B and C are placed side by side at the bottom since they have the clock signal at their inputs.



(a) 8-bit serial-in parallel-out shift register. (b) D flip-flop.

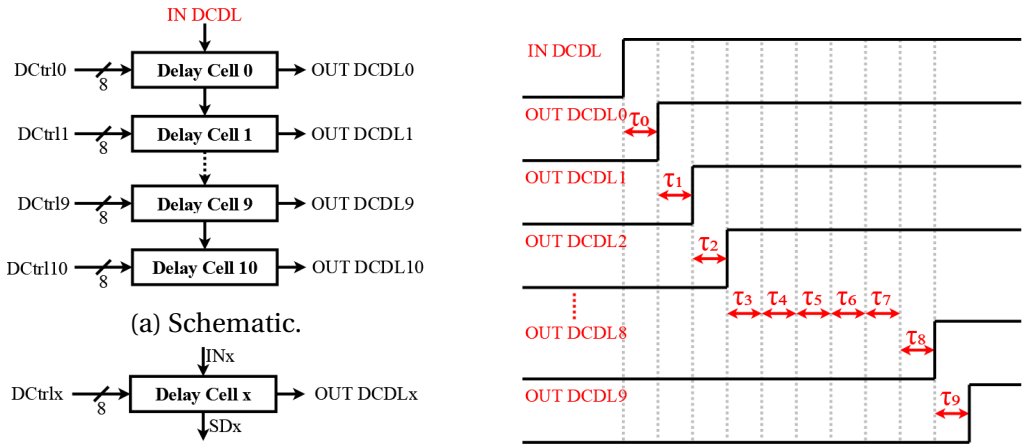
Figure 5.10.: FIFO memory blocs layout.

5.5. Digitally Controlled Delay Line

The block (e), the Digitally Controlled delay line (DCDL) synchronizes the sending process of the binary word sent to the DCA, hence controlling the duration τ_n of all 8 pulse samples (Fig. 5.3). According to the sample and hold envelope study in Chapter 2, the target range for τ_n is 100 ps to 700 ps to address the IEEE channels (300 to 700 ps for 499.2 MHz IEEE channels, 100 ps to 300 ps for the large-bandwidth IEEE channels).

Figure 5.11 displays the DCDL architecture and signal chronogram. The DCDL is also composed of 11 delay cells aiming to generate 8 delays τ_n (the 3 supplementary cells are respectively used to shape the rising edge propagating inside the DCDL, to reset the edge combiner after the generation of a pulse, and to charge the DCDL). Therefore, τ_1 corresponds to the first pulse sample duration, τ_2 to the second pulse sample duration, etc. The delay τ_n of

Figure 5.11c is controlled by the 8-bit word "DCtrl" of Figure 5.11a, which is supplied by the FIFO memory. Each delay cell generates a pair of delayed signals ("SD" and "OUT DCDL"). The delayed signal "SD" is connected to the next delay cell input signal, whereas the buffered delay signal "OUT DCDL" is connected to the edge combiner. It can be noted that the delay cell has been designed to obtain a delay τ_n proportional to the 8-bit word "DCtrl" value.



(a) Schematic.

(b) Delay Cell pin-out.

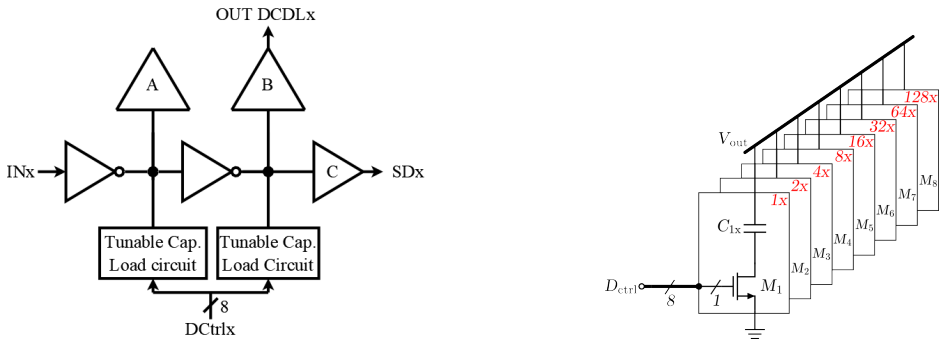
(c) Signal Chronogram.

Figure 5.11.: DCDL architecture and chronogram.

Figure 5.12 shows the DCDL delay cell schematics. From Figure 5.12a, the delay cell is composed of 2 inverters, 3 buffers, and 2 tunable capacitive load circuits. The circuit of Figure 5.12b controls the delay τ_n. The 3 buffers are implemented to isolate the inverter's output. The buffer B separates the second inverter output from the edge combiner (the buffer A is implemented to obtain the same delay for both tunable capacitive load circuits), while Buffer C separates the the same inverter output from the following delay input. The reason for this is to avoid that a delay cell influences the delay time of an adjacent delay cell. The tunable capacitive load circuit can control the inverter delay time using an 8-bit word "Dctrl." From Figure 5.12b, the tunable capacitive load circuit is composed of a set of 8 NMOS transistors whose drain terminals are connected to the output invert through a capacitor. In fact, the higher the 8-bit word "Dctrl" applied to their gate is, the higher the inverter capacitive load is and also the higher the slowing down of the delay cell is. Thus, the delay cell can be seen as a slowing down stage.

The 8 transistors have the same width (48 µm) and the same length (30 nm) Meanwhile, the 8 capacitors $C_{2^m x}$, with m as an integer between 0 to 7, have a value of $2^m \cdot C_x$ and also follow approximately a geometric progression with a common ratio of 2. For instance, the capacitors $C_{1x} = C_x$ and $C_{128x} = 128 \cdot C_x$ have a value of 28.1 fF and 3.6 pF. The signal "Dctrl.0" drives the gate of transistor M1, which is connected to the capacitor of capacitance C_{1x} (the smallest capacitor). It is the LSB. On the other hand, the signal "Dctrl.7" drives the gate of transistor M8, which is connected to the capacitor of capacitance C_{128x} (the biggest capacitor). It is the MSB.

The architecture of the delay control circuit of Figure 5.12b has been chosen because it enables an inverter delay directly proportional to the capacitance and also the Dctrl 8-bit word. An alternative architecture of delay cell could be on current-starving [54, 55]. In this case, the



(a) Delay Cell.

(b) Tunable capacitive load circuit.

Figure 5.12.: DCDL delay cell schematics.

control of the inverter delay is done using a programmable current source. Nevertheless, the inverter delay has a non-linear behavior, in addition to the more challenging current source layout design.

Figure 5.13 shows the layout of the DCDL. The ground and supply voltage metal layers are distributed over the DCDL layout to ensure a good supply voltage level all along the layout. The delay cells are placed from left to right, in addition to being equally spaced. From Figure 5.13, the directions of DCDL signal propagation and FIFO memory data propagation are opposite. Consequently, the delay control of the first delay cell (0) is supplied by the last 8-bit shift register (11), and so the one of the last delay cell (11) by the first 8-bit shift register (0). The interconnection between the delay cells has been implemented using 2 stacked metal layers to reduce the parasitic resistance of interconnection lines (these layers are the thickest among the available metal layers).

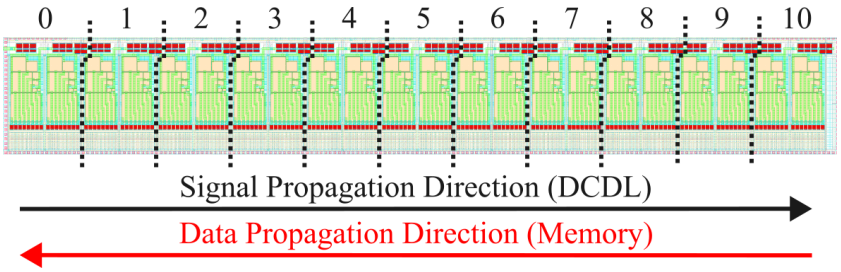


Figure 5.13.: DCDL layout.

Figure 5.14 displays the DCDL delay cell layout. The inverters and buffers are placed at the top, while the tunable capacitive load circuit is placed at the bottom, next to the FIFO memory, to reduce the rising and falling times of the DCDL output signals. These strongly impact the lowest value of τ_n. The capacitors have greater dimensions compared to the MOS transistors, occupying a larger surface of the DCDL delay cell layout. The placement of the capacitors is done to achieve a compact rectangular layout. The interconnection between the tunable capacitive load circuit and the inverters has been implemented using 2 stacked metal layers (thickest available) to achieve lower parasitic resistance.

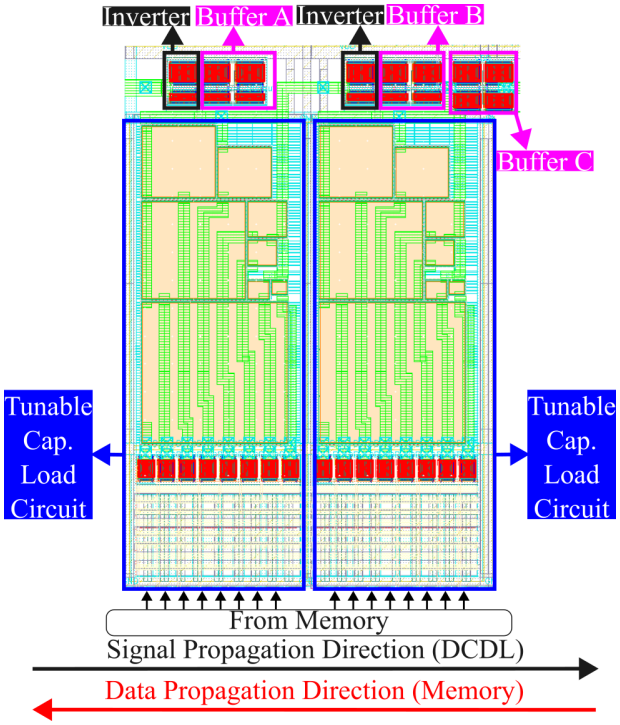


Figure 5.14.: DCDL delay cell layout.

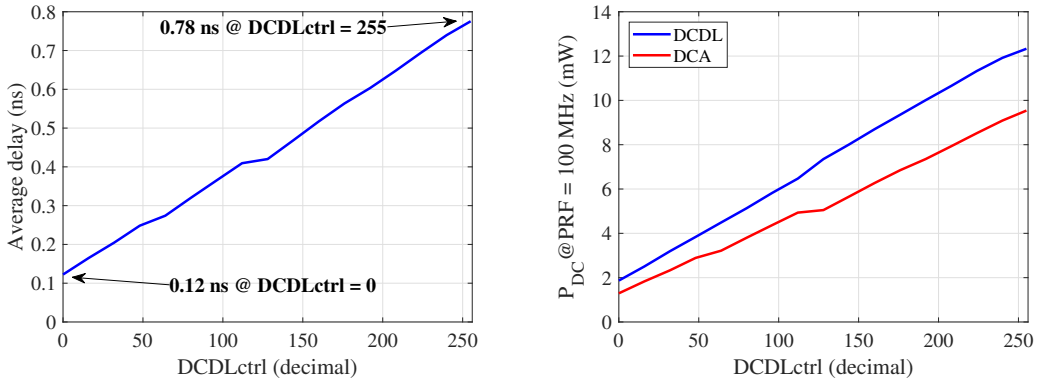
Figure 5.15 shows the post-layout simulation of the average delay time and power consumption of the 11 DCDL delay cells as a function of the 8-bit word "DCDLctrl" (parasitic elements associated with power supply decoupling capacitors have not been considered and only RF pads are taken into account). In these figures, all DCDL delay cells have the same 8-bit word "DCDLctrl" at their inputs, and the signal "IN DCDL" has a frequency of 100 MHz, which results in a PRF of 100 MHz. VCO frequency during this post-layout simulation is equal to 10 GHz but does not impact the DCDL behavior and its power consumption. Figure 5.15 also shows the power consumption of the DCA.

From Figure 5.15a, it can be observed that the average delay time increases linearly with increasing the 8-bit word DCDLctrl value. As expected to make pulses compliant with IEEE radio-frequency masks, the average delay is between 0.12 ns and 0.78 ns. Thereby, the shortest pulse has a duration of 0.96 ns and the longest one 6.24 ns.

From Figure 5.15b, it can be noticed that the DCDL and DCA power consumption are proportional to the input 8-bit word decimal value. Moreover, the DCDL and DCA power consumption are proportional to the pulse width. Besides, the DCDL drains more power than the DCA.

5.6. Edge Combiner

Finally, the block (f), which is the edge combiner, generates the 4-bit word to be sent to the DCA from the delayed edges provided by the DCDL. Figure 5.16 shows the edge combiner architecture and chronograms. The edge combiner is based on SR latches with buffered output,



(a) Average delay time.

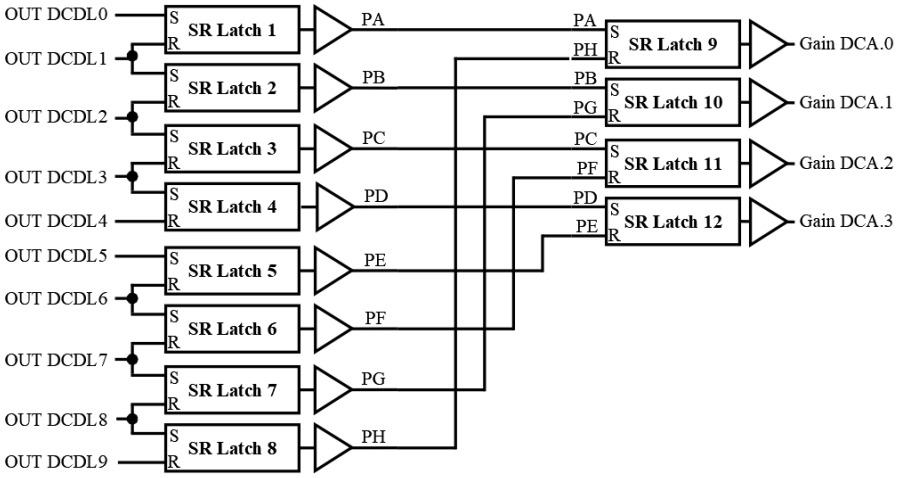
(b) Power consumption.

Figure 5.15.: Average delay time and power consumption of the 11 DCDL delay cells as a function of the 8-bit word "DCDLctrl" (Buffer Stage Mode A, PRF = 100 MHz, f_c = 10 GHz).

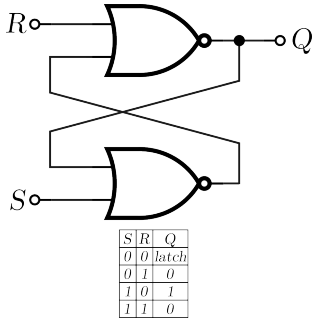
as displayed in 5.16a. The edge combiner input is the 10-bit signal generated by the DCDL ("OUT DCDL0" to "OUT DCDL9"). Meanwhile, the edge combiner output is the 4-bit signal that controls the DCA gain ("Gain DCA"). The SR latch has an architecture based on 2 NOR gates, as shown in Figure 5.16b. The SR latches 1 to 8 generate the signals "PA" to "PH". These signals are combined in SR latches 9 to 12 to generate the 4-bit signal "Gain DCA".

The chronograms for the two first SR latches are given in Figure 5.16c. It can be noted that the signals "PA" and "PB" are pulses whose widths are τ_1 and τ_2, respectively. Figure 5.16d shows the full chronogram of the edge combiner. Regarding the SR latches 9 to 12, the signals "PA" to "PD" preset these SR latches, while the signal signals "PE" to "PH" reset these SR latches. The signal "Gain DCA.0" has a positive and negative edge determined by the signals "PA" and "PH", and this signal is a pulse whose width is the sum of the 8 delays τ_n. The signals "Gain DCA.1", "Gain DCA.2" and "Gain DCA.3" have positive edges defined by the signals "PB", "PC" and "PD", respectively. On the other hand, the signals "Gain DCA.1", "Gain DCA.2" and "Gain DCA.3" have negative edges defined by the signals "PG", "PF" and "PE", respectively. These signals are pulses whose width are the sum from τ_2 to τ_7, from τ_3 to τ_6, and from τ_4 to $\tau_5$respectively. Thus, the positive edge of the signal "PA" defines the IR-UWB pulse start, while the positive edge of the signal "PH" the IR-UWB pulse end.

Figure 5.17 shows the layout of the edge combiner based on SR latches with buffered output. Moreover, Figure 5.18 displays the layout of the SR latch followed by a buffer. The ground and supply voltage metal layers are equally distributed over the edge combiner layout to ensure a good supply voltage level all along the layout. From Figure 5.17, the SR latches 1 to 4 are placed on the left, the SR latches 5 to 8 on the right, and finally, the SR latches 9 to 12 at the center. The placement of the SR latches 1 to 8 has been done to reduce the interconnection length between the DCDL delay cell and SR latch, thus reducing the rising and falling time of the DCDL output signal. Besides, the placement of the SR latches 9 to 12 has been done to reduce the interconnection length between the edge combiner output and DCA 4-bit word input, reducing the delay propagation of the edge combiner output signal. The interconnection

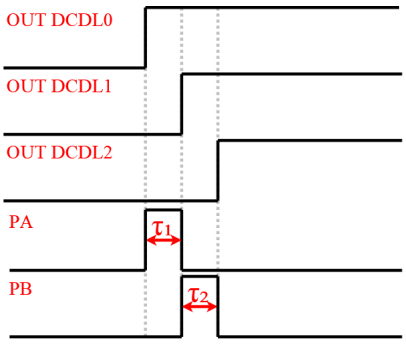


(a) Edge Combiner.

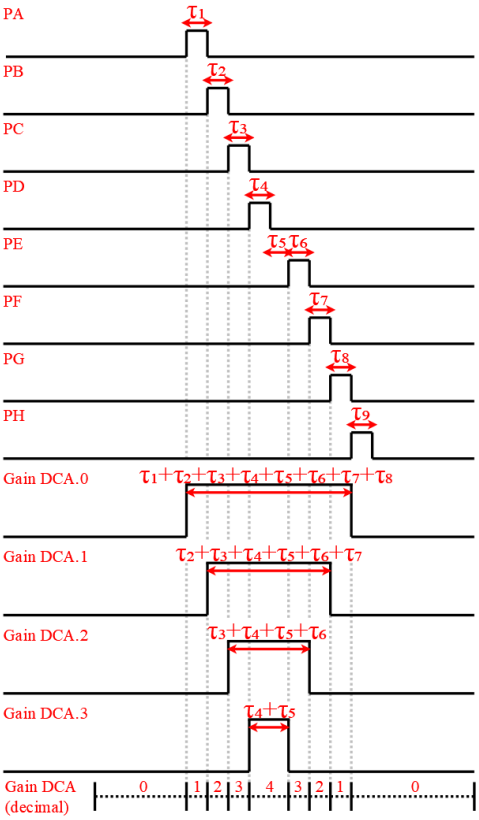


S	R	Q
0	0	latch
0	1	0
1	0	1
1	1	0

(b) SR latch.



(c) Chronogram concerning 2 SR Latches.



(d) Full chronogram.

Figure 5.16.: Edge Combiner architecture and chronograms.

between the SR latches 1 to 8, and the latches 9 to 12 has been implemented using the thickest metal layer available because it enables better mitigation of parasitic resistance.

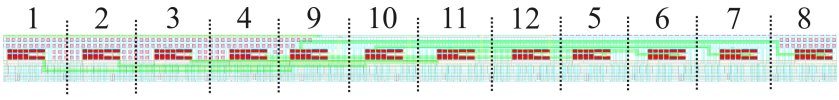


Figure 5.17.: Edge combiner layout.

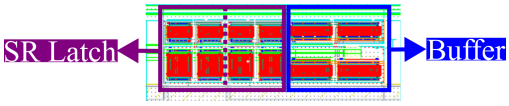


Figure 5.18.: Layout of SR latch followed by a buffer.

5.7. Global Layout

As cited earlier, this IR-UWB transmitter, with envelope shaping circuit, has been implemented and fabricated in a 28 nm CMOS process of TSMC, with a supply voltage of 0.9 V. All NMOS transistors bulk terminals are connected to the ground, while all PMOS transistors bulk terminals are connected to the positive supply voltage. Figure 5.19 displays the IR-UWB transmitter's global layout with the 36 required pads. Its surface without pads after the 10% shrink is 738 µm x 414 µm (i.e. 0.306 mm²), whereas its surface with pads is 1 mm x 0.664 µm (i.e. 0.664 mm²).

In addition, there are 4 dedicated power supplies: one for VCO, one for the buffer stage, one for DCA, and a last one for the 3 remaining blocks (labeled "VDD NUM"). The nomenclature "NUM" refers to the combination of the memory, DCDL, and edge combiner. Thus, 4 matrixes of power supply decoupling capacitors have been implemented on the core surface that is not occupied by the IR-UWB transmitter. Regarding post-layout simulations or measures, the circuit load is composed of an impedance of 2x50 Ω.

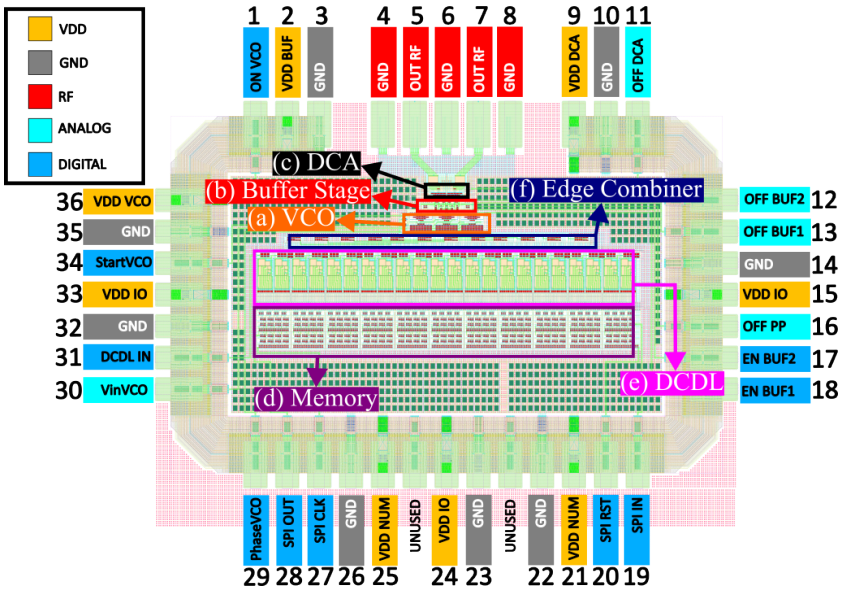


Figure 5.19.: IR-UWB Transmitter layout displaying the PAD pins.

The fabricated chip was encapsulated in a QFN-40 package, which has 40 pins. Figure 5.20 depicts the wire bonding plan of the proposed IR-UWB transmitter. The layout placement

strategy is similar to the wire bonding plan shown in Chapter 4. The layout is not placed at the center of the QFN-40 package, but rather at the north edge to reduce the wire bonding length of RF output (red). Moreover, the IR-UWB transmitter layout was aligned with pin 5 of Figure 5.20 to guarantee that the "OUT RF" bonding wires have the same length.

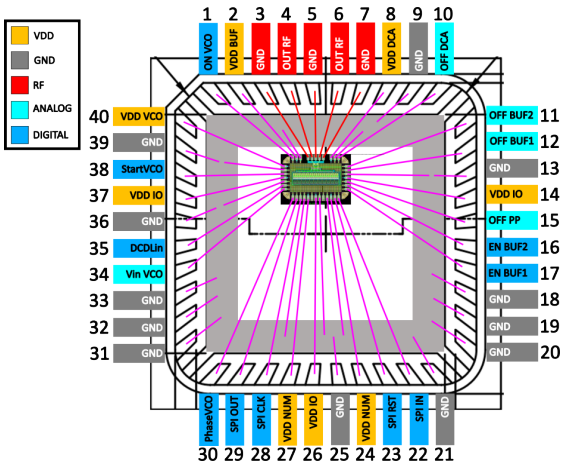


Figure 5.20.: Wire bonding plan of the proposed IR-UWB Transmitter.

5.8. Test Setup and Measurements Results

5.8.1. Test board design

To test the prototype chip, a two-layer Rogers equivalent PCB has been designed. Figure 5.21 depicts photos of the assembled test PCB. The PCB substrate is ZYF255DA. All six transmitter blocks (a to f) use a common ground plane. The TSMC 28 nm chip packaged in a socket QFN-40 is connected to the PCB using an appropriate socket.

Even if this PCB is different from the one presented in Chapter 4, the used PCB design strategy is similar. Thus, the ground plane has been implemented in the bottom layer of the PCB, and decoupling capacitors were placed as close as possible to the chip. The output RF lines are 50 Ω microstrip transmission line. As shown in Figure 5.21, the PCB has multiple switches like the PCB presented in Chapter 4. Many implemented switches allow switching between the ground, the positive voltage supply, and an external signal to reduce the number of required voltage sources. This is valid for all analog and digital input signals (Fig. 5.20), except for the "Start VCO" and "IN DCDL" which require periodic signals.

However, compared to the previous PCB, the digital inputs and output required by the memory which allow to control the 8 τ_n have been added ("SPI IN", "SPI CLK", "SPI RST", and "SPI OUT"). During the measurement, the STM32 microcontroller loads the memory through its SPI interface and a bidirectional level shifter. The level shifter is required because the STM32 microcontroller logic voltage is 3.3 V, whereas the prototype chip voltage supply is 0.9 V.

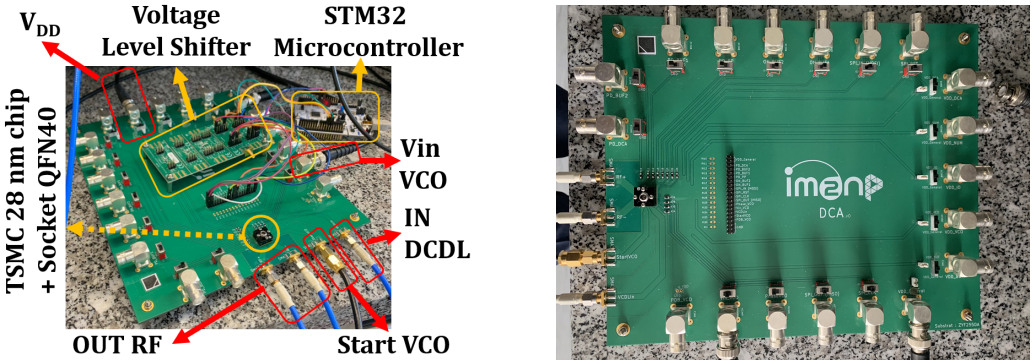
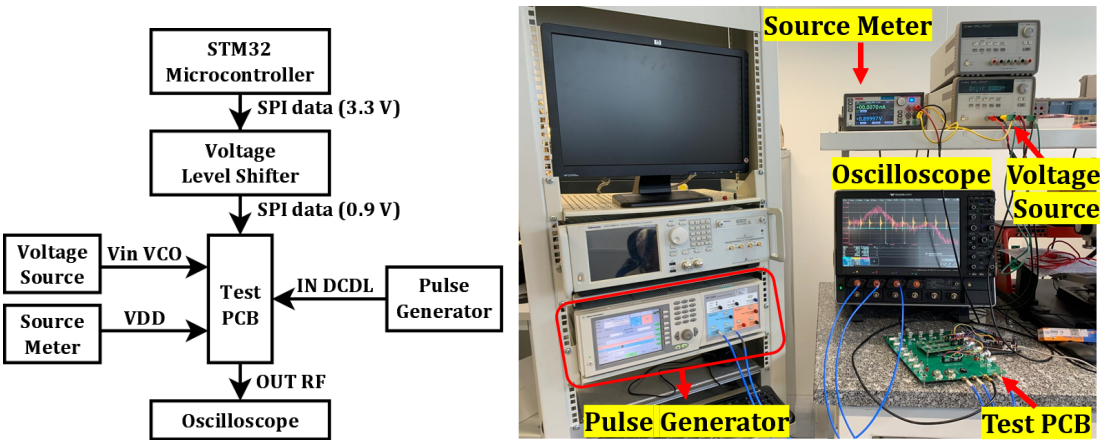


Figure 5.21.: Test PCB of the of the proposed IR-UWB Transmitter.

5.8.2. Test Setup

Figure 5.22 displays the test bench of the chip prototype. The signal "IN DCDL" is provided by the pulse pattern generator 81134A of Keysight [84]. This generator can provide programmable pulse periods from 15 MHz (66.6 ns) to 3.35 GHz (298.5 ps). Besides, it features an output amplitude of up to 2 Vpp. Similar to the test setup introduced in Chapter 4, the supply voltage of 0.9 V is provided by the source meter 2450 of Keithley [82], and the "Vin VCO" signal by a voltage source. The RF output signals are measured by the oscilloscope Wavemaster 813Zi-B of Teledyne Lecroy [83]. The output spectrum analysis is done in MATLAB from the signal data exported by this oscilloscope.



(a) Diagram. (b) Photo.

Figure 5.22.: Test bench of the measured IR-UWB transmitter.

5.8.3. Measurement Results

This sub-section addresses the measurement results of the proposed multi-standard IR-UWB transmitter with an envelope shaping circuit. It is divided into two parts, similar to Chapter 4. First, the implemented IR-UWB transmitter is presented. The circuit tuning capabilities

are studied as a function of the VCO input voltage ("Vin VCO") and DCDL delay control 8-bit word. ("DCDLctrl"). Moreover, a comparison between measurement and post-layout results is presented. Second, pulse examples compliant with IEEE channels are addressed. For each pulse example, it is verified if the synthesized pulse is compliant with the spectral requirements imposed by FCC (minimal bandwidth of 500 MHz) and IEEE 802.15.4 and 802.15.6 standards (minimal side-lobe rejection of 18 and 20 dB, respectively).

Regarding the measurements, the VCO is always on, and the buffer stage mode is set to A (all CML buffers are turned on). Besides, a cable attenuation of 1 dB has been considered.

5.8.3.1. Characterization

Figure 5.23 shows the measurement and post-layout simulation of the VCO frequency as a function of its input ("Vin VCO"). From this Figure, it can be observed that the measured oscillation frequency is between 1 GHz and 8.7 GHz. Thus, the prototype chip cannot cover the FCC band, unlike the prototype chip of Chapter 4. Comparing the measurement and post-layout simulation results, it can be seen that there is a larger discrepancy for low input VCO voltage. Indeed, the post-layout simulations presented in this chapter consider only the circuit blocks and RF output pads. Moreover, the lower measured maximum frequency (8.7 GHz) can be explained by the low contact surface of the power supply metal line with the VCO, as depicted in Figure 5.24. In the global layout of Chapter 4, the VCO is surrounded by the power supply metal line. Finally, the measured VCO gain is around -18.1 GHz/V. Meanwhile, the simulated VCO gain is around -23.4 GHz/V.

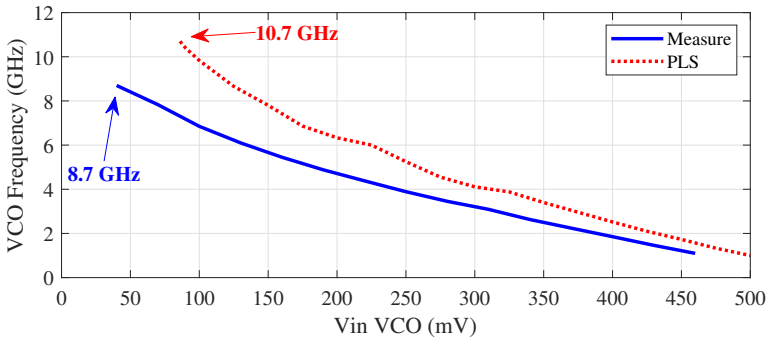


Figure 5.23.: Measured and simulated VCO frequency as a function of the VCO input voltage (Buffer Stage Mode A).

Figure 5.25 displays the measurement and post-layout simulation of the pulse synthesizer output voltage and power consumption as a function of the oscillation frequency. From Figure 5.25a, it can be observed that the measured output voltage is between 0.3 Vpp and 1.1 Vpp. It tends to decrease with an increasing oscillation frequency. Comparing the measurement and post-layout simulation results, it can be noticed that the measured output voltage is weaker. This can be partially explained by the attenuation of the SMA cable and bonding wires. Despite the lower level, the measured output voltage is potentially high enough for the generation of IR-UWB pulses addressing the IEEE standards.

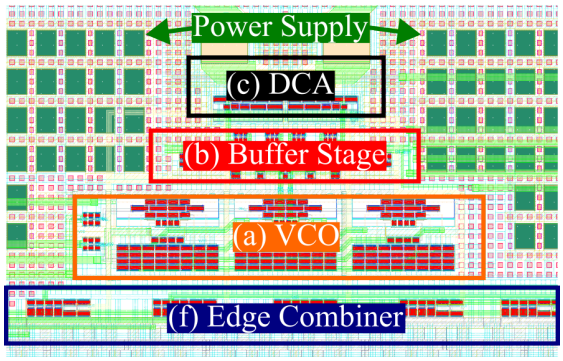
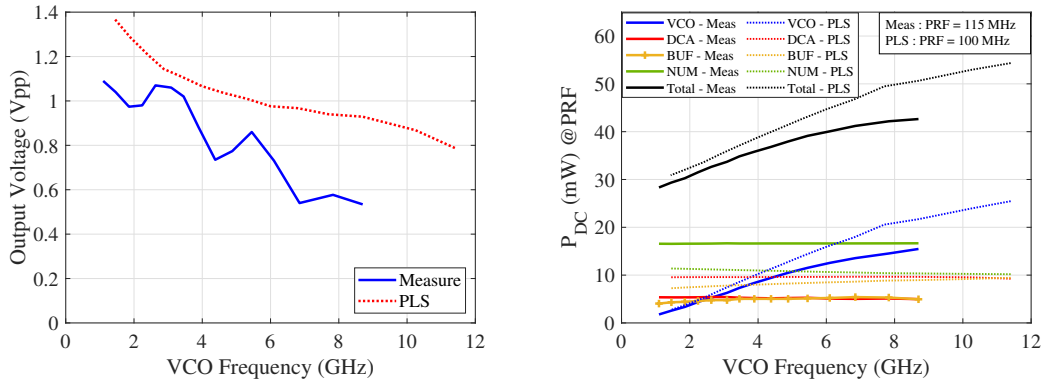


Figure 5.24.: Zoomed IR-UWB transmitter layout displaying the power supply connection.

From Figure 5.25b, the total always-on power consumption is approximately proportional to the oscillation frequency. The VCO power consumption is the most dependent on the oscillation frequency, while the blocks (b) to (f) have a power consumption weakly sensitive to the oscillation frequency, as expected.

Comparing the measurement and post-layout simulation results, it can be seen that the measured power consumption is lower for all oscillation frequencies, except for the combination of memory, DCDL, and edge combiner.



(a) Output voltage.

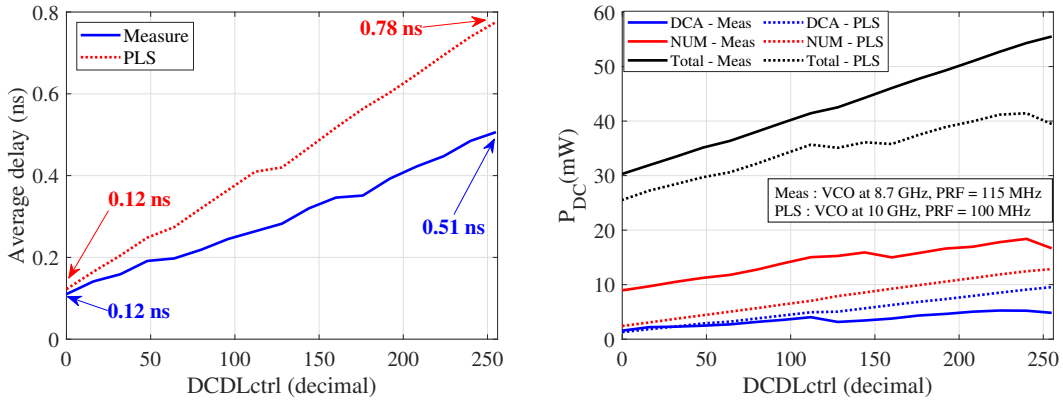
(b) Power consumption.

Figure 5.25.: Measured and simulated output voltage and always-on power consumption as a function of the oscillation frequency (Buffer Stage Mode A).

Figure 5.26 gives the measurement and post-layout simulations of the DCDL average delay and power consumption as a function of the DCDL delay control 8-bit word. All DCDL delay cells have the same 8-bit word "DCDLctrl" at their inputs. From Figure 5.26a, it can be observed that the measured average delay time increases linearly with increasing 8-bit word DCDLctrl value as expected. The measured average delay is between 0.12 ns and 0.51 ns. Therefore, this

enables the shortest pulse of 0.96 ns and the longest pulse of 4.08 ns. As a result, this range of pulse duration allows making pulses addressing only the larger-bandwidth IEEE channels. Indeed a pulse of 4 ns is too large in bandwidth to comply with the spectral mask of the 499.2 MHz IEEE channels. The discrepancy between post-layout simulations and measurement related to the pulse duration can be attributed to the model of the capacitor employed in DCDL (Fig. 5.12), which seems to be under-estimated. The average sample duration is 1.55 ps/LSB.

From Figure 5.26b, it can be observed that the DCA and the set of blocks (d) to (f) power consumption are proportional to the DCDL input 8-bit word decimal value. It follows that the greater the pulse width, the higher the power consumption.



(a) Average delay time.

(b) Power consumption.

Figure 5.26.: Measured and simulated average delay time and power consumption as a function of the 8-bit word "DCDLctrl" (Buffer Stage Mode A).

5.8.3.2. Pulse synthesis

Regarding the IR-UWB pulse synthesis, Figures 5.27 and 5.28 display the IR-UWB measured pulse waveforms which try to address IEEE 802.15.4 channels 1 to 6 and 7 to 12, respectively. Table 5.2 shows the parameters of the IR-UWB measured pulse associated with their measured voltage, emitted energy, and estimated spectral efficiency.

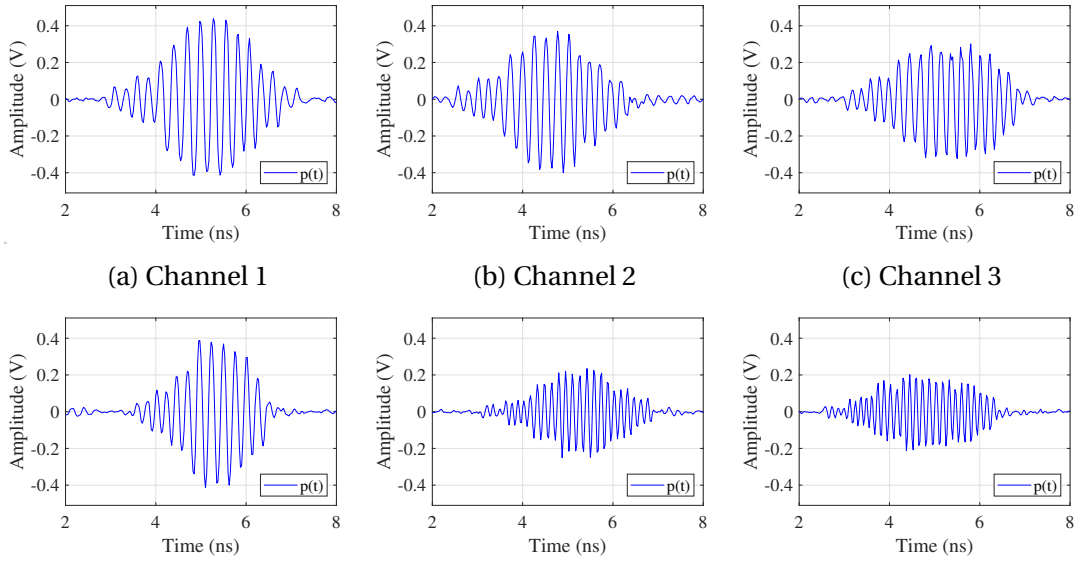
Figure 5.29 and 5.30 display the IR-UWB measured pulse addressing all the 499.2 MHz channels of the IEEE standard 802.15.4 within the FCC band and ETSI band, respectively. Finally, Figure 5.31 shows the IR-UWB measured pulse addressing large bandwidth channels (4, 7, and 11) of the IEEE standard 802.15.4.

From Table 5.2, the measured IR-UWB pulses have a duration between 3.74 ns and 4.47 ns, except for the measured pulse addressing the IEEE channel 12 (3.1 ns). From Figures 5.27 and 5.28 and Table 5.2, the measured pulse output voltage is between 0.41 Vpp and 0.85 Vpp. The output voltage tends to be lower when the pulse central frequency is increased. Besides, the measured pulse emitted energy is between 0.32 pJ and 1.77 pJ. Of course, the pulse emitted energy is higher when the output voltage is greater, and the pulse duration is longer.

Table 5.2.: IR-UWB measured pulse parameters and performance.

Ch.	f_c (MHz)	BW (MHz)	Buffer Stage Mode	DCDLctrl (decimal)	T_E (ns)	Vpp (V)	E_p (pJ)	Side-Lobe Rejection (dB)	Spectral Efficiency (%)
1	3494.4				4.29	0.85	1.77	26.40	
2	3993.6	499.2	A	255	4.47	0.77	1.25	24.30	-*
3	4492.8				4.36	0.62	1.05	25.71	
4	3993.6	1331	A	192	4.02	0.80	1.15	22.20	38.34
5	6489.6	499.2	A	255	4.15	0.49	0.44	12.30	-*
6	6988.8				4.47	0.41	0.40	12.23	
7	6489.6	1081	A	255	4.24	0.52	0.51	23.56	37.52
8	7488				4.22	0.51	0.59	11.57	
9	7987.2	499.2	A	255	4.19	0.56	0.70	13.50	-*
10	8496.4				4.45	0.57	0.55	13.24	
11	7987.2	1331	A	192	3.74	0.53	0.48	22.95	41.87
12	8985.6		A	255	3.10	0.51	0.32	9.22	-*
13	9484.8	499.2	-	-	-	-	-	-	-
14	9984		-	-	-	-	-	-	-
15	9484.8	1355	-	-	-	-	-	-	-

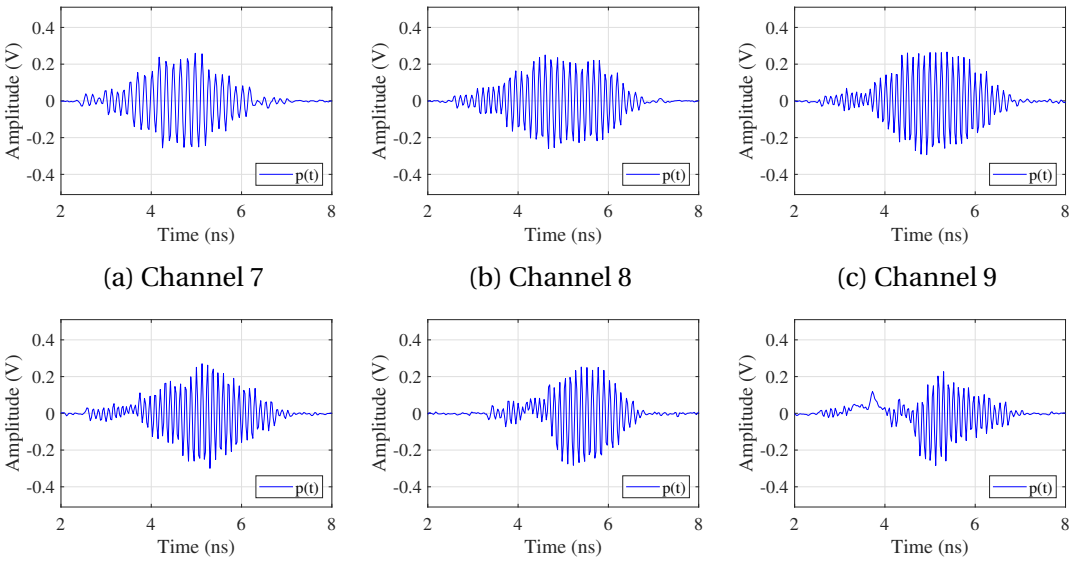
* Spectral efficiency not applicable because pulse does not fit into IEEE masks



(a) Channel 1 (b) Channel 2 (c) Channel 3

(d) Channel 4 (e) Channel 5 (f) Channel 6

Figure 5.27.: Measured output voltage for IEEE 802.15.4 channels 1 to 6 (Buffer Stage Mode A)



(a) Channel 7 (b) Channel 8 (c) Channel 9

(d) Channel 10 (e) Channel 11 (f) Channel 12

Figure 5.28.: Measured output voltage for IEEE 802.15.4 channels 7 to 12 (Buffer Stage Mode A)

From Figure 5.29, it can be observed that the 9 measured output spectra are compliant with the minimal bandwidth BW_{-10dB} of 500 MHz imposed by FCC. However, as expected, due to the discrepancy of the DCDL performances, they do not fit into the IEEE 802.15.4 standard mask even with the DCDL set to generate the maximum pulse duration. From Table 5.2, the output spectra of Figure 5.29 achieved a maximal side-lobe rejection of 26.4 dB (IEEE Channel 1). This is a lower side-lobe suppression compared with the prototype chip of Chapter 4 (26.4 dB vs 31.8 dB).

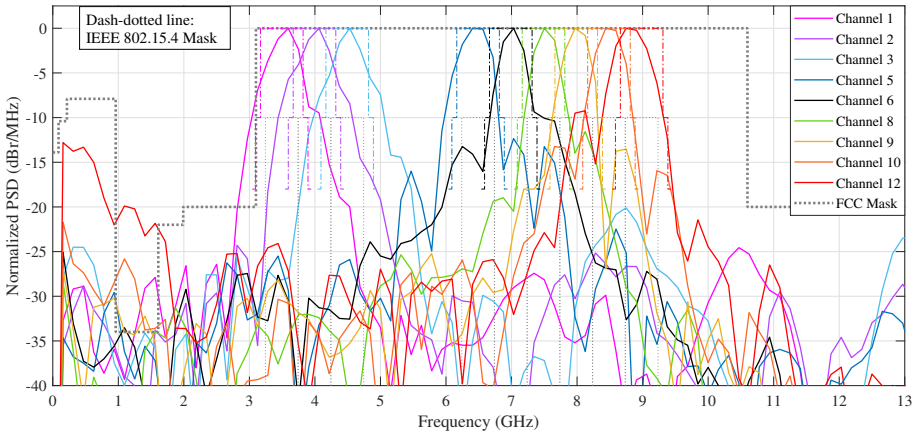


Figure 5.29.: Measured output spectrum for 499.2 MHz Channels with FCC regulatory mask (Buffer Stage Mode A).

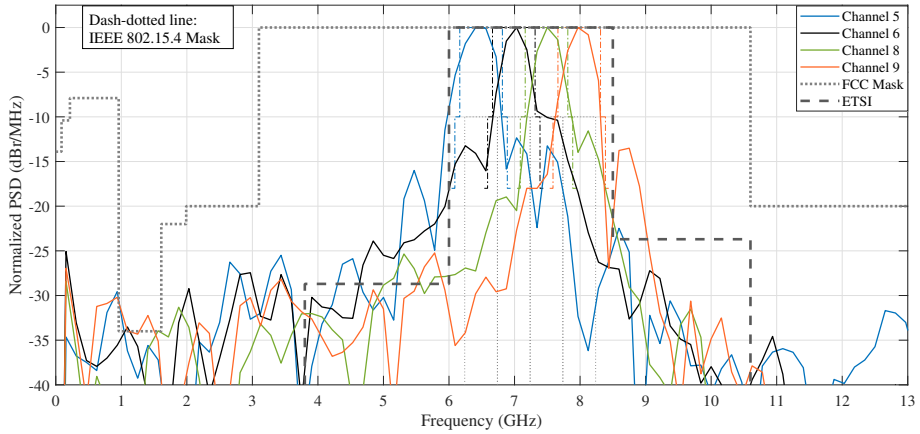


Figure 5.30.: Measured output spectrum for 499.2 MHz Channels with FCC and ETSI regulatory masks (Buffer Stage Mode A).

Nevertheless, from Figure 5.31, it can be seen that the 3 measured output spectra are compliant with the IEEE 802.15.4 standard in addition to the minimal bandwidth BW_{-10dB} of 500 MHz imposed by FCC. From Table 5.2, the output spectra of Figure 5.31 achieved a side-lobe rejection between 22.2 dB and 23.6 dB, and an estimated spectral efficiency between 38.3% and 41.9%. These are lower when compared with the prototype chip of Chapter 4, but the pulse envelope is integrated into the chip at the opposite of the previous one.

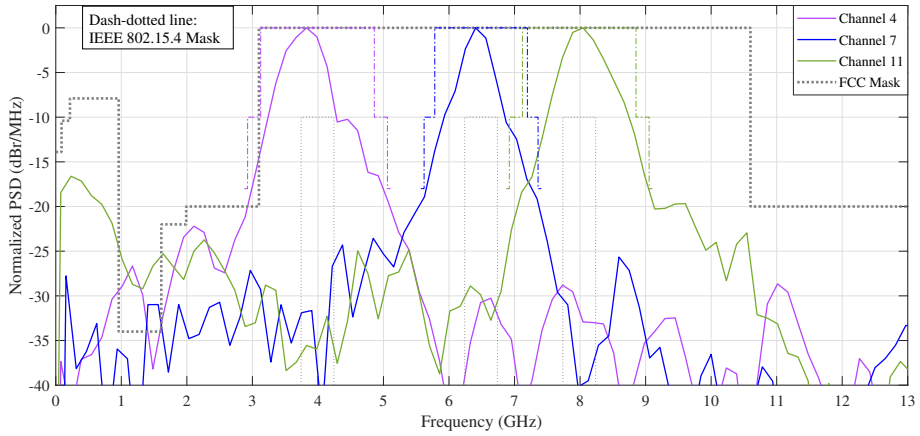


Figure 5.31.: Measured output spectrum for large bandwidth Channels with FCC regulatory mask (Buffer Stage Mode A).

Table 5.3 shows the measured power consumption for a PRF of 115 MHz of the full IR-UWB transmitter and each dedicated power supply (VCO, BUF, DCA, and NUM). From this table, it can be noticed that the VCO always-on power consumption is higher when the pulse central frequency increases. On the other hand, the power consumption of other dedicated power supplies (BUF, DCA, and NUM) is slightly sensitive to the oscillation frequency. Finally, the power consumption is lower when the pulse duration is decreased.

In general, the major part of the IR-UWB power consumption comes from the combination of memory, DCDL, and edge combiner. Among the blocks (a) to (c), Table 5.3 suggests that the DCA is the one that has the lowest power consumption.

Finally, the measured static power P_{0Hz} for the VCO, buffer stage, and DCA is 23.71 µW, 4.93 µW, and 6.84 µW, respectively. Moreover, the static power measured in the dedicated power supply NUM is 180 µW. As a result, the total measured static power is 215.48 µW (Fig. 5.32).

Table 5.3.: IR-UWB transmitter performance in terms of the power consumption.

Ch.	f_c (MHz)	BW (MHz)	P_{DC} (mW) Always-on	P_c (mW) @PRF = 115 MHz			
			VCO	Buffer Stage	DCA	Memory + DCDL + Edge Combiner*	Total
1	3494.4	499.2	7.40	5.05	5.31	16.61	34.37
2	3993.6		8.49	5.11	5.24	16.63	35.47
3	4492.8		9.50	5.17	5.18	16.64	36.50
4	3993.6	1331	8.49	4.79	4.65	16.16	34.08
5	6489.6	499.2	12.63	5.35	4.93	16.66	39.56
6	6988.8		13.30	5.38	5.02	16.67	40.37
7	6489.6	1081	12.63	5.35	4.93	16.66	39.56
8	7488	499.2	13.74	5.43	4.81	16.68	40.65
9	7987.2		14.11	5.45	4.77	16.69	41.01
10	8496.4		14.50	5.41	5.12	16.70	41.72
11	7987.2	1331	14.11	5.11	4.68	16.14	40.04
12	8985.6	499.2	14.74	5.35	5.08	16.70	41.87
13	9484.8		-	-	-	-	-
14	9984		-	-	-	-	-
15	9484.8	1355	-	-	-	-	-

* Measured together (common power supply VDD NUM)

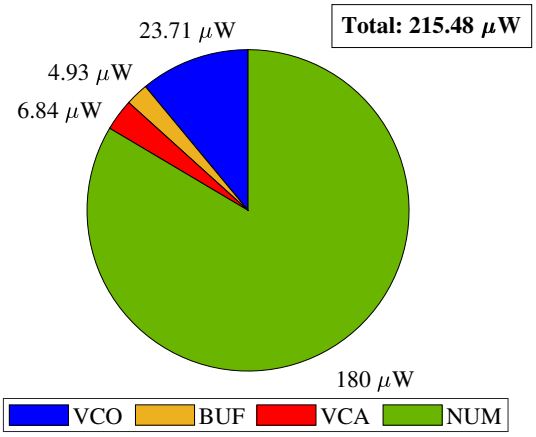


Figure 5.32.: Measured static power P_{0Hz} of the proposed IR-UWB transmitter.

5.9. Conclusion

In this chapter, the design of a multi-standard IR-UWB transmitter with its envelope shaping circuit has been presented. It corresponds to an extension of the IR-UWB transmitter addressed in Chapter 4. The architecture of the envelope shaping circuit has been chosen to achieve a non-uniform sample and hold envelope. This envelope shaping circuit controls the gain of a digitally controlled amplifier.

As previously, the proposed IR-UWB transmitter has been implemented and fabricated in a 28 nm CMOS technology of TSMC, with a supply voltage of 0.9 V. However, it has six main blocks: a voltage-controlled oscillator, a buffer stage, a digitally controlled amplifier, a memory, a digitally controlled delay line, and an edge combiner. The last three blocks form the envelope shaping circuit. These blocks have been designed to generate pulses addressing the IEEE channels within the 3.1-10.6 GHz frequency band. The memory that controls the pulse sample duration is configured using the SPI interface of an STM32 microcontroller.

In Table 5.4, a comparison between the proposed IR-UWB transmitters in this chapter and Chapter 4, and UWB transmitters addressed in Chapter 3 is done. From the measurement results of the prototype chips, the proposed IR-UWB transmitter with pulse shaping circuit achieved a frequency range (1-8.7 GHz) narrower than the IR-UWB transmitter of Chapter 4 (1-10.6 GHz). Indeed, the transmitter of Chapter 4 can generate pulses addressing all the IEEE 802.15.4 standard channels (15), while the transmitter of Chapter 5 can generate pulses addressing only 3 large-bandwidth IEEE channels. These pulses did not address the 499.2 IEEE channels mostly because of the limitations of the DCDL in terms of maximum step delay. Thus, the generated pulse presents a bandwidth larger than the one allowed by the IEEE masks.

Comparing the measured pulses, the ones generated by the IR-UWB transmitter having an envelope shaping circuit achieved lower side-lobe rejection (26.7 dB vs 31.8 dB), lower spectral efficiency (41.8% vs 52.7%), but greater amplitude (0.85 Vpp vs 0.79 Vpp), and greater emitted energy (1.77 pJ vs 1.58 pJ). The envelope shaping of DCDL followed by an edge combiner (sample and hold envelope of 8 samples) has potential because it achieved a side-lobe rejection better than the uniform sample and hold of Chapter 2 (24.3 dB). In addition, the measurement results indicate this circuit's reasonable capacity to control the pulse duration, which is important for the multi-band design.

Comparing the IR-UWB transmitter proposed in this Chapter with the ones of the state-of-art, the proposed one achieved a great central frequency range, being better than all transmitters except for [65, 67, 68]. However, this frequency range is not wide enough to cover the IEEE channels in the FCC band. This can attributed to the VCO power supply issues. Besides, the proposed circuit does not address any 499.2 MHz IEEE channel, similar to the transmitters of [21, 52]. The reason for this is the short DCDL maximum delay time (510 ps), which compromises the transmitter pulse duration tuning capabilities.

In conclusion, the proposed IR-UWB transmitter with envelope shaping circuit achieved a good central frequency range and side-lobe rejection. It has the potential to comply with the IEEE standard masks. Nevertheless, it presented limitations in terms of pulse duration tuning, which impacted the number of addressed IEEE channels.

There are feasible solutions to improve this transmitter. The first is to change the placement of the transmitter blocks in the global layout to achieve a better VCO power supply (better

oscillation frequency). The second consists of changing the capacitor model in the delay cell or implementing a delay control based on current starving [54, 55] to obtain a larger pulse duration range.

Table 5.4.: Performance comparison with state-of-the-art IR-UWB transmitters

	Vauché TCSI'17 [21]†	Haapala JSSC'20 [51]	Miranda CICC'20 [52]	Chen RFIC'22 [54]&	Chen ISSCC'22 [57]†	Song VLSI'23 [58]†	Phan TCSI'08 [61]	Schmickl TCSI'20 [62]	Zhang LMWT'22 [63]	Ryckaert JSSC'07 [65]	Streel JSCC'17 [66]	Bechthum ESSCIRC'23 [67]	Singh JSSC'21 [68]	This Work Chapter 4 VCA	This Work Chapter 5 DCA
Process (nm)	130	65	65	28	40	28	180	180	28	90	28 (FD-SOI)	22 (FD-SOI)	28	28	
Supply Voltage (V)	1.2	1.2	1.2	0.9	1.25	0.9	1.5	1	0.9	1	0.9	0.8	0.9	0.9	
Core Area (mm²)	0.11	0.22	N/A	0.25	N/A	1.33	0.3	0.25	0.21	0.07	0.55	0.09	0.15	0.15	0.31
Die Area (mm²)	1.31	1.1	0.7	N/A	8.8	N/A	0.66	3.91	N/A	N/A	0.93	1.0	2.37	0.45	0.66
Architecture	Delay Line	Delay Line	Delay Line	LO (External)	LO (Mixer)	LO	LO (LC Tank)	LO (LC Tank)	LO (LC Tank)	LO (Ring)	LO (Ring)	LO (Ring)	LO (Ring)	LO (Ring)	
Pulse Shaping	Delay Line	Delay Line	Delay Line	Delay Line	LUT Flip-flop	Delay Line	LO Modulation	LO Modulation	Counter	PA-FLL	Counter	Delay Line	Delay Line	AWG♠	Delay Line
Modulation	OOK DB-BPSK	OOK	OOK	OOK BPSK	N/A	BPSK	OOK	N/A	BPSK	BPSK	2-PPM BPSK	BPSK	BPSK	BPSK	
Spectral compliance	FCC	ETSI	FCC	FCC	FCC	FCC	FCC	ETSI	FCC	FCC	FCC	FCC	FCC	FCC	
Freq. Range (GHz)	3.1-4.9	6-8.5	3.6-7.5	4-9	6.5-10	6-9	3-5	6-8.8	5-10	3-10	3.5-4.5	3-9	3-10	1-10.6	1-8.7
Mod. BW (GHz)	1/1.3	0.5	1/1.3	0.5/1/1.3	0.5/1	0.5	0.5	0.5	0.5/1/1.3	0.5	0.5	0.5	0.5/1	0.5/1/1.3	1/1.3
Side-lobe rejection (dB)	18	30	23.8*	31	25*	31	18	18	21*	24*	23*	29	32	31.8	26.7
IEEE 802.15.4 Addressed Channels (Total)	4 (1)	5,6,8,9 (4)	4,7 (2)	2-12 (11)	5-15 (11)	5,6,8,9 10,12 (6)	1-3 (3)	5,6,8,9 (4)	5-15 (11)	1-3,5,6 8-10,12-14 (11)	1-3 (3)	1-3,5,6 8-10,12 (9)	1-14 (14)	1-15 (15)	4,7,11 (3)
IEEE 802.15.6 Addressed Channels (Total)	None (0)	3-6 (4)	None (0)	1-8 (8)	3-10 (8)	3-8 (6)	0-2 (3)	3-6 (4)	3-10 (8)	0-10 (11)	0-2 (3)	0-8 (9)	0-10 (11)	0-10 (11)	None (0)
Spectral Eff. (%)* @BW = 499.2 MHz	-	[49.5-55.5]	-	[44.2-55.5]	[40.2-61.6]	[49.8-51]	[53.1-54.3]	48.2	63.5	56.3	-	[47.8-52.7]	[41.2-51.9]	[51.9-59.5]	-
Spectral Eff. (%)* @BW = 1081 MHz	-	-	62.8	47.9	46.5	-	-	-	44.7	-	-	-	40.93	47.9	37.52
Spectral Eff. (%)* @BW = 1331 MHz	-	-	-	[45.2-45.8]	-	-	-	-	48.3	-	-	-	[33.6-35.1]	[48.6-52.7]	[38.3-41.8]
Spectral Eff. (%)* @BW = 1355 MHz	-	-	-	-	-	-	-	-	44.3	-	-	-	-	49.3	-
Do the pulses fit into IEEE masks?*	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	No	Yes	Yes	Yes	No
Do the pulses have a BW_{-10dB} greater than 500 MHz?*	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	No	Yes	Yes
Amplitude (Vpp)	0.9	0.46	0.91	0.6*	N/A	0.55*	0.16	1	0.43	N/A	0.9	0.18	0.2	0.79	0.85
Emitted Energy E_p (pJ/pulse)	0.48	0.83	2.4	0.82*	0.86*	0.84*	0.11	0.25	0.98*	1*	0.41	0.87*	1.7	1.58	1.77
Dynamic Energy E_{ac} (pJ/pulse)	146	63	8.5	660	N/A	N/A	16.8	6.2	N/A	40	158◇	96	27	325.3	-
Efficiency E_p/E_{ac} (%)	0.32	1.28	15.3	0.07*	0.02*	1.2*	0.63	7.5	0.07	2.5*	0.26	1*	6.2	0.75	-
Static power (µW)	100	0.38	13	N/A	N/A	N/A	390	N/A	N/A	640	14.4	N/A	N/A	30.69	215.48
P_C (mW) @PRF = 3.9 MHz	0.67◇	0.25◇	0.05◇	4.49◇	15.4◇	0.27◇	0.46◇	0.03◇	5.1	0.80◇	0.63◇	0.38◇	0.11◇	16.0	-
P_C (mW) @PRF = 15.6 MHz	2.38◇	0.98◇	0.15◇	17.97◇	61.6	1.09◇	0.65◇	0.10◇	20.3	1.26◇	2.47◇	1.5◇	0.42◇	16.2	-

† Paper includes a receiver. & Carrier input from an external signal generator. * Estimated from reported pulse spectrum. ◇ Estimated power consumption. ♠ Combined with a pre-distortion technique.

Conclusion

IR-UWB communications are based on the transmission of short-duration pulses at a moderate transmission rate (up to 10 Mbps). They are well-suited for short-range communications and can offer a real-time location with a 5 cm accuracy. Besides, they enable the transmitter to start up and shut down at the bit scale, in addition to inducing power consumption proportional to the data rate.

Since the use of IR-UWB communications within the frequency band of 3.1-10.6 GHz was initially authorized by the FCC in 2002, they have been normalized in several standards, particularly within the WPAN and WBAN IEEE standards. (802.15.4 and 802.15.6 respectively). These IEEE standards specify distinct radio frequency masks with respect to 499.2 MHz. Additionally, the WPAN standard equally establishes standardized channels with larger bandwidths.

Thus, the main objective of this thesis was to design a multi-standard and multi-band IR-UWB transmitter capable of synthesizing pulses addressing the IEEE channels in the FCC band. To achieve this, the circuit should be able to control the pulse shape and its central frequency. Besides, this control should be fine and large enough to compensate the PVT variations, achieve a high enough side-lobe rejection, and also protect adjacent channels and neighboring wireless systems.

To do this, Chapter 1 introduced the IR-UWB communications features and spectral requirements. The most important points are that theFCC imposes a minimal absolute bandwidth of 500 MHz, whereas the IEEE WPAN and WBAN standards establish radio-frequency masks requiring a minimal side-lobe rejection of 18 dB and 20 dB, respectively.

Chapter 2 investigated continuous pulse envelopes in a first time. The goal was to find an easily synthesizable continuous envelope that achieves high side-lobe rejection while respecting the spectral requirements. Regarding the continuous envelopes, the asymmetrical trapezoidal shape has demonstrated significant flexibility in meeting IEEE standards and FCC spectral constraints, enhancing side-lobe rejection, and increasing pulse energy.

However, sample and hold envelopes have equally been investigated because they are easier to synthesize from an electrical point of view since digital electronic can be used. However, it appears that continuous envelope uniform sampling should employ a large number of samples to accomplish good side-lobe rejection due to aliasing. Instead of employing a large number of samples, a constrained optimization of the sample and hold envelope has also been proposed to obtain better side-lobe rejection with fewer samples. The constrained optimization results have shown that it is more efficient to optimize the envelope step duration rather than the step amplitude levels.

Chapter 3 addressed a literature survey on the IR-UWB transmitter. From the literature, there are two main pulse synthesis methods: pulse direct synthesis and frequency transposition pulse synthesis. The first method uses a delay line to synthesize the pulse directly into the targeted frequency, whereas the second method utilizes a modulated VCO. From the reported

works, a IR-UWB transmitter based on a ring oscillator and pulse shaping circuit composed of VCDL and recombination circuit is the best choice to address the IEEE channels in the FCC band and accomplish better side-lobe suppression.

Chapter 4 presents the implementation of a multi-standard IR-UWB transmitter based on frequency transposition synthesis and ring oscillator with the 28 nm CMOS technology. The proposed transmitter includes pulse shaping capabilities through a VCA combined with a pre-distortion technique. Regarding the central frequency range and the number of addressed IEEE standardized channels, the proposed IR-UWB transmitter is a promising solution. Furthermore, it features excellent side-lobe rejection when compared to the works reported in the literature. This improvement results from the employment of asymmetrical envelopes associated with the pre-distortion of the VCA gain control.

Chapter 5 concludes this work by showing an extended version of the proposed IR-UWB transmitter, which implements its own envelope-shaping circuit. This shaping circuit is essentially based on a DCDL followed by an edge combiner to obtain a non-uniform sample and hold envelope. As a result, it has the potential to comply with IEEE radio-frequency masks. However, it demonstrated some limitations especially regarding the tuning of pulse sample duration, which affect negatively the number of addressed IEEE channels. Possible improvements in the DCDL design can be made, such as using a better capacitor model or implementing a delay control based on the current transistor instead of a tunable capacitive load circuit.

To conclude, the first main contribution of this work is the demonstration of the relevance for IR-UWB applications of trapezoidal envelopes, and more generally of the asymmetrical ones. A second contribution is the demonstration of the fact that tuning only the step duration of the sample in a sample and hold envelope having a constant amplitude step is the most efficient regarding side-lobe rejection. Moreover, a third contribution is the practical implementation using a 28 nm technology of the heart of an IR-UWB transmitter based on envelope frequency transposition which is able to cover the 3.1-10.6 GHz frequency band (VCO + buffer + VCA). Finally, the fourth contribution is the proposition of a non-uniform sample and hold envelope generator architecture based on a DCDL even if this generator must be improved to obtain in measurement the required performances to be compliant with 499.2 MHz IEEE channels.

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APPENDIX

A. Continuous Envelopes Equations

A.1. Rectangular

Combining expression (2.11) into equation (2.3), the emitted pulse mono-lateral Fourier transform can be computed as:

$$P_R^+(f) = \frac{A\tau_p}{\sqrt{2}}\text{sinc}\left((f-f_c)\tau\right)\exp\left(-j\varphi\right) \tag{A.1}$$

Applying expression (2.11) on equation (2.5), the relation between rectangular envelope bandwidth BW and attenuation X_{dB} can be expressed as follows:

$$X_{dB} = 10\log\left(\frac{1}{\text{sinc}^2\left(\frac{BW}{2}\cdot\tau\right)}\right) \tag{A.2}$$

$$X_{dB} = -10\log\left(\text{sinc}^2\left(\frac{BW}{2}\cdot\tau\right)\right) \tag{A.3}$$

$$10^{\frac{-X_{dB}}{10}} = \text{sinc}^2\left(\frac{BW\cdot\tau}{2}\right) \tag{A.4}$$

where:

$$0 \leq 10^{\frac{-X_{dB}}{10}} \leq 1 \tag{A.5}$$

since τ= 1 s, expression (A.4) is hence:

$$10^{\frac{-X_{dB}}{10}} = \text{sinc}^2\left(\frac{BW}{2}\right) \tag{A.6}$$

It is necessary first to calculate the side-lobe frequency to calculate the side-lobe rejection. From expression (2.11), the PSD of the rectangular envelope is:

$$\left|X_R(f)\right|^2 = A^2\tau^2\text{sinc}^2\left(f\tau\right) \tag{A.7}$$

since τ = 1 s and assuming an amplitude A = 1 , expression (A.7) is hence:

$$\left|X_R(f)\right|^2 = \text{sinc}^2\left(f\right) \tag{A.8}$$

The side-lobe frequency is a local maximum of the expression (A.8), as indicated in Figure A.1.

To find the local maximum, it is first necessary to derive the function (A.8), such that [85]:

$$\frac{\mathrm{d}}{\mathrm{d}f}\left|X_R(f)\right|^2 = \frac{2\mathrm{sinc}(f)\cdot\left[\pi f\cos(\pi f)-\sin(\pi f)\right]}{\pi f^2} \tag{A.9}$$

A local maximum is a critical point [85]. A critical point is a point at which the derivative is zero, such that:

$$\frac{\mathrm{d}}{\mathrm{d}f}\left|X(f)\right|^2 = 0 \tag{A.10}$$

This last equation has multiple solutions. $f = 0$ Hz is a solution, however $f = 0$ Hz corresponds to the main lobe frequency, as indicated in Figure A.1. Considering positive frequency ($f > 0$ Hz), a possible solution can be found in the following equation:

$$\mathrm{sinc}(f) = 0 \Leftrightarrow f = n \neq 0 \;;\; n \in \mathbb{Z} \tag{A.11}$$

where n is an integer. The solutions of equation (A.11) correspond to the local minimum of function (A.8), as shown in Figure A.1. Meanwhile, another possible solution can be obtained in the following equation:

$$\pi f\cos(\pi f)-\sin(\pi f) = 0 \tag{A.12}$$

$$\pi f = \tan(\pi f) \tag{A.13}$$

Solving equation (A.13) numerically, the lowest value of f that satisfies equation (A.13) is approximately $f = 1.43$ Hz.

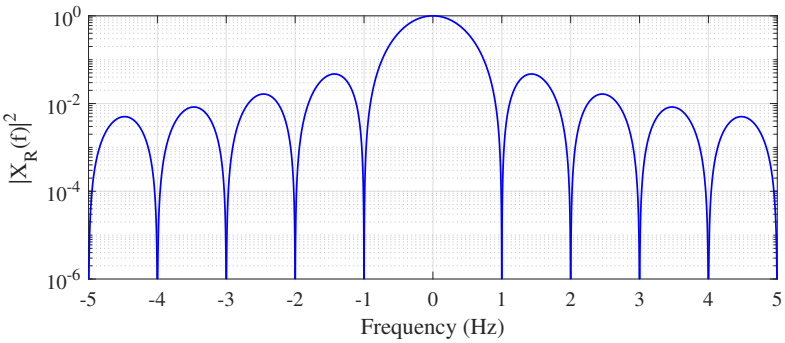


Figure A.1.: $\left|X(f)\right|^2$ as function of frequency.

A.2. Symmetrical Triangular

Applying the last expression into expression (2.3), the emitted pulse mono-lateral Fourier transform can be computed as:

$$P_{ST}^{+}(f) = \frac{A\tau_p}{2}\mathrm{sinc}^2\left[(f-f_M)\frac{\tau_p}{2}\right]\exp(-j\varphi) \tag{A.14}$$

Applying expression (2.17) on equation (2.5), the relation between symmetrical triangular envelope bandwidth BW and attenuation X_{dB} can be written as follows:

$$X_{dB} = 10\log\left(\frac{1}{\text{sinc}^4\left(\frac{BW}{2}\cdot\frac{\tau}{2}\right)}\right) \tag{A.15}$$

$$X_{dB} = -10\log\left(\text{sinc}^4\left(\frac{BW\cdot\tau}{4}\right)\right) \tag{A.16}$$

$$10^{\frac{-X_{dB}}{10}} = \text{sinc}^4\left(\frac{BW\cdot\tau}{4}\right) \tag{A.17}$$

since $\tau = 1$ s, accordingly expression (A.17) is:

$$10^{\frac{-X_{dB}}{10}} = \text{sinc}^4\left(\frac{BW}{4}\right) \tag{A.18}$$

From expression (2.17), the ESD of the symmetrical triangular envelope is:

$$\left|X_{ST}(f)\right|^2 = \frac{A^2\tau^2}{4}\text{sinc}^4\left(\frac{f\tau}{2}\right) \tag{A.19}$$

since $\tau = 1$ s and assuming an amplitude $A = 1$, expression (A.19) is hence:

$$\left|X_{ST}(f)\right|^2 = \frac{1}{4}\text{sinc}^4\left(\frac{f}{2}\right) \tag{A.20}$$

where the side-lobe frequency is a local maximum of function (A.20), as indicated in Figure A.2. Deriving function (A.8), the following expression is obtained:

$$\frac{\mathrm{d}}{\mathrm{d}f}\left|X_{ST}(f)\right|^2 = \frac{\text{sinc}^3\left(\frac{f}{2}\right)\cdot\left[\pi f\cos\left(\frac{\pi f}{2}\right)-\sin\left(\frac{\pi f}{2}\right)\right]}{\pi f^2} \tag{A.21}$$

Applying expression (A.21) on equation (A.10), the resulting equation is given as follows:

$$\frac{\text{sinc}^3\left(\frac{f}{2}\right)\cdot\left[\pi f\cos\left(\frac{\pi f}{2}\right)-\sin\left(\frac{\pi f}{2}\right)\right]}{\pi f^2} = 0 \tag{A.22}$$

where this last equation solutions correspond to critical points of expression (A.20). As observed for the rectangular envelope, equation (A.22) has multiple solutions. $f = 0$ Hz is a solution that is not useful. Considering positive frequency ($f > 0$ Hz), a possible solution can be found in the following equation:

$$\text{sinc}(f) = 0 \Leftrightarrow f = 2n \neq 0 \;;\; n \in \mathbb{Z} \tag{A.23}$$

The solutions of equation (A.23) correspond to the local minimum of function (A.20), as indicated in Figure A.2. It should be noticed that these frequency values are double compared with the ones from the rectangular envelope. This highlights that the symmetrical envelope spectrum is wider for strong attenuation. On the other hand, another solution can be achieved

in the equation below :

$$\pi f \cos\left(\frac{\pi f}{2}\right) - 2\sin\left(\frac{\pi f}{2}\right) = 0 \tag{A.24}$$

$$\frac{\pi f}{2} = \tan\left(\frac{\pi f}{2}\right) \tag{A.25}$$

Solving equation (A.25) numerically, the lowest value of f that satisfies equation (A.25) is approximately $f = 2.86$ Hz. This value is the double obtained for the rectangular envelope. Thus, it can inferred that the side-lobe rejection of the symmetrical triangular envelope will be higher than the one of the rectangular envelope.

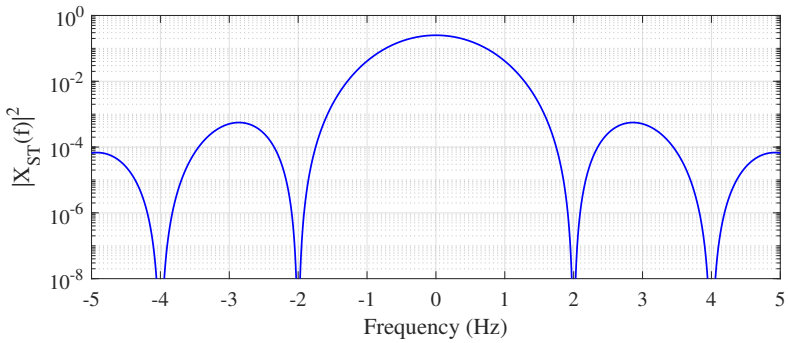


Figure A.2.: $|X(f)|^2$ as function of frequency.

A.3. Asymmetrical Triangular

Figure A.3 displays the asymmetrical triangular envelope and its derivative.

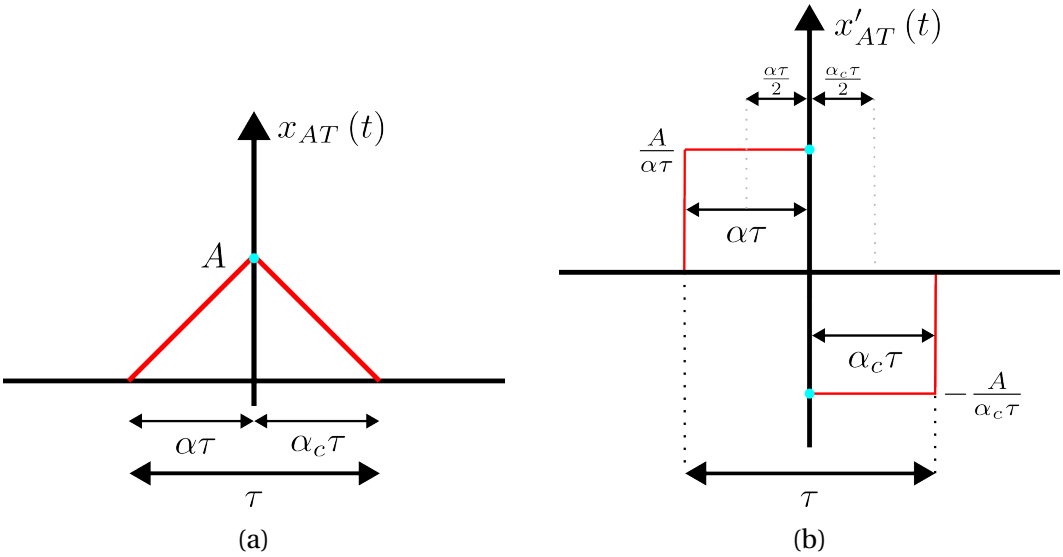


Figure A.3.: Asymmetrical triangular envelope and its derivative.

To obtain the asymmetrical triangular envelope Fourier transform, first of all, the derivative expression of the asymmetrical triangular envelope (Fig. A.3b) is described as follows:

$$x'_{AT}(t) = x'_{AT-R}(t) + x'_{AT-F}(t) \tag{A.26}$$

$$x'_{AT-R}(t) = \frac{A}{\alpha\tau} \cdot \Pi_{\alpha\tau}\left(t + \frac{\alpha\tau}{2}\right) \tag{A.27}$$

$$x'_{AT-F}(t) = -\frac{A}{\alpha_c\tau} \cdot \Pi_{\alpha_c\tau}\left(t - \frac{\alpha_c\tau}{2}\right) \tag{A.28}$$

where $x'_{AT-R}(t)$ and $x'_{AT-F}(t)$ correspond to the ascending and descending slope of the triangular envelope, respectively.

From the time differentiation property of Fourier transform [42], the Fourier transform of expression (A.27) can be calculated as follows:

$$X_{AT-R}(j\omega) \cdot j\omega = \mathscr{F}\left\{x'_{AT-R}(t)\right\} \tag{A.29}$$

$$X_{AT-R}(j\omega) \cdot j\omega = A\text{sinc}\left(\frac{\alpha\omega\tau}{2}\right) \cdot \exp\left(j\frac{\alpha\omega\tau}{2}\right) \tag{A.30}$$

$$X_{AT-R}(j\omega) \cdot j\omega = A\text{sinc}\left(\frac{\alpha\omega\tau}{2}\right) \cdot \left[\cos\left(\frac{\alpha\omega\tau}{2}\right) + j\sin\left(\frac{\alpha\omega\tau}{2}\right)\right] \tag{A.31}$$

$$X_{AT-R}(j\omega) = \frac{A}{\omega}\text{sinc}\left(\frac{\alpha\omega\tau}{2}\right) \cdot \left[-j\cos\left(\frac{\alpha\omega\tau}{2}\right) + \sin\left(\frac{\alpha\omega\tau}{2}\right)\right] \tag{A.32}$$

$$X_{AT-R}(j\omega) = \frac{A}{\omega}\text{sinc}\left(\frac{\alpha\omega\tau}{2}\right)\sin\left(\frac{\alpha\omega\tau}{2}\right) - j\frac{A}{\omega}\text{sinc}\left(\frac{\alpha\omega\tau}{2}\right)\cos\left(\frac{\alpha\omega\tau}{2}\right) \tag{A.33}$$

From the following trigonometrical identity:

$$\sin(2t) = 2\sin(t)\cos(t) \tag{A.34}$$

the expression (A.33) is hence manipulated as follows:

$$X_{AT-R}(j\omega) = \frac{A}{\omega}\text{sinc}\left(\frac{\alpha\omega\tau}{2}\right)\sin\left(\frac{\alpha\omega\tau}{2}\right) - j\frac{A}{\alpha\omega^2\tau}\sin(\alpha\omega\tau) \tag{A.35}$$

$$X_{AT-R}(j\omega) = \frac{A\alpha\tau}{2}\text{sinc}^2\left(\frac{\alpha\omega\tau}{2}\right) - j\frac{A}{\omega}\text{sinc}(\alpha\omega\tau) \tag{A.36}$$

On the other hand, the Fourier transform of expression (A.28) can be calculated as follows:

$$X_{AT-F}(j\omega) \cdot j\omega = \mathscr{F}\left\{x'_{AT-F}(t)\right\} \tag{A.37}$$

$$X_{AT-F}(j\omega) \cdot j\omega = A\text{sinc}\left(\frac{\alpha\omega\tau}{2}\right) \cdot \exp\left(-j\frac{\alpha\omega\tau}{2}\right) \tag{A.38}$$

$$X_{AT-F}(j\omega) \cdot j\omega = -A\text{sinc}\left(\frac{\alpha_c\omega\tau}{2}\right) \cdot \left[\cos\left(\frac{\alpha_c\omega\tau}{2}\right) - j\sin\left(\frac{\alpha_c\omega\tau}{2}\right)\right] \tag{A.39}$$

$$X_{AT-F}(j\omega) = \frac{A}{\omega}\text{sinc}\left(\frac{\alpha_c\omega\tau}{2}\right)\sin\left(\frac{\alpha_c\omega\tau}{2}\right) + j\frac{A}{\omega}\text{sinc}\left(\frac{\alpha_c\omega\tau}{2}\right)\cos\left(\frac{\alpha_c\omega\tau}{2}\right) \tag{A.40}$$

$$X_{AT-F}(j\omega) = \frac{A\alpha_c\tau}{2}\text{sinc}^2\left(\frac{\alpha_c\omega\tau}{2}\right) + j\frac{A}{\omega}\text{sinc}\left(\alpha_c\omega\tau\right) \tag{A.41}$$

Combining expressions (A.36) and (A.41), the asymmetrical triangular envelope Fourier transform can be evaluated as follows:

$$X_{AT}\left(j\omega\right) = X_{AT-R}\left(j\omega\right) + X_{AT-F}\left(j\omega\right) \tag{A.42}$$

$$\begin{aligned} X_{AT}\left(j\omega\right) = \frac{A\tau}{2}&\left[\alpha\text{sinc}^2\left(\frac{\alpha\omega\tau}{2}\right) + \alpha_c\text{sinc}^2\left(\frac{\alpha_c\omega\tau}{2}\right)\right] \\ &+ j\frac{A}{\omega}\left[\text{sinc}\left(\alpha_c\omega\tau\right) - \text{sinc}\left(\alpha\omega\tau\right)\right] \end{aligned} \tag{A.43}$$

since:

$$\omega = 2\pi f \tag{A.44}$$

The asymmetrical triangular envelope Fourier transform can be alternatively calculated as follows :

$$\begin{aligned} X_{AT}\left(f\right) = \frac{A\tau}{2}&\left[\alpha\text{sinc}^2\left(\alpha f\tau\right) + \alpha_c\text{sinc}^2\left(\alpha_c f\tau\right)\right] \\ &+ j\frac{A}{2\pi f}\left[\text{sinc}\left(2\alpha_c f\tau\right) - \text{sinc}\left(2\alpha f\tau\right)\right] \end{aligned} \tag{A.45}$$

It is worth pointing out that :

$$\lim_{f\to 0}\text{Im}\left\{X_{AT}\left(f\right)\right\} = 0 \;;\; 0 \le \alpha \le 1 \tag{A.46}$$

since:

$$\begin{aligned} \left[\text{Re}\left\{X_{AT}\left(f\right)\right\}\right]^2 = &\left(\frac{A\tau}{2}\right)^2\left[\alpha\text{sinc}^2\left(\alpha f\tau\right)\right]^2 \\ &+ \left(\frac{A\tau}{2}\right)^2\cdot 2\alpha\alpha_c\text{sinc}^2\left(\alpha f\tau\right)\text{sinc}^2\left(\alpha_c f\tau\right) \\ &+ \left(\frac{A\tau}{2}\right)^2\left[\alpha_c\text{sinc}^2\left(\alpha_c f\tau\right)\right]^2 \end{aligned} \tag{A.47}$$

$$\begin{aligned} \left[\text{Im}\left\{X_{AT}\left(f\right)\right\}\right]^2 = &\left(\frac{A}{2\pi f}\right)^2\text{sinc}^2\left(2\alpha_c f\tau\right) \\ &- \left(\frac{A}{2\pi f}\right)^2\cdot 2\text{sinc}\left(2\alpha_c f\tau\right)\text{sinc}\left(2\alpha f\tau\right) \\ &+ \left(\frac{A}{2\pi f}\right)^2\text{sinc}^2\left(2\alpha f\tau\right) \end{aligned} \tag{A.48}$$

it is possible to write:

$$\left|X_{AT}\left(f=0\right)\right|^2 = \left(\frac{A\tau}{2}\right)^2 \tag{A.49}$$

$$\begin{aligned}\left|X_{AT}\left(f=\frac{BW}{2}\right)\right|^2 = &\left(\frac{A\tau}{2}\right)^2\left[\alpha\text{sinc}^2\left(\frac{\alpha BW\cdot\tau}{2}\right)\right]^2\\ &+\left(\frac{A\tau}{2}\right)^2\cdot 2\alpha\alpha_c\text{sinc}^2\left(\frac{\alpha BW\cdot\tau}{2}\right)\text{sinc}^2\left(\frac{\alpha_c BW\cdot\tau}{2}\right)\\ &+\left(\frac{A\tau}{2}\right)^2\left[\alpha_c\text{sinc}^2\left(\frac{\alpha_c BW\cdot\tau}{2}\right)\right]^2\\ &+\left(\frac{A}{\pi BW}\right)^2\text{sinc}^2\left(\alpha_c BW\cdot\tau\right)\\ &-\left(\frac{A}{\pi BW}\right)^2\cdot 2\text{sinc}\left(\alpha_c BW\cdot\tau\right)\text{sinc}\left(\alpha BW\cdot\tau\right)\\ &+\left(\frac{A}{\pi BW}\right)^2\text{sinc}^2\left(\alpha BW\cdot\tau\right)\end{aligned} \tag{A.50}$$

Applying expression (A.45) on equation (2.5), the relation between asymmetrical triangular envelope bandwidth BW and attenuation X_{dB} can be described as follows:

$$\begin{aligned}10^{\frac{-X_{dB}}{10}} = &\left[\alpha\text{sinc}^2\left(\frac{\alpha BW\cdot\tau}{2}\right)\right]^2\\ &+2\alpha\alpha_c\text{sinc}^2\left(\frac{\alpha BW\cdot\tau}{2}\right)\text{sinc}^2\left(\frac{\alpha_c BW\cdot\tau}{2}\right)\\ &+\left[\alpha_c\text{sinc}^2\left(\frac{\alpha_c BW\cdot\tau}{2}\right)\right]^2\\ &+\frac{4}{(\pi BW\cdot\tau)^2}\text{sinc}^2\left(\alpha_c BW\cdot\tau\right)\\ &-\frac{8}{(\pi BW\cdot\tau)^2}\text{sinc}\left(\alpha_c BW\cdot\tau\right)\text{sinc}\left(\alpha BW\cdot\tau\right)\\ &+\frac{4}{(\pi BW\cdot\tau)^2}\text{sinc}^2\left(\alpha BW\cdot\tau\right)\end{aligned} \tag{A.51}$$

since $\tau = 1$ s, hence:

$$\begin{aligned}10^{\frac{-X_{dB}}{10}} = &\left[\alpha\text{sinc}^2\left(\frac{\alpha BW}{2}\right)\right]^2\\ &+2\alpha\alpha_c\text{sinc}^2\left(\frac{\alpha BW}{2}\right)\text{sinc}^2\left(\frac{\alpha_c BW}{2}\right)\\ &+\left[\alpha_c\text{sinc}^2\left(\frac{\alpha_c BW}{2}\right)\right]^2\\ &+\frac{4}{(\pi BW)^2}\text{sinc}^2\left(\alpha_c BW\right)\\ &-\frac{8}{(\pi BW)^2}\text{sinc}\left(\alpha_c BW\right)\text{sinc}\left(\alpha BW\right)\\ &+\frac{4}{(\pi BW)^2}\text{sinc}^2\left(\alpha BW\right)\end{aligned} \tag{A.52}$$

A.3.1. Saw-tooth

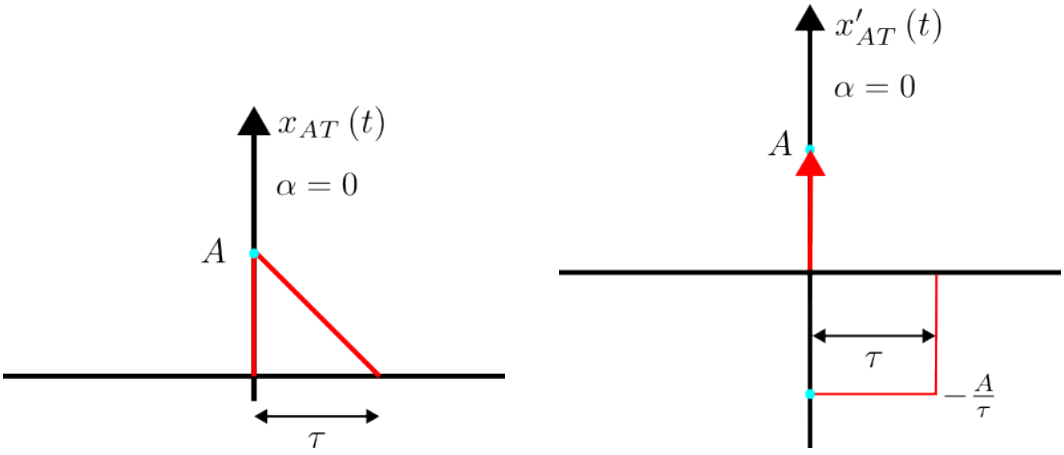
In particular, when the symmetry factor α is either 0 or 1, the asymmetrical triangular envelope can be defined as a saw-tooth envelope. For instance, if $\alpha = 0$, the expression (A.45) can manipulated as follows:

$$X_{AT}(f) = \frac{A\tau}{2}\text{sinc}^2(f\tau) + j\frac{A}{2\pi f}\left[\text{sinc}(2f\tau) - 1\right] \tag{A.53}$$

On the other hand, if $\alpha = 1$, the expression (A.45) can written as follows:

$$X_{AT}(f) = \frac{A\tau}{2}\text{sinc}^2(f\tau) + j\frac{A}{2\pi f}\left[1 - \text{sinc}(2f\tau)\right] \tag{A.54}$$

Moreover, a mathematical demonstration of the expression (A.53) is given. Figure A.3 displays the saw-tooth envelope waveform and its derivative ($\alpha = 0$).



(a) (b)

Figure A.4.: Saw-tooth envelope and its derivative ($\alpha = 0$).

To obtain the saw-tooth envelope Fourier transform, first of all, the derivative expression of the asymmetrical triangular envelope (Fig. A.4b) is described as follows:

$$x'_{AT}(t) = A\delta(t) - \frac{A}{\tau}\cdot\Pi_\tau\left(t + \frac{\tau}{2}\right) \tag{A.55}$$

From the time differentiation property of Fourier transform [42], the Fourier transform of expression (A.55) can be calculated as follows:

$$X_{AT}(j\omega)\cdot j\omega = \mathscr{F}\left\{x'_{AT}(t)\right\} \tag{A.56}$$

$$X_{AT}(j\omega)\cdot j\omega = A - A\,\text{sinc}\left(\frac{\omega\tau}{2}\right)\exp\left(-j\frac{\omega\tau}{2}\right) \tag{A.57}$$

$$X_{AT}(j\omega)\cdot j\omega = A - A\,\text{sinc}\left(\frac{\omega\tau}{2}\right)\cdot\left[\cos\left(\frac{\omega\tau}{2}\right) - j\sin\left(\frac{\omega\tau}{2}\right)\right] \tag{A.58}$$

$$X_{AT}(j\omega)\cdot j\omega = A - A\,\mathrm{sinc}\left(\frac{\omega\tau}{2}\right)\cos\left(\frac{\omega\tau}{2}\right) + jA\,\mathrm{sinc}\left(\frac{\omega\tau}{2}\right)\sin\left(\frac{\omega\tau}{2}\right) \tag{A.59}$$

$$X_{AT}(j\omega) = -j\frac{A}{\omega} + j\frac{A}{\omega}\,\mathrm{sinc}\left(\frac{\omega\tau}{2}\right)\cos\left(\frac{\omega\tau}{2}\right) + \frac{A}{\omega}\,\mathrm{sinc}\left(\frac{\omega\tau}{2}\right)\sin\left(\frac{\omega\tau}{2}\right) \tag{A.60}$$

$$X_{AT}(j\omega) = \frac{A}{\omega}\,\mathrm{sinc}\left(\frac{\omega\tau}{2}\right)\sin\left(\frac{\omega\tau}{2}\right) + j\frac{A}{\omega}\left[\mathrm{sinc}\left(\frac{\omega\tau}{2}\right)\cos\left(\frac{\omega\tau}{2}\right) - 1\right] \tag{A.61}$$

$$X_{AT}(j\omega) = \frac{AT}{2}\mathrm{sinc}^2\left(\frac{\omega\tau}{2}\right) + j\frac{A}{\omega}\left[\mathrm{sinc}\left(\omega\tau\right) - 1\right] \tag{A.62}$$

Finally, replacing ω for $2\pi f$ in the expression (A.62), it becomes the expression (A.53). In addition, it possible to obtain the expression (A.54) from expression (A.53) using the the time reversal property of Fourier transform [42, 44]. It is worth pointing out that the sinc function (2.12) is even.

From expression (2.17), assuming $\alpha = 0$, the ESD of the saw-tooth envelope can be expressed as follows:

$$\left|X_{AT}\left(f\right)\right|^2 = \left(\frac{A\tau}{2}\right)^2 \cdot \mathrm{sinc}^4\left(f\tau\right) + \left(\frac{A}{2\pi f}\right)^2 \cdot \left[\mathrm{sinc}\left(2f\tau\right) - 1\right]^2 \tag{A.63}$$

since $\tau = 1$ s and assuming an amplitude $A = 1$, the expression (A.63) is hence:

$$\left|X_{AT}\left(f\right)\right|^2 = \frac{\mathrm{sinc}^4\left(f\right)}{4} + \frac{\left(\mathrm{sinc}\left(2f\right) - 1\right)^2}{4\pi^2 f^2} \tag{A.64}$$

Assuming a symmetry factor $\alpha = 1$, the expression (A.64) is also obtained. Deriving the function (A.64), the following expression is given:

$$\begin{aligned}\frac{\mathrm{d}}{\mathrm{d}f}\left|X_{AT}\left(f\right)\right|^2 = {} & \frac{\sin^3\left(\pi f\right)\left[2\pi f\cos\left(\pi f\right) - \sin\left(\pi f\right)\right]}{2\pi^2 f^3} \\ & - \frac{1}{2\pi^2 f^3} - \frac{\pi f\cos\left(\pi f\right) - 3\sin\left(\pi f\right)}{2\pi^3 f^4} \\ & + \frac{\sin\left(\pi f\right)\left[\pi f\cos\left(\pi f\right) - 2\sin\left(\pi f\right)\right]}{2\pi^4 f^5}\end{aligned} \tag{A.65}$$

The function (A.65) does not have a null value for any frequency except at 0 Hz. As a result, the function (A.64) has no local maxima except at 0 Hz. In addition, from Figure 2.5, when the symmetry factor approaches 0 or 1, the side-lobe frequency approaches infinity, such as:

$$\lim_{\alpha\to 0^+} f_{Side-Lobe}\left(\alpha\right) = \infty \tag{A.66}$$

$$\lim_{\alpha\to 1^-} f_{Side-Lobe}\left(\alpha\right) = \infty \tag{A.67}$$

Since the side-lobe frequency approaches infinity, the expression (A.64) is strongly attenuated by the factor $1/f^2$, such that is approaches zero as indicated below:

$$\lim_{f\to\infty}\left|X_{AT}\left(f\right)\right|^2 = 0 \tag{A.68}$$

Consequently, the side-lobe rejection tends to the infinity. Therefore, from these equations, it can be stated that the ideal saw-tooth envelope does not present any side-lobes, like the ideal Gaussian envelope.

A.4. Symmetrical Trapezoidal

Figure A.5 displays the symmetrical trapezoidal envelope and its derivative.

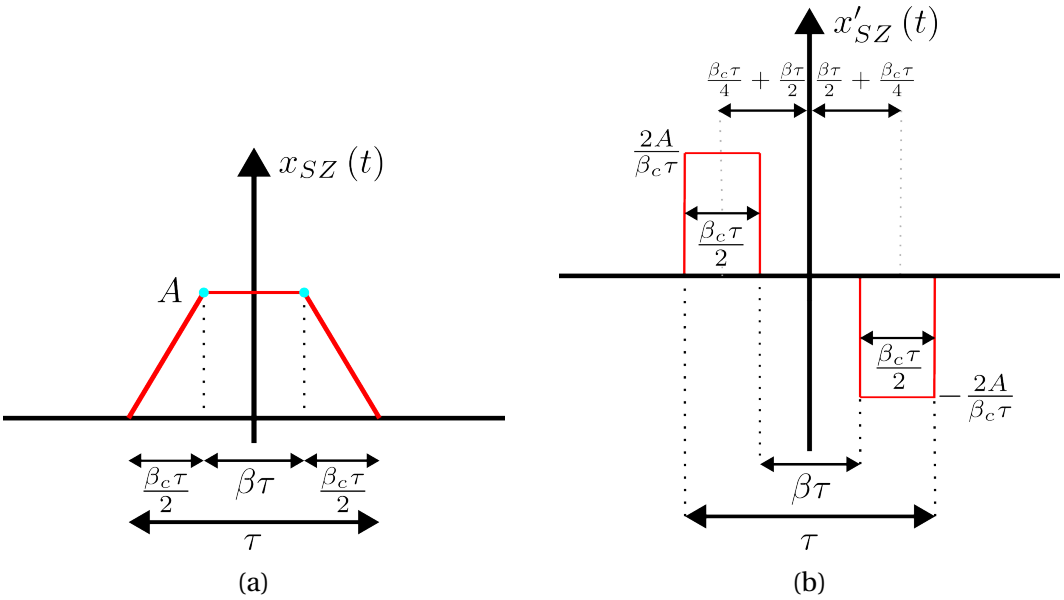


Figure A.5.: Symmetrical trapezoidal envelope and its derivative.

To obtain the symmetrical trapezoidal envelope Fourier transform, first of all, the derivative expression of the symmetrical trapezoidal envelope (Fig. A.5b) is described as follows:

$$x'_{SZ}(t)=\frac{2A}{\beta_c\tau}\cdot\Pi_{\frac{\beta_c\tau}{2}}\left(t+\frac{\beta_c\tau}{4}+\frac{\beta\tau}{2}\right)-\frac{2A}{\beta_c\tau}\cdot\Pi_{\frac{\beta_c\tau}{2}}\left(t-\frac{\beta_c\tau}{4}-\frac{\beta\tau}{2}\right) \tag{A.69}$$

$$x'_{SZ}(t)=\frac{2A}{\beta_c\tau}\cdot\Pi_{\frac{\beta_c\tau}{2}}\left(t+\frac{\tau(1+\beta)}{4}\right)-\frac{2A}{\beta_c\tau}\cdot\Pi_{\frac{\beta_c\tau}{2}}\left(t-\frac{\tau(1+\beta)}{4}\right) \tag{A.70}$$

From the time differentiation property of Fourier transform [42], the Fourier transform of expression (A.70) can be calculated as follows:

$$X_{SZ}(j\omega)\cdot j\omega=\mathscr{F}\left\{x'_{SZ}(t)\right\} \tag{A.71}$$

$$X_{SZ}(j\omega)\cdot j\omega=A\text{sinc}\left(\frac{\beta_c\omega\tau}{4}\right)\left[\exp\left(j\frac{\omega\tau(1+\beta)}{4}\right)-\exp\left(-j\frac{\omega\tau(1+\beta)}{4}\right)\right] \tag{A.72}$$

$$X_{SZ}(j\omega)\cdot j\omega=A\text{sinc}\left(\frac{\beta_c\omega\tau}{4}\right)\cdot 2j\sin\left(\frac{\omega\tau(1+\beta)}{4}\right) \tag{A.73}$$

$$X_{SZ}(j\omega) = \frac{2A}{\omega}\text{sinc}\left(\frac{\beta_c\omega\tau}{4}\right)\cdot\sin\left(\frac{\omega\tau(1+\beta)}{4}\right) \tag{A.74}$$

$$X_{SZ}(j\omega) = \frac{A\tau(1+\beta)}{2}\text{sinc}\left(\frac{\omega\tau(1-\beta)}{4}\right)\text{sinc}\left(\frac{\omega\tau(1+\beta)}{4}\right) \tag{A.75}$$

From expression (A.44), replacing ω for $2\pi f$, the symmetrical trapezoidal envelope Fourier transform can be expressed as follows :

$$X_{SZ}(f) = \frac{A\tau(1+\beta)}{2}\text{sinc}\left(\frac{f\tau(1-\beta)}{2}\right)\text{sinc}\left(\frac{f\tau(1+\beta)}{2}\right) \tag{A.76}$$

Applying expression (A.76) on equation (2.3), the emitted pulse mono-lateral Fourier transform can be computed as:

$$P^{+}_{SZ}(f) = \frac{A\tau(1+\beta)}{2\sqrt{2}}\text{sinc}\left(\frac{\tau(f-f_c)(1+\beta)}{2}\right)\text{sinc}\left(\frac{\tau(f-f_c)(1-\beta)}{2}\right)\exp(-j\phi) \tag{A.77}$$

Applying expression (A.76) on equation (2.5), the relation between symmetrical triangular envelope bandwidth BW and attenuation X_{dB} can be expressed as follows:

$$X_{dB} = 10\log\left(\frac{1}{\text{sinc}\left(\frac{BW\cdot\tau(1-\beta)}{4}\right)^2\cdot\text{sinc}\left(\frac{BW\cdot\tau(1+\beta)}{4}\right)^2}\right) \tag{A.78}$$

$$X_{dB} = -10\log\left(\text{sinc}\left(\frac{BW\cdot\tau(1-\beta)}{4}\right)^2\cdot\text{sinc}\left(\frac{BW\cdot\tau(1+\beta)}{4}\right)^2\right) \tag{A.79}$$

$$10^{\frac{-X_{dB}}{10}} = \text{sinc}\left(\frac{BW\cdot\tau(1-\beta)}{4}\right)^2\cdot\text{sinc}\left(\frac{BW\cdot\tau(1+\beta)}{4}\right)^2 \tag{A.80}$$

since $\tau = 1$ s, accordingly the expression of (A.80) is:

$$10^{\frac{-X_{dB}}{10}} = \text{sinc}\left(\frac{BW(1-\beta)}{4}\right)^2\cdot\text{sinc}\left(\frac{BW(1+\beta)}{4}\right)^2 \tag{A.81}$$

A.5. Asymmetrical Trapezoidal

Figure A.6 displays the asymmetrical trapezoidal envelope and its derivative.

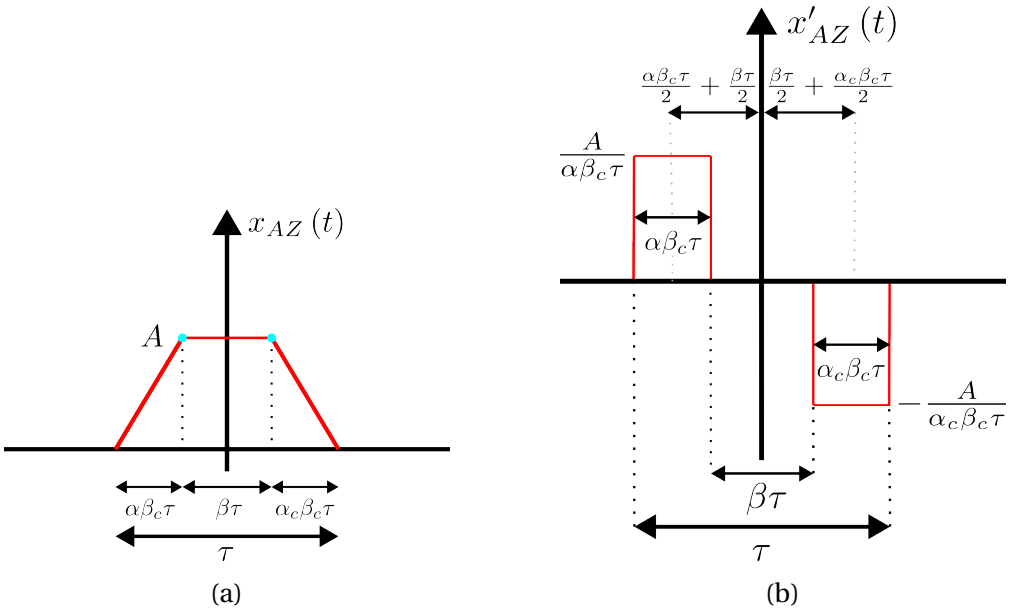


Figure A.6.: Asymmetrical trapezoidal envelope and its derivative.

To reach the asymmetrical trapezoidal envelope Fourier transform, first of all, the derivative expression of the asymmetrical triangular envelope (Fig. A.6b) is described as follows:

$$x'_{AZ}(t) = x'_{AZ-R}(t) + x'_{AZ-F}(t) \tag{A.82}$$

$$x'_{AZ-R}(t) = \frac{A}{\alpha\beta_c\tau} \cdot \Pi_{\alpha\beta_c\tau}\left(t + \frac{\alpha\beta_c\tau}{2} + \frac{\beta\tau}{2}\right) \tag{A.83}$$

$$x'_{AZ-F}(t) = \frac{A}{\alpha_c\beta_c\tau} \cdot \Pi_{\alpha_c\beta_c\tau}\left(t - \frac{\alpha_c\beta_c\tau}{2} - \frac{\beta\tau}{2}\right) \tag{A.84}$$

where $x'_{AZ-R}(t)$ and $x'_{AZ-F}(t)$ correspond respectively to the ascending and descending slope of the trapezoidal envelope. Alternatively, the expressions (A.83) and (A.84) can be rewritten as follows:

$$x'_{AZ-R}(t) = \frac{A}{\alpha\beta_c\tau} \cdot \Pi_{\alpha\beta_c\tau}\left(t + \frac{\tau(\alpha+\beta-\alpha\beta)}{2}\right) \tag{A.85}$$

$$x'_{AZ-F}(t) = \frac{A}{\alpha_c\beta_c\tau} \cdot \Pi_{\alpha_c\beta_c\tau}\left(t - \frac{\tau(\alpha_c+\beta-\alpha_c\beta)}{2}\right) \tag{A.86}$$

From the time differentiation property of Fourier transform [42], the Fourier transform of expression (A.85) can be calculated as follows:

$$X_{AZ-R}(j\omega) \cdot j\omega = \mathscr{F}\left\{x'_{AZ-R}(t)\right\} \tag{A.87}$$

$$X_{AZ-R}(j\omega)\cdot j\omega = A\text{sinc}\left(\frac{\alpha\beta_c\omega\tau}{2}\right)\exp\left(j\frac{\omega\tau(\alpha+\beta-\alpha\beta)}{2}\right) \tag{A.88}$$

$$\begin{aligned} X_{AZ-R}(j\omega)\cdot j\omega = {} & A\text{sinc}\left(\frac{\alpha\beta_c\omega\tau}{2}\right)\cos\left(\frac{\omega\tau(\alpha+\beta-\alpha\beta)}{2}\right) \\ & + jA\text{sinc}\left(\frac{\alpha\beta_c\omega\tau}{2}\right)\sin\left(\frac{\omega\tau(\alpha+\beta-\alpha\beta)}{2}\right) \end{aligned} \tag{A.89}$$

$$\begin{aligned} X_{AZ-R}(j\omega) = {} & -j\frac{A}{\omega}\text{sinc}\left(\frac{\alpha\beta_c\omega\tau}{2}\right)\cos\left(\frac{\omega\tau(\alpha+\beta-\alpha\beta)}{2}\right) \\ & + \frac{A}{\omega}\text{sinc}\left(\frac{\alpha\beta_c\omega\tau}{2}\right)\sin\left(\frac{\omega\tau(\alpha+\beta-\alpha\beta)}{2}\right) \end{aligned} \tag{A.90}$$

$$\begin{aligned} X_{AZ-R}(j\omega) = {} & \frac{A\tau(\alpha+\beta-\alpha\beta)}{2}\text{sinc}\left(\frac{\alpha\beta_c\omega\tau}{2}\right)\text{sinc}\left(\frac{\omega\tau(\alpha+\beta-\alpha\beta)}{2}\right) \\ & - j\frac{A}{\omega}\text{sinc}\left(\frac{\alpha\beta_c\omega\tau}{2}\right)\cos\left(\frac{\omega\tau(\alpha+\beta-\alpha\beta)}{2}\right) \end{aligned} \tag{A.91}$$

On the other hand, from the time differentiation property of Fourier transform [42], the Fourier transform of expression (A.86) can be calculated as follows:

$$X_{AZ-F}(j\omega)\cdot j\omega = \mathscr{F}\left\{x'_{AZ-F}(t)\right\} \tag{A.92}$$

$$X_{AZ-F}(j\omega)\cdot j\omega = A\text{sinc}\left(\frac{\alpha_c\beta_c\omega\tau}{2}\right)\exp\left(-j\frac{\omega\tau(\alpha_c+\beta-\alpha_c\beta)}{2}\right) \tag{A.93}$$

$$\begin{aligned} X_{AZ-F}(j\omega)\cdot j\omega = {} & A\text{sinc}\left(\frac{\alpha_c\beta_c\omega\tau}{2}\right)\cos\left(\frac{\omega\tau(\alpha_c+\beta-\alpha_c\beta)}{2}\right) \\ & + jA\text{sinc}\left(\frac{\alpha_c\beta_c\omega\tau}{2}\right)\sin\left(\frac{\omega\tau(\alpha_c+\beta-\alpha\beta)}{2}\right) \end{aligned} \tag{A.94}$$

$$\begin{aligned} X_{AZ-F}(j\omega) = {} & -j\frac{A}{\omega}\text{sinc}\left(\frac{\alpha_c\beta_c\omega\tau}{2}\right)\cos\left(\frac{\omega\tau(\alpha_c+\beta-\alpha_c\beta)}{2}\right) \\ & + \frac{A}{\omega}\text{sinc}\left(\frac{\alpha_c\beta_c\omega\tau}{2}\right)\sin\left(\frac{\omega\tau(\alpha_c+\beta-\alpha_c\beta)}{2}\right) \end{aligned} \tag{A.95}$$

$$\begin{aligned} X_{AZ-F}(j\omega) = {} & \frac{A\tau(\alpha_c+\beta-\alpha_c\beta)}{2}\text{sinc}\left(\frac{\alpha_c\beta_c\omega\tau}{2}\right)\text{sinc}\left(\frac{\omega\tau(\alpha_c+\beta-\alpha_c\beta)}{2}\right) \\ & + j\frac{A}{\omega}\text{sinc}\left(\frac{\alpha_c\beta_c\omega\tau}{2}\right)\cos\left(\frac{\omega\tau(\alpha_c+\beta-\alpha_c\beta)}{2}\right) \end{aligned} \tag{A.96}$$

Combining expressions (A.91) and (A.96), the asymmetrical trapezoidal envelope Fourier transform can be evaluated as follows:

$$X_{AZ}(j\omega) = X_{AZ-R}(j\omega) + X_{AZ-F}(j\omega) \tag{A.97}$$

$$\begin{aligned}\mathrm{Re}\left(X_{AZ}\left(j\omega\right)\right) = &\frac{A\tau\left(\alpha+\beta-\alpha\beta\right)}{2}\mathrm{sinc}\left(\frac{\alpha\beta_c\omega\tau}{2}\right)\mathrm{sinc}\left(\frac{\omega\tau\left(\alpha+\beta-\alpha\beta\right)}{2}\right)\\ &+\frac{A\tau\left(\alpha_c+\beta-\alpha_c\beta\right)}{2}\mathrm{sinc}\left(\frac{\alpha_c\beta_c\omega\tau}{2}\right)\mathrm{sinc}\left(\frac{\omega\tau\left(\alpha_c+\beta-\alpha_c\beta\right)}{2}\right)\end{aligned} \tag{A.98}$$

$$\begin{aligned}\mathrm{Im}\left(X_{AZ}\left(j\omega\right)\right) = &-\frac{A}{\omega}\mathrm{sinc}\left(\frac{\alpha\beta_c\omega\tau}{2}\right)\cos\left(\frac{\omega\tau\left(\alpha+\beta-\alpha\beta\right)}{2}\right)\\ &+\frac{A}{\omega}\mathrm{sinc}\left(\frac{\alpha_c\beta_c\omega\tau}{2}\right)\cos\left(\frac{\omega\tau\left(\alpha_c+\beta-\alpha_c\beta\right)}{2}\right)\end{aligned} \tag{A.99}$$

From equation (A.44), replacing ω for $2\pi f$, the asymmetrical trapezoidal envelope Fourier transform can be written as follows :

$$\begin{aligned}\mathrm{Re}\left(X_{AZ}\left(f\right)\right) = &\frac{A\tau\left(\alpha+\beta-\alpha\beta\right)}{2}\mathrm{sinc}\left(\alpha\beta_c f\tau\right)\mathrm{sinc}\left(f\tau\left(\alpha+\beta-\alpha\beta\right)\right)\\ &+\frac{A\tau\left(\alpha_c+\beta-\alpha_c\beta\right)}{2}\mathrm{sinc}\left(\alpha_c\beta_c f\tau\right)\mathrm{sinc}\left(f\tau\left(\alpha_c+\beta-\alpha_c\beta\right)\right)\end{aligned} \tag{A.100}$$

$$\begin{aligned}\mathrm{Im}\left(X_{AZ}\left(f\right)\right) = &-\frac{A}{2\pi f}\mathrm{sinc}\left(\alpha\beta_c f\tau\right)\cos\left(\pi f\tau\left(\alpha+\beta-\alpha\beta\right)\right)\\ &+\frac{A}{2\pi f}\mathrm{sinc}\left(\alpha_c\beta_c f\tau\right)\cos\left(\pi f\tau\left(\alpha_c+\beta-\alpha_c\beta\right)\right)\end{aligned} \tag{A.101}$$

since:

$$\begin{aligned}&\left[\mathrm{Re}\left\{X_{AZ}\left(f\right)\right\}\right]^2 = \left(\frac{A\tau}{2}\right)^2\left(\alpha+\beta-\alpha\beta\right)^2\mathrm{sinc}^2\left(\alpha\beta_c f\tau\right)\mathrm{sinc}^2\left(f\tau\left(\alpha+\beta+\alpha\beta\right)\right)\\ &+\left(\frac{A\tau}{2}\right)^2 2\left(\alpha+\beta-\alpha\beta\right)\left(\alpha_c+\beta-\alpha_c\beta\right)\mathrm{sinc}\left(\alpha\beta_c f\tau\right)\\ &\cdot\mathrm{sinc}\left(f\tau\left(\alpha+\beta-\alpha\beta\right)\right)\mathrm{sinc}\left(\alpha_c\beta_c f\tau\right)\mathrm{sinc}\left(f\tau\left(\alpha_c+\beta-\alpha_c\beta\right)\right)\\ &+\left(\frac{A\tau}{2}\right)^2\left(\alpha_c+\beta-\alpha_c\beta\right)^2\mathrm{sinc}^2\left(\alpha_c\beta_c f\tau\right)\mathrm{sinc}^2\left(f\tau\left(\alpha_c+\beta+\alpha_c\beta\right)\right)\end{aligned} \tag{A.102}$$

$$\begin{aligned}&\left[\mathrm{Im}\left\{X_{AZ}\left(f\right)\right\}\right]^2 = \left(\frac{A}{2\pi f}\right)^2\mathrm{sinc}^2\left(\alpha_c\beta_c f\tau\right)\cos^2\left(\pi f\tau\left(\alpha_c+\beta-\alpha_c\beta\right)\right)\\ &-\left(\frac{A}{2\pi f}\right)^2 2\mathrm{sinc}\left(\alpha_c\beta_c f\tau\right)\mathrm{sinc}\left(\alpha\beta_c f\tau\right)\\ &\cdot\cos\left(\pi f\tau\left(\alpha_c+\beta-\alpha_c\beta\right)\right)\cos\left(\pi f\tau\left(\alpha+\beta-\alpha\beta\right)\right)\\ &+\left(\frac{A}{2\pi f}\right)^2\mathrm{sinc}^2\left(\alpha\beta_c f\tau\right)\cos^2\left(\pi f\tau\left(\alpha+\beta-\alpha\beta\right)\right)\end{aligned} \tag{A.103}$$

it is possible to write:

$$\left|X_{AZ}\left(f=0\right)\right|^2 = \left(\frac{A\tau}{2}\right)^2\left(1+\beta\right)^2 \tag{A.104}$$

$$
\begin{aligned}
&\left|X_{AZ}\left(f=\frac{BW}{2}\right)\right|^2=\left(\frac{A\tau}{2}\right)^2\left(\alpha+\beta-\alpha\beta\right)^2\operatorname{sinc}^2\left(\frac{\alpha\beta_c BW\cdot\tau}{2}\right)\operatorname{sinc}^2\left(\frac{BW\cdot\tau\left(\alpha+\beta+\alpha\beta\right)}{2}\right)\\
&+\left(\frac{A\tau}{2}\right)^2 2\left(\alpha+\beta-\alpha\beta\right)\left(\alpha_c+\beta-\alpha_c\beta\right)\operatorname{sinc}\left(\frac{\alpha\beta_c BW\cdot\tau}{2}\right)\\
&\cdot\operatorname{sinc}\left(\frac{BW\cdot\tau\left(\alpha+\beta-\alpha\beta\right)}{2}\right)\operatorname{sinc}\left(\frac{\alpha_c\beta_c BW\cdot\tau}{2}\right)\operatorname{sinc}\left(\frac{BW\cdot\tau\left(\alpha_c+\beta-\alpha_c\beta\right)}{2}\right)\\
&+\left(\frac{A\tau}{2}\right)^2\left(\alpha_c+\beta-\alpha_c\beta\right)^2\operatorname{sinc}^2\left(\frac{\alpha_c\beta_c BW\cdot\tau}{2}\right)\operatorname{sinc}^2\left(\frac{BW\cdot\tau\left(\alpha_c+\beta+\alpha_c\beta\right)}{2}\right)\\
&+\left(\frac{A}{\pi BW}\right)^2\operatorname{sinc}^2\left(\frac{\alpha_c\beta_c BW\cdot\tau}{2}\right)\cos^2\left(\frac{\pi BW\cdot\tau\left(\alpha_c+\beta-\alpha_c\beta\right)}{2}\right)\\
&-\left(\frac{A}{\pi BW}\right)^2 2\operatorname{sinc}\left(\frac{\alpha_c\beta_c BW\cdot\tau}{2}\right)\operatorname{sinc}\left(\frac{\alpha\beta_c BW\cdot\tau}{2}\right)\\
&\cdot\cos\left(\frac{\pi BW\cdot\tau\left(\alpha_c+\beta-\alpha_c\beta\right)}{2}\right)\cos\left(\frac{\pi BW\cdot\tau\left(\alpha+\beta-\alpha\beta\right)}{2}\right)\\
&+\left(\frac{A}{\pi BW}\right)^2\operatorname{sinc}^2\left(\frac{\alpha\beta_c BW\cdot\tau}{2}\right)\cos^2\left(\frac{\pi BW\cdot\tau\left(\alpha+\beta-\alpha\beta\right)}{2}\right)
\end{aligned}
\tag{A.105}
$$

Applying expression (A.45) on equation (2.5), the relation between asymmetrical trapezoidal envelope bandwidth BW and attenuation X_{dB} can be described as follows:

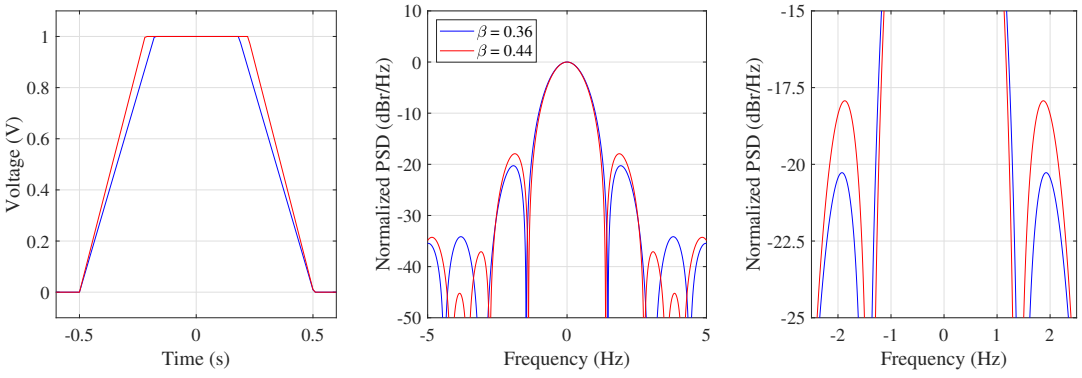
$$
\begin{aligned}
&10^{\frac{-X_{dB}}{10}}=\left(\frac{\alpha+\beta-\alpha\beta}{1+\beta}\right)^2\operatorname{sinc}^2\left(\frac{\alpha\beta_c BW\cdot\tau}{2}\right)\operatorname{sinc}^2\left(\frac{BW\cdot\tau\left(\alpha+\beta+\alpha\beta\right)}{2}\right)\\
&+\frac{2\left(\alpha+\beta-\alpha\beta\right)\left(\alpha_c+\beta-\alpha_c\beta\right)}{\left(1+\beta\right)^2}\operatorname{sinc}\left(\frac{\alpha\beta_c BW\cdot\tau}{2}\right)\\
&\cdot\operatorname{sinc}\left(\frac{BW\cdot\tau\left(\alpha+\beta-\alpha\beta\right)}{2}\right)\operatorname{sinc}\left(\frac{\alpha_c\beta_c BW\cdot\tau}{2}\right)\operatorname{sinc}\left(\frac{BW\cdot\tau\left(\alpha_c+\beta-\alpha_c\beta\right)}{2}\right)\\
&+\left(\frac{\alpha_c+\beta-\alpha_c\beta}{1+\beta}\right)^2\operatorname{sinc}^2\left(\frac{\alpha_c\beta_c BW\cdot\tau}{2}\right)\operatorname{sinc}^2\left(\frac{BW\cdot\tau\left(\alpha_c+\beta+\alpha_c\beta\right)}{2}\right)\\
&+\frac{4}{\left(\pi BW\cdot\tau\right)^2\left(1+\beta\right)^2}\operatorname{sinc}^2\left(\frac{\alpha_c\beta_c BW\cdot\tau}{2}\right)\cos^2\left(\frac{\pi BW\cdot\tau\left(\alpha_c+\beta-\alpha_c\beta\right)}{2}\right)\\
&-\frac{8}{\left(\pi BW\cdot\tau\right)^2\left(1+\beta\right)^2}\operatorname{sinc}\left(\frac{\alpha_c\beta_c BW\cdot\tau}{2}\right)\operatorname{sinc}\left(\frac{\alpha_c\beta_c BW\cdot\tau}{2}\right)\\
&\cdot\cos\left(\frac{\pi BW\cdot\tau\left(\alpha_c+\beta-\alpha_c\beta\right)}{2}\right)\cos\left(\frac{\pi BW\cdot\tau\left(\alpha+\beta-\alpha\beta\right)}{2}\right)\\
&+\frac{4}{\left(\pi BW\cdot\tau\right)^2\left(1+\beta\right)^2}\operatorname{sinc}^2\left(\frac{\alpha\beta_c BW\cdot\tau}{2}\right)\cos^2\left(\frac{\pi BW\cdot\tau\left(\alpha+\beta-\alpha\beta\right)}{2}\right)
\end{aligned}
\tag{A.106}
$$

since $\tau = 1$ s, therefore the expression of (A.106) is:

$$
\begin{aligned}
10^{\frac{-X_{dB}}{10}} &= \left(\frac{\alpha+\beta-\alpha\beta}{1+\beta}\right)^2 \operatorname{sinc}^2\left(\frac{\alpha\beta_c BW}{2}\right)\operatorname{sinc}^2\left(\frac{BW\left(\alpha+\beta+\alpha\beta\right)}{2}\right) \\
&+ \frac{2\left(\alpha+\beta-\alpha\beta\right)\left(\alpha_c+\beta-\alpha_c\beta\right)}{\left(1+\beta\right)^2}\operatorname{sinc}\left(\frac{\alpha\beta_c BW}{2}\right) \\
&\cdot \operatorname{sinc}\left(\frac{BW\left(\alpha+\beta-\alpha\beta\right)}{2}\right)\operatorname{sinc}\left(\frac{\alpha_c\beta_c BW}{2}\right)\operatorname{sinc}\left(\frac{BW\left(\alpha_c+\beta-\alpha_c\beta\right)}{2}\right) \\
&+ \left(\frac{\alpha_c+\beta-\alpha_c\beta}{1+\beta}\right)^2 \operatorname{sinc}^2\left(\frac{\alpha_c\beta_c BW}{2}\right)\operatorname{sinc}^2\left(\frac{BW\left(\alpha_c+\beta+\alpha_c\beta\right)}{2}\right) \\
&+ \frac{4}{(\pi BW)^2\left(1+\beta\right)^2}\operatorname{sinc}^2\left(\frac{\alpha_c\beta_c BW}{2}\right)\cos^2\left(\frac{\pi BW\left(\alpha_c+\beta-\alpha_c\beta\right)}{2}\right) \\
&- \frac{8}{(\pi BW)^2\left(1+\beta\right)^2}\operatorname{sinc}\left(\frac{\alpha_c\beta_c BW}{2}\right)\operatorname{sinc}\left(\frac{\alpha_c\beta_c BW}{2}\right) \\
&\cdot \cos\left(\frac{\pi BW\left(\alpha_c+\beta-\alpha_c\beta\right)}{2}\right)\cos\left(\frac{\pi BW\left(\alpha+\beta-\alpha\beta\right)}{2}\right) \\
&+ \frac{4}{(\pi BW)^2\left(1+\beta\right)^2}\operatorname{sinc}^2\left(\frac{\alpha\beta_c BW}{2}\right)\cos^2\left(\frac{\pi BW\left(\alpha+\beta-\alpha\beta\right)}{2}\right)
\end{aligned}
\tag{A.107}
$$

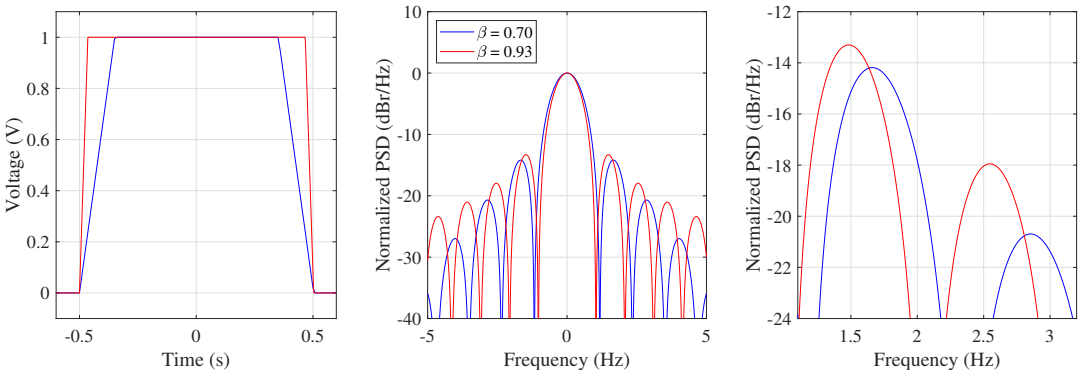
B. Symmetrical Trapezoidal envelope bandwidth particularities

The curves of Figures 2.8c and 2.8d have two steep rises. These steep rises can be explained in Figures B.1 and B.2. Figure B.1 presents symmetrical trapezoidal envelope waveforms and spectra for several values of β (0.36 and 0.44). Figure B.2 presents symmetrical trapezoidal envelope waveforms and spectrum for several values of higher β (0.73 and 0.93). From Figure B.1, it can be noticed that the adjacent lobe rejection for $\beta = 0.44$ is lower than 18 dB, whereas the adjacent lobe for $\beta = 0.36$ is greater than 20 dB. The bandwidth $BW_{-X=20dB}$ for $\beta = 0.44$ includes the first adjacent lobe, unlike the bandwidth BW_{-20dB} for $\beta = 0.36$. Hence, for a surface factor greater than 0.44, the bandwidth BW_{-20dB} includes at least the first side-lobe. Furthermore, from Figure B.2, it can be seen that the second side-lobe rejection for $\beta = 0.93$ is 18 dB, whereas the second side-lobe rejection of $\beta = 0.70$ is greater than 20 dB. The bandwidth BW_{-20dB} for $\beta = 0.93$ encompasses the first and second side-lobes, contrary to the bandwidth BW_{-20dB} for $\beta = 0.70$. Accordingly, for a surface factor greater than 0.93, the bandwidth BW_{-20dB} covers at least the first and second side-lobes. In conclusion, each steep rise corresponds to the inclusion of an adjacent side-lobe at the envelope spectrum bandwidth.



(a) Waveform (b) Spectrum (c) Spectrum (Zoomed)

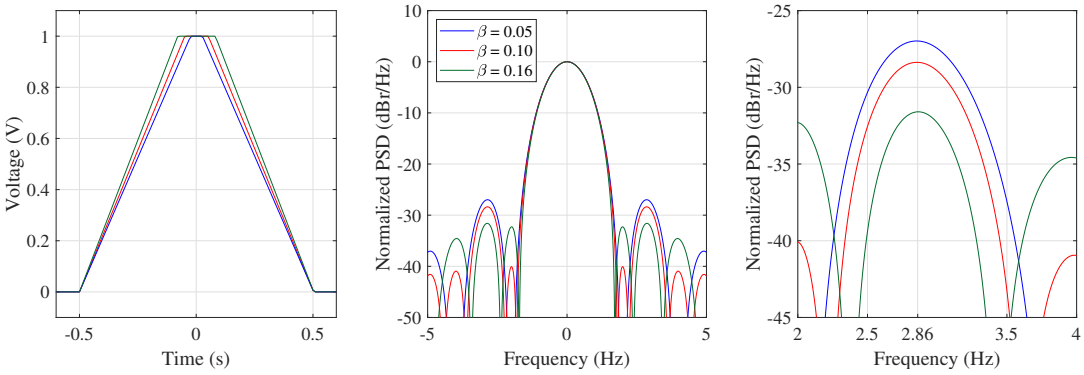
Figure B.1.: Symmetrical trapezoidal envelope waveforms and spectra for $\beta = 0.36$ and 0.44 ($\tau = 1$)



(a) Waveform (b) Spectrum (c) Spectrum (Zoomed)

Figure B.2.: Symmetrical trapezoidal envelope waveforms and spectra for $\beta = 0.70$ and 0.93 ($\tau = 1$)

Besides, from Figure 2.9, it can be observed that for a surface factor lower than 0.164, the frequency remains approximately at 2.86 Hz. Figure B.3 presents symmetrical trapezoidal envelope waveforms and spectra for several values of β (0.05, 0.10 and 0.16). From Figure B.3, it can be perceived that all three side-lobes are at the same frequency (2.86 Hz). Hence, symmetrical trapezoidal envelopes whose shape resembles a triangle have nearly the same side-lobe frequency.



(a) Waveform (b) Spectrum (c) Spectrum (Zoomed)

Figure B.3.: Symmetrical trapezoidal envelope waveforms and spectra for $\beta = 0.05$, 0.10 and 0.16 ($\tau = 1$).

C. Sample and Hold Envelope Equations

C.1. Uniform Sample and Hold

First of all, the expression (2.53) can be rewritten as follows:

$$x_{USH}(t) = \sum_{n=1}^{N} x_C(n\tau_S - \sigma_0) \cdot \Pi_{\tau_n}(t - (n\tau_S - \sigma_0)) \tag{C.1}$$

Shifting to the frequency domain, the Fourier transform of the uniform sample and hold envelope is given as follows:

$$X_{USH}(f) = \sum_{n=1}^{N} x_C(n\tau_S - \sigma_0) \cdot \tau_s \cdot \text{sinc}(f\tau_S) exp(-j2\pi f(n\tau_S - \sigma_0)) \tag{C.2}$$

$$X_{USH}(f) = \tau_s \cdot \text{sinc}(f\tau_S) \sum_{n=1}^{N} x_C(n\tau_S - \sigma_0) exp(-j2\pi f(n\tau_S - \sigma_0)) \tag{C.3}$$

From expression (C.3), an expression is defined as:

$$X_\pi(f) = \sum_{n=1}^{N} x_C(n\tau_S - \sigma_0) exp(-j2\pi f(n\tau_S - \sigma_0)) \tag{C.4}$$

Shifting this expression to the time domain, the following expression is calculated such as:

$$x_\pi(t) = \sum_{n=1}^{N} x_C(n\tau_S - \sigma_0) \delta(t - (n\tau_S - \sigma_0)) \tag{C.5}$$

From the Dirac delta sifting property [44], the expression (C.5) can be rewritten as:

$$x_\pi(t) = x_C(t) \sum_{n=1}^{N} \delta(t - (n\tau_S - \sigma_0)) \tag{C.6}$$

Hence, it can be observed that $x_C(t)$ is multiplied by a Dirac comb function [43]. Alternatively, from the convolution property, the Fourier transform expression (C.4) can be expressed as [42, 43]:

$$X_\pi(f) = X_C(f) * \mathscr{F}\left\{\sum_{n=1}^{N} \delta(t - (n\tau_S - \sigma_0))\right\} \tag{C.7}$$

where:

$$\mathscr{F}\left\{\sum_{n=1}^{N} \delta(t - (n\tau_S - \sigma_0))\right\} = exp(j2\pi\sigma_0)\mathscr{F}\left\{\sum_{n=1}^{N} \delta(t - n\tau_S)\right\} \tag{C.8}$$

and $\mathscr{F}\{\}$ is the Fourier transform operator. Since a Fourier transform of a Dirac comb function is also a Dirac comb function [43], the Fourier transform expression (C.8) is written as:

$$\mathscr{F}\left\{\sum_{n=1}^{N}\delta\left(t-(n\tau_S-\sigma_0)\right)\right\}=exp\left(j2\pi\sigma_0\right)\cdot\frac{1}{\tau_S}\delta\left(f-\frac{n}{\tau_S}\right) \tag{C.9}$$

Therefore:

$$X_\pi(f)=X_C(f)*exp\left(j2\pi\sigma_0\right)\cdot\frac{1}{\tau_S}\delta\left(f-\frac{n}{\tau_S}\right) \tag{C.10}$$

Given the convolution of any time function with the Dirac delta function leaves that function unchanged (replication property of the Dirac delta function) [44], the expression (C.10) can be written as:

$$X_\pi(f)=\frac{exp\left(j2\pi\sigma_0\right)}{\tau_S}\cdot\sum_{n=1}^{N}X_C\left(f-\frac{n}{\tau_S}\right) \tag{C.11}$$

Finally, the Fourier transform of uniform sample and hold envelope (C.3) can be manipulated as [13]:

$$X_{USH}(f)=\text{sinc}\left(f\tau_S\right)exp\left(j2\pi\sigma_0\right)\cdot\sum_{n=1}^{N}X_C\left(f-\frac{n}{\tau_S}\right) \tag{C.12}$$

Alternatively, from equation (2.47), this Fourier transform can be expressed as:

$$X_{USH}(f)=\text{sinc}\left(\frac{f}{F_S}\right)exp\left(j2\pi\sigma_0\right)\cdot\sum_{n=1}^{N}X_C\left(f-nF_S\right) \tag{C.13}$$

C.2. Optimization constraints

Concerning approach B (non-uniform sample and hold), considering an asymmetrical envelope, to respect the condition given by the equation 2.58, the interval of allowed values of ρ_i is defined as follows :

$$\rho_1=\left[\rho_{min},1-(N-1)\,\rho_{min}\right] \tag{C.14}$$

$$\rho_2=\left[\rho_{min},1-(N-2)\,\rho_{min}-\rho_1\right] \tag{C.15}$$

$$\rho_3=\left[\rho_{min},1-(K-3)\,\rho_{min}-\left(\rho_1+\rho_2\right)\right] \tag{C.16}$$

where ρ_{min} corresponds to the minimal normalized sample duration set for optimization. The value of ρ_{min} should be greater than 0 since τ_n should be greater than 0. The general range of allowed values of ρ_i is given as follows :

$$\rho_i=\left[\rho_{min},1-(K-i)\,\rho_{min}-\sum_{j=1}^{i-1}\rho_j\right]\quad;\quad 1<i<N \tag{C.17}$$

Finally, to comply with equation 2.58, the last normalized sample duration is expressed as

follows :

$$\rho_N = 1 - \sum_{i=1}^{N-1} \rho_i \tag{C.18}$$

Nevertheless, if a symmetrical envelope, whose number of samples is even, is taken into account, the interval of allowed values of ρ_i is described as follows :

$$\rho_1 = \left[\rho_{min}, \frac{1 - 2\,(N-1)\,\rho_{min}}{2} \right] \tag{C.19}$$

$$\rho_2 = \left[\rho_{min}, \frac{1 - 2\,(N-2)\,\rho_{min} - 2\rho_1}{2} \right] \tag{C.20}$$

$$\rho_3 = \left[\rho_{min}, \frac{1 - 2\,(N-3)\,\rho_{min} - 2\left(\rho_1 + \rho_2\right)}{2} \right] \tag{C.21}$$

Thus:

$$\rho_i = \left[\rho_{min}, \frac{1 - 2\,(N-i)\,\rho_{min} - 2\sum_{j=1}^{i-1} \rho_j}{2} \right] \quad ; \quad 1 < i < \frac{N}{2} \tag{C.22}$$

To comply with equation 2.58, the last normalized sample duration is expressed as follows :

$$\rho_N = \frac{1}{2} \left(1 - 2 \sum_{i=1}^{\frac{N}{2}-1} \rho_i \right) \tag{C.23}$$

Alternatively, if a symmetrical envelope, whose number of samples is odd, is taken into account, the interval of allowed values of ρ_i is written as follows :

$$\rho_1 = \left[\rho_{min}, \frac{1 - 2\,(N-2)\,\rho_{min} - \rho_{min}}{2} \right] \tag{C.24}$$

$$\rho_2 = \left[\rho_{min}, \frac{1 - 2\,(N-3)\,\rho_{min} - \rho_{min} - 2\rho_1}{2} \right] \tag{C.25}$$

$$\rho_3 = \left[\rho_{min}, \frac{1 - 2\,(K-4)\,\rho_{min} - \rho_{min} - 2\left(\rho_1 + \rho_2\right)}{2} \right] \tag{C.26}$$

Hence:

$$\rho_i = \left[\rho_{min}, \frac{1 - 2\,(K-i-1)\,\rho_{min} - \rho_{min} - 2\sum_{j=1}^{i-1} \rho_j}{2} \right] \quad ; \quad 1 < i < \frac{N+1}{2} \tag{C.27}$$

To comply with equation 2.58, the last normalized sample duration is expressed as follows :

$$\rho_N = 1 - 2 \sum_{i=1}^{\frac{N-1}{2}} \rho_i \tag{C.28}$$