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Bandwidth Enhancement of GaN-Based High-Efficiency Power Amplifiers for Telecommunication Applications

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Dedicated to my beloved parents, my esteemed and cherished family, my friends and all those who have contributed to this project for their continuous support, encouragement and motivation

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List of Abbreviations

0G to 5G	Zero to Fifth Generation
BS	Base Station
BTS	Base Transceiver Station
CDMA	Code Division Multiple Access
CMOS	Complementary Metal Oxide Silicon
dB	Decibel
dBm	Decibel reference to 1milliwatt
DPA	Doherty Power Amplifier
DC	Direct Current
EER	Envelope Elimination and Restoration
FET	Field Effect Transistor
GaN	Gallium Nitride
GSM	Global System for Mobile Communication
GaAs	Gallium Arsenide
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistors
IMN	Input Matching Network
LTE	Long Term Evolution
LDMOS	Laterally Diffused Metal Oxide Silicon
LNA	Low Noise Amplifier
MTS	Mobile Telephone System
MIMO	Multiple Input Multiple Output
MOS	Metal Oxide Silicon

OMN	Output Matching Network
PA	Power Amplifier
PAPR	Peak-to-average Power Ratios
pHEMT	Pseudomorphic Heterojunction Bipolar Transistor
QAM	Quadrature Amplitude Modulation
Q	Quality Factor
RF	Radio Frequency
SC-FDMA	Single Carrier Frequency Division Multiple Access
Si	Silicon
SiC	Silicon Carbide
SiGe	Silicon-Germanium
TDMA	Time Division Multiple Access
MN	Matching Network
OFDM	Orthogonal Frequency Division Multiplexing

General Introduction

Mobile phone communications have become an essential part of our daily lives. Since the emergence of smartphones in 2007, there has been a growing demand for higher data rates and increased network capacity. This has led to extensive research and development efforts in the field of communication standards. By 2018, the groundwork had been laid for the next milestone in mobile communication: the 5G standard. However, the continuous advancement of cellular systems like 5G, as well as future generations, will require even greater transmitter efficiency and cost reduction. Consequently, the architecture of the base transceiver station (BTS) will become more challenging with the introduction of each new standard. Therefore, the deployment of 5G networks is resulting in an expansion of transmission channels and frequency bands managed by mobile telephone operators. To address the escalating costs associated with the proliferation of connection relays, it becomes crucial to design a broadband transmission chain for the RF transmitter used in base stations. By leveraging advanced materials like Gallium Nitride (GaN), it becomes possible to utilize higher frequencies and power levels.

The power amplifier (PA) is an essential component in the base transceiver architecture because of its significant power usage. Additionally, it acts as a limiting factor for the operating frequency of the base station power amplifier. However, this power amplifier operates with complex modulation techniques like Quadrature Amplitude Modulation (QAM), Orthogonal frequency division multiplexing (OFDM), Code division multiple access (CDMA), etc. These modulations result in the creation of highly time-varying envelope communication signals characterized by high peak-to-average power ratios (PAPRs); therefore, to withstand such signals, power amplifiers are required to have high efficiency, not only at saturation but also at a lower output power level. This is not the case for conventional power amplifiers, which can have very high efficiency at their maximum output power but show a sharp efficiency drop with output power back-off.

To increase the back-off efficiency, different power amplifier topologies have been proposed both at the power amplifier and at the system levels, such as the Doherty power amplifier and the Chireix out-phasing power amplifier, which is based on the Load Modulation concept, or Envelope Elimination and Restoration (EER) and Envelope Tracking (ET) techniques, which is based on the supply modulation.

Among all these techniques, the Doherty Power Amplifier gained the highest popularity due to its architectural simplicity in addition to maximizing power efficiency while maintaining relative linearity of PA for high PAPR signals.

Doherty power amplifier offers the advantage of maintaining high efficiency across a wide range of output power levels, but it has a natural limitation in terms of bandwidth. This thesis proposes an improved Doherty amplifier architecture that aims to enhance the performance of RF power amplifiers for mobile wireless communications. Specifically, it focuses on adjusting and optimizing the output networks and phase slope between the main and auxiliary amplifiers to improve the performance of the amplifier's power-added efficiency (PAE), power gain, and output power within a wider bandwidth.

In the first chapter, we discuss the background of cellular communication standards and how it has led to the emergence of 5G. We briefly introduce the architecture of the radio frequency front end in an RF transmitter and the performance metrics of an RF power amplifier. We also provide an overview of the GaN RF power device technology used in this work, as well as other RF power device technologies. Next, we focus on the theory and definition of power amplifier characteristics, specifically the power amplifier classes of operation based on the modification of conduction angle. Finally, we introduced the conventional methodology for designing an RF power amplifier.

In Chapter 2, we discuss and provide an overview of various impedance-matching network topologies used in designing RF power amplifiers. These matching networks play a crucial role in ensuring optimal amplifier performance. We specifically focus on designing single, Pi, T, and dual-section lumped element-based lowpass impedance matching networks. Analytical methods are employed for designing these networks. We determine the fractional bandwidth of these lowpass matching networks and suggest the one with the widest bandwidth as the recommended input and/or output matching network for the GaN-based RF power transistor.

The third chapter focuses on designing the input and output matching networks for a wideband single-stage RF power amplifier. The goal is to improve the matching bandwidth beyond what can be achieved using the analytical method. MATLAB optimization solvers, such as fminunc, fminsearch, and fmincon, are used and compared to determine the optimal values for the lumped elements. Thereafter, the simulated results of the designed GaN-based single-stage class-B RF power amplifier are compared in terms of the optimized six- and four-element lowpass input and output matching network pairs to the single-stage RF power amplifier. Thus, the matching network pairs that produce better PA performance over the desired bandwidth are identified and selected.

In the last chapter, we discuss the theory and simulation study of the frequency behaviour of two Doherty power amplifier techniques: the conventional and the inverted. These amplifiers are evaluated in the frequency range of 2 GHz to 3 GHz using GaN-based transistors. The goal is to compare the bandwidth performance in terms of the voltage standing wave ratio (VSWR) or reflection coefficient, of both

Doherty power amplifier topologies at full and 6 dB backoff power levels. The study demonstrates that it is important to optimize their output networks and also the input phase slope between the main and auxiliary amplifiers, mainly if a more realistic transistor model is used. Then we proposed a design method based on optimization of the values of some key elements to reach maximum bandwidth for the Doherty. Additionally, we compare the harmonic balance simulation results of the complete conventional and inverted Doherty power amplifier circuits in terms of power added efficiency (PAE) and power gain.

Lastly, the general conclusion provides a summary of the entire work presented in this thesis, and prospects for further research are also presented.

Chapter 1: Introduction and Overview

1.1 Introduction

The telecommunications industry has experienced a significant boom in the recent years as a result of the growing demand for communication between people. Modern means of communication are now available to a wide audience, thanks to advances in research and industrialization. However, there is a constant need for research work to improve different performances of telecommunication systems.

In this chapter, we briefly describe history of cellular communication standards from the First generation (1G) to Fifth generation (5G) and then we present the RF front-end architecture, with a focus on the power amplifier. Furthermore, the RF power amplifier performance metrics, RF power device technology and the theory and concept of power amplifier classes of operations are presented. Finally, we conclude the first chapter by presenting the design methodology of RF power amplifier.

1.2 Cellular Telecommunication evolution

Over the last four decades, five generations of cellular networks have emerged, with a new standard emerging every 10 years or so. Since the first deployment of cellular networks, a lot of changes have been introduced in the cellular world. This first part will cover the evolution of mobile communications standards. Figure 1. 1 illustrates the generations of cellular mobile communication, and a brief description of each generation is given as follows:

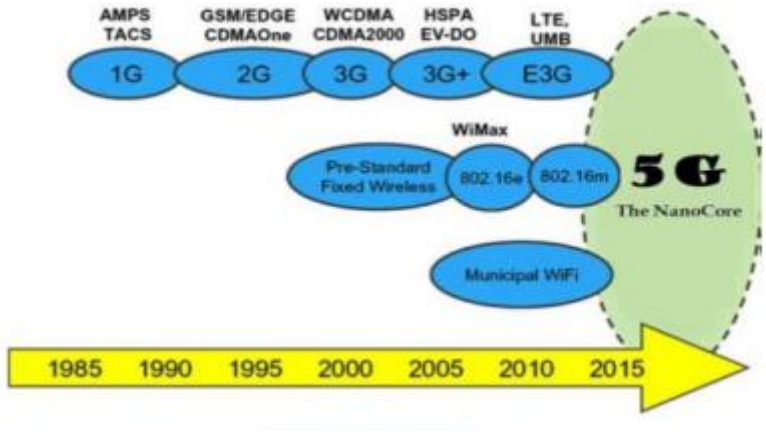


Figure 1. 1: Evolution of cellular communication block diagram [1]

1.2.1 From First Generation (1G) to Fourth Generation (4G)

In the middle of the 20th century, first mobile phone began to appear for some applications but there were only a few channels available and at fixed operating frequency. In 1970, 0G, a precursor to the first generation (1G) cellular system, was introduced. It was a mobile telephony technology known as Radiotelephone that was used in cars before cell phones became popular.

Next to the 0G system, is the First Generation (1G) cellular system, which was the first commercial cellular network launched in the 1980S [1, 2].The cell phones used in the first generation were analog cell phones in which the user has to enable a transmission button and disable reception, making it become a 'press to transmit system'. 1G cellular systems include poor voice links, security issues, low capacity and unreliable handoff.

The deployment of 2G networks started in Europe in the early 1990s and aimed to provide a secure and reliable voice communication channel and allowed some small data-oriented services. The 2G standard implemented the Code division multiple access (CDMA) and GSM concepts.

GSM is the most widely used 2G technique and is dominating the world today [2]. The GSM interface is based on two types of techniques namely TDMA and CDMA [3]. While CDMA assigns each user a unique code to communicate over a multiplex physical channel, TDMA divides the signal into time slots.Because of the GSM standard, international roaming between mobile phone operators became very common, allowing subscribers to use their phones in many parts of the world.Many of the mobile services that we use today were first introduced via 2G networks. Short-Message-Service (SMS), picture messages and MMS were among them. Both the sender and receiver of messages are more secure with 2G systems, and as such, all text messages are digitally encrypted, allowing data to be transferred in a way that only the intended recipient can receive and read it. With "General Packet Radio Service" (GPRS) and Enhanced Data Rates for GSM Evolution" (EDGE), the 2G standard was updated twice to 2.5G and 2.75G enhancing its maximum speed to 171kbps and 384kbps respectively.

In the year 2003, 3G technology was introduced. It employed the "Universal Mobile Telecommunications System (UMTS)" as its primary network architecture. Its main advancement to its predecessor 2G was significantly higher bandwidth. As a result, 3G became the first mobile "multi-media standard". 3G allows the use of internet services such as video streaming or email exchange. Data rates are much higher than with 2G, but still under 2Mbps.

3G technologies allow network operators to provide users with a broader range of more advanced services while achieving greater network capacity through improved spectral efficiency. Wide area

wireless telephony, broadband wireless data, mobile television, and global positioning system (GPS) are among the services available in 3G systems.

The fourth-generation standard was released in the year 2012. Its main goal is to provide high-speed communication with enhanced security to enable high-definition mobile television (TV), video conferencing, and pervasive computing, with a bandwidth of up to 150Mbps. While 4G sets the standard and general conditions, Long Term Evolution (LTE) standards provide the technological foundation to meet these standards. The enhanced LTE+ or LTE Advanced are meeting the 4G standard requirements.

The 4G standard air interface is based on orthogonal frequency division multiple access (OFDMA) for Downlink and single carrier frequency division multiple access (SC-FDMA) for Uplink technology and the use of Multiple input Multiple output (MIMO) systems. To reach ultra-wide bands, 4G uses carrier aggregation (CA), which allows the assignment of two or more frequency blocks to be allocated to one user.

1.2.2 The Fifth-Generation New radio (5G NR)

In 2018 the 3rd Generation Partnership Project (3GPP), a global standardization initiative that aims to harmonize the different cellular networks worldwide presented “phase 1” of the 5G New radio (NR). It has three main objectives, which are to enhance high-speed communication with high capacities and to ensure ultra-reliable low latency communications and massive machine-type communications. More than just higher data rates, the 5G standard also aims for the connection of everything, everywhere. With bandwidths of up to 1Gbps, 5G is designed to ensure low latency communication by making it the perfect communication technology for augmented reality applications, gaming, machine-to-machine communication, and smart devices when quick reaction plays a vital role [3].

Among other evolutions, 5G NR gives access to a new frequency range in the millimeter waves (24 GHz – 100 GHz). 5G NR air interface is based on orthogonal frequency division modulation (OFDM). It is particularly efficient as it allocates dynamically very narrow time and frequency slots to each user.

1.3 Radio Frequency (RF) Front-End Architecture:

The RF front end is key to any wireless system. It consists of electronic circuitry and an antenna to transform electrical signals into electromagnetic waves, which are then transmitted and received through the air.

Figure 1. 2 illustrates the RF front-end system which comprises both the transmitting and receiving paths.

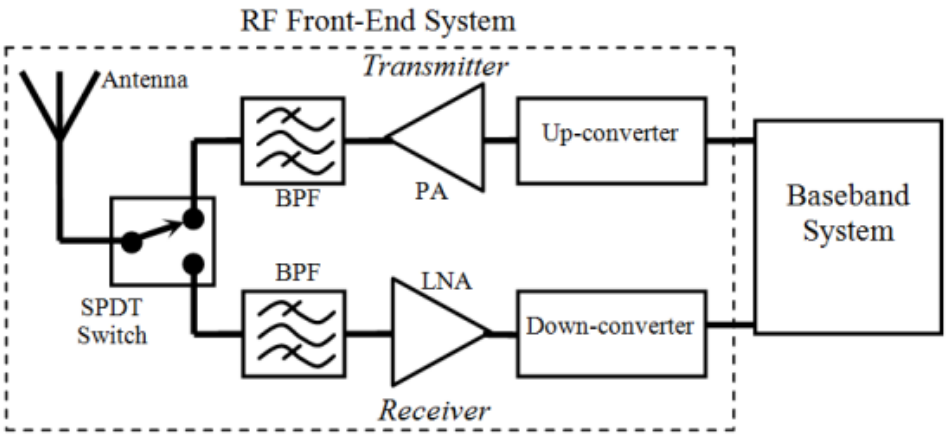


Figure 1. 2: RF front-end system [4]

The Up and Down converters enable transposing the baseband signal to high and low frequencies, respectively, by adjusting the Local Oscillator.

Modern RF transmitters are composed of several sub-circuits which include power amplifiers, oscillators, mixers, filters, and baseband circuitry.

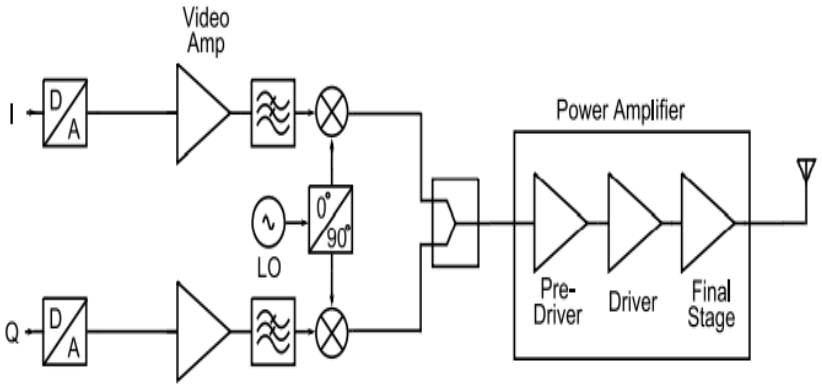


Figure 1. 3: Modern RF transmitter architecture [5]

These Front-End circuits can be implemented using a variety of technologies with the primary purpose of lowering cost, improving power efficiency, and reducing size. Within the transmitter architecture, the power amplifier (PA) is the most critical component and as such accounts for 50% of the overall power consumption, and its performances determine the quality of communication systems. Given this, the work in this thesis is mostly focused on the power amplifier in the RF transmitter block.

1.3.1 RF Power Amplifier performance parameters

The metrics that are usually used to assess the performance of power amplifiers are described in this section. They are:

- Power gain, Output power and 1dB Gain compression point (P1dB)
- Drain Efficiency and Power Added Efficiency

For an easier description of the aforementioned RF power amplifier performance metrics, let's consider the symbolic representation of the flowing in and out of power, as illustrated in Figure 1. 4.

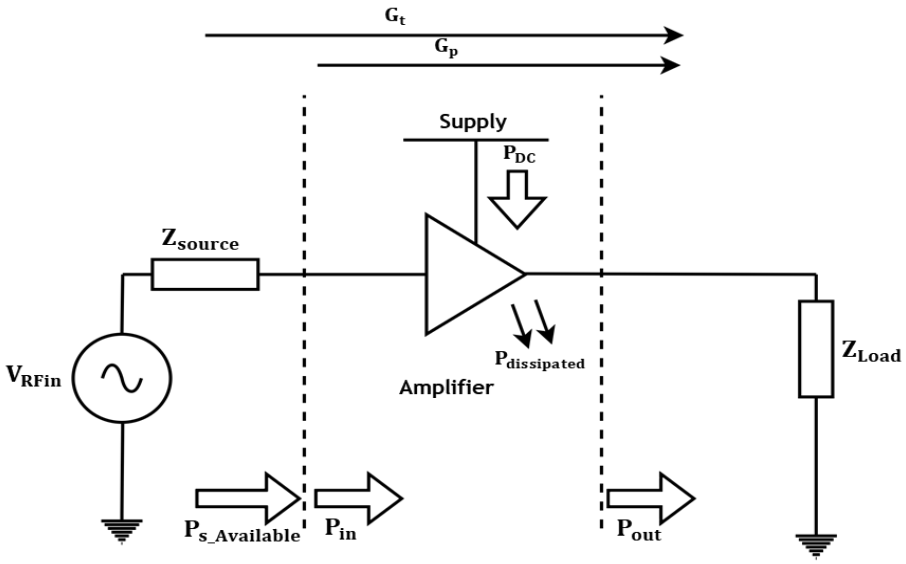


Figure 1. 4: Illustration of flowing-in and out of power (P_{in} and P_{out}) in a power amplifier circuits with source and load impedances

The input AC source of the amplifier with an RF voltage V_{RFin} and a source impedance (Z_{source}) delivers input power to the power amplifier. Thereafter, the amplified output signal is then sent to the load impedance Z_{load}.

From Figure 1. 4, the power gain (G_p) of the amplifier is given by the ratio of the average RF output power (P_{out}) over the average RF input power (P_{in}) , in Watt, as expressed in equation (1.1).

$$G_p = \frac{P_{out,RF}}{P_{in,RF}} \tag{1.1}$$

It is generally expressed in dB as:

$$G_{p\_dB} = 10 \log_{10} \frac{P_{out,RF}}{P_{in,RF}} \tag{1.2}$$

The input or output power can also be expressed in dBm as:

$$P_{dBm} = 10.\log_{10}.(\frac{P_{Watt}}{10^{-3}}) \tag{1.3}$$

The ratio of the output power to the available power from the source is known as the transducer gain of the amplifier.

$$G_t = \frac{P_{out,RF}}{P_{S\_available}} \tag{1.4}$$

The source impedance must be matched to the conjugate of the input impedance to the amplifier to guarantee maximum transfer of power from the source to the load. As a result of this, the input power P_{in} to the amplifier becomes equal to the power available at the source ($P_{S\_available}$). Additionally, the transducer gain (G_t) also becomes equal to the power gain (G_p) of the amplifier.

Gain compression is one of the methods of quantifying the non-linearity of an amplifier. It is therefore a measure of the linear handling capability of an amplifier. The RF power amplifiers are mainly characterised based on their 1dB compression point (P1dB) and are referred to as the signal power at which the gain of an amplifier is 1dB lower than the ideal linear gain [6] as shown in Figure 1. 5. Furthermore, the compression point can also be expressed in terms of output power 1dB compression point (OP1dB) or the input power 1dB compression point (IP1dB).

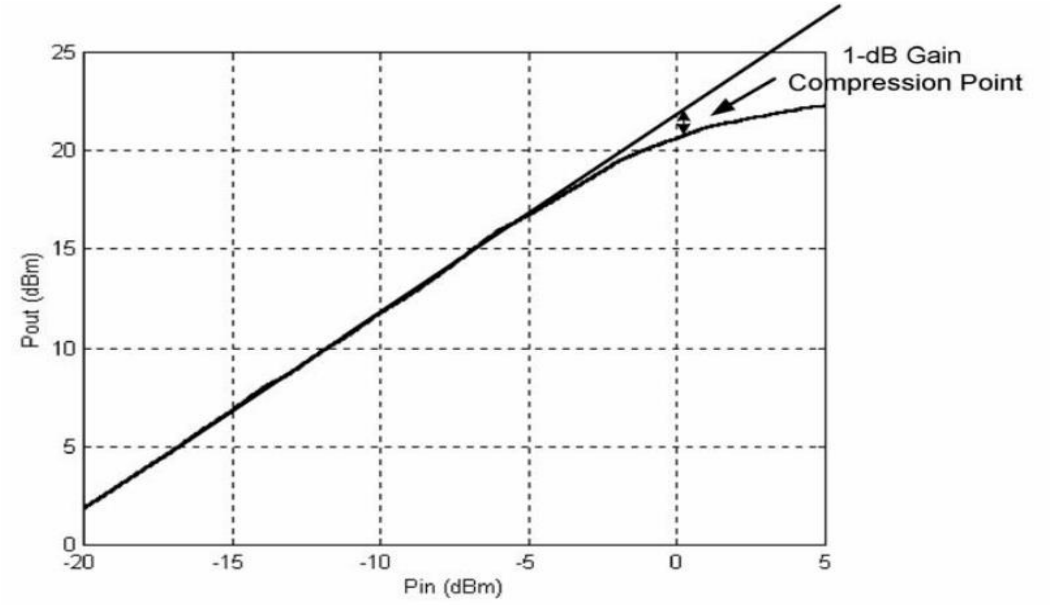


Figure 1. 5: Output power versus Input power showing the1dB compression point [7].

The efficiency of an amplifier is determined by a measure of DC power (P_{DC}) conversion to the RF power. However, due to the power dissipation ($P_{dissipated}$) exhibited by the amplifier, only a portion of the DC power is converted to the RF power during the amplification process. Hence, two different expressions for a power amplifier's efficiency exist. The first is the drain efficiency (D.E) usually expressed in percentages, quantifies the extent to which the power amplifier converts DC power to RF output power. It is mathematically given as:

$$D.E = \frac{P_{out,RF}}{P_{DC}} \tag{1.5}$$

The second expression of the power amplifier efficiency is the Power Added Efficiency (PAE) also expressed in percentage takes into account the input power to the amplifier as given in equation (1.6).

$$PAE = \frac{P_{out,RF} - P_{in,RF}}{P_{DC}} = D.E * (1 - \frac{1}{G_p}) \tag{1.6}$$

As observed from equation (1.6), the PAE can also be written as a function of D.E and G_p. Consequently, as the power gain increases to a higher value, the Power Added Efficiency becomes closer to the drain efficiency. In this work, PAE is considered as the measure of performance of power amplifier efficiency.

1.4 RF Power Device Technology

1.4.1 Transistor technologies

The travelling wave tubes (TWT) are utilized in satellite communications due to its large power requirements at high frequencies, solid-state power amplifiers on the other hand are key solutions in almost all modern low-to-medium RF power applications. The frequency and the desired output power level are the main performance parameter to consider when determining the choice of the RF power device to be used.

Due to the tremendous investments made by the integrated circuit (IC) industry, silicon-based transistors appear to be the cheapest materials used in the RF field. Three different types of silicon-based transistors are briefly described as follows:

- Complementary Metal Oxide Silicon Field Effect Transistor (CMOS-FET)

Most integrated circuits (IC) are based on CMOS transistors because, it is a low-cost technology allowing high component-density applications. CMOS development is limited to low power application due to its breakdown voltage limits, as illustrated on Fig. 1.6, but the CMOS technologies allows for the integration of the power structure and control/intelligence circuits on the same die, thereby decreasing the complexity of more advanced systems.

- Laterally diffused metal oxide silicon Field Effect Transistor (LDMOS-FET) technology is a Motorola-invented technology. LDMOS has been the default choice for any high-power PA application below some GHz and this has led to the annihilation of the RF-power Si bipolar industry except for a few small pockets that still manufacture such devices for specific applications [8,9,10].

This technology is mostly used as a power device for example in LTE macro base stations. Although it is limited to some GHz frequency bands, it can generate several hundred watts of power at a lower cost.

- Silicon-Germanium Heterojunction Bipolar Transistor (SiGe-HBT)

The performance of SiGe technology in terms of efficiency or linearity is better than that of CMOS but only confined to low-power and high-frequency applications.
Silicon-based transistors are cheap but have lower performances in terms of efficiency, noise, and output power compared to Gallium Arsenide or Gallium Nitride in many RF applications.

- Gallium Arsenide (GaAs) Technology

GaAs is expensive than Si but quickly took over the microwave world at a design frequency of above 2GHz. This initially occurred in the low noise receiving applications. High-power GaAs to the tune of tens of watts became available despite some serious material and reliability issues which took one or two decades to resolve.

GaAs transistors present a higher performance than silicon-based transistors in terms of electrical velocity, breakdown voltage or thermal conductivity . Gallium Arsenide technology has been used in the form of a bipolar device, known as the Heterojunction Bipolar Transistor (HBT). It has been a default technology for low-power mobile handset PAs because the transistor requires only a single supply voltage and can be completely turned off. Furthermore, other developed structure of this technology is GaAs Pseudomorphic High Electron Mobility Transistors (pHEMT). They are used for low to medium-power applications and also aided the evolution of cellular-based telecommunications in the last two decades.

- Silicon Carbide (SiC) and Gallium Nitride (GaN) for very high power

Recent development in RF technology for high power led to the emergence of high bandgap semiconductors. Even though Silicon Carbide (Sic) has been the most popular choice device technology, it has now been overtaken by Gallium Nitride (GaN) with effect from the year 2000. The high breakdown voltage of GaN greatly increases the maximum output power, and by combining GaN with the thermal conductivity of Sic, GaN on Sic-HEMT will certainly translate into a perfect candidate for achieving both high power and high efficiency. As the power requirement of modern mobile communication standards like 5G is increasing, GaN is becoming attractive for power amplifier used in base transceiver station (BTS).

Figure 1. 6 below illustrates the transistor technologies and their applications.

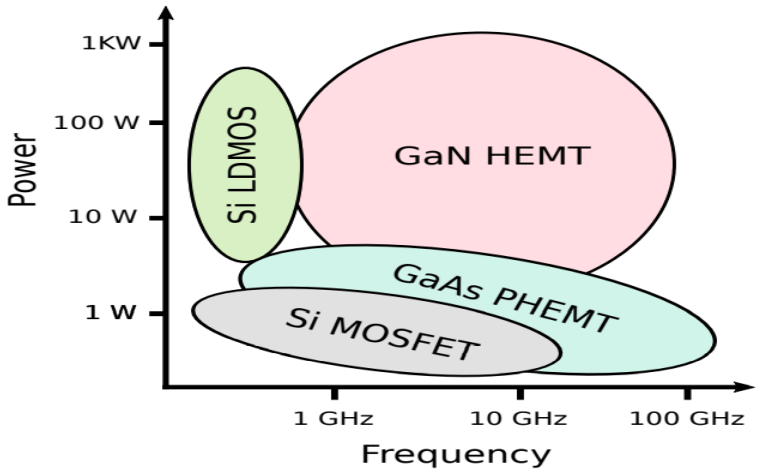


Figure 1. 6: Transistors technologies and their applications [11]

Table 1. 1 compares some of the properties of the main semiconductor materials used in RF designs.

Table 1. 1: Comparison of the main RF semiconductor materials [11]

Material Property	Silicon	SIC	GaAs	GaN
Band Gap (eV)	1.12	2.86	1.42	3.39
Breakdown Field (kV/cm^2)	300	2000	400	2000
Saturation Electrical Velocity (cm/s)	9E6	2E7	1.3E7	2.3E7
Electron mobility (cm^2/ (V.s))	1450	500	8500	800
Thermal conductivity (W/ (cm.C))	1.45	3.5	0.46	1.3

1.4.2 General Ideal Transistor model

Different transistor models are available for the design of Power Amplifiers but their architectures are quite similar. Thus, the Field Effect Transistor (FET) model is used in characterising the behaviour of transistors in this thesis. Figure 1. 7 shows the Ideal Field effect transistor.

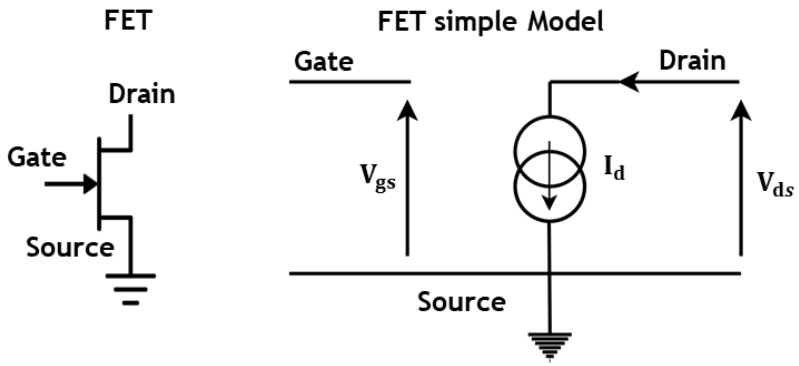


Figure 1. 7: The basic form of modelling the fundamental operation of Field Effect Transistor

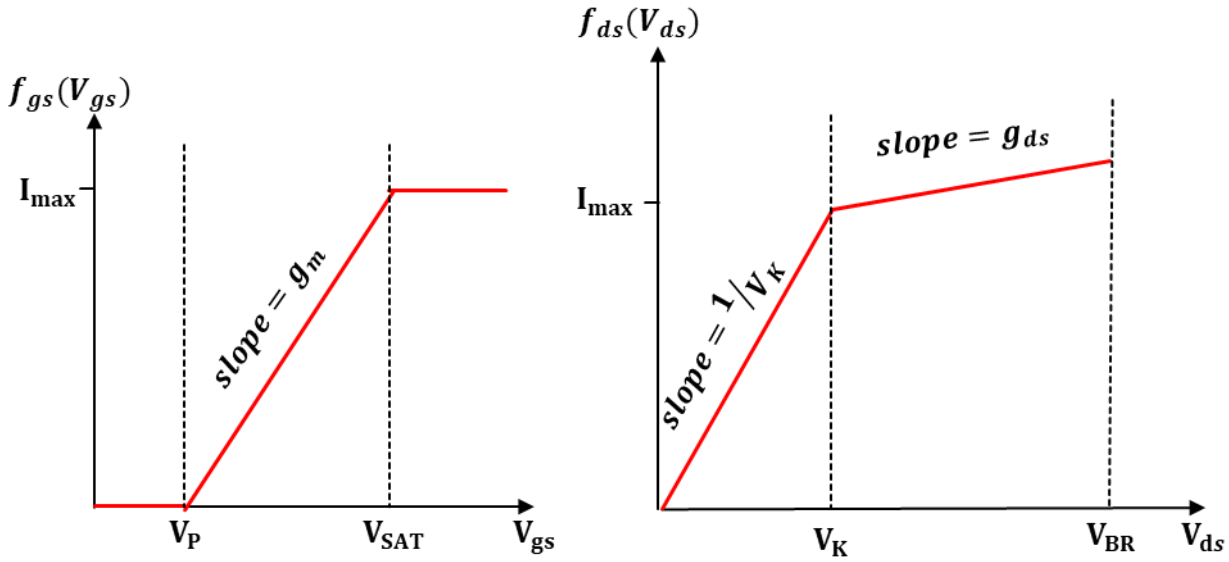
The Field effect transistor is a voltage-controlled current source device with an output current I_{ds} that is determined by the gate-to-source and drain-to-source voltages. The piece-wise linear expression given in equations (1.7) can be used to characterised the drain current I_{ds} as a separable function of the gate voltage V_{gs} and the drain voltage V_{ds} [12].

$$I_{ds} = F(V_{ds}, V_{gs}) = F_{ds}(V_{ds}) \, . \, F_{gs}(V_{gs}) \tag{1.7}$$

Figure 1. 8 illustrates the general relationships between the drain current I_{ds} and the two voltages (gate and drain voltage). Subsequently, the two separable functions of equation (1.7) are described by the following expressions :

$$F_{Vgs}(V_{gs}) = \begin{cases} 0, if\ V_{gs} < V_P \\ g_{m(V_{GS}-V_P)}, \quad if\ V_P \leq V_{gs} \leq V_{SAT} \\ I_{max}, \quad if\ V_{SAT} < V_{gs} \end{cases} \tag{1.8}$$

$$F_{Vds}(V_{ds}) = \begin{cases} \dfrac{V_{ds}}{V_K}, if\ 0 < V_{ds} < V_K \\ 1 + \dfrac{g_{ds}(V_{dS} - V_K)}{I_{max}}, if\ V_K < V_{ds} < V_{BR} \end{cases} \tag{1.9}$$



(a) (b)

Figure 1. 8: The two separated functions $F_{GS}\ VS\ V_{gs}$ (left) and $F_{ds}\ VS\ V_{ds}$ (right)

As shown in Figure 1.8a, the pinchoff voltage V_P which is the minimum gate voltage required to turn on the transistor and the saturation voltage V_{SAT} are the parameters that define the function (F_{GS}). The V_{SAT}

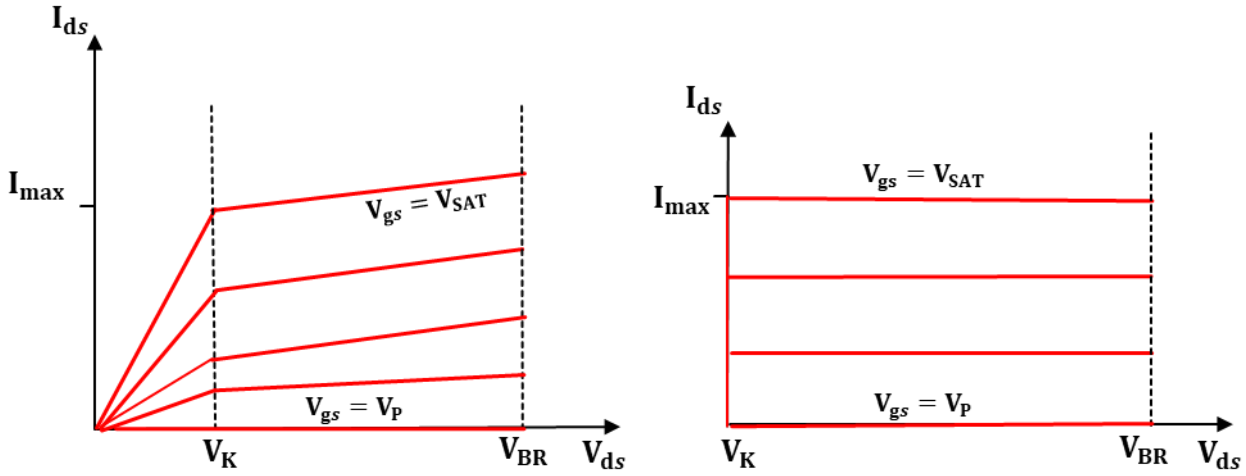
voltage is the voltage at which the transistor current is maximum. The maximum transistor current is expressed as :

$$I_{max} = g_m.(V_{SAT} - V_P) \tag{1.10}$$

Consequently, when V_{gs} value becomes greater than the V_P, the drain current increases and the transconductance g_m is taken as the slope of the F_{GS} in the region between the V_P and V_{SAT}.

The function F_{ds} shown in Figure 1.8b is given at $V_{gs} = V_{SAT}$ and allows to introduce the breakdown voltage V_{BR} and the knee voltage V_K. The transistor acts like a resistor when V_{ds} is less than the knee voltage, V_K . This, therefore, implies that the transistor is in the ohmic region of the I-V curve . For the case when V_{ds} is greater than the knee voltage V_K, the slope of the F_{ds} function is given by the output conductance g_{ds}. Thus, the current is less dependent on V_{ds} and the transistor nearly functions as an ideal current source controlled by V_{gs} in this region. A V_{ds} voltage greater than the maximum drain voltage (V_{BR}) of the transistor, may cause damage to the device. For the transistor to behave as an ideal current source that solely depends on gate voltage V_{gs}, both the knee voltage V_K and output conductance g_{ds} are set to zero for simplicity's sake.

Figure 1.9a shows the DC characteristics or I-V curves for the non-zero value of knee voltage and output conductance, while the ideal DC curve for the case when both the knee voltage and output transconductance are zero is illustrated in Figure 1.9b.



(a) (b)

Figure 1. 9: FET I-V curves with:

(a) The non-zero value of Knee voltage and output conductance

(b) The ideal voltage-controlled current source model where $g_{ds} = 0$ and $V_K = 0$

The ideal transistor model case described above does not fully reflect the complex behaviour of a real transistor, but it is however realistic enough to serve as the foundation for the development theory underlying the power amplifier architectures and modes of operation [13]. Hence, a large signal power amplifier cannot be designed with this simple transistor model.

1.4.2.1 A general nonlinear model of the FET-based Transistor

Figure 1. 10 represents the general topology of the nonlinear large-signal model for the metal-semiconductor field effect transistors (MESFETs), MOS or LDMOS transistors, and the high electron mobility transistors (HEMTs).

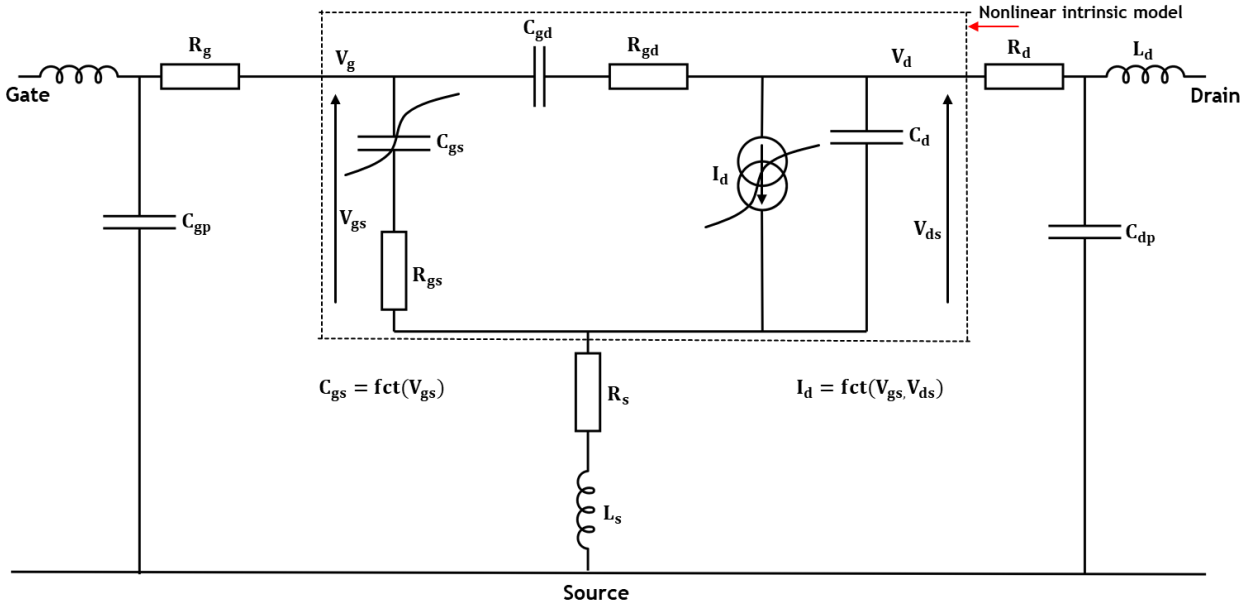


Figure 1. 10: Large signal equivalent circuit of field effect transistor

The extrinsic part of the nonlinear model of Figure 1. 10 represents the accesses to the active part of the transistor and is comprised of the following lump components [14, 15, 16] associated to gate, drain and source terminals: the lead inductances (L_g, L_d *and* L_S), the pad capacitances (C_{gp} *and* C_{dp}), and the ohmic and bulk resistances (R_g, R_d *and* R_S). Similarly, the intrinsic part of the nonlinear model is described by the channel resistances R_{gs} and R_{gd}, the nonlinear drain current source I_d, the gate-source capacitance C_{gs}, the feedback gate-drain capacitance C_{gd}, and the drain-source capacitance C_d.The capacitances (C_{gs} *and* C_{gd}) are considered as the nonlinear functions of the transistor model and represent its charge depletion region.

1.4.3 Operating principle of Power amplifier

The primary purpose of the RF power amplifier is to increase the power of the RF input signal as they propagate through coaxial cables or radio waves so that the receiver can interpret them appropriately.

Solid state conventional power amplifier is generally based on a common source (CS) configuration of a field effect transistor (FET) as illustrated in Figure 1. 11.

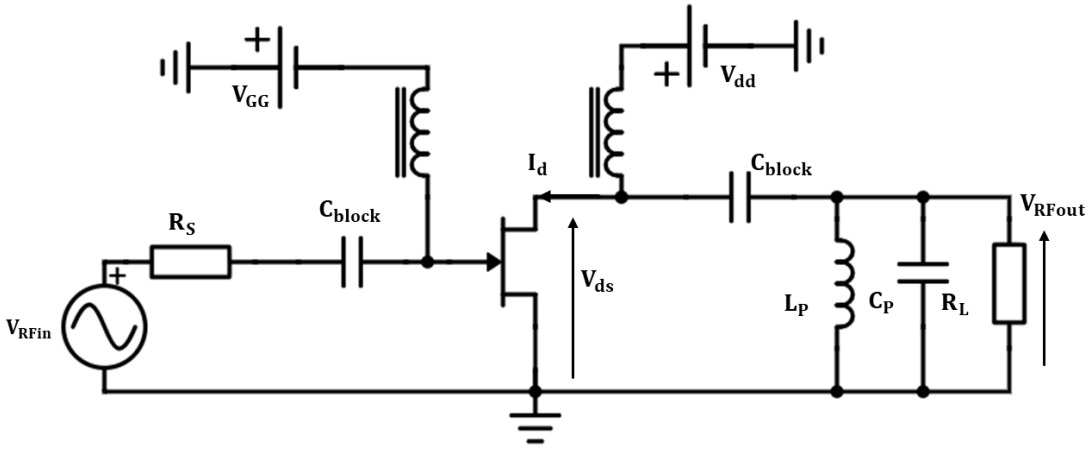


Figure 1. 11: Ideal Current Source Transistor PA

Generally, PAs are categorised into two groups based on their mode of operation. First, is the PA group that operates on the principle of conduction angle (θ) modification, while the second group is the switching PAs.

The first group consist of class A, AB, B and C power amplifiers while the second group is comprised of class D, E and F PAs. However, only the first group is described in this section.

Thus, the conduction angle (θ) of the first group of power amplifiers is referred to as the portion of the RF cycle in which the amplifiers are conducting current in response to the input signal. It is measured in degrees or radians. The idealized I-V curve using a FET-based transistor is used to illustrate the operations of class A, AB, B and C amplifiers.

Therefore, a FET-based amplifier is said to be a current source amplifier used in saturation and cutoff regions and is linearly controlled by the gate voltage up to the maximum current I_{max}. The characteristics of these amplifiers are described by considering the purely sinusoidal drain-source voltage, filtered by the parallel LC circuit, centred at the bias voltage (V_{dd}).

1.4.3.1 Class A power amplifier

A class A power amplifier is one in which the transistor conducts current for the full 360 degrees of the input cycle [12]. In analog design, the term class A amplifier is often used interchangeably with the term linear amplifier.

Figure 1. 12 shows the ideal curve characteristics for class A amplifiers relating the drain current (I_{ds}) to the gate and drain voltages. Furthermore, the output drain voltage and current waveforms plotted against conduction angle $\theta = \omega_0 . t$ are also presented.

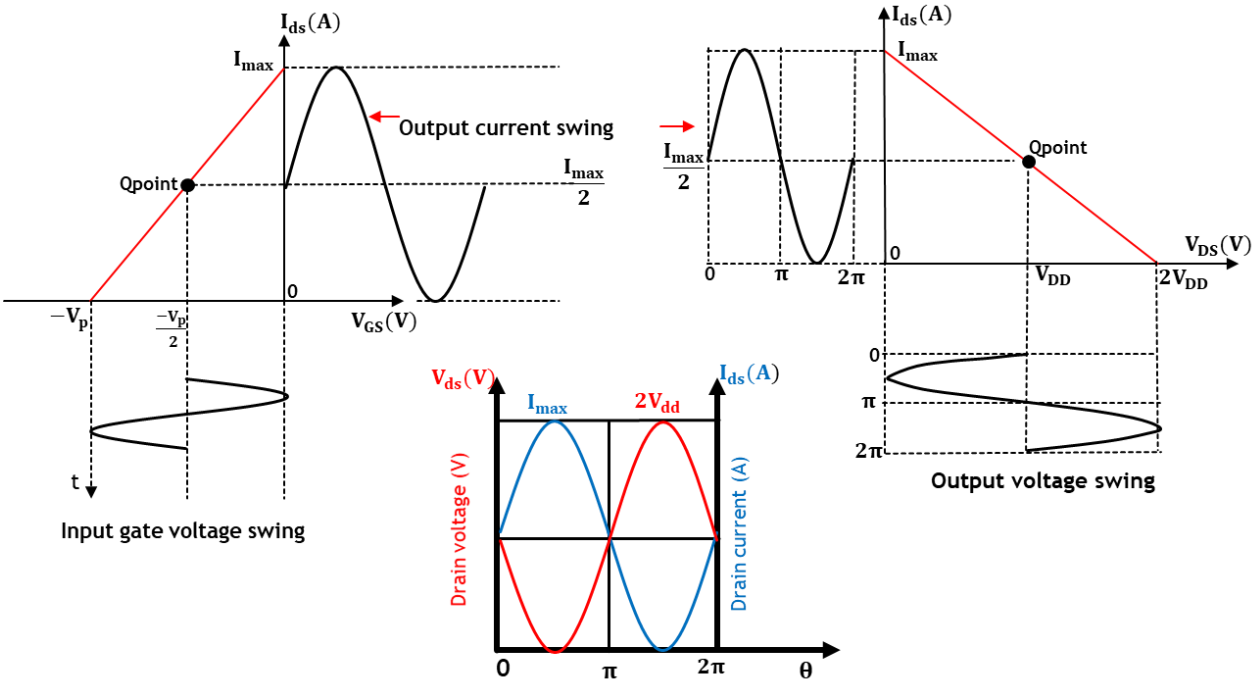


Figure 1. 12: I-V characteristics curve with the drain voltage and current waveforms at maximum input drive for class A amplifier

The transistor current and voltage waveforms for the class A amplifier are shown in Figure 1. 12 for maximum excursion, leading to maximum power. The variation of the conduction angle for the fundamental drain current is obtained by simply adjusting the gate voltage from a reference point called pinchoff voltage $(-V_p)$. The fundamental drain current waveform for the class A amplifier conducts current in the whole RF cycle. As such the amplifier DC drain current will always conduct current even when there is no RF swing thereby leading to a higher DC power consumption which in turn limits the efficiency of the class A amplifier at power backoff.

The maximum output power and theoretical efficiency for a class A power amplifier can be achieved when:

- the drain current swings from 0 to maximum current I_{max}. This require a bias current I_{dd}= Im_{ax}/2 and a gate voltage value $V_{GSA} = \frac{-V_p}{2}$.
- the drain voltage swing is maximum from Vdmin to Vdmax. Vdmin is the lower limit of the saturation area, in an ideal case it is considered null. Vdmax is the maximum drain voltage before breakdowm. For an ideal case, the voltage swing from 0 to $2V_{dd}$ as observed in Figure 1. 12.

To reach maximum drain voltage, the optimum load resistance presented to the drain of the current source must be real. It's value is given by the ratio of the maximum fundamental RF drain voltage V_{d1} to the maximum drain current I_{d1} at an operating frequency of Fo.

$$R_{Lopt} = \frac{V_{d1\_max}}{I_{d1\_max}} \tag{1.11}$$

The corresponding optimum resistance in this case is given by the following formula:

$$R_{Lopt,A} = \frac{V_{d1\_max}}{\frac{I_{max}}{2}} = \frac{2.V_{dd}}{I_{max}} \tag{1.12}$$

The equations for the DC power supply and output power for the class A power amplifier, with the DC drain current at bias point $I_{d0} = \frac{I_{max}}{2}$, are given as:

$$P_{dc} = V_{dd}.I_{d0} = V_{dd}.\frac{I_{max}}{2} \tag{1.13}$$

The output power at fundamental frequency, considering a real load resistance is given by:

$$P_{out,RF} = \frac{1}{2}.V_{d1}.I_{d1} \tag{1.14}$$

The maximum output power at the maximum excursion of drain current and voltage is then:

$$P_{out,RF} = \frac{1}{2}.V_{d1\_max}.I_{d1\_max} = \frac{1}{2}.V_{dd}.\frac{I_{max}}{2} \tag{1.15}$$

Subsequently, the maximum drain efficiency is given as the ratio of RF maximum output power to the DC power supply as defined by equation (1.16):

$$D.E = \frac{1}{2} = 50\% \tag{1.16}$$

Hence, the class A amplifier provides a linear output with the lowest distortion and limited efficiency level.

1.4.3.2 Class B power amplifier

The power efficiency of an amplifier can be improved by biasing the gate of the transistor at the pinchoff point $(-V_p)$ on the I-V curve shown in Figure 1. 13, such that it conducts current for one-half of the RF cycle. The outcome of this operation resulted in class B amplifier, which has a conduction angle of 180 degrees. When no input signal is applied, the transistor is turned off and the Quiescent drain current is zero, meaning no current flows through the amplifier. The drain current is assumed to be a half-rectified sine wave. Even though the output drain current will have a significant spectral content at harmonic frequencies, the tank circuit loading the amplifier will reduce the harmonics on the drain voltage to an acceptable level, or cancel the harmonics in an ideal case to achieve a sinusoidal drain voltage.

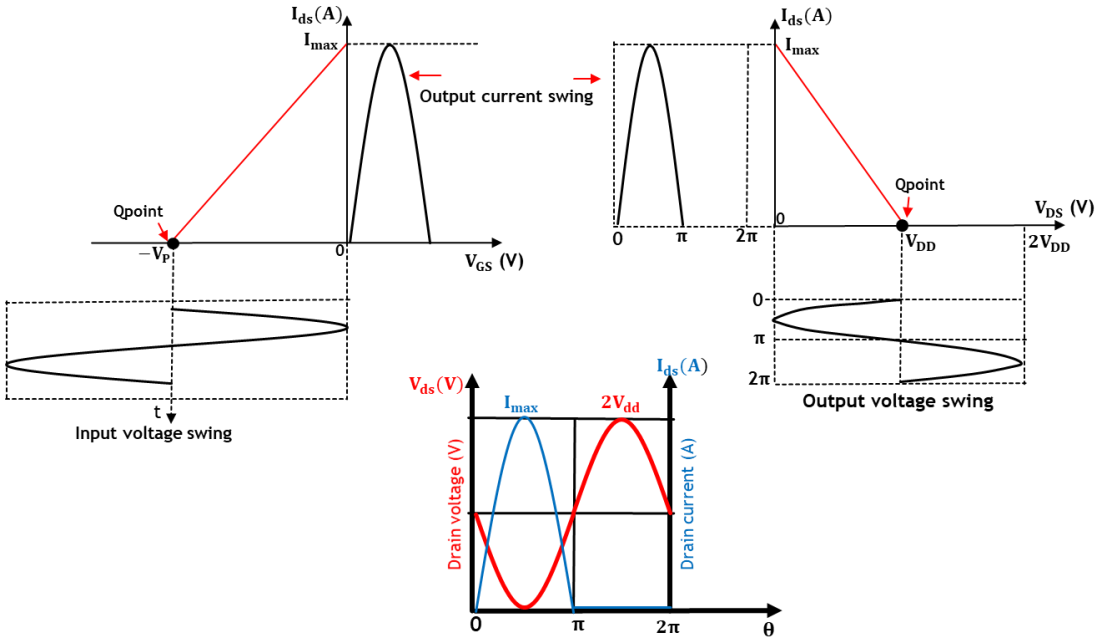


Figure 1. 13: I-V characteristics curve with the drain voltage and current waveforms at maximum input drive for class B amplifier

The drain current (I_{ds}) in the class B amplifier is a half sine-wave and can be represented as a Fourier-series , while the DC component of the drain current is given by:

$$I_{d0-B} = \frac{1}{2\pi}\int_0^{\pi} I_{max}\,.\sin(\omega_0 t)\,d(\omega_0 t) = \frac{I_{max}}{\pi} \tag{1.17}$$

And the fundamental component of the drain current can be obtained by [12]:

$$I_{d1} = \frac{1}{\pi}\int_0^{\pi} I_{max}\sin^2(\omega_0 t)\,d(\omega_0 t) = \frac{I_{max}}{2} \tag{1.18}$$

From the Fourier series expansion, we can see that the current at the fundamental frequency is the same as in class A. So, the optimum load R_{Lopt} and the maximum output power equation for a class B power amplifier are the same as that of a class A power amplifier.

$$R_{Lopt\_B} = R_{Lopt\_A} \; and \; P_{out\_B} = P_{out\_A} \tag{1.19}$$

The DC supply power for the class B amplifier is given by :

$$P_{DC\_B} = I_{d0-B} \cdot V_{dd} = \frac{I_{max}}{\pi} . V_{dd} \tag{1.20}$$

The maximum drain efficiency for the class B amplifier is given by:

$$D.E = \frac{\frac{1}{2} . \frac{I_{max}}{2} . V_{dd}}{\frac{I_{max}}{\pi} . V_{dd}} = \frac{\pi}{4} = 78.5\% \tag{1.21}$$

1.4.3.3 Class A-B Power Amplifier

The efficiency and linearity of the class AB amplifier are a compromise between the class A and class B amplifiers. To strike a balance between having good linearity and high efficiency, the class AB active device should operate with a conduction angle greater than 180 degrees of class B, by biasing the gate of the transistor somewhere between the pinchoff point and the class A gate bias point. The efficiency of class AB amplifiers also lies between 50% of class A and 78.5% of class B amplifiers. Figure 1. 14 illustrates the I-V curve with the output current and voltage waveforms for the class AB amplifier.

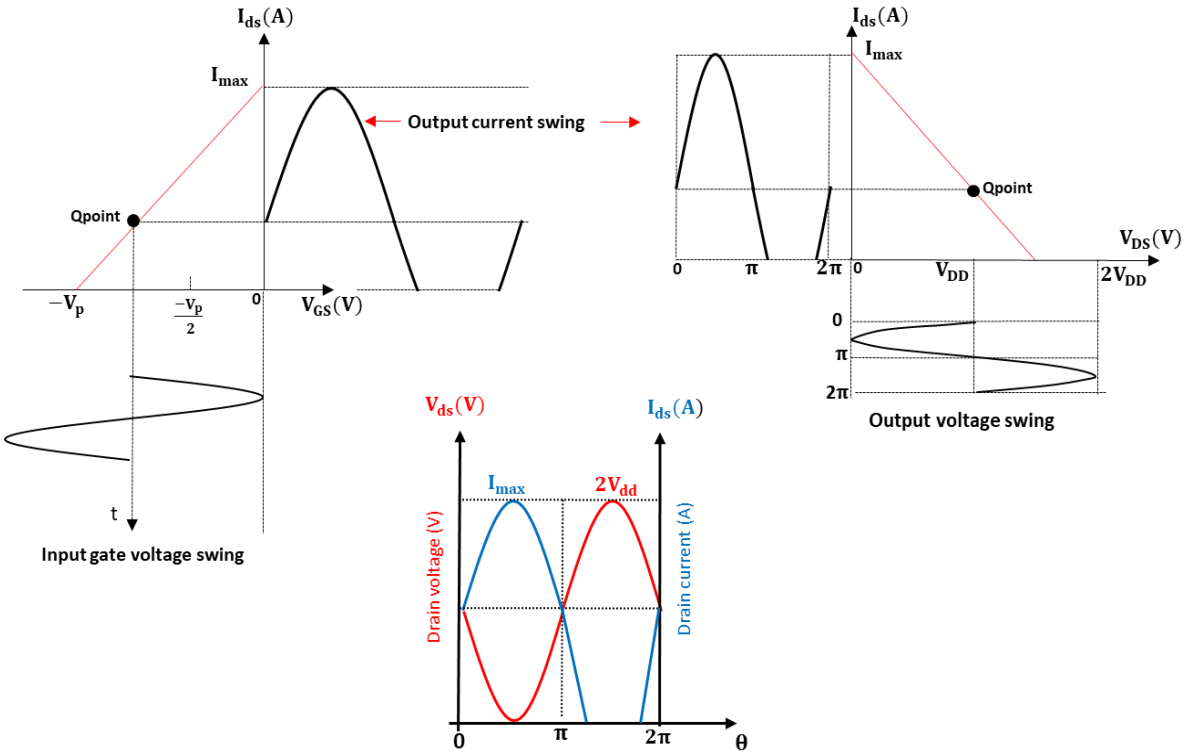


Figure 1. 14: I-V characteristics curve with the drain voltage and current waveforms at maximum input drive for class AB amplifier

1.4.3.4 Class C- Power Amplifier

The gate of the transistor for the class C amplifier case is biased at a gate voltage value below the pinchoff point such that it only conducts current for less than half of the RF input cycle (<180°) to achieve higher efficiency than class A, B and AB amplifiers. Figure 1. 15 shows the I-V curve characteristics with the output drain current and voltage waveforms for the class C amplifier. The output voltage waveform for the class C amplifier is still the same as that of class A, B and AB amplifiers, while the drain output current waveform conduction angle lies between 0 and 180°. Hence, the efficiency of the class C amplifier can be improved from the class B (78.5%) efficiency to about 100% by reducing its conduction angle between 0 and 180°, this will however be at the expense of good linearity with the class C amplifier becoming more non-linear than the class A, B or AB amplifier.

The class C amplifier is mostly used in applications with constant envelope modulation signals [11] or pulsed signal.

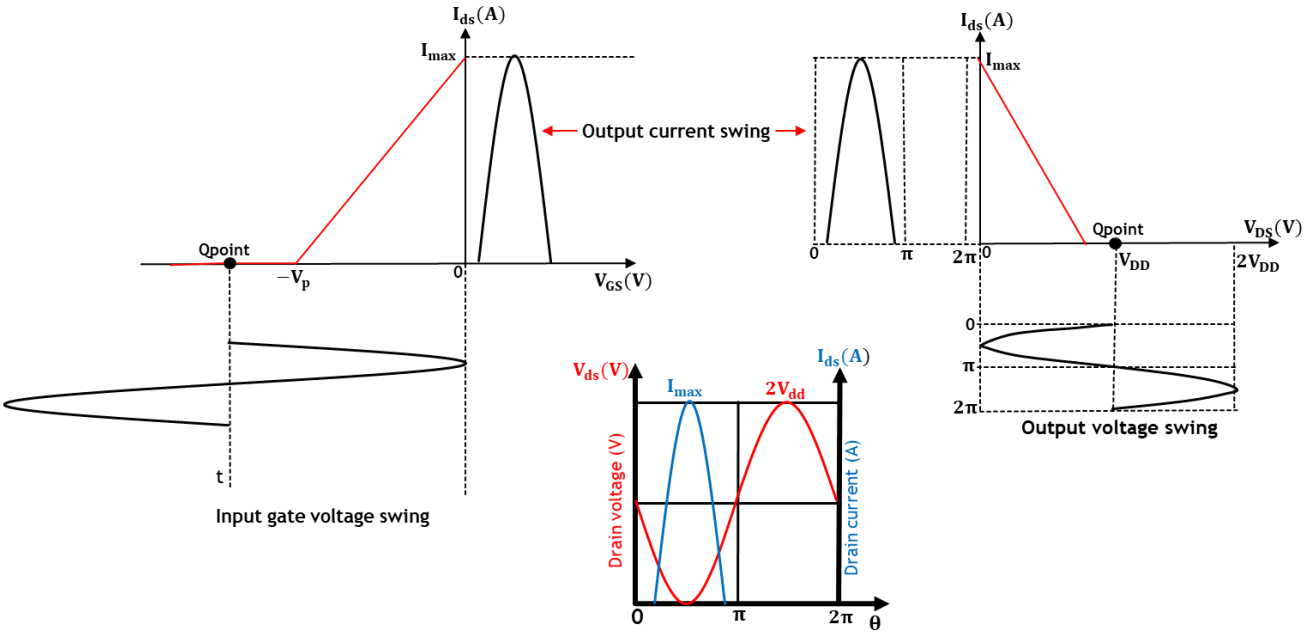


Figure 1. 15: I-V characteristics curve with the drain voltage and current waveforms at maximum input drive for class C amplifier

1.4.3.5 Review of classes A to C power amplifier operating principles

Table 1. 2 gives the summary of the class A, B, AB and C power amplifiers' characteristics according to their operating points (Qpoints), conduction angles and gate biasing voltage.

Table 1. 2: Comparison of the characteristics of Power amplifier classes

Class of Amplifier	Biased gate voltage (V_{GS})	Quiescent drain current I_{DQ}	Conduction angle (θ)
A	$\frac{-V_p}{2}$	$\frac{I_{max}}{2}$	360°
B	$-V_p$	0	180°
AB	between class A pinchoff point to $-V_p$	$(0, \frac{I_{max}}{2})$	(180°, 360°)
C	$< -V_p$	0	(0°, 180°)

The DC and fundamental drain components of the power amplifier's drain currents can be calculated by Fourier series analysis as a function of the conduction angle. The results are given by the following equations [13]:

$$I_{d0} = \frac{I_{max}\left(\sin\frac{\theta}{2} - \frac{\theta}{2}\cos\frac{\theta}{2}\right)}{\pi\left(1 - \cos\frac{\theta}{2}\right)} \tag{1.22}$$

$$I_{d1} = \frac{I_{max}(\theta - \sin\theta)}{2\pi\left(1 - \cos\frac{\theta}{2}\right)} \tag{1.23}$$

Equations (1.22) and (1.23) can further be written as :

$$\frac{I_{d0}}{I_{max}} = \frac{\left(\sin\frac{\theta}{2} - \frac{\theta}{2}\cos\frac{\theta}{2}\right)}{\pi\left(1 - \cos\frac{\theta}{2}\right)} \tag{1.24}$$

$$\frac{I_{d1}}{I_{max}} = \frac{(\theta - \sin\theta)}{2\pi\left(1 - \cos\frac{\theta}{2}\right)} \tag{1.25}$$

Because in the ideal case the maximum magnitude of the drain voltage at fundamental (V_{d1_max}) is equal to the bias voltage V_{dd}, the theoretical maximum drain efficiency of the amplifiers as a function of the conduction angle is given by half of the ratio of the fundamental drain current to the DC drain current of equations (1.22) and (1.23), and is written as :

$$Drain\ Efficiency\ (D.E) = \frac{1}{2}.\frac{I_{d1}}{I_{d0}} = \frac{(\theta - \sin\theta)}{4\left(\sin\frac{\theta}{2} - \frac{\theta}{2}\cos\frac{\theta}{2}\right)} \tag{1.26}$$

The plot of the DC and fundamental drain currents amplitude normalized to ($I_{max} = 1$) of equations (1.24) and (1.25) as well as the maximum drain efficiency of equation (1.26) against conduction angle (θ) is illustrated in Figure 1. 16.

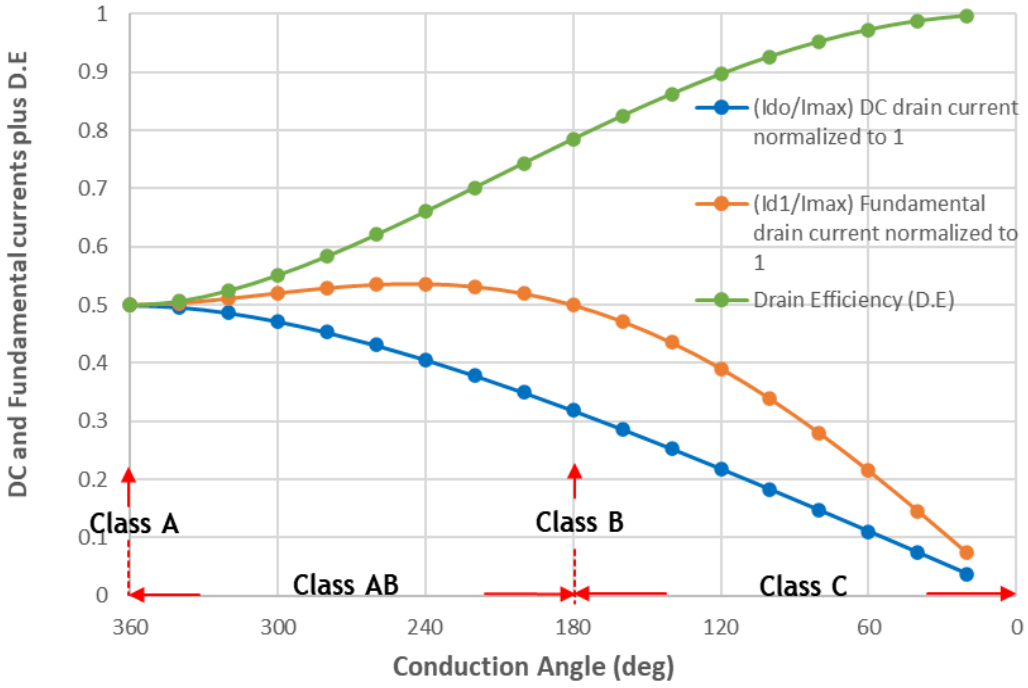


Figure 1. 16: Normalized DC and fundamental drain currents as well as the maximum achievable drain efficiency against conduction angle for different power amplifier classes.

It can be seen from Figure 1. 16 that the DC component of the drain current decreases with a decrease in conduction angle, while the magnitude of the fundamental part of the drain current for the class AB amplifier is higher than that of the class A amplifier. Moreover, the magnitude of the fundamental drain current for the class A amplifier is the same as that of class B and the DC drain current of the class B amplifier is lower than that of the class A amplifier.

The maximum achievable efficiency of the class B amplifier is higher than that of the class A. The drain efficiency of the class C amplifier can be increased towards unity (100%) by decreasing the conduction angle, but in this case, I_{d1} and the output power fall to low values.

1.5 RF power amplifier design methodology

We can now go ahead to design and simulate a high-efficiency power amplifier. The first step in the design of an RF power amplifier is to choose a suitable transistor technology. This is then followed by determining the transistor's biasing point using the ADS simulation software to generate I-V

characteristics and to calculate the design parameters of the power amplifier. And lastly, the simulated results of the designed RF power amplifier are presented and analysed.

1.5.1 GaN Transistor Model

The GaN HEMT transistor is selected as a power device for power amplifier design because it has high power density and voltage operation value than the GaAs-based transistor. Figure 1. 17 illustrates the active part model to be used in the design of the RF power amplifier. A total gate width of 3mm is required to achieved an output power around 25 Watt.

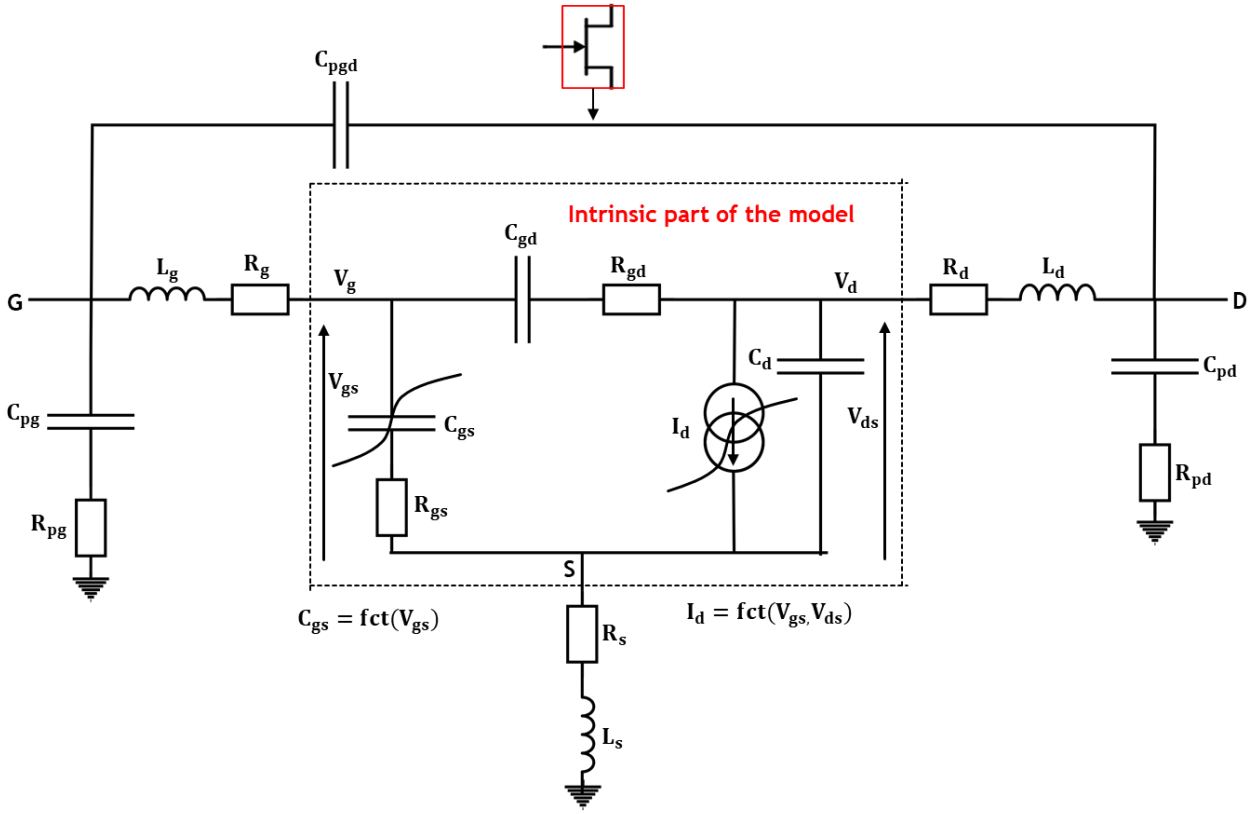


Figure 1. 17: GaN transistor model

As shown in Figure 1. 17, the transistor model is closed to the one presented in Figure 1. 10, with only some difference on the access elements of the extrinsic part.

1.5.1.1 Drain current source and estimation of the optimum load

The next step is to use the transfer characteristic of the transistor to establish the maximum drain current (I_{max}), drain voltage swing (V_{ds}), gate voltage swing (V_{Gs}) and the fundamental load resistance (R_{opt}) obtained from the simulated I-V plot of the GaN transistor. The resulting I-V plots are shown in Figure 1. 18.

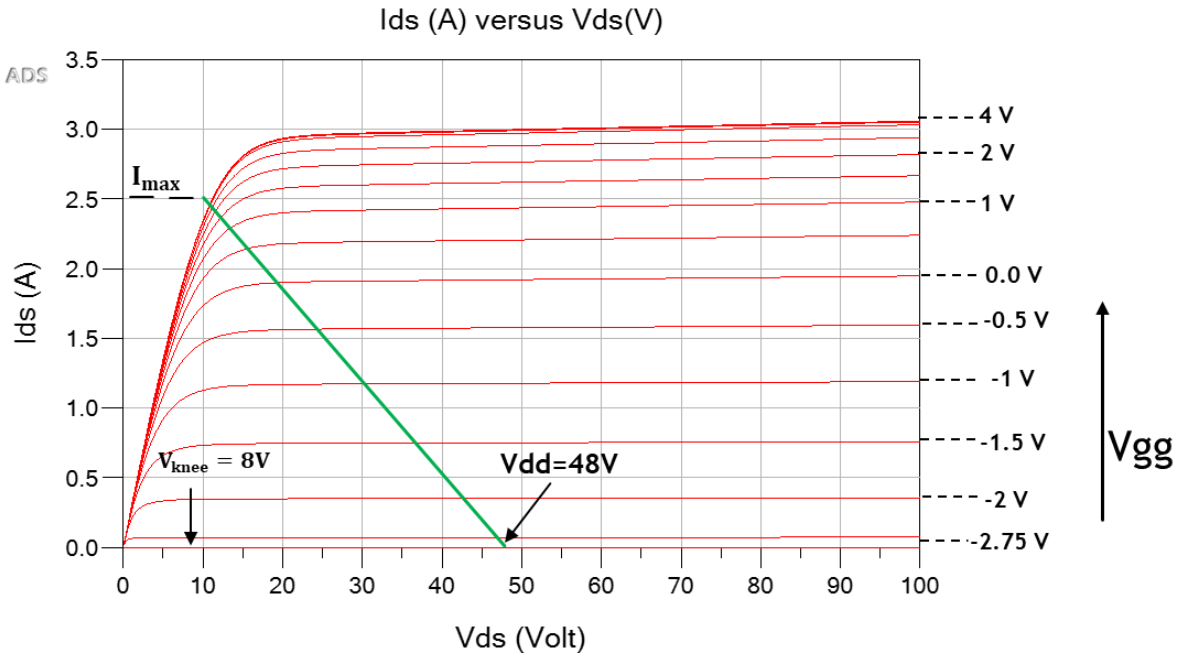


Figure 1. 18: I-V plot result for different Gate voltages

From the I-V curve plot of Figure 1. 18, the theoretical optimum load resistance $R_{opt\_theoretical}$ is computed to allow the maximum excursions of drain current and voltage. Thus, the following numerical values are considered:

$$R_{opt\_theoretical} = \frac{(V_{dd} - V_{knee})}{\frac{I_{max}}{2}} = \frac{(48-8)}{1.25} = 32\ \Omega \tag{1.27}$$

Where: $I_{max} = 2.5$ A, is the maximum RF current, $V_{dd} = 48$ V, is the drain-biasing voltage and $V_{Knee} = 8$ V, is the knee voltage at which the maximum drain current is achieved

The theoretical value of $R_{opt\_theoretical} = 32\ \Omega$ obtained in equation (1.27) is an estimated value of the load resistance presented across the drain and source terminals of the transistor because the final choice of the optimum load resistance for the design of the RF power amplifier depends on the large signal behaviour of the transistor.

1.5.2 Adjustment of the optimum load by nonlinear simulations

Our goal here is to determine the optimal load impedance to present at the output of the transistor to obtain the desired power levels. To do this, ADS Harmonic Balance simulation with a sinusoidal input signal at the operating frequency Fo=2.5 GHz is carried out. Figure 1. 19 below shows the circuit diagram for the simulation. At the input, an ideal matching network is used comprising of a transformer and series inductor to cancel the effect of the input capacitance at Fo. While the output side consists of the previously calculated optimum load resistance $R_{opt\_theoretical}$ in parallel with self-inductance Lp.

The RF choke (RFC) is used to block the higher frequency RF signals and allow only the DC current signals to pass through it. The gate bias voltage is chosen to be Vgg=-2.75 V for operation close to class B. The first step is to adjust the shunt inductance Lp to achieve maximum output power. The result is illustrated in Figure 1. 20 at two input power levels, one corresponding to the amplifier compression and the second is at around 10 dB power backoff.

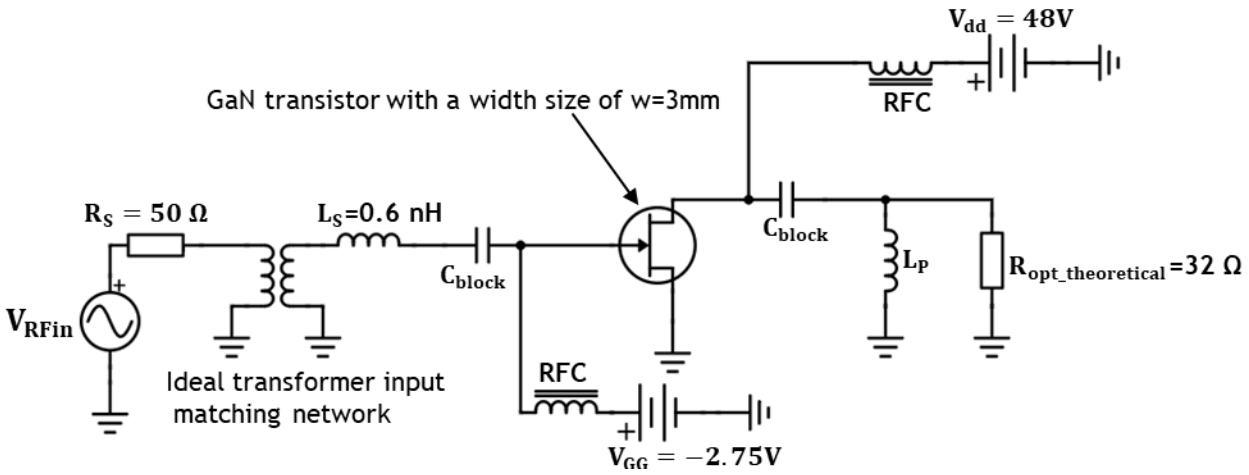


Figure 1. 19: Circuit diagram of the harmonic balance simulation

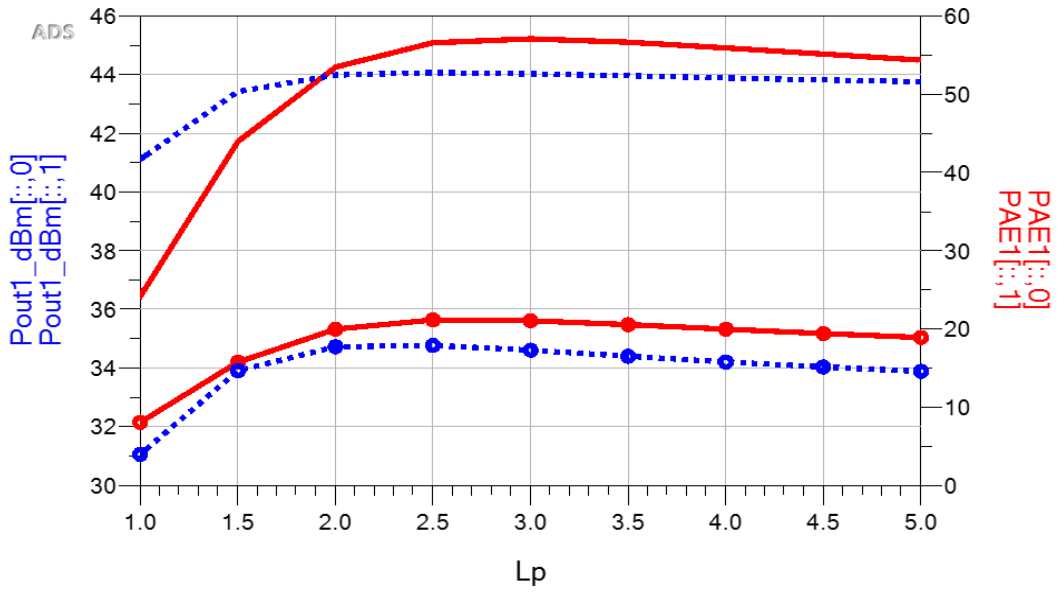


Figure 1. 20: Output power (dotted line) and Power Added Efficiency (PAE) (Solid line) performances at two input power levels versus Lp (nH)

For an inductor Lp value of 3.1 nH, maximum output power is achieved, meaning that the drain current (I_d) and the voltage across the drain-source terminals (V_{ds}) of the transistor are out of phase corresponding to a purely resistive load. We can therefore deduce that there is a resonance between Lp and the output parasitic capacitance (Cd) of the transistor. The output parasitic capacitance can be calculated by :

$$Cd = \frac{1}{(2.\pi.Fo)^2.Lp} = 1.3\,pF \tag{1.28}$$

To verify that the output of the transistor can be modelled by only the capacitance Cd at frequencies around Fo=2.5GHz, we perform simulations of the power amplifier performances at different frequencies of 2, 2.5 and 3 GHz. For each frequency, we make a sweep of Lp to find the optimum value and we calculate the equivalent value of Cd. Hence, the performances are plotted as a function of calculated capacitance Cd and is illustrated in Figure 1. 21. We observed that in all the three frequency cases, the optimum value of Cd is around 1.3 pF, thereby validating the use of a simplified transistor model composed of only Cd in the frequency band of interest as a first estimation.

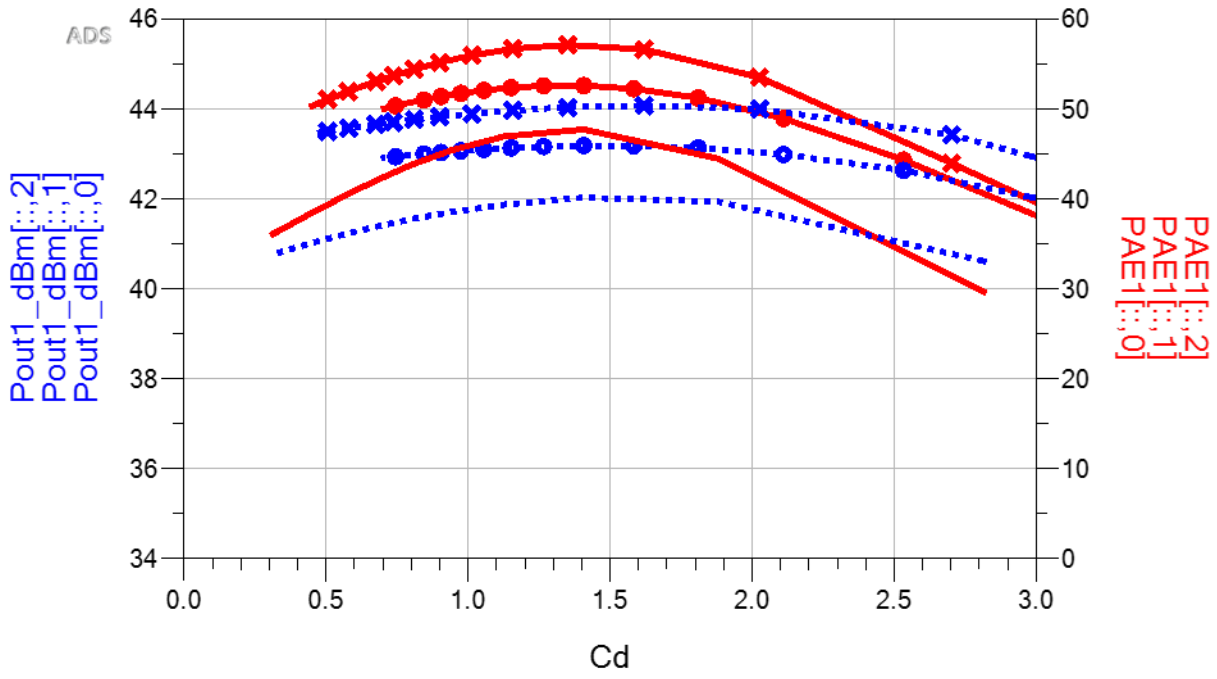


Figure 1. 21: Output power (dotted line) and Power Added Efficiency (PAE) (Solid line) performances as a function of Cd (pF) for three different frequencies of 2 GHz (circle-symbol), 2.5 GHz (x-symbol) and 3 GHz (no-symbol) versus equivalent capacitance Cd (pF).

Next is to run an harmonic balance simulation at an operating frequency of 2.5 GHz by varying the load resistor R_{Lopt} over an input power level in the compression region of the amplifier as shown in Figure 1. 22.

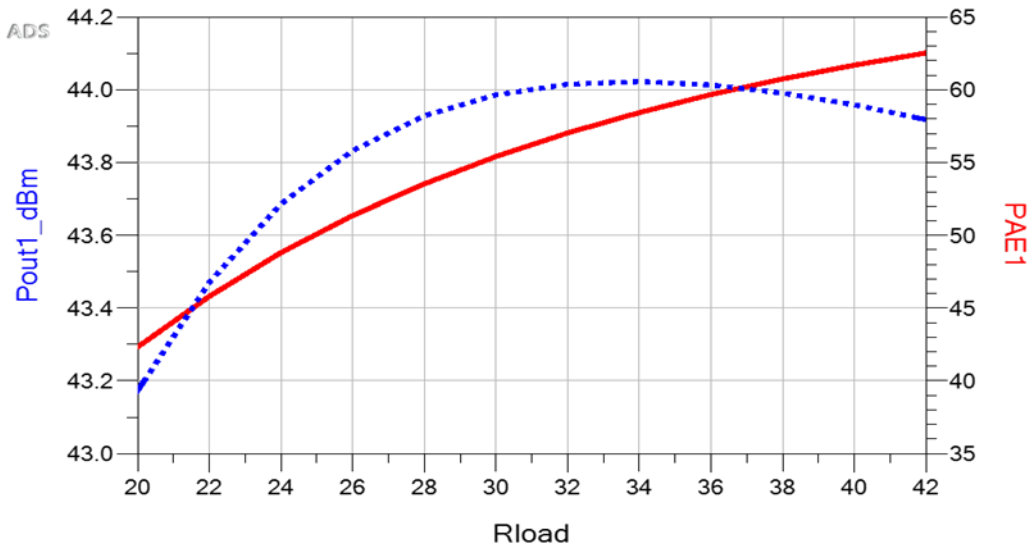


Figure 1. 22: Output power (dotted line) and PAE (solid line) of the power amplifier performances as a function load resistance $R_{Lopt}(\Omega)$ at a design frequency of 2.5 GHz.

The choice of the optimum load resistance which is an important parameter for the design of an RF power amplifier depends on the application. Maximum PAE is obtained at higher value of R_{Lopt} but this leads to a high saturation of the amplifier. Figure 1. 23 shows the comparison of the amplifier performances at an operating frequency of 2.5 GHz in terms of output power and PAE for three different values of RF load resistances of 32 Ω, 36 Ω and 42Ω. We can deduce from Figure 1. 23 that a load resistor of 36 Ω allows a good compromise between the output power level and PAE. This value is chosen for the design of the RF power amplifier.

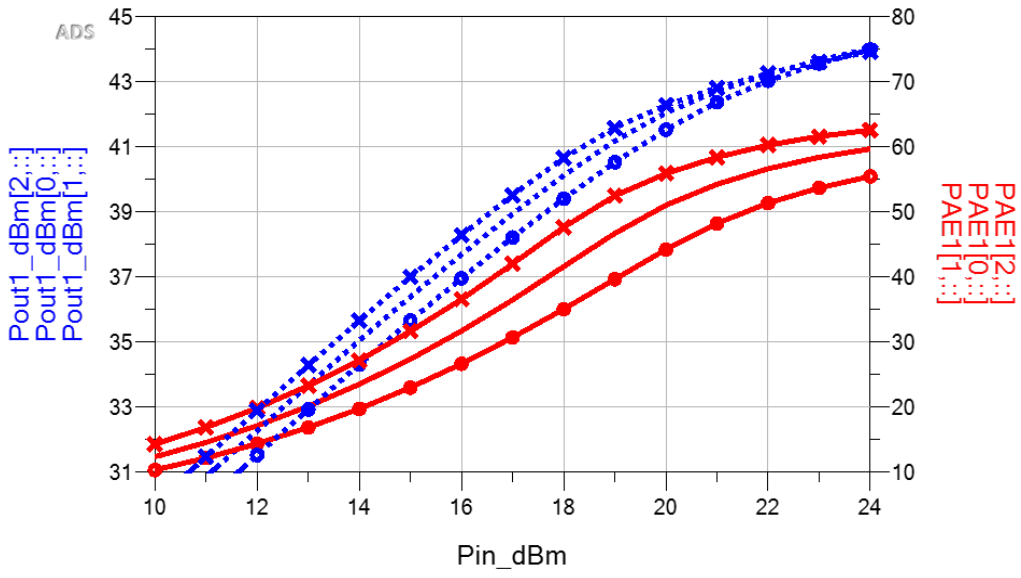


Figure 1. 23: Output power (dotted line) and PAE Performances (solid line) at three load resistances of 32 Ω ohm (circle-symbol), 36 Ω (no-symbol) and 42 Ω (x-symbol) versus input power.

However, it should be noted that the saturation performance can change depending on the load conditions at the output of the amplifier at harmonic frequencies. Thus, the amplifier performances when short circuits are introduced at the output of the transistor at harmonic frequencies are closed to those obtained in Figure 1. 23.

Similarly, the corresponding design values of the gate resistance (R_g) and parasitic input capacitance (C_g) to the transistor of Figure 1. 19 at a load resistance of $R_{Lopt} = 36\,\Omega$ are obtained from the Harmonic Balance simulation results of the input impedance presented by the gate terminal of the transistor. Figure 1. 24 shows the simulated results of the real and imaginary parts of the transistor's input impedance against the input power.

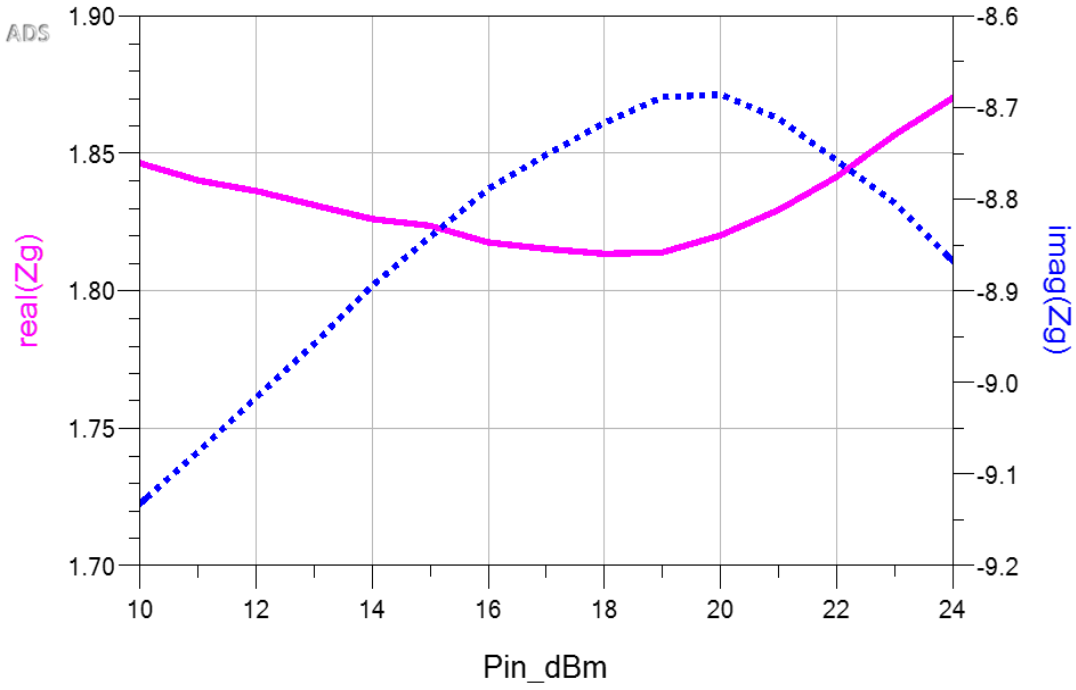


Figure 1. 24: Real part (solid line) and imaginary part (dotted line) of the transistor's input impedance versus input power

From the graph of Figure 1. 24, the expression of the transistor input impedance at an input power of 22 dBm and Fo=2.5 GHz, is given as :

$$Z_g = R_g + jX_g = (1.8 - j8.8)\,\Omega \qquad (1.29)$$

From equation (1.29), the input gate resistance of the transistor is approximately equal to $R_g = 1.8\,\Omega$ and the estimated value of the parasitic gate capacitance C_g of the transistor is calculated using the imaginary part of input impedance of equation (1.29):

$$C_g = \frac{1}{X_g \omega_0} = 7.2\ pF \tag{1.30}$$

Table 1. 3 summarizes the design parameter values for the GaN transistor of Figure 1. 19 to be used in the design of an RF power amplifier.

Table 1. 3: Design parameter values for the GaN transistor with a gate width size W= 3 mm

$V_{GG}(V)$	$V_{ds}(V)$	$I_{max}\,(A)$	$R_g(\Omega)$	$R_{Lopt}(\Omega)$	$C_g(pF)$	$C_d(pF)$	$L_P(nH)$
-2.77	48	2.5	1.8	36	7.2	1.3	3.1

1.6 Conclusion

This chapter has presented the fundamental theory of RF power Amplifier Design. A brief presentation of mobile communications cellular standards were discussed. Also, in this chapter, we described the criteria for selection of the transistor technology used for the amplifier designs, in which GaN-HEMT technology today is consider to have greater potential than LdMOS-based technology in terms of power performance and ease of adaptation. The architecture of the radio frequency front end in an RF transmitter and the performance metrics of an RF power amplifier are briefly introduced.

The analysis of the different PA classes of operation is presented with a calculation of theoretical efficiency. The chapter is concluded with the introduction of RF power amplifier design methodology and the calculation of PA design parameter values.

Chapter 2: Analysis of Different Impedance Matching Network Architectures and Design of Input and Output Matching Networks for the GaN-type RF Power Transistor

2.1 Introduction

The need to optimize the operation of higher frequency (HF) circuits in wireless transmission systems in terms of gain and consequently power transfer at different points of the transmitting chain necessitates the design of an impedance matching network that can match a given load impedance (Z_L) to a source impedance (Z_S) at the desired frequency range [17,18].

Power transfer maximization is essential at every interface of the complete Radio Frequency (RF) network for the achievement of higher overall network efficiency [19,20]. In addition to maximum power transfer, impedance matching can also help in minimizing the noise figure in low noise amplifier (LNA), minimization of the ripples in the gain response of transmission line terminations and achievement of maximum saturated output power for the power amplifier (PA) [14,15,18-20]. Also, it is a standard in RF/Microwave Engineering that all the commercial ports of all RF products are normally designed with 50Ω source and load impedance; hence this invokes the need for impedance matching as well.

A lot of related work done so far has concentrated on using a distributed element to design matching network, thereby making it possible to formulate an equations for designing N-paths matching networks. Some studies have discussed matching network designs that use lumped elements [21,22]. However, it is harder to derive an expression for the matching network with lumped elements compared to using distributed elements. According to [23], an impedance-matching network may consist of either only lumped or distributed elements, or their combinations.

The distributed element-based matching network using either microstrip line elements or any other appropriate transmission medium offers excellent performance, but has the disadvantage of being bulky in size which therefore limits their usage to frequencies over a few Gigahertz. Furthermore, lumped element-based matching networks are smaller in size and are considered for the design of the matching network in this thesis.

In this Chapter, we are presenting an analysis of different topologies of impedance matching networks consisting of ideal passive components using the analytical methods. The fractional bandwidth of the single, Pi, T and Dual sections lowpass matching networks is determined, and the network with the largest bandwidth is recommended as an input and/or output matching network to the GaN-based RF power transistor. This input and output matching network presents an optimum source and load impedance to the RF power amplifier to compensate for the gate and drain interconnections of the GaN transistor respectively.

Generally, for a power amplifier, the transistor input is conjugately matched for maximum gain with good return loss and circuit stability performance, while the output of the transistor is matched to the required load for maximum power or maximum efficiency [24].

2.2 The Principles of impedance matching

The main principles and tools for impedance matching are described in this section. Generally, an optimum solution depends on the circuit requirements such as the simplicity in practical realization, the frequency bandwidth and minimum power ripple, design implementation and adjustability, stable operation conditions and harmonic suppression. As a result, different techniques of matching network using lumped elements and transmission lines are available [25].

Typical matching networks, also referred to as lossless networks, make use of only reactive components that store energy rather than dissipating energy. This characteristic follows naturally from the purpose of a matching network, namely, to enable maximum power transfer from source to load. Hence, the matching network uses capacitors and inductors, and not resistors. Matching networks composed of reactive components are frequency dependent, hence for a 2 elements network, perfect matching only occurs at one frequency which is the centre frequency at which the two reactance cancels or resonates each other, while the impedance match became worst at any other frequency outside the centre frequency. But this creates a problem while attempting to design a wideband matching network. As the desired bandwidth increases, the design of the matching network gets increasingly complicated for most electronics and RF microwave engineers, especially when it must be done over a wide band.

2.2.1 Source and Load sides Impedance matching

This section described the conjugate impedance matching method of improving the matching network bandwidth. Figure 2. 1 shows the source and load impedances of a sinusoidal generator with a voltage amplitude of V_S at a design frequency, F_0.

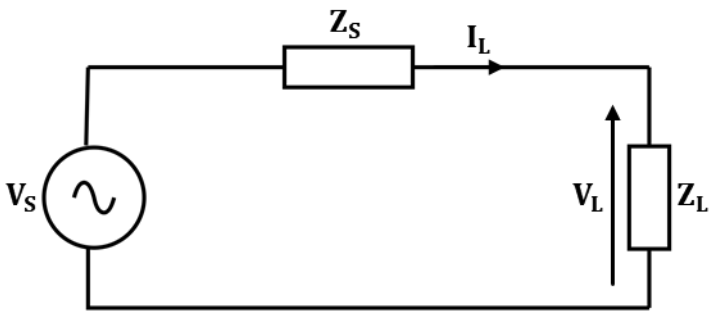


Figure 2. 1: Source and Load Impedances of an AC Generator

Referring to Figure 2. 1, the expression for the power delivered to the load at frequency Fo, is given as follows [25]:

$$P_L = \frac{1}{2} {I_L}^2 \, Re(Z_L(Fo)) = \frac{1}{2} {V_S}^2 \left| \frac{1}{Z_S(Fo) + Z_L(Fo)} \right|^2 Re(Z_L(Fo)) \tag{2.1}$$

Where, $Z_S(Fo) = R_S(Fo) + jX_S(Fo)$, $Z_L(Fo) = R_L(Fo) + jX_L(Fo)$, are the complex impedances at Fo.

When both the real and imaginary parts of Z_S and Z_L are substituted into equation (2.1), then, the delivered power to the load now becomes :

$$P_L = \frac{1}{2} {V_S}^2 \frac{R_L}{(R_S + R_L)^2 + (X_S + X_L)^2} \tag{2.2}$$

It is, therefore, necessary to vary the load impedance Z_L until maximum power is delivered to the load for a fixed source impedance(Z_S). To achieve maximum power, the first condition is that, the sum of the reactive part ($X_S + X_L$) of equation (2.2) must be equal to zero, and as such:

$$X_L = -X_S \tag{2.3}$$

Thus, the simplified version of equation (2.2) now becomes :

$$P_L = \frac{1}{2} {V_S}^2 \frac{R_L}{(R_S + R_L)^2} \tag{2.4}$$

Therefore, the derivative of the power delivered to the load with respect to the real part of the load impedance of equation (2.4) must be zero to maximise the output power. This derivative leads to the second condition and the resulting expression is given by:

$$R_S = R_L \tag{2.5}$$

Thus, from equations (2.3) and (2.5), the conjugate matching condition to achieve maximum power transfer has been fulfilled. Thus:

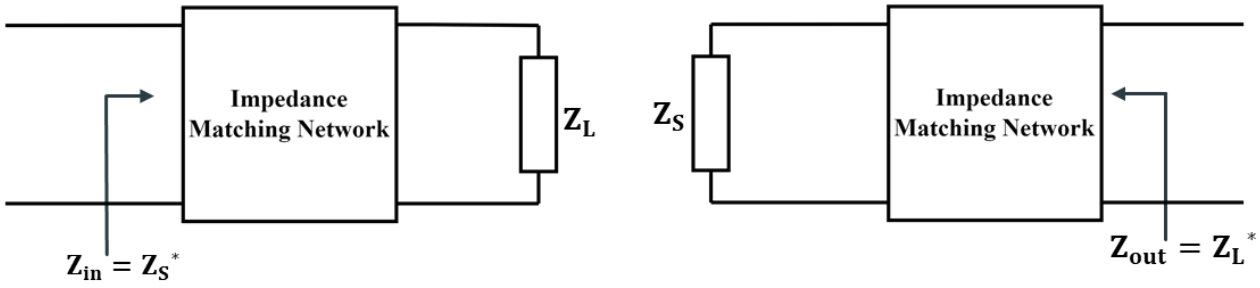
$$Z_L = {Z_S}^* \tag{2.6}$$

Therefore, the maximum power delivered to the load, also known as available power, is determined by substituting equation (2.5) into (2.4). The resulting expression is given by:

$$P_{Lmax} = \frac{{V_S}^2}{8R_S} \tag{2.7}$$

In a general case, when the source and load impedances are fixed, a passive 2-port network is inserted between the source and load impedances to realize impedance matching. This allows for the transfer of

the maximum available RF power from the source to the load, at the operating frequency.This is illustrated in Figure 2.2a where the load presented to the input of the network is equal to the complex conjugate of the source impedance (Z_S). Using the reciprocity theorem, the load presented at the output of the network must be equal to the complex conjugate of the load impedance (Z_L), when the network is loaded on Z_S, as illustrated in Figure 2.2b.



(a) Source side matching (b) Load side matching

Figure 2. 2: Impedance Matching network

The performance of an impedance matching network at a given operating frequency within the bandwidth of interest can be defined by the following parameters:

- Reflection coefficient (Γ): The reflection coefficient (Γ-gamma) represents the ratio of the amplitude of the reflected voltage to the incident voltage in a network. It describes how much voltage is reflected from the load as a result of an impedance mismatch.
  For the matching network of Figure 2.2a, the expression for the input reflection coefficient is given as:

$$\Gamma = \frac{Z_{in} - Z_S}{Z_{in} + Z_S} \tag{2.8}$$

  Where Z_{in} represents the input impedance of the matching network and Z_S denotes the source impedance. According to equation (2.8), when $Z_{in} = Z_S$, the reflection coefficient (Γ) becomes 0, indicating perfect matching.

- Voltage Standing Wave Ratio (VSWR): The ratio of a standing wave peak amplitude to its minimum amplitude is known as the voltage standing wave ratio. The expression for the VSWR in terms of the input reflection coefficient of the matching network is given by:

$$\text{VSWR} = \frac{1 + |\Gamma|}{1 - |\Gamma|} \tag{2.9}$$

Consequently, $\text{VSWR} = 1$, is the minimum desired value of VSWR that will guarantee the maximum power transfer between the source and the load of the matching network as the reflection coefficient (Γ) at this point is zero.

Different matching network topologies allowing the maximum transfer of power from the source to the load side of any given network are available, and their usage depends on the design specifications. For an application involving narrow-band matching, single-section L-matching as well as Pi and T matching networks offer a good candidate, whereas multisection L-matching is recommended for the wideband and broadband matching applications [26, 27].

2.2.2 Parallel-Series and Series-Parallel Impedance Transformation

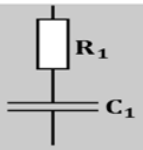
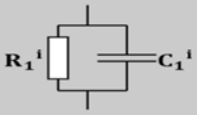
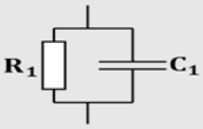
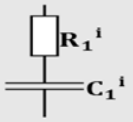
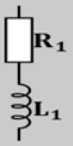
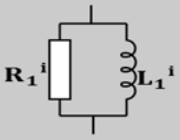
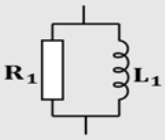
In this section, equations to transform series R-C or R-L to parallel R-C or R-L circuits and vice-versa at an operating frequency F_0 are presented.

While analysing different topologies of impedance-matching networks, it might be necessary to transform a parallel network into a series network or vice-versa.

This transformation means that at the operating frequency F_0, or radian frequency $\omega_0 = 2\pi F_0$, the impedances presented are similar in terms of real and imaginary parts. For example, the series R-C circuit at the input of the transistor can be transformed into a parallel R-C circuit and still presents the same impedance at the operational frequency F_0.

The most common transformations and their corresponding equations are listed in Table 2. 1

Table 2. 1: R-C and R-L Network Transformation

Original Circuit	Transformed Circuit	Formula
		$R_1{}^i = R_1 \frac{R_1{}^2 C_1{}^2 \omega_0{}^2 + 1}{R_1{}^2 C_1{}^2 \omega_0{}^2}$ $C_1{}^i = C_1 \frac{1}{R_1{}^2 C_1{}^2 \omega_0{}^2 + 1}$
		$R_1{}^i = R_1 \frac{1}{R_1{}^2 C_1{}^2 \omega_0{}^2 + 1}$ $C_1{}^i = C_1 \frac{R_1{}^2 C_1{}^2 \omega_0{}^2 + 1}{R_1{}^2 C_1{}^2 \omega_0{}^2}$
		$R_1{}^i = R_1 \frac{R_1{}^2 + L_1{}^2 \omega_0{}^2}{R_1{}^2}$ $L_1{}^i = L_1 \frac{R_1{}^2 + L_1{}^2 \omega_0{}^2}{L_1{}^2 \omega_0{}^2}$
		$R_1{}^i = R_1 \frac{L_1{}^2 \omega_0{}^2}{R_1{}^2 + L_1{}^2 \omega_0{}^2}$ $L_1{}^i = L_1 \frac{R_1{}^2}{R_1{}^2 + L_1{}^2 \omega_0{}^2}$

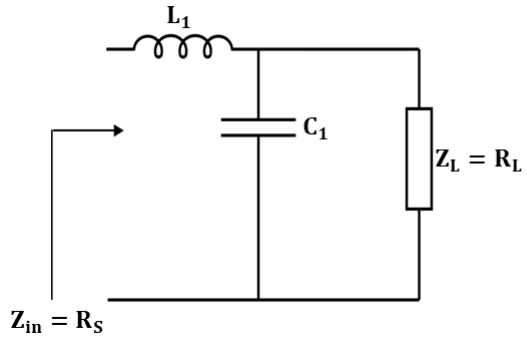
2.3 Single-section L-matching network

2.3.1 L- Matching Network with real source and load impedances

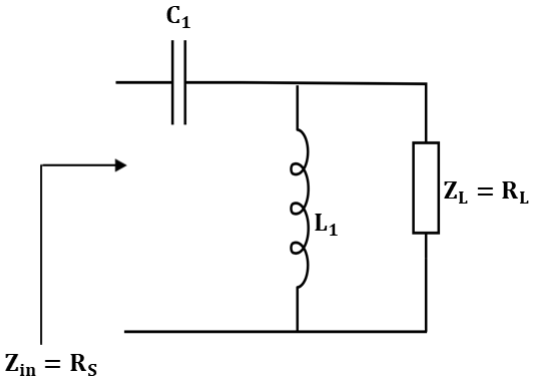
The simplest impedance transformation network is the single-section L-matching network, which requires just two reactive components [28]. It is used in this part to transform a real load impedance (R_L) to a real source impedance (R_S).

Figure 2. 3 below illustrates four possible arrangements of the two reactive components of the matching network. Two of the arrangement (Figure 2.3 a & c) are in lowpass configuration while the remaining two (Figure 2.3 b & d) are in high-pass configuration.

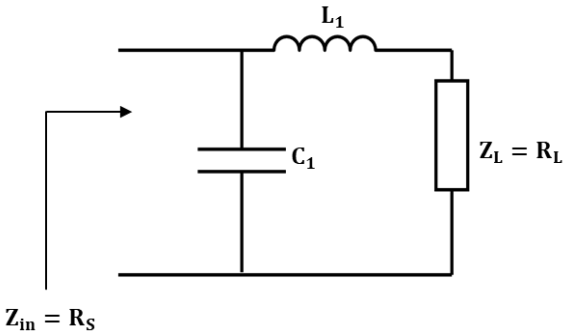
Single-section L-matching networks can also be classified in terms of impedance transformation.We have step-up and step-down impedance transformation.The difference between them as shown in Figure 2. 3 is that, for a step-up impedance transformation, the source impedance (R_S) is greater than the load impedance (R_L) while for the step-down impedance transformation, the load impedance is higher than the source impedance [29].



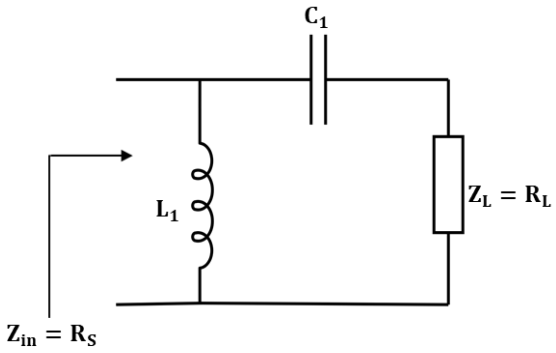
(a) Lowpass MN ($R_S < R_L$)



(b) High pass MN ($R_S < R_L$)



(c) Lowpass MN ($R_S > R_L$)



(d) High pass MN ($R_S > R_L$)

Figure 2. 3: Possible arrangement of Single section L-Matching Network (MN)

To demonstrate the matching network principle, we study the lowpass matching network of case (a) shown in Figure 2.3(a), where $R_S < R_L$.

Using the equations in Table 2. 1, the impedance Z_{in} is given by equation (2.10):

$$Z_{in} = \frac{R_L}{{R_L}^2 {C_1}^2 {\omega_0}^2 + 1} + j\,[L_1\omega_0 - \frac{{R_L}^2 C_1 \omega_0}{{R_L}^2 {C_1}^2 {\omega_0}^2 + 1}] \tag{2.10}$$

To guarantee an impedance match between the source and load resistors; the impedance Z_{in} must be equal to the conjugate of impedance Zs, as such, $Z_{in} = {Z_S}^* = R_S$.

By equating the real and imaginary parts of equation (2.10) to R_S and 0 respectively, we obtain the following system of equations:

$$R_S = \frac{R_L}{{R_L}^2 {C_1}^2 {\omega_0}^2 + 1} \tag{2.11}$$

$$L_1\omega_0 = \frac{R_L{}^2 C_1 \omega_0}{R_L{}^2 C_1{}^2 \omega_0{}^2 + 1} \tag{2.12}$$

From equations (2.11) and (2.12), the expression for the lumped components of the single-section lowpass matching network is found to be:

$$C_1 = \frac{1}{R_L \omega_0}\sqrt{\frac{R_L - R_S}{R_S}} \tag{2.13}$$

$$L_1 = \frac{R_S}{\omega_0}\sqrt{\frac{R_L - R_S}{R_S}} \tag{2.14}$$

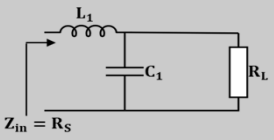
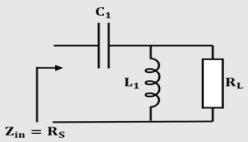
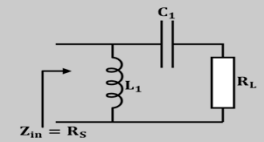
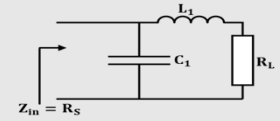
Therefore, the quality factor (Q) of the matching network of Figure 2.3 (a) is given by:

$$Q = \frac{1}{2}\sqrt{\frac{R_L - R_S}{R_S}} \tag{2.15}$$

Based on these equations, it can be verified that the matching network can transform the load resistance R_L to the source resistor R_S at Fo if R_L is greater than R_S.

Table 2. 2 shows the summary of the design equations based on the real source and load impedances of the four network topologies in Figure 2. 3, computed at the center angular frequency $\omega_0 = 2\pi F_0$.

Table 2. 2: Matching of Two Real Impedances using two reactive elements

Type	Circuit	Inductor(L)	Capacitor(C)	Quality factor (Q)
1		$L_1 = \frac{R_S}{W_0}\sqrt{\frac{R_L - R_S}{R_S}}$	$C_1 = \frac{1}{R_L W_0}\sqrt{\frac{R_L - R_S}{R_S}}$	$Q = \frac{1}{2}\sqrt{\frac{R_L - R_S}{R_S}}$
2		$L_1 = \frac{R_L}{W_0}\sqrt{\frac{R_S}{R_L - R_S}}$	$C_1 = \frac{1}{R_S W_0}\sqrt{\frac{R_S}{R_L - R_S}}$	$Q = \frac{1}{2}\sqrt{\frac{R_L - R_S}{R_S}}$
3		$L_1 = \frac{R_S}{W_0}\sqrt{\frac{R_L}{R_S - R_L}}$	$C_1 = \frac{1}{R_L W_0}\sqrt{\frac{R_L}{R_S - R_L}}$	$Q = \frac{1}{2}\sqrt{\frac{R_S - R_L}{R_L}}$
4		$L_1 = \frac{R_L}{W_0}\sqrt{\frac{R_S - R_L}{R_L}}$	$C_1 = \frac{1}{R_S W_0}\sqrt{\frac{R_S - R_L}{R_L}}$	$Q = \frac{1}{2}\sqrt{\frac{R_S - R_L}{R_L}}$

2.3.2 L-Matching Network with complex source impedance and real load impedance

The matching network of Table 2. 2 only deals with the matching of two real impedances (i.e. source and load impedances). However, in some cases the source impedance is a complex impedance consisting of a parallel connection of capacitor C_P and the source resistor R_S as depicted in Figure 2. 4 below. This category of matching network is used to matched the impedance presented to the ouput terminal of a transistor. The output impedance of a transistor is given by the parallel connection of the drain parasitic capacitance Cds and the output drain current source. Thus, to present an optimum load resistance (Ropt) to the drain current source, Cds has to be considered in the network design.

The design equations of the four matching networks shown in Figure 2. 4 based on complex source impedance and real load impedance are listed in Table 2. 3 below. For cases (a) to (d), the parallel connection of C_P and R_S can possibly be transformed into a series connection at an operating frequency F_0 to simplify the analysis of the network, and its new component values which now becomes (C^i_P and R^i_S), are determined using the equations given in Table 2. 1 without affecting the impedance matching condition at Fo.

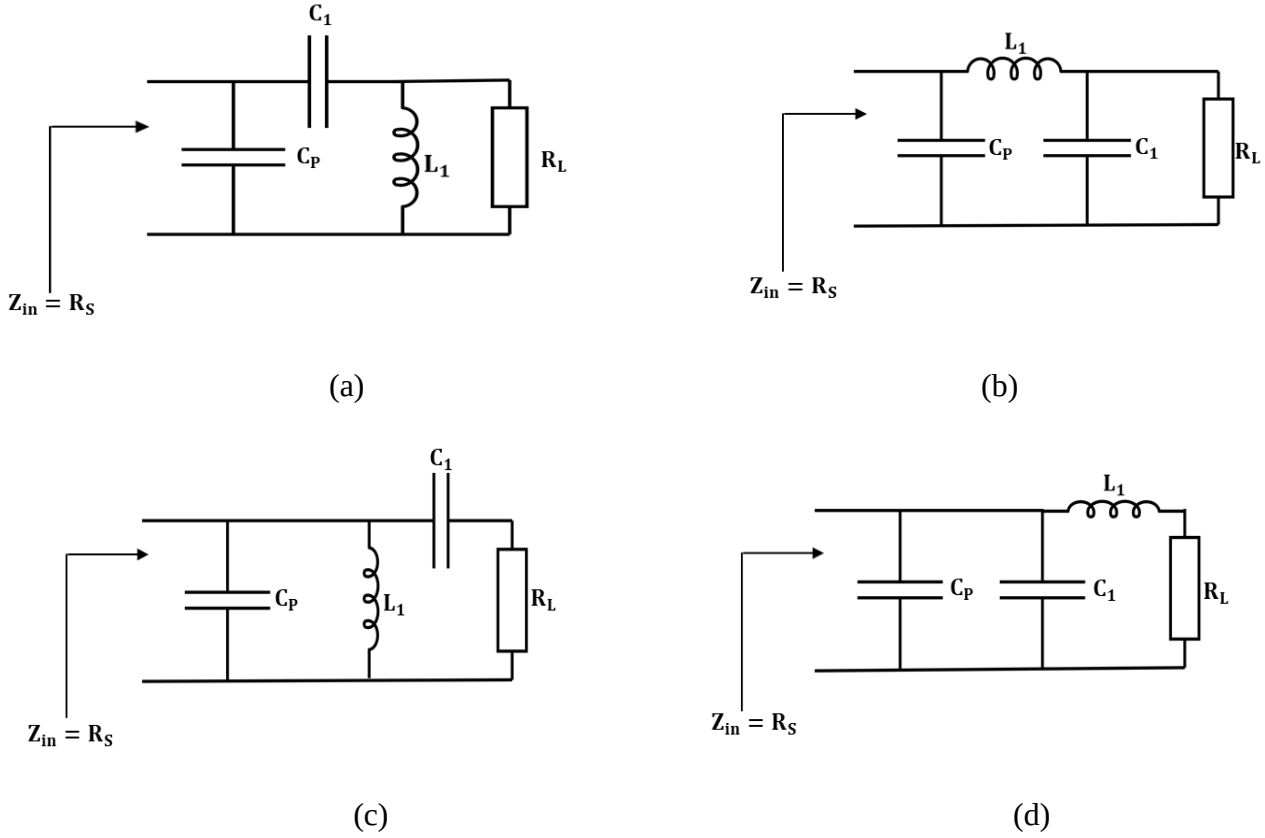


Figure 2. 4: Single-section lumped element-based lowpass L-matching networks with complex source impedance and real load impedance

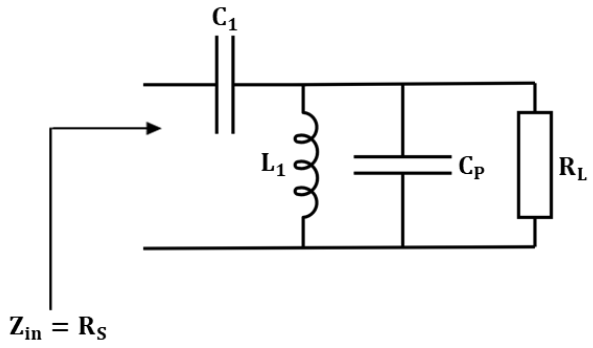
Table 2. 3: Design equations for Single section lumped element-based lowpass L-matching networks with complex source and real load impedances

Type	Inductor (L)	Capacitor (C)
Fig. 2.4a	$\mathbf{L_1} = \frac{R_S}{\omega_0}\frac{R_S C_P \omega_0 + \sqrt{\frac{R_L}{R_S} - 1 + R_S R_L C_P{}^2 \omega_0{}^2}}{R_S{}^2 C_P{}^2 \omega_0{}^2 + 1}$	$\mathbf{C_1} = \frac{1}{R_L \omega_0}\sqrt{\frac{R_L}{R_S} - 1 + R_S R_L C_P{}^2 \omega_0{}^2}$
Fig. 2.4b	$\mathbf{L_1} = \frac{R_L}{\omega_0}\sqrt{\frac{R_S}{R_L - R_S + \omega_0{}^2 C_P{}^2 R_S{}^2 R_L}}$	$\mathbf{C_1} = \frac{R_S C_P \omega_0 + \sqrt{\frac{R_L - R_S + \omega_0{}^2 C_P{}^2 R_S{}^2 R_L}{R_S}}}{\omega_0 (R_L - R_S)}$
Fig. 2.4c	$\mathbf{L_1} = \frac{R_S}{\omega_0}\frac{1}{R_S C_P \omega_0 + \sqrt{\frac{R_S - R_L}{R_L}}}$	$\mathbf{C_1} = \frac{1}{R_L \omega_0}\sqrt{\frac{R_L}{R_S - R_L}}$
Fig. 2.4d	$\mathbf{L_1} = \frac{R_L}{\omega_0}\sqrt{\frac{R_S - R_L}{R_L}}$	$\mathbf{C_1} = -C_P + \frac{1}{R_S \omega_0}\sqrt{\frac{R_S - R_L}{R_L}}$

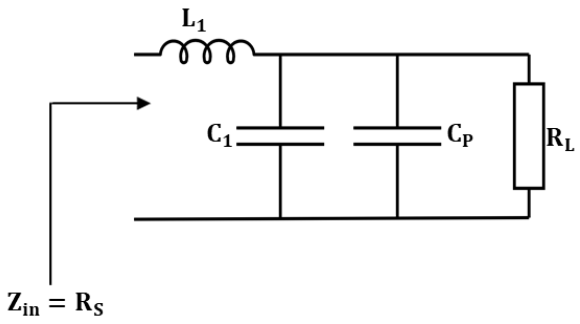
2.3.3 L- Matching Network with real source impedance and complex load impedance

In this part, we consider that the load is complex and is represented by a parallel RC or RL circuit. Using Table 2. 1, the parallel connection of capacitor C_P and the load resistor R_L shown in Figure 2. 5 can be transformed into a series connection at Fo. Then, the expression for determining the matching network parameters (L_1 & C_1) of Figure 2. 5 can be easily analyzed.

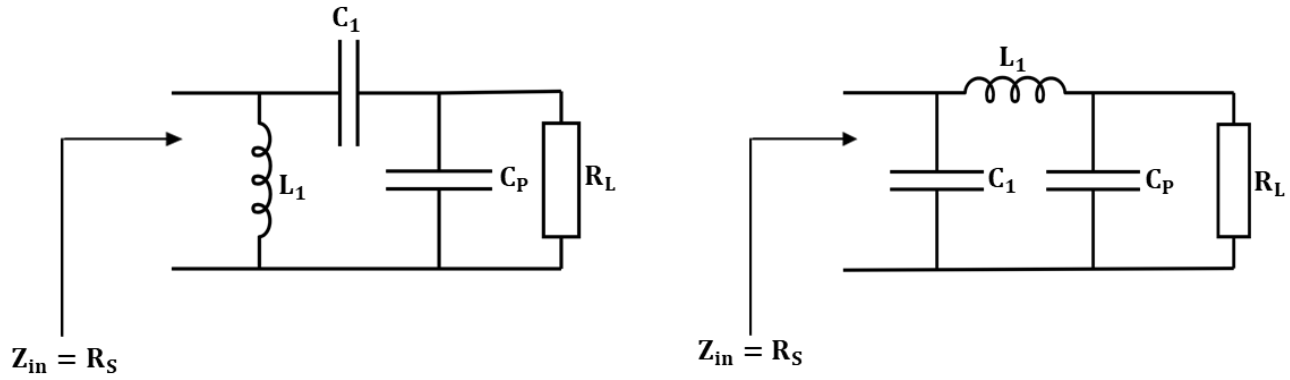
Table 2. 4 shows the summary of the design equations of the complex load impedances of Figure 2. 5.



(a)



(b)



(c) (d)

Figure 2. 5: Single-section lumped element-based lowpass L-matching networks with real source impedances and complex load impedances

Table 2. 4: Design equations for Single section lumped element-based lowpass L-matching networks with real source and complex load impedances

Type	Inductor (L)	Capacitor (C)
Fig. 2.5a	$\mathbf{L_1} = \frac{R_S}{\omega_0}\sqrt{\frac{R_L - R_S}{R_S}}$	$\mathbf{C_1} = -C_P + \frac{1}{R_L\omega_0}\sqrt{\frac{R_L - R_S}{R_S}}$
Fig. 2.5b	$\mathbf{L_1} = \frac{R_L}{\omega_0}\frac{1}{R_L C_P \omega_0 + \sqrt{\frac{R_L - R_S}{R_S}}}$	$\mathbf{C_1} = \frac{1}{R_S\omega_0}\sqrt{\frac{R_S}{R_L - R_S}}$
Fig. 2.5c	$\mathbf{L_1} = \frac{R_S}{\omega_0}\sqrt{\frac{R_L}{R_S - R_L + \omega_0^2 C_P^2 R_L^2 R_S}}$	$\mathbf{C_1} = \frac{R_L C_P \omega_0 + \sqrt{\frac{R_S - R_L + \omega_0^2 C_P^2 R_L^2 R_S}{R_L}}}{\omega_0(R_S - R_L)}$
Fig. 2.5d	$\mathbf{L_1} = \frac{R_L}{\omega_0}\frac{R_L C_P \omega_0 + \sqrt{\frac{R_S}{R_L} - 1 + R_S R_L C_P^2 \omega_0^2}}{R_L^2 C_P^2 \omega_0^2 + 1}$	$\mathbf{C_1} = \frac{1}{R_S\omega_0}\sqrt{\frac{R_S}{R_L} - 1 + R_S R_L C_P^2 \omega_0^2}$

2.3.4 Conclusion on L Matching Network

The quality factor (Q) of any matching network configuration, which comprises a purely resistive source and load impedances, can also be defined as a function of bandwidth as the ratio of the operating frequency (F_0) to the bandwidth (BW) of the network.

$$Q_{BW} = \frac{F_0}{BW} \tag{2.16}$$

The 2 elements L-matching network has the disadvantage of not allowing an RF circuit designer to have control over the choice of its Quality factor (Q) since the Q of the L-matching network is defined once its R_S and R_L are known (see Table 2. 2). However, if either the source or load impedances are complex, then the quality factor will become a function of the real parts of the impedances and their imaginary parts. Thus, the use of a single-section L-matching network imposes a constraint on the quality factor of the matching network.

Furthermore, the lack of circuit-Q versatility in a matching network can be a barrier, especially if a given bandwidth is required. This drawback is overcome using more elements matching network as described in the following sections.

2.4 Cascaded L-Sections Matching Networks

If an impedance matching is required over a wider range of frequencies, then this can be achieved by cascading L-matching networks in series [30,31]. The two basic network topologies for the multistage L-matching networks for a case where the source resistance is lower and higher than the load resistance ($R_S<R_L$, $RS>R_L$) are shown in Figure 2. 6 & Figure 2. 7 respectively. Just like the previously discussed matching network, a multistage L-matching network can also have low pass and high pass frequency response characteristics.

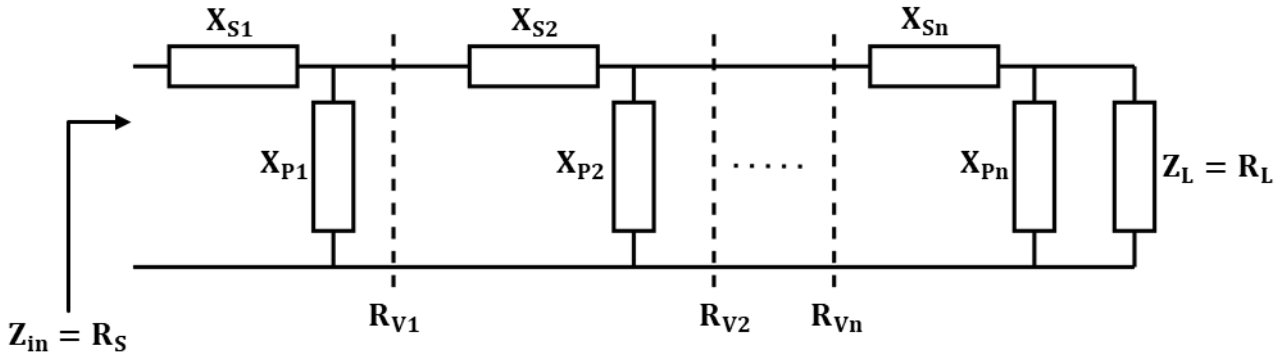


Figure 2. 6: Multi-stage L-section Matching Network for $R_S<R_L$ case

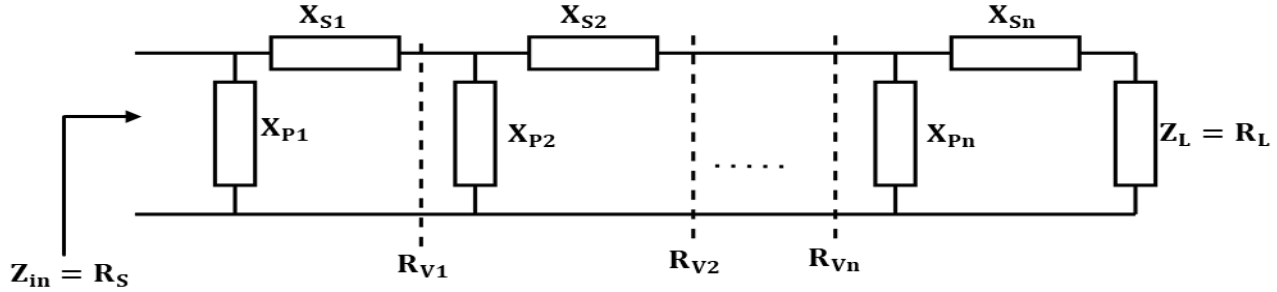


Figure 2. 7: Multi-stage L-section Matching Network for $R_S>R_L$ case

2.4.1 Double Section Lowpass L-matching Network

The double-section lowpass L-matching network is comprised of two-series connected networks of L and C, arranged between the real source and load resistors as shown in Figure 2. 8.

With a 4-elements matching network, it is possible to realize perfect matching at 2 frequencies, leading to maximum power transfer on a larger bandwidth.

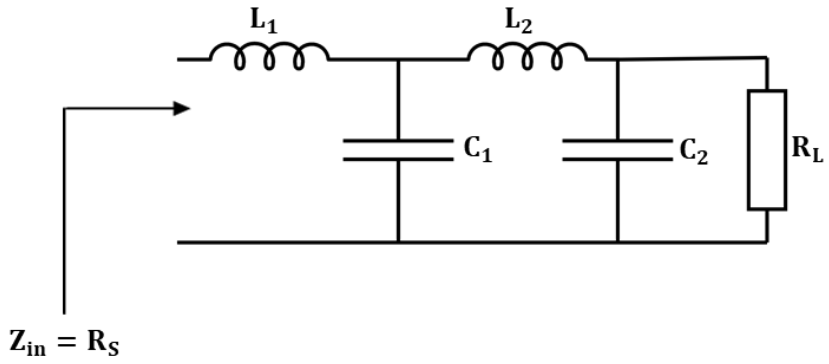


Figure 2. 8: Dual Section Lowpass Impedance Matching Network

The synthesis of the double-section lowpass matching network is done by splitting the network into two L-sections and solving them individually by introducing two complex impedances at the midpoint of the network, one at the source side and the other at the load side, as illustrated in Figure 2. 9.

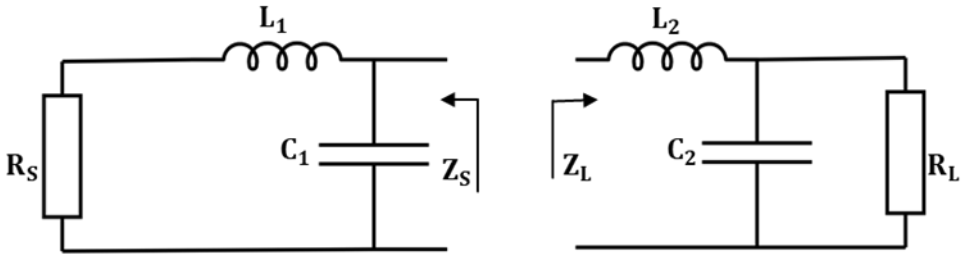


Figure 2. 9: Splitting of dual section matching network

For perfect impedance matching to take place, the complex impedances Z_S and Z_L must be conjugate; as such, $Z_S=Z_L^*$. Using two different frequencies, F_1 and F_2, and the real and imaginary parts of the two complex impedances, we are dealing with a system of four equations with four unknowns L_1, L_2, C_1, and C_2.

The equation for the complex impedance (Z_S) seen toward the source side can be written as [30,31]:

$$Z_S = \frac{R_S}{{R_S}^2{C_1}^2\omega_1{}^2 + (L_1C_1\omega_1{}^2 - 1)^2} + j\omega_1\left(\frac{L_1(1 - L_1C_1\omega_1{}^2) - {R_S}^2C_1}{{R_S}^2{C_1}^2\omega_1{}^2 + (L_1C_1\omega_1{}^2 - 1)^2}\right) \quad (2.17)$$

For the impedance seen towards the load:

$$Z_L = \frac{R_L}{1 + {R_L}^2 {C_2}^2 {\omega_2}^2} + j\omega_2 \left(L_2 - R_L \frac{R_L C_2}{1 + {R_L}^2 {C_2}^2 {\omega_2}^2} \right) \tag{2.18}$$

By equating the real parts of the two complex impedances, we obtained the following system of equations:

$$\frac{R_L}{1 + {R_L}^2 {C_2}^2 {\omega_1}^2} = \frac{R_S}{{R_S}^2 {C_1}^2 {\omega_1}^2 + (L_1 C_1 {\omega_1}^2 - 1)^2} \tag{2.19}$$

$$\frac{R_L}{1 + {R_L}^2 {C_2}^2 {\omega_2}^2} = \frac{R_S}{{R_S}^2 {C_1}^2 {\omega_2}^2 + (L_1 C_1 {\omega_2}^2 - 1)^2} \tag{2.20}$$

Similarly, the conjugate of the imaginary parts of the two complex impedances are related by the following expressions: Imaginary (Z_L) = - Imaginary (Z_S), hence the following equations are given :

$$L_2 - R_L \frac{R_L C_2}{1 + {R_L}^2 {C_2}^2 {\omega_1}^2} = \frac{L_1(-1 + L_1 C_1 {\omega_1}^2) + {R_S}^2 C_1}{{R_S}^2 {C_1}^2 {\omega_1}^2 + (L_1 C_1 {\omega_1}^2 - 1)^2} \tag{2.21}$$

$$L_2 - R_L \frac{R_L C_2}{1 + {R_L}^2 {C_2}^2 {\omega_2}^2} = \frac{L_1(-1 + L_1 C_1 {\omega_2}^2) + {R_S}^2 C_1}{{R_S}^2 {C_1}^2 {\omega_2}^2 + (L_1 C_1 {\omega_2}^2 - 1)^2} \tag{2.22}$$

Where ω_1 and ω_2 are the matching radian frequencies.

Solving the above four equations simultaneously, the design equations for the network parameters of Figure 2. 8 are given as follows:

$$C_1 = \frac{\sqrt{2}}{A R_S} \sqrt{A - B + \sqrt{B^2 - \left(\frac{A^2}{\alpha^2} + 2A(B - A) \right)}} \tag{2.23}$$

Where,

$$\alpha = \frac{1}{\omega_1 \omega_2} \sqrt{\frac{R_L - R_S}{R_L}} \tag{2.24}$$

$$A = 2\alpha \omega_1 \omega_2 \tag{2.25}$$

$$B = {\omega_1}^2 + {\omega_2}^2 \tag{2.26}$$

$$L_1 = \frac{2}{AC_1} \tag{2.27}$$

$$L_2 = R_S R_L C_1 \tag{2.28}$$

$$C_2 = \frac{L_1}{R_S R_L} \tag{2.29}$$

The above design equations indicate that the matching network of Figure 2. 8 can only be adopted if $R_L > R_S$. Similarly, the analysis of the high pass double section L-matching network shown in Figure 2. 10, which comprises inductors and capacitors as the shunt and series elements respectively, can be done in the same way as the lowpass double-section matching network.

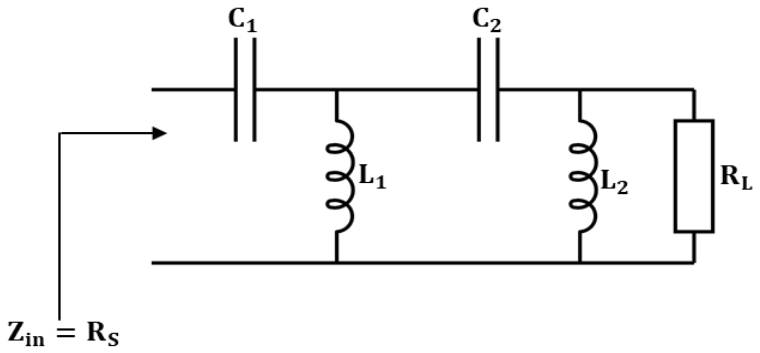


Figure 2. 10: Dual Section High-pass Impedance Matching Network

2.5 Design of an input and output impedance matching networks for a GaN-type RF power transistor

2.5.1 Power amplifier matching

When designing a power amplifier, it is necessary to use matching networks at both the input and output of an RF power transistor within the desired frequency range. The input matching network is responsible for transforming the impedance between the source and the gate of the GaN transistor, allowing it to flatten the small signal gain and leading to a better input return loss.

On the other hand, the output matching network focuses on achieving impedance transformation between the drain-current source of the transistor and the load impedance to ensure maximum output power.

The matching conditions can be written at the gate and drain terminals of the transistor. The two system impedances (R_S & R_L) which are usually equal to 50Ω as shown in Figure 2. 11, are transformed to the optimum input impedance (Zin_opt) and optimum output impedance (Zout_opt) respectively.

To simplify the design analysis, we considered the input impedance Z_g to the GaN transistor as a complex impedance consisting of gate resistance (R_g) connected in series with the parasitic gate capacitance (C_g) as illustrated in Figure 2. 11.

The impedance Zin_opt, seen at the output of the input matching network, must be equal to the complex conjugate of the gate impedance Z_g of the transistor at any given design radian frequency (ω). Thus, the two impedances are related by the following equation:

$$Zin\_opt(\omega) = {Z_g}^*(\omega) = R_g + \frac{j}{C_g.\omega} \tag{2.30}$$

Furthermore, at the drain terminal, an optimum real load resistance (R_{opt}) of equation (1.11) must be presented to the drain current source to maximise the output power with the aid of the output matching network.

By taking into consideration the parasitic capacitor C_d connected between the drain and source terminals of the transistor, the expression of the load presented to the transistor drain at any given design radian frequency (ω) is:

$$Zout\_opt(\omega) = \left(\frac{1}{Yd(\omega)}\right)^* = \frac{1}{\frac{1}{R_{opt}} - j.C_d.\omega} \tag{2.31}$$

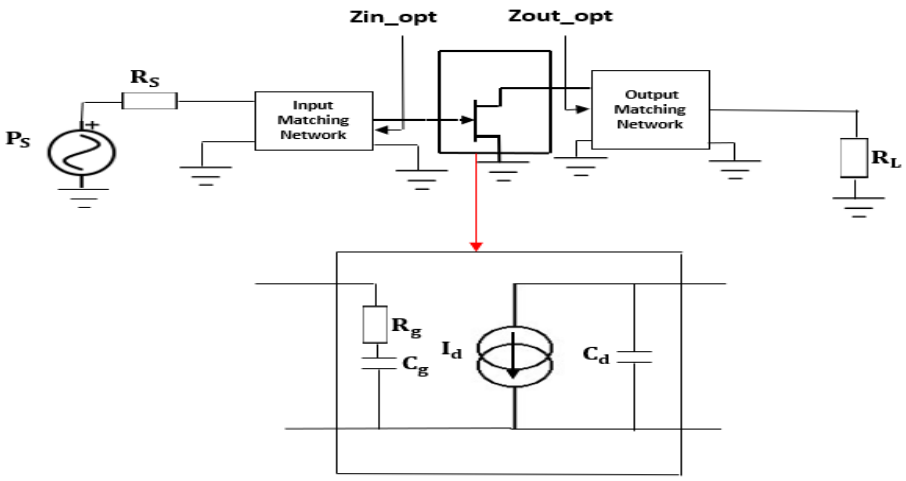


Figure 2. 11: Schematic of a single-ended power amplifier showing the simplified model of the transistor composed of parasitic capacitances Cg and Cd

To demonstrate the design of the input and output matching networks, we used the same GaN transistor shown in Chapter 1 of this thesis. The transistor design parameter values are derived from the complete model of the GaN transistor shown in Figure 1. 17 and are listed in Table 1. 3. The operating frequency of $Fo = 2.5$ GHz is chosen for the design.

2.5.2 Dealing with Complex Loads

Although some of the matching networks described in the preceding section focused on purely resistive sources and loads. However, for power amplifier design applications, both the source and load impedances include reactance. This section will therefore present strategies for dealing with complex sources and loads.

Generally, the resistive and reactive components are present in the input and output impedances of transistors, mixers, antennas, and other RF devices. A practical, complex impedance matching problem is illustrated in Figure 2. 12.

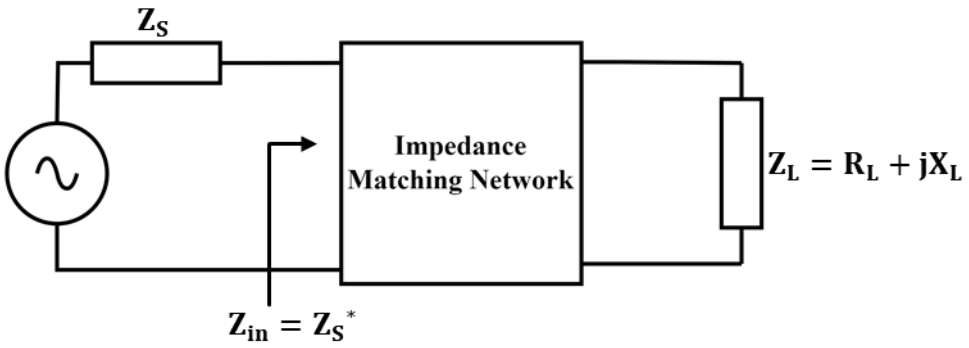
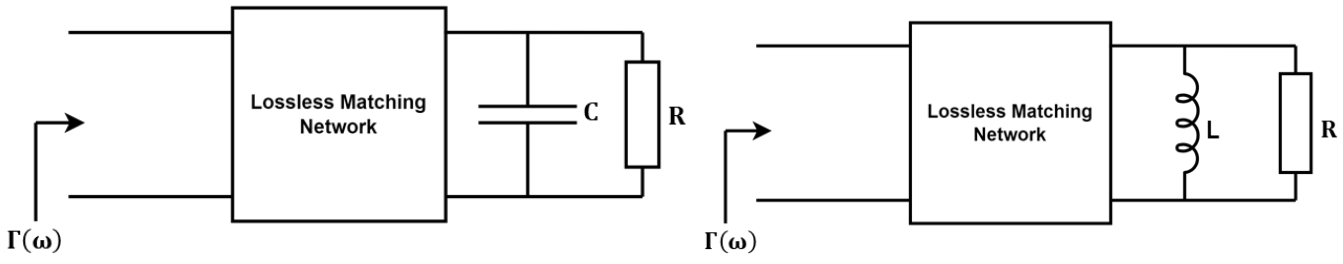
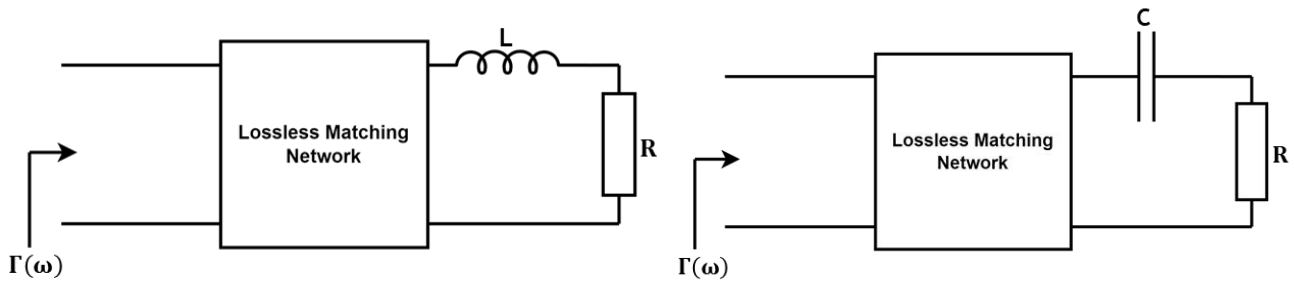


Figure 2. 12: Matching a complex load to a source impedance

Bode and Fano in Refs. [33] and [34] demonstrated how bandwidth limitations exist on the impedance-matching network of a complex load. Thus, reactive loads with energy storage components limit the bandwidth of a matching network. These theoretical limits are referred to as the Bode-Fano limit or Bode-Fano criteria. The Bode-Fano Limits are therefore used as a yardstick to justify the claim that the more reactive energy stored in a load, the narrower the bandwidth of the impedance match. The basic circuits for the different types of reactive loads are shown in Figure 2. 13.



(a) Parallel R-C Load (b) Parallel R-L Load



(c) Series R-L Load (d) Series R-C Load

Figure 2. 13: Bode-Fano Limits for circuits with reactive loads

The Bode-Fano Limits of the Four Simple reactive load circuits shown in Figure 2. 13 above can be written as follows:

(a) Parallel R-C Load:

$$\frac{BW}{F_0}\ln\left(\frac{1}{\Gamma avg}\right) \leq \frac{\pi}{R_L(W_0C)} \tag{2.32}$$

(b) Parallel R-L Load:

$$\frac{BW}{F_0}\ln\left(\frac{1}{\Gamma avg}\right) \leq \frac{\pi(W_0L)}{R_L} \tag{2.33}$$

(c) Series R-L Load:

$$\frac{BW}{F_0}\ln\left(\frac{1}{\Gamma avg}\right) \leq \frac{\pi R_L}{(W_0L)} \tag{2.34}$$

(d) Series R-C Load:

$$\frac{BW}{F_0}\ln\left(\frac{1}{\Gamma avg}\right) \leq \pi R_L(W_0C) \tag{2.35}$$

The average absolute value of the magnitude of reflection coefficient $\Gamma(\omega)$, denoted as Γavg, can be determined by looking into the matching network shown in Figure 2. 13. The centre frequency is represented by F_0.

The above equations can further be simplified by writing them in terms of reactance (X) and susceptance (B):

Parallel Load:

$$\frac{BW}{F_0}\ln\left(\frac{1}{\Gamma avg}\right) \leq \frac{\pi G}{|B|} \tag{2.36}$$

Series Load:

$$\frac{BW}{F_0}\ln\left(\frac{1}{\Gamma avg}\right) \leq \frac{\pi R_L}{|X|} \tag{2.37}$$

Where $G = \frac{1}{R_L}$, is the conductance of the load, B is the susceptance, and X is the load reactance.

Equations (2.36) and (2.37) can further be simplified and written in terms of the load quality factor Q:

$$\frac{BW}{F_0}\ln\left(\frac{1}{\Gamma avg}\right) \leq \frac{\pi}{Q} \tag{2.38}$$

The expression of equation (2.38) shows that the more reactive energy stored in a load, the narrower the bandwidth of the match. Additionally, for the same average in-band reflection coefficient, the higher the Q, the narrower the bandwidth of the matching.

Consequently, the fractional bandwidth limitation for an equivalent series (R_g C_g) presented to the gate terminal of the GaN transistor of Figure 2. 11, at a reflection coefficient threshold of ($\Gamma = -20\ \text{dB} = 0.1$) and operating frequency of F_o=2.5 GHz, can be determined by re-arranging equation (2.35), and is given as:

$$FBW_{max} = \left(\frac{2\pi^2 R_g F_0 C_g}{\ln\left(\frac{1}{\Gamma}\right)}\right)\% = 27.8\% \tag{2.39}$$

Similarly, the maximum achievable fractional bandwidth of the equivalent parallel (R_{opt} // C_d) presented to the drain-source terminal of the GaN transistor of Figure 2. 11, under the same design conditions is computed by re-arranging equation (2.32), and is given as:

$$FBW_{max} = \left(\frac{1}{2.F_0 R_{opt}.C_d.\ln\left(\frac{1}{\Gamma}\right)}\right)\% = 185.6\% \tag{2.40}$$

The values of the series (R_g C_g) and the parallel (R_{opt} // C_d) of the GaN transistor are provided in Table 1. 3. The results clearly show that the bandwidth is limited by the input network.

2.5.3 Design of Lowpass input matching networks

The lowpass matching network types where the source resistance (R_S) is greater than the load resistance (R_L) are designed as the input matching network to the single-stage RF power amplifier shown in Figure

2. 11. The parasitic capacitance (C_g) and gate resistance (R_g) of the GaN transistor are taken into consideration while designing the network.

The following lumped element-based lowpass input matching networks are considered for design:

i. Single Section Lowpass input L-matching network
ii. Pi and T Section Lowpass input matching network
iii. Double Section Lowpass input L-matching network
iv. Triple Section Lowpass input L-matching network

2.5.3.1 Single Section Lowpass Input L-Matching Network Design

The design steps for the single-section low pass input L-matching network of Figure 2. 14 with a series inductance (L_1) and shunt capacitance (C_1) are described in this section.

This network is used to transform the input impedance of the GaN transistor to a 50Ω source impedance at the operating frequency Fo. The initial lumped element values L_{1o} and C_{1o} of the network are computed at $Fo = 2.5$ GHz using the equations of the type 4 network shown in Table 2. 2 above by first ignoring the parasitic gate capacitor of the transistor. As a result, the network's initial values are given as: $L_{1o} = 0.59$ nH , $C_{1o} = 6.59$ pF.

By considering the parasitic capacitor C_g at the input of the transistor shown in Figure 2. 11, the new series inductance L_1 is computed using the following formula:

$L_{1n} = L_{1o} + \frac{1}{C_g.\omega 0^2} = 1.16$ nH, where the C_g for the GaN transistor is given as: C_g=7.2 pF

Table 2. 5 gives a summary of the final calculated values for the network parameters in Figure 2. 14

Table 2. 5: lumped elements values for single section lowpass IMN at 2.5 GHz

C_1(pF)	L_{1n} (nH)
6.59	1.16

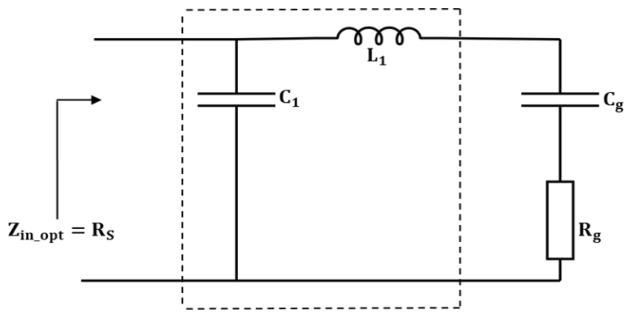


Figure 2. 14: Single Section Lowpass Input L-Matching Network

Figure 2. 15 shows the simulation result of the matching network in terms of the input return loss plot over the desired frequency band. To compare the bandwidth performance of all the input and output matching networks, we use the fractional bandwidth defined in equation (2.41). Thus, the simulated fractional bandwidth for the input return loss result of the designed single-section input matching network, centred at a design frequency of 2.5 GHz and at -20dB threshold is 2.4 %.

$$Fractional\ bandwith = \frac{F_{high} - F_{low}}{F_0}\% \tag{2.41}$$

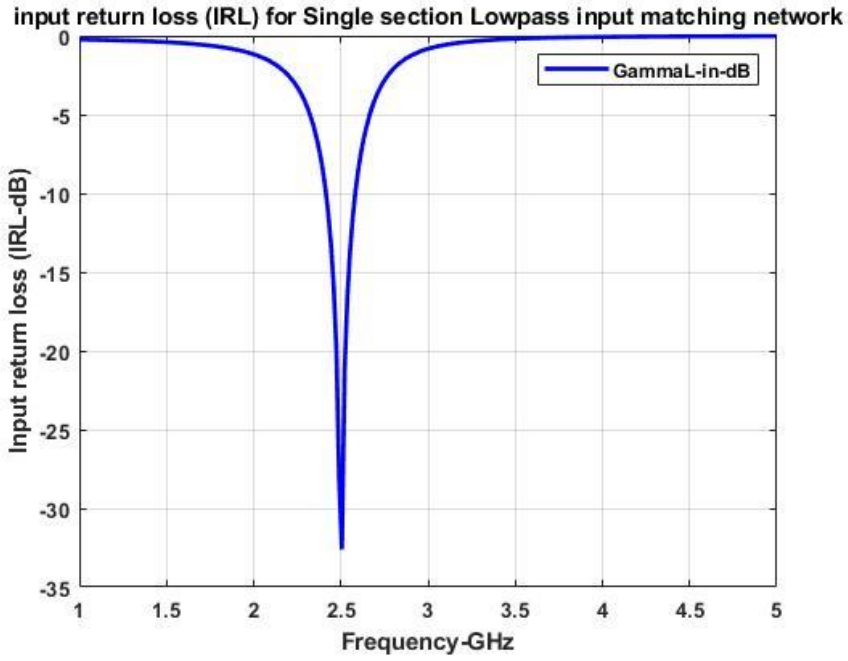


Figure 2. 15: Input return loss results for Single section lowpass input matching network (IMN)

2.5.3.2 Pi section Lowpass input matching network design

The design steps for the Pi section lowpass input matching network to the GaN transistor of Figure 2. 11 are described as follows:

Let consider the Pi section lowpass input matching network shown in Figure 2. 16 below.

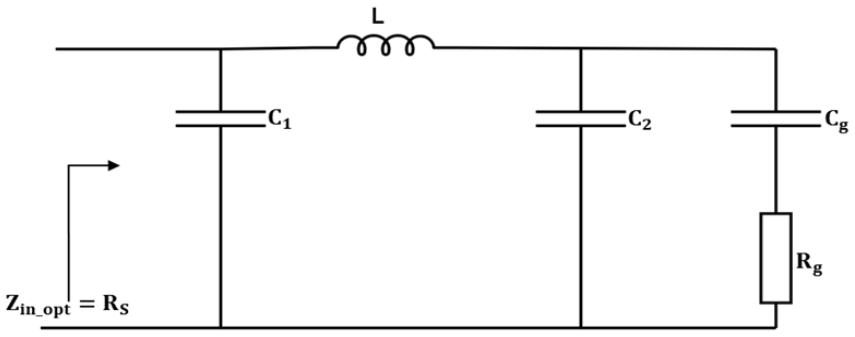


Figure 2. 16: Pi Section Lowpass Input Matching Network

The analysis of the Pi-matching network is done by first transforming the series RC load, composed of the transistor gate elements R_g and C_g, into parallel RC load at the matching frequency (ω_0) using the equations in Table 2. 1. The modified network is illustrated in Figure 2. 17.

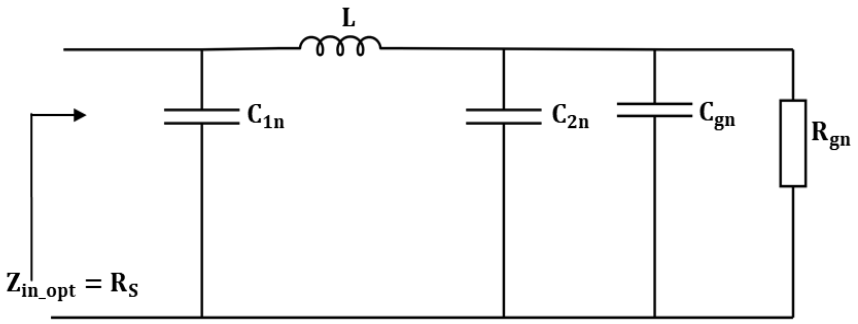


Figure 2. 17: Modified Pi Section Lowpass Input Matching Network

On the load side, the two parallel capacitors (C_{2n} and C_{gn}) are added together to form a single capacitor to simplify the analysis. To analyze the network, we first determine the network parameters without considering the gate's parasitic capacitance. The design equations for capacitors C_1 and C_2 are determined based on the matching network shown in Figure 2. 16. The input admittance equation for this matching network is expressed in the form of real and imaginary parts (see equation (2.42)).

$$Y_{in\_opt} = \frac{R_g}{{X_L}^2 + {R_g}^2((1 - X_L B_2)^2)} + j\left(B_1 + \frac{-jX_L + R_g B_2\left(R_g - R_g X_L B_2\right)}{{X_L}^2 + {R_g}^2((1 - X_L B_2)^2)}\right) \tag{2.42}$$

In this equation, the reactance terms are given as: $X_L = L.\omega$, $B_1 = C_1.\omega$, $B_2 = C_2.\omega$

For a given inductance (L) value and by equating the real and imaginary parts of the admittance (Y_{in_opt}) to $\frac{1}{R_S}$ and zero respectively at the center frequency Fo, the design equations for the susceptances B_{1o} and B_{2o} (>0) are given by:

$$B_{20} = \frac{1 + \sqrt{\frac{R_S}{R_g} - \frac{{X_{Lo}}^2}{{R_g}^2}}}{X_{Lo}} \tag{2.43}$$

$$B_{10} = \frac{X_{Lo} - {R_g}^2 B_{20}(1 - X_{Lo}B_{20})}{{X_{Lo}}^2 + {R_g}^2((1 - X_{Lo}B_{20})^2)} = \frac{X_{Lo} - {R_g}^2 B_{20}(1 - X_{Lo}B_{20})}{R_S . R_g} \tag{2.44}$$

And the corresponding fixed inductive reactance X_{Lo} calculated at the design radian frequency of the network ω_o is:

$$X_{Lo} = \omega_0 . L \tag{2.45}$$

The two shunt capacitance values of the Pi network computed in terms of the derived susceptances are given by:

$$C_1 = \frac{B_{10}}{\omega_0} \tag{2.46}$$

$$C_2 = \frac{B_{20}}{\omega_0} \tag{2.47}$$

When the gate parasitic capacitance of the network is taken into consideration; then the design equations for the network parameters of the modified Pi-section lowpass input matching network of Figure 2. 17 in terms of the new gate resistance and gate capacitance values at Fo becomes:

$$B_{2on} = \frac{1 + \sqrt{\frac{R_S}{R_{gn}} - \frac{{X_{Lo}}^2}{{R_{gn}}^2}}}{X_{Lo}} \tag{2.48}$$

$$B_{1on} = \frac{X_{Lo} - {R_{gn}}^2 B_{2on}(1 - X_{Lo} B_{2on})}{{X_{Lo}}^2 + {R_{gn}}^2((1 - X_{Lo}.B_{2on})^2)} \tag{2.49}$$

Then, the new capacitance C_{2n} at the load side of Figure 2. 17 is given by the following equation:

$$C_{2n} = \frac{B_{2on}}{\omega_0} - C_{gn} \tag{2.50}$$

While the new capacitor value at the source side is:

$$C_{1n} = \frac{B_{1on}}{\omega_0} \tag{2.51}$$

From the above equations, a sweep of the L values can be done to evaluate the matching performances with the calculated C1 and C2 elements. The maximum value of L is calculated from equation (2.48) as follows:

$${X_{Lo}}^2 \left({B_{2n}}^2 + \frac{1}{{R_{gn}}^2} \right) - 2 X_{Lo} B_{2n} + \left(1 - \frac{R_S}{R_{gn}} \right) = 0 \tag{2.52}$$

The solution to equation (2.52) yields the following equation:

$$X_{Lo} = \frac{B_{2n} + \frac{1}{R_{gn}}\sqrt{{B_{2n}}^2 R_S R_{gn} - 1 + \frac{R_S}{R_{gn}}}}{{B_{2n}}^2 + \frac{1}{{R_{gn}}^2}} = L.\omega_0 \tag{2.53}$$

Thus, the maximum value of $X_{Lo} = L_{max}.\omega_o$ is achieved when B_{2n} is minimum. Where B_{2n} is the total susceptance of the parallel combination of capacitors C_{2n} and Cgn of Figure 2. 17. And the minimum susceptance value at which the maximum inductance (L_{max}) is achieved, is $B_{2min} = C_{gn}.\omega_0$.

To validate this, a plot of the calculated capacitance values of equations (2.50) and (2.51) was carried out over a range of inductance values of $L_{min} = \frac{L_{max}}{4}$ to L_{max}.

As depicted from the results shown in Figure 2. 18 and Figure 2. 19 below, the optimum value of the inductance that will guarantee good matching around the desired bandwidth is $L = L_{max} = 1.15\,nH$. This optimum inductance value is achieved at a point where the two capacitors are minimum. Therefore, the corresponding maximum fractional bandwidth value at the -20dB limit at which this maximum inductance value is attained, as shown in Figure 2. 19, is 2.24 %.

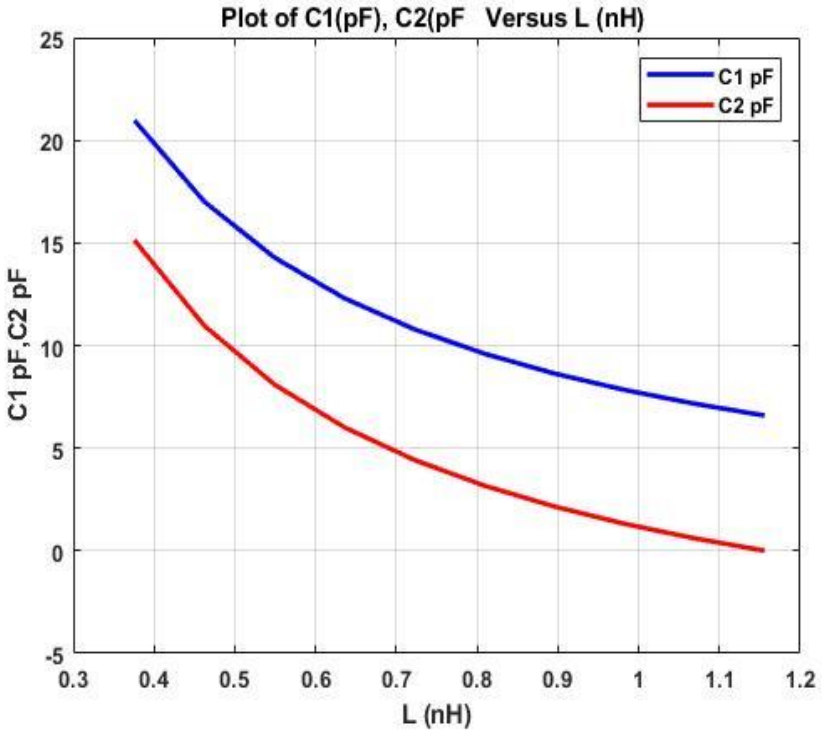


Figure 2. 18: C_1 (pF) and C_2(pF) Versus L (nH) for the Pi-section input matching network

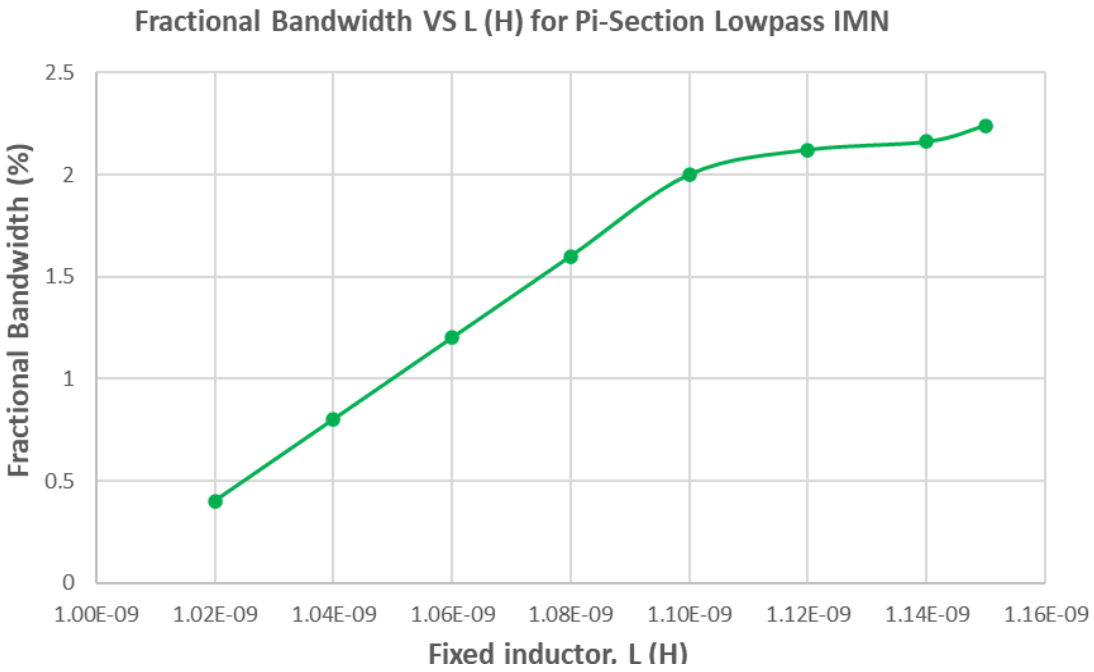


Figure 2. 19: Fractional bandwidth Versus L (nH) for the Pi-section input matching network

Table 2. 6: Derived component values for Pi section lowpass input matching network

L_{max} (nH)	C_{1n}(pF)	C_{2n}(pF)
1.15	6.59	0

Table 2. 6 shows the summary of the design parameter values for the Pi-section input matching network. It can be observed that the fixed maximum inductance value of the network is the same as that of the single-section lowpass L-matching network. The input return loss for the Pi-section lowpass input matching network is therefore similar to those presented in Figure 2. 15. This, therefore implies that the Pi section matching network does not improve the matching network bandwidth.

2.5.3.3 T- section Lowpass input matching network design

Figure 2. 20 below shows how the T-section matching network can be deployed as an input-matching network to the GaN transistor of Figure 2. 11. The equations for computing the values of the two series inductances are derived for a given value of the shunt capacitance. Thus, the design equations for the lowpass T-section input matching network are given as follows:

First, the initial expressions of the inductances denoted as L_{1o} and L_{2o} are derived from the expression of the input impedance (Z_{in}) of equation (2.54) seen at the input of the matching network when Cg is not taken into consideration.

$$Z_{in} = \frac{R_g}{(1 - B_C X_2)^2 + \left(B_C R_g\right)^2} + j\left(X_1 + \frac{\left(X_2 - B_C {X_2}^2 - B_C {R_g}^2\right)}{(1 - B_C X_2)^2 + \left(B_C R_g\right)^2}\right) \quad (2.54)$$

Where: $X_2 = L_{2o}.\,\omega$, $B_C = C.\,\omega$, $X_1 = L_{1o}.\,\omega$

The optimum value of Z_{in} is achieved by equating the real and imaginary parts of equation (2.54) to R_S and zero respectively at the center frequency Fo. Thus, the design equations for the reactances X_{1o} and X_{2o} at Fo are given as:

$$X_{2o} = \frac{1 + \sqrt{\frac{R_g}{R_S} - {B_{Co}}^2 {R_g}^2}}{B_{Co}} \quad (2.55)$$

$$X_{1o} = \frac{B_{Co}\left({X_{2o}}^2 + {R_g}^2\right) - X_{2o}}{\frac{R_g}{R_S}} \quad (2.56)$$

B_{Co} is calculated at the center radian frequency ω_o and is written as:

$$B_{Co} = \omega_0 . C \quad (2.57)$$

Consequently, the equations for computing the values of the two series inductances at a center frequency of $F_0 = 2.5$ GHz are given by:

$$L_{1o} = \frac{X_{1o}}{\omega_0} \quad (2.58)$$

$$L_{2o} = \frac{X_{2o}}{\omega_0} \quad (2.59)$$

When the parasitic gate capacitance connected in series with the inductance, L_2 as illustrated in Figure 2. 20, is considered, the new value of the inductance to compensate for the parasitic capacitance is given by:

$$L_2 = L_{2o} + \frac{1}{C_g {\omega_0}^2} \quad (2.60)$$

The Maximum value of C for the T-section input matching network is achieved when the content of the square root of equation (2.55) is greater than or equal to zero.

$$\frac{R_g}{R_S} - {B_{Co}}^2 {R_g}^2 \geq 0 \quad (2.61)$$

Further simplification of equation (2.61) yields:

$$B_{Co\_max} = \frac{1}{\sqrt{R_S . R_g}} = \omega_0 . C_{max} \tag{2.62}$$

The simulation result of Figure 2. 21 shows the plot of the two calculated inductances of equations (2.58) and (2.60) against a range of fixed capacitance values from $C_{min} = \frac{C_{max}}{4}$ to C_{max}, while Figure 2. 22 illustrates the plot of the fractional bandwidth for the input return loss result of the T-section input matching network at the -20 dB limit against the specified range of the fixed capacitance values.

It can be seen from the two graphs that the optimum value of the fixed capacitance at center frequency F_o is given as 6.71pF. Thus, at this point, the two series inductance values are at their minimum, and the maximum matching bandwidth of 2.24 % is achieved.

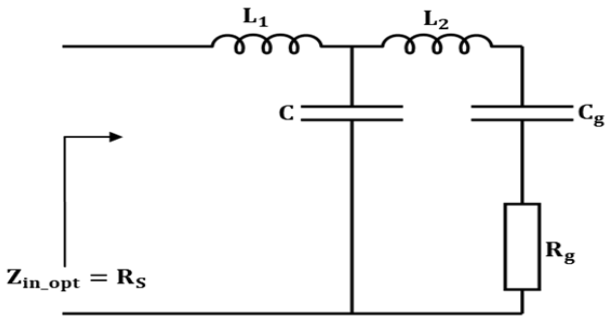


Figure 2. 20: T- Section Lowpass Input Matching Network

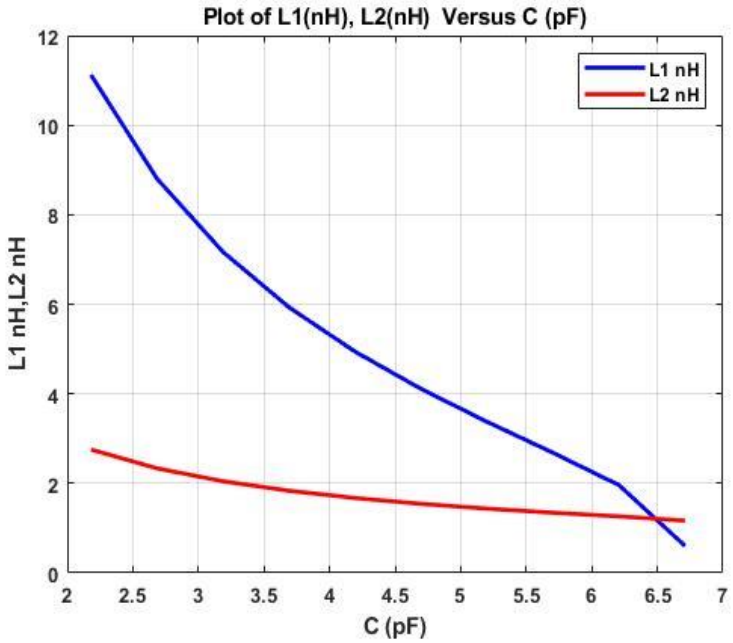


Figure 2. 21: L_1 (nH) and L_2(nH) Versus C (pF) for the T-section input matching network

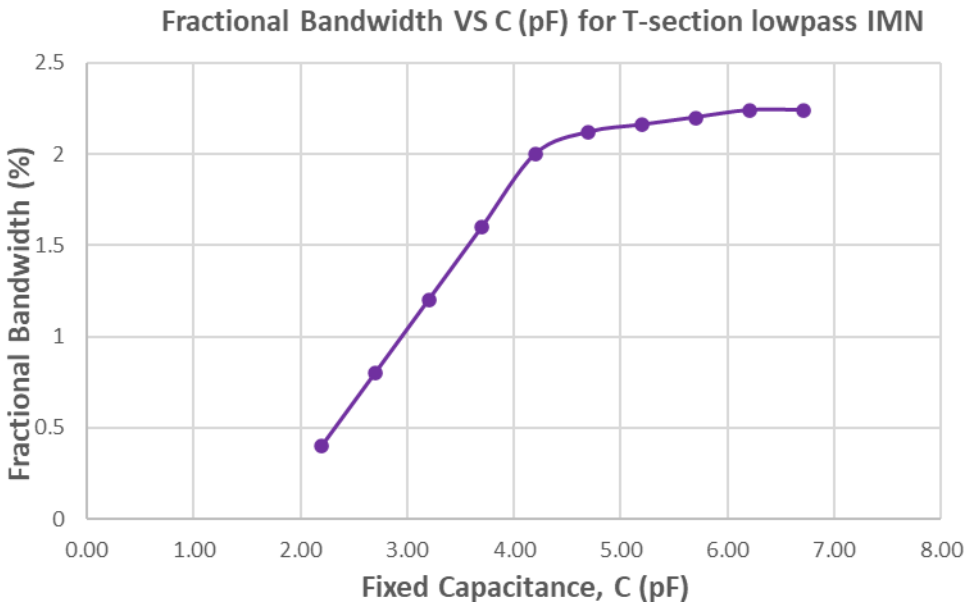


Figure 2. 22: Fractional bandwidth Versus C (pF) for the T-section input matching network

Table 2. 7 shows the summary of the matching network parameter values of Figure 2. 20 calculated at a design frequency of 2.5 GHz.

Table 2. 7: Derived component values for T- section lowpass input matching network

L_1(nH)	L_2(nH)	C (pF)
0.65	1.17	6.71

The input return loss variation with frequency of the T-section input matching network is the same as those of the designed Pi and the single-section input matching networks above. Therefore, the T-section input matching network also does not increase the matching bandwidth of the single-section input matching network.

2.5.3.4 Double section lowpass input L-matching network design

In an attempt to determine the matching network topology that will guarantee impedance match over a wider frequency band, the double section lowpass input L-matching is also being considered as an input matching network to the single-ended power amplifier shown in Figure 2. 11.

The proposed double-section lowpass input L-matching network for the power amplifier is shown in Figure 2. 23:

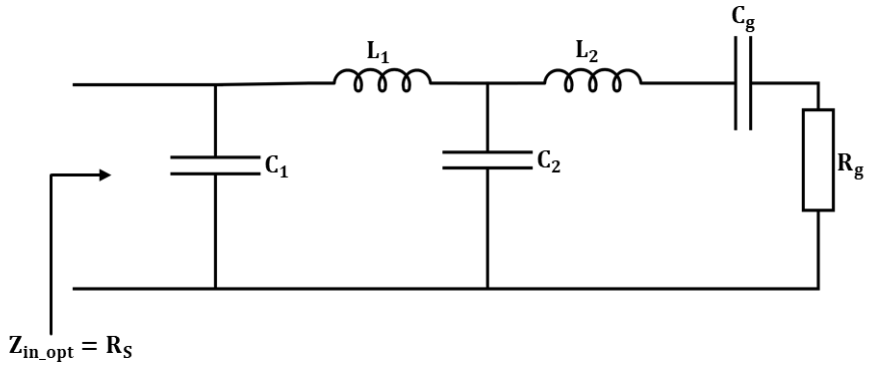


Figure 2. 23: Double section lowpass input matching network with parasitic gate capacitor (C_g)

The main goal of the proposed matching network architecture shown in Figure 2. 23 is to match the source impedance R_S to a complex gate impedance of the transistor composed of Rg in series with Cg. As such, the matching network design follows a similar procedure to that of the purely real-to-real resistive double-section lowpass impedance matching network described in Figure 2. 8 above, in which the matching network is divided into two L-sections, as illustrated in Figure 2. 24 below.

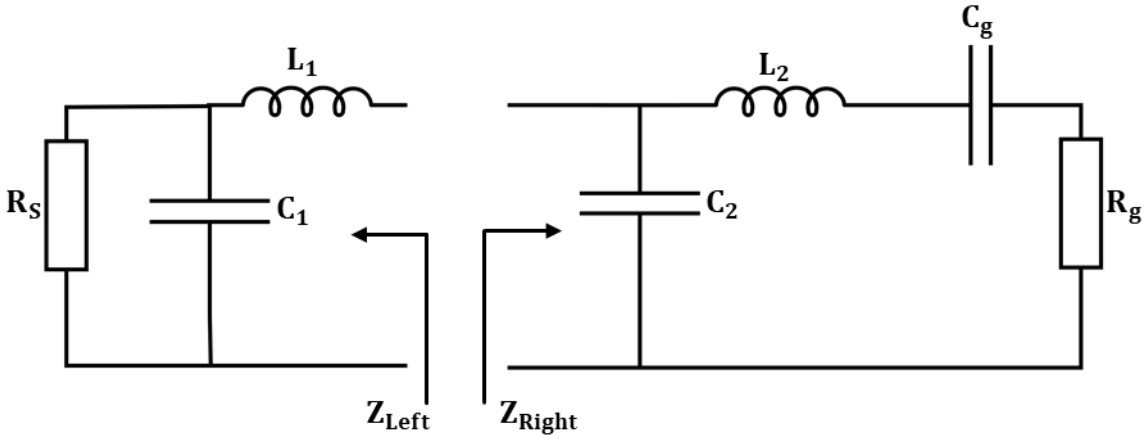


Figure 2. 24: Splitting of double-section lowpass matching network into two L-sections

The equations of the impedance seen at the left half and right half L-sections are derived at two distinct frequencies, ω_1 and ω_2, and are expressed in the form of real and imaginary parts using the following equations:

$$Z_{Left} = \frac{R_S}{1 + (R_S C_1 \omega_1)^2} + j\left(L_1\omega_1 - \frac{{R_S}^2 C_1 \omega_1}{1 + (R_S C_1 \omega_1)^2}\right) \tag{2.63}$$

$$Z_{Right} = \frac{R_g\left(1+\frac{C_2}{C_g}-C_2L_2{\omega_2}^2\right)+R_gC_2\omega_2\left(L_2\omega_2-\frac{1}{C_g\omega_2}\right)}{\left(1+\frac{C_2}{C_g}-C_2L_2{\omega_2}^2\right)^2+\left(R_gC_2\omega_2\right)^2} + j\frac{\left(L_2\omega_2-\frac{1}{C_g\omega_2}\right)\left(1+\frac{C_2}{C_g}-C_2L_2{\omega_2}^2\right)-{R_g}^2C_2\omega_2}{\left(1+\frac{C_2}{C_g}-C_2L_2{\omega_2}^2\right)^2+\left(R_gC_2\omega_2\right)^2} \quad (2.64)$$

By equating the real part of equations (2.63) and (2.64) together, we obtained the following set of polynomial equations:

$$\left(R_g-R_S\right)-\left(R_S{R_g}^2{\omega_1}^2+\frac{R_S}{{C_g}^2}\right){C_1}^2+\left(R_g{R_S}^2{\omega_1}^2\right){C_2}^2+\left(2R_S{\omega_1}^2\right)L_1C_1 - \left(R_S{\omega_1}^4\right){L_1}^2{C_1}^2-\left(\frac{2R_S}{C_g}\right)C_1+\left(\frac{2R_S{\omega_1}^2}{C_g}\right){C_1}^2L_1=0 \quad (2.65)$$

$$\left(R_g-R_S\right)-\left(R_S{R_g}^2{\omega_2}^2+\frac{R_S}{{C_g}^2}\right){C_1}^2+\left(R_g{R_S}^2{\omega_2}^2\right){C_2}^2+\left(2R_S{\omega_2}^2\right)L_1C_1 - \left(R_S{\omega_2}^4\right){L_1}^2{C_1}^2-\left(\frac{2R_S}{C_g}\right)C_1+\left(\frac{2R_S{\omega_2}^2}{C_g}\right){C_1}^2L_1=0 \quad (2.66)$$

Furthermore, the imaginary part of the impedance (Z_{Left}) of equation (2.63) is related to the Z_{Right} of equation (2.64) according to the following equation: Imag(Z_{Left}) = - Imag (Z_{Right}). Thus, this equality results in the following set of polynomial equations:

$$\left(\frac{R_S}{R_g}\right)L_1+L_2-{R_S}^2C_2-\left(R_gR_S+\frac{R_S}{R_g{C_g}^2{\omega_1}^2}\right)C_1+\left({R_S}^2{\omega_1}^2\right)L_2{C_2}^2 - \left(\frac{R_S{\omega_1}^2}{R_g}\right){L_1}^2C_1+\left(\frac{2R_S}{R_gC_g}\right)L_1C_1-\frac{R_S}{R_gC_g{\omega_1}^2}=0 \quad (2.67)$$

$$\left(\frac{R_S}{R_g}\right)L_1+L_2-{R_S}^2C_2-\left(R_gR_S+\frac{R_S}{R_g{C_g}^2{\omega_2}^2}\right)C_1+\left({R_S}^2{\omega_2}^2\right)L_2{C_2}^2 - \left(\frac{R_S{\omega_2}^2}{R_g}\right){L_1}^2C_1+\left(\frac{2R_S}{R_gC_g}\right)L_1C_1-\frac{R_S}{R_gC_g{\omega_2}^2}=0 \quad (2.68)$$

Where, C_g=7.2 pF, R_g=1.8 Ω and R_S=50 Ω.

For any given value of ω_1 and ω_2, the solution to the system of equations (2.65) to (2.68) with four unknowns is very complicated. To find the solution, we used the MATLAB vpasolve solver for symbolic equations to find the solutions to equations (2.67) and (2.68) numerically. Thus, the "vpasolve" optimum values of the matching network of Figure 2. 23 computed at two different frequencies around the frequency band of interest are determined and are listed in Table 2. 8 below.

Table 2. 8: Lumped component values for the double section lowpass input matching network

ω_1(GHz)	ω_2(GHz)	L_1(nH)	L_2(nH)	C_1(pF)	C_2(pF)
2.3	2.7	0.73	0.73	25.2	6.69
2.41	2.61	0.69	0.72	31.6	6.53

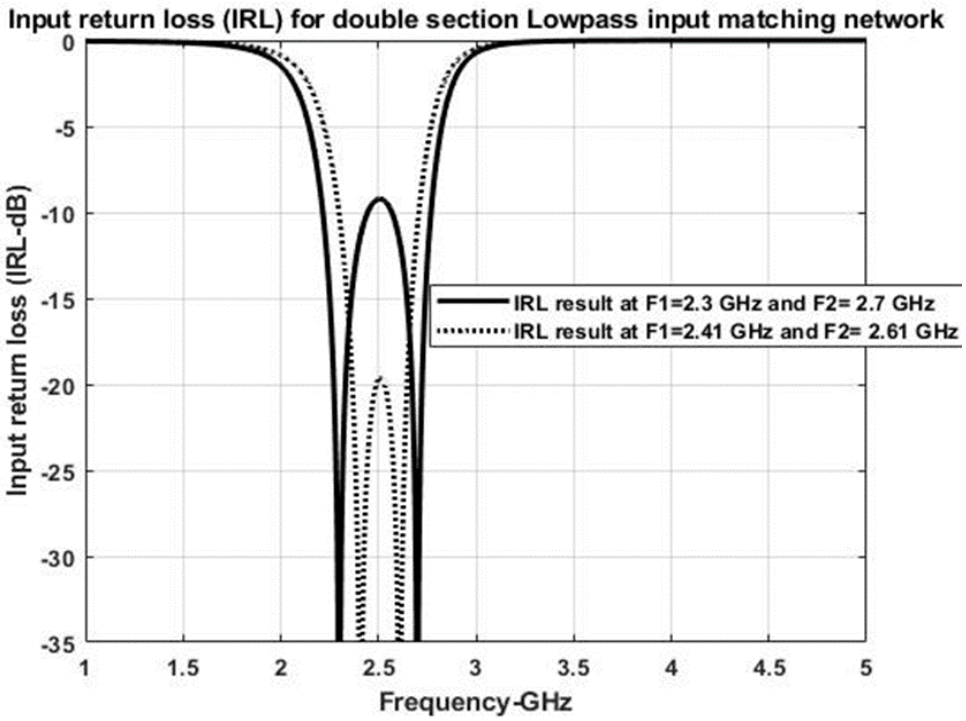


Figure 2. 25: Input return loss plot for double section Matching network

Figure 2. 25 shows the input return loss results of the double-section lowpass input matching network at two different sets of frequency points around the operating frequency of 2.5 GHz. As seen from the result, the peak value of the input return loss of the double section lowpass input matching network designed at frequency points of 2.3 GHz and 2.7 GHz is -8 dB, while the peak value of the input return loss of the matching network designed at frequency points of 2.41 GHz and 2.61 GHz is -20 dB. The fractional bandwidth of the double-section lowpass input matching network at the -20 dB return loss

threshold centred at a design frequency of 2.5 GHz is 10.8%. Furthermore, the matching network achieved a perfect matching at F1= 2.41 GHz and F2= 2.61 GHz.

2.5.4 Comparison of results for lowpass input matching networks

The comparison of the fractional bandwidth and impedance match results for all four cases of the single, Pi, T, and double section lowpass input matching networks with parasitic capacitance at the load side is shown in Figure 2. 26 and Figure 2. 27, respectively.

It can be seen from Figure 2. 26 that the computed fractional bandwidth for the double section lowpass input matching network designed at two frequency points offers a higher bandwidth performance when compared to its single, Pi, and T-section matching network counterparts. Similarly, the comparison of the Smith chart plots of the input reflection coefficient across the desired frequency band for the four input-matching networks is shown in Figure 2. 27.

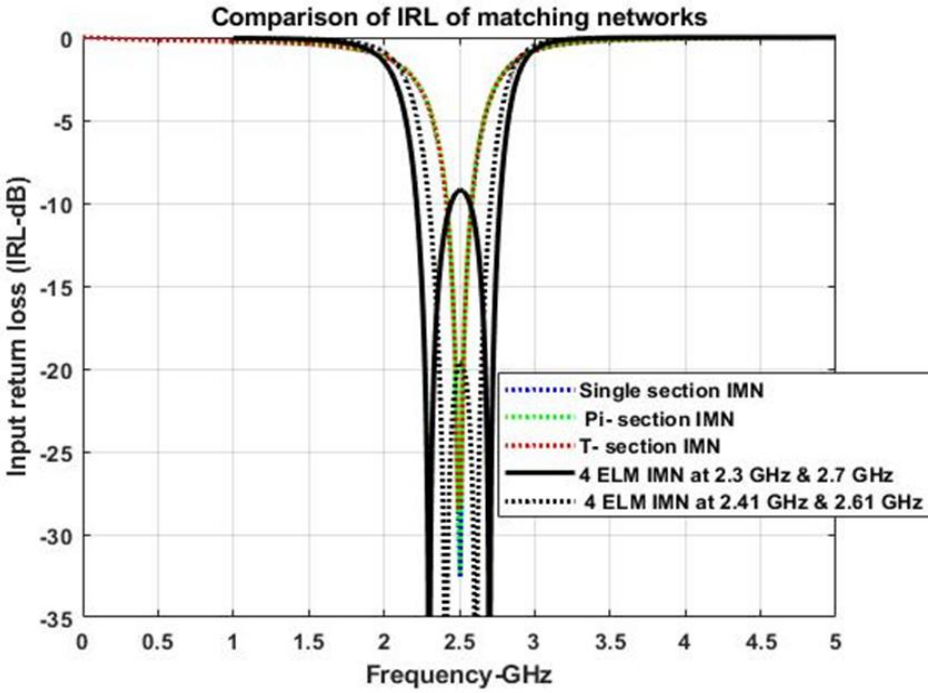


Figure 2. 26: Comparison of input return loss for the Single, Pi, T and Dual section lowpass input matching network

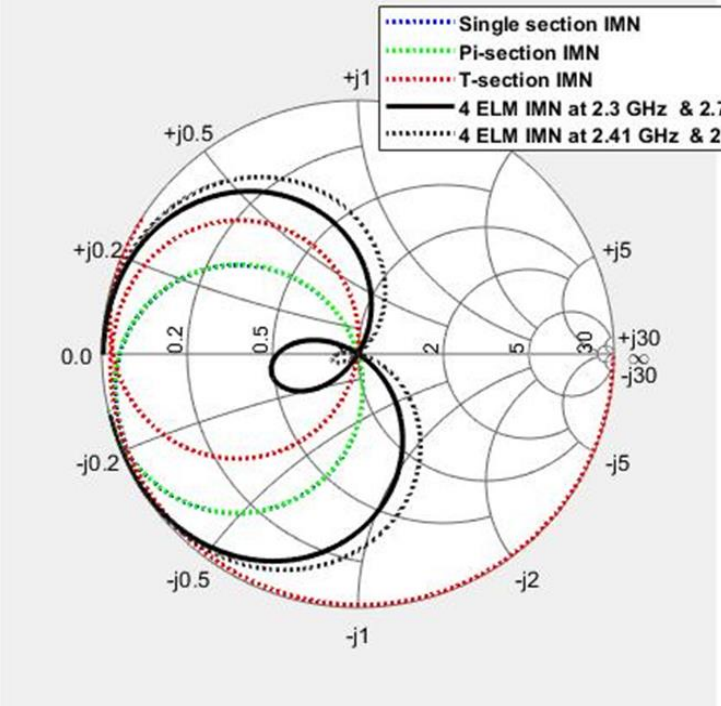


Figure 2. 27: Comparison of input reflection coefficient for the Single, Pi, T and Dual-section lowpass input matching network

2.5.5 Design of Lowpass output matching networks

The lowpass matching network types in which the source impedance is less than the load impedance are considered for design as the output matching network to the single-stage RF power amplifier shown in Figure 2. 11. The effect of the parasitic drain capacitance is considered while designing the matching network. Consequently, the following lumped element-based lowpass output matching networks are designed:

i. Single Section Lowpass output matching network
ii. Pi and T- Sections Lowpass output matching network
iii. Double Section Lowpass output matching network

2.5.5.1 Single section lowpass output matching network design

The design step for the single-section lowpass output matching network of Figure 2. 28, which comprises load resistance ($R_L = 50\Omega$), and the parasitic output drain capacitor (C_d=1.3pF) is described in this section. The optimum resistance (R_{opt}) seen at the output of the transistor is taken as the source impedance to match the network.

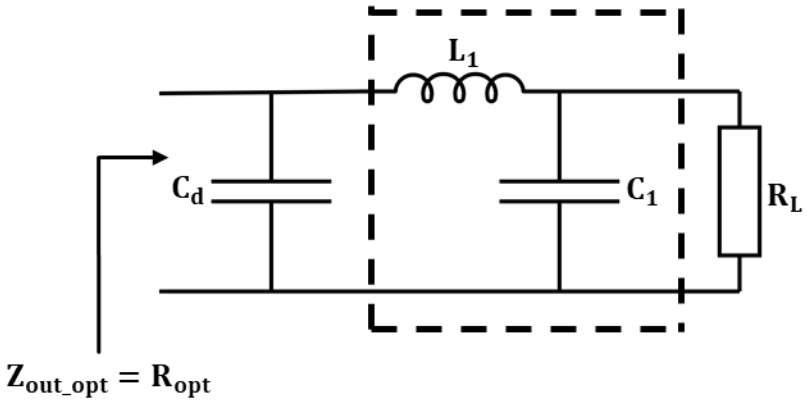


Figure 2. 28: Single Section Lowpass Output Matching Network

The equations of the type 1 network shown in Table 2. **2** above are used to calculate the initial matching network parameters consisting of a series inductance (L_{1o}) and shunt capacitance (C_{1o}) when both the source and load resistances are real. But, the network of Figure 2. 28 involves a reactive source impedance and resistive load impedance; as such, the network is modified by first transforming the parallel resistor-capacitor $(R_{opt}//C_d)$ seen at the input to the network into series to compensate for the parasitic drain capacitor (C_d) at Fo. Thus, the modified matching network is illustrated in Figure 2. 29. The equations used in calculating the new values of the transformed $R_{opt_{new}}$& C_{dnew} are given in Table 2. 1.

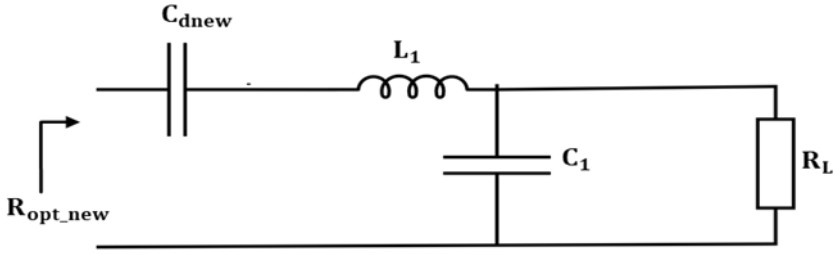


Figure 2. 29: Modified Single Section Lowpass Output Matching Network

The total series inductance value (L_1) that will compensate for the series new parasitic drain capacitance (C_{d_new}) at Fo in Figure 2. 29 is determined using the following expression:

$$L_1 = L_{1o} + \frac{1}{C_{d_{new}}.{\omega_0}^2} \tag{2.69}$$

Where, (L_{1o}) is the inductance value calculated using type 1 network equation of Table 2. 2.

Table 2. 9, therefore, gives all the network parameter values of a single-section lowpass output matching network shown in Figure 2. 28 calculated at a design frequency of 2.5 GHz. The designed matching network is simulated using MATLAB software. The output return loss result of the matching network is

shown in Figure 2. 30, and the simulated fractional bandwidth of the matching network at the -20 dB threshold and centred at a design frequency of 2.5 GHz is 24.4 %.

Table 2. 9: Network parameter values for single section lowpass output matching network

$R_{opt}(\Omega)$	$R_L(\Omega)$	$R_{opt\_new}(\Omega)$	$C_d(pF)$	$C_{d\_new}(pF)$	$L_1(nH)$	$C_1(pF)$
36	50	23.4	1.3	3.7	2.7	1.4

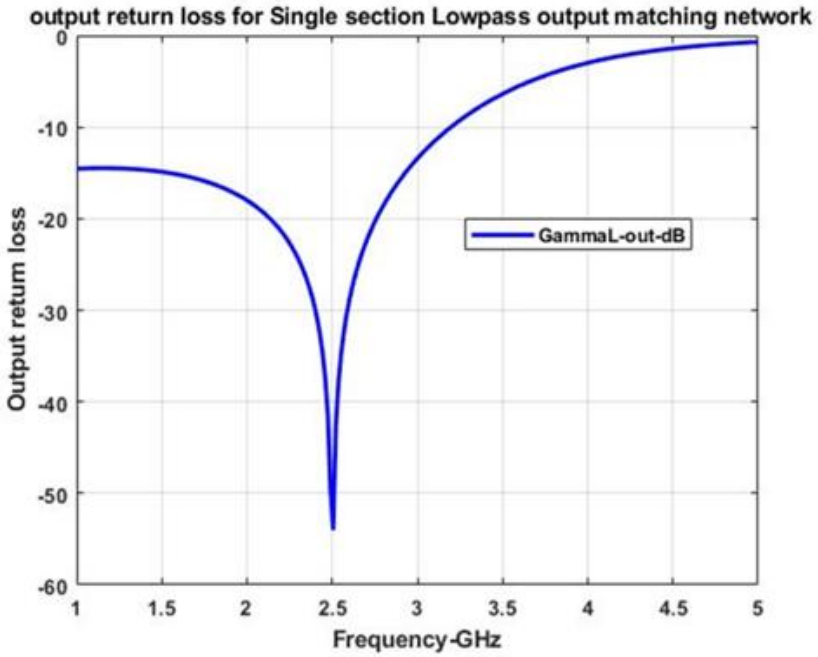


Figure 2. 30: Output return loss plot for single section matching network

2.5.5.2 Pi-section lowpass output matching network design

The design procedure for the Pi-section lowpass output matching network shown in Figure 2. 31 below is similar to that of the corresponding Pi-section input matching network described in Section 2.5.3.2 of this thesis.

Figure 2. 31 shows how the Pi-section lowpass matching network is applied as an output matching network to the GaN transistor. The design equations for this network are the same as the derived equations for the Pi section lowpass input matching network described in Section 2.5.3.2. The value of the capacitor C_2 at a design frequency, F_0 is computed from equation (2.70), where X_{Lo} is a fixed inductive reactance at ω_o. The total capacitor presented to the drain terminal of the transistor is given by ($C_T = C_d + C_1$). The initial value of the shunt capacitance C_{1o} of the network at F_0 without considering the parasitic drain capacitance (C_d) is computed from equation (2.71), while the final value

of the capacitor C_1 at the input to the matching network when C_d is considered is calculated using equation (2.72).

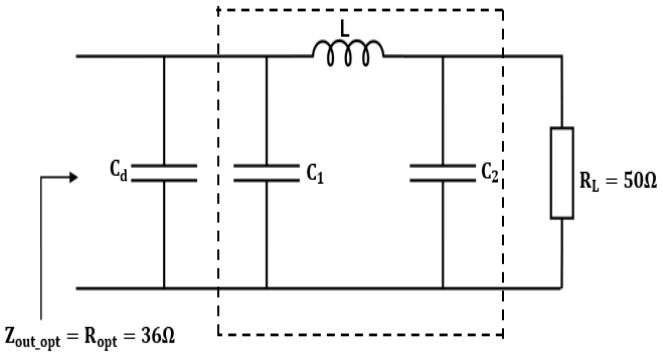


Figure 2. 31: Pi- Section Lowpass output matching network

$$B_2 = \frac{1 + \sqrt{\frac{R_{opt}}{R_L} - \frac{{X_{Lo}}^2}{{R_L}^2}}}{X_{Lo}} \tag{2.70}$$

$$B_{1o} = \frac{X_{Lo} - {R_L}^2 B_2 (1 - X_{Lo} B_2)}{{X_{Lo}}^2 + {R_L}^2 ((1 - X_{Lo} B_2)^2)} \tag{2.71}$$

$$C_1 = C_{1o} - C_d \tag{2.72}$$

From equation (2.70) an expression of the inductive reactance X_{Lo}value of the network at ω_o is derived as:

$$X_{Lo} = \frac{B_2 + \frac{1}{R_L}\sqrt{{B_2}^2 R_{opt} R_L - 1 + \frac{R_{opt}}{R_L}}}{{B_2}^2 + \frac{1}{{R_L}^2}} = L.\omega_0 \tag{2.73}$$

Furthermore, to determine the optimum inductance value L at which the maximum matching bandwidth around the frequency band of interest is attained, a plot of capacitances C_1 and C_2 values over a range of inductance values, as shown in Figure 2. 32, is carried out. The range of inductance values is sweeped between $L_{min} = \frac{L_{max}}{4}$ to L_{max}. Where L_{max} is the maximum inductance value corresponding to the minimum value of susceptance B_2 shown in equation (2.73). Using equation (2.70), the maximum value of X_{Lo} corresponds to a maximum inductance value of :

$$L_{max} = \frac{\sqrt{R_{opt}.R_L}}{\omega_0} \tag{2.74}$$

Additionally, Figure 2. 33 shows the plot of the fractional bandwidth for the output return loss of the Pi-network at a -20 dB limit against a range of the fixed inductance (L) value. From the results, the maximum matching fractional bandwidth is achieved when the optimum fixed inductance value is $L_{max} = 2.7\ nH$ and the two shunt capacitances are at their minimum values. The fractional bandwidth value under this condition is found to be 19.2 %.

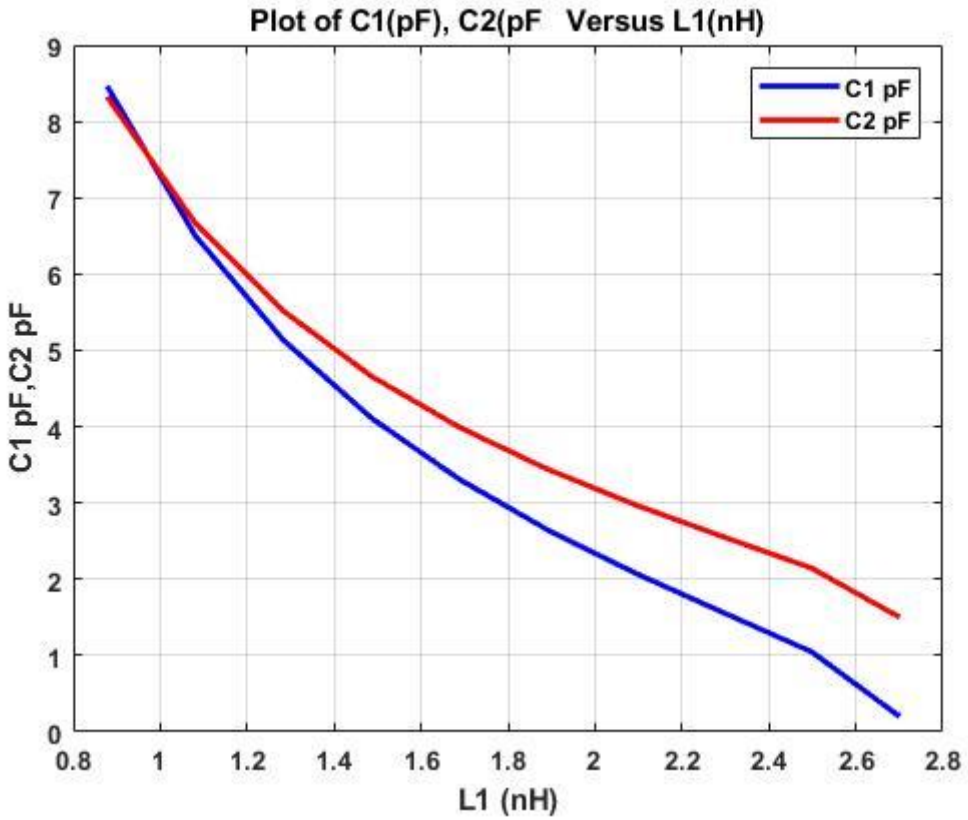


Figure 2. 32: C_1 (pF) and C_2(pF) Versus L (nH) for the Pi-section output matching network

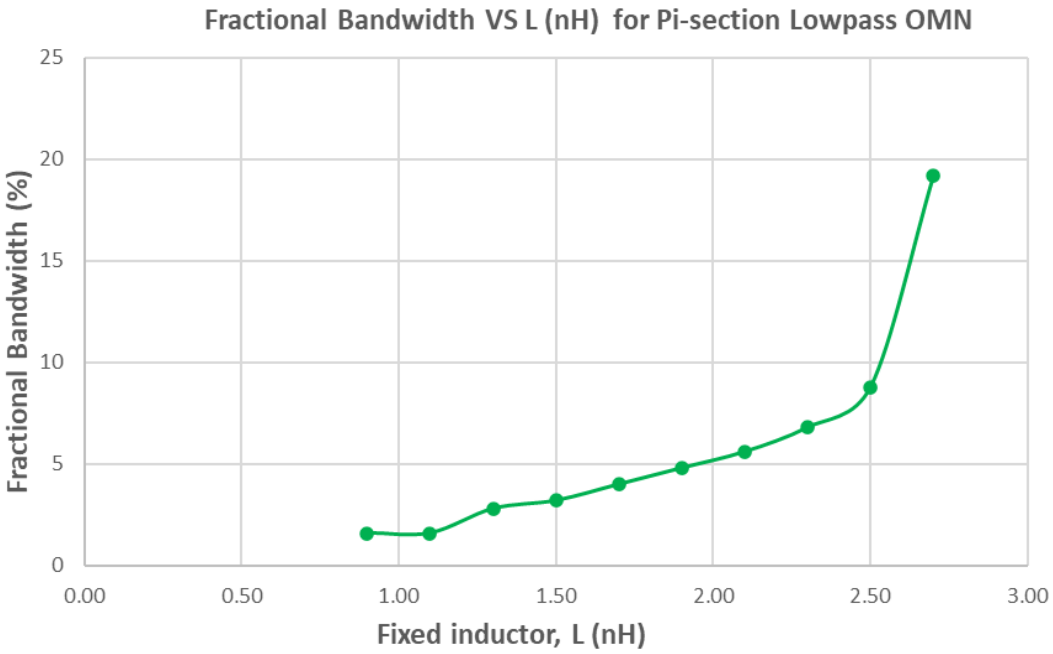


Figure 2. 33: Fractional bandwidth Versus L(nH) for the Pi-section output matching network

Table 2. 10 gives the design network parameter values for the Pi-section lowpass output matching network at an operating frequency of $F_0 = 2.5$ GHz.

Table 2. 10: Lumped elements values for the Pi-section lowpass OMN

$R_{opt}(\Omega)$	$R_L(\Omega)$	$C_d(pF)$	$L_{max}(nH)$	$C_1(pF)$	$C_2(pF)$
36	50	1.3	2.7	0.54	1.75

Similarly, Figure 2. 34 shows the optimum simulation results in the form of the output return loss plot for the network parameter values at an operating frequency of 2.5 GHz, in which the fractional bandwidth of the output return loss at the -20dB limit is 19.2%.

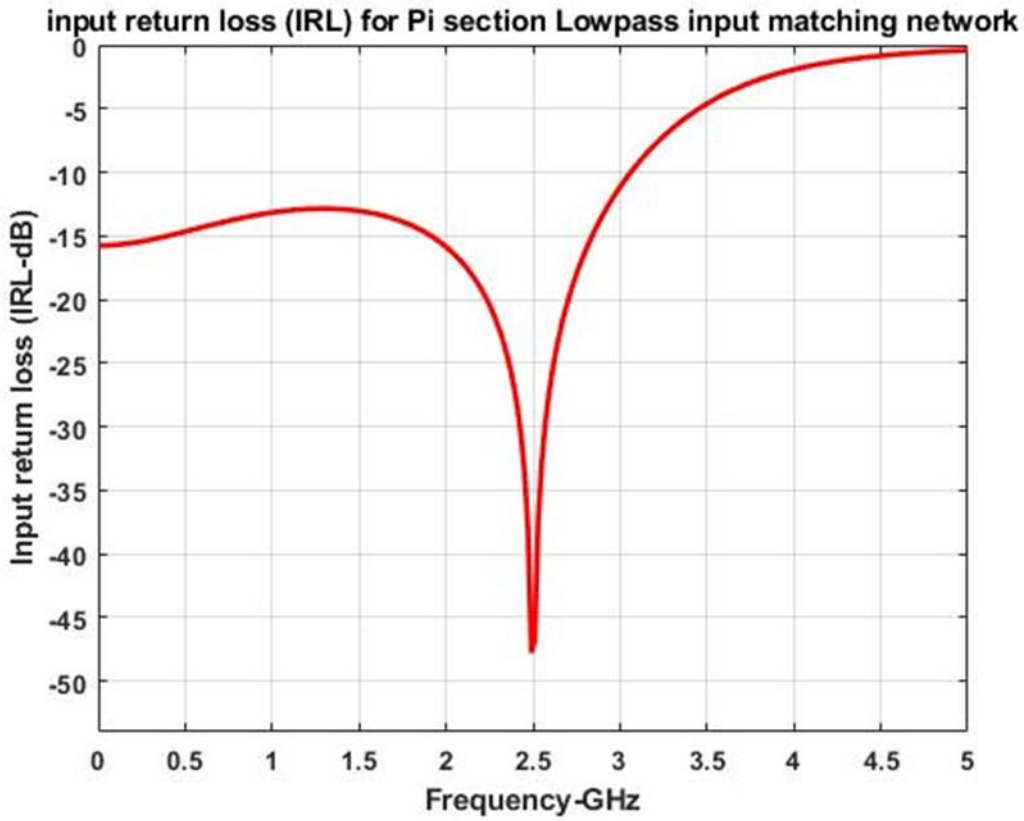


Figure 2. 34: Output return loss plot of Pi section Matching network

2.5.5.3 T- section Lowpass output matching network design

The design procedure for the T-section lowpass output matching network shown in Figure 2. 35 is similar to that of the T-section lowpass input matching network. The parallel (R_{opt} // C_d) at the input of the matching network is transformed into series ($R_{opt_{new}} C_{dnew}$) at a design frequency of 2.5 GHz using the equation of parallel-to-series R-C transformation shown in Table 2. 1. The modified T-section output matching network is illustrated in Figure 2. 36.

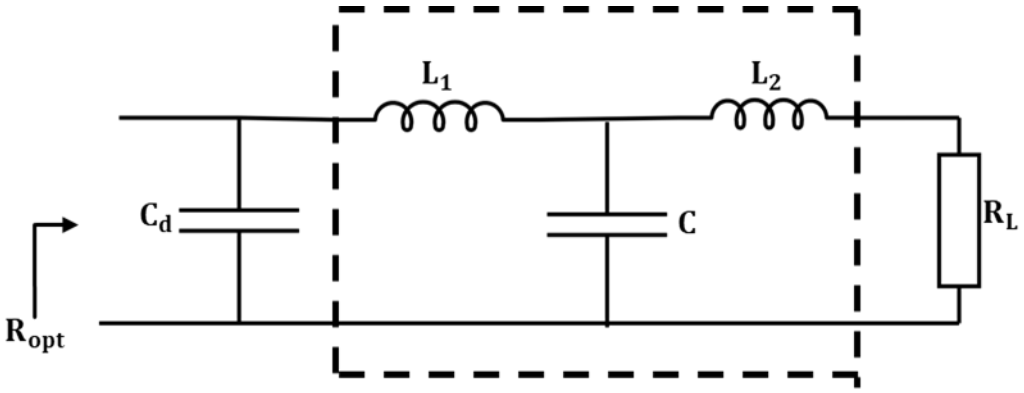


Figure 2. 35: T- Section Lowpass output Matching Network

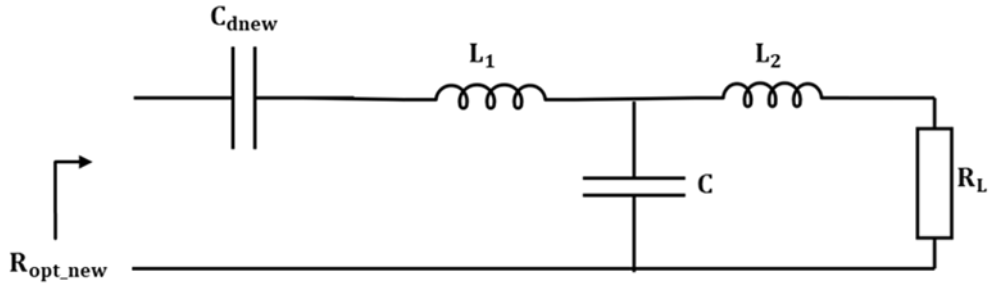


Figure 2. 36: Transformed T-Section Lowpass output Matching Network

Thus, the design equations for computing the network parameters of the T-section output matching network at an operating frequency $F_0 = 2.5$ GHz are similar to equations (2.53) and (2.54) obtained in section 2.5.3.3 by replacing R_g and R_S with R_L and R_{opt}, respectively as follows:

$$X_2 = \frac{1 + \sqrt{\frac{R_L}{R_{opt}} - {B_{Co}}^2 {R_L}^2}}{B_{Co}} \tag{2.75}$$

$$X_1 = \frac{B_{Co}\left({X_2}^2 + {R_L}^2\right) - X_2}{\frac{R_L}{R_{opt}}} \tag{2.76}$$

The initial value of inductance L_1, denoted as L_{1o}, is then computed as:

$$L_{1o} = \frac{X_1}{\omega_0} \tag{2.77}$$

The final value of the inductance L_1 to compensate for the new serie parasitic drain (C_{d_new}) capacitance of Figure 2. 36 at a center frequency of 2.5 GHz is given by:

$$L_1 = L_{1o} + \frac{1}{C_{d\_new}.{\omega_0}^2} \tag{2.78}$$

And the value for the inductance L_2 is given as:

$$L_2 = \frac{X_2}{\omega_0} \tag{2.79}$$

Furthermore, the maximum fixed capacitance (C) value of the T-section output matching network is determined by the expression given in section 2.5.3.3.

$$C_{max} = \frac{1}{\omega_0 \sqrt{R_{opt}.R_L}} \tag{2.80}$$

Figure 2. 37 and Figure 2. 38 illustrate the plot of the two calculated inductance values of equations (2.78) and (2.79) over the range of fixed capacitance values from $C_{min} = \frac{C_{max}}{4}$ to C_{max} and that of the fractional bandwidth of the output return loss of the network at a -20 dB limit against the specified range of the fixed capacitance values, respectively. The two plots authenticate that the optimum fixed capacitance value to achieve a maximum matching bandwidth of 15.2% is found to be 1.5pF. This optimum capacitance value corresponds to the point where the two series inductance of the T-section output matching network are at their minimum values.

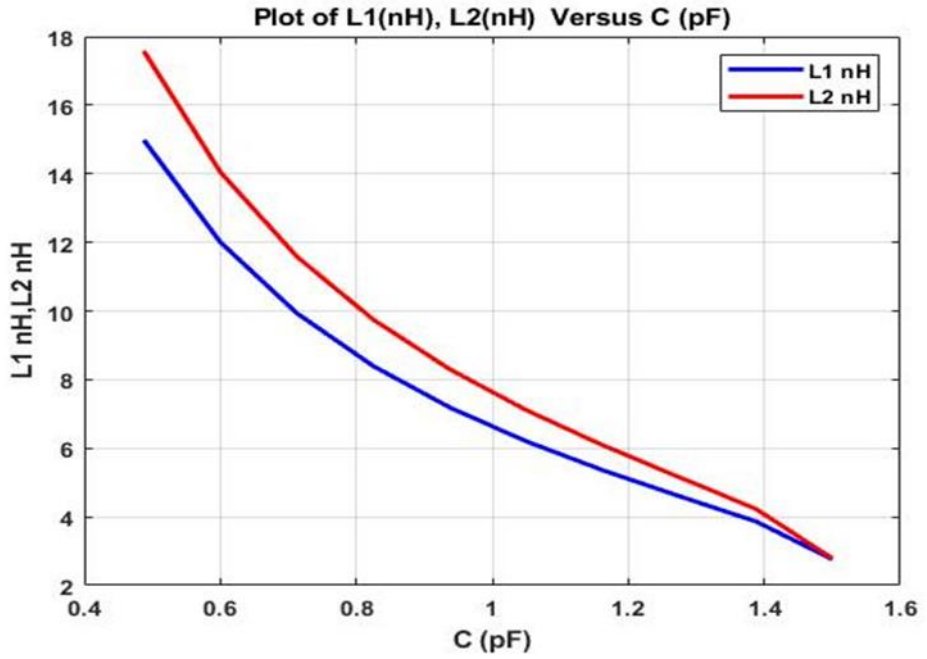


Figure 2. 37: L_1 (nH) and L_2(nH) Versus C (pF) for the T-section output matching network

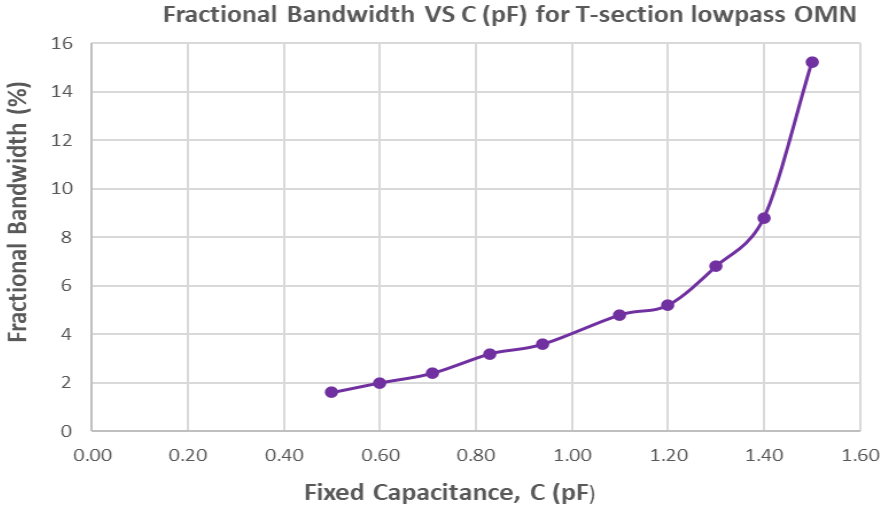


Figure 2. 38: Fractional bandwidth Versus C (pF) for the T-section output matching network

The designed network parameters for the T-section lowpass output matching network are given in Table 2. 11.

Table 2. 11: Network parameter values for T-section lowpass output matching network

$R_{opt}(\Omega)$	$R_L(\Omega)$	$C_d(pF)$	$C_{d\_new}(pF)$	$L_1(nH)$	$L_2(nH)$	C (pF)
36	50	1.3	3.7	3.86	2.79	1.5

Consequently, the output return loss result of the T-section lowpass output matching network at a -20 dB limit and centred at a design frequency of 2.5 GHz around the desired bandwidth is shown in Figure 2. 39, respectively.

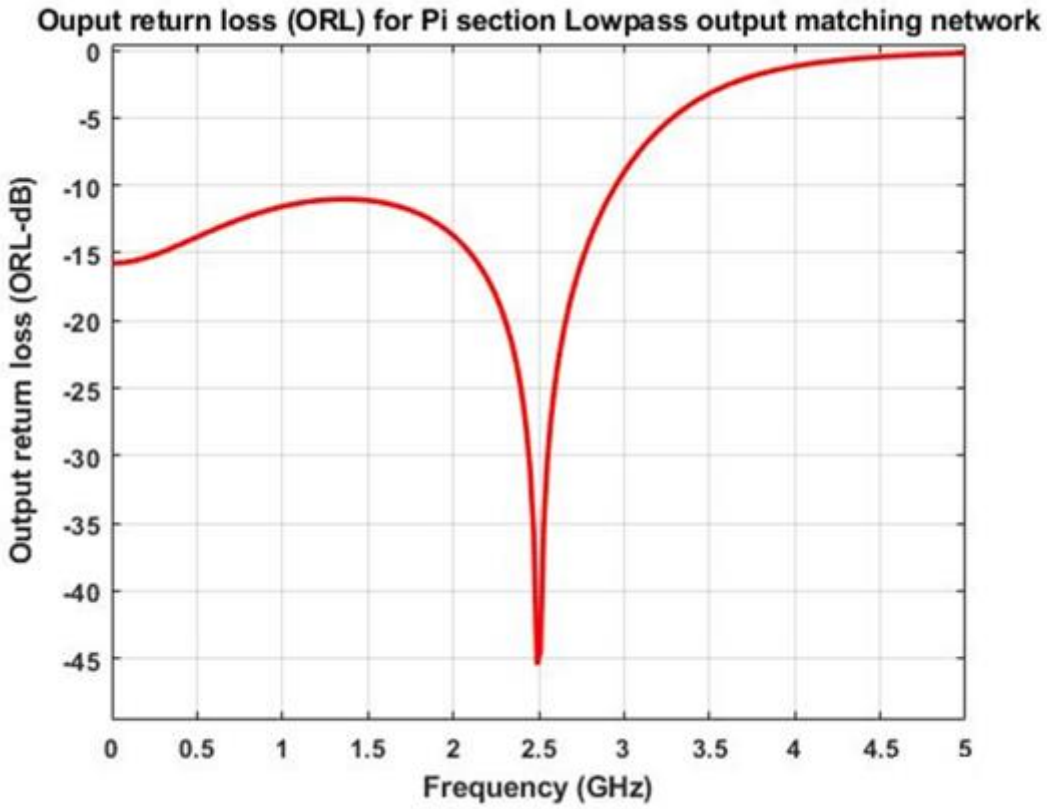


Figure 2. 39: Output return loss plot for T-section lowpass output matching network

2.5.5.4 Double section lowpass output matching network design

The design equations for the double-section lowpass output matching network consisting of two series-connected L-networks and a virtual resistor (R_V) introduced in between the L-networks, as shown in Figure 2. 40, are given in this section.

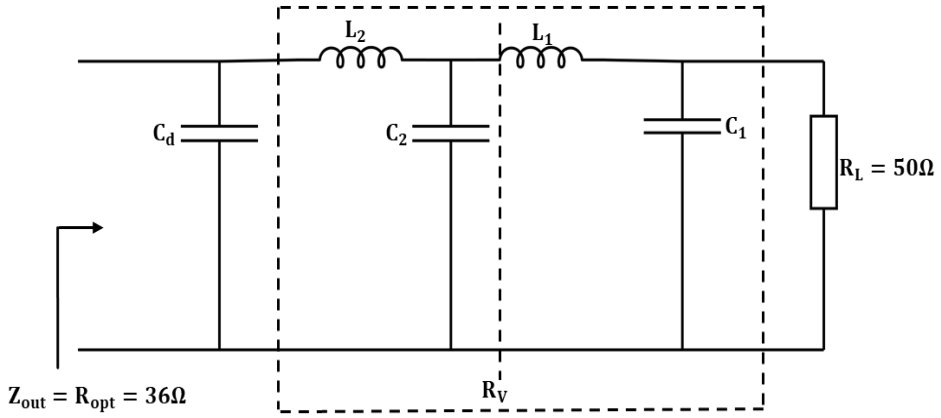


Figure 2. 40: Double section lumped element-based lowpass output matching network with parasitic drain capacitor (C_d)

The maximum bandwidth for a double-section L-matching network (without C_d, (R_V) and real of (R_{opt})) is achieved when the virtual resistor (R_V) is selected such that it is equal to the geometric mean of the two impedances to be matched. The following expression is then used [30]:

$$R_V = \sqrt{R_{opt}R_L} \tag{2.81}$$

The double-section matching network shown in Figure 2. 40 is modified by transforming the parallel connections of the optimum resistance (R_{opt}) and drain parasitic capacitance (C_d) at the input of the matching network into series. This transformation is determined using the equation for converting parallel RC to series RC networks shown in Table 2. 1. The modified double-section lowpass output matching network with the new optimum resistance (R_{opt_n}) and parasitic drain capacitance (C_{dn}) values is illustrated in Figure 2. 41 below.

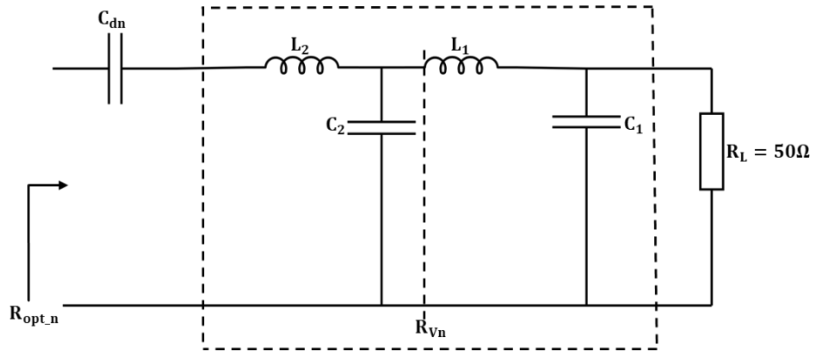


Figure 2. 41: Modified Double- Section Lowpass output Matching Network

Subsequently, the design equations for the lumped components of the modified double-section lowpass output matching network at a designed radian frequency of (ω_0) are given as follows:

$$R_{Vn} = \sqrt{R_{opt\_n} R_L} \tag{2.82}$$

$$L_1 = \frac{C_1 {R_L}^2}{1 + (C_1 \omega_0 R_L)^2} \tag{2.83}$$

$$C_1 = \frac{1}{\omega_0 R_L} \sqrt{\frac{R_L}{R_{opt\_n}} - 1} \tag{2.84}$$

$$C_2 = \frac{1}{\omega_0 R_{Vn}} \sqrt{\frac{R_{Vn}}{R_{opt\_n}} - 1} \tag{2.85}$$

$$L_{2o} = \frac{C_2 {R_{Vn}}^2}{1 + (C_2 \omega_0 R_{Vn})^2} \tag{2.86}$$

The final inductance value L_2 at the input of the matching network, which compensates for the new series parasitic drain capacitance (C_{dn}) shown in Figure 2. 41, is given by equation (2.87).

$$L_2 = L_{2o} + \frac{1}{C_{dn} {\omega_0}^2} \tag{2.87}$$

Table 2. 12 depicts the design network parameter values for the double-section lowpass output matching network shown in Figure 2. 41 at a design frequency of 2.5 GHz.

Table 2. 12: Lumped component values for the double section lowpass OMN

L_1(nH)	C_1(pF)	L_2(nH)	C_2(pF)
1.48	0.87	2.11	1.27

The output return loss plot of the matching network is shown in Figure 2. 42. The simulated fractional bandwidth of the output return loss at the -20dB limit is 24%.

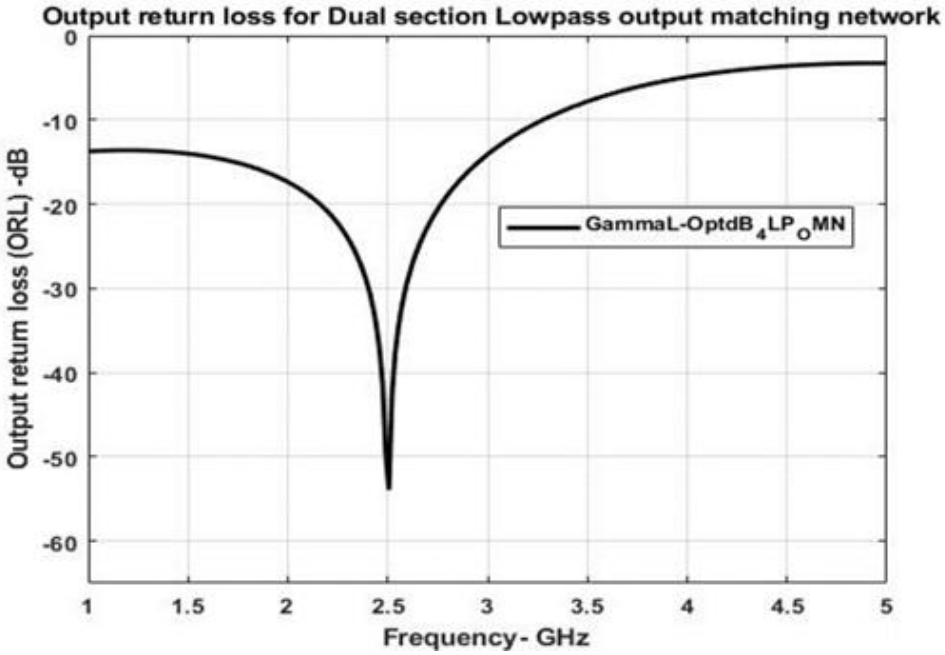


Figure 2. 42: Output return loss for Double-section lowpass output matching network (OMN)

2.5.6 Comparison of results of lowpass output matching networks

Figure 2.43 shows the comparison of the output return loss performance of the four output-matching network topologies with parallel parasitic drain capacitance and the optimum load resistance (R_{opt}) at the drain terminal of the single-stage RF amplifier in Figure 2. 11. The four network topologies are : the single-section lowpass OMN, T-section lowpass OMN, Pi-section lowpass OMN, and double-section lowpass OMN. From the results, it can be observed that the fractional bandwidth of the double-section and single-section lowpass output matching networks, at a -20 dB limit around the operating frequency of 2.5 GHz, is approximately 24%. Furthermore, the fractional bandwidth of the Pi and T-section lowpass output matching networks under the same matching condition is 19.2% and 15.2% respectively. Although the number of lumped components in the matching network has increased from two to four, the derived design equations for analyzing the matching network does not result in a significant improvement in the matching bandwidth. Therefore, in chapter three of this thesis, we will attempt to enhance these results by adjusting the component values of the double and triple-section matching networks using MATLAB optimization solvers.

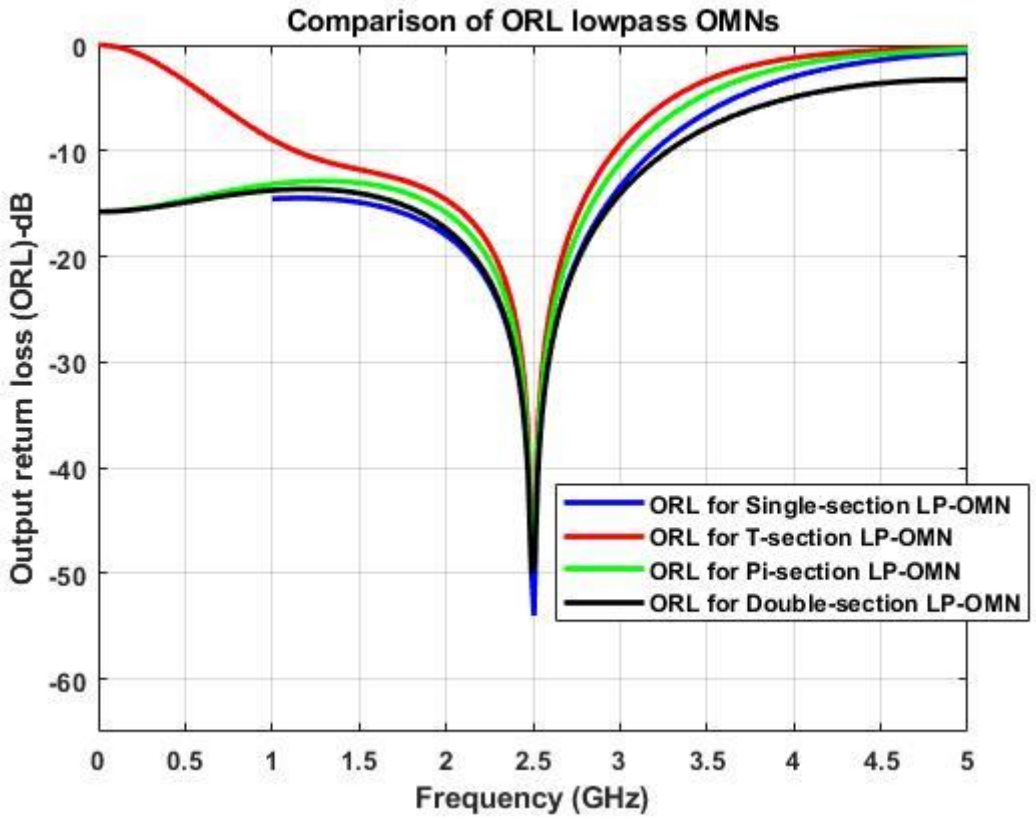


Figure 2. 43: Comparison of output return loss for the Single, T, Pi and Dual section lowpass output matching network

2.6 Conclusion

In this chapter, we presented a general overview and in-depth analysis of different topologies of lumped element-based matching networks using the analytical method. The goal is to investigate the effects of the ideal lumped components on the bandwidth of the matching networks. The given equations allow to respect matching conditions at the center frequency Fo, or at 2 frequencies in the case of bandwidth for the double-section matching network. These equations are used to design the transitor's matching networks by taking into consideration the parasitic capacitors at the gate and drain terminals of the GaN transistor. The return loss results of the designed input and output matching network configurations over a frequency band of 2.1 GHz to 2.9 GHz around a center frequency of 2.5 GHz are compared. The simulation results of the input return loss showed that the double-section lowpass input matching network has better impedance match performance and a higher fractional bandwidth of 10.8 % at a -20 dB return loss threshold. While for the case of the output matching network under the same matching condition, the output return loss results of the double and single sections lowpass output matching networks approximately present the same and higher fractional bandwidth performance of 24 % as

compared to that of the Pi- and T-sections lowpass output matching networks, which have fractional bandwidths of 19.2% and 15.2 %, respectively.

The optimum matching bandwidth for both the input and output matching networks has not been achieved when the transistor's parasitic capacitances are considered. As such, the network parameter values for the double and triple section lowpass output and input matching networks should be optimized using MATLAB optimization solvers to increase the matching bandwidth performance.

Chapter 3: Optimization methods for the design of matching circuit

3.1 Introduction

In the previous chapter, we introduced the analytical method for matching a resistive load to the resistive source impedance of a voltage source. This method involves using a limited number of lumped elements in the matching circuits. We discussed this before considering the reactive components of the load or source impedance in the network analysis.

However, when a matching network contains a complex source or load impedance with many lumped elements, it becomes extremely difficult to find an expression for these components. This makes it challenging to achieve wideband matching for the transistor. Hence the need for optimization methods for designing the impedance matching networks.

The MATLAB optimization toolbox helps minimise a given objective function while satisfying the constraint [35,36].

This chapter describes the method of optimizing the lumped elements of a matching network using the conventional optimization toolbox solvers in MATLAB software. These solvers are used to determine the optimum lumped element values of the six- and four-element lowpass input and output matching networks to the single-stage RF power amplifier of Figure 2. 11.

Subsequently, the performance of these optimized matching networks is compared in terms of the output power, power gain, and power-added efficiency of the designed single-stage RF power amplifier. The input and output matching network pairs that exhibit a wide bandwidth of RF power amplifier performances are identified and selected.

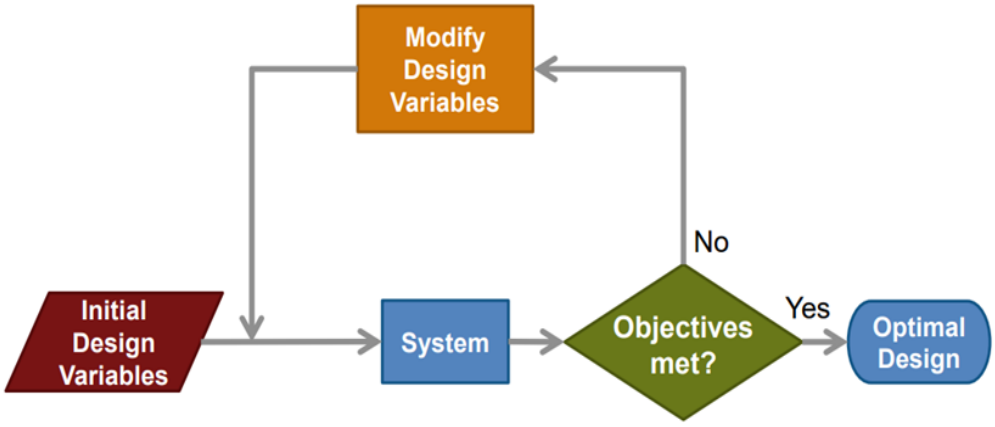


Figure 3. 1: Design optimization process [36]

3.2 Introduction to MATLAB Optimization for Impedance Matching

3.2.1 The Optimization principle

A simplified illustration of the optimization process is shown in Figure 3. 1, which serves as an introduction to optimizing the matching network. In our situation, we need to optimize the values of the lumped LC elements that make up the matching network. To achieve this, we employ matching circuit analysis and apply electrical laws to calculate the input impedance with respect to frequency. First, we can determine the initial values of the LC elements using either the analytical method explained in the previous chapter, the alternative method, or by choosing them randomly. The outcome of the system equation of an input impedance to the matching network is used to derive an expression for calculating an objective function numerically. Subsequently, a solver is employed to adjust the LC elements until the specified stopping criteria are satisfied.

3.2.2 Description of the system and objective function for impedance matching

This section focuses on defining the optimization problem for an impedance-matching network. The main goal of using the optimization solvers is to determine the optimum values of the passive components that will make the bandwidth of an RF power amplifier as wide as required.

A double-section lowpass lumped element-based input matching network for the RF power transistor consisting of reactive load impedance and resistive source impedance, as shown in Figure 3. 2, is used to describe the optimization problem.

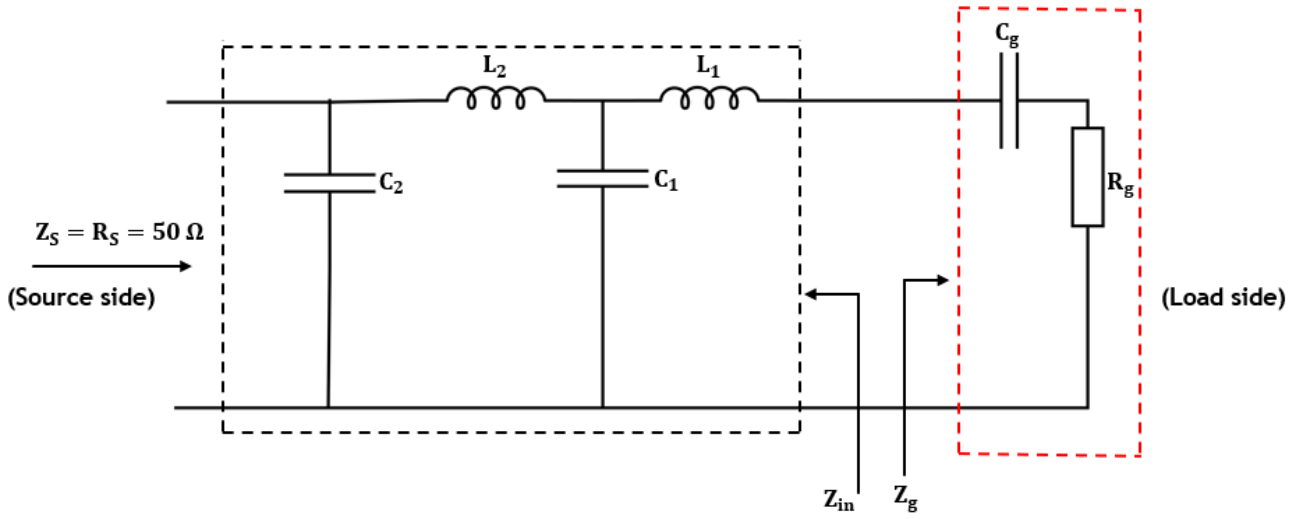


Figure 3. 2: Double section lowpass input L-matching network

The optimization problem to be used in analysing the performance of the optimization Toolbox solvers is given by the following expression:

$$Z_{in} = Z_g^{\,*} \tag{3.1}$$

Where; $Z_g = R_g - \frac{j}{C_g.\omega_n}$ is the simplified representation of the gate impedance of an RF power transistor, and Z_{in} is the optimum value of the RF amplifier input impedance seen at the output of the matching network shown in Figure 3. 2, it is expressed as:

$$Z_{in} = Z_{L1} + \cfrac{1}{Y_{C1} + \cfrac{1}{Z_{L2} + \cfrac{1}{Y_{C2} + \cfrac{1}{R_S}}}} \tag{3.2}$$

Where: $Z_{L1} = jL_1\omega$, $Y_{C1} = j.C_1.\omega$, $Z_{L2} = jL_2\omega$, $Y_{C2} = j.C_2.\omega$, $\omega = 2\pi F$

By substituting the expressions for the capacitive and inductive reactances into equation (3.2), the formula of Z_{in} now becomes:

$$Z_{in}(\omega) = jL_1\omega + \cfrac{1}{jC_1\omega + \cfrac{1}{jL_2\omega + \cfrac{1}{jC_2\omega + \cfrac{1}{R_S}}}} \tag{3.3}$$

For this application example, the gate resistance and parasitic gate capacitance of the RF transistor are given as $R_g = 1.8\,\Omega$ and $C_g = 7.2\,pF$. Therefore, the goal of the optimization solvers is to optimize C1, C2, L1, and L2 to ensure that the optimum input impedance (Z_{in}) of the transistor is equal to the complex conjugate of the transistor's gate impedance (Z_g), which also represents the load impedance of the matching network.

The mean squared error (MSE) or criterion value, denoted by E(x), is used in the optimization process to represent the objective function, and x is a vector containing the optimization variables given as:

$$x = [C1(pf);\ C2(pf);\ L_1(nH);\ L_2(nH)] \tag{3.4}$$

The MSE is calculated using the average squared difference between $Z_g^{\,*}$ and Z_{in} over a total number of N-frequency points (Nfreq_pts) in the bandwidth of interest.

$$E(x) = \frac{1}{Nfreq\_pts} \sum_{n=1}^{Nfreq\_pts} \left| Z_g^{\,*}(F_n) - Z_{in}(F_n) \right|^2 \tag{3.5}$$

3.2.3 Overview of Optimization Toolbox Solvers

There are different methods to solve optimization problems and the choice depends on description of the system, description of the objectives and constraints. Optimization Toolbox solvers in MATLAB are classified into four categories [36]:

(i) **Minimizers:** A local minimum of an objective function that is close to a given initial value X_0 can be found using solvers in this group. These solvers handle unconstrained optimization, linear, quadratic, cone and general nonlinear programming problems.

(ii) **Equation solvers**: This method is based on symbolic mathematical computation to find the expression of variables from system equations. It is therefore considered a form of optimization technique.

(iii) **Least-squares (Curve-fitting) solvers:** This group of solvers attempt to minimize the sum of squares of a function. These solvers deal with issues like fitting parameterized nonlinear models to data. They also deal with problems like finding bounded or linearly constrained solutions.

(iv) **Multiobjective minimizers:** The multi-objective minimizer solver seeks to locate a point where a set of functions is below predetermined values (fgoalattain) or to minimize the maximum value of a given function (fminimax) [36].

In the proposed application, a non-linear optimization method is required, considering the system equations and objective function. Consequently, fminunc, fminsearch, and fmincon MATLAB solvers are considered as the optimization solvers for determining the optimal lumped element values. Their properties are briefly described in the following parts.

3.2.3.1 The 'fminunc' Optimization solver:

The fminunc solver is an optimization solver used to find the minimum of an unconstrained multivariable function. It is a nonlinear programming solver specified by $\min_x f(x)$, where f(x) is a function that returns a scalar and x is a vector or matrix argument. Moreover, the term unconstrained means no constraint is placed on the range of x values.

The quasi-Newton and Trust-Region algorithms are algorithms used by the fminunc optimization solver. The Quasi-Newton algorithm is the default algorithm for the fminunc solver, and the Trust-Region algorithm is only applicable when there is a need to provide the gradient information of a function.

3.2.3.2 The 'fminsearch' Optimization solver:

The fminsearch optimization solver is similar to the fminunc solver in that both are used to find the minimum of an unconstrained multivariable function. However, the fminsearch solver applied the

derivative-free method and Nelder-Mead Simplex (direct search) algorithm of Lagarias et al. [37] to minimise function. Unlike the fminunc solver, the direct search method algorithm used by the fminsearch solver does not use numerical or analytical gradients. Thus, convergence to a local minimum using a direct search algorithm is not guaranteed.

The fminsearch solver can only minimize real numbers. This, therefore, implies that the local minimum x of an objective function must either be a vector or an array of real numbers. Alternatively, the objective function can be written in the form of real and imaginary parts when it has complex values.The fminsearch solver is less efficient than the fminunc solver for problems of an order greater than two. Meanwhile, for nondifferentiable or discontinuous problems, the fminsearch solver is powerful [38].

3.2.3.3 The 'fmincon' Optimization solver:

This solver is used to find the minimum of a constrained multivariable function. It is a nonlinear programming solver used to locate the minimum of functions specified in the following form:

$\min_x f(x)$ such that: $A*x \leq b$, $Aeq*x = beq$ (Linear constraints)

$C(x) \leq 0$, $Ceq(x) = 0$ (nonlinear constraints)

$Lb \leq x \leq Ub$ (bounds)

While b and beq are vectors, A and Aeq are matrices. Functions that return vector values are given by C(x) and Ceq(x), while f(x) is a function that returns a scalar value. The fmincon optimization solver has five different algorithms: the interior point algorithm, which is the default algorithm of the fmincon solver; active-set; sequential quadratic programming (Sqp); Sqp-legacy; and trust-region-reflective algorithms. The fmincon solver is applicable when the constraint and the objective function to be minimized are continuous. In addition to this, the objective and constraint functions must be real values and not complex [39].

It is highly recommended to always start with the default algorithm (Interior-Point) when applying the fmincon solver to find the minimum of a constrained function. However, when the size of the objective function to be optimized is in the range of small and medium, the Sqp or active-set algorithm is used to obtain more speed.

3.3 Optimization of the four-element lowpass input and output matching network parameters with unconstrained and constrained solvers

This part presents the performance characteristics of the fminsearch, fminunc and fmincon optimiser functions by running an impedance-matching network program at different frequencies within the bandwidth of interest.

3.3.1 Optimization of the four-element lowpass input matching network parameters with unconstrained and constrained solvers:

The fminsearch and fminunc solvers are classified as unconstrained solvers, while the fmincon solver based on interior point, SQP, and active-set algorithms is regarded as a constrained solver.

3.3.1.1 Fminsearch solver

The fminsearch optimization solver applies the Nelder-Mead simplex method, which is a derivative-free method, to find the minimum of an unconstrained multivariable function based on the following steps:

Step1: We begin by writing the objective function given in equation (3.5) as a MATLAB M-file function. This optimization is carried out at two frequency points around the bandwidth of interest. The two frequency points are $f_1 = 2.3\ GHz$ and $f_2 = 2.7\ GHz$ in the frequency band of 2.1 GHz to 2.9 GHz.

Step 2: We invoke the fminsearch optimization routines on the objective function. The designed network parameter values of the four-element lowpass input matching network shown in Figure 2. 23 are taken as the initial lumped element values (x_0) of the optimization routines and are written in matrix form as: $x_{0=}[C_1(\text{pf});\ C_2(\text{pf});\ L_1(\text{nH});\ L_2(\text{nH})]$ = [25.2; 6.69; 0.73; 0.73]. The options structure for monitoring the fminsearch optimization process as it attempts to find the minimum of the objective function and multiple stopping criterias are added:

- Termination tolerance of x values = 1e-9
- maximum number of function evaluations allowed = 5000
- maximum number of iterations allowed = 2000.

Consequently, after 207 iterations, the fminsearch optimization routine produces the following optimum lumped element values as a solution:

$$\mathbf{x_{fminsearch}} = \begin{bmatrix} C_{1opt}(\text{pf}) \\ C_{2opt}(\text{pf}) \\ L_{1opt}(\text{nH}) \\ L_{2opt}(\text{nH}) \end{bmatrix} = \begin{bmatrix} 25.187 \\ 6.6927 \\ 0.7278 \\ 0.7312 \end{bmatrix}$$

And the function value at the solution ($x_{fminsearch}$) is returned as $fval_{fminsearch} = 5.7756e-21$. This function value represents the error value of the optimization problem specified in equation (3.5).

Figure 3. 3 shows the matching result of the optimized network parameter values in the form of input return loss.

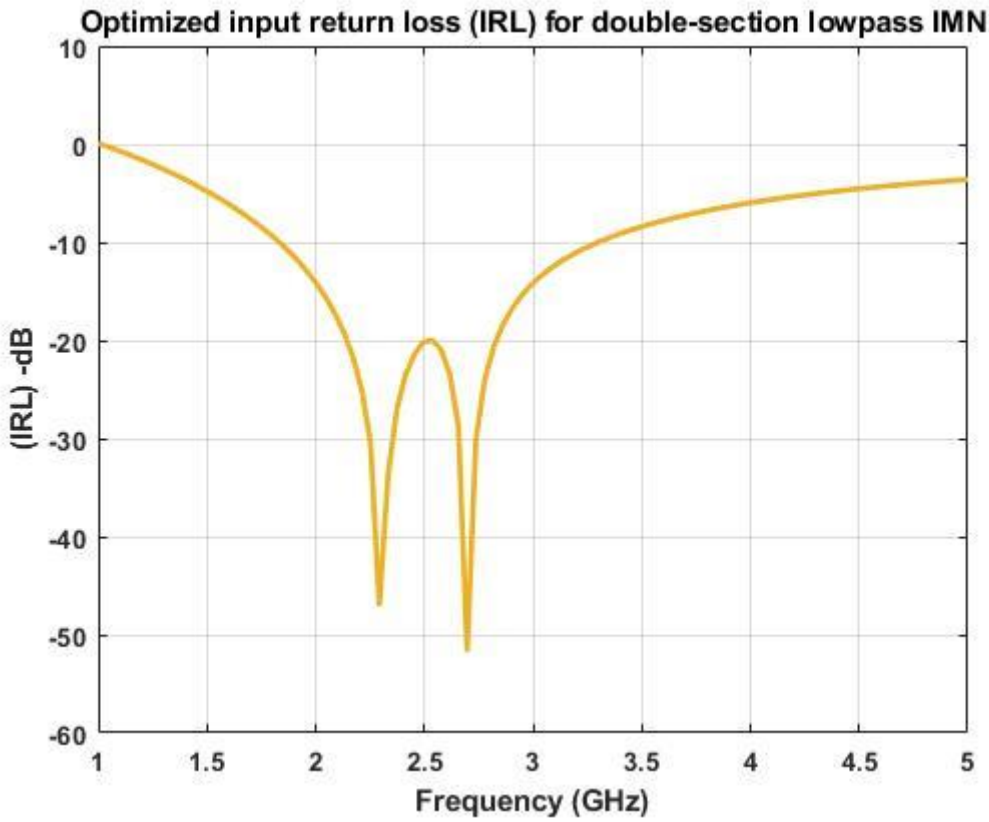


Figure 3. 3: Input return loss result for the fminsearch optimization solver being used to optimized the Four lumped element values

The result shows a better matching bandwidth with two notches in the reflection coefficient plot at 2.3 and 2.7 GHz frequencies. Although the optimized values are very close to the initial values that we got through the analytical method in Section 2.5.3.4 of this thesis, it resulted in the improvement of the matching bandwidth from 10.8% to 27.6% at a -20 dB limit and a centre frequency of 2.5 GHz around the desired bandwidth, as illustrated in Figure 3. 3.

3.3.1.2 Fminunc solver

The fminunc optimization solver follows the same strategy as the fminsearch solver in searching for the local minimum of an unconstrained multivariable objective function near the initial value x_0.

The default 'Quasi-Newton algorithm' is used, and other options are set as in the previous case. A step tolerance is added and fixed to 1e-14 to eventually stop the solver when the evolution of the objective function is very low.

The solution ($x_{fminunc}$) to the fminunc optimization solver after 29 iterations is the same as that obtained in the fminsearch solver; however, the value of the function count, which represents the calculated error of the fminunc solver, is $fval_{fminunc} = 5.0365e-13$. Thus, the input return loss result of the optimized matching network parameters using the fminunc optimizer is similar to that of the Fminsearch solver.

3.3.2 Optimization of the four-element lowpass input matching network parameters with Fmincon solvers

The fmincon solver is a constrained linear optimization used to find the constrained minimum of an objective function starting from an initial value of x0.

In this case, the lower (lb) and upper (ub) bound values of the matching network parameters (x) are defined so that the optimization solution lies between the two boundaries. Thus, the lower and upper bound values for the optimization variable are chosen as:

Lb= [0.5 pf; 0.5 pf; 0.1 nH; 0.1 nH], Ub= [55 pF; 55 pF; 3 nH; 3 nH].

Subsequently, the solution to the fmincon solver is presented using three different algorithms: (I) the interior point algorithm, which is the default algorithm for the fmincon solver; (II) the sequential quadratic programming (SQP) algorithm; and (III) the active-set algorithm. The stopping criteria for this solver are the same as in the previous cases, except that the maximum number of iterations is not fixed.

Thus, by applying (I), the interior point algorithm method, the solution ($x_{fmincon1}$) to the fmincon solver after 15 iterations is the same as that obtained in the fminsearch optimization solver and the function count value is $fval_{fmincon1} = 5.0863e-13$.

When (II), the SQP algorithm method is applied, the solution ($x_{fmincon2}$) to the fmincon optimization solver after 12 iterations is the same as that obtained in the fminsearch solver. Furthermore, the function count value for the fmincon solver with the SQP algorithm is $fval_{fmincon2} = 4.2188e-13$.

Similarly, when (III), the active-set algorithm is used, the solution ($x_{fmincon3}$) to the fmincon optimization solver after 5 iterations is the same as that obtained in the fminsearch solver but has the highest function value of $fval_{fmincon3} = 1.5674e-06$.

The solutions to the fmincon optimization solver for the three algorithms are very closed. The summary of the results of the optimizer functions indicating the criterion value and the number of iterations performed by each solver is presented in Table 3. 1.

Table 3. 1: The summary of the results of the optimization solvers with four lumped elements-based lowpass input matching network

	Fminsearch solver	Fminunc solver	Fmincon solver (Interior point algorithm)	Fmincon solver (SQP-algorithm)	Fmincon solver (Active-set algorithm)
Criterion value	5.78e-21	5.04e-13	5.09e-13	4.22e-13	1.57e-06
Number of iterations	207	29	15	12	5

It can be seen from Table 3. 1 that the criterion values of the optimization solvers are almost equal to zero, and the fmincon solver using the active-set algorithm has a better performance than the remaining solvers for having the lowest number of iterations (5).

3.3.3 Optimization of the four-element lowpass output matching network parameters with unconstrained and constrained solvers:

The analysed network parameter values of the four-element lowpass output matching network of Figure 2. 40 are optimized in the same way as they have been done with those of the four-element lowpass input matching network. Thus, the network parameter values of the analysed matching network in Figure 2. 40 are considered the initial values for the optimization solvers and are given as:

$x_0 = [C_1(\text{pf}); C_2(\text{pf}); L_1(\text{nH}); L_2(\text{nH})] = [0.87; 1.27; 1.48; 2.11]$.

Therefore, the optimized four-element lowpass output matching network parameter values for the two unconstrained solvers (fminsearch and fminunc) under the same matching conditions as the previous case are the same and are given as:

$$\mathbf{x_{fminsearch}} = \mathbf{x_{fminunc}} = \begin{bmatrix} C_{1opt}(\text{pf}) \\ C_{2opt}(\text{pf}) \\ L_{1opt}(\text{nH}) \\ L_{2opt}(\text{nH}) \end{bmatrix} = \begin{bmatrix} 2.4815 \\ 1.1719 \\ 2.599 \\ 3.0622 \end{bmatrix}$$

Similarly, the constrained fmincon solver optimum network parameters at three different algorithms give the same optimum values as:

$$\mathbf{x}_{\mathbf{fmincon\ (for\ all\ the\ 3\ algorithms)}} = \begin{bmatrix} C_{1opt}(\text{pf}) \\ C_{2opt}(\text{pf}) \\ L_{1opt}(\text{nH}) \\ L_{2opt}(\text{nH}) \end{bmatrix} = \begin{bmatrix} 2.483 \\ 1.1777 \\ 2.5481 \\ 3 \end{bmatrix}$$

The optimized matching network parameter values of the constrained and unconstrained optimization solvers are approximately the same. Thus, the fractional bandwidth of the resulting optimized output return loss result shown in Figure 3. 4 for the double-section lowpass output matching network at a -20 dB threshold and centred at a design frequency of 2.5 GHz around the desired bandwidth has increased from the initial 24.4% to 52%.

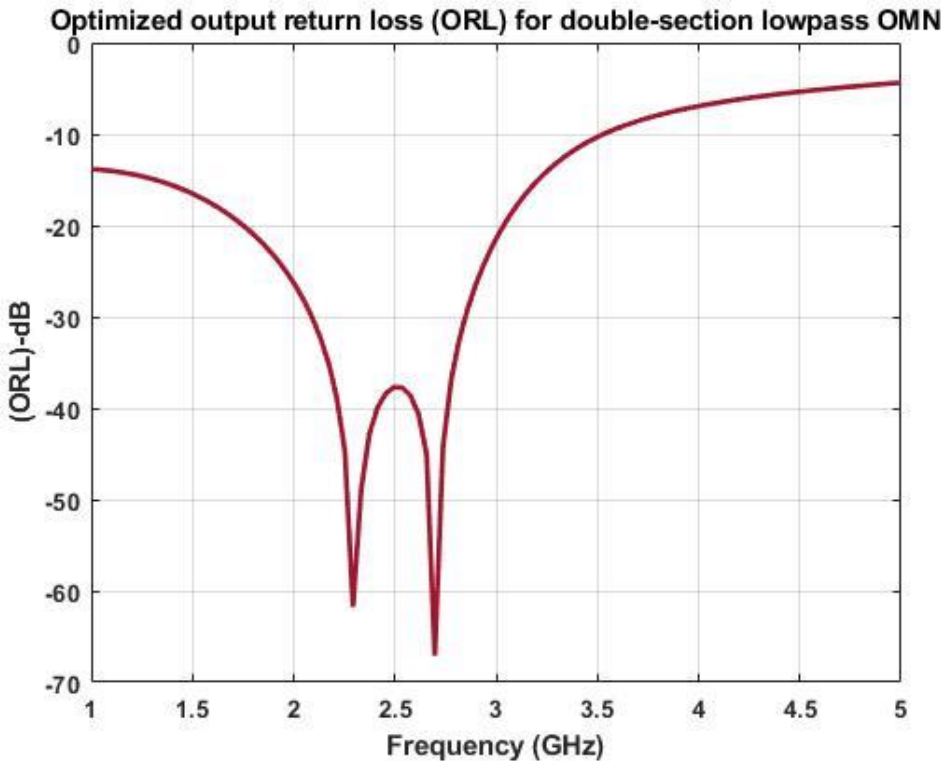


Figure 3. 4: Output return loss result of the optimized 4 elements output matching network by all the five optimization solvers.

Table 3. 2 summarises the results for all the optimization solvers' performance based on the number of iterations and criterion values.

Table 3. 2: The summary of results of the optimization solvers with a four lumped elements-based lowpass output matching network

	Fminsearch solver	Fminunc solver	Fmincon solver (Interior point algorithm)	Fmincon solver (SQP-algorithm)	Fmincon solver (Active-set algorithm)
Criterion value	1.54e-17	7.76e-10	0.2104	0.2104	0.2104
Number of iterations	475	63	51	28	28

It can be seen from Table 3. 2 that the criterion values for the unconstrained solvers (fminsearch and fminunc) are equal to zero; this, therefore, denotes a perfect impedance match of the solver's optimization variables, but the two unconstrained solvers have the disadvantage of having a higher number of iterations. Furthermore, the criterion values for the constrained solver at three different algorithms are equal and close to zero. Therefore, the fmincon solver with SQP and active-set algorithms has the lowest number of iterations (28), while the number of iterations for the fmincon solver with interior point algorithm is 51. Consequently, the fmincon solver using SQP and active-set algorithms offers a good compromise between having a criterion value close to zero and the lowest number of iterations.

3.4 Optimization of the six-element lowpass input and output matching network parameters with unconstrained and constrained solvers

In the quest to further improve the matching bandwidth beyond what is obtained with the four-element lowpass input and output matching networks, the six-element lowpass input and output matching network parameters are also considered for optimization in this section. The network parameters of the six-element lowpass input matching network to the RF power amplifier of Figure 2. 11 are first designed using the analytical method. Then, the calculated network parameter values are optimized using MATLAB optimization solvers.

3.4.1 Optimization of six-element lowpass input matching network parameters with unconstrained and constrained solver

3.4.1.1 Selection of initial values for lowpass six-element input matching network using the analytical method

Let us consider the six-element (triple-section) lowpass input matching network consisting of two virtual resistors between the source and load resistances shown in Figure 3. 5 below.

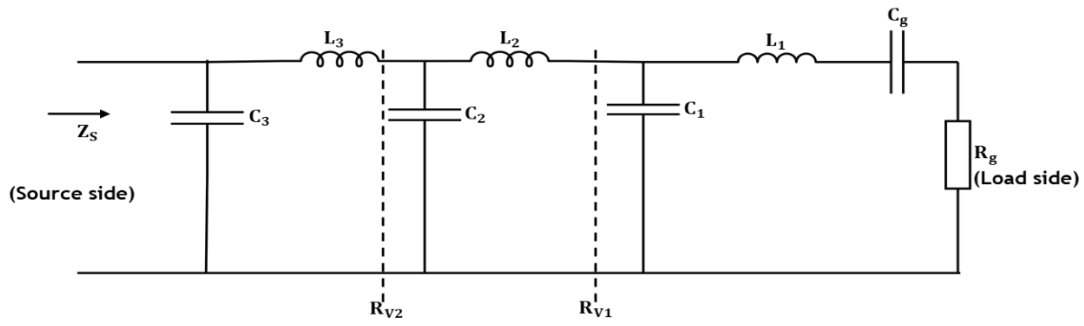


Figure 3. 5: Triple section lowpass input L-matching network with virtual resistors

To match any resistive impedances between the source and load sides of a multi-section L-matching network shown in Figure 3. 5, the optimum matching bandwidth of the network is attained when the ratio of the two succeeding virtual resistances is equal [30].

In our case, we need to consider the gate capacitance Cg at the transistor input. The method we propose to find the initial values is to use the virtual resistance approach, thereby compensating for the effect of the series capacitance Cg on the inductance L1.

The ratios of the successive virtual resistances for the n-section matching network are written as:

$$\frac{R_{V1}}{R_{Smaller}} = \frac{R_{V2}}{R_{V1}} = \cdots\cdots \frac{R_{Larger}}{R_{Vn-1}} \tag{3.6}$$

Where, $R_{Smaller}$ and R_{Larger} are the smallest and largest values of the terminating impedances of the network, respectively. In addition to this, the virtual resistances $R_{V1}\ to\ R_{Vn-1}$ lie between the two-terminating impedances.

For the matching network of Figure 3. 5, the expressions of the virtual resistances are given as:

$$R_{V1} = \frac{(R_S R_g)}{R_{V2}} \tag{3.7}$$

$$R_{V2} = \sqrt[3]{R_S{}^2 R_g} \tag{3.8}$$

Thus, the expression for the matching network parameters at a center frequency $f_0 = 2.5\ GHz$ is given as follows:

We start by giving an expression for computing the initial value of the inductance L1 of Figure 3. 5 without considering the gate capacitance Cg:

$$L_{1o} = \frac{1}{\omega_0}\sqrt{R_g R_{V1} - {R_g}^2} \tag{3.9}$$

Then, the L_1 value to compensate for the series capacitance C_g is given in equation (3.10):

$$L_1 = L_{1o} + \frac{1}{C_g {\omega_0}^2} \tag{3.10}$$

The expressions for the remaining matching network parameters are written as follows:

$$C_1 = \frac{L_{1o}}{R_g R_{V1}} \tag{3.11}$$

$$L_2 = \frac{1}{\omega_0}\sqrt{R_{V1} R_{V2} - {R_{V1}}^2} \tag{3.12}$$

$$C_2 = \frac{L_2}{R_{V1} R_{V2}} \tag{3.13}$$

$$L_3 = \frac{1}{\omega_0}\sqrt{R_{V2} R_S - {R_{V2}}^2} \tag{3.14}$$

$$C_3 = \frac{L_3}{R_{V2} R_S} \tag{3.15}$$

Table 3. 3 shows the initial lumped element values for the six-element (triple-section) lowpass input matching network of Figure 3. 5 with $Z_S = R_S = 50\Omega$, $R_g = 1.8\Omega$, and $C_g = 7.2$pf.

Table 3. 3: Initial lumped element values for triple section lowpass IMN

$C_1(pf)$	$C_2(pf)$	$C_3(pf)$	$L_1(nH)$	$L_2(nH)$	$L_3(nH)$
16.63	5.492	1.813	0.726	0.494	1.497

The input return loss result of the matching network computed with the initial lumped element values is illustrated in Figure 3. 6.

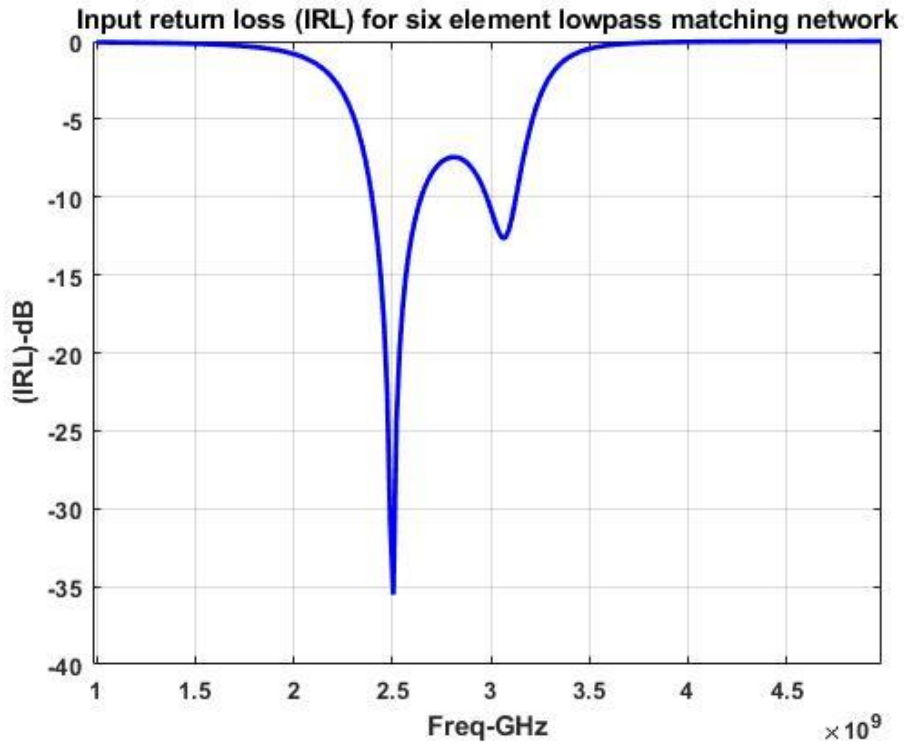


Figure 3. 6: Initial results of the input return loss for a triple section lowpass lumped element-based input matching network (IMN)

It can be observed from Figure 3. 6 that the optimum bandwidth of the network has not been achieved due to the variation of the transistor's gate impedance Z_g with its parasitic capacitance Cg. To improve the bandwidth of the matching network, the above initial lumped element values of Table 3. 3 are optimized using MATLAB optimization solvers.

3.4.2 Optimization results of six-element lowpass input matching network parameters

The procedure for optimizing the initial values of the six-element lowpass input matching network of Figure 3. 5 is similar to that of the four-element lowpass matching network. But, in this case, the optimization is carried out at three frequency points around the bandwidth of interest. The frequency points are: $f_1 = 2.25\ GHz$, $f_2 = 2.62\ GHz$, and $f_3 = 2.95\ GHz$.

The initial lumped element values given in Table 3. 3 above are taken as the initial values (x_0) of the optimization routine and are written in matrix form as:

x_0=[C_1(pf); C_2(pf); C_3(pf); L_1(nH); L_2(nH);L_3(nH)]=[16.633;5.4920;1.8134;0.7261;0.4943; 1.4970].

The fmincon solver lower (Lb) and upper (Ub) bound values of the six-element lowpass input matching network parameters are defined so that the optimization solution lies between the two boundaries.

Thus, the lower and upper bound values of the optimization variable are chosen as:

Lb = [1pf; 1pf; 1pf; 0.1nH; 0.1nH; 0.1nH], Ub = [55pF; 55pF; 55pF; 3nH; 3nH; 3nH].

The optimized network parameter values for the two unconstrained solvers (fminsearch and fminunc) and all the three fmincon solver algorithms under the same matching conditions as the previous case with a four-element matching network are approximately the same and are given as:

$$\mathbf{x_{optimised}} = \begin{bmatrix} C_{1opt}(pf) \\ C_{2opt}(pf) \\ C_{3opt}(pf) \\ L_{1cg\_opt}(nH) \\ L_{2opt}(nH) \\ L_{3opt}(nH) \end{bmatrix} = \begin{bmatrix} 59.682 \\ 58.2531 \\ 6.1483 \\ 0.511 \\ 0.5806 \\ 0.1247 \end{bmatrix}$$

Figure 3. 7 shows the matching result of the optimized network parameter values in the form of input return loss.

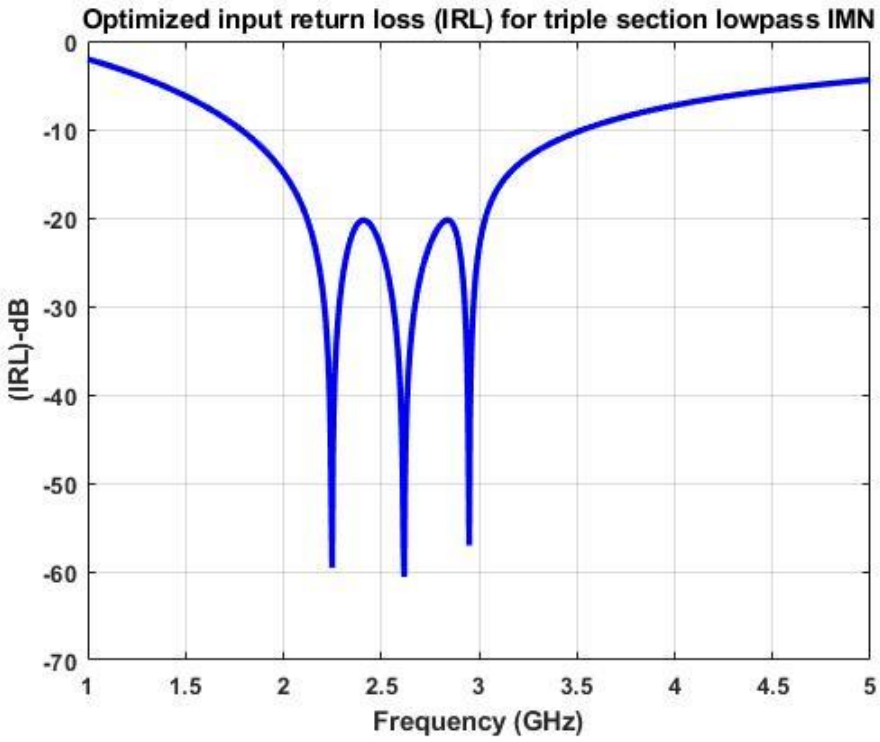


Figure 3. 7: Input return loss results of the fminsearch and fminunc optimization solvers for optimizing the lumped element values

The result shows a better matching bandwidth with three notches of the reflection coefficient at 2.25, 2.61 and 2.95 GHz frequencies, as expected. The computed fractional bandwidth of the optimized six-element lowpass input matching network at a -20 dB threshold centred around an operating frequency of 2.5GHz within the bandwidth of interest (2.1 GHz-2.9 GHz) has increased from 27.6% of the optimized four-element lowpass input matching network to 36.4%.

Table 3. 4 summarises the results for all the optimization solvers' performance in terms of their number of iterations and criterion values. All the optimization solver methods approximately give the same six-element optimum matching network parameter values, resulting in a perfect match as the criterion values E(x) for all the optimizer functions are close to zero.

Table 3. 4: Summary of the results of the optimization solvers with six elements lowpass input matching network (in terms of criterion values E(x) and number of iterations)

	Fminsearch solver	Fminunc solver	Fmincon solver (Interior point algorithm)	Fmincon solver (SQP-algorithm)	Fmincon solver (Active-set algorithm)
Criterion value E(x)	1.5158e-21	4.1462e-10	0.067007	0.067007	0.067007
Number of iterations	1326	100	74	63	54

By comparing the performance of the solvers in terms of the number of iterations, the Fminsearch solver using the Nelder-Mead simplex algorithm has the highest number of iterations compared to the other algorithms. While the fmincon solver using the active-set algorithm works best for having the lowest number of iterations (54) than the remaining solvers.

3.4.3 Optimization of six-element lowpass output matching network parameters with unconstrained and constrained solvers

The procedure for optimizing the six-element (triple-section) lowpass output matching shown in Figure 3. 8 follows a similar strategy used in optimizing the six-element (triple-section) lowpass input matching network described in the previous section. The fminsearch and fminunc optimization solvers are the unconstrained solvers for finding the optimum values of the matching network parameters shown in Figure 3. 8. The initial values of the network parameters to be optimized are selected in the same way as those of the triple-section lowpass input matching network.

3.4.3.1 Selection of Initial values for lowpass six-element output matching network using analytical method

The design equations to determine the initial values of the matching network parameters of Figure 3. 8 are derived first by transforming the parallel connection of the optimum resistance (R_{opt}) and parasitic drain capacitance (C_d) at the input to the matching network into series using the equation of Table 2. 1.

The schematic of the modified network showing the new values of the transformed parasitic drain capacitance and the optimum resistance is shown in Figure 3. 9.

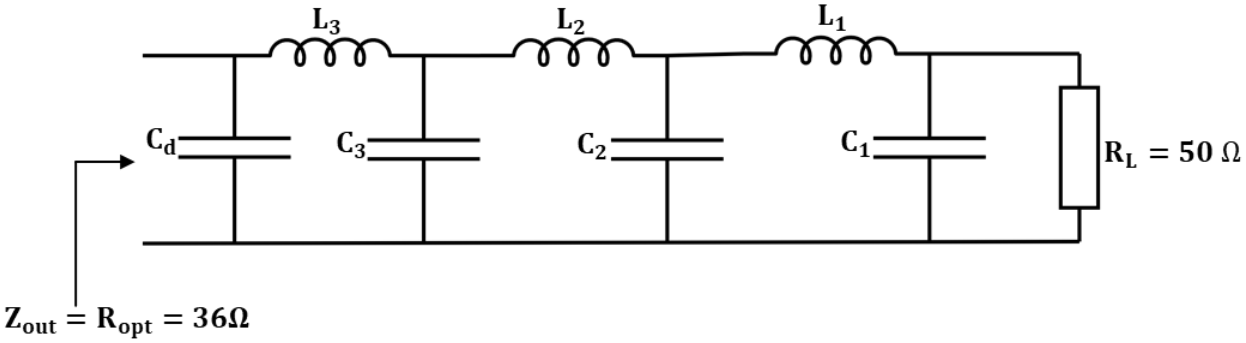


Figure 3. 8: Triple-section lowpass output matching network with parasitic drain capacitor (C_d)

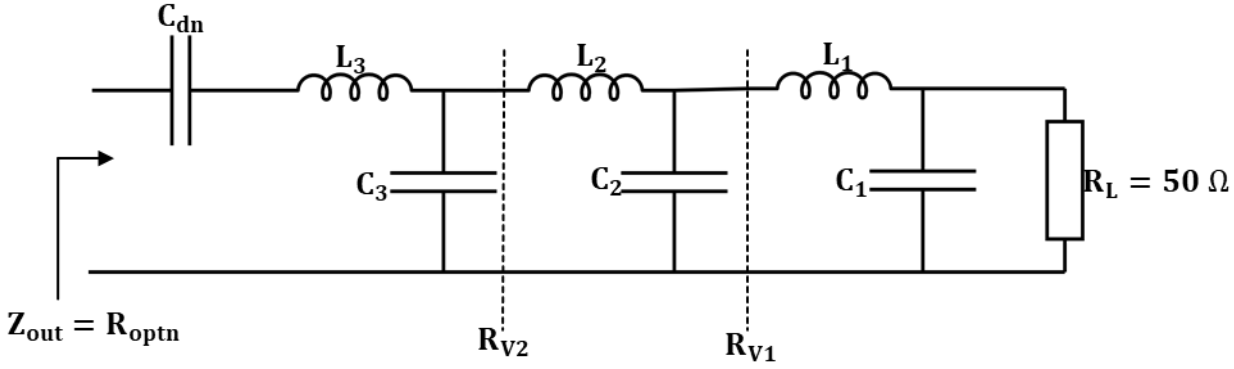


Figure 3. 9: Modified Triple- Section Lowpass output Matching Network

From Figure 3. 9, the design equations for the network lumped components at a designed radian frequency ω_0 are given as follows:

$$L_1 = \frac{C_1 {R_L}^2}{1 + (C_1 \omega_0 R_L)^2} \tag{3.16}$$

$$C_1 = \frac{1}{\omega_0 R_L} \sqrt{\frac{R_L}{R_{V1}} - 1} \tag{3.17}$$

$$L_2 = \frac{C_2 {R_{V1}}^2}{1 + (C_2 \omega_0 R_{V1})^2} \tag{3.18}$$

$$C_2 = \frac{1}{\omega_0 R_{V1}} \sqrt{\frac{R_{V1}}{R_{V2}} - 1} \tag{3.19}$$

$$L_{3o} = \frac{C_3 {R_{V2}}^2}{1 + (C_3 \omega_0 R_{V2})^2} \tag{3.20}$$

$$C_3 = \frac{1}{\omega_0 R_{V2}} \sqrt{\frac{R_{V2}}{R_{optn}} - 1} \tag{3.21}$$

The total inductance value (L_3) at the input of the matching network that compensates for the series parasitic drain capacitance (C_{dn}) shown in Figure 3. 9 is given by:

$$L_3 = L_{3o} + \frac{1}{C_{dn} {\omega_0}^2} \tag{3.22}$$

Table 3. 5 shows the initial lumped element values for the six-element section lowpass output matching network of Figure 3. 8 with $R_{opt} = 36\ \Omega$, $R_L = 50\ \Omega$ and $C_d = 1.3$ pf

Table 3. 5: Initial lumped element values for triple section lowpass OMN

$C_1(pf)$	$C_2(pf)$	$C_3(pf)$	$L_1(nH)$	$L_2(nH)$	$L_3(nH)$
0.66	0.88	1.14	1.33	1.03	1.89

The output return loss result of the matching network computed with the initial lumped element values is illustrated in Figure 3. 10.

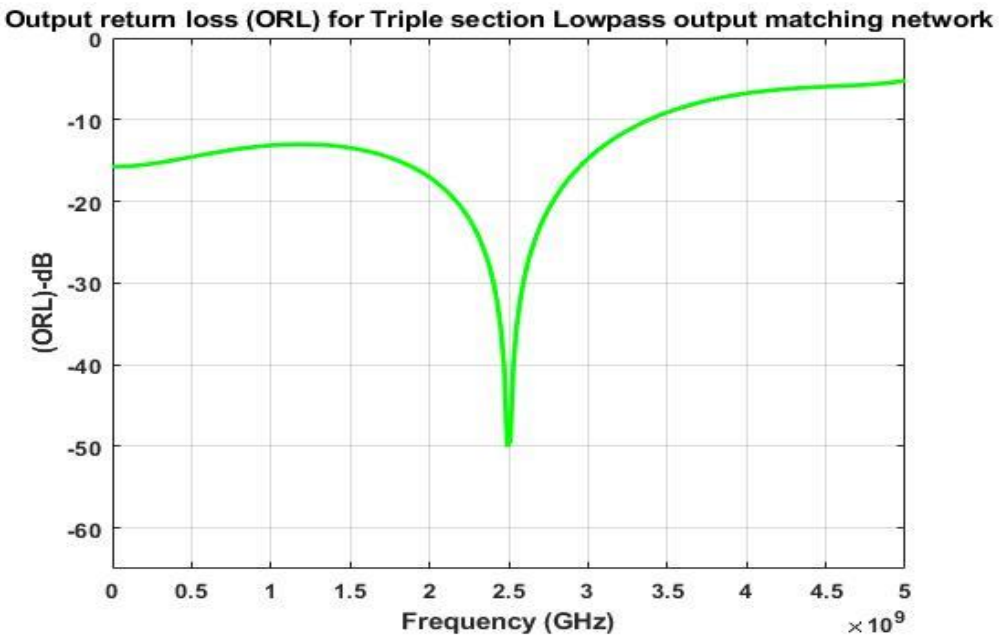


Figure 3. 10: Initial results of the output return loss for a Six-Element Lowpass lumped element-based output matching network (OMN)

As observed from the result of Figure 3. 10, the matching fractional bandwidth is approximately the same as that of the single, double and T-section lowpass output matching networks. Hence, the need to improve the bandwidth of the six-element lowpass output matching network using the MATLAB optimization solver approach becomes paramount.

3.4.3.2 Optimization result of the six-element lowpass output matching network parameters with Fminsearch solver

Following the insufficient matching bandwidth presented by the initial values of the matching network parameters for the triple-section lowpass output matching network, the initial values are therefore optimized by the fminsearch optimization solver at three frequency points of 2.1, 2.5, and 2.9 GHz using the same procedures as those of the triple-section lowpass input matching network. Thus, the optimum lumped component values and the criterion value E(x) for the network shown in Figure 3. 8 after 2000 iterations are given as:

$$\mathbf{x_{fminsearch}} = \begin{bmatrix} C_{1opt}(pf) \\ C_{2opt}(pf) \\ C_{3opt}(pf) \\ L_{1cg\_opt}(nH) \\ L_{2opt}(nH) \\ L_{3opt}(nH) \end{bmatrix} = \begin{bmatrix} 2.219 \\ 1.4049 \\ 0.8727 \\ 2.3352 \\ 2.1242 \\ 2.1215 \end{bmatrix}$$

$$fval_{fminsearch} = 4.9$$

Figure 3. 11 shows the matching result of the optimized network parameter values in the form of output return loss.

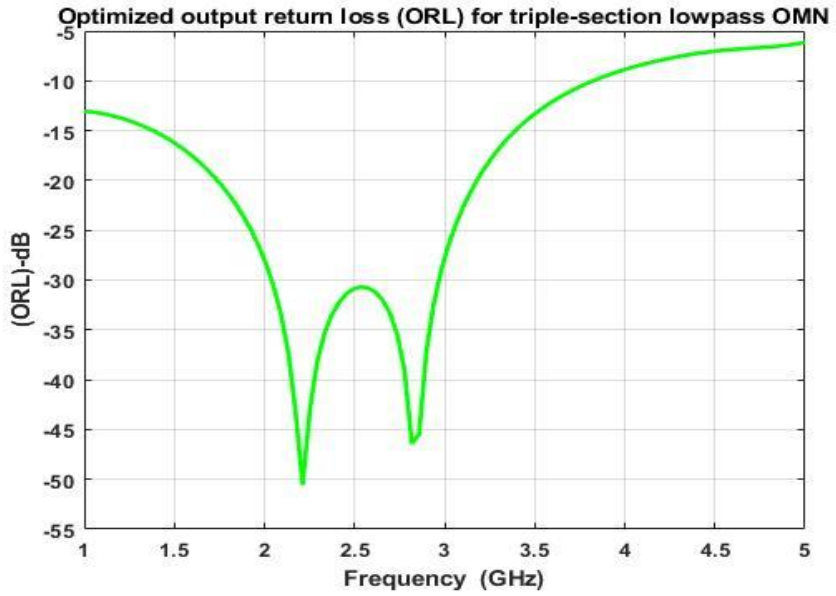


Figure 3. 11: Output return loss result of the fminsearch optimization solver used for optimizing lumped element values

The result shows an improvement in the fractional bandwidth at the -20 dB threshold around the bandwidth of interest to 57.6%. But the return loss result still did not show a good impedance match as the impedance match occurs only at two frequency points instead of three.

3.4.3.3 Optimization result of the six-element lowpass output matching network parameters with Fminunc solver

The procedure for optimizing the lumped component values of the triple-section lowpass output matching network with the fminunc optimization solver is similar to how the solver is used to optimize the input matching network counterpart. Consequently, the optimum network parameter values ($x_{fminunc}$) and the criterion value E(x) produced by the fminunc solver after 160 iterations are given by:

$$\mathbf{x_{fminunc}} = \begin{bmatrix} C_{1opt}(pf) \\ C_{2opt}(pf) \\ C_{3opt}(pf) \\ L_{1cg\_opt}(nH) \\ L_{2opt}(nH) \\ L_{3opt}(nH) \end{bmatrix} = \begin{bmatrix} 2.8298 \\ 2.5227 \\ 1.063 \\ 2.4306 \\ 2.8872 \\ 3.0857 \end{bmatrix}$$

$$fval_{fminunc} = 1.0368e - 10$$

Figure 3. 12 shows the matching result of the optimized network parameter values in the form of output return loss.

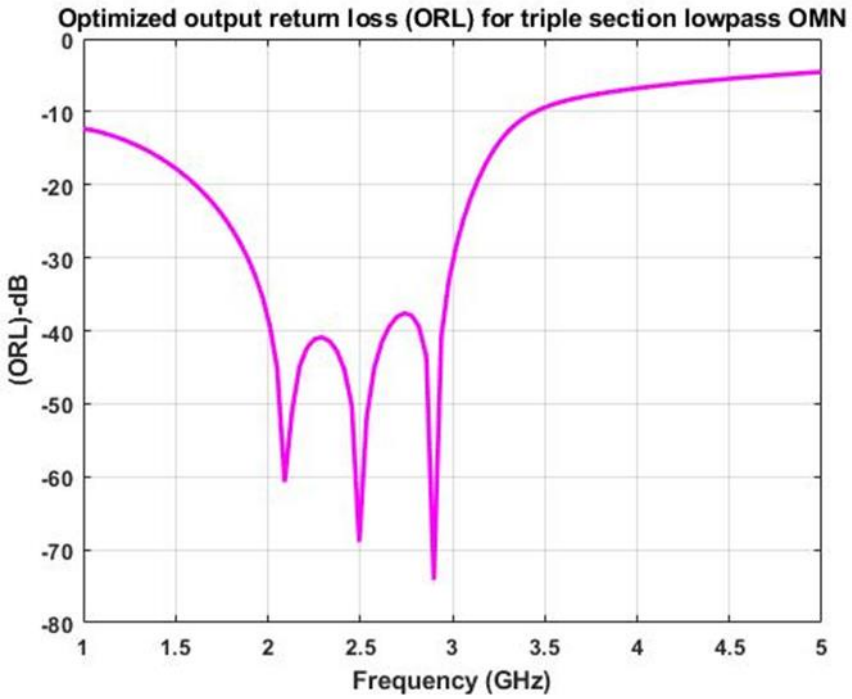


Figure 3. 12: Output return loss result for the fminunc solver optimized lumped element values

The fractional bandwidth of the output return loss at the -20 dB threshold centred around 2.5 GHz within the frequency band of interest is 60.8% and is higher than that of the optimized lowpass four-element output matching network . The return loss result, in this case, shows a good matching bandwidth as it presents all the three notches of the reflection coefficient at 2.1, 2.5, and 2.9 GHz frequencies, respectively.

3.4.3.4 Optimization result of the six-element lowpass output matching network parameters with Fmincon solver

The optimization of the triple-section lowpass output matching network parameters is carried out using three different algorithms of the fmincon solver in the same way it is done with the triple-section lowpass input matching network case. Since the optimization with the fmincon solver requires us to define a set of lower and upper boundaries within which the optimization solution lies, the lower and upper bound values of the optimization variable for the triple-section lowpass output matching network are chosen as: Lb= [0.5 pf; 0.5 pf; 0.5 pf; 0.1nH; 0.1nH; 0.1nH], ub= [55pF; 55pF; 55pF; 3nH; 3nH; 3nH]. Therefore, the optimized network parameter values and the criterion value E(x) of the fmincon solver with interior point algorithm after 112 iterations are given as:

$$\mathbf{x_{fmincon1}} = \begin{bmatrix} C_{1opt}(pf) \\ C_{2opt}(pf) \\ C_{3opt}(pf) \\ L_{1cg\_opt}(nH) \\ L_{2opt}(nH) \\ L_{3opt}(nH) \end{bmatrix} = \begin{bmatrix} 2.8623 \\ 2.5735 \\ 1.0875 \\ 2.3667 \\ 2.7765 \\ 3 \end{bmatrix}$$

The function value is $\mathrm{fval}_{\mathrm{fmincon1}} = 0.2372$

Figure 3. 13 shows the matching result of the optimized network parameter values in the form of output return loss. Thus, for the fmincon optimization solver using the SQP algorithm, the optimized network parameter values and the criterion value E(x) of the solver after 41 iterations are the same as those of the fmincon solver with the interior point algorithm. Likewise, the solutions to the fmincon solver using the active-set algorithm after 33 iterations are the same as those of the default interior-point algorithm.

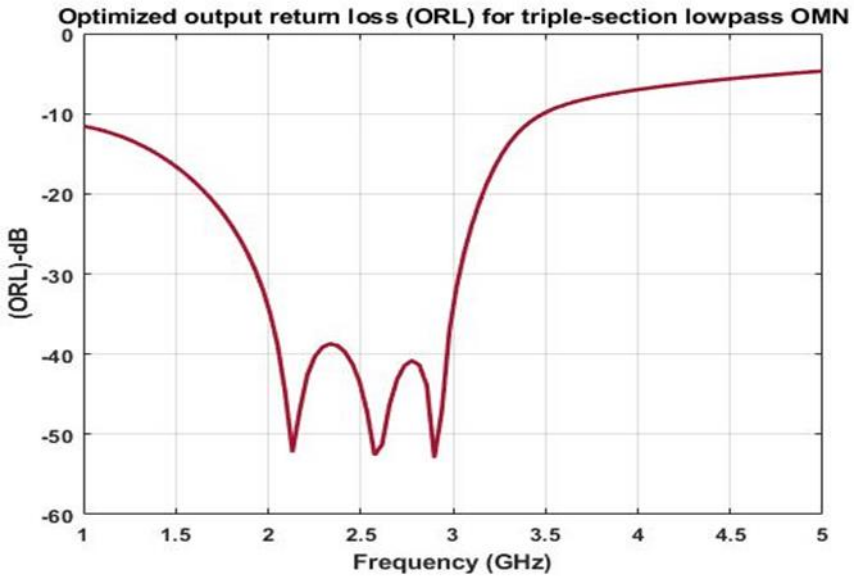


Figure 3. 13: Output return loss result of the 3 fmincon optimization solver algorithms for optimizing lumped element values

The output return loss of Figure 3. 13 also shows a good impedance match with a fractional bandwidth of 60% at the -20 dB limit and centred at 2.5 GHz around the desired frequency band.

Table 3. 6 compares the performance of the optimization solvers in terms of their number of iterations and criterion values E(x). The fminunc solver has the lowest criterion value, with its criterion value approximately equal to zero. Thus, the optimized network parameter values by the fminunc solver are the optimum as they achieved the highest fractional bandwidth of 60.8% at the -20 dB threshold centred at a design frequency of 2.5 GHz in the frequency range of 2.1 GHz to 2.9 GHz. Furthermore, the

fmincon solver using the active-set algorithm offers a good compromise for having the lowest number of iterations with a relatively low criterion value.

Table 3. 6: Summary of the results of the optimization solvers with six elements lowpass output matching network (in terms of criterion values E(x) and number of iterations)

	Fminsearch solver	Fminunc solver	Fmincon solver (Interior point algorithm)	Fmincon solver (SQP-algorithm)	Fmincon solver (Active-set algorithm)
Criterion value E(x)	4.9	1.0368e-10	0.2372	0.2372	0.2372
Number of iterations	2000	160	112	41	33

3.5 General comparison of the optimization solvers' performance for a six-element lowpass input matching network.

Optimiser functions may present different convergences and solutions when the initial values of the matching network parameters are far from the optimum solution. Thus, the performance of the optimization solvers is compared by generating random initial values in a range of -100% to +100% and -50% to +50% deviations from the optimum value. Furthermore, the optimization solvers are placed in a loop program that runs about 1000 times to generate random initial values at each loop over the specified ranges. The optimiser function with a large percentage of random initial values with the minimum criterion value E(x) is identified and recommended for optimizing all the different configurations of the impedance-matching network parameters.

To compare the criterion value E(x) of the optimization solvers, Figure 3. 14 and Figure 3. 15 showed plots of the empirical cumulative distribution function (CDF) of the criterion value E(x) for each solver over the two specified ranges of initial values. F(x) or E(x) is the probability of the criterion value having a value less than or equal to the error as given in equation (3.23).

$$\mathrm{F}(\text{criterion value}) = P(E(x) \leq (\text{criterion value}) \tag{3.23}$$

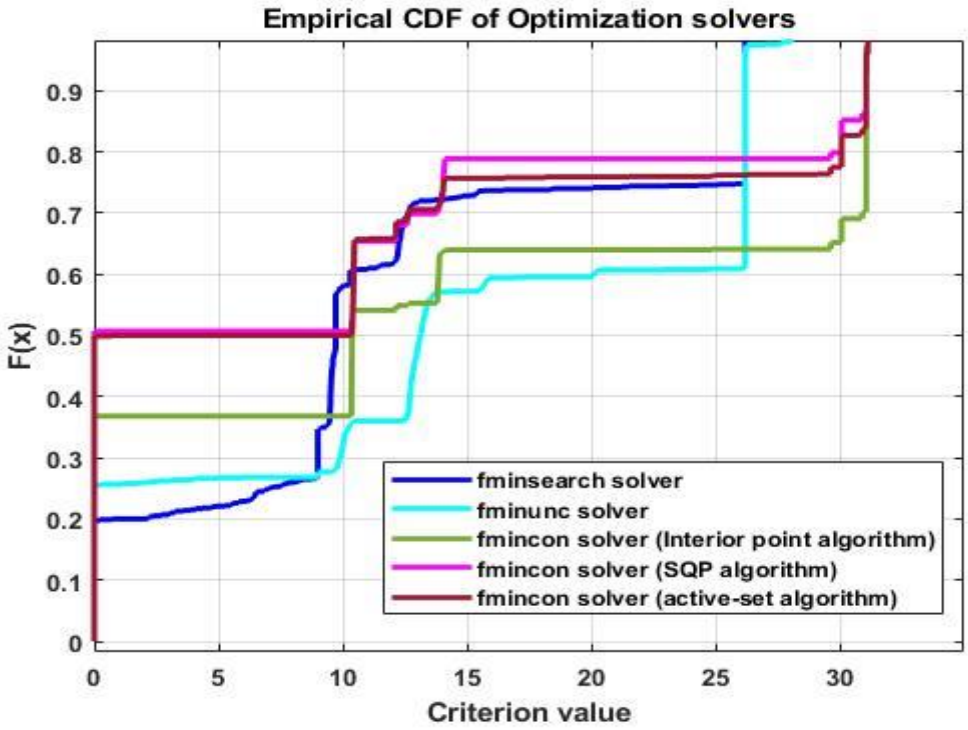


Figure 3. 14: Empirical CDF plot of criterion value of optimization solvers for -100% to +100% of initial values around the optimum value

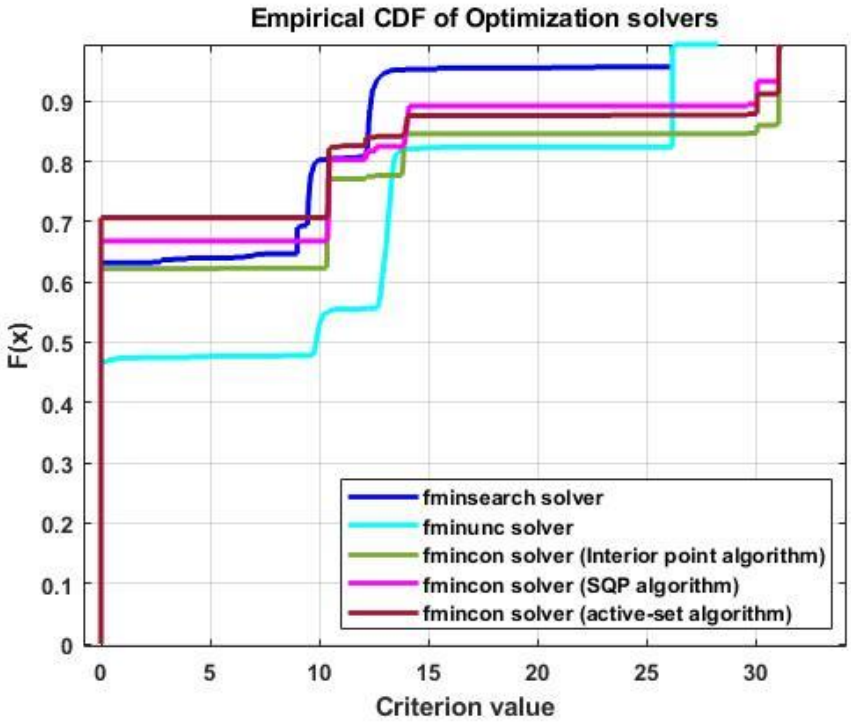


Figure 3. 15: Empirical CDF plot of criterion values of optimization solvers for -50% to +50% of initial values around the optimum value

Figure 3. 14 illustrates the CDF plot for 1000 samples of random initial values within the range of +/-100% of the optimum values, while Figure 3. 15 is for the +/-50% range. As seen from Figure 3. 14 and Figure 3. 15, for a criterion value lower than 10, the solution is considered good, as the network parameter values in these ranges present three notches of the reflection coefficient around the desired frequency band. Table 3. 7 gives each solver's percentage of better solutions for both the +/-100% and +/-50% ranges.

Table 3. 7: The percentage range of good solutions for each solver

	Fminsearch	Fminunc-solver	Fmincon-solver (Interior point algorithm)	Fmincon-solver (SQP-algorithm)	Fmincon-solver (Active-set algorithm)
Percentage (%) of good solutions for +/- 100%	19.9%	25.7%	36.8%,	50.7%,	49.9%
Percentage (%) of good solutions for +/- 50%	63.2%	46.9%	62.2%	66.8%	70.7%

As illustrated in Table 3. 7, the result of Figure 3. 14 shows that about 50.7%, 49.9%, 36.8%, 25.7%, and 19.9% of the 1000 samples of random initial values within the range of -100% to +100% of the optimum values have a criterion value close to zero when optimized by fmincon solver (SQP algorithm), fmincon solver (active-set algorithm), fmincon solver (interior point algorithm), fminunc solver, and fminsearch solver, respectively. The fmincon solver (SQP algorithm) has better convergence performance, with a higher percentage of its random initial values being optimized to optimum values over ten frequency points within the bandwidth of interest.

Similarly, Figure 3. 15 shows that when the random initial values are between +/- 50% close to the optimum values, the fmincon solver (active-set algorithm) offers a better convergence performance when compared to the remaining optimization method, with 70.7% of its random initial values presenting an approximate criterion value of zero.

3.6 Design and Simulation of 2.5GHz GaN-Based Single-Stage RF Power Amplifier.

3.6.1 Input and output matching network for the single-stage RF power amplifier

The need for higher RF power amplifier performance over a wide bandwidth calls for the design of a wideband power amplifier (PA) for wireless transmitter applications.

The design and simulation of a 25 W class B single-stage RF power amplifier in the frequency range of 2.1 GHz to 2.9 GHz are presented in this section. The considered power device is a GaN high-electron-mobility transistor (HEMT) presented in Chapter 1 of this thesis. The Advanced Design System (ADS) software tool from Agilent is used to design the proposed class B single-stage RF power amplifier. The optimized six- and four-element lowpass matching networks, designed in the previous section of this chapter, are considered the possible input and output matching network pairs of the amplifier. The matching network pairs that resulted in good PA performance over the desired bandwidth are identified and selected. The performances of the simulated RF power amplifier over the desired bandwidth are given in terms of the maximum output power, power gain and Power Added Efficiency (PAE) at a 1dB gain compression point.

The input matching network to the power amplifier ensures that the source impedance (Z_S) of the amplifier matches its input impedance (Z_{in}) to maximise the gain of the amplifier, and the output matching network transforms the system impedance ($Z_L = 50\ \Omega$) to an optimal load resistance ($R_{opt} = 36\ \Omega$) at an operating frequency of 2.5 GHz.

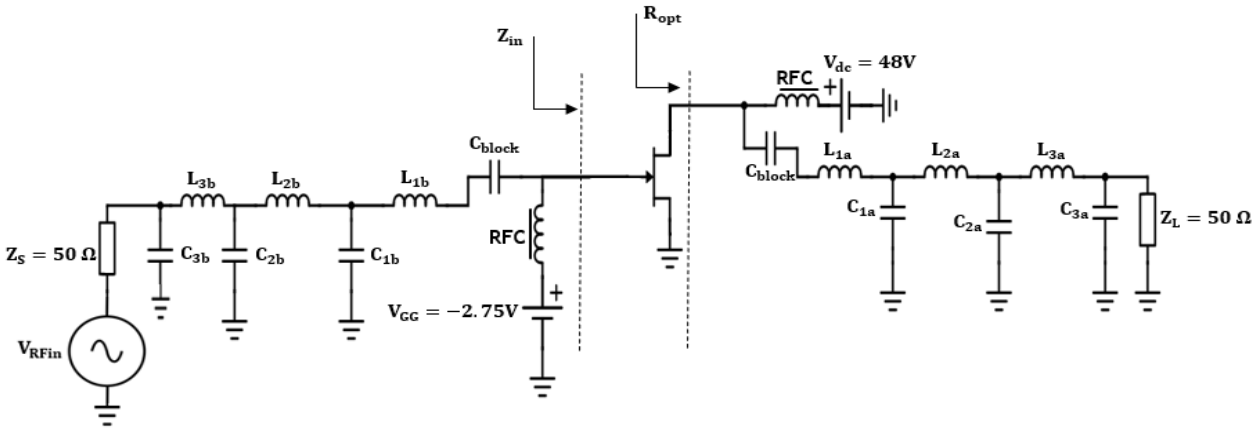


Figure 3. 16: Single-stage RF power amplifier designed with the Triple sections lumped element-based lowpass input and output matching networks.

The simulation results for the single-stage RF power amplifier are analysed based on the following pairs of input and output matching networks to the RF power amplifier:

A. Double-section lowpass matching networks as the input and output matching networks.
B. Double-section lowpass matching network is the input matching network, while a triple-section lowpass matching network is the output matching network.
C. Triple-section lowpass matching network is the input matching network, while the double section lowpass matching network is the output matching network.
D. Triple-section lowpass matching networks as the input and output matching networks.

Figure 3. 16 shows the complete schematic of the designed single-stage RF power amplifier of case D with the triple-section lowpass matching networks as its input and output matching networks.

Table 3. 8 and Table 3. 9 give the designed matching network parameter values for the double-section lowpass input and output matching networks.

Table 3. 8: Designed input matching network (IMN) parameters values of the Double section lowpass input matching network

L_{1b} (nH)	L_{2b} (nH)	C_{1b} (pF)	C_{2b} (pF)
0.73	0.73	25.2	6.69

Table 3. 9: Designed output matching network (OMN) parameters values of the Double section lowpass output matching network

L_{1a} (nH)	L_{2a} (nH)	C_{1a} (pF)	C_{2a} (pF)
2.6	3.06	2.48	1.17

Furthermore, the summary of the designed matching network parameter values for the triple-section lowpass input and output matching networks is listed in Table 3. 10 and Table 3. 11, respectively.

Table 3. 10: Designed input matching network (IMN) parameters values of the Triple section lowpass input matching network

L_{1b} (nH)	L_{2b} (nH)	L_{3b} (nH)	C_{1b} (pF)	C_{2b} (pF)	C_{3b} (pF)
0.65	0.16	0.64	49.4	50.46	6.81

Table 3. 11: Designed output matching network (OMN) parameters values of the Triple section lowpass output matching network

L_{1a} (nH)	L_{2a} (nH)	L_{3a} (nH)	C_{1a} (pF)	C_{2a} (pF)	C_{3a} (pF)
2.43	2.89	3.09	2.83	2.52	1.06

Consequently, the output power, power gain, and power added efficiency performance of the single-stage RF PA amplifier versus input power with cases A to D matching network pairs at fundamental frequency Fo=2.5 GHz, are approximately the same and are depicted in Figure 3. 17. The RF power amplifier produced a maximum PAE of 63% with associated output power and power gain of 45 dBm and 17 dB, respectively.

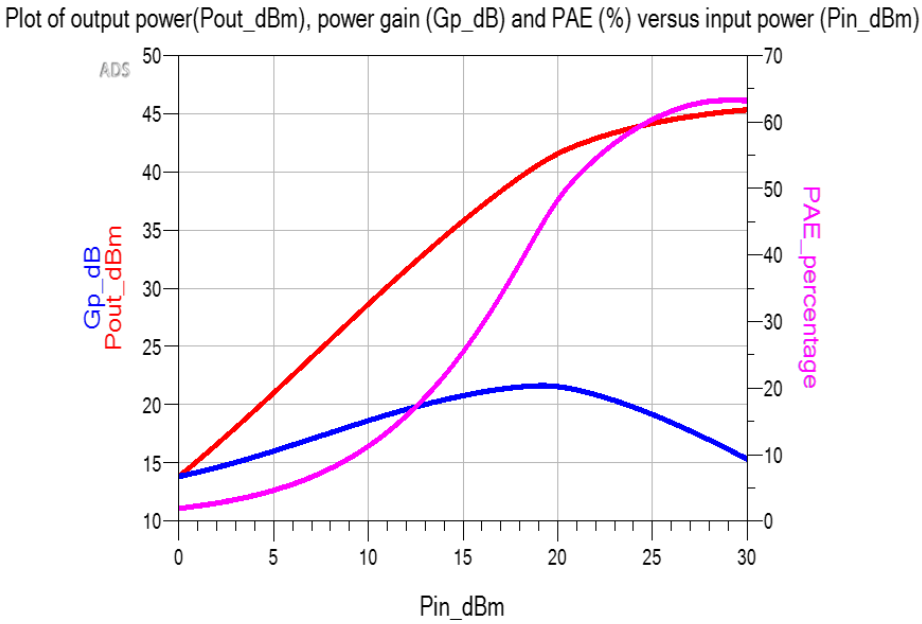


Figure 3. 17: Simulated results at the fundamental frequency of 2.5 GHz of power added efficiency (PAE), power gain (Gp) and output power (Pout) with cases A to D matching networks pairs.

3.6.2 Frequency sweep of the RF power amplifier simulation results

The RF power amplifier performances in terms of bandwidth using cases (A–D) matching network pairs are compared by sweeping the simulated result of Figure 3. 17 over the desired frequency band of 2.1 GHz to 2.9 GHz, centred at an operating frequency of 2.5 GHz.

Figure 3. 18 to Figure 3. 20 compare the bandwidth performance of the simulated result of the RF power amplifier with cases (A–D) as its matching network pairs at a 1 dB gain compression point over the desired frequency band of interest.

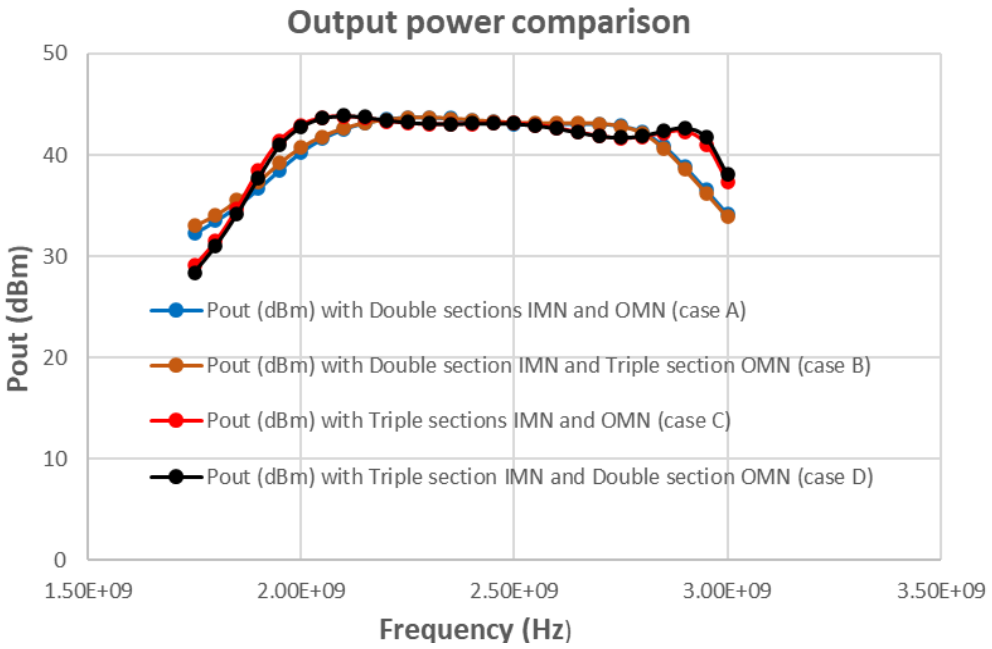


Figure 3. 18: Output power performance at 1dB gain compression

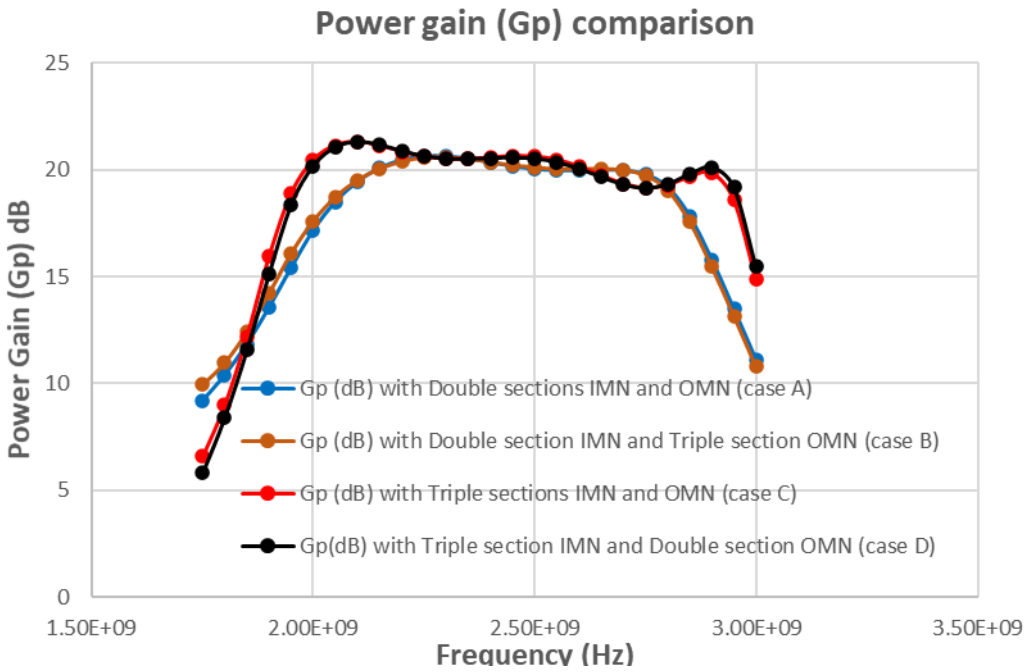


Figure 3. 19: Power gain performance at 1dB gain compression

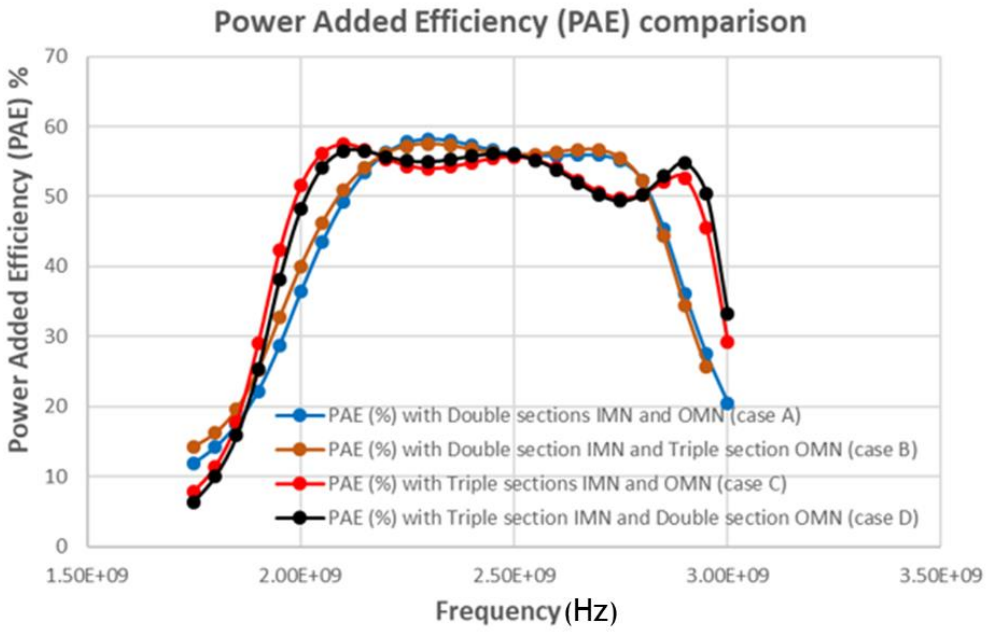


Figure 3. 20: Power Added Efficiency performance at 1dB gain compression

The simulation results of Figure 3. 18 to Figure 3. 20 show that the RF PA performances based on the designed input and output matching network pairs of the cases (C and D), i.e., using a triple-section lowpass matching network as the input matching network, present a better bandwidth performance over the frequency band of 2.1 to 2.9 GHz by producing an output power of 43 dBm and PAE of over 50% with an associated power gain in the range of 20.1-21.1dB over the desired frequency band.

3.7 Conclusion

In this chapter, we introduce the method of designing wide-band impedance matching networks using MATLAB optimization Toolbox solvers. These solvers are used to optimise the network parameters of the double and triple-section lowpass input and output matching networks to the power transistor in Figure 2. 11. The matching networks match complex load impedance to resistive source impedance and vice versa. The fractional bandwidth of the optimized double-section lowpass input and output matching networks is 27.6% and 52%, respectively. Similarly, the fractional bandwidth of the optimized triple-section lowpass input and output matching networks to the amplifier is 36.4% and 60.8%, respectively.

Furthermore, the performances of the MATLAB optimization solvers were compared using the optimized network parameters of the six-element lowpass input matching network when subjected to different randomly generated initial values in a range of +/-100% and +/-50% deviation from the optimum value. Both the fmincon optimization solver (SQP algorithm) and the fmincon solver (active-

set algorithm) are robust to variation of initial values and converge faster than the other three optimization solvers to optimum values.

We also design and simulate the single-stage class B RF power amplifier with four different lowpass matching network pairs as its input and output matching networks. The Cases D and C matching network pairs corresponding to the optimized triple section matching network at the input offer good performances over the frequency band of 2.1 to 2.9 GHz.

Chapter 4: The theory and design of the Doherty Power Amplifier (DPA)

4.1 Introduction

The high-efficiency Doherty RF power amplifier derives its name from the engineer William H. Doherty. He invented it in 1936 [40], during the work developed at Bell Telephone Laboratories on high-power radio transmitters used for terrestrial and trans-oceanic broadcasting and telephony. F.H. Raab [41] is the first to demonstrate the Doherty technique on solid-state amplifiers. The advent of digital cellular radio systems in the late 1990s provided an opportunity to focus new attention on Doherty amplifiers to improve the electrical efficiency of the base station transmitters.

Highly efficient RF power amplifiers are requested to operate with a complex modulation scheme like quadrature amplitude modulation (QAM). But the modulation scheme of this kind features a time-varying envelope with a very high peak-to-average power ratio (PAPR), and power amplifiers are expected to have high efficiency not only at saturation point but also at low power levels to cope with the resulting PAPR signals[42]. However, this is not the case for conventional power amplifiers, which only produce high efficiency at maximum output power and low efficiency at output power backoff.

Several techniques have been proposed to improve the backoff efficiency of the power amplifier in the base station transmitter with high PAPR signals. This includes Chireix out-phasing PA and Doherty power amplifier techniques, which work based on the load modulation concept, or envelope tracking (ET) and envelope elimination and restoration (EER) techniques, which work based on the supply modulation concept. The Doherty power amplifier is the most widely accepted technique among these solutions because of its ease of use and promising performance in wireless communication. This section is devoted to describing the basic operating principle of the Doherty amplifier.

4.2 Load Modulation using Doherty structure

The process of changing the effective load impedance presented to the drain terminal of a transistor by varying its output power level is referred to as load modulation. An ideal class B-biased FET-based transistor's load line is illustrated in Figure 4. 1. As shown in Figure 4. 1, the load line value of Ropt corresponds to the maximum voltage or current swing of the transistor. For a load line impedance higher than Ropt, the current amplitude of the transistor, in this case, is less than the maximum possible value, thereby leading the transistor to saturate at lower output power and consequently reach maximum efficiency at lower output power [43]. The Doherty amplifier technique offers a good solution using the load modulation concept to maintain maximum efficiency over a wide range of output powers.

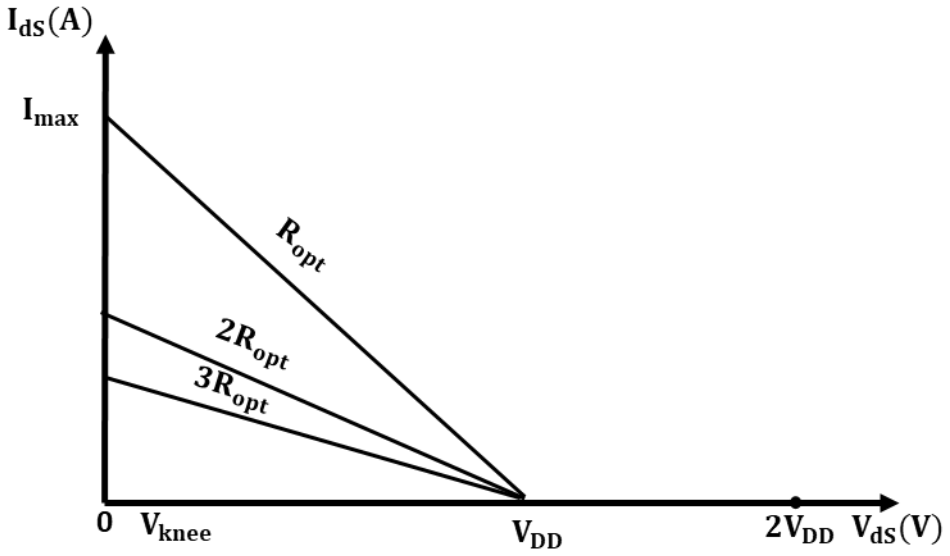


Figure 4. 1: Ideal Class B amplifier load lines

The Doherty amplifier technique allows the load impedance of the amplifier to be varied by the input signal power level using a combination of two amplifiers, as illustrated in Figure 4. 2.

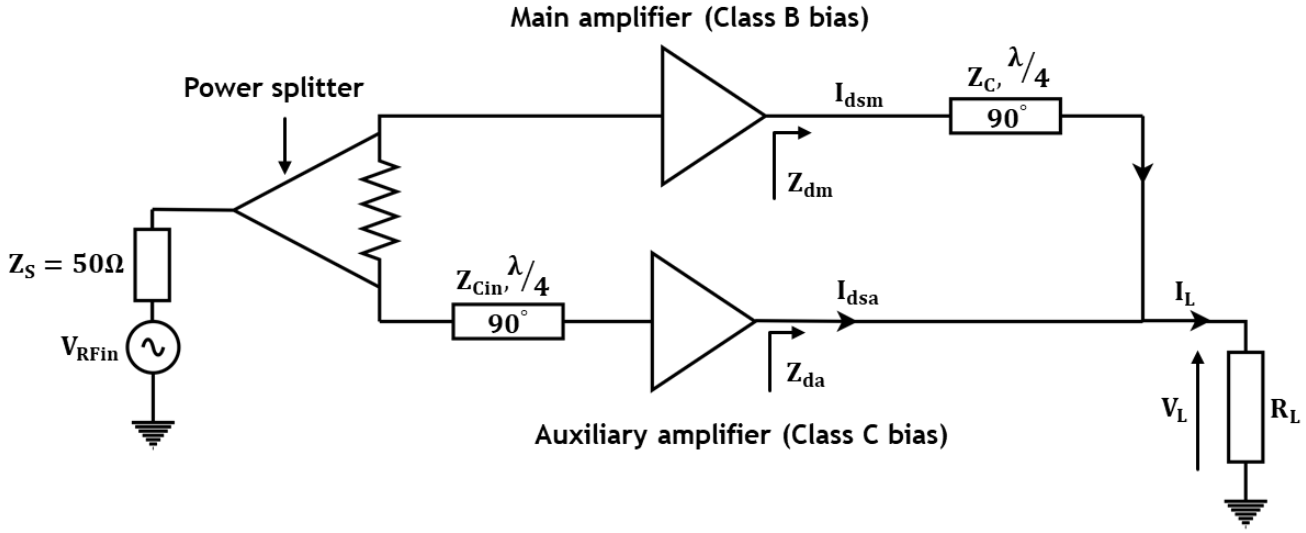


Figure 4. 2: Basic configuration of a Doherty amplifier

As seen from Figure 4. 2, the basic Doherty PA topology consists of Main (or Carrier) and Auxiliary (or Peaking) amplifiers as well as two quarter-wave transmission lines. The quarter-wave transmission line connected to the input of the Auxiliary amplifier offsets the 90° phase shift caused by the main amplifier's output quarter-wave transmission line. Furthermore, the Main and Auxiliary amplifiers are class B and C biased, respectively.

The advantages and disadvantages of DPA [44] are as follows:

- Advantages :

i. The DPA technique offers higher efficiency at backoff compared to other PA topologies.
ii. DPA is easy to implement due to its architectural simplicity and relative complexity.
iii. DPA can be used alone without other control circuits to ensure easy replacement of the amplifier when it is faulty without modifying the remaining sub-systems.

- Disadvantages

i. The DPA has a narrow bandwidth, typically caused by the quarter-wave transmission line.
ii. DPA may generate high distortion due to the high saturation of the main amplifier at a high power level and the low biasing condition of the auxiliary amplifier.

Figure 4. 3 illustrates the principle of load modulation with the use of two current sources, supplying currents I_1 and I_2 to a common load resistor R_L.

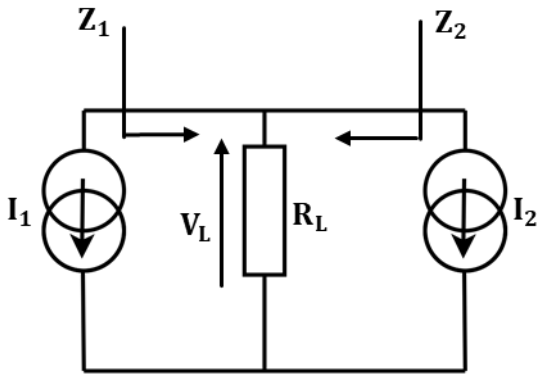


Figure 4. 3: Active load modulation concept using two current sources

As seen in Figure 4. 3, the voltage V_L across the load resistance R_L, when both currents flow into the load resistor, is given by [45,46]:

$$V_L = R_L(I_1 + I_2) \quad (4.\ 1)$$

The impedances seen by the current sources I_1 and I_2 are given as:

$$Z_1 = \frac{V_L}{I_1} = R_L(1 + \frac{I_2}{I_1}) \quad (4.\ 2)$$

$$Z_2 = \frac{V_L}{I_2} = R_L(1 + \frac{I_1}{I_2}) \quad (4.\ 3)$$

Therefore, we can deduce from equations (4. 1) to (4. 3) that the impedances Z_1 or Z_2 can be changed or pulled by varying the magnitude and/or phase of the current sources I_1 or I_2. The impedance value of Z_1 increases with I_2 if we consider I_2 to be in phase with I_1. However, this is contrary to the desired load variation concept illustrated in Figure 4. 1. Thus, the DPA technique incorporates an impedance inverter between I_2 and R_L to transform down the value of impedance Z_1 as current I_2 increases.

4.3 Determination of the load impedances seen by the Main and Auxiliary amplifiers when separated by the quarter-wave transmission line.

Figure 4. 5 shows the schematic of the DPA technique with the Main and Auxiliary devices connected across a load resistor R_L and separated by the quarter-wave transmission line. While the corresponding simplified circuit is depicted in Figure 4. 6. Furthermore, the RF current amplitudes of the Main and Auxiliary amplifiers plotted as a function of input voltage drive are shown in Figure 4. 4.

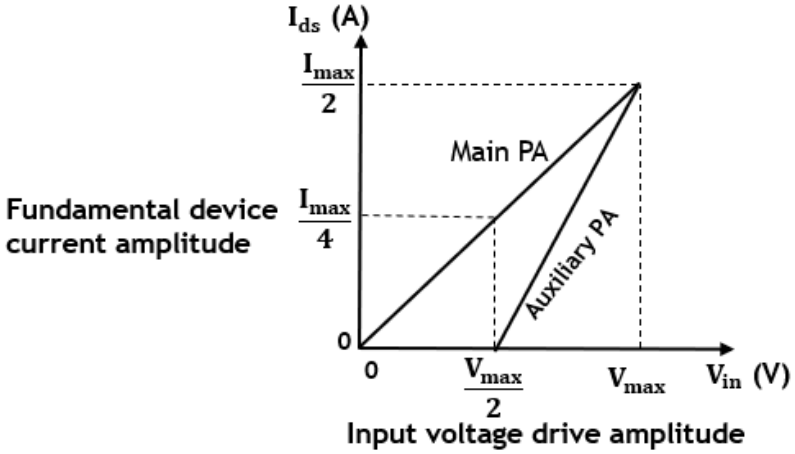


Figure 4. 4: Main and Auxiliary device RF current amplitude variation versus input drive

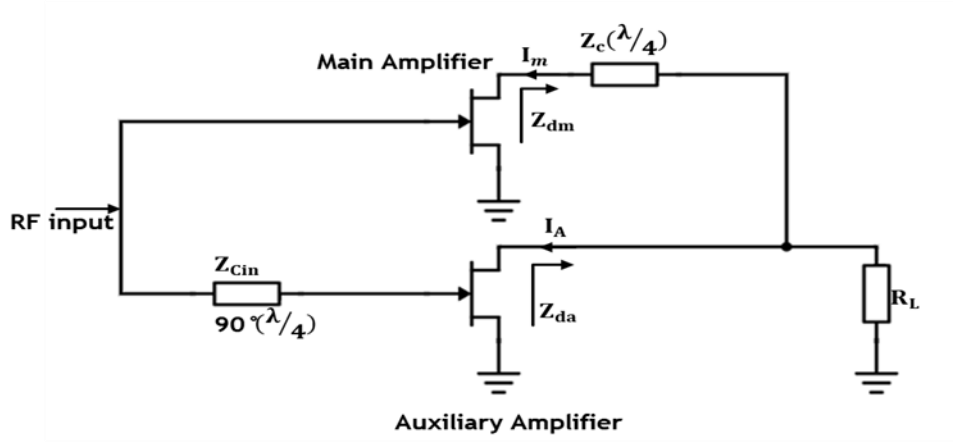


Figure 4. 5: Analysis circuit of the DPA technique

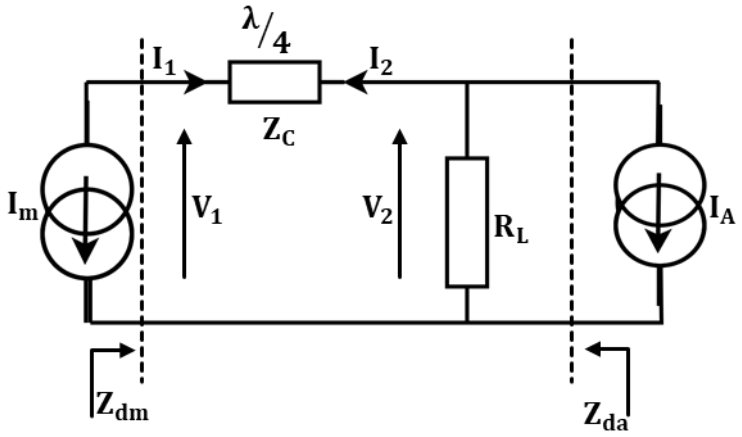


Figure 4. 6: The simplified circuit of the DPA technique

The analysis of the simplified circuit of the DPA shown in Figure 4. 6 helps us determine the load impedance values at the output of each transistor.

From Figure 4. 6 : Z_C is the characteristic impedance of the quarter-wave transmission line, the load impedance seen by the main amplifier is given by Z_{dm}, Z_{da} is the auxiliary amplifier's load impedance,the output current of the main amplifier is given by I_m, the output current of the auxiliary amplifier is given by I_A.

The currents (I_1, I_2) and voltages (V_1, V_2) at the ports of the quarter-wave transmission line with characteristic impedance (Z_C) and length (l) are related by the following matrix expression [47,48]:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} \cos\theta l & j.\ Z_C.\sin\theta l \\ \frac{j\sin\theta l}{Z_C} & \cos\theta l \end{bmatrix} . \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \quad (4.\ 4)$$

The term θl is equal to $\frac{\pi}{2}$ for a quarter-wave transmission line at the frequency Fo. This allows us to further rewrite the matrix expression of equation (4. 4) as:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & j.Z_C \\ \frac{j}{Z_C} & 0 \end{bmatrix} . \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \quad (4.\ 5)$$

Furthermore, the expressions of the currents at the ports of the quarter-wave transmission line of Figure 4. 6 as a function of the Main and Auxiliary amplifier currents are given as follows:

$$\begin{cases} I_1 = -I_m \\ I_2 = -\left(I_A + \frac{V_2}{R_L}\right) \end{cases} \quad (4.\ 6)$$

The solution to the matrix expression of equation (4. 5) relates the voltages (V_1 and V_2) across the ports of the quarter-wave transmission line as follows:

$$\begin{cases} V_1 = -j.Z_C.I_2 \\ V_2 = -j.Z_C.I_1 \end{cases} \quad (4.\ 7)$$

Similarly, the load impedances seen by the current sources of the Main and Auxiliary transistors are expressed as:

$$\begin{cases} Z_{dm} = \frac{V_1}{-I_m} \\ Z_{da} = \frac{V_2}{-I_A} \end{cases} \quad (4.\ 8)$$

By substituting the equations (4. 6) and (4. 7) into equation (4. 8), the expression of the load impedance seen by both devices now becomes:

$$\begin{cases} Z_{dm} = \frac{{Z_C}^2}{R_L} - j.Z_C\left(\frac{I_A}{I_m}\right) \\ Z_{da} = -j.Z_C\left(\frac{I_m}{I_A}\right) \end{cases} \quad (4.\ 9)$$

The quarter-wave transmission line at the input to the auxiliary amplifier in Figure 4. 5 helps to obtain a phase shift of 90° between the Main and Auxiliary transistor currents. Thus, the load impedances seen by the two devices become purely resistive and are given by:

$$\begin{cases} Z_{dm} = \frac{{Z_C}^2}{R_L} - Z_C\left(\frac{I_A}{I_m}\right) \\ Z_{da} = Z_C\left(\frac{I_m}{I_A}\right) \end{cases} \quad (4.\ 10)$$

When two amplifiers of the same size operate at a high input power level, and both amplifiers reach saturation with equal drain currents (I_m and I_A), the load impedance at the output of both amplifiers becomes:

$$\begin{cases} Z_{dm} = \dfrac{{Z_C}^2}{R_L} - Z_C \\ Z_{da} = Z_C \end{cases} \quad (4.\ 11)$$

For $Z_C = 2R_L$, both amplifiers will have the same load impedance presented on their drain terminals and combine to deliver maximum output power to the load. At this point, equation (4. 11) becomes:

$$Z_{dm} = Z_{da} = 2R_L \quad (4.\ 12)$$

At a low input power level, the auxiliary amplifier is turned off. This implies that the auxiliary amplifier current is zero. Therefore, the load impedance presented to the Main and Auxiliary amplifiers now becomes $4R_L$ and open-circuit, respectively. Moreover, the load impedance at medium input power levels varies from $4R_L$ to $2R_L$ for the Main amplifier and open-circuit to $2R_L$ for the Auxiliary amplifier. In this case, the auxiliary amplifier acts as an active load on the main amplifier. This power level at which the Auxiliary amplifier goes from off-state to conduction is called the transition point (α).

At a maximum power condition, the value of the characteristic impedance for the quarter wave transmission line (Z_C) at the output of the main amplifier of Figure 4. 5 is usually selected to be the conventional load line impedance R_{opt} of class B mode introduced in chapter 1 of this thesis. The value of the RF current flowing through the main amplifier branch based on this maximum power condition is given as:

$$I_m = \frac{I_{max}}{2} \quad (4.\ 13)$$

For $Z_C = 2R_L$, the expression for the load resistance, R_L, between the two amplifiers in terms of R_{opt} is:

$$R_L = \frac{R_{opt}}{2} \quad (4.\ 14)$$

And consequently:

$$Z_C = R_{opt} \quad (4.\ 15)$$

Table 4. 1 gives the variation of the impedance seen by the Main and Auxiliary amplifiers as a function function of the input power levels.

Table 4. 1: Different operating modes of the Doherty power amplifier

Input power level (P_{in})	Main amplifier load impedance (Z_{dm})	Auxiliary amplifier load impedance (Z_{da})
For: $P_{in} < P_{\alpha}$(power at transition point)	$2R_{opt}$	∞
For: $P_{\alpha} < P_{in} < P_{max}$	$2R_{opt}\ to\ R_{opt}$	$\infty\ to\ R_{opt}$
For : $P_{in} = P_{max}$	R_{opt}	R_{opt}

4.4 Drain voltages variation

Figure 4. 7 shows how the load impedances of the main amplifier vary as a function of the power level. It explains the physical limitations of the transistor and the transition point for operating the Doherty amplifier. At a low input power level, the Auxiliary transistor is off; as such, $I_A = 0$, while the Main amplifier transistor voltage (V_m) increases progressively as the current increases. For an ideal transistor, the main amplifier voltage tends toward its maximum value $V_m = V_{DD}$. It is considered that the saturation of the main amplifier occurs at a critical current I_C proportional to the maximum current, and is given by:

$$I_C = \alpha . I_{m\_max} \tag{4. 16}$$

The corresponding load impedance presented to the main amplifier at the critical point is proportional to the optimum load at full power, and is given by:

$$Z_{dm\_C} = \frac{R_{opt}}{\alpha} \tag{4. 17}$$

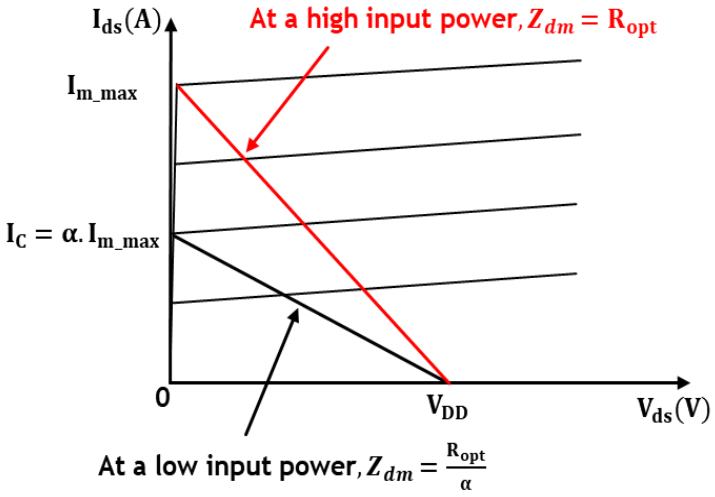


Figure 4. 7: Variation of main amplifier load impedances as a function of power level

From equation (4. 10), the voltage across the Main and Auxiliary amplifiers is expressed by the following relationship [10, 11]:

$$\begin{cases} V_m = \dfrac{{Z_C}^2}{R_L} I_m - Z_C I_A \\ V_A = Z_C I_m \end{cases} \tag{4. 18}$$

Based on equation (4. 18), we can determine the expressions for the DPA amplifier voltages as a function of the main amplifier current (I_m) and the I_C value associated with the critical point where the main amplifier becomes saturated and the auxiliary amplifier begins to produce current (I_A).

For Main amplifier voltage (V_m):

$$\begin{cases} V_m = \dfrac{{Z_C}^2}{R_L} I_m, for\ I_m < I_C\ \ (I_A = 0) \Rightarrow V_{m\_max} = \dfrac{{Z_C}^2}{R_L} I_C \\ V_m = V_{m\_max} = V_{DD}\ for\ I_m \geq I_C \end{cases} \tag{4. 19}$$

Where, V_{DD} is the drain bias voltage of the transistor.

When both transistors are saturated, we obtain the following expressions:

$$\begin{cases} V_{m\_max} = V_{A\_max} \Rightarrow, \\ \dfrac{{Z_C}^2}{R_L} \propto I_{m\_max} = Z_C . I_{m\_max} \end{cases} \tag{4. 20}$$

From equation (4. 20), we can deduce that:

$$\propto = \frac{R_L}{Z_C} \tag{4. 21}$$

At the critical point point $I_C = \alpha . I_{m\_max}$, the load impedance Z_{dm} is given by:

$$Z_{dm} = \frac{{Z_C}^2}{R_L} \tag{4. 22}$$

Since $Z_{dm} = \frac{R_{opt}}{\alpha}$, we can verify that:

$$\mathrm{Z_C = R_{opt}} \tag{4. 23}$$

For a main transistor current above the critical value (i.e. $I_m > I_C$), the current I_m will continue to increase while the main transistor voltage V_m remains constant at $V_m = V_{DD}$. Equation (4. 19) indicates that the auxiliary amplifier's voltage gradually increases from 0 to V_{DD} at the same time as the current I_m.

Figure 4. 8 illustrates the variation of the drain voltages of the Main and Auxiliary amplifiers as a function of the Main amplifier current.

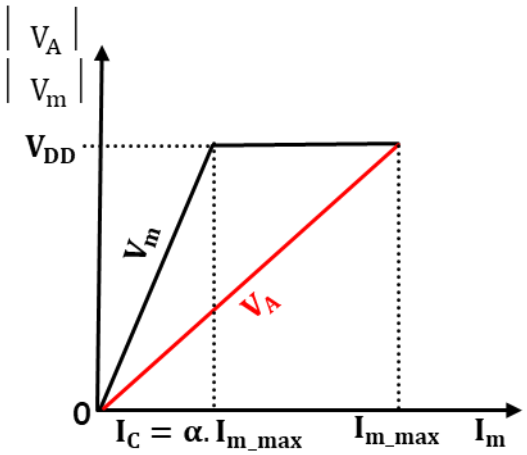


Figure 4. 8: Variation of drain voltages as a function of I_m

4.5 Drain currents variation

Figure 4. 9 illustrates the variation of the Main and Auxiliary drain currents as a function of power level (or I_m).

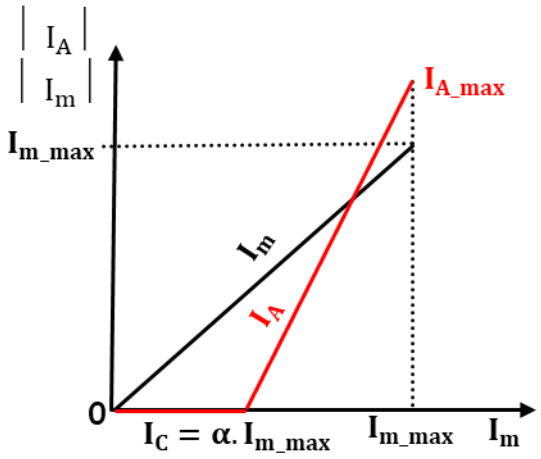


Figure 4. 9: Representation of drain currents as a function of current I_m or power level

As shown in Figure 4. 9, the main amplifier current gradually increases from 0 to I_{m_max}, while the auxiliary amplifier current I_A is zero until it reaches the critical current I_C and then increases progressively. I_{A_max} may be greater than I_{m_max} in a general case where no assumption is made regarding the size of the auxiliary transistor.

The auxiliary current I_A equations is given as [49,50]:

$$\begin{cases} for\ I_m < I_C \Rightarrow I_A = 0 \\ if\ I_m \geq I_C \Rightarrow I_A = k(I_m - I_C) \end{cases} \quad (4.\ 24)$$

From equations (4. 18) and (4. 26), we can determine the expression for k as follows:

$$V_m = \frac{{Z_C}^2}{R_L} I_m - Z_C k(I_m - I_C) \quad (4.\ 25)$$

$if\ I_m \geq I_C$, the voltage V_m remains constant as depicted in Figure 4. 8. Thus:

$$\frac{dV_m}{dI_m} = 0 \Rightarrow \frac{{Z_C}^2}{R_L} - Z_C k = 0 \quad (4.\ 26)$$

From equation (4. 26), the expression of k is found to be:

$$k = \frac{Z_C}{R_L} = \frac{1}{\alpha} \quad (4.\ 27)$$

The auxiliary current expression of equation (4. 26) now becomes:

$$\begin{cases} I_A = 0, for\ I_m < I_C \\ I_A = \frac{1}{\alpha}\left(I_m - \alpha . I_{m\_max}\right), for\ I_m > I_C \end{cases} \quad (4.\ 28)$$

When both amplifiers are saturated, we obtain the following relationship between their maximum drain currents.

$$I_{A\_max} = (\frac{1}{\alpha} - 1).I_{m\_max} \quad (4.\ 29)$$

This expression shows that the size of the amplifiers, or transistors is not identical. Hence, the ratio (r) of the size for the auxiliary amplifier to the main amplifier be expressed as:

$$r = \frac{I_{A\_max}}{I_{m\_max}} = (\frac{1}{\alpha} - 1) \quad (4.\ 30)$$

4.6 Efficiency variation as a function of the power level

4.6.1 Efficiency of the DPA at a low input power level (i.e., operation below the transition point, α)

At low power levels ($I_m < I_C$), the auxiliary current (I_A) is 0. We assume that the main amplifier transistor operates in class B biased mode, and the attained peak current is denoted as I_{m_peak} (refer to Figure 4. 10). The expressions for the D.C. current of the main amplifier (I_{m0}) and the RF current (I_{m1}) at the fundamental frequency (f_o) are given by [12, 49, 50]:

$$\begin{cases} I_{m1} = \frac{I_{m\_peak}}{2} \\ I_{m0} = \frac{I_{m\_peak}}{\pi} \end{cases} \quad (4.\ 31)$$

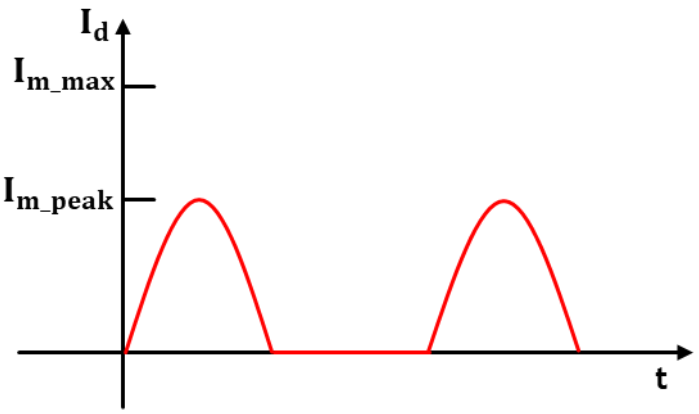


Figure 4. 10: General Half-sinusoidal drain current waveform for the main amplifier

And the expression for the output power of the main amplifier at f_o is given by:

$$\begin{cases} P_{fo,m} = \frac{1}{2}.real(Z_{dm}).{I_{m1}}^2, \\ \quad with\ Z_{dm} = \frac{R_{opt}}{\alpha} \\ P_{fo,m} = \frac{1}{8\alpha}.R_{opt}\,{I_{m\_peak}}^2 \end{cases} \quad (4.\ 32)$$

Similarly, the expression for the main amplifier's D.C. power supply is given by:

$$P_{DC,m} = I_{DC,m}.V_{DD} = \frac{I_{m\_peak}}{\pi}.V_{DD} \quad (4.\ 33)$$

Consequently, the expression of the efficiency at a low input power level when $I_m < I_C$ is given as:

$$D.E = \frac{P_{f_o}}{P_{DC}} = \frac{\pi R_{opt} I_{m\_peak}}{8\alpha.V_{DD}} \quad (4.\ 34)$$

From equation (1.19), we deduce the following expression that will be used to simplify the efficiency equation:

$$\frac{R_{opt}}{V_{DD}} = \frac{2}{I_{m\_max}} \quad (4.\ 35)$$

Thus, the expression of the efficiency of equation (4. 34) now becomes:

$$D.E = \frac{\pi}{4}.\frac{1}{\alpha}.\frac{I_{m\_peak}}{I_{m\_max}} \quad (4.\ 36)$$

4.6.2 Efficiency of the DPA at medium input power level (i.e., operation above the transition point, (α)

At medium power level, when $I_m \geq I_C$, considering the auxiliary amplifier D.C. current I_{A0} and RF current I_{A1} at the fundamental frequency f_o, the expression for the output power of the main amplifier at the fundamental frequency, f_o, is [49,50]:

$$\begin{cases} P_{fo,m} = \frac{1}{2}.real(Z_{dm}).{I_{m1}}^2 = \frac{1}{2} real\left\{\frac{{Z_C}^2}{R_L} - Z_C(\frac{I_{A1}}{I_{m1}})\right\}{I_{m1}}^2 \Rightarrow \\ P_{fo,m} = \frac{1}{2}\left\{\frac{R_{opt}}{\alpha} - Z_C(\frac{I_{A1}}{I_{m1}})\right\}{I_{m1}}^2 \end{cases} \quad (4.\ 37)$$

And that of the auxiliary amplifier at f_o is given as:

$$\begin{cases} P_{f_{o,A}} = \frac{1}{2}.real(Z_{da}).{I_{A1}}^2 = \frac{1}{2} real\left\{Z_C(\frac{I_{m1_o}}{I_{A1}})\right\}{I_{A1_o}}^2 \Rightarrow \\ P_{f_{o,A}} = \frac{1}{2} real\left\{Z_C(\frac{I_{A1_o}}{I_{m1_o}})\right\}{I_{m1_o}}^2 \end{cases} \quad (4.\ 38)$$

From equations (4. 37) and (4. 38), the expression for the total power of the Doherty amplifier at Fo is given by:

$$\begin{cases} P_{T,\,f_o} = P_{f_{o,m}} + P_{f_{o,A}} = \frac{1}{2}.\frac{R_{opt}}{\alpha}.{I_{m1}}^2 \\ P_{T,\,f_o} = \frac{1}{8}.\frac{R_{opt}}{\alpha}.{I_{m\_peak}}^2 \end{cases} \Rightarrow \quad (4.\ 39)$$

Subsequently, the expression of the D.C. power supply for the Main and Auxiliary amplifiers when $I_m \geq I_C$ is given as follows:

Assuming both transistors are biased in class B mode in this case, then we write:

$$\begin{cases} P_{DC,m} = I_{m0}.V_{DD} = \frac{I_{m\_peak}}{\pi}.V_{DD} \\ P_{DC,A} = I_{A0}.V_{DD} = \frac{I_{A\_peak}}{\pi}.V_{DD} \end{cases} \quad (4.\ 40)$$

Then, the total DC power $P_{T,DC}$ becomes:

$$P_{T,DC} = P_{DC,m} + P_{DC,A} = \frac{V_{DD}}{\pi}(I_{m\_peak} + I_{A\_peak}) \quad (4.\ 41)$$

From equation (4. 28), the expression for I_A in terms of I_m is: $I_{A\_peak} = \frac{1}{\alpha} I_{m\_peak} - I_{m\_max}$

Thus, $P_{T,DC}$ expression in terms of main amplifier current becomes:

$$P_{T,DC} = \frac{V_{DD}}{\pi}.I_{m\_max}\left\{\left(\frac{1}{\alpha}+1\right)\frac{I_{m\_peak}}{I_{m\_max}} - 1\right\} \quad (4.\ 42)$$

From equations (4. 39) and (4. 42) and using the expression of equation (4. 35) of R_{opt} , we deduce the expression of the efficiency when $I_m > I_C$ as:

$$D.E = \frac{\pi\left(\frac{I_{m\_peak}}{I_{m\_max}}\right)^2}{4\alpha\left\{\left(\frac{1}{\alpha}+1\right)\frac{I_{m\_peak}}{I_{m\_max}} - 1\right\}} \quad (4.\ 43)$$

4.6.3 Efficiency of the DPA at the maximum input power level

At high input power levels, the main and auxiliary amplifiers operate in the saturated region, as such, I_{m_peak} tends toward I_{m_max}. Consequently, the drain efficiency of the DPA at high input power is optimum by substituting $I_{m\_peak} = I_{m\_max}$ in equation (4. 43) to give:

$$D.E_{max} = \frac{\pi}{4} = 78.5\% \qquad (4.\ 44)$$

This maximum efficiency value is independent of α, i.e. the size of the transistors.

Figure 4. 11 illustrates the plot of the identical two-stage DPA (r=1) efficiency at $= \frac{1}{2}$, and that of the class B amplifier efficiency against $(\frac{I_{m\_peak}}{I_{m\_max}})$.

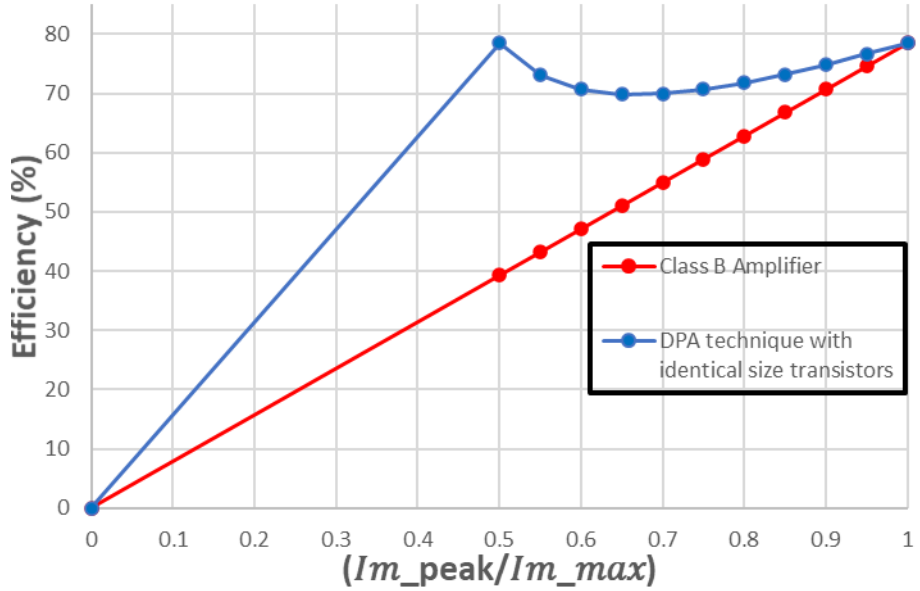


Figure 4. 11: Power efficiencies versus $(\frac{I_{m\_peak}}{I_{m\_max}})$ for classical Doherty power amplifier (DPA) and class B amplifier.

It can be observed from Figure 4. 11 that for identical transistor sizes, the DPA drain efficiency increases linearly up to the transition point (at $\frac{I_{m\_peak}}{I_{m\_max}} = 0.5$), then decreases as the auxiliary amplifier becomes active, and finally increases again until it reaches the maximum efficiency of 78.5% at high input drive. Additionally, the efficiency of the DPA configuration has an advantage over the conventional class B biased amplifier for achieving maximum efficiency of 78.5% at 6 dB power backoff (i.e., when the transition point $\alpha = \frac{1}{2}$).

4.6.4 Calculation of output power backoff (OBO)

The reduced power level at which the efficiency is maintained at its maximum value is defined as the difference between the peak power and the power at the transition point and is expressed as [49,50]:

$$OBO = 10\log\left(\frac{P_{max}}{P_{\alpha}}\right) \tag{4. 45}$$

Where the expressions for P_{max} and P_{α} are derived from equation (4. 32) and are given by:

$$\begin{cases} P_{max} = \frac{1}{8\alpha}.R_{opt}\ {I_{m\_max}}^2 \\ P_{\alpha} = \frac{1}{8\alpha}.R_{opt.}\alpha^2\ .{I_{m\_max}}^2 \end{cases} \tag{4. 46}$$

From equation (4. 46), the OBO expression now becomes:

$$OBO = 10\log\left(\frac{1}{\alpha^2}\right) \tag{4. 47}$$

Thus, the OBO for a conventional Doherty power amplifier with $\alpha = \frac{1}{2}$ is 6 dB.

4.7 Doherty power amplifier techniques with an auxiliary transistor that is twice the size of the main transistor

Having studied the DPA technique with identical-size transistors, it is possible to design a two-stage DPA with an auxiliary transistor that is twice the size of the main transistor. Hence, the size of an auxiliary transistor can be greater than that of the main transistor, and the size of the auxiliary transistor depends on the application and the shape of the signal to be amplified. As a result, the transition point (α) is shifted according to the signal's peak-to-average power ratio (PAPR). Adjusting the transition point makes it possible to obtain a range of variations in power levels at which maximum efficiency is achieved [46]. If the signal to be amplified has a high PAPR, the transition point should be low to maximize efficiency at low power levels.

The expressions for the maximum saturation currents of a DPA technique with an auxiliary transistor size twice as large as the main transistor are related as [49,50]:

$$I_{A\_max} = 2.I_{m\_max} \tag{4. 48}$$

From equation (4. 29), the transition point for this case is: $\alpha = \frac{1}{3}$

Thus, the main goal of this DPA technique is to make the auxiliary transistor more clamped than the main transistor, thereby delivering twice the main transistor's current to the load. In this case, the resistive load impedances presented to the output of both amplifiers are given by:

$$\begin{cases} \mathrm{Z_{dm}} = \dfrac{{Z_C}^2}{\mathrm{R_L}} - \mathrm{Z_C}\left(\dfrac{2.I_{m\_peak}}{I_{m\_peak}}\right) \Rightarrow \dfrac{{Z_C}^2}{R_L} - 2Z_C = R_{opt} \\ \mathrm{Z_{da}} = \mathrm{Z_C}\left(\dfrac{I_{m\_peak}}{2.I_{m\_peak}}\right) \Rightarrow \dfrac{Z_C}{2} = \dfrac{R_{opt}}{2} \end{cases} \quad (4.\ 49)$$

Consequently, both amplifiers are designed to deliver maximum power at high power levels when the load impedance presented at their output is R_{opt} for the main transistor and $\frac{R_{opt}}{2}$ for the auxiliary transistor.

Based on the above analysis, we can deduce the following expressions:

$$\begin{cases} \mathrm{Z_C} = R_{opt} \\ R_L = \dfrac{R_{opt}}{3} \end{cases} \quad (4.\ 50)$$

The output power backoff of the DPA method is 9.5 dB when the size of the Auxiliary transistor is twice as large as the main transistor, as calculated using equation (4. 47).

Table 4. 2 summarises the load impedance variation of the Main and auxiliary transistors as a function of the input power level when the size of the Auxiliary transistor is twice as large as the main transistor.

Table 4. 2: Load impedance variations of the DPA method for a case when the auxiliary transistor is twice as the size of the main transistor

Input power level (P_{in})	Main amplifier load impedance ($\mathrm{Z_{dm}}$)	Auxiliary amplifier load impedance ($\mathrm{Z_{da}}$)
For: $P_{in} < P_{\alpha}$(power at transition point)	$3R_{opt}$	∞
For: $P_{\alpha} < P_{in} < P_{max}$	$3R_{opt}\ to\ R_{opt}$	$\infty\ to\ \dfrac{R_{opt}}{2}$
For : $P_{in} = P_{max}$	R_{opt}	$\dfrac{R_{opt}}{2}$

Figure 4. 12 compares the performance of the DPA in two scenarios: when the auxiliary transistor size is the same as the main transistor, and when it is twice the size of the main transistor.

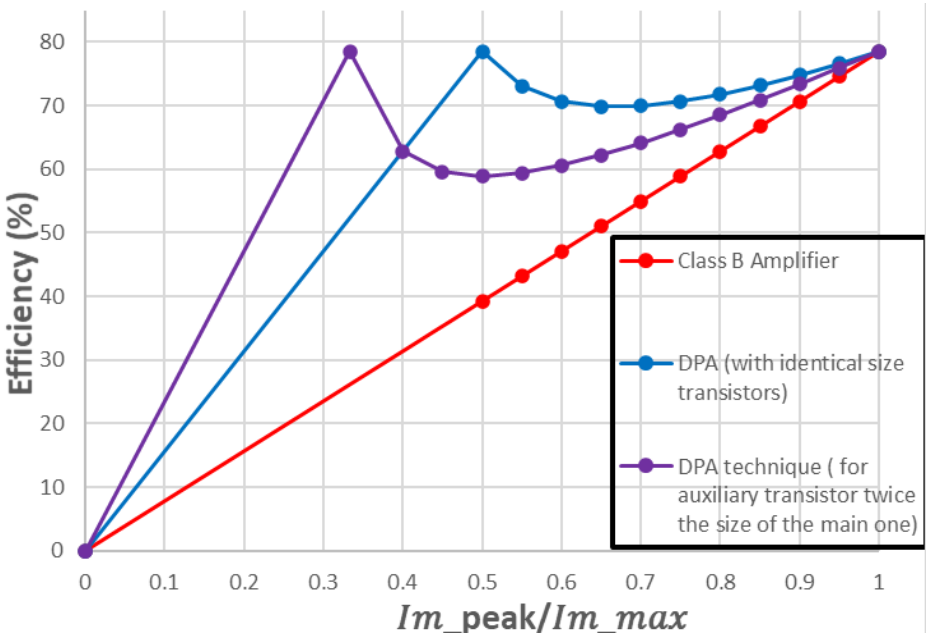


Figure 4. 12: Comparison of Efficiencies of DPA

It can be seen from Figure 4. 12 that the transition point for the DPA case where the size of the auxiliary amplifier is two times that of the main transistor has shifted from an input power drive of $\alpha = \frac{1}{2}$ to $\frac{1}{3}$, making it possible for the DPA to saturate and reach maximum efficiency at much lower power than with the identical-size case. However, in this case, the efficiency of the DPA between the transition point and maximum efficiency is lower than that of a DPA with the same transistor size. In an asymmetrical DPA case, the power delivered to the auxiliary transistor is twice that of the main transistor, and the impedance seen by the main transistor varies from R_{opt} to $3R_{opt}$. The impedance variation of the asymmetrical DPA architecture is higher than that of the DPA with identical-size transistors.

For more details on the Doherty amplifiers, Figure 4. 13 shows a conventional DPA structure consisting of an additional quarter-wave transmission line at the output of the Doherty amplifier. This quarter-wave transformer (Z_{C2}) at the load side of the DPA transforms the modulated impedance at node A to a 50-ohm system impedance to guarantee maximum power transfer to the load. The power splitter at the input of the DPA divides the RF input signal between the main and auxiliary amplifiers.

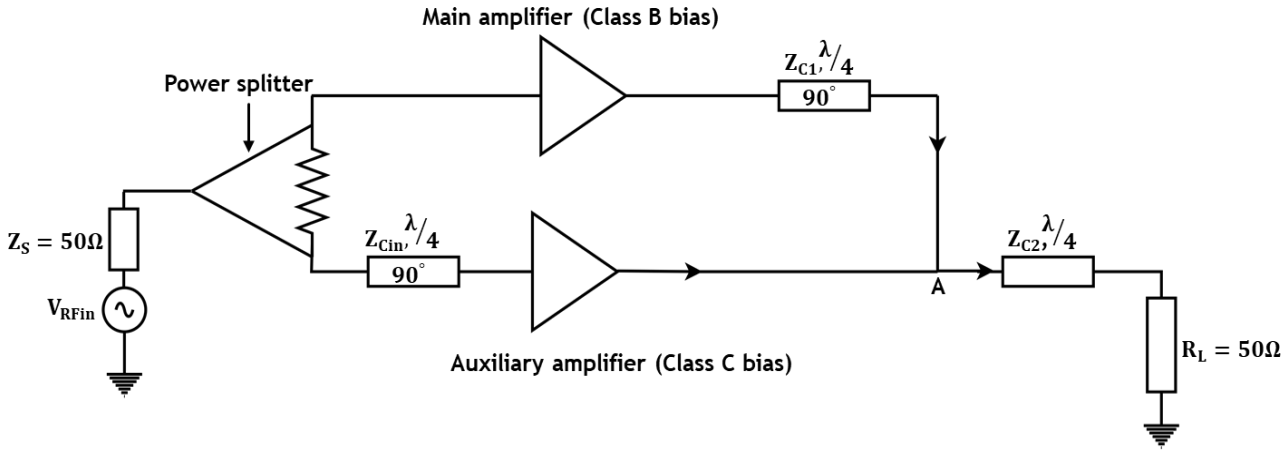


Figure 4. 13: Block diagram of the conventional two-stage DPA architecture

4.8 Design and implementation of a wideband Doherty power amplifier

4.8.1 Introduction

The Doherty power amplifier (DPA) has been proven to be highly efficient in several PA architectures, especially when used with high dynamic modulated signals. The goal is to use a single amplifier for a wide range of frequency bands instead of multiple narrowband amplifiers. This reduces system complexity and power consumption and improves the system's flexibility. However, the limited bandwidth of the architecture has been a challenge for its development. Manuel Cavarroc addressed this challenge in his article [51], presenting a DPA architecture that uses GaN HEMT transistors to achieve broadband operation over a 40% fractional bandwidth (FBW). This design was carried out in collaboration between the NXP semiconductors and XLIM research institute.

First, we will describe the DPA architecture designed by [51], which includes an input group delay control circuit and the corresponding circuit developed by the NXP manufacturing company. Thereafter, the performance obtained is presented. The amplifier results obtained are used as a reference when applying an optimization technique to enhance the bandwidth of a DPA using the fmincon MATLAB algorithm described in Chapter 2 of this thesis.

4.8.2 The description of the circuit

The DPA circuit developed by [51] can be used by the 5th generation mobile telephone base station in the frequency bands of 1.8 GHz to 2.7 GHz, with a centre frequency fc=2.25 GHz. It is a compact power

amplifier circuit delivering 15 watts of average power in each path of the massive multiple input multiple outputs (MIMO) transmitter architecture (32T or 64T) for small cell coverage infrastructure.

Figure 4. 14 shows the inverted GaN-based transistor DPA topology designed by Reference [51]. This inverted DPA architecture achieves a relatively large bandwidth but has increased area occupancy [52, 53].

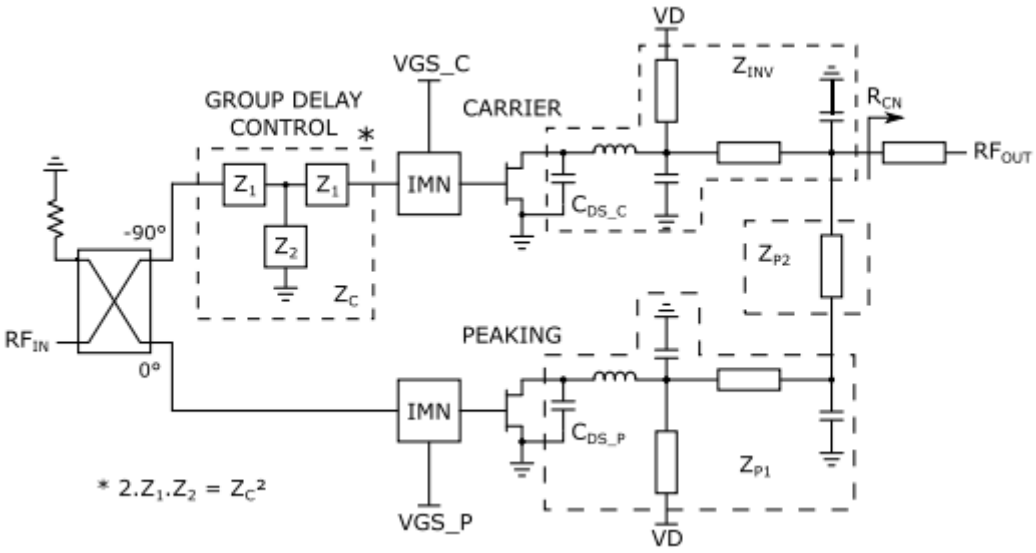


Figure 4. 14: The schematic circuit of the DPA developed by [51]

The output includes the quarter-wave transmission lines at the output of the main and auxiliary amplifiers which are designed in the form of a quasi-transmission line network to absorb the transistor output capacitance. Thus, the equivalent reactance at the common node maintains a low impedance in the current source reference plane at the second harmonic component. At the input, silicon-based integrated passive devices (IPDs) are used for the design of wideband input matching networks (IMNs) to increase the low input impedance presented to the transistor gate. The passive elements in the matching network consist of integrated capacitors and bonding wire inductors. Additionally, a commercial quadrature is employed at the input side of the DPA for power splitting and phase delay.

4.8.3 Adjustment of group delay

A limiting factor to the improvement of DPA bandwidth is the non-uniform phase dispersion between the main (carrier) and the auxiliary (peaking) amplifiers at the output [54,55]. A study by [51] revealed that the input phase difference and its variation across the frequency range of interest can be utilized to optimize the load impedance dispersion characteristics in the full power (FP) state. This optimization enables a better trade-off between peak power and back-off power, enhancing the bandwidth.

The optimum value for the corresponding group delay can be determined by adjusting the phase difference at the input of the main amplifier.Thus, the expression for the auxiliary amplifier current (I_a) during the load modulation is given as a function of the input phase difference ($\Delta\phi$) between the main and auxiliary amplifiers as:

$$I_a = |r|.I_m.e^{-j\Delta\phi} \quad (4.\ 51)$$

Where I_m is the main amplifier current, |r| is the ratio of the magnitude of the auxiliary to the main amplifier current and $\Delta\phi$ is the phase difference.

Consequently, the expression of the phase difference for a linear phase variation around the centre frequency (f_c) is given by:

$$\Delta\phi(\omega) = -\frac{\pi}{2} - \Delta\tau_{gd}.(\omega - \omega_o) \quad (4.\ 52)$$

Where; $\Delta\tau_{gd}$ is the relative group delay between the main and the auxiliary input paths.

The voltage standing wave ratio (VSWR) is used to evaluate the performance of the DPA both at full power and back-off power levels. Hence, adjusting the group delay can vary the VSWR of the main and auxiliary amplifiers at full power.

Therefore, a group delay value of $\Delta\tau_{gd} = 0$ corresponds to a constant 90° phase, as achieved with an input hybrid coupler.

For our study, the following expression of the group delay is used:

$$\Delta\tau_{gd} = \frac{1}{\gamma.2f_o} \quad (4.\ 53)$$

And γ is a variable being adjusted to improve the bandwidth of the VSWR.To show the effect of $\Delta\tau_{gd} = \frac{1}{\gamma.2f_o}$, we considered a simple output circuit composed of 4 quarter-wave (λ/4) transmission lines. A Peaking/Carrier gate periphery ratio |r| = 1.5 is chosen by [51] to maintain efficiency at back-off, on 8 dB theoretically. For a 100 W Doherty and a drain bias VD = 48 V, the optimal load line is $R_{OPT,\,C}$ = 18 Ω for the main or Carrier amplifier and $R_{OPT,\,P}$ = 12 Ω for the auxiliary or peaking amplifier.

The plot of the VSWR results achieved by [51] against different values of the combining node resistance (R_{CN}) of the DPA when $|r| = 1.5$ for the 2 cases with and without relative group dealy ($\Delta\tau_{gd} = 0$ and

$\gamma = 1.13$) is illustrated in Figure 4. 15. VSWR values are calculated at the band edge frequencies of 0.8fc=1.8 GHz and 1.2fc=2.7 GHz, corresponding to 40% of fractional bandwidth.

It can be seen from the result that it is possible to lower the output frequency load dispersion difference at full power to an optimum point corresponding to the frequency dispersion at low power by adopting an over-compensation strategy of ($\gamma = 1.13$) on the input relative group delay between the main and auxiliary paths of the amplifier. Thus, a VSWR of 1.16 at a combining node resistance value of $R_{CN} = 28\ \Omega$ is obtained over a 40% fractional bandwidth, allowing wideband behaviour.

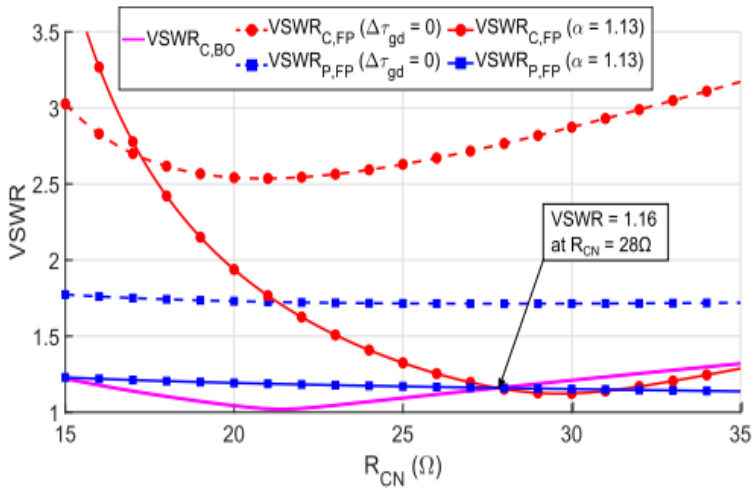


Figure 4. 15: Comparison between the calculated VSWR with and without relative group delay engineering at band edge frequencies [51]

As illustrated in Figure 4. 14, a network named “group delay control” is introduced at the input of the main amplifier. This network is designed using bandpass filter theory to achieve a flat group delay response adjusted to the optimum value. An order of n =3 is selected to minimize the transmission and return losses.

Figure 4. 16 shows the frequency response of the phase difference and the relative group delay over the desired frequency range of 1.8 GHz to 2.7 GHz.

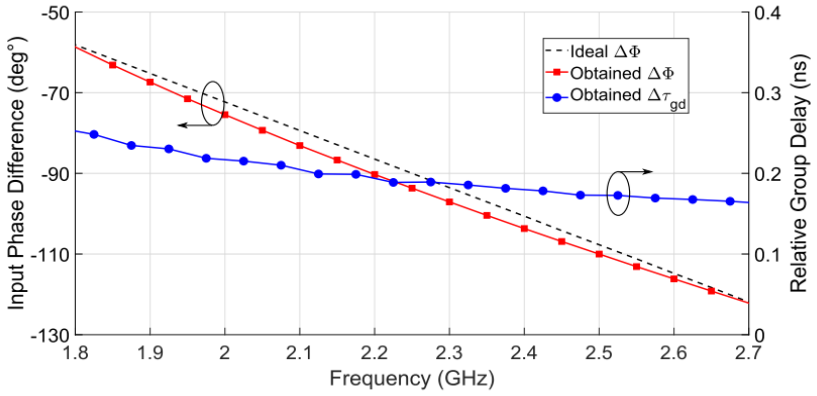


Figure 4. 16: Comparison of an ideal and obtained input phase difference ($\Delta\phi$) resulting in relative group delay ($\Delta\tau_{gd}$) [51]

4.8.4 The performances of the measured and experimental results obtained

A multi-layer, 1 mm-thick low insertion loss RF substrate ($d_k = 3.35$) was used by [51] to fabricate the Doherty power amplifier. It is a 50 Ω input-output multi-chip module assembly in an LGA package measuring 20mm by 16mm, as shown in Figure 4. 17 below.

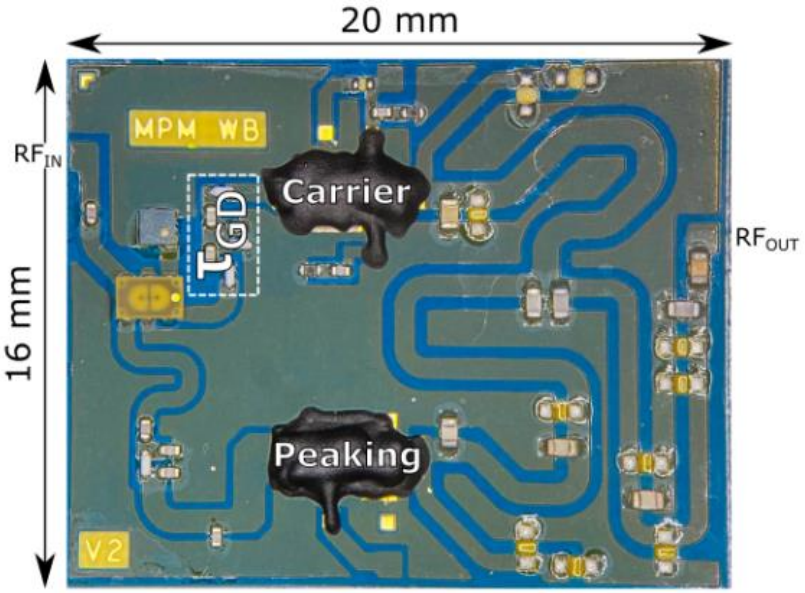


Figure 4. 17: A photograph of the multi-chip module DPA [51]

Furthermore, IPDs and GaN dice are attached to copper coins inserted through the substrate for thermal management. The module was soldered to an evaluation circuit board (EVB) with RF and DC access through a reflow process to perform measurements. The total area occupied by the DPA circuit now becomes 30 x 30 mm when the location of the RF bypass capacitor on the EVB is taken into consideration. Moreover, both the main and auxiliary amplifiers have the same drain-bias voltage of V_{ds}

= 48V, while the gate-bias voltages of the main and auxiliary amplifiers are set to -2.5V and -5.4V, respectively.

Consequently, Reference [51] conducted a comparison of the simulated and measured S-parameter results of his proposed DPA in Figure 4. 14. As depicted in Figure 4. 18, the results show a good location match of the auxiliary (peaking) amplifiers' OFF-state zeroes in transmission response and achieve 14.4 –17 dB small signal gain around the frequency band of 1.8 GHz to 2.7 GHz.

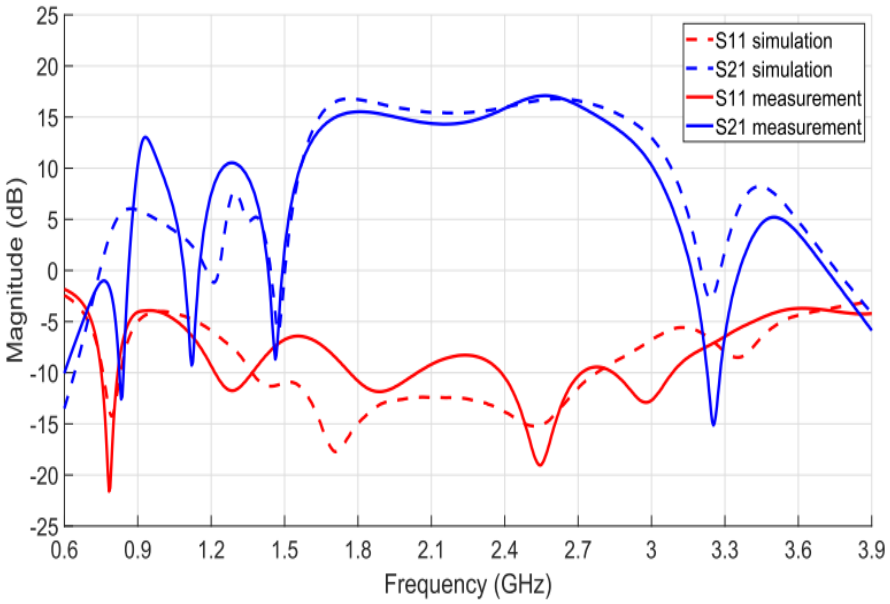


Figure 4. 18: The comparison of the measured and simulated S-parameters [51]

Additionally, the result in Figure 4. 19 shows the plot of the DPA measured efficiency and gain versus output power under the stimulus of a continuous wave (CW) signal.

As seen from the result, the dynamic behaviour of the fabricated DPA is maintained with relatively good AM/AM linearity over the 1.8 GHz to 2.7 GHz frequency band. At 8 dB output power back-off (OBO), the drain efficiency of the DPA over the desired frequency band is in the range of 51% to 57%.

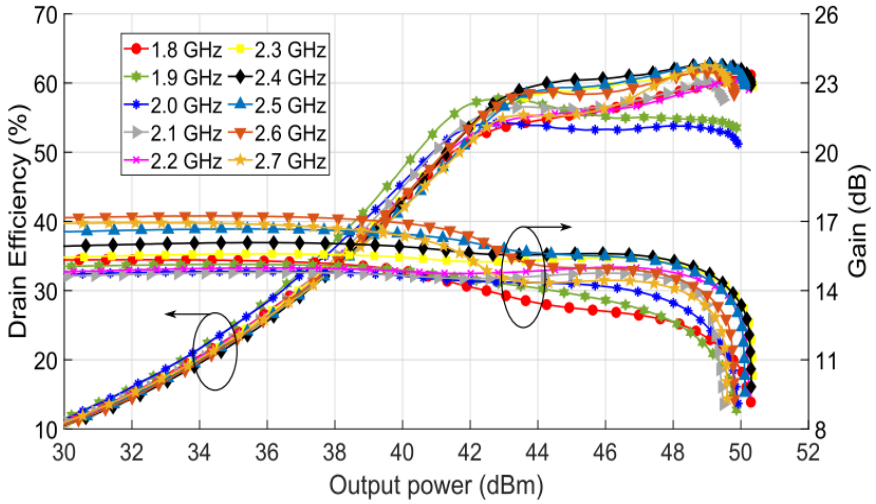


Figure 4. 19: Measured drain efficiency and gain performances under CW stimulus [51]

The amplifier has also been evaluated in terms of linearity, using different multiband scenarios and Digital Pre-Distortion systems developed by NXP.

In summary, the broadband capability of the DPA designed and fabricated by [51] is improved by controlling the input group delay at the input of the main (carrier) amplifier. Thus, the input group delay is a key parameter to consider when designing a large bandwidth Doherty amplifier. This result will be used to propose a design procedure that focuses on optimizing the group delay and the values of the Doherty amplifier output networks in the next section of this thesis.

4.9 Study of the frequency behaviour of an ideal elements of a DPA

4.9.1 Conventional DPA Architecture

4.9.1.1 An overview of the circuit

The Doherty power amplifier is generally considered to have low-bandwidth characteristics. In this part, the study of the frequency response of the Doherty output network is carried out both at high and low power levels. To do this, we considered an ideal GaN-based transistor model consisting of only a controlled drain current source and analyzed the frequency response on the main and auxiliary paths. This analysis is considered at the back-off power level when the auxiliary amplifier is in the OFF state and at the full power level when both amplifiers are active.

The conventional DPA circuit for analysing the frequency behaviour is composed of an output quarter-wave transmission line that presents the impedance Z_{CN} to the common node and the impedance

transformer at the output of the main amplifier, which is represented by the [ABCD] transmission matrix, as illustrated in Figure 4. 20 below.

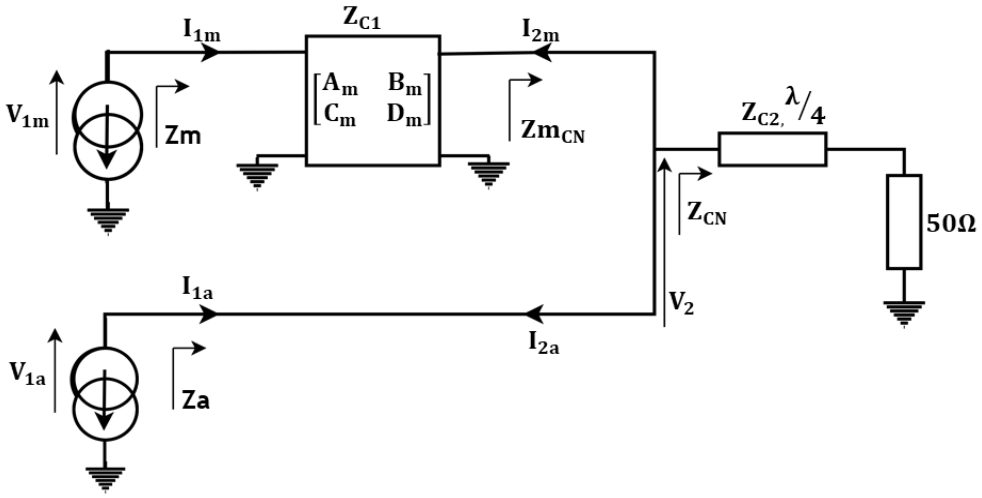


Figure 4. 20: The conventional DPA circuit with the output quarter-wave transmission line of the main amplifier represented by the [ABCD] transmission matrix.

From equation (4. 51), the expression for the ratio of the auxiliary to the main amplifier current sources is given as:

$$r = \frac{I_{1a}}{I_{1m}} = |r|.\, e^{-j\Delta\phi} \tag{4. 54}$$

The term "$\Delta\phi$", represents the phase difference between the two currents, equal to $\frac{\pi}{2}$ for $\omega = \omega_o$, which varies with frequency depending on the DPA circuit topology used. Its expression is given in equation (4. 52), as a function of the group delay.

4.9.1.2 Equations for describing the frequency behaviour of a conventional DPA

The [ABCD] transmission matrix facilitates the study of the frequency behaviour of a DPA. For example, it simplifies the calculation of the input impedance (Zin) of a quadripole with a loaded output impedance (Zout), as shown in Figure 4. 21.

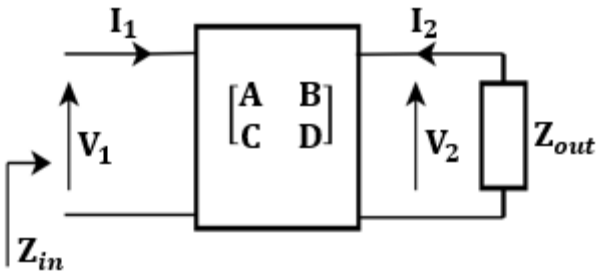


Figure 4. 21: The calculation of input impedance (Zin) of a quadripole loaded with (Zout) with transmission matrix

By definition, the input variables of the quadripole shown in Figure 4. 21 are given by the following equations:

$$\begin{cases} V1 = A.V2 - B.I2 \\ I1 = C.V2 - D.I2 \end{cases} \quad (4.\ 55)$$

Thus, the input impedance Zin is obtained from equation (4. 55) as the ratio of V1/I1.

$$Zin = \frac{A.Zout + B}{C.Zout + D} \quad (4.\ 56)$$

with:

$$\text{Zout} = -\frac{V2}{I2} \quad (4.\ 57)$$

With the auxiliary amplifier switched off at the back-off power level, the analysis of the conventional DPA circuit in Figure 4. 20 is simplified. Thus, the load section of the circuit now consists of only the quadripole matrix [Am Bm Cm Dm] at the output of the main amplifier cascaded with the quadripole matrix [ABCD] of the output quarter-wave transmission line.

Therefore, the impedance presented at the output of the main amplifier at the back-off (BO) power level is given as:

$$Zm\_BO = \frac{Ao.50 + Bo}{Co.50 + Do} \quad (4.\ 58)$$

Where:

$$\begin{bmatrix} Ao & Bo \\ Co & Do \end{bmatrix} = \begin{bmatrix} Am & Bm \\ Cm & Dm \end{bmatrix} . \begin{bmatrix} \cos\theta l & \text{j. } Z_C . \sin\theta l \\ \frac{\text{jsin}\,\theta l}{Z_C} & \cos\theta l \end{bmatrix} \quad (4.\ 59)$$

At full power level, a relationship is first established between the current I_{2m} and I_{2a} in Figure 4. 20. Knowing that the voltage V_2 is the voltage across the impedance Z_{CN} at the common node through which the currents I_{2m} and I_{2a} flow.

$$V_2 = -Z_{CN}(I_{2m} + I_{2a}) \quad (4.\ 60)$$

The main amplifier current is written as:

$$I_{1m} = -Cm.Z_{CN}(I_{2m} + I_{2a}) - Dm.I_{2m} \quad (4.\ 61)$$

Additionally, the ratio of the main amplifier current to the auxiliary amplifier current for the conventional DPA is given by:

$$r = \frac{I_{1a}}{I_{1m}} = -\frac{I_{2a}}{I_{1m}} \quad (4.\ 62)$$

From equations (4. 61) and (4. 62), we obtained:

$$\frac{I_{2a}}{I_{2m}} = \frac{-r.(Z_{CN}.Cm + Dm)}{r.Z_{CN}.Cm - 1} \quad (4.\ 63)$$

The impedance presented at the output of the matching quadripole at the main amplifier path, i.e. in the plane of Z_{CN}, is written as:

$$Zm_{CN} = -\frac{V_2}{I_{2m}} = Z_{CN}.(1 + \frac{I_{2a}}{I_{2m}}) \quad (4.\ 64)$$

Thus, equation (4. 64) makes it possible to calculate the impedance Zm seen by the main amplifier at full power (FP) and is therefore given as:

$$Zm = \frac{Am.Zm_{CN} + Bm}{Cm.Zm_{CN} + Dm} \quad (4.\ 65)$$

The impedance presented at the auxiliary amplifier path, i.e. in the plane of Z_{CN}, is written as:

$$Za = -\frac{V_2}{I_{2a}} = Z_{CN}.(1 + \frac{I_{2m}}{I_{2a}}) \quad (4.\ 66)$$

The above equations (4. 64) to (4. 66) are used to calculate the impedance presented to the drain of each transistor versus frequency for different current ratio r.

4.9.1.3 Analysing the frequency characteristic of the conventional DPA

The design of the DPA aims to achieve a VSWR of a maximum value of 1.2, which corresponds to a reflection coefficient value of less than -20.8 dB over the widest possible frequency bands with a target fractional bandwidth of 40% around 2.5 GHz, i.e., from 2 to 3 GHz.

We begin our analysis by considering the simulation of the frequency behaviour of the conventional DPA in Figure 4. 20 using only quarter-wave transmission lines.

Both transistors in the DPA circuit are presumed to deliver an equal amount of current at a full power level (i.e., |r|=1). When operating at high power, each transistor is presented with an optimum impedance of Ropt=36 Ω at the output. Conversely, at the back-off power level, the main amplifier's output is presented with an optimal impedance of Ropt=72Ω.

Consequently, Table 4. 3 summarises the conventional DPA circuit parameter values designed using quarter-wave transmission lines.

Table 4. 3: The conventional DPA circuit parameter values

Current ratio	Phase slope parameter	Opt. load at Full Power	Z_c main ¼ wave	Z commun node	Z_c output ¼ wave
$\|r\|$	γ	Ropt	$Z_{C1} = Ropt$	$Z_{CN} = \frac{Ropt}{1+\|r\|}$	$Z_{C2} = \sqrt{50.Z_{CN}}$
1	2	36 Ω	36 Ω	18 Ω	30 Ω

Figure 4. 22 illustrates the plot of the reflection coefficient in dB and the VSWR performance against frequency for the main amplifier at back-off power and for the main and auxiliary amplifiers at full power levels. However, it should be noted that the main amplifier determines the bandwidth limit of the DPA.

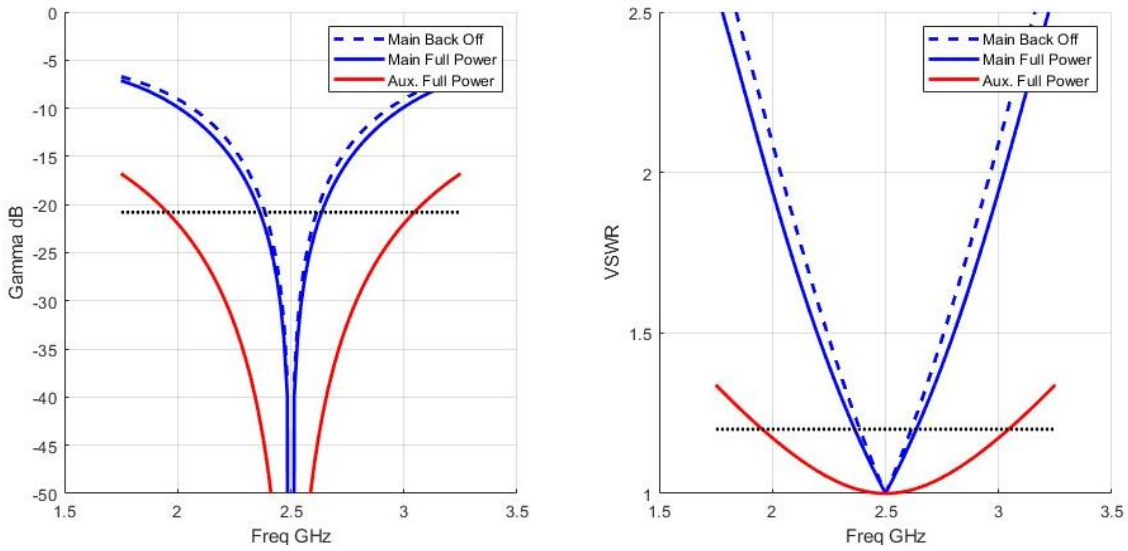


Figure 4. 22: Frequency response result of the reflection coefficient in dB and VSWR with Table 4. 3 element values

4.9.1.3.1 The effect of the optimum load impedance Ropt on the bandwidth of the conventional DPA

To evaluate the effects of adjusting some design parameters on the bandwidth of the DPA, the reflection coefficient and the VSWR are evaluated at the edge of the targeted bandwidth, either at 2 GHz or 3 GHz.We commence the analysis by first adjusting the optimum drain resistance of the DPA to see the effect on the bandwidth. Modifying the optimum load impedance means that the size of the devices and output power level are changing accordingly. The result is shown in Figure 4. 23.

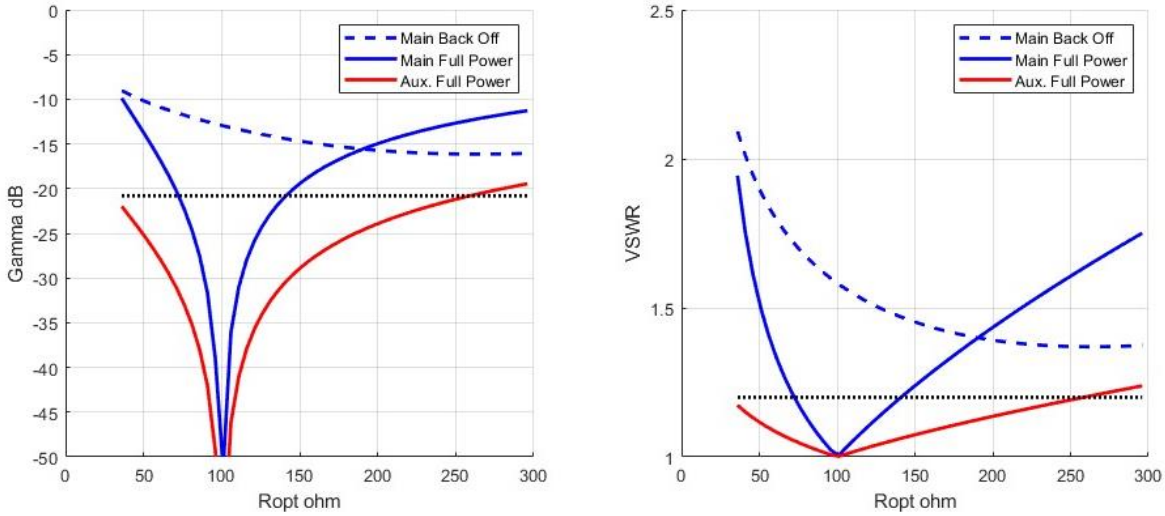


Figure 4. 23: Reflection coefficient in dB and VSWR against optimum drain resistance (Ropt)

As seen in Figure 4. 23, a perfect match is obtained at full power when the optimum drain load resistance value is Ropt = 100Ω which corresponds to characteristic impedances of $Z_{CN} = Z_{C2} = 50\ \Omega$, implying that a 100 Ω impedance is seen by each amplifier branch, hence $Z_{C1} = 100\ \Omega$. It can also be observed from the result that the bandwidth of the DPA at the back-off power level is always limited. As such, varying the optimum drain resistance affects the output power or the behaviour of the amplifier.

4.9.1.3.2 The effect of the current ratio |r| on the bandwidth of the conventional DPA

In this case, the size of the auxiliary amplifier is modified to be higher or lower than that of the main amplifier, thereby making the current ratio (|r|) value respectively greater or lower than one. Thus, the effect of varying the ratio size of the two transistors on the bandwidth is illustrated in Figure 4. 24.

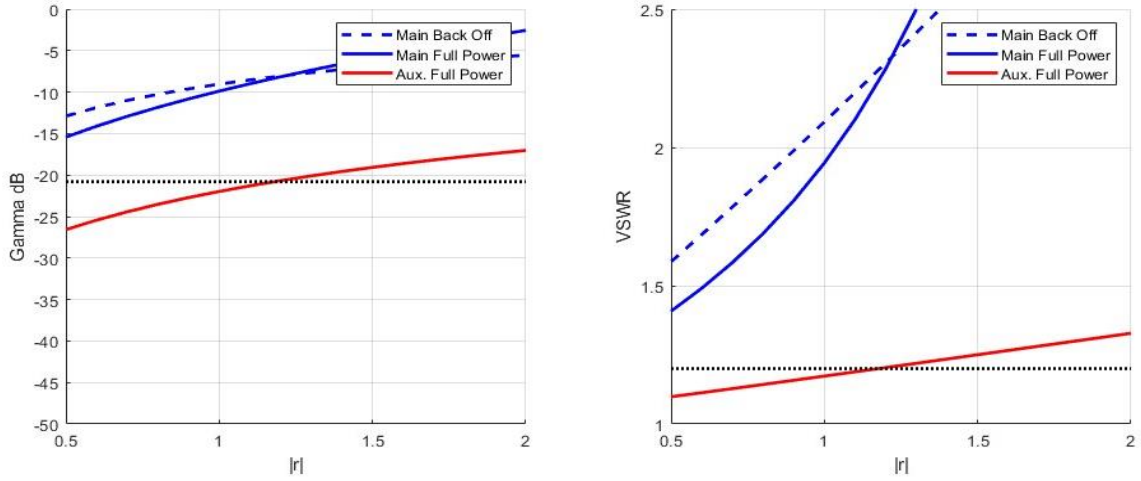


Figure 4. 24: Reflection coefficient in dB and VSWR against current ratio (|r|)

It can be seen from the result that the bandwidth of the amplifier can be improved by decreasing the current ratio. However, the back-off performance of the DPA, which is our main concern in the design of the DPA, is degraded when the current ratio is decreased.

4.9.1.3.3 The effect of the phase slope on the bandwidth of the conventional DPA

The phase slope parameter γ is used for adjusting the group delay ($\Delta\tau_{gd}$). Figure 4. 25 therefore shows the plot of the reflection coefficient and VSWR as a function of the phase slope parameter (γ). Reducing the phase slope parameter affects the DPA performance at high power levels and can be used to improve the bandwidth of either the auxiliary or the main amplifier or to find a compromise between them. In our case, this is achieved at $\gamma = 1.1$.

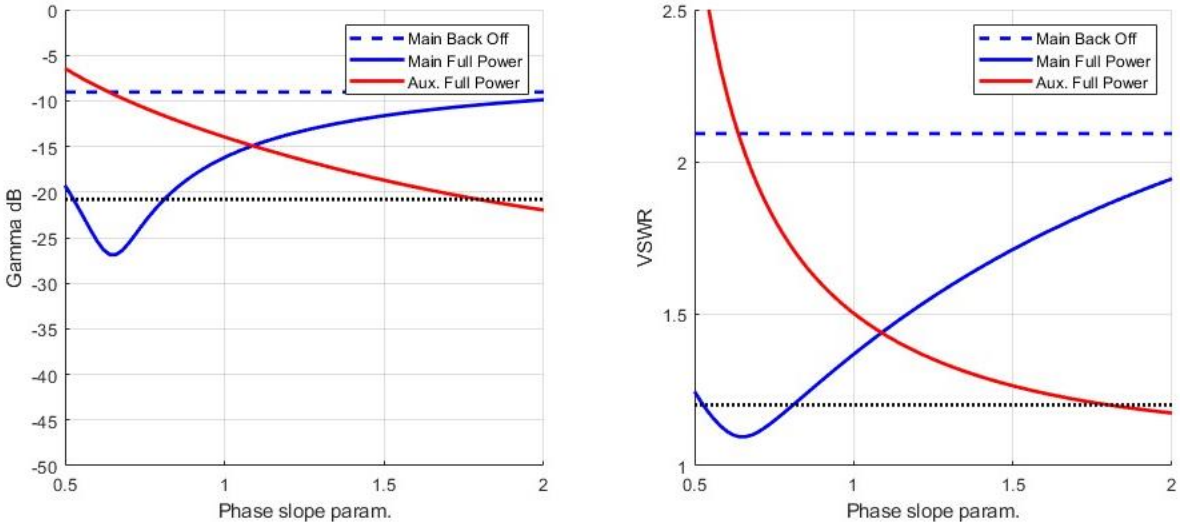


Figure 4. 25: The result of the reflection coefficient in dB and VSWR of a DPA at full and backoff power level as a function of the phase slope parameter (γ)

4.9.1.3.4 The effect of the common node impedance Z_{CN} on the bandwidth of the conventional DPA

At the centre frequency f_o, the value of the impedance Z_{CN} is chosen to ensure perfect matching at back-off and full power levels. Thus, the common node impedance expression at the centre frequency fo is given as $Z_{CN} = R_{CN} = \frac{Ropt}{1+|r|}$. Therefore, by adjusting the value of the impedance R_{CN}, the matching condition of the DPA at f_o will be altered. For example, Figure 4. 26 shows the frequency response performance of the conventional DPA in terms of the reflection coefficient and VSWR at a common node impedance value of $R_{CN} = 26\ \Omega$.

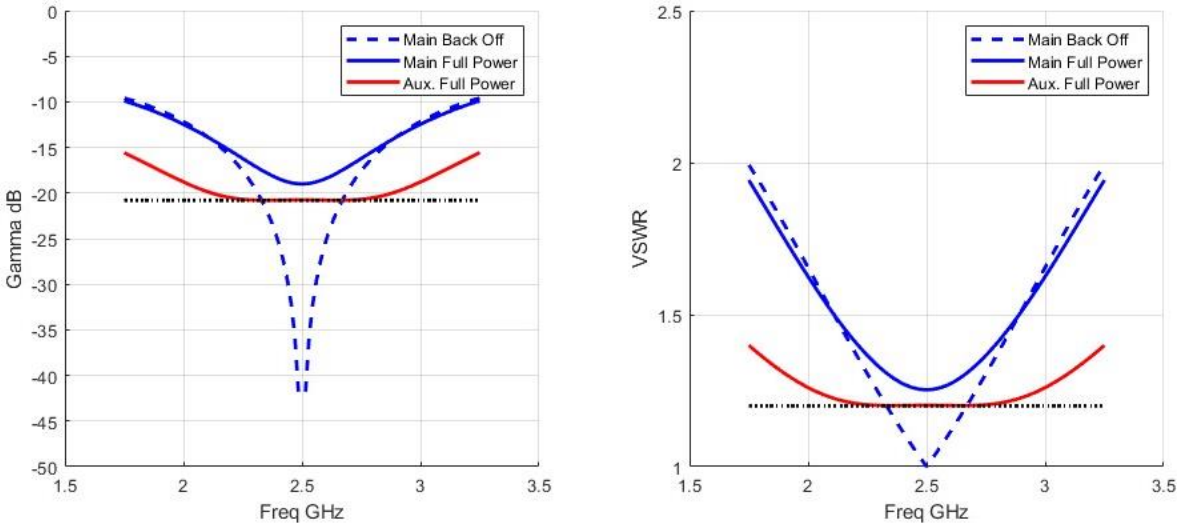


Figure 4. 26: Frequency response of the reflection coefficient in dB and VSWR

The bandwidth at the edges of the result of Figure 4. 26 is slightly better when compared to the result of Figure 4. 22 achieved for $R_{CN} = 18\ \Omega$.

4.9.1.3.5 Optimum parameters to improve the performances of the conventional DPA at the bandwidth edge

To summarize, it possible to find a set of design parameters that will yield similar matching results at the bandwidth's edge, whether it's 2 or 3 GH. For instance, by setting R_{CN} to 29 Ω and γ to 1.25, we achieve the result shown in Figure 4. 27. Although the desired target is not reached in this scenario, the matching can still be deemed acceptable across the entire bandwidth.

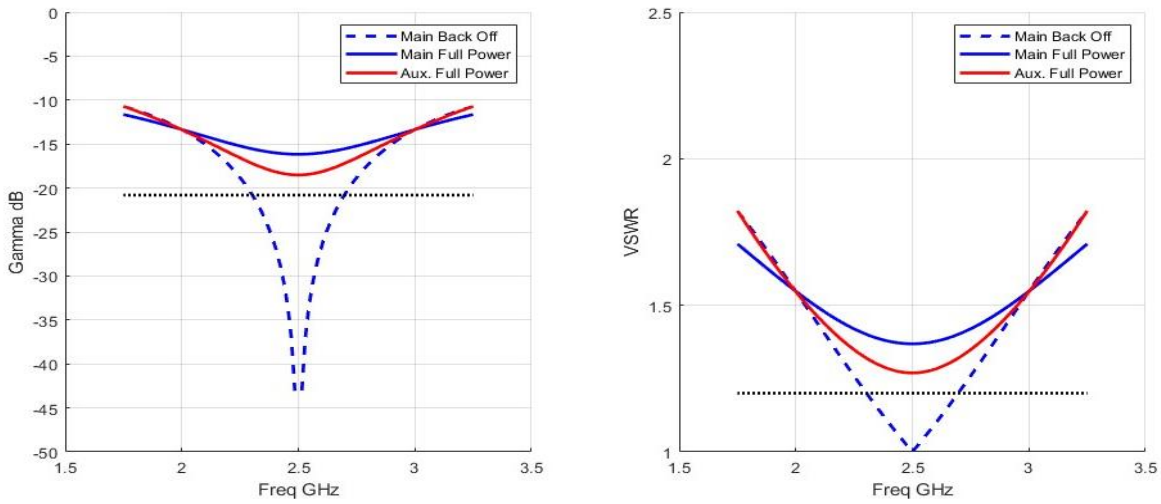


Figure 4. 27: Frequency response of the reflection coefficient in dB and VSWR

4.9.2 The inverted Doherty Power Amplifier Architecture

4.9.2.1 Presentation of the circuit configuration

Figure 4. 28 illustrates the proposed inverted Doherty amplifier design with a two-stage amplifier. The inverted Doherty amplifier uses two impedance transformation networks, which results in a 180° phase shift in the auxiliary amplifier path. The main amplifier requires a quarter-wave transmission line at its input for phase compensation. Furthermore, the inverted DPA architecture allows more parameter adjustment than the conventional structure. At the back-off power level, the auxiliary path acts as a stub, restoring the impedance at the common node so that it can be exploited to improve the bandwidth. Another advantage of the Doherty architecture is its ability to consider the transistors' output parasitic elements (drain-source parasitic capacitance, Cd and bonding-wire inductance, Lb) in the impedance transformation circuits.

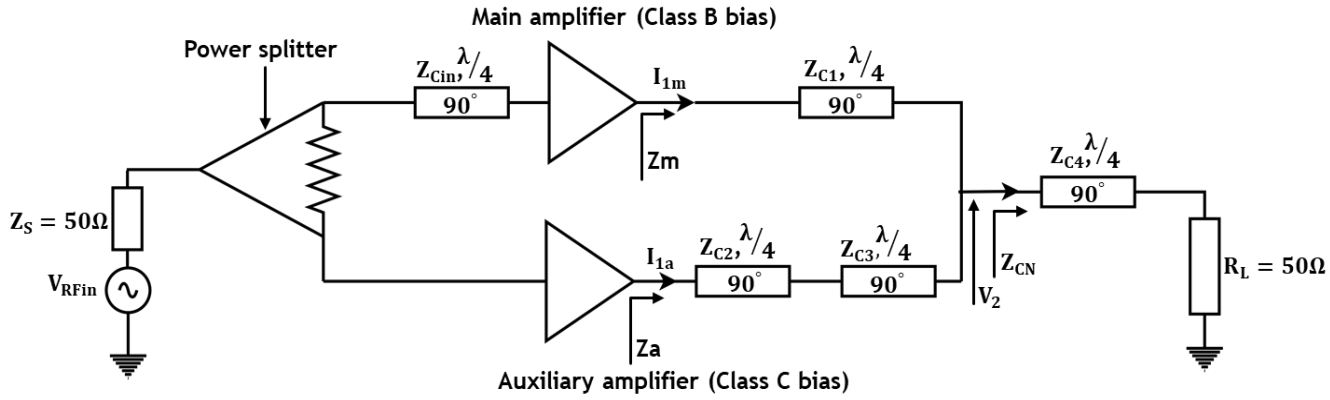


Figure 4. 28: The proposed inverted DPA

To analyse the inverted DPA and derive its design equations, we represent it using a simplified circuit with specific notations. Please refer to Figure 4. 29 below.

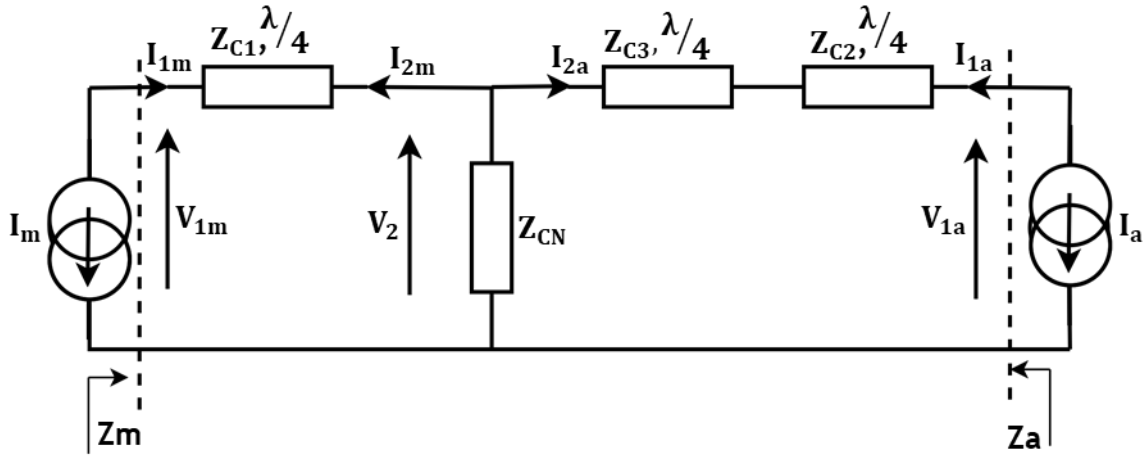


Figure 4. 29: Equivalent circuit diagram of the proposed inverted DPA

First, the expression for the ratio of the current I_{1a} at the output of the auxiliary amplifier to the current I_{1m} of the main amplifier of the inverted DPA is also assumed to be:

$$r = \frac{I_{1a}}{I_{1m}} = |r|.e^{j\Delta\phi} \tag{4. 67}$$

In this part, the amplifier is studied at a centre frequency f_o. Compared to the conventional DPA case, here, the current I_{1m} lags behind I_{1a} by a phase difference of $\Delta\phi = \frac{\pi}{2}$ at centre frequency f_o, and equation (4. 67) now becomes:

$$r = \frac{I_{1a}}{I_{1m}} = j.|r| \tag{4. 68}$$

The resulting expression for cascading the transmission matrix of the two quarter-wave transmission lines at the output of the auxiliary amplifier shown Figure 4. 28 andFigure 4. 29 having characteristic impedances Zc3 and Zc2 at a fundamental frequency f_o is written as:

$$[Z_{23}] = \begin{bmatrix} -\frac{Z_{c2}}{Z_{c3}} & 0 \\ 0 & -\frac{Z_{c3}}{Z_{c2}} \end{bmatrix} \tag{4. 69}$$

Furthermore, the equations relating the parameters at the terminal ends of the quarter-wave transmission lines in Figure 4. 29 are then given as follows:

$$\begin{cases} V_2 = -Z_{CN}(I_{2m} + I_{2a}) \\ V_{1m} = -j.Z_{c1}.I_{2m} \\ I_{1m} = -\frac{j.V_2}{Z_{c1}} \\ V_{1a} = -\frac{Z_{c2}}{Z_{c3}}V_2 \\ I_{1a} = \frac{Z_{c3}}{Z_{c2}}I_{2a} \end{cases} \tag{4. 70}$$

From these equations, the impedance seen by each current source of the inverted DPA is established as:

$$\begin{cases} Zm = \frac{V_{1m}}{I_{1m}} = \frac{Z_{c1}^2}{Z_{CN}} - \frac{Z_{c1}.Z_{c2}}{Z_{c3}}.|r| \\ Za = \frac{V_{1a}}{I_{1a}} = \frac{Z_{c1}.Z_{c2}}{Z_{c3}}.\frac{1}{|r|} \end{cases} \tag{4. 71}$$

The impedance seen by the main amplifier must be equal to Ropt at high power, and the auxiliary amplifier of size |r| is loaded by Ropt/|r|.

From the expression of the impedance Za in equation (4. 71), we can deduce the relationship between the characteristic impedances and Ropt as:

$$\frac{Z_{c1}.Z_{c2}}{Z_{c3}} = Ropt \tag{4. 72}$$

Then, by substituting the impedance Zm in equation (4. 71) with $Ropt$, the expression for the characteristic impedance at the output of the main amplifier becomes:

$$Z_{c1} = \sqrt{Z_{CN}.(1 + |r|).Ropt} \tag{4. 73}$$

To compute the values of the impedances Z_{c1} and Z_{c2}, it is necessary to determine the expression for the impedance Z'_{CN} seen by the auxiliary amplifier at the common node path. Thus, the expression for this impedance is written as:

$$Z'_{CN} = -\frac{V_2}{I_{2a}} = Z_{CN}.(1 + \frac{I_{2a}}{I_{2m}}) \quad (4.\ 74)$$

Where:

$$\frac{I_{2a}}{I_{2m}} = \frac{V_{1m}}{I_{1a}}.\frac{Z_{c3}}{-j.Z_{c1}.Z_{c2}} \quad (4.\ 75)$$

And,

$$\frac{V_{1m}}{I_{1a}} = \frac{V_{1m}}{j.|r|.I_{1m}} = \frac{Zm}{j.|r|} \quad (4.\ 76)$$

Using equations (4. 75) and (4. 76), the following expression for Z'_{CN} is obtained:

$$Z'_{CN} = \frac{Z_{c1}.Z_{c3}}{Z_{c2}}.\frac{1}{|r|} \quad (4.\ 77)$$

Similarly, by using equations (4. 72) and (4. 73), the expression for Z'_{CN} is further written as:

$$Z'_{CN} = Z_{CN}.\frac{1+|r|}{|r|} \quad (4.\ 78)$$

The transmission lines with the characteristic impedances Z_{c2} and Z_{c3} are used to transform the impedance Z'_{CN} at the common node to Ropt/(|r|) presented to the output of the auxiliary amplifier. This can be done by calculating the intermediate resistance R_{int} between the two transmission lines using the following formula:

$$R_{int} = \sqrt{Z_{CN}.\frac{1+|r|}{|r|}.\frac{Ropt}{|r|}} \quad (4.\ 79)$$

The following expressions are then achieved:

$$Z_{c2} = \sqrt{\frac{Ropt}{|r|}.R_{int}} \quad (4.\ 80)$$

$$Z_{c3} = \sqrt{Z_{CN}.\frac{1+|r|}{|r|}.R_{int}} \quad (4.\ 81)$$

The design parameters of an inverted DPA, such as the characteristic impedances of the multiple quarter-wave transmission lines, depend on the chosen common node impedance Z_{CN}. This is evident from the previous equations.

4.9.2.2 Equations for describing the frequency characteristics of an inverted DPA

In this part, we will study the frequency characteristic of an inverted DPA in Figure 4. 28 by first characterising the quarter-wave transmission lines at the output of both amplifiers in terms of the ABCD parameters of transmission matrix. Thus, the simplified version of the inverted DPA shown in Figure 4. 30 below is used to study the frequency behaviour.

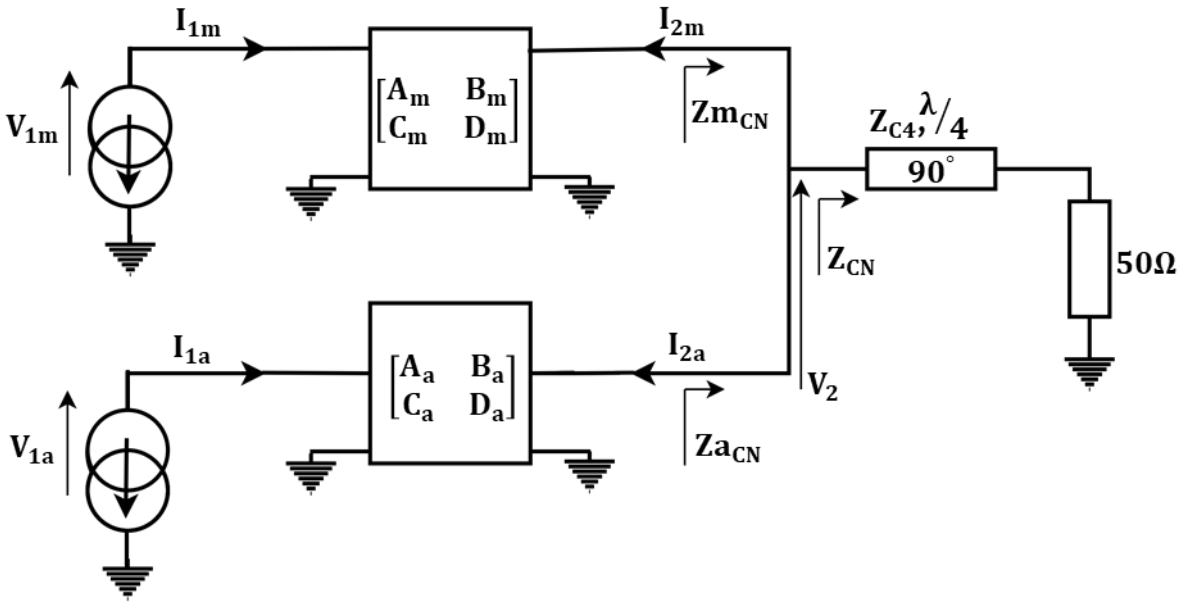


Figure 4. 30: The simplified version of the proposed inverted DPA

The first step is to obtain a general relationship between the currents I_{2a} and I_{2m}. To do this, we give the expressions for the currents I_{1a} and I_{1m} using ABCD parameters, as:

$$\begin{cases} I_{1m} = -Cm.Z_{CN}(I_{2m}+I_{2a}) - Dm.I_{2m} \\ I_{1a} = -Ca.Z_{CN}(I_{2m}+I_{2a}) - Da.I_{2a} \end{cases} \quad (4.\ 82)$$

By taking the ratio of the currents $r = \frac{I_{1a}}{I_{1m}}$, we obtain:

$$\frac{I_{2m}}{I_{2a}} = \frac{Z_{CN}.Ca - r.(Z_{CN}.Cm + Dm)}{r.Z_{CN}.Cm - Z_{CN}.Ca - Da} \quad (4.\ 83)$$

For each amplifier, the impedance seen at the output of the matching quadripoles of Figure 4. 30 is written as:

$$\begin{cases} Zm_{CN} = -\dfrac{V_2}{I_{2m}} = Z_{CN}.(1 + \dfrac{I_{2a}}{I_{2m}}) \\ Za_{CN} = -\dfrac{V_2}{I_{2a}} = Z_{CN}.(1 + \dfrac{I_{2m}}{I_{2a}}) \end{cases} \quad (4.\ 84)$$

These equations can be used to calculate the impedances seen by the main and auxiliary amplifiers at full power, given by:

$$\begin{cases} Zm = \dfrac{Am.Zm_{CN} - Bm}{Cm.Zm_{CN} - Dm} \\ Za = \dfrac{Aa.Za_{CN} - Ba}{Ca.Za_{CN} - Da} \end{cases} \quad (4.\ 85)$$

Then, by knowing the current ratio $r = \frac{I_{1a}}{I_{1m}}$, equation (4. 85) allows to calculate the impedances presented to each current source. This calculation can be made at Full Power or at Back-Off.

At the back-off power level, the auxiliary amplifier is turned off, i.e., current I_{1a}=0 or r=0, then, the current ratio expression of equation (4. 83) now becomes:

$$\frac{I_{2m}}{I_{2a}} = \frac{Z_{CN}.Ca}{-Z_{CN}.Ca - Da} \quad (4.\ 86)$$

Thus, using the current ratio expression of equation (4. 86), the impedances presented at the output of each transistor are calculated.

4.9.2.3 The study of the frequency behaviour of the inverted DPA

The design goal of the inverted DPA is to achieve a maximum value of VSWR = 1.2, corresponding to a reflection coefficient value of less than -20.8 dB over the widest possible frequency band. The target fractional bandwidth is 40%, and it is centred around the operating frequency of 2.5 GHz within the desired frequency range of 2 GHz to 3 GHz. These values are calculated at back-off power for the main amplifier and full power for the main and auxiliary amplifiers.

First, we analyze the frequency behaviour of the inverted DPA shown in Figure 4. 28. It is designed using a quarter-wave transmission line.

Therefore, for a symmetrical two-stage inverted DPA circuit, the two transistors deliver the same amount of current at a high-power level (i.e.,$|r| = 1$), with an optimum load impedance of $R_{opt} = 36\ \Omega$. Thus, the main amplifier optimum drain resistance at back-off power is $R_{opt} = 72\ \Omega$.

For $|r| = 1$, the design equations for the inverted DPA network parameters become:

$$\begin{cases} Z_{c1} = \sqrt{2.Z_{CN}.Ropt} \\ R_{int} = \sqrt{2.Z_{CN}.Ropt} \\ Z_{c2} = \sqrt{Ropt.R_{int}} \\ Z_{c3} = \sqrt{2.Z_{CN}.R_{int}} \\ Z_{c4} = \sqrt{50.Z_{CN}} \end{cases} \quad (4.\ 87)$$

As stated previously, the characteristic impedances of the quarter-wave transmission lines depend on the choice of the common node impedance Z_{CN}. This provides additional adjustment possibilities compared to the conventional DPA architecture. Furthermore, it is also possible to adjust the intermediate impedance R_{int}, between the two quarter-wave transmission lines at the output of the auxiliary amplifier as well as the phase slope parameter, γ.

Table 4. 4 summarises the values of the circuit parameters of the inverted DPA at a real common node impedance value of Z_{CN} = R_{CN} = Ropt/2=18 Ω (like the conventional DPA case) and Z_{CN} = R_{CN} = Ropt=36 Ω.

Table 4. 4: The network parameter values of the inverted DPA

	Current ratio	Z common node	Phase slope param.	Opt. load at Full Power	Z_{c1} main ¼ wave	R inter-mediate	Z_{c2} Aux. ¼ wave	Z_{c3} Aux. ¼ wave	Z_{c4} output ¼ wave
	$\|r\|$	Z_{CN}	γ	Ropt	Z_{C1}	*Rint*	Z_{c2}	Z_{c3}	Z_{C4}
Case 1	1	18 Ω	2	36 Ω	36 Ω	36 Ω	36 Ω	36 Ω	30 Ω
Case 2	1	36 Ω	2	36 Ω	51 Ω	51 Ω	42.8 Ω	60.5 Ω	42.4 Ω

Consequently, Figure 4. 31 shows the plot of the frequency response of the reflection coefficient in dB and VSWR for case 1, which has a common node impedance of R_{CN} = Ropt/2=18 Ω. The results of the frequency response are close to those obtained for the conventional or classical Doherty power amplifier architecture.

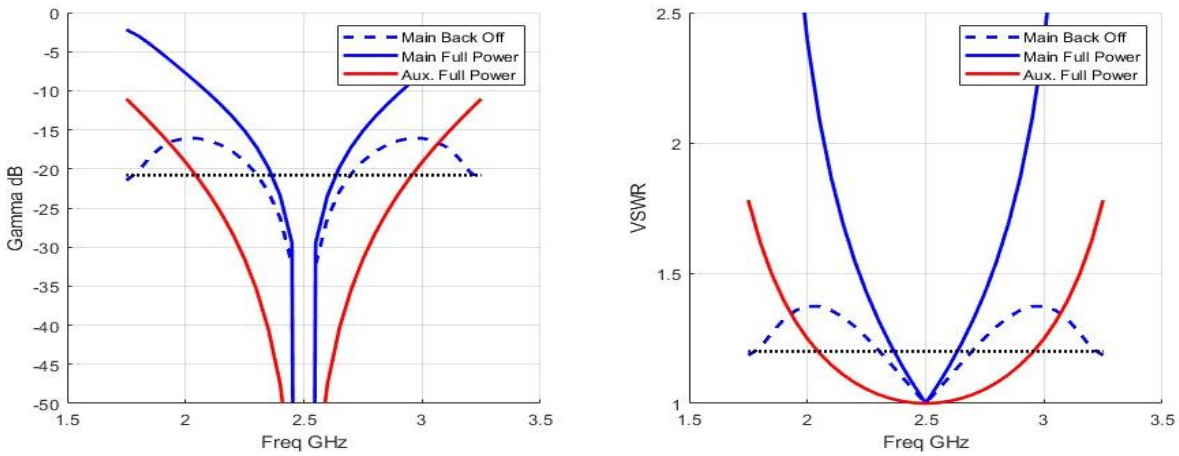


Figure 4. 31: Frequency response of the reflection coefficient in dB and VSWR for case 1 of Table 4. 4

Similarly, the simulation result for the frequency response of the inverted DPA for case 2 with a common node impedance of R_{CN} = Ropt=36 Ω shows a different result compared to case 1, as the bandwidth of both the main and auxiliary amplifiers has greatly improved, as illustrated in Figure 4. 32.

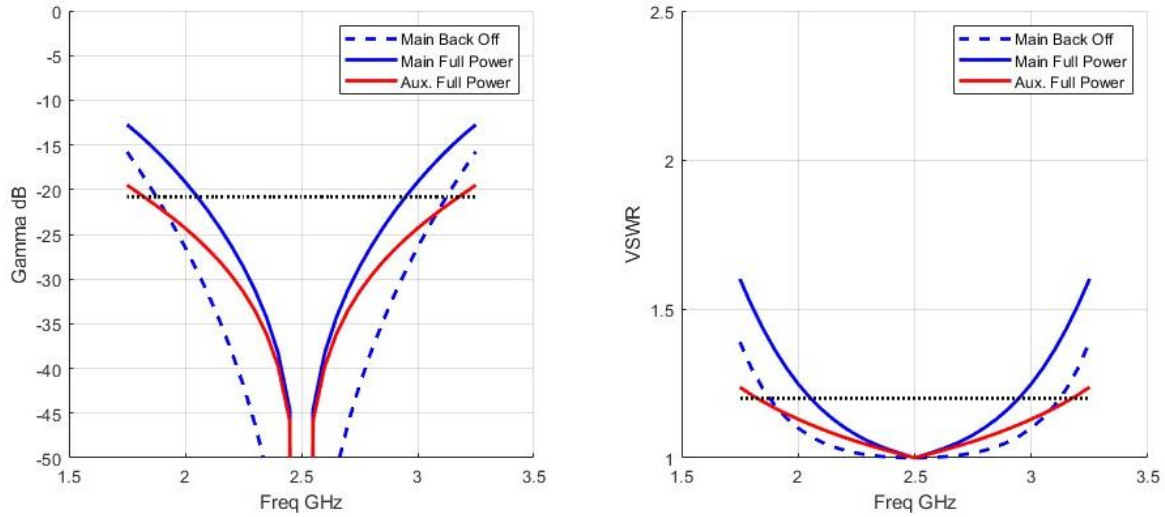


Figure 4. 32: Frequency response of the reflection coefficient in dB and VSWR for case 2 of Table 4. 4

4.9.2.3.1 Adjustment of the common node impedance (Z_{CN}) of the inverted DPA

The results of Figure 4. 31 and Figure 4. 32 showed that the choice of the common node impedance Z_{CN} at the centre frequency f_o significantly affects the bandwidth performance of the inverted DPA. In this part, a sweep of $Z_{CN} = R_{CN}$ is carried out, and the values of the characteristic impedances of the transmission lines for the inverted DPA are updated for each value of R_{CN}. Additionally, the reflection

coefficient and the VSWR values of the inverted DPA are calculated at the edge of the targeted bandwidth, i.e., either at 2 GHz or 3 GHz.

As illustrated in Figure 4. 33 below, it can be seen that the plots of the reflection coefficient and the VSWR of the inverted DPA against common node resistance R_{CN} confirm the strong influence of the choice of the common node resistance on the frequency response performance. Thus, the optimum value of the common node resistance is found to be $R_{CN} = 33\ \Omega$.

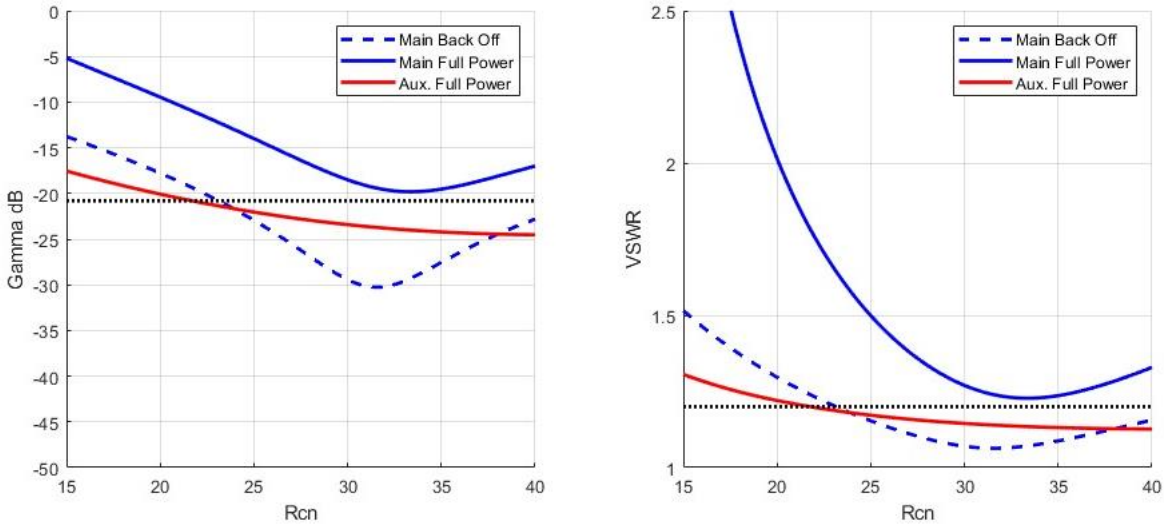


Figure 4. 33: The result of the reflection coefficient in dB and VSWR of a DPA at full and backoff power levels against the common node resistance (R_{CN})

4.9.2.3.2 Adjustment of the phase slope parameter γ of the inverted DPA

The phase slope parameter (γ) is used to adjust the phase slope of the inverted DPA around the centre frequency of the two amplifier currents. Figure 4. 34 shows how adjusting the phase slope of the inverted DPA affects its performance at high power levels by improving the bandwidth of the auxiliary and main amplifiers. This result is achieved at an optimum common node resistance value of R_{CN} =33 Ω and at the edge of the targeted bandwidth, i.e., either at 2 GHz or 3 GHz. As seen from Figure 4. 34, an optimum value of the phase slope parameter of $\gamma = 1.5$ allows the desired performance to be obtained with a VSWR or reflection coefficient value of less than 1.2 or -20.8 dB over the entire bandwidth of interest.

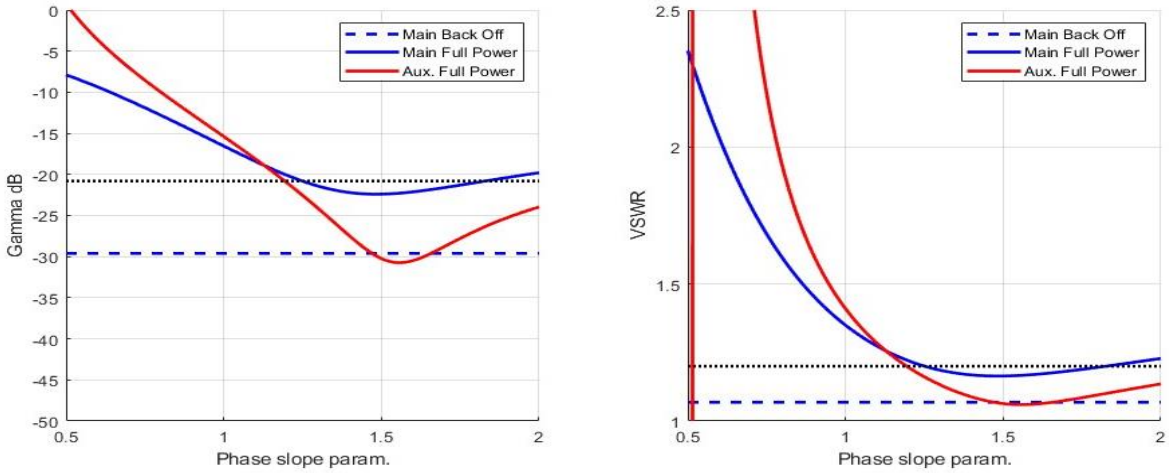


Figure 4. 34: The result of the reflection coefficient in dB and VSWR of a DPA at full and backoff power levels as a function of the phase slope parameter (γ)

4.9.2.3.3 Adjustment of the intermediate resistance (R_{int}) of the inverted DPA

It is also possible to adjust the intermediate resistance (R_{int}) between the two quarter-wave transmission lines at the output of the auxiliary amplifier while maintaining the matching conditions at the centre frequency fo. Thus, Figure 4. 35 below shows the result obtained by starting from the previously obtained optimum values of R_{CN} =33 Ω and $\gamma = 1.5$.

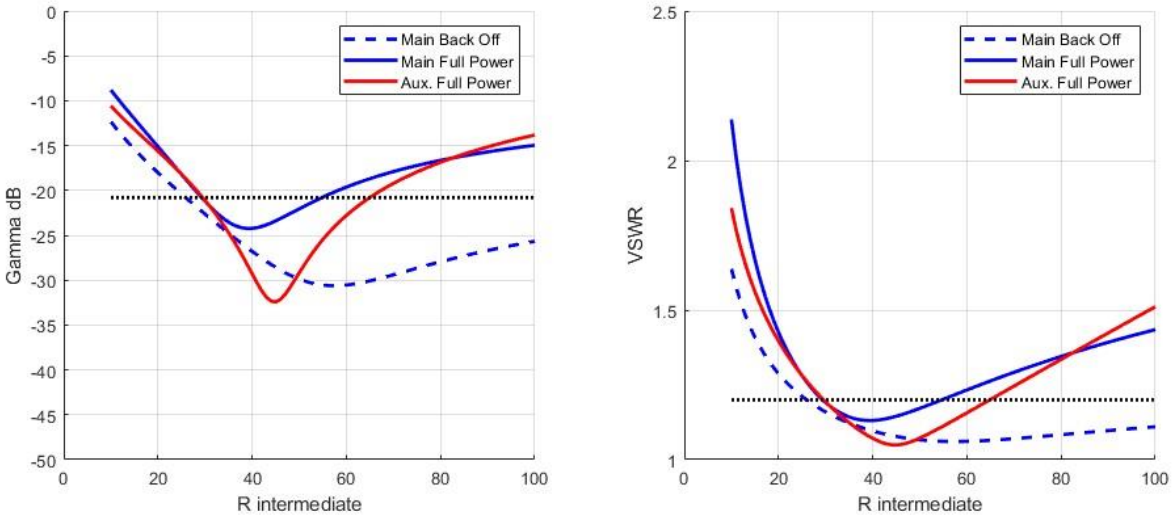


Figure 4. 35: Reflection coefficient in dB and VSWR against the intermediate resistance (R_{int})

4.9.2.3.4 The summary of the results

From the above results about the effect of adjusting the Z_{CN}, phase slope, and R_{int} of an inverted DPA on the bandwidth performance, Figure 4. 36 shows the frequency response obtained in terms of the reflection coefficient and VSWR. Table 4. 5 also gives the corresponding optimum values of the inverted DPA circuit parameters.

Table 4. 5: The optimum values of the inverted DPA network parameters for $|r| = 1$

	Current ratio	Z common node	Phase slope param.	Opt. load at Full Power	Z_{c1} main ¼ wave	R inter-mediate	Z_{c2} Aux. ¼ wave	Z_{c3} Aux. ¼ wave	Z_{c4} output ¼ wave
	$\|r\|$	Z_{CN}	γ	Ropt	Z_{C1}	*Rint*	Z_{c2}	Z_{c3}	Z_{C4}
Optimum case	1	33 Ω	1.5	36 Ω	48.7 Ω	40 Ω	38 Ω	51.4 Ω	40.6 Ω

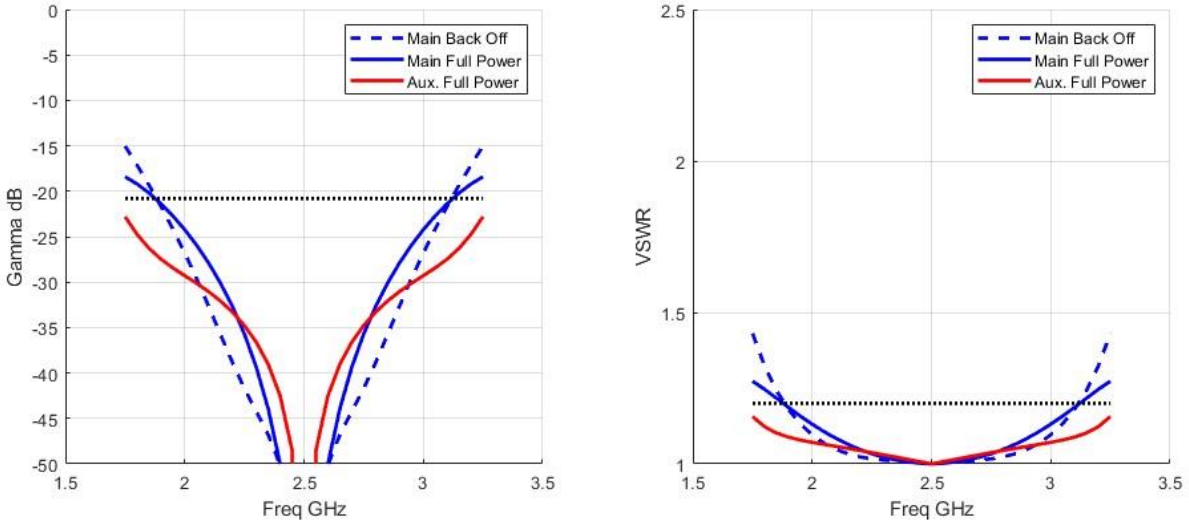


Figure 4. 36: Frequency response of the reflection coefficient in dB and VSWR for $|r| = 1$ and optimum values given in Table 4. 5

Similarly, by applying the same approach to an asymmetrical two-stage inverted Doherty amplifier case with a current ratio |r|=1.5, the following result is obtained:

Table 4. 6: The optimum values of the inverted DPA network parameters for $|r| = 1.5$

	Current ratio	Z common node	Phase slope param.	Opt. load at Full Power	Z_{c1} main ¼ wave	R inter-mediate	Z_{c2} Aux. ¼ wave	Z_{c3} Aux. ¼ wave	Z_{c4} output ¼ wave
	$\|r\|$	Z_{CN}	γ	Ropt	Z_{C1}	*Rint*	Z_{c2}	Z_{c3}	Z_{C2}
Optimum case	1.5	33 Ω	1.3	33 Ω	54.5 Ω	33 Ω	28.1 Ω	42.6 Ω	40.6 Ω

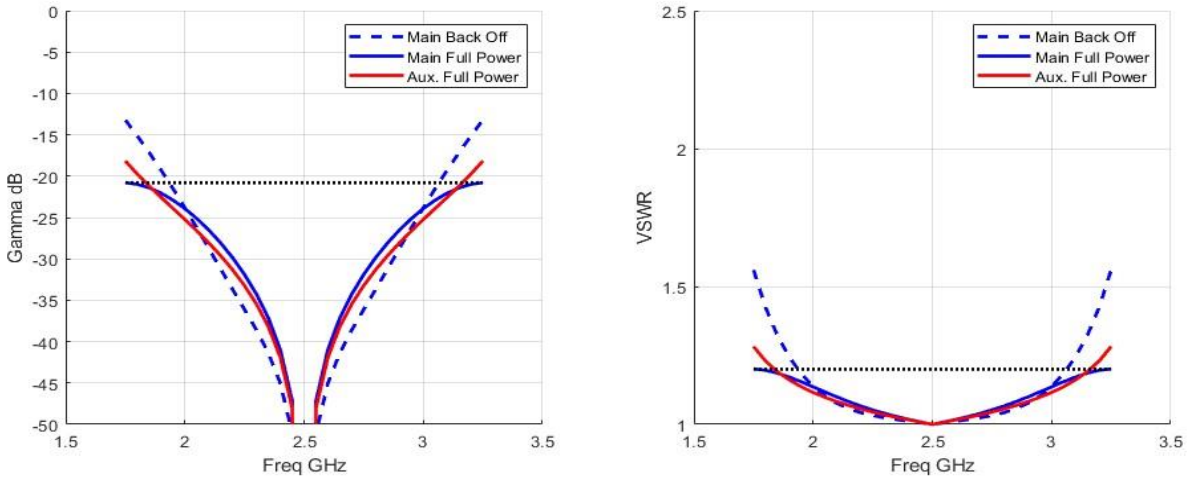


Figure 4. 37: Frequency response of the reflection coefficient in dB and VSWR for $|r| = 1.5$ and optimum values given in Table 4. 6

4.9.3 Conclusion about the results of the designed conventional DPA and the inverted DPA with ideal components

To summarize, the results of both the conventional and inverted DPAs showed that optimizing the DPA structures enhances the operating bandwidth. However, the improvement in bandwidth for the conventional DPA architecture is minimal. On the other hand, the inverted DPA topology offers the potential to adjust various circuit parameters to control the bandwidth limits. Notably, the slope of the phase variation between the main and auxiliary amplifier currents, as highlighted in the work of [51], is a crucial parameter for adjusting and controlling the bandwidth limit.

4.10 Bandwidth Limitation of a Doherty Power Amplifier

In practice, the bandwidth of the Doherty power amplifier is often lower than its theoretical limitations. While the use of a quarter-wave (λ/4) transmission line contributes to the bandwidth limitation of DPA, the main reason for the reduced bandwidth is the presence of device output parasitic capacitance and the compensation methods employed to mitigate their effects [56, 57].

A simplified GaN-based transistor model shown in Figure 4. 38 with an equivalent output parasitic capacitance (Cd) is used for analysing the DPA output network.

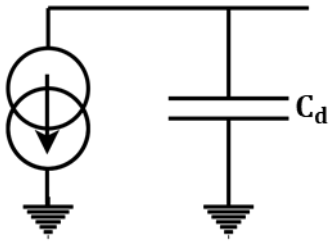


Figure 4. 38: Analysing of Doherty power amplifier (DPA) using a simplified model of the device output parasitic capacitance

Thus, the commonly used methods of compensating for the output parasitic capacitances in DPAs are described in this section. These include the quarter-wave transmission line reactance compensation technique, parasitic absorption using the Pi network, and quasi-lumped (QL) equivalent quarter-wave transmission line network methods.

4.10.1 Quarter-wave (λ/4) transmission line only

The design of a DPA, as shown in Figure 4. 39, involves the use of a quarter-wave transmission line at the main amplifier's output. This transmission line transforms the impedance at the common node A ($Z_A = \frac{R_{opt}}{2}$) between the main and auxiliary amplifiers to an optimal theoretical impedance value ($Z_{dm} = 2.R_{opt}$) that the main amplifier sees. The quarter-wave transmission line output network serves as a reference to study how to compensate for the output parasitic capacitance, Cd.

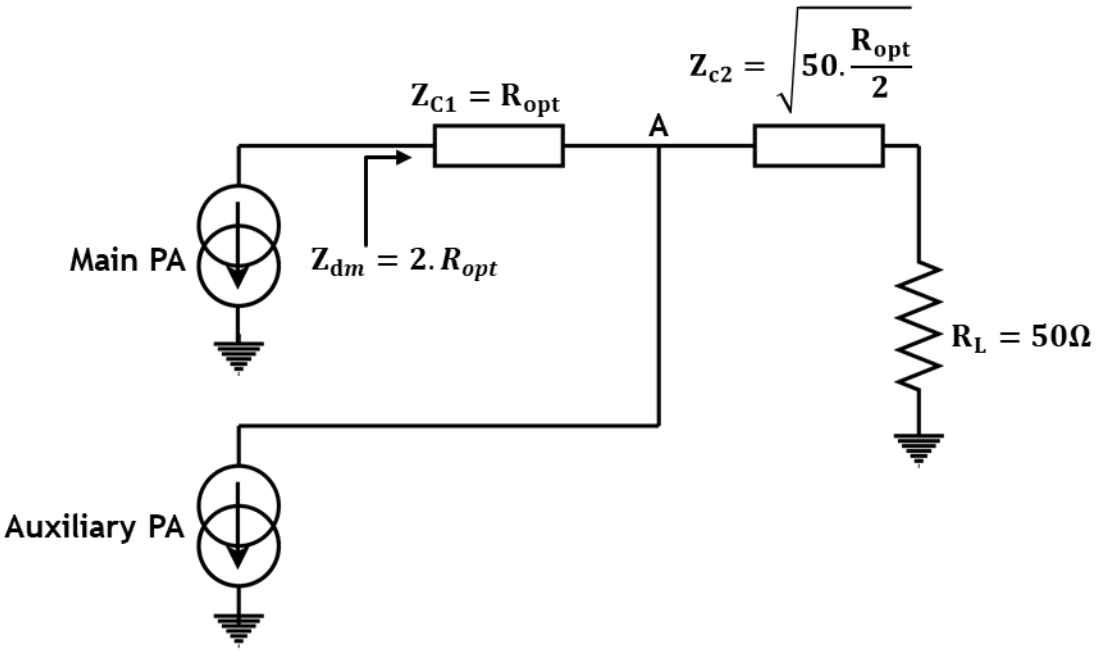


Figure 4. 39: Schematic of the output network for a DPA without the output parasitic capacitance of the main amplifier and using only the quarter-wave transmission line.

An S-parameter simulation using ADS software is carried out to determine the matching bandwidth performance of the quarter-wave transmission line, as illustrated of Figure 4. 40.

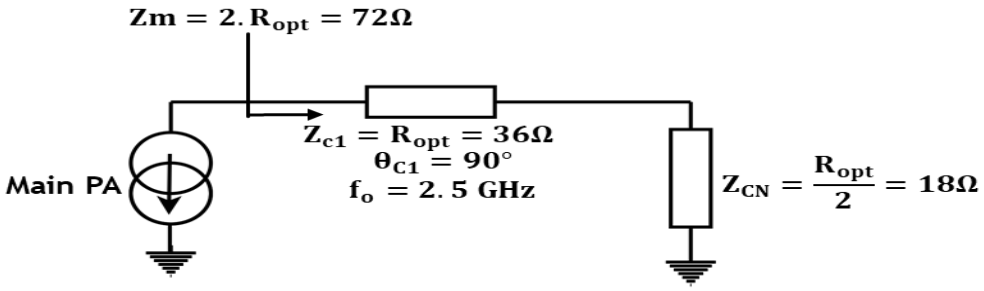


Figure 4. 40: Schematic diagram of the S-parameter simulation of λ/4 transmission line at the output of the main amplifier without LC resonant circuit.

Based on previous studies and summarized theoretical results in Table 4. 3 for conventional Doherty and Table 4. 4 for the inverted DPA, we can conclude that when the current ratio |r| equals 1 at full power, the quarter wave transmission line at the output of the main amplifier has the following characteristics:

Table 4. 7: Quarter-wave transmission line characteristics at full power

Z common node	Opt. load at Full Power	Z_{c1} main ¼ wave
Z_{CN}	Ropt	Z_{C1}
18 Ω	36 Ω	36 Ω

The simulated result of the frequency response analysis of the λ/4 transmission line shown in Figure 4. 40 in terms of the reflection coefficient is illustrated in Figure 4. 41 below.

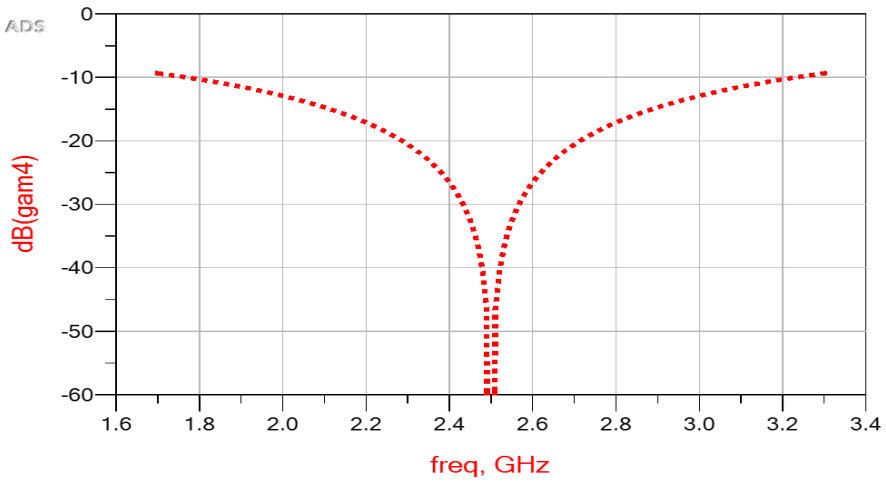


Figure 4. 41: Reflection coefficient of the output λ/4 transmission line of a DPA against frequency without the parasitic capacitor Cd

From the simulation result of Figure 4. 41, the fractional bandwidth of the λ/4 transmission line at the output of the main amplifier of Figure 4. 39 without Cd at a -20 dB reflection coefficient threshold and centred at a design frequency of 2.5 GHz is 17.2%.

4.10.2 Parasitic compensation method using a quarter-wave (λ/4) transmission line and an LC network at the left port of the λ/4 transmission line

In this case, we consider the effect of incorporating a parasitic capacitance (Cd) and a shunt inductor (Ls) to cancel the reactive part of the output impedance presented to the amplifier at the fundamental frequency of 2.5 GHz.

The schematic set-up of the S-parameter simulation for the λ/4 transmission line at the output of the main amplifier of Figure 4. 39 with an LC resonant circuit at the left port of the TL is illustrated in Figure 4. 42.

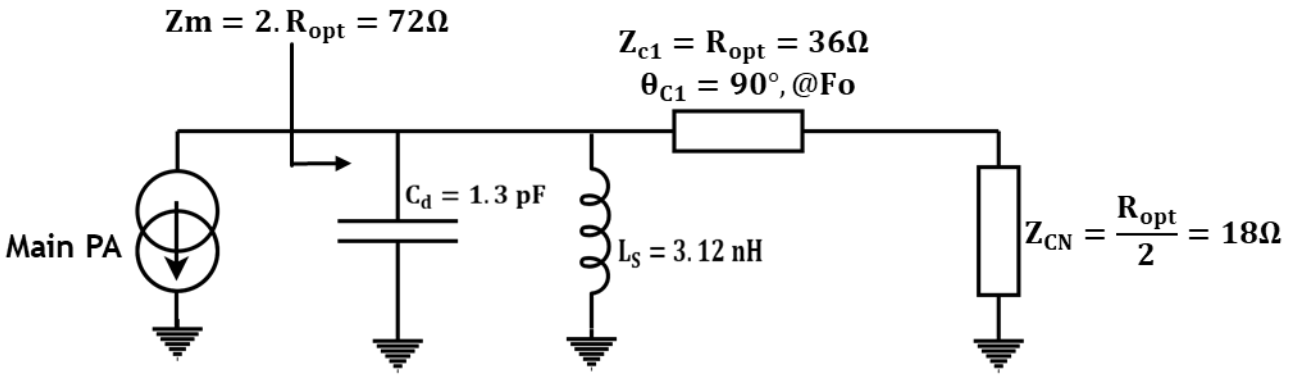


Figure 4. 42: Schematic diagram of the S-parameter simulation of a λ/4 transmission line at the output of the main amplifier with an LC resonant circuit.

The output parasitic capacitance value of the GaN transistor is given as Cd =1.3 pF. Thus, the corresponding shunt inductance is given by:

$$L_S = \frac{1}{\omega_0{}^2 C_d} = 3.12\ nH \tag{4. 88}$$

4.10.3 Realization of the output network of the DPA with CLC Pi-network

The λ/4 transmission line can be replaced by an equivalent CLC elements π-network as illustrated in Figure 4. 43.

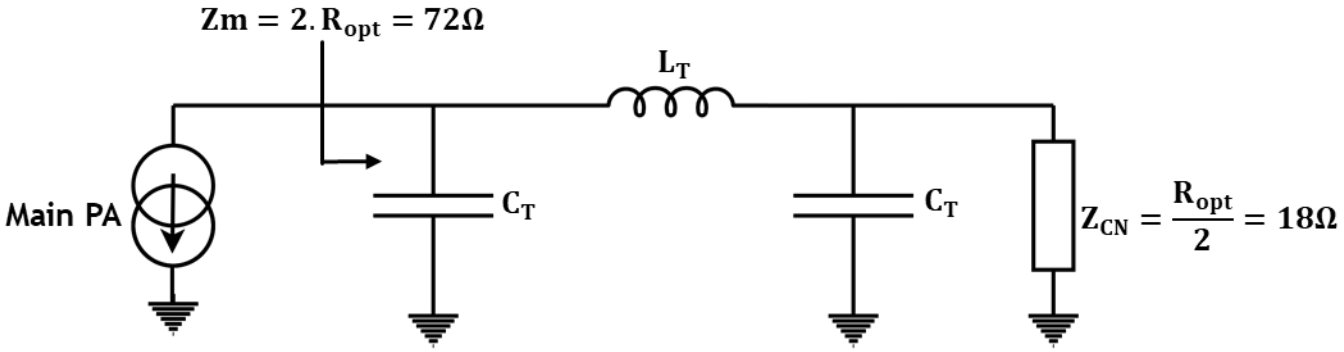


Figure 4. 43: A Pi-network used to absorb device output parasitic capacitance in DPA.

In this case, the parasitic capacitance at the output of the main amplifier is absorbed by the shunt capacitance, C_T. The expressions for the inductance L_T and capacitance C_T of Figure 4. 43 at a centre angular frequency, ω_o, are given by:

$$L_T = \frac{Z_C}{\omega_o} = 2.29\ nH \tag{4. 89}$$

$$C_T = \frac{1}{Z_C.\omega_o} = 1.77\ pF \tag{4. 90}$$

Where $Z_C = R_{opt} = 36\ \Omega$, is the characteristic impedance of the equivalent quarter wave transmission line.

4.10.4 Realization of the output network of the DPA with a Quasi-lumped (QL) network

Another method of reactive compensation involved using a quasi-lumped network with a modified transmission line and the parasitic capacitance Cd at the two terminals, as shown in Figure 4. 44.

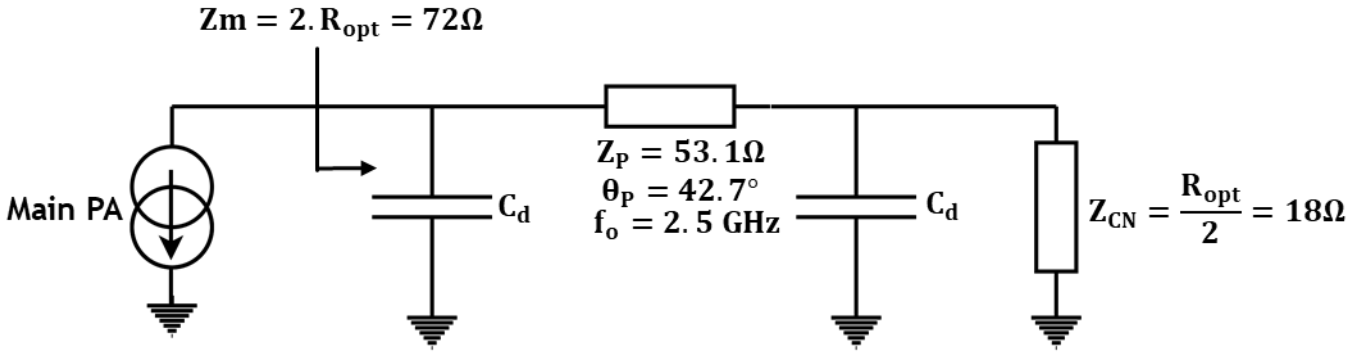


Figure 4. 44: The QL network used to absorb device output parasitic capacitance.

The electrical length θ_P, and the characteristic impedance, Z_P, of the transmission line of Figure 4. 44. are given by the following expressions [58, 59]:

$$\theta_P = \quad \cos^{-1}(\omega_o . C_d . Z_C) = 42.7° \tag{4. 91}$$

$$Z_P = \frac{Z_C}{\sin(\theta_P)} = 53.1\ \Omega \tag{4. 92}$$

Where $Z_C = R_{opt} = 36\ \Omega$, is the characteristic impedance of the quarter wave transmission line. The output parasitic capacitance is: $C_d = 1.3\ pF$

The QL-lumped element network was proposed as an alternative wideband output network to the LC-network of Figure 4. 42 in Reference [56] and has been successfully implemented in a DPA circuit, thereby achieving over 40% drain efficiency at 6 dB output power back-off in the frequency range of 1.7 to 2.1 GHz. However, a practical restriction on the Quasi-Lumped network is to ensure that the expression $\omega_o . C_d . Z_C < 1$ must be satisfied to achieve real values of both θ_P and Z_P. This implies that there is an upper-frequency limit above which the QL network cannot be used.

The expression $\omega_o . C_d . Z_C$ is computed at a design frequency of 2.5 GHz and is determined to be: $\omega_o . C_d . Z_C = 0.735 < 1$. Hence, the length θ_P and impedance Z_P of the QL network are real values, as indicated by equations (4. 91) and (4. 92), respectively.

4.10.5 Realization of the output network of a DPA with the amplifier parasitic capacitance (Cd) and bonding-wire inductance (Lb)

The previous result shows that the quasi-lumped network, with a modified transmission line and Cd at the two end terminals, is a good choice to match the output of the transistor when the bandwidth is considered. Furthermore, the device's terminal using bond wire and lines can be modelled by an inductance of Lb = 0.2 nH. Figure 4. 45 shows the circuit diagram of the equivalent quarter-wave transmission line reactive compensation method, which consists of the output parasitic capacitance (Cd) and connecting bond wire inductor (Lb) of the active device. Thus, the equivalent quarter-wave transmission line acts as an impedance inverter at a design frequency (fo) if its length (θ_T) and the characteristic impedance Z_T are accurately selected.

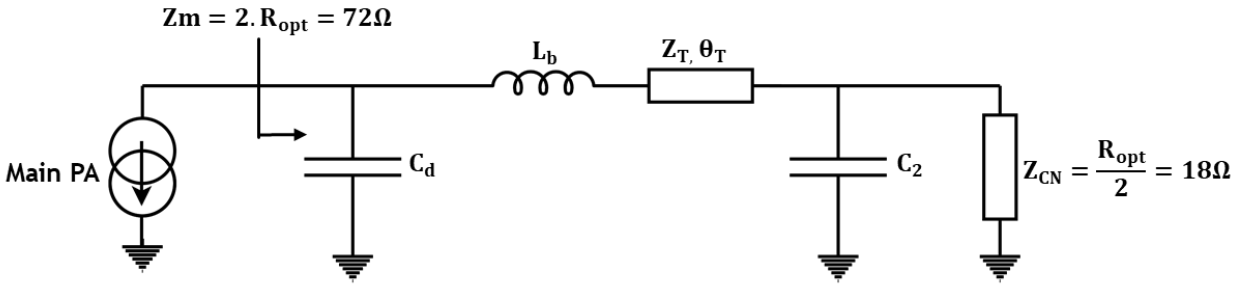


Figure 4. 45: Output network of a DPA with the amplifier parasitic capacitance (Cd) and bonding-wire inductance (Lb)

The transmission matrix expression for the circuit in Figure 4. 45 is given by the product of the matrices of the various elements that constitute the schematic. The circuit is broken down into sub-circuits (Cd and Lb) and (Z_T and C2). Thus, the overall transmission matrix of the circuit is given as:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Total} = \begin{bmatrix} 1 & jL_b\omega_o \\ jC_{ds}\omega_o & 1 - L_bC_{ds}{\omega_o}^2 \end{bmatrix} * \begin{bmatrix} \cos\theta_T - Z_T C_2\,\omega_o \sin\theta_T & jZ_T \sin\theta_T \\ \frac{j\sin\theta_T}{Z_T} + jC_2\omega_o\cos\theta_T & \cos\theta_T \end{bmatrix} \quad (4.\ 93)$$

Subsequently, if we assume the total transmission matrix of equation (4. 93) to be equivalent to the transmission matrix of the quarter-wave transmission line, then we obtain:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Total} = \begin{bmatrix} 0 & j.Z_c \\ j/Z_c & 0 \end{bmatrix} \quad (4.\ 94)$$

From equation (4. 93), the expressions for the total transmission matrix parameters are given as follows:

$$A_{Total} = (1 - L_bC_2{\omega_o}^2)\cos\theta_T - \left(Z_T\,C_2\,\omega_o + \frac{L_b\omega_o}{Z_T}\right)\sin\theta_T \quad (4.\ 95)$$

$$B_{Total} = jZ_T\sin\theta_T + jL_b\omega_o\cos\theta_T \quad (4.\ 96)$$

$$C_{Total} = j(C_d\omega_o + (1 - L_bC_d{\omega_o}^2)C_2\omega_o)\cos\theta_T + j\left\{-Z_TC_2C_d{\omega_o}^2 + \frac{1 - L_bC_d{\omega_o}^2}{Z_T}\right\}\sin\theta_T \quad (4.\ 97)$$

$$D_{Total} = -C_d\omega_o\,Z_T\sin\theta_T + (1 - L_bC_d{\omega_o}^2)\cos\theta_T \quad (4.\ 98)$$

Thus, by equating the term B_{Total} of equation (4. 96) to $j.Z_c$ of the quarter-wave transmission line, we obtained the expression for the characteristic impedance (Z_T) of the equivalent transmission line as:

$$Z_T = \frac{Z_c - Lb.\omega_o.\cos(\theta_T)}{\sin(\theta_T)} \tag{4. 99}$$

Equating the term $A_{Total} = 0$, gives the expression for the output capacitance of the network as:

$$C_2 = \frac{1 - (Lb.\frac{\omega_o}{Z_T}).\tan(\theta_T)}{\omega_o(Lb.\omega_o + Z_T.\tan(\theta_T))} \tag{4. 100}$$

The expression of C_2 can also be written in the following form upon eliminating the Z_T and θ_T term from equation (4. 100):

$$C_2 = \frac{C_d - \frac{L_b}{{Z_c}^2}}{1 - L_b C_d {\omega_o}^2} \tag{4. 101}$$

Similarly, from the $D_{Total} = 0$, we obtained the expression for the angle θ_T as:

$$\theta_T = \text{acos}(\omega_o.C_d.Z_C) \tag{4. 102}$$

The expression for θ_T is true only if $(\omega_o.C_d.Z_C) \leq 1$ or:

$$Z_{c\_max} = \frac{1}{C_{ds}.\omega_o} \tag{4. 103}$$

The above equations are applied at a drain-source parasitic capacitance $C_d = 1.3pF$, bonding-wire inductance $L_b = 0.2\,nH$ and the characteristic impedance of the λ/4 TL $Z_C = R_{opt} = 36\Omega$. Table 4. 8 summarises the network parameter values of Figure 4. 45 calculated at a design frequency of 2.5 GHz.

Table 4. 8: Design parameters values of the quasi-lumped network of Figure 4. 45

$Z_T(\Omega)$	$\theta_T(deg)$	$C_2(pF)$
49.7	42.7	1.22

Bandwidth comparison of the DPA output networks

Figure 4. 46 compares the fractional bandwidth of the five analysed methods of mitigating the effect of the output parasitic elements on the bandwidth of a Doherty power amplifier.

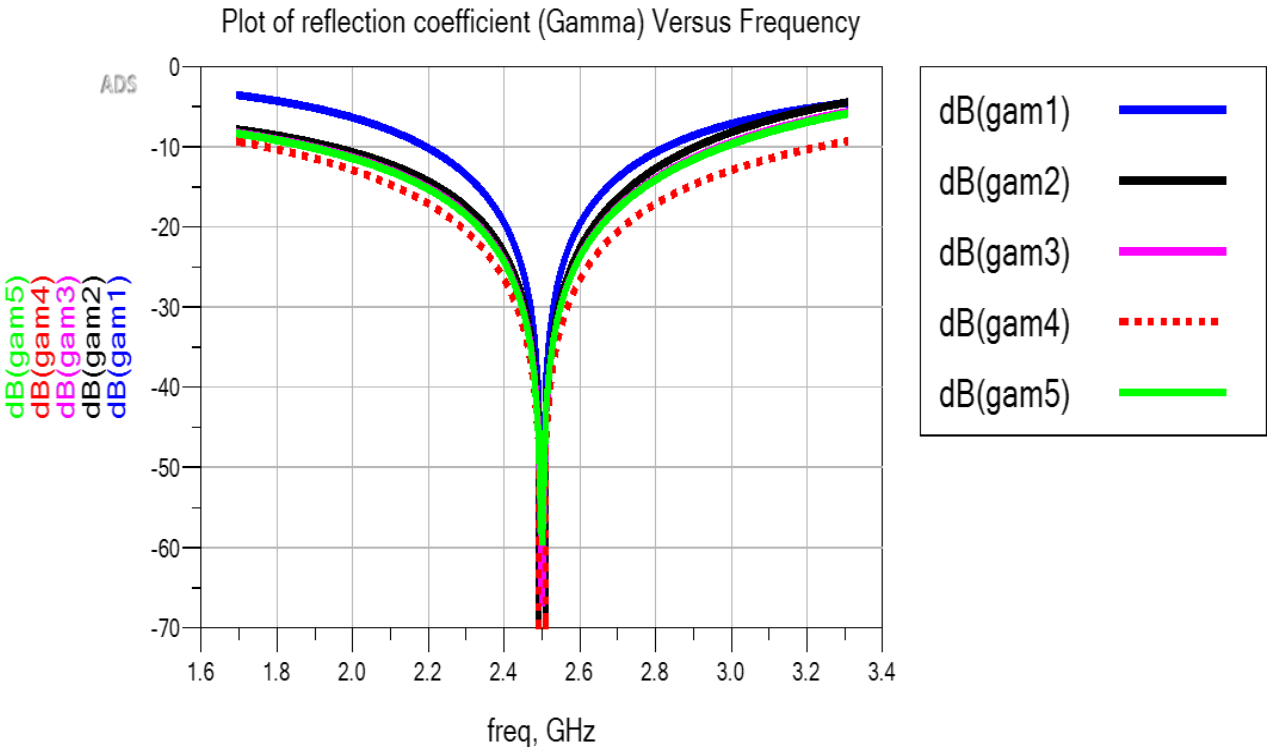


Figure 4. 46: Comparison of the fractional bandwidth of the methods of compensating for the parasitic output capacitance of a DPA

Legend:
dB(gam1): A quarter-wave transmission line with a LC tank at the left port of the λ/4 TL
dB(gam2): A lowpass Pi-output compensation network
dB(gam3): A quasi-lumped output compensation network (Cd-modified TL-Cd network)
dB(gam4): A λ/4 TL output compensation network without capacitance Cd
dB(gam5): Output network compensation of a DPA with capacitance (Cd) and bond-wire inductance (Lb)
NB: dB(gam3) = dB(gam5) result

Similarly, Table 4. 9 compares the fractional bandwidth performance of the DPA output networks at a -20 dB reflection coefficient threshold and a center frequency of 2.5 GHz.

Table 4. 9: Fractional bandwidth comparison of the DPA output networks

DPA output networks	LC - λ/4 TL network	Low Pass (C_T - L_T - C_T) Pi network	(Cd-modified TL-Cd) network	λ/4 TL network	(Cd- Lb-modified TL-C2) network
Fractional bandwidth (%) at a -20 dB limit	7.6	10.8	**13.2**	**17.2**	**13.2**

The results shown in Table 4. 9 demonstrate that the simulated output network of a DPA with the amplifier's parasitic capacitance (Cd) and bonding-wire inductance (Lb) from Figure 4. 45 is identical to the quasi-lumped network displayed in Figure 4. 44. Both networks exhibit a fractional bandwidth of 13.2%, based on the reflection coefficient at a -20 dB threshold, centred around a design frequency of 2.5 GHz. This fractional bandwidth is the closest to the reference λ/4 DPA output network, which has a fractional bandwidth of 17.2%.

4.11 Optimization of the inverted DPA bandwidth when the output parasitic elements of the transistor are considered

4.11.1 The complete design of the inverted DPA circuit

To achieve more realistic results, the parasitic output elements of the transistor are considered in the design of the inverted DPA. This output element includes the parasitic capacitance (Cd) and the drain or output self-inductance (L_b).

4.11.2 Improving the bandwidth of an inverted DPA using the optimization method

4.11.2.1 The optimization process

In the previous study, we have seen that it is possible to optimise the bandwidth of an inverted DPA by adjusting the impedance R_{CN} seen at the common node, the intermediate impedance R_{int} between the two quarter-wave transmission lines at the output of the auxiliary amplifier, and by varying the input phase slope difference between the main and auxiliary currents as a function of the phase slope parameter γ. In this part, an optimization method with a MATLAB function is used to find the optimum parameters of the inverted DPA.

Thus, by considering the limit of the characteristic impedances of the inverted DPA indicated by the maximum impedance of equation (4. 103), the optimization parameters will focus on the characteristic impedances (Z_{c1}, Z_{c2}, $Z_{c3,}$ and Z_{c4}) as well as the phase slope parameter γ.

The following are the input variables to the optimization function:

- The frequency range of the optimization = 2 GHz to 3 GHz
- The main amplifier optimum load impedance, Ropt= 36 Ω
- The main amplifier output parasitic capacitance, Cd = 1.3 pF
- The access self-inductance of the transistor, L_b = 0.2 nH
- The initial value of the phase slope parameter, $\gamma = 2$

- The magnitude of the current ratio is |r|=1 for symmetrical Doherty transistors and |r| >1 for asymmetrical Doherty transistors case
- The common node resistance value is given as R_{CN} = Ropt= 36 Ω
- Subsequently, the calculation of the following initial values of the optimization parameters (Zc1, Zc2, Zc3, and Zc4) is carried out using equations (4. 87)
- Then, using Zc1 and Zc2 characteristic impedances, the characteristic impedance Z_T and the capacitor C_2 of the equivalent quarter-wave transmission line of Figure 4. 45 are calculated. This network in Figure 4. 45 is chosen as the output compensation network for the main and auxiliary amplifiers.
- Then, the MATLAB fmincon optimization solver using the sequential quadratic programming (Sqp) algorithm is invoked on the optimization objective function. This solver is utilized to find the minimum values of the optimization variables while considering constraints on the parameters to be optimized.
- The objective function of the optimization program is based on the calculation of the reflection coefficients as follows:
    - Case (a): The calculation of the objective function is based on the square of the sum of reflection coefficients of the main amplifier at back-off power, the main amplifier and the auxiliary amplifier at full power.
    - Case (b): The calculation of the objective function is based on the maximum values of the reflection coefficients of the main amplifier at back-off power, the main amplifier and the auxiliary amplifier at full power.

4.11.2.2 Applying the equivalent quarter-wave transmission line network as the output compensation network of the inverted DPA

The output compensation network of Figure 4. 45 is chosen as the output network of the inverted DPA transistors. Consequently, the inverted DPA circuit is now represented as follows:

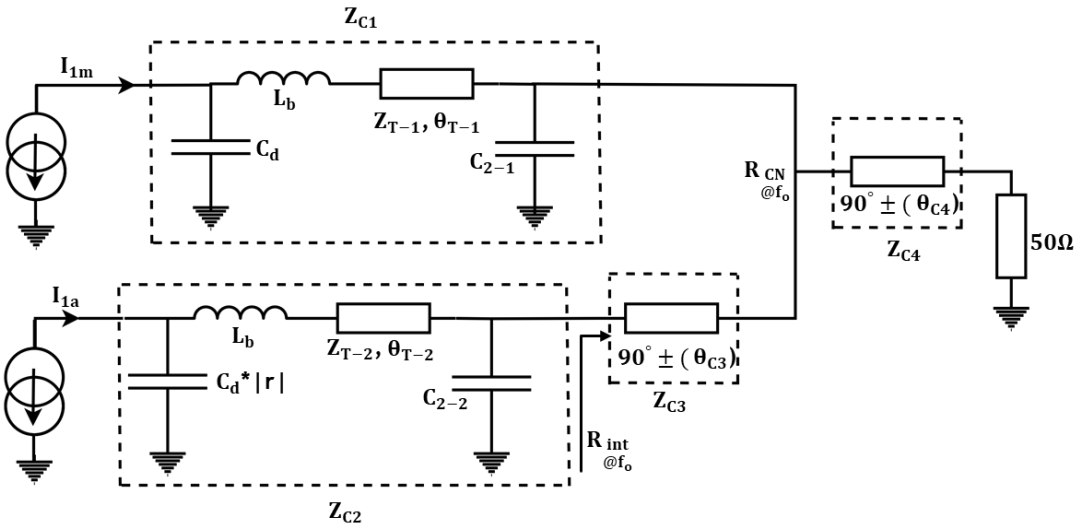


Figure 4. 47: The output network of the proposed inverted DPA

Table 4. 10 gives the summary of the input values of the optimization function.

Table 4. 10: The input values to the optimization function

fmin Optim. GHz	fmax Optim. GHz	Current ratio	Z common node (ohms)	Opt. load at Full Power (ohms)	Ouput Capa. pF	Output Induc. nH
f_{min}	f_{max}	$\|r\|$	Z_{CN}	Ropt	C_d	Lb
2	3	1	36	36	1.3	0.2

Using equation (4. 87), the initial values of the optimization variables (Zc1, Z_{C2}, Z_{C3} and Z_{C4}) in Figure 4. 47, are determined. However, the maximum value of the characteristic impedance Z_{C1} and Z_{C2} are given by:

$$Z_{c1\_max} = Z_{c2\_max} = \frac{1}{C_d . \omega_o} = 49\Omega \tag{4. 104}$$

Thus, $Z_{c1} = 49\ \Omega$ is taken as the initial value of the characteristic impedance at the output of the main amplifier. The calculated initial values of the optimization variables are given in Table 4. 11.

Table 4. 11: The initial values of the optimization variables

Phase slope param.	Z_{c1} main ¼ wave	R inter-mediate	Z_{c2} aux. ¼ wave	Z_{c3} aux. ¼ wave	Z_{c4} output ¼ wave
γ	Z_{C1}	*Rint*	Z_{c2}	Z_{c3}	Z_{C4}
2	49 Ω	50.9 Ω	42.8 Ω	60.5 Ω	42.4 Ω

From the calculated initial values of the impedances Z_{C1} and Z_{C2}, the equivalent transmission line output compensation network elements of the inverted DPA consisting of the characteristic impedance Z_T and its length θ_T, as well as the output capacitance C_2 values can be determined for both the main and auxiliary sections and are therefore given in Table 4. 12 below.

Table 4. 12: The values of the output network parameters of an inverted DPA

Z_{c1} with parasitic elements			Z_{c2} with parasitic elements		
Z_{T-1}	θ_{T-1} (d°)	C_{2-1} (pF)	Z_{T-2}	θ_{T-2} (d°)	C_{2-2} (pF)
-	0	1.3	82.5 Ω	29°	1.27

The impedance transformation network at the output of the main amplifier in Figure 4. 47 thus becomes a Pi-network composed of Cds-Lb-Cds passive elements. Using the values in Table 4. 12, the matching performance of the inverted DPA in terms of the reflection coefficient and VSWR is illustrated in Figure 4. 48.

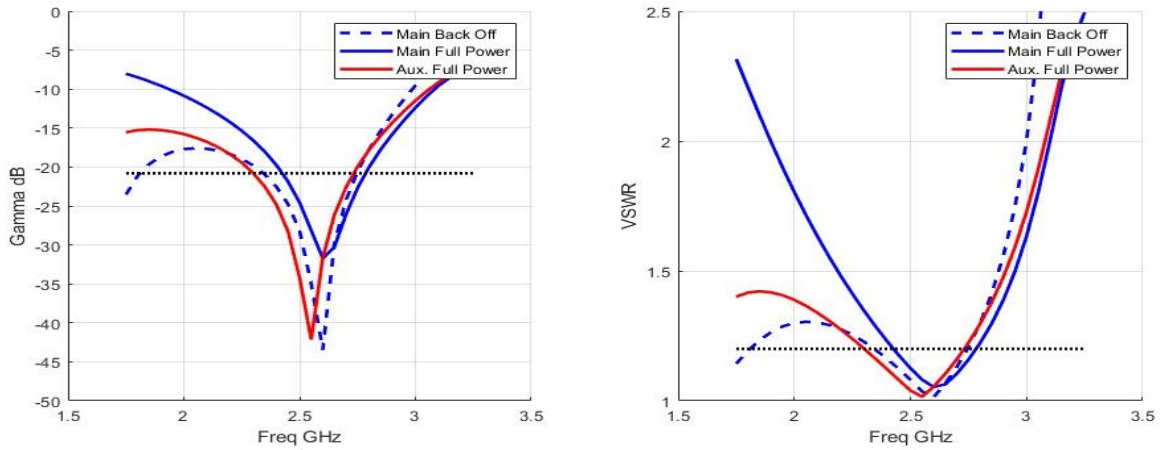


Figure 4. 48: The result of the reflection coefficient in dB and the VSWR performance of a DPA at full and backoff power levels against frequency with initial values

As seen from the result of Figure 4. 48, the matching conditions of the inverted DPA were achieved at the centre frequency of 2.5 GHz and degraded continuously thereafter regardless of the operating conditions of the amplifier.

Following the optimization of the calculated initial values of Table 4. 11 using the fmincon MATLAB optimizer function with the SQP algorithm, the optimized values of the optimization variables based on the case (a) objective function and at a phase slope parameter value of $\gamma = 2$ are therefore given in Table 4. 13 below.

Table 4. 13: Optimized values at $\gamma = 2$

Phase slope param.	Z_{c1} main ¼ wave	Z_{c2} aux. ¼ wave	Z_{c3} aux. ¼ wave	Z_{c4} output ¼ wave
γ	Z_{C1}	Z_{c2}	Z_{c3}	Z_{C4}
2 - case (a)	39.8 Ω	29.5 Ω	33.9 Ω	33.6 Ω

Consequently, Figure 4. 49 shows the frequency response result of the matching conditions of the inverted DPA in terms of the reflection coefficient and VSWR.

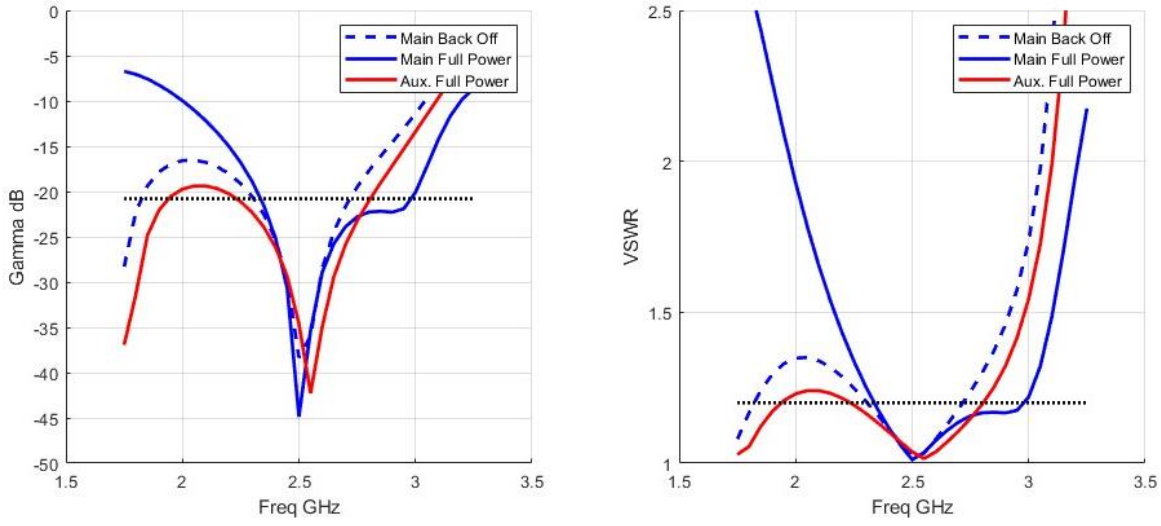


Figure 4. 49: Reflection coefficient in dB and the VSWR performance against frequency with optimized values (Table 4. 13) for $\gamma = 2$

To improve the result, the phase slope parameter γ is added as an optimization variable. The new resulting optimized values based on the cases (a) and (b) objective functions are given in Table 4. 14 below.

Table 4. 14: The new optimized values based on the two cases of the objective function

Phase slope param.	Z_{c1} main ¼ wave	Z_{c2} aux. ¼ wave	Z_{c3} aux. ¼ wave	Z_{c4} output ¼ wave
γ	Z_{C1}	Z_{c2}	Z_{c3}	Z_{C4}
8.8 (case a)	32.1 Ω	16.9 Ω	17.1 Ω	27 Ω
4.3 (case b)	34.7 Ω	14.8 Ω	20.2 Ω	30 Ω

Thus, Figure 4. 50 and Figure 4. 51 showed the plot of the reflection coefficient and the VSWR of the inverted DPA against frequency using the new optimized values in Table 4. 14.

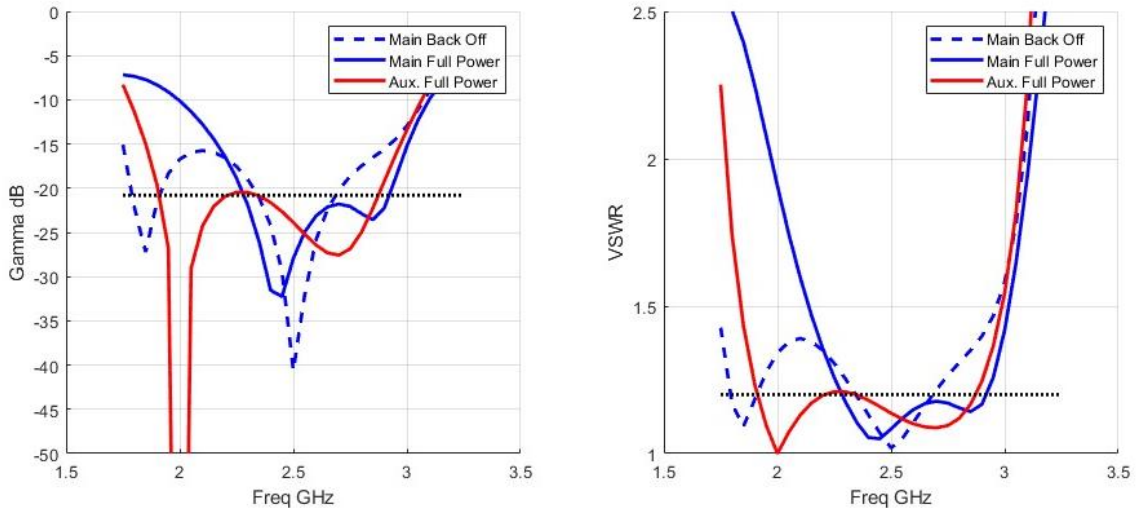


Figure 4. 50: Reflection coefficient in dB and the VSWR performance against frequency based on case (a) objective function

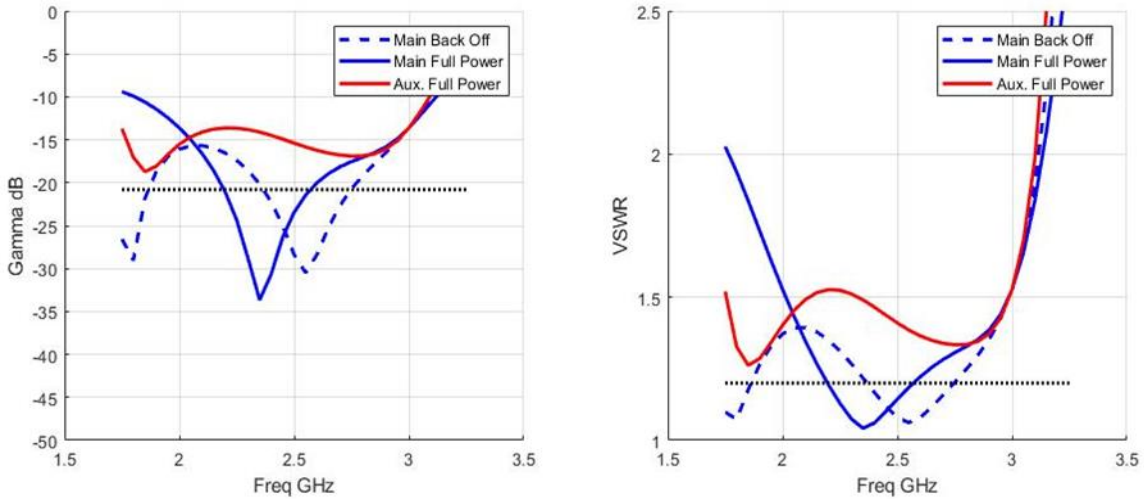


Figure 4. 51: Reflection coefficient in dB and the VSWR performance against frequency based on case (b) objective function

The result of Figure 4. 50 at the edge of the targeted bandwidth (i.e., 2 GHz) indicates that the VSWR or reflection coefficient of the main amplifier at back-off power and the auxiliary amplifier at full power have better performance as their reflection coefficient or VSWR values are close to the threshold value, while that of the main amplifier at full power is far from the threshold value. For the result of Figure 4. 51, the reflection coefficient or VSWR performances of the main amplifier at full and back-off power levels, as well as that of the auxiliary amplifier at full power at 2 GHz, the edge of the targeted bandwidth are relatively better when compared with that of Figure 4. 50.

Furthermore, it can be observed from the results of Figure 4. 49, Figure 4. 50, and Figure 4. 51 that the parasitic elements at the output of the transistors degrade the impedance-matching performance of the amplifier. As such, optimizing the phase slope parameter γ alone is not enough to achieve better impedance-matching performance but has the advantage of allowing the values of the characteristic impedances of the transmission lines to be chosen. Thus, the lengths of the transmission lines (Z_{c3} and Z_{c4}) will also be optimized using the fmincon optimizer function. The consequence will be shifting the impedance matching of the transmission lines by presenting a complex impedance computed at the centre frequency (fo) for the intermediate node between the two transmission lines at the output of the auxiliary amplifier and for the common node of the inverted DPA.

Table 4. 15 below therefore gives the values of the optimization variables based on the case (b) objective function. The optimization variables include the length of the transmission lines.

Table 4. 15: The values of the optimization variables when the length of the quarter-wave transmission lines is considered

Phase slope param.	Z_{c1} main ¼ wave	Z_{c2} aux. ¼ wave	Z_{c3} aux. ¼ wave	Z_{c4} output ¼ wave	Z_{c3} aux. Correction angle $90^o + \theta_{C3}$	Z_{c4} output Correction angle $90^o + \theta_{C4}$
γ	Z_{C1}	Z_{c2}	Z_{c3}	Z_{C4}	θ_{C3}	θ_{C4}
3.18	41.4 Ω	28.7 Ω	40.2 Ω	35.6 Ω	-1.4	+12.7

Figure 4. 52 depicts the corresponding optimized results of the frequency response of the inverted DPA in the form of the reflection coefficient and the VSWR.

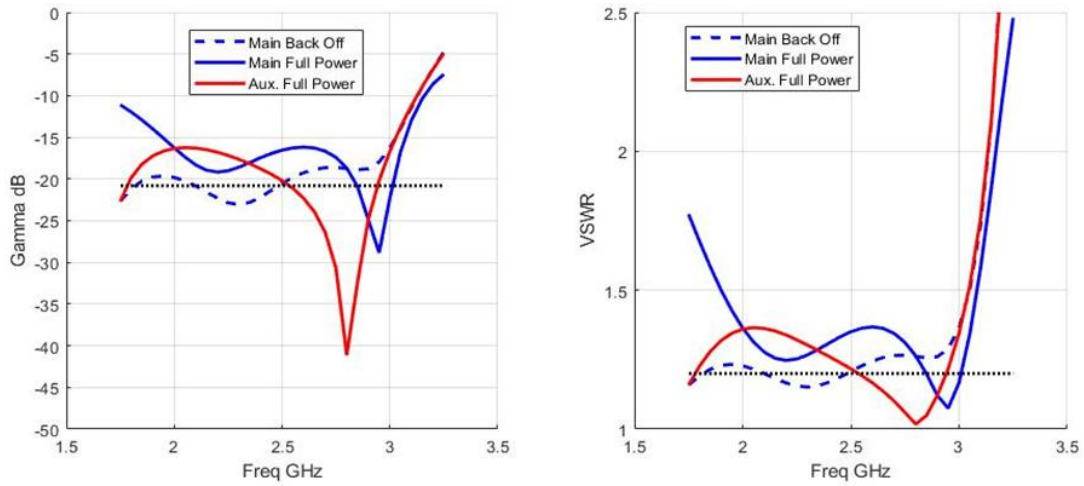


Figure 4. 52: Reflection coefficient in dB and the VSWR performance against frequency with optimization of the length of Z_{c3} and Z_{c4} (Table 4. 15)

The length correction of the equivalent transmission line with characteristic impedances (Z_{c1} and Z_{c2}) at the output of the main and auxiliary amplifiers mentioned earlier improves the matching characteristic. Although the target may not be fully achieved, the matching performance can be deemed acceptable.

Additionally, the optimization result for the asymmetrical inverted DPA case with a current ratio value of |r|=1.5 is illustrated in Figure 4. 53. The corresponding values of the optimization variables based on the case (b) objective function are given in Table 4. 16. This result shows a higher degradation in the matching performance as compared to the symmetrical inverted DPA case with a current ratio value of |r|=1 in Figure 4. 52.

Table 4. 16: The values of the optimization variables for the asymmetrical inverted Doherty power amplifier (DPA) case at |r|=1.5

Phase slope param.	Z_{c1} main ¼ wave	Z_{c2} aux. ¼ wave	Z_{c3} aux. ¼ wave	Z_{c4} output ¼ wave	Z_{c3} aux. Correction angle $90^o + \theta_{C3}$	Z_{c4} output Correction angle $90^o + \theta_{C4}$
γ	Z_{C1}	Z_{c2}	Z_{c3}	Z_{C4}	θ_{C3}	θ_{C4}
3.6	44.8 Ω	20.4 Ω	33 Ω	35.2 Ω	-0.13	+12.9

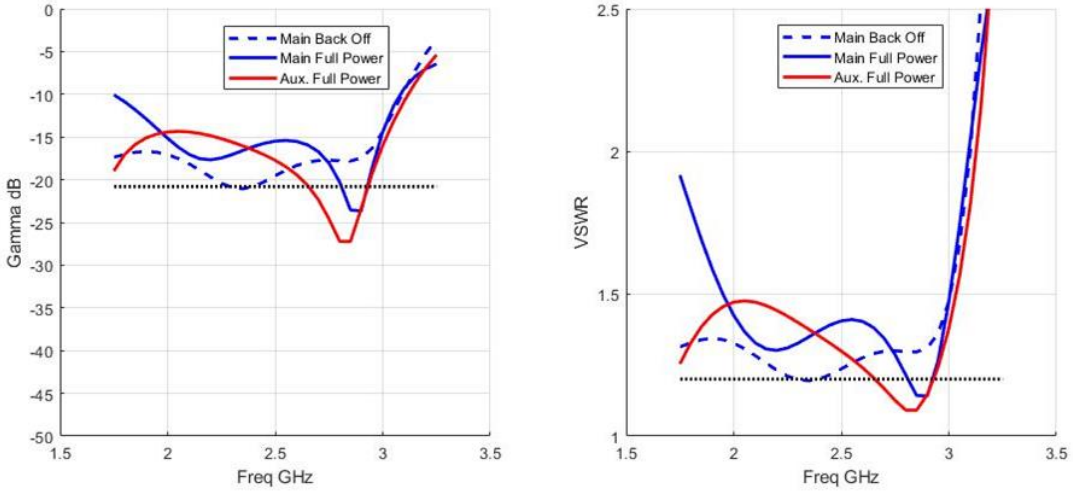


Figure 4. 53: Reflection coefficient in dB and the VSWR performance against frequency for the asymmetrical |r|=1.5 inverted DPA case (Table 4. 16)

In conclusion, the optimization method enables the frequency response of the amplifier to be significantly improved by varying the phase slope parameter γ, the characteristic impedances of the four-equivalent quarter-wave transmission lines, and the electrical lengths of the transmission lines (Z_{c3} and Z_{c4}).

4.12 Harmonic balance simulation results of the conventional and the proposed inverted

4.12.1 Conventional Doherty Power Amplifier

Figure 4. 54 shows the complete schematic diagram of the conventional DPA. The amplifier contains symmetrical two-stage amplifiers, namely, the class B-biased main amplifier and the class C-biased auxiliary amplifier. Both the main and auxiliary amplifiers have the same drain-biased voltage of V_{ds} = 48V. Furthermore, the gate-biased voltage for the main and auxiliary amplifiers is given as V_{Gsm} = -2.75V and V_{Gsa} = -3.5V respectively.

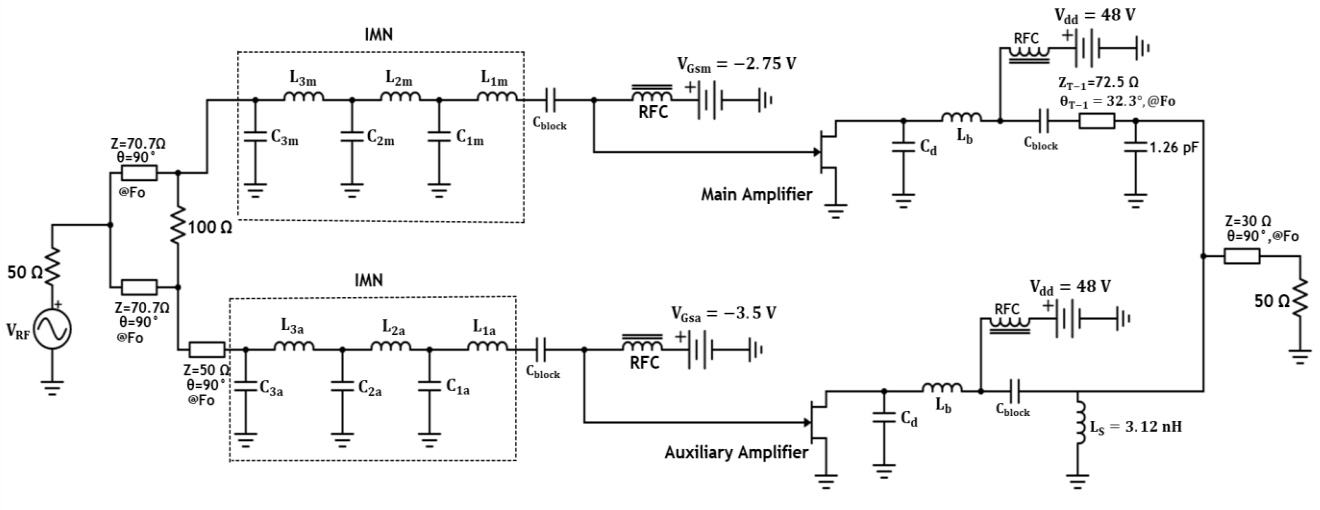


Figure 4. 54: The complete schematic diagram of the conventional DPA

Moreover, the schematic diagram of the simplified GaN transistor model used in designing the conventional and the proposed inverted DPAs is illustrated in Figure 4. 55. In this model, only the equivalent output parasitic capacitance Cd of the device is considered.

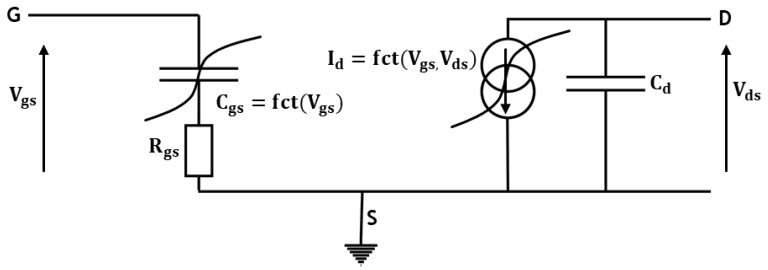


Figure 4. 55: The simplified GaN transistor model

From Figure 4. 54, it can be seen that the quarter-wave transmission line at the output of the main amplifier is represented by the parasitic compensation network of Figure 4. 45. The series bonding wire inductance (L_b) and the shunt LC network at the output of the auxiliary amplifier helps in compensating the reactive part of the parasitic capacitance of the auxiliary transistor. Furthermore, the triple-section lowpass input matching network designed in chapter 2 of this thesis is modified and considered as the input matching network for both the main and auxiliary amplifiers. This lumped element matching network is used to transform the 50Ω system impedance into the desired optimum source impedance values over the desired frequency range of 2-3 GHz.

Table 4. 17 gives the modified values of the input matching network parameters for the main and auxiliary amplifiers of Figure 4. 54. The network parameter values for the conventional DPA are given in Table 4. 3 above.

Table 4. 17: The conventional DPA input matching network parameter values

Input matching networks	L1 (nH)	L2 (nH)	L3 (nH)	C1 (pF)	C2 (pF)	C3 (pF)
Main PA	0.54	0.16	0.61	49.4	50.5	6.63
Auxiliary PA	0.5	0.16	0.61	49.4	50.5	6.63

Thus, Figure 4. 56 and Figure 4. 57 showed the harmonic balance simulation results of the power added efficiency (PAE) and power gain versus the output power at different frequency values within the targeted frequency band of 2-3 GHz.

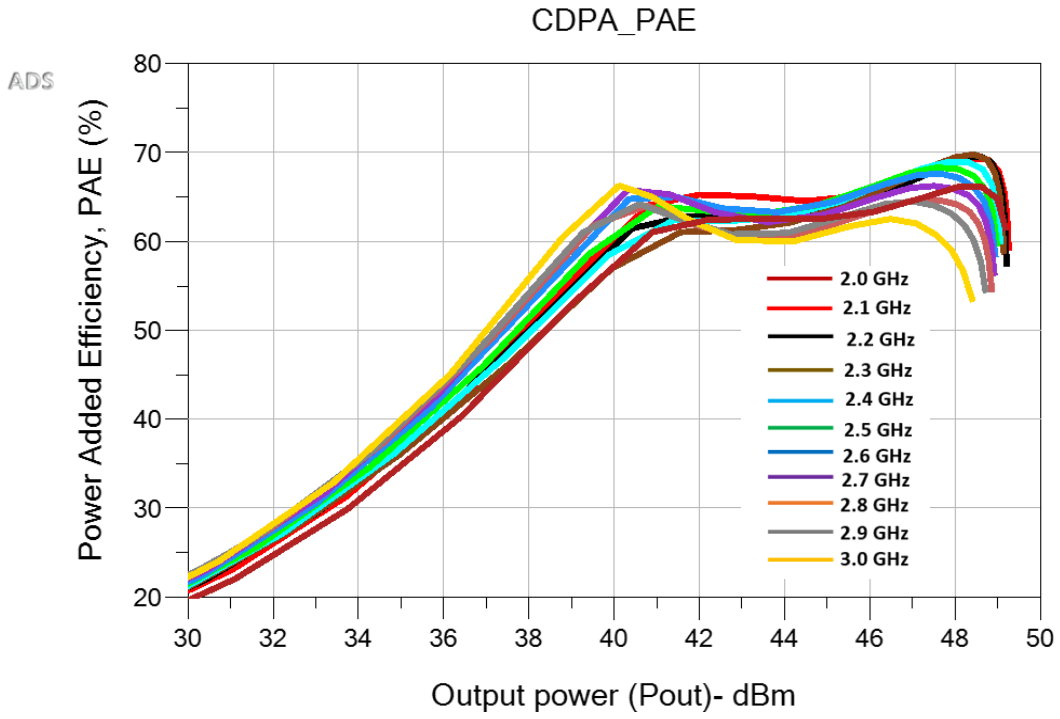


Figure 4. 56: Simulated power added efficiency (PAE) versus the output power in the frequency range of 2–3 GHz for the conventional DPA

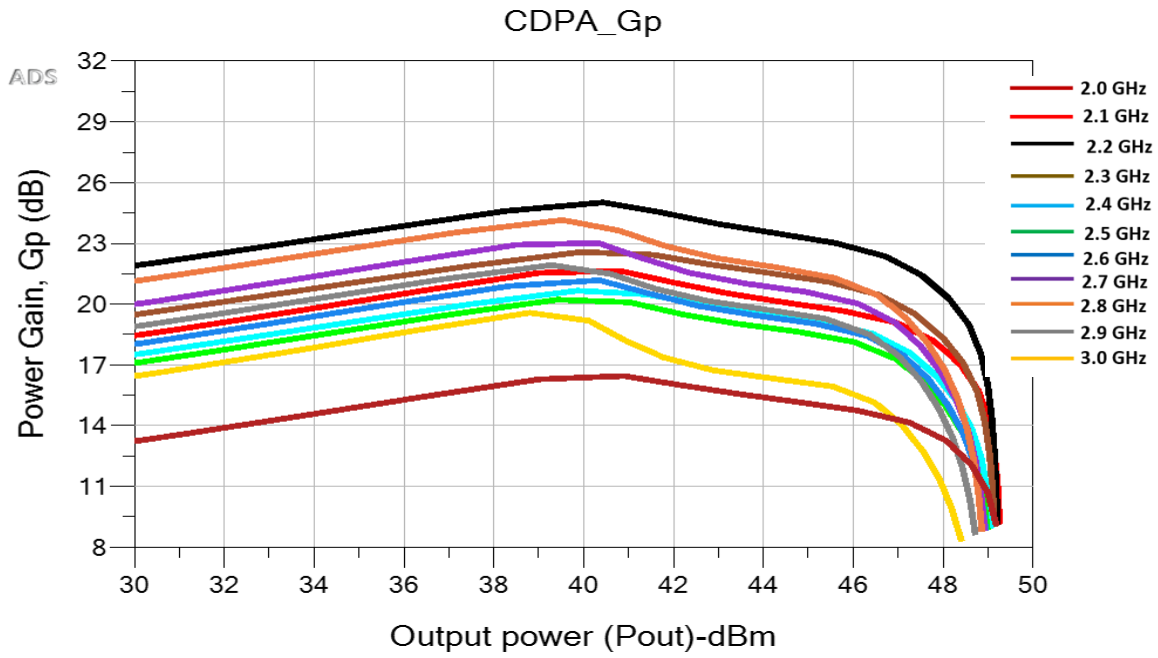


Figure 4. 57: Simulated power gain versus the output power in the frequency range of 2–3 GHz for the conventional DPA

From these results, the behaviour of the conventional DPA is evident, as such, the performance of the simulated PAE achieved at maximum output power and 6 dB output power back-off (OBO) levels in the targeted frequency band of 2-3GHz, which represent 40% fractional bandwidth are measured to be 63%-66.1% and 57%-62% respectively. Moreover, the corresponding power gain performance (see Figure 4. 57) of the conventional DPA (CDPA) at 6 dB output power back-off over the desired bandwidth is 16.3-25 dB.

4.12.2 The proposed inverted Doherty power amplifier (IDPA)

The proposed inverted DPA architecture is presented in Figure 4. 58 below. In this architecture, the output of the auxiliary amplifier is composed of two-section transmission lines for bandwidth extension at full and back-off power levels. The quarter-wave transmission line at the output of the main amplifier and the first quarter-wave transmission line at the output of the auxiliary amplifier are represented by an equivalent quarter-wave transmission line network consisting of two shunt capacitances and a series connected bond-wire inductance and reduced transmission line. This representation helps in absorbing the device output parasitic capacitance as well as enhancing the bandwidth of the amplifier.

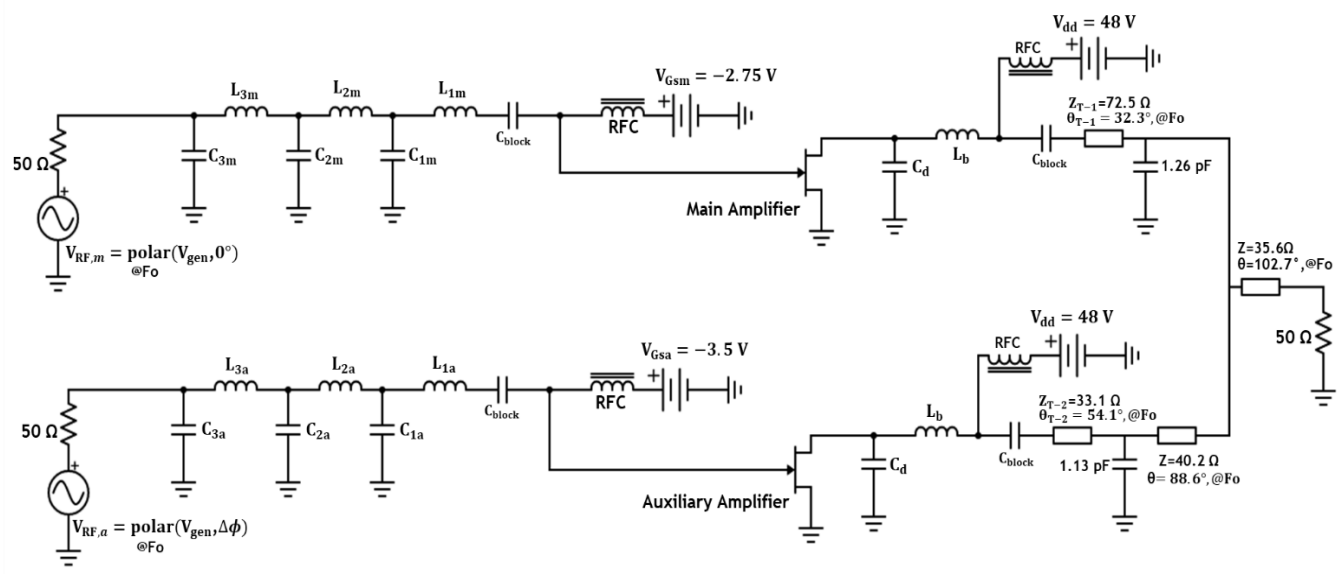


Figure 4. 58: The complete schematic diagram of the proposed inverted DPA

The two symmetrical size transistors of the inverted DPA and their biasing conditions are as obtained with the conventional DPA case. Furthermore, the two voltage sources each with a series 50Ω impedance are improvised as the power sources for the main and auxiliary amplifier paths to allow for the control of the input group delay (or phase slope parameter) between the main and auxiliary amplifiers. This phase slope parameter γ is used to improve the bandwidth of the amplifier.

The expression for the input phase difference of the two voltage sources as a function of frequency and phase slope parameter is given by :

$$\Delta\phi = 90° - \frac{(f - f_o)}{\gamma f_o} \qquad (4.\ 105)$$

where $f_o = 2.5\ GHz$ is the centre frequency and f is any given frequency value around the centre frequency within desired the frequency band of 2-3GHz.The optimized network parameter values of the inverted DPA are given in Table 4. 15.

Similarly, the triple-section lowpass input matching network designed in Chapter 2 of this thesis has been modified and used as the input matching networks for both the main and auxiliary amplifiers of Figure 4. 58. Consequently, Table 4. 18 summarises the modified values of the input matching network parameters for the main and auxiliary amplifiers of Figure 4. 58. Additionally, Figure 4. 59 and Figure 4. 60 showed the corresponding simulated results of the power added efficiency (PAE) and power gain against the output power for the inverted DPA architecture at different frequencies around the targeted frequency band of 2-3 GHz.

Table 4. 18: The inverted DPA input matching network parameter values

Input matching networks	L1 (nH)	L2 (nH)	L3 (nH)	C1 (pF)	C2 (pF)	C3 (pF)
Main PA	0.6	0.15	0.62	49.4	50.5	6.8
Auxiliary PA	0.5	0.16	0.62	49.4	50.5	6.7

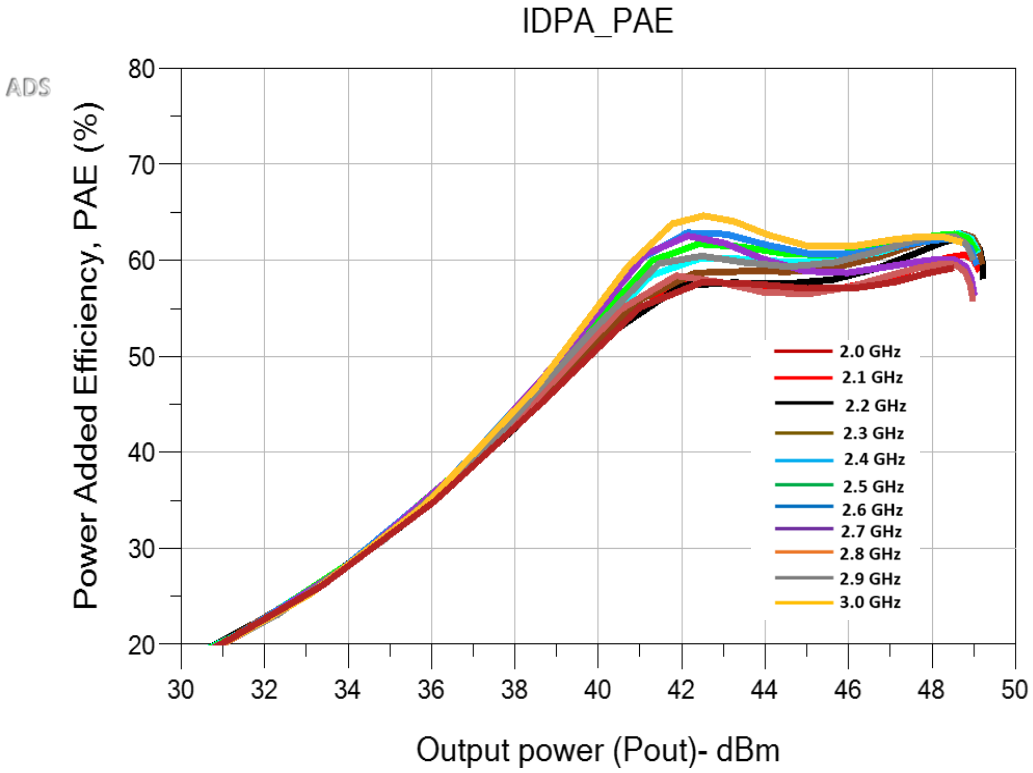


Figure 4. 59: Simulated power added efficiency (PAE) versus the output power in the frequency range of 2–3 GHz for the inverted DPA

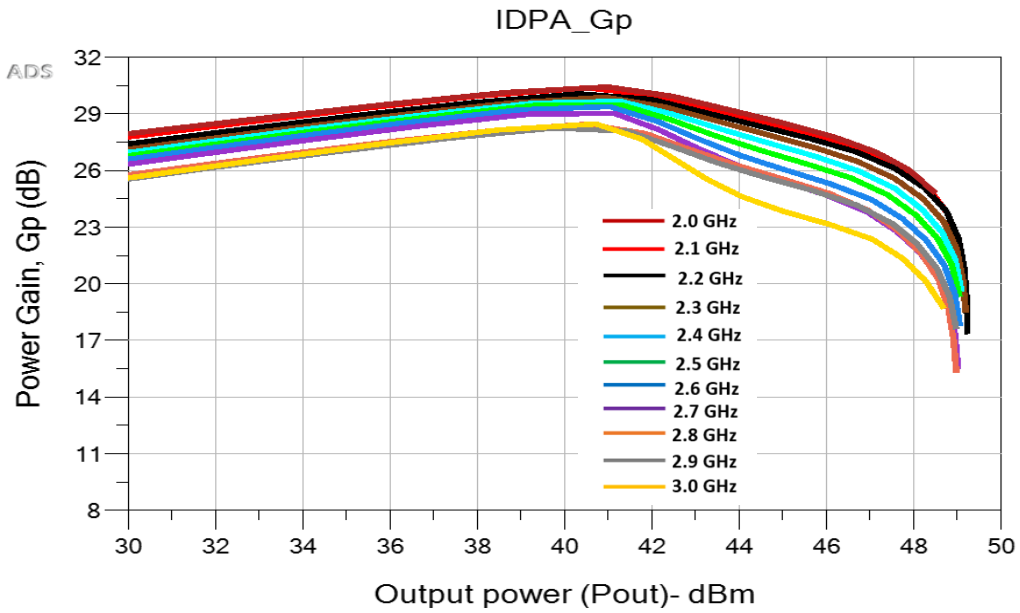


Figure 4. 60: Simulated power gain versus the output power in the frequency range of 2–3 GHz for the inverted Doherty power amplifier (DPA)

It can be seen from the result that the dynamic behaviour of the inverted DPA is well maintained over the desired frequency band of 2-3 GHz. Thus, the PAE and power gain performance achieved at both maximum output power and 6 dB output power back-off levels is less dispersive when compared to that of the conventional DPA case. As such, the performance of the inverted DPA in terms of PAE and power gain is higher than that of the conventional DPA over the frequency band of interest.

4.13 Harmonic balance simulation results of the proposed inverted DPA using a complex GaN transistor model

The schematic diagram of the GaN transistor model used to design the inverted DPA is shown in Figure 1. 17. The model takes into account all the parasitic capacitances, inductances, and resistances associated with the gate, source, and drain terminals. Additionally, it also considers the parasitic capacitances between the gate and drain (Cgd) terminals, as well as between the drain and source (Cd) terminals. The complete schematic diagram of Figure 4. 58 is also used to perform the analysis. However, the lumped element values of the triple-section lowpass input matching networks, which were designed in Chapter 2 of this thesis, have been adjusted to enhance the bandwidth performance. Thus, Table 4. 19 gives the corresponding values of the input matching network parameters for the main and auxiliary amplifiers.

Table 4. 19: The input matching network parameter values of the inverted DPA with complex GaN transistor model

Input matching networks	L1 (nH)	L2 (nH)	L3 (nH)	C1 (pF)	C2 (pF)	C3 (pF)
Main PA	0.52	0.16	0.62	49.4	50.9	6.6
Auxiliary PA	0.1	0.16	0.64	49.4	50.8	6.6

The Figure 4. 61 and Figure 4. 62 showed the simulated results for the power added efficiency (PAE) and power gain. They illustrate how the inverted DPA performs with a complex transistor model across different frequencies in the 2-3 GHz range.

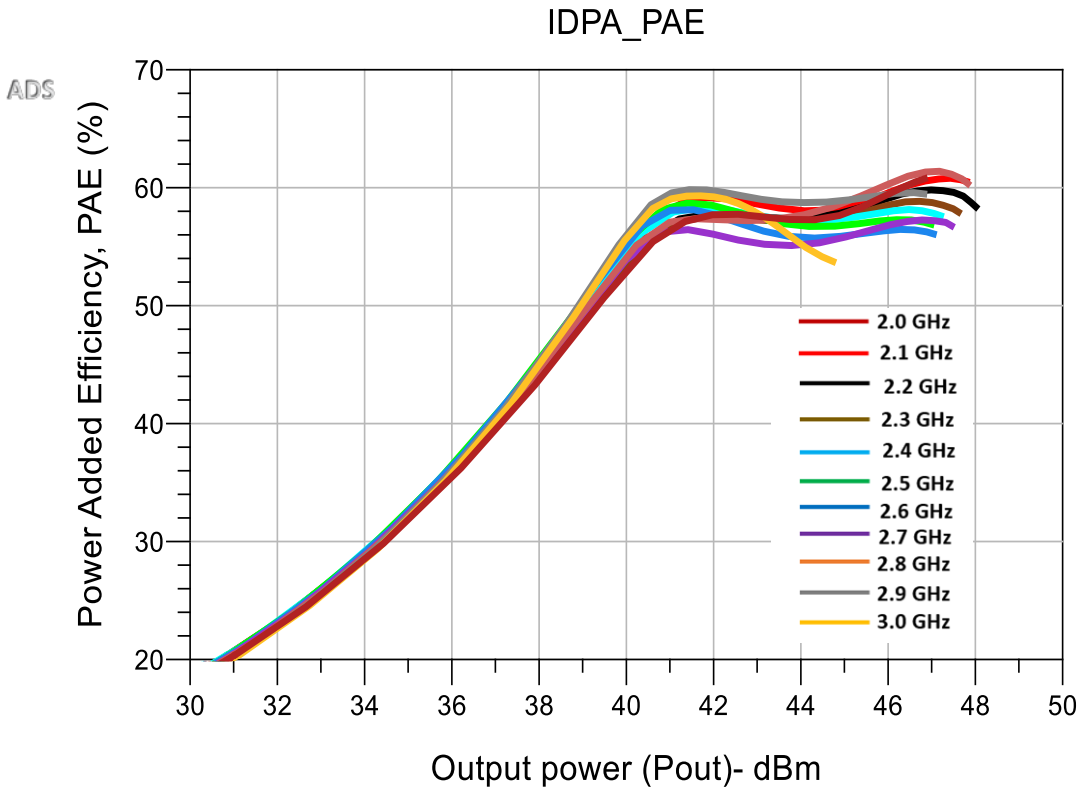


Figure 4. 61: Simulated power added efficiency (PAE) versus the output power in the frequency range of 2–3 GHz for the inverted DPA with complex GaN transistor model

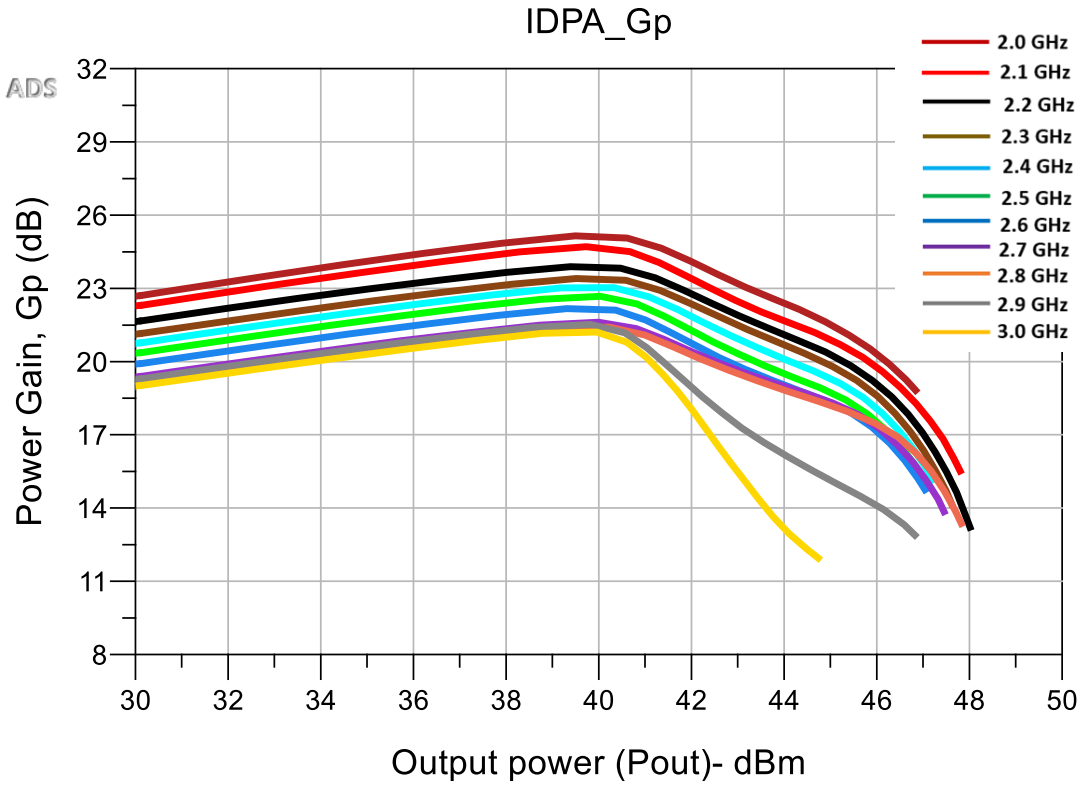


Figure 4. 62: Simulated power gain versus the output power in the frequency range of 2–3 GHz for the inverted DPA with complex GaN transistor model

The simulation result in Figure 4. 61 shows that the power added efficiency (PAE) achieved a performance of 52.5% to 57% at the maximum output power and 50.8% to 53.5% at the 6 dB output power back-off (OBO) levels, within the frequency range of 2 to 3 GHz. Furthermore, Figure 4. 62 demonstrates a power gain performance of 21 dB to 25 dB over the desired bandwidth at the 6 dB output power back-off.

4.14 Conclusion

This chapter presents the theory and design of the Doherty power amplifier (PA) technique. We conducted a study on the efficiency of a symmetrical two-stage Doherty PA. The performance characteristics of the Doherty PA are explained for both the conventional and proposed inverted topologies.

We conducted a study on the frequency behaviour of the conventional DPA and an inverted DPA, proposed by [51], with a phase control as a function of frequency between the main and auxiliary amplifiers. We optimized the output network parameters of the proposed inverted DPA using the MATLAB fmincon optimizer function with the SQP algorithm and compared it with the conventional DPA. The results showed that optimizing the inverted DPA output network can enhance its operational

bandwidth, as indicated by the reflection coefficient and VSWR. The applied optimization procedure can be used as a design method for the adjustment of phase slope, characteristic impedance and length of transmission lines.

To further compare the bandwidth performance of these DPA topologies, we carried out non-linear simulation of the conventional and the inverted DPA on the ADS software using simple and complex GaN transistor models. The simulation results of the power added efficiency (PAE) and power gain at both the maximum and 6 dB output power back-off levels for the proposed inverted DPA over the desired frequency band of 2-3 GHz demonstrate a wider bandwidth and less frequency dispersion compared to the conventional DPA case.

General Conclusion

As an introduction to this work, we present the evolution of cellular communication standards and architecture of the radio frequency front end in an RF transmitter. Performance metrics of an RF power amplifier and an overview of the GaN-based RF power device technology used in this work, as well as other RF power device technologies was provided. We also analyze the various classes of operation for power amplifiers and we conclude the chapter by presenting the methodology for designing RF power amplifiers and determining the values of PA design parameters.

In chapter two, we provided a general overview and detailed analysis of different configurations of lumped element-based matching networks using the analytical approach. We specifically focus on designing single, Pi, T, and dual-section lumped element-based lowpass impedance matching networks. The equations provided enable us to satisfy the matching conditions at the centre frequency Fo or at two frequencies in the case of the double-section matching network's bandwidth. These equations aid in the design of the transistor's matching networks, taking into account the parasitic capacitors at the GaN transistor's gate and drain terminals. We compared the return loss results of these lowpass input and output matching network configurations over a frequency range of 2.1 GHz to 2.9 GHz, centred around 2.5 GHz.

Despite considering the transistor's parasitic capacitances, we have not achieved the optimal matching bandwidth for both the input and output matching networks. Thus, it becomes necessary to optimize the network parameter values of the double and triple section lowpass input and output matching networks using optimization solvers, in order to enhance the matching bandwidth performance.

In the 3rd chapter, we present a method for creating wide-band impedance matching networks using optimization solvers in MATLAB's Optimization Toolbox. These solvers are utilized to optimize the network parameters values of the double and triple-section lowpass input and output matching networks for the power transistor illustrated in Figure 2. 11. The purpose of these matching networks is to match resistive source impedance to complex load impedance, and vice versa. The fractional bandwidth achieved by the optimized double-section lowpass input and output matching networks is 27.6% and 52%, respectively. Similarly, the optimized triple-section lowpass input and output matching networks for the amplifier achieve a fractional bandwidth of 36.4% and 60.8%, respectively.

Additionally, we compared the performance of the MATLAB optimization solvers using the optimized network parameters of the six-element lowpass input matching network, subjecting them to various randomly generated initial values within a range of +/-100% and +/-50% deviation from the optimum

value. Both the fmincon optimization solver with the SQP algorithm and the fmincon solver with the active-set algorithm demonstrate robustness to variations in initial values and converge more quickly to the optimal values compared to the other three optimization solvers.

Furthermore, we design and simulate a single-stage class B RF power amplifier with four different sets of lowpass matching networks for its input and output. The case corresponding to the optimized triple-section input matching network and double-section output matching network exhibits excellent performance. These matching network pairs operate within the frequency range of 2.1 to 2.9 GHz. They deliver an output power of 43 dBm, with a power-added efficiency (PAE) of over 50%. Additionally, they exhibit an associated power gain ranging from 20 dB to 21 dB.

In the 4th chapter, we described the theory and design of two Doherty power amplifier techniques: the conventional Doherty and the proposed inverted Doherty. These amplifiers were evaluated in the frequency range of 2 GHz to 3 GHz, utilizing GaN-based transistors. The equations for varying the load and characteristic impedances presented to the output of the Doherty power amplifiers as a function of frequency were derived. The objective was to compare their bandwidth performance, specifically in terms of the voltage standing wave ratio (VSWR) or reflection coefficient, of both Doherty power amplifier topologies at full power and 6 dB backoff power levels. Bandwidth improvement was accomplished by adjusting and optimizing the output networks and the phase slope between the main and auxiliary amplifiers of the DPA circuits. Furthermore, by using the MATLAB fmincon optimizer function with the SQP algorithm, we optimized the output network parameters of the proposed inverted DPA and compared them with the conventional DPA. The results demonstrated that optimizing the output network of the inverted DPA can significantly improve its operational bandwidth, as evident from the frequency response of the VSWR or reflection coefficient. However, the conventional DPA architecture showed minimal improvement in bandwidth.

In order to further evaluate the bandwidth performance of these DPA topologies, we performed non-linear simulations using both simple and complete GaN transistor models. The simulations were conducted on the ADS software. The results, focusing on the frequency response of the power added efficiency (PAE) and power gain at full and 6 dB output power back-off levels, indicated that the proposed inverted DPA has a wider bandwidth and less frequency dispersion compared to the conventional DPA case over the desired frequency band of 2-3 GHz.

PERSONAL CONTRIBUTIONS

- Improvement of the matching bandwidth of impedance-matching networks by designing them using the optimization method for RF power amplifier applications. Evaluation of the convergence of different optimization algorithms for matching elements.
- Study of the frequency behaviours of the conventional and the proposed inverted Doherty power amplifiers by deriving the equations of the load and characteristic impedances presented to the output of the Doherty power amplifiers as a function of frequency.
- Proposition of the Doherty design method to increase bandwidth performances based on optimization of the output network parameters and the phase slope between the main and auxiliary amplifiers of the proposed inverted DPA.
- Harmonic balance simulations of the conventional and the proposed inverted DPAs global circuits.

FUTURE PROSPECTS

- Verification of the behaviour of the designed inverted Doherty power amplifier with an industrial foundry or using hybrid components.

Résumé en français

Candidate : Abdulrazaq ABDULAZIZ, PhD Student, Universite de Poitiers, France

Thesis title: Bandwidth Enhancement of GaN-Based High-Efficiency Power Amplifiers for telecommunication applications

Titre de la thèse : Amélioration de la bande passante d'amplificateurs de puissance GaN pour applications de télécommunication

Résumé du Chapitre 1

Pour répondre aux demandes croissantes de transmission de données sans fil, sur des bandes de fréquences multiples et larges, il est important de rechercher des architectures électroniques capables de fonctionner efficacement sur de larges bandes passantes. Le chapitre I présente le contexte du travail de recherche et décrit brièvement l'histoire des normes de communication cellulaire, de la première génération (1G) à la cinquième génération (5G), ainsi que l'architecture frontale RF d'un émetteur radio, en mettant l'accent sur le transistor de puissance qui constitue la base de l'amplificateur de puissance RF proposé pour l'analyse et la conception dans le cadre de cette thèse.

Dans la section I.2, nous présentons l'évolution de la communication cellulaire en décrivant brièvement les cinq générations de réseaux cellulaires qui ont vu le jour au cours des 40 dernières années.

En 2018, la 5G est proposé avec trois objectifs principaux, qui sont d'améliorer les communications à haut débit avec des capacités élevées, d'assurer des communications ultra-fiables à faible latence et des communications massives de type machine.

Dans la section 1.3, nous expliquons brièvement le système frontal RF d'un émetteur RF moderne. Le frontal RF, qui est la clé de tout système sans fil, se compose de plusieurs sous-circuits, notamment des amplificateurs de puissance, des oscillateurs, des mélangeurs, des filtres et des circuits en bande de base. Au sein de l'architecture de l'émetteur, l'amplificateur de puissance (PA) est le composant le plus critique et, en tant que tel, représente 50 % de la consommation d'énergie globale, de plus ses performances déterminent la qualité des systèmes de communication. C'est pourquoi les travaux de cette thèse sont principalement axés sur l'amplificateur de puissance dans le bloc d'émission RF. Les paramètres de performance les plus importants utilisés pour évaluer la performance de l'amplificateur de puissance RF sont présentés. Parmi ces paramètres il y a le rendement en puissance ajoutée (PAE), le gain de puissance, la puissance de sortie et le point de compression du gain à 1 dB.

La section 1.4 donne un aperçu de la technologie des dispositifs de puissance RF à base de GaN utilisée dans ce travail, ainsi que d'autres technologies de dispositifs de puissance RF. La fréquence et le niveau de puissance de sortie souhaités sont les principaux paramètres de performance à prendre en compte pour déterminer le choix du dispositif de puissance RF à utiliser. Si les transistors à base de silicium sont à faible coût, leurs performances sont limitées en termes de rendement, de bruit et de puissance de sortie, ce qui a conduit à l'utilisation de matériaux III/IV tels que l'arséniure de gallium (GaAs) ou le nitrure de gallium (GaN) dans de nombreuses applications RF de puissance.

Des modèles généraux de transistors à effet de champ (FET) idéaux et non linéaires pour la conception d'amplificateurs de puissance sont également présentés. Ensuite, les caractéristiques des classes de fonctionnement d'amplificateurs de puissance, qui fonctionnent selon le principe de variation de l'angle de conduction, sont analysées. Ce groupe d'amplificateurs de puissance est constitué des amplificateurs de classe A, AB, B et C. Les calculs des valeurs moyennes des tensions et courant de drain permettent d'estimer la consommation électrique, alors que les amplitudes donnent la puissance de sortie délivrée par les transistors. Ces grandeurs permettent le calcul du rendement électrique de l'amplificateur. Des comparaisons sont menées entre ces différentes classes de fonctionnement. Nous avons conclu ce chapitre en présentant la méthodologie de conception des amplificateurs de puissance RF qui permet d'établir les valeurs des paramètres de conception des amplificateurs de puissance pour un modèle de transistor GaN. Après simulation non linéaire du type équilibrage harmonique, les performances en rendement et puissance sont également données pour un fonctionnement à une fréquence de 2.5 GHz, comme illustré sur la figure ci-dessous pour différentes valeurs de la résistance de charge.

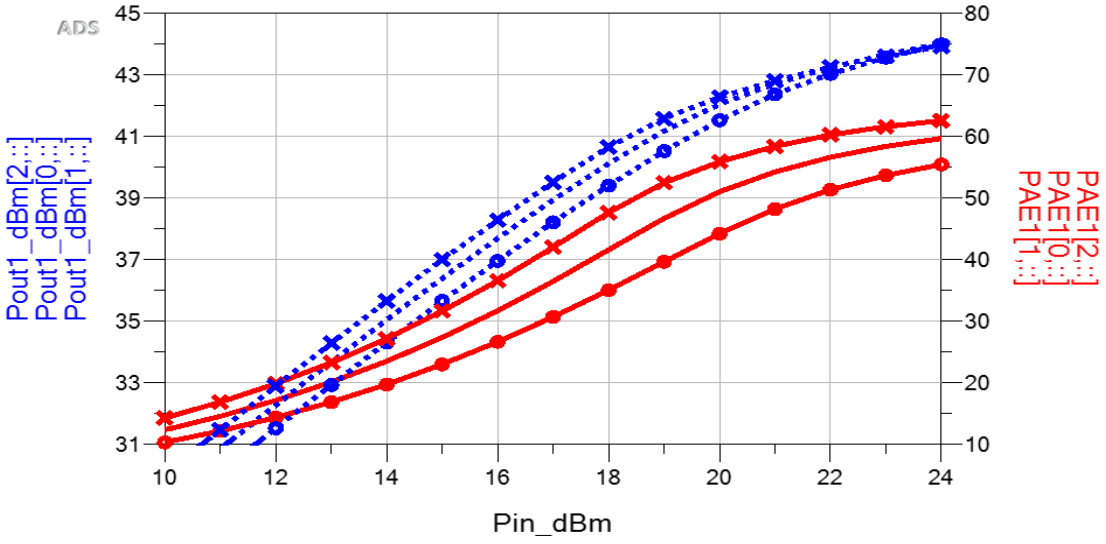


Figure 1.23 du manuscrit: Puissance de sortie (ligne pointillée) et Performances en PAE (ligne continue) pour trois résistances de charge de 32 Ω ohm (symbole du cercle), 36 Ω (pas de symbole) and 42 Ω (symbole x) en fonction de la puissance d'entrée.

Résumé du Chapitre 2

Le chapitre 2 de cette thèse est consacré à une présentation générale et à une analyse détaillée de différentes configurations de réseaux d'adaptation d'amplificateurs à base d'éléments localisés, en utilisant des approches analytiques de calcul des valeurs de composants.

Les réseaux d'adaptation sont conçus pour assurer un transfert de puissance maximal entre les différents éléments du système RF dans la gamme de fréquence souhaitée. L'optimisation du transfert de puissance est essentielle entre chaque fonction électronique des systèmes radiofréquences (RF) pour obtenir une meilleure efficacité globale. Outre le transfert maximal de puissance, l'adaptation d'impédance peut également contribuer à minimiser le facteur de bruit dans les amplificateurs à faible bruit (LNA), à minimiser les ondulations dans la réponse de gain et à atteindre une puissance de sortie saturée maximale pour l'amplificateur de puissance (PA).

Le réseau d'adaptation basé sur des éléments localisés est de plus petite taille que celui obtenu avec des éléments distribués et sera ainsi utilisé pour la conception du réseau d'adaptation dans cette thèse. Ainsi, l'objectif de ce chapitre est de concevoir et d'analyser analytiquement les réseaux d'adaptation L passe-bas simples (2 éléments passifs), Pi, T (3 éléments) et à double section (4 éléments) comme réseaux d'adaptation d'entrée et de sortie des transistors.

Les performances d'un réseau d'adaptation d'impédance à une fréquence de fonctionnement donnée dans la bande passante considérée peuvent être définies par le coefficient de réflexion (Γ-gamma) qui représente le rapport des ondes réfléchies et incidentes dans un réseau d'adaptation, ou par le rapport d'onde stationnaire (ROS ou VSWR). Les largeurs de bande fractionnelle de ces réseaux d'adaptation sont calculées et comparées avec pour objectif que leur coefficient de réflexion soit inférieur ou égal à une valeur seuil de -20 dB centrée sur une fréquence de conception de 2,5 GHz. Le réseau ayant la plus grande largeur de bande est recommandé comme réseau d'adaptation d'entrée et/ou de sortie pour le transistor de puissance RF à base de GaN.

Étant donné le rôle important d'un amplificateur de puissance RF pour garantir une station émettrice-réceptrice de base très puissante et efficace énergétiquement, la conception des réseaux d'adaptation de sortie et d'entrée est la clé pour atteindre cet objectif. En général, pour un amplificateur de puissance, l'entrée du transistor est chargée par son impédance d'entrée conjuguée pour obtenir un gain maximal, tandis que la sortie du transistor est adaptée à la charge requise pour obtenir une puissance maximale ou un rendement maximal.

Lors de l'analyse de différentes topologies de réseaux d'adaptation d'impédance, il peut être nécessaire de transformer un réseau parallèle en un réseau série ou vice-versa. Par exemple, le circuit R-C parallèle à l'entrée du transistor peut être transformé en circuit R-C série et présenter toujours la même impédance à la fréquence de fonctionnement F_0. Les équations de conception pour transformer un circuit série R-C ou R-L donné en circuit parallèle R-C ou R-L et vice-versa à une fréquence de fonctionnement F_0 sont présentées à la section 2.2 du présent chapitre.

Dans la section 2.3, les équations de conception pour l'analyse du réseau d'adaptation en L, passe-bas à section unique, avec des impédances de source et de charge réelles puis avec une impédance de source complexe et une impédance de charge réelle ou vice-versa sont dérivées. Le réseau d'adaptation en L à 2 éléments présente l'inconvénient de ne pas permettre au concepteur de circuits RF de contrôler le facteur de qualité (Q) qui dépend des résistances de source de source R_S et de charge R_L. Il en est de même pour des impédances de source ou de charge complexes. Ainsi, l'utilisation d'un réseau d'adaptation en L à section unique impose la largeur de bande sur laquelle les impédances sont adaptées. Cet inconvénient est surmonté en utilisant plus d'éléments passifs dans le réseau d'adaptation.

La section 2.4 de ce chapitre se concentre sur l'élaboration des équations de conception pour l'analyse du réseau d'adaptation L passe-bas à double section, soient 4 éléments. Deux réseaux d'adaptation en L passe-bas à section unique sont montés en série pour former ce que l'on appelle le réseau à double section afin d'améliorer la largeur de bande d'adaptation du réseau. La synthèse est effectuée en écrivant les équations d'adaptation parfaite à deux fréquences distinctes. Pour ce faire, on divise le réseau en deux sections L et on les résout individuellement en introduisant deux impédances complexes dans le plan médian du réseau, l'une du côté de la source et l'autre du côté de la charge.

Dans la section 2.5, nous avons conçu les réseaux d'adaptation d'entrée et de sortie passe-bas à section simple, Pi, T et double pour l'amplificateur de puissance RF, en tenant compte des capacités parasites de grille et de drain à l'entrée et à la sortie du transistor GaN. Nous avons comparé les résultats en termes de coefficient de réflexion de ces configurations de réseaux d'adaptation d'entrée et de sortie passe-bas sur une gamme de fréquences de 2,1 GHz à 2,9 GHz, centrée autour de 2,5 GHz. Les résultats de la simulation indiquent que le réseau d'adaptation d'entrée passe-bas à double section présente une meilleure performance d'adaptation d'impédance et une largeur de bande fractionnelle plus élevée de 18,4 % à un seuil Γ-gamma de -20 dB. D'autre part, dans les mêmes conditions d'adaptation, les résultats des réseaux d'adaptation, passe-bas de sortie à double et simple section, ont montré des performances similaires et une largeur de bande fractionnelle améliorée de 24%, par rapport aux réseaux d'adaptation passe-bas de sortie à sections en Pi et en T. En prenant en compte les capacités d'entrée et de sortie du transistor, la largeur de bande d'adaptation optimale souhaitée des réseaux d'adaptation d'entrée et de

sortie de l'amplificateur de puissance RF à base de GaN n'a pas été atteinte en utilisant les expressions analytiques. Il est donc nécessaire d'optimiser les valeurs des paramètres du réseau des réseaux d'adaptation d'entrée et de sortie passe-bas à double et triple section à l'aide de solveurs d'optimisation, afin d'améliorer les performances de la largeur de bande d'adaptation.

Résumé du Chapitre 3

Lorsqu'un réseau d'adaptation est utilisé pour adapter une source d'impédance complexe ou une impédance de charge complexe, il devient extrêmement difficile de trouver une expression pour les composants à utiliser pour augmenter la bande passante. Afin d'obtenir une adaptation à large bande pour le transistor, il est nécessaire de disposer de méthodes numériques d'optimisation pour la conception des réseaux d'adaptation d'impédance.

Dans ce troisième chapitre, nous présentons une méthode pour créer des réseaux d'adaptation d'impédance à large bande à l'aide de solveurs d'optimisation dans la boîte à outils d'optimisation de MATLAB. Ces solveurs sont utilisés pour optimiser les valeurs des paramètres des réseaux d'adaptation d'entrée et de sortie passe-bas à double et triple section pour le transistor de puissance RF. Pour ce faire, les valeurs des éléments localisés des réseaux d'adaptation d'entrée et de sortie passe-bas à double et triple sections vers l'amplificateur de puissance RF sont d'abord calculées à une fréquence centrale de 2,5 GHz à l'aide des méthodes analytiques détaillées au chapitre 2. Les valeurs calculées de ces éléments sont ensuite optimisées à l'aide des solveurs d'optimisation. L'équation de l'impédance observée à l'entrée d'un réseau d'adaptation est utilisée pour dériver une expression permettant de définir la fonction objective des solveurs d'optimisation.

La section 3.2 présente une vue d'ensemble des solveurs d'optimisation MATLAB. Il existe donc différentes méthodes pour résoudre les problèmes d'optimisation et le choix dépend de la description du système, de la description des objectifs et des contraintes.

Dans l'application que nous proposons, une méthode d'optimisation non linéaire est nécessaire, compte tenu des équations du système et de la fonction « objectif ».

Dans la section 3.3, nous avons présenté les résultats de simulation des réseaux d'adaptation d'entrée et de sortie passe-bas à double section, optimisés pour le transistor de puissance RF en termes de coefficients de réflexion d'entrée et de sortie, à l'aide des solveurs d'optimisation fminsearch, fminunc et fmincon. De même, la section 3.4 présente les résultats de simulation des réseaux d'adaptation d'entrée et de sortie à triple section passe-bas optimisés pour le transistor de puissance RF.

La largeur de bande fractionnelle obtenue par les réseaux d'adaptation d'entrée et de sortie passe-bas à double section (4 éléments passifs) optimisés est de 27,6 % et 52 %, respectivement. Quant aux réseaux d'adaptation d'entrée et de sortie passe-bas à triple section (6 éléments) optimisés pour l'amplificateur, ils atteignent une largeur de bande fractionnelle de 39,6 % et 60,8 %, respectivement. L'amélioration de la largeur de bande fractionnelle est significative lorsque nous la comparons à la largeur de bande

fractionnelle avant optimisation, soit obtenue à l'aide de la méthode analytique. L'optimisation des réseaux d'adaptation d'entrée et de sortie passe-bas à double et triple section a été effectuée à deux et trois points de fréquence respectivement, dans la gamme de fréquences visée de 2,1 à 2,9 GHz.

Un exemple de coefficient de réflexion est donné ci-dessous, après optimisation du circuit de charge d'un transistor modélisé par une capacité de sortie, pour une structure d'adaptation composée de 6 éléments LC passe bas.

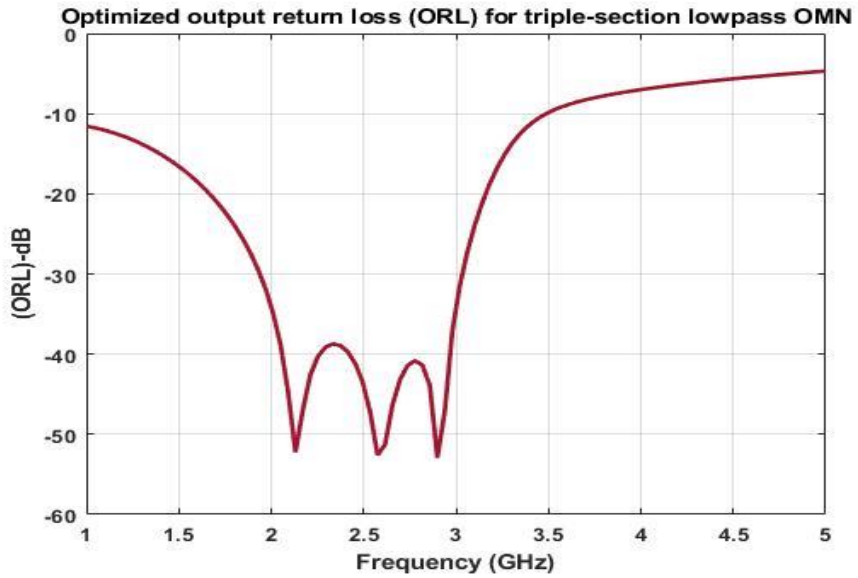


Figure 3. 21 du manuscrit: Coefficient de réflexion en sortie obtenu après optimisation des valeurs des 6 éléments d'adaptation avec le solveur fmincon (interior point algorithm)

Dans la section 3.5, les performances des solveurs d'optimisation MATLAB ont été comparées à l'aide des paramètres optimisés du réseau d'adaptation d'entrée passe-bas à six éléments lorsqu'ils sont soumis à différentes valeurs initiales générées de manière aléatoire dans une plage de +/-100 % et +/-50 % d'écart par rapport à la valeur optimale. Le solveur d'optimisation fmincon (algorithme SQP) et le solveur fmincon (algorithme active-set) sont tous deux robustes à la variation des valeurs initiales et convergent plus rapidement que les trois autres solveurs d'optimisation vers les valeurs optimales.

Enfin, dans la section 3.6, une conception et une simulation, de l'amplificateur de puissance RF de classe B à un étage, ont été réalisées en considérant les réseaux d'adaptation passe-bas optimisés à double et triple sections en entrée en sortie du transistor GaN. Le cas correspondant au réseau d'adaptation d'entrée à triple section optimisé et au réseau d'adaptation de sortie à double section présente d'excellentes performances, dans lequel l'amplificateur de puissance RF délivre une puissance de sortie de 43 dBm, avec un rendement en puissance ajoutée (PAE) de plus de 50 %, et un gain de puissance de 20 dB à 21 dB, dans la gamme de fréquence de 2,1 à 2,9 GHz.

Résumé du Chapitre 4

Le chapitre 4 traite de l'étude théorique et de la simulation du comportement en fréquence de deux techniques d'amplification de puissance : le Doherty conventionnel et le Doherty inversé proposé. Ces amplificateurs sont évalués dans la gamme de fréquences de 2 GHz à 3 GHz en utilisant des transistors à base de GaN. L'objectif est de comparer les performances de la bande passante en termes de rapport d'ondes stationnaires de tension (VSWR) ou de coefficient de réflexion, des deux topologies d'amplificateurs de puissance Doherty, à des niveaux de puissance maximaux et à des niveaux de puissance correspondant à un recul de 6 dB. Pour ce faire, nous ajustons et optimisons leurs réseaux de sortie et la pente de phase entre l'amplificateur principal et l'amplificateur auxiliaire. En outre, nous comparons les résultats de simulation de l'équilibre harmonique des circuits complets d'amplificateurs de puissance Doherty (APD) conventionnels et inversés en termes d'efficacité de la puissance ajoutée (PAE) et de gain de puissance, à pleine puissance et à des niveaux de puissance de sortie à 6 dB de recul.

La section 4.2 est consacrée à la description du principe de fonctionnement de l'amplificateur de Doherty. La technique de l'amplificateur de Doherty permet de faire varier l'impédance de charge de l'amplificateur en fonction du niveau de puissance du signal d'entrée en utilisant une combinaison de deux amplificateurs.

Ainsi la topologie de base d'un amplificateur de puissance de Doherty se compose d'un amplificateur principal (ou carrier) et d'un amplificateur auxiliaire (ou peaking), ainsi que de deux lignes de transmission quart d'onde. En outre, les amplificateurs principal et auxiliaire sont respectivement polarisés en classe B et C afin de décaler la mise en conduction de l’auxiliaire. Le principe de modulation de charge de l'amplificateur Doherty est expliqué. On en déduit que les impédances de charge Zdm ou Zda, que voient l'amplificateur principal et l'amplificateur auxiliaire, peuvent être modifiées ou ajustées en changeant l'amplitude et/ou la phase de leurs sources de courant.

Au paragraphe 4.3, nous avons dérivé une expression pour les impédances de charge vues par les amplificateurs principal et auxiliaire lorsqu'ils sont séparés par la ligne de transmission quart d'onde. La ligne de transmission quart d'onde à l'entrée de l'amplificateur auxiliaire permet d'obtenir un déphasage de 90° entre les courants des transistors principal et auxiliaire.

Les expressions du rendement électrique de l'amplificateur de puissance Doherty à des niveaux de puissance d'entrée faibles, moyens et élevés sont également dérivées. En outre, les rendements de drain des amplificateurs de puissance Doherty, symétriques et asymétriques à deux étages, sont comparés.

Une architecture Doherty dite inversée est également proposée et étudiée. Les caractéristiques de performance de l'amplificateur de puissance de Doherty sont expliquées pour les topologies conventionnelles et inversées proposées, utilisant deux transistors symétriques.

En parallèle avec ce travail de thèse [51] dans le cadre de la thèse de M. Cavarroc avec l'entreprise NXP et notre laboratoire, la technique Doherty inversée a été étudiée et mise en œuvre dans un amplificateur pour massive MIMO. Une attention particulière a été portée à l'effet du déphasage entre les commandes des amplificateurs principal et auxiliaire. Il a été montré l'intérêt de modifier la pente de variation de la phase en fonction de la fréquence pour augmenter la bande passante de l'amplificateur.

Nous avons mené une étude sur le comportement en fréquence de l'APD conventionnel et de l'APD inversé proposé. L'objectif était d'établir les équations des impédances présentées à chaque étage en fonction du mode de fonctionnement, recul en puissance ou pleine puissance, afin de pouvoir comparer les 2 structures en terme de bande passante . Nous avons optimisé les paramètres du réseau de sortie du APD inversé en utilisant la fonction d'optimisation fmincon de MATLAB avec l'algorithme SQP et nous l'avons comparé au APD conventionnel. Les résultats ont montré que l'optimisation du réseau de sortie et de la pente de phase améliore la largeur de bande opérationnelle, comme l'indiquent les tracés du coefficient de réflexion et du ROS. L'amélioration de la largeur de bande est plus importante pour l'APD inversé par rapport à l'architecture APD conventionnelle. L'optimisation a également été menée en prenant en compte les capacités de sortie des transistors et en les intégrant dans les réseaux de charge. Cette étude nous a permis de mettre au point une méthodologie de conception du circuit de charge de l'amplificateur, représenté sur la figure suivante:

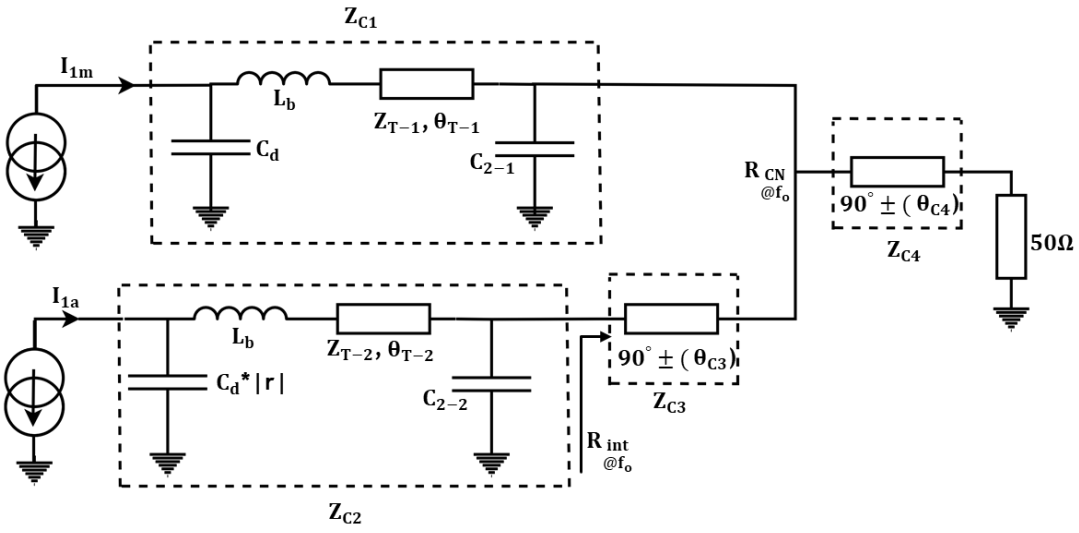


Figure 4. 63: Le réseau de sortie du DPA inversé propose pour l'optimisation

Pour mieux comparer les performances de ces topologies d'APD en matière de largeur de bande, nous avons effectué une simulation non linéaire des circuits globaux de l'APD conventionnel et de l'APD inversé sur le logiciel ADS en utilisant des modèles de transistors GaN simples et complexes. Les résultats de la simulation sont donnés en termes de réponse en fréquence du rendement en puissance ajoutée (PAE) et du gain de puissance pour des niveaux de puissance de sortie maximale et avec un recul de 6 dB sur la bande de fréquence souhaitée de 2-3 GHz. Le Doherty inversé après optimisation montre un fonctionnement optimal sur une plus largeur de bande plus large que l'APD conventionnel.

References

[1] Mohammad Meraj ud in Mir and Dr Sumit Kumar, " Evolution of Mobile Wireless Technology from 0G to 5G ", *International Journal of Computer Science and Information Technologies,* Vol.6(3), pp.2545-2551, 2015.

[2] " Radiolinja's History ", 20 April 2004, Retrieved 23 December 2009.

[3] Nikhil Bhandari, Shivinder Devra, and Karamdeep Singh, " Evolution of Cellular: From 1G 5G ", *International Journal of Engineering and Techniques,* Vol.3(5), Sept-Oct 2017.

[4] N.A. Shairi, B.H. Ahmad and Peng Wen Wong, " SPDT Discrete Switch Design using Switchable Radial Stub Resonator for WiMAX and LTE in 3.5GHz Band ", *IEEE International RF and Microwave Conference (RFM2013),* Penang, Malaysia,2013.

[5] Weng Chuen Edmund Neo, " Highly Efficient and Highly Linear RF Power Amplifiers ", *PhD dissertation at Delft University of Technology,* Netherlands, 2010.

[6] B. Razavi, " RF Microelectronics ", *Prentice Hall,* 1998.

[7] Stephen Terry, " Development of a High-Efficiency, Low-power RF Power Amplifier for use in a High-Temperature Environment ", *Masters Thesis Dissertation at the University of Tennessee*, Knoxville, 2002.

[8] S.C. Cripps, " RF Power Amplifiers for Wireless Communications ", *2nd edn. Artech House, Norwood*, 2006.

[9] S.C. Cripps, " RF Power Amplifiers for Wireless Communications ", *Artech House*, 1999.

[10] H.L.Krauss, C.W.Bostian and F.H.Raab, " Solid State Radio Engineering ", *Wiley*,1980.

[11] Kimon Vivien, " Linearity and Efficiency of Load Modulated Power Amplifiers ", *PhD Dissertation at Université Paris-Est*, France, 2020.

[12] W.Hallberg, *"* Frequency Reconfigurable and Linear Power Amplifiers Based on Doherty and Varactor load Modulation Techniques", *Thesis for the Degree of Licentiate of*

Engineering, Department of Microtechnology and Nanoscience, Chalmers University of Technology Gothenburg, Sweden, 2016.

[13] Tian He, *"* Design of Radio Frequency Power Amplifiers For High Efficiency and High Linearity*", M.sc Dissertation at California State University,* Chico, 2009.

[14] F. Ellinger, J.Kucera, and W.Baechtold, *"* Improvements on a GaAs MESFET model for Nonlinear RF Simulations*", IEEE MTT-S International Microwave Symposium Digest (Cat. No.98CH36192),* pp.1623-1626, Baltimore, MD, USA, 1998.

[15] C.J. Wei, Y.Tkachenko, and D.Bartle, *"* An accurate Large-signal model of GaAs MESFET which accounts for charge conservation, dispersion, and self-heating *", IEEE Transactions on Microwave Theory and Techniques,* vol.46 (11), pp.1638-1644, November 1998.

[16] I.Angelor, L.Bengtsson, and M.Garcia, *"* Extensions of the chalmers Nonlinear HEMT and MESFET model*", IEEE Transactions on Microwave Theory and Techniques,* vol.44 (10), pp.1664-1674, October 1996.

[17] S.C. Dutta Roy, " Characteristics of Single-and Multiple-Frequency Impedance Matching Networks ", *IEEE Transactions on Circuits and Systems*, Vol.62, No.3, pp.222-225, March 2015.

[18] F. R-I. Gomez, " Design of Impedance Matching Networks for RF Applications ", *Asian Journal of Engineering and Technology*, Vol.06, No.04, pp.47-56, September 2018.

[19] A.A. Modesto, F. Santos, J.H. Pereira, B. Leite and A.A. Mariano, " A CMOS power amplifier with reconfigurable power cells and matching network for 2.4GHz wireless communications ", *International Journal of Electronics and Communications (AEU),* Vol.111, pp.1-10, November 2019.

[20] H. Oraizi and A-R. Sharifi, " Design and Optimization of Broadband Asymmetrical Multisection Wilkinson Power Divider ", *IEEE Transactions on Microwave Theory*

Techniques, Vol.54, pp.2220-2231, 2006.

[21] Y. Liu, Y.J. Hao, and Y.Hao, " Lumped Dual Frequency Transformer For Frequency Dependent Complex Loads ", *Progr. Electromagn. Res.*, Vol.126, pp.121-138, 2012.

[22] Y.Liu, Y. Chen and Y.J. Zhao, " Lumped Triple-Frequency Impedance Transformer ", *Electron.Lett*., Vol.48, No.19, pp.1193-1194, Sept. 13, 2012.

[23] Michael Steer, " Microwave and RF Design: A Systems Approach ", *SciTech Publishing; INC*, Raleigh, North Carolina, pp. 413,2010.

[24] T.T.Ha, " Solid-State Microwave Amplifier Design ", *John Wiley & Sons, Hoboken, Nj,*1981.

[25] Andrei Grebennikov, " RF and Microwave Power Amplifier Design", *McGraw-Hill Professional Engineering,* U.S.A, 2005.

[26] J. Yousaf, H. Jung, K.Kim, and W.Nah, " Design, Analysis, and Equivalent Circuit Modelling of Dual Band Pifa Using a Stub for Performance Enhancement ", *Journal of Electromagnetic Engineering and Science*, Vol.16, pp.169-181, 2016.

[27] J. Yousaf, M. Amin, S. Iqba, and H. Durrani, " Analysis of Conducted Emission Measurements of Dc-Dc Converter with Load For Proper Filter Design ", *International Journal of Microwave and Optical Technology*, Vol.10, pp.464-470,2015.

[28] Gary Breed, " Improving the Bandwidth of Simple Matching Networks ", *High Frequency Electronics Summit Technical Media, LLC,* 2008.

[29] J. Yousaf, Z. Mehmood, W. Abbas and K. Shehzad, " Design of Broadband Matching Network for Complex Reactive Load Using L-Matching ", *In Proceedings of The Pakistan Academy of Sciences, Physical and Computational Sciences,* Vol.54, No.3, pp.243-255,2017.

[30] Chris Bowick, et al, " RF Circuit Design ", *2nd ed., Newnes imprint, Elsevier*, Chapter 4,

2008.

[31] B.Becciolini, " Impedance Matching Networks Applied to RF Power Transistors ", *RF Application Information Freescale Semiconductor*, 2005.

[32] Francois de Dieuleveult, Olivier Romain, " Electronique Appliquée Aux Hautes Fréquences : Principles et applications ", *Dunod*, 2ième édition, 2008.

[33] Hendrik W.Bode, " Network Analysis and Feedback Amplifier Design ", *Institute News and Radio Notes*, D.Van Nostrand Co.,Inc New York,1945.

[34] R.M.Fano, " Theoretical Limitations on the Broadband Matching of Arbitrary Impedances ", *Journal of Franklin Institute*, January-February,1950.

[35] Nelder, J.A and Mead,R, " A simplex method to a function minimization ", *Comput.J.,7*, pp.308-313,1965.

[36] fr.mathworks.com, " Optimization Toolbox ", *(nd) Retrieved from :* http://www.fr.mathworks.com/help/optim/index.html, Searched in Nov 2022.

[37] The Mathworks, Inc., " Solving optimization problems with MATLAB ", *Retrieved from:* https://www.matlabexpo.com/content/dam/mathworks/mathworks-dot-, 2018.

[38] The Mathworks, " Optimization Toolbox for use with MATLAB ", *Mathworks, Inc.*,2001.

[39] J.C. Lagarias, J.A. Reeds, M.H.Wright, and P.E.Wright, " Convergence properties of the Nelder- Mead Simplex Method in low Dimensions ", *SIAM Journal of Optimization*, Vol.9, Number 1, 1998, pp.112-147.

[40] W.H. Doherty, " A new high-efficiency amplifier for modulated waves ", *Proceeding of the IRE*, vol.24, no.9, 1936.

[41] F.H. Raab, " Efficiency of Doherty RF Power-Amplifier Systems ", *IEEE Transactions on Broadcasting*, vol. BC-33, no.3, pp.77-83, Sept.1987.

[42] Abbas Nasri et al, " Design of a wideband Doherty power amplifier with high efficiency for 5G applications ", *Electronics Journal*, 10,873, 2021.

[43] Eric Kerherve, " Linearization and Efficiency Enhancement Techniques for Silicon Power Amplifiers from RF to mmW ", *Elsevier Inc.,* pp.83, 2005.

[44] Yang, Youngoo, Jaehyok Yi, Young Yun Woo, and Bumman Kim, " Optimum Design for Linearity and Efficiency of a Microwave Doherty Amplifier Using a New Load Matching Technique ", *Microwave Journal,* vol.12, 2001.

[45] M. Iwamoto, A. Williams, C. Pin-Fan, A. G. Metzger, L. E Larson, and P. M.Asbeck, " An Extended Doherty Amplifier with High Efficiency Over a Wide Power Range ", *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 12, pp. 2472-2479, Dec 2001.

[46] B. Kim, I. Kim, and J. Moon, " Advanced Doherty Architecture ", *IEEE Microwave Journal*, vol. 11, no. 5, pp. 72-86, Aug. 2010.

[47] Mehran Yahyavi, " On the design of high-efficiency RF Doherty power amplifiers ", *PhD dissertation at Technical University of Catalonia (UPC),* BarcelonaTECH, 2016.

[48] Nicolas DUBUC, " Modelisation Electrothermique de Transistors MESFET SiC Et Optimization d'une Architecture Doherty Pour L'amplification de Puissance A Haut Rendement ", *PhD dissertation at Ecole Doctorate Science Technologie-Sante, Universite de Limoges,* November 2003.

[49] Cyril LAGARDE, " Modélisation de Transistor de Puissance en Technologie GaN : Conception d'un amplificateur de Type Doherty pour les Emetteurs a puissance adaptative ", *PhD dissertation at Ecole Doctorale Science-Technologie, Université de Limoges,* September, 2006.

[50] Nicolas DUBUC, Claude Duvanaud, and Philippe Bouysse, " Analysis of the Doherty technique and application to a 900 MHz power amplifier ", *amsacta.unibo.it/id/eprint/434/1/JGM3_Dubuc.pdf,* 2002.

[51] Manuel Cavarroc et al, " Compact 40% Fractional Bandwidth Doherty PA with Input Group Delay Engineering ", *IEEE MTT-S International Microwave Symposium (IMS 2023),* Vol.33, No.6, San Diego, CA, USA, June 2023.

[52] S. Bassam, W. Chen, M. Helaoui, and F. Ghannouchi, " Transmitter architecture for CA: Carrier aggregation in LTE-advanced systems ", *IEEE Microw. Mag.,* vol. 14, no. 5, pp. 78–86, Jul. 2013.

[53] J. Wong, N. Watanabe, and A. Grebennikov, " High-power high-efficiency broadband GaN HEMT Doherty amplifiers for base station applications ", *in Proc. IEEE Topical Conf. RF/Microw. Power Model. Radio Wireless Appl. (PAWR),* Jan. 2018, pp. 16–19.

[54] C. Chu et al., " Waveform engineered sequential load modulated balanced amplifier with continuous class-F-1 and class-J operation ", *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 2, pp. 1269–1283, Feb. 2022.

[55] H. Jang and R. Wilson, " A 225 Watt, 1.8–2.7 GHz broadband Doherty power amplifier with zero-phase shift peaking amplifier ", *in IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2018, pp. 797–800.

[56] J. H. Qureshi, N. Li, W. C. E. Neo, F. van Rijs, I. Blednov, and L. C. N. de Vreede, " A wide-band 20W LMOS Doherty power amplifier ", *in IEEE Int. Microwave Symp. Dig.*, pp. 1504–1507, May 2010.

[57] D. Kang, D. Kim, Y. Cho, B. Park, J. Kim, and B. Kim, " Design of Bandwidth-Enhanced Doherty Power Amplifiers for Handset Applications ", *IEEE Trans. Microwave Theory Tech.*, vol. 59, no. 12, pp. 3474– 3483, Dec. 2011.

[58] David Gustafsson, " Extending the Bandwidth of the Doherty Power Amplifier ", *PhD thesis dissertation at Microwave Electronics Laboratory, Department of Microtechnology and Nanoscience-MC2 Chalmers University of Technology Gothenburg*, Sweden, 2014.

[59] Gholamreza Nikandish, and Anding Zhu, " Breaking Bandwidth Limit: A Review of Broadband Doherty Power Amplifier Design for 5G ", *IEEE Microwave Magazine,* August 2019.

Abstract

The work presented in this thesis focuses on the design and analysis of single-ended and Doherty power amplifier configurations by using analytical and optimization methods to determine the values of lumped element-based matching networks. Given the important role of an RF power amplifier in ensuring a powerful and efficient base transceiver station, the selection and adjustment of the input and output matching networks of the transistor is a key point. The objective of this dissertation is to propose a design method for an RF power amplifier circuit to enhance the bandwidth performance of the power amplifier in the base transceiver station, specifically in terms of power added efficiency (PAE), power gain, and output power. Firstly, the design of the single, Pi, T, dual, and triple sections lowpass input and output matching networks to the RF power amplifier is presented. Optimization methods are evaluated to find the element values of the matching networks for a GaN-based RF power transistor operating at 2.5 GHz.

In the last part, we examine the efficiency of the Doherty Power Amplifier (DPA) for base stations when operating at backoff power levels and at full power. The design, analysis, and simulation of the frequency behaviour of conventional and inverted DPA architectures in the frequency range of 2 GHz to 3 GHz using a GaN-based FET transistor are presented. By adjusting and optimizing their output networks and the phase slope between the two amplifiers, it is possible to improve the bandwidth of the DPA. We find that the inverted DPA offers better bandwidth performance. Based on this finding, we propose a design method for the inverted DPA, which involves adjusting various parameters using an optimization technique. Finally, we performed a harmonic balance simulation on both the global conventional and the proposed inverted Doherty PA circuits, which have a peak power of about 47 dBm. The simulated results confirm that the frequency response of the proposed inverted DPA, in terms of the power added efficiency (PAE) and power gain at full and 6 dB output back-off power levels, is less dispersive compared to the conventional DPA case. The performance of the inverted DPA achieved a PAE of 52.5% to 57% at the maximum output power and 50.8% to 53.5% at the 6 dB output power back-off (OBO) levels, in the frequency range of 2 to 3 GHz.

Keywords: RF power amplifier, Doherty structure, GaN transistor, input and output matching networks, optimization method, Power added efficiency, Bandwidth.

Résumé

Le travail présenté dans cette thèse consiste en la conception et l'analyse de configurations conventionnelles et de type Doherty d'amplificateurs de puissance en utilisant des méthodes analytiques et d'optimisation afin de déterminer les éléments des réseaux d'adaptation. Etant donné le rôle important d'un amplificateur de puissance RF pour assurer une station d'émission très puissante et efficace, la conception des réseaux d'adaptation, d'entrée et sortie des transistors, est un élément clé. L'objectif de cette thèse est de proposer une méthode de conception d'amplificateurs de puissance RF pour améliorer les performances en termes de rendement en puissance ajoutée (PAE), de gain de puissance et de puissance de sortie sur une grande bande passante de l'amplificateur de puissance pour les stations de base. Tout d'abord, la conception des réseaux d'adaptation d'entrée et de sortie passe-bas à section simple, Pi, T, double et triple de l'amplificateur de puissance RF est présentée. Des méthodes d'optimisation sont évaluées pour déterminer les valeurs des éléments des réseaux d'adaptation pour le transistor de puissance RF de type GaN, utilisé à 2.5 GHz.

Dans la dernière partie, les architectures d'amplificateur Doherty DPA sont testées en terme de rendement pour des conditions de fonctionnement en recul de puissance ou à pleine puissance. Nous analysons le comportement en fréquence des DPA conventionnel et inversé en ajustant les réseaux de sortie, pour un fonctionnement de 2 à 3 GHz. Par l'application d'outils d'optimisation des circuits d'adaptation de sortie et de la pente de phase entre les amplificateurs, il est possible d'améliorer la bande passante de l'amplificateur Doherty. Les résultats montrent que la réponse en fréquence du DPA inversé est moins dispersive que dans le cas du DPA conventionnel. Nous proposons alors une méthode de conception d'amplificateurs Doherty , basée sur l'optimisation de différents paramètres de la structure. Enfin, une simulation de type équilibrage harmonique a été réalisée sur les circuits PA Doherty proposés pour une puissance crête d'environ 47 dBm. Les résultats de la simulation ont confirmé que les performances du DPA inversé, en termes de rendement en puissance ajoutée PAE et de gain de puissance à la fois à la puissance de sortie maximale et à 6 dB de recul, sont maintenues à fort niveau sur une plus grande bande passante que dans le cas du DPA conventionnel. La PAE de l'amplificateur Doherty inversé est comprise entre 52,5 % et 57 % à la puissance de sortie maximale, puis 50,8 % à 53,5 % avec un recul de 6 dB, dans la gamme de fréquence de 2 à 3 GHz.

Mots-clés: Amplificateur de puissance RF, structure Doherty, transistor GaN, réseau d'adaptation d'entrée et de sortie, méthodes d'optimisation, rendement, bande passante.