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Experimental and Simulation Study of GaN Device Size Limitations for High-Efficiency Power Converters

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« Crystals are like people: it is the defects in them which tend to make them interesting »

Sir Colin Humphreys

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Outline

Acknowledgments vi
Outline vi
Acronyms xiv
General Introduction 1
Context 1
Objectives and Thesis Organization 3
Chapter I AlGaN/GaN-on-Silicon Devices for Power Electronics, State-of-the-Art and Scaling Perspectives 6
I.1 Gallium Nitride: From the Raw Material to its Applications 8
I.1.a Gallium Nitride: A Wide Band Gap Material 8
I.1.a.i Wide Band Gap Semiconductors 8
I.1.a.ii The Crystalline Properties of Gallium Nitride 11
I.1.a.iii The Polarization Properties of Gallium Nitride 14
I.1.b Gallium Nitride: A Material Used to Make Power Devices 19
I.1.b.i Power Devices with GaN 19
I.1.b.ii The Specificity of Lateral AlGaN/GaN-on-Si Power Devices 26
I.1.c Gallium Nitride: From the Power Device Performances to its Applications 30
I.1.c.i Transistor Hard and Soft Switching 30
I.1.c.ii A Wide Range of Applications for GaN transistors 33
I.1.d Summary 36
I.2 Device Architecture to Improve the Breakdown Voltage and Method to Study the Electric Field 37
I.2.a Device Architecture Improvements for High Breakdown Voltage 37
I.2.a.i The Field Plates 37
I.2.a.ii The Low Conductive Layer 40
I.2.a.iii The Polarization Super Junction 41
I.2.a.iv The Epitaxial Layers Engineering 42
I.2.a.v The Substrate Removal 43
I.2.b Method to Probe the Electric Field 44

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I.3 State-of-the-Art of the Switching Loss Measurement Techniques 45
I.3.a Different Switching Loss Origins 45
I.3.b Different Setups for Loss Extraction.....46
I.3.b.i Double Pulse Test (DPT).....46
I.3.b.ii Calorimetric Measurement Test.....47
I.3.b.iii Opposition Test Method 48
I.3.b.iv Indirect Measurement Method.....48
I.3.b.v Analytical Model 49
I.3.b.vi Summary.....49
I.3.c Different Loss Extraction.....50
Conclusion.....52
Chapter II Experimental Study of the High Voltage Limitations of AlGaN/GaN-on-Si Schottky Barrier Diode 54
II.1 Breakdown Analysis in AlGaN/GaN Devices for Power Electronics 56
II.1.a Literature Review: AlGaN/GaN Power Devices Lateral Breakdown Analysis.....57
II.1.a.i AlGaN/GaN Schottky Diodes Lateral Breakdown Analysis 57
II.1.a.ii Complementary Techniques and Studies in Breakdown Analysis of AlGaN/GaN High Electron Mobility Transistors.....63
II.1.a.iii Summary.....67
II.1.b Literature Review: Vertical Breakdown Mechanisms 68
II.1.b.i Literature Hypothesis.....68
II.1.b.ii Main Identified Dependence.....71
II.2 The Identification of the Two Breakdown Modes by the Substrate Connection Dependence on the Breakdown Voltage 73
II.2.a Experimental Protocol.....73
II.2.a.i Samples Description 73
II.2.a.ii Electrical Characterization Procedure.....75
II.2.b Experimental Results.....75
II.2.b.i Diodes Leakage Trends and Contributions.....75
II.2.b.ii Breakdown Voltage Extraction in the Different Configurations as a Function of the Anode-to-Cathode Distance 77
II.3 Device Limitations with a Floating Substrate 81

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II.3.a Method Description and Experimental Presentation....81
II.3.a.i Method Description....81
II.3.a.ii Experimental Presentation....82
II.3.b Experimental Results....86
II.3.b.i Long Anode-to-Cathode Distance Devices....86
II.3.b.ii Short Anode-to-Cathode Distance Devices....89
II.3.b.iii Summary....94
II.4 Device Limitations with Grounded Substrate....96
II.4.a Method Description....96
II.4.b Experimental Results....97
II.4.b.i General Trends....97
II.4.b.ii Failure Analysis for Every Identified Categories....99
II.4.b.iii Summary....103
Conclusion....104
Chapter III Improving the AlGaN/GaN Schottky Diode TCAD Modeling Based on Experimental Measurements....105
III.1 State-of-the-Art Approach Limits and Proposed Method Description....108
III.1.a Limit of the Approach Present in the Literature to Simulate the Electric Field Distribution in AlGaN/GaN Lateral Power Devices....108
III.1.a.i Two-Dimensional Analytical Model....108
III.1.a.ii Technology Computer Aided Design (TCAD)....109
III.1.b Proposed Method to Probe the Different Contribution of Buffer Traps on the Device Characteristics....112
III.2 Modeling of the Capacitive 2DEG Depletion Control....117
III.2.a Buffer Layers Affecting the Capacitance Dependence at First Order....117
III.2.a.i Sample and Method Presentation....117
III.2.a.ii Impact of the Substrate Presence....120
III.2.a.iii Impact of the Piezoelectric Model Activation in the Buffer Layers....120
III.2.a.iv Impact of the Back Barrier Presence....123
III.2.a.v Discrepancy between the Electric field Distribution and the Experimental Breakdown Measurements....123
III.2.b Buffer Traps Impact on the Capacitive Temperature Dependence....125

Cette thèse est accessible à l'adresse : https://theses.insa-lyon.fr/publication/2023ISAL0021/these.pdf
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III.2.b.i Sample Presentation and Preliminary Study 125
III.2.b.ii Experimental Study 128
III.2.b.iii TCAD Qualitative Simulation Study of Buffer Traps 130
III.2.b.iv TCAD Fit on the Experimental Data and the Possible Interpretations 136
III.2.b.v V_{Ga}-$(O_N)_x$ Hypothesis Verification 138
III.2.c Implementation of Deep Acceptor Traps in the Simulated AlGaN/GaN Schottky Diode and Evaluation of the Electric Field Change 141
III.3 Buffer Charge Movement Modeling Through Vertical Current Temperature Dependence 145
III.3.a Current Status on the Vertical Current Knowledge and the Different Reported Transport Mechanisms 145
III.3.a.i Current Status on the Vertical Current Knowledge 145
III.3.a.ii Ohmic Conduction 147
III.3.a.iii Recombination Limited Transport 148
III.3.a.iv Space Charge Limited Current 149
III.3.a.v Hopping Versus Poole Frenkel Mechanisms 150
III.3.a.vi Summary of the Bulk Transport Mechanisms 152
III.3.b Experimental Analysis and Interpretation of the Vertical Current Temperature Dependence 153
III.3.b.i Preliminary Experimental Studies 153
III.3.b.ii Model Fitting 155
III.3.b.iii Fitting Parameter Interpretation 160
III.3.b.iv Summary 162
III.3.c TCAD Simulation and Modeling Study to Reproduce the Experimental Trend 163
III.3.c.i Simulated Structure Presentation 163
III.3.c.ii Simulation Results 165
III.3.c.iii Discussion 168
III.3.d Summary 169
III.4 Capacitance Deep Level Transient Fourier Spectroscopy (C-DLTFS) of Schottky AlGaN/GaN-on-Si Schottky Diode 170
III.4.a Samples and Characterization Setup Presentation 170
III.4.b Experimental Results 172

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III.4.b.i Arrhenius Plot 172
III.4.b.ii Filling Pulse Width Dependence 173
III.4.c Discussion on the Possible Trap Origins 175
Conclusion 179
Chapter IV Evaluation of AlGaN/GaN Fully-Recessed MOS-HEMT Hard Switching Losses 180
IV.1 State-of-the-Art of E-mode Transistor Switching Losses 182
IV.1.a Simulation Approach 182
IV.1.b Experimental Approach 184
IV.1.b.i Analytical Design Rules of Hard Switching Losses (versus Temperature, OFF-State Blocking Voltage or ON-State Current) 184
IV.1.b.ii Blocking Time Impact before Switching Event 186
IV.1.b.iii External Gate Resistance Impact 187
IV.1.b.iv On-state Gate Driving Voltage Impact 187
IV.1.b.v Comparison between Power Transistor Technologies 188
IV.1.c Mixed Approach 189
IV.1.d Summary 190
IV.2 Experimental and Simulation Study of Hard Switching Performance of E-mode Power Transistors 191
IV.2.a Methodology and Experimental/Simulation Tools Description 191
IV.2.a.i Sample Description 191
IV.2.a.ii Methodology Description 192
IV.2.a.iii Experimental Circuit Description 194
IV.2.a.iv LTSpice Simulation Presentation 196
IV.2.b Results 198
IV.2.b.i Impact of the Recess Depth on E-Mode 650 V/30 A MOS-HEMT Transistors' Hard-Switching Losses 198
IV.2.b.ii E-mode 650 V/1 A Transistor Switching Loss Analysis 205
Conclusion 208
General Conclusion 209
Summary, Results and Scientific Contributions 209
Limitations of the presented studies and perspectives 212

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Annexe A : Time Dependent Dielectric Breakdown: From the Physical Origin to the Electrical Analysis I
A.1 Physics of Time Dependent Dielectric Breakdowns I
A.2 Weibull Statistics to Study the Time Dependent Dielectric Breakdown II
Annexe B : Electrical and Physical Failure Analysis Techniques IV
B.1 Lock-in Thermography (LiT) [249], [445] IV
B.2 Focused Ion Beam Scanning Electron Microscopy (FIB-SEM) VII
Annexe C : Perimeter Versus Surface Contribution in the Vertical Leakage Temperature Dependence Through an AlGaN-on-Si Epitaxy IX
C.1 Normalisation Trials Varying Contact Diameters IX
C.2 Verification that the Perimeter Contribution in the Ohmic Regime Follows the Same Temperature Dependence than the Analytical Fit X
C.2.a Method Description XI
C.2.b Results XII
Annexe D : Mobility Model in the Bulk Material for the Study of the Vertical Current Through the Epitaxy XIII
D.1 Presentation of The Different Bulk Mobility Models XIII
D.1.a Lattice Temperature Dependent Model XIII
D.1.b Lattice Temperature and Ionized Doping Impurities Dependent Model XIV
D.1.c High-Electric Field Dependent Model XV
D.2 Model Choice and Parameters' Determination XVI
D.2.a Model Chosen for GaN bulk XVI
D.2.b Model for the Other Materials XX
Annexe E : Deep Level Transient Fourier Spectroscopy (DLTFS) XXI
E.1 Experimental Setup XXI
E.2 Different Electrical Measurements XXIII
E.2.a Temperature Scans/ Filling Pulse Scans XXIII
E.2.b Arrhenius Plot XXIV

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Annexe F : Double Source Test Complementary Information XXVII
F.1 Electrical Circuit XXVII
F.1.a Circuit Presentation and Elements XXVII
F.1.b Circuit Functioning and Typical Waveforms XXIX
F.1.c The Probes Choice Justification XXXI
F.2 Circuit modeling for LTSpice Simulations XXXIII
F.2.a Electrical Model XXXIII
F.2.a.1st Non-Ideal Inductance and Capacitors XXXIII
F.2.a.2nd Lossy Transmission Line XXXIV
F.2.b Model Fitting XXXVII
F.3 Probes' Propagation Time Compensation XL
F.3.a Current Probe XL
F.3.b Voltage Probes XLI
F.4 Technology Comparison with GaN Systems p-GaN gate XLI
Annexe G : Transistor LTSpice Model XLIV
G.1 Electrical Model XLIV
G.1.a Model Presentation XLIV
G.1.b Model Parameter Differences Between the Model Calibrated for Deep and Shallow Recess Transistors XLVIII
G.2 Thermal Model XLIX
G.2.a Model Presentation XLIX
G.2.b Negligible Self-Heating Effect During a Single Hard-Switching Event L
Résumé étendu (français) ..... A
Bibliography i
Author's Bibliography: ..... - 1 -

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Acronyms

2DEG *2-Dimensional Electron Gas*
2DHG *2-Dimensional Hole Gas*
3DHG *3-Dimensional Hole Gas*
AC *Alternating Current*
ADC *Analog to Digital Converter*
ALD *Atomic Layer Deposition*
ALE *Atomic Layer Etching*
AlN *Aluminium Nitride*
BB *Back Barrier*
BEOL *Back-End Of Line*
BJT *Bipolar Junction Transistor*
BV *Breakdown Voltage*
CCD *Charge Coupled Device*
CCM *Continous Current Mode*
CEA *Commissariat à l'Energie Atomique et aux énergies alternatives*
CL *CathodoLuminescence*
CMOS *Complementary Metal Oxide Semiconductor*
CTE *Coefficient of Thermal Expension*
CVS *Constant Voltage Stress*
DAB *Dual Active Bridge*
DC *Direct Current*
DFN *Dual Flat No Leads*
DH-HEMT *Double Heterojunction High Electron Mobility Transistor*
DLTFS *Deep Level Transient Fourier Spectroscopy*
DLTS *Deep Level Transient Spectroscopy*
DPT *Double Pulse Test*
DST *Double Source Test*
DUT *Device Under Test*
EL *ElectroLuminescance*
EMC *ElectroMagnetic Coupling*
EMMI *Emission Microscopy*
ESB *Energy Selective Backscattered*
ESD *ElectroStatic Discharge*
FEM *Finite Element Method*
FEOL *Front-End Of Line*
FIB *Focused Ion Beam*
FIB-SEM *Focused Ion Beam-Scanning Electron Microscopy*
FOM *Figure Of Merit*

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FP LMTO *Full Potential-Linear Muffin-Tin Orbital*
Ga *Gallium*
Ga_2O_3 *Gallium Oxide*
GaN *Gallium Nitride*
GaN:C *Carbon doped Gallium Nitride*
GET *Gate Edge Terminaison*
GIT *Gate Injection Transistor*
GR *Growth Rate*
HAADF *High-Angle Annular Dark Field*
HBT *Heterojunction Bipolar Transistor*
HD-GIT *Hybrid Drain-Gate Injection Transistor*
HERA DLTS *High Energy Resolution Analysis Deep Level Transient Spectroscopy*
HFET *Heterojunction Field Effect Transistors*
HVPE *Hybride Vapor Phase Epitaxy*
HVSMU *High-Voltage Source Measurement Unit*
IGBT *Isolated Gate Bipolar Transistor*
IMS *Insulator Metal Substrate*
INES *Institut National de l'Énergie Solaire*
InGaAs *Indium Gallium Arsenide*
InSb *Indium Antimonide*
LCL *Low Conductive Layer*
LEM *Light Emission Microscopy*
LETI *Laboratoire d'Electronique et de Technologie de l'Information*
LiDAR *Light Detection And Ranging*
LiT *Lock-in Thermography*
MBE *Molecular Beam Epitaxy*
MEA *More Electric Aircraft*
MFCMU *Multi-Frequency Capacitance Measurement Unit*
MIS *Metal Insulator Semiconductor*
MOS *Metal Oxide Semiconductor*
MOSFET *Metal Oxide Semiconductor Field Effect Transistor*
MOVPE *Metal Organic Vapor Phase Epitaxy*
N *Nitrogen*
NH_3 *Ammonia*
NNH *Nearest Neighbor Hopping*
OBC *On Board Charger*
PCB *Printed Circuit Board*
PEM *Photon Emission Microscopy*
PF *Poole Frenkel*
PFC *Power Factor Correction*
PL *PhotoLuminescence*
PLC *Power Line Cycle*

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PSJ *Polarization Super Junction*
PVD *Physical Vapor Deposition*
PWM *Pulse Width Modulation*
ReSurf *Reduced Surface electric field*
RF *Radio Frequency*
RMBE *Reactive Molecular Beam Epitaxy*
RR *Ramp Rate*
RTA *Rapid Thermal Annealing*
SBD *Schottky Barrier Diode*
SCLC *Space Charge Limited Current*
SEM *Scanning Electron Microscopy*
SiC *Silicon Carbide*
SIMS *Secondary Ion Mass Spectroscopy*
SiN *Silicon Nitride*
SiO_2 *Silicon Dioxide*
SJ *Super Junction*
SL *Super Lattice*
SMU *Source Measure Unit*
SOA *Safe Operation Area*
SRL *Strain Relief Layer*
SSPC *Steady-State PhotoCapacitance*
STEM *Scanning Transmission Electron Microscopy*
TCAD *Technology Computer Aided Design*
TDDB *Time Dependent Dielectric Breakdown*
TEM *Transmission Electron Microscopy*
TFEE *TransFerred Electron Effect*
TIM *Thermal Infrared Microscopy*
TMAl *TrimethylAluminium*
TMGa *TrimethylGallium*
UID *Unintentionally Doped GaN*
UID-GaN *Unintentionnally Doped Gallium Nitride*
VNA *Vectorial Network Analyzer*
VRH *Variable Range Hopping*
WBG *Wide Band Gap*
XPS *X-rays Photoelectron Spectrometry*
ZVS *Zero Voltage Switch*

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General Introduction

Context

Nowadays the astonishing rise of electrification in our society creates a huge demand for technologies related to power conversion systems (example: laptop or cell phone chargers, electric vehicle chargers, *etc*). This is bringing a lot of opportunities for research and development centers such as the Commissariat à l'Energie Atomique et aux énergies alternatives (CEA) and especially the Laboratoire d'Electronique et de Technologie de l'Information (LETI) as well as academic laboratories such as Ampère Laboratory to develop highly efficient electrical systems.

The mainstream silicon technology reveals its limits for certain applications especially in power electronics. Gallium Nitride (GaN) based Heterojunction Field Effect Transistors (HFET) have managed to enter the power semiconductor device market for several years now. Discrete devices are currently available in the 100-900 V and range and from few amperes to 100 A [1], [2]. Its revenue is more than 10M dollars for three years (the main players being: EPC™, Infineon™ (Panasonic™), Innoscience™, GaN Systems™, Navitas™, Power Integrations™, Transphorm™ and STMicroelectronics™) as shown in **Figure 1** with more than 10% quarter to quarter growth. The latest data report a 2021 revenue of 126M dollars [3].

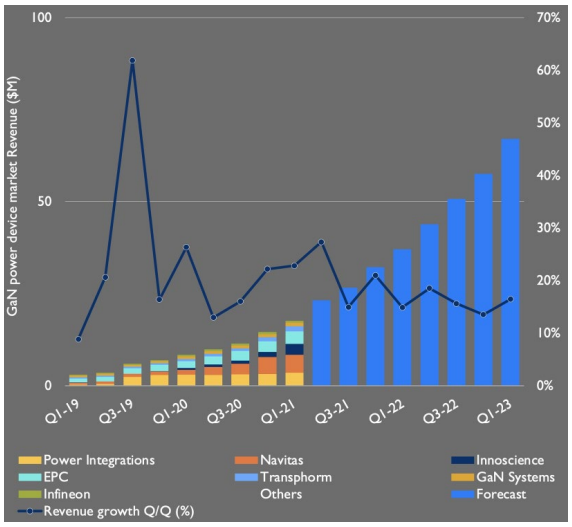

Figure 1: GaN power device revenue from 2019 to Q1-2021 and its forecast for the end of 2021, 2022 and the beginning of 2023 [4].

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Nevertheless, these GaN-based power switches have not reached their theoretical maximum performance in conduction and during switching. The device length scaling may help in reaching these limits according to Johan T. Strydom in the book of Meneghesso *et al.* [5, pp. 145–148] as illustrated in **Figure 2**, for the following reasons:

- The static on-state resistance[1] ($R_{DS,ON}$ in **Figure 2**) is decreased. This is interesting to lower the conduction losses. In addition, the specific on-state resistance ($R_{ON} = R_{DS,ON} \times A$ in **Figure 2**) is expected to be even more reduced with the downsized wafer area required to build the transistor,

- The transistor-related charges (Q_{XX} in **Figure 2**) are decreased (divided by three when the length is divided by three in **Figure 2**). This would lower the switching time (switching speed increased) and therefore the switching losses.

Both allow improving the efficiency of the power converter (ex: chargers) in which they are used. Nevertheless, this approach is limited by:

- The possible reduction of the breakdown voltage in blocking mode with the expected increase of the lateral electric field at a given bias (multiplied by three "3× V/µm" when the length is divided by three in **Figure 2**),

- The switching speed increase because the parasitic elements perturbation on the switching waveform will be enhanced. This may alter the switching stability.

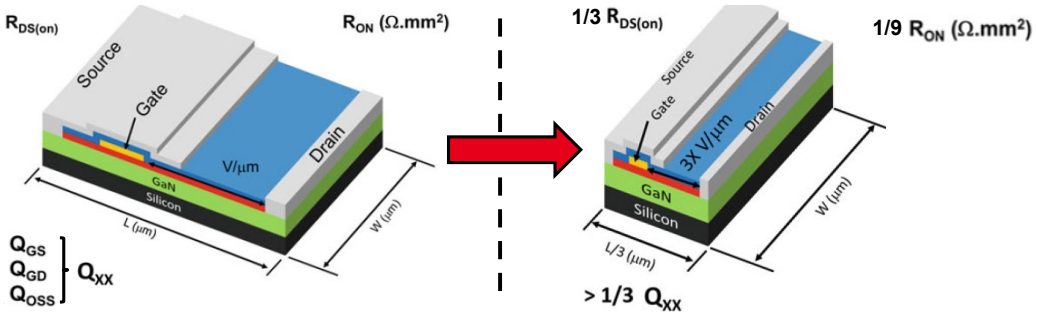

Figure 2: Effect overview of the GaN transistor length scaling down on its relevant electrical properties (adapted from [5, p. 146]).

[1] This is different from the dynamic on-state resistance (non-permanent on-state resistance increase after having been stressed in the off-state [6]. Nowadays, some manufacturers report "current-collapse-free" devices [7]. However, to be accurate, it concerns applications in the 100 kHz range because systems were limited to an accurate acquisition after some microseconds [8]. For applications above the MHz range, multiple pulse fast acquisition system was shown to be required for the characterization of GaN technology enabling the observaion of the potential limits of these "current-collapse free" devices with respect to more conventional GaN devices for soft-switching applications [9].

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Objectives and Thesis Organization

To surpass the possible scaling limitations presented before, the purpose of this PhD is to provide a better understanding:

- On the **device electric field distribution in blocking mode**,
- On the **transistor hard switching losses**.

With these targets in mind, Chapter 1 is first intended to provide basic knowledge on the AlGaN/GaN lateral power devices from the material properties to its applications. On the one hand, it highlights the interesting material properties that initiated the research and development on this material: the GaN high critical electric field (for high voltage applications) as well as its piezoelectric properties (responsible for the formation of a high electron mobility two-dimensional electron gas used for the low on-state resistance). And on the other hand, the technology developed at CEA LETI will be introduced emphasizing the current technological challenges (normally-off operation, low leakage level, *etc*) as well as a comparison of this technology with respect to the different existing ones in GaN but also with respect to more mature technologies (silicon and silicon carbide). After that, a focus on the electric field management will be performed with on the one side the engineering elements allowing to improve the breakdown voltage and on the other side the different methods proposed to probe and study it. A dedicated focus on the switching loss measurement techniques will be presented with a proper definition of the different types of losses and the measurement and extraction methods of the state-of-the-art.

As for the rest of this manuscript, it follows different problematics stated below:

⁂ What is currently limiting the device breakdown voltage?

Chapter 2 is intended to address this question on the 650 V/6 A AlGaN/GaN-on-Si Schottky barrier diode manufactured at CEA LETI. To do so, the breakdown mechanisms as well as the techniques to identify them reported in the AlGaN/GaN power device literature will be presented. This part will be followed by the general identification of the different breakdown mechanisms in the studied devices will be introduced especially by connecting the substrate to the anode or not. Then the breakdown location will be investigated in both breakdown modes (vertical and lateral). This will be realized by analyzing the dependency of the breakdown voltage with respect to

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temperature, layout and epitaxy and also by means of a failure and physical analysis (Lock-in thermography and Focused ion beam scanning electron microscopy). This study will be used as a reference for the electric field simulation study proposed in the Chapter 3 in addition to proposing possible layout and epitaxial optimization for the breakdown voltage.

- Is the Technology Computer-Aided Design (TCAD) modeling proposed in the literature sufficient enough to reproduce the current experimental breakdown voltage? What are the missing elements? Which electrical characterizations would allow their calibration?

Chapter 3 is intended to develop the TCAD modeling of AlGaN/GaN-on-Si Schottky barrier diodes fabricated at CEA LETI to be able to get a representative image of the experimental electric field. To do so, limits of the state-of-the-art approach will be reported before describing the methodology adopted in this thesis to deal with the modeling of buffer traps. Based on capacitance-temperature measurements and TCAD analysis, deep acceptor traps present in the buffer layers are identified based on their electrical properties. After that, a study performed on the experimental vertical current temperature dependence will be presented, highlighting the impact of some donor traps on the vertical conduction which plays a role in the electric field distribution. Finally, Deep Level Transient Fourier Spectroscopy (DLTFS) allowing to probe traps near the anode will be presented before summarizing the different obtained results.

- What are the impacts of the transistor layout and process parameter that may be changed due to the scaling down on the switching losses?

Chapter 4 is dedicated to the study of the 650 V rated AlGaN/GaN-on-Si power transistors switching losses. In this chapter, the layout (gate, gate to drain and field plates length) and process parameters (gate recess depth) dependencies will be studied. Indeed, these parameters may be changed in the device length scaling down. This can provide scaling guidelines to optimize the switching losses. Coupled with well-calibrated TCAD simulation deck allowing to reproduce static on and off experimental measurements (as developed in Chapter 3), it would ease the device design. Thus a state-of-the-art of the switching loss-oriented studies performed in the literature will be presented to situate the following studies. Switching losses of 650 V/30 A transistors with two

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different gate recess depths will be compared and analyzed to understand the origin of the switching loss differences thanks to LTSpice simulations mainly and TCAD simulations. Finally, the layout limitation of the scaled 650 V/1 A transistors will be enhanced as well as some observations on the hard switching performance.

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Chapter I
AlGaN/GaN-on-Silicon Devices for Power Electronics, State-of-the-Art and Scaling Perspectives

This chapter explains the technical reasons for the astonishing growth of GaN power devices on the market. The current limitations in terms of electric field management will be emphasized with the different proposed solutions to tackle the problem. After that, key knowledge will be given to understand switching losses.

Outline

Chapter I AlGaN/GaN-on-Silicon Devices for Power Electronics, State-of-the-Art and Scaling Perspectives 6

I.1 Gallium Nitride: From the Raw Material to its Applications 8

I.1.a Gallium Nitride: A Wide Band Gap Material 8

I.1.a.i Wide Band Gap Semiconductors 8

I.1.a.ii The Crystalline Properties of Gallium Nitride 11

I.1.a.iii The Polarization Properties of Gallium Nitride 14

I.1.b Gallium Nitride: A Material Used to Make Power Devices 19

I.1.b.i Power Devices with GaN 19

I.1.b.ii The Specificity of Lateral AlGaN/GaN-on-Si Power Devices 26

I.1.c Gallium Nitride: From the Power Device Performances to its Applications 30

I.1.c.i Transistor Hard and Soft Switching 30

I.1.c.ii A Wide Range of Applications for GaN transistors 33

I.1.d Summary 36

I.2 Device Architecture to Improve the Breakdown Voltage and Method to Study the Electric Field 37

I.2.a Device Architecture Improvements for High Breakdown Voltage 37

I.2.a.i The Field Plates 37

I.2.a.ii The Low Conductive Layer 40

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I.2.a.iii The Polarization Super Junction 41
I.2.a.iv The Epitaxial Layers Engineering 42
I.2.a.v The Substrate Removal 43
I.2.b Method to Probe the Electric Field 44
I.3 State-of-the-Art of the Switching Loss Measurement Techniques 45
I.3.a Different Switching Loss Origins 45
I.3.b Different Setups for Loss Extraction 46
I.3.b.i Double Pulse Test (DPT) 46
I.3.b.ii Calorimetric Measurement Test 47
I.3.b.iii Opposition Test Method 48
I.3.b.iv Indirect Measurement Method 48
I.3.b.v Analytical Model 49
I.3.b.vi Summary 49
I.3.c Different Loss Extraction 50
Conclusion 52

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I.1 Gallium Nitride: From the Raw Material to its Applications

In this subsection, a description of GaN-based technology is presented from the raw material properties to its final applications in power converters passing by device properties.

I.1.a Gallium Nitride: A Wide Band Gap Material

In the first part, Gallium Nitride material properties will be presented. Its belonging to the wide band gap semiconductor category (material prone to extend the limits of silicon power electronics devices) will be firstly introduced. Secondly, its specific crystalline structure, the doping impurities and the crystal imperfections of the material used for power devices will be detailed. Thirdly, its piezoelectric properties allowing to obtain a 2-Dimensional Electron Gas (2DEG) will be presented as well as its interesting electronic transport properties.

I.1.a.i Wide Band Gap Semiconductors

Wide Band Gap (WBG) semiconductors are considered to have properties that are very interesting for power electronics. They are characterized by their larger band gap with respect to the silicon (Silicon Carbide (4H-SiC): 3.23 eV [10]; Gallium Nitride (2H-GaN): 3.4 eV [10]; Gallium Oxide (Ga_2O_3): 4.8-4.9 eV [11]; Aluminum Nitride (AlN): 6.2 eV [10]; Diamond: 5.46-5.6 eV [12]). Their properties are compared with respect to the Silicon for three different categories of applications as represented in the radar chart of **Figure 3**:

- High-voltage properties:
  - Band gap E_G: energy difference between the minimum of the conduction band and the maximum of the valence band in the Brillouin zone. It is important for high voltage applications because the critical electric field is related to this quantity as exposed in **Equation 1**. For power electronics, this is also interesting because the higher the band gap the higher the energy enabling the thermal generation of carriers. The latter lead to unwanted leakage at high temperature, therefore WBG semiconductors exhibit lower leakage at high temperature. Finally, having a high band gap make the semiconductor less sensitive to irradiation for a certain energy range. This is useful in harsh environments (nuclear power plants, spatial). The 3.4 eV (at room temperature since it slightly decreases with temperature according to the relation given in the book of

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Levinshtein *et al.* [10]) of GaN is superior to the value of SiC or Si as shown in **Figure 3** which makes it suitable for high-voltage applications.

$$E_C \propto {E_G}^{\gamma}$$

Equation 1: Critical electric field relation with the band gap [13], [14] (E_C: critical electric field; E_G: band gap; γ: power coefficient (state-of-the-art value: 1.83 [13])).

- Critical electric field E_C: It is the maximum electric field the material can withstand without irreversible damage. As expected, in accordance with **Equation 1**, GaN has a higher critical electric field (3.3 MV/cm in **Figure 3**) with respect to Si and SiC.

- High-temperature properties:

  - Thermal conductivity k: It represents the ability of a material to conduct heat. It is especially interesting to limit self-heating thus preventing performance limitations and reliability issues in high-power-density and high-temperature applications. In **Figure 3**, it can be seen that this is not the main asset of GaN but rather that of SiC.

  - Melting point T_C: Temperature above which the material melts. Again, the parameter is higher for SiC, which makes this material very interesting for high-temperature applications.

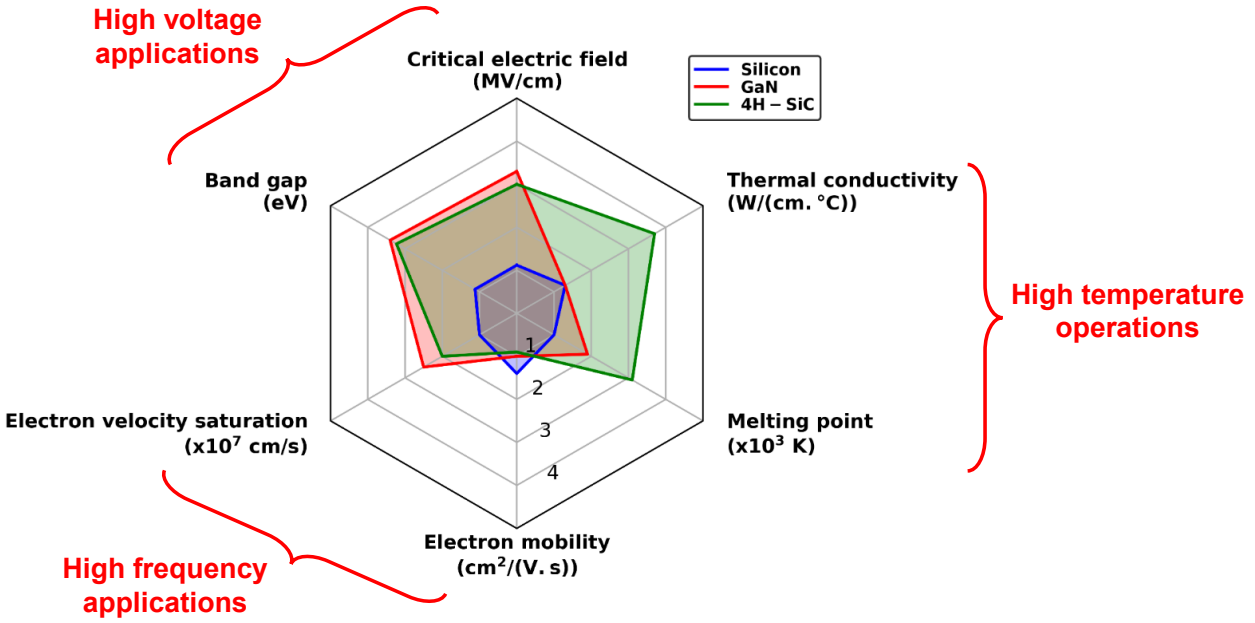

Figure 3: Bulk material properties at 300 K (room temperature): the most common wide band gap semiconductors (SiC, GaN) compared to the widely used silicon (based on [10]).

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- High-frequency properties:

  - Electron mobility μ_n: It is the ability for the electron to move inside the crystal under a certain electric field. It can be drastically reduced by either crystalline defects, temperature (phonon-electron interactions), the presence of other carriers or impurities. In **Figure 3**, it can be seen that this is not the main asset of either GaN or SiC since their mobility reaches 1000 $cm^2/(V.s)$ whereas the silicon one approaches 1500 $cm^2/(V.s)$. Nevertheless, as it will be described later on, lateral GaN devices benefit from the high mobility (close to 2000 $cm^2/(V.s)$ [15]) of a 2-Dimensional Electron Gas (2DEG).

  - Electron velocity saturation v_{sat}: It is the maximum electron speed reached under high electric field. According to **Equation 2** exposed in the paper of Marino *et al.* [16], having a large saturation velocity induces a large device cut-off frequency. This simple approach has to be nuanced with more recent formula in the paper of Kwak *et al.* [17] (**Equation 3**) in which the contribution of access resistance and parasitic capacitance limits the cut-off frequency. This formula is closer to the real device than one based on material properties.

$$f_T = \frac{v_{sat}}{2 \times \pi \times L_G}$$

Equation 2: Cut-off frequency in the paper of Marino *et al.* (f_T: cut-off frequency ; v_{sat}: velocity saturation; L_G: gate length) [16].

$$f_T = \frac{g_m}{2 \times \pi \times (C_{GS} + C_{GD})}$$

Equation 3: Cut-off frequency in the paper of Kwak *et al.* (f_T: cut-off frequency ; g_m: transconductance; C_{GS}: gate-to-source capacitance; C_{GD}: gate-to-drain capacitance) [17].

The material properties comparison is useful to target the possible application range of these wide band gap semiconductors. This is especially done using Figure Of Merit (FOM) proposed by Baliga *et al.* [18] (indication for low-frequency power switching applications) and Johnson *et al.* [19] (indication for high-power applications at high frequency) as summarized in the paper of Islam *et al.* [20]. However, it is still limited to material. More elements are required to verify if the material can be effectively used for power devices such as the capability of making low resistive ohmic contacts, the capability of growing or depositing a dielectric layer with a good interface quality and the capability to modulate the conductivity of the material with doping impurities. Moreover, its commercialization depends also on the overall cost (raw material cost and fabrication cost which include the wafer size) of the device as well as the device performances which may differ with the type of device: vertical or lateral.

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I.1.a.ii The Crystalline Properties of Gallium Nitride

GaN is a III-V semiconductor. This means that it is made of atoms from the third column in Mendeleev's Periodic Table: Gallium (Ga) and atoms from the fifth columns: Nitrogen (N). It was for the first time epitaxially grown on a sapphire substrate in 1969 by Maruska *et al.* [21] using Hybride Vapor Phase Epitaxy (HVPE). The grown crystal had a hexagonal (Wurtzite) lattice as in GaN devices nowadays and as illustrated in **Figure 4**. However, it must be mentioned that another crystalline structure exists: cubic (Zinc Blend) structure. It is thermodynamically metastable whereas the wurtzite structure is mechanically and thermally more stable [22] and it does not exhibit spontaneous piezoelectric properties mandatory for the 2DEG formation (I.1.a.iii).

† **The GaN Wurtzite (2H) lattice**

As shown in **Figure 4**, this crystalline structure is obtained by the interception of two hexagonal close-packed sub-lattices of Gallium and Nitrogen respectively having the same vertical axis (c-axis). This vertical axis is also the growth axis of lateral power devices to get the piezoelectric effect required to form the 2DEG. Moreover, two growth directions can be distinguished: N-faced growth directed by the $[000\bar{1}]$ crystal vector as illustrated in **Figure 4(a)** for which the growth direction is the same as that of the spontaneous polarization vector and Ga-faced growth directed by the [0001] crystal for which the growth direction is opposite as that of the spontaneous polarization vector. Commercialized lateral power AlGaN/GaN devices and the devices studied in this manuscript use Ga-faced growth. The crystal parameters (a = 3.189 Å & c = 5.185 Å) were found using X-ray analysis by the Debye-Scherrer technique [21].

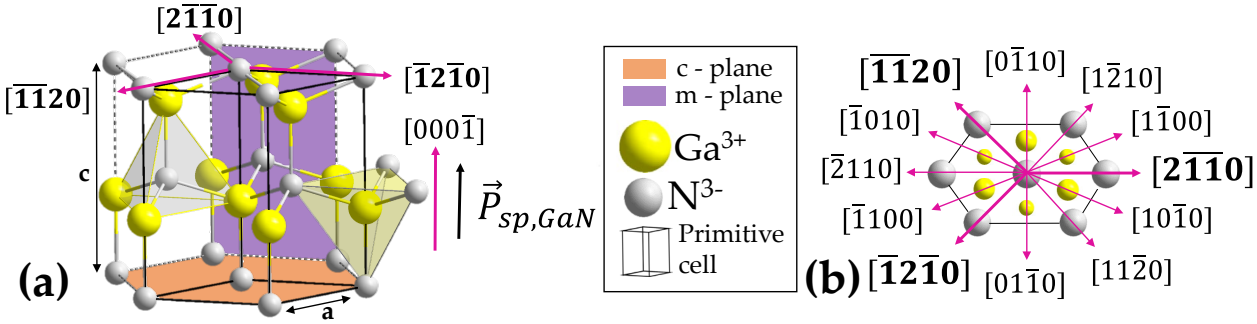

Figure 4: (a) N-face GaN wurtzite crystalline structure with well-known crystal planes (b) Crystal vectors [hklm] with l=-(h+k) in the c-plane (taken and adapted from [23], [24]).

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† **The GaN Crystalline Imperfections:**

They are usually classified with respect to their spatial dimension as shown in **TABLE 1**.

TABLE 1: Defect classification as a function of their spatial extension (more details in [25]).

Defect type	Point defect (0D)	Line defect (1D)	Surface defect (2D)	Volume defect (3D)
Example	Substitional defect, Interstitial defect, Vacancy, Frenkel defect, Schottky defect	Screw dislocations, Edge dislocations	Surface recombination, grain boundaries,	Void, cluster

A crystal imperfection or defect can be modeled as a trap in semiconductor physics with a specific energy level. Depending on its energy distance with respect to the band (conduction or valence band) they are either called shallow or deep traps. The most common shallow traps are doping impurities. The latter will be described with other well-known traps for the GaN in the following list:

- Doping impurities: They are atoms intentionally introduced in the crystalline structure to modify the semiconductor electrical properties (conductivity, carrier mobility etc.). They are usually on the substitutional sites meaning that they are either on the N-site or on the Ga-site. GaN can be n-doped with silicon (Si_{Ga}) or with oxygen (O_N) [26] or germanium Ge_{Ga} [27] and p-type with magnesium (Mg_{Ga}) [28]. P-type doping is limited in GaN because on the one hand, magnesium can be "passivated" with the creation of neutral complexes such as with hydrogen [29] or oxygen ($Mg_{Ga}O_N$) [30]. This is especially the case when p-type layers are formed at the beginning of the process and therefore when a post-deposition anneal cannot be performed as suggested by Amano *et al.* [28] to break those complexes. It can be on the other hand compensated by the creation of nitrogen vacancies which act as donor traps [27].

- Native defects: Gallium vacancies V_{Ga} (missing gallium atoms in the crystal) or nitrogen vacancies V_N are common point defects in GaN [27]. Their concentration depends on the electronic environment during growth and therefore on the position of the Fermi level in the

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band gap as shown in the calculations of Lyons *et al.* [27] (based on the method proposed by Freysoldt *et al.* [31]). Based on these calculations, a gallium vacancy is more stable in the n-type condition and a nitrogen vacancy in the p-type condition [27] (experimentally confirmed by the absence gallium vacancy in GaN:Mg samples using Positron Annihilation Spectroscopy (PAS) [32]). Nevertheless, gallium vacancies are more likely to be found within a complex, tied to oxygen atom(s) as shown with the calculations of Neugebauer *et al.* [33] in **Figure 5(a)** based on density-functional theory, *ab initio* pseudopotentials, and a supercell approach. These complexes were shown to behave as acceptor traps as shown by Elsner *et al.* [34] thanks to *ab initio* local-density-functional cluster method AIMPRO, and a self-consistent charge density-functional-based tight binding method SCC-DFTB. In this PhD manuscript, this complex will be related to the device capacitance characteristic (III.2.b.v).

- Dislocations (screw, edge or mixed): there are defect lines due to crystal irregularities formed during growth or due to strain. These kinds of defects are present in structures in which the different layers exhibit different lattice parameters which is especially the case in heteroepitaxy (illustration for the GaN epitaxy grown on a silicon substrate in **Figure 5(b)**). These defects may participate in the device electrical behavior, introducing leakage in the device as shown in III.3.b.iii.

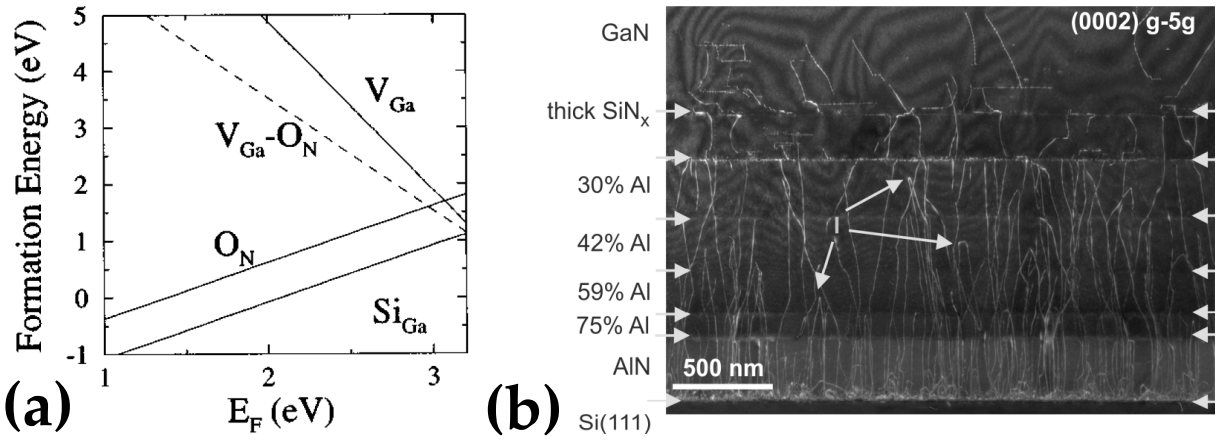

Figure 5: (a) Defect formation energy as a function of the Fermi level position [33] (based on density-functional theory, *ab initio* pseudopotentials, and a supercell approach) (b) Weak-Beam Dark Field Transmission Electron Microscopy (TEM) of a GaN-on-Si epitaxy with some screw dislocations loops (« l » in the figure) to reduce their expansion to the surface thanks to specific buffer layers [35].

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- Impurities: Many impurities can be found in the GaN layers/interfaces (carbon (C), iron (Fe), oxygen (O), hydrogen (H)) [27]. Some of them are inherent to the growth technic such as carbon and hydrogen provided by gas precursors during Metal Organic Vapor Phase Epitaxy (MOVPE): Trimethylaluminium and Trimethylgallium. Some others are intentionally inserted in the crystal for their insulating properties thanks to an additional gas source: carbon [36] or iron [37]. In lateral power devices, carbon is widely used:

  - It has an amphoteric behavior. This means that depending on its position in the crystal, it can be either a deep acceptor trap when it is in the N-site C_N or a donor trap in interstitial site C_i or in the Ga-site C_{Ga} [27]. Deep acceptor traps were reported by theoretical calculations to be in the 0.8-0.9 eV range from the valence band (Vienna Ab initio Simulation Package (VASP) using the projector augmented-wave method and performing Heyd-Scuseria-Ernzerhof hybrid functional calculations [38]–[40])

  - It can be intentionally introduced thanks to an ethylene (C_2H_4) or acetylene (C_2H_2) source during MOVPE growth [41].

However, it must be mentioned that all the mechanisms having an energy level in the 0.8-0.9 eV are not always related to carbon as shown in the discussion of III.2.b.iv.

I.1.a.iii The Polarization Properties of Gallium Nitride

- **Spontaneous Polarization:**

Wurtzite GaN has a spontaneous polarization for two reasons:

- As gallium and nitrogen atoms have different electronegativities (gallium being electropositive and nitrogen electronegative), the crystal holds thanks to ionic bonds where nitrogen attracts the shared electrons. This is why, Crystal structure in **Figure 4** and **Figure 6** are represented with Ga^{3+} and N^{3-} and not with Ga and N.

- The wurtzite structure is asymmetric. Consequently, the negative electric charge barycenter and the positive electric charge barycenter in the primitive cell do not overlap thus creating an electric dipole as shown in **Figure 6(a)**. Therefore by taking a step back, the crystal lattice can be represented as a stack of charged sheets and can be simplified for a given layer by a charged sheet at the top and at the bottom of the layer as shown in **Figure 6(b)**. This leads to the formation of a polarization field named $\overrightarrow{P_{SP}}$. Then as the Zinc Blend structure of GaN is cubic (symmetric structure), it does not exhibit a spontaneous polarization.

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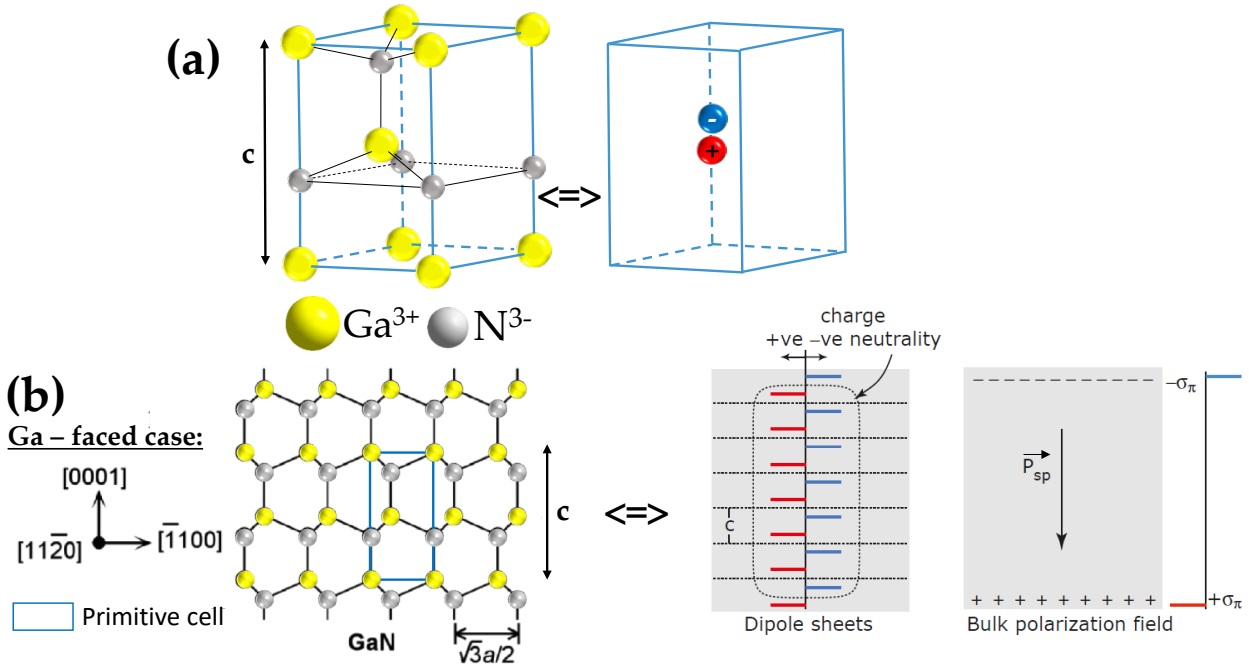

Figure 6: (a) Ga-faced primitive cell and its equivalent in terms of electric charge barycenters (b) Ga-faced GaN crystal structure cross-section and its dipole sheet representation from a microscopic point of view in the center and a wider point of view on the right (taken and adapted from [42]).

The same property is also observed for an AlN layer and therefore, for the generic ternary alloy $Al_xGa_{1-x}N$ following the expression:

$$\left\|\overrightarrow{P_{SP\,Al_xGa_{1-x}N}}\right\|(x) = -0.090 \times x - 0.034 \times (1-x) + 0.021 \times x \times (1-x)\ C/m^2$$

Equation 4: Spontaneous polarization of the $Al_xGa_{1-x}N$ compound [43].

† **Piezoelectric Polarization:**

In addition to spontaneous polarization, GaN exhibits piezoelectric polarization. This means that when GaN is strained, the primitive cell (showed on the left-hand side of **Figure 6(a)**) is either lengthened or shrink in the c-direction modifying the distance between the charge barycenters (showed on the right-hand side of **Figure 6(a)**), thus modifying the electric field dipole. This is taken into account with another polarization field $\overrightarrow{P_{PE}}$. This is especially the case for the AlGaN/GaN heterojunction as illustrated in **Figure 7**. Indeed by using **Equation 5**, it can be deduced that the AlGaN lattice parameter is smaller than the GaN one (represented by the black dots in **Figure 7**). Therefore, when depositing, the AlGaN layer, the latter is strained (tensile strain) as well as the GaN layer (compressive strain) as shown on the left. Whereas, if the AlGaN layer is

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relatively small with respect to the GaN layer (which is the case for AlGaN/GaN power devices), the latter can be assumed pseudomorphic (without strain) and the AlGaN withstands the overall strain as shown on the right. The resulting piezoelectric field in the latter configuration can be calculated using **Equation 6**, which depends on the lattice mismatch, the piezoelectric coefficient and the stiffness properties of the material.

$$a_{Al_xGa_{1-x}N}(\mathrm{x}) = -0.077 \times \mathrm{x} + 3.189\ \text{Å}$$

Equation 5: Lattice parameter of the $Al_xGa_{1-x}N$ compound [44].

$$\left\|\overrightarrow{P_{PE\,Al_xGa_{1-x}N}}\right\|(\mathrm{x}) = 2 \times d_{31} \times \left(\frac{a(x)-a(0)}{a(0)}\right) \times \left(C_{11}(\mathrm{x}) + C_{12}(\mathrm{x}) - 2 \times \frac{C_{13}(\mathrm{x})^2}{C_{33}(\mathrm{x})}\right) \mathrm{C/m^2}$$

Equation 6: Piezoelectric polarization of the $Al_xGa_{1-x}N$ compound deposited on a GaN layer (d_{31}: piezoelectric coefficient [$C.m^{-2}.Pa$]; C_{11}, C_{12}, C_{13}, C_{33}: stiffness constants [Pa]) [43].

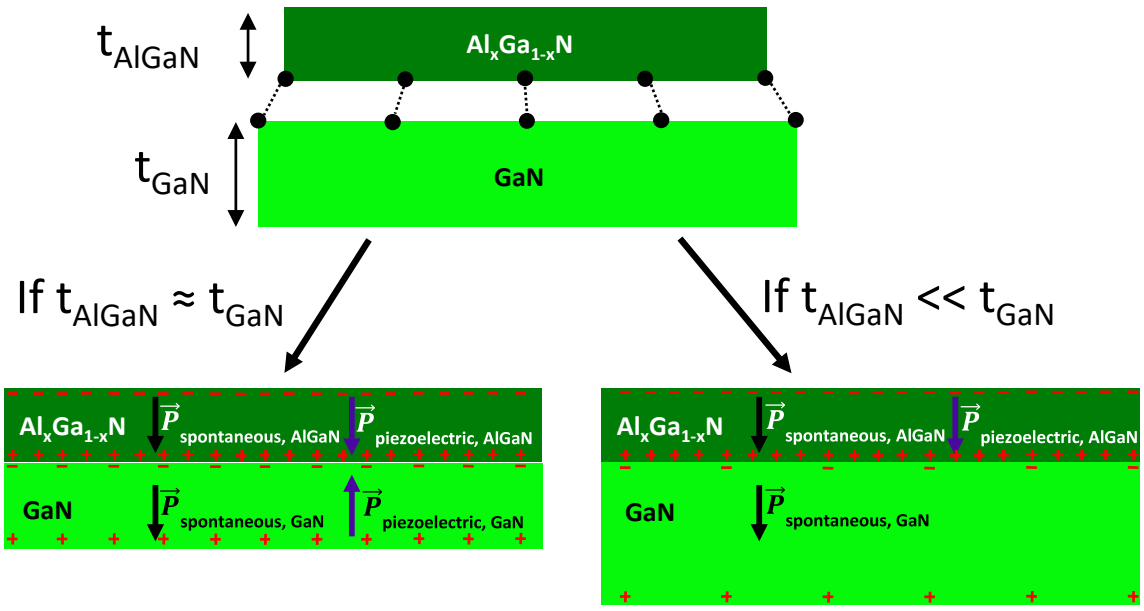

Figure 7: AlGaN/GaN heterostructure sheet charge formation and the resulting polarization field using Maxwell's law: $\sigma = \vec{\nabla}.\vec{P}$ (positive direction represented in the figure).

The 2DEG originates from the charge compensation of the piezoelectric charge at the interface of the heterostructure according to Ambacher *et al.* [45]. To keep the charge in the whole system null, ionized donor traps $\sigma_{interface}$ present at the passivation/$Al_xGa_{1-x}N$ interface

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compensate the electron charge density n_S as proposed by Ibbetson *et al.* [46] assumed at 1.65 eV from the conduction band (illustrated on the charge diagram in **Figure 8**). The study of Bare Surface Barrier Height led by Koley *et al.* [47] proposes that the energy distribution of these donor traps can be limited to a single energy level. An X-Ray Photoelectron Spectrometry (XPS) study proposed in 2003 that these donor traps could be nitrogen vacancies [48]. Further studies proposed that the Fermi level is pinned [49], [50]. It is pinned either at the interface at roughly 1.6 eV from the conduction band thanks to the presence of V_{Ga}/V_{Al}-O_N acting as acceptor traps and oxygen acting as donor traps according to Jang *et al.* [50] or it is pinned by donor traps in the passivation according to Bakeroot *et al.* [49].

Using either Poisson (quantization effects not included) or Schrödinger-Poisson (including quantization effects) equations, the band diagram illustrated in **Figure 8** can be obtained. The triangular quantum well highlighted in the figure leads to one-dimensional confinement of the electrons: their energy is quantized in this direction (x direction in **Figure 8**) and they can be considered as free carriers in the other two directions.

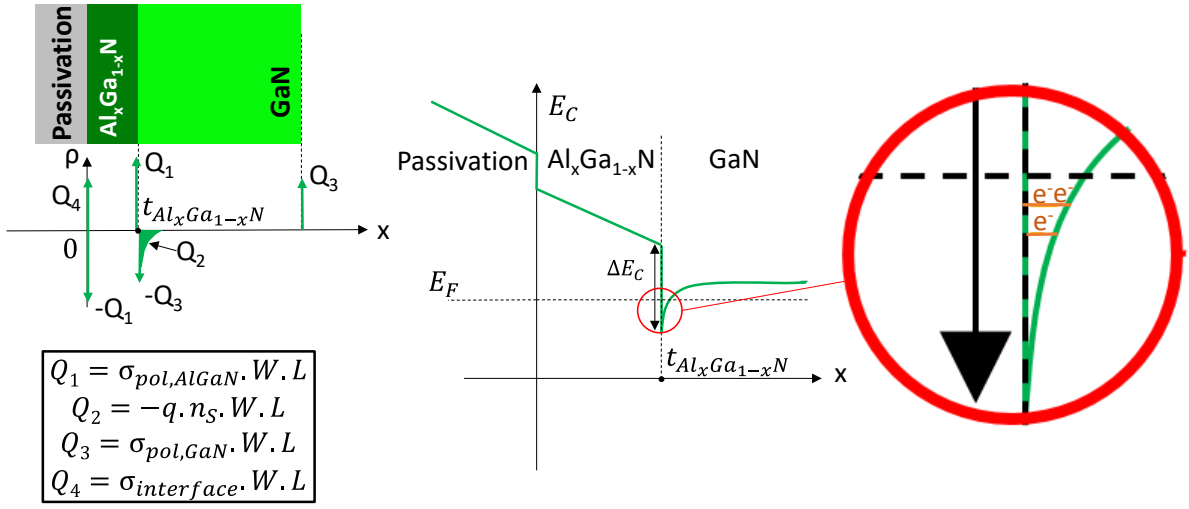

Figure 8: Charge and band diagram of a Passivation/AlGaN/GaN stack.

In 1991 (published in 1992), Asif Khan *et al.* [51] observed for the first time a 2DEG in an AlGaN/GaN structure by making mobility measurements versus temperature on the structure.

As the GaN layer is always an Unintentionally Doped Gallium Nitride (UID-GaN) layer, there is a weak interaction between electrons and ionized doping impurities with respect to a Metal

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Oxide Semiconductor (MOS) channel (for which an inversion channel occurs in a region in which doping impurities are ionized) leading to a high mobility reaching 2300 $cm^2/(V.s)$ at room temperature [52]. Note that the electron scatterings with the non-ionized impurities are negligible (background doping $\approx 10^{16}$ cm^{-3}) [42, p. 180]. The presence of ionized impurities in the bulk conduction path explains also the mobility difference ($\mu_{bulk} = 1000$ $cm^2/(V.s)$ versus $\mu_{2DEG} \approx 2000$ $cm^2/(V.s)$) with the 2DEG in which electrons are confined at the interface at room temperature [53].

Moreover, introducing a thin AlN barrier layer (≈ 1 nm) in between the $Al_xGa_{1-x}N$ and the GaN layers limits the penetration of electronic wave functions of the 2DEG electrons as shown in **Figure 9(a)** [42, p. 195]. This removes the alloy scattering. As an example, the mobility was increased from 1287 $cm^2/(V.s)$ to 1770 $cm^2/(V.s)$ at room temperature in the experimental study of Miyoshi *et al.* [54].

The 2DEG electron density depends on the barrier layer: AlN, AlGaN composition (aluminum mole fraction and thickness) [55], [56] as shown in **Figure 9(b)**. An electron density within the range of 0.1 to 2×10^{13} cm^{-2} can be obtained which roughly gives a sheet resistance of several hundred Ω/□.

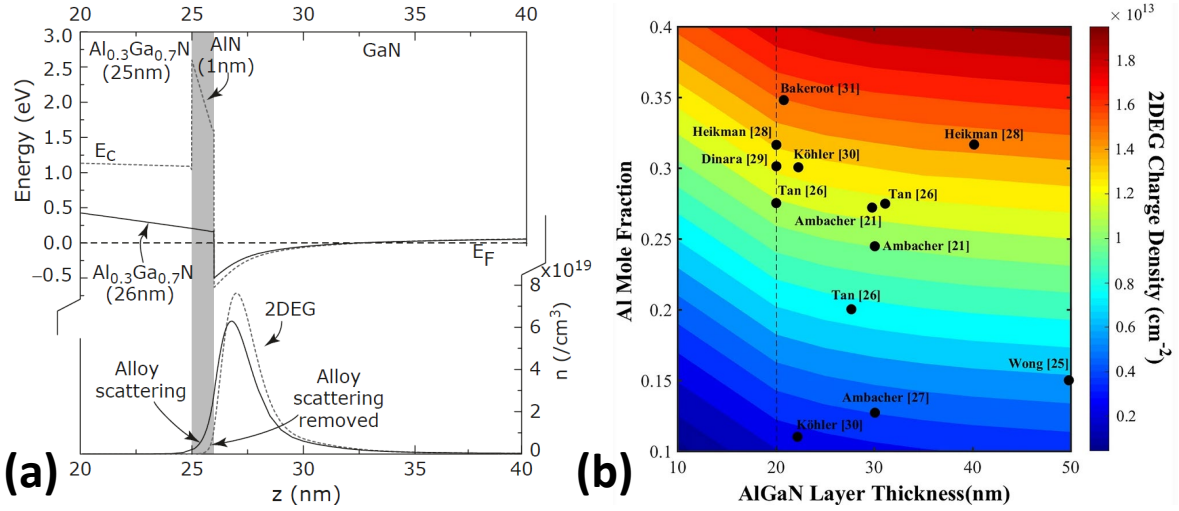

Figure 9: (a) Band diagram and electron density for an $Al_{0.3}Ga_{0.7}N$ (26 nm)/GaN and an $Al_{0.3}Ga_{0.7}N$ (25 nm)/AlN (1 nm)/GaN charge and band diagram of a Passivation/AlGaN/GaN stack (b) Contour plot of 2DEG charge density for GaN HEMT from the literature as a function of AlGaN barrier layer thickness and its Aluminum mole fraction [56].

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I.1.b Gallium Nitride: A Material Used to Make Power Devices

I.1.b.i Power Devices with GaN

In power electronics, power semiconductor devices are mainly used in power modules and especially in static[2] power converters. Among the different components found in static power converters, two semiconductor devices will be dealt with in the manuscript: Schottky diodes and Metal Insulator Semiconductor (MIS) transistors.

I.1.b.i.1st The lateral AlGaN/GaN Schottky Diode

A Schottky diode is a two-terminal (anode and cathode) power device with two distinct regimes. In on-state or forward regime ($V > 0$ V, or in the non-ideal case above the forward voltage V_F), current can flow and is limited by the series resistance of the non-ideal device as shown in **Figure 10(a)**. In off-state ($V < 0$ V) or reverse regime, the electron flow is blocked (to be accurate, the non-ideal device exhibits some leakage in that regime). It is therefore unidirectional in current and in voltage.

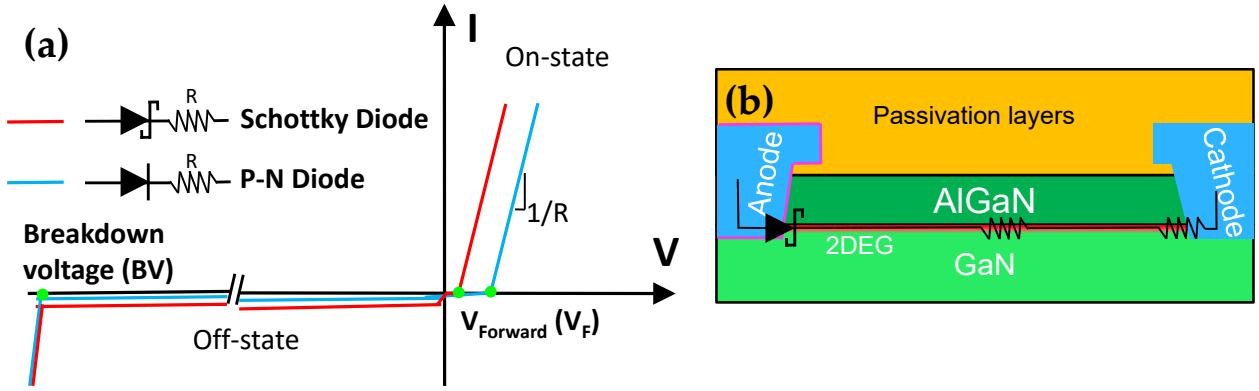

Figure 10: (a) I(V) characteristic of Schottky and p-n diode (b) Generic cross-section of a lateral AlGaN/GaN Schottky diode with a recessed anode (Schottky contact) and cathode (ohmic contact).

[2] The word « static » means that there are no moving parts inside the converter. Thus no transduction from the electrical to the mechanical domain is present in the converter

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With the AlGaN/GaN heterojunction, a Schottky diode can be obtained by crossing the latter with two contacts as shown in **Figure 10(b)**. The Schottky behavior and the ohmic contact are obtained by choosing a metal with the right work function as it will be shown later. The distance between both electrodes is chosen according to the voltage range of the diode [57]. The advantage of using a heterojunction is the very low resistance induced by the 2DEG making the conduction losses very low.

At CEA LETI, the Schottky diode is designed to withstand 650 V in reverse and to conduct 6 A in forward regime [58]. In the 100 to 650 V and several amperes range, the existing diodes in silicon are p-n and the SiC ones are Schottky [59]. With respect to p-n diodes, Schottky diodes forward voltage is smaller (as illustrated in **Figure 10(a)**) because they have a smaller built-in potential. Moreover, since the conduction in on-state for GaN and SiC Schottky diodes is due to majority carriers (electrons), their reverse recovery charge Q_{RR} (as sketched in **Figure 11(a)**) is negligible with respect to fast recovery silicon p-n diodes as experimentally shown in **Figure 11(b)**. Indeed, the switching time is not limited by the recombination of injected minority carriers [60, p. 122]. This makes them more suitable for high-frequency applications. It can be noticed in **Figure 11(b)** that the SiC Schottky diode has the smallest Q_{RR}. However, to this day, the GaN diodes significant advantages over SiC ones have not been demonstrated yet [61].

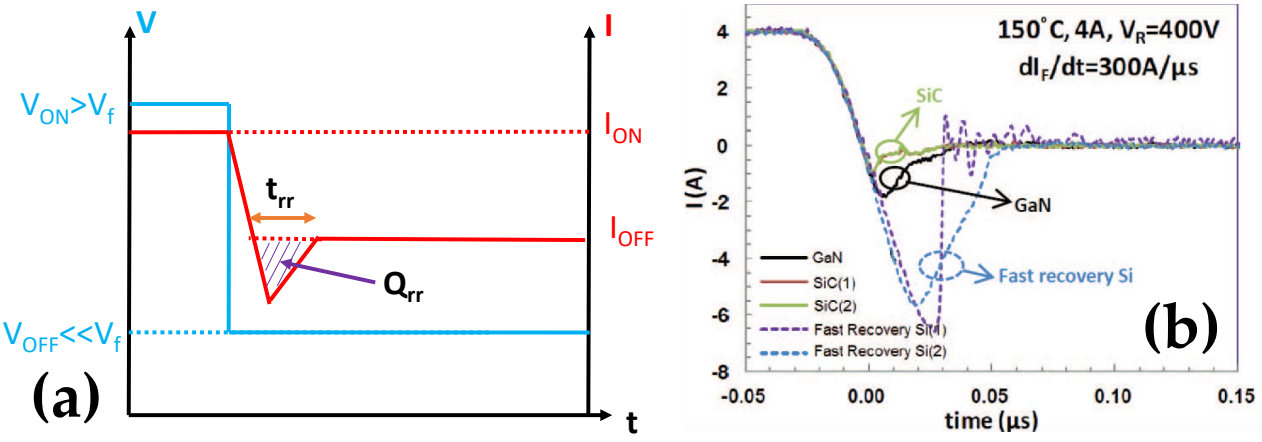

Figure 11: (a) Turn-off signal waveform with reverse recovery charge identification (b) Experimental comparison of a vertical Silicon p-n diode and a vertical SiC diode with respect to a lateral GaN Schottky diode on the Reverse Recovery charge [62].

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I.1.b.i.2nd The lateral AlGaN/GaN Power Transistor

A transistor is a three-terminal (source, gate and drain) power electronic device that is used as a voltage or current control switch. In this manuscript, the focus will be on the voltage control one. This means that by applying a voltage on the gate V_{GS} (reference to the source) below a threshold voltage V_{TH}, the transistor blocks the current from flowing from the drain to the source (blocking mode or off-state) as shown on the left side in **Figure 12(a)**. When V_{GS} exceeds a certain bias the transistor lets the current flow from the drain to the source as shown on the left side in **Figure 12(b)**. In on-state, the transistor is characterized by its on-resistance R_{ON} which is for the static one inversely proportional to the slope in the output characteristic at the on-state voltage (V_{GS} = 6 V in our case) as illustrated in **Figure 12(b)**. By the way, in this figure, at V_{GS} = 0 V, the current is near zero confirming what was written before. It can also be observed that the AlGaN/GaN transistor is bidirectional in current since current flows in the third quadrant (green in **Figure 12(b)**). This is possible because this is not a bipolar transistor thus the electrons can flow in both directions (from source to drain and from drain to source) in the 2DEG. Nevertheless, it is non-ideal because it has a diode-like behavior for which the corresponding forward voltage increases when V_{GS} decreases.

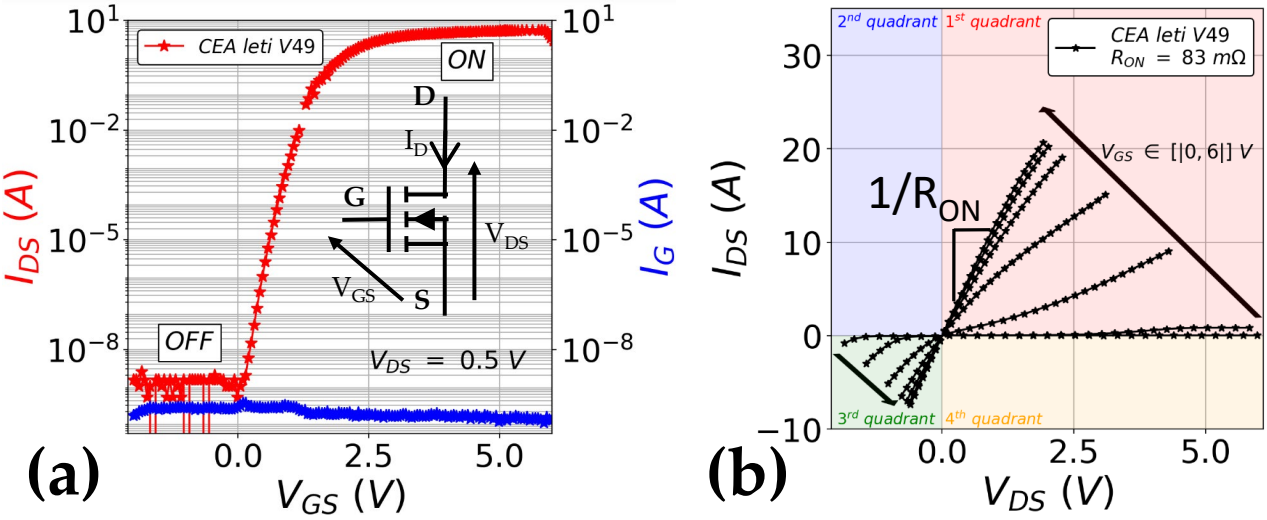

Figure 12: (a) Transfer characteristic of a typical 650 V/30 A AlGaN/GaN transistor (b) Output characteristic of the same transistor.

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In power electronics, it is important for a transistor to be normally-off meaning an enhancement mode behavior. In this case, the threshold voltage V_{TH} is higher than 0 V. Several definitions are proposed for this parameter depending on the supplier. For instance, Infineon™ proposes the V_{GS} at V_{DS} = 10 V for which I_{DS} = 2.6 mA [63] whereas GaN Systems™ proposes the voltage when $V_{GS} = V_{DS}$ for which I_{DS} = 7.5 mA [64]. At CEA, an approach closer to the physical definition of the threshold voltage (voltage for which the current starts to be drained) and thus will be used in this manuscript by default for CEA devices. The drain to source is slightly biased: 0.5 V and the threshold voltage V_{TH} and V_{PO} are defined as the voltage for which the current density (current normalized by the transistor width) reaches 10^{-5} and 10^{-10} A/mm respectively. The normalization allows getting the same threshold voltage whatever the device current rating. They are illustrated in **Figure 13** with two curves corresponding to a normally-on/off transistor.

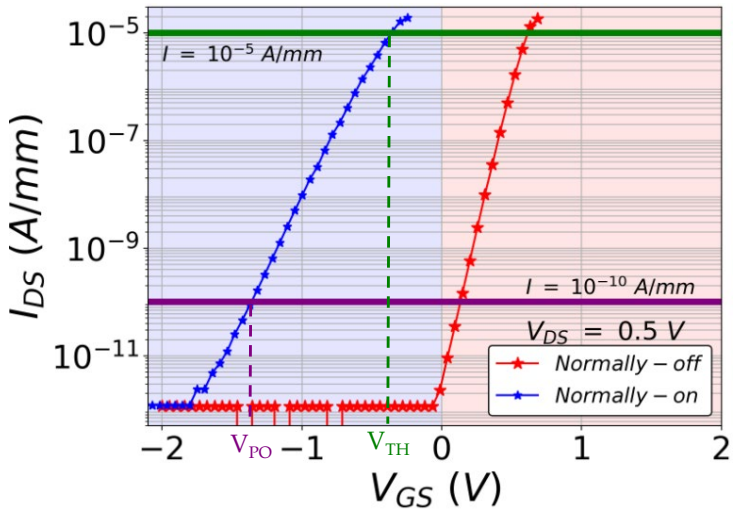

Figure 13: Threshold voltage V_{TH} and V_{PO} definition in the transfer characteristic.

Being normally-off and having a V_{TH} rather high with respect to 0 V has three advantages:

- Fail-safe operation: if the gate driver fails and its output goes to zero volt, the HEMT switches to the off-state preventing any short circuit [65]
- Noise immunity: when the device is switched from the on to the off-state, oscillations on the gate signal might occur as it will be detailed further. Nevertheless, having a V_{TH} rather high with respect to 0 V prevents unwanted turn-on (false turn-on) [66]
- Single polarity gate control: indeed a single voltage polarity makes the gate driver simpler which takes less space and design time [67]

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In the AlGaN/GaN literature, several architectures of normally-off devices were proposed as illustrated for the main ones in **Figure 14**. Except for the cascode technology in **Figure 14(a)** that needs a low-voltage silicon transistor to make the normally-off function, other normally-off transistor architectures are entirely made with GaN as semiconductor. As it can be seen in **Figure 14**, the source and the drain are directly connected to the 2DEG while the gate is in between the two other electrodes and "cuts" the 2DEG to obtain the normally-off function. This is done either electrostatically with the p-GaN acceptor ionization in **Figure 14(a)** and **(b)** with the p-GaN gate or Gate injection transistor (GIT) or by recessing the heterojunction and placing a Metal Insulator Semiconductor (MIS) Gate as in **Figure 14(d)** or by a 3D MIS control for the 3D-patterned gate illustrated in **Figure 14(e)**. The advantage and drawbacks of each technology are summarized in **TABLE 2**.

Other technologies to obtain normally-off operation are under study even though they are not in the spotlight such as the Fluorine implanted gate [68], [69], the p-GaN buried region [70] or the multi p-GaN well gate [71]. Furthermore, improvement of cascode configuration with a monolithic integration was proposed [72], [73]. The manuscript author contributed to [72].

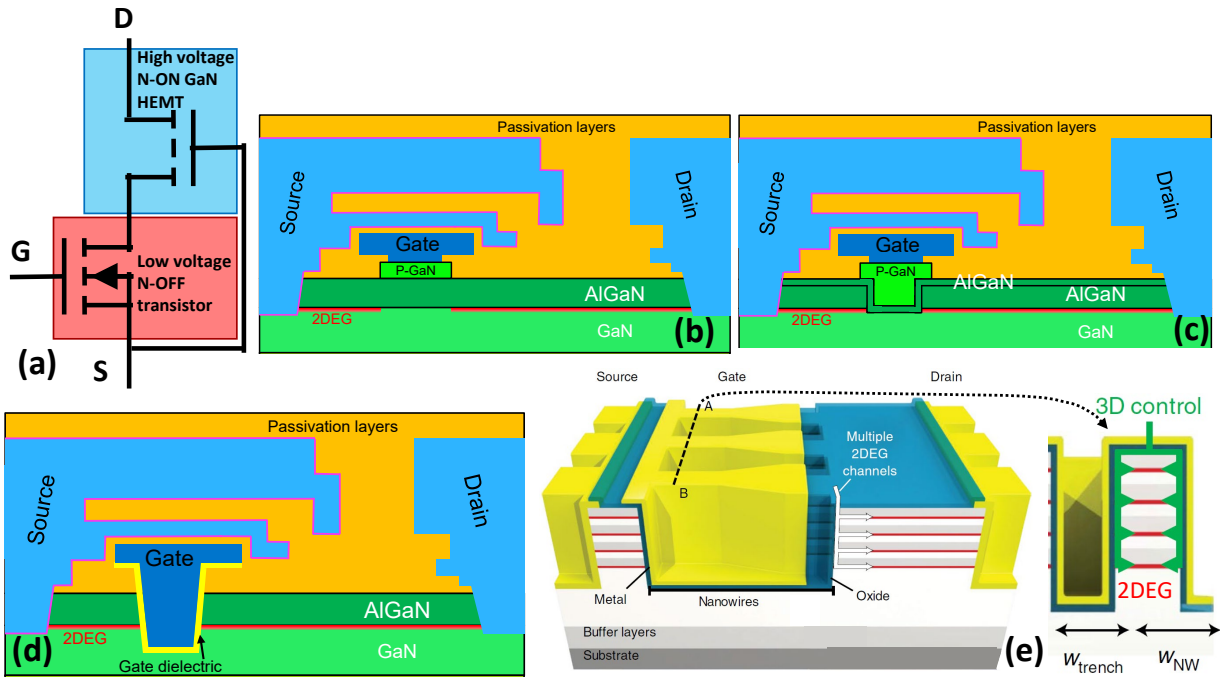

Figure 14: (a) Cascode transistor (b) p-GaN gate or Gate injection transistor (GIT) (c) p-GaN Through Recess and Regrowth Gate (TRRG) (d) Recessed MIS-Gate (e) 3D-patterned gate (taken and adapted from [74]).

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TABLE 2: Comparison between the main normally-off transistor architectures.

Architecture name	Advantages	Drawbacks
Cascode (Transphorm™ [75])	High V_{TH} [76]	- Package cost [67], [77] - Large parasitic inductance → oscillation (additional energy losses) + switching speed limitation [67], [77]
p-GaN (GaN Systems™ [78], TSMC™ [79], IMEC [80])	Large transconductance (gm) [67]	Gate reliability [81]
p-GaN TRRG (Infineon™ [82], Panasonic™ [83])	Large gm [67]	Specific gate driver [82] (less scientifically studied)
Recessed MIS-Gate (CEA LETI [84])	Large gm [67] Low gate leakage [85]	Threshold voltage instability [86]
3D-patterned (EPFL [87], National Cheng Kung University [88])	Large gm [67] Very low R_{ON} → multi-channel	Small nanowire → V_{TH} > 0 V [74]

A figure of merit in which transistors having different architectures can be compared is the specific on-state resistance $R_{ON,SP}$ (area covered by the device times the on-state resistance) versus the breakdown voltage (BV). These experimental devices can be compared with respect to theoretical expectations proposed by Gaska *et al.* [89]. For AlGaN/GaN lateral power device, the authors proposed **Equation 7**. It takes into account the electric field distribution non-uniformity with the term β_e corresponding to the ratio between the breakdown voltage and the ideal breakdown voltage (for which the electric field is uniform from the gate to drain). **Figure 15(a)** illustrates the ideal electric field profile (dashed line) as well as the β_e calculation for a non-ideal profile. It also assumes that the main contribution of the on-resistance is coming from the gate to drain region and the ohmic contacts. For the vertical devices, the formula is given in [89] (not presented here).

$$R_{ON,SP} = R_{ON} \times \mathrm{A} = 2 \times R_C \times \frac{BV}{\beta_e \times E_C} + \frac{1}{q \times \mu_{2DEG} \times n_{S,2DEG}} \times \frac{BV^2}{{\beta_e}^2 \times {E_C}^2}$$

Equation 7: Specific on-state resistance $R_{ON,SP}$ analytical expression for lateral AlGaN/GaN single channel devices ($R_{ON,SP}$: on-state specific resistance; R_{ON}: on-state resistance; A: device area; R_C: contact resistance; BV: Breakdown Voltage; β_e: electric field non-uniformity coefficient; E_C: critical electric field; μ_{2DEG}: 2DEG electron mobility; $n_{S,2DEG}$: 2DEG electron density) [89].

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Figure 15(b) shows the $R_{ON,SP}$ vs BV for state-of-the-art lateral AlGaN/GaN transistors with the theoretical expectation for vertical silicon, silicon carbide devices and lateral GaN transistors (with and without ideal ohmic contact and electric field). Focusing on the theoretical expectation, lateral GaN devices seem most promising than their Si and SiC counterparts. Nevertheless, experimental transistors (single channel) are still far from the theoretical expectation. The first reason could be that the theoretical on-resistance does not take into account the source to gate and gate resistance. Indeed by comparing dashed and continuous line, ideal curve is approaching real devices. The second reason could be that the electric field distribution is not well managed because by reducing β_e, ideal curves are shifted to the left (orange vs red curves). To exceed the actual single-channel limit, EPFL proposed a multi-channel architecture [74].

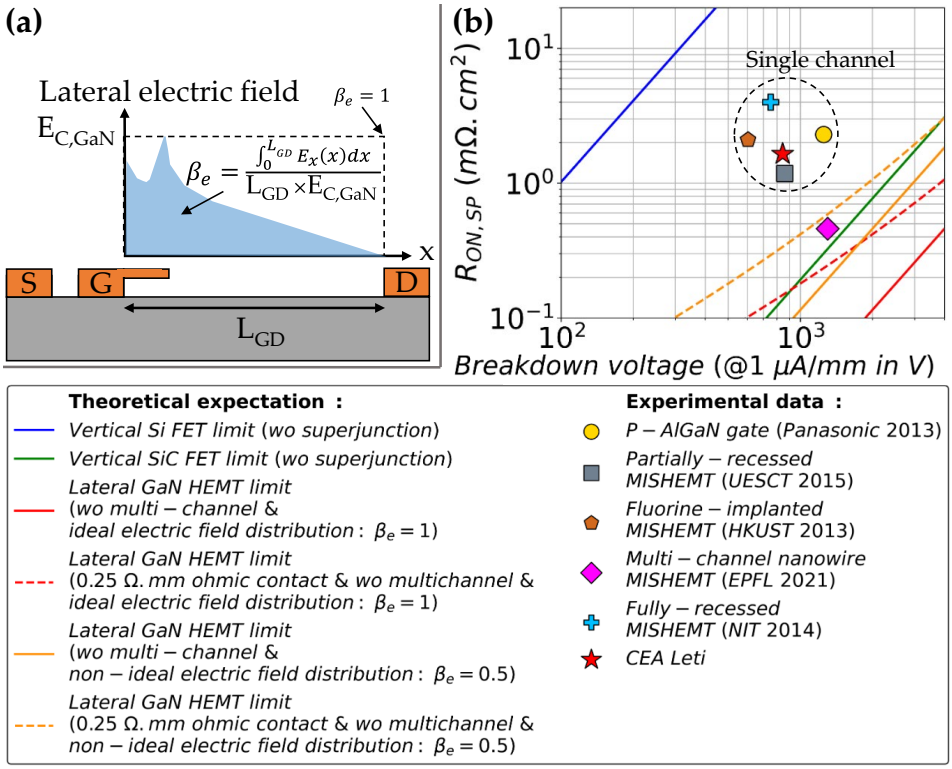

Figure 15: (a) Electric field profile in the 2DEG at the breakdown with the illustration of the electric field non-uniformity coefficient; (b) $R_{ON,SP}$ vs BV of state-of-the-art enhancement mode transistors (Panasonic™ 2013 [90]; UESCT 2015 [91]; HKUST 2013 [92]; EPFL 2021 [74]; NIT 2014 [93]) with respect to the theoretical expectation [89] (used parameters: $\epsilon_{r,Si} = 11.4$; $E_{C,Si} = 0.3$ MV/cm; $\mu_{Si} = 1400$ cm²/(V.s); $\epsilon_{r,SiC} = 9.66$; $E_{C,Si} = 3.0$ MV/cm; $\mu_{SiC} = 900$ cm²/(V.s); $n_{S,2DEG} = 1.0\times10^{13}$ cm²; $E_{C,GaN} = 3.3$ MV/cm; $\mu_{2DEG} = 2000$ cm²/(V.s)). Note: transistors from the literature for which the breakdown voltage at 1 µA/mm was neither provided nor represented in a figure were not taken into account.

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Nevertheless, this Figure Of Merit (FOM) is still limited because it takes into account neither dynamic effects such as current collapse nor switching aspects. For the latter, FOM such as the gate charge Q_G as a function of R_{ON} can be used (Q_G was not available for the studied devices) or R_{ON} vs C_{OSS} (output capacitance) or R_{ON} vs Q_{RR} [94].

I.1.b.ii The Specificity of Lateral AlGaN/GaN-on-Si Power Devices

I.1.b.ii.1st The Substrate and the Epitaxy

† **The Substrate**

GaN can be grown on several kinds of substrate as listed in **Figure 16(a)** with the most common ones being: sapphire, silicon carbide and silicon. As it can be seen in **Figure 16(a)**, the latter is used in part because of its lower cost. Moreover, for mass production, large wafers are preferable because it allows processing more dies at once. This is why silicon substrates are well-suited and were the choice of CEA LETI more than a decade ago. Thus, devices studied in this manuscript are built on 200 mm (8 inches) silicon substrates. Nevertheless, as it can be seen in **Figure 16(b)**, this technology has two significant drawbacks. The large lattice mismatch is the root cause of both. Indeed, silicon has a larger lattice parameter (a_{Si} = 5.431 Å [12] and a_{GaN} = 3.189 Å [10]). Without buffer layer engineering (described in the next paragraph), it would cause a huge dislocation density. This mismatch is worsened in temperature with the Coefficient of Thermal Expansion (CTE) mismatch (α_{Si} = 2.6·10^{-6} °C^{-1} versus α_{GaN} = 3-5·10^{-6} °C^{-1} for T ∈ [25, 150] °C [12]).

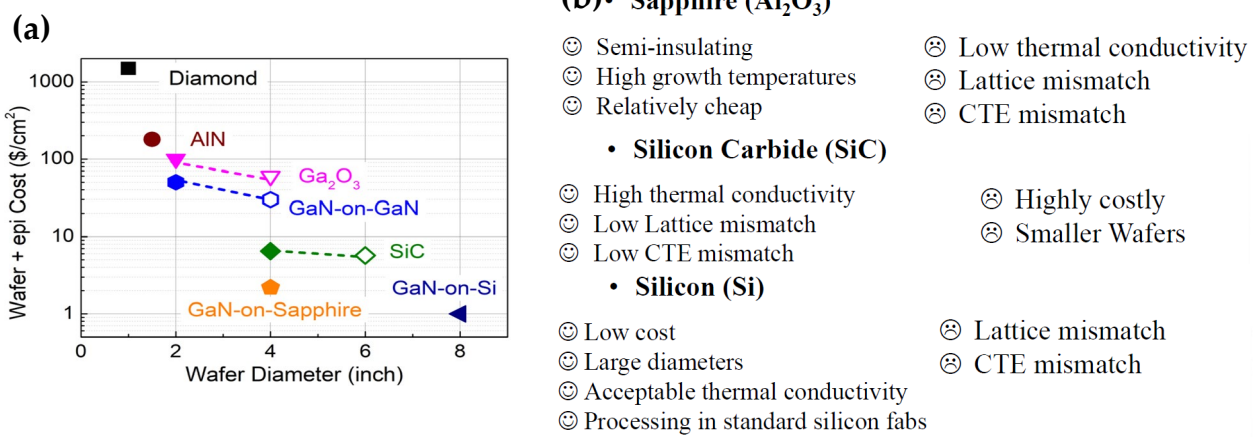

Figure 16: (a) Wafer and epitaxy cost as a function of the available wafer size [95] (b) Advantage and drawbacks of the main substrate technology in 2021 [96].

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† The Epitaxy

To deal with defects formation due to the lattice and CTE mismatch between GaN and Si and get a pseudomorphic (strain-free) top GaN layer, several types of epitaxies were proposed. They are composed of:

- A nucleation layer in AlN as shown in contact with the silicon substrate in **Figure 17**. Its small lattice parameter ensures good strain management compensating the thermal expansion coefficient difference between the buffer layers and silicon in order to get a low bow after the cool-down post-deposition [97]. Nevertheless, the dislocation density is huge [98].
- Stack of $Al_xGa_{1-x}N$ layers called strain relief layers. By tailoring the layers' thickness and composition: they progressively match the GaN lattice parameter reducing the wafer bow and density of defects (dislocations, pits) as shown in the study of Yamaoka *et al.* [99] and Charles *et al.* [100].
- A thick GaN layer because the overall epitaxial thickness counts for the vertical breakdown [101] (because the substrate is connected to either the source/anode of the device hence creating a vertical electric field in blocking mode). It is usually composed of a carbon-doped layer GaN:C to improve breakdown voltage and reduce lateral and vertical leakages [102] and an unintentionally doped GaN layer (UID-GaN).

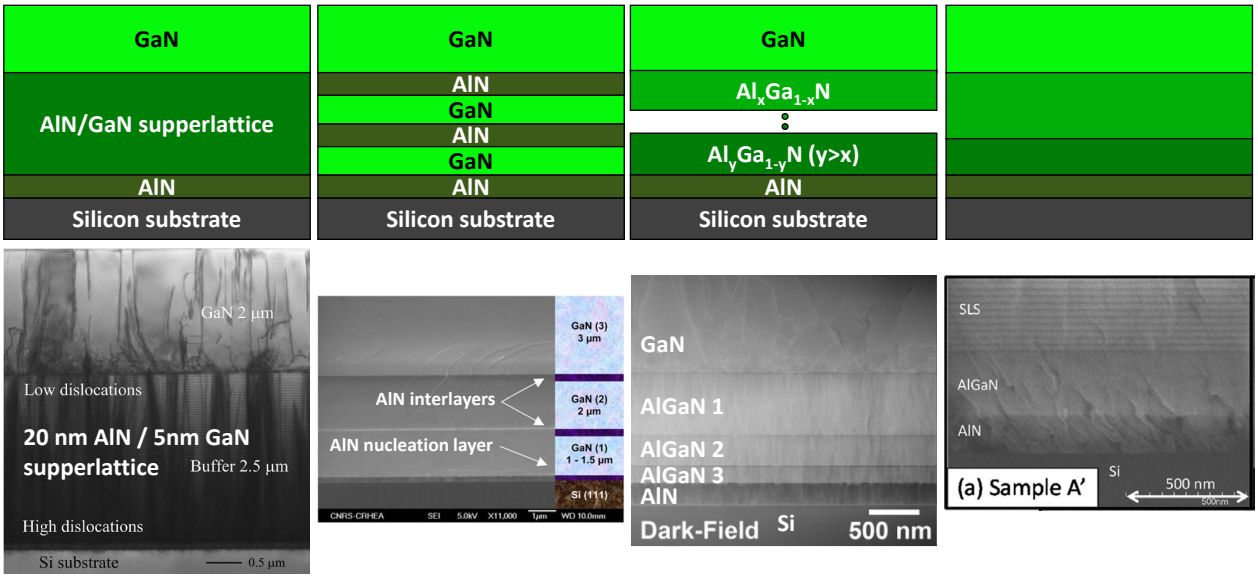

Figure 17: Different types of GaN-on-Si epitaxies (cross-section schematics at the top and electron microscope images at the bottom): AlN/GaN superlattice on the left [103]; AlN interlayers in the left-center [104]; Step graded AlGaN in the right-center [105]; Mixed structure on the right [99].

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I.1.b.ii.2nd The Front-End Of Line and the Back-end Of Line

To develop the power device, several technological building blocks are necessary. In this section, the attention will be focused on the Front-End of Line (FEOL) development mainly made at CEA LETI because they are linked to the studies performed during this PhD. Back-End Of Line (BEOL) fabrication steps consist in depositing thick passivation layers and creating metal interconnections (crucial role for high current devices). Here are the main FEOL building blocks:

† **Ohmic and/or Schottky contact:**

At CEA Leti, having a recessed-ohmic contact in contact with the 2DEG leads to a lower contact resistance as demonstrated by Greco *et al.* [106]. The latter is constituted of a Ti/Al bilayer whereas the Schottky contact is made of TiN. Those materials were chosen according to the obtained Schottky barrier height exposed in the study of Liu [107]. Moreover, having a fully-recessed Schottky contact with thinner passivation under the first field plate (element developed later), lead to improve leakage/forward voltage (black triangles in **Figure 18(a)**) (Biscarrat *et al.* [58]).

† **MOS-Gate**

This building block is important as it electrostatically controls the on/off states of the transistor. Developments were performed to increase the V_{TH} as shown in **Figure 18(b)** (Vauche *et al.* [108]).

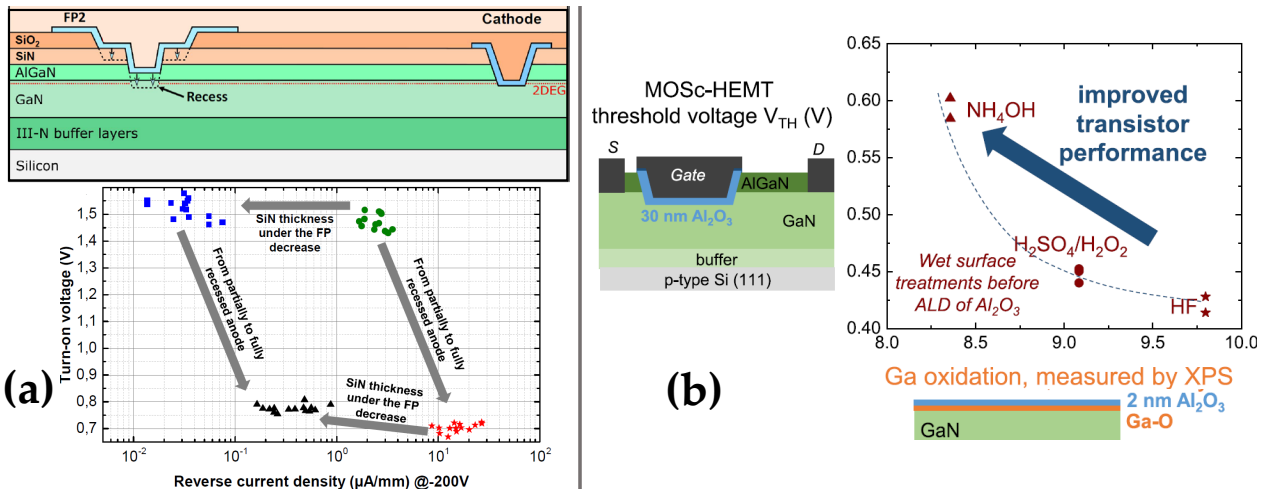

Figure 18: (a) Schottky contact forward voltage improvement and leakage reduction by having a fully-recessed Schottky contact and reducing passivation thickness [58] (b) GaN dielectric interface optimization with wet treatments to optimize the V_{TH} [108].

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I.1.b.ii.3rd The Packaging

To entirely benefit from the device properties, the packaging in which the bare die is embedded must be optimized on three different aspects:

- Reduced parasitic inductance and resistance due to the internal wire bonding → Allows to increase the power converter efficiency [109], [110],
- Small footprint on the Printed Circuit Board (PCB),
- High thermal efficiency.

As it can be seen in **Figure 19(a)**, the cited companies manufactured different packages that are compared with respect to their thermal resistance R_{TH} and area footprint. The ideal case would be on the bottom left-hand corner of the figure, where Surface Mount Technology (SMT) packages are set. Thus, a Dual Flat No-leads (DFN) package (belonging to the SMT package) was chosen for the device studied in this manuscript as shown in **Figure 19(b)**.

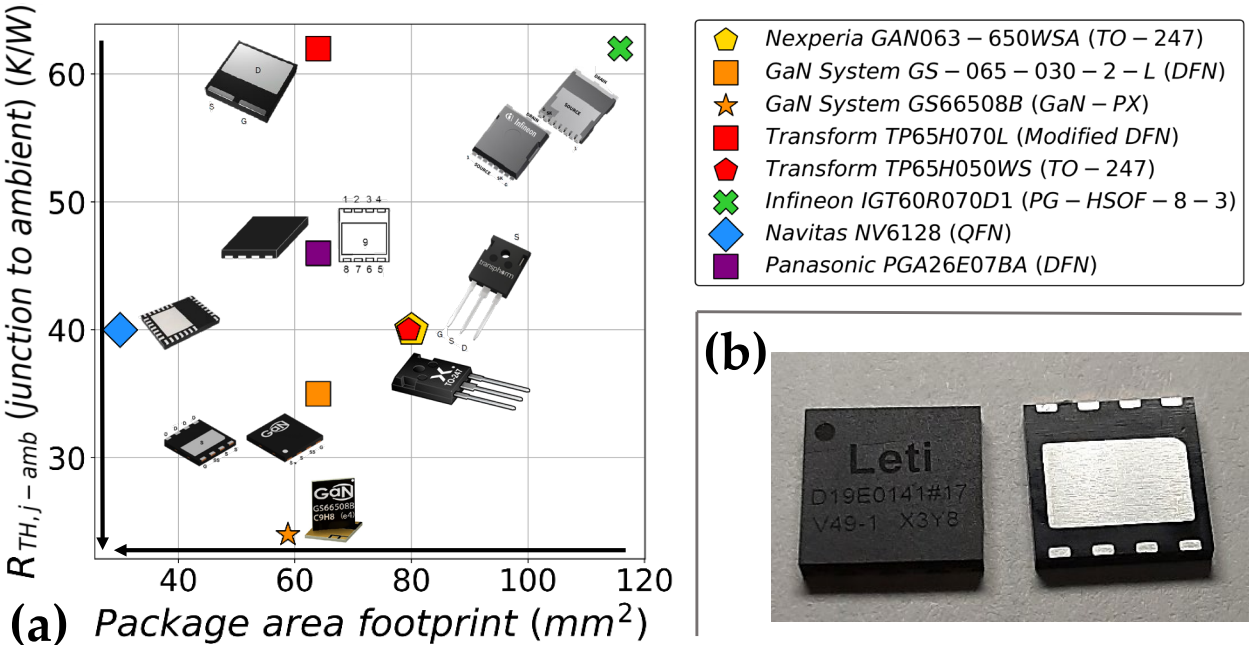

Figure 19: (a) Thermal resistance versus their area footprint for the package of different companies for 650 V/20-30 A rated transistors (GAN063-650WSA [111]; GS-065-030-2-L [64]; GS66508B [112]; TP65H070L [113]; TP65H050WS [75]; IGT60R070D1 [114]; NV6128 [115]; PGA26E07BA [116]) (b) CEA LETI bottom cooled 8×8 mm^2 DFN package.

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I.1.c Gallium Nitride: From the Power Device Performances to its Applications

GaN devices are already on the market. They are present in different applications and are expected to be adopted in several other ones. This part will present the two different transistor switching modes namely hard and soft switching before introducing the different existing and future applications of lateral AlGaN/GaN power devices.

I.1.c.i Transistor Hard and Soft Switching

As presented earlier, in power electronics, transistors are used as a switch from the on to the off state (turn-off or blocking) and *vice versa* (turn-on or priming). The transitions between both states are classified into two different categories: hard and soft switching. If in the I_{DS} vs. V_{DS} locus characteristics represented in **Figure 20**, it exists times t_{i_s} for which the current and the voltage are not null (meaning that the current and the voltage waveform are overlapping on the signal waveform as illustrated in phases 2 and 3 in **Figure 21**), it is called hard-switching (red curves in **Figure 20**). Otherwise, it is a soft-switching (blue curves in **Figure 20**). In that case, switching losses are drastically reduced as well as switching noise because the transient is slower by the presence of snubber and thus the dv/dt and di/dt are smaller. However, the devices number in the converter is higher [117], the gate control circuit is more complex [117] and the AlGaN/GaN power transistors are prone to more current collapse (on-resistance increase after turning the transistor off) [6] which makes soft-switching not suitable for all applications. Totem-pole Power Factor Correction boost converters, buck converters, motor control inverters, and single-ended flyback circuits topology present hard-switching whereas usual soft-switching topologies are Zero Voltage Switching converters, LLC converters, Active Clamp Flyback [118]. Thus, studies on hard-switching are interesting to be performed, as studied in this PhD manuscript (Chapter IV).

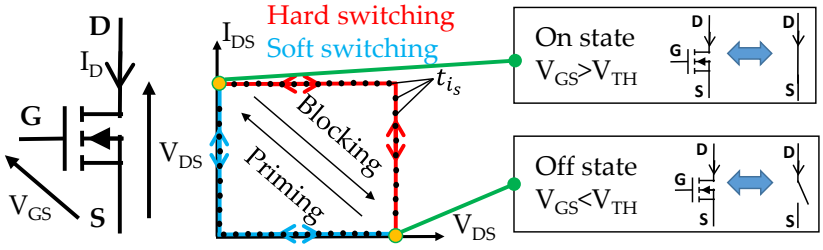

Figure 20: The power transistor symbol (on the left) with an ideal locus of $I_{DS}(V_{DS})$ in which each point correspond to a specific time t_{i_s} during switching between the on and off states (on the right).

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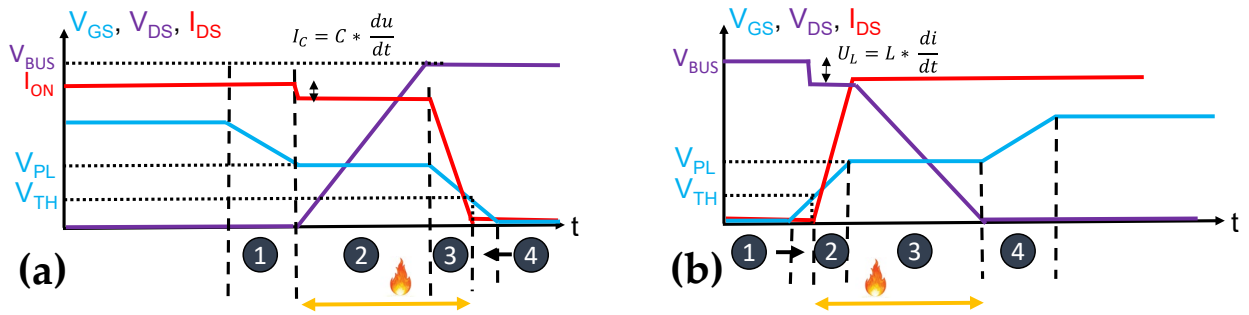

Figure 21: Schematics of the switching waveforms (adapted from [119]) with the flame representing losses during (a) the turn-off switching: blocking (b) the turn-on switching: priming.

Four switching steps can be identified in hard switching waveforms as it can be seen in **Figure 21**. There are described in the following paragraphs for the turn-on case to show the importance of transistor capacitance during switching (turn-off consists in the reverse behavior):

- Step (1): The gate voltage is increased until the threshold voltage (blue curve in **Figure 21(b)**). It mainly charges the capacitance C_{GS} with the charge Q_{GS1} [119] as illustrated in **Figure 22** (left side) to make the channel conductive.

- Step (2): The gate voltage is increased to the Miller plateau or voltage V_{PL} (blue curve in **Figure 21(b)**). This again charges C_{GS} with the charge Q_{GS2} [119] to reach the required current I_{ON} as illustrated in **Figure 22** (center left). This is why it is named the "di/dt period". Hence:

  - The larger the drain current, the longer this period,
  - The larger the gate to source capacitance, the longer this period.

- Step (3): The gate voltage stays constant at the Miller voltage (blue curve in **Figure 21(b)**). The drain to source voltage drops during the discharge of the gate to drain and the drain to source capacitances (C_{GD} and C_{DS} respectively with their respective charges Q_{GD} and Q_{DS} [119]) as illustrated in **Figure 22** (right side). This is thus named "dv/dt period". Hence:

  - The larger the off voltage (V_{BUS}), the longer this period,
  - The larger the drain to gate capacitance, the longer this period,
  - The larger the drain to source capacitance, the longer this period.

- Step (4): The gate voltage is increased until the on-voltage (blue curve in **Figure 21(b)**) while the gate to drain and gate to source capacitances finishes charging (**Figure 22** (right side)).

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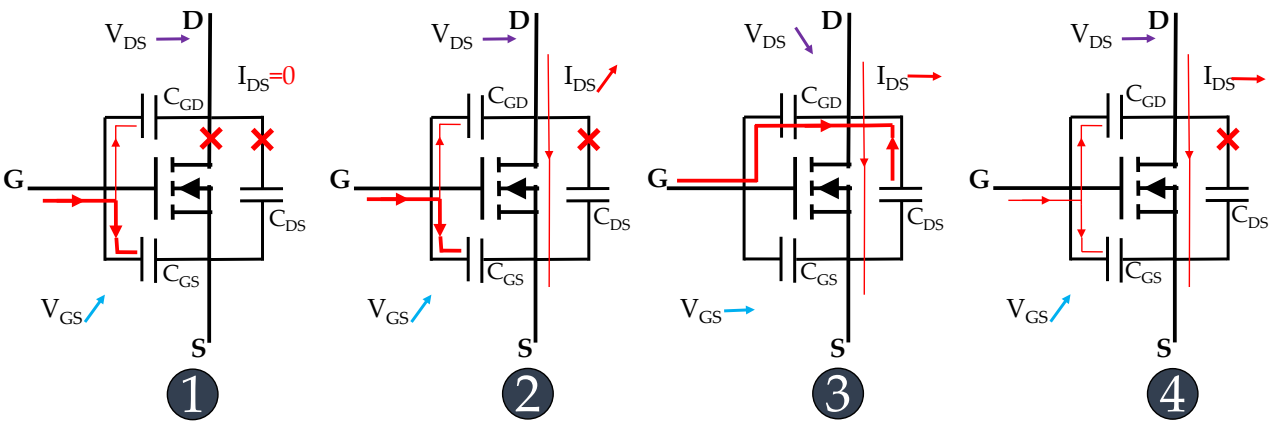
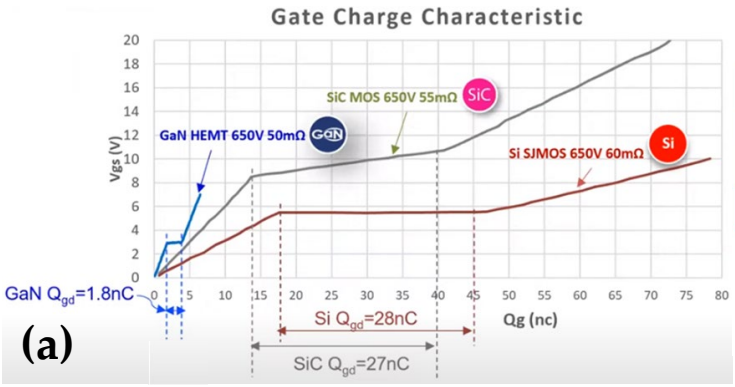


Figure 22: Transistor electrical behavior during the switching steps (adapted from [120]).

As stated earlier and in the light of the above explanation, a good physical quantity to gauge the switching speed of the device is the gate charge Q_G as shown in **Figure 23(a)**. Indeed the larger this quantity is to reach the on-voltage $V_{GS,ON}$, the longer the switching will be. Hence, to compare devices, as mentioned in the limitation of $R_{ON,SP}$ vs BV FOM, other FOMs have been proposed such as Q_G as a function of R_{ON} or R_{ON} vs C_{OSS} (output capacitance) or R_{ON} vs Q_{RR} [94] as shown in **Figure 23(b)**. The potential of GaN device is clearly enhanced with its lower FOM 1, 2 and 3.



600V FETs	Ron (mohm)	Ciss (nF)	FOM 1 (Ron*Ciss)	Coss (nF)@400V	FOM2 (Ron*Coss)	Qrr(uC)	FOM3 (Ron*Qrr)
Si SJ	37	7.24	267	0.38	14	36	1332
SiC MOS	120	1.2	144	0.09	10.8	0.053	6.3
GaN HFET	25	.52	13	0.13	3.25	0.113	2.8

Si SJ: Infineon IPW65R037C6. SiC MOSFET: Rohm SCT2120AF GaN HFET: GaNSystem GS66516T

advantage of fast gate driving capability

Reduction in switching loss in hard or soft switched converter

Reverse recovery loss reduction

(b)

Figure 23: (a) Gate charge characteristic of three different 650 V/30 A technologies [121] (b) Comparison of several static and switching-related properties of GaN, SiC and Si power transistors proposed by Chauhan [96] based on Huang's table [94].

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I.1.c.ii A Wide Range of Applications for GaN transistors

As it can be seen in **Figure 24**, GaN is expected to overcome the silicon Super Junction (SJ) vertical transistor limits for mid-range power transistors (≈ 0.01-10 kW) because the power converter switching frequency can be increased. This is the consequence of the switching time reduction. This increased frequency allows to reduce the size of passive components (inductance and capacitor) inside the converter. This has two advantages:

- Reduces the overall power converter size → Increased power density as shown with the little box challenge (smaller 2 kW power converter having at least 95%) [122],
- Increases the power converter efficiency (less power losses in the passive devices) with respect to silicon converter [123], [124].

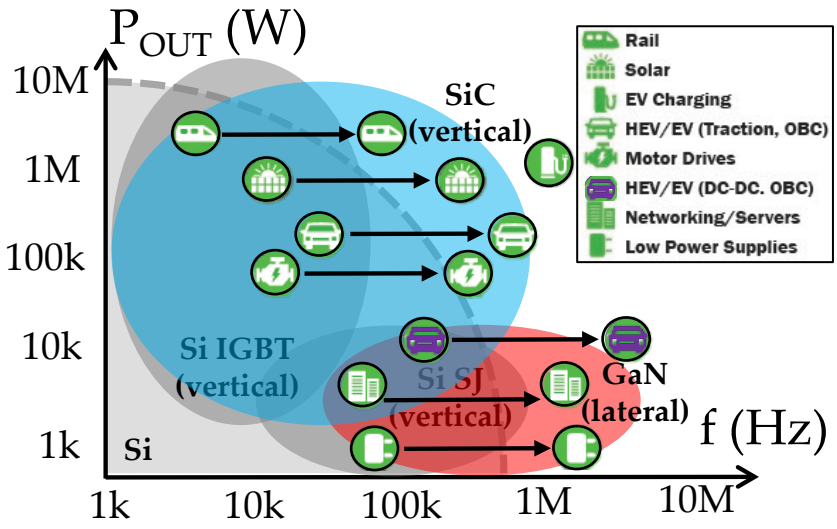

Figure 24: Power converter applications in the output power versus frequency graph in which GaN, SiC and Si power transistor application ranges are displayed (adapted from [125]).

I.1.c.ii.1st Consumer Applications

As far as the author knows, this was the first application available on the market. Consumer power converters are for instance mobile phone chargers (example: Samsung mobile phone **45 W** with GaN System device [126]) or laptop chargers (example: Dell laptop **90 W** charger with Navitas devices [127]). Nevertheless, to this day, these chargers remain more expensive than their silicon counterparts.

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I.1.c.ii.2nd Automotive Applications

For automotive applications, GaN could be used in two types of converters as shown in **Figure 25** in addition with Light Detection And Ranging (LiDAR) system in autonomous vehicles:

- On board charger (OBC) ranging from **3.3 kW** for single-phased converter (For instance: Alternative Current (AC) to Direct current (DC) (85 V/265 V → 200 V/450 V) two Continuous Conduction Mode (CCM) interleaved boost Power Factor Correction (PFC) converters in parallel, which operate 180° followed by a Pulse Width Modulation (PWM) Zero Voltage Switch (ZVS) full-bridge DC-DC converter by Gautam *et al.* [128]) to **22 kW** for three-phase power converter (Lu *et al.* [129]).
- DC/DC converters in the **hundreds of Watts to several kW range**. For instance: the five-phase fully regulated bi-directional 48 V to 12 V, 3 kW proposed by Jones *et al.* [130] reaches a 96% efficiency and uses 80 V/90 A related transistors. Another example would be the 500 W 200 V to 13.6 V by Matsumori *et al.* [131] made with a boost converter in series with a LLC resonant soft-switching DC 272 V/ DC 13.6 V.
- LiDAR needs current pulse (>10 A) within a short time (up to 200 MHz) [132], [133]

Other converters are present in electric vehicles as shown in **Figure 25** but are not really suited for GaN devices or there is no significant advantage to use them. For instance, the main traction inverter is in the 30 to 400 kW range [134] and can require 1200 V rated transistor (not available in GaN yet) because 800 V-battery can be used [135]. Nevertheless, the study of Lu *et al.* demonstrated a hybrid Si and GaN 150 kW T-type three-level phase-leg inverters [135] reducing the switching losses of 1200 V Si Isolated Gate Bipolar Transistor (IGBT) by switching with half voltage. Moreover, the voltage limitation can be overcome with multi-level architectures [136].

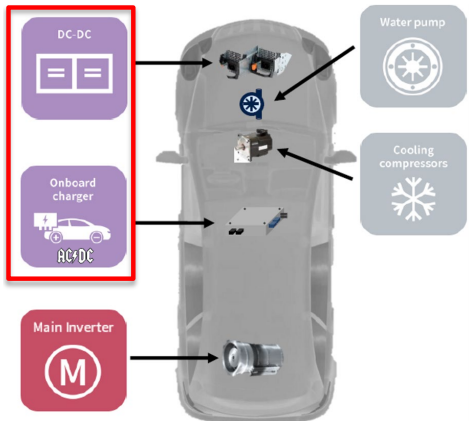

Figure 25: Power converter in the electric vehicle application (GaN target framed in red) [77].

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I.1.c.ii.3rd Photovoltaic Applications

As for the photovoltaic domain, the advantage is to reduce production costs thanks to the switching frequency increase allowing to use smaller capacitors and inductors that are cheaper [137, p. 244]. The advantage of GaN converter over silicon converter was demonstrated by Acansky *et al.* [124], by comparing the first generation of GaN device (300 kHz) with the well-established silicon technology (100 kHz) as shown in **Figure 26(a)** for input power higher than 50 W (blue vs. pink curves). The power converter (micro-inverter) transforms the continuous voltage of the photovoltaic cell(s) to an alternative signal (230 V for instance) as illustrated in **Figure 26(b)**. This is possible thanks to different converter topologies as summarized in the paper of Yuan *et al.* [138]. For instance, CEA LETI and the Institut National de l'Énergie Solaire (INES) collaborated for the release of a **400 W** DC 44 V to AC 230 V micro-inverter [139]. Micro-inverter allows the output power optimization of a multi-panel system preventing output power reduction of all cells when only one is defective due to aging, shading or reduced gain.

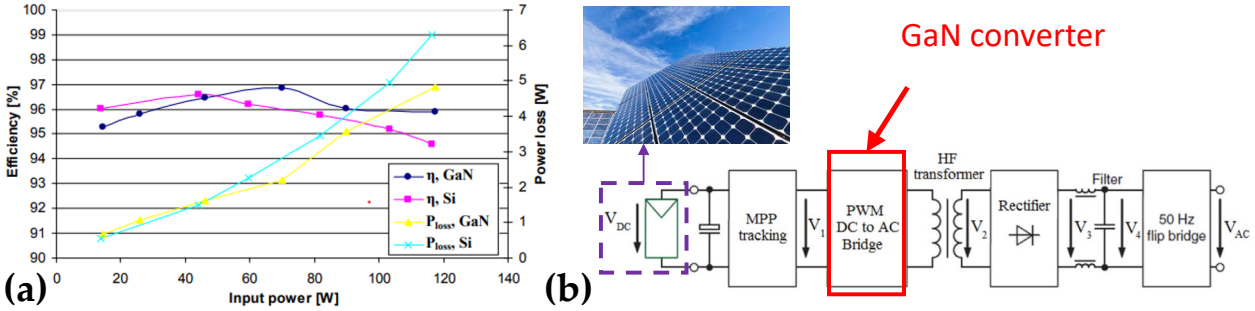

Figure 26: (a) Power converter efficiency as a function of the input power for Si and GaN devices [124] (b) Circuit function from the photovoltaic cell to the AC grid (taken and adapted from [140]).

I.1.c.ii.4th More Electric Aircraft Applications

As converter power density is increased, weight is saved which is interesting for More Electric Aircraft (MEA). For this application, Dual Active Bridge (DAB) DC/DC converters in the **kW range** are used. The frequency increase is visible by comparing the 270 V to 28 V, 3 kW SiC power converter of Pugliese *et al.* (40 kHz to 60 kHz for an efficiency maximum of 96.5%) [141] with the 270 V to 28 V, 3 kW GaN power converter of Quanxue *et al.* (100 kHz to 300 kHz for a maximum efficiency of 95%) [142].

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I.1.c.ii.5th Data centers and industrial Applications

To power servers in data centers or electrical machines in the industry, power converters in the **kW range** are used. GaN-based power converter allows to save room because the converter power density is increased. This is realized using two power converters in series:

- Power Factor Correction (PFC) that is used to convert the alternative 230 V signal to a continuous 400 V. This can be done using a hard switching Bridgeless Totem Pole PFC in Continuous Conduction Mode (CCM) as exposed in the study of Zhou *et al.* [143]. The topology advantage is to eliminate the Graetz bridge of classic PFC [144], [145].
- LLC resonant soft-switching DC/DC converters that transform the 400 V DC to DC voltage ranging from 5 to 56 V [121].

I.1.d Summary

Within this first chapter section, it was initially shown that wurtzite GaN is mainly interesting for making lateral power active devices (diodes and transistors) because it has a high critical electric field and a high mobility reached in a 2DEG at the heterojunction in between two piezoelectric materials even though crystal defects are present.

After that, the Schottky diode as well as the different normally-off transistor architectures were presented with a focus on the technology developed at CEA LETI (epitaxy on a foreign substrate, MOS Gate, Schottky and ohmic contact). Nevertheless, it was shown on the $R_{ON,SP}$ vs BV FOM that the transistor performances were far from the theoretical expectation proposed by Gaska *et al.* [89]. This is probably due to the electric field management, which will be the first topic tackled in this manuscript.

To finish, on the one hand, lateral AlGaN/GaN Schottky diode has been shown to be suited for high-frequency applications because it has a negligible Q_{RR} due to its unipolar characteristic. Nevertheless, its superiority with respect to SiC diode in the same voltage and current rating has not been proven yet. On the other hand, lateral AlGaN/GaN transistors have a wide range of applications in power converters: from tens of Watts to several tens of kiloWatts with hard/soft switching topologies. This is why assessing and proposing ways to optimize the transistor hard switching performance will be studied in the last chapter of this manuscript.

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I.2 Device Architecture to Improve the Breakdown Voltage and Method to Study the Electric Field

In this subsection, a review of the different architectural elements that improve the breakdown voltage will be presented to place the technology developed at CEA LETI with respect to the state-of-the-art. This study leads to the release of a patent during the PhD [146]. After that, the different techniques available in the literature to study the electric field of the AlGaN/GaN lateral devices will be introduced to evaluate if they can be used for our purposes. It can be noted that all the already known techniques for vertical devices (MESA, Junction Termination Extension (JTE), guard rings) cannot be implemented on lateral devices.

I.2.a Device Architecture Improvements for High Breakdown Voltage

Five different architectural features were proposed to increase the breakdown voltage. They will be presented in the following subparts. It must be noted that architectural elements specific to p-GaN gate (for instance in [147]) will not be discussed.

I.2.a.i The Field Plates

The field plate is a metal element either electrically connected to the electrode as represented in **Figure 27(b)** for the diode case or electrostatically (**Figure 28(c)**). It has the same physical principle as the transistor case by replacing the anode with the gate and/or source and the cathode with the drain. This structure helps to distribute the lateral electric field in the region between the anode and the cathode (or between the gate and the drain) as illustrated in **Figure 27(a)** and **(b)** for $V_{CATHODE}$ = BV1 or V1. Therefore, the critical electric field is reached at a higher voltage with a field plate (BV2 in **Figure 27(b)**). Thus, as a rule, the field plates increase the breakdown voltage by reducing the electric field peaks in the channel (the ideal case for which the electric field is uniformly distributed is however difficult to achieve).

From the switching perspective, this metallic extension forms a Metal Insulator Semiconductor (MIS) capacitor [148] with the channel located at the AlGaN/GaN interface as shown in **Figure 27(b)**. Thus, it may increase the device capacitance and therefore the charge required to switch it, which can increase the switching losses (increased switching time).

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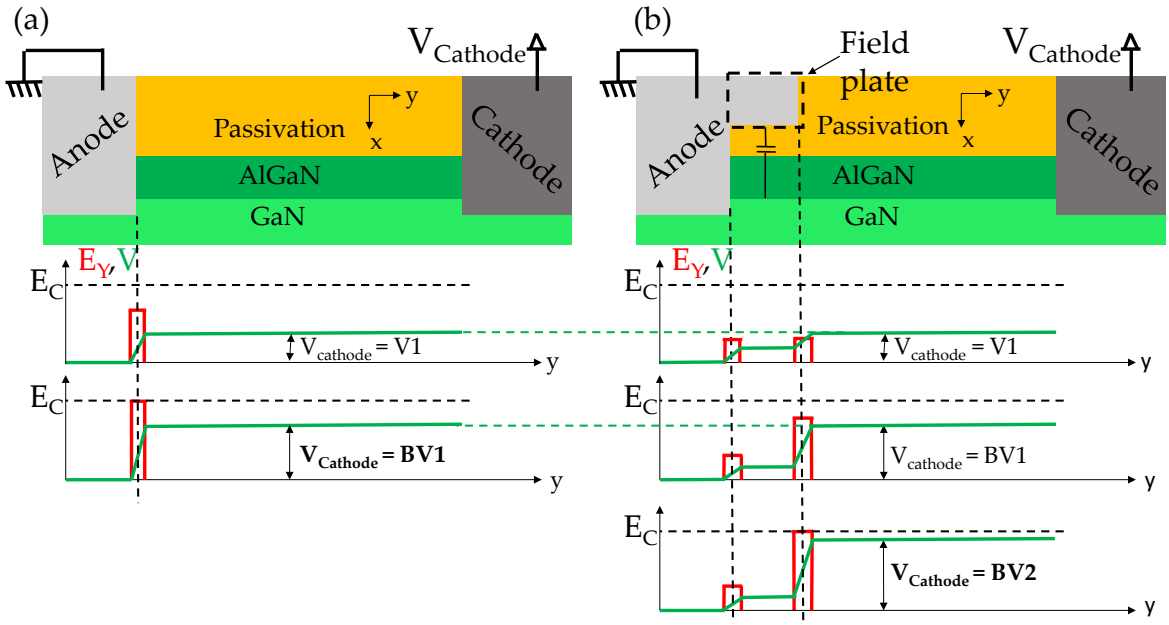

Figure 27: Field plate working principle in the ideal case (lateral electric field only) adapted from the explanation of Ma *et al.* [149] (a) Device without field plate (b) Device with a field plate.

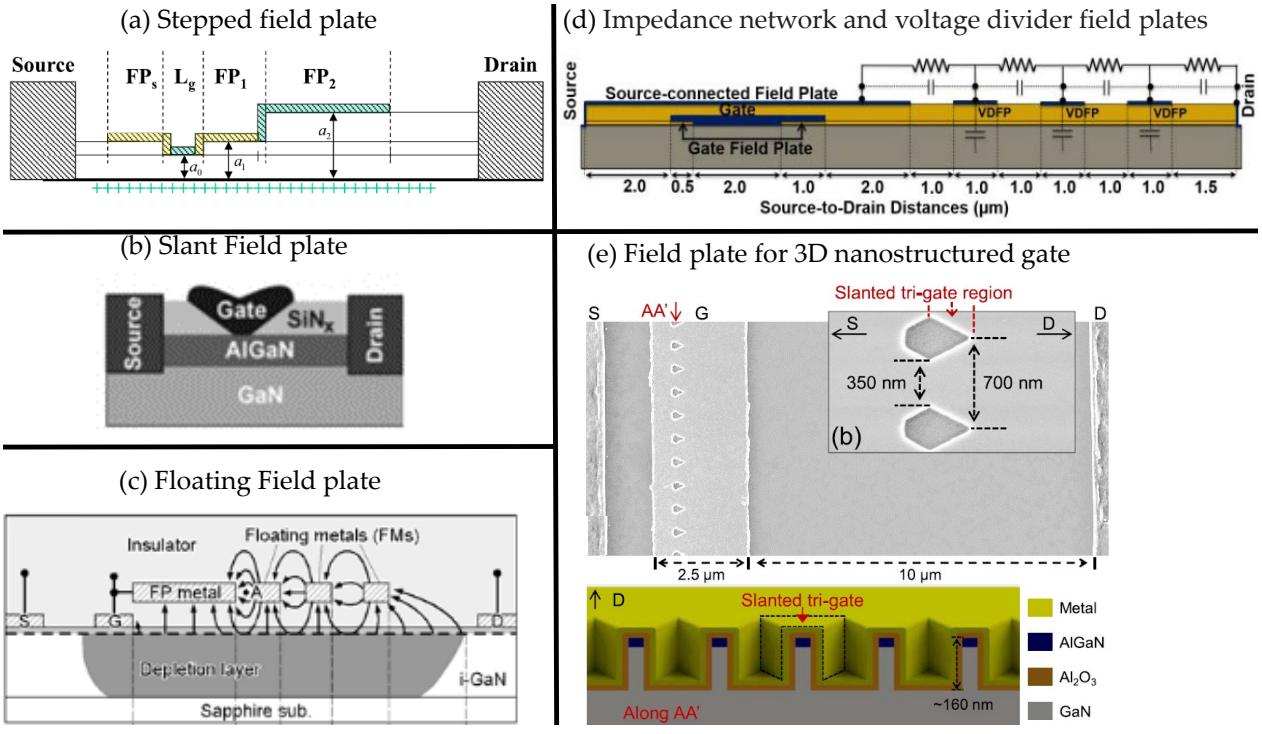

Figure 28: The different kinds of field plate architecture (source of the pictures: (a) Stepped field plate [150] (b) Slant field plate [151] (c) Floating field plate [152] (d) Impedance network and voltage divider field plates [153] (e) Field plate for 3D nanostructured gate [149].

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The first one is the stepped field plate as illustrated in **Figure 28(a)**. It is the technique used at CEA LETI up to now. It is one of the easiest in terms of implementation. Several parameters have to be tuned to optimize this structure. The first one is the length of the field plate and the second one is its height with respect to the neighboring one(s). Considering the electric field at the FP_1/FP_2 transition in **Figure 28(a)**. The larger is FP_2 and the smaller the transition is, the smaller the electric field at the transition because the capacitive coupling difference between both will be reduced. However, the high electric field created at the transition between two adjacent field plates can limit the breakdown voltage of the device as reported by Hu *et al.* in [154].

By shrinking the length of the field plates and reducing the transition height, the slanted field plate can be obtained as illustrated in **Figure 28(b)**. It has a very uniform electric field distribution under the field plate. However due to the fact that the angle with the horizontal plane is small (6° by Wong *et al.* [155]) the process to achieve it is expensive and requires lots of etching steps as described in the patent: US8980759B1 [156].

Some floating metallic extensions of the field plate can be created between the gate and drain as illustrated in **Figure 28(c)** (or cathode to anode [157]). The capacitive coupling between the floating metal and the field plate extends the action range of the field plate, distributing the electric field over a larger area. The drawback is that floating metals can be charged during the process leading therefore to unexpected device characteristics such as higher on-resistance.

To overcome this drawback, resistive elements can be connected to the floating field plates and the electrode creating a voltage divider as illustrated in **Figure 28(d)**. The metallic parts therefore undergo a linear potential drop making the lateral electric field in the channel quasi-uniform by capacitive coupling. However, no real implementation of this device already exists.

Finally, the slanted field plate concept can be implemented only the tri-gate structure proposed by EPFL [149]. The gate stack including the channel is a fin that controls the 2DEG depletion from the lateral sides. The slanted field plate is created by the angle that is designed in the layout of the devices. The main limitation is the fins' width that has to be in the tens of nanometers range for a full depletion at $V_G = 0$ V [149], [158]. It was increased to 200 nm with a p-GaN layer in the gate stack [159], which can only influence the top channel in a multi-channel device [74].

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I.2.a.ii The Low Conductive Layer

The Low Conductive Layer (LCL) or slow gate concept is an extension of the voltage divider field plate concept illustrated in **Figure 28(d)**. It consists of the addition of a highly resistive layer between the source and the drain and the LCL and can be inserted above or below the 2DEG as it can be seen in **Figure 29(a)**. It allows smoothing the electric field distribution along the device length by imposing a resistive potential drop close to the 2DEG. As the lateral electric field is uniform, the device shows a capacity to withstand high voltages. This technology has been patented in US9673285B2 [160] and US20130056753 [161].

One of the requirements for this technology to work is that the layer resistance must be high enough to prevent excess leakage current. A 1 MΩ/□ sheet resistance is recommended in US20130056753 [161] whereas in the [0,8 GΩ/□; 10 GΩ/□] range is proposed by Gaevski *et al.* [162].

From the switching perspective, this is also a very interesting concept. Indeed when the V_{GS} = 0 V and the LCL is connected to the gate, the 2DEG is depleted along the whole device length, making the capacitances of the transistor C_{DS}, C_{GS} and C_{GD} smaller [162]. This can make the switching faster and potentially reduces the switching losses. Moreover, at the working frequency, the layer can be "invisible" by making the RC characteristic time of the layer smaller than the period associated to the working frequency. In other terms, at operating frequencies [f_{MIN}, f_{MAX}], $\tau_{LCL} = R_{LCL}.C_{LCL} > 1/(2.\pi.f_{MIN})$ [162].

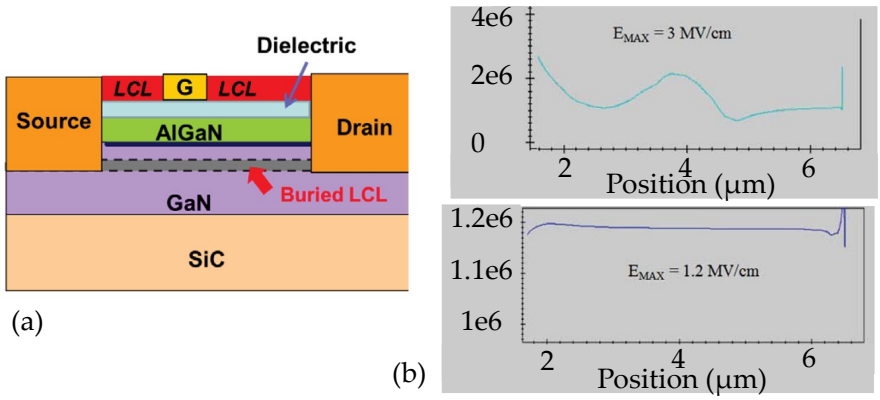

Figure 29: The low conductive concept (taken from [89]) (a) The different position of the Low conductive layer with respect to the conductive 2DEG (b) Electric field distribution between the gate and the drain at a given bias from 2D simulations (software not specified) without LCL (top) and with LCL (bottom).

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I.2.a.iii The Polarization Super Junction

The Polarization Super Junction (PSJ) comes from the Silicon Super Junction (SJ) concept [163]. It was developed by the Japanese company POWDEC and the University of Sheffield in England (patent: EP2988324 [164]). This concept is based on a charge balance to make the horizontal and vertical electric field uniform. Indeed in on-state, there is a charge balance between the 2-Dimensional Hole Gas (2DHG) and the 2DEG and also between the polarization charges as illustrated in **Figure 30(a)** for a transistor and for a diode (**Figure 30(b)**). In the off-state, as the 2DHG and the 2DEG are depleted, only the polarization charges remain. The constant distribution of charges along the length of the device makes the potential drop linear and therefore the electric field is uniform. This characteristic makes it better in terms of lateral voltage withstanding with respect to the conventional structure.

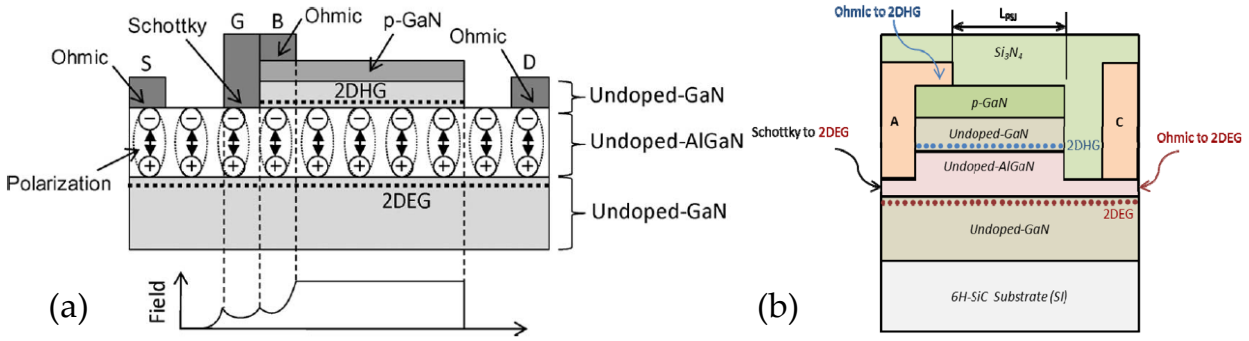

Figure 30: The Polarization Super Junction concept (a) Implemented on a transistor (taken from [165]) (b) Implemented on a diode (taken from [166]).

Here are other features that make this architecture interesting:

- As the Hybrid Drain-Gate Induced Transistor (HD-GIT) developed by Panasonic™, the PSJ is not sensitive to current collapse as shown in the study of Kawai *et al.* [167]. This may reduce the conduction losses.
- This architecture showed a 40% wider Safe Operation Area (SOA) boundary than conventional GaN transistors in the paper of Shankar *et al.* [168] because of the better electric field distribution, which is a big advantage for the use in hard switching.

However, it has two limitations: hole ohmic contact is hard to make on GaN layer without gold or a highly p-doped GaN layer and a parasitic capacitance is created between the two two-dimensional gases as shown in the paper of Unni *et al.* [166] in the diode implementation.

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I.2.a.iv The Epitaxial Layers Engineering

Numerous studies were proposed to improve the breakdown voltage by epitaxial layer engineering and can be grouped in two different categories:

- $Al_xGa_{1-x}N$ as a buffer layer close to the 2DEG or as back barrier [169]–[173] which is also called a Double Heterojunction HEMT (DH-HEMT) (with a step in the gate to drain region [174]) or a p-GaN buried layer(s) [175]–[177] (with a doping gradient [178]). The breakdown voltage is either improved due to an increase of the 2DEG electron confinement preventing source to drain punch-through breakdown as shown in **Figure 31(a)** or due to the Reduced Surface Electric Field (ReSurf) effect (electrostatic depletion of the channel electron allowing a more uniform electric field distribution as explained for high voltage lateral silicon transistor by Ludikhuize *et al.* [179]) as illustrated in **Figure 31(b)**.

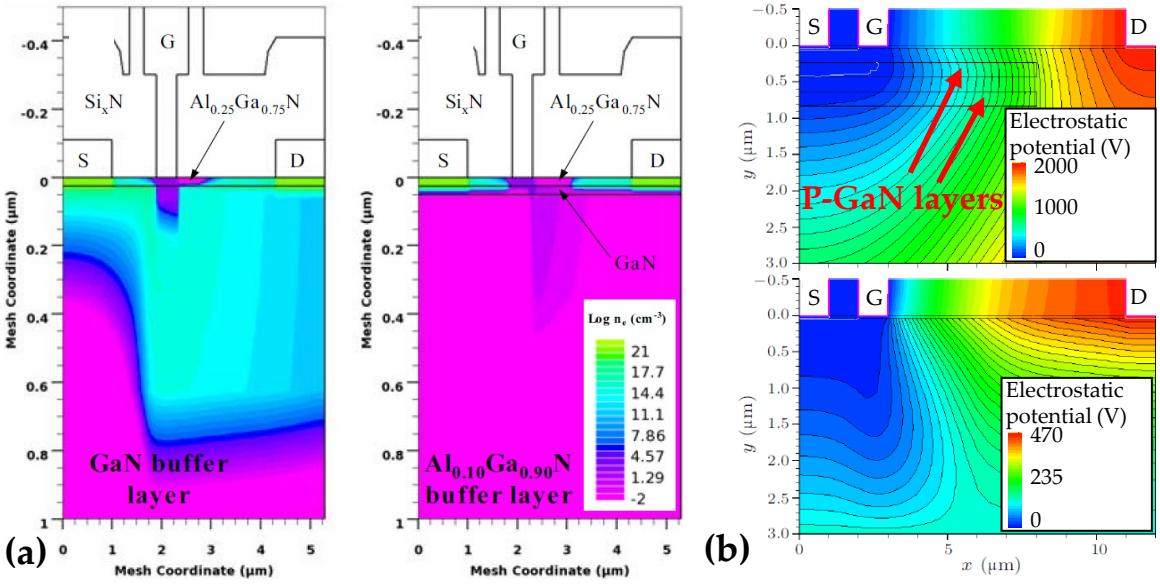

Figure 31: (a) Electron density mapping in blocking mode of a transistor without (on the left) and with (on the right) $Al_xGa_{1-x}N$ buffer layer [173] (b) Electrostatic potential mapping at the transistor breakdown for a transistor with (on the top) and without (on the bottom) two buried p-GaN back barrier showing the ReSurf effect [176].

- Stepped n-doped channel [180] that increases the breakdown voltage by pushing the high electron density area towards the drain or step-etch heterojunction [181] that shapes the electric field (no physical explanation available in the reference)

The limitations of both categories reside in the difficulty of breaking the epitaxial buffer horizontal invariance. For instance, the structure in **Figure 31(b)**, requires an implantation step in between epitaxial steps.

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I.2.a.v The Substrate Removal

The local (**Figure 32(a)**) or entire substrate removal breakdown voltage improvement when the substrate is floating for long gate-to-drain distance has been experimentally demonstrated by Visalli *et al.* [182] and Srivastava *et al.* [183] as shown in **Figure 32(b)**. It should prevent the hypothetical vertical breakdown limit probably limited by avalanche in silicon according to Visalli *et al.* [182]. However, as shown in **Figure 32(c)**, the maximum achievable current is reduced due to an increased self-heating effect according to the authors of [183]. Nevertheless, some years ago, Abid *et al.* demonstrated that the local substrate removal and the Physical Vapor Deposition (PVD) of a thick AlN followed by a thick copper layer leads to the reduction of the high-voltage trapping mechanism that occurs at the usual AlN/Si interface [184].

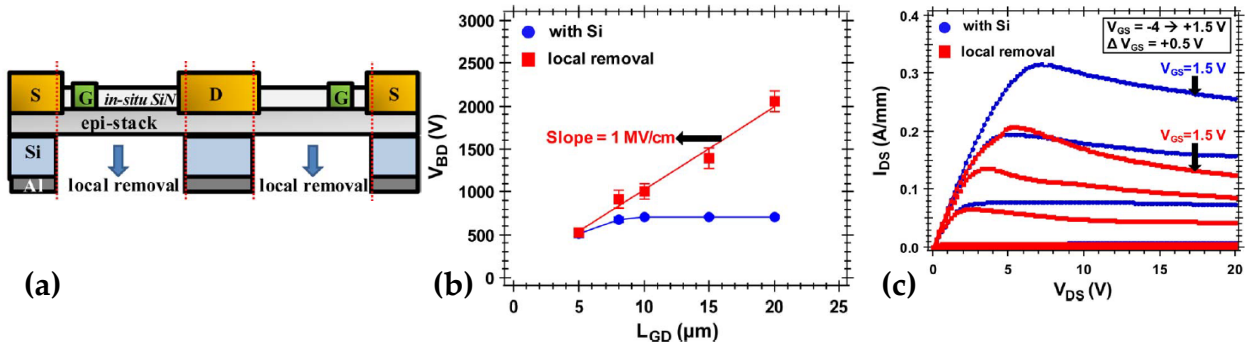

Figure 32: (a) Partial substrate removal illustration [183] (b) Effect on the lateral breakdown (floating substrate) of a transistor in OFF-state [183] (c) Effect on the output characteristic of the transistor [183].

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I.2.b Method to Probe the Electric Field

In the literature, several experimental methods were proposed to probe the electric field in the device. As it can be seen in **TABLE 3**, the main limitations are that they were either proposed for RF devices (having no field plates that may reflect optical beam) or limited to the available device surface (passivation in the studied devices are micrometer thick). This is why no details were brought in this manuscript. Nevertheless, simulation methods (analytical model and Technology Computer Aided Design (TCAD) simulation) exist. Their descriptions and limitations will be detailed in III.1.a because it is the introduction of the studies proposed in this chapter.

TABLE 3: Experimental techniques to probe the electric field in the AlGaN/GaN devices.

Technique name (small description)	Limitations
Micro-Raman temperature measurement [185] (detection of highly field-accelerated carrier that induces self-heating)	• Limited to on-state measurements (high dissipated power) of RF devices • Complicated with field plates that shield beams [186] • Surface electric field only
Liquid-crystal electrography [187] (electric field sensitive crystal deposited at the surface and that modifies the electrical properties of the back-side illumination)	• Surface electric field only • Complicated with field plates that shield beams [186]
Kelvin probe microscopy [188] (electric field sensitive cantilever that scans the device surface)	Surface electric field only (complicated with thick passivation layers)
Franz-Keldysh photocurrent spectroscopy [189] (field-assisted current generated by a front side illumination)	• Limited to the electric field estimation in the AlGaN • Complicated with field plates that shield beams [186] • Depends on the electron effective mass in the $Al_xGa_{1-x}N$
Two photons Optical Beam Induced Current [190] (carriers generation through photon absorption collected by the electrode after drifting under the applied electric field)	• Complicated with field plates that shield beams [186]
Electric field induced second harmonic generation [191] (indirect electric field measurement: front side detection of photon having a pulsation 2ω that results from the conversion of two photons (pulsation ω). The conversion is allowed by third-order non-linear susceptibility $\chi^{(3)}$ of the AlGaN/GaN heterojunction and the efficiency is electric field dependent)	• Complex optical setup • Limited to the electric field in the 2DEG • Complicated with field plates that shield beams [186]

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I.3 State-of-the-Art of the Switching Loss Measurement Techniques

Having described the motivation of studying hard switching losses in I.1.c.ii, this part will be focused on their origins and the experimental setups to extract them.

I.3.a Different Switching Loss Origins

In the power converter transistors, apart from the conduction losses due to either the leakage in off-state or the dynamic on-resistance in on-state (coming either from self-heating effects or trapping mechanisms known as current collapse [192]) that will not be discussed in the manuscript, switching losses happen. Their contribution follows the switching frequency trend. Above 20 kHz, they become the main part of the total losses [192]. They are classified into five types of losses:

1. Pure switching losses (E_{SW}) correspond to the energy that is dissipated during switching through the resistive elements of the packaged device from the overall supplied energy.

2. Gate losses (E_G) correspond to the energy dissipated in the gate resistors (element introduced to slow down the switching speed) and the PCB routine during the gate charging/discharging.

3. Output capacitance losses (E_{OSS}) correspond to the energy dissipated through the resistive elements of the circuit or redistributed to the load of the converter during another switching period after being stored during a switching event (turn on/off) into the output capacitance $C_{OSS} = C_{GD} + C_{DS}$. They are called losses in the literature because in the extraction loss methods, all the energies stored in the intrinsic capacitances are lost. However, in a converter, a part of this energy can be redistributed to the load connected to the output of the power converter and therefore a part of this energy could be reused.

4. Reverse conduction losses (E_{SD}) correspond to the losses when the transistor works in the 3RD quadrant introduced before (**Figure 12(b)**). The losses are encountered for instance in synchronous buck/boost converters, which is mainly a low power converters issue [193]. It may be used in Totem-pole PFC where the two high-frequency transistors are in silicon and the two low-frequency diodes are replaced by two GaN transistors working as rectifiers [194].

5. Reverse recovery losses (E_{RR}) correspond to the energy dissipated when the body diode of the transistor is turned off. Since there is no body diode in GaN transistors, these losses are null (except in the case of a cascode architecture because the low-voltage silicon transistor has a body diode).

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To summarize the list of switching losses, they are due to energy dissipation through Joule effect. The only limitation at this point is the extracted E_{OSS} which will always be overestimated with the following experimental setup which is performed without converter load.

I.3.b Different Setups for Loss Extraction

To this day, there are five different proposed setups:

I.3.b.i Double Pulse Test (DPT)

Double Pulse Test (DPT) is the most common test in the literature [195]–[199]. As shown in **Figure 33(a)**, it consists of an inductive loop constituted by the HS (High Side) transistor and the inductance L_{DPT} that will charge the LS (Low Side) transistor. During phase 1 (see **Figure 33(b)**), the LS is in the OFF state. In phase 2, the LS is turned-on to charge the inductance L_{DPT} until the on-current I_{ON} is reached. In phase 3, the LS is switched from the ON-state to the OFF-state and E_{OFF} can be extracted with the integral of $I_{DS} \times V_{DS}$ which gives the resistive dissipated energy $E_{I/V}$ (purple in **Figure 33(c)**) and the energy stored in the LS: E_{OSS}. At the end of phase 3, the LS is switched from the OFF-state to the ON-state and E_{ON} can be extracted with the integral of $I_{DS} \times V_{DS}$ which gives the resistive dissipated energy $E_{I/V}$ (blue in) and the energy stored in the HS: E_{qOSS}.

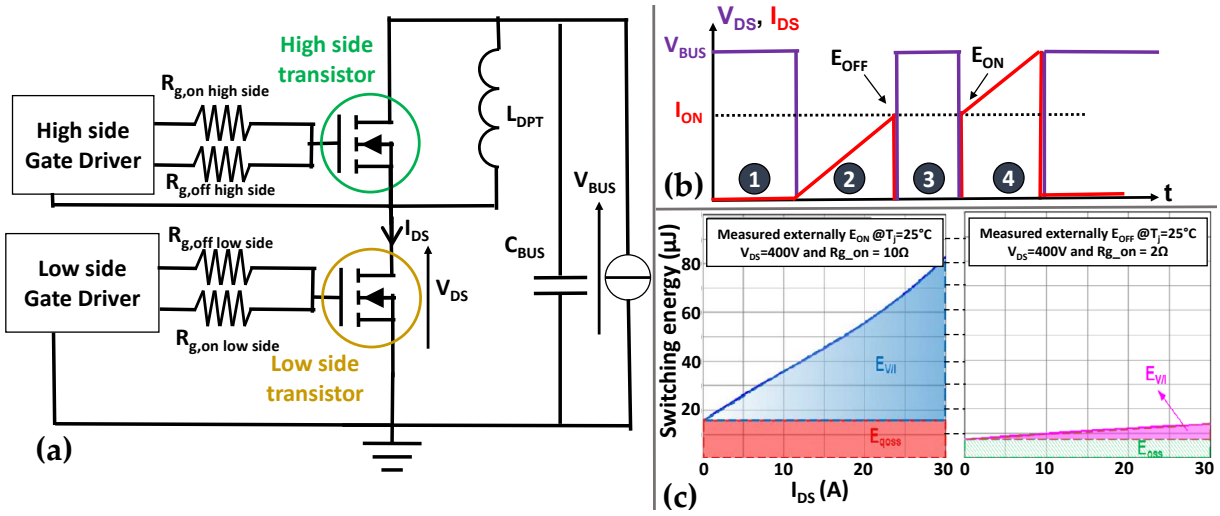

Figure 33: Double pulse measurement (a) Circuit design (b) Signal waveform (c) Switching energy extraction (adapted from [197]).

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Nevertheless, this technique has five limits:

- The voltage and current probes must have large bandwidth otherwise high frequency signals are filtered which induces measurement errors.
- Both must not disturb the circuit behavior: very low inductive behavior for the current probe and very high impedance for the voltage probe which is difficult to have [200], [201] especially because the current probe is often a current viewing resistor inserted inside the power circuit.
- A deskewed method must be used to synchronize the current and the voltage that were probed [200], [201] (delay induced by probe cable).
- It does not differentiate in C_{OSS} the capacitance from the device and the one of the PCB [202].
- Low accuracy for soft switching applications [203].
- The inductance L_{DPT} must be sufficiently high to obtain the same current for the turn-off and turn-on (case of the **Figure 33(b)**).

I.3.b.ii Calorimetric Measurement Test

It consists in measuring the switching losses dissipated from the circuit by heat. This method is well suited for soft-switching applications because DPT is not accurate enough for this [203]. The loss measurement can be done in several ways:

- Measuring the coolant parameters, differential temperature, and flow rate in an adiabatic chamber in which the temperature is controlled by a thermal exchanger [204], [205]
- Placing the circuit in a thermally insulated box. The dissipated power (heat) is measured based on the temperature difference T_{box}-T_{amb} (temperature in the box minus ambient temperature) times the thermal resistance R_{TH} of the insulated box. A fan makes the box temperature homogenous and its contribution to the box temperature is calculated and removed [206], [207].
- Placing the circuit in a thermally insulated box in which a thermometer that is sticked to a heat sink thermally connected to the DUT. The losses are thermally dissipated in the heat sink measurement thanks to a calibrated thermal model [203], [208].
- A thermometer is placed in a thermally insulated box connected to the device (thermal pad + thermal spreader + Vias in the PCB) to measure the thermal dissipated power [209].
- Thermal camera can be placed over the device to measure its temperature. The dissipated power is then calculated thanks to a thermal model [210]

However, an accurate thermal model calibration has to be performed [209] as well as dealing with thermal leakage. Furthermore, conduction and switching losses can be segregated by either an estimation based on static on-resistance (which may lead to errors) or adjusted by changing the setup switching frequency [203], [207], [209].

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I.3.b.iii Opposition Test Method

This experimental setup is constituted of two switching cells (Cell 1 & 2 in **Figure 34(a)**) made out of two transistors connected by an inductance at their midpoint as initially proposed by Turpin *et al.* [211] and used in other articles [212], [213], [201]. They are both connected to the same DC bus (stabilized by a capacitor), which has an ammeter and a voltmeter to measure the losses. It is possible to get good switching losses estimation by on the one hand, estimating or neglecting some losses (conduction, inductance, capacitor losses) and on the other hand, driving correctly the driver to obtain the drain to source waveform (blue and red curves) and the inductance current (green curve) in **Figure 34(b)** and **(c)**.

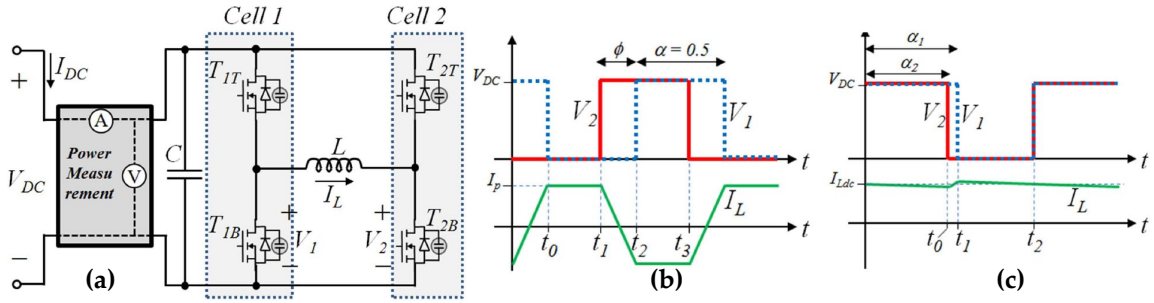

Figure 34: Opposition method [201] (a) Circuit schematic (b) Signal waveform for the turn-off losses (E_{OFF}) (c) Signal waveform for the turn-on losses (E_{ON}).

Even though it prevents high-frequency measurement errors induced by probes in the DPT [214], the proposed method has two main limitations:

- Many transistors are required: 4 which may not be adapted for the research level. For instance when device availability is restricted. Or, when the device reproducibility is rather low, the switching losses errors can be rather high. Furthermore driving accurately non-identical transistors can be difficult.
- Segregation of the losses remains a challenge [207]: for instance, conduction losses must be estimated which means that current collapse modeling and device self-heating must be quite accurate at many temperatures especially below the microsecond range.

I.3.b.iv Indirect Measurement Method

The method consists of measuring the difference between the input and the output power of a switching system, the total losses are equal to the subtraction of both terms [215]. It takes into account switching losses, conduction losses, inductance losses and capacitance losses. Other losses than the switching ones can be modeled depending on several parameters (transistor on-resistance,

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capacitance and inductance characteristics). A specific algorithm can be used to find out the optimal parameters and hence have a good estimation of the switching losses. Indeed, it is used to reduce the error between the experimental losses and the estimated losses for several biasing conditions. However, the method precision depends on the model accuracy as for the previous tests and may be dependent on the power bench design [212].

I.3.b.v Analytical Model

This method consists in inserting in the circuit the transistors equations modeled in its different regimes (on-state, off-state, semi-on-state) with its intrinsic capacitances [216], [217]. However, the difficulty is that the transistor equations are non-linear that makes their resolution really complex and even impossible. Therefore, for the circuit-level modeling, the equation has to be linearized by piece, which will insert some uncertainty in the final energy loss extraction.

I.3.b.vi Summary

For this PhD, a method enabling an easy, accurate and fast hard switching setup was required hence the calorimetric and the analytical one were rejected. The opposition method was not used because it is not suited for research purposes as detailed above. Experience in Ampere laboratory was available on another method similar to the DPT called Double Source Test (DST) as introduced in the study of Garrab *et al.* [218]. Therefore, this was the chosen setup for the study proposed in this manuscript. It has two advantages over the DPT:

- The voltage and the current source are independent → No need of different inductive loads to work with a constant step 2 timing in **Figure 33(b)**.
- There is no blocking stress as illustrated in the first step in **Figure 33(b)**. This means that even for stress-sensitive devices, the stress in the blocking phase (equivalent to step 3 in **Figure 33(b)**) is the only applied stress before the turn-on event. This is very important when studying the current collapse or $R_{ON,DYN}$.

Nevertheless, identified probes issues: impact on the switching characteristic and signal skewing have to be limited. In this PhD, it was limited by using high bandwidth probes and by compensating the propagation time as detailed in Annexe F.3.

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I.3.c Different Loss Extraction

The switching performance of a transistor can be evaluated through six different parameters at a given blocking voltage (V_{BUS}), on-current (I_{BIAS}), temperature, gate polarization ($V_{G,OFF}/V_{G,ON}$), gate resistance (R_G):

- The turn-off time $t_{OFF} = t_{d(OFF)} + t_f$ as described in **Figure 35** [219]
- The turn-on time $t_{ON} = t_{d(ON)} + t_r$ as described in **Figure 35** [219]

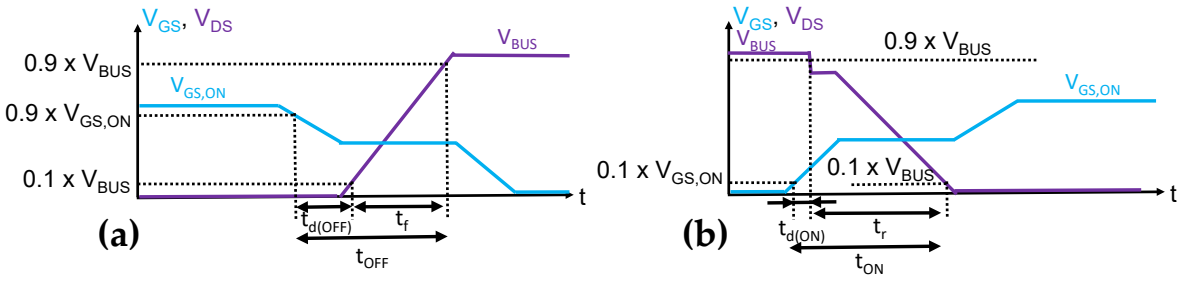

Figure 35: Switching time definition on the signal waveforms during (a) turn-off (b) turn-on.

- Current slew rate (off/on) $\left(\frac{dI_{DS}}{dt}\right)_{OFF/ON}$. This can be defined as the maximum of the derivative function [220].
- Voltage slew rate (off/on) $\left(\frac{dV_{DS}}{dt}\right)_{OFF/ON}$. This can be defined as the maximum of the derivative function [220].
- The turn-off losses E_{OFF}
- The turn-on losses E_{ON}

The two last parameters are the ones interesting for this PhD. They are commonly defined by the integral of the power $V_{DS} \times I_{DS}$ as shown in the following expression:

$$E_{OFF/ON} = \int_{t_{b,OFF/ON}}^{t_{e,OFF/ON}} V_{DS}(t) \times I_{DS}(t) dt$$

Equation 8: Generic turn-off/on energy [199] ($E_{OFF/ON}$: Turn-off/on energy; $t_{b,OFF/ON}$: integration beginning time; $t_{e,OFF/ON}$: integration ending time).

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The main issue is that there is a lot of beginning and ending time definitions as it was shown in the study of Keuck *et al.* [215] and reported in **Figure 36(a)** for semiconductor device companies. The small uncertainty on the extracted value for E_{OFF} and E_{ON} observed on SiC device (**Figure 36(b)** and **(c)**) are enhanced for 900 V GaN device due to the large oscillations' presence as shown in **Figure 36(d)** and **(e)**. This may be due to the use of the 1st generation of Transphorm™ cascode transistor (unique 900 V GaN device available at the time and still during the writing of this manuscript with the third generation [2]) known for complex switching. Thus, IEC 60747-9 standard will be used in this manuscript.

(a)

Standard	Turn-off		Turn-on	
	Start	End	Start	End
IEC 60747-9 (1998)	v_{ds2} at 10% V_1	i_{s2} at 2% i_L	i_{s2} at 10% i_L	v_{ds2} at 2% V_1
IEC 60747-8 (2010)	v_{ds2} at 10% V_1	i_{s2} at 10% i_L	i_{s2} at 10% i_L	v_{ds2} at 10% V_1
Mitsubishi (F series) [6]	v_{ds2} at 10% V_1	i_{s2} at 10% i_L	i_{s2} at 10% i_L	v_{ds2} at 10% V_1
Infineon [7]	v_{ds2} at 10% V_1	i_{s2} at 2% i_L	i_{s2} at 10% i_L	v_{ds2} at 2% V_1
ABB [8]	at 90% $v_{gs,on}$	10…20 µs after start	at 10% $v_{gs,on}$	10…20 µs after start
Wolfspeed [9, cf.]	v_{ds2} at 0% V_1	i_{s2} at −10% i_L	i_{s2} at 0% i_L	v_{ds2} at −10% V_1
E-Step Rule	at 5% V_1	when $dE/dt < 0.5\% V_1 I_L$ after first power peak	at 95% V_1	when $dE/dt < 0.5\% V_1 I_L$ after first power peak

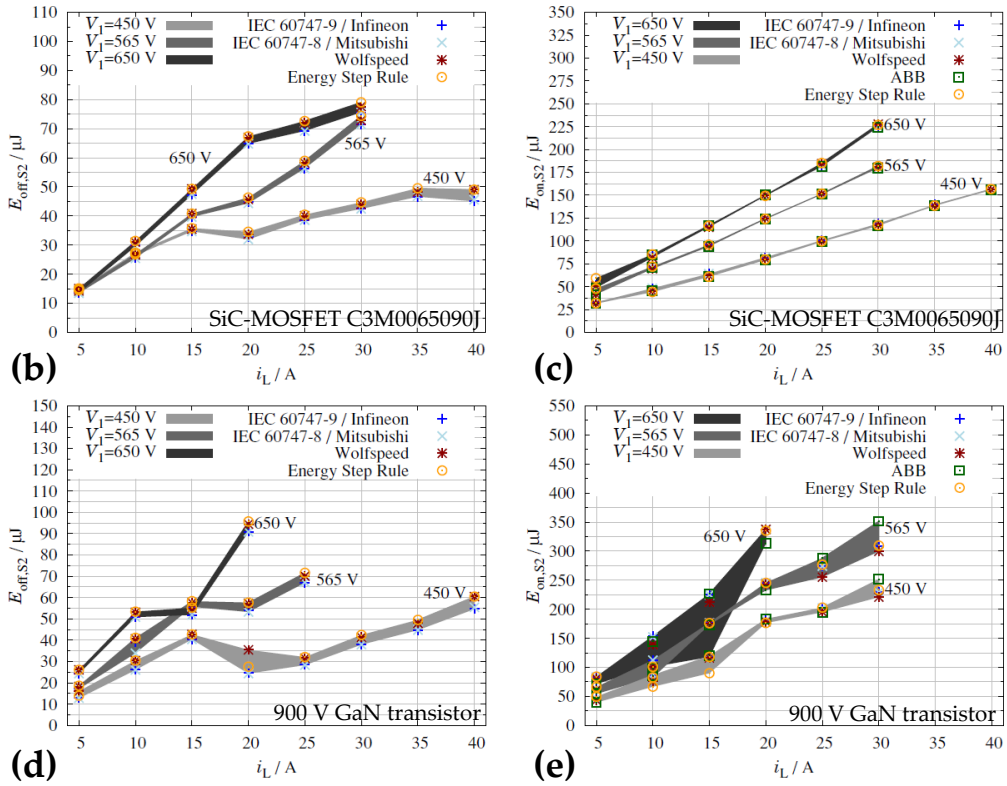

Figure 36: (a) Integration limits definitions reported by Keuck *et al.* [215]; (b) Extracted E_{OFF} (c) Extracted E_{ON} from the DPT at 75°C of a SiC device [215] (d) Extracted E_{OFF} (e) Extracted E_{ON} from the DPT at 75°C of a GaN device [215].

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Conclusion

Within this first chapter, the properties of wurtzite GaN (high critical electric field and a high mobility reached in a 2DEG at the heterojunction in between two piezoelectric materials: $Al_{1-x}Ga_xN$/GaN) were shown to be very interesting to manufacture lateral power devices (diodes and transistors).

The resulting Schottky diode as well as the different normally-off transistor architectures were presented. A brief introduction of their different specific building blocks (epitaxy on a foreign substrate, MIS Gate, Schottky and ohmic contacts) focused on the technology developed at CEA LETI was given to be more familiar with the devices studied in the rest of the manuscript. Moreover, the wide range of possible applications (consumer, automotive, industry, photovoltaic, more electric aircraft) was described as well as the advantages of GaN devices with respect to the vertical Si and SiC counterparts (negligible Q_{RR}, lower $R_{ON} \times C_{OSS}$, lower $R_{ON} \times Q_G$) for these specific applications.

Nevertheless, it was shown on the $R_{ON,SP}$ vs BV figure of merit that the transistor performance was far from the theoretical expectation proposed by Gaska *et al.* [89]. This is probably due to the electric field management, which will be the first tackled topic of this manuscript. Thus, the different architectural elements that were shown to improve the breakdown voltage (field plate, PSJ, LCL, buffer engineering, substrate removal) were presented to place the field plate structure used at CEA LETI among the other existing solutions. The different techniques to probe or evaluate the electric field in order to point out the breakdown device limitations without device degradations were presented. Only the TCAD simulation tools were shown to be adapted for the field plates and passivation structure of the CEA LETI power devices. This tool will be discussed in detail and the beginning of a calibration method will be proposed in the third chapter. This will be preceded and referenced by the experimental destructive study performed in the second chapter to identify the breakdown device limitations.

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To finish, the last subpart was dedicated to the loss definitions and the switching test bench. It was emphasized that in this manuscript, only losses related to the transistor ($E_{I/V}$ and $E_{OSS/qOSS}$) will be studied (in the fourth chapter) by means of a Double Source Test bench developed during this PhD. Indeed, the other available tests are either not adapted to research purpose or to soft switching losses or are not accurate enough. Thus the loss extraction will be done by integrating the product $V_{DS} \times I_{DS}$ during the switching period (turn-on and turn-off) with the time limitation defined by the IEC 60747-9 standard.

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Chapter II
Experimental Study of the High Voltage Limitations of AlGaN/GaN-on-Si Schottky Barrier Diode

This chapter is dedicated to the identification of the breakdown voltage limitation in the AlGaN/GaN-on-Si Schottky barrier diode. At first, an overview of the breakdown mechanisms reported in the AlGaN/GaN power device literature will be presented. In the second part, the different breakdown modes that can be identified in the studied devices will be introduced. Then, the different breakdown modes (vertical and lateral) will be analyzed with respect to their temperature, layout and epitaxial dependence. A failure and physical analysis will be presented to show the breakdown location in all the different configurations and regimes presented in the second part. This study will be used as a reference for the simulation study proposed in the third chapter and will give perspectives in terms of design (layout, epitaxy) optimization.

Outline

Chapter II Experimental Study of the High Voltage Limitations of AlGaN/GaN-on-Si Schottky Barrier Diode 54

II.1 Breakdown Analysis in AlGaN/GaN Devices for Power Electronics 56

II.1.a Literature Review: AlGaN/GaN Power Devices Lateral Breakdown Analysis 57

II.1.a.i AlGaN/GaN Schottky Diodes Lateral Breakdown Analysis 57

II.1.a.ii Complementary Techniques and Studies in Breakdown Analysis of AlGaN/GaN High Electron Mobility Transistors 63

II.1.a.iii Summary 67

II.1.b Literature Review: Vertical Breakdown Mechanisms 68

II.1.b.i Literature Hypothesis 68

II.1.b.ii Main Identified Dependence 71

II.2 The Identification of the Two Breakdown Modes by the Substrate Connection Dependence on the Breakdown Voltage 73

II.2.a Experimental Protocol 73

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II.2.a.i Samples Description 73
II.2.a.ii Electrical Characterization Procedure 75
II.2.b Experimental Results 75
II.2.b.i Diodes Leakage Trends and Contributions 75
II.2.b.ii Breakdown Voltage Extraction in the Different Configurations as a Function of the Anode-to-Cathode Distance 77
II.3 Device Limitations with a Floating Substrate 81
II.3.a Method Description and Experimental Presentation 81
II.3.a.i Method Description 81
II.3.a.ii Experimental Presentation 82
II.3.b Experimental Results 86
II.3.b.i Long Anode-to-Cathode Distance Devices 86
II.3.b.ii Short Anode-to-Cathode Distance Devices 89
II.3.b.iii Summary 94
II.4 Device Limitations with Grounded Substrate 96
II.4.a Method Description 96
II.4.b Experimental Results 97
II.4.b.i General Trends 97
II.4.b.ii Failure Analysis for Every Identified Categories 99
II.4.b.iii Summary 103
Conclusion 104

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II.1 Breakdown Analysis in AlGaN/GaN Devices for Power Electronics

Breakdown and degradation mechanisms identification in power devices have always been a challenge to push further their voltage ranges and their reliabilities. The lateral AlGaN/GaN power devices follows this trends as illustrated by the different reviews proposed by the Padova university team [221]–[223]. It is known that they can be split into two different breakdown modes as illustrated in **Figure 37**: the lateral breakdown mode that will be presented in a first part (focusing our attention on Schottky diodes) and the vertical breakdown mode (drain-substrate in the case of transistors and cathode-substrate for Schottky diodes) that will be dealt with in a second part.

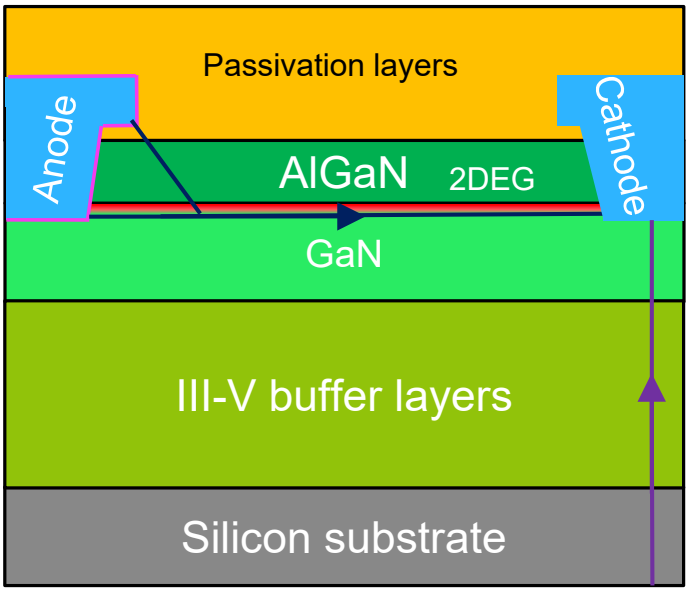

Figure 37: Potential current leakage path during the lateral breakdown (dark blue) and vertical breakdown (purple) for a generic AlGaN/GaN lateral Schottky diode with the substrate connected to the anode.

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II.1.a Literature Review: AlGaN/GaN Power Devices Lateral Breakdown Analysis

In the literature, the main part of the breakdown analysis has been performed on transistors, as it has been summarized in the study of Cai *et al.* [224]. Nevertheless, as Schottky diode is the studied device, the first part of this literature review will be focused on it. The second part will be focused on the additional characterization techniques used in transistor studies as well as a specific transistor study performed on transistors interesting for this chapter.

II.1.a.i AlGaN/GaN Schottky Diodes Lateral Breakdown Analysis

To this day, three different methods are used to analyze the Schottky diode breakdown voltage variations: the experimental Constant Voltage Stress (CVS) coupled with TCAD simulation method, the breakdown voltage scalability comparison method and the TCAD-simulations-based studies. They will be detailed in the next sub-sections.

II.1.a.i.1st The Experimental Constant Voltage Stress (CVS) Coupled with TCAD Simulation Techniques

This method was proposed and used in many studies performed by the Interuniversity MicroElectronics Center (IMEC) team [154], [225]–[227]. Their study was focused on Schottky diodes having a Gated Edge Termination (GET) technology. This specific diode architecture is illustrated in **Figure 38(a)**. It is characterized by its Schottky contact, which is built by partially recessing the AlGaN barrier. The GET termination: usually a Silicon Nitride (SiN) is then deposited and shaped on its extrema not to touch the ohmic contact. This dielectric is opened (with a length called L_{SC} in **Figure 38(a)**) to form the Schottky contact after metal deposition. This GET dielectric prevents excessive leakage current that may occur at the edge of the Schottky contact.

† **Method description**

After having determined in the study of Hu *et al.* that this specific technology was limited by a Time Dependent Dielectric Breakdown (TDDB) [154] (detail on the physical phenomenon provided in Annexe A.1), the following 3-steps method has been used to compare different technological parameters:

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- Step 1: Perform an electrical breakdown voltage measurement test at high temperature or at every tested temperature as shown in **Figure 38(b)** (in which the test was performed at 150°C). The purpose of this is to determine the voltage used in the next electric test.

- Step 2: Perform a Constant Voltage Stress (CVS) on non-already tested devices. The chosen voltage is slightly lower than the breakdown voltage determined in the previous steps. The test consists in applying a constant voltage stress in reverse mode and monitoring the leakage current until the breakdown occurs as illustrated in **Figure 38(c)**. The test is performed at high temperature to reduce the time required to break the devices. The obtained time to breakdown t_{BD}: stress time for which the current skyrockets in **Figure 38(c)**, is used afterward within a Weibull distribution to characterize the breakdown. This distribution is characterized by a characteristic time τ (roughly equals to 50 s and 2000 s for the REF and THIN PASS structure respectively in **Figure 38(c)**) and a shape parameter β. Details on the Weibull analysis are provided in the Annexe A.2.

- Step 3: Compare the impact of the technological parameter in TCAD simulations on their electric field distribution differences to justify the difference of the extracted τ at the previous step as shown in **Figure 38(d)**.

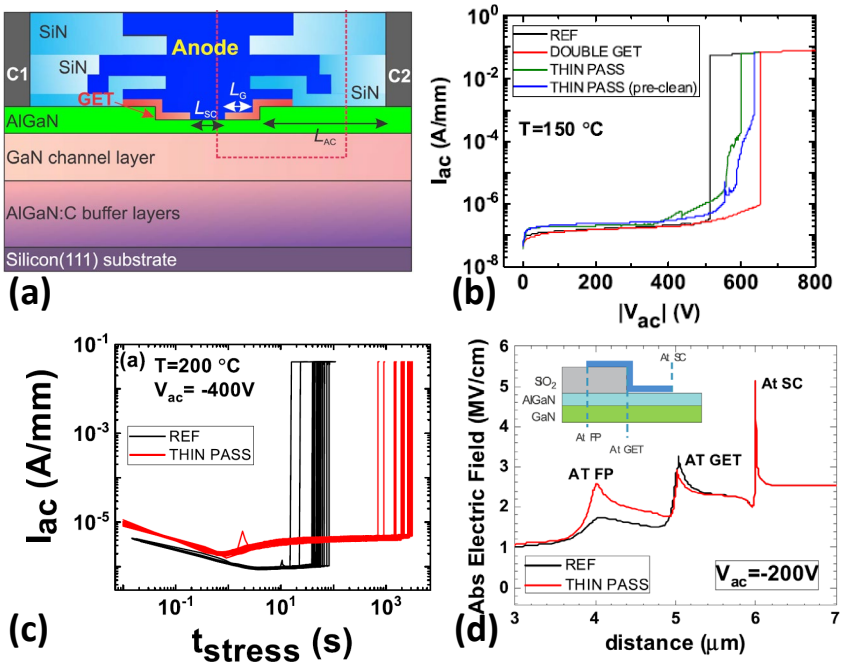

Figure 38: (a) Gate Edge Termination (GET) architecture schematic cross-section [228] (b) Current versus voltage characteristics in reverse mode until breakdown comparing different passivations at 150°C [227] (c) Constant Voltage Stress (CVS) comparing two passivation thicknesses at 200°C [227] (d) TCAD simulation of the electric field in the AlGaN comparing two passivation thicknesses at -200 V [227].

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† **Technological studied parameter**

With this method, the IMEC team has studied the impact of:

- Capping layers (layer in between the AlGaN barrier and the "path dielectric" made with SiO_2) [225], revealing that it is better to use a SiN rather than a GaN capping layer.
- Passivation thickness and GET dielectric constant [226], [227], demonstrating that reducing the passivation made with SiO_2 illustrated in **Figure 38(d)** or adding a second GET dielectric increases the device lifetime. Both results are explained by the electric field smoothing in TCAD simulation.
- Passivation process quality [227], demonstrating that the process choice (treatment before the GET dielectric deposition) can improve the reliability of the device.

† **Method limitations**

The method is pretty effective to compare the reliability in between two technological choices and estimate the technology lifetime (as illustrated for gate dielectric lifetime estimation of HEMT transistor in [229]). However, the limitation is that the breakdown location is not accurately found. In fact, the TCAD simulations are used only to verify if the electric field changes are coherent with the experimental breakdown. This means that TCAD tool is used only to assess how is the electric field changing as a whole and not at a specific place.

II.1.a.i.2nd The Comparison of the Breakdown Voltage Scalability

A widely-known method to compare the breakdown capability between two diode architectures or layout is to weigh up their breakdown voltage as a function of the anode-to-cathode distance: L_{AC} characteristics [228], [230]–[238]. The best illustration of this method was performed on a fully recessed anode and cathode Schottky Barrier Diode shown in **Figure 39(a)** [230]. Its breakdown voltage scalability has been experimentally tested with anode-to-cathode distance ranging from 5 to 30 µm as shown in **Figure 39(b)**. In this figure, the performance of this study has been compared with on the one hand, the literature values and on the other hand, the theoretical breakdown voltage expectation assuming that the lateral electric has a non-ideal distribution: triangular-shaped electric field distribution characterized by a $\beta = 0.5$ Gaska factor (described in I.1.b.i.2nd). To be more specific, the electric field is equal to the theoretical GaN critical electric field: $E_{C,GaN}$ of 3.3 MV/cm [10] at the anode and linearly decreasing up to be null at the cathode.

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Comparing curves in **Figure 39(b)**, the proposed diode (red curve) is better than some articles in the literature (blue, yellow and pink curves) and closer to the non-ideal model (green curve). However, this is still far from the theoretical model. Another way to assess electric field distribution non-ideality is to calculate the slope of the curve of **Figure 39(b)** and compare it with theoretical GaN critical electric field as shown in some articles (especially in the transistor literature) [183], [228], [239]. For instance, the ideal triangular shape has a slope of 1.7 MV/cm ($\beta \times E_{C,GaN}$).

To extend the bibliography on the transistors, according to the TCAD simulation of Chen *et al.* [240], impact ionization could be (because no experimental proof) one of the breakdown mechanisms responsible for this regime. Consequently, the breakdown voltage, in this study, has been shown to be dependent on the GaN layer doping level.

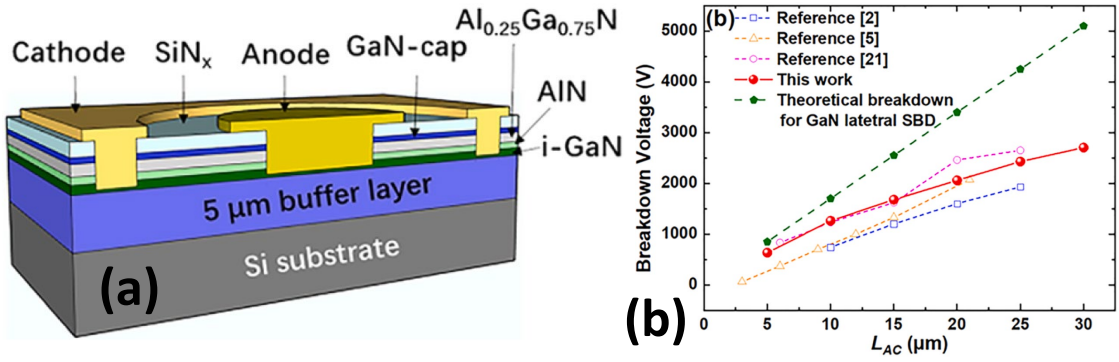

Figure 39: (a) Fully recessed Schottky Barrier diode schematic cross-section [230] (b) Breakdown voltage as a function of the anode-to-cathode distance (with a triangular-shaped electric field distribution assumed in the model) [230].

This method has been used to study, the impact on the breakdown voltage of:

- The device architecture choice [231]
- The field plate layout [232], [237], [238]: with or without first field plate [232], [238] & with or without second field plate [237]. Without surprise, adding a field plate is beneficial
- Anode recess [233], [236]. Depending on the diode layout, it worsens or improves the breakdown voltage capability.
- A specific surface treatment under the first field plate [236] that reduces the leakage current by limiting the electric field at the contact increasing the breakdown voltage
- p-GaN contact length in a hybrid-anode diode (architecture not detailed here) [234]

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If a sufficiently wide range of anode-to-cathode distances is used, two different regimes can be seen in the breakdown voltage versus anode-to-cathode distance characteristics as illustrated in **Figure 40(b)** for the diode shown in **Figure 40(a)**.

For a floating substrate configuration, as shown in **Figure 40(b)**, two different regions can be identified: a pseudo linear part (at low anode-to-cathode distance and studied as exposed before) and a saturation (at larger anode-to-cathode distance). These two regimes were analyzed in the study of Jiang *et al.* with Emission Microscopy (EMMI) to observe breakdown leakage-induced hot spots [238]. The hot spot visible from the anode to the cathode in **Figure 40(c)** made them confirm the hypothesis of a lateral breakdown. Whereas the spot visible at the anode in **Figure 40(d)** made them assert that the breakdown was vertical (as proposed by Visalli *et al.* [241] and confirmed by the TCAD simulation of Shen *et al.* [240] for AlGaN/GaN HEMT) and initiated at the GaN surface. It can be noted that a lateral hypothesis for this regime will be shown in this chapter. To be exhaustive, the saturation can be prevented by the substrate full or partial removal as initially shown by Visalli *et al.* [182]–[184], [242]. However, the static on-state resistance increases [183], [242], [184].

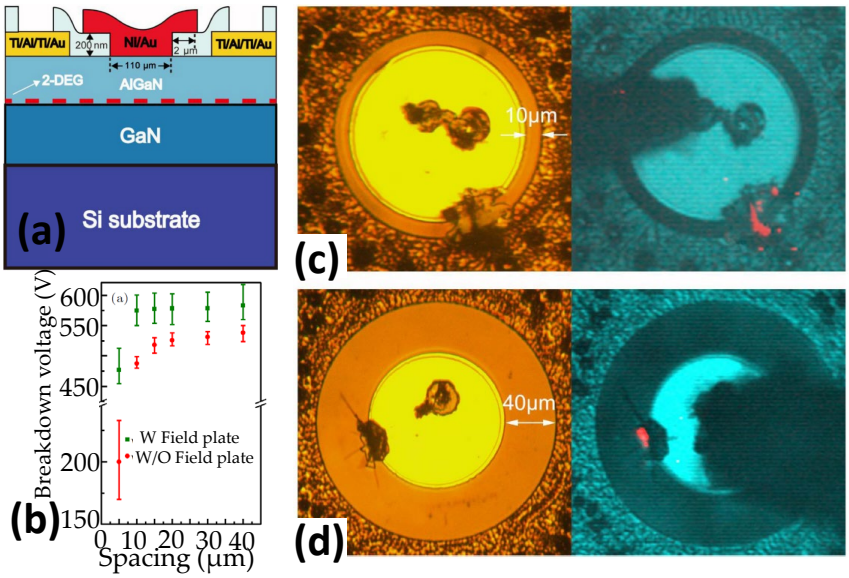

Figure 40: (a) Schottky Barrier diode schematic cross-section [238] (b) Breakdown voltage with a floating substrate as a function of the anode-to-cathode distance with and without field plate (adapted from [238]) (c) & (d) Optical microscope (on the left) and EMMI (on the right) images of Schottky barrier diode after breakdown (broken with a floating substrate) having an anode-to-cathode distance of 10 µm and 40 µm respectively [238].

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II.1.a.i.3rd TCAD Simulation Studies

The last method relies only on the TCAD simulations [243], [244] and focused on the influence of doping impurities/impurities in the epitaxial layers but also on the passivation layers [245].

This method has been used to study, the impact on the breakdown voltage of:

- The Magnesium doped back barrier parameters (distance to the 2DEG, doping concentration, doping dispersion) [244]
- The carbon donor traps compensation ratio [243] on the structure as shown in **Figure 41(a)**. The simulation clearly shows that the electric field even at the surface depends on the trap properties in the buffer. Thus, special care must be taken to them when doing TCAD simulation. However, as no reference has proposed to calibrate the buffer traps, it may explain why no deep interpretation on the electric field value or on the electric field change at a specific point in the structure was made.
- Using high permittivity dielectric among passivation layers [245]. It is used below field plate(s) to increase the electrostatic effect of the above field plate(s) and thus change the electric field management.

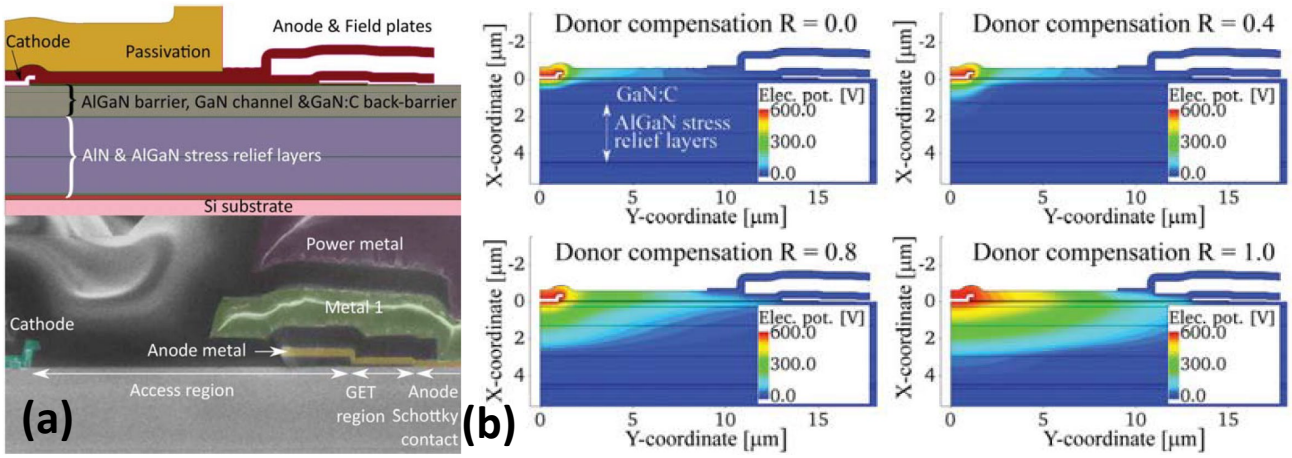

Figure 41: (a) Schottky Barrier diode schematic cross (top) and the corresponding scanning electron microscope picture (bottom) [243] (b) Electrostatic potential mapping obtained for different compensation ratios in the trap buffer [243].

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II.1.a.ii Complementary Techniques and Studies in Breakdown Analysis of AlGaN/GaN High Electron Mobility Transistors

Some interesting electrical and physical failure analysis techniques were used for transistors only. These techniques will be presented here because some of them will be used in the chapter. In addition the impact of the substrate connection on transistor will be introduced as similar result will be presented in the study performed on Schottky diodes.

II.1.a.ii.1st Electrical Failure Analysis Techniques

Lock-in thermography (LiT) is a complementary technique to the previously discussed EMMI for defects detection. Indeed, it allows detecting a different wavelength range. Here is a precision on their characteristics:

- Emission Microscopy (EMMI) or Photon Emission Microscopy (PEM): from 400 nm to 1100 nm → Visible to near-infrared if they use silicon-based Charge Coupled Device (CCD) camera [246] or from 0.9 µm to 1.7 µm if they use Indium Gallium Arsenide (InGaAs) sensors [246]

This method can detect ElectroLuminescence (EL) phenomena as shown in **Figure 42(a)** due to either the hot electron detection or the generation of defects as schematized in **Figure 42(b)**.

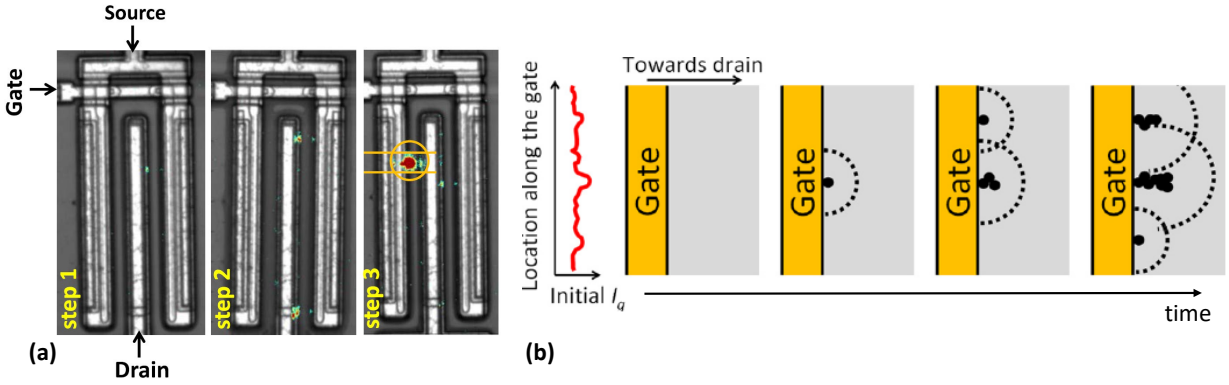

Figure 42: Electroluminescence images at different stress times (breakdown at step 3) for a transistor biased at V_{GS} = -5 V and V_{DS} = 600 V [247] (b) Schematized defects formation associated with the gate leakage increase during the stress (taken and adapted from [248]).

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- Lock-in Thermography (LiT): from 3 µm to 5 µm [249] → Far infrared if they use Indium Antimonide (InSb) sensors [246] or from 7.5 µm to 13 µm [250] → Far infrared

The last technique was used once in the GaN literature to inspect the failure of packaged devices as shown in **Figure 43(a)** and **(b)** [251]. It reveals that the failure was not related to the package but rather to the semiconductor device itself as shown in **Figure 43(c)** and **(d)**. Details about the LiT techniques are given in part II.3.a.

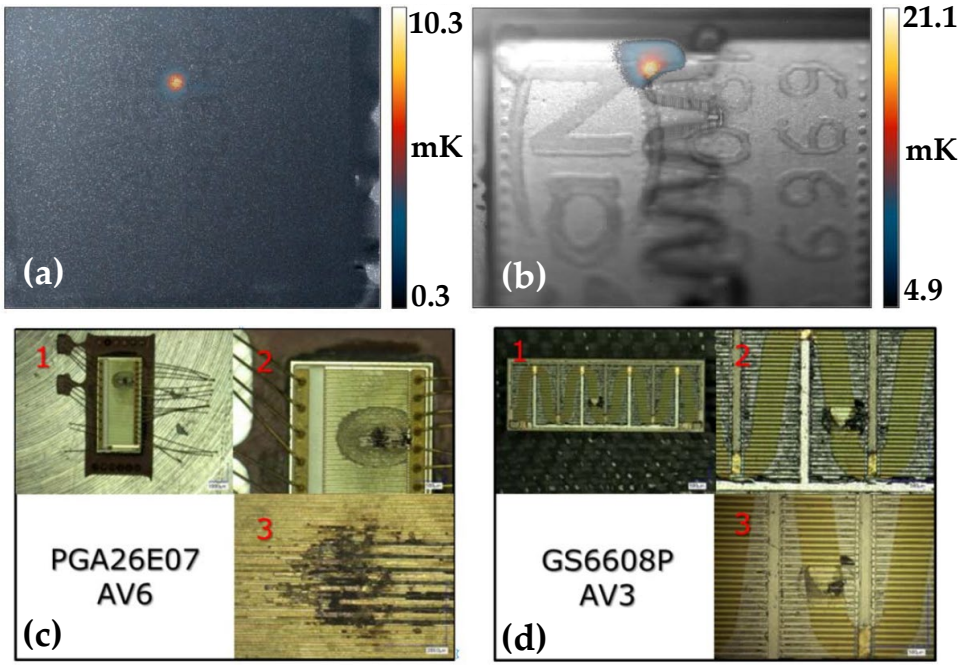

Figure 43: Lock-in thermography of packaged devices from (a) Panasonic™ [251] and (b) GaN Systems™ [251]. Microscopy images of the device failure (c) Panasonic™ [251] and (d) GaN Systems™ [251].

II.1.a.ii.2nd Physical Failure Analysis Techniques

In the transistor literature, breakdown locations are inspected thanks to two electron microscopies.

- Scanning Electron Microscopy (SEM). It was used to inspect surface degradation caused by Electrostatic Discharge (ESD) of Radio Frequency (RF) HEMT [252] or after fast cyclic test [253]. However, it can also be used to observe device cross-section with a resolution below the 100 nm range thanks to the use of a Focused Ion Beam apparatus as explained in Annexe B.2.

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- Transmission Electron Microscopy (TEM). It was used to report a dielectric breakdown between the drain edge of the gate as shown in the picture in **Figure 44(a)** with the simplified schematic in **Figure 44(b)** after the failure place detection by EMMI [247]. It was also used to observe the epitaxial degradation caused by cycling tests [253]. It is more time-consuming than the previous one (due to the sample preparation) and used to probe a very specific region (ten of nanometers wide) of the transistor. The best illustration is the gate drain-edge inspection shown in the picture in **Figure 45(b)** of a transistor having a gate-injection degradation (degradation mechanism schematized in **Figure 45(a)**).

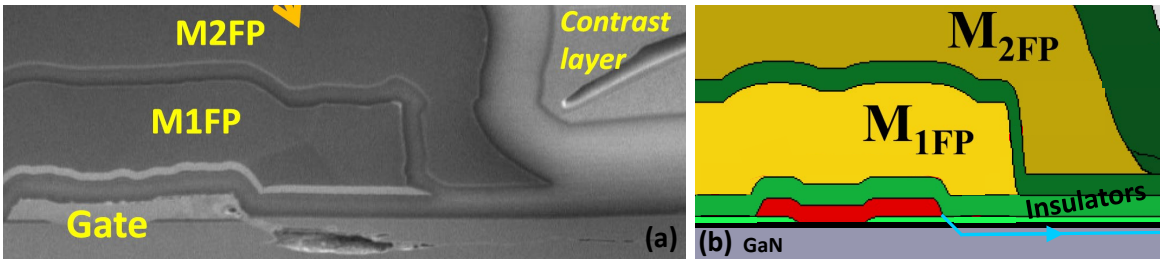

Figure 44: (a) TEM observation of the broken transistor (taken and adapted from [247]) (b) Schematized cross-section with the conductive path from the gate field plate corner to the GaN layer in cyan (taken and adapted from [247]).

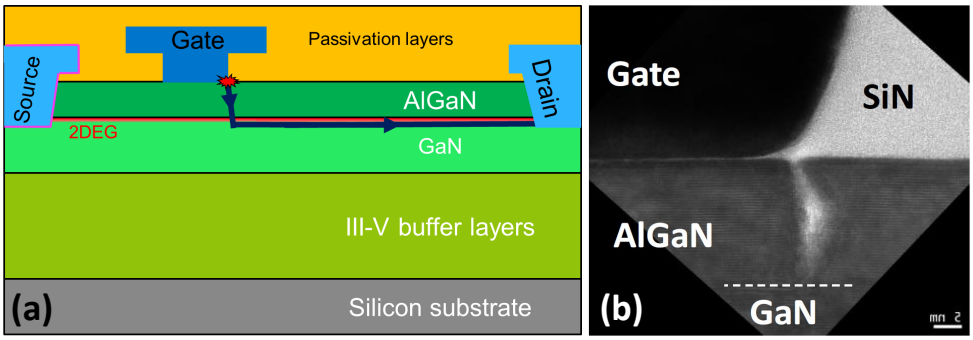

Figure 45: (a) Schematic of a gate injection breakdown with the current flow (b) TEM picture of the gate Schottky contact corner [254].

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II.1.a.ii.3rd The Substrate Connection Impact on the Transistor Breakdown Voltage

The impact of the substrate connection on the transistor breakdown voltage has been studied in the study of Zhang *et al.* [255] and Tang *et al.* [256]. In their studies, they have demonstrated that by keeping the substrate floating, the breakdown voltage could be improved as illustrated in **Figure 46(a)**. In the case for which the vertical current through the entire epitaxy is symmetric with respect to the voltage bias, Zhang *et al.* [255] revealed that the substrate potential is roughly equal to half the drain voltage as shown in **Figure 46(b)**. This indirect increase of the substrate potential (named auto-polarization) and its consequence will be observed for Schottky diodes in this manuscript (II.2.b.ii) justifying the presence of this subsection.

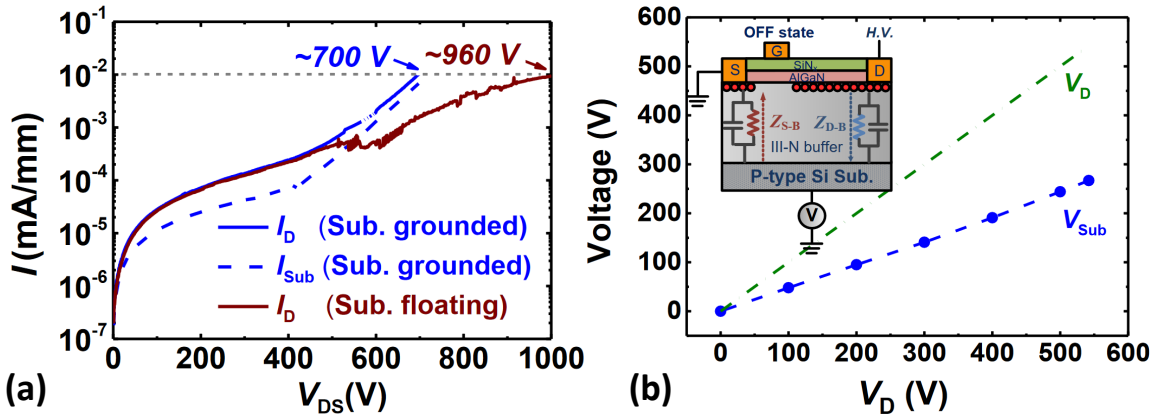

Figure 46: (a) Current versus voltage characteristics of a transistor in blocking mode until breakdown with and without grounded substrate [255] (b) Substrate and drain voltage measurements during the drain voltage sweep [255].

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II.1.a.iii Summary

In a nutshell, the lateral breakdown of lateral AlGaN/GaN Schottky Barrier Diode has already been investigated in the literature through experimental studies (based on CVS voltage stress and breakdown scalability) and TCAD simulation studies. The first experimental-based study was focused on the GET diode and that its reliability can be improved using SiN capping layers and a treatment pre-dielectric deposition as well as adjusting the passivation thickness [154], [225]–[227]. The second experimental method allows investigating the breakdown voltage difference between different diode architectures [231]. It was demonstrated that with a floating substrate, the breakdown voltage versus the anode-to-cathode distance characteristics exhibits two regimes. On the one hand, the first regime (at short distance) depends linearly on the distance and was studied as a function of the anode recess [233], [236], the field plate presence (higher breakdown voltage when having field plates) [232], [237], [238] and surface treatment (higher breakdown voltage when using a specific treatment before the anode metal deposition) [236]. On the other hand, a saturation (for long distances) was linked to a vertical limitation at the GaN surface under the anode. Another hypothesis will be proposed in this chapter to explain the saturation. Pure TCAD simulation studies showed that doping impurities/impurities in the epitaxy has to be accurately tailored for optimizing the electric field distribution.

Nonetheless, on AlGaN/GaN Schottky diode:

- No strict identification of the breakdown location was demonstrated yet for the two regimes identified in the breakdown versus the anode-to-cathode characteristics. This limitation will be addressed by using techniques presented in II.1.a.ii (Lock-in Thermography and FIB-SEM observations)
- The field plate presence was studied but the quantitative field plate length impact on the breakdown voltage has not been studied yet and will be in this chapter.
- Some of the epitaxial parameters (p-GaN back barrier doping, dispersion and distance to the 2DEG) have been studied in simulation but not experimentally. The impact of the back-barrier to 2DEG distance will be here studied experimentally to assess its quantitative impact on the breakdown voltage.

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II.1.b Literature Review: Vertical Breakdown Mechanisms

In the literature [101], [171], [253], [257]–[264], the vertical breakdown has been extensively studied and is the main limit to reach the 1200 V rated lateral GaN device.

In a first section, the vertical breakdown literature hypothesis will be presented before introducing the main factors involved in the vertical breakdown voltage value.

II.1.b.i Literature Hypothesis

Initially, the articles were focusing their attention on Direct Current (DC) or quasi-DC bias conditions as summarized in the first subsection. This constitutes the core of the available papers on the subject. However, two years ago, the Indian Institute of Science team led by Mr. Shrivastava demonstrated that the breakdown mechanism as well as the epitaxial estimated lifetime changes from DC conditions if the applied stress was closer to the application (pulsed stress). Thus, the second subsection will describe their findings.

II.1.b.i.1st Under DC Stress

To this day, it seems to be acknowledged that the breakdown exhibits a time dependence with a small temperature dependence (**Figure 47(a)**) and a strong electric field dependence (**Figure 47(b)**) as exposed in the paper of Borga [257].

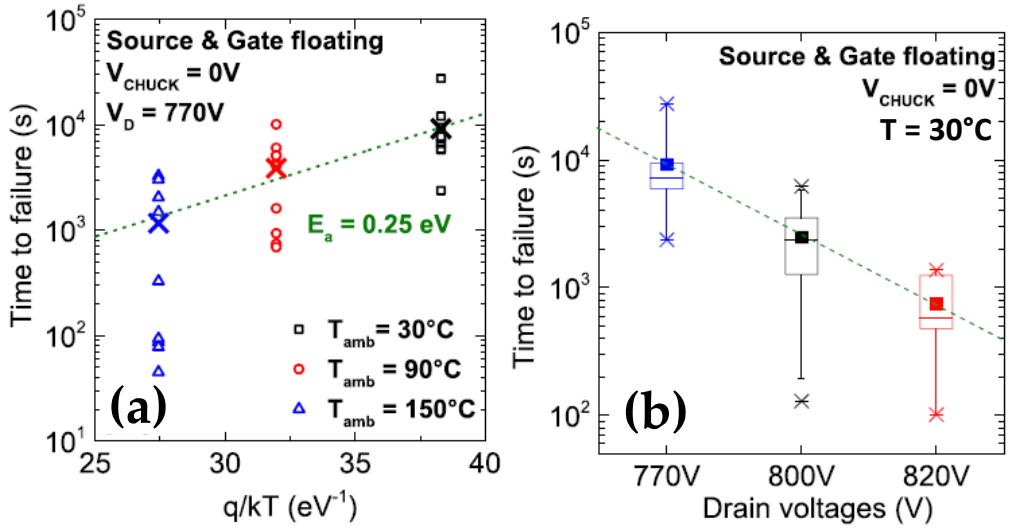

Figure 47: (a) Time to failure of a transistor vertical breakdown as a function of the temperature [257] (b) Time to failure of a transistor vertical breakdown as the vertical bias [257].

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However, there are two different hypotheses on the vertical breakdown locations as illustrated in **Figure 48(a)**:

1. At the Nucleation layer/Silicon interface as proposed by [171], [257], [258]. The study of Borga *et al.* [258], released in 2020, revealed that the AlN/Si junction could be modeled as a p-Si/n^+-Si/AlN junctions (in which the n^+ region models the inversion layer created at the AlN/p-Si interface). To summarize, it was shown that an avalanche occurs in the silicon substrate (near the interface). This avalanche provides more electrons than the thermal generation that limits the current in the region 2 in **Figure 48(b)**. Thus, the current should be limited by the electron injection at the AlN/Si interface. However, despite the huge advancement brought by this study, the author does not have shown the breakdown exact location. This is could be the case if no other junction appears in the epitaxy.

2. An avalanche in the GaN top layer. Indeed this was proposed with the TCAD simulation made by Cornigli *et al.* in [259]. This seems to be consistent with the high electric field in this region according to Borga *et al.* point of view in their 2017 article [257].

Therefore, there is nowadays no strong consensus on the breakdown location even though the last promising explanation seems the Borga's *et al.* one [258]. The task is especially hard since the breakdown destroys the sample preventing a post-breakdown physical analysis as shown in [171].

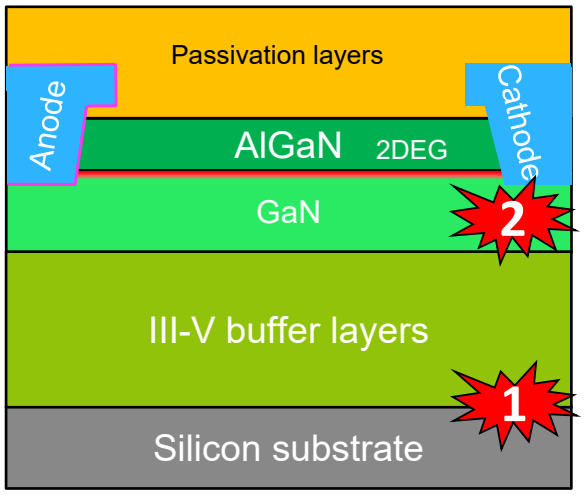

Figure 48: Diode cross-section schematics exhibiting the two different hypotheses on the vertical breakdown location.

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II.1.b.i.2nd Under Pulsed Stress

In 2020, the study of Shankar *et al.* in [253] revealed a new breakdown mechanism: fatigue due to a repetitive piezoelectric strain induced by a repetitive pulsed electric stress. Indeed, by stressing the device with a pulsed source (closer to the application), a strain accumulation in the device was discovered below the drain contact as it is enhanced by comparing the µ-Raman mapping (that probes the stress undergone by the crystal) in **Figure 49(a)** and **Figure 49(b)**. A part of the applied bias energy was lost into the creation of micro-cracks in the crystal lattice as illustrated in **Figure 49(d)**. Micro-cracks were spatially identified by means of Photoluminescence (PL) and were characterized in depth thanks to CathodoLuminescence (CL) in the article and shown with TEM images (not shown here). Those micro-cracks create additional conductive paths leading to the premature failure. This is different from a DC stress as enhanced by the comparison of µ-Raman mapping in **Figure 49(a)** and **Figure 49(c)**. Indeed, instead of the compressive stress accumulation under the drain contact, the DC stress causes a tensile strain in between the gate and the drain.

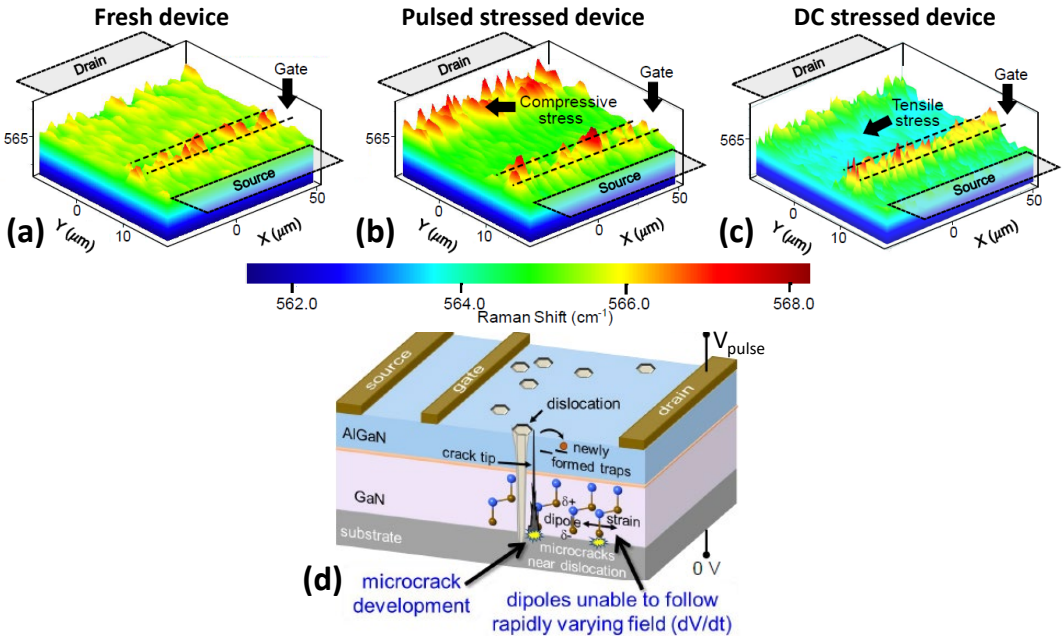

Figure 49: (a) µ-Raman mapping of transistor between the source and the drain for: (a) a fresh device (b) a device stressed with pulsed bias (c) a device stressed with DC bias (d) Transistor schematics showing the formation of micro-cracks (identified by PL, CL and TEM images) near the dislocation during the repetitive pulsed stress causing the device early failure (taken and adapted from [253]).

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II.1.b.ii Main Identified Dependence

Having described the different mechanisms leading to the vertical breakdown after a DC or pulsed stress, the main factors to improve the breakdown will be briefly introduced here (DC stress only because it has not been studied for pulsed stress).

II.1.b.ii.1st The Buffer Thickness and its Composition

First and foremost, the main criterion is the total thickness of the epitaxy. The thicker the epitaxy, the larger the electric field spreading at a given bias voltage [101], [261], [262]. This was especially presented in the study of Fabris *et al.* [261] as shown in **Figure 50(a)**. Indeed, the breakdown voltage has linear dependence with the Super Lattice (SL) thickness as well as the Carbon doped GaN (GaN:C) thickness. Furthermore, the breakdown can be improved by changing the epitaxial composition as it was demonstrated by Tajalli *et al.* in [263] as shown in **Figure 50(b)** in which the breakdown voltage has been improved by replacing a step-graded (SG) buffer (reference) by a Super Lattice even though the total epitaxial thickness was shrunk from 5.8 µm to 5.1 µm. The authors explained that this is due to the decrease in dislocation concentration and a reduced carbon incorporation that reduces the leakage through the epitaxy and thus increases the breakdown voltage.

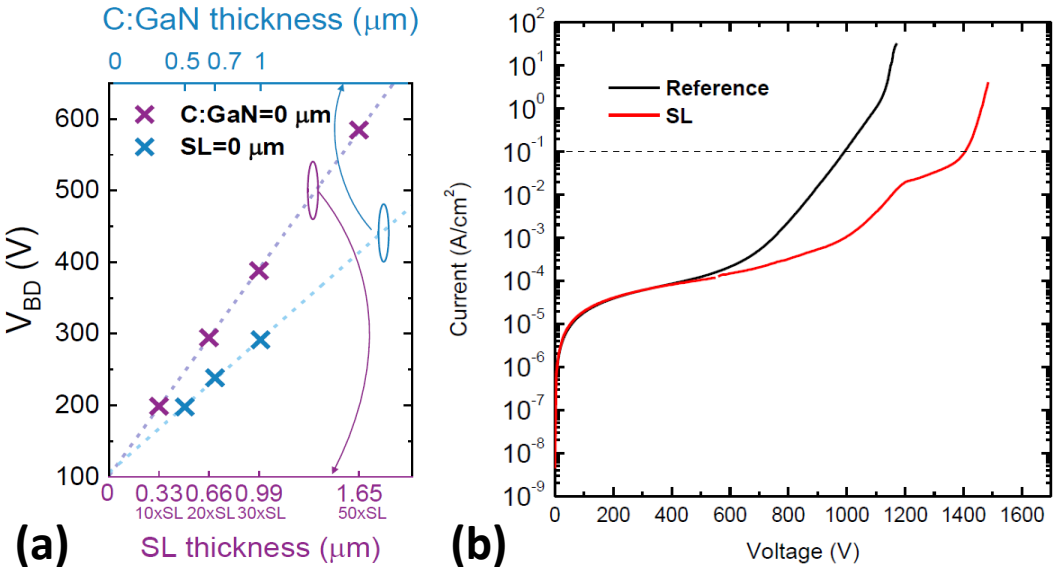

Figure 50: (a) Breakdown voltage as a function of the different epitaxial layer thicknesses [261] (b) Vertical leakage measurement made on two different epitaxies [263].

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II.1.b.ii.2nd The Substrate Properties

The properties of the substrate are also significant parameters that play a role on the overall vertical breakdown voltage. First, the increase of the substrate resistivity leads to a higher breakdown voltage as shown in **Figure 51(a)**. In fact, the voltage range (between V_{PL1} and V_{PL2}) in which the current is stable, increases with the resistivity because it increases the depletion region thickness increasing the voltage (V_{PL2}) at which avalanche occurs in the substrate [260]. The limit of this approach is that it creates back-gatting effects worsening the dynamic behavior of the transistor [260]. Second, p^+ region can be formed to increase the breakdown voltage as shown in **Figure 51(b)**. According to the authors, these regions block the edge current flow.

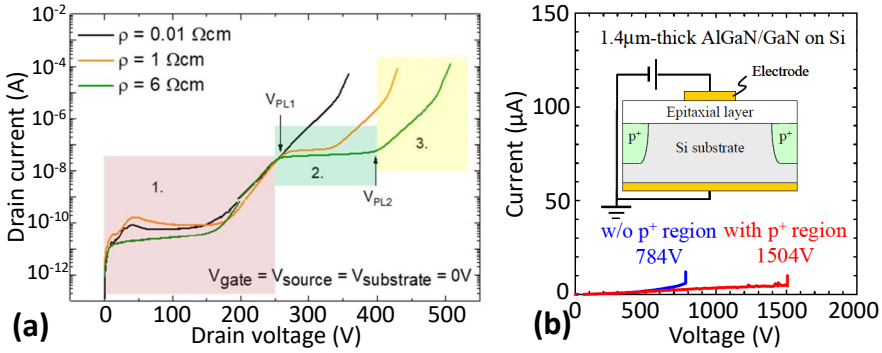

Figure 51: (a) Vertical leakage measurement made on three wafers with different resistivities [260] (b) Vertical leakage measurement made on wafer with or without p^+ implantation [264].

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II.2 The Identification of the Two Breakdown Modes by the Substrate Connection Dependence on the Breakdown Voltage

The breakdown mode depends on the buffer and layout optimization. This of course depends on the technology maturity as well as the design (architecture, layout, epitaxial) choice. Indeed a power device optimized for a 100 V rating on an epitaxy that can withstand 1000 V has more chances of being laterally than vertically limited in terms of Breakdown Voltage (BV). On the contrary, using a very long device on a 1000 V epitaxy would lead to a vertical limitation. In addition, depending on the substrate polarization or not, the leakage mechanism as well as the breakdown may be different.

Thus, this part is dedicated to the identification of the different breakdown modes in two different biasing conditions: substrate connected to the anode and floating substrate. The substrate connected to the cathode case has not been retained for its dramatic current collapse [265].

II.2.a Experimental Protocol

II.2.a.i Samples Description

To identify and understand the breakdown modes, the device itself (without layout consideration) must be described. It consists of a 650 V/ 6 A fully-recessed Schottky Barrier Diode meaning that the Schottky contact electrode as well as the ohmic one are in direct contact with the 2DEG as illustrated in **Figure 52(a)** [58]. To achieve 6 A, the diode has a specific width of at least 40 and up to 60 mm. The 3.9 µm epitaxy was grown on a (111)-oriented, 1 mm thick silicon substrate with a diameter of 200 mm. Its resistivity is between 3 and 20 Ω.cm. The Metal Organic Vapor Phase Epitaxy (MOVPE) was grown on an Aixtron® Crius® R200 tool. It is subdivided into three different parts. First, the nucleation layer and the following transition layers are forming the III-V buffer in **Figure 52(a)**. The second part is a carbon-doped GaN (GaN:C). Last but not least, the top heterojunction composed of an Unintentionally Doped GaN (UID) with an embedded Back Barrier (BB), AlN and AlGaN barrier layers. On top of this stack, Silicon Nitride (SiN) and Silicon Dioxide (SiO_2) are then deposited to make passivation layers in **Figure 52(a)**. The contacts

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as well as the field plate structure were formed with the use of several masks and etching steps. A metal deposition of Titanium Nitride (TiN) was used for the Schottky contact whereas the ohmic contact is made of a Titanium/Aluminum bilayer. The resulting structure forms four different field plates at the anode. Their lengths are called FPG0, FPG1, FPG2 and FPG3, whereas the cathode has only one field plate with a length named FPD.

In this part, the back-barrier in the epitaxy is the closest to the GaN:C as illustrated in **Figure 52(b)** (this will not always be the case in all the part of this chapter). This study was done by varying the device size (limited to the distance between the anode and the cathode: L_{AC}) from the smallest (16 µm) to the longest (30 µm) as shown in **TABLE 4**.

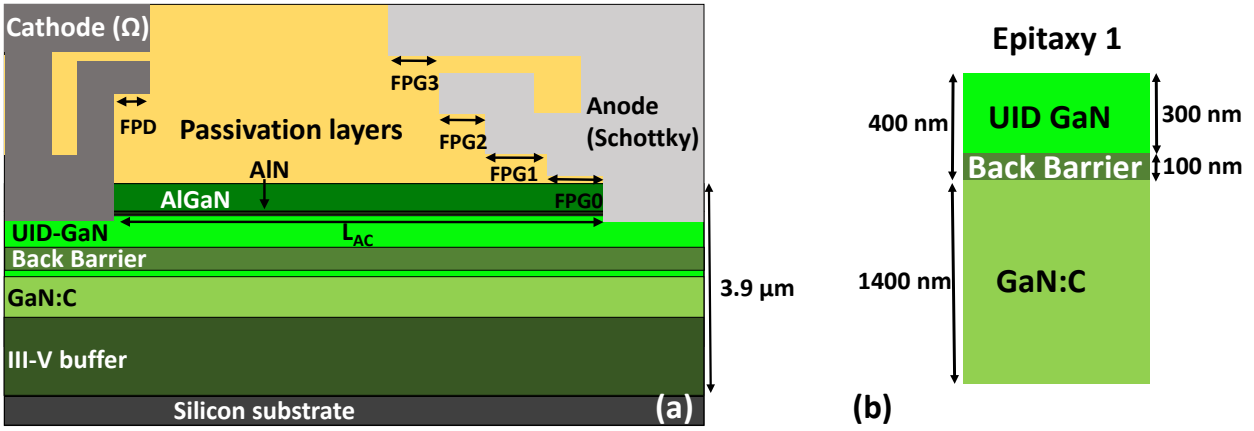

Figure 52: (a) Schematic cross-section of the Schottky diode with the most prominent layout parameters (L_{AC}, FPGx, FPD) (b) Schematic of the investigated epitaxial stack.

TABLE 4: Layout parameters for the different studied diodes (The variable parameter values are underlined and in bold).

Layout name	L_{AC} (µm)	FPG0 (µm)	FPG1 (µm)	FPG2 (µm)	FPG3 (µm)	FPD (µm)
LAC-16	**16**	2	2	2	2	0.5
LAC-20	**20**	2	2	2	2	0.5
LAC-25	**25**	2	2	2	2	0.5
LAC-30	**30**	2	2	2	2	0.5

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II.2.a.ii Electrical Characterization Procedure

The measurements were performed with a Keithley 2657A high power system sourceMeter® Source Measure Unit (SMU) Instrument.

To identify the breakdown modes for every device layouts presented in **TABLE 4**, three different biasing conditions were used. The first one was a pure vertical measurement in which the substrate was grounded and a positive bias is applied at the cathode while the anode was kept floating. The second one is a pure lateral measurement; meaning that the substrate is kept floating while the anode is grounded and a positive bias is applied at the cathode. The last but not the least configuration consists of short-circuiting the anode with the substrate. Thus, the vertical and horizontal leakage contributions are expected to be present in the current-voltage characteristic.

The breakdown voltage measurement consists of applying a voltage sweep with a step of 1 V until the compliance is reached. The compliance is set at 20 and 5 mA for connected and floating substrate respectively. The breakdown voltage is defined as the voltage before which the device reaches the compliance. It physically corresponds to an abrupt current increase.

II.2.b Experimental Results

II.2.b.i Diodes Leakage Trends and Contributions

In this part, the device general breakdown trends of the measurements for a given length (20 µm) are presented. In **Figure 53(a)**, the electrical characteristics of at least sixteen devices for each configuration are shown. The first noticeable thing is the sudden current jump occurring at voltage ranging from 200 V to 500 V. This corresponds to an abrupt change in the measurement range. This artefact makes the current level measurement wrong for voltages lower than the one at the abrupt change. However, the voltage stress should not be affected. The second noticeable thing is that the current level dispersion between dies is rather low on the rest of the characteristics whatever the biasing conditions. This allows, on the one hand, the identification of two outliers. Especially in the configuration with the anode and the substrate connected together as identified in **Figure 53(a)**. On the other hand, the current level comparison can be done on representative dies as displayed in **Figure 53(b)**.

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It can be observed that for this specific layout, the breakdown voltage in floating substrate configuration (green curve) is higher than the vertical one (blue curves). In addition, two main trends can be extracted from the current levels in the configuration with the short-circuited anode and substrate (red curves) with respect to the other two. Indeed, for voltage below 500 V, the curve matches the green curves corresponding to the lateral leakage. Whereas for voltages higher than 700 V to the breakdown at roughly 1100 V, the current level is superimposed with the vertical configuration.

Thus, by extrapolating the above observation, supposing that the vertical breakdown voltage will stay constant whatever the layout, it is clear that once the anode has been short-circuited with the substrate, the breakdown voltage will be the minimum between the vertical and the lateral one. In the next section, the breakdown mode prevailing for all the available device sizes will be analyzed.

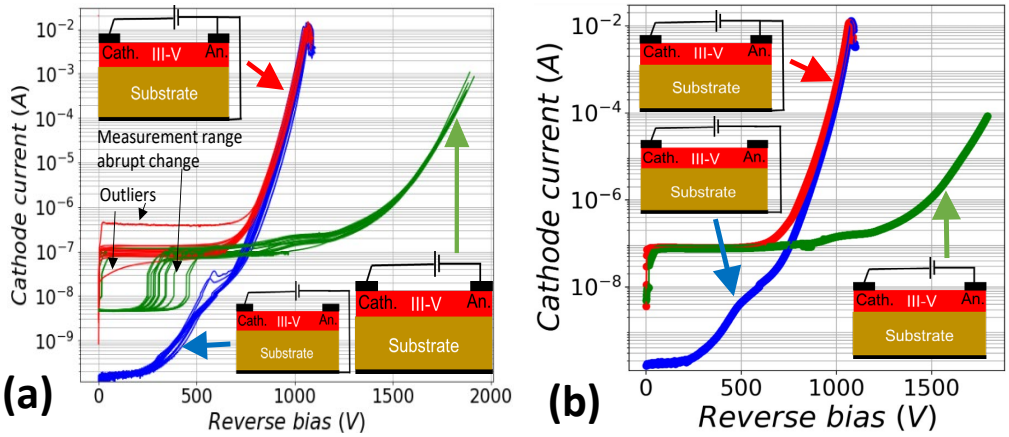

Figure 53: (a) Reverse characteristic of the diodes made with LAC-20 architecture of epitaxy 1 and W = 40 mm in different electrical configurations (sixteen devices per condition) (b) Typical reverse characteristic of the diode made with LAC-20 architecture of epitaxy 1 and W = 40 mm in different electrical configurations.

Finally, the most careful readers may have noticed the sudden current decrease just before the vertical breakdown in **Figure 53(a)** and **(b)**. The origin of this strange phenomenon has not been investigated in the PhD. However, the compliance-related hypothesis has been discarded by changing the compliance value to 100 mA in breakdown measurement as shown in **Figure 54**. It might be due to charge movements in the buffer that were identified by substrate ramping measurements [266], [267].

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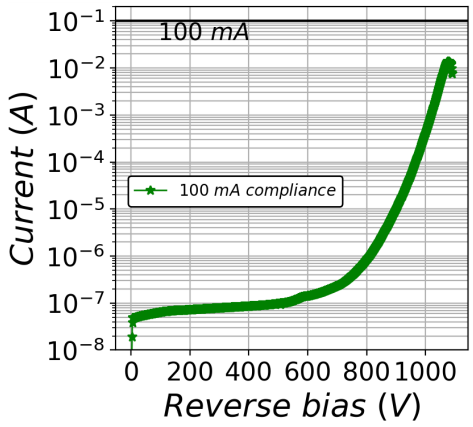

Figure 54: Breakdown measurements performed on a FPG0-3 architecture (W = 60 mm) on a wafer having the epitaxy 1 (The measurement point when the compliance was reached, has been removed).

II.2.b.ii Breakdown Voltage Extraction in the Different Configurations as a Function of the Anode-to-Cathode Distance

By extracting the breakdown voltage for each configuration and all the devices, the graph representing the breakdown voltage as a function of the cathode-to-anode distance can be displayed as in **Figure 55(a)**. It can be noted that for all the device sizes, the breakdown voltage with floating substrate is the highest. When the anode is tied to the substrate, the breakdown voltage (≈ 1100 V[3]) is the same as when the anode is left floating suggesting that it is limited by its vertical component. As it is circled in red, the first noticeable thing is the huge error bars for the devices having an anode-to-cathode distance of 25 µm and that were tested with floating substrate (green curve). By looking at the counting distribution as a function of the breakdown voltage displayed in **Figure 55(b)**, two distinct groups are visible and identified with the numbers in the figure. The largest one (numbered 2 in **Figure 55(b)**) is centered around 1950 V whereas the lowest (numbered 1 in **Figure 55(b)**) extends from 1550 V to 1700 V. To figure out the origin of this unexpected trend, the breakdown voltage as a function of the die placement on the wafers belonging to the analyzed split were plotted in **Figure 56**. It can be seen that the devices from distribution

[3] Assuming that the electric field is uniformly distributed within the GaN epitaxy, it corresponds to an average electric field of 2.8 MV/cm. It is smaller than the GaN critical electric field of 3.3 MV/cm meaning that there is room for improvement.

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one (red die in the figure) are mainly located on wafer #05. However, there is no preferential place (either at the center or at the wafer edges). In addition, their places are different from one wafer to the other and their voltage range is different. Finally, a more in-depth analysis of process variability is necessary to identify the cause of wafer #05 defectivity. As this analysis has not been performed, the elements of the distribution are considered as outliers, which gives the green curve a shape already observed in the literature [183], [239]–[241], [262], [268] for transistors and [269] diodes as shown in **Figure 57**.

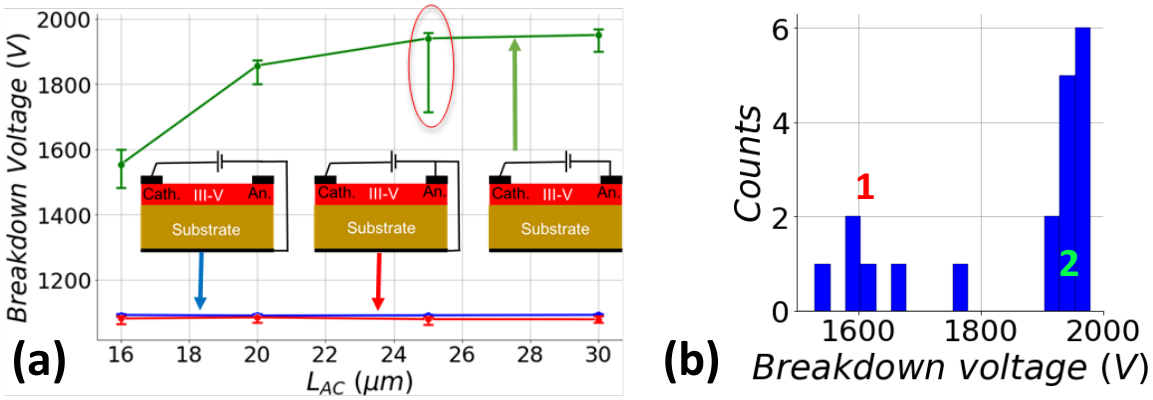

Figure 55: (a) Breakdown voltage as a function of the anode-to-cathode distance on epitaxy 1 (each point is the median of 8 devices with error bars represented by the first and the third quartile) (b) Breakdown voltage distribution depending on their values.

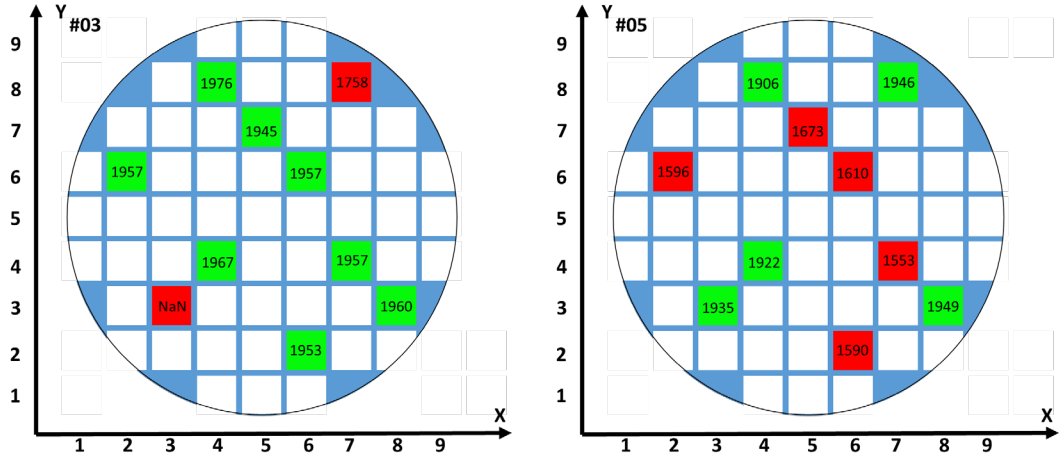

Figure 56: Breakdown voltage mapping on the two tested wafers (#03 and #05) having the epitaxy 1.

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Two different regimes can be identified as already seen in the literature:

- At low L_{AC}, a linear part can be seen for anode-to-cathode distance lower than 20 µm. As it depends on a lateral dimension, it is assumed to be a lateral breakdown. As previously presented in the state-of-the-art, some articles are extracting the linear slope [183], [228], [239] representing how non-ideal the electric field distribution is. The closest this slope is from the critical electric field, the more ideal is the electric field distribution (and the β factor presented in I.1.b.i.2nd will be closer to 1). In our case the slope cannot be extracted with few L_{AC} values in this regime (assuming that the 16 µm and 20 µm devices are fully in the linear regime, it would correspond to an average lateral electric field of 0.75 MV/cm which is far from the GaN critical electric field 3.3 MV/cm).

- At high L_{AC} a saturation part can be seen for an anode-to-cathode distance higher than 20 µm. As previously shown in the literature, the saturation should be limited by vertical conduction as proposed by Visalli *et al.* [241] and confirmed by the TCAD simulation of Shen *et al.* [240] and asserted by the study of Jiang *et al.* [238] presented in the state-of-the-art.

The breakdown voltage limitation in both regimes will be studied in detail in the following part (II.3).

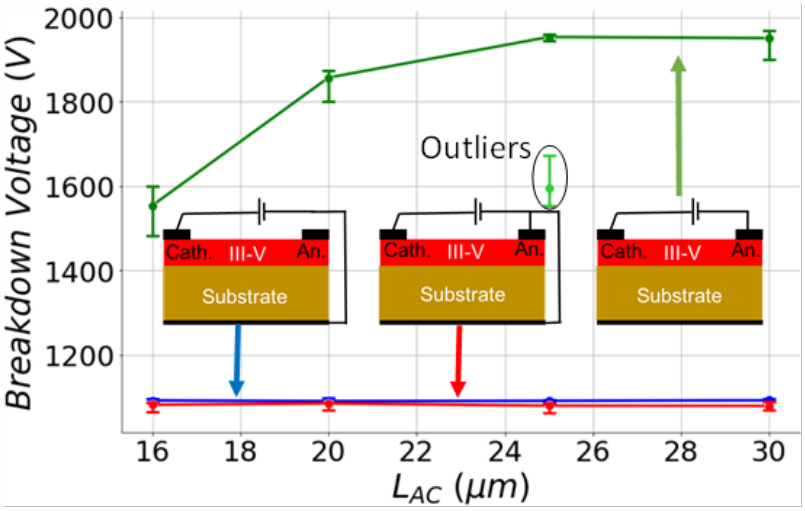

Figure 57: Breakdown voltage as a function of the anode-to-cathode distance characteristic on epitaxy 1 (each point is the median of 8 devices with error bars represented by the first and the third quartile).

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A last important thing is the fact that the breakdown voltage values (1500 V to 1950 V) are between one to two times its vertical limiting value of 1100 V. An auto-polarization of the substrate and buffer should occur and at least pusher further (to higher cathode voltage) the vertical device limitation (occurring when a voltage difference of 1100 V between the cathode and the anode happens) as already demonstrated in the transistor literature (II.1.a.ii.3rd). In fact, if there was no auto polarization, the substrate should stay at a voltage near zero volts because it is the initial voltage of breakdown measurements; hence, there would be a voltage difference between the substrate and the cathode leading unfortunately to a vertical breakdown.

In summary, in this part it was demonstrated that the device with the substrate connected to the anode is limited by the vertical breakdown whatever the available anode-to-cathode length. Moreover, it was strongly suggested that the leakage current before the breakdown has two major contributions: below 500 V, the lateral current has the main contribution whereas the vertical current is the major contribution up to the breakdown. When the substrate is floating the breakdown voltage is higher because the substrate auto-polarization relieves the vertical electric field under the cathode. Furthermore, by varying the device anode-to-cathode length, the different regimes in the breakdown voltage versus the anode-to-cathode distance were identified: the linear regime at small anode-to-cathode distance (expected to be limited by a lateral breakdown) and the saturation at long anode-to-cathode distance (expected to be limited by a vertical breakdown). The identification of the anode-to-cathode distance at which each regime occurs will be used to inspect the breakdown mechanism in both regimes in the following parts of the chapter.

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II.3 Device Limitations with a Floating Substrate

In this part, the two regimes identified previously in the breakdown voltage versus the anode-to-cathode characteristic when the substrate was floating (linear and saturation regime) will be deeply investigated. A methodology that was developed and followed to identify the breakdown mechanism and its location is presented. Moreover, the layout (field plate lengths) and epitaxial (back-barrier to 2DEG distance) dependence of the lateral breakdown with short anode-to-cathode distance will be studied here. This work is of high interest especially because it allows qualitatively gauging the effect of lateral electric field on the breakdown voltage.

II.3.a Method Description and Experimental Presentation

II.3.a.i Method Description

To perform the analysis, the methodology described in **Figure 58** was followed. It begins with the electrical characterization at 25°C with the same procedure as the one presented in the previous part (II.2.a.ii). It allows the study of the breakdown voltage dependence with respect to the layout and the epitaxy. And if necessary, the breakdown temperature dependence can be studied to discriminate a breakdown mechanism from another. After the electrical analysis, general observation with the microscope was performed to analyze the macroscopic physical degradation. Some of the interesting devices are electrically tested to determine the right biasing for the lock-in thermal camera observation. The study ends with the physical and electrical analysis performed with Lock-in Thermography (LiT) and Focused Ion Beam-Scanning Electron Microscopy (FIB-SEM) on the most interesting devices to directly observe the location of the damaged area and help identify the breakdown mechanism.

It must be noted that concerning the analysis technique, Emission Microscopy (EMMI) was not used because the thick metal (several micrometers) would prevent the top-view observation below them because of its shielding effect as highlighted in one of the Schroder talk [186] (slide 11).

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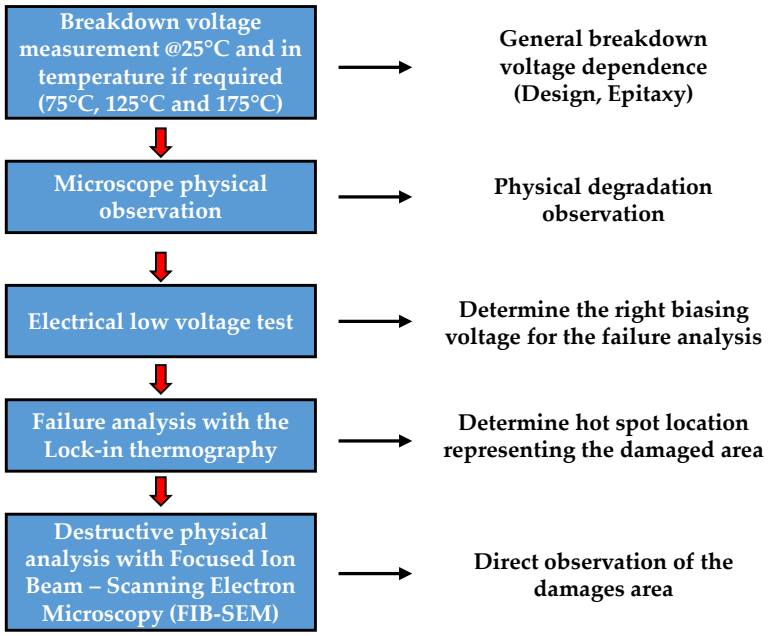

Figure 58: General method followed for the breakdown mechanism identification of devices broken with a floating substrate.

II.3.a.ii Experimental Presentation

For this work, several layouts as presented in **TABLE 5** were required. For the breakdown identification, a single layout was used for the long anode-to-cathode distance (LAC-30) as well as for short anode-to-cathode distance (FPG0-1). All the other layouts reported in **TABLE 5** are used for the epitaxial and layout impact on the breakdown voltage study made on small anode-to-cathode distance. For that, the two first categories consist of layout variation first field plate length named FPG0 (in blue in **TABLE 5**) and the cathode field plate length called FPD (in black in **TABLE 5**). After that, to analyze the impact of the anode field plate length sum, the layouts called FPG0-1, FPG1-1d5 and LAC-16 will be compared. To study the impact of the epitaxial stack on the breakdown voltage (especially for small anode-to-cathode layout), the epitaxy 1 and 2 presented in **Figure 59** will be compared. The difference relies on the distance between the back barrier and the 2DEG (300 nm and 200 nm for the epitaxy 1 and 2 respectively).

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TABLE 5: Layout parameters for the devices studied in the floating substrate configuration (Studied parameter variations are underlined and in bold).

Layout name	L_{AC} (µm)	FPG0 (µm)	FPG1 (µm)	FPG2 (µm)	FPG3 (µm)	$\sum_i FPGi$	FPD (µm)
FPG0-1	16	**1**	1	1	1	**4**	0.5
FPG0-2	16	**2**	1	1	1	5	0.5
FPG0-3	16	**3**	1	1	1	6	0.5
FPD-0d25	16	2	2	2	2	8	**0.25**
FPD-1	16	2	2	2	2	8	**1**
FPD-2	16	2	2	2	2	8	**2**
FPG1-1d5	16	1	1.5	1.5	1	**5**	0.5
LAC-16	16	2	2	2	2	**8**	0.5
LAC-30	**30**	2	2	2	2	8	0.5

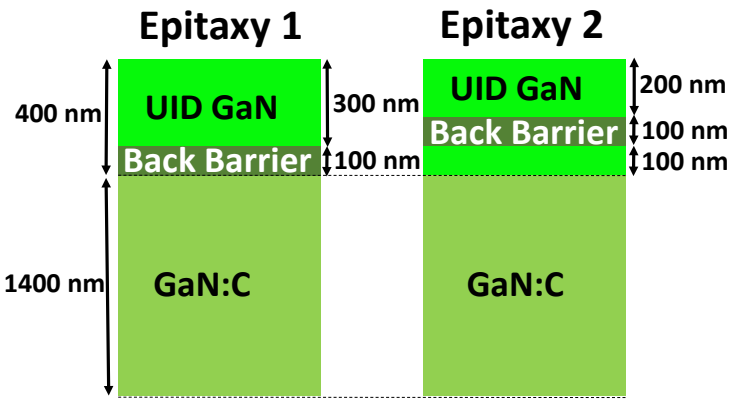

Figure 59: Schematic of the two investigated epitaxial stacks.

Before moving to the presentation of the different results, here is a small introduction to the different characterization techniques used in this chapter (further details are reported in Annexe B).

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Focused Ion Beam Scanning Electron microscopy (FIB-SEM) is used to observe device cross-section with a final picture resolution below the 100 nm range as shown in the bibliography (II.1.a.ii.2nd). In our case, it is used to observe the damage caused by the breakdown. To do so, several electron sensors are placed within the FIB-SEM apparatus as follows:

- In the SEM column:
  - Secondary Electron Secondary Ion (SESI) sensor: It was the most used detector used in this study. It has a relatively good topographic resolution (with respect to the other sensors) and it is not that much disturbed by the charging in dielectrics.
- In the FIB column:
  - InLens (Secondary electron detection too) sensor: It has the best topographic resolution (with respect to the other sensors) but it is sensitive to the charging in dielectrics.
  - Energy Selective Backscattered (ESB) sensor: It has the worst topographic resolution (with respect to the other sensors). However, it is very sensitive to the atomic number making it very useful to identify matter migration.

Lock-in Thermography (LiT) as shown in the bibliography is an imaging method sensitive to infrared radiation emission due to the local heat dissipation in a sample from the Joule effect. A non-uniformity in the current density can lead to a local temperature increase that can be identified by the system. The system can be therefore used to identify the location of device failure that can originate from its intrinsic properties or extrinsic defects.

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The readers must be aware that usually the LiT is performed in forward bias after having stressed the device. In fact, this regime provides enough power to be dissipated by the device due to the bias limitations previously mentioned. In this sense, two devices (with the same layout: FPG0-2) were tested in forward bias with the thermal camera. The first one was not stressed before the test and thus called "fresh" device. The result of the thermal camera is shown in **Figure 60(a)**. A clear large heat spot is visible meaning that the device self-heating is uniform. Thus as expected, there is no preferential current path. This device is compared with a device respectively stressed at 1000 V and 500 V as shown in **Figure 60(b)**. The lock-in signature of this device in **Figure 60(c)** exhibits the same trend as the "fresh" device meaning that there was no degradation resulting in current crowding. On other devices, voltage biases near breakdown were tried without any change in the leakage as shown in **Figure 60(b)** limiting this kind of approach. Thus the thermal camera was used once the device was broken.

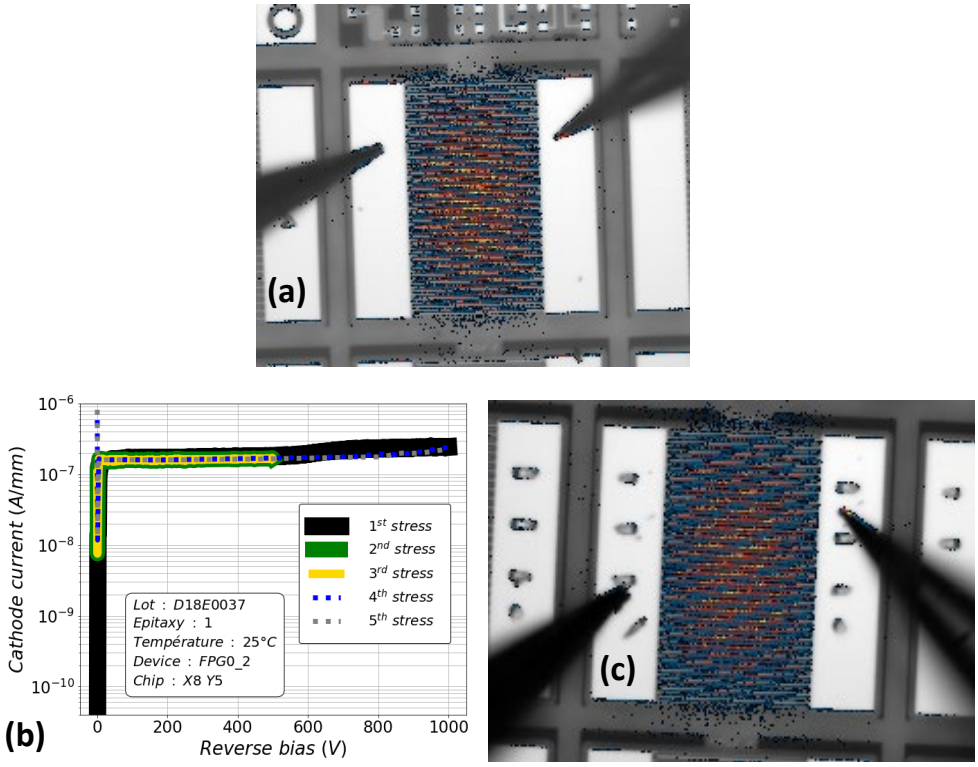

Figure 60: (a) Thermal camera observation at a forward bias of 0.5 V (11.2 mA), 25 Hz with an integration time of 2 min of the "fresh" device (b) Repetitive voltage stress applied on the "stressed" without reaching the breakdown voltage (c) Thermal camera observation at a forward bias of 0.47 V (11.9 mA), 25 Hz with an integration time of 2 min of the "stressed" device.

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II.3.b Experimental Results

As explained in the second part (II.2.b.ii), the broken devices with floating substrate can be subdivided into two groups: either short or long anode-to-cathode distance. The two following sections will analyze in detail the breakdown mechanism of both sizes.

II.3.b.i Long Anode-to-Cathode Distance Devices

As mentioned in the previous part (II.2.b.ii), the long anode-to-cathode distance devices broken with a floating substrate exhibit a saturation in breakdown voltage by further increasing this distance. In the literature, it is written that the breakdown is limited by the vertical conduction as proposed by Visalli *et al.* [241], Shen *et al.* [240] and Jiang *et al.* [238]. In this section, it will be shown that this is not the only breakdown mechanism that can explain the saturation.

To begin with, the microscope observation after breakdown reveals that the main part of the broken device presents a huge degraded area with one or more melted fingers as it can be observed in **Figure 61**. This prevents identifying the physical location of the failure point because the dissipated heat lead to the formation of a crater.

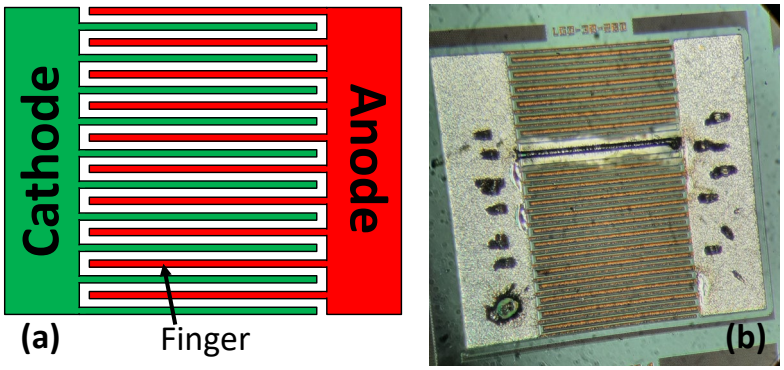

Figure 61: (a) Top view schematic of an interdigitated diode (b) Microscope observation of a broken LAC-30 device.

To discriminate breakdown mechanisms, breakdown measurements were performed at three other temperatures: 75°C, 125°C and 175°C. The raw measurements are displayed in **Figure 62(a)**. First, it can be observed that the current exponentially increases with the temperature but no clear trend concerning the current value before breakdown stands out. By extracting the breakdown voltage for every device and at all temperatures as shown in **Figure 62(b)**, it is clear

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that the breakdown voltage decreases with the temperature. Therefore, the impact ionization can be discarded from the origin of this breakdown.

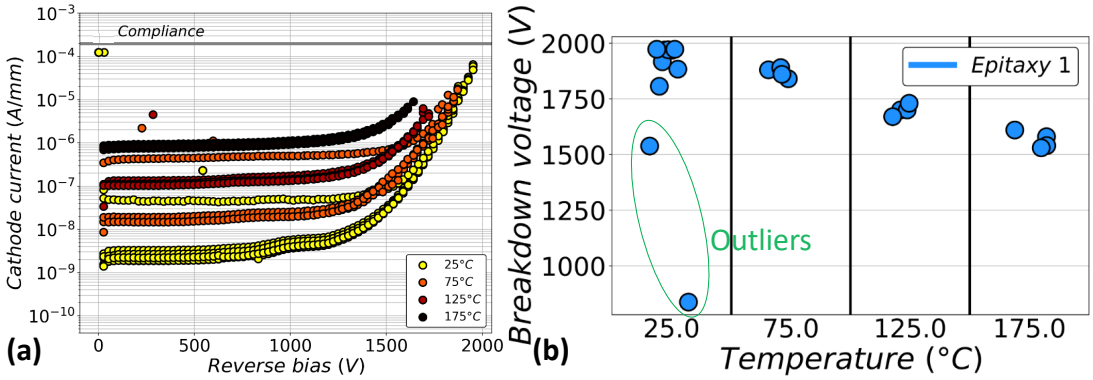

Figure 62: (a) Floating substrate reverse breakdown measurement in temperature of LAC-30 devices on the epitaxy 1 (b) Breakdown voltage as a function of the temperature on the epitaxy 1 for the LAC-30 (note: points are randomly placed on the x-axis for a given temperature).

Nevertheless, two values at 25°C are out of this tendency. Looking at the breakdown voltage over the wafer in **Figure 63(a)**, they are placed in the wafer edge, which might be explained by a process non-uniformity. Removing these points leads to **Figure 63(b)**. By making a linear fit, the trend drops of 2.5 V every degree. However, there is no data available to compare this.

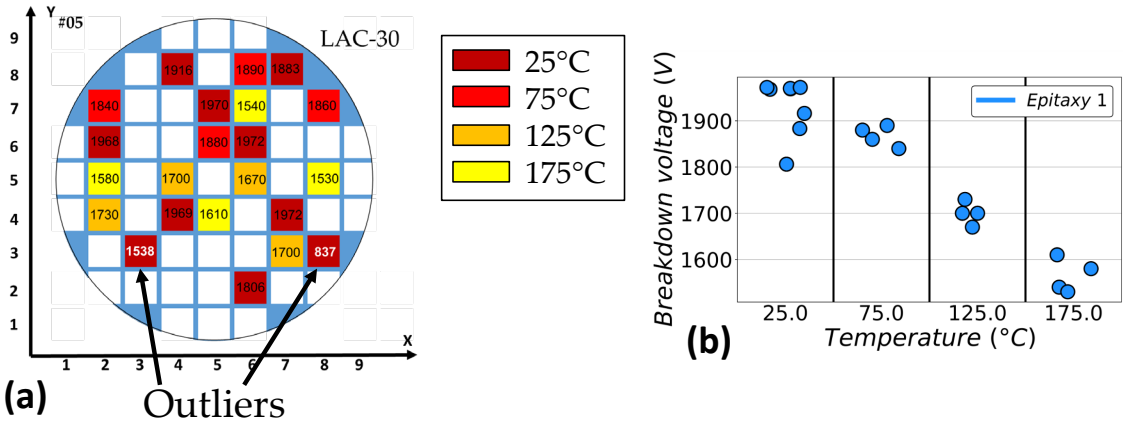

Figure 63: (a) Breakdown voltage mapping on wafer #05 having epitaxy 1 and a LAC-30 layout (b) Breakdown voltage as a function of the temperature on the epitaxy 1 for LAC-30 without outliers (note: points are randomly placed on the x-axis for a given temperature).

The advantage of decreasing the breakdown voltage with temperature is that less power is dissipated in the device during the breakdown before the compliance mechanism stops the power

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supply. Hence fewer degradations and especially at the surface were observed (not shown here). It even leads to no visible degradation on the surface with the microscope at high temperature. Thus, a device broken at 175°C not presenting any damage on the surface was chosen and investigated. Its electrical characteristic before breakdown is shown in **Figure 64(a)**. An electrical failure analysis with the Lock-in Thermography was performed on this device as shown in **Figure 64(b)**.

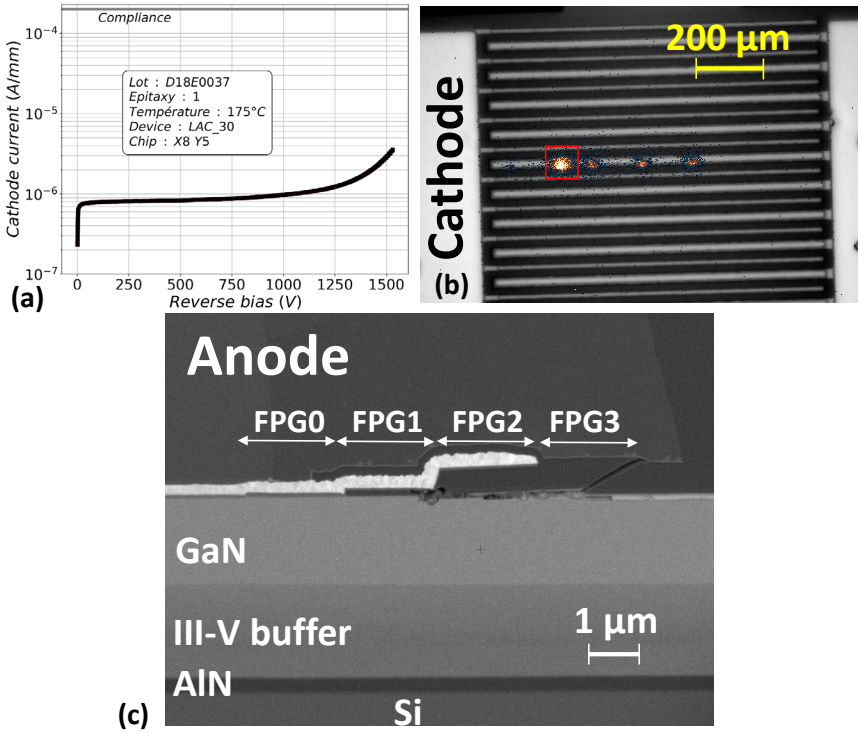

Figure 64: (a) Reverse breakdown measurements at 175°C of a LAC-30 on the epitaxy 1 (b) Thermal camera observation (overlay between microscope and amplitude picture) of the device broken with the previous electrical test at a reverse bias of 1.5 V (1 mA), 25 Hz with an integration time of 2 min 30 s (c) FIB-SEM (ESB sensor) most interesting cross-section in the area framed in red in the above picture.

Four different hot spots are visible on a single anode finger. The area framed in **Figure 64(b)** was observed and the cross section in **Figure 64(c)** was obtained. In addition to a crack caused by a mechanical strain released below the fourth field plate, a melted path is visible. It begins from the edge of the second field plate and follows the surface interface between GaN and passivation that corresponds to the AlGaN/AlN/GaN heterointerface. Thus, it strongly suggests that saturation of the breakdown for long L_{AC} layouts could come from a non-uniformity in the electric field distribution that cannot be compensated by the auto-polarization.

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II.3.b.ii Short Anode-to-Cathode Distance Devices

In the previous chapter part (II.2.b.ii), it was shown that below a certain anode-to-cathode distance: L_{AC} the curve representing the breakdown voltage as a function of this distance exhibits a linear trend. As far as the author's knowledge, the unique hypothesis proposed following the TCAD simulation of Shen *et al.* [240] to explain this regime is the impact ionization. Indeed, the time-dependent dielectric breakdown enhanced in the GET diode studied by IMEC [225]–[227] was not situated on the BV vs L_{AC}. It will be shown in the section that the breakdown is caused by the dielectric breakdown below the first field plate due to the non-uniformity of the electric field.

To discriminate the impact ionization mechanism from the possible hypothesis, breakdown measurements in temperature were performed on a FPG0-1 device as previously done for LAC-30. The raw measurements are displayed in **Figure 65(a)**. As already seen for LAC-30 device, the current exponentially increases with the temperature. By extracting the breakdown voltage for every device and at all temperatures as shown in **Figure 65(b)**, some abnormal values are visible. The investigation of the wafer map (**Figure 66(a)**) did not show any trend and would require further investigations to explain the outliers. Nevertheless, as the other measurements at the same temperature were packed, this abnormal behavior can be considered as outliers. The curves without these outliers are displayed in **Figure 66(b)**. The decreasing trend is smaller than the one observed for longer devices. Thus, impact ionization can be rejected from the breakdown mechanism list.

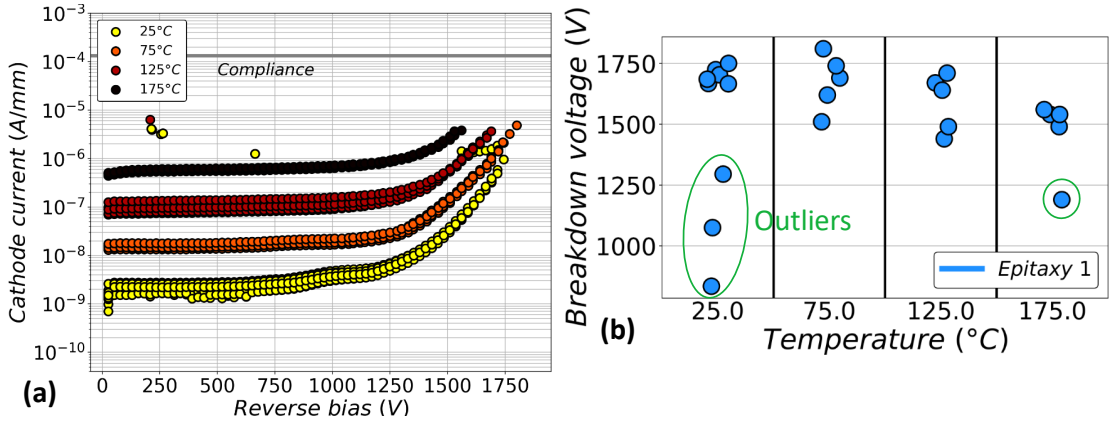

Figure 65: (a) Floating substrate reverse breakdown measurement in temperature of FPG0-1 devices on the epitaxy 1 (b) Breakdown voltage as a function of the temperature on the epitaxy 1 for the FPG0-1 (note: points are randomly placed on the x-axis for a given temperature).

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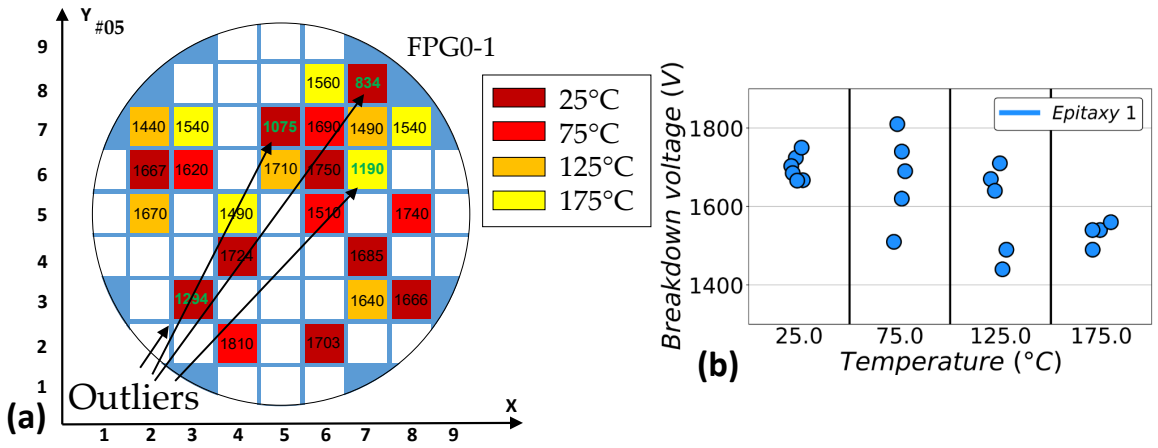

Figure 66: (a) Breakdown voltage mapping on the wafer #05 having the epitaxy 1 and a FPG0-1 layout (b) Breakdown voltage as a function of the temperature on the epitaxy 1 for the FPG0-1 without outliers (note: points are randomly placed on the x-axis for a given temperature).

As well as for long device, a diode presenting no damage on its surface was chosen to perform the failure analysis as presented in **Figure 67**. Its electrical characteristic before breakdown is shown in **Figure 67(a)**. Very diffuse hot spots appear on the surface with the LiT apparatus (**Figure 67(b)**). They are spread over two anode fingers and a cathode finger. As the injected electrical power is lower than in the long device case, it means that the effective degraded area is wider in this case. By scrutinizing the area framed in red in **Figure 67(b)** with the FIB-SEM, a hugely damaged area is visible under the first field plate with a more discrete melted path at the heterojunction that should continue until the cathode. This signature is very similar to the observation of Rossetto *et al.* in [247], in their study on normally-on GaN-on-Si HEMT under blocking mode stress. Thus, as well as the long device, the breakdown voltage of relatively small diode is also limited by the non-uniformity of the electric field. Moreover, the anode-to-cathode distance plays a role on the electric field distribution since the failure location changes. Nevertheless, the breakdown is still caused by the dielectric failure. It can be noticed that a similar breakdown phenomenon was already reported in Gate Edge Termination (GET) diodes in the case of substrate and anode connected together as in the study of Hu *et al.* [154] which demonstrates similarity in breakdown mechanisms with or without substrate connection.

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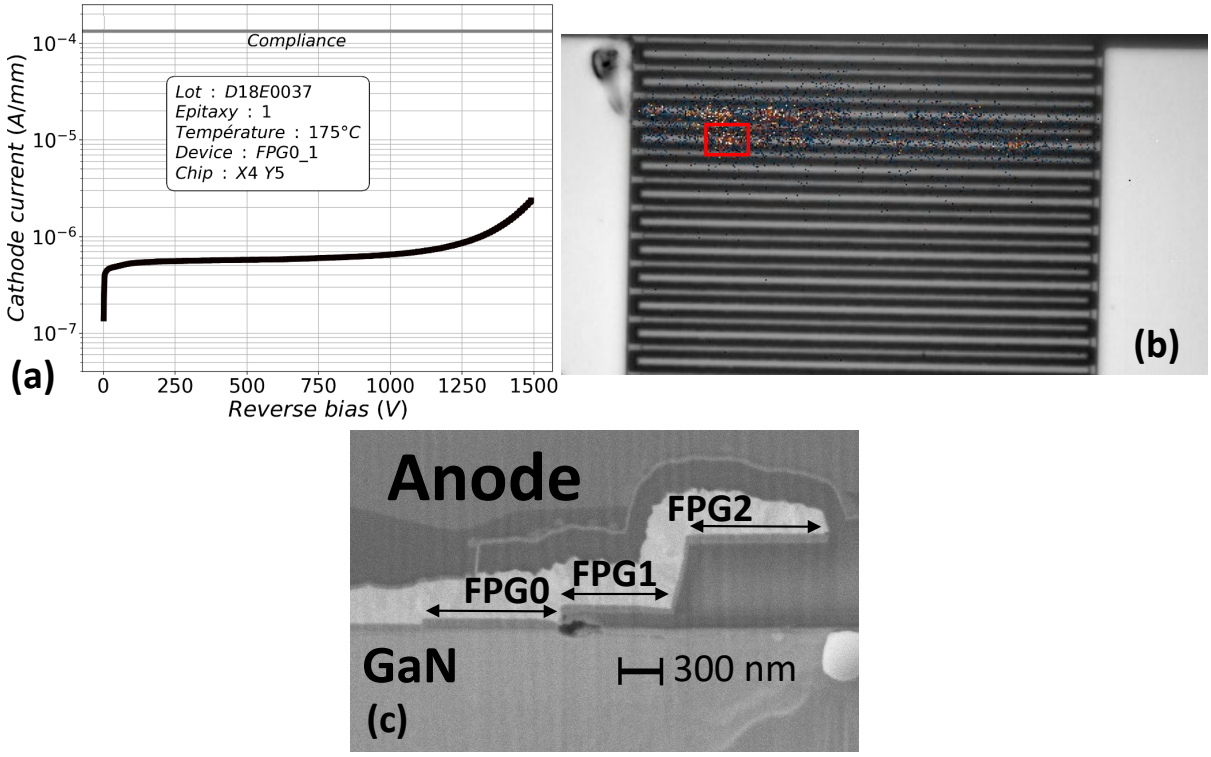

Figure 67: (a) Reverse breakdown measurements at 175°C of an FPG0-1 on the epitaxy 1 (b) Thermal camera observation (overlay between microscope and amplitude picture) of the device broken with the previous electrical test at a reverse bias of 0.3 V (6.6 mA), 25 Hz with an integration time of 3 min (c) FIB-SEM (SESI sensor) cross-section in the area framed in red in the above picture.

The next two paragraphs are dedicated to the analysis of the breakdown voltage variation with respect to the layout and epitaxial parameters for optimization guideline perspectives.

II.3.b.ii.1st Layout Dependences

To perform this analysis, two different layout parameters are studied: the first anode field plate length called FPG0 (from 1 µm to 3 µm) and the cathode field plate length named FPD (from 0.25 µm to 2 µm). The other layout parameters are described in **TABLE 5**. As shown in **Figure 68(a)**, whatever the epitaxy, the breakdown voltage median decreases when the first anode field plate length increases. This is coherent with what was shown in a previous study [247].

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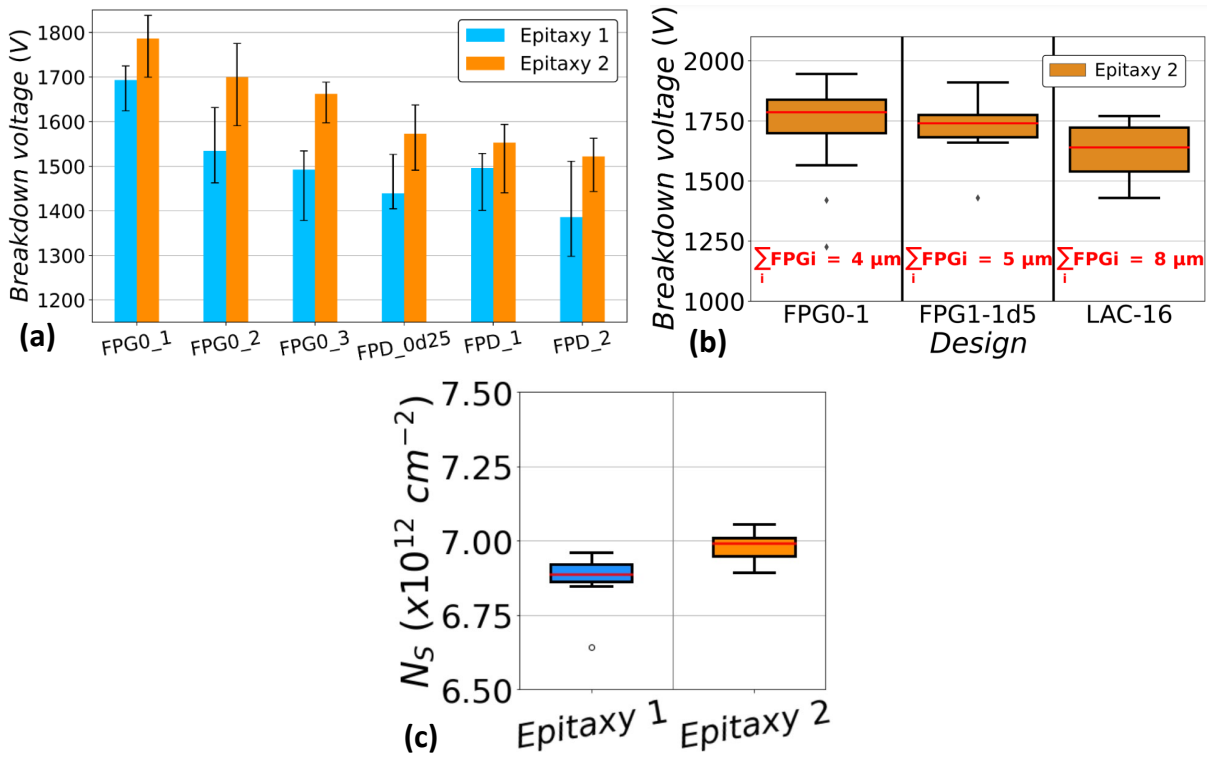

Figure 68: (a) Breakdown voltage of epitaxy 1 and epitaxy 2 (the back barrier is 100 nm closer to the back barrier in the epitaxy 2) dependence on the layout (sixteen tested devices and error bars represent the first and the third quartile) (b) Breakdown voltage as a function of the sum of anode field plate length (FPG0-1: 4 µm; FPG1-1d5: 5 µm and LAC-16: 8 µm) for the epitaxy 2 (c) Electron density in the channel as a function of the epitaxy extracted with a gated Van der Pauw structure.

On the contrary, the variation of the cathode field plate length has no impact on the breakdown voltage. Thus, with floating substrate, the electric field in its critical region should not significantly change with the cathode field plate length. Nonetheless, this parameter is known for having an impact on the current collapse which depends on the electric field at the cathode [270], [271]. In addition, the "FPG0" device category has a completely higher breakdown voltage values with respect to the "FPD" category. The difference between both categories relies on the length of the anode field plate (as can be seen in **TABLE 5**). Thus, the comparison of different layouts having different sums of the anode field plate lengths is shown in **Figure 68(b)**. Indeed, layouts FPG0-1, FPG1-1d5 and LAC-16 (presented in **TABLE 5**) are compared and show a decrease in the breakdown voltage median when the sum is increased. It suggests that smaller field plate layouts are preferable for higher breakdown voltage. Here is the following proposed explanation:

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- In blocking mode, the potential drop is not uniform between the two electrodes (anode and cathode) as illustrated in **Figure 69** for short **(a)** and **(b)** long field plate:

  - As explained in the first chapter, there are potential drops in a short distance just below field plate transitions resulting in electric field peak.
  - When the field plate is long, capacitive coupling prevents the potential drop below field plate. Hence, the lateral electric field is lower at field plate transition and especially at the first field plate corner which is limiting ($\|\vec{E}\|$=E_C at BV) in **Figure 69**.

However, neither study on each field plate length contribution (FPGi, i Є [|1,3|]) nor with smaller field plate layouts could have been performed because the specific layouts were not present in the mask set.

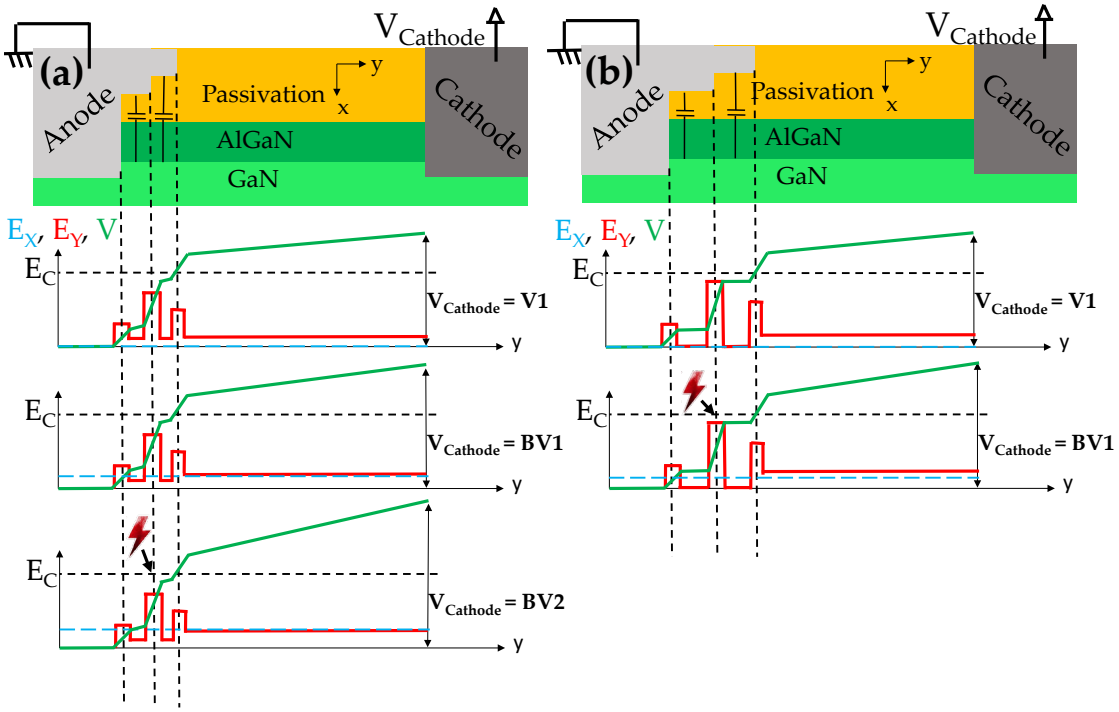

Figure 69: Field plate impact on the electrostatic potential distribution for (a) short field plate (b) long field plate layouts (E=E_X+E_Y for graphic simplification purposes).

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II.3.b.ii.2nd Epitaxial Dependences

Comparing the two different epitaxies on the different proposed layouts is pretty clear in **Figure 68(a)**. Indeed, the breakdown voltage median is always higher with the epitaxy 2. Two hypotheses are proposed to explain this difference. This could be either due to the electron density difference in the 2DEG or to the Reduced Surface Electric Field (ReSurf) effect [175]. Capacitive measurements were performed on specific test structures called gated-Van Der Pauw (Schematics of the test structure in Figure 4 of [270]) with a square active area with 200 µm edges to extract the electron density in the 2DEG. The tests were conducted with a small signal of 40 mV at a frequency of 1 kHz. The results show a slightly higher 2DEG electron density in the case of epitaxy 2 as shown in **Figure 68(c)**. Thus, the higher breakdown voltage of epitaxy 2 cannot be explained by a lower 2DEG electron density and the Resurf effect of the Back barrier is the remaining hypothesis.

II.3.b.iii Summary

In summary, the electrical and physical failure analysis performed on device electrically broken with a floating substrate, enhances that the electric field non-uniformity below the anode field plates limits voltage withstanding capabilities.

Long anode-to-cathode devices (> 20 µm) exhibit a breakdown voltage saturation limiting the voltage range of the architecture. The analysis showed that the breakdown occurs between the second anode field plate corner and the heterojunction (as shown with the red path in **Figure 70**). This is different from the expected vertical limitation proposed in the literature. Thus, with respect to a study on the epitaxial leakage that could have been directly proposed with the state-of-the-art hypothesis, a field plate configuration optimization (FPG2 and/or FPG3 closer to the 2DEG) could be suggested in a first step.

As for the small anode-to-cathode devices (= 16 µm), a dielectric failure was also observed for the first time on a Schottky diode between the first anode field plate corner and the heterojunction (as shown with the cyan path in **Figure 70**). Moreover, it was shown that the breakdown voltage can be optimized by using smaller field plate length (smaller than the micrometer range) and by narrowing the distance between the Back barrier and the 2DEG. This gives perspectives for future experimental studies to optimize the breakdown.

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Technology Computer Aided Design (TCAD) is able to tackle problematics involving epitaxial structure and device architecture. Nevertheless, it was not used in this part because the right identification of the breakdown location is not possible without careful consideration. Indeed, as presented in the state-of-the-art (II.1.a.i), the authors limit their analysis to the match in between the experimental breakdown voltage and the electric field uniformization. Indeed, elements have to be taken into consideration to rely upon the TCAD simulation results. The best example would be the buffer traps studied by Bakeroot *et al.* on the electric field as shown in the state-of-the-art presentation [243]. Perhaps charge transport mechanisms too. The considerations to get a sufficient electric field precision and representativity will be discussed in the third chapter of the manuscript.

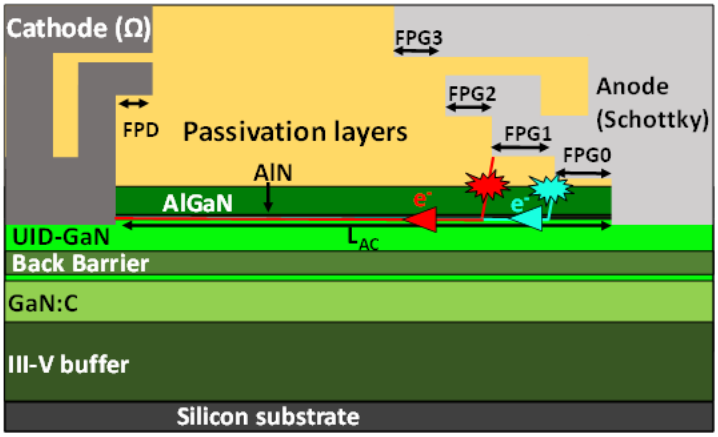

Figure 70: Schematic cross-section of the diode representing the post-breakdown electron flow for two layout categories: 1/ long anode-to-cathode layouts in red (LAC > 20 µm) and 2/ Layouts having a sixteen-micrometer anode-to-cathode distance in cyan.

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II.4 Device Limitations with Grounded Substrate

At CEA Leti, the substrate is always connected either to the anode as for the power diodes or to the source for the power transistor. This is because the well-known current collapse (a very important property for the end-user) is drastically reduced in this configuration. Thus, the breakdown limitations understanding is needed in this configuration to engineer devices to withstand higher voltages.

II.4.a Method Description

To study the breakdown voltage in the configuration with a substrate connected to the anode, breakdown measurements (test parameters are presented in II.2.a.ii) are performed on several device layouts. The different layouts have already been presented before but they are again reported in **TABLE 6**. It consists first of the "LAC" category in which the anode-to-cathode distance is varied from 16 to 30 µm. And two other categories with an anode-to-cathode distance equal to 16 µm: "FPG0" and "FPD" which the first anode field plate and the cathode field plate length are carried from 1 to 3 µm and from 0.25 to 2 µm. The broken device is then electrically tested after the breakdown measurement. To do so, they are again tested in reverse regime at 25°C but at lower voltage. It consists of applying a voltage sweep with a step of 1 V from -3 V to 40 V. The compliance is set at 100 µA. After the electrical analysis, general observation with the microscope was performed to analyze the macroscopic physical degradation. The analysis end with the physical and electrical analysis made with the Lock-in Thermography (LiT) and the Focused Ion Beam-Scanning Electron Microscopy (FIB-SEM) on the most interesting devices.

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TABLE 6: Layout parameters for the different studied layouts with substrate-connected configuration (Studied parameters are underlined and in bold).

Layout name	L_{AC} (µm)	FPG0 (µm)	FPG1 (µm)	FPG2 (µm)	FPG3 (µm)	FPD (µm)
FPG0-1	16	**1**	1	1	1	0.5
FPG0-2	16	**2**	1	1	1	0.5
FPG0-3	16	**3**	1	1	1	0.5
FPD-0d25	16	2	2	2	2	**0.25**
FPD-1	16	2	2	2	2	**1**
FPD-2	16	2	2	2	2	**2**
LAC-16	**16**	**2**	**2**	**2**	**2**	0.5
LAC-20	**20**	2	2	2	2	0.5
LAC-25	**25**	2	2	2	2	0.5
LAC-30	**30**	2	2	2	2	0.5
FPG0-3.5-sp	16	**3.5**	0.5	0.5	2	0.5

II.4.b Experimental Results

II.4.b.i General Trends

After the breakdown measurements, the devices are then observed with a binocular microscope. They are electrically tested: cathode to substrate (vertical leakage); cathode to anode with and without substrate connected to the anode. This is done sweeping the cathode voltage from 0 to 40 V with a 100 µA compliance. Unexpectedly, the device currents are neither always fully deteriorated nor physically degraded with visible degraded area. Therefore, they are classified into four different categories as reported in **Figure 71**:

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- Category 1: Devices for which the currents are entirely deteriorated (meaning that the compliance in the post-breakdown electrical tests is reached within few volts) and exhibit damaged areas on their surface (in orange in **Figure 71**). This is what was expected and it constitutes the main part of every layout except for the FPG0-3 layout.

- Category 2: Devices that present neither physical nor electrical degradation (in purple in **Figure 71**). This is unexpected because the devices, current and voltage level are identical to the first category. Interesting discussion will be proposed in the following sub-section (II.4.b.ii.3rd).

- Category 3: Devices for which only the vertical leakage is deteriorated and have a visible damaged area. It is a small part of long device: LAC-30 (25%) and a smaller part of the FPD-2 (20%).

- Category 4: Devices for which the lateral current is degraded (higher current than the non-stressed device) and either have no other degradation or the vertical current is deteriorated (compliance reached after few volts) and have a visible damaged area.

Each category will be discussed in detail in the next section (II.4.b.ii).

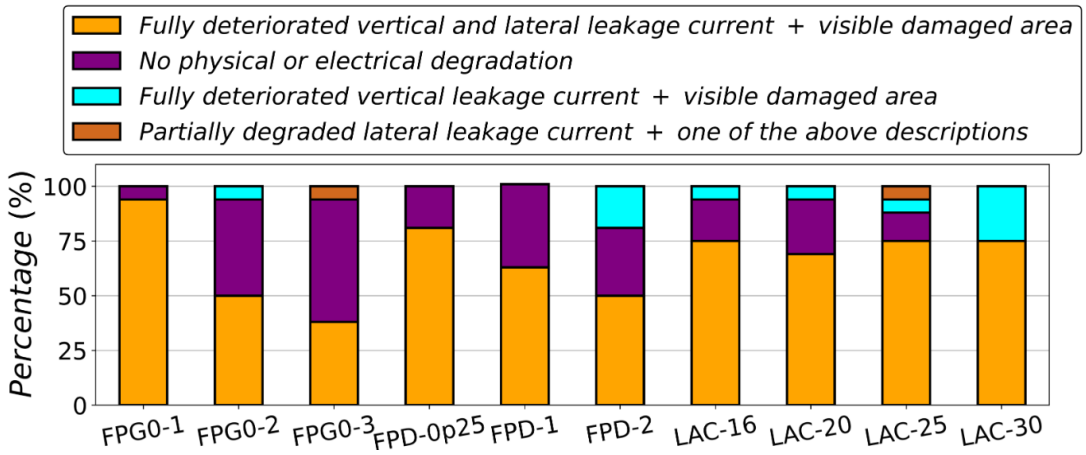

Figure 71: Classification in different categories after breakdown measurements in percentage per occurrence of the different architectures performed on the epitaxy 1 (sixteen tested devices for each layout).

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II.4.b.ii Failure Analysis for Every Identified Categories

II.4.b.ii.1st Category 1: Fully Deteriorated Vertical and Lateral Leakage Current with Visible Damaged Area

As illustrated in **Figure 72(a)**, the device surface is highly deteriorated. This makes the electrical and physical failure analysis hard. Indeed the thermal signature shown in **Figure 72(b)** was not related to a specific physical signature when making FIB-SEM observation in the region marked in red in **Figure 72(c)**. In addition, the power dissipated during breakdown was sufficiently high to create an 8 µm deep crater in the silicon substrate at the breakdown location (where the electron flow is perpendicular to the electrodes fingers in **Figure 72(c)**). Nevertheless, when performing the FIB-SEM observation, a huge degraded area was observed underneath the anode field plate as it can be seen in **Figure 72(d)**. The origin of this will be discussed in the following sub-section (II.4.b.ii.3rd).

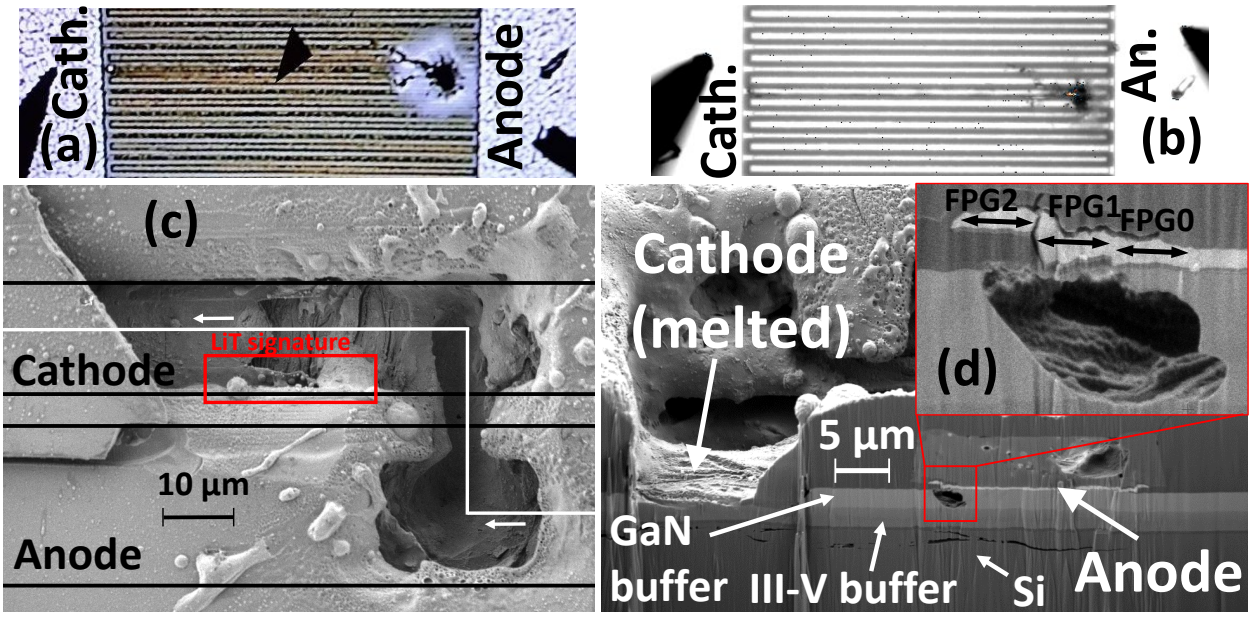

Figure 72: (a) Optical microscope observation of a FPG0-1 diode on the epitaxy 1 belonging to the first group (b) LiT observation at V = 0.19 V (500 µA) during 2 min at a frequency of 16.6 Hz (c) FIB-SEM (SESI sensor) top view observation of the same diode with the electron flow in white (d) FIB-SEM (SESI sensor) most interesting cross-sectional observation of the same diode.

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II.4.b.ii.2nd Category 3: Fully Deteriorated Vertical Leakage Current

With a long anode-to-cathode distance and a vertical breakdown limited by the electron injection at the AlN/Si interface (rather far from the surface), a broken device showing only a vertical current deterioration after the breakdown as illustrated in **Figure 73(a)** is not surprising. Even though the high power dissipated during breakdown made the electrodes melt on the anode and cathode side as shown in **Figure 73(b)**, the main physical deterioration is on the cathode side. By observing the cross section at the breakdown location (**Figure 73(c)**) and a little bit further (**Figure 73(d)**), the breakdown seems to be caused by a dielectric breakdown of the AlN. Indeed, by superimposing an ellipse to the melted area, the intercept between the minor and the major axis is matched with the AlN/Si interface. Nevertheless, by carefully observing the cross-section at the breakdown location, no hyperbolic form is visible in the AlGaN buffer as it can be seen in the GaN buffer in **Figure 73(c)**. This probably means that the current was drained through a dislocation in this region. Finally, the white spot visible in the silicon may result from a hole flow that made the GaN or the metal migrate.

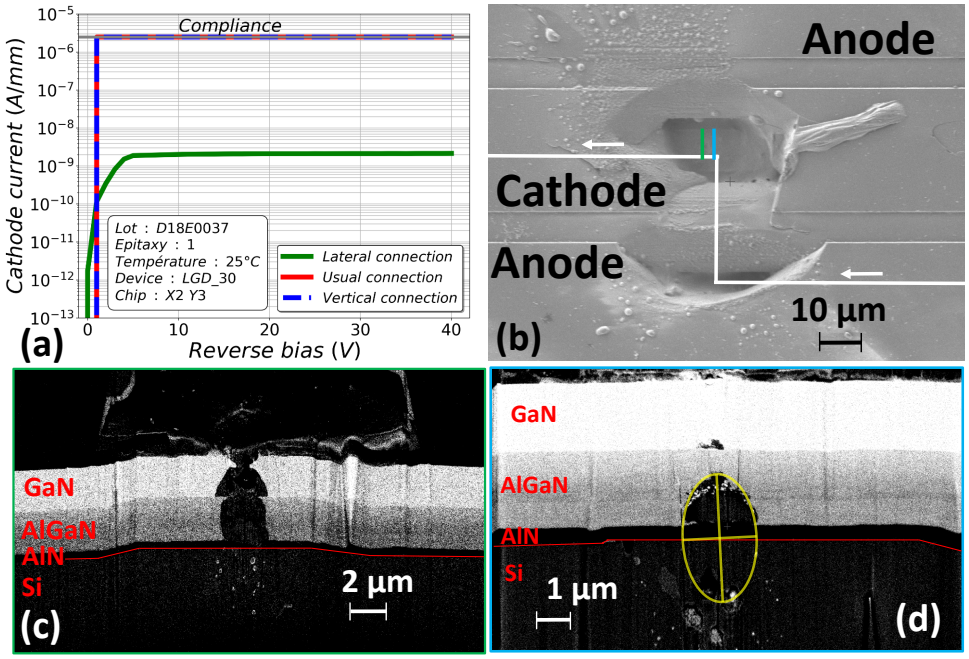

Figure 73: (a) Electrical characteristic (general, lateral and vertical leakage) of a LAC-30 diode on the epitaxy 1 belonging to the third group (b) FIB-SEM (SESI sensor) top view observation of the same diode with the electron flow in white and the location of the cross-sectional observation (ESB sensor): (c) at the breakdown location (d) a little further the latter.

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II.4.b.ii.3rd Category 2: No Physical or Electrical Degradation

As described before, some of the devices having undergone a breakdown measurement do not exhibit visible damaged area on their surface as shown in **Figure 74(a)** and no leakage deterioration as shown in **Figure 74(b)**. The most interesting is that this behavior depends on the device layout. Indeed, it constituted more than fifty percent of the FPG0-3 layouts. From the literature, it is known that by tailoring the first anode field plate length, the electric field below in the channel is changed (increase in the study of Rossetto *et al.* [247]). There is probably a field-assisted mechanism occurring under the anode field plate that helps the breakdown voltage capability with its presence. Moreover, this breakdown voltage withstanding ability is repeatable several times as shown in **Figure 75**. In this figure, the third try exhibits a lower leakage at low voltage. From the previous study (II.2.b.i), the lateral leakage current is the main contribution to this regime. Therefore, there was probably a degradation close to the 2DEG and the anode during the two first breakdown measurements that might explain the leakage lowering. The breakdown voltage capability dependence on FPG0 and the leakage lowering are perhaps correlated to the same field-assisted mechanism under the anode field plates. This reminds us, the degradation found in the previous sub-section (II.4.b.ii.1st) in **Figure 72**. In fact, there was a melted area below the anode field plate and not at the Schottky contact.

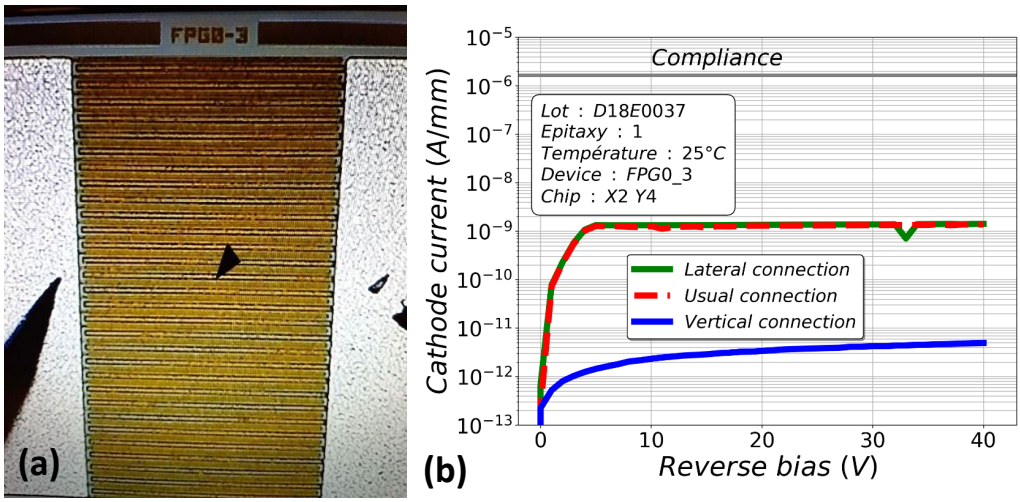

Figure 74: Classification in different groups after breakdown measurements in percentage per occurrence of the different architectures performed on the epitaxy 1 (sixteen tested devices for each layout).

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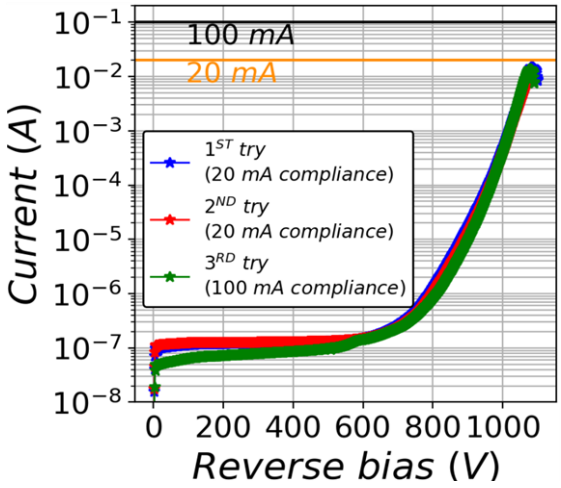

Figure 75: Consecutive breakdown measurements performed with an interval of approximately 1 min of a unique device with a FPG0-3 architecture on the epitaxy 1 and W = 60 mm.

To discriminate a mechanism from another, it was proposed to study the temperature dependence of the breakdown withstanding capabilities on a layout that has a long first anode field plate length: FPG0-3.5-sp. Despite the fact that many of the measurements at 125°C were saved by the compliance as it can be observed in **Figure 76**, the other temperatures demonstrated that after testing the devices until 650 V, the capability of withstanding the vertical breakdown voltage seems to diminish with temperature. Indeed, four devices were able to withstand the breakdown at 25°C, two at 75°C and only one at 175°C.

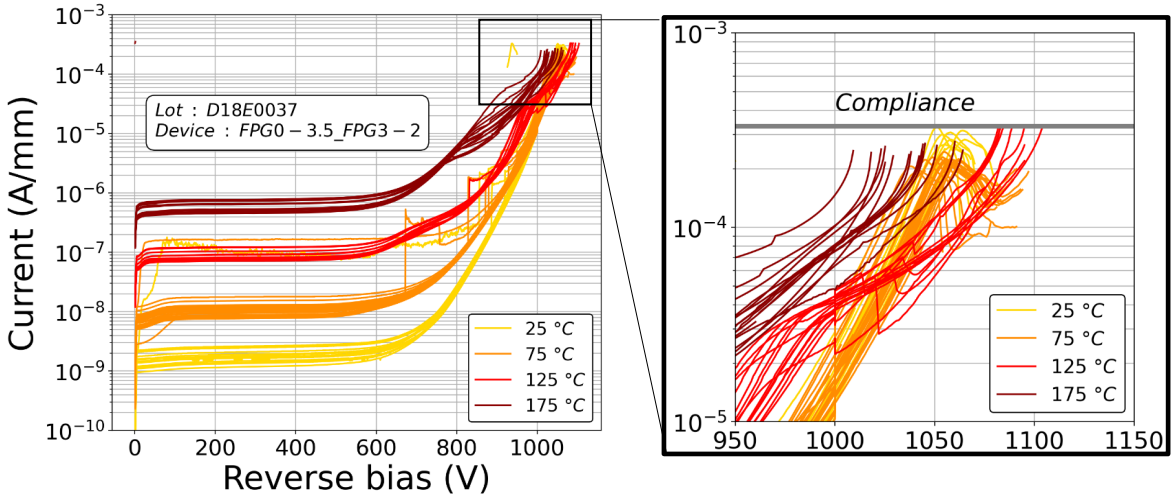

Figure 76: Breakdown measurements at different temperatures of FPG0-3.5-sp (W = 60 mm) device with the substrate connected to the anode.

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Assuming that the previously described field-assisted mechanism probably observed under the anode field plate (in **Figure 72(d)**) helps to withstand the vertical breakdown and knowing that the vertical breakdown withstanding capability diminishes with temperature, this would mean that the mechanism is worsened with temperature. Thus it could correspond to an impact ionization mechanism. To verify our findings, a study under ultraviolet light could have been performed to emulate the electron generation (as it is done in [272]) instead of the impact ionization but the field plate presence prevent such experiment.

It is therefore clear that the link between the possible impact ionization occurring under the anode field plate and the vertical breakdown voltage is hard to draw. Nonetheless, there is still some hope that future studies will find out the interaction that has not been found yet. Indeed, the Hong Kong University has already studied the indirect consequence of impact ionization occurring under the source field plate (in between the gate and drain) during off-state stress: the threshold voltage V_{TH} negative shift as shown in [272], [273].

II.4.b.iii Summary

In summary, the electrical and physical failure analysis made device electrically broken with a substrate connected to the anode revealed that the vertical breakdown is caused by a dielectric breakdown of the AlN nucleation layer most probably at a place in which the current is drained by a dislocation.

Moreover, it was proposed for the first time that having a small anode-to-cathode distance and a long first field plate length at the anode may create an impact ionization mechanism that could help the device withstand vertical breakdown. Other experiences especially with ultraviolet light could confirm the hypothesis.

Furthermore, the interaction between the impact ionization occurring below the anode field plate and the AlN dielectric breakdown has not been found yet. This could be the topic of future studies.

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Conclusion

In this chapter, breakdown measurements made on lateral power Schottky diodes fabricated at CEA LETI with or without the substrate connected to the anode at different temperatures were analyzed. Electrical and physical failure analysis was performed to identify the breakdown mechanisms and location. Moreover, different layouts and epitaxies were tested to quantitatively assess their impact on the breakdown voltage.

Devices with the substrate connected to the anode were shown to be limited by the vertical breakdown whatever the anode-to-cathode distance available. On the one hand, for the first time, an experimental proof of the nucleation layer (AlN) dielectric breakdown probably assisted by the already present dislocations was provided. On the other hand, it suggested for the first time that this breakdown could be withstood thanks to an impact ionization mechanism occurring below the anode field plate. This is especially the case for short devices when the first anode field plate is long (3 µm here). Nevertheless, the link between the impact ionization and the vertical breakdown has not yet been found. This could be the subject of future experimental and/or TCAD studies.

Devices with a floating substrate were shown to have a higher breakdown voltage with respect to the vertical one, strongly suggesting the substrate auto-polarization. By varying the anode-to-cathode length from 16 µm to 30 µm, two different regimes were identified:

- A linear regime at small anode-to-cathode distance in which the breakdown increases with the distance. This part is expected to be limited by a lateral breakdown according to the literature. This was confirmed with the first observation on a Schottky diode of a dielectric breakdown between the first anode field plate corner and the heterojunction. In addition, this breakdown can be improved with the ReSurf effect by narrowing the distance between the back-barrier and the heterojunction and also by using smaller field plate lengths (smaller than the micrometer range). Technology Computer Aided Design (TCAD) was not used at this point for a layout and epitaxial optimization because several elements need to be taken into consideration as previously discussed. This work will be initiated in the next chapter.

- A saturation of the breakdown voltage for long devices. This is expected to be limited by a vertical breakdown as proposed by the literature. However, the failure analysis revealed a dielectric breakdown between the second anode field plate corner and the heterojunction adding a potential second explanation to the saturation phenomenon.

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Chapter III
Improving the AlGaN/GaN Schottky Diode TCAD Modeling Based on Experimental Measurements

This chapter is dedicated to the modeling of AlGaN/GaN Schottky Barrier Diode (SBD) fabricated at CEA LETI. A first part will emphasize the state-of-the-art limits (modeling of buffer traps) as well as the methodology proposed to deal with them. In a second part, the results of the capacitance temperature dependence study will be presented. After that, the study of the experimental vertical current temperature dependence will be introduced. The advancement of the study performed in TCAD on the vertical conduction will be summarized. Finally, the Deep Level Transient Fourier Spectroscopy (DLTFS) results will be introduced before concluding on the different obtained results.

Outline

Chapter III Improving the AlGaN/GaN Schottky Diode TCAD Modeling Based on Experimental Measurements 105
III.1 State-of-the-Art Approach Limits and Proposed Method Description 108
III.1.a Limit of the Approach Present in the Literature to Simulate the Electric Field Distribution in AlGaN/GaN Lateral Power Devices 108
III.1.a.i Two-Dimensional Analytical Model 108
III.1.a.ii Technology Computer Aided Design (TCAD) 109
III.1.b Proposed Method to Probe the Different Contribution of Buffer Traps on the Device Characteristics 112
III.2 Modeling of the Capacitive 2DEG Depletion Control 117
III.2.a Buffer Layers Affecting the Capacitance Dependence at First Order 117
III.2.a.i Sample and Method Presentation 117
III.2.a.ii Impact of the Substrate Presence 120
III.2.a.iii Impact of the Piezoelectric Model Activation in the Buffer Layers 120

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III.2.a.iv Impact of the Back Barrier Presence 123
III.2.a.v Discrepancy between the Electric field Distribution and the Experimental Breakdown Measurements 123
III.2.b Buffer Traps Impact on the Capacitive Temperature Dependence 125
III.2.b.i Sample Presentation and Preliminary Study 125
III.2.b.ii Experimental Study 128
III.2.b.iii TCAD Qualitative Simulation Study of Buffer Traps 130
III.2.b.iv TCAD Fit on the Experimental Data and the Possible Interpretations 136
III.2.b.v V_{Ga}-$(O_N)_x$ Hypothesis Verification 138
III.2.c Implementation of Deep Acceptor Traps in the Simulated AlGaN/GaN Schottky Diode and Evaluation of the Electric Field Change 141
III.3 Buffer Charge Movement Modeling Through Vertical Current Temperature Dependence 145
III.3.a Current Status on the Vertical Current Knowledge and the Different Reported Transport Mechanisms 145
III.3.a.i Current Status on the Vertical Current Knowledge 145
III.3.a.ii Ohmic Conduction 147
III.3.a.iii Recombination Limited Transport 148
III.3.a.iv Space Charge Limited Current 149
III.3.a.v Hopping Versus Poole Frenkel Mechanisms 150
III.3.a.vi Summary of the Bulk Transport Mechanisms 152
III.3.b Experimental Analysis and Interpretation of the Vertical Current Temperature Dependence 153
III.3.b.i Preliminary Experimental Studies 153
III.3.b.ii Model Fitting 155
III.3.b.iii Fitting Parameter Interpretation 160
III.3.b.iv Summary 162
III.3.c TCAD Simulation and Modeling Study to Reproduce the Experimental Trend 163
III.3.c.i Simulated Structure Presentation 163
III.3.c.ii Simulation Results 165
III.3.c.iii Discussion 168
III.3.d Summary 169

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III.4 Capacitance Deep Level Transient Fourier Spectroscopy (C-DLTFS) of Schottky AlGaN/GaN-on-Si Schottky Diode....170

III.4.a Samples and Characterization Setup Presentation....170

III.4.b Experimental Results....172

III.4.b.i Arrhenius Plot....172

III.4.b.ii Filling Pulse Width Dependence....173

III.4.c Discussion on the Possible Trap Origins....175

Conclusion....179

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III.1 State-of-the-Art Approach Limits and Proposed Method Description

To this day, several articles proposed to study the electric field distribution by means of analytical model or TCAD in the lateral AlGaN/GaN power device for a specific purpose. Nevertheless, to simplify the simulation and to save calculation time, simplifications are made on the structure. Usually, it does not prevent the author to study the impact of the targeted parameter (layer thickness, field plate length) as shown in the previous chapter. However, the simplifications are usually not sufficient to perform an architecture optimization based on TCAD simulations because the order of magnitude of the electric field has to be accurate as well as the amplitude difference between two places in the device. Thus, the first part will be dedicated to a summary of the different proposed approaches and then, based on the identified limitation (lack of buffer traps calibration method), the initiated method proposed in this PhD will be described.

III.1.a Limit of the Approach Present in the Literature to Simulate the Electric Field Distribution in AlGaN/GaN Lateral Power Devices

In the literature, two different methods were proposed to simulate the electric field distribution. The first one is to use two-dimensional analytical modeling, as it will be presented in the first part. The second one and the most used is the Technology Computer Aided Design (TCAD) as introduced in the second part.

III.1.a.i Two-Dimensional Analytical Model

This approach is not new but it had taken a second breath within the last few years [268], [274], [275]. Two different calculation methods are used: The Equivalent Potential Method (EPM) [275] and the classic resolution of Poisson equation with the continuity equation [268], [274]. Avalanche model can be used in both methods as well as uniform trap distributions.

As the approach do not compare simulation results with experimental measurements, the traps introduced are coming from other studies. For instance, the trap parameters in the study of Kabemura *et al.* [274] are from the work of Zhou *et al.* [276]. As traps found in the references are not demonstrated to be sufficient for an electric field study, this may be a problem.

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The advantage of this method is the computation time because the structure is rather simple as exposed in **Figure 77(a)**. The electric field at the heterojunction at different voltages (shown in **Figure 77(b)**) as well as the breakdown voltage (initiated by avalanche) are obtained. However, the main drawback relies on the time required to set up all the equations with all the boundary conditions and the data display when the device architecture is complex. Liu *et al.* thus recommend to make TCAD simulation first before modeling to prevent mistakes [275]. This is why the major part of the literature performs their simulation in a TCAD environment only.

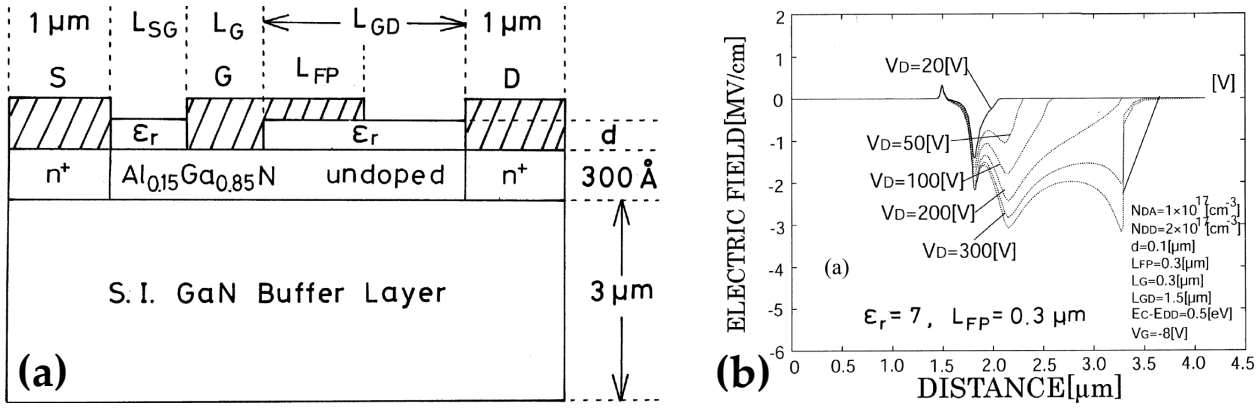

Figure 77: (a) Simulated structure with a two-dimensional analytical modeling approach [274] (b) Typical obtained electric field in the channel at different voltages [274].

III.1.a.ii Technology Computer Aided Design (TCAD)

As mentioned earlier in the introduction of the sub-part (III.1.a), this is the most used technique to perform electric field simulation and thus breakdown voltage study in AlGaN/GaN lateral power devices [176], [228], [240], [241], [243]–[245], [259], [277]–[283], [283]–[286]. The simulation can be performed with different softwares: ISE™ Dessis®, Silvaco™ Atlas®, Synopsys™ Sentaurus®.

They perform Finite Element Method (FEM) on a computer-assisted tailored mesh solving Poisson equation (see **Equation 9**) and the continuity equation for electrons and holes (**Equation 10** and **Equation 11** respectively). It allows observing different physical quantity variations (electron density, electric field …) in a semiconductor device submitted to an electrical, thermal, mechanical or optical stress.

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$$\epsilon_s \times \nabla^2\varphi(x,y,z,t) = -q \times (n(x,y,z,t) - p(x,y,z,t) + {N_D}^+(x,y,z,t) - {N_A}^-(x,y,z,t))$$

Equation 9: Poisson equation (ϵ_s: semiconductor permittivity; φ: electrostatic potential; q: elementary charge; n: electron density; p: hole density; ${N_D}^+$: ionized donor density; ${N_A}^-$: ionized acceptor density) [60].

$$\frac{\partial n(x,y,z,t)}{\partial t} = \frac{1}{q} \times \vec{\nabla}.\overrightarrow{J_n}(x,y,z,t) + G_n(x,y,z,t) - R_n(x,y,z,t)$$

Equation 10: Continuity equation for electrons (n: electron density; q: elementary charge; $\overrightarrow{J_n}$: electron current density vector; G_n: electron generation rate; R_n: electron recombination rate) [60].

$$\frac{\partial p(x,y,z,t)}{\partial t} = -\frac{1}{q} \times \vec{\nabla}.\overrightarrow{J_p}(x,y,z,t) + G_p(x,y,z,t) - R_p(x,y,z,t)$$

Equation 11: Continuity equation for holes (p: hole density; q: elementary charge; $\overrightarrow{J_p}$: hole current density vector; G_p: hole generation rate; R_p: hole recombination rate) [60].

To simulate the electric field distribution, the authors are making assumptions (detailed below) to simplify the structure to reduce the computing time while keeping good accuracy. Nevertheless, the assumptions have limits. The assumptions must be in accordance with the aim of the simulation. The point here is not to criticize the simplification made by the authors but more to be aware of the part that can be simplified if their absence has no impact on the obtained results.

For AlGaN/GaN lateral power devices or associated technological building blocks, the layout of the active area (transistor and diode) is always well-represented. However, the substrate, the buffer layer and the defects within these layers are prone to some simplifications/assumptions:

- The substrate is sometimes removed [241], [278], [280], [286]. This is especially done for the simulation with floating substrate.

- The buffer layers are sometimes removed [241] and not mentioned [240].

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- The trap properties (energy level, capture cross-section, concentration) are chosen in accordance with other articles. Especially for GaN:C buffer and the GaN top layers, their choice comes from:

    - Back (or substrate) biased drain transient experimental work (principle of the experiment [287]) as the work of Zhou *et al.* in [276] which was chosen in the study of Pharkphoumy *et al.* [283] and Wu *et al.* [286], to simulate GaN buffer layers.
    - Current collapse simulation: [288] as in the work of Cornigli [259] to simulate the presence of carbon in the transition layer.
    - Deep Level Transient Spectroscopy: [289] in the study of Khediri *et al.* [284] to simulate the presence of carbon in the transition layer.

As a rule, the main identified difference between the studies using buffer traps is the huge discrepancy of the used trap concentration. In fact, it leads to a completely different electric field distribution as demonstrated by Bakeroot *et al.* [243]. Indeed, as for the carbon case, the ratio between carbon atoms that are in Ga-site (considered as donor traps) and those in N-site (considered as acceptor traps) was shown to have a significant impact on the electric field at a given bias. It must be noted that (as it will be demonstrated further) the quantity that matters for the electric field is the concentration difference between acceptor and donor traps noted [A] - [D] (III.2.b.iii.2nd). To quantitatively assess the impact of this quantity on the electric field, **Figure 78** reports the different electric field distributions at 650 V of simulations with a low concentration difference between acceptor and donor traps ([A] - [D] = 10^{17} cm^{-3}) as used in [259], [281], [285], [290] and a high concentration difference ([A] - [D] = 5×10^{18} cm^{-3}) as used in [267], [291], [292]. It is clear that with a high concentration difference, the electric field is crowded at the cathode whereas it seems equally distributed between the anode and the cathode in the other case.

This is why, in the proposed calibration procedure, several characterization techniques are proposed to determine some quantities associated to buffer traps (energy level, capture cross-section, concentration).

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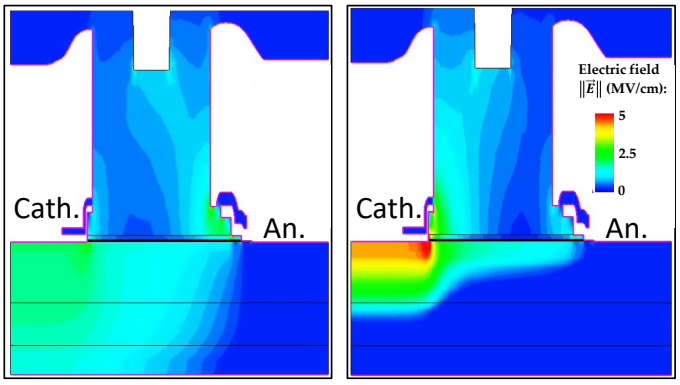

Figure 78: Electric field mapping at 650 V of a diode with the substrate connected to the anode for two different [A] - [D] quantities: 10^{17} cm^{-3} (on the left) and 5×10^{18} cm^{-3} (on the right).

III.1.b Proposed Method to Probe the Different Contribution of Buffer Traps on the Device Characteristics

In the previous subpart, it was shown that no suitable calibration method to perform a quantitative electric field study already exists. This is mainly because the simulation articles rely on other studies not performed on the same device and that trap properties are not verified for the electric field.

The proposed method relies on different axes as exposed in **Figure 79**:

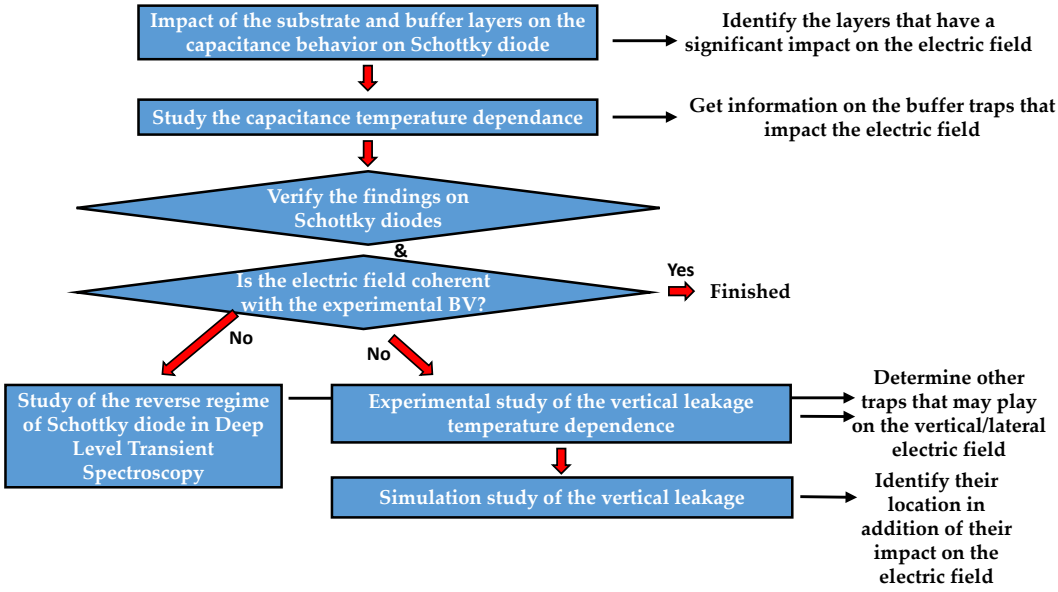

Figure 79: General method developed in this thesis to identify the necessary elements allowing to get a simulated electric field coherent with the experimental breakdown voltage.

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- It begins with the device capacitance study at 25°C. By matching the simulation curve with the experimental one, the layers that have a significant impact on the electric field can be identified.

  Justification:

  1. **The reverse capacitance of the diode follows the 2DEG progressive depletion** from the anode to the cathode as exposed in the study of Weiss *et al.* [148]. This is because the non-linear behavior of the capacitance characteristic represents the capacitive coupling between the field plates and the 2DEG (that is progressively depleted with the reverse bias). This is also valid for the Miller: C_{RSS} or output: C_{OSS} capacitance of the transistor as shown in [293]. To illustrate this idea, **Figure 80** represents the electron density mapping at different reverse biases for a generic diode. The progressive depletion of the 2DEG can be observed with the main capacitive contribution (in red) are shown for each bias. This explains the different plateaus observed on the diode capacitive characteristic in **Figure 81**. The voltage at which the transition occurs is named a depletion voltage. The narrower the field plate from the heterojunction, the higher the capacitive coupling, resulting in distinct plateaus in a multiple field plate system followed by a capacitance drop as it can be seen at low voltage on the capacitive characteristic.

  2. **The electrostatic equipotential changes accordingly to the 2DEG progressive depletion** as it can be observed with electrostatic equipotential lines in **Figure 82(a), (b), (c), (d)** and **(e)**.

  3. **The electric field is related to the electrostatic potential** ($\vec{E} = -\overrightarrow{grad}(V)$) which can also be observed comparing **Figure 82(d)** and **(e)** with **Figure 82(f)** and **(g)** (the narrower the electrostatic equipotential lines, the larger the electric field).

     → Thus, the study of the capacitive characteristic is important to get information on parameters impacting the 2DEG depletion and therefore the electric field.

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Limit identification: A comparison between the experimental breakdown voltage and the electric field in simulation will be presented in III.2.a.v. The two layouts: FPG0-1 and LAC-16 that were experimentally compared in II.3.b.ii.1st with the substrate floating[4] will be used. The simulation comparison consists of comparing electric field distribution at 1700 V (voltage close to the experimental breakdown of FPG0-1).

- It is followed by a capacitance temperature dependence study on transistor (device for which the temperature dependence was important) in III.2.b. This allows the identification of deep acceptor traps present in the epitaxy by means of TCAD simulation fitting on experimental curves. The same limit identification step will be presented to assess if the current modeling is sufficient and to justify the following studies.

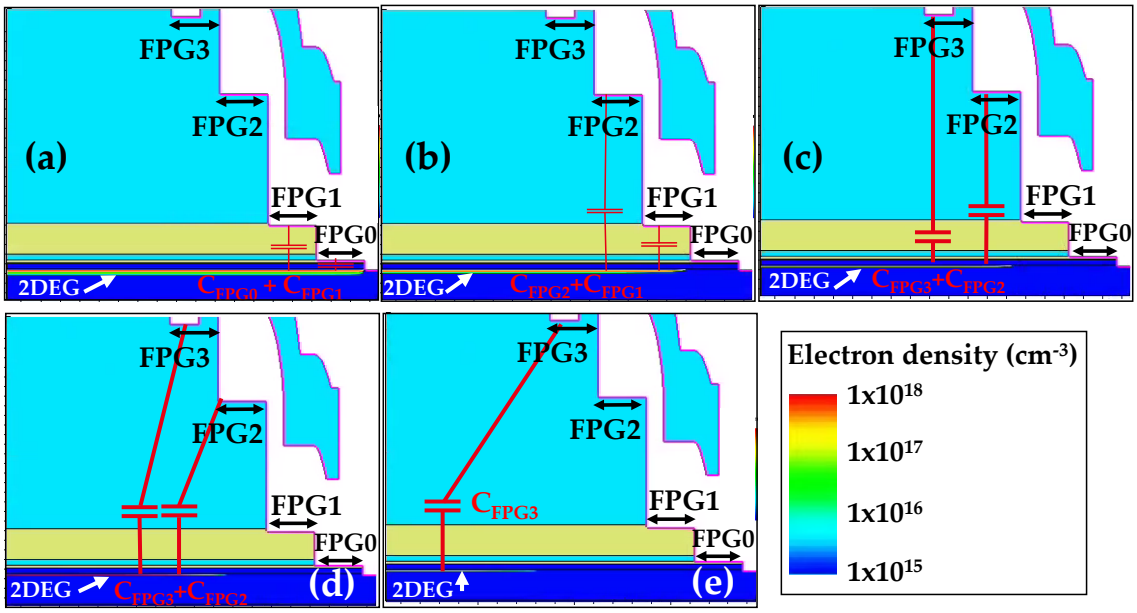

Figure 80: Simulation of the electron density mapping as a function of the applied reverse bias: (a) 0.5 V; (b) 15 V; (c) 40 V; (d) 80 V; (e) 125 V for a generic diode with the substrate connected to the anode. The most significant capacitive contributions are illustrated in red. To justify this, variation of field plate length was performed enhancing the impact of the respective field plate on the characteristic (not shown here).

[4] This comparison study could not have been performed with respect to devices with the anode connected to the substrate (usual configuration) because in that configuration, devices available during the PhD were vertically limited as shown in the previous chapter.

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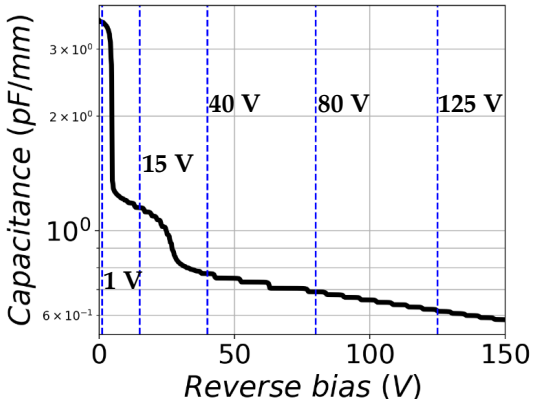

Figure 81: Capacitive characteristic at 25°C of a generic diode.

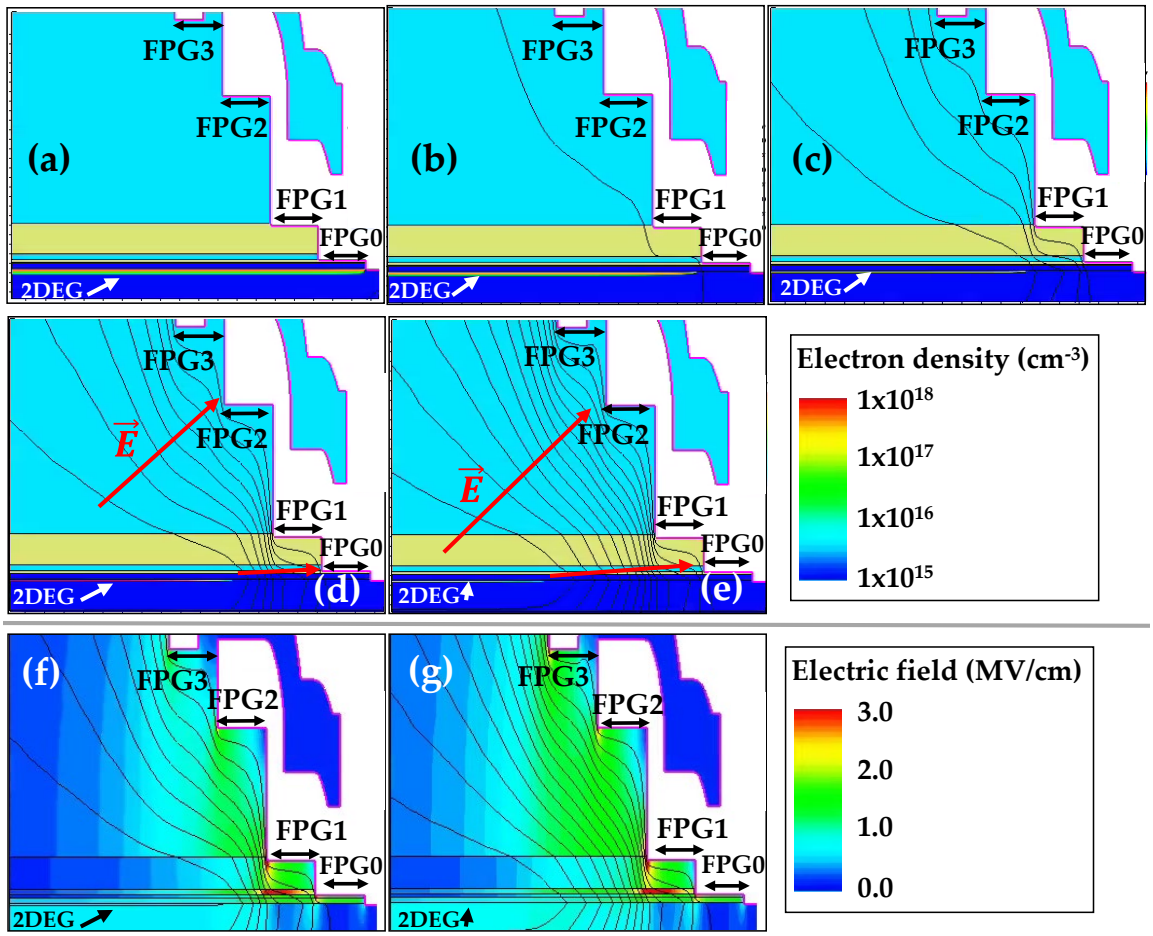

Figure 82: Simulation of the electron density mapping as a function of the applied reverse bias: (a) 0.5 V; (b) 15 V; (c) 40 V; (d) 80 V; (e) 125 V for a generic diode with the substrate connected to the anode. Simulation of the electric field mapping as a function of the applied reverse bias: (f) 80 V; (g) 125 V for a generic diode. The equipotential lines are represented in black.

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- A study on the vertical current (III.3.b) allows to get information on the related traps present in the epitaxy. Indeed, this could lead to the identification of traps that may impact the electric field due to the presence of leakage path passing through these traps. This was performed by analytically modeling the experimental temperature measurements allowing to extract their energy levels.

  Limit identification: When moving to TCAD simulation (III.3.c), it will be demonstrated that this information (trap energy level) is not sufficient to reproduce the experimental vertical measurements in simulation and therefore improve the TCAD modeling.

- Deep Level Transient Fourier Spectroscopy (DLTFS) was performed on the diode to identify traps that may have an impact on the electric field. This was performed in the regime (0 to 100 V), in which the 2DEG depletion occurs near the anode contact. Indeed, it studies the capacitance transient behavior in reverse, after a "filling pulse" in which the diode is polarized at 0 V. Thus traps for which the state (ionized or not) changes during this test may have an impact on the electric field. This will be presented in III.4.

Nevertheless, the method is not complete yet because the time required to perform experiments and simulations is huge. Moreover, direct measurements that would give all the information on the buffer traps are missing. This requires further studies, especially concerning the epitaxy. For instance, the impact of the different growth parameters on the presence of certain traps and their impact on the breakdown voltage.

For the readers' information, it must be mentioned that the measurement called "back (or substrate) biased drain transient" cannot bring more information on the buffer traps without having accurately modeled the vertical current in the epitaxy as exposed by Pagnano *et al.* [287].

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III.2 Modeling of the Capacitive 2DEG Depletion Control

As mentioned in the previous part, the first step of the methodology is to understand the key parameters to model the capacitive coupling and therefore the electric field. To do so, a first part will determine which is the most relevant simplification in TCAD simulation to be able to model correctly the capacitive coupling while reducing the computation time. A second part will be focused on the capacitive temperature dependence to identify traps that significantly affect the electric field.

III.2.a Buffer Layers Affecting the Capacitance Dependence at First Order

In this subpart, substrate and epitaxial layers' impact on the capacitive characteristic will be analyzed at 25°C for an AlGaN/GaN lateral Schottky diode with the substrate connected to the anode as it is the configuration used for the application.

III.2.a.i Sample and Method Presentation

To perform these simulations, the same kind of device layout used in the previous chapter (Chapter II) will be simulated. It simply consists of the Schottky diode architecture illustrated in **Figure 83(a)** with a layout FPG0-1 (L_{AC} = 16 µm; FPG0 = FPG1 = FPG2 = FPG3 = 1 µm; FPD = 0.5 µm; W = 60 mm) which is why the technology description will not be presented again. However, with respect to the previous chapter, the epitaxy is slightly changed: the GaN:C has a 1.3 µm thickness and the last 500 nm of the epitaxy is composed of an unintentionally doped GaN layer with a 100 nm thick embedded back-barrier situated at 300 nm from the heterojunction as illustrated in **Figure 83(b)**. The experimental electrical characterizations and simulations are performed with a backside contact that is always connected to the anode.

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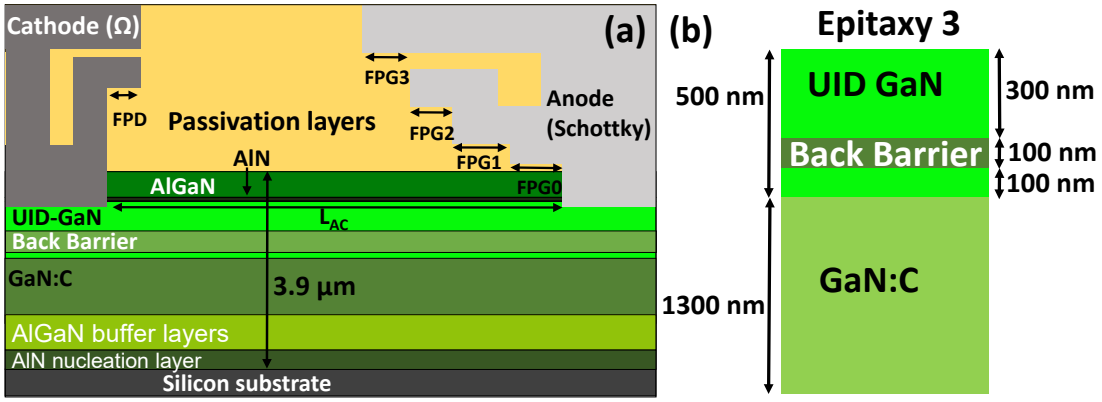

Figure 83: (a) Schematic cross-section of the Schottky diode architecture (b) Schematic of the investigated epitaxial stack.

The experimental capacitance measurements were performed with the Keysight® B1505 with a Multi-Frequency Capacitance Measurement Unit (MFCMU) and a High-voltage Source Measurement Unit (HVSMU). A voltage sweep from 0 V to 200 V with a step of 1 V was applied at the cathode as well as a small signal of 50 mV at 10 kHz. The Direct Current (DC) and Alternating Current (AC) signals were mixed with the N1260A Bias Tee. The integration time was done over two Power Line Cycles (PLC). To have a constant ramp rate equal to 2 V/s during the whole sweep, the delay time was set at 500 ms.

The TCAD simulations are performed on Synopsys™ Sentaurus® [294]. As for the device physics, Vurgaftman values with the piezoelectric polarization strain model are used [295] for the spontaneous and piezoelectric polarization charge calculations. It was activated at the AlGaN/Si_3N_4 interface and at the GaN/AlN/AlGaN interfaces. To compensate the polarization charges at the AlGaN/Si_3N_4, surface donor traps with a concentration of 5×10^{13} cm^{-2} at an energy of 1.6 eV below the conduction band [46], [50]. To match the electron density in the 2DEG of this epitaxy (7.2×10^{12} cm^{-2}), the activation of this model was set at 87.2% (measurements were made with the same measurement condition and with the same structure as explained in II.3.b.ii.2nd). In the buffer layers, as the strain evolves during growth [100], it is hard to model. To begin, it was activated assuming that the GaN layers are pseudomorphic (all epitaxial layers are strained to match the GaN lattice parameter) as it seems to be the case in the study of Bakeroot *et al.* [243] (in which carbon impact on the electric field was studied). A discussion on this choice will be dedicated.

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The different simulated structures are illustrated in **Figure 84**. The first one called simulation 1 consists of the same epitaxy as the experimental one (**Figure 83(a)**) except that the nucleation layer has been replaced by a layer having the same properties as the layer above it. Thus the addition of this layer with the AlGaN buffer layers (**Figure 83(a)**) forms the AlGaN buffer in **Figure 84(a)**. This simplification is justified by the fact that for the vertical leakage study, the nucleation layer properties have been changed because the conduction through this layer is hard to model (replaced by a 5 nm AlN in Longobardi *et al.* study [296]; the conduction discontinuity: ΔE_C has been changed from ≈ 2 eV to ≈ 1 eV in the study of Sayadi *et al.* [297] or Borga *et al.* [258]). The substrate contact is taken at the bottom of the silicon (shown in pink in **Figure 84(a)**). The second simulated structure called simulation 2, consists of the first one in which the substrate was removed as shown in **Figure 84(b)**. Finally, by removing the back barrier from the second structure, the third structure called simulation 3 is built as shown in **Figure 84(c)**.

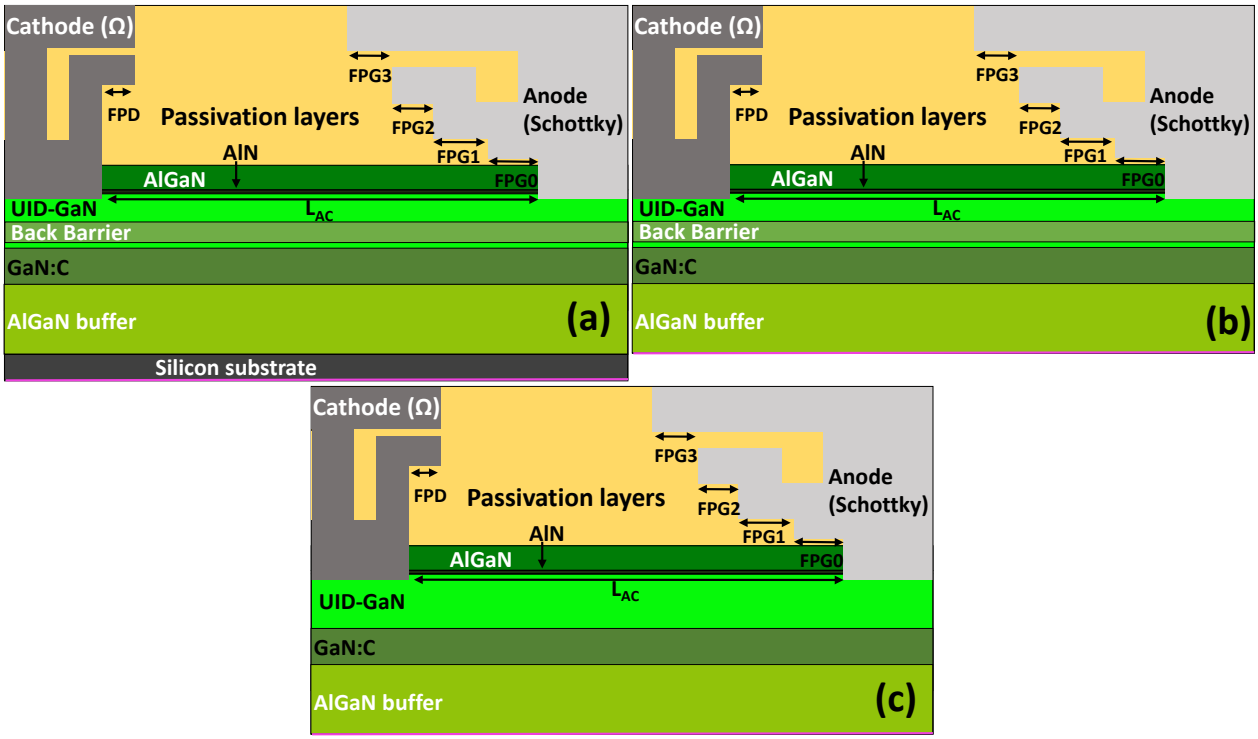

Figure 84: Simulated diode architecture (a) With silicon substrate and with back barrier (simulation 1) (b) Without silicon substrate and with back barrier (simulation 2) (c) Without silicon substrate and without back barrier (simulation 3).

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III.2.a.ii Impact of the Substrate Presence

The 1 mm-thick silicon substrate is really important with respect to the GaN epitaxy. Removing this chunk of material would lighten the simulation converging time. Thus the capacitance characteristics with (simulation 1) and without the substrate (simulation 2) were compared as shown in **Figure 85**. It is clear that in addition to matching the experimental curve, the substrate removal does not significantly change the characteristics. Thus for the rest of the capacitance study, the substrate will be removed.

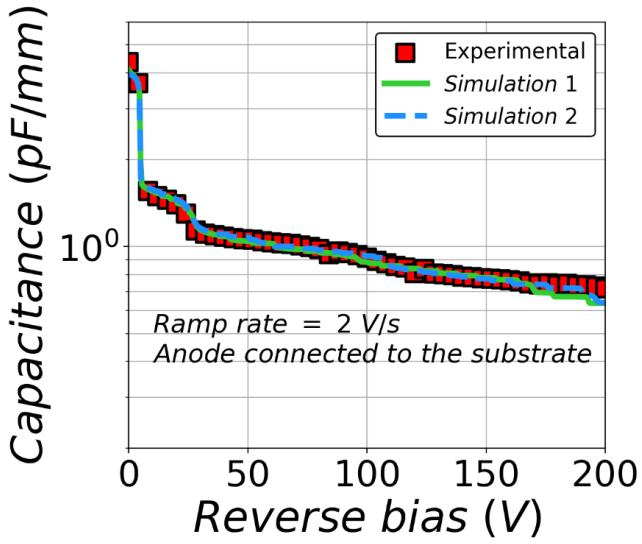

Figure 85: Capacitance characteristics at 25°C with the substrate connected to the anode of the simulated diode (simulation 1 and 2) superimposed with the representative experimental one.

III.2.a.iii Impact of the Piezoelectric Model Activation in the Buffer Layers

As mentioned earlier, the internal strain in the epitaxy is hard to model because there is no information available about it. The only thing known is that the overall wafer strain is quasi-null (this was determined with bow measurement as exposed in the study of Charles *et al.* [100]). It can be supposed that there is some stress released due to the presence of dislocations but it is impossible to attest that the internal strain has completely vanished. Therefore, the capacitance characteristics were plotted with and without activation of the piezoelectric model in the buffer layers as displayed in **Figure 86**. In this figure, by removing the piezoelectric model, the capacitance drops a little bit in the entire voltage range and consequently, does not match the experimental curve. After further

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investigation, it was figured out that the capacitance lowering was due to the 3-Dimensional Hole Gas (3DHG [298]) removal in the buffer layer as shown by comparing **Figure 87(a)** (without piezoelectric model) and **Figure 87(b)** (with piezoelectric model). Indeed as highlighted in the figure, its presence allows reducing the capacitance thickness in between the substrate and the cathode.

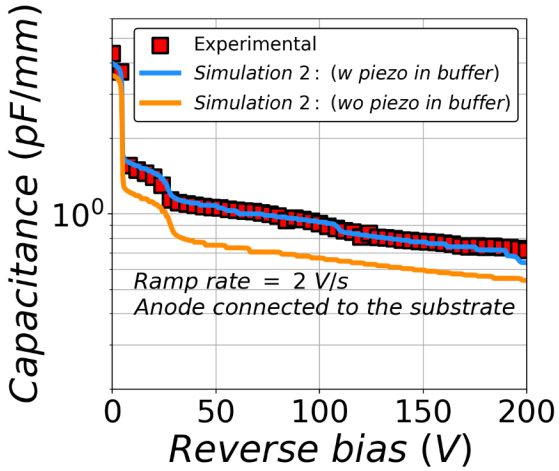

Figure 86: Capacitance characteristics with the substrate connected to the anode of the simulation 2 structure with and without piezoelectric model activated in the buffer layers superimposed with the representative experimental one.

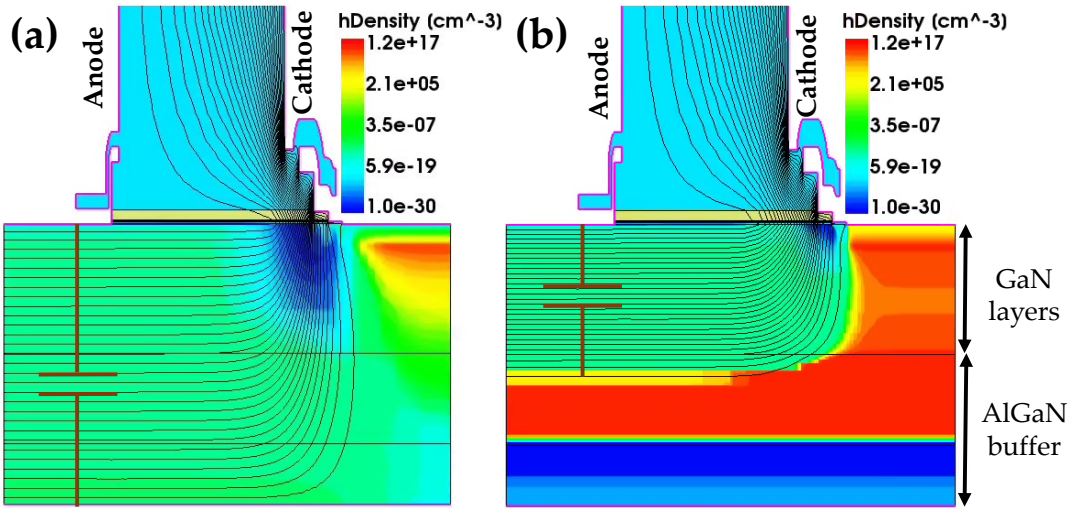

Figure 87: Hole density mapping of the diode with the substrate connected to the anode with electrostatic equipotential lines at 200 V and 25°C for: (a) Simulation 2 (without piezoelectric model activated in the buffer layers) (b) Simulation 2 (with piezoelectric model activated in the buffer layers).

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Hole gas in the GaN-on-Si epitaxy has already been shown three times in the literature:

- In the study of Sun *et al.* [299] (study of the presence of 2-Dimensional Hole Gas (2DHG) presence in GaN-on-Si epitaxy). They demonstrated that 2DHG are effectively present in their GaN-on-Si epitaxy. This was based on capacitance measurement made on a vertical stack by comparing experimental results and TCAD simulations.

- In the study of Bakeroot *et al.* [243] (study of the electric field variation in a GET Schottky diode by changing the ratio between acceptor and donor traps induced by the carbon content), in which they are present in the deep buffer layers whatever the carbon incorporation. Their presence is potentially justified by the charge compensation of the piezoelectric model.

- In the study of Lingaparthi *et al.* [300] (study of the electron source in multi-channel structure made with AlGaN/GaN heterojunction). There is a formation of 2DHG due to the charge compensation of the piezoelectric model in the multi-channel structure (not in the epitaxy). Nevertheless, by placing interface donor traps at those interfaces, they were able to match the experimental Gated Van Der Pauw capacitance characteristics.

Hence, the presence of hole gas observed in the presented simulations seems coherent with the literature. However, as there is no consensus, this point should be considered with caution. This is why the manuscript always mentions when this model is turned on or off. Nevertheless, it is clear that buffer layers must be taken into account in the simulations.

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III.2.a.iv Impact of the Back Barrier Presence

The back barrier has been shown to have a significant impact on the breakdown voltage as shown by varying its distance with respect to the 2DEG (II.3.b.ii.2nd). As shown in **Figure 88**, it has a very slight impact on the capacitance characteristic. This means that the capacitance fitting is a necessary condition but not a sufficient one.

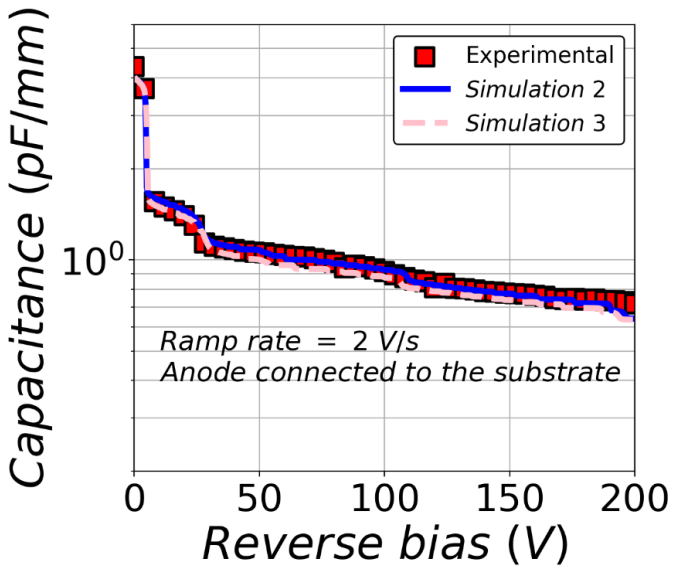

Figure 88: Capacitance characteristics with the substrate connected to the anode of the simulated structure (simulations 2 and 3) superimposed with the representative experimental one.

III.2.a.v Discrepancy between the Electric field Distribution and the Experimental Breakdown Measurements

To check whether the TCAD simulations are coherent with the experimental results in terms of breakdown voltage or not, the experimental breakdown voltage obtained with the substrate floating between two different layouts: FPG0-1 and LAC-16 is compared with the electric field distribution in the GaN channel (1 nm below the heterojunction) near the FPG0-1 experimental breakdown voltage (1700 V). As a precaution, this comparison is made with and without piezoelectric model in the buffer layers.

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First, it is reminded that experimentally, the layout FPG0-1 has a higher breakdown voltage than the LAC-16 layout as shown in **Figure 68(b)**. Moreover, it was demonstrated that the breakdown occurs at the anode side (at the first field plate end). This is why the following observations are focused on that device part:

- When the piezoelectric model in buffer layers is turned on as shown in **Figure 89(a)**, the electric field in the GaN channel at the anode side is unexpectedly higher than the GaN critical electric field. This is probably due to the fact that the electric field is not distributed within the entire epitaxial stacks as shown in **Figure 87(b)**. Moreover, the electric field peaks are higher for the FPG0-1 layout which is not coherent with the experimental results.
- When the piezoelectric model in buffer layers is turned off as shown in **Figure 89(b)**, the electric field in the GaN channel at the anode side is close to the GaN critical electric field which is more what can be expected. However, the electric field peaks are still higher for the FPG0-1 layout, which is not coherent with the experimental results.

The higher electric field for FPG0-1 observation is valid also with a cutline at 1 nm below the first anode field plate (not shown here). Therefore, the electric field distribution is not accurate enough to perform a layout optimization when the device is scaled down.

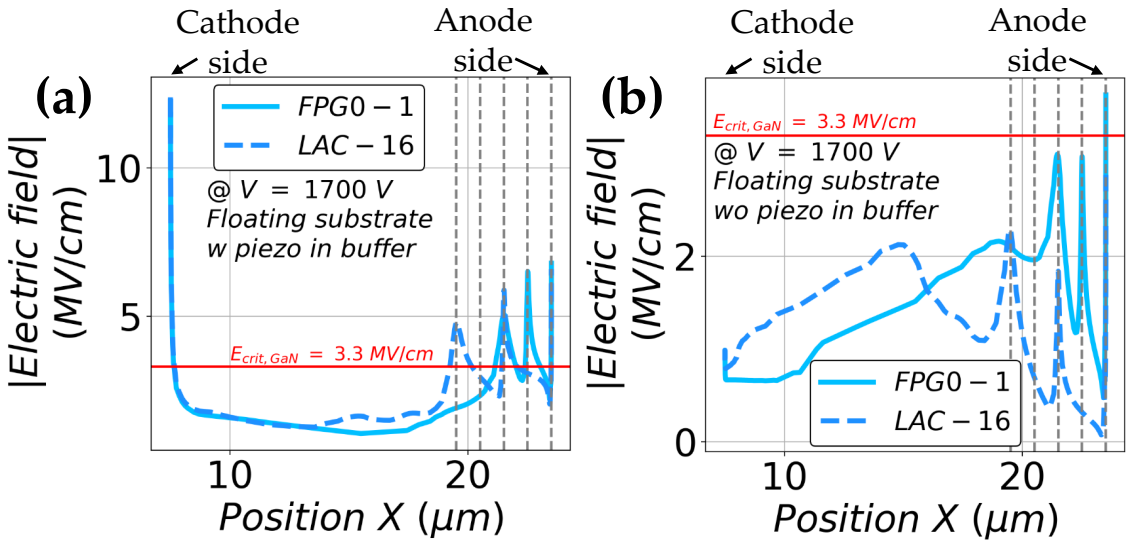

Figure 89: Electric field distribution in the GaN at 1 nm from its interface with the AlN of the simulated structure (simulation 2) with the substrate floating at 25°C and V = 1700 V: (a) With the piezoelectric model activated in the buffer layers (b) Without the piezoelectric model activated in the buffer layers.

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III.2.b Buffer Traps Impact on the Capacitive Temperature Dependence

After having seen that it is not possible to explain the breakdown voltage layout dependency with a floating substrate configuration (shown in II.3.b.ii) with the current modeling as demonstrated in III.2.a.v, the analysis of the capacitance temperature dependence may lead to the discovery of some buffer traps that may have a role on the electric field. This study was carried out on other wafers (with similar epitaxies) on which transistors were fabricated.

This capacitance temperature study makes the parallel between TCAD simulations and the electrical measurement. At first, an experimental part is dedicated to the study of the GaN:C epitaxial growth rate and the ramp rate variation impact on the capacitive characteristics. This was done to indirectly assess the role of the carbon content and have a second reference on the trap kinetics. The second part consists in the qualitative TCAD analysis of the traps parameters' impact on the capacitive characteristics. Finally, the TCAD trap parameters were adjusted thanks to the experimental concentration of species known in the epitaxy and the qualitative analysis. The comparison of the obtained trap parameters with the literature will be done to find out the possible origin of the traps. The study was the topic of one of the author's publications [301].

III.2.b.i Sample Presentation and Preliminary Study

III.2.b.i.1st Sample Presentation

The samples used for this study are very similar to the epitaxy presented in the diode study (II.2.a.i). This means that the epitaxy is grown on a p-doped silicon substrate that has a 200 mm diameter. It was grown on the same reactor and the silicon substrate has the same resistivity range. The epitaxy is a little bit thicker in this case (4.05 µm instead of 3.9 µm) and therefore the buffer layers do not have exactly the same thickness. However, it does not hinder the parallel between traps that are present in the epitaxy for transistor and the one for diodes. As for the transistor, Atomic Layer Etching (ALE) [302] was used to obtain the recessed gate architecture as illustrated in **Figure 90** splitting the 2DEG in two. The latter allows the normally-off operation for the transistor. After the surface cleaning step, a dielectric layer is deposited by Atomic Layer Deposition (ALD) [303]. The metallization and passivation layers engineering allows building the field plate structure as shown in **Figure 90**. At the gate side, three field plates: a gate field plate

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(with a length Fpg) and two source field plates (with a length Fps1 and Fps2) are formed whereas at the drain side, three field plates are present. Those field plates are designed to meet the breakdown voltage and the current collapse requirements [84].

The electrical measurements again were performed using the Multi-Frequency Capacitance Measurement Unit (MFCMU) and the High-voltage Source Measurement Unit (HVSMU) of the Keysight® B1505 power device analyzer mixed with the N1260A Bias Tee. The drain voltage was swept from 0 V to 200 V with a step of 2 V. The gate is biased to have a voltage between the gate and the source (V_{GS}) equal to -2 V whereas the substrate is grounded. The small signal has a frequency of 1 MHz and an amplitude of 40 mV. The measurements were performed under dark illumination. The integration time was done over two Power Line Cycles (PLC). To be able to tune the ramp rate (verified with time monitoring during the whole sweep), the delay time was adjusted: 1 ms for 7 V/s and 360 ms for 3 V/s. It was chosen to perform the study on the Miller capacitance: C_{RSS}. It could have been done on the output capacitance: C_{OSS} which is expected to give similar results because both depend on the 2DEG depletion.

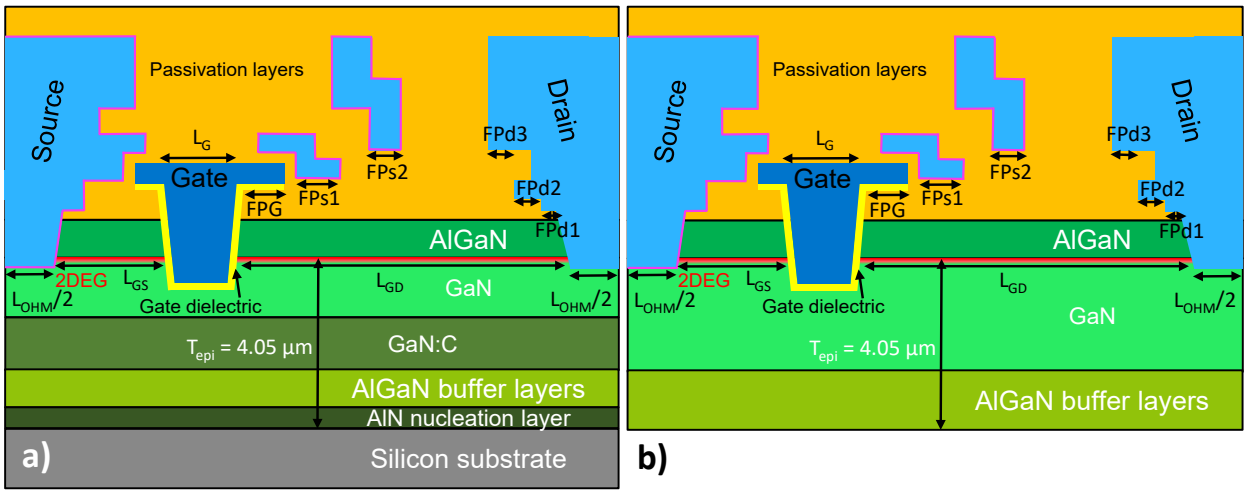

Figure 90: Transistor cross-section [301] of (a) the experimental (b) the simulated transistor.

The same TCAD simulation features described in the previous part (III.2.a.i) are reused. Especially, the substrate simplifications presented in the first part are taken for granted.

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Piezoelectric model in buffer layers is turned off here (capacitance curves do not vary with it for transistors).

III.2.b.i.2nd Preliminary Study

To begin with, a preliminary study was proposed to evaluate the variation of atomic species when the Growth Rate (GR) used for the Carbon doped GaN (GaN:C) growth on test wafers. The atomic concentrations were monitored with Secondary Ion Mass Spectroscopy (SIMS). The growth rate used were 5.8 µm/h and 10 µm/h. The concentrations of carbon, oxygen and hydrogen are reported in **TABLE 7**. On the one hand, the only species that varies with the GaN:C epitaxial growth rate is the carbon. Its concentration increases significantly with the growth rate. In addition, its concentration increases as the epitaxy is growing, this is why the top and the bottom concentrations on the GaN:C layer are reported in **TABLE 7**. The carbon content is inherent to the growth technique that uses precursors with carbon atoms: TrimethylGallium (TMGa) (and TrimethylAluminium (TMAl) in $Al_xGa_{1-x}N$). On the other hand, the oxygen and the hydrogen concentrations are different in the GaN buffer layers or in the III-V buffer ($Al_xGa_{1-x}N$ and AlN layers). The oxygen content is constant in the III-V buffer and is roughly equal to 1 a.u. whereas it is in between 0.3 to 0.5 a.u. in the GaN buffer. The hydrogen content is also inherent to the growth technique because it comes with TMGa, TMAl and ammonia (NH_3) precursors. Its concentration is equal to 3-7 a.u. in the GaN buffer whereas in the III-V buffer, it is equal to 7-9 a.u.

These information will be useful to either test if the carbon may be involved in the capacitance temperature dependence or verify the hypothesis on the possible origin of trap related to the temperature dependence.

TABLE 7: Atomic concentrations in the GaN epitaxy depending on the different studied GaN:C epitaxial growth rate [301].

GaN:C Epitaxial Growth Rate (µm/h)	$[C]_{GaN:C,\ top}$ (a.u.)/ $[C]_{GaN:C,\ bottom}$ (a.u.)	$[O]_{GaN\ buffer}$ (a.u.)/ $[O]_{III\text{-}V\ buffer}$ (a.u.)	$[H]_{GaN\ buffer}$ (a.u.)/ $[H]_{III\text{-}V\ buffer}$ (a.u.)
5.8	100/20	0.3-0.5/1	3-7/7-9
10	300/50	0.3-0.5/1	3-7/7-9

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III.2.b.ii Experimental Study

III.2.b.ii.1st Indirect Assessment of the Carbon Role on the Capacitive Temperature Dependence Through the GaN:C Epitaxial Growth Rate Change

First and foremost, by looking at the non-linear capacitance characteristic of the transistor at a given temperature (and ramp rate) as shown in **Figure 91(a)**, three depletion voltages can be identified. They correspond to the voltage for which the capacitance drops as already seen with diode. Physically, they respectively correspond to the 2DEG depletion under the gate field plate, the source field plates that has first a Fps1 length (in **Figure 90(a)**) and a Fps2 length after. Focusing our attention on the temperature dependence at a given Growth Rate (GR) (and ramp rate), it can be seen that the temperature dependence concerns only the depletion voltages. To be more precise, they decrease with the temperature. For amplitude reason, this study will be focused on the third one. For this study, it will be defined as the voltage for which the capacitance is equal to 0.005 pF/mm.

Moving on to the growth rate dependence, 5.8 µm/h and 10 µm/h were studied at a fixed ramp rate of 3 V/s. In **Figure 91(b)**, by comparing both growth rates, the decreasing trends differ only by their value at 25°C. The 5.8 µm condition (in blue) has a higher depletion voltage.

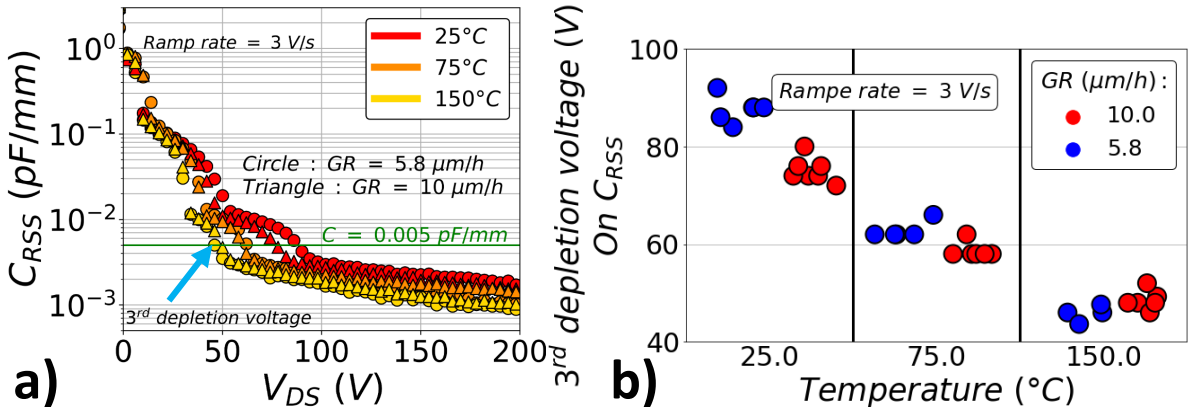

Figure 91: For two different GaN:C epitaxial growth rates (a) $C_{RSS}(V_{DS},T)$ experimental curves of representative transistors (transistors having a median behavior among the tested transistors) with V_{GS} = -2 V [301] (b) 3rd depletion voltage temperature dependence for several devices as a function of the GaN:C epitaxial growth rate [301].

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However, with respect to the significant induced change in the carbon content as exposed in **TABLE 7**, the capacitance temperature dependence seems not correlated with that parameter.

The theoretical expression of the depletion voltage as proposed by Ishida *et al.* in [304], proposes a linear dependency with the depleted charge as described with the following equation:

$$V_D = \frac{\sigma_{GaN}}{\epsilon_r} \times d$$

Equation 12: Depletion voltage expression (σ_{GaN}: surface charge density that is depleted; ϵ_r: relative permittivity of the depleted region; d: depleted distance).

This formula can be applied in our case considering that the capacitive coupling of field plate locally depletes the 2DEG underneath it (as exposed in the study of Weiss *et al.* [148]). To verify if the electron density in the 2DEG: N_S would be responsible for the capacitance temperature dependence, measurements were performed on 200×200 µm² Gated-Van Der Pauw structure (Schematics of the test structure in Figure 4 of [270]). The capacitance measurements exposed in **Figure 92(a)** were performed with a small signal of 40 mV at a frequency of 1 kHz. The integration of the obtained capacitance characteristics for the three temperatures of this study (25°C, 75°C and 150°C) and the two growth rates are summarized in **Figure 92(b)**. It can be seen that the electron density in addition of being independent on the growth rate, is rather constant with temperature even though a slight increase may be seen. Therefore, the decrease in depletion voltages cannot be explained by the electron density and would rather come from the non-ideality of the system: traps.

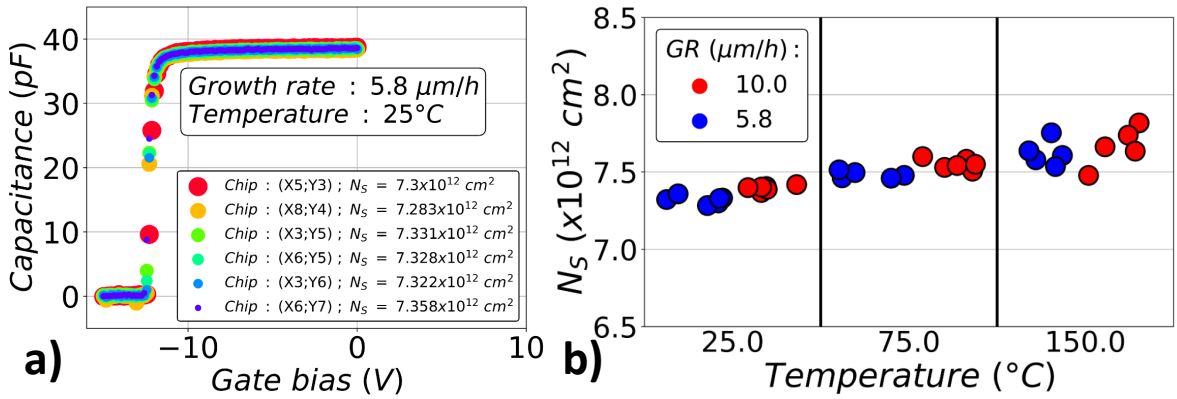

Figure 92: (a) Gated Van Der Pauw capacitance versus voltage characteristic [301] (b) Electron density (extracted from the Gated Van der Pauw measurements) as a function of the temperature for two different growth rates [301].

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III.2.b.ii.2nd Second Temperature Dependence Through DC Bias Ramp Rate Variation

To confirm the trap origin of this temperature dependence, the DC bias Ramp Rate (RR) was varied from 3 V/s to 7 V/s for a given growth rate of the GaN:C layer (5.8 µm/h). On the raw characteristics in **Figure 93(a)**, the difference can be seen only for the curve corresponding to 75°C. The depletion voltage at this temperature follows the ramp rate trend. Furthermore, this observation is valid for several devices as shown in **Figure 93(b)**. Therefore, the time and the temperature dependence of the capacitance characteristics is similar to the trapping capture kinetics. Thus, buffer traps will be studied in the next part.

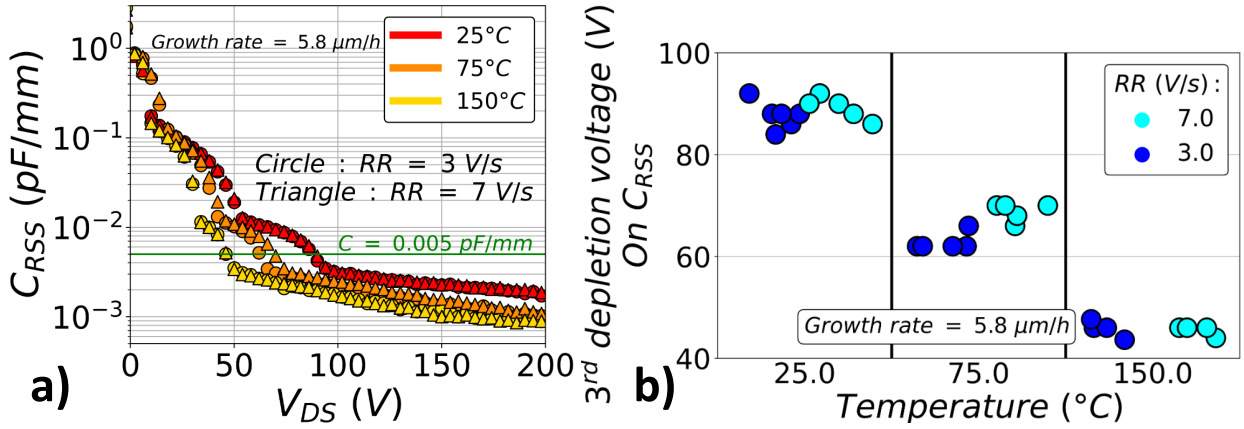

Figure 93: For two different DC ramp rates (a) $C_{RSS}(V_{DS},T)$ experimental curves of representative transistors (transistors having a median behavior among the tested transistors) with V_{GS} = -2 V [301] (b) 3rd depletion voltage temperature dependence for several devices as a function of the DC bias ramp rate [301].

III.2.b.iii TCAD Qualitative Simulation Study of Buffer Traps

TCAD simulations will be used to study the qualitative behavior of buffer traps (especially acceptor traps) on the capacitance temperature dependence. To do so, the auto-compensation model has been used [137]. Deep acceptors trap at 0.9 eV from the valence band with shallow donor traps at 0.11 eV from the conduction band are used simultaneously in the buffer to simulate AlGaN/GaN device [281], [305], [306]. Indeed, it allowed reproducing the semi-insulating properties of carbon-doped layers as described by Uren *et al.* [267] to be able to explain several unexpected characteristics such as the dynamic electric field variation [307], the current collapse [308]–[310], the threshold voltage instabilities [311] and the backgating transient measurements [290]. The deep

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acceptor traps at 0.9 eV from the valence band are related to the carbon in N-site: C_N based on calculation with the generalized Kohn-Sham scheme and the hybrid functional of Heyd, Scuseria, and Ernzerhof (HSE) performed by Lyons *et al.* [40]. Whereas the shallow donor traps come from Amstrong *et al.* study in which the extracted energy level of 0.11 eV from Steady-State PhotoCapacitance (SSPC) spectra has been attributed to carbon on Ga-site: C_{Ga} [312]. In our study, only the trap position in the gap proposed in this model will be used. The trap level origin (the one of acceptor traps) will be discussed within sections III.2.b.iv and III.2.b.v.

Within the TCAD simulation, these traps are uniformly distributed in the equivalent place of the GaN:C in **Figure 90(a)** and in the AlGaN buffer layer in **Figure 90(b)**. To obtain in simulation, the electron density of the 2DEG at 25°C (GaN:C epitaxial growth rate of 5.8 µm/h): 7.35×10^{12} cm^{-2} as reported in **Figure 92**, the piezoelectric model was activated at 77 %. To begin with the traps' concentration (acceptor and donor type together) was chosen to be roughly equal to 5×10^{18} cm^{-3} and the initial compensation value was set to 99.4 % as in [290].

Several splits were proposed in **TABLE 8** and studied to understand how do they affect the capacitance temperature dependence trend. The used trap concentration are in the same range as the one used in the following references [267], [291], [292]. All the simulations were performed at 3 V/s. First, the acceptor traps' energy level (split 1, 2 and 3) impact was analyzed to understand how do their ionization change the temperature dependence. Secondly, donor traps' density was varied (split 2, 4 and 5) to confirm the temperature dependence origin hypothesis. Meanwhile, the absolute traps' concentration will be changed while keeping the acceptor and donor traps' concentration difference ([A] – [D]) constant (split 5 and 8) to demonstrate that the [A] – [D] quantity is very important in our case to get the same temperature dependence. Finally, the acceptor traps' hole capture cross section will be varied (split 5, 6 and 7) in order to assess its role on the temperature dependence.

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TABLE 8: TCAD simulations split table (changed parameter in red) [301].

Split	E_A-E_V (eV)	[A] (cm^{-3})	σ_{A,h^+} (cm^2)	E_C-E_D (eV)	[D] (cm^{-3})
1	0.6	2.5×10^{18}	1×10^{-16}	0.11	2.485×10^{18}
2	0.9	2.5×10^{18}	1×10^{-16}	0.11	2.485×10^{18}
3	1.3	2.5×10^{18}	1×10^{-16}	0.11	2.485×10^{18}
4	0.9	2.5×10^{18}	1×10^{-16}	0.11	2.44×10^{18}
5	0.9	2.5×10^{18}	1×10^{-16}	0.11	2.4×10^{18}
6	0.9	2.5×10^{18}	1×10^{-17}	0.11	2.4×10^{18}
7	0.9	2.5×10^{18}	1×10^{-15}	0.11	2.4×10^{18}
8	0.9	1×10^{19}	1×10^{-16}	0.11	0.99×10^{19}

III.2.b.iii.1st The Deep Acceptor Traps' Energy Dependence

The acceptor traps' energy level was studied through three different energy levels with respect to the valence band: 0.6 eV, 0.9 eV and 1.3 eV (split 1, 2 and 3 in **TABLE 8** respectively). **Figure 94** represents the capacitance temperature dependence for each energy level (5a, 5b and 5c respectively). The temperature dependence is observable only for 0.9 eV with respect to 0.6 eV and 1.2 eV for which all the curves in temperature are superimposed.

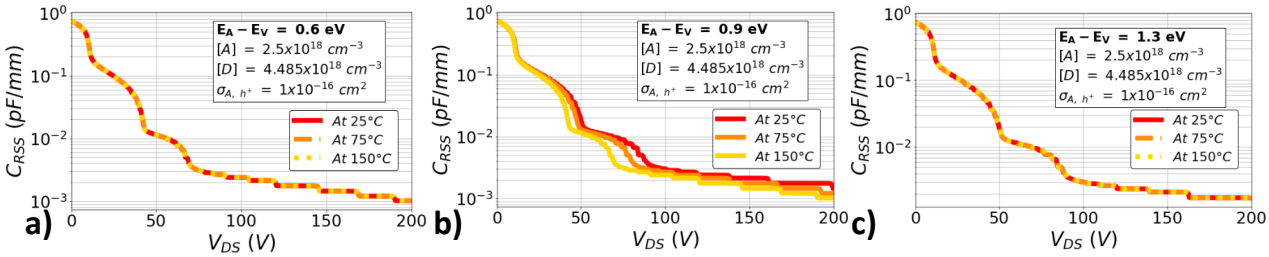

Figure 94: Simulated $C_{RSS}(V_{DS})$ at three different temperatures (25°C, 75°C and 150°C) for different energy levels for the acceptor traps [301]: (a) 0.6 eV (Split 1) (b) 0.9 eV (Split 2) (c) 1.3 eV (Split 3).

The contribution of the excess acceptor trap ionization on the 2DEG can be proposed to explain the temperature dependence by carefully looking at **Figure 95**. Indeed by comparing the excess acceptor traps' ionization (in red in the colormap) at 0 V and 75 V for the two extremum temperatures (25°C and 150°C), it can be seen that there are more excess ionized acceptor traps at 75 V and 150°C (**Figure 95(d)**). The excess acceptor traps' ionization distribution is the same in

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all the other conditions: pinned at the interface between the UID GaN (without trap region) and the region in which traps were inserted. These excess acceptor traps' ionization corresponds to fixed negative charges that are therefore more numerous in the case at 75 V and 150°C. Thus to keep the same electrostatic equilibrium (same number of negative charges) from 25°C to 150°C, some charges (electrons) in the 2DEG have to be removed explaining the more advanced depletion of the 2DEG at high temperature (at a given bias). This means that the depletion voltage reduction when increasing the temperature is due to the temperature dependence of the excess acceptor traps' ionization with respect to the already ionized shallow donor traps.

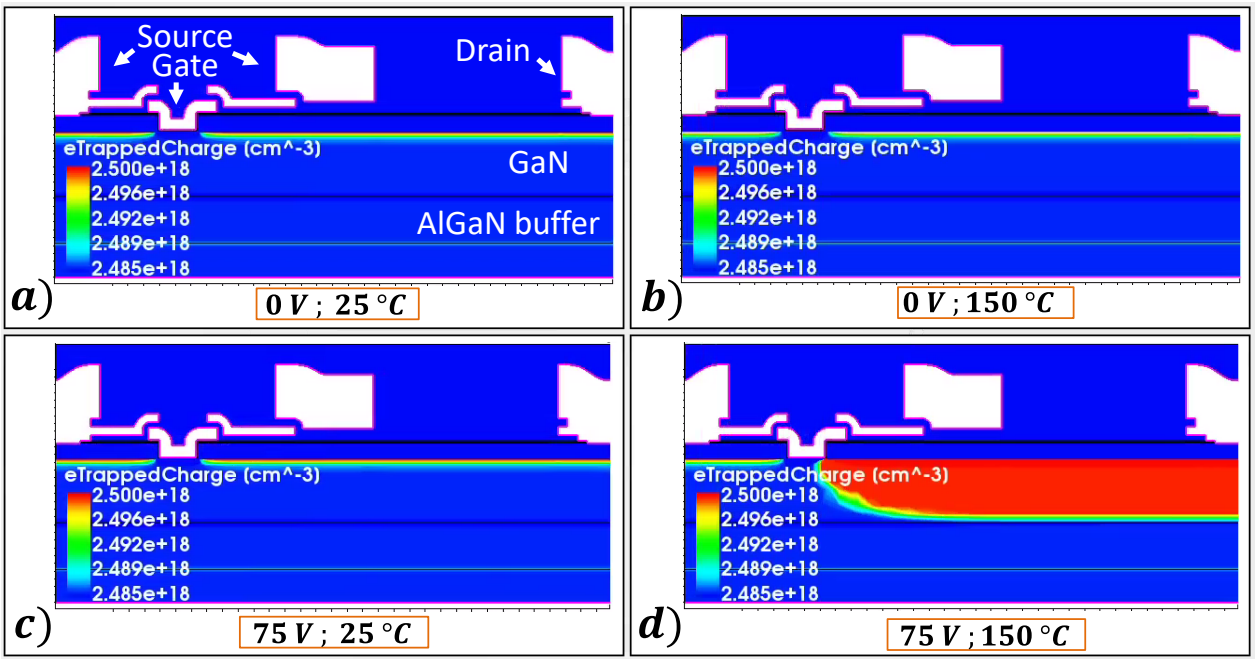

Figure 95: Acceptor trap ionization mapping in TCAD for E_A-E_V = 0.9 eV (split 2) [301] at (a) V_{GS} = -2 V; V_{DS} = 0 V; T = 25°C (b) V_{GS} = -2 V; V_{DS} = 0 V; T = 150°C (c) V_{GS} = -2 V; V_{DS} = 75 V; T = 25°C (d) V_{GS} = -2 V; V_{DS} = 75 V; T = 150°C. The lower tick parameter of the colored scale corresponds to the concentration of the donor traps.

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III.2.b.iii.2nd The Traps' Concentration Dependence

Focusing our attention on the traps' concentration, first the impact of the absolute donor traps' concentration: [D] is studied. This is performed keeping the acceptor traps' density equal to 2.5×10^{18} cm^{-3} while varying the concentration of donor traps' from 2.4×10^{18} cm^{-3} to 2.485×10^{18} cm^{-3} as illustrated in **Figure 96(a)**. As it can be seen, when the donor traps' concentration is reduced, the amplitude of the third depletion voltage (V3) with temperature is increased. This goes in the direction of the proposed hypothesis. Indeed, the decrease in the donor traps' concentration implies a higher number of possible excess acceptor traps' ionization which leads to a larger 2DEG depletion difference at a given bias between two different temperatures.

Moreover, if one changes the absolute concentration of acceptor and donor traps at the same time keeping the difference between both: [A] - [D] constant, it does not change the capacitance temperature dependence as it can be seen in **Figure 96(b)** (for which [A] - [D] = 1×10^{17} cm^{-3} and [A] + [D] has been changed from 0.99×10^{19} cm^{-3} to 3.99×10^{19} cm^{-3} which respectively corresponds to split 5 and 8 in **TABLE 8**). Again, this is because the number of excess acceptor traps that can be ionized with temperature does not change.

Hence, these two last paragraphs with their observations validate the proposed hypothesis for which the ionization of the excess acceptor traps with respect to the shallow donor traps (assuming that all the shallow donor traps are entirely ionized) is responsible for the capacitance temperature dependence. Thus, the latter depends on the one hand on the quantity [A] - [D] and on the other hand on the acceptor trap properties.

III.2.b.iii.3rd The Deep Acceptor Trap Hole Cross-section Dependence

Having summarized the different dependencies of the capacitance temperature variation, the role of deep acceptor trap hole capture cross-section remains to be seen. It was investigated by varying this parameter from 1×10^{-17} cm^2 to 1×10^{-15} cm^2 (corresponding to splits 5, 6 and 7 in **TABLE 8**). The third depletion voltage (V3) as a function of the temperature for these cross-sections has been displayed in **Figure 96(c)**. The main difference stands at 75°C, in which the depletion voltage is lowered for a higher cross-section. This is still in accordance with the presented hypothesis because the higher the cross-section, the higher the probability for an acceptor

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trap to be ionized thus leading to a higher number of negative fixed charges and as a consequence a larger 2DEG depleted area in the same bias and temperature conditions.

Hence, from this qualitative TCAD simulation study, several things were enhanced:

1. The transistor capacitance negative temperature dependence rises from the presence of excess deep acceptor traps' ionization with respect to the ionized shallow donor traps,
2. The excess ionized acceptor traps' concentration is responsible for the amplitude of the depletion voltage variation with temperature,
3. The deep acceptor traps' properties (energy level and hole capture cross-section) determine if and how the temperature dependence will occur between 25°C and 150°C.

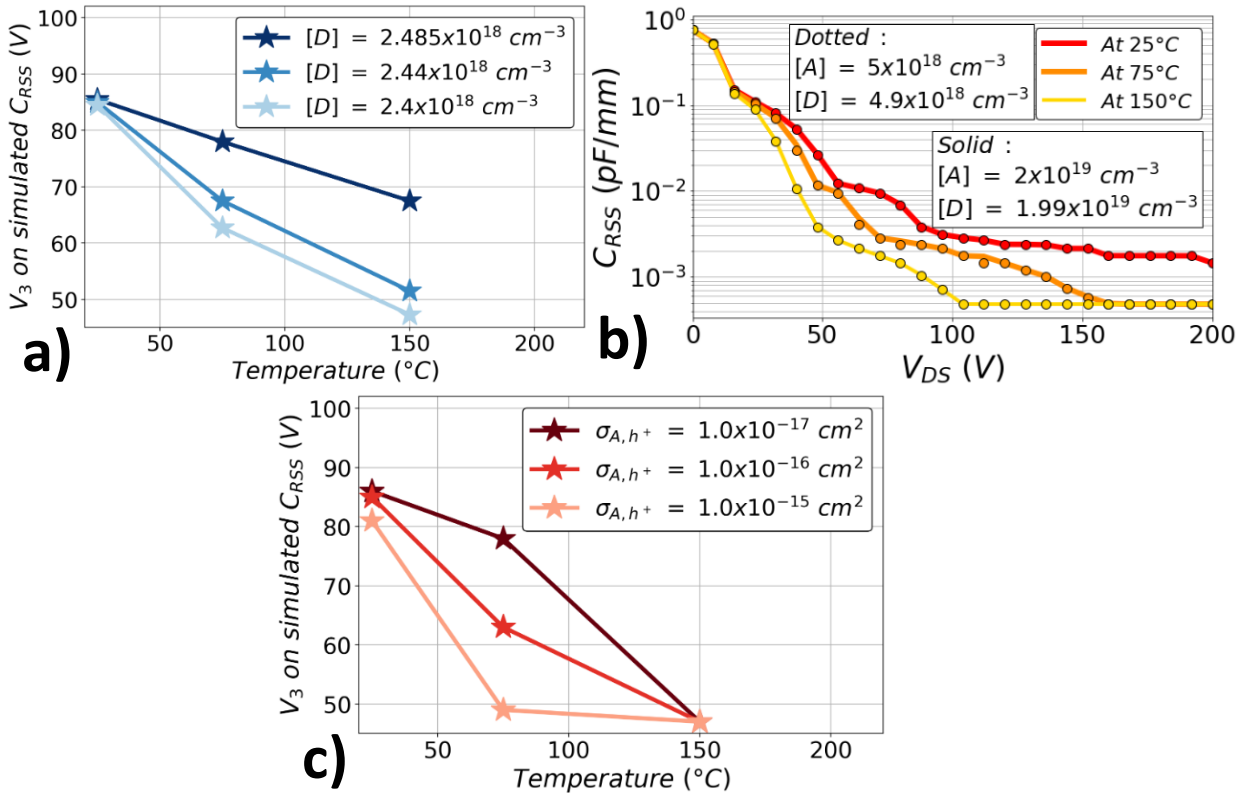

Figure 96: TCAD simulation results [301]: (a) Third depletion voltage (V3) as a function of temperature for different donor traps' concentrations (Splits 2, 4 and 5) (b) $C_{RSS}(V_{DS},T)$ for different absolute acceptor and donor traps' concentrations, keeping [A] - [D] = 1×10^{17} cm^{-3} (split 5 and 8) (c) The third depletion voltage (V3) as a function of the temperature for deep acceptor trap hole cross-section (splits 5, 6 and 7).

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III.2.b.iv TCAD Fit on the Experimental Data and the Possible Interpretations

After having learnt in TCAD simulation how does the capacitance temperature dependence vary with the different available parameters (traps' concentration, traps' energy level, trap capture cross-section), fits can be made. The parameters used in simulation to achieve it:

- [A] - [D] = 1×10^{17} cm^{-3}. This is not unusual because it has already been used in several articles [281], [285], [290].
- The couple : E_A-E_V = 0.9 eV and $\sigma_{A,h^+} = 1\times10^{-16}$ cm^2

This was done for a ramp rate of 3 V/s (**Figure 97(a)**) and the trap kinetics was confirmed with 7 V/s (**Figure 97(b)**). These figures show a very good match in terms of depletion voltage. Nevertheless, at high temperature: 75°C and 150°C, the simulation curves differ a little bit from the experimental ones after 100 V. The capacitance plateau (observable at high voltage when the 2DEG is completely depleted) is reached at lower voltage in simulation for these temperatures. The trap non-uniform distribution in the real device is the main proposed hypothesis, as it will be detailed a little bit further.

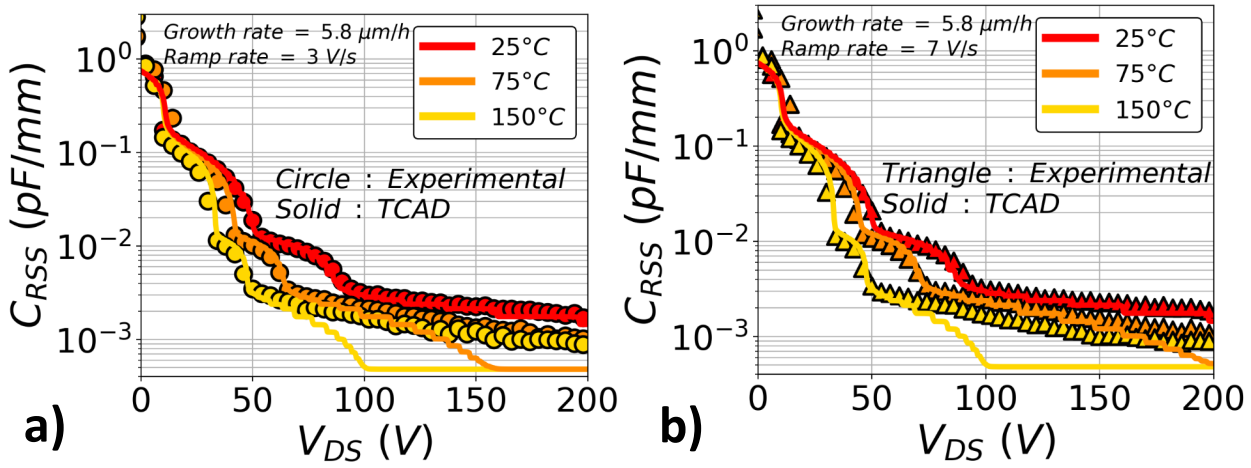

Figure 97: TCAD fit of the experimental data (GaN:C epitaxial growth rate of 5.8 µm/h) [301] for two different ramp rates of (a) 3 V/s (b) 7 V/s using the following TCAD parameters: [A] - [D] = 1×10^{17} cm^{-3}; E_A-E_V = 0.9 eV; $\sigma_{A,h^+} = 1\times10^{-16}$ cm^2.

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Moreover, the couple (E_A-E_V ; σ_{A,h^+}) is not the unique solution to make the fit. Several possible couples were found for energy levels from 0.8 eV to 1.0 eV as shown with the red dots in **Figure 98**. In this energy range, the different points follow an exponential relationship (black curve). The comparison of these points with the literature reported deep acceptor traps [289], [313]–[321], focusing our attention in this energy range, allows discarding involving carbon on the N-site alone: C_N, gallium vacancy alone: V_{Ga} or tied to a silicon atom on the Ga-site: V_{Ga}-Si_{Ga} because of the hole capture cross-section huge difference. Remaining possible traps are associated with oxygen atom(s) on the N-site. This is a key element that will be used in the next paragraph to assess that the properties of the trap in the study of Polyakov *et al.* [320] can fit the experimental data meaning that gallium vacancy tied to oxygen atom(s) on the N-site could be the defect related to the capacitance temperature dependence.

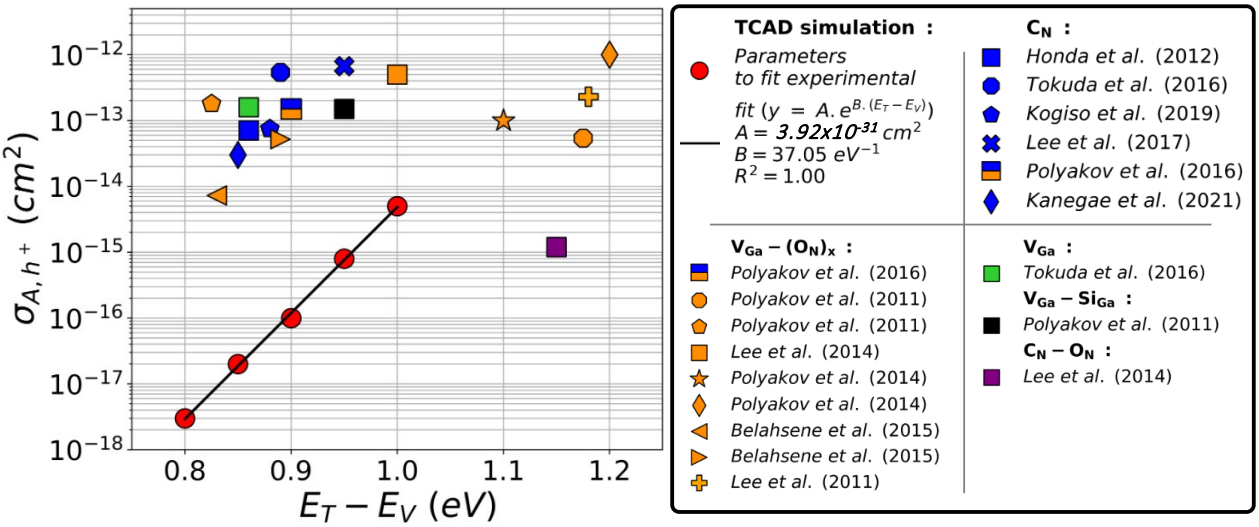

Figure 98: Acceptor trap cross-section as a function of their position in the gap (Energy level with respect to the valence band ranging from 0.8 eV to 1.2 eV) [301]. Each hypothesis proposed by the authors [289], [313]–[321] has a given color (C_N: carbon on the N-site; V_{Ga}-$(O_N)_x$: gallium vacancy with oxygen atom(s) on the N-site; V_{Ga}: gallium vacancy; V_{Ga}-Si_{Ga}: gallium vacancy with a silicon atom on the Ga-site; C_N-O_N: carbon on the N-site with an oxygen atom on the N-site).

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III.2.b.v V_{Ga}-$(O_N)_x$ Hypothesis Verification

Fitting the experimental data using energy level in the [1.0; 1.2] eV range with the previous consideration (acceptor and donor traps' concentration: [A] & [D] arbitrarily chosen while [A] - [D] is constant and equal to 1×10^{17} cm^{-3}) was not possible. In this energy range, the choice of the traps' concentration matters because it plays a role on the position of the depletion voltage at 75°C as the hole cross-section. The limits of the previous approach is possibly due to the distribution of the excess acceptor ionized traps as it can be seen in **Figure 99**. Indeed, their distribution is uniform for 0.8 eV and 0.9 eV whereas it begins to be non-uniform for 1.0 eV with a maxim at the interface between the region with traps and the top UID GaN (without traps) layer. Thus, the following hypothesis was proposed: as long as the excess acceptor trap ionization distribution is approximately constant, the previously made qualitative study is valid.

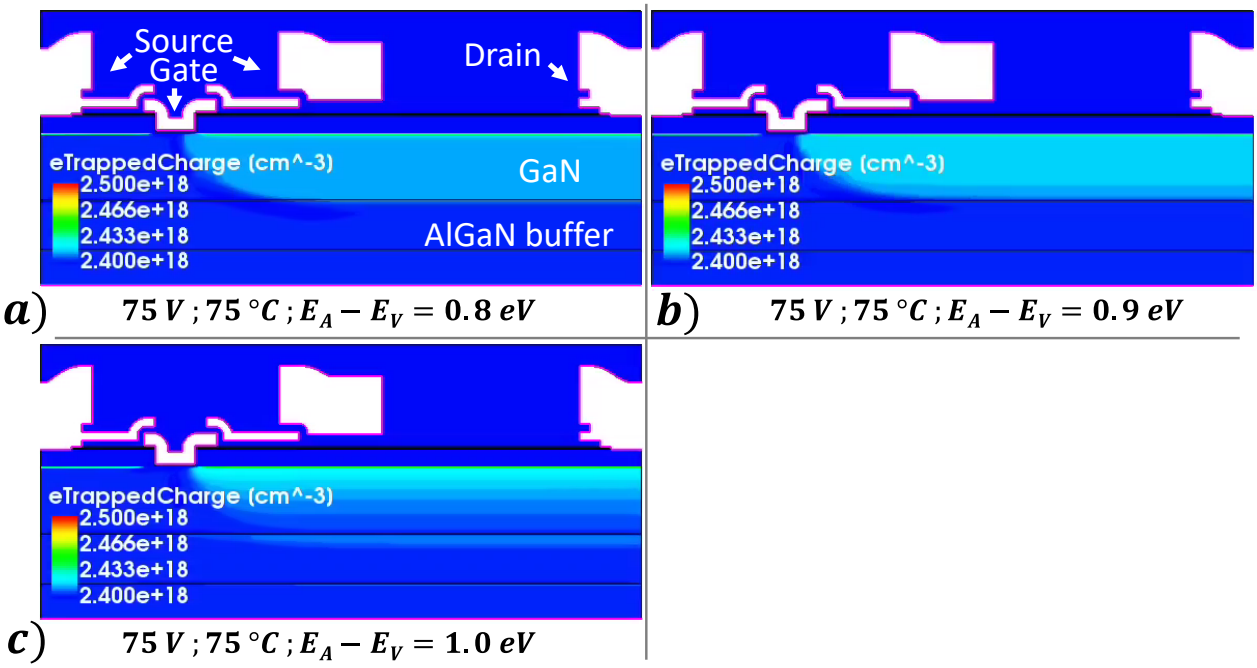

Figure 99: Acceptor trap ionization mapping in TCAD simulations for V = 75 V; T = 75°C and [A] - [D] = 1×10^{17} cm^{-3} [301] with: (a) E_A-E_V = 0.8 eV; $\sigma_{A,h^+} = 3\times10^{-18}$ cm^2 (b) E_A-E_V = 0.9 eV; $\sigma_{A,h^+} = 1\times10^{-16}$ cm^2 (c) E_A-E_V = 1.0 eV; $\sigma_{A,h^+} = 5\times10^{-15}$ cm^2. The lower tick parameter of the colored scale is set to the donor traps' concentration.

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As mentioned earlier, the remaining defect hypotheses are related to oxygen on the N-site meaning as the traps' concentration matters for higher energy range, the deep acceptor traps' concentration can be curved by the oxygen concentration measured by Secondary Ion Mass Spectroscopy (SIMS) as reported in **TABLE 7** keeping of course the same quantity [A] - [D] as previously. Thus for the forthcoming fit (exposed in **Figure 100**), the top 200 nm of the UID GaN were free of traps, the concentration of acceptor traps: [A] was equal to 0.5 a.u. in the remaining GaN layers of **Figure 90(b)** and equal to 1 a.u. in the $Al_xGa_{1-x}N$ buffer layers of **Figure 90(b)**. As for the trap properties, those reported in the study of Polyakov *et al.* [320] (E_A-E_V = 1.1 eV and $\sigma_{A,h^+} = 1\times10^{-13}$ cm^2) were used and were the only properties enabling a good fit. Hence, the origin of the capacitance temperature dependence of the studied transistors could come from V_{Ga}-$(O_N)_x$.

Furthermore, this fit (**Figure 100**) matches better the experimental curves (after 100 V) with respect to the one in **Figure 97(a)**. They especially differ in the spacial distribution of traps. A closer trap distribution to the real device as exposed in **Figure 100** leads to a better match. Thus, a very good fitting on the trap distribution would lead to an even better fit.

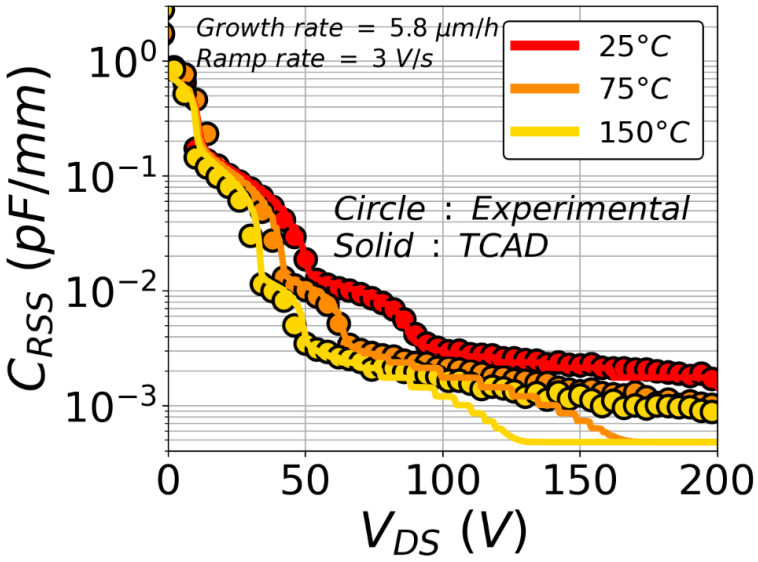

Figure 100: TCAD fit of the experimental data (GaN:C epitaxial growth rate of 5.8 µm/h and a ramp rate of 3 V/s) [301]. The simulation has been performed with [A] is equal to 1 a.u. in the $Al_xGa_{1-x}N$ buffer layers and 0.5 a.u. in the GaN except for the last two hundred nanometers. In addition of [A] - [D] = 1×10^{17} cm^{-3}; E_A-E_V = 1.1 eV and $\sigma_{A,h^+} = 1\times10^{-13}$ cm^2.

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To conclude, it was shown by means of experimental study correlated with TCAD simulations that the Miller and output capacitance temperature dependence, from 25°C to 150°C, of fully-recessed AlGaN/GaN MOS-HEMT, made on a 200 mm GaN-on-Si epitaxy is due to the presence of deep acceptor traps which could be related to gallium vacancy tied to oxygen atom(s) on the N-site. This was performed by first experimentally analyzing the temperature variation of the depletion voltage as a function of the GaN:C epitaxial growth rate and the voltage sweep rate. This step discards the carbon from being responsible for the temperature dependence and highlights its similarity with trapping kinetics. The TCAD qualitative study of the different trap parameters allowed the identification of the most relevant parameters and qualify their impact on the temperature-dependent characteristics. It clearly showed that the temperature-dependent ionization of the deep acceptor traps (or its excess with respect to the already ionized shallow donor traps) is responsible for the early depletion of the 2DEG causing the negative shift of the depletion voltage on the capacitance characteristics. Finally, fitting the experimental curves at all temperatures was performed. This was especially done with deep acceptor trap properties (energy level and hole capture cross-section) reported in the literature corresponding to V_{Ga}-$(O_N)_x$. Their concentration was bound to the experimental oxygen concentration measured in the epitaxy by SIMS.

Having identified a potential buffer trap, it was proposed in the next section to assess if the insertion of the trap is sufficient to model the device electric field.

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III.2.c Implementation of Deep Acceptor Traps in the Simulated AlGaN/GaN Schottky Diode and Evaluation of the Electric Field Change

The buffer traps were implemented into the diode architecture ([A] = 1×10^{17} cm^{-3}; E_A-E_V = 1.1 eV and $\sigma_{A,h^+} = 1\times10^{-13}$ cm^2, [D] = 5×10^{14} cm^{-3} [5]; E_C-E_D = 0.11 eV and $\sigma_{D,e^-} = 1\times10^{-15}$ cm^2) except in the last 500 nm. Looking at the capacitance temperature dependence in between the simulations and the experimental measurements in **Figure 101**, it can be observed that as in the transistor capacitance characteristic, there is an early depletion of the 2DEG. This phenomenon is enhanced by temperature leading to the plateau observed for 75°C and 150°C. This is again supposed to be associated with the non-uniform traps' concentration in the buffer.

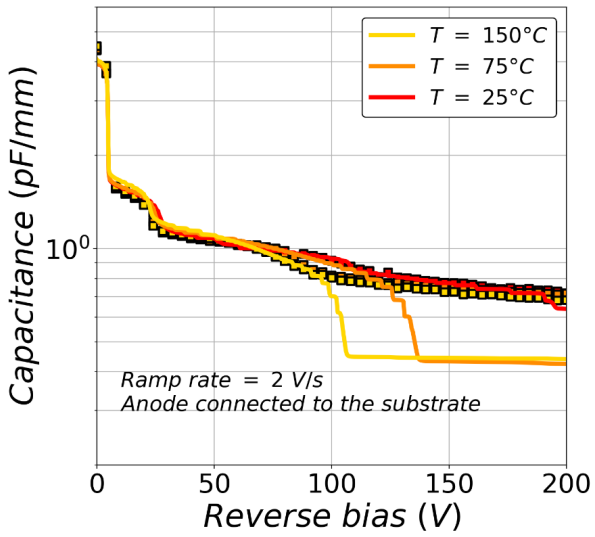

Figure 101: Capacitance temperature dependence of the diode obtained with experimental measurements (squares) and in TCAD simulations (continuous lines) at a ramp rate of 2 V/s.

[5] With respect to the study performed on transistors, using a donor concentration of 1×10^{15} cm^{-3} slightly lowers the capacitance characteristics of the simulated diode. The origin was not investigated because on the one hand, the change in [D] from 1×10^{15} cm^{-3} to 5×10^{14} cm^{-3} allows a [A] – [D]= 1×10^{17} cm^{-3}. On the other hand, this condition potentially depends on the donor trap properties (E_C-E_D, σ_{D,e^-}) that were chosen according to the literature and not thanks to experimental measurement in this manuscript. This may change with more experimental investigations.

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As there is no specific remark going against the implementation of these buffer traps, their impacts on the electric field distribution need to be analyzed. As performed before, this is realized comparing the FPG0-1 and the LAC-16 layout with the substrate floating on their electric field distribution at 1700 V with the epitaxy 1. Indeed the experimental breakdown voltage comparison has been analyzed in II.3.b.ii.1st showing that the FPG0-1 layout has the highest breakdown voltage. The electric field comparison displayed in **Figure 102** was performed along a cutline at 1 nm under the first anode field plate because the breakdown location for these layouts was shown to occur at the edge of the first field plate corner (II.3.b.ii). As a precaution, this comparison is made with and without piezoelectric model in the buffer layers. And, this is all the more interesting here because the relative variation changes in between layouts changes depending on the piezoelectric model activation in the buffer layers. Here are the different observations:

- Introducing buffer traps (with an acceptor traps dominance) reduces the amplitude of the electric field peak at the anode and increases at the cathode (comparing **Figure 102(a)** with **(c)** and **Figure 102(b)** with **(d)**).
- With the buffer traps, the higher electric field peak at the anode is visible for the FPG0-1 layout when the piezoelectric model is not activated in the buffer layers (see **Figure 102(d)**) whereas it is visible for the LAC-16 layout when the piezoelectric model is activated in the buffer layers (see **Figure 102(c)**). The latter situation does correspond to the experimental results. The exact explanation of the relative difference between layouts with and without piezoelectric model in the buffer layers was not found. Nevertheless, as it can be seen by looking at the electrostatic potential mapping (in **Figure 103(a)** and **(b)**), the piezoelectric model in the buffer imposes that the buffer under the anode is dominated by the vertical electric field especially in particular along the purple line (dominated by the lateral electric field when it is not activated). This is due to the vertical leakage of 1×10^{-8} A/mm under the anode enhanced in **Figure 103(c)** that is not visible when the model is de-activated (**Figure 103(d)**).

Note: The absolute electric field values in the case where the piezoelectric model is activated in the buffer layers (**Figure 103(a)** and **(b)**) are not realistics. Indeed peaks are higher than the critical electric field of the passivation layer in which the cutline was taken (reported to be close to 10 MV/cm [322]. This is due to the vertical electric field contribution as mentionned in the second point. Nevertheless, the point here is to stress that the presence of leakage current into deep buffer layers may be useful to reproduce the electric field peak relative variation between both studied layouts correponding to their experimental breakdown voltage difference.

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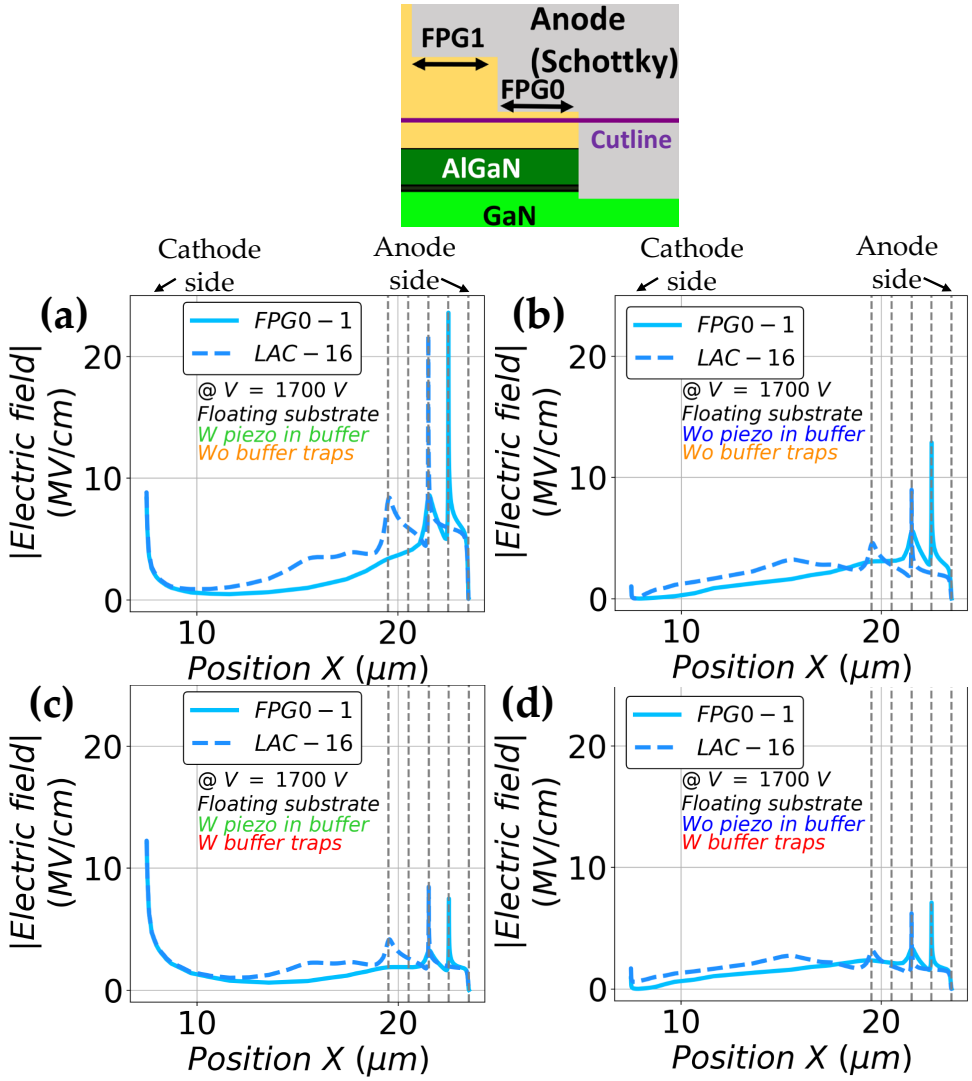

Figure 102: Absolute electric field distribution at 1700 V of the diode with the floating substrate along a cutline represented in purple as shown on the top of this figure: (a) With piezoelectric model in the buffer and without buffer traps (b) Without piezoelectric model in the buffer and without buffer traps (c) With piezoelectric model in the buffer and with buffer traps (d) Without piezoelectric model in the buffer and with buffer traps.

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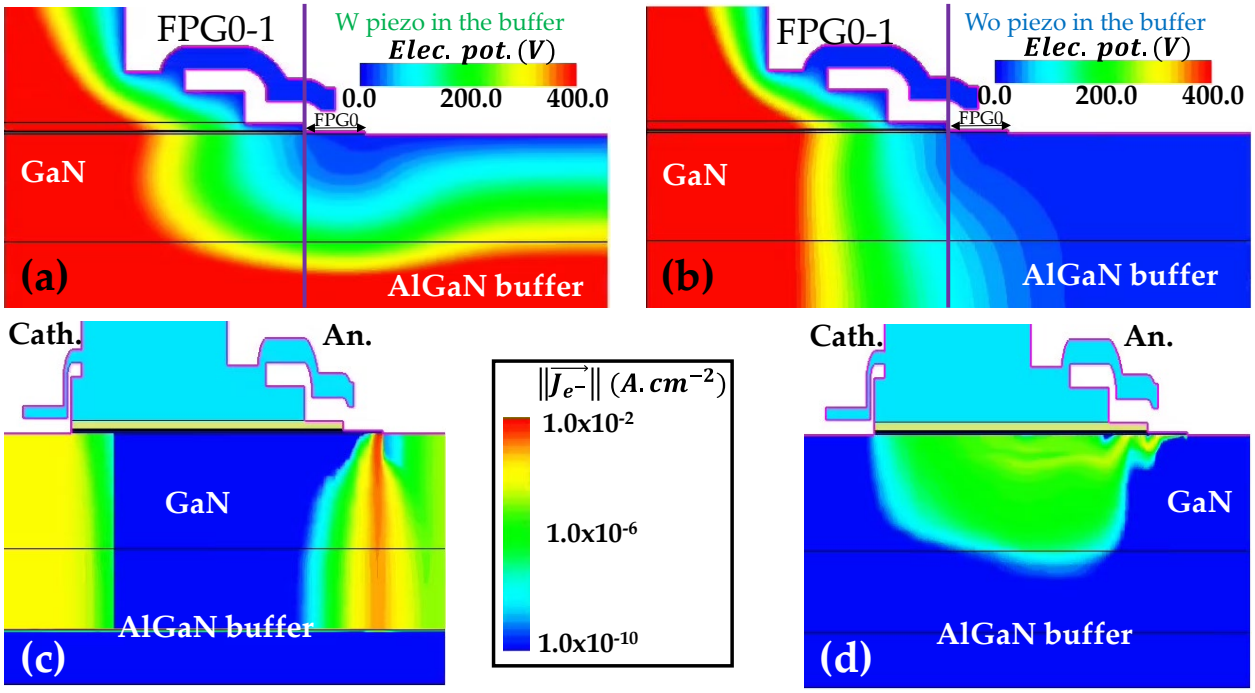

Figure 103: Electrostatic potential color mapping of the FPG0-1 layout at 1700 V with a floating back electrode (a) With the piezoelectric model activated in the buffer (b) With the piezoelectric model activated in the buffer.

Two conclusions rise from these two observations:

- The breakdown voltage layout dependence identified experimentally with the substrate floating may result from the presence of a leakage current passing through either the deep buffer layers or the substrate.
- The presence of the piezoelectric model in the buffer layer allows reproducing a vertical leakage. However, the obtained electric field value is rather incoherent (peaks are too high with respect to the GaN critical electric field) with the experimental results. Thus, the aforementioned leakage current passing through the deep buffer layers or the substrate may result from relaxed layers and/or a conduction through non-already identified traps such as threading dislocations.

This is why, on the one hand, the vertical current from the substrate to the cathode was investigated through its experimental temperature dependence, and, on the other hand, Deep Level Transient Fourier Spectroscopy (that probes traps impacting the electric field near the anode) was performed to potentially identify traps responsible for the electron injection in the substrate enhanced in **Figure 103(c)**.

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III.3 Buffer Charge Movement Modeling Through Vertical Current Temperature Dependence

As mentioned in the first part (III.1), the second step of the methodology consists in understanding how charges move in the buffer. This could lead to the identification of traps that may impact the electric field due to the presence of leakage path passing through these traps. To do so, a study on the vertical leakage was proposed. At first, a subpart is dedicated to the current status of the vertical current knowledge as well as the different charge transport mechanisms. In a second subpart, the temperature dependence of the vertical leakage will be studied through analytical modeling. This will potentially help us to identify the traps and the transport mechanisms that allow to interpret the experimental results. After that, the TCAD simulation study performed to grasp the impact of defect on the leakage current will be presented.

III.3.a Current Status on the Vertical Current Knowledge and the Different Reported Transport Mechanisms

III.3.a.i Current Status on the Vertical Current Knowledge

From the different past studies, three different regions can be identified as illustrated in **Figure 104**. The region numbered two and three were already exhaustively studied especially in the studies of Borga *et al.* [258] and Sayadi *et al.* [297]. They demonstrated that the current in the second region is limited by the thermal generation of electrons in the silicon substrate. Whereas the third region (before breakdown) is limited by the transport through the AlN/Si barrier that is potentially assisted by the huge density of traps in this area.

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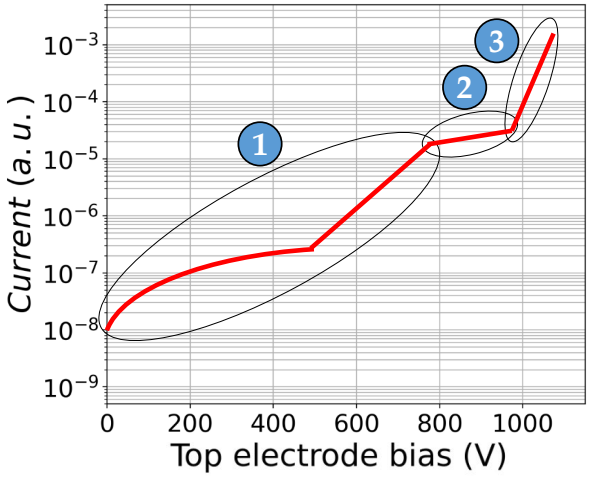

Figure 104: Different identified regions in a vertical generic curve.

Regarding the first region, there is no consensus on the conduction mechanism. It seems that it could be conduction in the volume. Indeed, mechanisms described within the following sections are reported in the literature. Nevertheless, to this day, no one has proposed yet an explanation for the entire regime of an entire GaN-on-Si epitaxy for power applications (meaning between zero volts to the voltage between regions 1 and 2 in **Figure 104**) at different temperatures yet.

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III.3.a.ii Ohmic Conduction

The first mechanism identified is the ohmic mechanism. It occurs when the traps are located near the band edges: conduction band for electron trap and valence band for the hole trap. Indeed, the thermal energy $K_B \times T$ is sufficient to allow the carriers to be emitted into the band. With the help of the electric field, these carriers are able to participate into the conduction as illustrated in **Figure 105(a)**. It was identified by means of a log(J) versus log(V) display of the vertical current characteristic with a slope of 1 as it can be seen in the study of Moens *et al.* [323]. In fact the current density is proportional to the voltage [60]. Moreover, as it depends on the carrier thermal generation and has an Arrhenius temperature dependence as described in the book of Sze [60] and used in the analytical model in the study of Lin *et al.* [324].

However, the slope at lower temperatures is not always equal to one as it can be seen in the study of Borga *et al.* [257]. Indeed as shown in **Figure 105(b)** a lower slope can be identified meaning that something else is regulating the current-voltage dependence at lower temperature. The only mechanism found that could explain this behavior is the recombination limited model as presented in the next section.

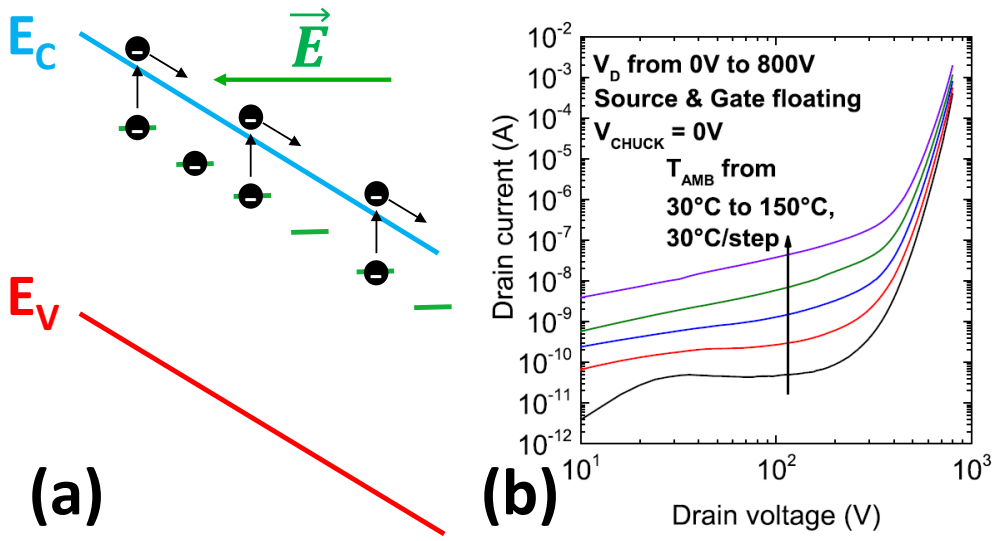

Figure 105: (a) Energy band diagram of ohmic conduction (b) Temperature-dependent experimental vertical leakage [257].

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III.3.a.iii Recombination Limited Transport

This mechanism has not been reported up to now in the GaN literature. To be more exact it comes from the organic device literature [325], [326]. The first condition for this mechanism to occur is a huge asymmetry between the carrier mean drift length having the following equation:

$$w_{n,p} = \mu_{n,p} \times \tau_{n,p} \times \left\|\vec{E}\right\|$$

Equation 13: Carrier mean drift length ($\mu_{n,p}$: carrier mobility; $\tau_{n,p}$: carrier recombination lifetime; $\vec{E}$: electric field).

This is precisely the case for the carriers in the GaN bulk. Indeed, the carrier mobility has two decades of difference. The low field electron mobility is around 1000 cm²/(V.s) [137] whereas the hole low field mobility is around 20 cm²/(V.s) [327]. The second condition is that the lowest mean carrier drift length (holes for GaN) must be smaller than the device size. This condition is not really straightforward to verify. Indeed, following the doping dependence of the Scharfetter relation reported in [328] (assuming that this relation is the same for traps), the carrier recombination lifetime $\tau_{n,p}$ can vary in the range of ns (without traps), 100 ps (with 1×10^{17} cm^{-3} of traps) and 10 ps (with 1×10^{18} cm^{-3} of traps). Assuming that the electric field is uniform in the GaN epitaxy at 50 V applied bias, the mean drift length varies in the range of 26 µm (without traps), 2.6 µm (1×10^{17} cm^{-3} of traps), 0.26 µm (1×10^{18} cm^{-3} of traps). This second condition is valid in the studied case because at least two impurity atoms have a concentration exceeding the concentration of 1×10^{17} cm^{-3} within the epitaxy (observed in SIMS not shown here for confidentiality reason).

In this transport, the amount of carriers (hole for GaN) collected at the electrode is reduced because they are trapped before. Therefore the current is less dependent on the applied voltage as the ohmic transport as exposed in the following expression:

$$J = e \times G \times \sqrt{\mu_n \times \tau_n} \times \sqrt{\boldsymbol{V}}$$

Equation 14: Current density expression of the recombination limited model in case for which the mobility of the electrons is way higher than the one of holes (e: elementary charge; G: generation rate; $\mu_{n,p}$: carrier mobility; $\tau_{n,p}$: carrier recombination lifetime; V: applied voltage).

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III.3.a.iv Space Charge Limited Current

This type of transport is present in the literature usually for insulators with trap levels [329]. An insulator embedded in between two electrodes in the dark with only one discrete energy level (as illustrated in **Figure 106(a)**) that is governed by the Space Charge Limited Current (SCLC) exhibits three different regions in its current versus voltage characteristic as shown in **Figure 106(b)**:

1. An ohmic regime (J α V) that is characterized by the fact that the emission rate from the traps is larger than the capture rate. Thus traps are partially filled (as illustrated in **Figure 105**).
2. A trap-filling limit: V_{TFL}. It is a voltage for which all the traps are filled meaning that the capture rate is larger than the emission.
3. A Child's law regime (J is proportional to V^2). At this point, the injected carrier is free to move in the conduction band and can travel to the next electrode without decaying in any trap because they are already filled.

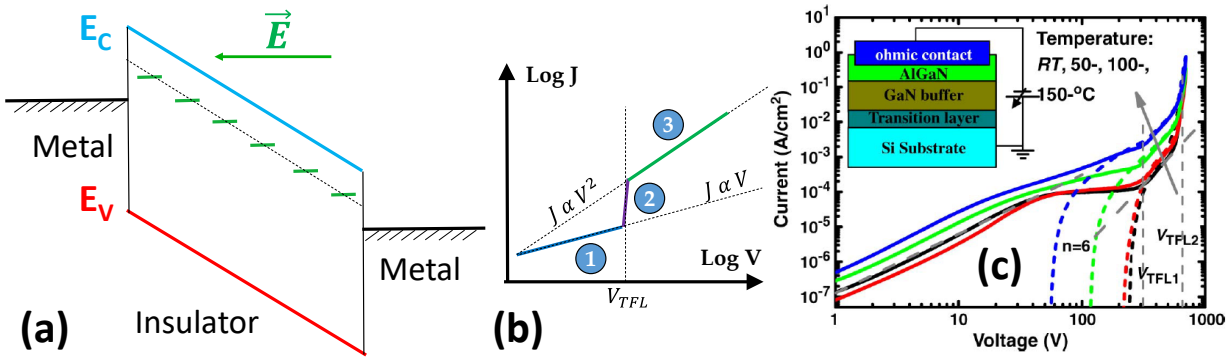

Figure 106: (a) Energy band diagram of a metal/insulator/metal structure with a discrete trap energy level (b) A typical current density versus voltage characteristic of Space Charge Limited model (V_{TFL}: Trap-filled limit voltage) (c) Vertical leakage current with a slope of 6 [276].

With more than one trap level, additional regimes are placed in between the ohmic and the child's law regime following a V^m trend with m>1 is present in the current characteristics as explained by Rizzo *et al.* [330]. This is why experimental studies try to identify V^m with a high m value and the V_{TFL} [276], [323]. However, none of these studies show neither a comparison with other possible mechanisms from the next section nor an SCLC analytical model fit for all the different measured temperatures with for instance the model reported in the study of Zubair *et al.* [331].

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III.3.a.v Hopping Versus Poole Frenkel Mechanisms

At relatively high voltage, hopping models: Variable Range Hopping (VRH), Nearest Neighbor Hopping (NNH) and Poole Frenkel (PF) were proposed in the GaN literature [332], [333]. They are described with the following equations:

$$J = C_1 \times \boldsymbol{E} \times e^{\frac{q\times\sqrt{\frac{q}{\pi\times\epsilon_0\times\epsilon_r}}\times\sqrt{\boldsymbol{E}}}{K_B\times T} - \frac{q\times\phi_t}{K_B\times T}}$$

Equation 15: Current density expression of the Poole Frenkel (PF) model (C_1: Arbitrary constant; E: electric field; q: elementary charge; ϵ_0: vacuum permittivity; ϵ_r: relative permittivity; K_B: Boltzmann constant; T: Temperature; ϕ_t: trap energy level) [334]–[336].

$$J = C_2 \times q \times \boldsymbol{E} \times \left(\frac{T_0}{T}\right)^{0.35} \times e^{-\left(\frac{T_0}{T}\right)^{1/n+1}}$$

Equation 16: Current density expression of the Variable Range Hopping (VRH) model (C_2: Arbitrary constant; q: elementary charge; E: electric field; T_0: Characteristic temperature; T: Temperature; n: number of spacial dimensions) [337].

$$J = C_3 \times K_B \times T \times q \times a \times e^{\frac{q\times a\times\boldsymbol{E}}{K_B\times T} - \frac{\boldsymbol{\phi_t}}{K_B\times T} - 2\times\frac{a}{\alpha}} \quad (hyp. \ : q \times a \times \boldsymbol{E} \approx 10 \times K_B \times T)$$

Equation 17: Current expression of the Nearest Neighbor Hopping (NNH) model (C_3: Arbitrary constant; K_B: Boltzmann constant; T: Temperature; q: elementary charge; a: mean hopping distance; E: electric field; ϕ_t: trap energy level; α: decay length) [337].

As illustrated in **Figure 107(a)**, the hopping mechanism corresponds to a tunneling process in which the carrier "hops" through a barrier (having a field-dependent barrier height) from one trap to another [338]. The traps can have different origins and therefore different properties such as energy levels [338]. The VRH occurs in an environment where the carrier concentration is rather low with respect to the NNH [339]. However, the main difference relies on their dependence: they both depend on the spatial distance between traps but the variable range hopping depends also on the trap energy level (this is why it is categorized as an activated process) [340]. As for the Poole Frenkel mechanism, it consists of the thermal excitation of trapped carriers over a barrier that depends on the electric field [338] as shown in **Figure 107(a)**. The VRH can be observed on a log-log plot as for the ohmic transport as it is proportional to the electric field. Whereas the NNH is identified in the ln(J) vs T or 1000/T plot as shown in **Figure 107(b)** and the PF in the

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ln(J/E) vs $E^{0.5}$ as shown in **Figure 107(c)**. It must be noticed that PF and the NNH have quasi the same exponential temperature dependence by comparing **Equation 15** and **Equation 17**. This means that the choice in between both mechanisms must be carefully justified. However, this is something missing in the studies of the vertical current temperature in the GaN-on-Si structures [257], [333], [336]. In fact, the mechanisms are identified dealing only with the parameter of interest: the trap energy level without looking at the consistency of all the extracted parameters: the extracted permittivity and the decay length are missing in [257], [336] and [333] respectively. By doing so, the right mechanism and therefore the right interpretation can be missed as it will be explained in the next subpart (III.3.b.ii.5th). Another approach (with respect to the one presented in **Figure 107(b)** and **(c)**) consists in identifying a PF regime by fitting the curve with TCAD simulations using a well-defined mobility [259]. However, the fit is valid at a unique temperature as it can be seen in **Figure 107(d)** weakening the proposed approach.

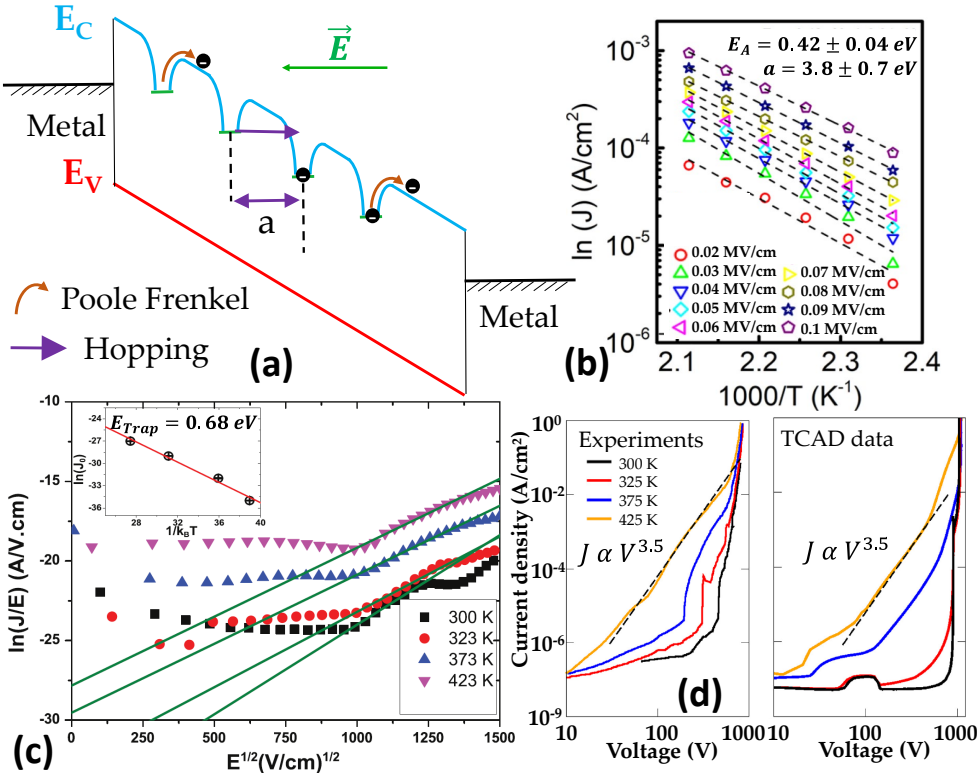

Figure 107: (a) Energy band diagram of a metal/insulator/metal structure with a discrete trap energy level submitted to Poole Frenkel (PF) and Hopping mechanisms (b) Parameters extraction from a NNH mechanism [333] (c) Parameter extraction from a PF mechanism [336] (d) Vertical current parallel in between experimental and simulation with a Poole Frenkel mobility model [259].

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III.3.a.vi Summary of the Bulk Transport Mechanisms

Different transport mechanisms were identified in the literature. There analytical models are summarized in **TABLE 9**. These analytical models will be useful to identify the transport mechanism in the studied GaN-on-Si epitaxy.

TABLE 9: Transport mechanism summary reported in GaN literature (C_i: constant; A_i: effective area; V: Voltage; E_A: Activation energy; K_B: Boltzmann constant; T: Temperature; q: elementary charge; G: generation rate; $\mu_{n,p}$: carrier mobility; $\tau_{n,p}$: carrier recombination lifetime; E: electric field; T_0: Characteristic temperature; n: number of spacial dimensions; ϕ_t: trap energy level; a: mean hopping distance; ϕ_t: trap energy level; α: decay length).

Transport model		Analytical model	Références
Ohmic conduction		$I = C_1 \times A_1 \times V \times e^{-\frac{E_A}{K_B \times T}}$ (Arrhenius temperature dependence [60], [324])	[257], [276], [323], [334]
Recombination limited model		$I = A_2 \times q \times G \times \sqrt{\mu_n \times \tau_n} \times \sqrt{V} \times e^{-\frac{E_A}{K_B \times T}}$ $(\mu_n \gg \mu_p)$	([325], [326]: not in GaN literature)
Space Charge Limited Current (SCLC)		$I \, \alpha \, V^m : m > 2$	[257], [259], [276], [323], [333]
Hopping	Variable Range Hopping (VRH)	$I = C_2 \times A_3 \times q \times E \times \left(\frac{T_0}{T}\right)^{0.35} \times e^{-\left(\frac{T_0}{T}\right)^{1/n+1}}$	[332], [335], [339]–[341]
	Nearest Neighbor Hopping (NNH)	$I = C_3 \times A_4 \times q \times K_B \times T \times a \times e^{\frac{q \times a \times E}{K_B \times T} - \frac{\phi_t}{K_B \times T} - 2 \times a/\alpha}$ $(q \times a \times E \approx 10 \times K_B \times T)$	
Poole Frenkel (PF)		$I = C_4 \times A_5 \times E \times e^{\frac{q \times \sqrt{\frac{q}{\pi \times \epsilon_0 \times \epsilon_r}} \times \sqrt{E}}{K_B \times T} - \frac{q \times \phi_t}{K_B \times T}}$	[257], [323], [333], [335], [336], [342]

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III.3.b Experimental Analysis and Interpretation of the Vertical Current Temperature Dependence

After having presented the previous studies on the vertical current analysis, let us move on to the analysis of the experimental vertical current through the epitaxy. This study was the topic of one of the author's publications [343]. The analysis is split into three sections. First, different preliminary experiments will be presented to justify the chosen experimental protocol and the fitting on a single die as well. After that, the fitting performed with analytical model will be detailed and the interesting extracted parameters will be enhanced. Finally, a discussion will be introduced on the extracted parameter to propose hypotheses on the vertical current origin.

III.3.b.i Preliminary Experimental Studies

III.3.b.i.1st Sample Presentation and Methodology

This study is performed on the same epitaxy used in the previous part for the diode capacitance study (III.2.a.i). This means that the 3.9 µm III-V epitaxy was grown on a p-doped (111)-oriented, 1 mm thick silicon substrate. It has a diameter of 200 mm and a resistivity between 3 and 20 Ω.cm. The Metal Organic Vapor Phase Epitaxy (MOVPE) was grown on an Aixtron® Crius® R200 tool. As illustrated in **Figure 108(a)**, it begins with a nucleation layer and the following transition layers or Strain Relief Layer (SRL). A carbon-doped GaN (GaN:C) is then formed. The last hundred nanometers are made with an Unintentionally doped GaN layer. The top contact is a Ti/Al bilayer circular ohmic contact with a variable diameter: D_{OHM}. The default diameter being 357 µm.

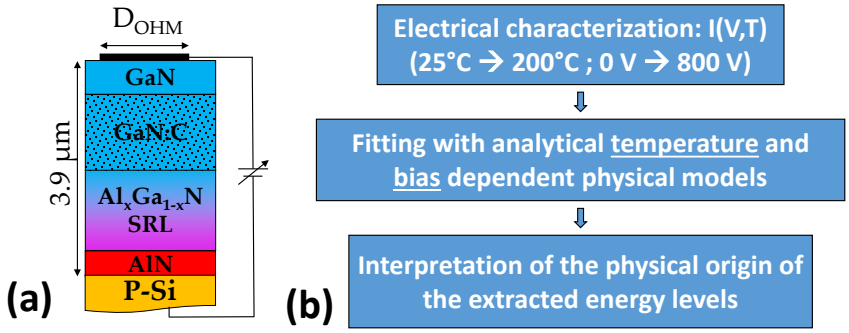

Figure 108: (a) Simplified schematic of the vertical epitaxy [343] (b) Diagram presenting the methodological steps [343].

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The methodology of this sub-part is rather simple as illustrated in **Figure 108(b)**. It consists in performing electric sweep from 0 V to 800 V with a 1 V step at a default ramp rate of 20 V/s. This ramp rate has been chosen to identify the trap responsible for the conduction only without being disturbed by trapping mechanisms. This is also done at several temperatures ranging from 25°C to 200°C with a 25°C increase between each temperature. The measurements are integrated on two Power Line Cycle (PLC) for their accuracy. Finally, they are performed under white light illumination to allow studying the last mechanism in a larger voltage range as explained in the next sub-section. These measurements will be fitted with analytical models as those presented in the previous section (III.3.a.vi). Thus, transport mechanisms responsible for the leakage will be identified and the relevant parameters will be extracted to interpret the current physical origin.

It must be noticed that, throughout the entire study, the leakage characteristics are always displayed in Ampere (A) and not normalized by the top electrode area (in A/cm²). This is because the perimeter contribution has a significant contribution below 500 V as exposed in Annexe C.1.

III.3.b.i.2nd Impact of the Microscope Light Illumination

As shown in **Figure 109(a)**, the illumination has strictly no impact on the vertical current levels at high temperature whatever the voltage. At lower temperature (75°C in **Figure 109(b)**), the plateau limited by the thermal generation of electron in the substrate starts at 600 V whereas it pushed further 800 V with light without changing current level of the exponential regime that starts near 400 V. Thus, using this white light illumination allows increasing the range in which the exponential regime occurs at low temperature, pushing further the apparition of the well-known current plateau. This will be useful to identify the right transport mechanism within this range.

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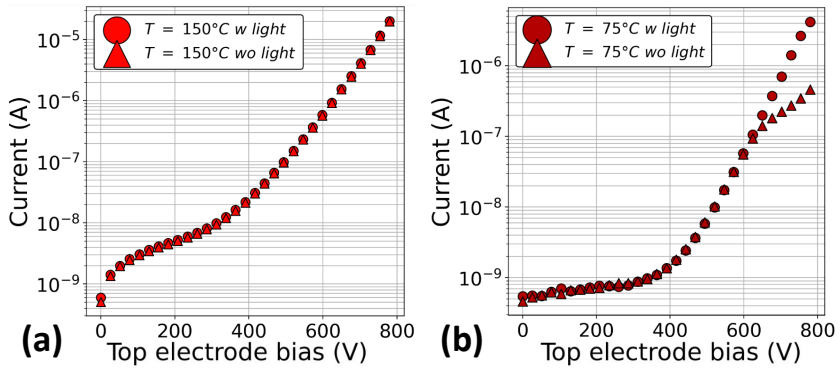

Figure 109: White light illumination impact on the vertical current measured at a ramp rate of 20 V/s (a) at 150°C (b) at 75°C (note that the leakage below 400 V was limited by the new high voltage measurement unit that has a higher low detection limit).

III.3.b.i.3rd Die to Die Variation

The traps distribution (even for those responsible for the conduction) may not have an uniform distribution on the entire wafer surface. The die-to-die variability has therefore to be at least checked. It is clear that in **Figure 110(a)** and **(b)**, curves are pretty well matched for the two different temperatures (75°C and 150°C respectively). The same matching is observed (not shown here) for all the temperatures used in this study. Thus, the analytical model fitting can be performed on a single die, which could represent the entire wafer.

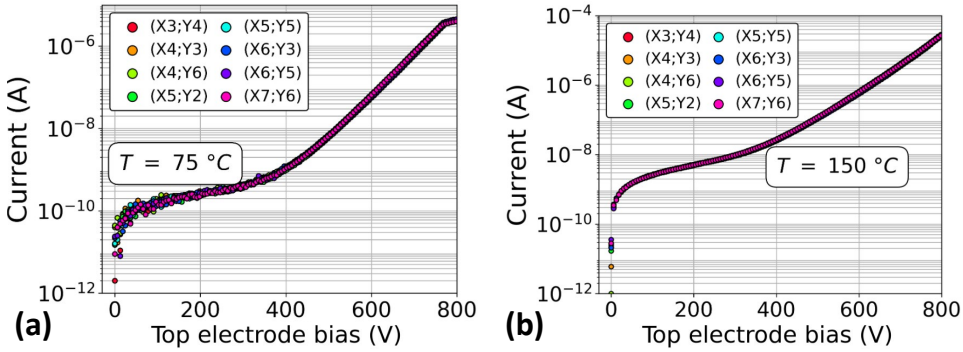

Figure 110: Die-to-die variations of the vertical leakage current at 20 V/s (a) at 75°C (b) at 150°C.

III.3.b.ii Model Fitting

In this section, the temperature leakage trends will be first presented before presenting the different analytical models that will be used to fit the experimental data. Then, the different fittings for each transport mechanism will be detailed.

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III.3.b.ii.1st Experimental Results

The obtained experimental curves are shown in **Figure 111**. It can be seen that the vertical current increases with the voltage and the temperature as well. At temperature ranging from 25°C to 75°C, the beginning of the plateau limited by the thermal generation of electron in the n-doped substrate can be identified. The curves can be split into different regions. The part below 200 V seems to have a smaller voltage dependency than an exponential one. This is why nearest neighbor hopping and Poole-Frenkel transport can be discarded from the possible transport mechanisms in this region. On the contrary, above 500 V, the voltage dependence clearly seems exponential potentially corresponding to the later mechanisms.

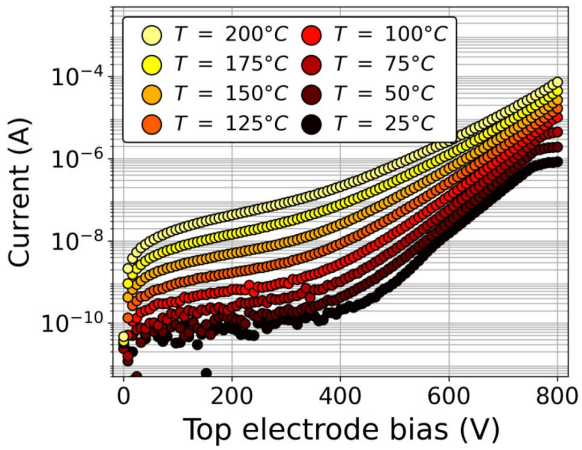

Figure 111: Experimental vertical current characteristics at temperatures ranging from 25°C to 200°C [343].

III.3.b.ii.2nd Transport Mechanism Analytical Models

Following the observations of the rough curves and by matching the last with analytical models, three different mechanisms were found relevant to fit the curves for the whole temperature and bias range. They are all reported in **TABLE 10**. As it will be presented in the next subsection the two first mechanisms: ohmic and recombination-limited model are sufficient to explain the experimental behavior from 0 V to 400 V in the whole temperature range due to their small voltage temperature (proportional to the voltage or the square root of the voltage respectively). They are both activated exponentially with the temperature (Arrhenius relation). The last mechanism: nearest neighbor hopping exponentially depends on the voltage and on the temperature which is coherent with what was observed at higher voltages.

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TABLE 10: Transport mechanism used to fit the vertical experimental curves [343] (C_i: constant; A_i: effective area; V: Voltage; E_A: Activation energy; K_B: Boltzmann constant; T: Temperature; q: elementary charge; G: generation rate; $\mu_{n,p}$: carrier mobility; $\tau_{n,p}$: carrier recombination lifetime; E: electric field; ϕ_t: trap energy level; a: mean hopping distance; ϕ_t: trap energy level; α: decay length).

Transport model	Analytical model
Ohmic conduction	$I = C_1 \times A_1 \times V \times e^{-\frac{E_A}{K_B \times T}}$
Recombination limited model	$I = A_2 \times q \times G \times \sqrt{\mu_n \times \tau_n} \times \sqrt{V} \times e^{-\frac{E_A}{K_B \times T}}$ $(\mu_n \gg \mu_p)$
Nearest Neighbor Hopping (NNH)	$I = C_3 \times A_4 \times q \times K_B \times T \times a \times e^{\frac{q \times a \times E}{K_B \times T} - \frac{\phi_t}{K_B \times T} - 2 \times a/\alpha}$ $(q \times a \times E \approx 10 \times K_B \times T)$

III.3.b.ii.3rd Ohmic Model Contribution

First, the ohmic model is used. As presented before, it has a slope of one in the log(I) versus log(V) plot. Nevertheless, as it can be seen in **Figure 112** by comparing the experimental curves to the analytical model with the final parameters, the experimental curves do not completely matched a slope of one. However, they are closer to this behavior at high temperature and within the 100 V surroundings and the slope is decreasing at low temperature. This is why the fit was made by focusing the matching within this region. The choice of the best fitting parameters was made by means of graphical observation as well as the margin of error values. This method is by far better than using a least squares method. Indeed, this algorithm does not take into account the observation on the experimental slope (closer to one at high temperature). The extracted activation energy is equal to 0.76 eV with a margin of error of 30 meV. Note: the author verified that the perimeter contribution follows the same activation in energy as explained in Annexe C.2.

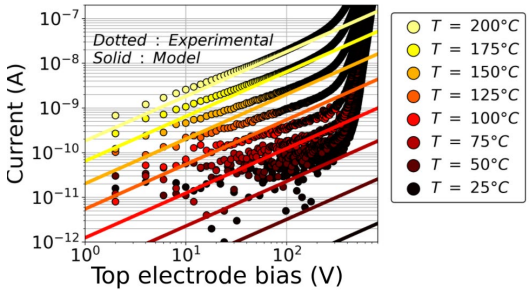

Figure 112: Ohmic model contribution superimposed to the experimental values (fitting parameter: E_A = 0.76 eV).

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III.3.b.ii.4th Recombination-Limited Model Contribution

To complete the fitting at small voltages and low temperatures, recombination-limited was used. Its contribution is shown in **Figure 113(a)**. Its contribution begins to be significant for the 150°C curve (light orange in **Figure 113(a)**) for voltage below 100 V until the 25°C curve (black in **Figure 113(a)**) for voltage below 400 V.

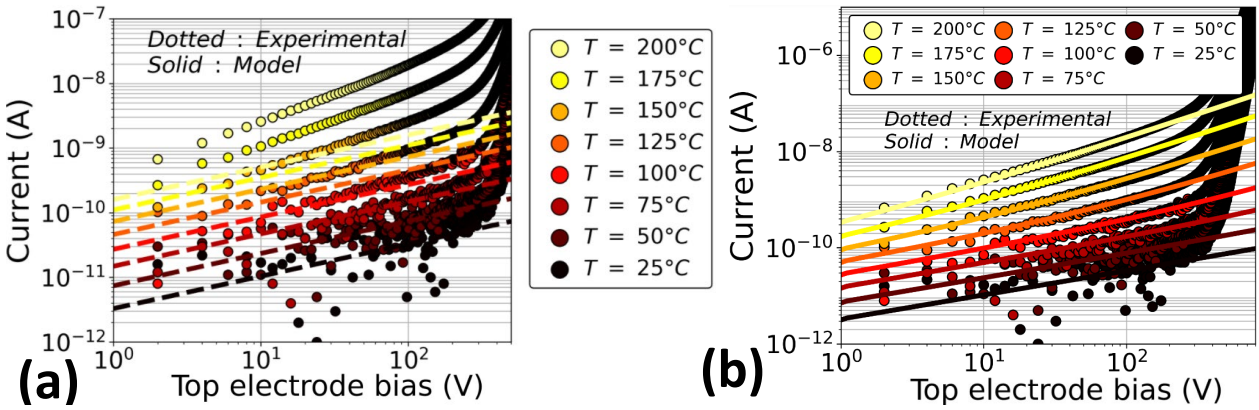

Figure 113: (a) Recombination-limited model contribution superimposed to the experimental values (fitting parameter: E_A = 0.27 eV) (b) Ohmic and recombination-limited model contributions (models in parallel) superimposed to the experimental values.

The model parameters as well as the margin of error were chosen again by graphical method to get the best matching between experimental curves and the ohmic and recombination models taken in parallel (the resulting current is the sum of both contribution) as shown in **Figure 113(b)**. The extracted activation energy is equal to 0.27 eV with a margin of error of 20 meV.

III.3.b.ii.5th Nearest Neighbor Hopping Model Contribution

To understand the last part of the graph (region above 400 V), models having an exponential dependence on the electric field: Poole Frenkel and Nearest Neighbor Hopping were compared. A linear fit was performed by means of the least squares method for each temperature.

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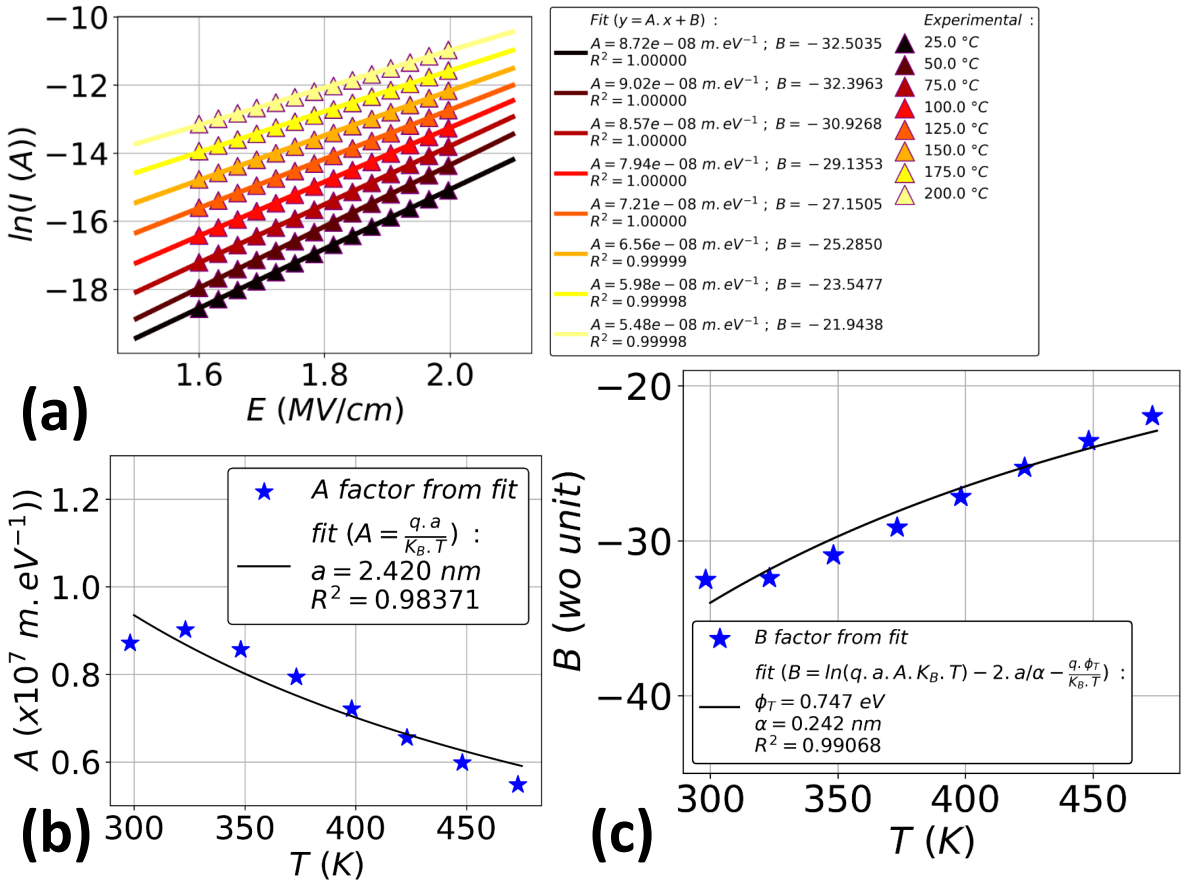

Figure 114: (a) Linear fit of the ln(I) versus E of the experimental vertical current at temperatures ranging from 25°C to 200°C (adapted from [343]). (b) Extraction of the mean hopping distance of the nearest neighbor hopping mechanism from the slope of the previous graph (c) Extraction of the trap energy level and the decay length of the nearest neighbor hopping mechanism from the y-axis intercept of the previous graph.

This was performed on the ln(I) versus E as exposed in **Figure 114(a)** for the nearest neighbor hopping and in the ln(I/E) versus the square root of E for the Poole Frenkel case (not shown here). It must be mentioned that the electric field uniform distribution was assumed.

As for the nearest neighbor hopping model, thanks to the slope and the y-axis intercept of the linear fit at each temperature, the trap energy level, the mean hopping distance and the decay length can then be extracting. This was performed by fitting their temperature dependence as shown in **Figure 114(b)** and **Figure 114(c)**. It gives a mean hopping distance of 2.42 nm and a decay length of 2.4 Å and an extracted energy level of 0.75 eV. By means of graphical methods when the

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model curves were superimposed with the experimental curves as it can be seen in **Figure 115**, the margin of error of 10 meV was determined.

As for the Poole Frenkel mechanism, a similar approach has been performed. However the fits gave a trap energy level of 1.88 eV and a relative permittivity of 1.59 which is inconsistent with the expected value for GaN: 8.9 [10].

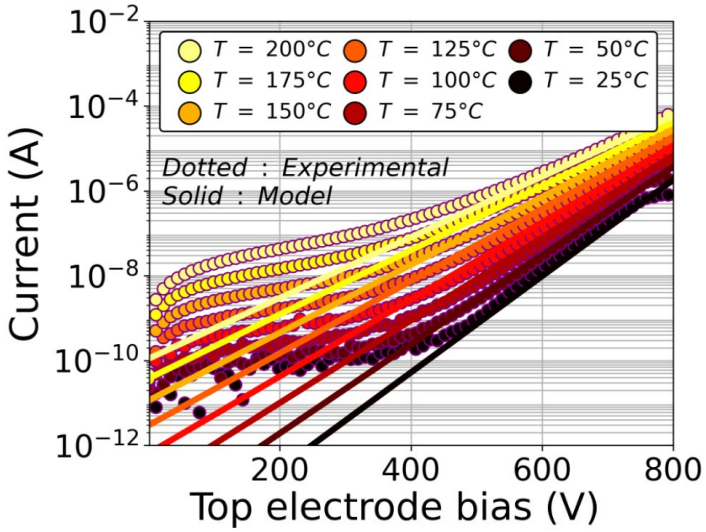

Figure 115: Nearest neighbor hopping model contribution superimposed to the experimental values (fitting parameter: E_A = 0.75 eV).

III.3.b.iii Fitting Parameter Interpretation

In this section, the energy values corresponding to trap energy levels identified in the previous section (III.3.b.ii) will be compared to the study of the literature to be able to propose hypotheses on the origin of the vertical current. They are summarized in **TABLE 11**. Two traps origin will be then discussed. A trap having an energy of 0.27 eV responsible for the recombination-limited model and another with an energy near 0.75-0.76 eV responsible for the ohmic and hopping model.

TABLE 11: Extracted energy from the fit on the vertical experimental curves.

Transport model	Analytical model
Recombination limited model	0.27 ± 0.02 eV
Ohmic conduction	0.76 ± 0.03 eV
Nearest Neighbor Hopping (NNH)	0.75 ± 0.01 eV

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† **Hypothesis on the 0.27 ± 0.02 eV energy level**

Energy levels embedded in this range were reported in the bulk GaN or AlGaN literature [313], [344]–[349]. They were extracted thanks to Deep Level Transient Spectroscopy (DLTS). Nevertheless, there is currently no consensus on the exact origin of the defect.

Several studies from the Soh *et al.* [346], Park *et al.* [347] and Cho *et al.* [348] showed that the capture kinetics follows a logarithm trend which corresponds to an extended defect such as dislocations. Moreover, as the trap concentration gradually decreases with the Rapid Thermal Annealing (RTA) temperature, Soh *et al.* [346] proposes that clusters are formed all around them. However, the latter were not able to found out if it was around screw, edge or mixed dislocations.

Three point defects were proposed to form the clusters. First, nitrogen vacancy: V_N has been proposed by Cho *et al.* [348]. Indeed, in the case of ohmic contact formation, the DLTS amplitude of the peak related to this defect increases with the etching bias as well as the concentration of nitrogen vacancy concentration as shown by Choi *et al.* [350]. Gallium vacancy: V_{Ga} or gallium and nitrogen vacancy pair V_N-V_{Ga} were proposed by Fang *et al.* [351] because it was shown in the *ab initio* simulation study of Wright *et al.* that these defects have lower formation energy in N-rich environment (such environment in which the device were grown for this study) with respect to nitrogen vacancy [352].

† **Hypothesis on the 0.76 ± 0.03 eV energy level**

This energy level has not been observed in many articles in the literature. Indeed, the study of Asghar *et al.* performed on vertical p-n diode grown on a MOCVD reactor [353] reports a similar energy level (E2: 0.76 ± 0.02 eV). The proposed hypothesis is nitrogen atom in interstitial site: N_i. It must be mentioned that this hypothesis is consistent with the growth of the studied sample in this manuscript because it is performed in an N-rich environment.

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III.3.b.iv Summary

By adding the contribution of all the identified mechanisms (transport mechanisms in parallel) as shown in **Figure 116(a)**, the curves are pretty well matched with the experimental one as it can be seen in **Figure 116(b)**. The region in which each transport is dominant are enhanced in the same figure with the green lines. At high voltage (above 400 V), the nearest neighbor hopping transport through nitrogen in interstitial sites prevails whereas at low voltage (below 400 V), the ohmic transport through nitrogen in interstitial sites prevails at high temperature (> 150°C) and the recombination-limited model prevails at low temperature (< 75°C).

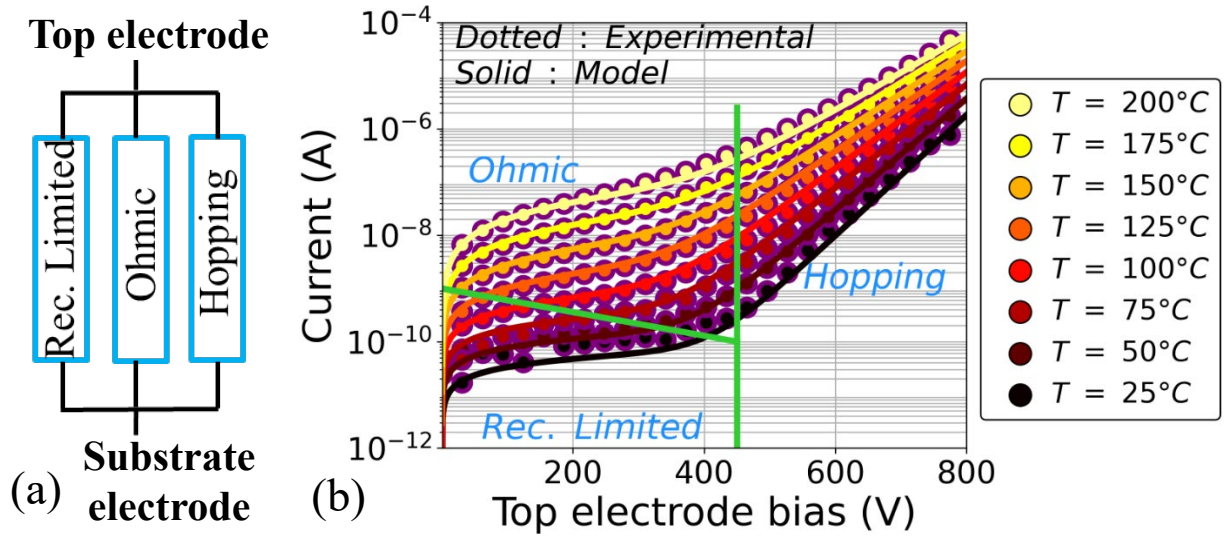

Figure 116: (a) Vertical current transport mechanism contributions (in parallel) [343] (b) Fitting with the experimental data [343].

Nevertheless, this approach identifies only traps related to the limiting conduction mechanism. It is perhaps not sufficient to be able to reproduce the right band bending in TCAD to be able to reproduce the experimental leakage of the entire vertical structure. Indeed, elements that are not participating in the conduction such as fixed charges (not known yet) may change the band diagram as it will be discussed in the next part.

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III.3.c TCAD Simulation and Modeling Study to Reproduce the Experimental Trend

This part presents the limitation of one of the state-of-the-art approaches [258] (which consists in studying the vertical current by placing fixed charges at the AlN/Si interface and adjusting the barrier height seen by the electron to let current flow in the GaN layers) and the possible future studies for the vertical current modeling of the GaN-on-Si epitaxy. Indeed, it will be shown that, without traps consideration, temperature-dependent current can be formed but additional considerations (discussed at the end) must be taken to fit the order of magnitude of the experimental current. This study is limited to 100 V corresponding to the detected ohmic and recombination-limited transport region.

III.3.c.i Simulated Structure Presentation

One-dimensional simulations were performed in this study. Indeed, running two-dimensional simulations in which the top electrode shorter than the substrate electrode was tested but it led to convergence issues in the transition layers. Thus, it was decided to neglect charge lateral movement [354] in a first place.

The simulated structure (**Figure 117(b)**) is very similar to the experimental one (**Figure 117(a)**). The silicon substrate has a 1 mm thickness and has a residual p-doping[6] of 0.7×10^{15} cm^{-3} (equivalent to 20 Ω.cm, the maximum expected resistivity because it leads to a wider current plateau [260] and therefore has a higher probability to be detected on the curve). The diffusion of aluminum in the silicon substrate (due to the high growth temperature of the AlN nucleation layer [355]) as shown in **Figure 117(c)** was not taken into account at first for simplicity purposes. The GaN:C is replaced by a GaN layer to prevent the traps calculation complexity. The epitaxy thickness is the same as for the experiment. Finally, the metal work function in contact with GaN has been set to 3.9 eV to have an ohmic contact (for electrons) and the contact with silicon has been defined as equivalent to an ohmic contact.

[6] The substrate conductivity has been also studied (not shown here). It revealed that it modulates the conductivity through the entire stack by changing the electric field distribution in between the silicon and the epitaxy.

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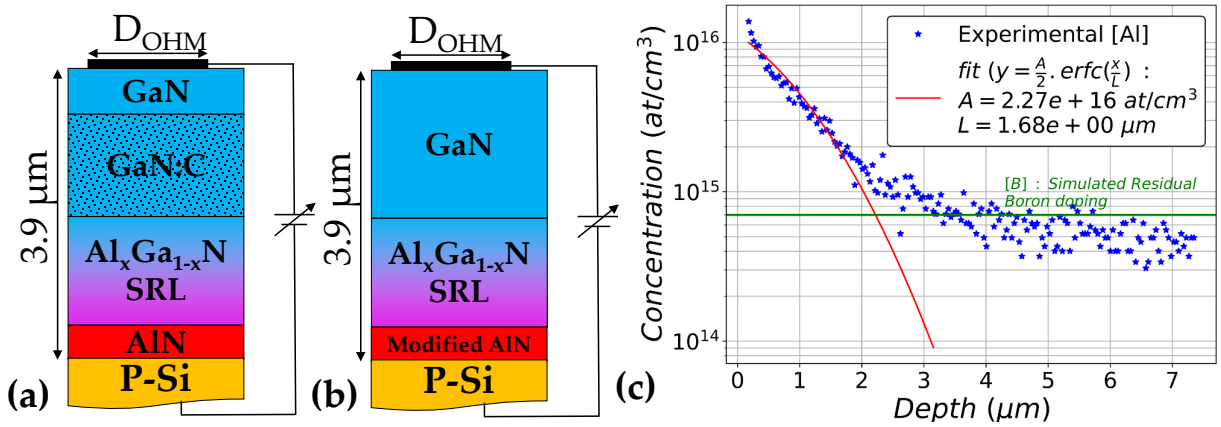

Figure 117: Simplified schematic of the (a) experimental vertical epitaxy (b) simulated structure (c) aluminum diffusion in the silicon substrate fitting with a corrected error function profile.

The AlN nucleation layer has been replaced by the "modified AlN" which consists of an $Al_xGa_{1-x}N$ layer in which the aluminum mole fraction is varied to tune the band discontinuity ΔE_C at the interface with the silicon substrate. The latter is reported to be between 1 to 1.3 eV in the study of Sayadi *et al.* [297] and equal to 1.08 eV in the study of Borga *et al.* [258].

Here is the list of models used for this simulation:

- Thermionic model,
- Positive fixed charges at the "Modified AlN"/Si interface: Q_{fix},
- Tunneling model with a non-local mesh (tunneling mass by default: $0.4 \times m_0$ [258]),
- Shockley-Read-Hall (SRH) with default GaN parameter [356],
- Avalanche with default GaN and Si parameter [356],
- The electron/hole mobility in the nitride layers has been modified following the experimental measurement as exposed in Annexe D. It must be mentioned that the high field model has not been used in the presented simulation because it leads to convergence issues.

Transient measurements from 0 to 100 V are presented in this section. Three different parameters were varied as detailed in **TABLE 12**:

- The aluminum molar fraction of the "Modified AlN" to tailor the band discontinuity ΔE_C with the silicon,
- The tunneling mass at the "Modified AlN"/Si interface,
- Positive interface charge concentration at the "Modified AlN"/Si interface.

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TABLE 12: Simulation split table (changed parameter in red).

Simulation split	Aluminum molar fraction x of the "Modified AlN" (wo unit)	Tunneling mass (×m_0)	Positive fixed charge at the "Modified AlN"/Si interface (cm^{-2})
1	0.35	0.4	1×10^{13}
2	0.4	0.4	1×10^{13}
3	0.45	0.4	1×10^{13}
4	0.47	0.4	1×10^{13}
5	0.48	0.4	1×10^{13}
6	0.49	0.4	1×10^{13}
7	0.5	0.4	1×10^{13}
8	0.48	0.2	1×10^{13}
9	0.48	0.4	0.7×10^{13}
10	0.48	0.4	2×10^{13}

III.3.c.ii Simulation Results

The vertical current of the structure presented in **Figure 117(b)** has a specific temperature dependence as shown in **Figure 118(a)**. Indeed, as it can be seen in the logarithm-logarithm (log-log) of the 5th split, the current exhibits a linear shape with a slope of approximately one. Thus, the transport is ohmic (may be recombination limited at high temperature for voltage higher than 100 V). This current has temperature dependence. Its related activation energy (Arrhenius dependence) extraction is performed at a given voltage: 30 V as illustrated in **Figure 118(b)**. The impact of the different parameters on this activation energy will be presented in the next subsection.

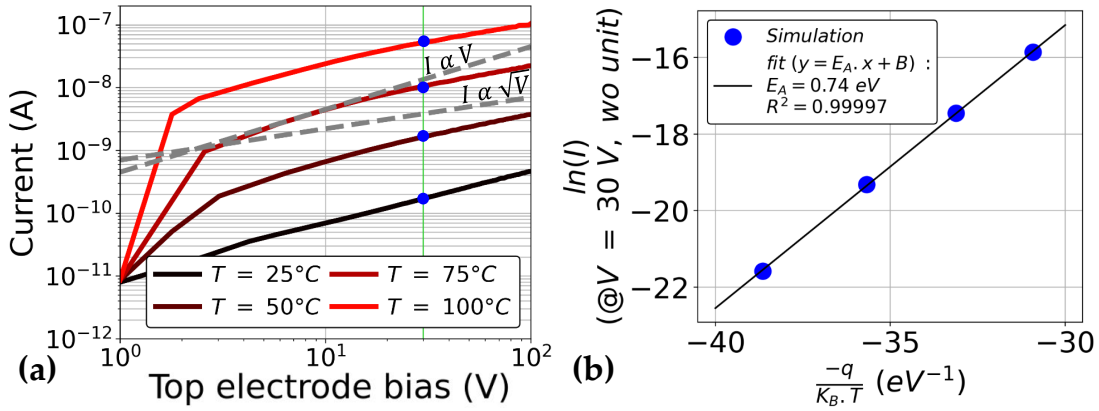

Figure 118: (a) Vertical current (log-log) characteristic of the simulated structure at four different temperatures (b) Activation energy of the simulated current extracted at 30 V.

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III.3.c.ii.1st Impact of the Barrier Height at the Modified AlN/Si interface

Varying the aluminum content in the modified AlN (from 0.35 to 0.5 corresponding to split 1 to 7) significantly changes the activation energy of the current in between 0 to 100 V as demonstrated with the two different regimes in **Figure 119(a)**. Indeed, below 0.45, the activation energy reaches a bottom limit of 0.66 eV. And in between 0.45 to 0.5, it increases linearly passing by the 0.76 eV found experimentally (III.3.b). In **Figure 119(b)**, it can be seen that for x = 0.45 eV, the conduction band drop at 100 V occurs only in the silicon substrate. This means that the 0.66 eV is related to this region. Moreover, increasing the molar fraction makes the GaN buffer more resistive with respect to the silicon because the higher the mole fraction, the higher the proportion of the conduction band drop in the GaN epitaxy as illustrated in **Figure 119(b)**. Thus, activation energy higher than 0.66 eV can be explained either by the electron injection through the GaN epitaxy or by the GaN resistivity increase.

Diminishing the electron effective mass (from $0.4\times m_0$ to $0.2\times m_0$ in splits 5 and 8 respectively) for a 0.48 mole fraction, does not change the current value and therefore the activation energy (not shown here since no change is observed). Hence, tunneling does not contribute to electron injection, which is thus due to thermionic emission.

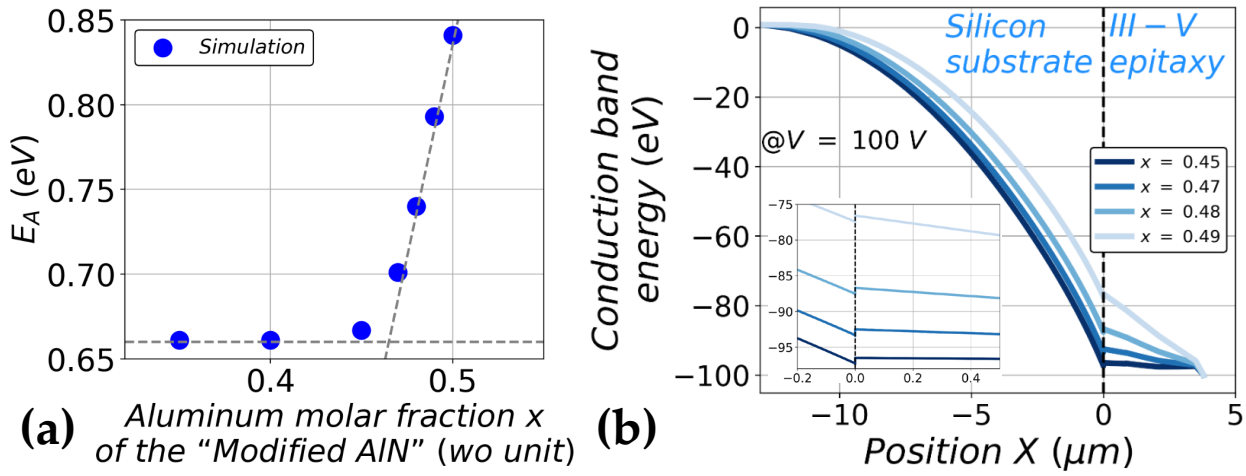

Figure 119: (a) Activation energy as a function of the aluminum molar fractions of the "Modified AlN" (b) Conduction band energy along a vertical cutline of the vertical simulated structure at 100 V and 25°C for different aluminum molar fractions of the "Modified AlN" corresponding to split 3 to 6.

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III.3.c.ii.2nd Impact of the Fixed Charges at the Modified AlN/Si interface

The choice of the fixed charge concentration has a significant impact on the current thermal activation as demonstrated in **Figure 120(a)**. The larger the fixed charge concentration, the lower the activation energy. Indeed, it influences the band bending in the GaN as well as in the Si as shown in **Figure 120(b)**. Thus, it seems that this parameter has the same impact as the previously seen aluminum molar fraction. This means that different couples (x; Q_{fix}) can lead to the same activation energy. This might not be a problem since this is valid for a limited barrier height. Above a certain ΔE_C, thermionic will disappear and the current will be null. Thus a comparison with the experimental current at this stage can be done.

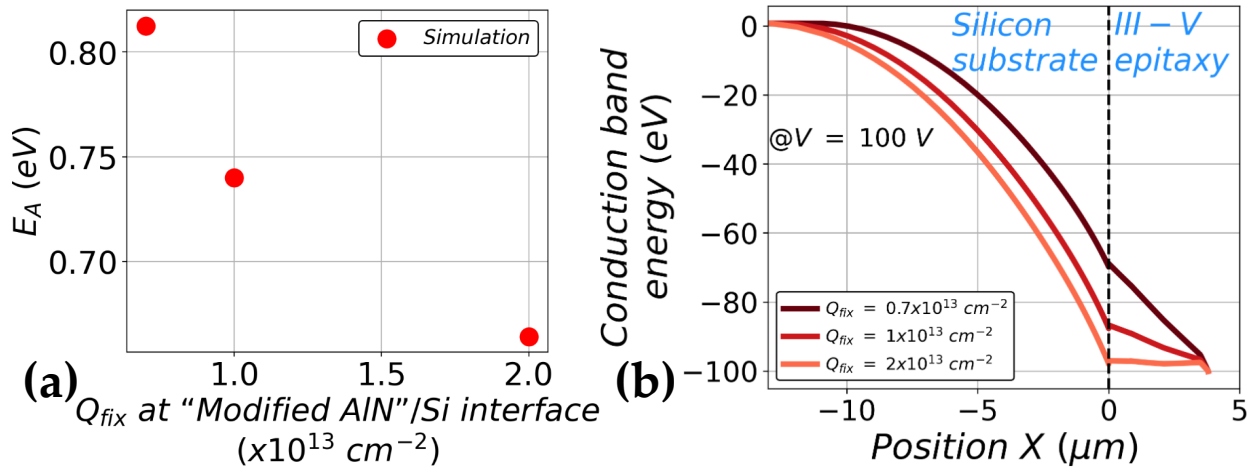

Figure 120: (a) Activation energy as a function of the positive fixed charge concentration at the "Modified AlN"/Si interface (b) Conduction band energy along a vertical cutline of the vertical simulated structure at 100 V and 25°C for different positive fixed charge concentrations at the "Modified AlN"/Si interface corresponding to split 9, 5 and 10.

III.3.c.ii.3rd Comparison with the Experiments

The simulations obtained with a positive fixed charge equal to 1×10^{13} cm^{-2} and a molar fraction of 0.485 (giving a 0.755 eV) are compared with the experiment in **Figure 121(a)**. It can be observed that the simulation current has several orders of magnitude difference with respect to the experiments (comparison is limited to voltages below 100 V, corresponding to ohmic and recombination limited transport in the experiment). The different proposed ways to reach the experimental current fit will be discussed in the next section.

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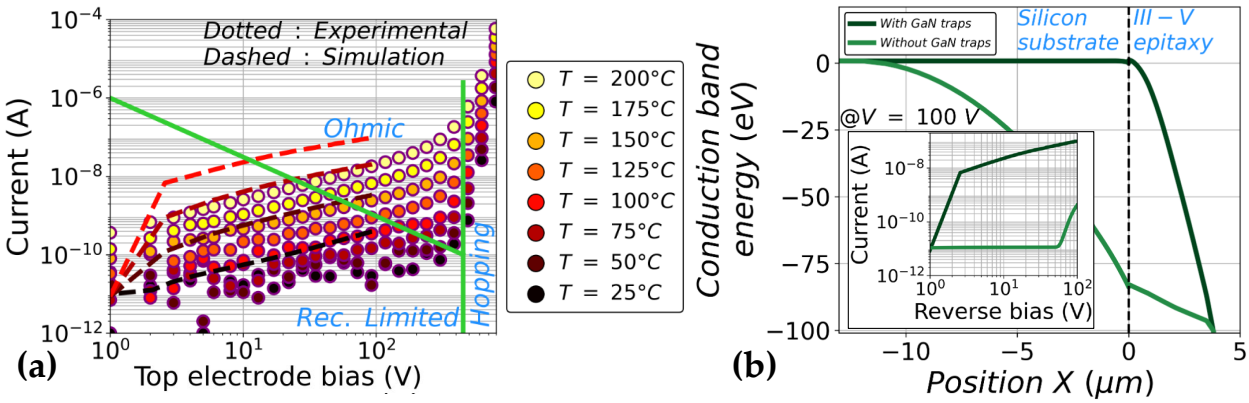

Figure 121: (a) Vertical current of the experimental (dots) superimposed with the simulated structure (x = 0.485; Q_{fix} = 1×10^{13} cm^{-2}) (b) Conduction band energy along a vertical cutline of the vertical simulated structure at 100 V and 25°C and vertical current of the simulated structure with and without traps in the GaN epitaxy except in the last 500 nm (deep acceptor traps at E_V+1.1 eV; σ_{A,h^+} = 1×10^{-13} cm²; [A] = 1 u.a.).

III.3.c.iii Discussion

To be able to reach the experimental current order of magnitude in TCAD simulation, the electron flow needs to be decreased while keeping the same activation energy. Here are two different approaches in simulation to reach this objective:

- Make the GaN buffer more resistive introducing the deep acceptor traps found in the C(V,T) measurement performed on transistors (III.2.b). This approach was initiated during this PhD. As illustrated in **Figure 121(b)**, acceptor introduction allows to make the GaN epitaxy withstand the whole voltage but the current even at high temperature (not shown here) is null below a tens of volts. Localized dislocation with a screening approach (proposed by Qwah *et al.* [357]) allows overcoming this limit. This was tested in this PhD. It was performed without specific dislocation transport because the dislocation-related mechanism identified in the experimental part (recombination-limited) is already available in the TCAD tool. However, the temperature dependence is hard to grasp which is why it is not presented here.
- Make the "Modified AlN"/Si interface more complex (solution discussed during an exchange with Synopsys™). Nevertheless, the parameters used for this will not be justified with experimental measurements.

These approaches are quite time consuming and based on experimental data. It is preferable to start from experimental data (solution discussed during an exchange with Synopsys™). For instance, identifying the region in which the current (ohmic or NNH associated to nitrogen on

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interstitial site N_i) is limited. This can be done by modifying the N_i concentration indirectly by varying the ammonia partial pressure in each layer individually during epitaxial growth. Doing so in the AlN would potentially improve our understanding on the AlN/Si interface (for a future TCAD modeling). Indeed the trap related to the recombination-limited transport are dislocations with a cluster of punctual defects for which their concentrations depend on the growing conditions. These dislocations are potentially threading dislocations beginning at the AlN/Si interface.

Once this is done and the TCAD modeling reproduces the experimental recombination-limited and ohmic transport, Nearest Neighbor Hopping model can be implemented in TCAD simulations using Physical Model Interface (PMI) proposed by Synopsys to finalize fitting.

III.3.d Summary

In this part, it was presented that the vertical leakage current is subdivided into three different regions. On the one hand, the current in the two last regions is limited either by the thermal generation of electrons in the silicon substrate or by the transport through the AlN/Si barrier that is potentially assisted by the huge density of traps due to the lattice mismatch. On the other hand, it was found that in the main voltage range, the vertical current is limited by bulk traps within the GaN epitaxy: through dislocations with a cluster of punctual defects such as gallium vacancies V_{Ga} alone or paired with nitrogen vacancies V_N (E_T = 0.27 eV) for low voltage and temperature and nitrogen on interstitial sites N_I (E_T = 0.75-0.76 eV) for high voltage and temperature (boundaries can be found in **Figure 116**).

A TCAD simulation study was initiated enhancing the limitation of the state-of-the-art approach (fixed charge at the AlN/Si interface and barrier lowering while no traps are inserted in the GaN epitaxy). The GaN epitaxy is not resistive enough, leading the potential drop to occur in the substrate and the current temperature dependence to be ruled by the latter. The discussion on the possible future studies, proposes to start from an experimental study with varying epitaxial growth conditions (especially ammonia partial pressure) in the different layers. This would give more insight into the leakage origin: the layers limiting the current and perhaps give a hint of how to deal with the AlN/Si TCAD interface modeling by varying the nucleation layer growth parameters.

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III.4 Capacitance Deep Level Transient Fourier Spectroscopy (C-DLTFS) of Schottky AlGaN/GaN-on-Si Schottky Diode

As mentioned in the first part (III.1), the third step of the methodology consists in identifying traps that impact the electric field near the anode contact. To do so, a Deep Level Transient Fourier Spectroscopy is proposed and was one of the author's publications topic [358]. To differentiate etching-related traps identification from other traps, this study will be performed on samples with different etching recipes.

III.4.a Samples and Characterization Setup Presentation

In this part, the test vehicle is again the 650 V/6 A Schottky diode fabricated at CEA LETI with the FPG0-1 layout (60 mm width). Its cross-section is illustrated in **Figure 122(a)**, with an anode-to-cathode distance (L_{AC}) equals to 16 µm. The anode field plate lengths: (FPG0 to FPG3) are equal to 1 µm and the cathode field plate length (FPD) is equal to 0.5 µm. However, the epitaxy was grown in another epitaxial tool: AIXTRON® G5+® and the total thickness is reduced from 3.9 µm to 3.5 µm. Nevertheless, the different top layer compositions and thicknesses are similar to the one presented in II.2.a.i. Furthermore, the growth technique (MOVPE) is also the same which allows us to identify similar defects.

In this study, two samples of Schottky diodes will be studied. They differ by the ICP-RIE recipe used for the etching as detailed in **TABLE 13**. After the etching step, photoresist was removed with an O_2/N_2 plasma (dry stripping). The surface was cleaned using EKC265 (a wet clean of DuPont® EKC Technology) followed by rinsing and the deposition of Titanium Nitride (TiN) and Tungsten (W) to form the Schottky electrode.

TABLE 13: Experimental ICP-RIE split table.

Experimental split	ICP source (W)	RF bias (V)	BCl_3/Cl_2 ratio
LV 90 V	500	90	1
LV 237 V	300	237	4

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Scanning Transmission Electron Microscopy (STEM) in High-Angle Annular Dark Field (HAADF) can be observed in **Figure 122(a)** and **(b)**. It can be seen that there is no etching morphology difference between the two devices. The experimental splits were tested in the dark on a High Energy Resolution Analysis Deep Level Transient Spectroscopy (HERA DLTS) system (PhysTech® GmbH): FT-1030 HERA DLTS® [359], [360]. Measurements were performed from 50 K to 425 K. Only Capacitance DLTFS (C-DLTFS) results (using Boonton 7200 capacitance meter) are presented through the first order Fourier sine (resp. cos) coefficient b1 (resp. a1) to represent the DLTFS signal [359], [361]. More details on the DLTS technique are summarized in Annexe E.

The results exposed in the following part were recorded for both samples using DLTFS at different reverse biases: -10 V; -20 V; -50 V; -70 V and -90 V keeping the positive voltage bias equal to 0 V (or -0.1 V) to probe different regions of the heterojunction device. By default, the filling pulse time was 100 µs and the time window τ_W was 2.048 ms.

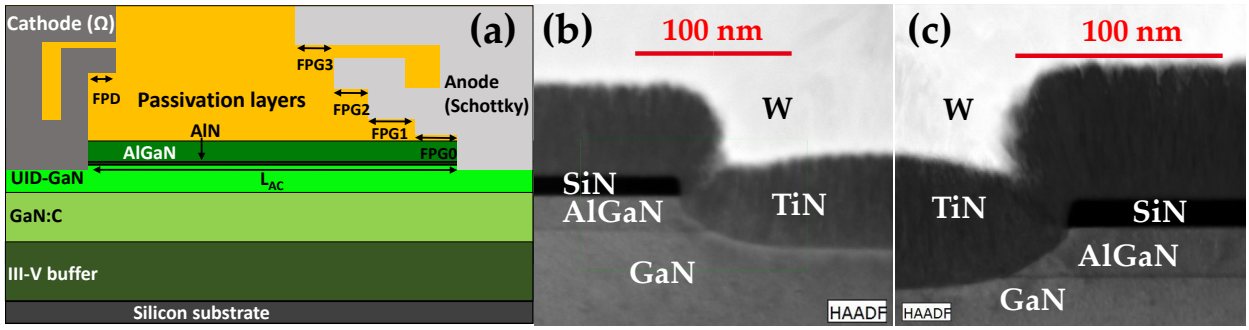

Figure 122: (a) Schottky diode cross-section (adapted from [358]) (b) LV 90 V Schottky interface (adapted from [358]) (c) LV 237 V STEM observation of the Schottky interface (adapted from [358]).

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III.4.b Experimental Results

Several traps were identified during the different tests. Arrhenius plots were fitted with the trap capture kinetic formula described in Annexe E using the electron effective mass $m^*_{e^-} = 0.2 \times m_0$ [362]. This allows the energy level as well as the electron capture cross-section extraction to classify them as described in the first section. Their filling pulse width dependence will be then evaluated in order to determine if they are punctual or extended defects.

III.4.b.i Arrhenius Plot

For all the identified traps, Arrhenius plots were calculated thanks to the extracted characteristic time τ using DLTFS as shown for instance in **Figure 123**. It allows extracting two energy levels E_1 (0.48 eV below the conduction band) and E_2 (0.51 eV below the conduction band) with their corresponding capture cross-sections $\sigma_{e^-,1} = 5.9 \times 10^{-16}\ cm^2$ and $\sigma_{e^-,2} = 1.56 \times 10^{-13}\ cm^2$. This was performed for all the biasing conditions except for the LV 237 V sample at -90 V for which two trap peaks were de-convoluted using HERA-DLTS and Provencher's CONTIN algorithm [363], [364].

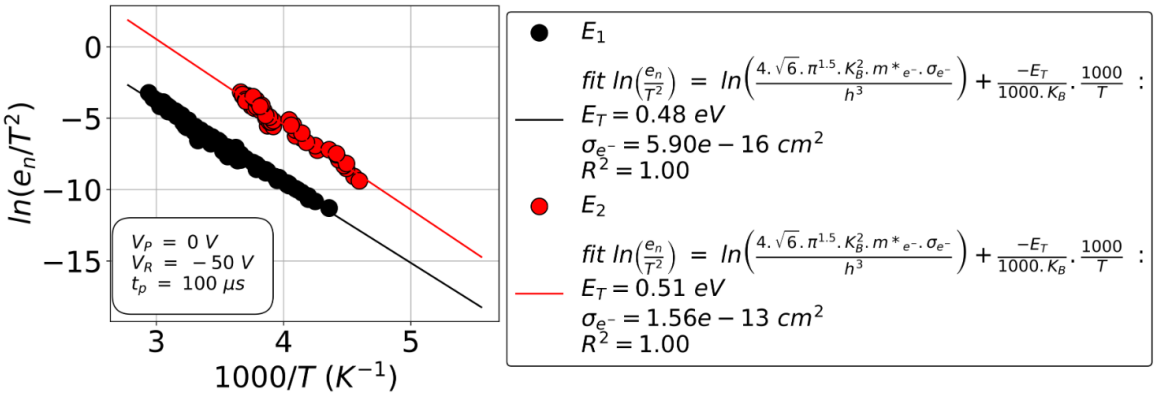

Figure 123: Recorded DLTFS Arrhenius plot of the LV 237 V sample at V_R = -50 V; V_P = 0 V and t_P = 100 µs (adapted from [358]).

The different identified traps were grouped according to their properties: energy level difference within a range of 20 meV and cross-sections within one and a half-decade range. They are called D_i with $i \in [|1, 7|]$ as reported in **TABLE 14**. Range values are empirical but the different groups were confirmed especially with their qualitative common Fourier coefficient dependency as a function of the filling pulse time (t_P).

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TABLE 14: Categories of donor traps D_i ($i \in [|1,7|]$) based on the energies and cross-sections extracted from Arrhenius plots for the different samples (LV 90 V and LV 237 V) and at different bias conditions (V_P, V_R) (adapted from [358]). The author's proposed hypothesis for each category (at the bottom) resulting from the discussion in III.4.c.

		D1		D2		D3		D4		D5		D6		D7	
		E_T (eV)	σ (cm²)	E_T (eV)	σ (cm²)	E_T (eV)	σ (cm²)	E_T (eV)	σ (cm²)	E_T (eV)	σ (cm²)	E_T (eV)	σ (cm²)	E_T (eV)	σ (cm²)
V_P = -0.1 V	LV 237 V									0.53	1.55×10^{-13}				
V_R = -10 V	LV 90 V													0.57	4.45×10^{-12}
V_P = -0.1 V	LV 237 V							0.50	1.73×10^{-13}						
V_R = -20 V	LV 90 V							0.49	7.58×10^{-15}	0.54	2.85×10^{-13}				
V_P = 0 V	LV 237 V					0.48	5.90×10^{-16}	0.51	1.56×10^{-13}						
V_R = -50 V	LV 90 V			0.46	2.56×10^{-13}					0.52	1.49×10^{-14}				
V_P = 0 V	LV 237 V					0.47	7.14×10^{-16}					0.55	4.33×10^{-15}		
V_R = -70 V	LV 90 V											0.55	1.39×10^{-14}		
V_P = 0 V	LV 237 V	0.40	7.98×10^{-18}			0.47	1.13×10^{-15}					0.55	4.21×10^{-15}		
V_R = -90 V	LV 90 V											0.56	1.59×10^{-14}		
Proposed Hypothesis		C_{Ga}-V_N		Surface recombination		Etching related		Native defects or related complex		C_N-C_{Ga}		N_{Ga}		Etching related	

III.4.b.ii Filling Pulse Width Dependence

By looking at the signature[7] of every trap group as a function of the filling pulse time (t_P) in **Figure 124**, since none of them has a linear increase with the logarithm of the filling pulse width (signature of extended defects such as dislocations according to [365]), they could correspond to point defects. The observed signatures can be split in two different categories:

- Category A (D1, D2 and D5 in **Figure 124(a)**, **(b)** and **(e)** respectively): their peak amplitude is proportional to the filling pulse width logarithm in a single part of the plot. This trend has already been seen in the literature [346], [366],

[7] The signature using either the a_1 or b_1 coefficients are identical (not shown here)

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- Category B (D3, D4, D6 and D7 in **Figure 124(c)**, **(d)**, **(f)** and **(g)** respectively): linear increase with the logarithm of the filling pulse width along two subsequent slopes.

In the paper of Soh *et al.* [346], when the curves exhibit a linear increase with the logarithm of the filling pulse width in a specific part, this involves the proximity of the point defects with a dislocation (assertion agreed by Polenta *et al.* [367]). Nevertheless, no consensus seems to be established yet which implies further investigations.

Finally, a decrease in the DLTFS peak can be observed at high t_P for groups D1, D3, D4 and D6 in **Figure 124(a)**, **(c)**, **(d)** and **(f)**. According to Soh *et al.* [346], it would correspond to an emission process in the main capturing section. However, the DLTS analyses the emission section, thus a hypothesis of a capture process during the emission section is more coherent.

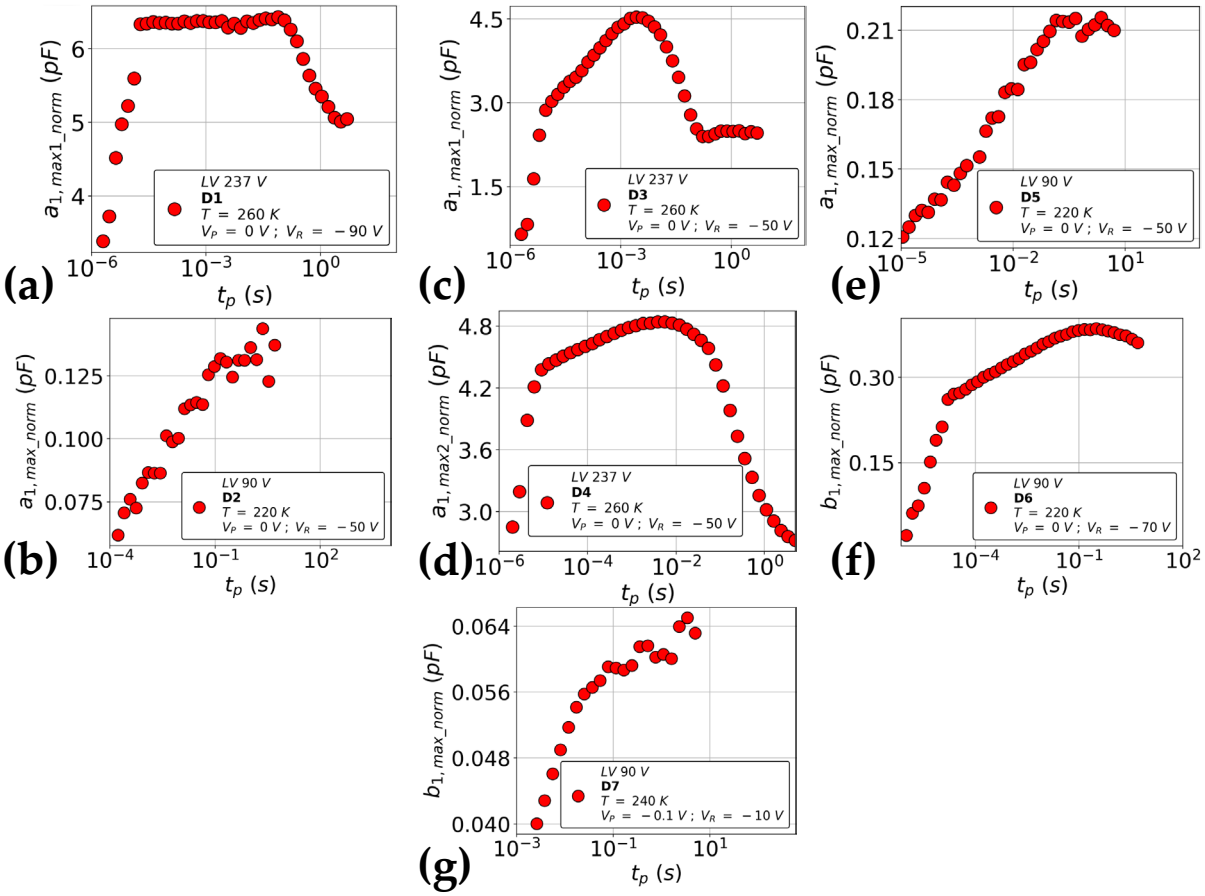

Figure 124: Normalized peak amplitude versus the filling pulse width: t_p for the different trap categories observed in this DLTFS study for both samples (adapted from [358]) (a) D1 (b) D2 (c) D3 (d) D4 (e) D5 (f) D6 (g) D7. Note: Some signals are not displayed on the entire t_P range because peaks were either out of the measured range or too small.

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III.4.c Discussion on the Possible Trap Origins

In this section, the different donor trap categories D_i ($i \in [|1, 7|]$) will be compared on the one hand to the traps reported in the literature. This is done by comparing trap properties: energy level from E_C-$E_T \in [0.36, 0.61]$ eV with their reported cross-section in **Figure 125** and also without reported cross-section. On the other hand, comparison with the theoretical studies of Jenkins *et al.* [368] and Gorczyca *et al.* [369] will be done. The trap presence at a given bias (V_P; V_R) condition is not discussed here because peak can be hidden by others at a given bias.

- Group D1 {(0.4 eV, 7.98×10^{-18} cm^2)}: The nearest traps from the literature present in **Figure 125** were reported in [346], [370]. The silicon on the gallium site Si_{Ga} hypothesis suggested by Soh *et al.* [346] is rejected because no silicon is present in the studied samples. However, the carbon-related hypothesis proposed by Ferrandis *et al.* [370] coming from *ab initio* computations of Matsubara *et al.* [371] (C_{Ga}-V_N have the (3+/2+) thermodynamic transition at 0.40 eV) is coherent with the point nature of the defects shown in the previous section. Moreover, it was found only in the LV 237 V split that has a higher RF etching bias than the LV 90 V split. The increase in the nitrogen vacancies V_N with a higher RF etching seems coherent with the C_{Ga}-V_N hypothesis. By contrast, a 0.4 eV trap (without cross-section) was found by Tanaka *et al.* and Arehart *et al.* in [372], [373]. Its presence in GaN-on-SiC and not in GaN-on-GaN samples made by Tanaka *et al.* think that this is a crystal mismatch defect [372]. It was present in ammonia-Molecular Beam Epitaxy (MBE) grown samples with a high NH_3/Ga flux ratio, hence by assuming that the high NH_3/Ga flux leads to a lower nitrogen vacancy concentration, this means that the traps reported in [372], [373] may be not V_N-related. The trap reported in [372], [373] might be associated with higher cross-section traps as reported by Honda *et al.* [289] (carbon-related traps), Ferrandis *et al.* [374] (damaged induced defect) and Polyakov *et al.* [375] (bulk defect). Whereas, group D1 can be related to C_{Ga}-V_N.

- Group D2 {(0.46 eV, 2.56×10^{-13} cm^2)}: in **Figure 125** it is located near the trap reported by [375]–[378] and has the same energy level as the one (without extracted cross-section) reported in [379]–[381]. This trap is present titanium-based contacts, not for the tantalum or indium-based ones (Boturchuk *et al.* [376]) and for nickel and gold-based contacts [375], [377],

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[378], which means that the trap is located near the surface but not related to surface contamination. Its concentration increases after electron or neutron bombardment [378], [379] and its disappearance with proton irradiation [377]. Its presence in lateral transistors (Polyakov *et al.* [375]) as well as in n-GaN samples shows that it is not specific to a device. The 0.45 eV (without cross-section) found in AlGaN/GaN superlattices [380] do not bring additional information since cross-section is rather important. Nevertheless, it is present in the LV 90 V sample only meaning that it should be related to the etching conditions. Hence, the most probable hypothesis would be surface recombination.

- Group D3 {(0.48 eV, 5.9×10^{-16} cm^2); (0.47 eV, 7.14×10^{-16} cm^2); (0.47 eV, 1.13×10^{-15} cm^2)}: they are far from the other points in literature in **Figure 125** suggesting the novelty of the associated traps. It is found only in the LV 237 V sample leading to an etching conditions induced trap hypothesis. Further studies in which the different etching parameters are investigated are necessary to push further the understanding.

Groups D4 and D5 exhibit a large capture cross-section dispersion. This specific obtained shape could be the topic of future studies since it was not investigated in this study.

- Group D4 {(0.5 eV, 1.73×10^{-13} cm^2); (0.49 eV, 7.58×10^{-15} cm^2); (0.51 eV, 1.56×10^{-13} cm^2)}: in **Figure 125** it is located near the traps reported by [376], [382]–[384]. They seem to be independent of the growth technique because they were found in samples grown by Reactive Molecular Beam Epitaxy (RMBE) and Metal Organic Vapor Phase Epitaxy (MOVPE). Ferrandis *et al.* [383] propose an etching-related hypothesis that could be questioned here in the present study because they were found in non-etched samples [384]. The same goes for the dislocation hypothesis of Boturchuk *et al.* [376] because the filling pulse width dependence is not provided. The absence of trap cross-section in the article of Götz *et al.* [385] and finding the group in both studied samples (LV 237 V & LV 90 V), do not bring additional information. Hence, the author of the manuscript proposes that traps correspond to native defects or related complexes since they do not seem to depend on the growth technique or on the etching conditions.

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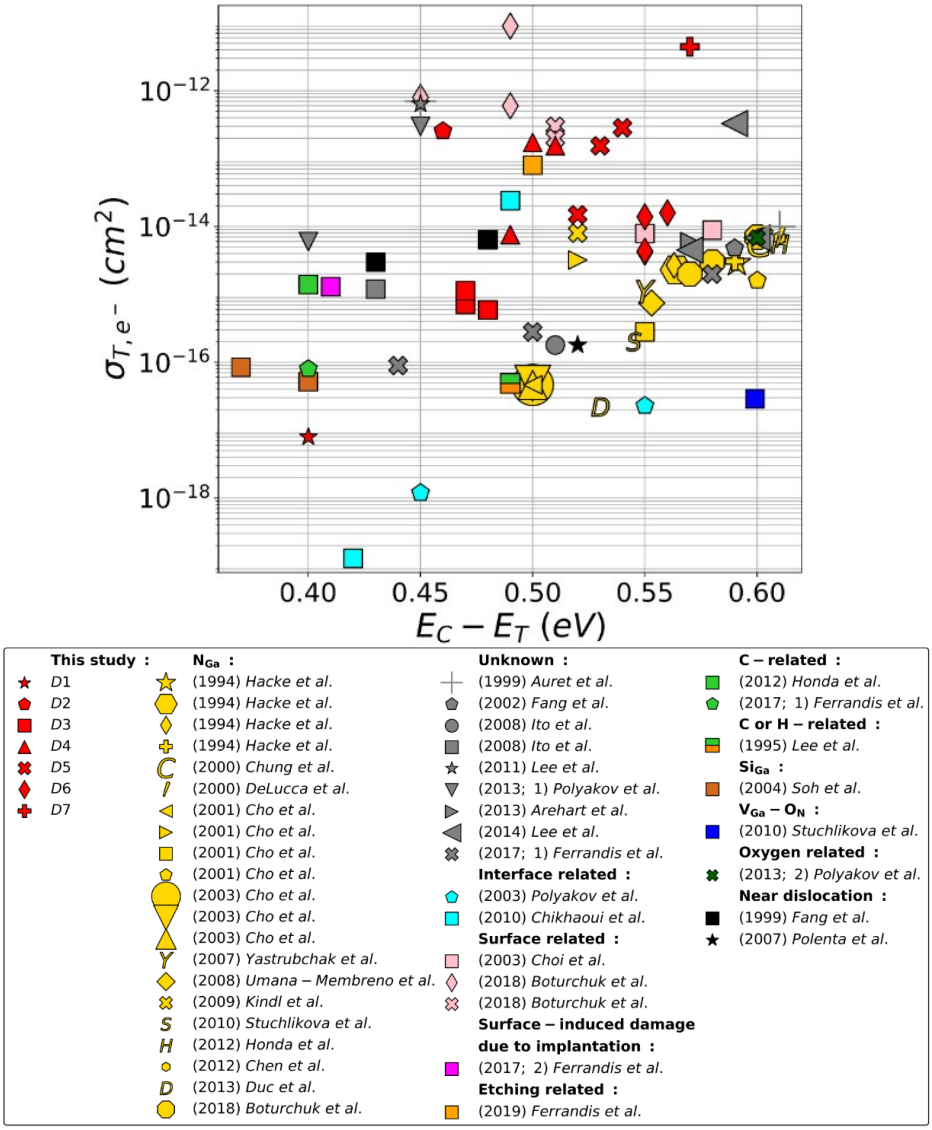

Figure 125: Cross-section as a function of the trap energy from DLTS measurements from this study and the literature corresponding to point defect with an energy level between 0.36 eV and 0.61 eV (Authors references: (1994) Hacke *et al.* [386]; (1995) Lee *et al.* [387]; (1999) Auret *et al.* [377]; (1999) Fang *et al.* [384]; (2000) Chung *et al.* [388]; (2000) Delucca *et al.* [389]; (2001) Cho *et al.* [390]; (2002) Fang *et al.* [391]; (2003) Cho *et al.* [392]; (2003) Choi *et al.* [350]; (2003) Polyakov *et al.* [380]; (2004) Soh *et al.* [346]; (2007) Yastrubchak *et al.* [366]; (2007) Polenta *et al.* [367]; (2008) Umana-Membreno *et al.* [393]; (2008) Ito *et al.* [394]; (2009) Kindl *et al.* [395]; (2010) Stuchlikova *et al.* [396]; (2010) Chikhaoui *et al.* [382]; (2011) Lee *et al.* [378]; (2012) Honda *et al.* [289]; (2012) Chen *et al.* [349]; (2013) Duc *et al.* [397]; (2013; 1) Polyakov *et al.* [375]; (2013) Arehart *et al.* [398]; (2013; 2) Polyakov *et al.* [399]; (2014) Lee *et al.* [400]; (2017; 1) Ferrandis *et al.* [370]; (2017; 2) Ferrandis *et al.* [374]; (2018) Boturchuk *et al.* [376]; (2019) Ferrandis *et al.* [383]) (adapted from [358]).

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- Group D5 {(0.53 eV, 1.55×10^{-13} cm^2); (0.54 eV, 2.85×10^{-13} cm^2); (0.52 eV, 1.49×10^{-14} cm^2)}: the smallest capture cross-section of the group (last in the list) is located in **Figure 125** near the trap reported by [390], [395]. However, those authors proposed an hypothesis that is not used in the present study because their interpretation is based on energy level comparison that do not match (error margin provided by the respective authors taken into account) that are different. The *ab initio* computations of Matsubara *et al.* [371] revealed that the carbon on the gallium site coupled with a carbon on the nitrogen site: C_N-C_{Ga} has a (+/0) thermodynamic transition at 0.52 eV. This hypothesis is coherent with their finding in MOVPE samples [390], [395] (presence of carbon in the gas precursors: TriMethylAluminium (TMAl) and TriMethylGallium (TMGa)) and finding it whatever the etching condition (LV 237 V & 90 V). Thus, D5 could be associated to C_N-C_{Ga}.

- Group D6 {(0.55 eV, 4.33×10^{-15} cm^2); (0.55 eV, 1.39×10^{-14} cm^2); (0.55 eV, 4.21×10^{-15} cm^2) ; (0.56 eV, 1.59×10^{-14} cm^2)}: there is a small dispersion (in energy and cross-section) in **Figure 125** and found near the trap reported by Choi *et al.* [350] and not far from [398], [400]. A parallel with the trap reported by Yastrubchak *et al.* [366] and Hwang *et al.* [379] cannot be drawn due to the filling pulse width dependence difference and the absence of capture cross-section respectively. However, to start the discussion, Choi *et al.* [350] reported that its trap was not related to the etching step which is also the case of D6. Moreover, the AlGaN/passivation or AlGaN traps can be rejected in the present study because it is present in as-grown GaN sample. Nevertheless, a native defect is coherent with its presence in n-GaN [350] and AlGaN/GaN system [380], [398], [400]. Jenkins *et al.* [368] and Gorczyca *et al.* [369] theoretically calculated nitrogen on the Ga site (antisite): N_{Ga} position (energy level) in the band gap. An energy of 0.55 eV was found by the most recent study [369] (based on *ab initio* calculations using a supercell approach in connection with the Full Potential-Linear Muffin-Tin Orbital (FP LMTO) method). This is therefore the chosen hypothesis.

- Group D7 {(0.57 eV, 4.45×10^{-12} cm^2)}: it is far from the other points in **Figure 125** suggesting its novelty. It is found in the LV 90 V sample only leading to an etching-related trap hypothesis. Further investigations with each etching parameter could be performed in the future to evaluate their influence on the presence of this group.

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Conclusion

In this chapter, the modeling of AlGaN/GaN Schottky Barrier Diode (SBD) fabricated at CEA LETI was tackled for a future breakdown voltage (BV) optimization. The proposed methodology that was initiated was split in three parts and consisted in identifying buffer traps that are required to get a representative electric field in TCAD simulations.

1. Capacitance characteristic was temperature dependence study performed on transistors by means of experimental and TCAD studies allowed to identify buffer deep acceptor traps properties (E_T-E_V; σ_{A,h^+}) within the whole GaN epitaxy except in the last few hundreds of nanometers. Here are the obtained information:
    - Acceptor traps' and donor traps' (E_C-E_T = 0.11 eV, $\sigma_{D,e^-} = 1\times10^{-15}$ cm^2) concentration difference respects: [A] – [D] = 1×10^{17} cm^{-3}.
    - The acceptor traps are related to V_{Ga}-$(O_N)_x$. This hypothesis was proposed by comparing its extracted (TCAD fit) properties (E_T-E_V = 1.1 eV, $\sigma_{A,h^+} = 1\times10^{-13}$ cm^2) with the literature and by bonding their concentration with the oxygen experimental one's ([A] = 1 a.u in the AlGaN buffer layer and [A] = 0.5 a.u in the GaN:C).

2. The experimental and TCAD vertical current temperature dependence study revealed that:
    - Two traps are responsible for the vertical leakage: dislocations with a cluster of punctual defects such as gallium vacancy V_{Ga} alone or paired with a nitrogen vacancy V_N (E_T = 0.27 eV) for low voltage and temperature and nitrogen on interstitial sites N_I (E_T = 0.75-0.76 eV) for high voltage and temperature.
    - TCAD modeling is limited by its AlN/Si interface to reproduce the experimental behavior. Further experimental studies based on epitaxial growth parameter variations are proposed to take into account vertical leakage in TCAD.

3. DLTFS performed on samples having different Schottky contact etching recipes revealed:
    - New etching-related traps (E_C-E_T = 0.47-0.48 or 0.57 eV) that would be located near the contacts since they rise from physical/chemical degradations of the etched surface.
    - Other donor traps in the 0.40 to 0.56 eV range. These latters may be related to deep acceptor traps compensation or to the vertical leakage in the deep buffer layers or substrate that would explain the experimental breakdown voltage dependency. Thus, they would be located in the bulk except for the surface recombinations. Nevertheless, this could not have been pushed further during the PhD.

However all these studies were not sufficient to reproduce the experimental breakdown voltage variation (lateral limitation) in TCAD simulation. Indeed, additional understandings on the vertical current are required to reach this target.

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Chapter IV
Evaluation of AlGaN/GaN Fully-Recessed MOS-HEMT Hard Switching Losses

This chapter is dedicated to the impact study of the fully-recessed MOS-HEMT layout (gate, gate to drain and field plates length) and process parameters (gate recess depth) that may be changed in the device length scaling down on the hard switching losses. The purpose is to extract scaling guidelines to optimize the switching losses. Coupled with TCAD simulation deck well calibrated allowing to reproduce static on and off experimental measurements (as started in the previous chapter), it would ease the device design. A first part will summarize the switching loss-oriented studies performed in the literature. After that, switching losses of 650 V/30 A DFN packaged transistors with two different gate recess depths will be compared and analyzed to understand the origin of the switching loss difference thanks to LTSpice simulations mainly and TCAD simulations. Finally, the layout limitation of the scaled 650 V/1 A DFN packaged transistors will be enhanced as well as some observation on the hard switching performance.

Outline

Chapter IV Evaluation of AlGaN/GaN Fully-Recessed MOS-HEMT Hard Switching Losses 180

IV.1 State-of-the-Art of E-mode Transistor Switching Losses 182

IV.1.a Simulation Approach 182

IV.1.b Experimental Approach 184

IV.1.b.i Analytical Design Rules of Hard Switching Losses (versus Temperature, OFF-State Blocking Voltage or ON-State Current) 184

IV.1.b.ii Blocking Time Impact before Switching Event 186

IV.1.b.iii External Gate Resistance Impact 187

IV.1.b.iv On-state Gate Driving Voltage Impact 187

IV.1.b.v Comparison between Power Transistor Technologies 188

IV.1.c Mixed Approach 189

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IV.1.d Summary 190

IV.2 Experimental and Simulation Study of Hard Switching Performance of E-mode Power Transistors 191

IV.2.a Methodology and Experimental/Simulation Tools Description 191

IV.2.a.i Sample Description 191
IV.2.a.ii Methodology Description 192
IV.2.a.iii Experimental Circuit Description 194
IV.2.a.iv LTSpice Simulation Presentation 196

IV.2.b Results 198

IV.2.b.i Impact of the Recess Depth on E-Mode 650 V/30 A MOS-HEMT Transistors' Hard-Switching Losses 198
IV.2.b.ii E-mode 650 V/1 A Transistor Switching Loss Analysis 205

Conclusion 208

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IV.1 State-of-the-Art of E-mode Transistor Switching Losses

This section summarizes the state-of-the-art on hard switching of AlGaN/GaN lateral transistors with a focus on switching time and switching losses. Articles taking about hard-switching impact on dynamic on-resistance [401]–[404] ($R_{ON,dyn}$ or current collapse phenomena), on V_{TH} instabilities [405] and on power converter efficiency [406] were not considered because they were not tackled in the PhD. The articles listed in the previous sentence concern AlGaN/GaN MIS-HEMTs whereas other studies performed on p-GaN gate and cascode architectures are listed in the review of Zu *et al.* [199].

The articles of interest were grouped into two categories depending on their approach: simulation and experimental approaches. It must be mentioned that only the p-GaN gate HEMT has been studied so far. Finally, a study coupling both aspects will be presented.

IV.1.a Simulation Approach

The simpler approach to tackle is to use simulation tools. Three different simulations tools were reported in [214], [407]–[409]: LTSpice®, PLECS®, Silvaco® (TCAD tool). They performed hard switching in a Double Pulse Test (DPT) circuit of transistors modeled with:

- Spice model provided by the manufacturer (GaN Systems™ in the case of [407], [408]),
- Analytical expression of the transistor losses ($E_{I/V}$, E_{OSS}, E_{qOSS}) based on the transistor properties (transconductance gm, threshold voltage V_{TH}, gate to drain charge Q_{GD}, gate to source charge Q_{GS}, internal gate resistance $R_{G,int}$) and on biasing conditions (turn-on/off gate voltage $V_{G,ON/OFF}$, blocking voltage V_{DS} and on-current I_{DS}) [214],
- Finite element modeling solving Poisson and carrier continuity equations as explained in III.1.a.ii in the case of TCAD [409].

The simulations have two different purposes:

- Provide the loss dependence values as a function of the temperature and biasing current for circuit designers as illustrated in **Figure 126(a)** as proposed by [214], [407], [408],
- Evaluate the impact on the Gate Injected Transistor (GIT architecture which is the most widely used architecture nowadays) switching time of the gate, source and drain field

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plate, an AlGaN buffer and a gate insulator [409]. They have found that considering the three elements is very interesting as shown in **Figure 126(b)**. However, the comparison with experimental results (reported also in **Figure 126(b)**) is irrelevant for two reasons: device current range is not the same (simulated devices barely conduct one Ampere whereas TPH3207WS is a 50 A device which implies different device properties such as capacitance characteristics that would impact the switching speed) and the experimental setup (gate resistance; driver) are not matched with TCAD simulations.

The main limit of these approaches is the discrepancy between simulations that do not take into account circuit parasitic elements such as stray inductance and parasitic capacitance. This was emphasized by Soares de Oliveira [410, p. 132] as enhanced in **Figure 126(c)**. Another possible limit could be the modeling accuracy (characteristic discreapancy between the model and the experiments) that may induce loss estimation errors.

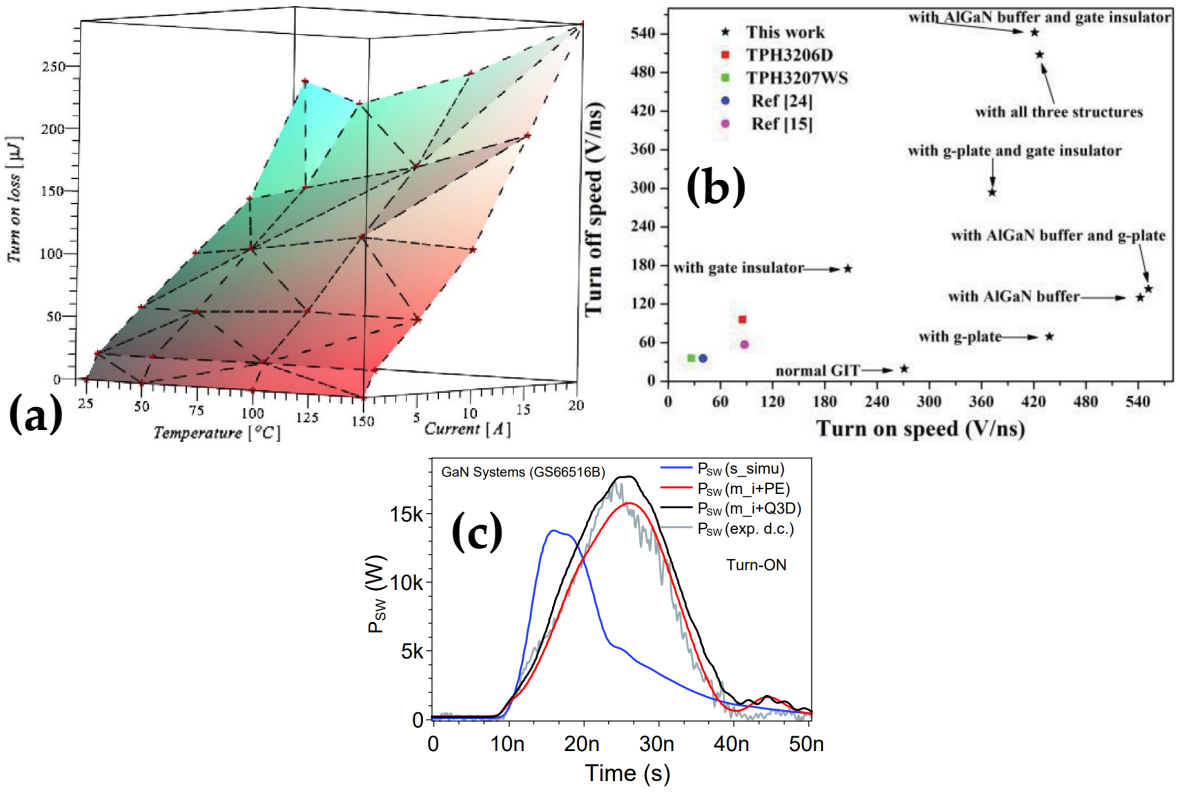

Figure 126: (a) LTSpice simulated turn-on losses of GaN System™ GS66508 as a function of the temperature and on-current [407] (b) TCAD simulated turn-on/off speed for different GIT architecture considerations [409] (c) Turn-on switching power in the experiment with deskewed signals (grey), simulations with ANSYS™ Q3D® circuit parasitic (black), simulations with probe model and loop inductance (red) and simulation without parasitic (blue) [410, p. 132].

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IV.1.b Experimental Approach

Due to the limitation enounced before the main part of the studies are experimental. They are grouped and presented depending on the study purpose concerning the hard switching losses.

IV.1.b.i Analytical Design Rules of Hard Switching Losses (versus Temperature, OFF-State Blocking Voltage or ON-State Current)

The first purpose is to propose analytical expressions of the transistor losses as a function of the operating junction temperature T_j, the blocking voltage V_{BUS} and the on-state current I_{BIAS} for power circuit designers. This was performed by:

- Jones *et al.* [411], [412] and Hou *et al.* [192], [195], [202], [413] on GaN Systems™ devices,
- Yang *et al.* [414] on a commercial p-GaN device,
- Sabzevari *et al.* [198] on Infineon™ device.

With this information, the prediction of converter losses can be performed as in the study of Hou *et al.* [415]. As illustrated in **Figure 127**, losses increase when the three operating parameters (T_j, V_{BUS}, I_{BIAS}) individually increase. The increase with:

- The blocking voltage V_{BUS} is associated to the additional time required to reach the final value while having the same dv/dt. In other words, the charge Q_{GD} is increased with the voltage V_{BUS} ($Q_{GD} = C_{GD}(V_{GD}) \times V_{GD}$). Thus, with the same charging capacity (same driver and charging current), the gate charge will be longer as shown **Figure 128(a)**.

- The on-state current I_{BIAS}. As demonstrated in the study of Sun *et al.* [416], the turn-on time increases while the turn-off time decreases. This can be explained by the variation of the charge/discharge current (**Equation 18** and **Equation 19**) as a function of the Miller/plateau voltage that varies with the biasing current as it can be seen in **Figure 128(b)**. In the turn-off, the current rise has possibly a major impact on the losses with respect to the switching time reduction.

- The junction temperature T_j is associated to the transconductance reduction with temperature [411] explained by the 2DEG mobility degradation [417].

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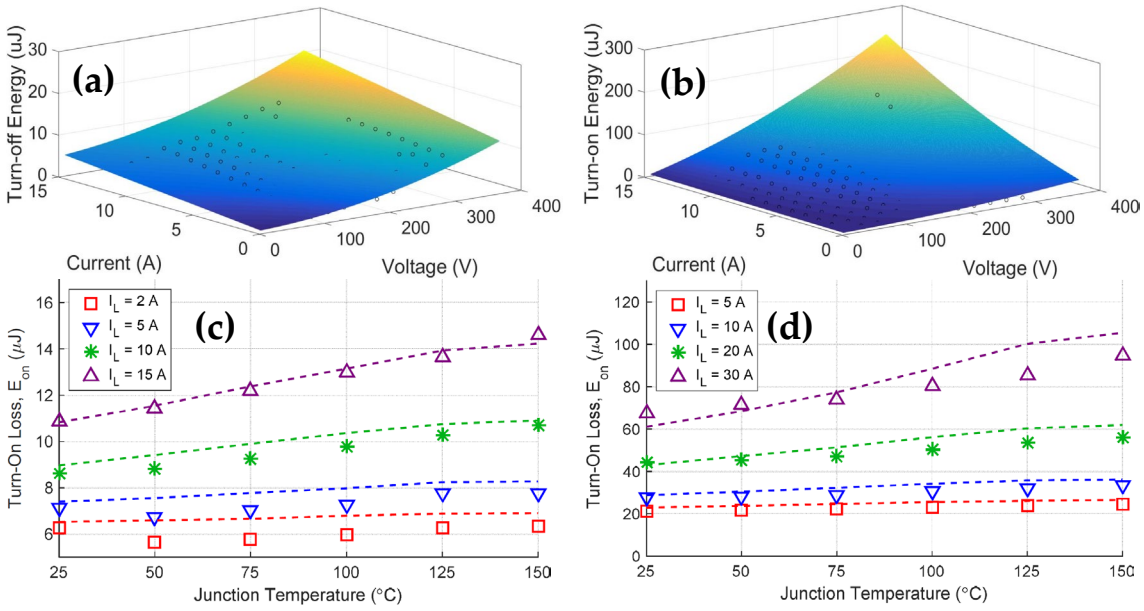

Figure 127: (a) Turn-off (b) Turn-on switching energy as a function of the blocking voltage and the on-state current (dots: experimental data; color map: analytical fit) [198]. (c) Turn-off (d) Turn-on switching energy as a function of the junction temperature (squares, triangles, stars: experimental data; dashed lines: analytical fit) [411].

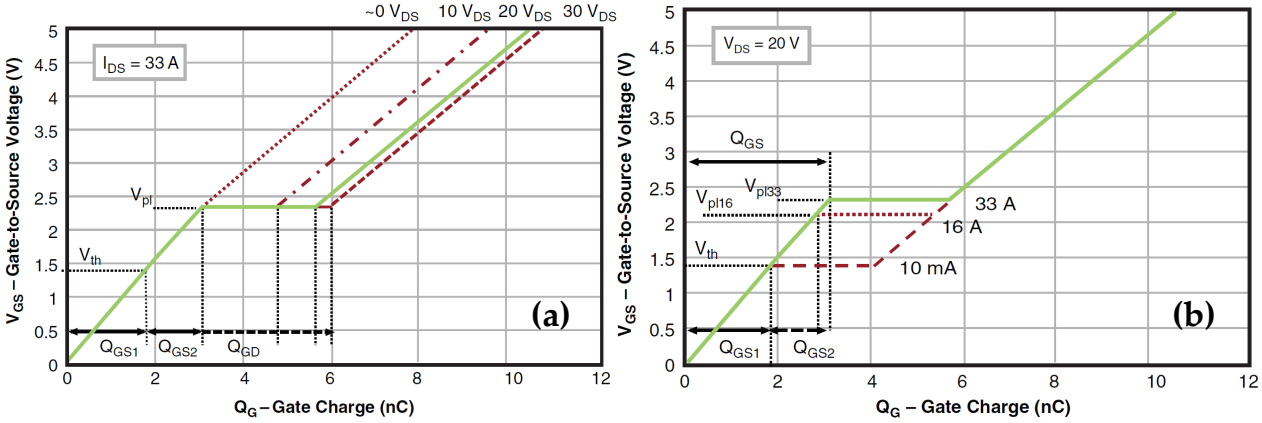

Figure 128: (a) Gate charge as a function of the blocking voltage [119, p. 92] (b) Gate charge as a function of the on-state current [119, p. 94].

$$I_{charge} = {V_G - V_{PL}}/{R_{G,ON}}$$

Equation 18: Charge current expression (V_{PL}: plateau voltage; $R_{G,ON}$: on-state external gate resistance) [119, p. 93].

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$$I_{Discharge} = {}^{V_{PL}}/_{R_{G,OFF}}$$

Equation 19: Discharge current expression (V_{PL}: plateau voltage; $R_{G,OFF}$: off-state external gate resistance) [119, p. 93].

IV.1.b.ii Blocking Time Impact before Switching Event

In the study of Yang *et al.* [418], they proposed a circuit (illustrated in **Figure 129(a)**) allowing to control the blocking time just before the start of the DPT as shown in **Figure 129(b)**. They demonstrate that using a smaller gate resistance limits the impact of the trapping responsible for the V_{TH} shift (enhanced with the blocking time) on the switching losses by comparing **Figure 129(c)** and **Figure 129(d)**.

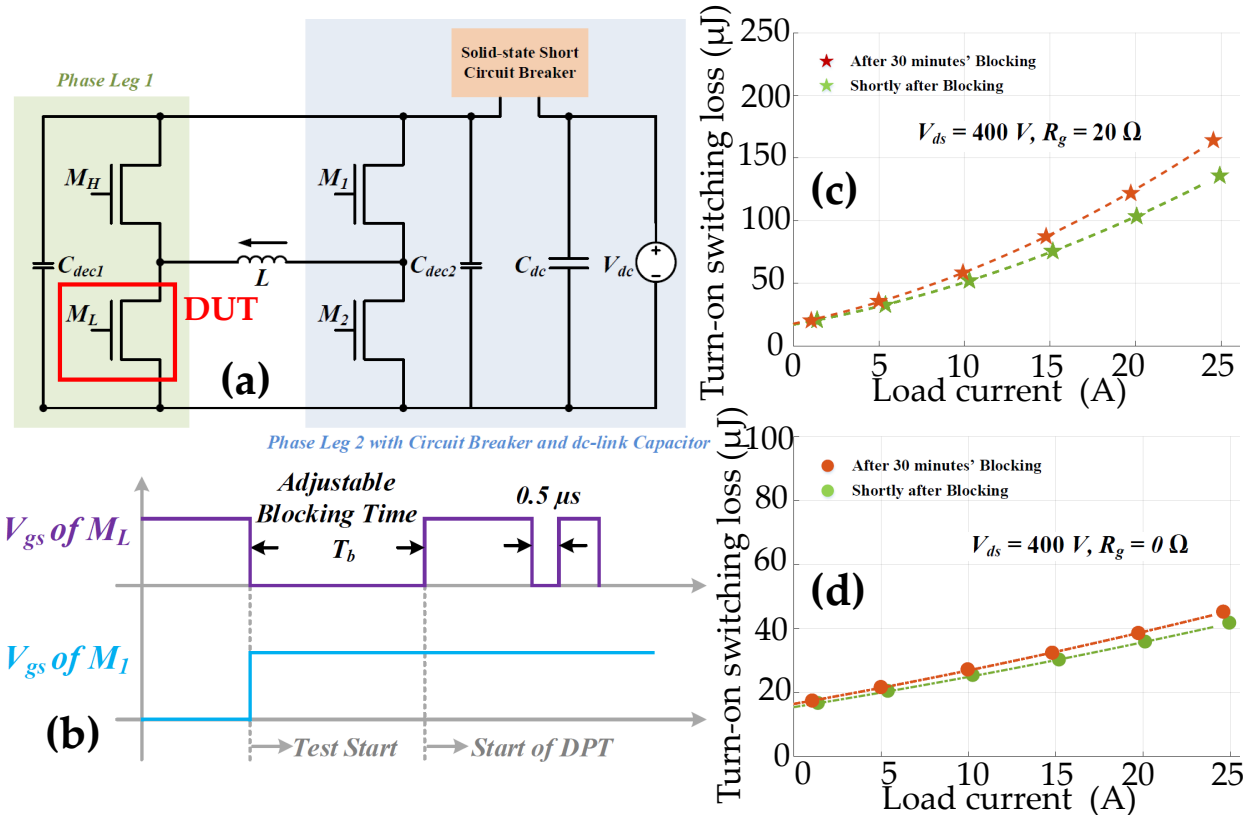

Figure 129: (Adapted from [418]) (a) DPT circuit schematics allowing an adjustable switching time (b) Modified DPT signal waveforms (c) Turn-on switching energy as a function of the on-state current with a gate resistor of 20 Ω for two different blocking times (d) Turn-on switching energy as a function of the on-state current without gate resistor for two different blocking times.

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IV.1.b.iii External Gate Resistance Impact

External gate resistance was shown to be an effective tool to slow down the transition speed reducing the parasitics-induced oscillation peak that could degrade the gate electrode [119], [419], [420]. Thus, information about their impact on the switching losses are interesting for power circuit designers. They are tackled in several articles [195], [414], [416], [421], and what is important to notice is that turn-on/off losses are increased due to the longer gate charging time (smaller charging current in **Equation 18** and **Equation 19**).

IV.1.b.iv On-state Gate Driving Voltage Impact

To optimize the switching performance (reduce the losses) while being sure not to exceed gate voltage upper limit, the on-state driving voltage was investigated. This was performed on a 650 V/13 A p-GaN gate transistor (transistor part number not specified) with external gate resistors: $R_{G,ON}/R_{G,OFF}$ = 10 Ω/1.5 Ω by Wang *et al.* [67] as illustrated in **Figure 130(a)**. The driving voltage was tested from 4 V to 6 V (driving gate voltage was tested above 4 V to prevent current collapse resulting from a V_{TH} shift [67, Fig. 5]). Two observations can be extracted from **Figure 130(a)** for the switching performance optimization:

- The turn-on energy (E_{ON}) is reduced by increasing the driving voltage. It is explained by the faster commutation (high dv/dt in **Figure 130(b)**). However, the driving voltage cannot be increased more to not exceed the 10 V limit (limit set to prevent the time-dependent dielectric breakdown of the Schottky junction [422]) in **Figure 130(c)**.
- The turn-off energy (E_{OFF}) does not vary with on-state driving voltage.

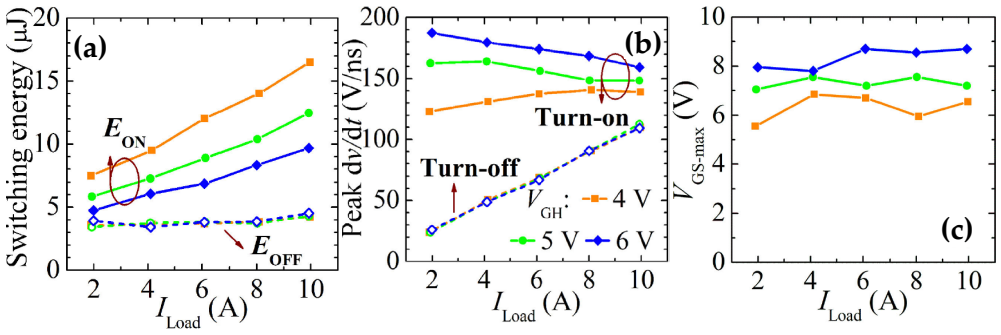

Figure 130: (a) Switching energy (b) Derivative peak of the drain voltage signal during switching (c) Maximum applied voltage on the gate as a function of the on-state current for a 650 V/13 A p-GaN gate transistor (Transistor part number not specified; Adapted from [67]).

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IV.1.b.v Comparison between Power Transistor Technologies

Comparison between different power transistors technologies is relevant to power circuit designers as proposed by Badawi [423] and Li *et al.* [424]. As **Figure 131** illustrates, the turn-on and turn-off energies of the SiC Metal Oxide Semiconductor Field Effect Transistor (MOSFET) are much bigger than these of Si Super Junction which are bigger than the one of GaN transistors (no explicit explanation provided by the author). This is probably due to the higher gate charge ($Q_{G,SiC}$ = 61 nC, $Q_{G,Si}$ = 35 nC) and device input resistance ($R_{G\text{-}int,SiC}$ = 13 Ω, not provided for the other transistors).

This kind of study can be difficult to interpret because:

- Devices do not have the same current rating (from 16 A to 20 A in [423] and 10 A to 15 A in [424])
- It is not shown in [423] but experimental setup can be different because drivers as well as packaging (TO-220 and DFN in [424]) are not the same for all transistors which may induce different overlap between current and voltage due to different circuits (as highlighted with the simulation approach limitation in IV.1.a).

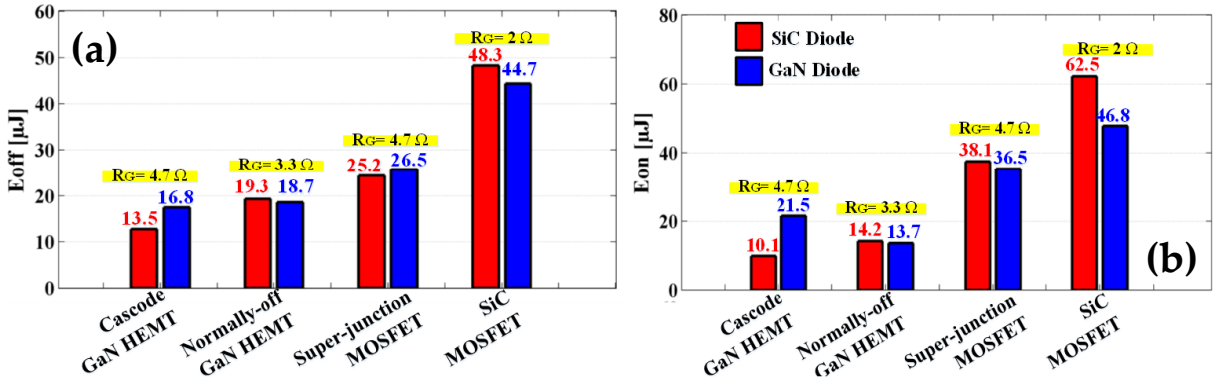

Figure 131: (a) Turn-off (b) Turn-on energy losses for different power transistors (Cascode: TPH3006PD; SiC MOSFET: SCT2120AF; Si Super Junction: IPP25R125C7; GaN HEMT: Home-made Ferdinand Braun Institute transistor) and different free-wheeling diodes technology (GaN or SiC) [423, p. 86].

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IV.1.c Mixed Approach

A new approach rose in the past few years to limit the impact of the circuit design on the extraction of the switching losses [410]. The concept relies on the following steps:

- Step n°1: Create electro-thermal Spice models of the transistor (or use the transistor model provided by the supplier [410]), discrete diodes, discrete inductances and capacitors, voltage/current probes to model the main circuit elements. These models are calibrated with:
  - Impedance characterizations for the discrete capacitors and inductances (electrical modeling only),
  - Static output, transfer and blocking characteristics ($I_{DS}(V_{DS})$ and $I_{DS}(V_{GS})$), capacitance ($C_{ISS}(V_{DS})$, $C_{OSS}(V_{DS})$, $C_{RSS}(V_{DS})$) at a single or different temperatures for the electrical model and a thermal model based either on analytical expressions (Cauer network as presented in [425]) or on thermal impedance measurements (Foster network as presented in [425]),
  - Forward, reverse and capacitance characteristic for the electrical model of the diode and same approach as the transistor for the diode thermal model,
  - Datasheet information and impedance characterization for voltage and current probes.
- Step n°2: Extracting the PCB-induced parasitic elements (RLC matrix) using ANSYS™ Q3D® or other software.
- Step n°3: Verify the good match between experimental measurements and simulations to validate circuit/device modeling.
- Step n°4: Extract the switching energy from the simulation not at the end of the probes but at the device terminations by removing the measurement tool.

However, to this day, the main drawback remains the time consumption as well as the modeling of common mode current (not tackled anywhere to the best of the author's knowledge). Moreover, the comparison between two circuits: one for GaN and the other for SiC will still have different parasitic elements that may affect the switching loss extraction.

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IV.1.d Summary

In this subpart, it was seen that the switching losses were studied through simulations (using PLECS, LTSpice or TCAD software). The studies are focused on the one hand providing switching loss estimation in different operating conditions or on the other hand on the switching loss estimation comparison between different transistors. Circuit designers are targeted by these studies. The main limitations being the circuit parasitic impact on the switching losses that are not taken into account as well as the precision of the available device model.

A second approach consists in performing experimental measurements using a Double Pulse Test setup. The impacts of the switching conditions (Temperature, Pre-stress time, on-state current, blocking voltage) on the switching losses on the p-GaN gate HEMT were reported from the literature. Most of these quantities (Temperature, on-state current, blocking voltage) increases the losses when they are larger. It was however reported that the effect of the blocking time or the switching losses can be mitigated by reducing the external gate resistance (faster transition). Indeed, external gate resistances are used to slow down the transition for safety reasons (avoid gate voltage degrading overshoot) which could increase the losses. It was also shown that the on-state gate driving voltage could be tailored to minimize the losses while keeping the gate voltage under the limit provided by the supplier. This approach is nonetheless bound by the circuit and the measuring elements (especially the shunt in the power loop) impact on the measured losses. These elements will result in discrepancy between the measurements and the real application.

A last approach was proposed to go beyond these limitations; it consists in making a simulation as close as possible to the experimental measurements in order to especially validate the device modeling in hard switching conditions. Nevertheless, the hard-switching losses comparison in simulation was skewed because different circuits are used for each transistor.

In this PhD manuscript, the objective is to make the comparison between transistors with the same impact of the testing circuit. Therefore switching losses will be extracted from experimental deskewed signals with the same testing circuit. The extracting switching losses will be compared together and not with results coming from another circuit. Thus, the relative difference between fabrication process as well as different layouts will be analyzed.

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IV.2 Experimental and Simulation Study of Hard Switching Performance of E-mode Power Transistors

IV.2.a Methodology and Experimental/Simulation Tools Description

IV.2.a.i Sample Description

In this study, three kinds of devices were studied:

- 650 V/30 A MOS-HEMTs fabricated at CEA LETI
- 650 V/30 A p-GaN gate transistors of GaN Systems™ [64]
- 650 V/1 A MOS-HEMTs fabricated at CEA LETI

IV.2.a.i.1st 30 A Transistors

In this study, the 650 V/30 A MOS-HEMTs fabricated at CEA LETI present two different gate recess depths as illustrated in **Figure 132**. They were obtained by tuning the Atomic Layer Etching (ALE) etching time of the gate recess. Nevertheless, the gate dielectric is identical for all devices. The epitaxy is the same as the one presented in III.2.b.i.1st.

A technology comparison with one of the state-of-the-art commercialized transistors, the p-GaN gate transistors of GaN systems™ having the closest packaging (DFN) [64] is also proposed in Annexe F.4. The proposed approach advantage with respect to the state-of-the-art is that the same testing circuit is used for this technology comparison allowing a pure device comparison.

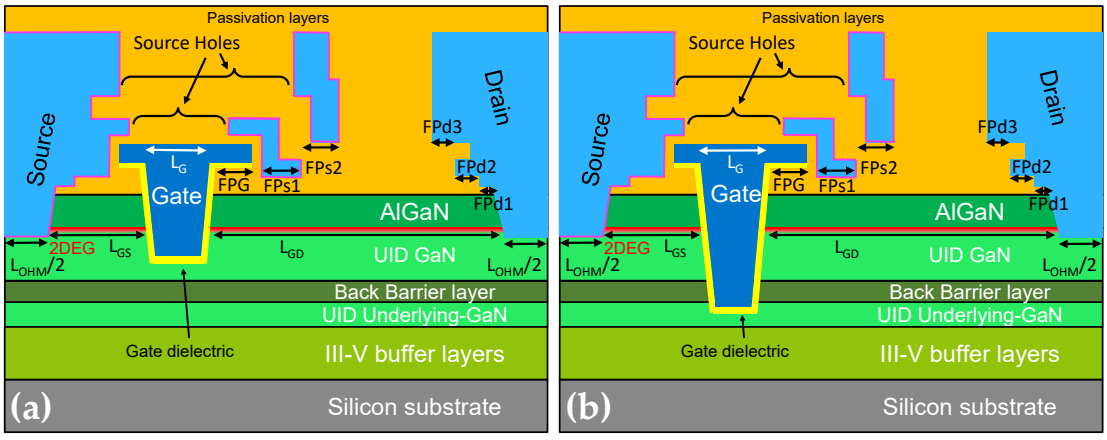

Figure 132: Schematic cross-section of the MOS-HEMT transistor with a (a) Shallow gate recess (b) Deep gate recess.

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IV.2.a.i.2nd 1 A Transistors

After that, transistors with a lower current rating were analyzed. Their epitaxy is the same as for the 30 A. They exhibit smaller gate to drain distance ("scaled layout") and several layout variations allowing to analyze their impact on the switching performance:

- Gate length L_G,
- Gate-to-drain distance L_{GD},
- Source holes presence,
- Gate field plate length FPG,
- Source field plate length FPs1, FPs2,

as illustrated on the device cross-section in **Figure 132**. Their quantitative variations are summarized in **TABLE 15**.

TABLE 15: Experimental layout split table (for a given column, the comparable split are in red).

Experimental split	L_G (µm)	L_{OHM} (µm)	L_{GS} (µm)	L_{GD} (µm)	Source holes	FPG (µm)	FPs1 (µm)	FPs2 (µm)	FPd1 (µm)	FPd2 & FPd3 (µm)
RF3	0.35	1.5	0.75	8	Yes	0.5	1.0	1.5	0.75	0.0
GF1	0.35	1.5	0.75	8	Yes	0.75	1.0	1.5	0.75	0.0
GF3	0.35	1.5	0.75	8	Yes	2	1.0	1.5	0.75	0.0
GL0	0.25	1.5	0.75	8	Yes	0.5	1.0	1.5	0.75	0.0
GL1	0.5	1.5	0.75	8	Yes	0.5	1.0	1.5	0.75	0.0
GX2	0.35	1.5	0.75	7	Yes	0.5	1.0	1.5	0.75	0.0
GX5	0.35	1.5	0.75	10	Yes	0.5	1.0	1.5	0.75	0.0
GG3	0.35	1.5	0.75	8	No	0.5	1.0	1.5	0.75	0.0
GG5	0.35	1.5	0.75	8	No	0.5	1.0	0.0	0.75	0.0
GG6	0.35	1.5	0.75	8	No	0.5	0.75	0.0	0.75	0.0
GG7	0.35	1.5	0.75	8	No	0.5	0.5	0.0	0.75	0.0

IV.2.a.ii Methodology Description

To analyze the previously presented samples, the flow chart illustrated in **Figure 133** was followed. Indeed in a first time, all the devices were characterized on their $I_{DS}(V_{DS})$ (on-state in pulsed mode at high current and off-state) and $I_{DS}(V_{GS})$ static characteristics with a Keysight® B1505 power analyzer (N1266 A expander module).

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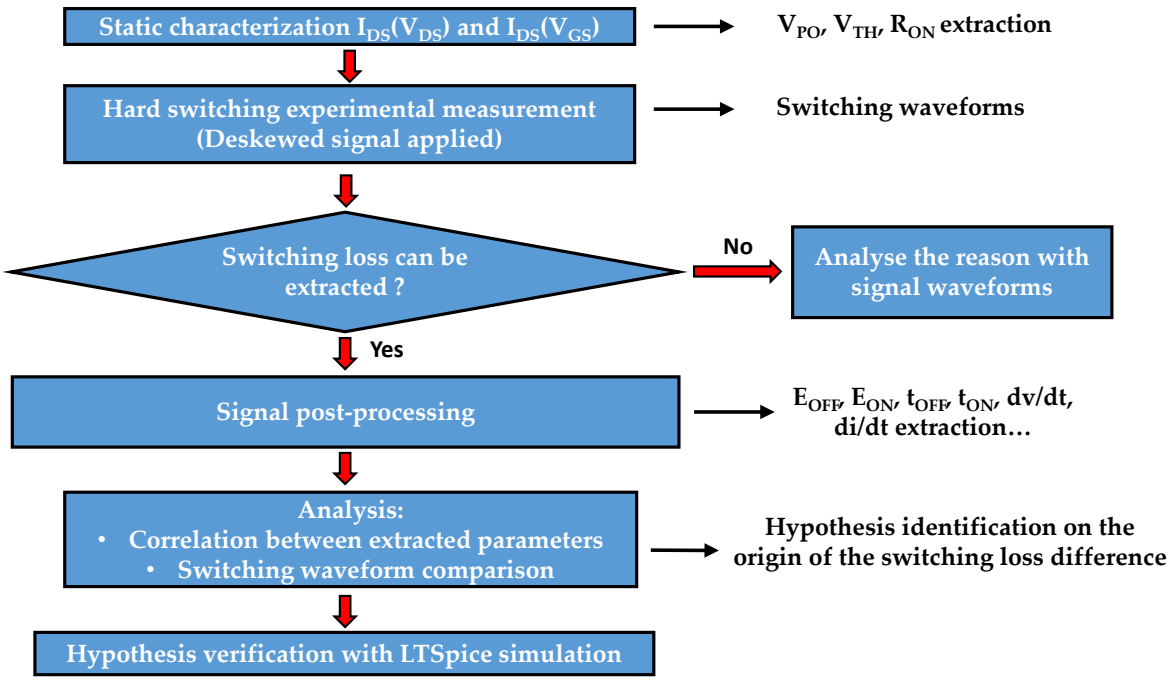

Figure 133: General method to analyze the impact of design and process variations on the transistor switching performance.

This allows the extraction of static parameters:

- V_{PO}, V_{TH}: voltages for which the current equals 10^{-10} A/mm and 10^{-5} A/mm respectively (graphical definition shown in **Figure 13**),
- R_{ON}: inverse of the $I_{DS}(V_{DS})$ curve slope at V_{GS} = 6 V for V_{DS} between 0.1 and 0.5 V.

After that, switching tests are performed on the Double Source Test (DST) bench. Note that propagation time through probing elements (current and voltage probe) are compensated before signal waveforms analysis as described in Annexe F.3. Two scenarios can be faced:

- Scenario 1: If switching losses can be extracted, switching parameters (dv/dt, di/dt, ton, toff, E_{ON}, E_{OFF}) are extracted. Switching losses are plotted as a function of switching or static properties in order to identify possible correlations that could allow proposing hypotheses on the physical origin reason of the switching loss differences. For the same purpose, switching waveforms are also observed. The hypotheses are then verified by means of LTSpice simulation presented in IV.2.a.iv.
- Scenario 2: Else, switching losses cannot be extracted. Signal waveforms are analyzed. This will be the case for some scaled 1 A transistors only as discussed in IV.2.b.ii.

This methodology applied to transistors variation exposed in IV.2.a.i.1st and IV.2.a.i.2nd provides additional understanding for the switching losses optimization of scaled transistors.

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IV.2.a.iii Experimental Circuit Description

The hard switching test circuit used in this PhD is a Double Source. As illustrated in **Figure 134**, a Labview application is controlling the drivers of the circuit power transistors including the Device Under Test (DUT). The main board (using Insulator Metal Substrate (IMS) technology) in which the DUT switches is powered with two different sources: a high voltage one (composed of a high voltage power supply and different capacitors) and one for the current (composed of a laboratory power supply, a current source circuit and an inductive load). More details about the circuit elements and working principle are provided in Annexe F.1 and F.2 respectively.

With respect to the Double Pulse Test (DPT), this circuit has on the one hand the capability of controlling the voltage and the current independently. On the other hand, there is no blocking stress of the DUT just before the switching events as presented in I.3.b.vi.

To observe signal waveforms, the current shunt and passive voltage probes described in **TABLE 16** were used (more details on the other probing techniques in Annexe F.3).

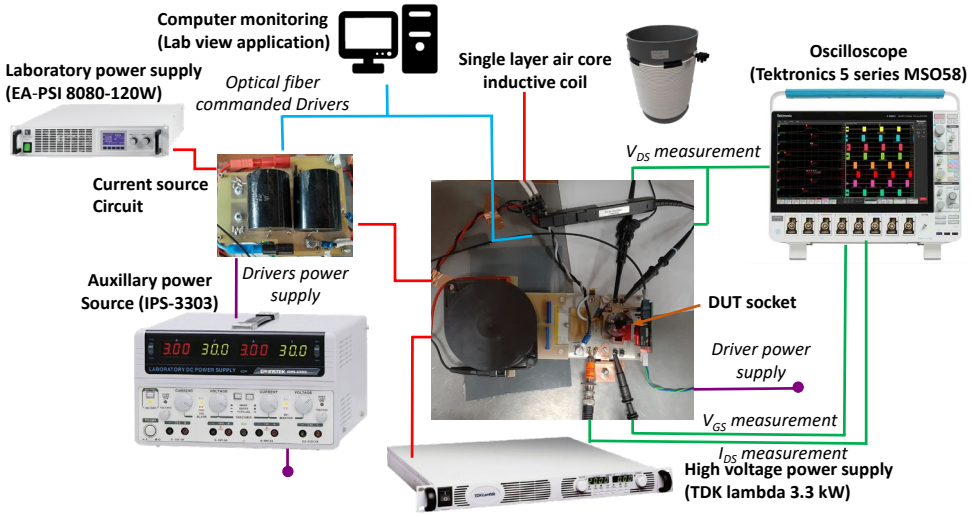

Figure 134: Physical implementation of the Double Source Test.

They were chosen according to the following criteria:

- Voltage probe: High bandwidth (no high-frequency harmonic filtering of the signal having high dv/dt), high input impedance and low input capacitance (reduce the impact on the switching characteristics),
- Current shunt: High bandwidth.

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TABLE 16: Probing elements of the Double Source Test.

Probes names	Purposes	Characteristics
Current shunt (SDN-414-10) [426]	I_{DS} measurements	Bandwidth = 2 GHz; R = 100 mΩ
High voltage probe TPP0850 [427]	V_D measurement	Bandwidth = 800 MHz; Attenuation factor = 50; Input resistance = 40 MΩ; Input capacitance = 1.8 pF; Propagation time = 6.1 ns
Voltage probe TPP0500B [428]	V_G, V_S, V_{KS} measurement	Bandwidth = 500 MHz; Attenuation factor = 10; Input resistance = 10 MΩ; Input capacitance < 4 pF; Propagation time = 5.3 ns
Oscilloscope MSO58 5 series [429]	Signals monitoring	Bandwidth = 500 MHz

The main testing conditions are summarized in **TABLE 17**. It must be noted that, due to the limited setup development time, the DUT driver has a single output, preventing the use of specific gate resistor values for the turn-off and turn-on steps. Moreover, it must be noted that the off-state gate driving voltage was chosen to prevent false turn-on events. Finally, the inductive load and the off-state times were increased and decreased respectively for 1 A transistors to limit the current drops during the blocking event.

TABLE 17: Testing conditions used with the Double Source Test.

Parameter names	Values
External gate resistance $R_{G,OFF} = R_{G,ON}$	15 Ω
On-state time before switching event t_{ON}	300 µs
Off-state time between turn-off and turn-on t_{OFF}	1.5 µs (30 A transistors)/ 0.8 µs (1 A transistors)
Inductive load	300 µH (30 A transistors)/ 1.1 mH (1 A transistors)
Gate driving voltage $V_{G,OFF}/V_{G,ON}$	-4 V/6 V

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IV.2.a.iv LTSpice Simulation Presentation

IV.2.a.iv.1st Circuit Model

To simulate the hard switching double source test within a Spice environment, the circuit illustrated in **Figure 135** was implemented. It takes into account the non-ideality of the elements that are the closest to the commutation cell (DUT and Schottky diode at the center of the figure). Thus, the voltage source is composed of two non-ideal capacitors in parallel with an ideal voltage source[8]. As for the current source, the twisted pairs as well as the inductance are non-ideal. Details on their modeling are provided in Annexe F.1.

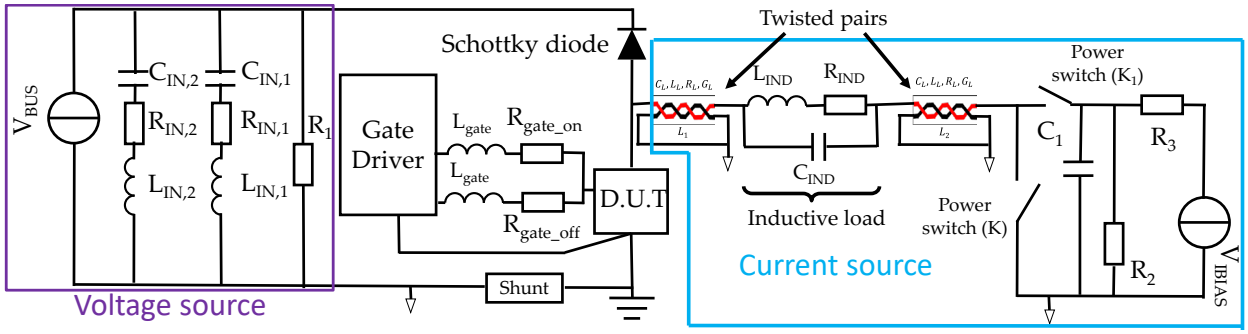

Figure 135: Simulated Double Source circuit schematics.

IV.2.a.iv.2nd Transistor Model

As for the transistor modeling, to this day, there are two main types of models [430]:

- Measurement based-empirical model like the Angelov's model that was initially developed for Heterojunction Bipolar Transistor (HBT) and Bipolar Junction Transistor (BJT) [431] and has been adapted for GaN [432].
- Physical-based compact model like the Advanced Spice Model High Electron Mobility Transistor (ASM-HEMT) [96].

The model used in this PhD belongs to the first kind. It was chosen, on the one hand, because it is known for being simpler, faster to converge even though it is limited in terms of scalability [430] (which is not critical for our purpose). And on the other hand, because the equation can be adapt to the gate type (recessed MOS-gate is different from the ASM-HEMT normally-on gate).

[8] The ideal voltage source is disconnected during the hard switching phase to emulate its non-ideality.

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The model (presented in detail in Annexe G) is constituted of four different parts:

- Access resistance due to the 2DEG, the ohmic contact, the metal resistance in the Front-end and Back-End of Line (calibration based on electrical measurements performed on test structures and unpackaged transistors),
- The resistive and inductive parasitic elements due to the packaging and the wire bonding especially (calibration based on the method described by Loris Pace [433]),
- The intrinsic small signal Metal Oxide Semiconductor (MOS) transistor model (calibration based on the experimental curve fitting of packaged transistors),
- The non-linear parasitic capacitance values (calibration based on LTSpice model fitting on experimental curves).

The model adjustment was performed on the two different packaged CEA transistors (deep and shallow recess). It was used to fit the characteristics of the transistor at 25°C as shown in **Figure 136** for the deep recess transistor (namely transfer, output, blocking, and capacitive (in blocking mode) characteristics). The model was not verified for other temperatures because hard switching tests are performed at room temperature and self-heating can be neglected for a single switching event coming after 300 µs in the on-state (justification in Annexe G.2).

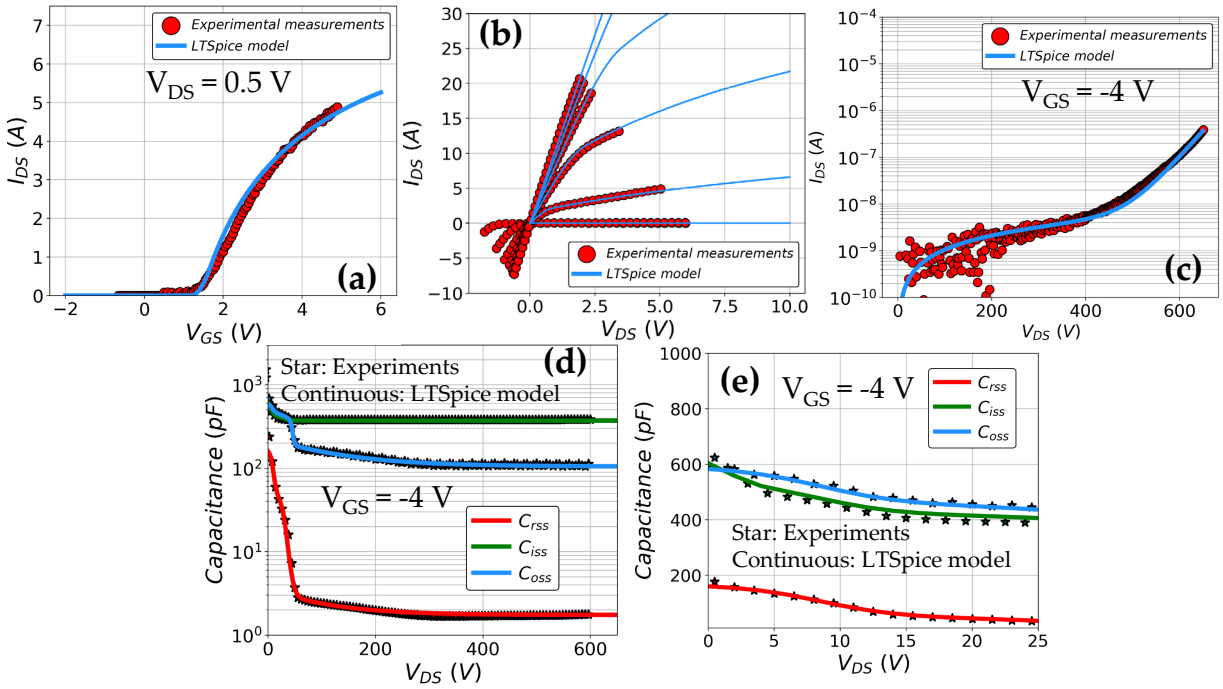

Figure 136: 30 A deep recess transistor model fitting with experimental data at 25°C on (a) the pulsed transfer characteristics (b) the pulsed output characteristics at $V_{GS} \in [|0,6|]$ V (c) the blocking characteristics (d) the C_{ISS}, C_{OSS}, C_{RSS} characteristics in logarithmic scale on the entire range (ramp rate: 3 V/s) (e) the C_{ISS}, C_{OSS}, C_{RSS} characteristics in linear scale at low voltage range (ramp rate: 3 V/s).

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IV.2.b Results

In this part, the results from the 30 A transistors will be presented first with the analysis of the gate recess impact on the hard switching. After that, the difficulty to get hard switching results for 1 A transistors will be analyzed and the most significant results will be presented.

IV.2.b.i Impact of the Recess Depth on E-Mode 650 V/30 A MOS-HEMT Transistors' Hard-Switching Losses

IV.2.b.i.1st Hard-Switching Loss Comparison

The switching losses are analyzed for both recess depths at 400 V/3 A and 400 V/5 A (not more than 5 A due to unwanted perturbations). In **Figure 137**, it can be clearly observed that, whatever the on-current, deep recess transistors (**Figure 137(b)**) exhibit higher losses than the shallow ones (**Figure 137(a)**). It can be noted (not shown here) that the dispersion comes from the E_{OFF} and the difference between 3 and 5 A as well as between deep and shallow recess resides in E_{ON}. This is why our attention will be focused on E_{ON}. According to Hou *et al.* [202], [413], E_{ON} has two contributions: the energy E_{qOSS} related to the self-discharging current from the Schottky diode connected to the DUT (that can be identified in **Figure 135**) and the energy related to the superposition of high voltage and current at the same time: $E_{I/Von}$. The latter is responsible for the loss difference since the Schottky diode and the biasing conditions are the same for both experimental splits. In the following part, the parameters that play on $E_{I/Von}$ and that differ between experimental splits will be identified.

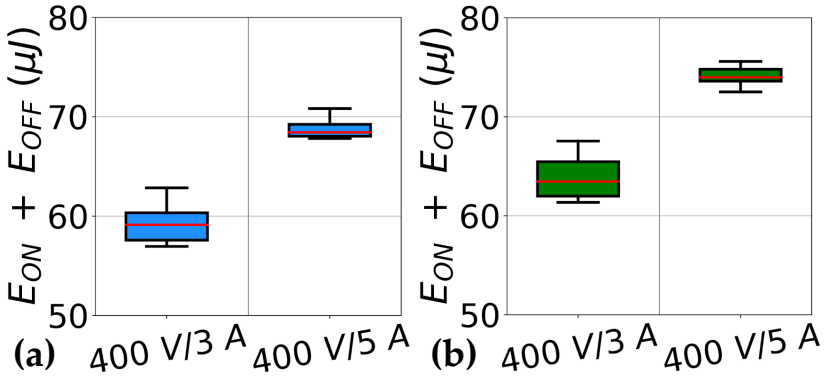

Figure 137: Experimental hard switching losses (E_{OFF} + E_{ON}) of 650 V/30 A transistors with a (a) shallow (8 devices) and (b) deep (6 devices) gate recess.

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IV.2.b.i.2nd Signal Waveforms Analysis

Looking at the switching waveforms at 400 V/5 A for both splits, it can be seen that:

- During turn-off (**Figure 138(a)**), switching waveforms are only shifted in time which explains no difference between losses,
- During turn-on (**Figure 138(b)**), signals' changes begin at the same time and it can be observed that V_{DS} drop-down is faster in the shallow recess case.

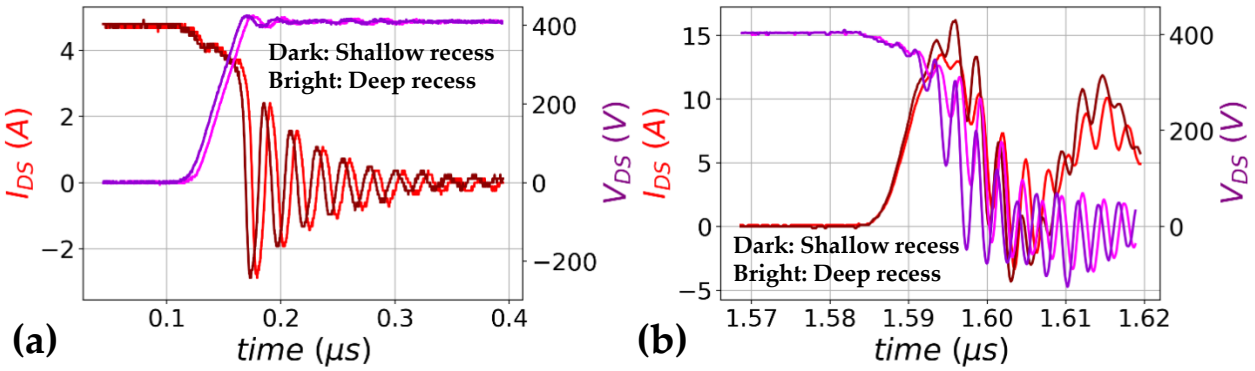

Figure 138: Experimental hard switching waveforms at 400 V/5 A of the deep and shallow gate recess transistors during (a) The turn-off (b) The turn-on.

IV.2.b.i.3rd Correlation Analysis

Plotting the turn-on energy as a function of the maximum derivative in **Figure 139(a)** clearly reveals that this physical quantity is related to the loss difference. The dv/dt values are usually related to the capacitance which is why they deserve greater interest. The capacitive characteristics illustrated in **Figure 140** show that there are several slight differences between the two splits. On the larger scale (0 to 600 V), in **Figure 140(a)**, it can be seen that C_{RSS} is a little bit higher in the deep recess case which can explain the increased C_{OSS} (= C_{RSS} + C_{DS}). Whereas, at low voltage (below 25 V), in **Figure 140(b)**, it can be clearly seen that in the deep recess case:

- The C_{RSS} value is slightly larger below 5 V which may explain the slightly higher C_{OSS},
- The C_{ISS} is significantly larger below 10 V.

→ These two observations are due to the larger gate surface in the deep recess case.

Hence, these observations on the capacitance characteristics at low and high voltage in blocking mode should contribute to the loss differences.

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Furthermore, by investigating the possible correlation with static parameters, it was found that the threshold voltage difference between the experimental split, as shown in **Figure 139(b)**, could be one of the possible reasons for the loss differences.

To figure out the main reasons for the loss differences, a study based on LTSpice simulations was performed as presented in the next part.

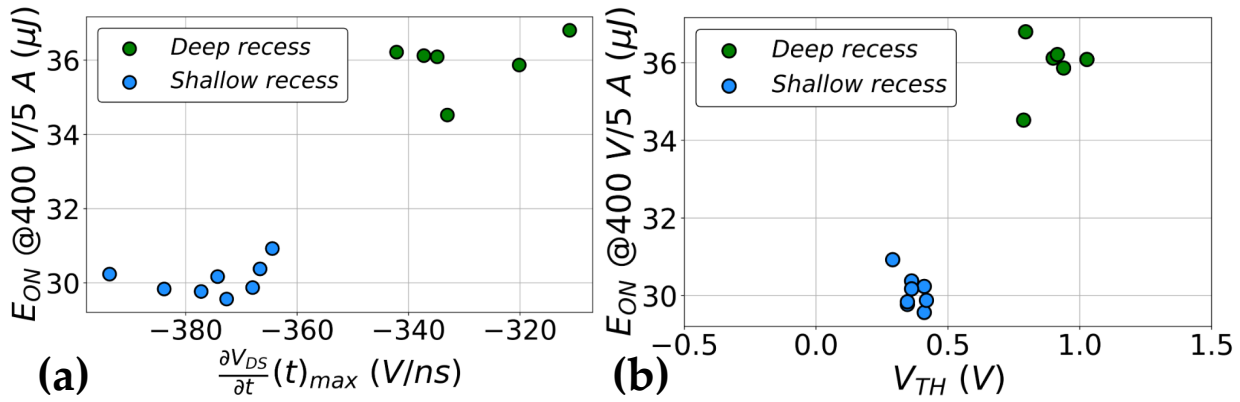

Figure 139: Experimental turn-on energy losses (E_{ON}) during hard switching as a function of (a) the derivative maximum of the measured drain to source voltage (V_{DS}) with respect to time (b) the threshold voltage (V_{TH}).

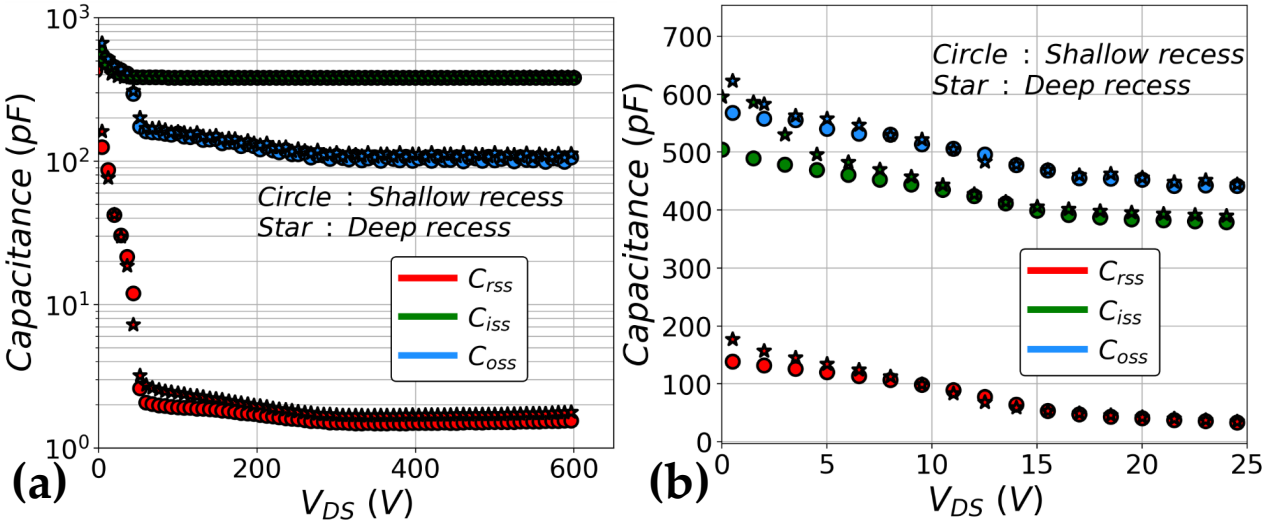

Figure 140: Experimental Miller (C_{RSS}), Input (C_{ISS}), Output (C_{OSS}) capacitance characteristics performed at a ramp rate of 3 V/s for the shallow and deep gate recess sample (a) in logarithmic scale (b) in linear scale.

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IV.2.b.i.4th Hypothesis Verification on LTSpice

To identify the elements that have the most significant impact on the switching losses and explain the difference between the studied experimental splits, LTSpice transistor model has been fitted on experimental deep and shallow recess data (explained in IV.2.a.iv.2nd). The model parameters that change between both cases were grouped when they target the same part of the device characteristic as detailed in **TABLE 18** (more quantitative details provided in Annexe G.1). Thus, the simulations were performed to extract hard switching losses from the transistor model fitting of the shallow gate recess and the deep gate recess cases by modifying a single or a group of characteristic model parameters (explained in **TABLE 18**) as illustrated in **Figure 141**. This figure clearly shows the two elements that influence the most hard-switching losses:

- The threshold voltage: V_{TH} change (change between "Shallow mod2" and "mod3"),
- The capacitance C_{GD} change at high voltage (change between "mod3" and "mod4"),

It must be noticed that the $E_{ON} + E_{OFF}$ quantities are different when comparing experimental data with simulation results. Tests were performed and show that parasitic elements in the power circuit play significantly on the on-state losses because of the induced dephasing between the voltage and current (not shown here). The next part will be dedicated to the physical explanation of the two physical parameter differences between the experimental splits.

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TABLE 18: LTSpice simulation splits.

Simulation split name	Characteristics
Shallow std	Model parameters allowing to fit the characteristics of the shallow recess split
Shallow mod1	Model parameters of "Shallow std" exept the model parameters that are fitting the blocking characteristic of "Deep std"
Shallow mod2	Model parameters of "Shallow mod1" exept the channel mobility of "Deep std"
Shallow mod3	Model parameters of "Shallow mod2" exept the threshold voltage of "Deep std"
Shallow mod4	Model parameters of "Shallow mod3" exept the model parameters to fit the C_{GD} characteristic at high voltage of "Deep std"
Shallow mod5	Model parameters of "Shallow mod4" exept the model parameters to fit the C_{GD} characteristic at low voltage of "Deep std"
Deep stp	Model parameters allowing to fit the characteristics of the deep recess split

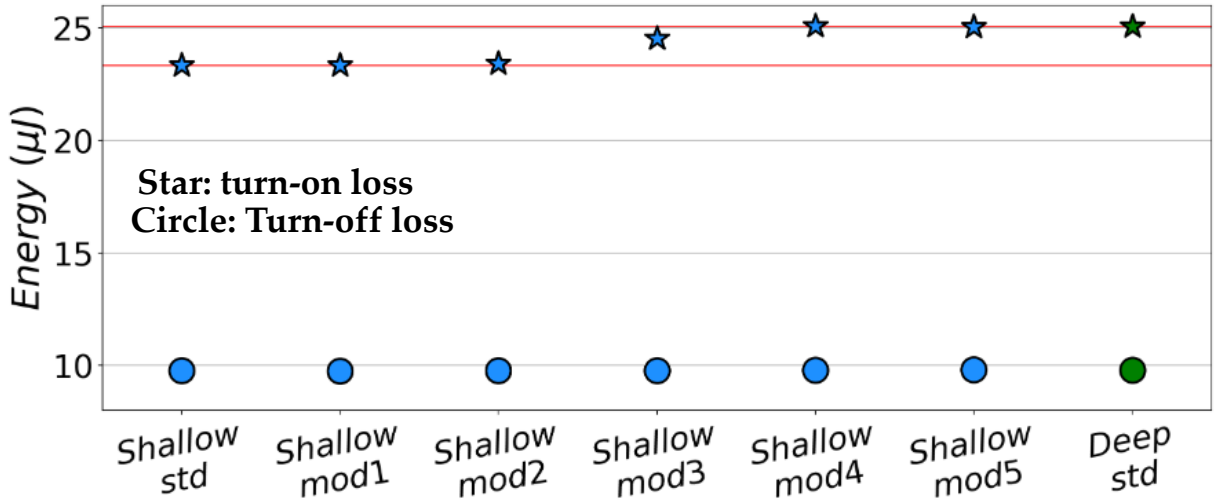

Figure 141: Simulated turn-on and turn-off energy losses during hard switching with transistor models going from the shallow to the deep gate recess model (fitted on experiments). The intermediate steps are named: modi with i Є [|1, 5|].

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IV.2.b.i.5th Physical Reasons of These Hypotheses

† C_{GD} difference at high voltage in blocking mode

As illustrated in **Figure 142**, at high voltage the 2DEG is completely depleted under the gate and source field plates. Thus, the remaining capacitive coupling between the gate and the drain relies on the fringing capacitance illustrated in purple in the figures. The larger the recess depth, the larger the capacitance.

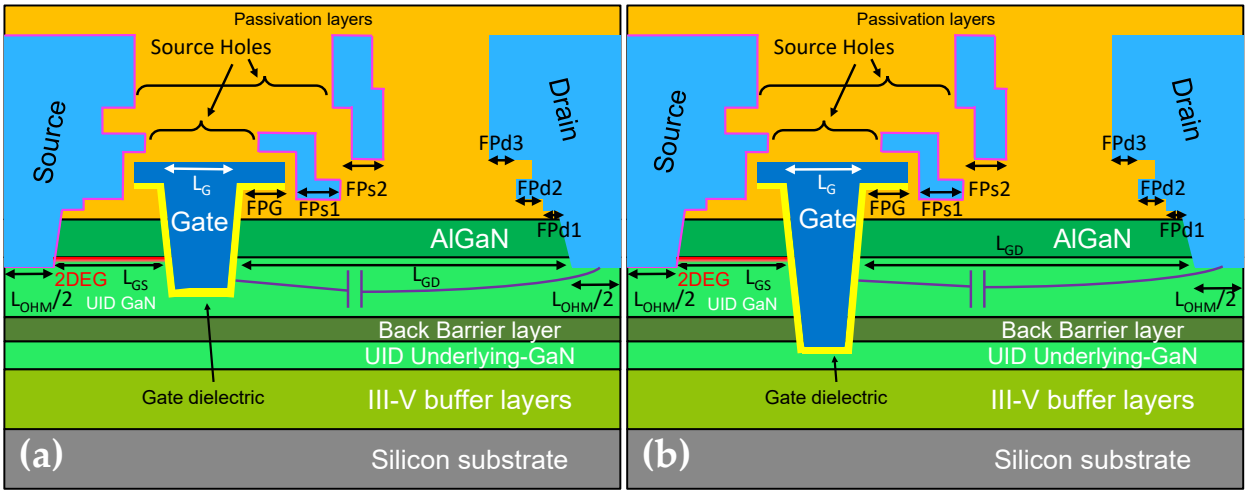

Figure 142: Schematic cross-section of the MOS-HEMT transistor with a (a) Shallow gate recess (b) Deep gate recess with the enhancement of the fringing capacitance (in purple) responsible for the high voltage Miller capacitance plateau.

† V_{TH} difference

By running TCAD simulations with the following conditions:

- Donor traps at the AlGaN/passivation interface (E_C-E_D = 1.6 eV [46], [50]; [D] = 5×10^{13} cm^{-2}) for the 2DEG formation[9],
- Piezoelectric model activated everywhere except at the Al_2O_3/GaN, Al_2O_3/AlN, Al_2O_3/AlGaN interfaces (this ideally assumes the interface traps completely compensate the spontaneous piezoelectric charges),
- Deep acceptor traps and shallow acceptor traps in the III-V buffer layers as enhanced in III.2.b.v and in [301] ([A] = 1 a.u. in the $Al_xGa_{1-x}N$ buffer layers ; [A] = 0.5 a.u. in the GaN except for the last two hundred nanometers; [A] – [D] = 1×10^{-17} cm^{-3}; E_A - E_V = 1.1 eV; $\sigma_A = 1\times10^{-13}$ cm^2; E_C – E_D = 0.11 eV),

[9] The 2DEG charge density does not need to be adjusted with the piezoelectric model activation because only the subthreshold regime which is limited by the carrier diffusion in the channel at the GaN/dielectric interface.

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the difference in the transfer characteristics without stress between the two experimental splits can be reported as shown in **Figure 143(a)** and **(b)**. On these figures, the experimental transfer before (**Figure 143(a)**) and after (**Figure 143(b)**) hard switching tests is also shown. It seems that hard switching tends to match the ideal scenario represented by TCAD simulation. Further investigations made on the back-barrier to 2DEG distance (**Figure 143(d)**) and III-V buffer to 2DEG distance (**Figure 143(c)**) demonstrate that the back barrier does not play a role on the threshold voltage value but the distance between the III-V buffer and the gate bottom does. Therefore, the closer the III-V buffer from the gate bottom, the larger the threshold voltage.

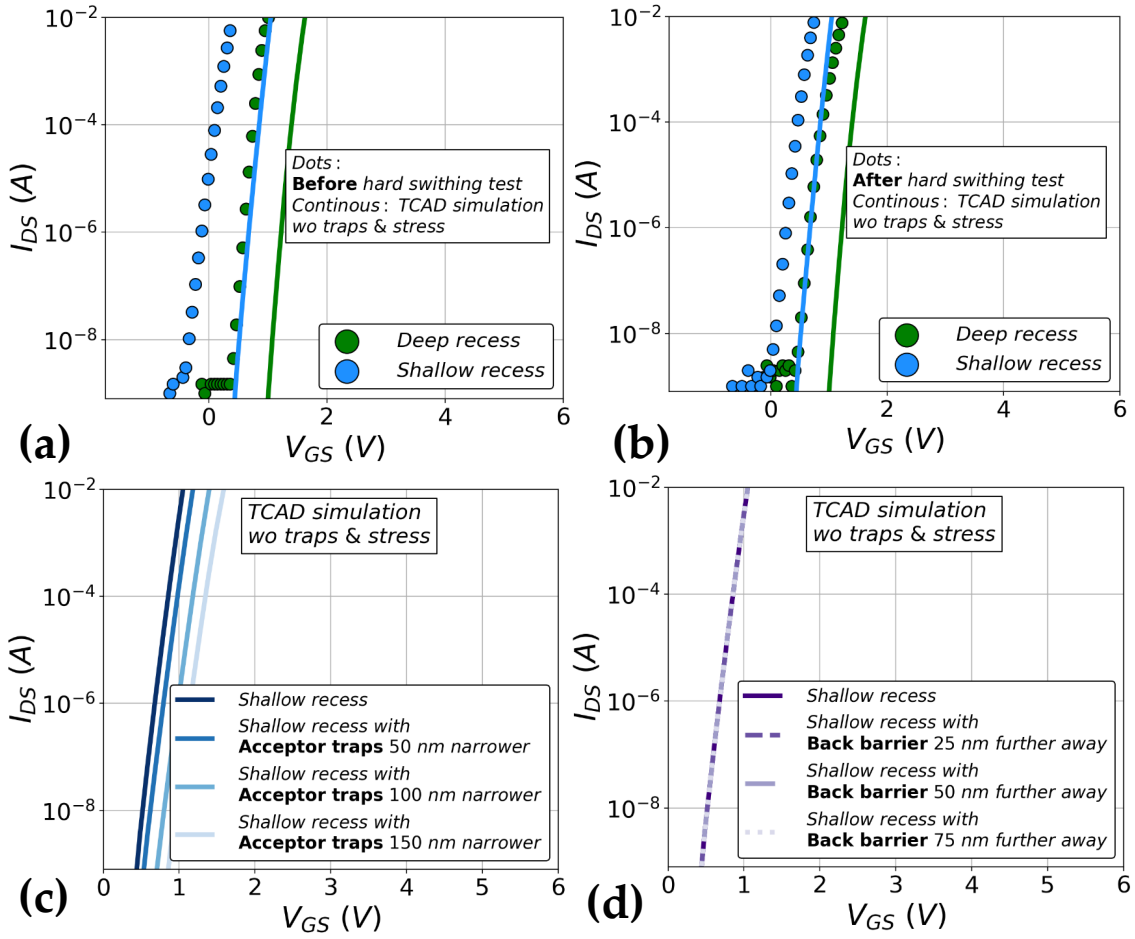

Figure 143: At 25°C, simulated transfer characteristics of a non-stressed device (simulation conditions at the beginning of the V_{TH} paragraph) superimposed with the experimental measurements (a) before and (a) after hard-switching tests. At 25°C, simulated transfert characteristics of the shallow recess when changing (c) the distance between the acceptor traps distribution and the gate bottom (d) the distance of the backbarrier with the heterojunction.

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IV.2.b.ii E-mode 650 V/1 A Transistor Switching Loss Analysis

IV.2.b.ii.1st Before Hard Switching Tests

In this PhD, part of the work consisted in participating in the design of the mask used to fabricate the 1 A transistors that are considered here. Another part of the work consisted of the follow-up of all of the fabrication steps including the proposal of solutions to optimize wafer dicing and DFN packaging. This subpart summarizes the results of the packaging step and the setup of the hard switching test bench as well as their limitations. Three observations can be made from **Figure 144(a)**:

- Lot of devices **were broken due to the packaging** step and some devices exhibited gate leakage (never seen for the 30 A packaged transistors). By looking at their proportion as a function of the source-to-drain field plate distance in **Figure 144(b)**, it is clear that the defectivity potentially comes from an ElectroStatic Discharge **(ESD) in between the edge of FPs2 and Fpd3 (peak effect)**.
- The functional devices proportion as a function of the source to drain field plate distance shown in **Figure 144(c)** follows the inverse trend with respect to the previous point, which means that packaging was the bottleneck of device supply for this PhD.
- **Gates broken when the drivers' power supply** was switched on which may be the origin of a non-recoverable breakdown of the gate. Its occurrence does not seem to be correlated with the device layout (that mainly changes the gate to drain region). It may be therefore due to **ESD between the gate and the source**.

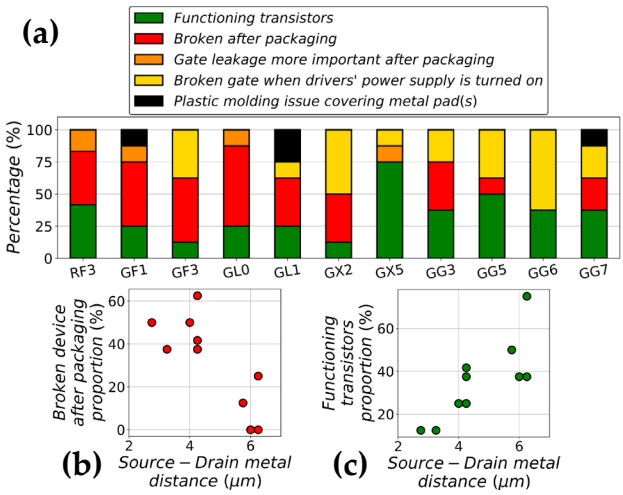

Figure 144: (a) Proportion bars for each device layout (8 devices per layout) of the packaged transistors status just before hard switching tests; Proportion of (b) broken or (c) functioning transistors as a function of the source to drain distance (L_{GD} - (FPG + FPs1 + FPs2 + FPd1 + FPd2 + FPd3) in terms of layout distances).

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IV.2.b.ii.2nd After Hard Switching Tests

† Impact of the gate length on the hard switching losses

Varying the gate length from 0.25 µm (GL0 layout in **TABLE 15**) to 0.5 µm (GL1 layout in **TABLE 15**), two observations can be made:

- The switching losses slightly decrease for smaller gate length layouts as illustrated in **Figure 145(a)**.
  Hypothesis: The threshold voltage (V_{TH}) roll-off (short channel effect that is ascribed to the reduction of the gate electrostatic control causing a V_{TH} lowering) makes the switching faster. It seems coherent with the correlation between E_{ON} and V_{TH} for the tested devices exposed in **Figure 145(b)**,
- The oscillation amplitudes are larger for smaller gate lengths during turn-on (**Figure 145(c)**) and not during turn-off (**Figure 145(d)**).
  The proposed hypothesis was that faster switching leads to more inductance feedback effects. However, there is no strong correlation between the current derivative maximum and the oscillation maximum as shown in **Figure 145(e)**. Further studies with a more physical-based compact model may be used to figure out the origin of this.

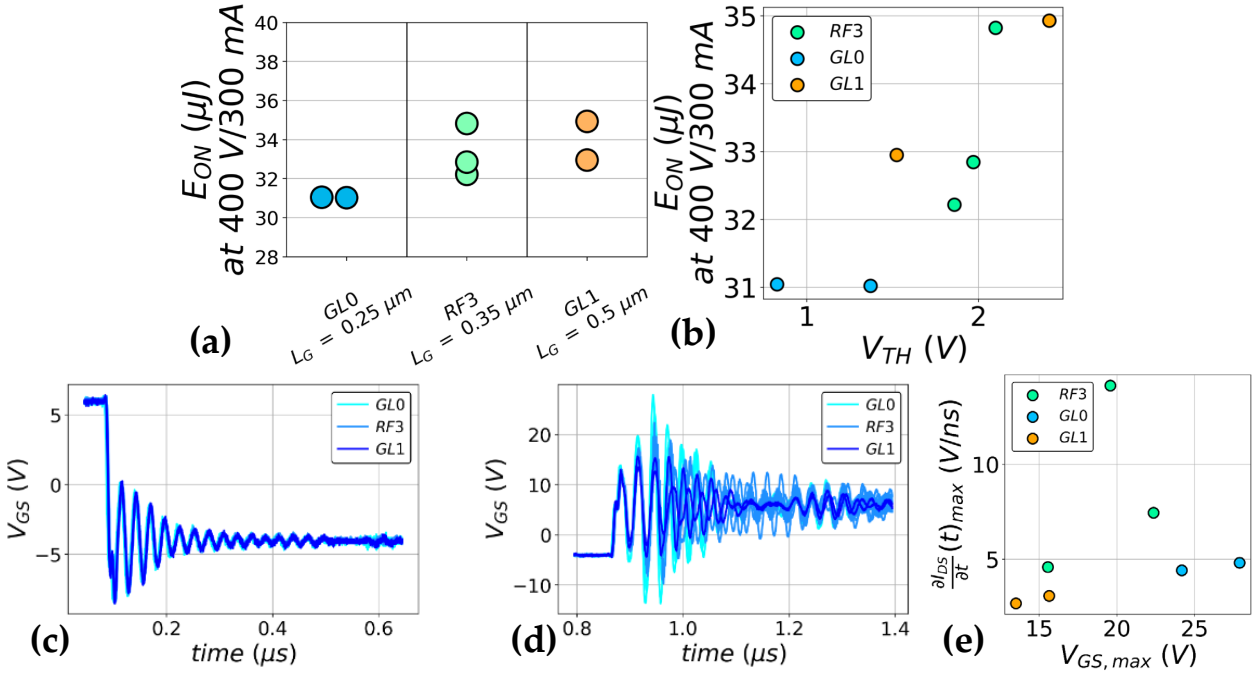

Figure 145: Experimental turn-on losses as a function of (a) the device layout (b) the static threshold voltage (V_{TH}) before the tests; measured experimental gate voltage during (c) hard turn-off (d) hard turn-on; (e) the derivative maximum of the measured drain-to-source voltage (V_{DS}) with respect to time as a function of the maximum measured gate-to-source voltage (V_{GS}).

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† **Some devices lead to unexpected hard switching waveforms**

Focusing our attention on devices having (RF3 in **TABLE 15**) or not (GG3 in **TABLE 15**) the source holes, it can be seen that the gate voltage does not reach the on-state driving voltage (6 V) before the turn-off (**Figure 146(a)**) and after the turn-on (**Figure 146(b)**). This comes with unexpected switching waveforms as illustrated with the V_{DS} signal that does not reach 400 V before the switching as illustrated in **Figure 146(c)** and **(d)**. Furthermore, this observation on the gate leakage is valid for the entire on-state regime before the hard-switching event. The comparison of the transfer function before and after hard switching measurement in **Figure 146(e)** reveals that there is no gate leakage path even at 6 V. Thus, the gate leakage hypothesis can be discarded. This unwanted phenomenon occurred on GG3, GG7, GG6, GX5, GF3 devices, which prevents any layout-related hypothesis by looking at **TABLE 15**. To this day, no hypothesis was found. It is suggested for the future to test possible cross-coupling hypothesis thanks to TCAD simulation in mixed mode simulation with LTSpice.

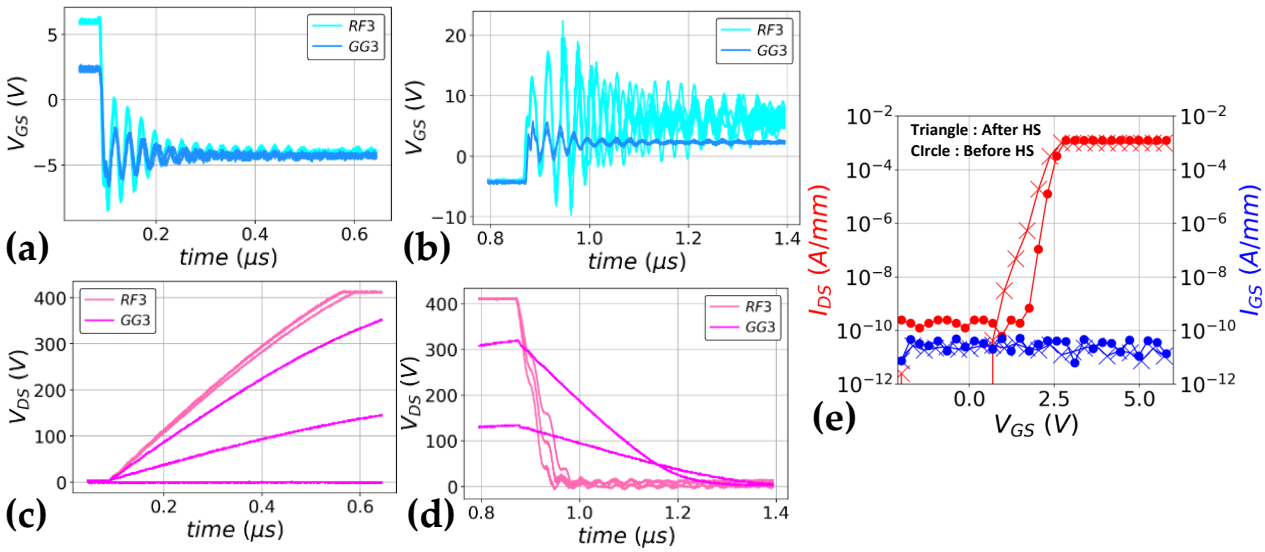

Figure 146: For transistor with (RF3 in **TABLE 15**) or without (GG3 in **TABLE 15**) source holes: Measured experimental gate voltage during (a) hard turn-off (b) hard turn-on; Measured experimental drain to source voltage during (c) hard turn-off (d) hard turn-on; (e) Experimental transfer characteristic at 25°C (compliance at 8 mA) before and after Hard Switching (HS) tests of a GG3 transistor.

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Conclusion

This chapter dealt with the study of the fully-recessed MOS-HEMT layout and process parameters' impact on the hard switching losses. Previous experimental/simulation studies performed on e-mode transistors were on the p-GaN gate HEMT. By contrast, with the most advanced technique to extract switching losses that rely on many modeling without taking into account electromagnetic coupling as well as common mode current (circuit design dependent), this PhD is focused on switching loss relative difference analysis with deskewed signal (probe propagation time compensation) and for the first time on GaN fully recessed MOS-HEMTs.

- The study of the recess depth revealed that the deeper the recess, the larger the switching losses especially during turn-on. Correlation and waveform observations oriented the research on the non-linear capacitance as well as threshold voltage to explain the difference. LTSpice simulations with a calibrated model on output, transfer, blocking and capacitance characteristics at 25°C were performed splitting the parameter differences between the shallow and the deep recess. They highlighted the significant impact of the threshold voltage (shown to be caused by the distance of the gate bottom with the buffer traps in TCAD simulations) and the $C_{GD}(C_{RSS})$ plateau at high voltage (influence of the recess depth on the effective gate area) on the switching losses.

- The layout dependence study performed on scaled transistors showed, first, that the packaging step limited the number of available devices probably due to electrostatic discharge in between the drain and the deported source field plates (probably due to peak effect). This can be mitigated by either moving apart these metals or by rounding metal corners by modifying the process flow. Secondly, it revealed that switching losses slightly decrease with smaller gate length layouts probably due to the V_{TH} decrease (roll-off). However, reducing this parameter makes the gate voltage oscillate which can be problematic (in terms of driving stability) if pushed too far. Finally, unexpected behavior was discovered: on-state driving voltage could not be reached and investigations did not succeed so far.

Furthermore, this chapter has shown the test bench limitation especially with the potential gate to source ESD occurring during driver power supply turn-on. Another limitation that was not presented here is that it was unstable at high current value. For instance, 30 A transistors could not be switched at 400 V/8 A and higher current without unwanted huge oscillations. This may be due to parasitic and ElectroMagnetic Coupling (EMC). However, this issue became known at the end of the PhD, when wire bondings of the package devices were adapted to match the DFN pinout of GaN Systems™ transistors. This aspect needs to be tackled before further hard-switching tests.

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General Conclusion

Summary, Results and Scientific Contributions

GaN was initially interesting for its material intrinsic properties: high critical electric field and polarisation (allowing high electron mobility reached in a 2DEG at the heterojunction in between two piezoelectric materials: $Al_{1-x}Ga_xN/GaN$). These properties were used to build Schottky diodes as well as normally-off power transistors. This is especially the case for the 650 V/6 A AlGaN/GaN-on-Si Schottky barrier diode and the 650 V/30 A AlGaN/GaN-on-Si fully-recessed MOS-HEMT manufactured at CEA LETI (studied in this manuscript). Both devices use a stepped field plate structure to withstand high voltage as well as insulating buffer layers. On the one hand, no strict advantage has been identified for the lateral GaN Schottky diode with respect to the vertical SiC one yet but it is a very useful test vehicle (especially for the breakdown studies performed in this thesis). The power transistor that was studied can be used in power converters (consumer, automotive, industry, photovoltaic, more electric aircraft applications) with an output power in the 0.01 to 10 kW range and have a switching frequency in the 10 kHz to 10 MHz. GaN transistors are more interesting with respect to the vertical Si and SiC counterparts in these power and switching frequency ranges for their negligible Q_{RR}, lower $R_{ON} \times C_{OSS}$ and lower $R_{ON} \times Q_G$.

Nevertheless, it was shown on the transistor $R_{ON,SP}$ vs BV figure of merit that its performance was far from the theoretical expectation probably due to a non-optimal electric field management. This figure of merit can be improved by scaling down the device length and putting efforts into electric field management. This is why the electric field distribution was tackled in this PhD.

This was performed first by analyzing the experiental breakdown voltage with a destructive technique to evaluate the experimental device limitation. Indeed, breakdown measurements made on lateral power Schottky diodes having different layouts and epitaxies with or without the substrate connected to the anode at different temperatures were analyzed to quantitatively assess their impact on the breakdown voltage. Electrical and physical failure analysis was performed to

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identify the breakdown mechanism and location. On the one hand, devices with the substrate connected to the anode were shown to be limited by the vertical breakdown whatever the anode-to-cathode distance available. For the first time an experimental proof of the nucleation layer (AlN) dielectric breakdown probably assisted by the already present dislocations was provided. On the other hand, devices with a floating substrate were shown to have a higher breakdown voltage with respect to vertical one, strongly suggesting the substrate auto-polarization. By varying the anode-to-cathode length from 16 µm to 30 µm, two different regimes were identified:

- A linear regime at small anode-to-cathode distance in which the breakdown increases with the distance. The lateral breakdown literature hypothesis was confirmed with the first observation on a Schottky diode of a dielectric breakdown between the first anode field plate corner and the heterojunction. In addition, this breakdown voltage can be improved with the ReSurf effect by narrowing the distance between the back-barrier and the heterojunction and also by using smaller field plate lengths (smaller than the micrometer range).
- A saturation of the breakdown voltage for long device. The vertical breakdown literature hypothesis was nuanced. Indeed, the failure analysis revealed a dielectric breakdown between the second anode field plate corner and the heterojunction adding a potential second explanation to the saturation phenomenon.

To be able to study the electric field in TCAD simulations and perform breakdown voltage optimization, a method was developed to calibrate the buffer trap properties (concentration, energy level and capture cross-section). The proposed methodology initiated during this PhD relies on different measurements summarized below. After adding the obtained traps to the TCAD simulation, the electric field representativity was assessed by comparing the simulations to the relative experimental lateral BV difference between two layouts.

1. Capacitance characteristic temperature dependence study was performed on transistors by means of experimental and TCAD studies. It identified buffer deep acceptor traps within the whole GaN epitaxy except in the last few hundreds of nanometers and their properties (E_T-E_V; σ_{A,h^+}) if employed with shallow donor traps (E_C-E_T = 0.11 eV, $\sigma_{D,e^-} = 1\times10^{-15}$ cm^2):
    - The acceptor traps are related to V_{Ga}-$(O_N)_x$. This hypothesis was proposed by comparing its extracted (TCAD fit) properties (E_T-E_V = 1.1 eV, $\sigma_{A,h^+} = 1\times10^{-13}$ cm^2) with the literature and by bonding their concentration with the oxygen experimental one's ([A] = 1 a.u in the AlGaN buffer layer and [A] = 0.5 a.u in the GaN:C),

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- Acceptor traps' concentration respects the following relation with the shallow compensating donor traps' concentration: $[A] - [D] = 1\times10^{17}$ cm^{-3}.

2. The experimental and TCAD vertical current temperature dependence study revealed that:
   - Two traps are responsible for the vertical leakage: dislocations with a cluster of punctual defects such as gallium vacancy V_{Ga} alone or paired with a nitrogen vacancy V_N (E_T = 0.27 eV) for low voltage and temperature and nitrogen on interstitial sites N_I (E_T = 0.75-0.76 eV) for high voltage and temperature.
   - At the end of the PhD, TCAD modeling is limited by its AlN/Si interface to reproduce the experimental behavior.

3. DLTFS performed on samples having different Schottky contact etching recipes revealed new etching-related traps (E_C-E_T = 0.47-0.48 or 0.57 eV) and other donor traps in the 0.40 to 0.56 eV range. The latter may be related to deep acceptor traps' compensation or to the vertical leakage in the deep buffer layers or substrate that would explain the experimental breakdown voltage dependency. Nevertheless, this could not have been pushed further during the PhD.

However, all these studies were not sufficient to reproduce the experimental breakdown voltage variations (lateral limitation) in TCAD simulation especially because the leakages in the buffer are not yet taken into account.

In parallel to these studies, the fully-recessed MOS-HEMT layout and process parameters' impact on the hard switching losses was studied for the first time. This was performed experimentally with LTSpice and TCAD simulations for in-depth analysis. Indeed, when the transistor is scaled down, the layout as well as the process, have to be adapted. Thus, their impacts on losses which will influence the power converter efficiency are relevant to study:

- The study of the recess depth revealed that the deeper the recess, the larger the switching losses especially during turn-on. The significant impact of the threshold voltage (shown to be caused by the distance of the gate bottom with the buffer traps in TCAD simulations) and the C_{GD}(C_{RSS}) plateau at high voltage (influence of the recess depth on the effective gate area) on the switching losses was highlighted.

- The layout dependence study performed on scaled transistors revealed that switching losses slightly decrease with smaller gate length layouts probably due to the V_{TH} decrease (roll-off). However, reducing this parameter makes the gate voltage oscillate which can be problematic (in terms of driving stability) if pushed too far.

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Limitations of the presented studies and perspectives

1. Concerning the electric field management study, the main limitations concern TCAD modeling improvement:
    - As a rule, the main limitation was that no device was laterally limited with the substrate connected to the anode. This introduced complexity in the study because the substrate potential becomes unknown.
      → Having laterally limited device should be considered for the future.
    - When the substrate is floating, the understanding was not sufficient to take into account vertical leakage in TCAD.
      → Further studies based on epitaxial growth parameter variations (especially for the nucleation layer) are proposed to bring further information.

2. Concerning the hard switching losses study, several limitations were identified:

- For the 30 A transistors study:

    - The gate control was not optimized (single external resistance instead of two different gate resistors). Thus the absolute performance of the transistor could not have been assessed during the PhD (note: only the relative difference was studied),
    - The bench could not switch at 400 V/8 A and higher current without unwanted huge oscillations. This may be due to parasitics ElectroMagnetic Coupling (EMC). However, this issue became known at the end of the PhD, when wire bondings of the package devices were adapted to match the DFN pinout of GaN Systems^{TM} transistors.
      → Further investigations should be performed (on Keysight^{TM} ADS®) comparing the parasitics induced by the studied circuit configuration (imposed by the DFN pinout of GaN Systems^{TM} device) with respect to a circuit in which the gate is on the other side of the DFN pinout.

- For the 1 A transistors study:

    - Potential gate to source ESD on 1 A occurred during drivers' power supply turn-on
      → Consider ESD protection in the input drivers' power supply.
    - The packaging step limited the number of available devices probably due to electrostatic discharge between the drain and the deported source field plates (probably due to peak effect).
      → In-depth study of the dicing step (during packaging) needs to be performed to improve its yield.
    - Unexpected behavior was discovered: on-state driving voltage could not be reached for several layouts and investigations did not succeed so far.
      → Relevant topic to tackle for future studies (test cross-coupling hypothesis with mixed-mode TCAD and LTSpice simulation).

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Annexe A: Time Dependent Dielectric Breakdown: From the Physical Origin to the Electrical Analysis

A.1 Physics of Time Dependent Dielectric Breakdowns

Dielectric electrical breakdown is a well-known phenomenon in Complementary Metal Oxide Semiconductor (CMOS) technology [434]. Indeed, gate reliability has been a hot research topic for years. The dielectric breakdown of an initial defect-free (intrinsic) dielectric is a three-step mechanism modeled with the percolation path theory as proposed by the IMEC study of Degraeve *et al.* [435] as illustrated in **Figure 147**:

1. Random generation and/or propagation of defects in the oxide due to the temperature (left of **Figure 147**).
2. Conductive path creation in the oxide and local increase of the temperature due to the non-elastic transport (middle of **Figure 147**)

   Note the formation of a conductive path is also called a "soft breakdown" since there is a steep current increase as shown in the study of Hu *et al.* [154]
3. Positive retroaction: Generation of traps assisted by the current flow and the temperature increase near the conduction path that increases the current leading to the breakdown (right of **Figure 147**)

Consequently, it is a time-dependent mechanism accelerated with temperature and applied electrical bias. Thus, the expression Time Dependent Dielectric Breakdown (TDDB) is commonly used. To study its lifetime, constant voltage or current stress are usually performed as presented in Martin's review [436].

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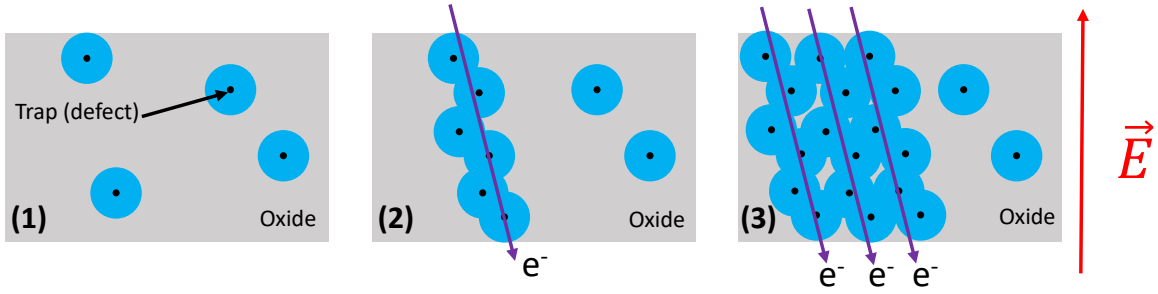

Figure 147: Steps involved in percolation path creation theory schematized steps (adapted from [435]).

A.2 Weibull Statistics to Study the Time Dependent Dielectric Breakdown

The distribution used to study the occurrence probability of the dielectric breakdown within the isolated gate or passivation is the Weibull distribution ([154], [247], [437]–[440] for AlGaN/GaN devices). The cumulative function has the following expression:

$$F(t) = 1 - e^{-\left(\frac{t}{\tau}\right)^{\beta}}$$

Equation 20: Weibull cumulative function.

It depends on the scale factor τ (equivalent to a characteristic time) representing the time for which 63% of the devices have failed as illustrated in **Figure 148(a)**. The β parameter is the shape or distortion parameter. To understand, the impact of this last parameter on the device lifetime, the failure rate can be used. It is expressed with the following expression [441]:

$$\lambda(t) = \left(\frac{\beta}{\tau}\right) \times \left(\frac{t}{\tau}\right)^{\beta-1}$$

Equation 21: Failure rate expression.

Indeed, as it can be seen in **Figure 148(b)**, for β<1, the devices fail in a very short time leading to an infant failure. Whereas a β>1 would lead to a wear-out failure. With the addition of some infant failure mechanisms and some wear-out mechanisms (that should have a different scale factor in a real system), one might recognize the well-known bath curve of a product lifetime [442], [443]. Furthermore, this parameter helps to identify which element is at the origin of the

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breakdown. In fact, it allows to differentiate the “extrinsic failure” (having a low β) from the “intrinsic failure” (having a high β) [444]. The intrinsic failure as it has a sharp distribution in time (observable in **Figure 148(a)**) would correspond to the ideal failure of the dielectric as described at the beginning of the section and observable in the study of Warnock *et al.* [440]. Whereas the extrinsic one has a broad distribution in time (observable in **Figure 148(a)**), which would correspond to a breakdown assisted by already present traps, impurities and structural non-homogeneity as demonstrated in [154], [437].

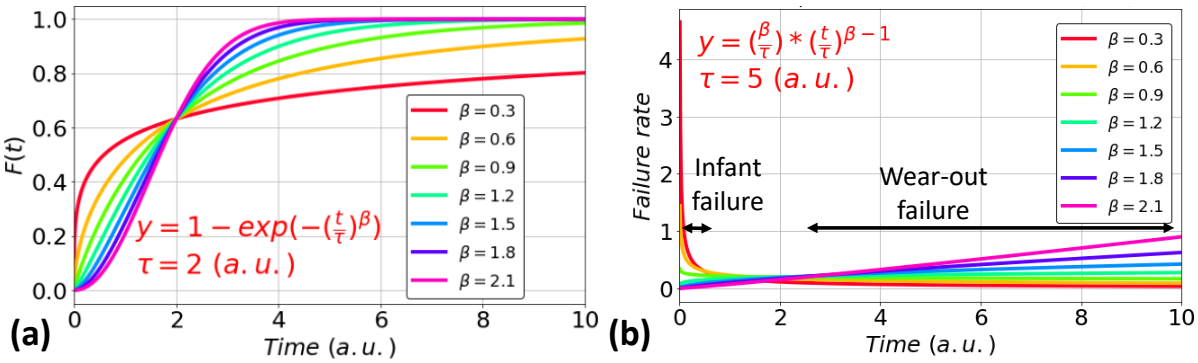

Figure 148: (a) Weibull cumulative function for different β parameters (b) Failure rate for different β parameters.

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Annexe B:
Electrical and Physical Failure Analysis Techniques

B.1 Lock-in Thermography (LiT) [249], [445]

Lock-in Thermography (LiT) is an imaging method sensitive to infrared radiation emission due to the local heat dissipation in a sample from the Joule effect. A non-uniformity in the current density can lead to a local temperature increase that can be identified by the system. The system can be therefore used to identify the location of device failure that can originate from its intrinsic properties or extrinsic defects. Thus, it is a powerful technique used in reliability and failure analysis teams. This is the result of the sum of two different tools:

- The thermography or Thermal Infrared Microscopy (TIM) part: an infrared camera that is sensitive to temperature variation at the surface of the sample. It should not be confused with Light Emission Microscopy (LEM) that is sensitive to the semiconductor light emission through field-accelerated carriers or radiative recombination of electron-hole pairs.

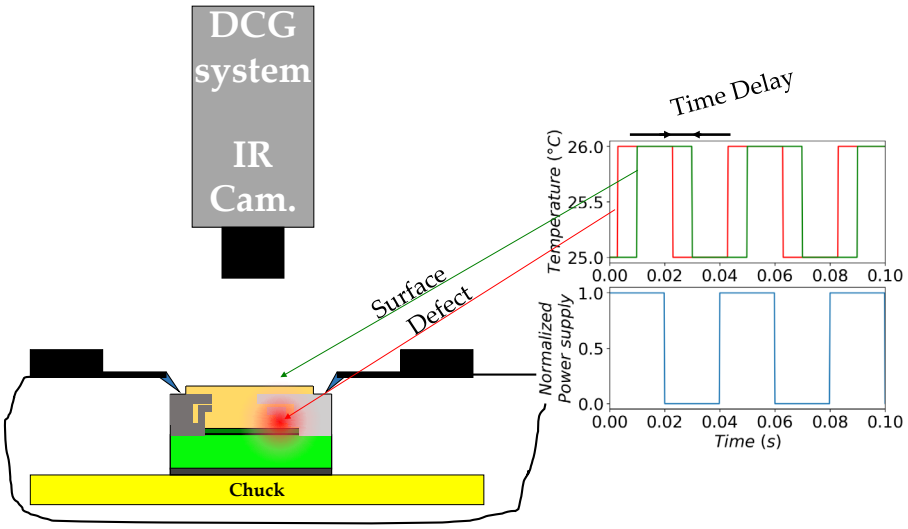

Figure 149: Schematic of the LiT setup at the macroscopic scale stressing the device at a frequency of 25 Hz.

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- The lock-in part: This technique allows reducing the noise contribution in an alternating signal (signal-to-noise ratio improved about more than an order of magnitude). In our case, the alternative signal is the surface temperature sensed by the thermal camera. Indeed as illustrated in **Figure 149**, when the device is biased with an alternating signal, that has a given frequency usually called the lock-in frequency (25 Hz in the figure), there is a local oscillation of the temperature inside the defective device (represented in red). This temperature oscillation will diffuse up to the surface with a certain time delay (represented in green). In the meantime, as shown in **Figure 150**, the camera is recording pictures at a frame rate: f_r higher than the lock-in frequency (from hundreds of Hz to some tens of kHz). The recorded pictures are then processed following the procedure described in **Figure 150**. It begins with the creation of two stack pictures respectively composed of pixels called S^{0° and S^{-90°. The pixels at a given time "z", are the product between the recorded pixel and a sinusoidal factor "A" (cosinusoidal factor "B" respectively) at a given time plus the resulting pixel S^{0° or S^{-90° from the previous picture acquisition. Thus, it is an iterative modified pixel stack from the beginning of the acquisition. The displayed amplitude and phase picture are composed of pixels resulting from the square root of the sum between S^{0° and S^{-90° at the power (the arctangent of the S^{-90° pixel over S^{0° respectively).

  From the amplitude picture, the in-plane special location of the hot spot can be determined. The phase can give information on the depth of the hot spot since it depends on the time delay required for the temperature to diffuse to the surface.

  However, excellent knowledge on the material thermal diffusion properties has to be known to extract this information. Furthermore, this system has some biasing limit ($|V| \leq 40V$). Furthermore, it has some requirement to get a good picture: 100 µW for a small spot; 1 mW for a widespread damage with our test setup.

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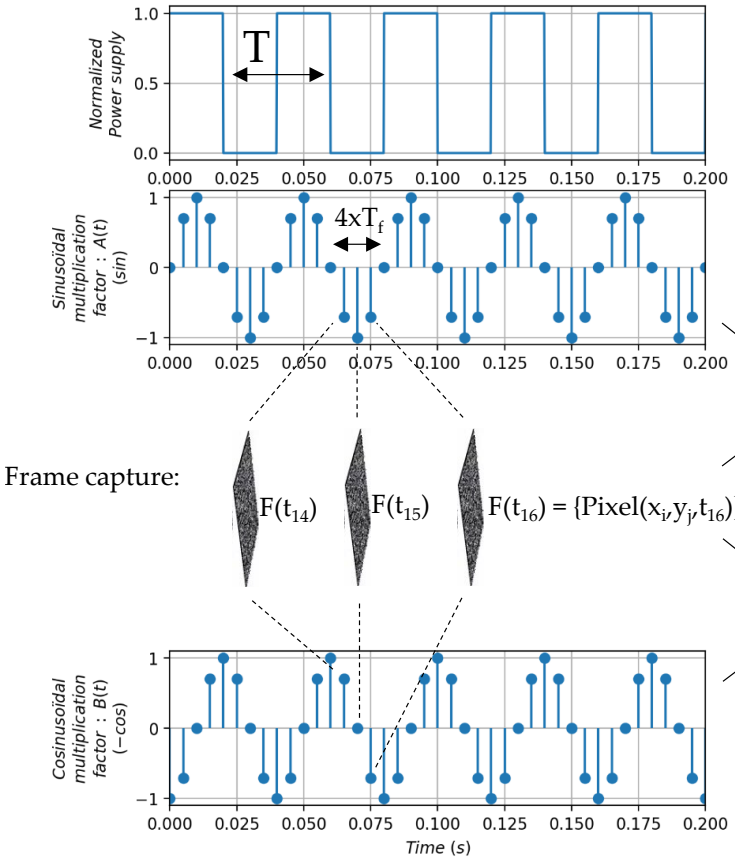


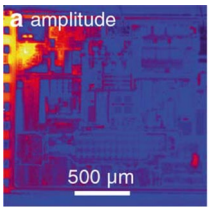
Caption :
f = 1/T : stressing frequency
$f_f = 1/T_f$: frame rate
→ $f<f_f$

$$S^{0^\circ}(x_i,y_j,t_z) = \sum_{l=0}^{z} Pixel(x_i,y_j,t_l) \times A(t_l)$$

$$S^{-90^\circ}(x_i,y_j,t_z) = \sum_{l=0}^{z} Pixel(x_i,y_j,t_l) \times B(t_l)$$

$$Amplitude(t_z) = \left\{ \sqrt[2]{S^{0^\circ}(x_i,y_j,t_z)^2 + S^{-90^\circ}(x_i,y_j,t_z)^2} \right\}_{x_i,y_j}$$

→ **Image of located dissipated power**



$$Phase(t_z) = \left\{ \arctan\left(\frac{S^{-90^\circ}(x_i,y_j,t_z)}{S^{0^\circ}(x_i,y_j,t_z)} \right) \right\}_{x_i,y_j}$$

→ **Image of the time delay**

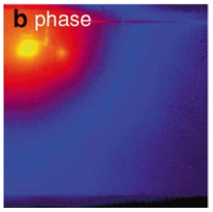


Figure 150: Lock-in correlation procedure at a lock-in frequency of 25 Hz and a frame rate of 200 Hz (amplitude and phase picture from [445]).

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B.2 Focused Ion Beam Scanning Electron Microscopy (FIB-SEM)

This characterization tool is used to observe the device cross-section with a final picture resolution below the 100 nm range. In our case, it is used to observe the damages caused by the breakdown. To achieve that, the probing station has two charged beams created by the two columns visible in **Figure 151(a)** and **(b)**. The Focused Ion Beam (FIB) is used to mil the surface in order to observe the cross-section as illustrated in **Figure 151(b)**. To do so, an inclined plan is first created until a given depth to let the electron beam from the Scanning Electron Microscopy (SEM) column (54° inclined with respect to the FIB column) impinging the whole cross-section to get a clear observation once the final depth is reached. Then, the FIB column moves at this given depth toward the defect until it is visible on the screen as illustrated in **Figure 151(b)**.

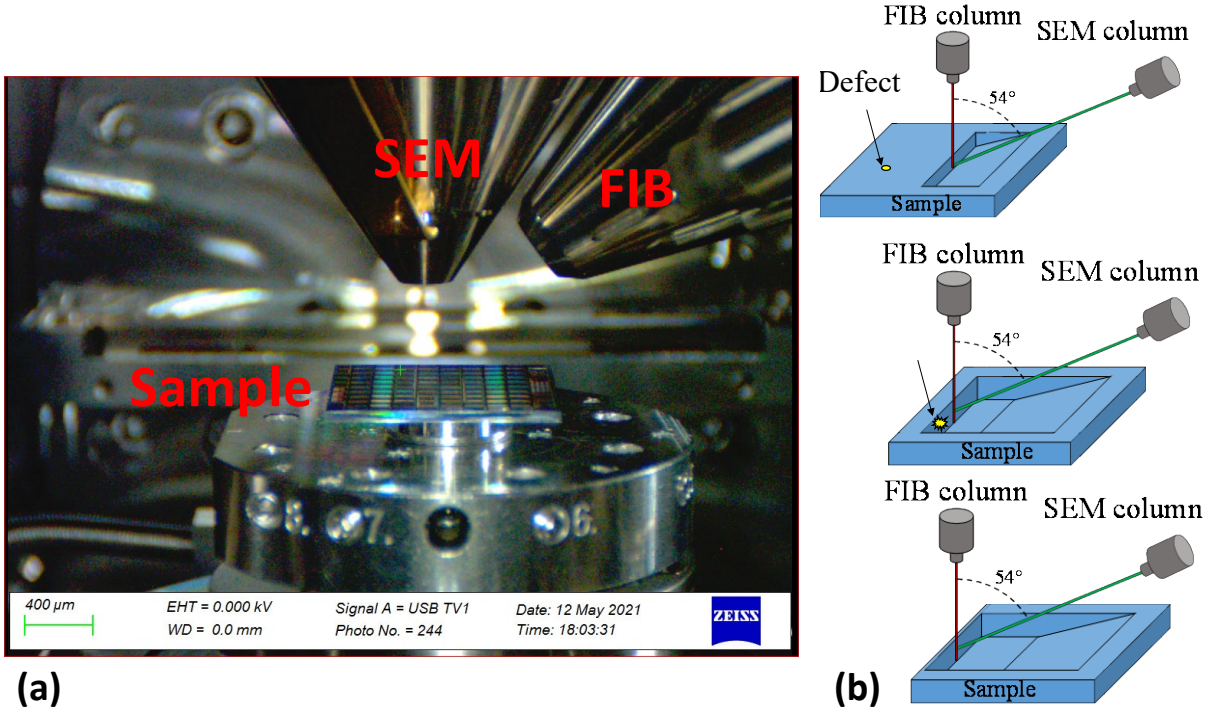

Figure 151: (a) Sample inside the FIB-SEM apparatus (b) Schematic FIB-SEM functioning.

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Several electron sensors having their specificities are placed within the FIB-SEM apparatus, here are those present in the used apparatus:

- In the SEM column:
  - Secondary Electron Secondary Ion (SESI) sensor: It was the most used detector used in this study. It has a reasonable topographic resolution and it is not that much disturbed by the charging in dielectrics.
- In the FIB column:
  - InLens (Secondary electron detection too) sensor: It has the best topographic resolution but it is sensitive to the charging in dielectrics.
  - Energy Selective Backscattered (ESB) sensor: It has the worst topographic resolution. However, it is very sensitive to the atomic number making it very useful to identify matter migration.

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Annexe C: Perimeter Versus Surface Contribution in the Vertical Leakage Temperature Dependence Through an AlGaN-on-Si Epitaxy

C.1 Normalisation Trials Varying Contact Diameters

By normalizing the vertical current flowing through the epitaxy (illustrated in **Figure 152(a)** and described in III.3.b.i.1st) by the top electrode surface having different diameter: D_{OHM} (ranging from 113 µm to 357 µm) at 150°C, the perimeter contribution can be enhanced. Indeed the following equation describes the surface ($J_{surface}$) versus the perimeter contribution ($P_{contact}/S.J_{peri}$) in the current normalized by the contact area:

$$I_{TOT}/S = J_{surface} + {}^{P_{contact}}/_{S} \times J_{Peri}$$

Equation 22: Current normalized by the electrode area expression (I_{TOT}: total current; S: electrode area; $J_{surface}$: Surface current density; $P_{contact}$: contact perimeter; $J_{perimeter}$: Perimeter current linear contribution).

By varying the electrodes' size, the $P_{contact}/S$ ratio changes. Thus, if the perimeter contribution is significantly high, the normalized curve between two different electrode sizes will not match. This is especially the case for the studied epitaxy below 500 V as it can be observed in **Figure 152(b)**. Thus below this bias the quantity I_{TOT}/S cannot be ascribed as a sum of different current densities corresponding to different transport mechanisms (because the surface for both mechanisms can be different. This is why in the manuscript, the vertical current is not normalized.

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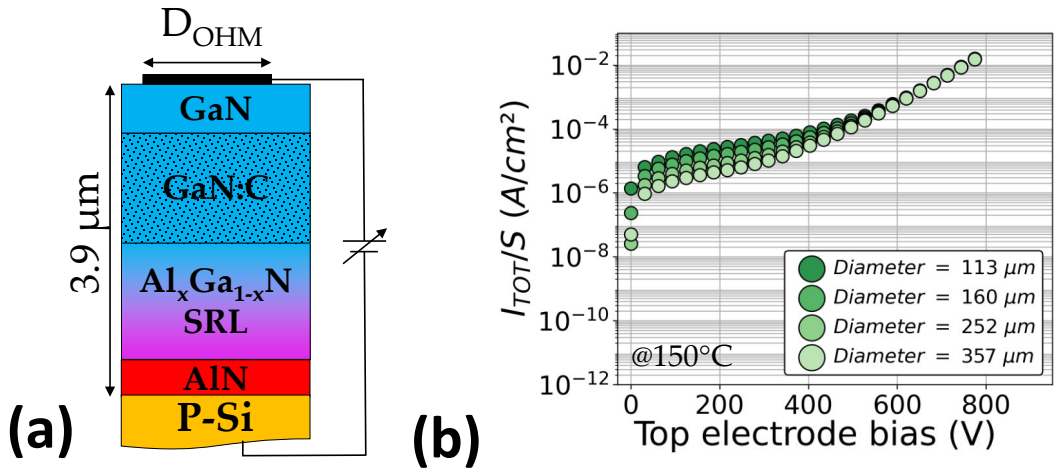

Figure 152: (a) Schematic cross-section of the biased epitaxy (b) Vertical current measurement normalized by the top electrode surface area at 150°C performed on top contact electrodes having different diameters.

C.2 Verification that the Perimeter Contribution in the Ohmic Regime Follows the Same Temperature Dependence than the Analytical Fit

In the first part of the annexe, it was shown that the vertical leakage cannot be normalized by the top electrode area below 500 V. Moreover, below this bias, two different transport mechanisms were shown to be responsible for the vertical current dependence: ohmic and recombination-limited. The purpose of this study is to verify if the extracted trap energy level corresponding to the activation of the transport mechanisms are the same as the temperature dependence of the peripheral contribution (in the temperature range in which the transport mechanism prevails). The described methodology work for the ohmic model but not for the recombination-limited because the current at low temperature (25°C, 50°C and 75°C) and at rather low bias for small diameter electrode was not sufficiently high to be measured.

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C.2.a Method Description

For each of the measured temperature and at a specific bias, the perimeter and the surface contribution can be extracted by doing a linear regression of the I_{TOT}/S quantity when it is plot as a function of the $P_{contact}/S$ ratio as illustrated in **Figure 153**.

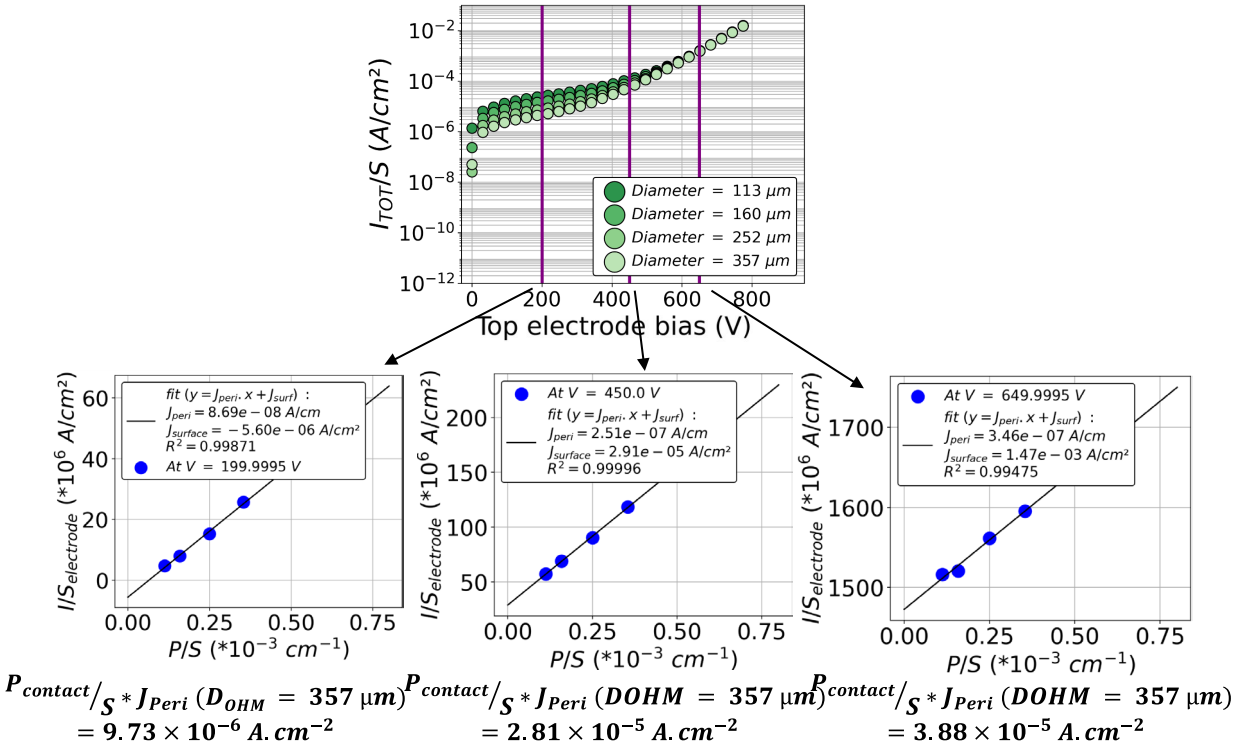

Figure 153: Extraction of the perimeter contribution and the surface contribution at three different biases: 200 V, 450 V and 650 V at a given temperature (150°C here).

After that, by plotting the $P_{contact}/S.J_{peri}$ quantity as a function of the temperature, the activation energy can be extracted by using the same temperature dependence as the analytical model of the transport mechanism.

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C.2.b Results

As for the ohmic case, it contributes at high temperature in between 0 V to 400 V as it was shown in III.3.b.iv. By performing, the methodology described before at high temperature (125°C to 200°C), an activation energy of 0.778 eV can be extracted as shown in **Figure 154**. It is within the 0.76 ± 0.03 eV extracted from the vertical current fit with analytical model confirming that the ohmic contribution is not uniform throughout the epitaxial cross-section and correspond to the low voltage and high temperature part of the entire characteristic.

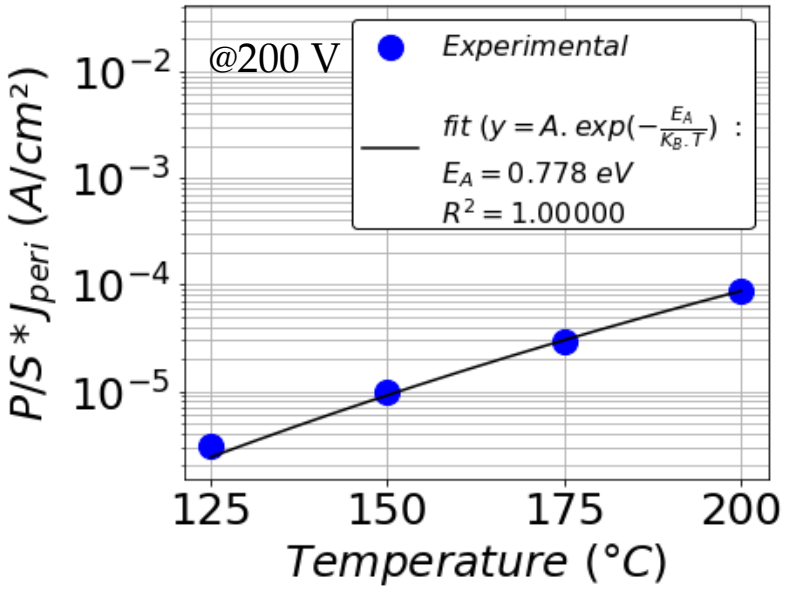

Figure 154: Temperature-dependence of the perimeter contribution at 200 V with its extracted temperature-dependence parameter.

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Annexe D: Mobility Model in the Bulk Material for the Study of the Vertical Current Through the Epitaxy

In this annexe, the different mobility model in the bulk material will be presented as well as their adaptation for GaN, AlGaN, AlN and Silicon material used in this manuscript.

D.1 Presentation of The Different Bulk Mobility Models

This part present the mobility usual model available in Sentaurus® TCAD tool by Synopsys™. This means that this is not an exhaustive list of the entire existing bulk mobility model.

D.1.a Lattice Temperature Dependent Model

The most simple mobility model (constant mobility model in Synopsys™) takes into account the carriers' (electron or holes) interaction with the phonon associated to the thermal vibration of the crystal lattice. It has the following expression for either electrons or holes:

$$\mu_C = \mu_{max} \times \left(\frac{T}{T_0}\right)^{\alpha}$$

Equation 23: Constant mobility model expression (μ_{max}[10]: Mobility at 300 K; T: Lattice temperature; T_0: Reference temperature (300 K in most cases)) [446].

[10] The name maximum has a meaning when this model is used in the Masetti's model described in the next page because it corresponds to mobility for which there are not a lot of doping impurities. Thus when the mobility as a function of the doping concentration is maximized.

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D.1.b Lattice Temperature and Ionized Doping Impurities Dependent Model

There are three different models taking into account the lattice temperature and the carriers' interaction with the ionized doping impurities: Masetti's model [447], Arora's model [446] and Philips Unified Mobility (PhuMob[11]) model [448], [449]. They have the following expressions:

$$\mu_D = \mu_{min} \times \left(\frac{T}{T_0}\right)^{\beta_1} + \frac{(\mu_{max} - \mu_{min}) \times \left(\frac{T}{T_0}\right)^{\beta_2}}{1 + \left(\frac{N}{N_{REF} \times \left(\frac{T}{T_0}\right)^{\beta_3}}\right)^{\alpha \times \left(\frac{T}{T_0}\right)^{\beta_4}}}$$

Equation 24: Arora's mobility model expression (μ_{min}: minimum expected mobility at 300 K; μ_{min}: Minimum expected mobility at 300 K; T: Lattice temperature; T_0: Reference temperature (300 K in most cases); N: Ionized doping impurity concentration; N_{ref}: Reference doping concentration; α, β_i ($i \in [|1,4|]$) : Fitting coefficient) [446].

$$\mu_D = \mu_{min1} \times e^{\frac{-P_C}{N}} + \frac{\mu_C - \mu_{min2}}{1 + \left(\frac{N}{C_r}\right)^{\alpha}} - \frac{\mu_1}{1 + \left(\frac{C_s}{N}\right)^{\beta}}$$

Equation 25: Masetti's mobility model expression with the Synopsys's formalism (μ_C: Mobility corresponding to the constant mobility model (this is where the temperature dependence is taken into account and where μ_{max} is defined); μ_{min_i} ($i \in \{1,2\}$): Minimum expected mobility at high doping concentration at 300 K; N: Doping concentration; C_s, C_r: Reference doping concentration parameters; μ_1 : Reference mobility parameter; P_C, α, β: Fitting coefficients) [447].

$$\mu_D = \frac{{\mu_{max}}^2}{\mu_{max} - \mu_{min}} \times \left(\frac{N_{ref}}{N_I}\right)^{\alpha_1} + \frac{\mu_{max} \times \mu_{min}}{\mu_{max} - \mu_{min}} \times \left(\frac{c}{N_I}\right)$$

Equation 26: PhuMob mobility model [448], [449] (μ_{min}: Minimum expected mobility at 300 K; μ_{max}: Maximum expected mobility at 300 K; N_I : Ionized doping impurity concentration; N_{ref}: Reference doping concentration; α_1, c: Fitting coefficients).

[11] This model takes also into account impurity scattering and electron/hole scattering

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D.1.c High-Electric Field Dependent Model

There are two different models taking into account the high electric field effect on the mobility. There are the model of Caughey-Thomas [450] and Farahmand [451] with the following expressions:

$$\mu_{HF} = \frac{\mu_{LF}}{\left(1 + \left(\frac{\mu_{LF} \times E}{v_{sat}}\right)^{\beta_0 \times \left(\frac{T}{T_0}\right)^{\beta exp}}\right)^{\frac{1}{\beta_0 \times \left(\frac{T}{T_0}\right)^{\beta exp}}}} \text{, } v_{sat} = A_{vsat} - B_{vsat} \times \left(\frac{T}{T_0}\right)$$

Equation 27: Caughey-Thomas's mobility model expression [450] (μ_{LF}: Low field mobility; β_O, β_{ext}: Reference temperature coefficients at 300 K; T: Lattice temperature; T_0: Reference temperature (300 K in most cases); E: Electric field; v_{sat}: Saturation velocity; A_{vsat}, B_{vsat} : Reference saturation velocity coefficients).

$$\mu_{HF} = \frac{\mu_{LF} + \mu_1 \times \left(\frac{E}{E_0}\right)^{\alpha} + \frac{v_{sat}}{E} \times \left(\frac{E}{E_1}\right)^{\beta}}{1 + \gamma \times \left(\frac{E}{E_0}\right)^{\alpha} + \left(\frac{E}{E_1}\right)^{\beta}}$$

Equation 28: Farahmand's mobility model expression with the Synopsys's formalism (Farahmand's model [451] exact expression that can be seen in the article of De Brida *et al.* [452], Schwierz *et al.* [453] and Sabui *et al.* [454] can be obtained with $\mu_1 = 0$) (μ_{LF}: Low field mobility; μ_1: Reference mobility parameter; E: Electric field; E_0, E_1: Reference electric fields; v_{sat}: Saturation velocity; α, β, γ: Fitting coefficients).

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D.2 Model Choice and Parameters' Determination

For the study of the vertical current, mobility models were chosen and their parameters were adapted to fit the experimental data summarized in the PhD dissertation of Vitanov [455]. The parameters adaptation was assisted and compared with the model proposed by other authors.

D.2.a Model Chosen for GaN bulk

For low-field mobility, Arora's model is the most used [451], [453], [454] in front of Masetti's one [452] as shown in **Figure 155(a)**. As shown in **Figure 155(a)**, the chosen model was the Arora's one and the coefficient for electrons were based on the one proposed by Farahmand *et al.* [451] and adapted to get a lower mobility at high temperature which would correspond to the experimental data exposed in green in **Figure 155(c)**. For holes, the chosen coefficients were chosen independently of the literature to fit the experimental data especially at high temperature. As for the ionized doping impurity concentration dependence, the coefficients chosen were for the electron based on the study of Sabui *et al.* [454] and on Synopsys coefficient [294] for the holes as illustrated in the **Figure 156(a)** and **(c)**.

As for high field dependence, it is common to represent the drift velocity instead of the mobility itself (which is the derivative of the drift velocity with respect to the electric field) for electrons as observed in **Figure 157**. For GaN, only the Farahmand's model (TransFerred Electron Effect (TFEE) model in Synopsys) is used because it allows reproducing the negative differential mobility as it can be seen in **Figure 157(c)** and **(d)** observable in the Monte-Carlos simulations. Nevertheless, this has not been enhanced experimentally (a single point in the experiment of Barker *et al.* is not sufficient), this is why the coefficients have been chosen to match the experimental curve proposed by Wraback *et al.*. For holes, coefficients were chosen to match the available data exposed in **Figure 157(e)**.

The chosen coefficients for low and high-field mobility model used in GaN bulk are summarized in **TABLE 19**.

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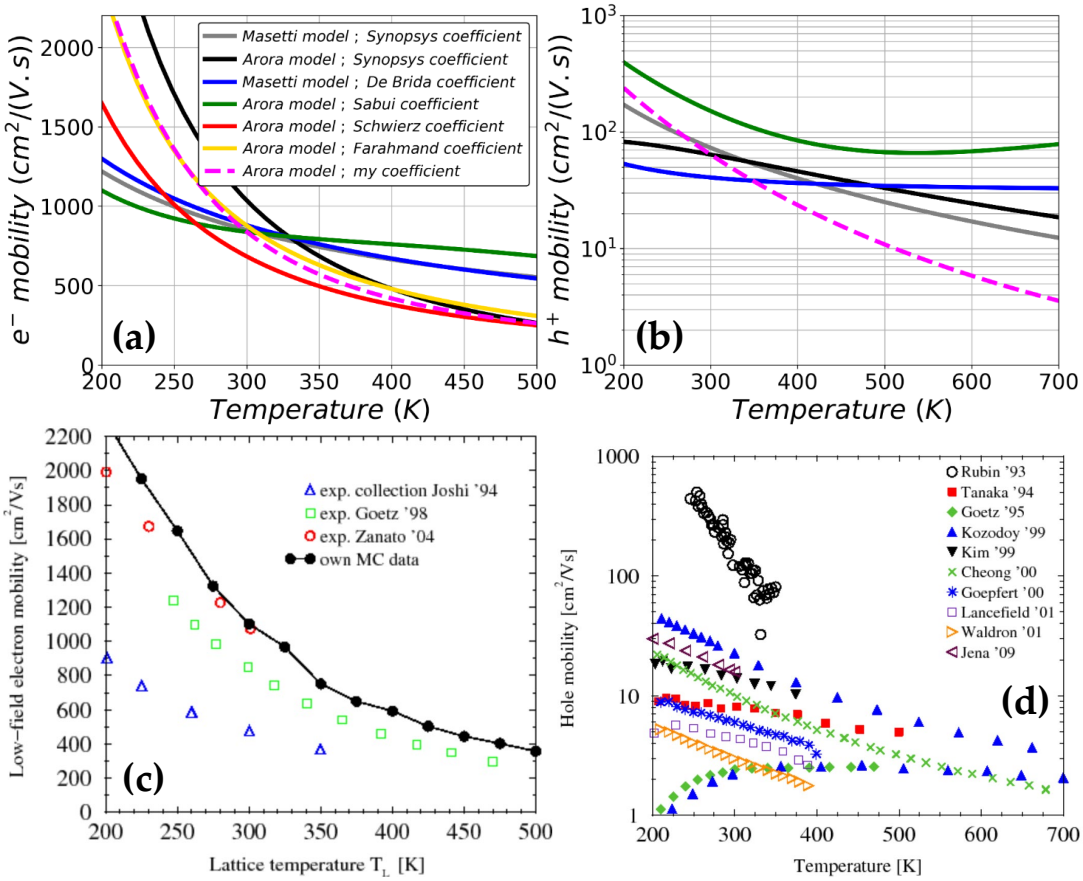

Figure 155: (a) Electron (Synopsys™ coefficients [294]; De Brida *et al.* [452]; Sabui *et al.* [454]; Schwierz *et al.* [453]; Farahmand *et al.* [451]) and (b) Hole model's temperature dependence (displayed for an ionized doping impurity concentration $N = 1\times10^{17}$ cm^{-3}). (c) Electron [455, Sec. 3.2.2 Electron Transport] and (d) Hole [455, Sec. 3.2.3 Hole Transport] experimental reported mobility's temperature dependence.

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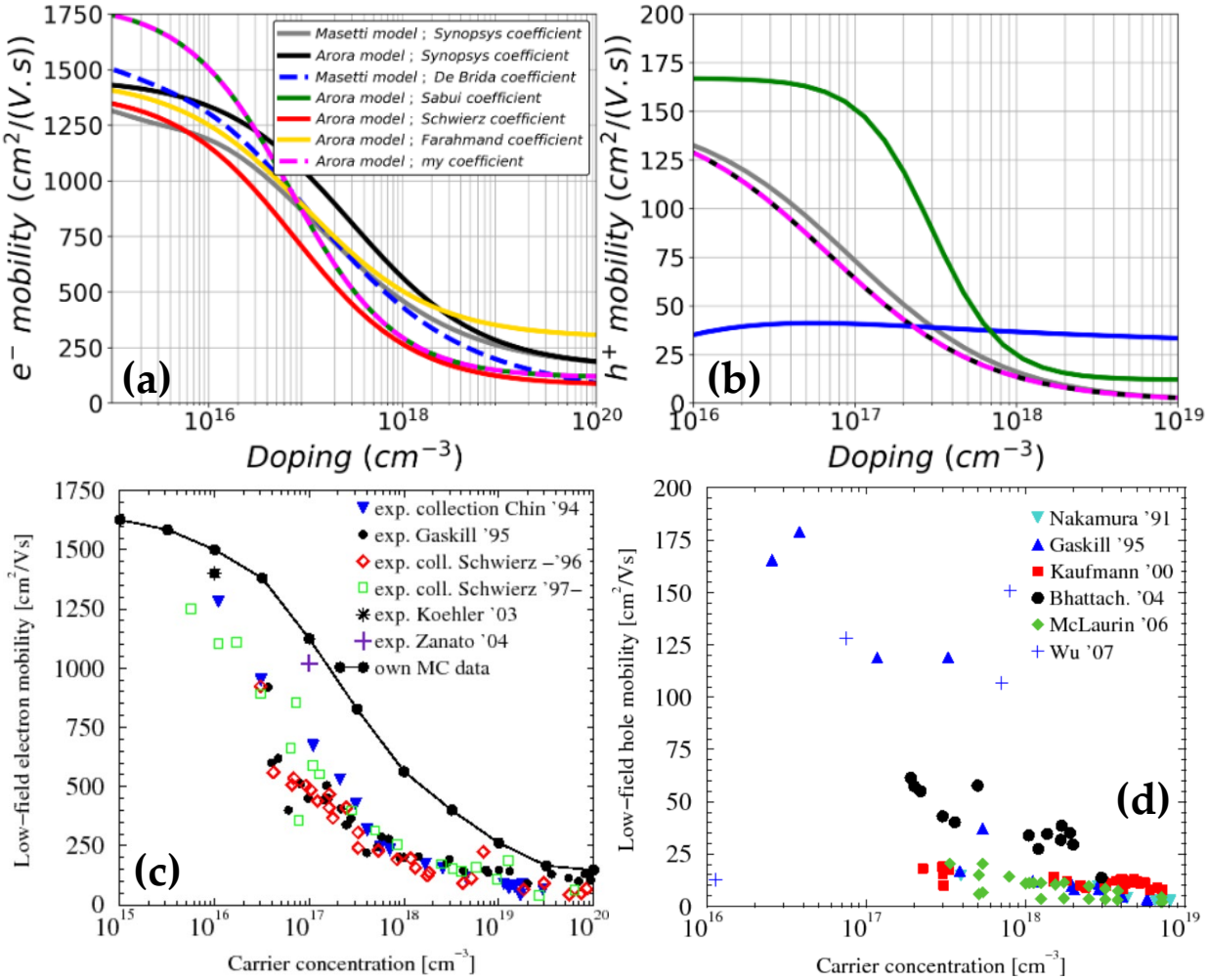

Figure 156: (a) Electron (Synopsys™ coefficients [294]; De Brida *et al.* [452]; Sabui *et al.* [454]; Schwierz *et al.* [453]; Farahmand *et al.* [451]) and (b) Hole model's ionized doping impurity concentration dependence (displayed for T = 300 K). (c) Electron [455, Sec. 3.2.2 Electron Transport] and (d) Hole [455, Sec. 3.2.3 Hole Transport] experimental reported mobility's ionized doping impurity concentration dependence.

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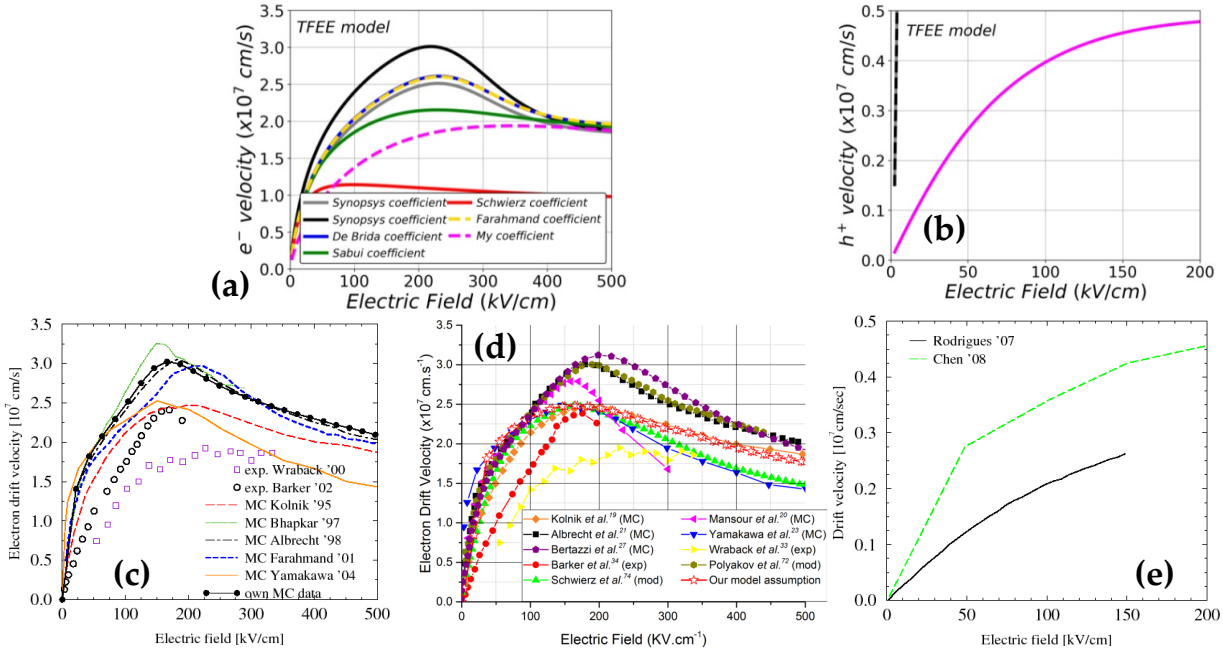

Figure 157: (a) Electron (Synopsys™ coefficients [294]; De Brida *et al.* [452]; Sabui *et al.* [454]; Schwierz *et al.* [453]; Farahmand *et al.* [451]) and (b) Hole model's high electric field dependence (displayed for T = 300 K and an ionized doping impurity concentration N = 1×10^{17} cm^{-3}). Electron (c) [455, Sec. 3.2.2 Electron Transport] (d) [454] and (b) Hole [455, Sec. 3.2.3 Hole Transport] experimental reported mobility's high electric field dependence.

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TABLE 19: Chosen coefficients for the Arora's and Farahmand's model used for GaN.

Model name	Parameter name	Value for electrons	Value for holes
Arora's	μ_{max} (cm²/(V.s))	1800	151
	μ_{min} (cm²/(V.s))	115	1
	α	0.8	0.9
	β_1	-1.5	-0.57
	β_2	-1.5	-2.23
	β_3	-3.02	-2.4
	β_4	-0.81	-0.146
	N_{REF} (cm^{-3})	7×10^{16}	7×10^{16}
Farahmand's	μ_1	0	0
	v_{sat} (cm/s)	0.7×10^{7}	0.5×10^{7}
	E_0 (V/cm)	1.3×10^{5}	1.7×10^{5}
	E_1 (V/cm)	1.3×10^{5}	1.7×10^{5}
	α	0.5	1.5
	β	2.1	5.19
	γ	5.5	1.4

D.2.b Model for the Other Materials

For the AlN and the AlGaN, the authors have not found references (except the temperature dependence in the AlN [12]) to make a good model calibration. Thus the default coefficient for the Arora's and Farahmand's models were used for both materials.

Concerning the silicon, PhuMob model was used with the default coefficients of Synopsys™.

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Annexe E:
Deep Level Transient Fourier Spectroscopy (DLTFS)

Deep Level Transient Spectroscopy (DLTS) is the best-adapted technique for trap identification. Nevertheless, the conventional DLTS has a lower energy resolution and signal-to-noise ratio with respect to the Deep Level Transient Fourier Spectroscopy (DLTFS) [361]. This annexe will be specific to measurements performed on Schottky diode, which are tested in the manuscript.

E.1 Experimental Setup

The experimental system available at Ampere Laboratory: High Energy Resolution Analysis Deep Level Transient Spectroscopy FT-1030 HERA DLTS® by PhysTech® GmbH is composed of four different parts as shown in **Figure 158(a):**

- Vacuum pump: vacuum is required to prevent humidity from freezing the system and for thermally insulating the Helium cooler.
- Liquid Helium cooler and a heating system: temperature control system based on liquid nitrogen to perform measurements in temperature from 50 K to 425 K.
- Measurement system: to perform the capacitance measurement, a Boonton 7200 capacitance meter is used.
- Cryogenic tower: cylindrical-shaped isolated box to maintain a constant temperature inside the volume in which the Device Under Test (DUT) is placed and to be able to change the temperature rather quickly.

The DUT is glued on an alumina substrate. The DUT metal pads are wire-bonded with the one of the substrate as shown in **Figure 158(b)**. The metal pads are electrically connected to the power source thanks to either pressed probing needles (as shown in **Figure 158(b)**) or welded wires.

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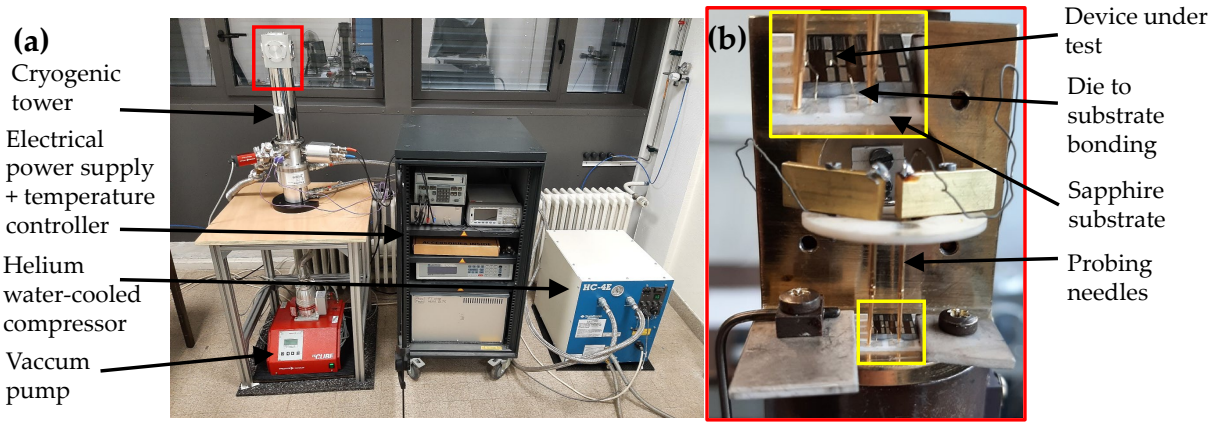

Figure 158: (a) Overall experimental setup (b) Experimental configuration inside the Cryogenic tower with a device in the test position.

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E.2 Different Electrical Measurements

E.2.a Temperature Scans/ Filling Pulse Scans

A single DLTFS measurement performed on a Schottky diode consists of biasing the diode with a reverse voltage V_R and applying a pulse V_P during a controlled time t_P at a constant temperature T as illustrated on the top of **Figure 159(a)**. The diode responds with the capacitance signal illustrated at the bottom of **Figure 159(a)** (constant capacitance after a long time under either V_R or V_P and transient behavior). The transient exponential decay behavior after the filling pulse is analyzed within the time window τ_W. The measurement system being constituted of an Analog to Digital Converter (ADC) records N measurement within the time window τ_W at equidistant time Δt as illustrated in **Figure 159(b)**. The Discrete Fourier coefficients c_n ($n \in [|0, N-1|]$) are then calculated following the expression [361] with a_n and b_n being its real (cosine coefficient) and imaginary part (sine coefficient) that will be used for the different scans' representation:

$$c_n = \frac{1}{2} \times (a_n - i \times b_n) = \frac{1}{N} \times \sum_{k=0}^{N-1} C_{meas}(k \times \Delta t) \times \exp(-i \times 2 \times \pi \times k \times n)$$

Equation 29: Discrete Fourier coefficient expression (N: sampling measurements number; C_{meas}: measured capacitance; Δt: time interval in between measurements; n: discrete Fourier coefficient order).

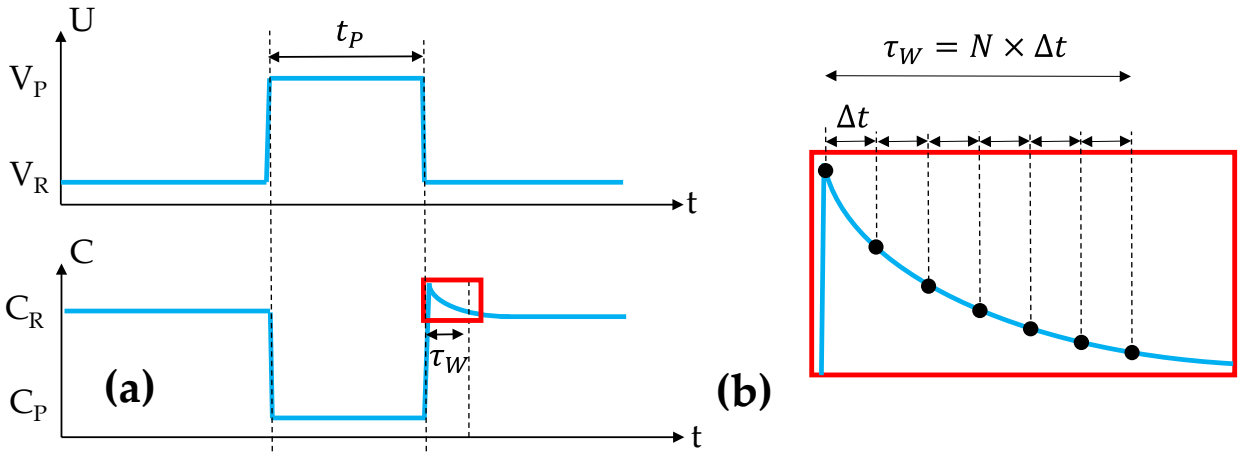

Figure 159: (a) Capacitance DLTS voltage and capacitance signal (b) Transient signal processing after the filling pulse.

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By varying either the temperature or the filling pulse width the temperature scan or the filling pulse scans can be obtained as shown in **Figure 160(a)** and **(b)** respectively. The $a_{1,max}$ coefficient displayed in **Figure 160(b)** corresponds to either a local or a global maximum in the temperature scan **Figure 160(b)** which allows assessing the filling pulse dependence of every detected traps.

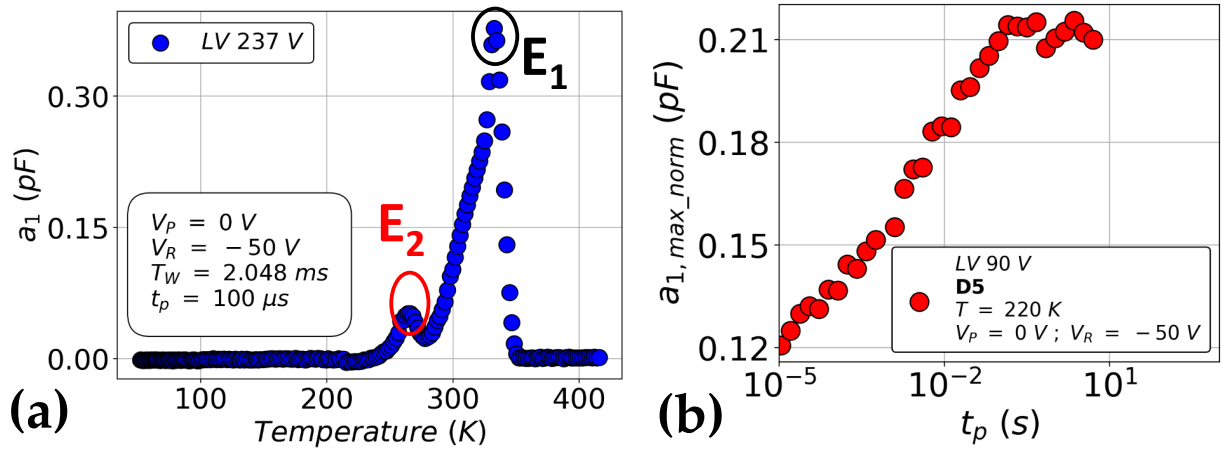

Figure 160: (a) Typical DLTFS temperature scan recorded at V_R = -50 V; V_P = 0.0 V; t_P = 100 µs and T_W = 2.048 ms (b) Typical DLTFS filling pulse width scan recorded at V_R = -50 V; V_P = 0.0 V; T = 220 K.

E.2.b Arrhenius Plot

† **DLTFS**

To extract the energy level E_T and the electron capture cross-section σ_{e^-} of traps. Arrhenius plot can be used using the following expression to extract these parameters:

$$\frac{e_n}{T^2} = \frac{4 \times \sqrt{6} \times \pi^{\frac{3}{2}} \times {m^*}_{e^-} \times {K_B}^2 \times \sigma_{e^-}}{h^3} \exp\left(\frac{-E_T}{K_B \times T}\right)$$

Equation 30: Electron emission rate e_n ($=1/\tau$) expression (T: temperature; K_B: Boltzmann constant, h: Planck constant; ${m^*}_{e^-}$: electron effective mass; σ_{e^-}: electron capture cross-section).

As an example, typical Arrhenius plot is shown in **Figure 161**. The characteristic time is extracted using the following expression for n = 1 [361]:

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$$\tau(a_n, b_n) = \frac{\tau_W}{2 \times \pi \times n} \times \frac{b_n}{a_n}$$

Equation 31: Trap characteristic time expression (τ_W: time window; n: discrete Fourier coefficient order; b_n: sine coefficient; a_n: cosine coefficient).

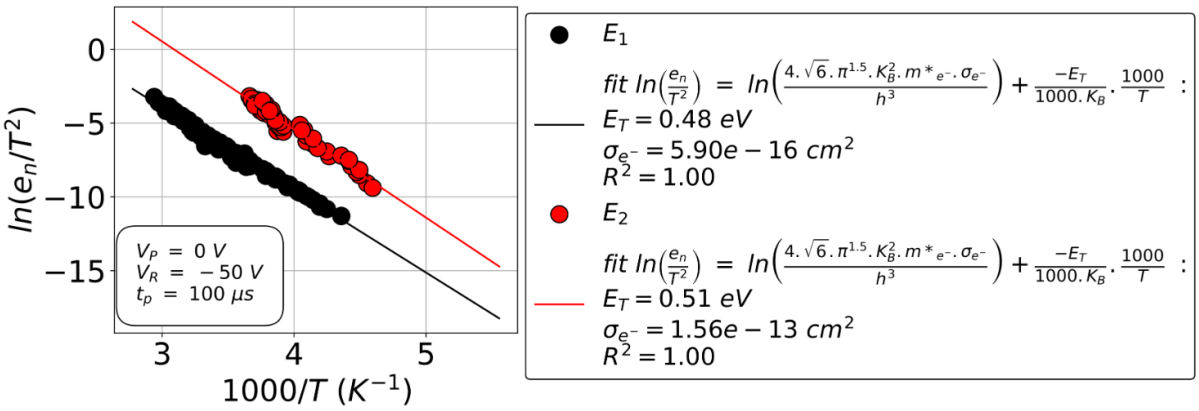

Figure 161: Typical DLTFS Arrhenius plot recorded at V_R = -50 V; V_P = 0 V and t_P = 100 µs.

† Comparison with respect to conventional DLTS

As mentioned earlier, DLTFS has better energy resolution and signal-to-noise ratio with respect to conventional DLTS (in addition to some other automations that save time) [361]. Indeed, instead of sampling the exponential decay with N measurements at each temperature, the conventional DLTS (boxcar technique) measures the capacitance difference at two specific times t_1 and t_2. The corresponding time constant τ is $(t_2-t_1)/\ln(t_2/t_1)$ as shown in **Figure 162**. The temperature for which the capacitance difference is maximum is then associated with τ. Performing the same analysis at different τ (and therefore different couples (t_2,t_1)) allows getting the Arrhenius plot.

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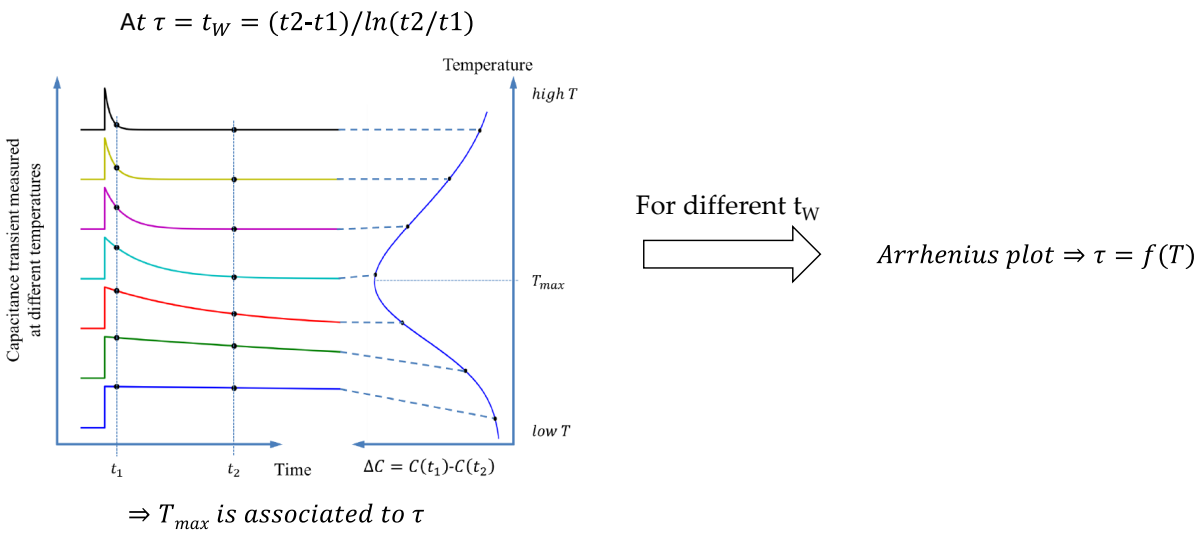

Figure 162: Conventional DLTS method to get the Arrhenius plot (taken and adapted from [360]).

† Comparison with respect to HERA DLTS

This technique was shown to have an energy resolution one order of magnitude bigger than conventional DLTS [456]. Indeed, the use of the Laplace transform allows getting sharper distribution emission coefficient peak with respect to the broad ΔC versus T exposed in **Figure 162**.

The author has not studied a lot this technique but from what he experienced, a comparison with the energy level obtained with DLTFS is advised to ensure the consistency of the results.

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Annexe F:
Double Source Test Complementary Information

Double Source Test (DST) was the circuit allowing to make transistor hard switching tests. This annexe will first present in detail the electrical circuit, its working principle and the justification of the probes choice. After that, the modeling of the circuit elements for the LTSpice simulations will be introduced. In a third part, the way propagation time was compensated will be presented. And finally, the technology comparison between fully-recessed MOS-HEMT built at CEA LETI with the p-GaN gate HEMT of GaN Systems^{TM} will be analyzed.

F.1 Electrical Circuit

F.1.a Circuit Presentation and Elements

The Double Source Test (DST) is composed of two distinct power sources, one for the voltage and the other for the current. In addition of not presenting any blocking stress before hard switching events, this is more convenient for hard-switching tests since it prevents huge experimental setup as it can be seen in the article of Weimer *et al.* [203, Fig. 1]. Indeed, this huge double pulse experimental setup (with many inductive loads) is necessary for working at a constant on-state time before hard-switching events while changing the on-state current value.

Both power sources (voltage source in purple and current source in cyan in **Figure 163**) are directly connected to the middle point: point in between the Schottky diode and the DUT drain electrode. Here are more details on the fabricated experimental bench:

- The Schottky diode: it was chosen to match the current rating of the transistor and it was a SiC diode to not limit the switching speed (negligible Q_{RR} and lower C_{OSS} with respect to Si diode). Thus, the 1200 V /33 A C4D10120E [457] was chosen for 30 A transistor and the 650 V/4 A Rohm SCS302AP [458] for 1 A transistors. Two things can be noticed. Firstly, the C4D10120E has a 1200 V rating for safety margin purpose because during the tests, a 650 V died for undetermined reason. Secondly, SiC Schottky diode does not exist below 2 A which probably limit the turn-off hard switching speed.

- The voltage source is composed of a voltage power supply (TDK lambda 3.3 kW). Two capacitors are added in parallel to ensure the voltage stability during the whole DST

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procedure with the polypropylene capacitors and during the hard switching event with the ceramic one. The resistor R_1 is there to discharge capacitors when the power supply is switched off.

- The current source is composed of a power supply in series with a 1 Ω resistor (R_3). In parallel of this, a polypropylene capacitor (to stabilize voltage) with a resistor R_2 (to discharge capacitor). The cumul of two power switches enables to get an on-demand pulsed current source. Indeed K_1 can block or not the previously described circuit whereas K can close the circuit to not supply the inductance while keeping the power supply on. To stabilize the current source a large inductance is placed in between the middle point and the previously described circuit. The current transport is carried on through twisted pairs that have a larger bandwidth with respect to simple parallel wires.

- The current shunt position is changed in between the circuit for 30 A transistors and for 1 A. On the one hand, for 30 A transistors, the mass is placed at the source (**Figure 163(a)**) because it reduces the gate oscillation amplitude. On the other hand, it was observed with 1 A transistor in the circuit illustrated in **Figure 163(a)** that the measured current value is very different from the expected one probably due to a large current flowing through the mass (not shown here). This is why the shunt has been connected in series with the transistors as illustrated in **Figure 163(b)**.

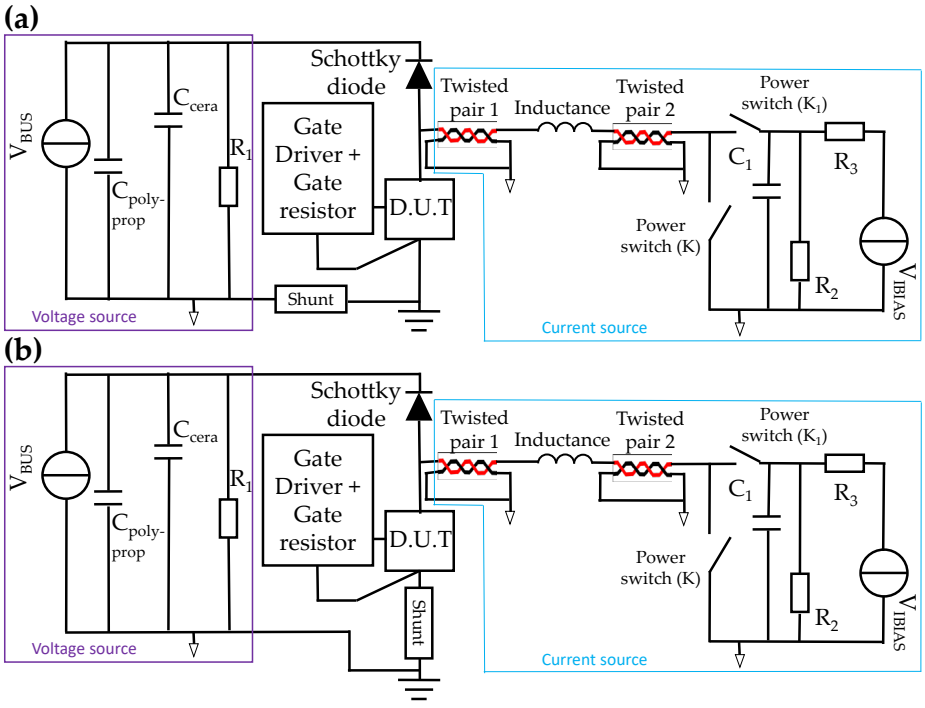

Figure 163: Schematized implementation of the Double Source Test (a) for 30 A transistors (b) for 1 A transistors.

The real implementation of this circuit is shown in **Figure 164**.

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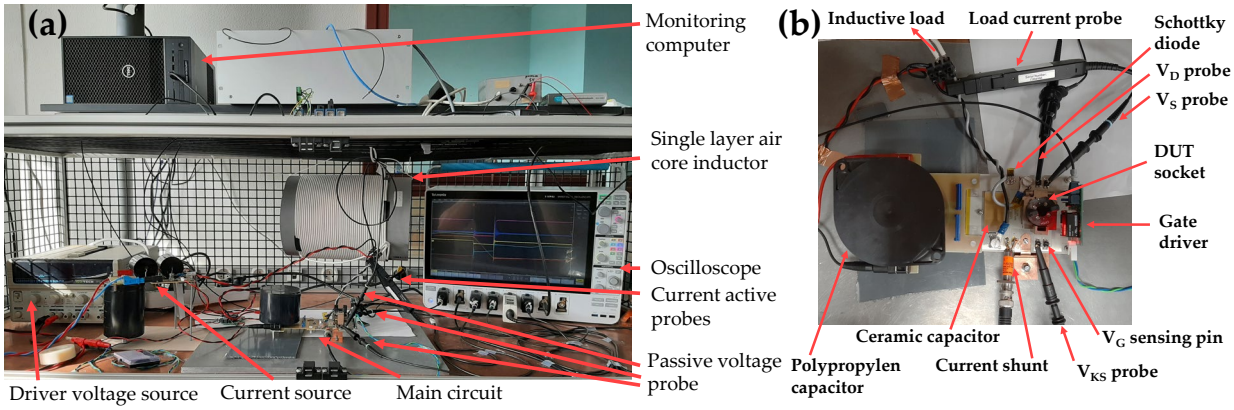

Figure 164: Real implementation of the Double Source Test circuit (a) Overall experimental bench setup (b) Zoom on the main boards.

F.1.b Circuit Functioning and Typical Waveforms

The Double Source Test enables a single switching event or multiple switching events. In this part, only the single switching mode will be described.

The sequence is controlled by three switches namely K1, K and the Device Under Test (DUT). The controlling gate-to-source waveforms are illustrated in **Figure 165(a)** with the corresponding main waveforms in **Figure 165(b)**. In the middle of both figures, two vertical lines are placed at the time for which the DUT undergoes the studied hard turn-on/off switching events (where E_{ON} and E_{OFF} are extracted).

Now, let us move on to the specific description of each sequence step considering only steps for which the power switch K1 is turned on:

- Step 2 (illustrated in **Figure 166(a)**): Power switch K1 has been turned on meaning that the current flows only in the current source loop since the power switch K is already on.
- Step 3 and 7 (illustrated in **Figure 166(b)**): The DUT is on meaning that the current flows in the DUT as well as in the power switch K. In step 3, the current through the DUT is limited by the inductance charge. Whereas in step 7, the inductance slows down the current balance between both branches
- Step 4 and 6 (illustrated in **Figure 166(c)**): The current charges the inductance while the DUT is turned-on. It might be noticed that step 4 and 6 timing are different to prevent the current from being higher than DUT current rating. Thus the on-state timing in the manuscript corresponds to $t_{ON,1}$ in the figure.

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- Step 5 (illustrated in **Figure 166(d)**): The DUT is hard switched off which forces the current to flow through the Schottky diode letting the DUT undergo high voltage before being hard turned on.
- Step 8 (illustrated in **Figure 166(e)**): It differs from step 2 because the inductance is still charged at the step beginning. Therefore, the inductance current is discharged through the Schottky diode.

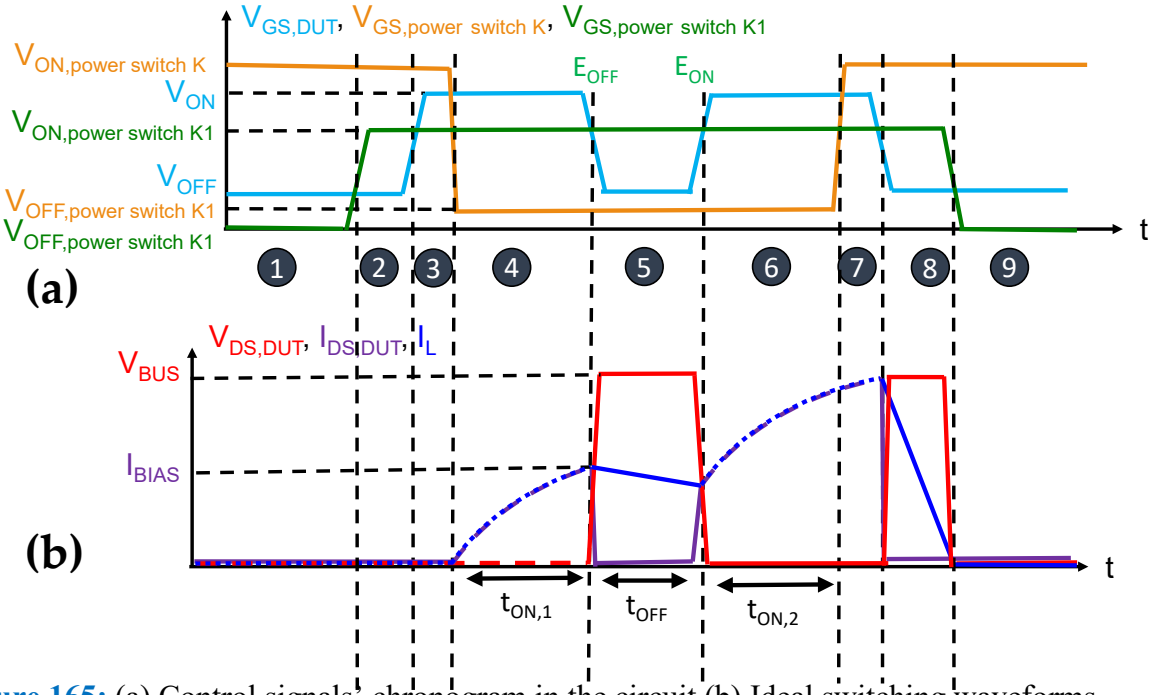

Figure 165: (a) Control signals' chronogram in the circuit (b) Ideal switching waveforms.

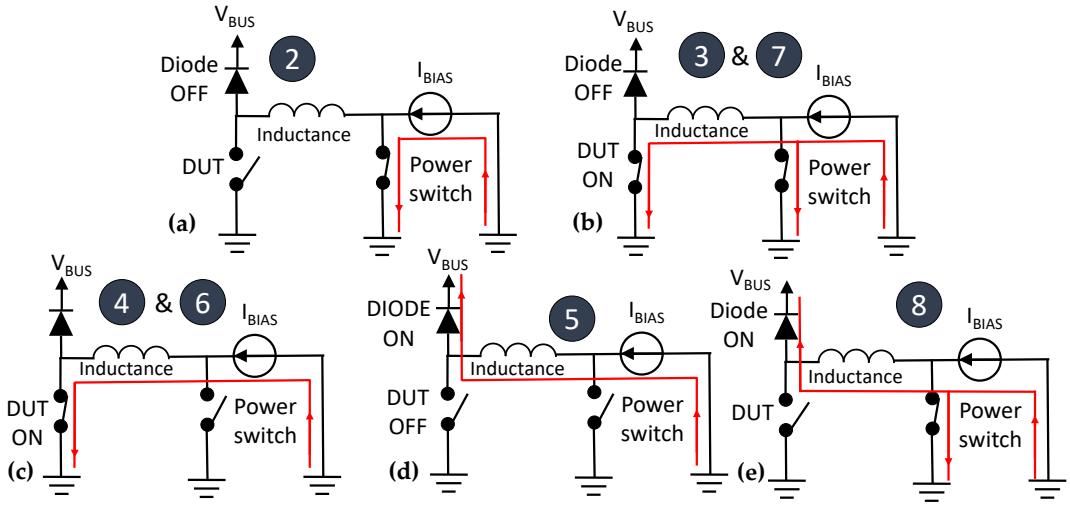

Figure 166: Equivalent circuit of the different phases: (a) phase 2 (b) phase 3 and 7 (c) phase 4 et 6 (d) phase 5 (e) phase 8.

XXX

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F.1.c The Probes Choice Justification

† Current probes

In this manuscript, the coaxial shunt SDN-414-10 [426] from T&M research™ was used but this is neither the only product in its category nor the only category as shown in **TABLE 20**. Indeed, several techniques exist. However, to this day, as it can be seen, the only existing ones having a high bandwidth are either the coaxial shunt or the current shunt resistor. In this PhD, both were tried. Nevertheless, the current shunt resistor implementation was not optimized (due to the lack of time). This might explain why higher current oscillation amplitude was observed. Thus, for the future, comparing optimized circuit with both techniques could be a good study for a possible optimization of the bench. Indeed, the current shunt resistor may reduce the added parasitic inductance in the power loop.

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TABLE 20: Current measurement techniques.

Instruments	Advantages	Drawbacks
Current transformer	Galvanic isolation [459]	- Large size and low bandwidth [459] - Additional inductance in the power loop [459]
Current probe Example: TCP0030A	Galvanic isolation [459]	- Large size and low bandwidth [459] - Additional inductance in the power loop [459]
Rogowski-coil Example: Pearson 2877 (Bandwidth = 200 MHz; t_r = 8.75 ns) or the CWT mini (Bandwidth = 17 MHz; t_r = 103 ns)	Galvanic isolation [459]	- Large size and low bandwidth [459] - Additional inductance in the power loop [459]
Coaxial shunt Example: SDN-414-10 (Bandwidth = 2 GHz; t_r = 0.18 ns used in [67], [195], [412], [424]) SDN-414-025 (Bandwidth = 1.2 GHz; t_r = 0.3 ns used in [460]) W-1-01C-1FC (Bandwidth = 800 MHz; t_r = 0.45 ns used in [410])	- High bandwith [459] - Smaller size (than current transformer and current probes) [459]	Non-galvanic isolation [459]
Current shunt resistor Ex : Flat SMD resistor used in [459]	- High bandwidth [459], [461] - Low parasitic inductance [459], [461] - Small foot print [459]	Non-galvanic isolation [459]

† Voltage probes

Two kinds of voltage probes exist as shown in **TABLE 21**: differential and passive probes. Only voltage passive probes propose large bandwidth. This is a huge requirement for the drain voltage measurement to prevent signal deformation and obtain accurate measurements. This is why they were used for the study presented in this manuscript.

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TABLE 21: High voltage probe types.

Instruments	Advantages	Drawbacks	Example
Differential probes	Galvanic isolation [200]	- Limited Bandwidth [200] - Longer connection to the device [200]	THDP0200 (Bandwith = 200 MHz; Max. voltage = 1000 V) presented in [200]
			TMDP0200 (Bandwith = 200 MHz; Max. voltage = 550 V) presented in [200]
Passive probes	High bandwidth [200]	Non-galvanic isolation [200]	TPP0850 (Bandwith = 800 MHz; Max. voltage = 1000 V) presented in [200]
			P5100A (Bandwith = 500 MHz; Max. voltage = 1000 V) presented in [200]
			PHV1000 (Bandwith = 400 GHz; Max. voltage = 1000 V)
			HVP120 (Bandwith = 400 MHz; Max. voltage = 1000 V) used in [410]

F.2 Circuit modeling for LTSpice Simulations

To be able to simulate the double source circuit described previously (Annexe F.1), several non-ideal elements were fitted on the model presented in F.2.a. The performed fitting is described in F.2.b.

F.2.a Electrical Model

F.2.a.1st Non-Ideal Inductance and Capacitors

The non-ideal models exposed in **Figure 167** were used in the studies presented in this manuscript. These are rather simple model. Nevertheless, they are sufficient to fit the model up to 120 MHz (upper limit of the E4990A impedance analyzer used in this PhD). Indeed, on the one hand, for capacitors, it takes into account the inductive behavior (L_{CAP} in **Figure 167(a)**) at high frequency with a dumping resistor (R_{CAP} in **Figure 167(a)**) for the behavior at the resonance frequency. On the other hand, for inductances, it takes into account the capacitive behavior (C_{IND} in **Figure 167(b)**) at high frequency with a dumping resistor (R_{IND} in **Figure 167(b)**) for the

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behavior at the resonance frequency. Other models exist especially for the RF domain with for instance integrated inductance model as the one used in [462].

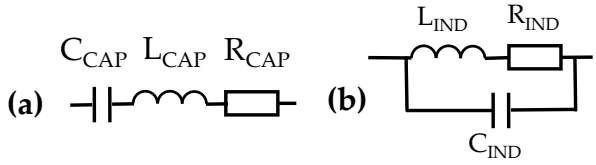

Figure 167: (a) Non-ideal capacitor model (b) Non-ideal capacitor model.

F.2.a.2nd Lossy Transmission Line

Transmission lines (twisted pairs or BNC cables in our circuit) are modeled with either non-lossy or lossy transmission line models. The lossy transmission line model is closer to the real lines which is why it was used in this PhD.

The lossy transmission line is constituted of infinitesimal cells such as the one represented in **Figure 168**.

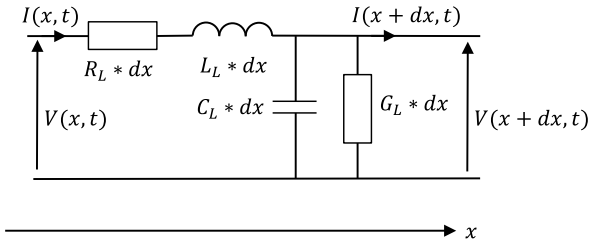

Figure 168: Infinitesimal cell with a size dx of a lossy transmission line (R_L: linear resistance; G_L: linear conductance; L_L: linear inductance; C_L: linear capacitance).

Here is the procedure to get the important equations and parameters of this model:

1. Apply the first and second Kirshhoff's law :

$$V(x+dx,t) - V(x,t) = -L_L \times dx \times \frac{\partial I(x,t)}{\partial t} - R_L \times dx \times I(x,t)$$

$$\Rightarrow \frac{V(x+dx,t) - V(x,t)}{dx} = -L_L \times \frac{\partial I(x,t)}{\partial t} - R_L \times I(x,t)$$

$$\xrightarrow[dx \to 0]{} \frac{\partial V(x,t)}{\partial x} = -L_L \times \frac{\partial I(x,t)}{\partial t} - R_L \times I(x,t) \quad (\mathbf{1})$$

$$I(x+dx,t) - I(x,t) = -C_L \times dx \times \frac{\partial V(x+dx,t)}{\partial t} - G_L \times dx \times V(x+dx,t)$$

$$\frac{I(x+dx,t) - I(x,t)}{dx} = -C_L \times \frac{\partial V(x+dx,t)}{\partial t} - G_L \times V(x+dx,t)$$

$$\xrightarrow[dx \to 0]{} \frac{\partial I(x,t)}{\partial x} = -C_L \times \frac{\partial V(x,t)}{\partial t} - G_L \times V(x,t) \quad (\mathbf{2})$$

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2. Derive (1) and (2) with respect to x applying Schwarz theorem (require solutions that are two time differentiable which is the case of plane waves that are constitute every waves):

$$\frac{\partial^2 V(x,t)}{\partial x^2} = L_L \times C_L \times \frac{\partial^2 V(x,t)}{\partial t^2} + (C_L \times R_L + G_L \times L_L) \times \frac{\partial V(x,t)}{\partial t} + G_L \times R_L \times V(x,t) \quad (\mathbf{3})$$

$$\frac{\partial^2 I(x,t)}{\partial x^2} = L_L \times C_L \times \frac{\partial^2 I(x,t)}{\partial t^2} + (C_L \times R_L + G_L \times L_L) \times \frac{\partial I(x,t)}{\partial t} + G_L \times R_L \times I(x,t) \quad (\mathbf{4})$$

From equations (3) and (4), the expression of the wave velocity is obtained:

$$u = \frac{1}{\sqrt{C_L \times L_L}}$$

Equation 32: Wave velocity inside a transmission line (L_L: linear inductance; C_L: linear capacitance).

3. Equation (3) and (4) in the complex frequency domain:

$$\frac{\partial^2 V}{\partial x^2} = -L_L \times C_L \times \omega^2 \times V + j \times \omega \times (C_L \times R_L + G_L \times L_L) \times V + G_L \times R_L \times V$$

$$\frac{\partial^2 V}{\partial x^2} = (R_L + j * \omega * L_L) * (G_L + j * \omega * C_L) * V$$

$$\Rightarrow \frac{\partial^2 V}{\partial x^2} = \gamma \times V \ (5)$$

$$\Rightarrow \frac{\partial^2 I}{\partial x^2} = \gamma \times I \ (6)$$

The solution of these second order linear differential equations are:

$$M(x) = M_P \times e^{-\gamma \times x} + M_R \times e^{\gamma \times x} \ with \ M \in \{V; I\}$$

This gives the expression of the propagation constant:

$$\gamma = \sqrt{(R_L + j \times \omega \times L_L) \times (G_L + j \times \omega \times C_L)}$$

Equation 33: Propagation constant of a lossy transmission line (ω: angular frequency; R_L: linear resistance; G_L: linear conductance; L_L: linear inductance; C_L: linear capacitance).

4. Equation (1) in the complex frequency domain with the solution of the voltage second order linear differential equation (5):

$$I = -\frac{1}{R_L + j \times \omega \times L_L} \times \frac{dV}{dx}$$

$$\Rightarrow I = \sqrt{\frac{G_L + j \times \omega \times C_L}{R_L + j \times \omega \times L_L}} \times (V_P \times e^{-\gamma \times x} - V_R \times e^{\gamma \times x}) = \frac{1}{Z_C} \times (V_P \times e^{-\gamma \times x} - V_R \times e^{\gamma \times x})$$

This gives the expression of the characteristic impedance:

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$$Z_C = \sqrt{\frac{R_L + j \times \omega \times L_L}{G_L + j \times \omega \times C_L}}$$

Equation 34: Characteristic impedance of a lossy transmission line (ω: angular frequency; R_L: linear resistance; G_L: linear conductance; L_L: linear inductance; C_L: linear capacitance).

5. To get the input impedance of the lossy transmission line that have a length L with a load impedance at the end (Z_L), VP and VR needs to be related to boundary conditions:

$$V(0) = V_P + V_R$$
$$I(0) = (V_P - V_R) \times \frac{1}{Z_C}$$
$$V(L) = V_P \times e^{-\gamma \times L} + V_R \times e^{\gamma \times L}$$
$$I(L) = (V_P \times e^{-\gamma \times L} - V_R \times e^{\gamma \times L}) \times \frac{1}{Z_C}$$

$$\left.\begin{aligned} V(L) + Z_C \times I(L) &= 2 \times V_P \times e^{-\gamma \times L} \\ V(L) - Z_C \times I(L) &= 2 * V_R * e^{\gamma * L} \end{aligned}\right\} \quad \begin{aligned} V_P &= \frac{V(L) + Z_C \times I(L)}{2} \times e^{\gamma \times L} \\ V_R &= \frac{V(L) - Z_C \times I(L)}{2} \times e^{-\gamma \times L} \end{aligned}$$

$$\frac{Z_{IN}}{Z_C} = \frac{V(0)}{Z_C \times I(0)} = \frac{V_P + V_R}{V_P - V_R} = \ \ldots = \frac{Z_L + Z_C \times \tanh(\gamma \times L)}{Z_C + Z_L \times \tanh(\gamma \times L)}$$

This gives the expression of the characteristic impedance:

$$Z_{IN} = Z_C * \frac{Z_L + Z_C \times tanh(\gamma \times L)}{Z_C + Z_L \times tanh(\gamma \times L)}$$

Equation 35: Input impedance of a lossy transmission line with a load impedance at the end (Z_L) (γ: propagation constant; Z_C: Characteristic impedance; L: line length).

6. The line properties can be deduced from the impedance of the line in short ($Z_L = 0\ \Omega$) and open ($Z_L = \infty\ \Omega$) circuit conditions (named Z_{IN_SC} and Z_{IN_OC} respectively):

$$\left.\begin{aligned} \Rightarrow Z_{IN_SC} &= Z_C \times \tanh(\gamma \times L) \\ \Rightarrow Z_{IN_OC} &= Z_C \times \coth(\gamma \times L) \end{aligned}\right\} \quad \begin{aligned} &\Rightarrow \boldsymbol{Z_C} = \sqrt{Z_{IN_SC} \times Z_{IN_OC}} \\ &\Rightarrow \boldsymbol{\gamma} = \frac{1}{L}\text{atanh}\left(\sqrt{\frac{Z_{IN_SC}}{Z_{IN_OC}}}\right) = \boldsymbol{\alpha} + j\boldsymbol{\beta} \end{aligned}$$

Note: α and β are the real and imaginary part of the propagation constant. If α is frequency independent, the signal is distorsionless (Heaviside condition).

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$$\boldsymbol{R_L} = real(\gamma \times Z_C)$$
$$\boldsymbol{G_L} = real(\gamma / Z_C)$$
$$\boldsymbol{L_L} = \frac{1}{\omega} \times im(\gamma \times Z_C)$$
$$\boldsymbol{C_L} = \frac{1}{\omega} \times im(\gamma / Z_C)$$

These properties can either provide the propagation time through the line of a given length with the wave velocity (**Equation 32**) or model transmission line in LTSpice using multiple π-cell modeling as exposed in the next part.

F.2.b Model Fitting

As it can be seen in **Figure 169**, four elements need to be modelled:

- The polypropylene capacitor ($C_{IN,2}$, $R_{IN,2}$, $L_{IN,2}$)
- The ceramic capacitor ($C_{IN,1}$, $R_{IN,1}$, $L_{IN,1}$)
- The inductive load (Single layer air core inductive coil)
- The current shunt
- The twisted pairs with their respective length L_1 and L_2 (C_L, I_L, R_L, G_L)

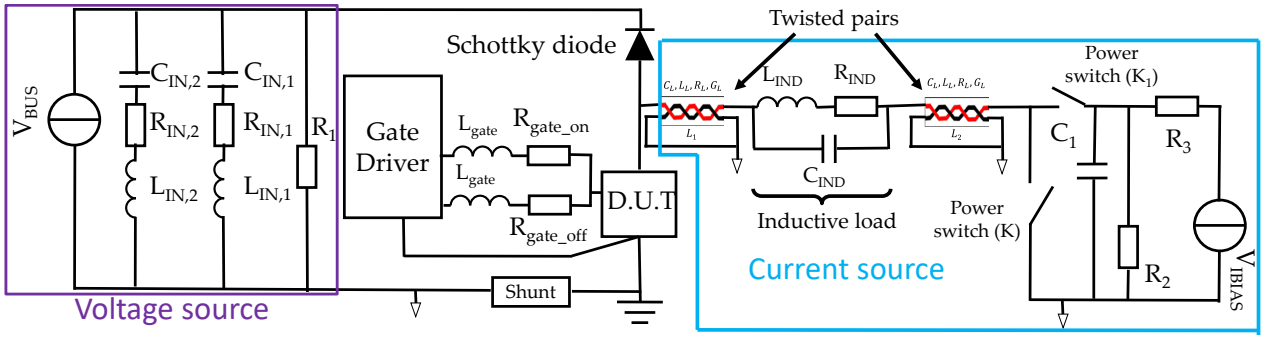

Figure 169: Simulated Double Source circuit schematics.

† **The capacitors and the inductance**

The parameters of the model presented in F.2.a.1st were obtained by fitting the simulated impedance characteristic of the model with the experimentally measured impedance (measurement performed with the Keysight™ E4990A impedance analyzer) as shown in **Figure 170**.

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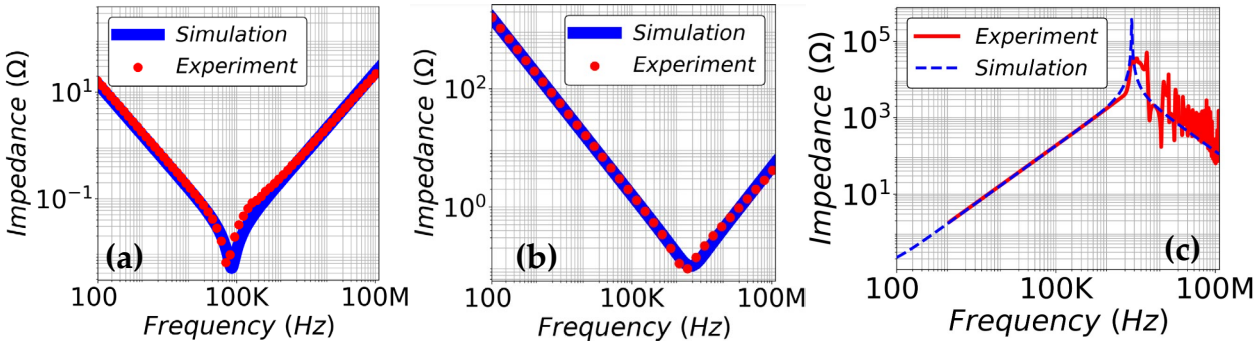

Figure 170: Experimental versus fitted LTSpice simulation impedance characteristic of the (a) polypropylene capacitor (b) ceramic capacitor (c) inductance.

TABLE 22: Modeling parameters of the discrete capacitors and inductance.

Electronic device	Parameter	Value
Polypropylen capacitor	$C_{IN,2}$	55.6 µF
	$R_{IN,2}$	9 mΩ
	$L_{IN,2}$	75 nH
Ceramic capacitor	$C_{IN,1}$	0.5 µF
	$R_{IN,1}$	200 mΩ
	$L_{IN,1}$	15 nH
Inductance	L_{IND}	292 µH
	R_{IND}	117 mΩ
	C_{IND}	12 pF

† The coaxial shunt

In the article of Wickramasinghe *et al.* [460], a shunt from the same serie (SDN-414-025) has been modeled with a resistor 25 mΩ in series with an inductance between 6 to 10 nH. The coaxial shunt is a SDN-414-10 which means that it has an internal resistance of 100 mΩ. Thus a resistance with value is used in series with a 10 nH inductance. Note that the inductance value is not that important and can be overestimated since the parasitic inductive elements due to the circuit are not taken into account.

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† Twitsted pairs

To model the twisted pairs, the lossy transmission line model (described in F.2.a.2nd) was used. The different linear properties of the line were extracted from impedance measurements in short and open conditions with a 1 m (to not be limited) and a 40 cm (for high-frequency accuracy) twisted pairs as exposed in **Figure 171**. The linear capacitance and inductance are easy to determine (L_L= 0.7 $\mu H/m$; C_L= 50 pF/m). However, high frequency effects such as skin effect (increase of the linear resistance with the frequency) and increase of the conductance with the frequency cannot be taken into account. Indeed, solution proposed in the literature works well in the AC domain but there is no confirmation in transient due to the Laplace transform use [463]. This is why the value at 10 kHz is used (R_L= 26 $\mu\Omega/m$; G_L= 0.1 μS/m). The closest line to the DUT has a length L_1 equals to 20 cm whereas the other has a 50 cm length. In LTSpice, it has been the lossy transmission line model has been implemented through a 20 π–cell structure as shown in **Figure 172**.

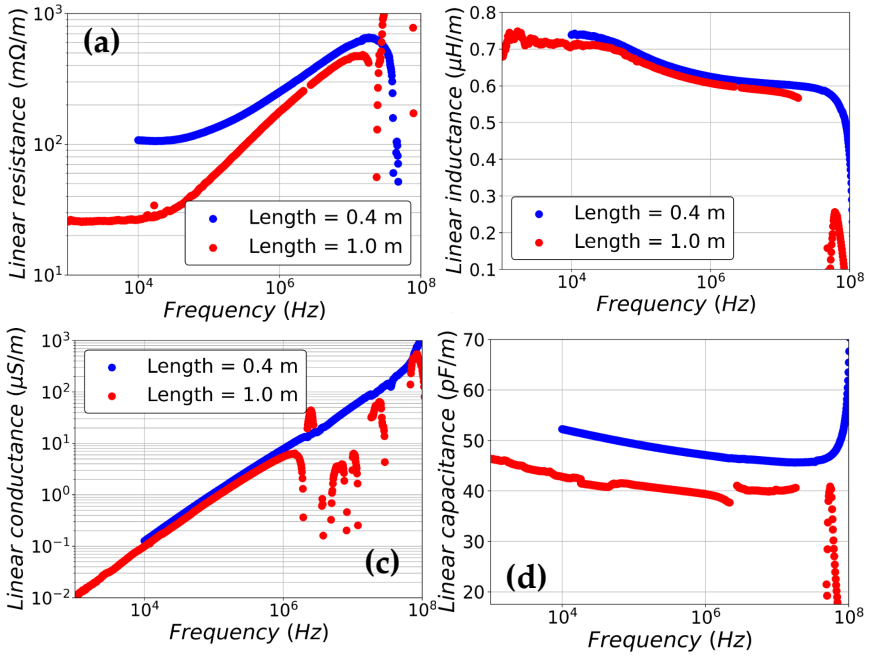

Figure 171: Twisted pair extracted (a) linear resistance (b) linear inductance (c) linear conductance (d) linear capacitance from its impedance in short and open circuit measurement.

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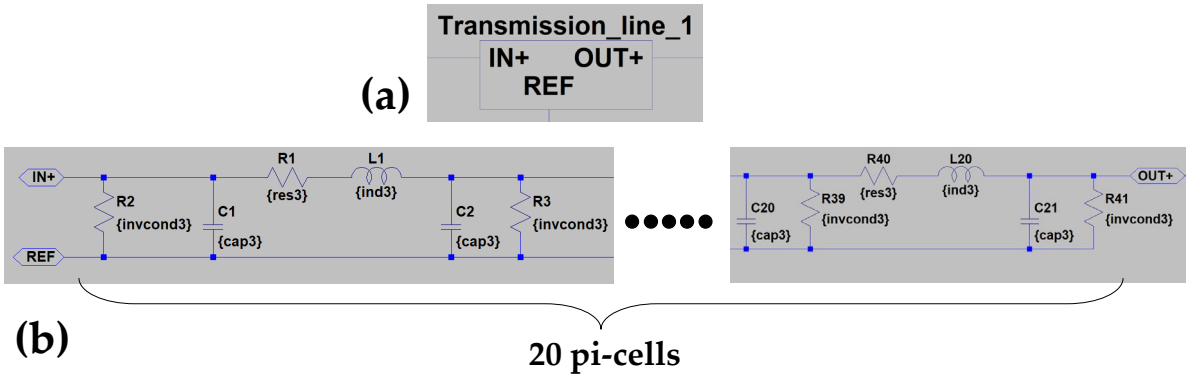

Figure 172: Lossy transmission line implemented model with 20 pi-cells (a) symbol and (b) real implementation (res3 = R_L×L/20 ; ind3 = I_L×L/20 ; invcond3 = G_L×L/21; cap3 = C_L×L/21).

F.3 Probes' Propagation Time Compensation

F.3.a Current Probe

The current probe is constituted of a coaxial shunt: SDN-414-10 [426] and a 1 m BNC coaxial cable: Radiall KX 15 reference [464] as it can be seen in **Figure 173**.

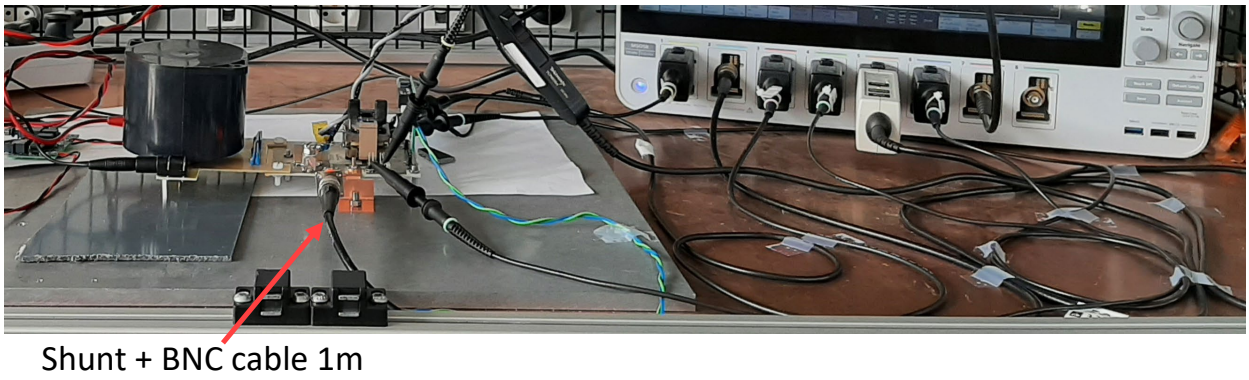

Figure 173: Visualization of the current probe implementation.

The propagation time is imposed by the coaxial cable. Note that no information has been provided by the supplier. Short and open impedance measurements performed on the cable were performed to extract the linear inductance and capacitance of the cable (with the method described in the point 6 of F.2.a.1st) as shown in **Figure 174**. It can be noted that whatever the length of the cable, properties are rather similar. With the extracted value of the 1 m cable, a wave velocity of 1.82×10^8 m/s is obtained which gives a **propagation time of 5.48 ns**.

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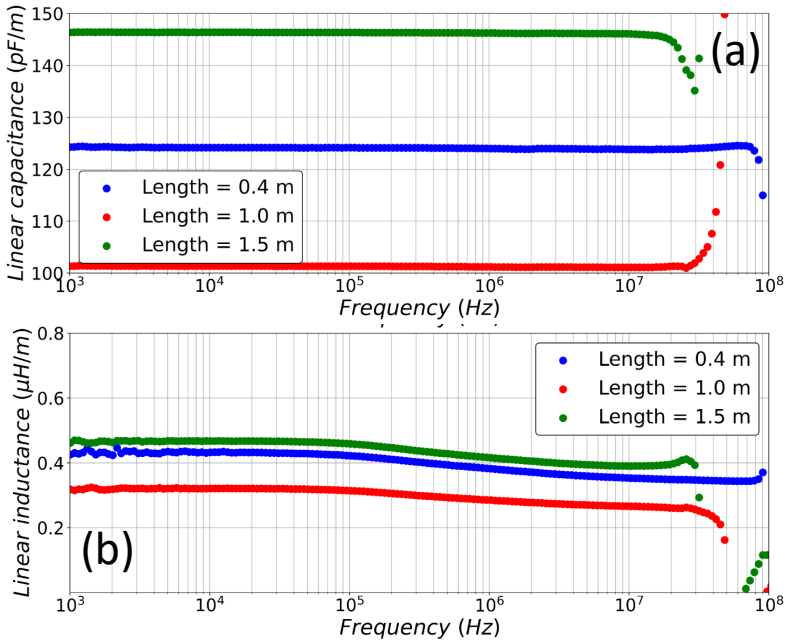

Figure 174: Linear (a) capacitance and (b) inductance of the Radiall KX15 coaxial cable.

F.3.b Voltage Probes

For both voltage probes' models (TPP0500B and TPP0850) the propagation delay times provided by the supplier either in the datasheet or displayed on the oscilloscope were taken. It is 6.1 ns for TPP0850 [427] and 5.3 ns for TPP0500B.

F.4 Technology Comparison with GaN Systems p-GaN gate

A technology comparison with one of the state-of-the-art commercialized transistors, the p-GaN gate transistors of GaN systems™ having the closest packaging (DFN) [64] is proposed here. The huge advantage of our approach is that the same testing circuit will be used for this technology comparison allowing a pure relative device comparison.

In the manuscript, it was shown that the deep recess has higher switching losses with respect to the shallow recess especially during turn-on as it can be observed again in **Figure 175(a)**, **(b)**, **(d)**, **(e)**, **(g)** and **(h)**.

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By comparing the hard switching losses at 400 V/3 A of the best 650 V/30 A fully-recessed MOS-HEMT transistors manufactured by CEA LETI (shallow gate recess) with respect to the p-GaN fabricated by GaN systems™ in **Figure 175(a)**, **(c)**, **(d)**, **(f)**, **(g)** and **(i)**, it can be seen p-GaN gate transistor has a lower turn-on energy. However, the threshold voltage difference cannot explain this difference (by contrast with the difference noticed in between shallow and deep recess (IV.2.b.i.4th)) since the threshold voltage of p-GaN gate is higher as enhanced in **Figure 176**. The difference is probably due to the lower C_{RSS} and C_{OSS} characteristics at high voltage as it can be seen in **Figure 177** (as it is partially for the difference noticed between shallow and deep recess (IV.2.b.i.4th)).

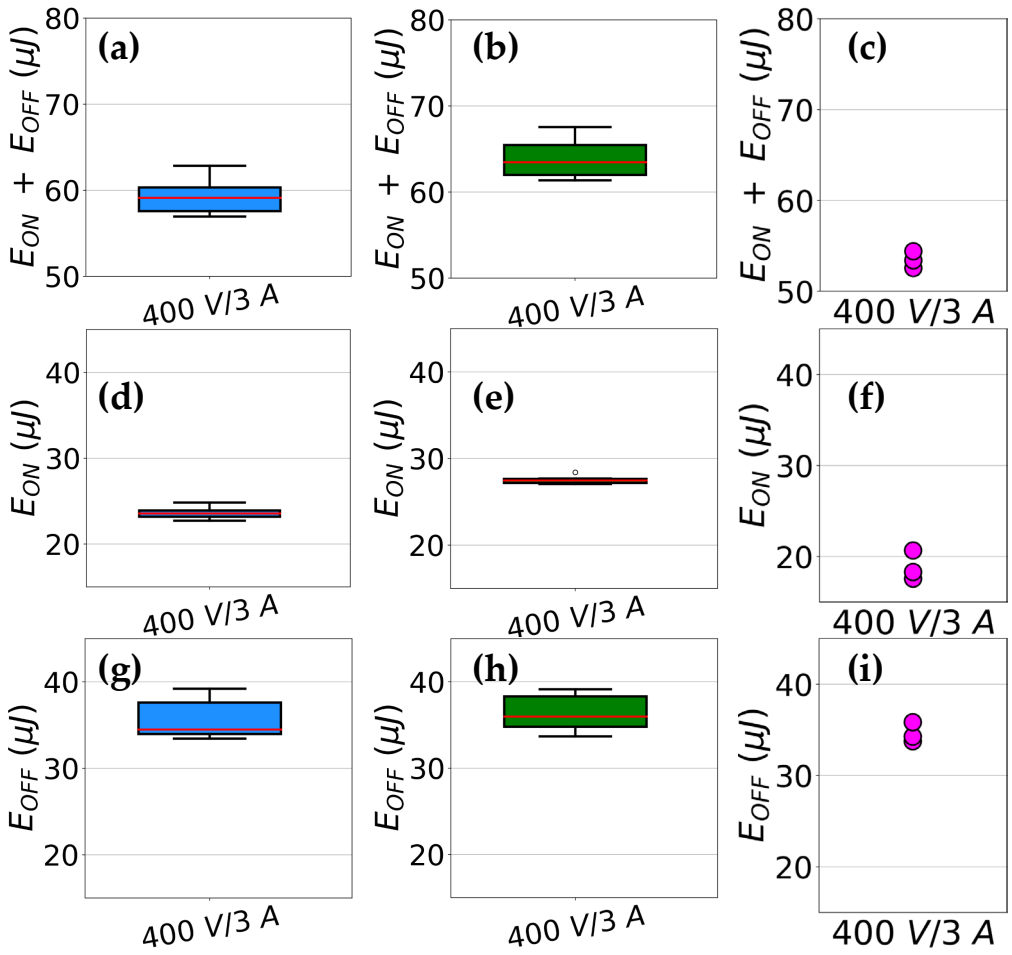

Figure 175: Extracted switching energy: (a), (b), (c) Addition of the turn-on and turn-off hard switching energy (d), (e), (f) Turn-on hard switching energy (g), (h), (i) Turn-off hard switching energy of the CEA LETI 650 V/30 A transistors: 8 deep (in green) and 6 shallow (blue) gate recess and 3 GaN Systems™ 650 V/30 A transistors (magenta).

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To go further, the state-of-the-art p-GaN gate technology may have better static characteristics at 25°C (high V_{TH} and lower R_{ON} (56 mΩ vs 82 mΩ measured but not shown here)) and also lower hard-switching losses at 400 V/3 A and 25°C however its gate fragility has been clearly observed. Indeed, no GaN Systems' device could have been tested after hard switching measurement. The gate may have been damaged by the driver power supply switch-off as the 1 A transistors.

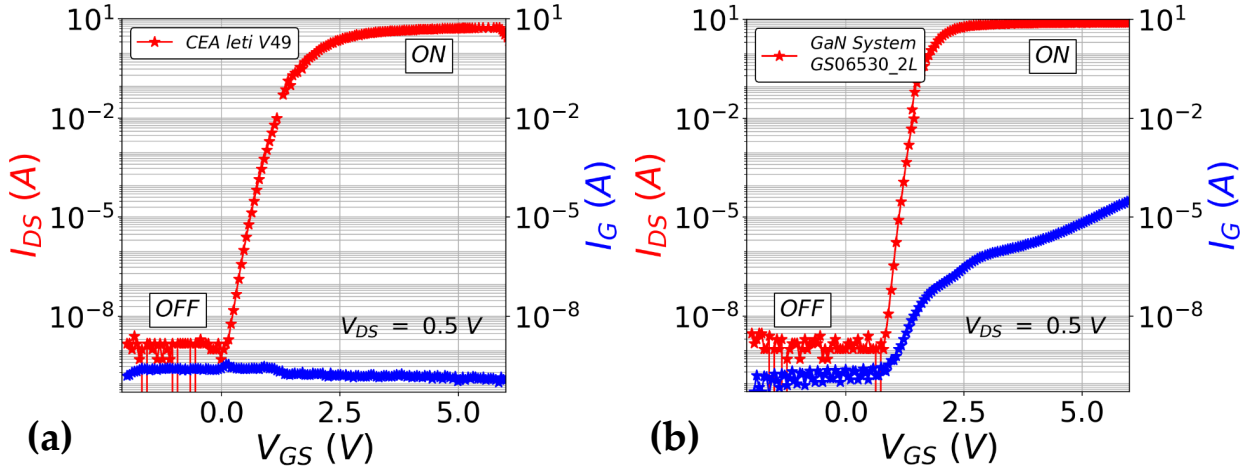

Figure 176: (a) Transfer characteristic of a typical 650 V/30 A AlGaN/GaN fully recessed MOS-HEMT transistor manufactured by CEA LETI (b) Transfer characteristic of a typical 650 V/30 A AlGaN/GaN p-GaN gate HEMT transistor manufactured by GaN Systems™.

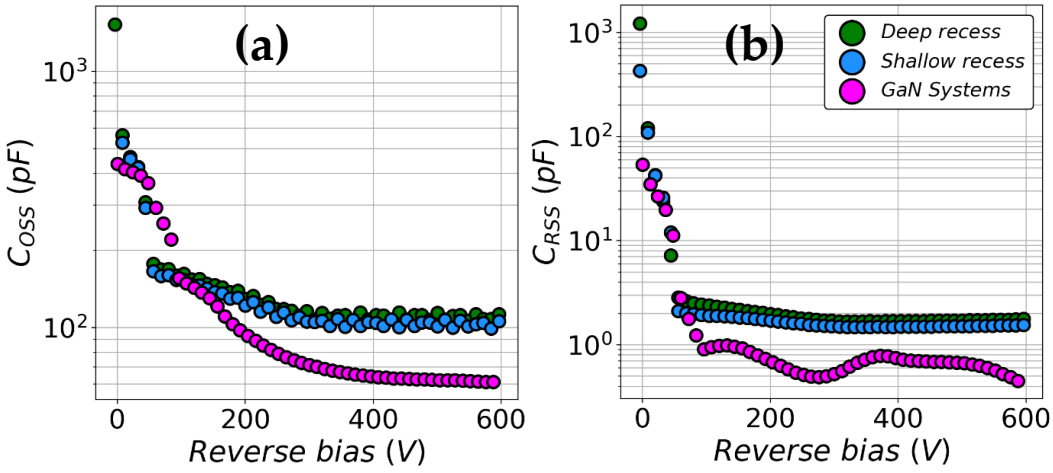

Figure 177: Capacitance characteristic at V_G = -4 V of the CEA LETI 650 V/30 A transistors: deep (in green) and shallow (blue) gate recess and the GaN Systems™ 650 V/30 A transistors (magenta) (a) C_{OSS} (b) C_{RSS}.

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Annexe G:
Transistor LTSpice Model

For this PhD, an LTSpice model for transistors was used. The latter was calibrated to perform hard-switching simulations in order to identify the physical parameters responsible for the hard-switching loss difference between 650 V/30 A AlGaN/GaN-on-Si fully recessed MOS-HEMT having different gate recess depths as presented in IV.2.b.i.4th.

This model is an electro-thermal model meaning that in addition of an electrical model, there is a thermal model that takes into account device self-heating. Both models will be presented in this annexe in addition of the parameter that has changed in between the model representing the experimental split studied in IV.2.b.i.4th.

G.1 Electrical Model

G.1.a Model Presentation

The electrical model can be split into two parts as it can be seen in **Figure 178**:

- The parasitics elements induced by the packaging (wire bonding mainly in the DFN package as shown in **Figure 179**). In our modeling, these parasitics are modeled through discrete inductive ($L_{D,pack}$, $L_{G,pack}$, $L_{S,pack}$, $L_{KS,pack}$) and resistive (R_{d_pack}, R_{g_pack}, R_{s_pack}, R_{ks_pack}) elements. They were calibrated by means of measurement performed on the Vectorial Network Analyzer (VNA): Keysight™ N5232A PNA-L with the cold-FET method described by Loris Pace in his PhD manuscript [433] (not detailed in this manuscript because no extra-content has been brought in this PhD).

It must be noted that as the substrate is wire-bonded to the source as it can be observed on the die bottom right-hand corner in **Figure 179**, the same thing is applied in the model in **Figure 178**.

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- The unpackaged transistor model is framed in red in the figure. It can be split in five different parts:

  - **The access resistances associated with the ohmic contact and the 2DEG resistance (Rdd, Rss).** They are calculated knowing the layout and physical parameters such as the 2DEG mobility, electron density and the contact resistivity that were measured using test structures (Transfer Line Method, Gated Van Der Pauw).
  - **The access resistances associated with the FEOL and BEOL metallization lines (R_{gg}, R_{dd_sup}, R_{ss_sup}).** The source and drain resistance were determined thanks to $R_{ON}(V_G)$ measurements performed on unpackaged devices whereas R_{gg} was determined using the method described by Loris Pace in his PhD manuscript [433].
  - **The parasitic capacitance (C_{GD}, C_{GS}, C_{DS}) in between transistor electrodes**. They are defined as a constant capacitance (C_{GD_c}, C_{GS_c}, C_{DS_c}) in parallel with a non-linear capacitance fitted on the experimental curves. The latter is defined by its charge with the following expression:

$$Q_{MN} = \sum_{i=1}^{J} B_{i,MN} \times \ln\left(1 + e^{\frac{V(M)-V_{DS}-D_{i,MN}}{E_{i,MN}}}\right)$$

Equation 36: Generic charge definition of the transistor non-linear capacitance ($B_{i,MN}, D_{i,MN}, E_{i,MN}$: Fitting constants; $MN \in \{SD, GS, GD\}$; J: number of exponential decay in the capacitance characteristics (1, 2, 3 for C_{GS}, C_{SD}; C_{GD} respectively)).

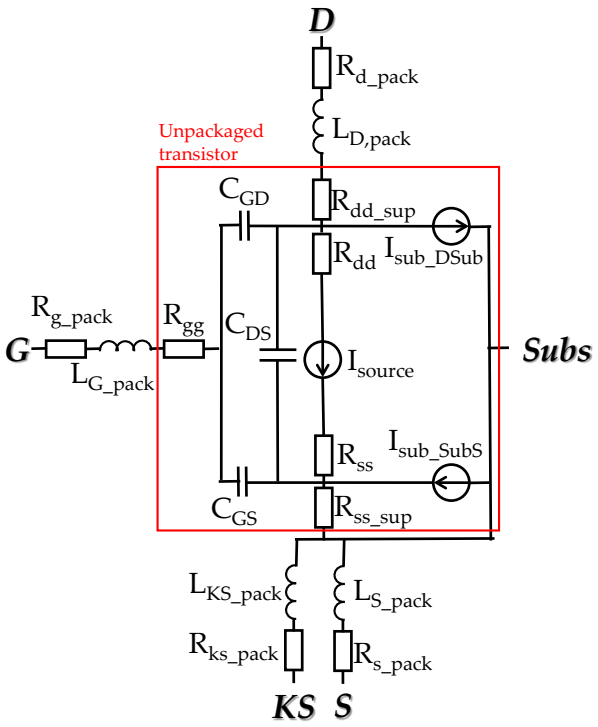

Figure 178: Equivalent circuit schematics of the transistor model.

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- **The main current source (I_{source}) is equivalent to the MOS channel of the MOS-HEMT.** It follows the well-known long channel MOSFET equations adapted from [465] (the reference nodes for the current calculation are those at the termination of the current source for the "source" and "drain"; whereas for the "gate", it is the common node between R_{gg} and C_{GD}) when V_{GS} - V_{TH} is higher than zero:

$$I_{DS} = \frac{W_g}{L_g} \times \mu_{eff} \times C_{ox,eff} \times \left((V_{GS} - V_{TH}) \times V_{DS} - \frac{{V_{DS}}^2}{2} \right)$$

Equation 37: Long channel MOSFET drain current in the linear regime ($C_{ox,eff}$: Effective oxide capacitance; μ_{eff}: Effective mobility; W_g: Gate width; L_g: Gate length; V_{GS}: Gate to source voltage; V_{TH}: Threshold voltage; V_{DS}: Drain to source voltage).

$$I_{DS} = \frac{W_g}{2 \times L_g} \times \mu_{eff} \times C_{ox,eff} \times (V_{GS} - V_{TH})^2$$

Equation 38: Long channel MOSFET drain current in the saturation regime ($C_{ox,eff}$: Effective oxide capacitance; μ_{eff}: Effective mobility; W_g: Gate width; L_g: Gate length; V_{GS}: Gate to source voltage; V_{TH}: Threshold voltage).

When the quantity V_{GS} - V_{TH} is lower than zero, the drain current follows this expression:

$$I_{DS} = G_{REV} \times \left(\frac{T}{T_0} \right)^{\beta} \times V_{DS}$$

Equation 39: Blocking MOSFET drain current (G_{REV}: Reverse conductivity; T_0: Reference temperature; β : Fitting parameter; V_{DS}: Drain to source voltage).

The W_g and L_g parameters are equal to the corresponding mask lengths whereas V_{TH} and the product $C_{OX,eff} \times \mu_{eff}$ are fitting parameters adjusted to fit the experimental curves $I_D(V_{GS})$ and $I_D(V_{DS})$ curves.

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- The vertical current source (I_{sub_DSub}, I_{sub_SubS}). As it was studied in the manuscript (III.3.b.iv), at high voltage, the vertical current is ruled by Nearest Neighbor Hopping (NNH) transport. The model current sources therefore follow its analytical expression with the parameters extracted from the fit in III.3.b.ii.5th (assuming that the vertical current between substrate and source has the same expression as the drain to substrate current[12]) :

$$I = L_{OHM} \times W_g \times q \times a \times K_B \times T \times DOS \times \nu \times e^{\frac{q \times a \times \frac{V}{d}}{K_B \times T} - \frac{q \times \phi_T}{K_B \times T} - 2 \times a \times \alpha}$$

Equation 40: Blocking MOSFET drain current (G_{REV}: Reverse conductivity; T_0: Reference temperature; α : Fitting parameter; V_{DS}: Drain to source voltage).

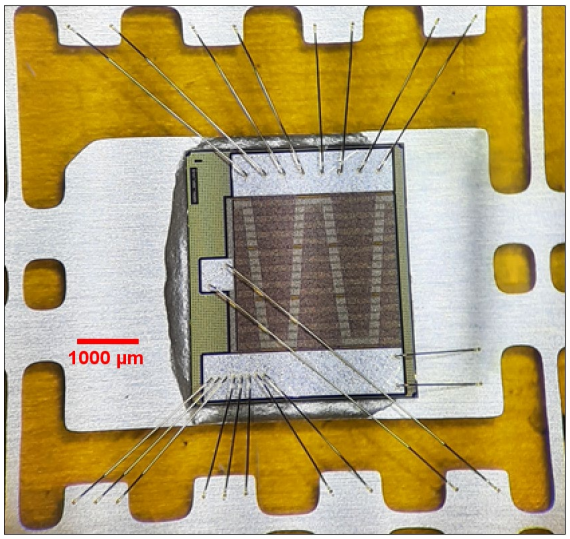

Figure 179: Wire bonding step picture during the packaging procedure.

[12] This point has not been verified during the PhD. Nevertheless, it does not matter because for our purpose, the voltage applied in between the source and the substrate does not exceed several volts meaning that the current can be neglected.

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G.1.b Model Parameter Differences Between the Model Calibrated for Deep and Shallow Recess Transistors

For the identification of the model parameters responsible for the hard-switching loss difference between the two different studied gate recess depths in IV.2.b.i.4th, one or different parameters changes were performed. **TABLE 23** summarizes the progressive change in the model parameters that were used in this study.

TABLE 23: LTSpice model parameters' changes.

Main targeted characteristics	Parameter name	Shallow std	Shallow mod1	Shallow mod2	Shallow mod3	Shallow mod4	Shallow mod5	Deep std
Leakage current in blocking mode	G_{rev} (pS)/ν (GHz)	6/332	12/507	12/507	12/507	12/507	12/507	12/507
On-state current	μ_{eff} ($cm^2/(V.s)$)	80	80	70	70	70	70	70
	V_{TH} (V)	0.75	0.75	0.75	1.2	1.2	1.2	1.2
C_{GD}	$C_{GD\ c}$ (pF)	1.46	1.46	1.46	1.46	1.75	1.75	1.75
	$B_{2,GD}$ (pF)/ $D_{2,GD}$ (V)/ $E_{2,GD}$ (V); $B_{3,GD}$ (pF) / $D_{3,GD}$ (V)	137/-34/4; 275/-12	137/-34/4; 275/-12	137/-34/4; 275/-12	137/-34/4; 275/-12	137/-34/4; 275/-12	220/-30/6; 357/-8.5	220/-30/6; 357/-8.5
C_{GS}	$B_{1,GS}$ (F)	0	0	0	0	0	0	3×10^{-11}

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G.2 Thermal Model

G.2.a Model Presentation

In the literature, there are two kinds of thermal models [425], [466]:

- The Cauer model, T-model or ladder network (illustrated in **Figure 180(a)**): it corresponds to physics. Indeed each thermal resistance and capacitance couple represent each layer of the stack through which the heat is dissipated (analytical expression: **Equation 41** and **Equation 42**). Thus, the temperature spreading through each layer can be followed on each node of the network. Using this model in G.2.b, it will be shown that device self-heating during a single hard switching pulse event can be neglected.

$$R_{TH} = \frac{L}{\lambda_{TH} \times A}$$

Equation 41: Thermal resistance expression (λ_{TH}: Thermal conductivity; A: Section through which the heat is dissipated; L : Layer length across which the heat travels).

$$C_{TH} = c_{TH} \times \rho \times V$$

Equation 42: Thermal capacitance expression (c_{TH}: Specific heat capacity; ρ: Volumic mass; V: Layer volume).

- The Foster model or π-model (illustrated in **Figure 180(b)**): it is a model adapted for a thermal impedance measurements calibration as described in [466].

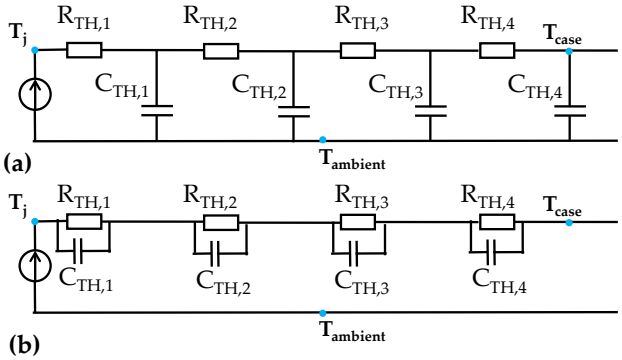

Figure 180: Thermal models: (a) Cauer model (b) Foster model.

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G.2.b Negligible Self-Heating Effect During a Single Hard-Switching Event

Before the hard-switching event, there is a period, in which the DUT is on while the inductive load is charging. During this PhD, the on-time was set to 300 µs. The thermal model assumes a dissipation through the back side of the sample only. The heat has to go through four different layers meaning that the model is composed of four RC patterns:

- The GaN epitaxy with $\lambda_{TH,GaN}$ = 130 W/(m.K) and $c_{TH,GaN}$ = 490 J/(Kg.K) [12]. This gives a thermal resistance of 3.3 mK/W and a thermal capacitance of 114 µJ/K.
- The silicon substrate with $\lambda_{TH,Si}$ = 130 W/(m.K) and $c_{TH,Si}$ = 700 J/(Kg.K) [12]. This gives a thermal resistance of 204.1 mK/W and a thermal capacitance of 3842 µJ/K.
- The silver glue $\lambda_{TH,SnAgCu}$ = 80 W/(m.K) and $c_{TH,SnAgCu}$ = 220 J/(Kg.K) [467]. This gives a thermal resistance of 66.3 mK/W and a thermal capacitance of 755 µJ/K.
- The thermal pad of the packaging (copper alloy with a matt tin coating) with $\lambda_{TH,Cu}$ = 400 W/(m.K) and $c_{TH,Cu}$ = 385 J/(Kg.K). This gives a thermal resistance of 53.1 mK/W and a thermal capacitance of 6471 µJ/K.

This model was submitted to an over-estimation of the power dissipated in the transistor as shown in **Figure 181**. To do so, the transistor behaves as a resistor (on-state resistance of 80 mΩ) and was stressed with linear increasing current (schematic of the current shape illustrated in **Figure 165**) reaching 10 A (lower than the maximum current undergone by the experimental device).

As a result, the junction temperature which corresponds to the temperature in the conductive channel (2DEG) to not exceed 2°C as shown in **Figure 181**. This is why the device self-heating was neglected.

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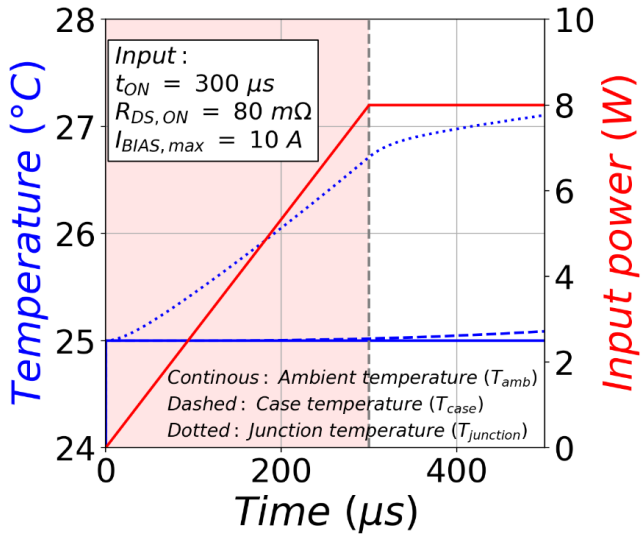

Figure 181: Thermal model time response assuming that the transistor is a 80 mΩ resistor undergoing a linear increase of the current reaching 10 A after 300 µs.

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Résumé étendu (français)

† Introduction générale

De nos jours, l'électrification de notre société crée une demande croissante de technologies associées à la conversion d'énergie (les exemples les plus connus étant les chargeurs de téléphones portables, d'ordinateurs portables, de voitures électriques, etc). S'en suit de très belles opportunités pour les centres de recherche tel que le Commissariat à l'Energie Atomique et aux énergies alternatives. L'électronique de puissance, au coeur de la conversion d'énergie, est aujourd'hui dominée par la technologie en silicium. Cependant, cette dernière révèle certaines limites qui peuvent être dépassées par des technologies à base de semiconducteurs dits à "grand gap" comme le carbure de silicium (4H-SiC) et le nitrure de Gallium (2H-GaN) qui fait l'objet de cette thèse. C'est dans ce contexte, que les transistors à haute mobilité électronique (HEMT) ont pu voir le jour. Ils sont aujourd'hui commercialisés par des industriels tel que EPC™, Infineon™, GaN Systems™, Navitas™ principalement [4].

Néanmoins, les performances théoriques de ces interrupteurs de puissance en conduction et en commutation n'ont pas encore été atteintes. Pour cela, une méthode d'optimisation proposée consiste à réduire la longueur du composant (Johan T. Strydom dans le livre de Meneghesso *et al.* [5, pp. 145–148]) comme illustré sur la **Figure 182**. En effet:

- La résistance à l'état passant ($R_{DS,ON}$ sur la **Figure 182**) va être réduite ce qui est intéressant pour diminuer les pertes en conduction, et la résistance spécifique va être d'autant plus faible. En effet, elle est proportionnelle à l'encombrement sur le wafer qui sera réduit ($R_{ON} = R_{DS,ON} \times A$ sur la **Figure 182**),
- Les charges associées aux transistors (Q_{XX} sur la **Figure 182**) vont être moins importantes. Par conséquent, la vitesse de commutation devrait être augmentée et de ce fait, les pertes en commutation réduites.

Ces deux points améliorent l'efficacité du convertisseur (ex : chargeur) dans lequel on retrouve le transistor. Cependant l'approche proposée reste limitée par :

- La possible réduction de la tenue en tension en blocage avec l'augmentation du champ électrique latéral (à tension donnée) (multipliée environ par trois "3× V/µm" avec une longueur divisée par trois sur la **Figure 182**),
- L'augmentation de la vitesse de commutation va cependant augmenter l'impact des éléments parasites sur les signaux de la commutation altérant possiblement sa stabilité.

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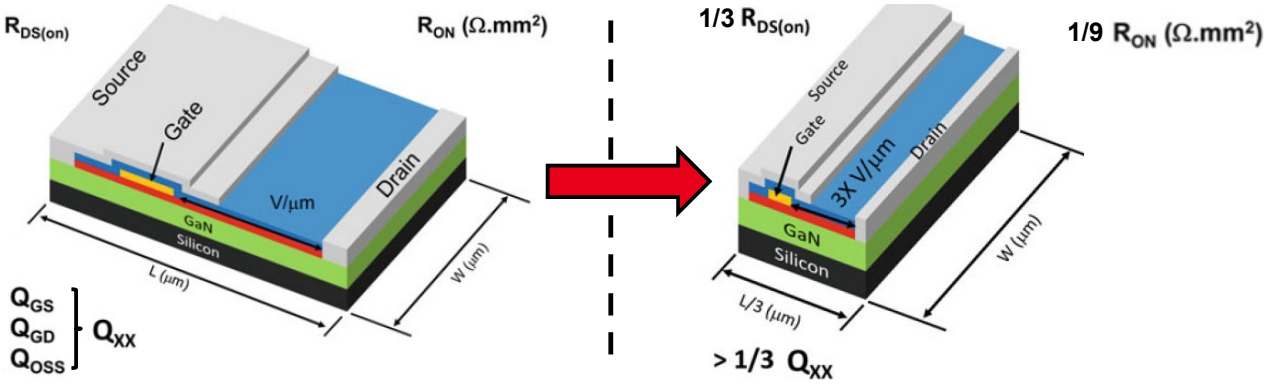

Figure 182 : Vue d'ensemble de l'effet de la réduction de la longueur de transistor sur certaines de ses caractéristiques (adapté à partir de [5, p. 146]).

Au regard des points évoqués précédemment, et à la lumière d'un état de l'art développé dans le Chapitre 1 (qui aura pour but de situer la technologie étudiée pendant cette thèse par rapport aux technologies concurrentes faites à partir de GaN ou de SiC ainsi que de justifier les choix d'orientation pris sur les différents axes de recherche détaillés par la suite), la thèse se propose d'apporter des éléments de compréhension sur :

- La distribution du champ électrique à l'état bloqué au vue d'une optimisation de cette dernière pour des composants à taille réduite. Cela commencera avec un statut sur les limites actuelles en terme de tenue en tension des diodes latérales Schottky fabriquées au CEA LETI dans le Chapitre 2 et une amélioration de la modélisation TCAD de ces composants dans le Chapitre 3.
- Les pertes en commutation avec une étude expérimentale de l'impact des procédés et du layout dans le Chapitre 4 avec l'utilisation de simulations LTSpice et TCAD pour l'analyse.

En effet ces connaissances sont nécessaires pour pouvoir réaliser un dimensionnement de composants tout en essayant d'optimiser à la fois la tenue en tension et les pertes en commutation qui peuvent être determinantes pour le fonctionnement du composant.

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† Chapitre 1 : Les composants à Hétéro-Jonction AlGaN/GaN sur Substrat Silicium pour l'Electronique de Puissance : Etat de l'art

Le Nitrure de Gallium dans sa configuration cristalline dite wurtzite (2H-GaN) est un semiconducteur à large bande d'énergie interdite (E_G = 3.4 eV par rapport au silicium : E_G = 1.1 eV [12]) ce qui lui confère des propriétés intéressantes pour l'électronique de puissance. Il possède un champ électrique de claquage élevé (E_C = 3.3 MV/cm par rapport au silicium : E_C = 0.3 MV/cm [12]) ce qui se révèle intéressant pour des applications de haute tension. De plus, c'est un materiau possédant deux types de polarisations :

- Une polarisation spontanée due à la non concordance des barycentres de charge dans la maille primitive comme illustré sur la **Figure 183(a)**. En prenant du recul sur le cristal (**Figure 183(b)**), les plans de charges résultants et constituant du cristal vont se compenser localement laissant uniquement deux plans de charges dipolaires aux interfaces du matériau. Il en résulte la formation d'un champ de polarisation spontanée.
- Une polarisation piézoélectrique ($\overrightarrow{P_{PZ}}$) s'ajoutant à la spontanée lorsque le matériau subit une déformation. C'est notamment le cas dans l'AlGaN comme montré sur la **Figure 183(c)**.

  → La création d'un gaz bidimensionel d'électrons (2DEG) à l'interface AlGaN/GaN est le résultat de la compension locale des charges de polarisation [45]. Il est caractérisé par une forte mobilité électronique allant jusqu'à 2300 cm²/(V.s) à 25°C [52]. Ce qui permet d'avoir notamment un composant ayant une faible résistance à l'état passant.

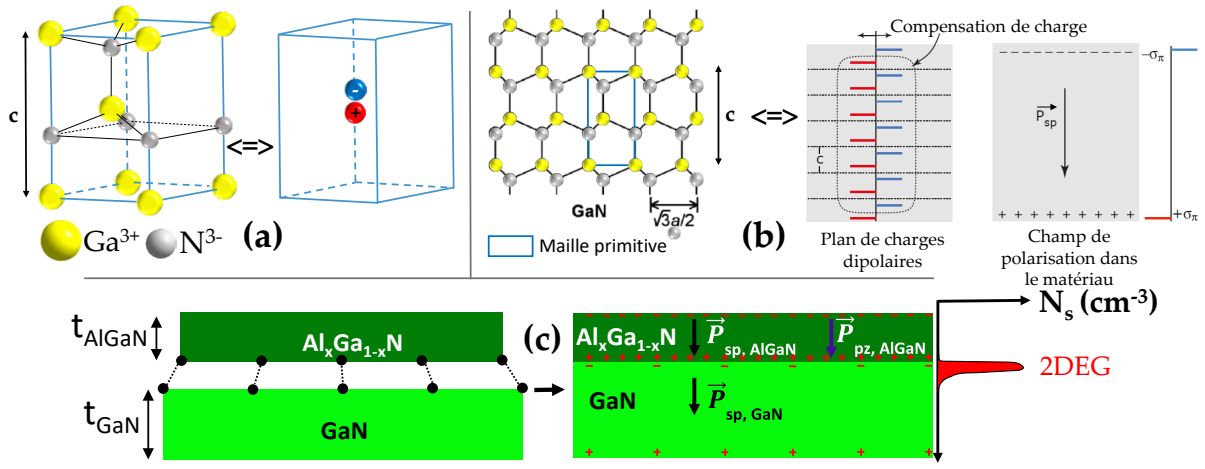

Figure 183 : (a) Maille primitive du GaN hexagonal avec son équivalent dipolaire (b) Vue d'ensemble du cristal avec sa représentation en plan de charge dipolaire entrainant un champ de polarisation spontanée $\overrightarrow{P_{SP}}$ (c) Représentation de la formation d'un gaz bidimensionnel d'électrons à l'hétéro-interface AlGaN/GaN où l'AlGaN est contraint au paramètre de maille du GaN relaxé.

C

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Ces propriétés sont utilisées pour fabriquer des diodes latérales Schottky et transistors latéraux à enrichissement (tension de seuil positive ; l'architecture la plus utilisée **Figure 184(a)**), notamment pour les diodes Schottky 650 V/6 A et les transistors 650 V/30 A (dont une partie du 2DEG est coupée par une grille type Metal Oxyde Semiconducteur (MOS) comme montré sur la **Figure 184(b)**), fabriqués tous deux, sur un substrat silicium 200 mm au CEA LETI. Cependant, la figure de mérite $R_{ON,SP}$ vs tenue en tension/BV (**Figure 184(c)**) du transistor montre que les performances théoriques ne sont pas encore atteintes probablement due à une gestion du champ électrique non-optimisée. En effet, on peut voir qu'en diminuant le facteur d'idéalité de la distribution du champ électrique β_e (défini sur la **Figure 184(d)**) (courbes rouges vers courbes oranges), les courbes théoriques se rapprochent des points expérimentaux. Ceci justifie de l'interêt

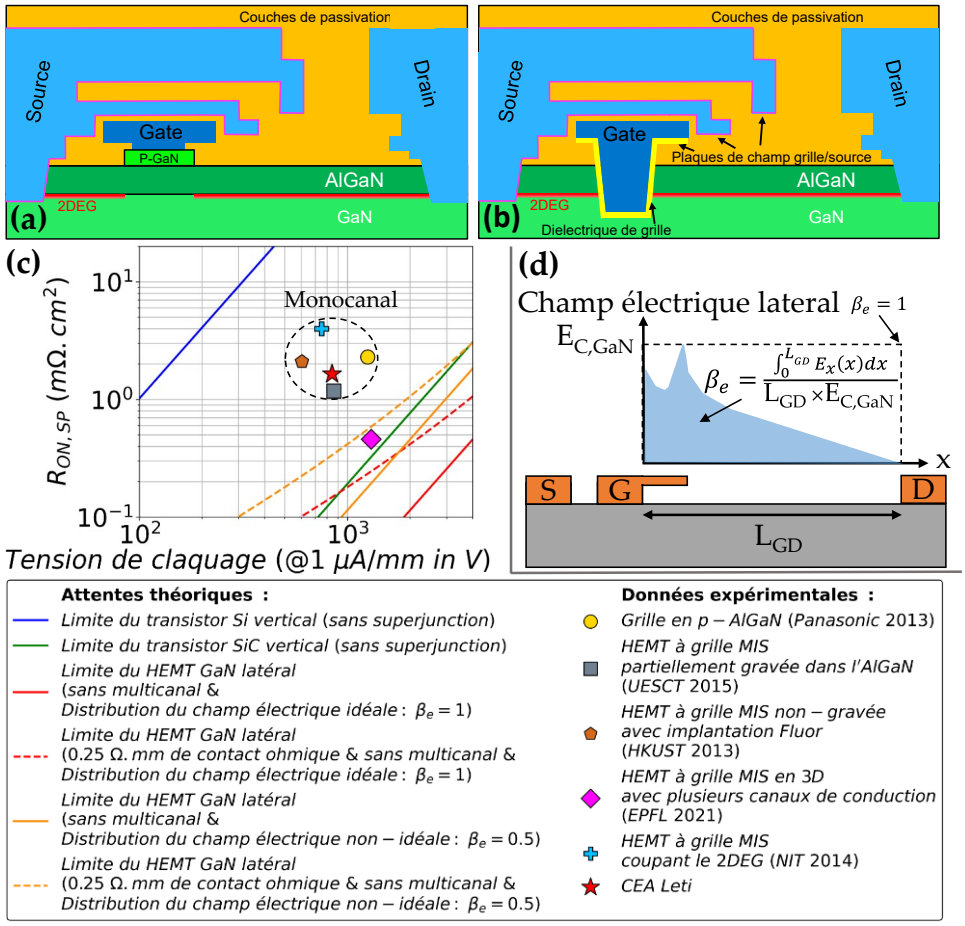

Figure 184 : (a) HEMT à grille p-GaN (b) HEMT à grille MOS jusqu'au 2DEG (c) $R_{ON,SP}$ vs tenue en tension de l'état de l'art des HEMT normally-off (références utilisées, listées sur **Figure 15**) par rapport aux attentes théoriques [89] (paramètres utilisés, listés sur **Figure 15**) (d) Définition du facteur d'idéalité de la distribution du champ électrique.

D

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porté à la réduction de la taille des composants (pour réduire la résistance spécifique) et à l'optimisation de la distribution du champ électrique. Ces transistors sont destinés à des applications domestiques (chargeurs de téléphone), aux voitures électriques, au photovoltaïque, à l'industrie et à l'aéronautique. Les convertisseurs visés ont une puissance de sortie comprise entre 0.01 et 10 kW et une fréquence de commutation allant de 10 kHz à 10 MHz [125]. Enfin, les transistors GaN se demarquent sur cette gamme vis-à-vis des transistors MOSFET SiC et à Superjonction en Silicium grâce à leurs meilleures figures de mérite : $R_{ON} \times C_{OSS}$, $R_{ON} \times Q_G$ [96].

On énumère, aujourd'hui, différentes solutions pour améliorer la tenue en tension des composants latéraux à hétérojonction : plaque de champ [149]–[153], couche « peu résistive » [89], [162], superjonction polaire [165], [166], ingénierie des couches de l'épitaxie [169]–[177], retrait partiel/complet du substrat [182]–[184]. Neanmoins la technique la plus répandue, reste les plaques de champ (comme utilisé au CEA). La **Figure 185** explique simplement leur fonctionnement dans le cas d'une diode (véhicule de test utilisé pour étudier la tenue en tension dans cette thèse). En effet, on peut y apercevoir un composant sans/avec plaque de champ ainsi que le champ électrique à différentes tensions. Dans le cas sans, en augmentant la tension on peut voir que toute la chute de potentiel et donc le champ électrique se trouve à la jonction métal-semiconducteur. Dans le cas avec, le couplage electrostatique imposé par la plaque de champ limite la chute de tension à cette jonction pour que la chute de tension puisse se faire plus loin dans le canal (à l'aplomb du bord de la plaque de champ).

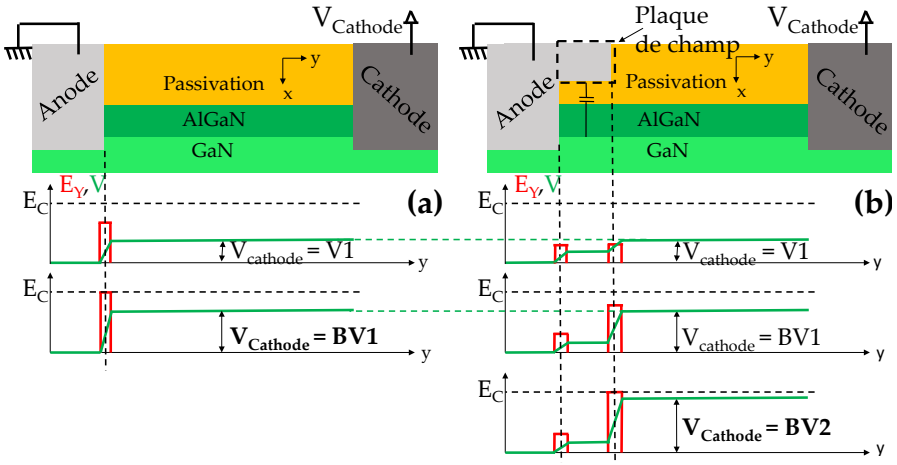

Figure 185 : Fonctionnement théorique d'une plaque de champ dans un cas idéal (champ électrique latéral uniquement) adapté à partir des explications de Ma *et al.* [149] pour un composant (a) sans plaque de champ (b) avec plaque de champ.

E

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Cela permet de distribuer le champ électrique plus uniformement entre les deux contacts.

Afin d'étudier expérimentalement le champ électrique dans le composant, différentes techniques ont été développées pour des applications radio-fréquence (et non de puissance) comme par exemple le « Electric field induced second harmonic generation » [191] ou bien le « Two photon Optical Beam Induced Current » [190]. Cependant ces techniques ne sont pas applicables aux composants de puissance du fait de la présence d'épaisses plaques de champ (refléchissant le signal optique dans la majorité des cas). C'est pour cela que le champ électrique sera étudié en simulation TCAD dans cette thèse avec une optimisation de la modélisation.

Concernant les pertes en commutation, elles ont lieu lors de la commutation dure, car on observe la superposition d'un fort courant (en rouge sur la **Figure 186**) et d'une forte tension (en violet sur la **Figure 186**) aux bornes du transistor ce qui induit des pertes par effet Joule dans le transistor. Il existe différentes méthodes expérimentales pour les mesurer : les méthodes calorimétriques [203]–[210], la méthode par opposition [201], [211]–[213], la mesure indirecte [215], l'estimation via un modèle analytique [216], [217] et la plus connue, le Double Pulse (DPT) [195]–[199]. Néanmoins, aucune de ces dernières ne sera retenue pour diverses raisons qui ne seront pas détaillées ici (complexité à mettre en place avec le temps accordé pendant la thèse, pas assez de composants disponibles, etc).

Une méthode similaire au Double Pulse a vu le jour dans les années 90 : le Double Source (DST) (présenté dans l'article de Garrab *et al.* [218]) et sera utilisée durant cette thèse. En effet, elle possède entre autres, l'avantage par rapport au DPT de ne pas stresser le composant avant la commutation ce qui limite son impact sur l'énergie mesurée.

Pour finir, lorsqu'on mesure les pertes en commutation, sur le DPT ou le DST, l'intégrale sur un interval de temps donné du produit du courant par la tension est effectué, ce qui implique :

- Que l'on choisisse une norme définissant le temps d'integration. En effet, Keuck *et al.* [215] ont démontré que selon la norme choisie pour des composants GaN, les pertes extraites sont différentes. Dès lors, les normes imposées par "IEC 60747-9 standard" (défini dans [215]) seront utilisées dans ce manuscrit.
- Que l'on synchronise les deux signaux dont on fait le produit. Ceci sera réalisé par la prise en compte des temps de propagation des différents moyens de mesure.

F

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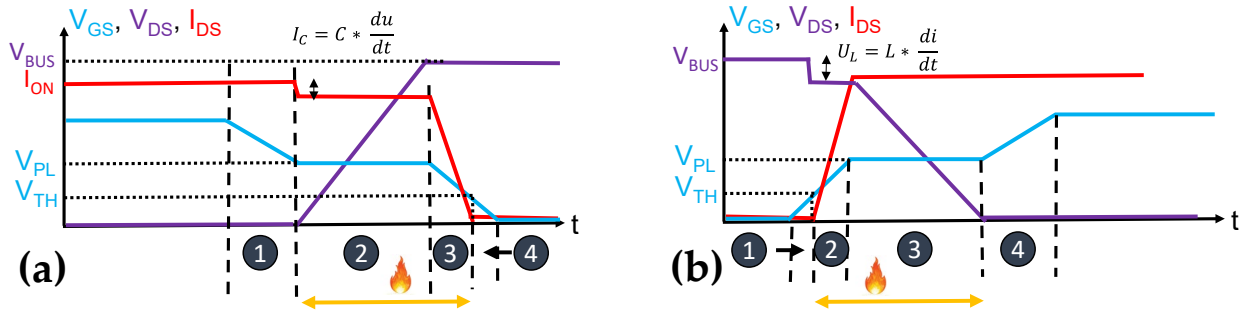

Figure 186 : Schéma des signaux associés à la commutation dure (adapté de [119]) avec la flamme représentant le moment où il y a des pertes pendant le passage à l'état (a) bloqué (b) passant.

† Chapitre 2 : Etude expérimentale de la limite de la tenue en tension des diodes Schottky AlGaN/GaN sur silicium

Avant d'étudier et d'optimiser la distribution du champ électrique, la limite expérimentale de la tenue en tension des composants actuels fabriqués au CEA LETI a été évaluée. Cette étude s'est portée sur les diodes Schottky qui se comportent similairement aux transistors en blocage. En effet la grille et la source correspondent à l'anode car elles sont à peu près au même potentiel et le drain correspond à la cathode. Cette étude est réalisé avec des tests non-réversibles où le composant est soumis à une rampe en tension jusqu'à atteindre une certaine compliance (la plupart des composants sont détruits une fois arrivés à ce point). Le travail a été mené sur deux épitaxies différentes illustrées sur la **Figure 187** ainsi que sur plusieurs « layout » de composants listés dans la **TABLE 24** mais aussi dans des conditions de polarisation du substrat différentes (connecté à l'anode ou laissé flottant). Des méthodes de caractérisations électriques et optiques ont été utilisées pour mener une analyse de défaillance et donc mettre en avant le mécanisme et le lieu de claquage.

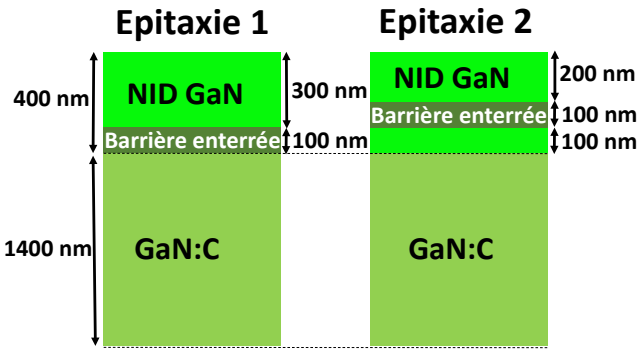

Figure 187 : Schéma des deux épitaxies étudiées (NID : Non-intentionnellement dopée).

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TABLE 24 : Différents "layout" étudiés (Variations du paramètre étudié en gras).

Nom de "layout"	L_{AC} (µm)	FPG0 (µm)	FPG1 (µm)	FPG2 (µm)	FPG3 (µm)	$\sum_i FPGi$	FPD (µm)
FPG0-1	16	**1**	1	1	1	**4**	0.5
FPG0-2	16	**2**	1	1	1	5	0.5
FPG0-3	16	**3**	1	1	1	6	0.5
FPD-0d25	16	2	2	2	2	8	**0.25**
FPD-1	16	2	2	2	2	8	**1**
FPD-2	16	2	2	2	2	8	**2**
FPG1-1d5	16	1	1.5	1.5	1	**5**	0.5
LAC-16	16	2	2	2	2	**8**	0.5
LAC-30	**30**	2	2	2	2	8	0.5

- Dans un premier temps, l'étude des composants claqués avec le substrat connecté à l'anode révèle que les composants sont limités par la tenue en tension verticale (entre la cathode et le substrat) vers 1000 V. Cela a été notamment montré par une invariance de la tension de claquage en fonction de la distance séparant l'anode et la cathode et par la prédominance des fuites verticales dans les fuites totales (non montré dans ce résumé). Et pour la première fois, une observation expérimentale du claquage diélectrique de la couche de nucléation (en AlN) a été divulguée comme on peut le voir sur la **Figure 188**. Ce claquage est potentiellement assisté par les dislocations car la fusion des materiaux dans les couches d'AlGaN du dessus forme un cône bien droit (**Figure 188(a)**). Le claquage est initié depuis de l'AlN car en s'éloignant du lieu de claquage (**Figure 188(b)**), on observe que la fusion des matériaux a une forme d'ellipse dont le centre se situe à l'interface AlN/Si où l'AlN est connu pour bloquer le passage d'électrons [297]).

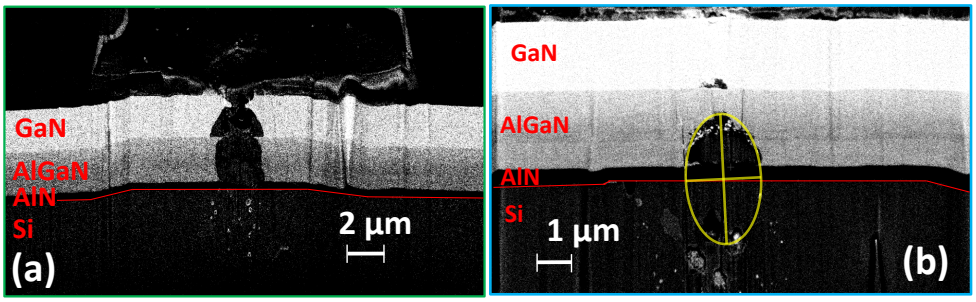

Figure 188 : Observation en coupe au FIB-SEM (capteur ESB): (a) du lieu de claquage (d) un peu plus loin.

H

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- Dans un second temps, l'étude des composants claqués avec le substrat flottant révèle que les composants ont une plus haute tension de claquage que la limite verticale précédemment étudiée. Cela suggère que le substrat s'auto-polarise pour empêcher que la tension entre le substrat et la cathode n'atteigne 1000 V lorsque la tension appliquée sur le composant (entre l'anode et la cathode) dépasse 1000 V. Ensuite en faisant varier la distance entre l'anode et la cathode et en regardant l'évolution de la tenue en tension, deux régimes ont pu être identifiés :

    - Le premier régime correspond à une dépendance linéaire de la tenue en tension en fonction de la distance entre les deux électrodes. Ce régime est visible lorsque la distance entre l'anode et la cathode est courte. Une étude en température de la tension de claquage, a permis deux choses. La première est de mettre de côté l'hypothèse d'un claquage par avalanche. En effet la tenue en tension diminue avec la température (non montré ici) alors que l'inverse serait observé avec un phénomène d'avalanche. La deuxième est que quand la tension de claquage diminue avec la température, la puissance dissipée lors du claquage diminue ce qui réduit la taille de la zone détruite. Dès lors l'observation du lieu de claquage par des observations détaillées par la suite est rendu possible. Cela a notamment pu être possible par une identification du lieu approximatif par caméra thermique comme montré sur la **Figure 189(a)** puis à l'aide de la microscopie électronique (FIB-SEM) comme montré sur la **Figure 189(b)**. Pour la première fois sur une diode Schottky latérale en nitrure de gallium, l'observation d'un claquage diélectrique entre la première plaque de champ et l'hétérojonction a pu être mise en avant. L'étude de la dépendance de ce claquage en fonction de l'épitaxie et du « layout » montre tout d'abord qu'une couche barrière enterrée plus proche de l'hétérojonction est favorable à une plus haute tenue en tension comme montré en comparant l'épitaxie 1 et 2 sur la **Figure 190(a)** probablement dû à l'effet ReSurf (Reduced Surface electric field). Ensuite, il est suggéré qu'avec les distances entre les plaques de champs et l'hétérojonction, des longueurs de plaque de champ en dessous du micromètre peuvent être envisagées pour avoir une meilleure tenue en tension comme montrée sur la **Figure 190(b)**. En effet, on peut voir qu'en réduisant la somme des longueurs des quatres plaques de champ, la tension de claquage augmente.

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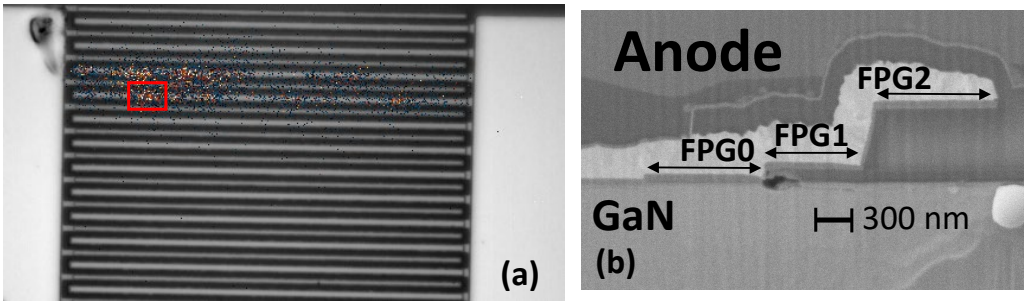

Figure 189 : (a) Observation avec la caméra thermique sous une tension inverse de 0.3 V (6.6 mA), fréquence de 25 Hz avec un temps d'intégration de 3 min (superposition entre l'image du microscope et le signal d'amplitude de la caméra thermique) d'un composant cassé (avec un "layout" FPG0-1 sur une épitaxie 1 à 175°C) (b) Observation en coupe avec le FIB-SEM (capteur SESI) de la zone encadrée en rouge sur la figure de gauche (a).

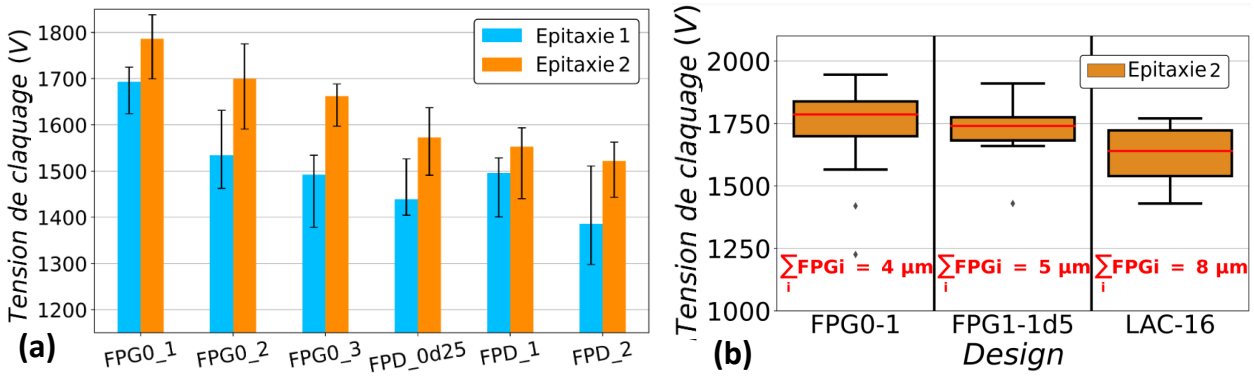

Figure 190 : (a) Tension de claquage du composant en fonction du "layout" pour les épitaxies 1 et 2 (seize composants testés et barres d'erreurs représentant le premier et troisième quartile) (b) Tension de claquage du composant en fonction de la somme des longueurs de plaque de champ (FPG0-1: 4 µm; FPG1-1d5: 5 µm and LAC-16: 8 µm) sur l'épitaxie 2.

- Le second régime correspond à une indépendance ou saturation de la tenue en tension en fonction de la distance entre les deux électrodes. Ce claquage a été caractérisé de la même manière que le régime précédent avec une étude en température. La tendance en température étant similaire, les mêmes observations, conclusions (réduction de la taille détruite avec la température et claquage non associé à un mécanisme d'avalanche) et protocoles d'analyse de défaillances proposés ont été similaires. Le lieu de claquage a dès lors pu être approximativement discerné à l'aide de caméra thermique comme montré sur la **Figure 191(a)**. Par la suite, des observations au microscope électronique (FIB-SEM) ont pu mettre en avant un claquage diélectrique entre le coin de la seconde plaque de champ et l'hétérojonction comme on peut le voir sur la **Figure 191(b)**. Cette observation nuance l'hypothèse proposée dans la littérature de claquage vertical sous l'anode par Visalli *et al.* [241], Shen *et al.* [240] et Jiang *et al.* [238].

J

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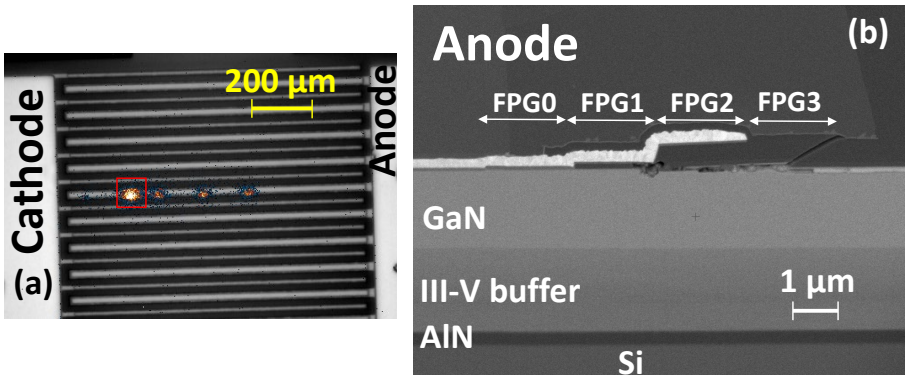

Figure 191 : (a) Observation à la caméra thermique à une tension inverse 1.5 V (1 mA), frequence de 25 Hz avec un temps d'intégration de 2 min 30 s (superposition entre l'image du microscope et le signal d'amplitude de la caméra thermique) d'un composant cassé (avec un "layout" LAC-30 sur une épitaxie 1 à 175°C) (b) Observation en coupe avec le FIB-SEM (capteur ESB) de la zone encadrée en rouge sur la figure de gauche (a).

† Chapitre 3: Amélioration de la modélisation TCAD de la diode Schottky AlGaN/GaN basée sur des mesures expérimentales

Pour étudier le champ électrique en simulation TCAD et réaliser une optimisation de la tenue en tension, il est nécessaire de développer une méthode afin de calibrer les propriétés (concentrations, niveau d'énergie et section de capture) des pièges présents dans les couches du buffer. La méthode initiée pendant cette thèse se base sur trois mesures différentes développées par la suite. Deux d'entre elles sont basées sur la réponse capacitive du composant. En effet, la réponse capacitive et le champ électrique sont deux grandeurs corrélées car les deux sont dépendentes de la désertion progressive du 2DEG (de l'anode à la cathode ou de la grille au drain) dans le composant. Pour s'en convaincre, Weiss *et al.* [148] ont tout d'abord démontré que la caractéristique capacitive non-linéaire de la diode était due aux différents couplages électrostatiques entre le 2DEG et les plaques de champ suivant la déplétion progressive de ce dernier. Ceci est aussi valable pour les capacités de Miller et de sortie du transistor de part la similarité structurelle des deux composants. Ensuite comme on peut le voir sur la **Figure 192(a), (b), (c), (d)** et **(e)**, les équipotentielles suivent la désertion progressive du 2DEG. Le potentiel électrostatique étant relié au champ électrique (par la relation $\vec{E} = -\overrightarrow{grad}(V)$ et par conséquent, on peut constater au milieu de la **Figure 192(f)** et **(g)** que le champ électrique est plus important quant les équipotentielles se rapprochent), on peut donc en déduire que le champ électrique est relié

K

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à la désertion du 2DEG. Quant à la dernière mesure, il s'agit d'étudier la dépendance en température du courant vertical afin de mettre en avant des pièges pouvant jouer sur la distribution du champ électrique de part la présence locale de courant de fuite.

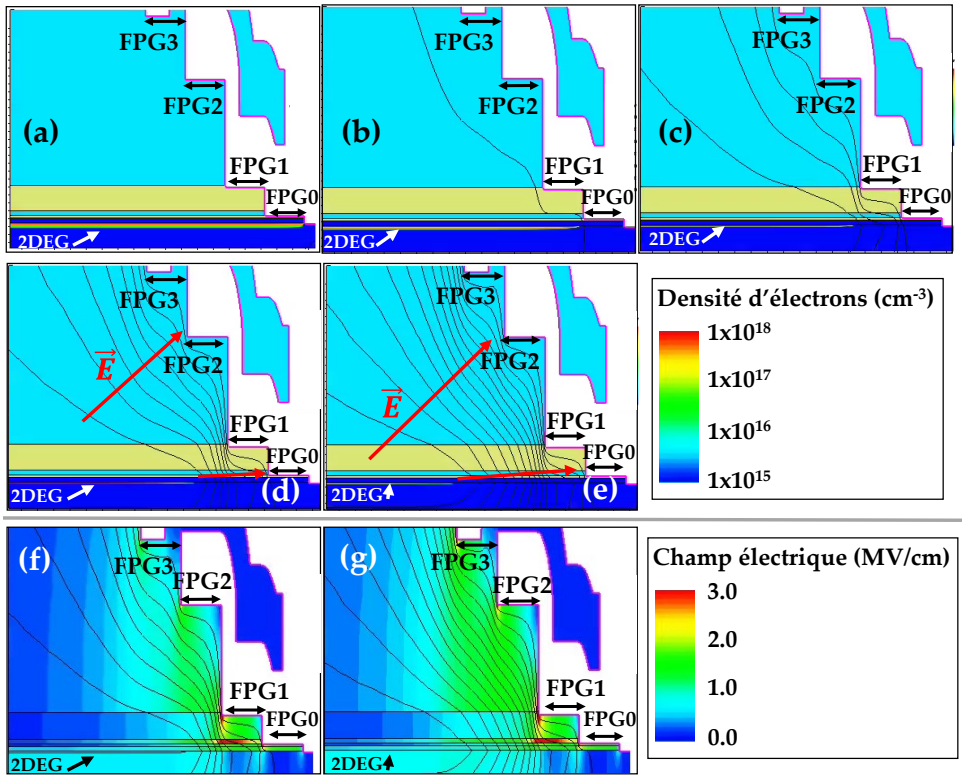

Figure 192 : Cartographie de la densité d'électrons simulée (avec les équipotentielles superposées) en fonction de la polarisation inverse appliquée : (a) 0.5 V ; (b) 15 V ; (c) 40 V ; (d) 80 V ; (e) 125 V sur une diode générique avec le substrat connecté à l'anode. Cartographie de la distribution du champ électrique (avec les équipotentielles superposées) en fonction de la polarisation inverse appliquée : (f) 80 V ; (g) 125 V sur la même diode générique.

Voici un résumé des différents résultats obtenus :

1. L'étude en température de la capacité de Miller ($C_{RSS} = C_{GD}$) des transistors réalisée à partir de mesures expérimentales et de simulations TCAD (analyse qualitative puis « fit » sur les courbes expérimentales (**Figure 193**)) a permis d'identifier des pièges profonds de type accepteurs dans l'épitaxie (sauf sur les dernières centaines de nanomètres) avec leurs propriétés (energie par rapport à la bande de valence : E_T-E_V ; section de capture des trous : σ_{A,h^+}) dans le cas où ils sont employés avec des pièges de type donneurs (E_C-E_T = 0.11 eV, $\sigma_{D,e^-} = 1\times10^{-15}$ cm^2) :

L

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- La différence de concentration entre les pièges de type donneurs et accepteurs est de : [A] – [D] = 1×10^{17} cm^{-3}.
- Les pièges de type accepteurs sont associés à des lacunes de gallium avec un/des atomes d'oxygène en site azote (V_{Ga}-$(O_N)_x$). Cette hypothèse a été proposée en comparant les propriétés (E_T-E_V = 1.1 eV, σ_{A,h^+} = 1×10^{-13} cm^2) extraites des "fit" en TCAD avec les pièges reportés dans la littérature comme montré sur la **Figure 194** et en fixant leur concentration avec celle de l'oxygène mesurée expérimentalement ([A] = 1 a.u dans les couches en AlGaN du buffer et [A] = 0.5 a.u dans le GaN:C).

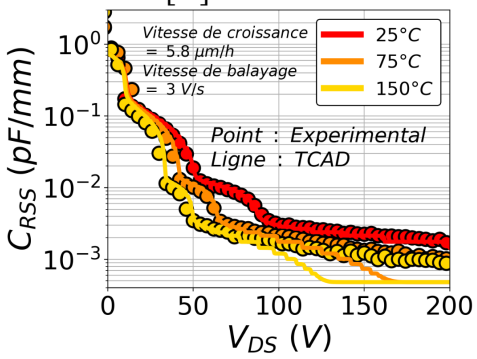

Figure 193 : Simulation TCAD calibrée pour correspondre aux mesures expérimentales (Vitesse de croissance du GaN:C de 5.8 µm/h et vitesse de balayage de 3 V/s) [301]. Les simulations ont été lancées avec une concentration de pièges accepteurs : [A] égal à 1 a.u. dans le buffer en $Al_xGa_{1-x}N$ et à 0.5 a.u. dans le GaN sauf dans les derniers 200 nm. De plus [A] - [D] = 1×10^{17} cm^{-3} ; E_A-E_V = 1.1 eV et σ_{A,h^+} = 1×10^{-13} cm^2.

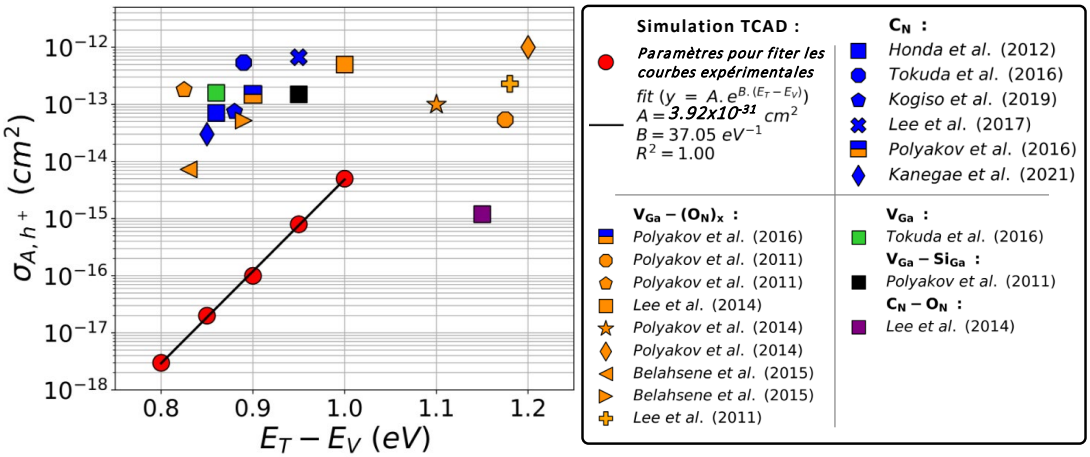

Figure 194 : Section de capture des pièges de type accepteurs en fonction de leur position dans la bande interdite (Niveau d'énergie entre 0.8 et 1.2 eV par rapport à la bande de valence) [301]. Chaque couleur proposée par les auteurs [289], [313]–[321] correspond à un défaut (C_N : Carbone en site azote ; V_{Ga}-$(O_N)_x$: Lacune de gallium avec un/des atome(s) d'oxygène en site azote ; V_{Ga} : Lacune de gallium ; V_{Ga}-Si_{Ga} : Lacune de gallium avec un atome de silicium en site gallium; C_N-O_N : Carbone en site azote avec un atome d'oxygène dans un autre site azote).

M

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2. L'étude expérimentale et en simulation TCAD des fuites verticales en température révèle que :

   - Deux pièges sont responsables de la fuite verticale : des pièges associés à des dislocations avec un agrégat de défauts ponctuels comme les lacunes de gallium V_{Ga} seule ou de paire avec des lacunes d'azote V_N (E_T = 0.27 eV) à faible tension et température (limité par la recombinaison dans la **Figure 195**) et de l'azote en site interstitiel (E_T = 0.75-0.76 eV) à haute tension et pour toutes les températures (conduction ohmique et par saut dans la **Figure 195**).
   - A la fin de cette thèse, la modélisation TCAD de ces fuites est limitée par la modélisation de l'interface AlN/Si pour reproduire le comportement expérimental.

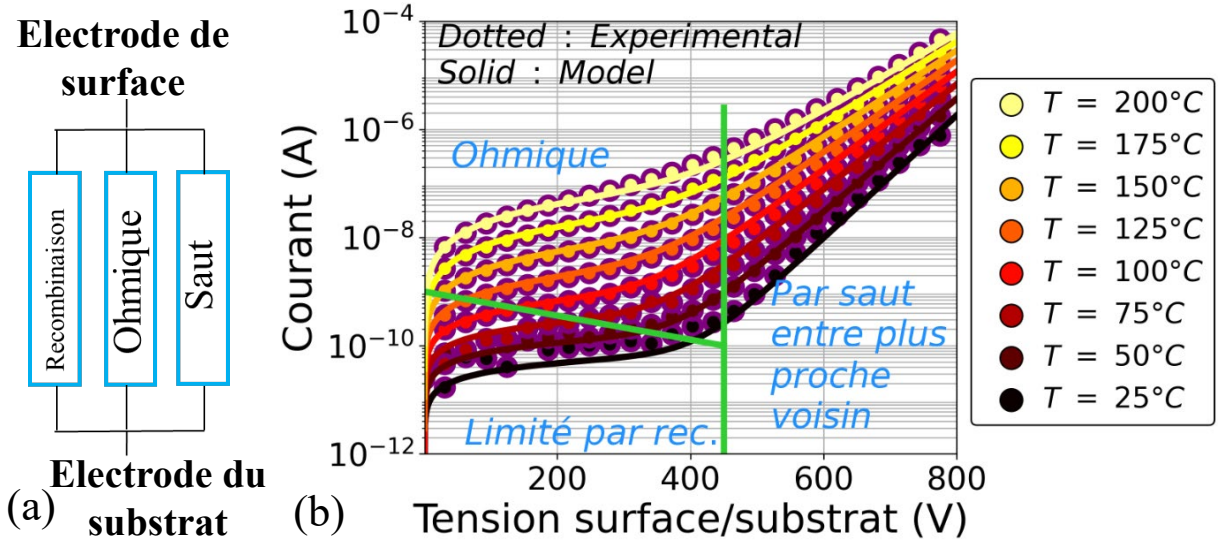

Figure 195 : (a) Contribution en parallèle des trois différents mécanismes de transport responsables de la fuite verticale [343] (b) Correspondance entre le modèle et les mesures expérimentales [343].

3. L'étude en DLTFS (Deep Level Transient Spectroscopy) réalisée sur des échantillons ayant des recettes de gravure du contact Schottky différentes ont révélé deux nouveaux pièges de type donneurs associés à la gravure (E_C-E_T = 0.47-0.48 ou 0.57 eV) et d'autres pièges de type donneurs déjà détectés dans la littérature ont été détecté dans la gamme [0.40, 0.56] eV comme résumé dans la **TABLE 25**. Ces derniers sont possiblement associés pour certains à la compensation des pièges de type accepteurs. Malheureusement, cet axe de recherche n'a pas pu être poussé plus loin lors de cette thèse pour des raisons de temps.

N

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TABLE 25 : Différentes catégories de pièges type donneurs D_i ($i \in [|1,7|]$) basées sur l'énergie et les sections de capture extraites des graphiques d'Arrhenius pour les deux échantillons (LV 90 V and LV 237 V) et les différentes conditions de polarisation (V_P, V_R) (table adaptée de [358]). La dernière ligne résume les différentes hypothèses proposées par l'auteur de ce manuscrit pour chaque catégorie suite à la discussion dans le paragraphe III.4.c.

		D1		D2		D3		D4		D5		D6		D7	
		E_T (eV)	σ (cm²)	E_T (eV)	σ (cm²)	E_T (eV)	σ (cm²)	E_T (eV)	σ (cm²)	E_T (eV)	σ (cm²)	E_T (eV)	σ (cm²)	E_T (eV)	σ (cm²)
V_P = -0.1 V	LV 237 V									0.53	1.55×10^{-13}				
V_R = -10 V	LV 90 V													0.57	4.45×10^{-12}
V_P = -0.1 V	LV 237 V							0.50	1.73×10^{-13}						
V_R = -20 V	LV 90 V							0.49	7.58×10^{-15}	0.54	2.85×10^{-13}				
V_P = 0 V	LV 237 V					0.48	5.90×10^{-16}	0.51	1.56×10^{-13}						
V_R = -50 V	LV 90 V			0.46	2.56×10^{-13}					0.52	1.49×10^{-14}				
V_P = 0 V	LV 237 V					0.47	7.14×10^{-16}					0.55	4.33×10^{-15}		
V_R = -70 V	LV 90 V											0.55	1.39×10^{-14}		
V_P = 0 V	LV 237 V	0.40	7.98×10^{-18}			0.47	1.13×10^{-15}					0.55	4.21×10^{-15}		
V_R = -90 V	LV 90 V											0.56	1.59×10^{-14}		
Hypothèse proposée		C_{Ga}-V_N		Recombinaison de surface		Associé à la gravure		Défaut natif ou complexe associé		C_N-C_{Ga}		N_{Ga}		Associé à la gravure	

Enfin, toutes ces études ont permis de mettre en évidence que les accepteurs des couches du « buffer » jouent au premier ordre sur l'aspect capacitif du composant mais la modélisation TCAD du composant n'a pas abouti pour reproduire les variations expérimentales de tenue en tension (non montré dans ce résumé). En effet, l'aspect résistif (par les fuites) n'a pas abouti par manque de temps car la modélisation TCAD des fuites verticales (en nottament de l'interface AlN/Si) nécessites plus d'étude expérimentales comme développé dans les perspectives.

O

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† Chapitre 4 : Evaluation des pertes en commutation dures des transistors latéraux AlGaN/GaN avec grille MOS gravé coupant le 2DEG

L'étude des pertes en commutation est une étape importante pour optimiser le design de composants afin de réduire ces dernières. Identifier les paramètres jouant sur ces dernières est donc crucial. Dans cette thèse, il a été proposé d'étudier dans un premier temps comment la profondeur de gravure de grille impactait les pertes en commutation dure. Cette étude a été réalisée sur des transistors 650 V/30 A développés au CEA LETI et packagés dans un DFN (Dual Flat No Lead). Dans un second temps, certains paramètres de « layout » (longueur de grille, distance grille/drain, longueur de plaque de champ de grille, source et présence de trous de source) ont été testés sur les pertes en commutation dure. Cette étude a été réalisée quant à elle, sur des transistors de petite taille (L_{GD} autour de 8 µm) 650 V/1 A développés au CEA LETI et packagés dans un DFN (Dual Flat No Lead). Ces deux études ont été faites au Laboratoire Ampère, sur un banc développé pendant cette thèse. Le banc expérimental reproduit le fonctionnement Double Source comme précisé dans l'introduction. Pour étayer l'analyse, des simulations sur LTSpice et en TCAD ont été lancées et utilisées. Voici les résultats importants rapportés durant cette thèse :

- L'étude de la profondeur de recess révèle que plus la gravure est profonde (par rapport au 2DEG comme illustré sur la **Figure 196(a)**), plus les pertes lors du passage à l'état passant sont importantes (comme l'illustre la **Figure 196(b)** et **(c)**).

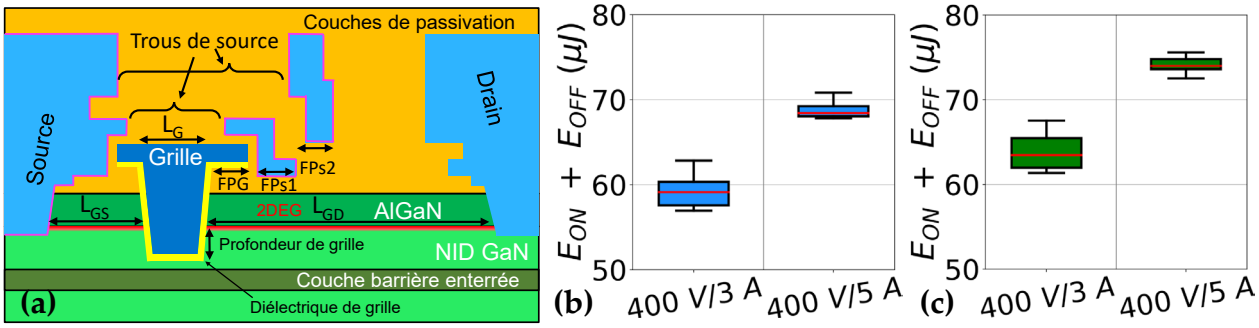

Figure 196 : (a) Schéma de la vue en coupe d'un transistor à grille MOS peu profonde coupant le 2DEG (b) Pertes en commutation dure ($E_{OFF} + E_{ON}$) des transistors 650 V/30 A avec une grille (a) peu profonde (8 composants testés) et (b) profonde (6 composants testés).

P

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Afin de comprendre l'origine de cette différence, le modèle LTSpice développé pour les transistors de puissance au CEA LETI a été utilisé après l'avoir adapté pour les besoins de la thèse. Cette adaptation a notamment été nécessaire pour que le modèle corresponde aux mesures de calibration (non détaillées ici) qui ont été choisies et réalisées durant cette thèse.

Dans un premier temps, le modèle a été calibré pour les deux profondeurs de grille étudiées sur les caractéristiques du transistor suivantes : transfert ($I_D(V_{GS})$ en direct), sortie ($I_D(V_{DS})$ en direct), blocage ($I_D(V_{DS})$ en blocage), capacité de sortie ($C_{OSS}(V_{DS})$ en blocage), d'entrée ($C_{ISS}(V_{DS})$ en blocage) et de recouvrement ($C_{RSS}(V_{DS})$ en blocage). Ceci donnant deux jeux de paramètres différents nommés "std". Les paramètres qui diffèrent entre les deux ont été identifiés et groupés lorsqu'ils modifiaient la même partie de courbe. Suite à cela, différents jeux de paramètres ont pu être créés pour passer progressivement du modèle correspondant à la gravure peu profonde à la gravure profonde. En comparant les pertes en commutations dures simulées (comme illustrée sur la **Figure 197**), il a pu être déterminé que la différence de tension de seuil et de plateau à haute tension de la capacité $C_{GD}(C_{RSS})$ (mise en avant sur la **Figure 198(a)**), entre les différentes profondeurs de gravure, était responsable de la différence de pertes.

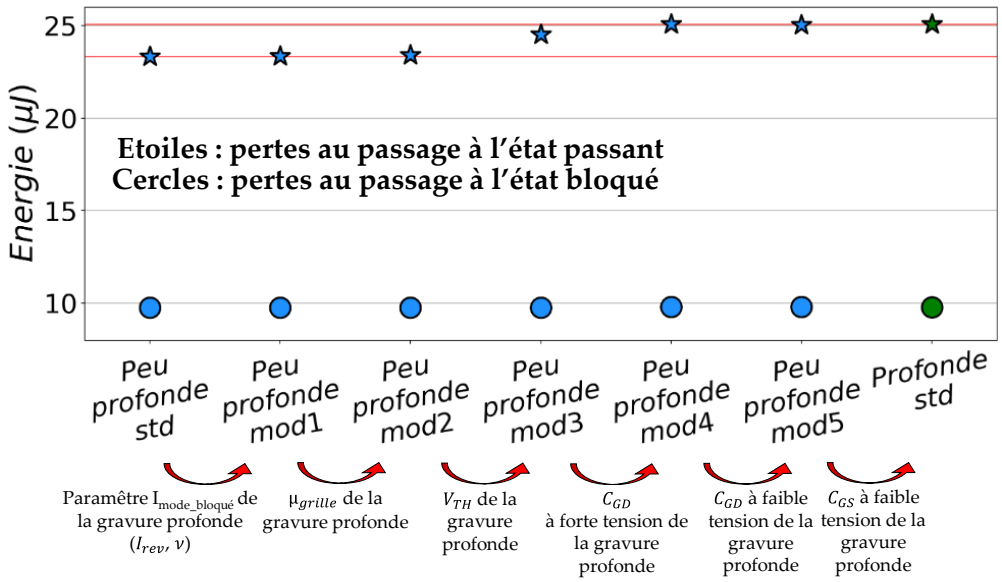

Figure 197 : Pertes en commutation dure simulées sur LTSpice avec un modèle de transistor partant et finissant avec des paramètres « fités » sur les courbes expérimentales des différentes gravures (nommée "std") et passant par un modèle intermédiaire changeant progressivement les paramètres pour passer de l'un à l'autre. Les jeux de paramètres intermédiaires sont appelés : modi avec i Є [|1, 5|].

Q

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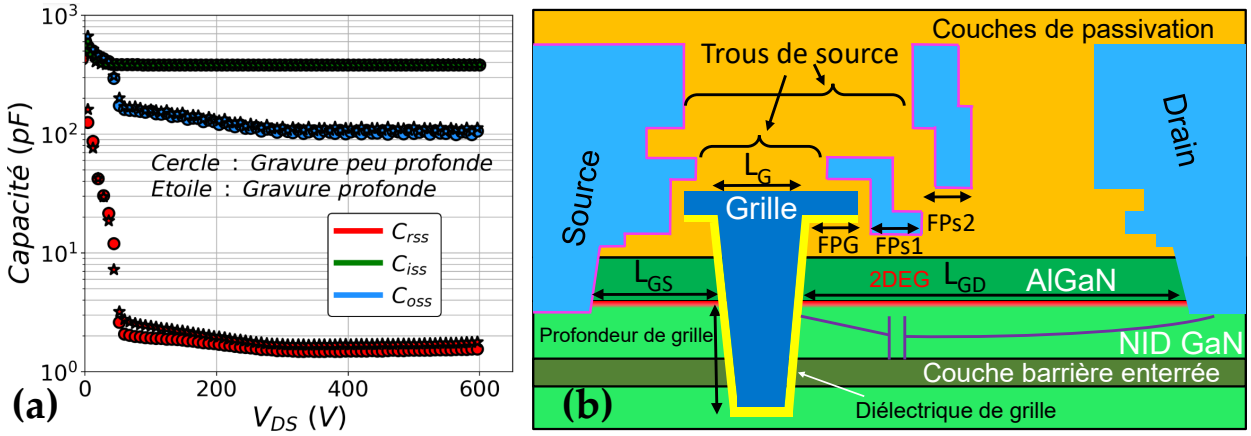

Figure 198 : (a) Caractéristique capacitive (C_{OSS}, C_{RSS}, C_{ISS}) en blocage à 25°C pour les deux profondeurs de gravure étudiées (b) Schéma de la vue en coupe d'un transistor à grille MOS profonde coupant le 2DEG avec la capacité résiduelle C_{GD} à haute tension en violet.

La différence de capacité à haute tension vient surement de la différence de surface de la capacité de frange illustrée en violet sur la **Figure 198(b)**. Tandis que la différence de tension de seuil est le résultat d'une différence de distance entre le contact MOS au fond de la gravure et des accepteurs (identifiés dans le chapitre 3) se situant dans les couches du « buffer ».

- L'étude de l'impact des choix de layout a pu être mené sur la variations de la longueur de la grille. L'étude révèle que les pertes au passage à l'état passant sont légèrement réduites lorsque la longueur de grille est réduite comme le montre la **Figure 199(a)**. Ceci est probablement dû à la différence de tension de seuil comme on peut le voir avec la corrélation entre ces deux grandeurs sur la **Figure 199(b)**. Cette différence est due à un effet de canal court appelé le « V_{TH} roll-off ».

Néanmoins comme on peut le voir sur la **Figure 199(d)** et non sur la **(c)**, les oscillations de grille sont augmentées lorsque la longueur de grille diminue. Il faut donc modérer l'avantage sur les pertes souligné par l'étude. En effet des oscillations de grille trop conséquentes pourraient s'avérer préjudiciables pour la stabilité des commutations (les fortes tensions pourraient à minima changer la tension de seuil et ainsi changer son comportement aux tensions de commande données).

R

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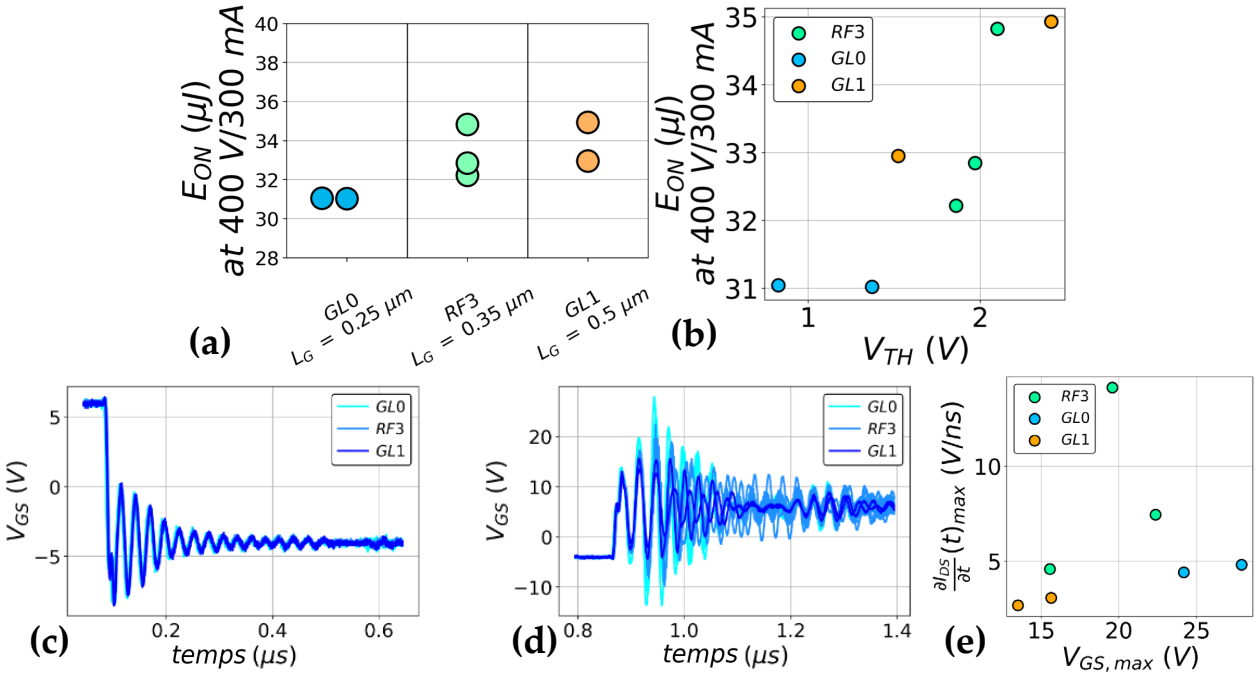

Figure 199 : Pertes experimentales lors du passage à l'état passant en fonction (a) du "layout" du composant (b) de la tension de seuil (V_{TH}) avant les tests; Tension de grille mesurée lors de la commutation dure (c) au passage à l'état off (d) au passage à l'état on; (e) Maximum de la dérivée temporelle expérimentale de la mesure de la tension drain-source (V_{DS}) en fonction de la tension maximale mesurée entre la grille et la source (V_{GS}).

TABLE 26 : Table référençant les différentes variations de "layout" étudiés.

Nom de "layout"	L_G (µm)	L_{GD} (µm)	Source holes	FPG (µm)	FPs1 (µm)	FPs2 (µm)
RF3	0.35	8	Yes	0.5	1.0	1.5
GF1	0.35	8	Yes	0.75	1.0	1.5
GF3	0.35	8	Yes	2	1.0	1.5
GL0	0.25	8	Yes	0.5	1.0	1.5
GL1	0.5	8	Yes	0.5	1.0	1.5
GX2	0.35	7	Yes	0.5	1.0	1.5
GX5	0.35	10	Yes	0.5	1.0	1.5
GG3	0.35	8	No	0.5	1.0	1.5
GG5	0.35	8	No	0.5	1.0	0.0
GG6	0.35	8	No	0.5	0.75	0.0
GG7	0.35	8	No	0.5	0.5	0.0

S

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L'étude sur l'impact du layout n'a cependant pas pu être effectuée sur les paramètres restant de la **TABLE 26**. En effet, comme on peut le voir sur la **Figure 200(a)**, peu de composants étaient fonctionnels (en vert) pour le test en commutation dure. En effet, dans un premier temps, l'étape de mise en boitier s'est révélée préjudiciable pour les composants. L'analyse de l'impact de la distance entre les métaux de source et de drain sur la **Figure 200(b)** et **(c)**, suggère que c'est le paramètre responsable de la casse lors de cette étape mais aussi que cette dernière est responsable du nombre de transistors fonctionnels restants car elle suit la tendance inverse par rapport à ce paramètre. La criticité de ce paramètre peut être réduite en arrondissant les coins des métaux si le problème venait d'un effet de pointe. Dans un second temps, l'allumage des commandes de grille (en jaune sur la **Figure 200(a)**) s'est aussi montré intransigeant. Les perturbations (décharges électrostatiques) engendrées sur la tension de grille ont dues être critiques pour ces composants de par leurs faibles tailles (transistors 1A). Dans un troisième temps, lors du test Double Source, la tension appliquée à l'état passant sur certains layouts (GG3, GG7, GG6, GX5, GF3) n'a pas pu atteindre les 6 V nominaux. Cela empêche le composant d'être faiblement résistif et donc limite son utilisation. Cela ne vient ni d'une fuite de grille (testée après commutation), ni du layout. Ce problème n'a pas pu être résolu mais il est certain qu'il mérite plus d'attention à l'avenir.

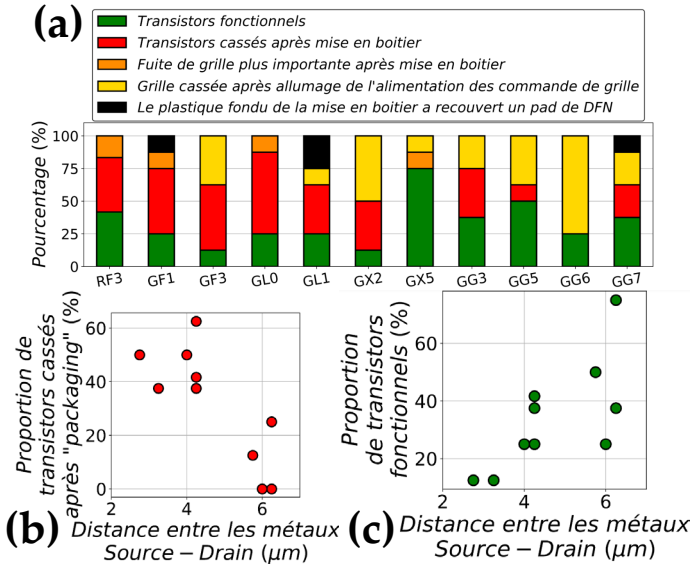

Figure 200 : (a) Proportion des différents état des transistors juste avant la commutation pour chaque "layout" de transistors (8 composants par "layout") ; Proportion des (b) cassés après mise en boitier et (c) fonctionnels en fonction de la distance entre les métaux de source et de drain (correspondant à L_{GD} - (FPG + FPs1 + FPs2 + FPd1 + FPd2 + FPd3)).

T

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† Conclusion et perspectives

Pour finir, nous avons vu que le nitrure de gallium est un semi-conducteur à grande largeur de bande interdite intéressant pour l'électronique de puissance grâce son fort champ de claquage et ses propriétés polaires (polarisations spontanée et piézoélectrique). Avec ce matériau, des diodes Schottky et des transistors à enrichissement latéraux peuvent être fabriqués. Ces transistors se démarquent des transistors MOSFET SiC et à superjonction en silicium grâce à leur meilleures figures de mérite : $R_{ON} \times C_{OSS}$, $R_{ON} \times Q_G$ [96]. Ils sont dès lors destinés à des applications domestiques (chargeurs de téléphone), aux voitures électriques, au photovoltaïque, à l'industrie ou encore à l'aéronautique, dans des convertisseurs ayant une puissance de sortie comprise entre 0.01 et 10 kW et une fréquence de commutation allant de 10 kHz à 10 MHz [125]. Pour optimiser les performances du convertisseur, il est nécessaire d'améliorer les performances du composant (qui ne sont pas optimales aujourd'hui sur la figure de mérite R_{ON} vs BV). Diminuer la taille des composants est une approche permettant de réduire le R_{ON} (en réduisant la résistance du chemin de conduction et l'encombrement sur le wafer) et possiblement de réduire les pertes (en augmentant la vitesse de commutation) mais nécessitant d'optimiser la distribution du champ électrique et de vérifier si la stabilité de la commutation n'est pas altérée par l'augmentation des effets parasites.

Dans un premier temps, un statut des limites de tenue en tension des diodes Schottky 650 V/6 A (véhicules de test) a été établi. Cela a été réalisé à partir d'études sur la tension de claquage en fonction de la connexion du substrat, du « layout » et de l'épitaxie mais aussi de techniques d'analyses de défaillance tel que la thermographie et les observations FIB-SEM. Ces études ont permis de mettre en avant un claquage vertical à l'interface AlN (couche de nucléation)/Si (substrat) lorsque le substrat est connecté (configuration la plus utilisée aujourd'hui et c'est la première fois que le claquage est observé physiquement) pour toutes les tailles de composants disponibles ce qui limite l'étude du champ électrique dans ce cas. Avec le substrat flottant, les composants sont limités latéralement quelle que soit la distance entre les électrodes, par un claquage diélectrique à l'extrémité des plaques de champ (première plaque de champ pour les petits composants (L_{AC} = 16 µm) et deuxième pour les longs (L_{AC} = 30 µm)). Ces observations nuancent l'hypothèse de l'état de l'art : une limite verticale pour les composants longs (caractérisées par une saturation de la tenue en tension en augmentant la distance anode/cathode).

U

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A l'avenir, une étude sur des composants plus petit limités latéralement semble être plus judicieuce sachant que cela n'a pas pu se faire durant la thèse (l'auto-polarisation du substrat ne sera pas présente ce qui fait une inconnue de moins pour le parallèle avec les simulations TCAD).

Dans un deuxième temps, la modélisation TCAD des diodes Schottky a été améliorée à partir de mesures capacitives et de fuites afin de prendre en compte les pièges jouant sur ces caractéristiques et pouvant influencer la distribution du champ électrique :

- L'étude expérimentale et en simulation TCAD de la capacité en température et en blocage (réalisée sur des transistors) a permis d'identifier des pièges profonds de type accepteurs dans l'épitaxie sauf sur les dernières centaines de nanomètres avec leurs propriétés (E_T-E_V = 1.1 eV, $\sigma_{A,h^+} = 1\times10^{-13}$ cm^2) dans le cas où ils sont employés avec des pièges de type donneurs dont les caractéristiques sont tirées de la littérature. Ces pièges de type accepteurs sont associés à des lacunes de gallium avec un/des atomes d'oxygène en site azote (V_{Ga}-$(O_N)_x$),
- L'étude expérimentale et en simulation TCAD des fuites verticales en température a mis en évidence deux pièges associés soit à des dislocations avec un agrégat de défauts ponctuels comme les lacunes de gallium V_{Ga} seules ou de pair avec des lacunes d'azote V_N (E_T = 0.27 eV) pour les fuites à faible tension et faible température, soit à de l'azote en site interstitiel (E_T = 0.75-0.76 eV) pour le reste de la caractéristiques de fuite. Néanmoins, la modélisation TCAD de ces fuites reste limitée par la modélisation de l'interface AlN/Si pour reproduire le comportement expérimental,
- L'étude DLTFS (Deep Level Transient Spectroscopy) réalisée sur des échantillons ayant des recettes de gravure du contact Schottky différentes ont révélé deux nouveaux pièges de type donneurs associés à la gravure (E_C-E_T = 0.47-0.48 ou 0.57 eV) et d'autres pièges de type donneurs déjà détectés dans la littérature ont été détectés dans la gamme [0.40, 0.56] eV. Certains sont possiblement associés à la compensation des pièges de type accepteurs (vu deux points auparavant). Ce point nécessite d'être poussé plus loin lors d'études futures.

→ Toutes ces études ont permis de mettre en évidence que les accepteurs des couches du « buffer » jouent au premier ordre sur l'aspect capacitif du composant. Néanmoins la modélisation TCAD du composant n'est pas aboutie pour reproduire les variations expérimentales de la tenue en tension (non montré dans le résumé). En effet, l'aspect résistif (par les fuites) n'a pas abouti. Des études expérimentales des fuites verticales sont donc nécessaires pour nottament mieux modéliser l'interface AlN/Si. Il est proposé de faire varier les paramètres de croissance des différentes couches d'épitaxie (notamment la couche de nucléation) pour en apprendre plus.

Dans un dernier temps, les pertes en commutation dure ont été étudiées expérimentalement pour comprendre comment les choix de procédés utilisés lors de la fabrication des transistors et les paramètres « layout » impactent ces dernières. Il faut savoir que ce travail n'a jamais été fait sur

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des composants à grille MOS qui coupe le 2DEG. Des outils de simulation tels que LTSpice et TCAD ont été utilisés pour compléter l'analyse. Voici les différents points mis en avant :

- L'étude de la profondeur de gravure de la grille montre que plus la gravure est profonde par rapport au 2DEG, plus les pertes lors du passage à l'état passant sont importantes. En modélisant les transistors avec leurs caractéristiques (courant en direct et en blocage et capacité en blocage) mesurées avant commutation pour les deux profondeurs de gravure en comparant des modèles intermédiaires sur les pertes, il a été montré que la tension de seuil V_{TH} (différence due selon les simulations TCAD à la proximité du fond de la grille avec les accepteurs du buffer) ainsi que la capacité de Miller à haute tension (due au couplage plus important avec les flancs de gravure lors d'une gravure profonde) étaient responsables de la différence de pertes entre les deux profondeurs de gravure.

- L'étude de l'impact des choix de layout a pu être menée sur la variation de la longueur de la plaque de champ de grille. L'étude révèle que les pertes au passage à l'état passant sont légèrement réduites lorsque la longueur de grille est diminuée. Ceci est probablement dû à la différence de tension de seuil (due à un effet de canal court). Malheuresement, cette étude n'a pas pu être effectuée sur les paramètres restants (Longueur de plaque de champ de grille et de source, distance grille/drain et présence d'un trou de l'électrode de source au-dessus de la grille). En effet, peu de composants étaient fonctionnels pour le test en commutation dure dû à :

  - L'étape de mise en boitier qui est sensible à la distance entre les métaux de source et de drain.
    → La criticité de ce paramètre pourra à l'avenir être réduite en arrondissant les coins des métaux si le problème venait d'un effet de pointe.

  - L'allumage des commandes de grille qui engendre potentiellement des décharges électrostatique critiques pour la grille des petits composants (1 A) testés.
    → Une potentielle amélioration de la commande pourrait éliminer ce point

→ Pour finir, sur l'aspect scientifique, certains « layouts » n'ont pas pu atteindre les 6 V nominaux. Ce problème n'a pas pu être résolu mais il est certain qu'il mérite plus d'attention à l'avenir nottament en vérifiant si cela ne peut pas venir de couplage croisé avec des essais avec les simulation LTSpice ou en envisageant des simulations mixtes (TCAD et LTSpice).

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Author's Bibliography:

† **Peer-reviewed journal's articles:**

- **Florian Rigaud-Minet**, Julien Buckley, William Vandendaele, Matthew Charles, Marie-Anne Jaud, Elise Rémont, Hervé Morel, Dominique Planson, Romain Gwoziecki, Charlotte Gillot, Véronique Sousa, 'Capacitance Temperature Dependence Analysis of GaN-on-Si Power Transistors'. *Energies* 15, no. 19 (26 September 2022): 7062. https://doi.org/10.3390/en15197062.

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- **Florian Rigaud-Minet**, Julien Buckley, William Vandendaele, Stéphane Bécu, Matthew Charles, Jérôme Biscarrat, Romain Gwoziecki, Charlotte Gillot, Véronique Sousa, Hervé Morel, Dominique Planson 'Vertical Current Temperature Analysis of GaN on Si Epitaxy through Analytical Modelling'. Solid States Devices & Materials (SSDM) 2022, Chiba (Japan), September 2022. https://confit.atlas.jp/guide/organizer/ssdm/events (not available during the PhD) or in https://hal-cea.archives-ouvertes.fr/LETI/cea-03875079v1 (not available during the PhD).

- (Invited Speaker) Blend Mohamad, Cyrille Le Royer, **Florian Rigaud-Minet**, Clemence Piotrowicz, Pedro Fernandes Paes Pinto Rocha, Camille Leurquin, William Vandendaele, René Escoffier, Julien Buckley, Stéphane Bécu, Jérôme Biscarrat, Romain Gwoziecki, 'Deep Insights of MIS-HEMT technology developments for power applications: Towards Industrialization', Seoul (Korea), March 2023. https://ewh.ieee.org/conf/edtm/2023/program/plenary.html

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† **Conference abstract + oral presentation:**

- Julien Buckley, René Escoffier, Stéphane Bécu, Jérôme Biscarrat, Murielle Fayolle-Lecocq, Blend Mohamad, **Florian Rigaud-Minet**, Matthew Charles, Laura Vauche, Cyrille Le Royer, Marie-Anne Jaud, William Vandendaele, Romain Gwoziecki, Charlotte Gillot, Marc Plissonnier, Véronique Sousa 'Lateral Gallium Nitride Power Diodes and MOS Channel Transistor on 200 mm CMOS platform'. 6th International Conference on Advanced Electromaterials (ICAE 2021), Jeju (Korea), November 2021.

- Julien Buckley, René Escoffier, Blend Mohamad, Stéphane Bécu, Jérôme Biscarrat, **Florian Rigaud-Minet**, Laura Vauche, Vishwajeet Maurya, Matthew Charles, Helge Haas, Murielle Fayolle Lecocq, Jérémy Martin, Van Sang Nguyen, Cyrille Le Royer, Romain Gwoziecki, Charlotte Gillot, Véronique Sousa. 'Gallium Nitride Power Devices for Power Conversion Applications'. International Conference on Electronic Materials and Nanotechnology for Green Environment (ENGE 2022), Jeju (Korea), November 2022.

† **Issued patents:**

- **Florian Rigaud-Minet**. HETEROJUNCTION ELECTRONIC COMPONENT COMPRISING A FIELD PLATE AND A P-DOPED FLOATING REGION. COMMISSARIAT AA LENERGIE ATOMIQUE ET AUX ENERGIES ALTERNATIVES [FR] US2021367069 (A1), issued 25 November 2021. https://worldwide.espacenet.com/publicationDetails/biblio?FT=D&date=20211125&DB=EPODOC&locale=fr_EP&CC=US&NR=2021367069A1&KC=A1&ND=4.

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† **Symposium poster:**

- **Florian Rigaud-Minet**, 'Experimental and simulation study of GaN device size limitations for high efficiency power converters'. Journée des électroniques de puissance CNRS GDR-SEEDS, March 2022. https://journeesdesep.sciencesconf.org/resource/page/id/3

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FOLIO ADMINISTRATIF

THESE DE L'UNIVERSITE DE LYON OPEREE AU SEIN DE L'INSA LYON

NOM : RIGAUD-MINET
(avec précision du nom de jeune fille, le cas échéant)

DATE de SOUTENANCE : 20/03/23

Prénoms : Florian Victor

TITRE : Experimental and Simulation Study of GaN Device Size Limitations for High Efficiency Power Converters

NATURE : Doctorat

Numéro d'ordre : 2023ISAL0021

Ecole doctorale : EEA 160

Spécialité : Electronique, micro et nanoélectronique, optique et laser

RESUME :

Nowadays the electrification of our society leads to a huge demand for technologies related to power conversion systems. Lateral Gallium Nitride (GaN) transistors made on silicon wafers were shown to be more adapted for high-efficiency power conversion over their silicon counterparts in the mid-voltage range (100 V–1000 V) at a reasonable cost. The targeted power converters are phone or laptop chargers, on-board chargers in electric vehicles, data center power supplies, micro-inverters for photovoltaics and more-electric-aircraft power converters. Power transistor scaling may be interesting to improve converter efficiency. Indeed, it could, on the one hand, reduce the transistor-related charges Q_{XX} decreasing the switching time and hence the switching losses or on the other hand, decrease the on-state static resistance $R_{DS,ON}$. However, the scaling should also result in a reduction of the device breakdown voltage as well as a switching that is more sensitive to parasitics that may have disturbed its stability/losses.

In this thesis, the electric field distribution management and the switching losses of lateral 650 V rated GaN-on-Silicon power devices built at CEA-LETI are studied. To do so, an electrical and physical failure analysis was performed to identify the voltage limitation of lateral GaN-on-Si diode test vehicles with different layouts and substrate connections. To study the electric field distribution by Technology Computer Assisted Design (TCAD) using Synopsys® Sentaurus™, the electric field variation should reproduce the experimental breakdown voltage. Thus, a buffer trap calibration method based on experimental protocols was initiated. Finally, a new hard switching characterization test bench was set up to study the transistor design and manufacturing process impact on the switching losses of lateral GaN-on-Si transistors. The results help to derive guidelines for the technology and design scaling of the future generations of fully recessed GaN-on-Si Metal Insulator Semiconductor High Electron Mobility Transistor (MIS-HEMT).

MOTS-CLÉS : Power electronics, Power devices, GaN devices, HEMT, Breakdown voltage, TCAD, Hard switching

Laboratoire (s) de recherche : Ampère, CNRS UMR 5005.

Directeur de thèse: Dominique Planson (Professeur des Universités), Hervé MOREL (Directeur de Recherche)

Président de jury :

Composition du jury : Frédéric MORANCHO (Professeur des Universités), Matteo MENEGHINI (Professeur des Universités), Nathalie LABAT (Professeure des Universités), Dominique Planson (Professeur des Universités), Hervé MOREL (Directeur de Recherche), Julien BUCKLEY (Docteur)

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