THÈSE

Pour l'obtention du Grade de

DOCTEUR DE L'UNIVERSITÉ DE POITIERS

FACULTÉ DES SCIENCES FONDAMENTALES ET APPLIQUÉES
(Diplôme National - Arrêté du 25 mai 2016)

Ecole Doctorale : Sciences et Ingénierie des Systèmes, Mathématique, Informatique

(SISMI)

SECTEUR DE RECHERCHE : ÉLECTRONIQUE, MICROÉLECTRONIQUE ET NANOÉLECTRONIQUE

PRÉSENTÉE PAR :

BHANU PRATAP SINGH JADAV

****

ANALYSIS AND DESIGN OF A NEW 24 GHZ ACTIVE PHASE SHIFTER, INTEGRATED IN A BICMOS SIGE:C 0.25 µm TECHNOLOGY FOR BEAMFORMING APPLICATIONS

****

DIRECTEUR DE THÈSE : **Jean-Marie PAILLOT**

CO-ENCADRANT : **David CORDEAU**

****

Soutenue le 13 Décembre 2019 devant la Commission d'Examen

****

JURY

Rapporteurs:

Jean-Baptiste BEGUERET	Professeur à l'Université de Bordeaux
Tchanguiz RAZBAN HAGHIGHI	Professeur à l'Université de Nantes

Examinateurs:

Julien SARRAZIN	Maître de conférences HDR à Sorbonne Université
David CORDEAU	Maître de conférences HDR à l'Université de Poitiers
Jean-Marie PAILLOT	Professeur à l'Université de Poitiers

Dedicated to my beloved parents and lovely sister…

ACKNOWLEDGEMENTS

With immense pleasure and heartfelt gratitude, I would like to sincerely acknowledge the much-appreciated love, support and invaluable contributions extended to me throughout my PhD journey.

In this regard, I would like to express my initial thanks to Mr Dominique BAILLARGEAT, Professor at the University of Limoges and former Director of the XLIM laboratory, for having welcomed me to laboratory xlim and to finance a part of my thesis.

I would like to convey my sincere gratitude towards the Director of my thesis, Mr Jean-Marie Paillot, Professor at the University of Poitiers and Director of the University Institute of Technology of Angoulême, for offering me the opportunity to pursue PhD under his supervision. He has been generous in his encouragement and for his timely feedback. His energy and liveliness have been inspirational. I am grateful to him for inspiring my interests in the subject and his support throughout this entire period.

I am thankful also to my co-director Mr David Cordeau, Maître de Conference HDR at the University of Poitiers, for his critical feedback and the many detailed explanation of the integrated circuit designing from the initial phases of the thesis. The quality of his supervision, involvement and valuable scientific advices were instrumental in defining the path of my research.

I would like to express my appreciation to the committee members, Professor Jean-Baptiste Beguret, Professor Tchanguiz Razban Haghighi and Professor Julien Sarrazin, for accepting the request to validate my thesis and participate in my oral defence. I am also thankful for their insightful comments and positive suggestions.

A special thanks to Sébastien Soubie, Computer Technician at the IUT Angoulême, "the Genius" of the laboratory, for his high availability, his good humour, his kindness, his efficiency and his precious help.

I remain thankful to all these people for their support and involvement in my work, despite unforgiving deadlines and commitments.

Along with them, my sincere thanks to Smail Bachir, Claude Duvanaud, Fabrice Wateau, Regis Lucas, Emilie Remond and Thami Zeghloul who were always ready to provide academic assistance whenever needed. My sincere thanks also go to Nelly Gilley, for her care, guidance, understanding and moral support. Despite her busy schedule, she always kept a

watchful eye over me and provided me with her valuable advice whenever needed to balance my work life and personal life.

A special mention of thanks to my friends Amit Karel, Arjun Maheshwari, Parth Raj Singh and Shubham Maheshwari for their unconditional friendship and moral support during my PhD. The years would not have passed without the friendship and lighter moments with my laboratory colleagues, Mariem, Serguei, Abdu, Mohamed, Younes, Tayeb, Maissa and Bogdon. My colleagues played a significant role during my PhD by sharing their knowledge and experience. A special thank also goes to Marion Giraud, Jean Marie Barth, Catherine Martinon, Françoise Mercier, Pratik Purkayastha, Rachid Chowdury and Celine Chowdury for introducing me to the French culture, cuisine and becoming my family in France.

I owe my deepest gratitude towards my mother Bhragulata Jadav, my father Hukam Singh Jadav, my lovely sister Bhanu Priya Jadav and my brother-in-law Digvijay Singh Chauhan for their belief in me, their eternal support and understanding of my goals and aspirations. Their infallible love and support has always been my support.

In the end, I would like to extend my warm and heartfelt gratitude towards each and everyone who has impacted this work for their constant love, support and encouragement.

Table of Contents

List of figures v

List of tables ix

List of Abbreviations xi

General Introduction 1

Chapter I: Introduction to the research work 6

Introduction 10

1 5G: The future vision 11

1.1 Key capabilities of 5G 12

1.2 Applications of the 5G 14

1.3 Spectrum for 5G 15

1.4 Research challenges in 5G and motivation of the thesis 15

2 Beamforming of Antenna array 16

2.1 Principle of the antenna array 16

2.2 Uniform linear antenna array 18

2.3 Uniform planar antenna array 19

2.4 Controlling the shape of the radiation pattern 21

3 Principle and state of the art of different methods to control the radiation pattern by phase synthesis. 22

3.1 Phase synthesis by Vector Modulators 23

3.1.1 Limitations 24

3.2 Phase synthesis by using Coupled Oscillator Arrays 25

3.2.1 Theory of oscillator 25

3.2.1.1 Oscillator's principle 26
3.2.1.2 Starting of oscillations 27
3.2.2 Coupled Oscillator Arrays (COAs) 28
3.2.3 Limitations 31
3.3 Phase synthesis by Injection locked Oscillator Array (ILOAs) 32
3.3.1 Injection locking phenomenon 33
3.3.2 Limitations of ILOs 36
3.4 Controlling the shape of the radiation pattern of an antenna array through injection locked oscillator array 39
4 The objective of the dissertation 41
5 Conclusion 43
Chapter II: Behavioural analysis of triple-push VCO and design of a new triple-push VCO 44
Introduction 48
1. Triple-push Oscillators 49
1.1. Triple-push Oscillator principle 50
1.2. Oscillation modes analysis in a triple-push oscillator 51
1.3. Different architectures of the triple-push 53
2. Design of the differential elementary VCO 55
2.1. Resonance tank design 57
2.2. Active part design 62
2.3. The layout of the VCO 63
3. Design of the differential triple-push VCO 67
3.1. Design of the output stage amplifier and buffer 68
3.2. The layout of the Triple-Push VCO 71
3.3. The Post layout simulation results of the TPVCO 72
4. Conclusion 76

Chapter III: Injection locked triple-push VCO based active phase shifter 78

Introduction 82

1. The Injection locking phenomenon in a triple-push Voltage Controlled Oscillator. 83

2. The 120° phase shifter..... 84

2.1. Design of a new 120° phase shifter at 8 GHz..... 86

2.1.1. Analysis and design of the 60° phase shifters 86

2.1.2. Design of the 120° phase shifter by using differential adders..... 88

2.2. Post-layout simulation results of the 120° phase shifter 92

3. Injection-locked triple-push VCO based RF active phase shifter..... 97

3.1. The architecture of the Injection Locked Triple-push VCO (ILTPVCO)..... 100

3.2. The layout of the IL TP VCO..... 103

3.3. Post layout simulation results..... 104

3.3.1. The performances of the active phase shifter without injection..... 104

3.3.2. The performances of the active phase shifter with injection..... 105

4. Resume of the phase shifter results..... 108

5. Conclusion 110

Final Conclusion 111

List of scientific publications 115

Résumé en français..... 116

References 126

List of figures

Figure 1.1: Advancement of the 'G' Technology [source: www.softwaretestinggenius.com]. 11
Figure 1.2: Enhancement of key capabilities from IMT-Advanced to IMT 2020 [4]. 13
Figure 1.3: 5G Spectrum GSMA Public Policy Position, November 2018. 15
Figure 1.4: Examples of geometric configurations of the antenna array: (a) linear, (b) planar, and (c) circular. 17
Figure 1.5: Representation of a uniform linear array 19
Figure 1.6: Rectangular planar antenna array. 20
Figure 1.7: Main lobe and side lobes level of the radiation pattern of an antenna array. 21
Figure 1.8: Vector modulator architecture used on (a) LO path; (b) RF path 23
Figure 1.9: Block diagram of a common vector modulator-based active phase shifter [20]. 24
Figure 1.10: Examples of different periodic signals 25
Figure 1.11: Linear model of an oscillator 26
Figure 1.12: Block diagram of an array of N coupled oscillators 29
Figure 1.13: Phase-Shift versus the angle θ 29
Figure 1.14: Two resistively coupled oscillators 30
Figure 1.15: General architecture of a phased-array transmitter using an ILOA 32
Figure 1.16: Simplified model of (a) LC oscillator (b) LC oscillator under injection. 33
Figure 1.17: Phasor diagram of the ILO of figure 1.16 (b) 34
Figure 1.18: Phase shift in an injection locked oscillator [40]. 36
Figure 1.19: Phase variation in an ILO 37
Figure 1. 20: (a) Phase shift variation of an injection locked oscillator, (b) Linear Phase shift variation by using a frequency tripler [22]. 38
Figure 1.21: Calculated linearity error of the phase shift obtained by injection locking in the oscillator. 38
Figure 1.22: Block diagram of an antenna array controlled by an ILOA. 39
Figure 1.23: Injection locking in a planar antenna array. 40
Figure 1.24: Schematic of a hybrid antenna array 41
Figure 1 25: The architecture of the proposed active phase shifter. 42
Figure 2.1: Design of (a) Push-push oscillator and (b) Triple-push oscillator 49

Figure 2.2: Triple-push oscillator operation. 50
Figure 2.3: Triple-push equivalent circuit model in the odd mode. 51
Figure 2.4: Triple-push equivalent circuit model in even mode 52
Figure 2.5: Different modes of oscillations for the triple-push oscillator 53
Figure 2.6: (a)Triple-push architecture by Yu-Long Tang and Huei Wang [47], (b) Architecture of the subcircuit oscillator. 54
Figure 2.7: Triple-push architectures (a) by B Çatli and M M Hella [52], (b) by C C Li, C C Chen, B J Huang, P C Huang, K Y Lin, and H Wang [54] 54
Figure 2.8: Schematic of the differential LC VCO 56
Figure 2.9: (a) Admittance Y_{in} presented to the resonance tank, (b) Schematic for the small-signal and low-frequency analysis of the cross-coupled NMOS differential pair. 57
Figure 2.10: Layouts of the shielded octagonal inductors with and without center tap. 58
Figure 2.11: Layout view of the octagonal differential inductor in QUBiC4X library 59
Figure 2.12: The simulated Quality factor of the differential inductor 59
Figure 2.13: Characteristics C(*Vtune*) of the varactor diode @ 8 GHz. 60
Figure 2.14: The Quality factor of the varactor diode @ 8 GHz. 61
Figure 2.15: Architecture of the current mirror for a single LC VCO. 63
Figure 2.16: Cross-section view of the QUBiC4X technology of NXP semiconductors 64
Figure 2.17: Layout of the LC VCO in the cadence design system 65
Figure 2.18: Post layout simulation results of the output frequency vs the tuning voltage. 65
Figure 2.19: Post layout time-domain simulation analysis of LC VCO at 8 GHz for *Vtune*=1.7 V 66
Figure 2.20: Simulated phase noise of the VCO for a tuning voltage of 1.7 V. 66
Figure 2.21: Triple-push LC VCO coupled via Varactor diodes. 67
Figure 2.22: Architecture of the differential amplifier and output buffer 69
Figure 2.23: Current mirror of the Triple-Push VCO providing biasing current for the three VCOs and the three output stage amplifiers 69
Figure 2.24: The layout of the triple-push VCO implemented in the QUBiC4X 0.25 µm SiGe:C BiCMOS process of NXP Semiconductors. 71
Figure 2.25: Post layout simulation of the output frequency vs the tuning voltage. 72
Figure 2.26: Post Layout simulation results of the output power, second harmonics and fundamental as a function of the tuning voltage in CADENCE®. 73

Figure 2.27: Time-domain post-layout analysis of the triple-push VCO (a) Output of the three VCO at 8 GHz and at 120° to each other, (b) Output of the triple-push VCO in odd mode at 24 GHz for *Vtune* = 2 V..... 74
Figure 3.1: The principle of injection locking in a triple-push oscillator 83
Figure 3.2: Architecture of a 120° phase shifter proposed by (a) W. Mielke [63], (b) Andrea Bevilacqua et Pietro Andreani [64] and (c) T. Chi, J. Luo, S. Hu, and H. Wang [65] 85
Figure 3.3: complete 120° phase shifter architecture. 86
Figure 3.4: Schematic of the 60° phase shifter..... 87
Figure 3.5: Construction of the vector P_2 from the algebraic notation $a + jb$ for a phase of 60° and a module of 1. 88
Figure 3.6: (a) Phase construction of $\overrightarrow{P_{3,300}}$ and $\overrightarrow{P_{3,120}}$, (b) Complete phasor diagram. 89
Figure 3.7: (a) Architecture of the differential adder, (b) Block diagram of the three differential adders connected to six output buffers. 90
Figure 3.8: Electrical circuit diagram of the 60° phase shifter tunable at 8 GHz. 91
Figure 3.9: The layout of the 120° phase shifter. 92
Figure 3.10: Input reflection coefficient (S11)..... 93
Figure 3.11: Phase error at the output of the 60° phase shifter 94
Figure 3.12: Phase errors between the three output signals. 95
Figure 3.13: Amplitude errors between the three output signals. 95
Figure 3.14: Different architectures for implementing the RF phase shift: (a) on the RF path; (b) on the IF path; (c) on the LO path; (d) in digital baseband 98
Figure 3.15: The architecture of the phased antenna array for the beamforming application in LO path. 99
Figure 3.16: Block diagram of the injection locked triple-push VCO. 101
Figure 3.17 : The layout of the injection locked triple-push VCO. 103
Figure 3.18: Frequency vs *Vtune* for the global circuit without injection..... 105
Figure 3.19: Input reflection coefficient (S11)..... 106
Figure 3.20: Post layout simulation of the phase shift obtained between the injection signal and output of one VCO with respect to *Vtune* and corresponding phase shift obtained at the output of the triple-push VCO 107
Figure 3.21: Post layout simulation result of the output power with respect to *Vtune*. 108

List of tables

Table 1.1: Generation of wireless technology [1]. 12
Table 2.1: Physical characteristics of the Inductor 58
Table 2.2: Summary of simulated varactor performances 61
Table 2.3: Dimensions of the transistors of the current mirror. 63
Table 2.4: Current mirror transistors' size for the complete triple-push VCO. 70
Table 2.5: Comparison with other triple-push VCOs between 20-30 GHz 73
Table 2.6: Summary of the triple-push VCO performances 73
Table 2.7: Rejection of the fundamental and second harmonic as a function of the temperature 75
Table 2.8: Rejection of the fundamental and second harmonic as a function of the supply voltage 75
Table 2.9: Rejection of the fundamental and second harmonic as a function of the process variations 75
Table 3.1: Summary of performances of the differential 120° tunable active phase shifter at 8 GHz. 96
Table 3.2: Static parameters of the overall circuit 104
Table 3.3: Post layout results of the active phase shifter 107
Table 3.4: Comparison of the performances of the developed system with the literature 109

List of Abbreviations

ADC	Analog to Digital Convertor
AR	Augmented Reality
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
CAD	Computer Aided Design
CDMA	Code Division Multiple Access
COAs	Coupled Oscillator Arrays
DAMPS	Digital Advanced Mobile Phone Service
DRM	Design Rule Manual
EVDO	Evolution Data Optimised
GSM	Global System for Mobile Communications
GSMA	Global System for Mobile Communications
HB	Harmonic Balance
HSPA	High Speed Packet Access
ICT	Information and Communication Technologies
IEEE	Institute of Electrical and Electronics Engineers
IF	Intermediate Frequency
ILOAs	Injection locked Oscillator Arrays
ILOs	Injection Locked Oscillators
ILTPVCO	Injection Locked Triple-Push Voltage Controlled Oscillator
IMT	International Mobile Telecommunications
IoT	Internet of Things
ITU	International Telecommunication Union

LO	Local oscillator
LTE	Long Term Evolution
MIM	Metal Insulator Metal
MIMO	Multiple Input Multiple Output
NMOS	Negative Channel Metal Oxide Semiconductor
PMOS	Positive Channel Metal Oxide Semiconductor
PSS	Periodic Steady State Simulation Analysis
PVT	Process Voltage and Temperature
QoE	Quality of Experience
QoS	Quality of Service
RAT	Radio Access Technologies
RF	Radio Frequency
SiGe	Silicon Germanium
SMS	Short Message Service
TPO	Triple-Push Oscillator
TPVCO	Triple-Push Voltage Controlled Oscillator
UMTS	Universal Mobile Telecommunications System
V2I/V2V	Vehicle to Infrastructure/Vehicle to Vehicle
VCO	Voltage Controlled Oscillator
VR	Virtual Reality
WiMAX	Worldwide Interoperability for Microwave Access
WRC	World Radiocommunication Conference

General Introduction

5G technology, i.e. fifth generation of wireless communication technology, arriving in 2020, is going to change the perception of the whole world towards technology advancement. It is the future of the next/new generation mobile network/wireless systems which will become the backbone of the Internet of Things (IoT), providing broadband and media everywhere, smart vehicles transport, critical services and infrastructure control, critical control of remote devices, human-machine interaction, sensors network etc... A new architecture, new communication technologies and new hardware with advanced high-tech software will implement this transformation to provide access to information and sharing of data anytime and anywhere. 5G key capabilities, recommended by the International Telecommunication Union (ITU), will be able to provide peak data rate up to 10 Gbits/sec per user/device with a latency of under 1 msec, ultra-high reliability (>99.999%) and high connection density. To support increased traffic capacity and enable the transmission bandwidths needed to support very high data rates, 5G will extend the range of frequencies used for mobile communications. According to a June 2019 report from Ericsson, 5G will reach 45% population coverage and 1.9 billion subscriptions by 2024, making it the fastest generation ever to be rolled out on a global scale. Even though the spectrum of 5G is not fixed, it is expected to be up to 300 GHz. Once 5G is deployed in 2020, the most critical challenge will be to control the massive traffic. The transmission of the signals with minimum losses and interference is going to be one of the most important factors.

Research for different challenges of 5G technologies has already started. One of the research challenges in 5G is beamforming and how to perform it at millimetre wave frequencies. It plays vital role in many applications for the transmission of data. In case of broadband and media, it creates new opportunities for mobile broadband evolution, enhances transmission in crowded areas, and improves the QoS (Quality of Service). For the Smart vehicles and transport, it provides improved fleet monitoring, navigation and augmented reality by orchestration of fast data and input interfaces with small latency. Critical controls of remote devices have significant benefits of efficiently controlling in hazardous environment by directing the signals at required positions, thereby increasing the efficiency and reducing cost. Human machine interaction will be reliable and precise especially for smart houses, child monitoring and remote health care. Indeed, it will improve the requirements for indoor and outdoor communication scenarios.

In this context, it seems interesting to develop an integrated circuit in the millimetre wave domain to control the transmission of signals. Associated to an antenna array, this circuit allows to perform beamforming, i.e. it allows the orientation and control of the radiation pattern in the desired direction. In millimetre waves, the ability to steer the beam allows to compensate for the losses due to the increase in frequency. This new circuit ensures a tunable RF phase shift between the input and the output. It is based on an original Injection Locked Triple-Push Voltage Controlled Oscillator (ILTPVCO) at 8 GHz. In these conditions, the frequency of the output signal is at 24 GHz. The objective of this dissertation is to present the analysis and the design of this fully integrated active RF phase shifter implemented in the QUBiC4X 0.25 µm SiGe:C BiCMOS process of NXP semiconductors.

This manuscript is composed of three chapters:

The first chapter begins with the introduction of the future vision of 5G, its applications, the spectrum of the 5G and different research challenges in 5G. A brief description of the beamforming basics using different methods to control the shape of the radiation pattern is discussed. Indeed, the control of the radiation pattern by amplitude and/or phase synthesis is first treated. Then, the state of the art of different phase synthesis techniques is reviewed. More specifically, the control of the radiation pattern by phase synthesis with external commanding through oscillators is illustrated.

The second chapter presents the design and implementation of a differential triple-push VCO. The chapter starts with the brief theory of the triple-push oscillator and its mode analysis. Different triple-push oscillators around 20-40 GHz designed previously are reviewed, and different architectures of previous triple-push oscillators are analysed. A new architecture of a differential triple- push VCO is proposed here. It consists of operating the coupling through the varactor diodes and isolating the output 3rd harmonic from the coupling circuit. The circuit is implemented in the QUBiC4X 0.25 µm SiGe:C BiCMOS process of NXP semiconductors and the post layout simulation results are presented.

The third chapter presents the proposed original architecture of an active RF phase shifter using an Injection Locked Triple-Push Voltage Controlled Oscillator (ILTPVCO). The chapter begins with the introduction of the 120° injection circuit. A novel architecture of a differential tunable 120° phase shifter at 8 GHz and integrated in the 0.25 µm BiCMOS SiGe:C technology is presented with the post-layout simulation results. In the second part, we

present the design and implementation of the new active phase shifter architecture designed with the combination of the 120° phase shifter and the triple-push VCO at a frequency of 24 GHz fully integrated on a silicon substrate using the 0.25 µm BiCMOS SiGe:C process of NXP semiconductors . Then the post-layout simulation results of the circuit are presented in order to evaluate the performances of the proposed active phase shifter and to validate the concept of this new architecture.

Chapter I: Introduction to the research work

Table of Contents

Chapter I: Introduction to the research work 6

Introduction 10

1 5G: The future vision 11

1.1 Key capabilities of 5G 12

1.2 Applications of the 5G 14

1.3 Spectrum for 5G 15

1.4 Research challenges in 5G and motivation of the thesis 15

2 Beamforming of Antenna array 16

2.1 Principle of the antenna array 16

2.2 Uniform linear antenna array 18

2.3 Uniform planar antenna array 19

2.4 Controlling the shape of the radiation pattern 21

3 Principle and state of the art of different methods to control the radiation pattern by phase synthesis. 22

3.1 Phase synthesis by Vector Modulators 23

3.1.1 Limitations 24

3.2 Phase synthesis by using Coupled Oscillator Arrays 25

3.2.1 Theory of oscillator 25

3.2.1.1 Oscillator's principle 26

3.2.1.2 Starting of oscillations 27

3.2.2 Coupled Oscillator Arrays (COAs) 28

3.2.3 Limitations 31

3.3 Phase synthesis by Injection locked Oscillator Array (ILOAs) 32

3.3.1 Injection locking phenomenon 33

3.3.2 Limitations of ILOs 36

3.4 Controlling the shape of the radiation pattern of an antenna array through injection locked oscillator array 39

4 The objective of the dissertation 41

5 Conclusion 43

Introduction

The objective of this first chapter is to present the framework of my thesis work and the different basic concepts involved in this dissertation. This chapter begins with the introduction of the future vision of 5G, its applications, the spectrum associated with 5G and different research challenges that need to be addressed from a research perspective. First, the principle and different types of antenna arrays, as well as the main characteristics of linear and planar antenna arrays, are presented. Then, the different techniques of the radiation pattern synthesis will be described. In addition, a state of the art of the different architectures for implementing phase shifts, used in the literature, is established. Subsequently, the emphasis is placed on the phase synthesis technique using an "Injection-Locked Oscillator Array" (ILOA). This technique is based on the use of a "slave oscillator" which, once synchronised to the injection frequency of the "master oscillator", generates a phase difference between the injected signal (master oscillator) and the output signal of the "slave oscillator". This phase difference is controlled by modifying the free-running frequency of the "slave oscillator" via its control voltage, referred to here as *Vtune*. Thus, to control an antenna array, it is sufficient to place a network of slave oscillators each associated with an antenna (or a group of antennas), all of them synchronised by an injection signal, in this case the LO signal. The independent control of the free-running frequencies (different *Vtune*) allows an independent control of the phase shift between each output signal and the injected signal. In the end, the objective of the thesis is presented, followed by the conclusion.

1 5G: The future vision

The fifth-generation, abbreviated as 5G, is the future of the next/new generation mobile networks/wireless systems. The arrival of 5G technology in 2020 has already boosted the major transformation in the wireless industry, which will completely change the communication system in the whole world (figure 1.1). In the coming years, sharing of data and access to information would be possible anytime and anywhere to anyone and anything. It would be able to provide very high data rates (typically of Gbps), very low latency (<1ms), ultra-high reliability (>99.999%), energy efficiency and extreme divide densities and will be accomplished by the development of LTE in combination with new radio access technologies (RAT). 5G will enhance the work and play in the cloud capacities, wireless connectivity of wearables, self-driving cars, smart homes, traffic safety/control, industrial process, automation, and very-high-speed media delivery. In short, it will accelerate the rapid development of the Internet of Things (IoT).

Rather than based on one specific radio-access technology, 5G is a portfolio of access and connectivity solutions addressing the demands and requirement of mobile communication beyond 2020. Table 1.1 summarises the generation of wireless technology.

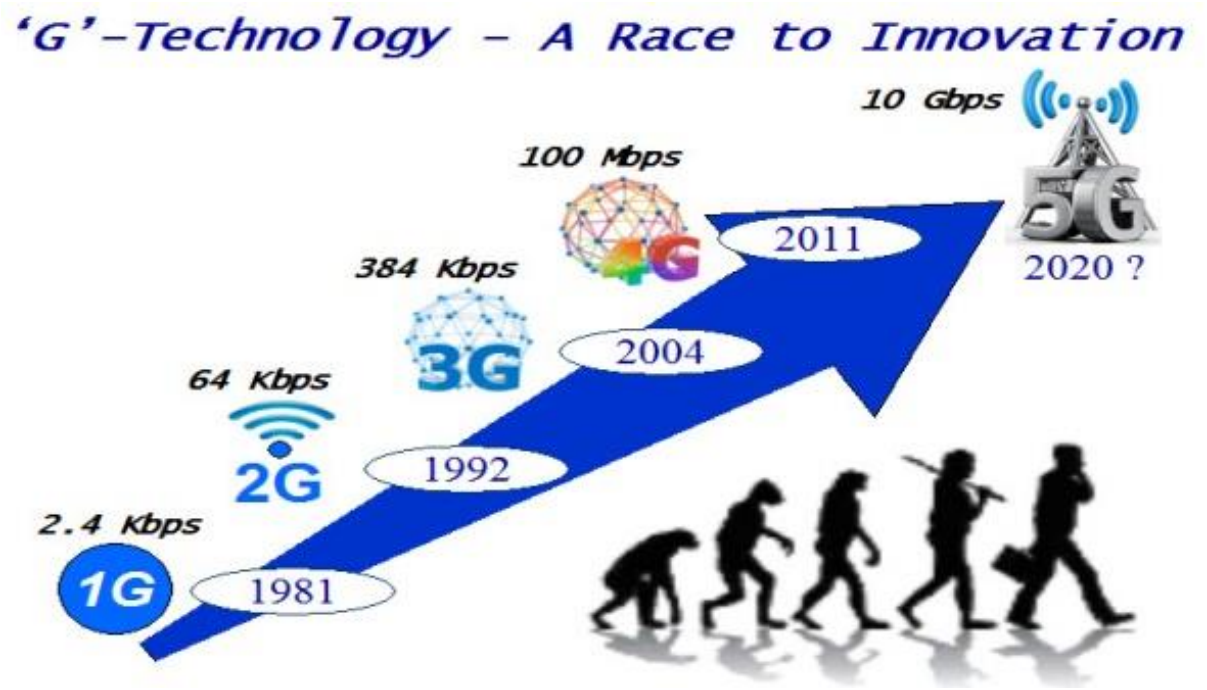


Figure 1.1: Advancement of the 'G' Technology [source: www.softwaretestinggenius.com].

Table 1.1: Generation of wireless technology [1].

Generation	Requirements	Comments
1G	➢ **No official requirements.** ➢ **Analog technology.**	➢ **Deployed in the 1980s.**
2G	➢ **No official requirements.** ➢ **Digital technology.**	➢ **First digital systems.** ➢ **Deployed in the 1990s.** ➢ **New services such as SMS and low-rate data.** ➢ **Primary technologies include IS-95 CDMA (CDMA One), IS-136 (DAMPS), and GSM.**
3G	➢ **ITU's IMT-2000 required 144 Kbps mobile, 384 Kbps pedestrian, 2 Mbps indoors.**	➢ **First deployment in 2000.** ➢ **Primary technologies include CDMA2000 1X/EVDO and UMTS-HSPA. WiMAX.**
4G (Initial Technical Designation)	➢ **ITU's IMT-Advanced requirements include the ability to operate in up to-40-MHz radio channels and with very high spectral efficiency.**	➢ **First deployment in 2010. IEEE 802.16m and LTE Advanced meet the requirements.**
4G (Current Marketing Designation)	➢ **Systems that significantly exceed the performance of initial 3G networks.** ➢ **No quantitative requirements.**	➢ **Today's HSPA+, LTE, and WiMAX networks meet this requirement.**
5G	➢ **ITU IMT-2020 has defined technical requirements for 5G, and 3GPP is developing specifications.**	➢ **First standards-based deployments in 2019 and 2020.**

1.1 Key capabilities of 5G

The expected enhanced key capabilities of 5G recommended by the International Telecommunication Union (ITU) are [2] [3]:

- Peak data rate: Under ideal conditions, it is expected to be 10 Gbits/sec per user/device. (20 Gbits/s under certain conditions).
- User experienced data rate: Up to 100 Mbit/s or Gbit/s in hotspots cases.

- Latency: <1 ms.
- Mobility: Up to 500 Km/hr with acceptable QoS (accommodate high-speed trains).
- Connection density: 10 times higher than 4G. $10^6/km^2$.
- Spectrum efficiency: 3 times more than 4G.
- Energy efficiency: 100 times as compared to 4G.
- Area traffic capability: Support up to 10 $Mbit/s/m^2$ area traffic capacity. Greater than 100 times current 4G.

The comparisons of the key capabilities of the IMT-2020 with IMT-Advanced are shown in figure 1.2. IMT-2020 will mainly boost the development of the Internet of Things (IoT). It will provide a broad platform for the smart wearable devices, applications, machines and other connected objection without the intervention of the humans. IMT-2020 would provide sustained and affordable future without increasing the cost energy consumption, network equipment cost, and deployment cost [2].

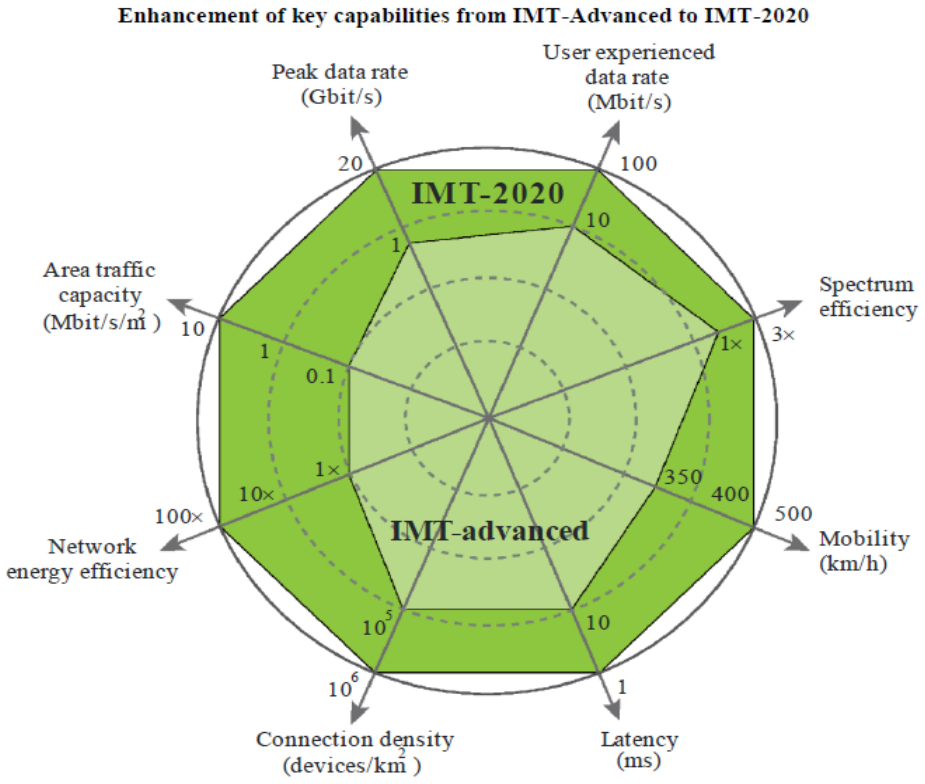


Figure 1.2: Enhancement of key capabilities from IMT-Advanced to IMT 2020 [4].

1.2 Applications of the 5G

Many Information and Communication Technologies (ICT) industrial bodies have already set the requirements in terms of what 5G is [2] [4]. As mentioned in the previous section, 5G will become a cornerstone in many of the economic sectors [5] [6] [7]. Some of the economic domains where 5G technology is going to play a significant role are as follows:

- Agriculture: Advancement in sensors and actuators to measure soil quality, prediction of climatic change, monitoring of cultivation, and livestock movements.
- Automobiles: Improvement in the autonomous vehicle control (self-driving), intelligent traffic control/safety, quality of life, V2V (vehicle-to-vehicle) and V2I (vehicle-to-infrastructure) communications.
- Construction/Building: Development of smart cities with remote accessibility, safety, monitoring, energy efficiency.
- Energy utilities: 5G could efficiently address oil supply unbalance and instability, fracking advancements and carbon constraints, as well as new decentralised business models, and renewable energy generation challenges of the energy utility industries.
- Finance (including banking): Security, fraud detection, and analytics improvement for financial activities such as trading, banking, and shopping.
- Health: Transforming healthcare with 5G is going to be a significant boom in global health which includes exercising at home, remote diagnosis and robotic-assisted surgery, wireless connectivity of health monitoring devices, continuous consumer health sensing, and medical alert.
- Manufacturing: With the introduction of wireless 5G technologies, industrial process control can be made more efficient, reliable, and accurate. Sufficiently low latency and ultra-reliable operation will enhance the factory cell automation and be associated with cloud robotics.
- Media on demand: High frequency with large bandwidth will provide an excellent user experience for viewing 3D and 4K formats on a mass scale. Future smartphone users will popularly enjoy Virtual Reality (VR) and Augmented Reality (AR).

- Public safety: Emergency communications for police, fire, rescue, ambulance, and medical emergency services needs a better reliable and available network. 5G radio access will multiply the efficiency in case of emergency during natural disasters natural calamities.

1.3 Spectrum for 5G

The spectrum of the 5G is not definitely fixed until now. WRC-19 (World Radiocommunication Conference) will take place from 28 October to 22 November 2019, and it will have a significant impact on the future of the 5G spectrum. In order to support increased traffic capacity and to enable the transmission bandwidths needed to support very high data rates, 5G will extend the range of frequencies used for mobile communications. 5G research targets a range between 300 MHz to 300 GHz [8] [9]. WRC-19 is vital for establishing international agreement of 5G bands above 24 GHz. 5G needs a significant amount of new harmonised mobile spectrum. Indeed, 5G needs spectrum within three key frequency ranges to deliver widespread coverage and support all user cases. The three estimated ranges are Sub-1 GHz, 1-6 GHz, and above 6 GHz (figure 1.3).

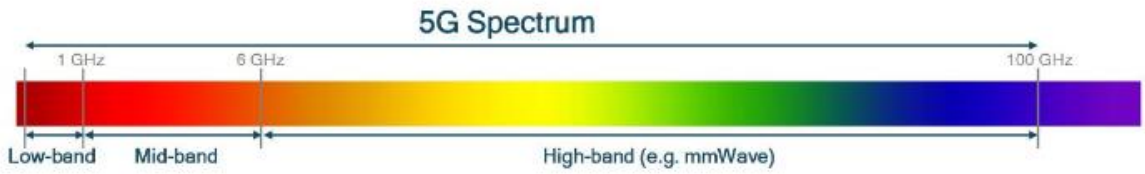


Figure 1.3: 5G Spectrum GSMA Public Policy Position, November 2018.

1.4 Research challenges in 5G and motivation of the thesis

Currently, many types of research are going on future 5G technology [10] [11]. Some of the delicate open research challenges are:

- Introduction of the mm-wave spectrum;
- Unavailability of the popular channel model;
- Site-Specific propagation;
- Antenna array design;
- Beamforming and beam training;

- Massive MIMO;
- Novel multiplexing;
- Non-orthogonality;
- Low latency and QoE;
- Energy efficiency;
- 5G Applications and standardisation.

There are several applications ready to implement in 5G technology. Moreover, once 5G is deployed in 2020, the most critical challenge would be to control the massive traffic. One of the research challenges in 5G is beamforming and how to perform it at millimetre wave frequencies. In this context, it seems interesting to study a system that is able to perform beamforming for the 5G standard. In this dissertation, an active phase shifter is designed in the millimetre wave to orientate and control the radiation pattern in the desired direction.

The active phase shifter is intended to be applied in the LO path for the application of the beamforming in 5G technology. A solution, among others, to focus the EM wave is to use Injection Locked Voltage Controlled Oscillators (ILVCO) which are associated with an antenna array. In this context, the main goal of this thesis will consist in the study and the design of an active phase shifter for phased array systems based on an original injection-locked triple-push VCO at 24 GHz integrated on silicon technology.

2 Beamforming of Antenna array

2.1 Principle of the antenna array

An antenna array is defined as a set of N distributed radiating elements in space. The amplitude and/or phase of the injected signal on each of these elementary antennas can be controlled to command the shape of the radiation pattern of the antenna array and to command its orientation. In particular, it is possible to choose these commands in order to create several lobes simultaneously or a single lobe in the direction of the incident signal and a zero in the direction of an interference wave. The number and type of elementary antennas constituting the array, as well as their geometric layout, represent the main characteristics of an antenna array. The main types of antennas used in antenna arrays are dipoles, monopoles, loop, slots,

horns, and microstrip patch antennas. For the reason of simplicity, implementation and manufacturing, identical elements are generally chosen. For the same reasons, equidistant uniformly spaced linear networks are mostly encountered in practice. The distance d between two antennas is called "step" of the network. The possible geometric configurations of the antenna array are of great variety, in general, they can be:

- linear: the antennas are aligned on a straight line,
- planar: the antennas are arranged on a plane,
- circular: the antennas are arranged on a circle,
- volume: the antennas are distributed in a volume.

The first three types of geometric arrangements are the most commonly used, as they are illustrated in figure 1.4.

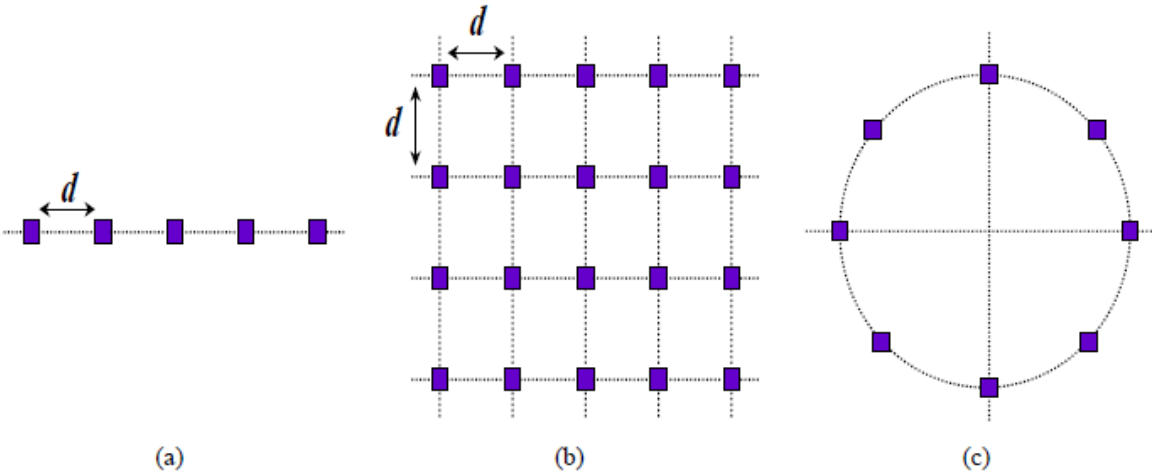


Figure 1.4: Examples of geometric configurations of the antenna array: (a) linear, (b) planar, and (c) circular.

Antenna arrays contribute to the improvement of the communication system performances while increasing the channel capacity, providing a wider band of coverage, and minimising the multipath fading and the interference between channels. Besides these advantages, the following properties describe a few assets of antenna arrays:

- The decrease of electromagnetic pollution: the shape of the radiation pattern can be optimised in order to reduce the side lobes. Similarly, the radiation pattern can be steered in the desired direction, and therefore, any radiations in useless directions are minimised.

- A better quality of the transmission/reception: the emitted power can be focused in the desired direction, and therefore, the wasted power in useless directions is reduced. One of the advantages resulting from this decrease is also the distribution of the power on all the power amplifiers constituting the transmission network. Similarly, for the reception, the noise provided by the interfering signals is minimised, leading to a reduced Bit Error Rate (BER), which is the priority of any transmission architecture.

2.2 Uniform linear antenna array

The radiation pattern of an antenna array is based on the basic physical structure of elementary antennas and the geometry of the array, and also on their control signals [12] [13]. When the elementary sources of a linear array are excited with the same amplitude, the antenna array is considered to be uniform and therefore is called equi-amplitude. In figure 1.5, we consider a uniform linear antenna array made of N identical equidistant elements with a distance d between them along an axis x, commanded by N sources with a mutual phase gradient of $\Delta\phi$ between them. The maximum distance between the reference antenna and the observation plane is represented by r, and θ is the angle of the main lobe direction.

Under these conditions, the total electrical field radiated by the antenna array, in the far-field, is given by:

$$E_{tot} = E_0 \times A(\Psi) \tag{1}$$

where,

- E_0 represents the electrical field radiated by one elementary antenna. It is called "element factor" and depends only on the physical characteristics of the elementary antenna;

- $A(\Psi)$ is the array factor and depends on the geometry of the array and the amount of the amplitude and phase of the signal applied to each elementary antenna. This array factor has the following formula:

$$A(\Psi) = \frac{1}{N} exp(j(N-1)\Psi/2)\ \frac{sin(N\Psi/2)}{sin(\Psi/2)} \tag{2}$$

where $\Psi = \frac{2\pi d}{\lambda} \times \sin(\theta) - \Delta\phi$ and λ is the wavelength

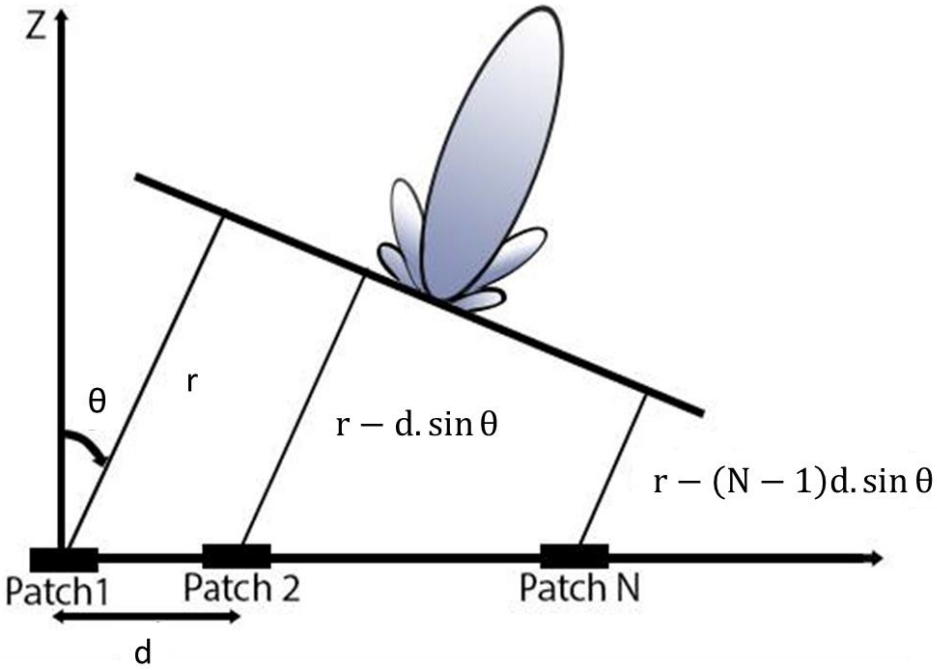


Figure 1.5: Representation of a uniform linear array

Therefore the total radiation pattern of the antenna array is defined by the product of the magnitude of the electrical field radiated by an elementary antenna and the one of the array factor, the latter being given by the following expression:

$$|A(\Psi)| = \frac{1}{N}\left|\frac{sin(N\Psi/2)}{sin(\Psi/2)}\right| \quad (3)$$

The total radiation pattern of the array depends more and more on the array factor and a little on the radiation pattern of each elementary antenna when the number N of the elementary antennas increased. In addition, we show that the maximum of the expression (3) occurs when Ψ is zero. As a consequence, the direction of the maximum radiation is given by: $\Delta\phi = \frac{2\pi d}{\lambda} \times \sin(\theta_0)$.

Therefore, from the direction of the desired radiation pattern θ, the phase shift $\Delta\phi$ applied between the radiating sources can be determined.

2.3 Uniform planar antenna array

A planar antenna array is a 2-D (two-dimensional) array obtained by arranging its antenna elements on a plane. The shape can be rectangular, circular, etc… Figure 1.6

illustrates a uniform rectangular planar array represented in 2-D. This array consists of N_x x N_y elements placed in the XY plane with respective spacing's d_x and d_y between the antenna elements.

In the same way, as in the case of a linear antenna array, the main lobe of the radiation pattern is steered in the desired direction but with additional angular freedom in this case (azimuth as well as elevation). Indeed, the variation of the radiation pattern with a linear array is only possible in the alignment of radiating sources while with a planar array scanning is possible in all desired angular directions [14].

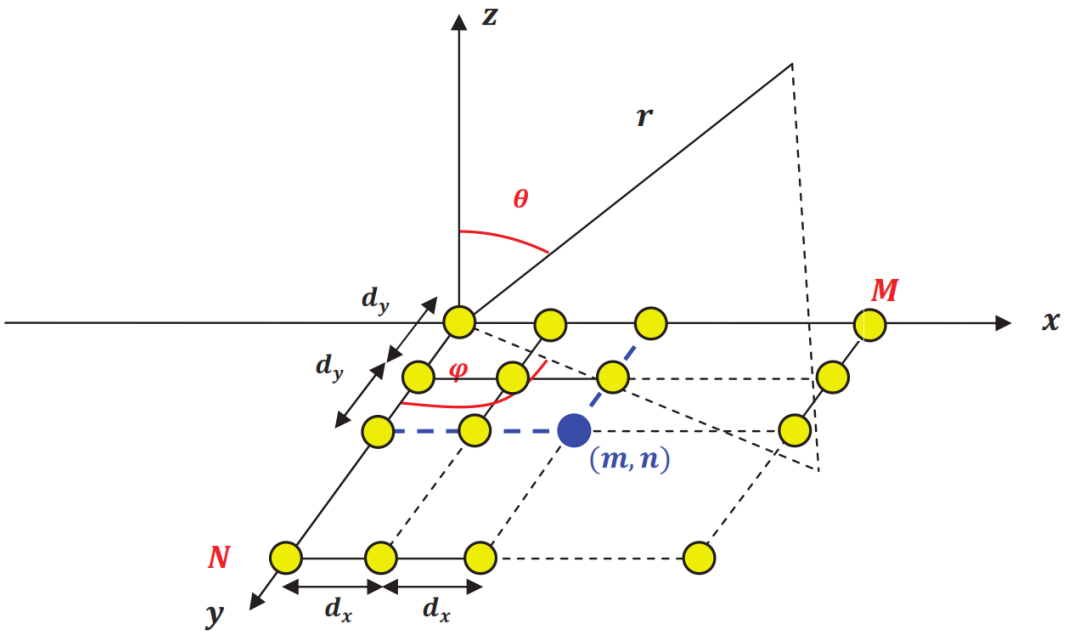


Figure 1.6: Rectangular planar antenna array.

The array factor AF_{plan} is the product of the two uniform linear network factors: one in the x-direction (AF_x) and another in the y-direction (AF_y) [15].

$$AF_{plan} = AF_x * AF_y = \sum_{m=0}^{N_x} e^{j(m-1)\psi_x} * \sum_{n=0}^{N_y} e^{j(n-1)\psi_y} \quad (4)$$

with $\psi_x = \frac{2\pi d_x}{\lambda} \sin\theta \cos\varphi - \Delta\varphi_x$ and $\psi_y = \frac{2\pi d_y}{\lambda} \sin\theta \sin\varphi - \Delta\varphi_y$

where $\Delta\varphi_x$ and $\Delta\varphi_y$ are the mutual phase gradient between the antenna elements in x and y directions, respectively.

The magnitude of the array factor is defined as:

$$\left|AF_{plan}(\psi)\right| = \left(\frac{1}{N_x}\left|\frac{sin\left(\frac{N\psi_x}{2}\right)}{sin\left(\frac{\psi_x}{2}\right)}\right|\right)\left(\frac{1}{N_y}\left|\frac{sin\left(\frac{N\psi_y}{2}\right)}{sin\left(\frac{\psi_y}{2}\right)}\right|\right) \quad (5)$$

Therefore, as in the case of a linear array, the maximum radiation direction (θ_0, φ_0) is obtained when the inter-element phase shifts at x and y are equal to:

$$\Delta\varphi_x = \frac{2\pi d_x}{\lambda} sin\,\theta_0\, cos\,\varphi_0 \quad , \quad \Delta\varphi_y = \frac{2\pi d_y}{\lambda} sin\,\theta_0\, sin\,\varphi_0$$

2.4 Controlling the shape of the radiation pattern

As mentioned above, an antenna array allows the distribution of the radiated energy in space to be controlled in order to optimise the link budget. This distribution is obtained by forming and controlling the radiation pattern. To achieve this, it is necessary to establish a control law consisting of injecting amplitude and/or phase weighting to the signals applied on each radiating elementary elements of the antenna array. This defines the required height and/or opening of the side lobes relative to those of the main lobes (figure 1.7).

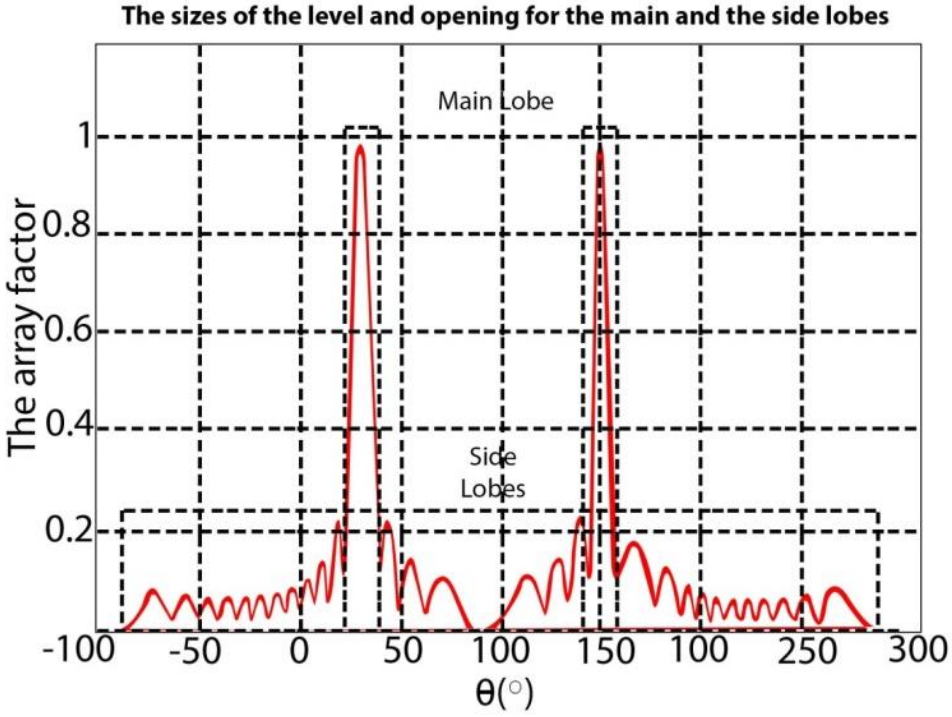


Figure 1.7: Main lobe and side lobes level of the radiation pattern of an antenna array.

The higher the sidelobe level, the lower the power assigned to the main lobe; hence, power is wasted. In a radiation pattern, it is necessary to reduce the side lobes levels for an imposed opening of the main lobe in order to concentrate power in the desired direction and thus minimise losses in other directions [16]. Under these conditions, three different types of synthesis can be considered:

Amplitude synthesis

This technique allows the synthesis of directional and symmetric lobes with the possibility of controlling the level of the side lobes [17] [18]. With the analysis techniques (Chebyshev, Fourier,...), the network coefficients can be determined. However, the applications for this type of synthesis are limited.

Amplitude and phase synthesis

This technique can be used to synthesise both directional lobes and side lobes whose levels are strongly controlled [17] [18]. This technique is useful for adaptive antenna applications but its implementation is complicated and expensive because it requires phase and amplitude synthesis methods, as the name implies.

Phase synthesis

This technique can be used to synthesise both directional lobes and side lobes that are "moderately controllable" [17] [18]. Nevertheless, the level received or transmitted in the direction of the useful radiation as well as the interference radiation can be controlled. Thus, this synthesis technique offers a good trade-off between the directivity of the radiation pattern and the low computing time as well as the reduced implementation costs compared to the two previous solutions. Phase synthesis is also referred to as "phased array antenna".

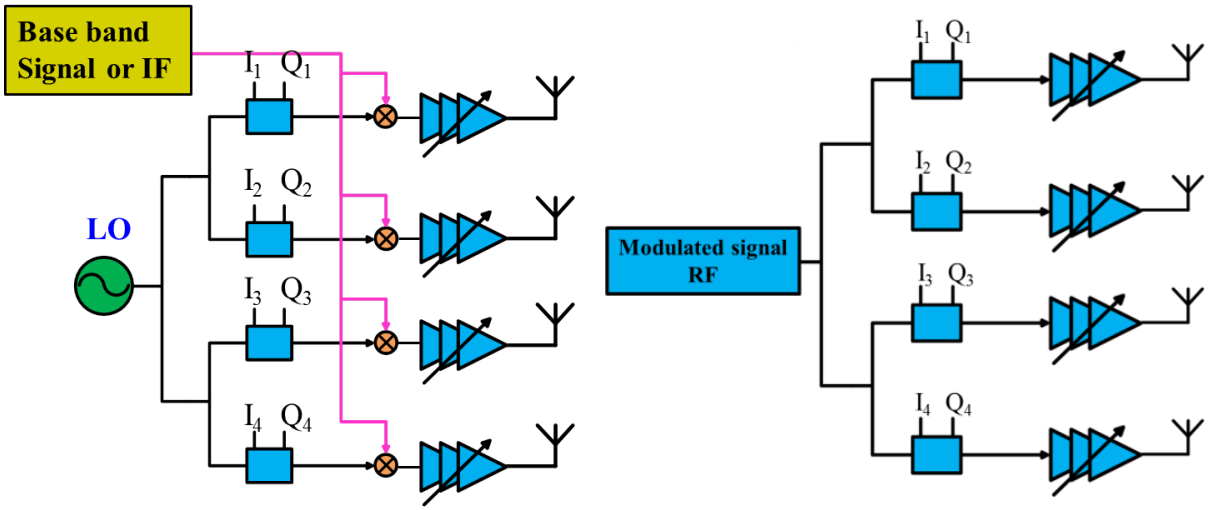
3 Principle and state of the art of different methods to control the radiation pattern by phase synthesis.

In this context, to control the radiation pattern by phase synthesis, several solutions using passive or active phase shifters can be used to achieve the electronic modification of the radiation pattern of a phased antenna array. Passive phase shifters present excellent linearity but suffer specifically from large chip area, significant insertion loss and amplitude variations [18] [19]. On the other hand, active phase shifters offer a high level of integration, no insertion losses and smaller amplitude variations, but they require large power consumption

compared to the passive ones. A variety of integrated active phase shifter architectures have been proposed in the literature [20] [21] [22]. In the following section, the state of the art of different phase shifters using vector modulator, coupled oscillators arrays and injection locked oscillator arrays is discussed.

3.1 Phase synthesis by Vector Modulators

A vector modulator is an RF/microwave circuit which can be used to perform beamforming of the antenna array by controlling both the amplitude and the phase of the signals applied on each element of the antenna array. Hence, vector modulators can provide an active solution for the beamforming on the LO path as well as on the RF path (figure 1.8).



(a) (b)

Figure 1.8: Vector modulator architecture used on (a) LO path; (b) RF path

The vector modulator allows the sidelobe level reduction while the antenna radiation pattern can be precisely positioned in any direction. Phase shift ranging from 0° to 360° can be obtained in steps that depend on the phase tracking accuracy. For instance, in the adaptive beam shaping system presented in [23], the alignment of the beam in the azimuthal direction is performed by vector modulators. The main constraints for vector modulators are:

- Phase/Amplitude accuracy over the system bandwidth and the phase shift range
- Minimum variation of the amplitude between the phase states
- Minimal insertion loss

- Low power consumption.

Vector modulator controls the signal into the desired vector location through command signals V_I and V_Q as illustrated in figure 1.9 where Φ_{th} is the synthesised phase shift and G_{th} is the gain of the active phase shifter [20].

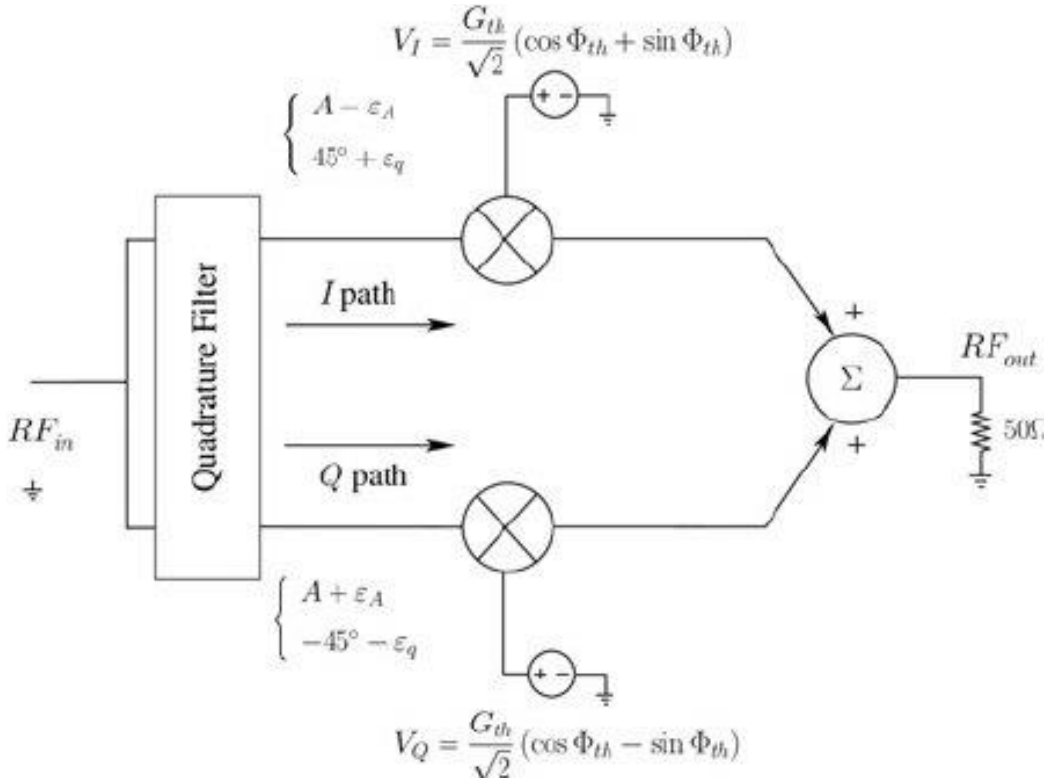


Figure 1.9: Block diagram of a common vector modulator-based active phase shifter [20].

3.1.1 Limitations

In the past, some active solutions using vector modulators as active phase shifters have been presented [24] [25] [26] [27], but none of these works presents the measurement results of the entire system including the antenna array. Indeed, an effective solution using vector modulators associated with a linear antenna array to perform beamforming has been presented in [20]. However, this type of synthesis is complicated and costly as it requires amplitude and phase control. Moreover, other recent works based on the vector-sum technique have been developed in order to obtain high phase resolution and accuracy [28] [29] [30]. Nevertheless, this solution suffers mainly from the complexity of the control circuit in order to obtain the desired phase resolution performances.

3.2 Phase synthesis by using Coupled Oscillator Arrays

3.2.1 Theory of oscillator

An electrical oscillator is an autonomous system that generates a signal with a fixed period (in the case of a simple oscillator) or variable (in the case of a voltage-controlled oscillator or VCO). An oscillator converts the direct current (DC) provided by a power supply into a continuously repeating alternative current (AC) signal. The signal shape can be sinusoidal, square or triangular, as shown in figure 1.10, or a distorted combination of the previous three.

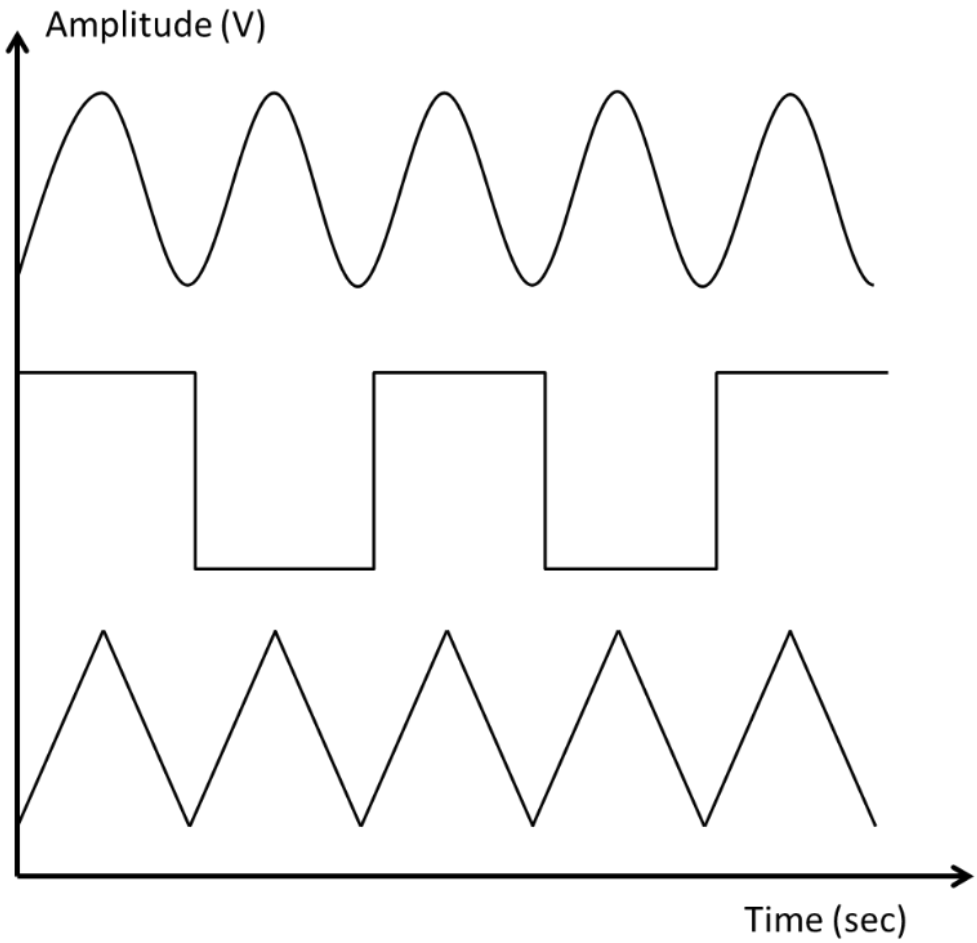


Figure 1.10: Examples of different periodic signals

Oscillators are used in many applications, like a clock, frequency generators, tuneable radio transmitters, the local oscillators. In all the radio frequency applications, it is necessary to have sinusoidal references of high spectral purity (low phase noise). This is one of the

essential characteristic of an oscillator. Indeed, this phase noise will determine the stability of the periodicity of the oscillations provided.

3.2.1.1 Oscillator's principle

An electronic oscillator is composed of a passive resonant circuit and an active circuit. Generally, the passive circuit is inductance-capacitance (LC) type, which determines the oscillation frequency of the oscillator and the active circuit is based on transistors. From a dynamic point of view, this system is autonomous and balanced, as shown in figure 1.11, where $H_1(j\omega)$ represents the transfer function of the active part and $H_2(j\omega)$ represents the transfer function of the resonator.

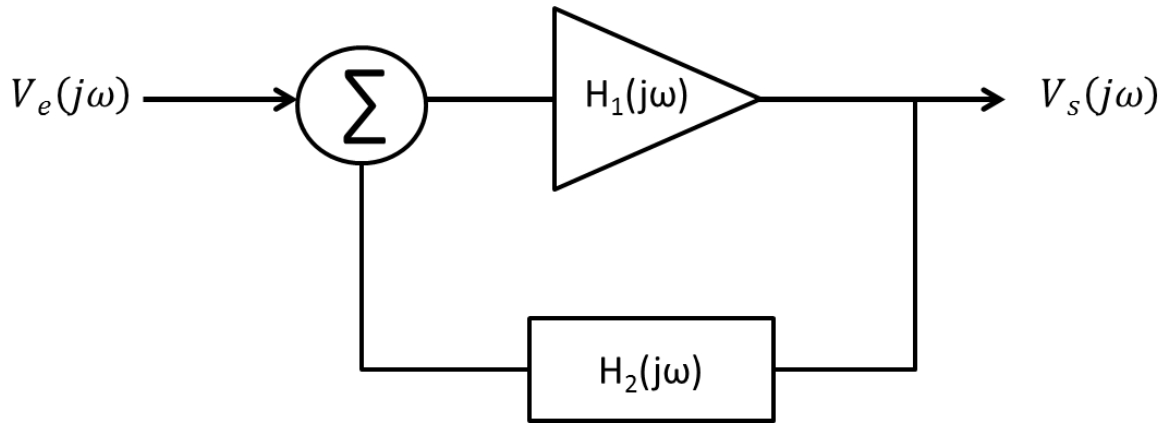


Figure 1.11: Linear model of an oscillator

This block diagram involves a linearization of the behaviour of the active part. It explains the conditions of existence of the oscillations and the starting conditions of oscillations.

The transfer function of this positive feedback system can be written as:

$$H(j\omega) = \frac{V_s(j\omega)}{V_e(j\omega)} = \frac{H_1(j\omega)}{1 - H_1(j\omega)\, H_2(j\omega)} \tag{6}$$

The existence of oscillations is determined by the instability of the system. In the above system, the instability is represented by the poles of the closed-loop function $H(j\omega)$. To find the poles of the equation, we equate the denominator to zero and look for the cases where denominator vanishes. Hence, we have:

$$1 - H_1(j\omega)\, H_2(j\omega) = 0 \tag{7}$$

To guarantee the existence of oscillations, the following are the two parts of the solution of the complex equation:

$$|H_1(j\omega)\, H_2(j\omega)| = 1 \; and \; Arg\big(H_1(j\omega)\, H_2(j\omega)\big) = 2\pi n \tag{8}$$

where n ∈ natural numbers.

These two conditions are popularly known as the Barkhausen stability criterion.

3.2.1.2 Starting of oscillations

When the electronic oscillator is switched on, the Barkhausen criterion is not enough to start the oscillations. In other words, in the real world, we cannot guarantee the starting of oscillations even if (7) is strictly verified. We have two cases:

- Case 1: $|H_1(j\omega)\, H_2(j\omega)| < 1$ (9)

In this situation, any existing oscillations are damped and vanish over time. The output of the system is made of hazardous oscillations of small amplitude. We deal with a system whose active part does not bring enough energy to compensate for the losses of the resonator.

- Case 2: $|H_1(j\omega)\, H_2(j\omega)| > 1$ (10)

In this situation, the active part provides more energy than the resonator losses. Hence the oscillations amplify in time and do not vanish. Without further indications, it is clear that such a situation is not possible in the real world since the amplitude of the oscillations only increases, tending towards infinity.

Limitations of oscillators

We have just seen that to guarantee the starting of the oscillations in the system, it is necessary that the active part of the oscillator provides little more energy than the losses presented by the resonance tank. However, when the amplitude of the oscillations becomes large, the components that constitute the active part eventually move from their linear operating range to a non-linear region, hence resulting in a reduction of the gain of the active part. This shifting to non-linear behaviour implies the generation of the harmonic components. The non-linear behaviour of the oscillators is explained by the non-linear Van der Pol equations [31]. The reduction in the gain will be carried out until the criterion

presented in the (7) is satisfied. Finally, to guarantee the starting and the maintenance of the oscillations in an electronic oscillator, the active part must provide an amount of energy slightly higher than the losses of the resonator and enough to keep the components of the active part in the linear region. The maximum oscillation frequency that can be reached by the fundamental frequency oscillators is basically limited by the components used in the active part of the oscillator. The transistor-based active component limits the oscillation frequency when the maximum available gain reaches unity. Harmonic oscillators are one of the better solutions to use at high frequency as they are not limited by the active component's constraints.

3.2.2 Coupled Oscillator Arrays (COAs)

R. York & al. introduced a new technique based on the synchronisation property of the coupled oscillators to steer the radiation pattern of an antenna array [32]. The synchronisation requirements can be satisfied by coupling the oscillators together by a coupling circuit. A constant phase gradient $\Delta\phi$ can be obtained between the adjacent elements by controlling the free-running frequencies of the outermost oscillators. In [21], it is shown that the theoretical limit of the phase shift that can be obtained by detuning the two end oscillators of the array by equal amounts but in opposite directions is only ± 90°. Nevertheless, the measurement results performed in [33] [34] shows that the maximum value of the phase shift Δϕ decreases by increasing the number of coupled oscillators. For a linear array (figure 1.12), a phase shift Δϕ between adjacent elements results in steering the beam to an angle θ off broadside, which is given by:

$$\theta = arcsin\left(\frac{\lambda}{2\pi d}\Delta\phi\right) \tag{11}$$

where d is the distance separating two antenna elements and λ is the free-space wavelength. In the case of differential oscillators, the theoretical limit of the phase shift is within ±180° due to the differential nature of the oscillator array providing a more efficient beam-scanning architecture (figure 1.13).

An analysis of N coupled Van der Pol oscillators has been performed by Liao and York in [35].

$$\theta_i = \omega_i t + \phi_i \tag{12}$$

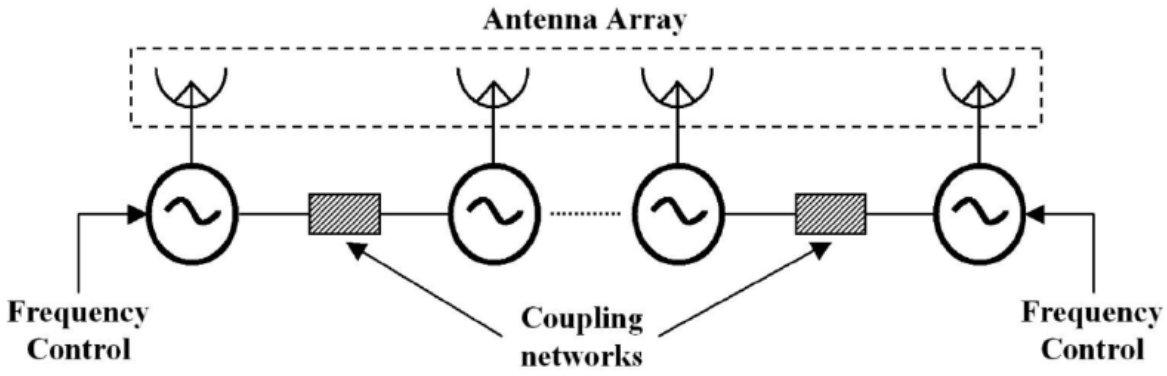


Figure 1.12: Block diagram of an array of N coupled oscillators

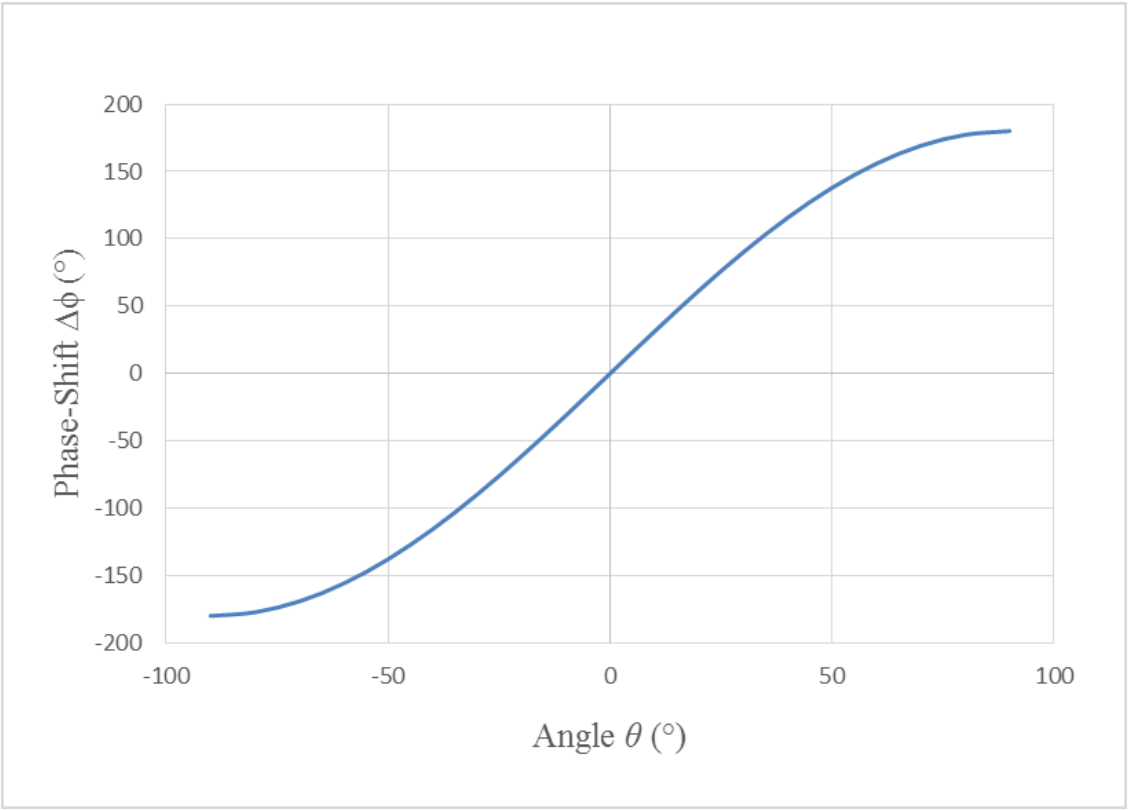


Figure 1.13: Phase-Shift versus the angle θ

According to this analysis, it is possible to write the phase dynamics for an array of N elements as follows:

$$\frac{d\theta_i}{dt} = \omega_i - \frac{\omega_i}{2Q} \sum_{j=1}^{N} Im\left\{k_{ij} \frac{A_j}{A_i} e^{J(\theta_j - \theta_i)}\right\} \quad (13)$$

where for the i^{th} oscillator, $\theta_i = \omega_i t + \phi_i$ is the instantaneous phase, ω_i is the free-running pulsation and $\emptyset_i$ is the initial phase. Furthermore, k_{ij} is the coupling coefficient between the i^{th} and j^{th} oscillator and Q is the resonator's quality factor.

Considering that y_{ijN} are the admittance parameters of the coupling matrix Y for an array of N coupled oscillators and if G_L is the conductance associated with the losses of the tank for one oscillator, then, we can write: $k_{ij} = y_{ijN}/G_L$. Under certain conditions, all of the oscillators are synchronised to the same pulsation ω_0, and the magnitude variations are nearly zero, which occurs when:

$$\frac{dA_i}{dt} = 0 \; and \; \frac{d\theta_i}{dt} = \omega_0 \;\; i = 1,2,\dots,N \tag{14}$$

By substituting (14) in (13) and considering that k_{ij} is real, we obtain

$$\omega_0 = \omega_i - \frac{\omega_i}{2Q} \sum_{j=1}^{N} k_{ij} \frac{A_j}{A_i} sin(\theta_j - \theta_i) \tag{15}$$

Now, if the coupling network consists of equal sub-networks (y_{ijN}) composed of series resistors Rc connecting adjacent oscillator elements. Thus, using (15), the phase shift obtained for two resistively coupled oscillators is presented below. In this case, oscillators 1 and 2 are two identical oscillators coupled through a resistor Rc, as shown in figure 1.14.

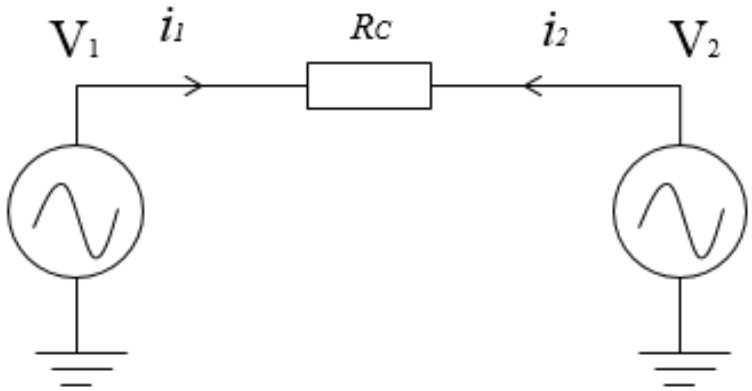


Figure 1.14: Two resistively coupled oscillators

In these conditions, $[Y_{ijN}]$ *is* given by:

$$[Y_{ijN}] = \begin{bmatrix} 1/R_c & -1/R_c \\ -1/R_c & 1/R_c \end{bmatrix} \quad (16)$$

To calculate the constant phase-shift $\Delta\phi$ distribution, we can apply the formula (15) for the oscillators 1 and 2, so that:

$$\omega_0 = \omega_1 + \frac{\omega_1}{2Q}\frac{1}{R_c G_L}\frac{A_2}{A_1}\, sin(\Delta\phi) \quad (17)$$

$$\omega_0 = \omega_2 - \frac{\omega_2}{2Q}\frac{1}{R_c G_L}\frac{A_1}{A_2}\, sin(\Delta\phi) \quad (18)$$

Nevertheless, since the two oscillators are considered identical and for a broadband or resistive coupling circuit, the synchronization frequency is expected to be located between the two oscillators' free-running frequencies [36], so that:

$$\omega_0 = \frac{\omega_2 + \omega_1}{2}$$

Thus, according to (17) and (18), this implies $A_1 = A_2$. In these conditions, the form of the phase difference $\Delta\phi$ is found by subtracting (18) and (17) so that:

$$\frac{\Delta\omega}{\omega_0} = \frac{sin(\Delta\phi)}{QR_c G_L} \quad (19)$$

with $\Delta\omega = \omega_2 - \omega_1$

Hence, the phase shit $\Delta\phi$ can be found as:

$$\Delta\phi = arcsin\left(\frac{\Delta\omega Q R_c G_L}{\omega_0}\right) \quad (20)$$

Thus, (20) proves that the inter-element phase shift $\Delta\phi$ can be adjusted by detuning the free-running frequencies of the oscillators 1 and 2.

3.2.3 Limitations

Theoretically, a 360° phase shift range with a high level of integration and reasonable power consumption can be obtained with such an architecture using differential oscillators. This approach using differential COAs has been implemented using four differential Voltage-Controlled-Oscillators (VCOs) coupled through a resistive network in [34]. However, this

structure suffers mainly from the instability of the synchronised frequency and the maximum inter-element phase shift is limited by the number of VCOs and remains inferior to 360°.

3.3 Phase synthesis by Injection locked Oscillator Array (ILOAs)

Concerning the ILOAs technique, all the oscillators are locked via an external injection signal and each oscillator is independently controlled by adjusting its free-running frequency. A phase difference is then created between the injected signal and the oscillator output. This phase created is controlled by the frequency difference between the free-running frequency of the oscillator and the injected signal frequency. The general architecture of an n-element phased-array transmitter using an ILOA as an active phase shifter allowing to perform beamforming by directly feeding the antenna elements is illustrated in figure 1.15.

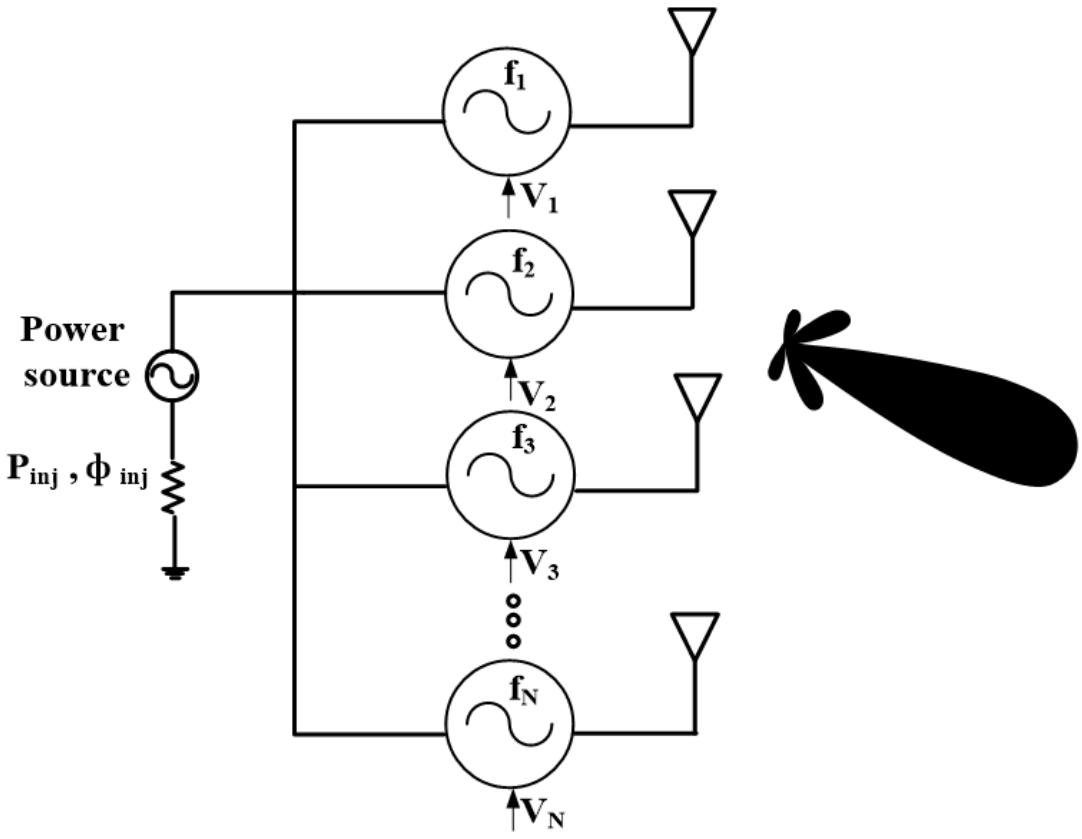


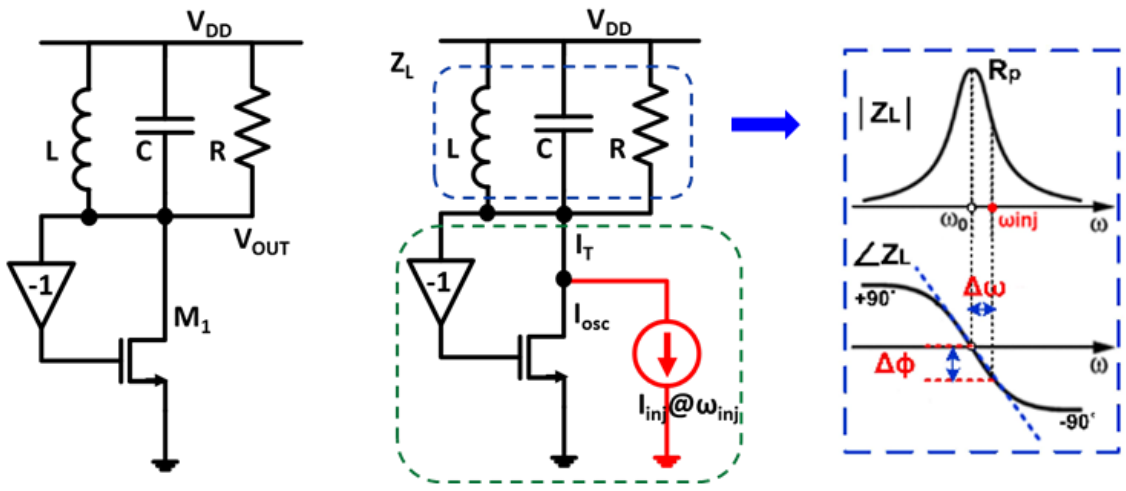
Figure 1.15: General architecture of a phased-array transmitter using an ILOA

With this technique, the synchronisation frequency can be more easily controlled, and therefore, this architecture presents a higher locking probability than the one using a COA. Nevertheless, the major drawback of an ILO is the non-linearity of the phase shift versus the difference between its free-running frequency and the frequency of the injection signal.

Indeed, this phase shift is only almost linear within the ±30° range, thus limiting the maximum phase shift range of the phase shifter. To overcome this issue, an architecture based on an ILO associated with injection locked frequency tripler is proposed in [22]. Although a continuous and linearly phase shift can be obtained, this technique is relatively complex.

3.3.1 Injection locking phenomenon

Injection locking is the frequency effect that occurs when an oscillator is disturbed by a second oscillator operating at a nearby frequency. When the coupling is strong enough, and the frequencies of the oscillators are near enough, the second oscillator can force the first oscillator to synchronise at the same frequency. This phenomenon is known as injection locking. The Dutch scientist, Christiaan Huygens discovered this phenomenon of injection locking in the early 17th century. He discovered that the two clocks on the wall moved in unison if the clocks were hung close to each other. The injection locking phenomenon is mathematically proven through equations by Alder, Kurokawa and many others [37] [38] [39]. To understand the injection locking phenomenon in the oscillators, let us consider the simple LC oscillator schematic shown in figure 1.16(a) [40]. The free-running resonant angular frequency of the oscillator, when $I_{inj} = 0$ is given by $\omega_0 = \sqrt{1/LC}$.



(a) (b)

Figure 1.16: Simplified model of (a) LC oscillator (b) LC oscillator under injection.

When an additional phase ϕ_0 is inserted at the drain of M_1 by adding a sinusoidal current and if the amplitude and the frequency of I_{inj} are appropriately chosen, the circuit oscillates at a new angular frequency ω_{inj} rather than ω_0 and injection locking occurs (figure 1.16(b)) [38].

Derivation of the Locking Equation

Locking range of the injection locked oscillator refers to the range of the frequencies ω_{inj} across which the injection locking holds. From the phasor diagram shown in figure 1.17, the equation of the locking range can be deduced.

Using the trigonometric identity, we obtain the following relation between the I_{osc}, I_{inj} and I_T as follows:

$$\frac{I_{inj}}{\sin \phi_0} = \frac{I_{osc}}{\sin(\theta - \phi_0)} = \frac{I_T}{\sin(\pi - \theta)} \tag{21}$$

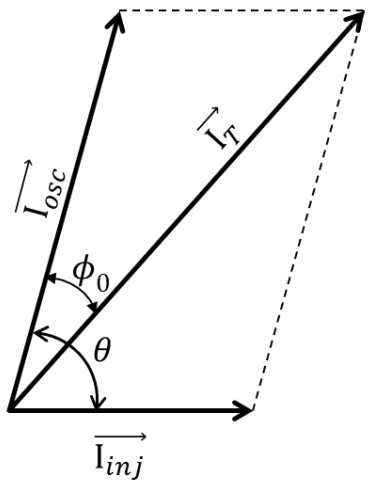


Figure 1.17: Phasor diagram of the ILO of figure 1.16 (b)

$$\frac{I_{osc}}{I_{inj}} = \frac{\sin(\theta - \phi_0)}{\sin \phi_0} = \sin\theta \cot\phi_0 - \cos\theta \tag{22}$$

Again from (21), we obtain:

$$\sin \phi_0 = \frac{I_{inj}}{I_T} \sin\theta \tag{23}$$

$$\frac{I_{osc} + I_{inj} \cos\theta}{I_{inj}} = \sin\theta \cot\phi_0 \tag{24}$$

Hence,

$$\tan \phi_0 = \frac{I_{inj} \sin\theta}{I_{osc} + I_{inj} \cos\theta} \tag{25}$$

Now consider the oscillator with a second-order parallel tank circuit (figure 1.16 (a). This tank circuit consisting of L, R and C exhibit an impedance of:

$$Z\,(j\omega) = \frac{1}{\frac{1}{R} + j\left(\omega C - \frac{1}{\omega L}\right)} = \frac{\frac{1}{R} - j\left(\omega C - \frac{1}{\omega L}\right)}{\frac{1}{R^2} + \left(\omega C - \frac{1}{\omega L}\right)^2} \tag{26}$$

So, the phase shift introduced by the tank circuit when it is near resonance is so that:

$$tan\,\alpha = -\left[\frac{\omega C - \frac{1}{\omega L}}{1/R}\right] = -\left[\frac{R}{\omega L}(\omega^2 LC - 1)\right] \tag{27}$$

$$tan\,\alpha = -\frac{R}{\omega L} LC\left(\omega^2 - \frac{1}{LC}\right) \tag{28}$$

where the following simplifications are used to simplify the solution:

$\omega_0^2 - \omega^2 \approx 2\omega_0(\omega_0 - \omega)\,; Q = R/\omega L\,; \omega_0 = \sqrt{1/LC}$

$$tan\,\alpha = \frac{2Q}{\omega_0}(\omega_0 - \omega) \tag{29}$$

Hence, the phase shift of the tank circuit near resonance by injection locking is given by:

$$tan\,\phi_0 = \frac{2Q}{\omega_0}\left(\omega_0 - \omega_{inj}\right) \tag{30}$$

Equating (25) and (30) we obtain:

$$\frac{2Q}{\omega_0}\left(\omega_0 - \omega_{inj}\right) = \frac{I_{inj}\,sin\,\theta}{I_{osc} + I_{inj}\,cos\,\theta} \tag{31}$$

$$\left(\omega_0 - \omega_{inj}\right) = \frac{\omega_0}{2Q}\frac{I_{inj}\,sin\,\theta}{I_{osc} + I_{inj}\,cos\,\theta} \tag{32}$$

$$\left(\omega_0 - \omega_{inj}\right) = \frac{\omega_0}{2Q}\frac{I_{inj}}{I_{osc}}\frac{sin\,\theta}{(1 + \frac{I_{inj}}{I_{osc}}cos\,\theta)} \tag{33}$$

For weak injection, i.e. $I_{inj} \ll I_{osc}$, (33) is reduced to:

$$(\omega_0 - \omega_{inj}) = \frac{\omega_0}{2Q}\frac{I_{inj}}{I_{osc}} sin\,\theta \tag{34}$$

$$\theta = arcsin\left\{\frac{2Q}{\omega_0}\frac{I_{osc}}{I_{inj}}(\omega_0 - \omega_{inj})\right\} \tag{35}$$

The locking range in low injection level is given at the edge of the locking range, i.e. when the angle reaches 90°. Hence, putting $sin\,\theta = 1$ in (34), we obtain:

$$\omega_{lock} = \frac{\omega_0}{2Q}\frac{I_{inj}}{I_{osc}} \tag{36}$$

where ω_{lock} is called the locking range of the injection-locked oscillator. When the injected signal frequency is tuned over the locking range, i.e. $\omega_0 \pm \omega_{lock}$, the phase difference will vary between $-90° < \theta < +90°$ [41]. The input-output phase difference across the locking range is demonstrated in figure 1.18.

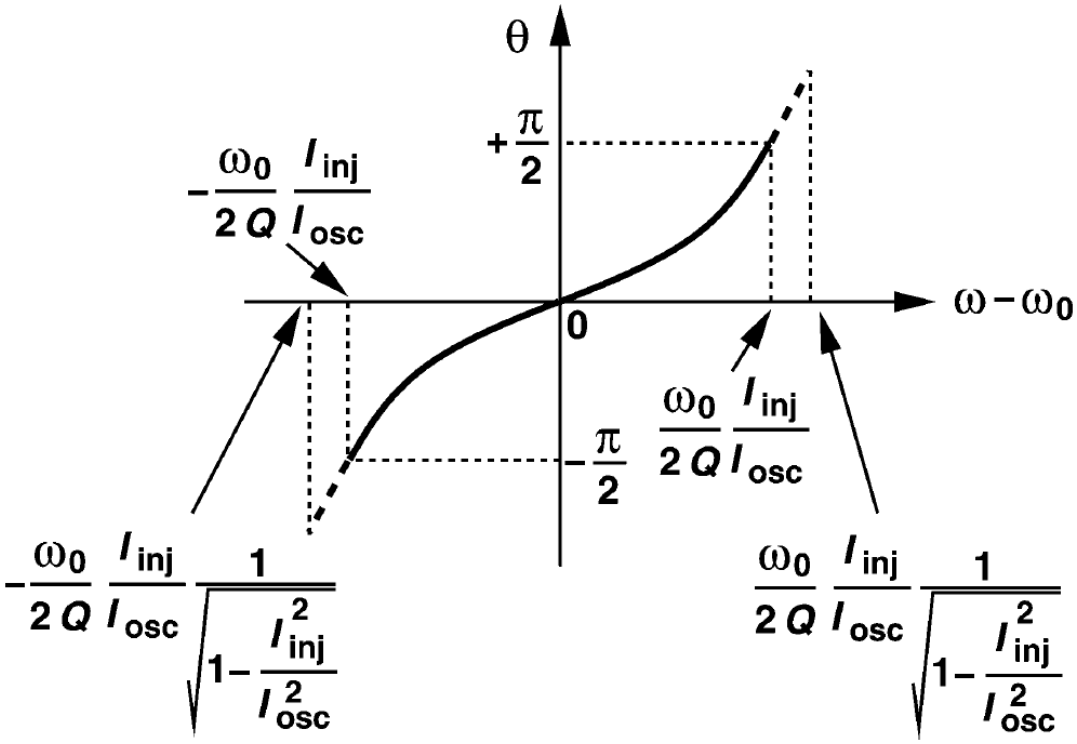


Figure 1.18: Phase shift in an injection locked oscillator [40].

3.3.2 Limitations of ILOs

When an oscillator is injection locked by an external RF signal, its output frequency is equal to the external RF signal frequency and the phase shift is equal to the phase difference

between the input signal and the output signal. This phase shift can be varied by changing the free-running oscillator's frequency within the locking range (ω_{lock}). Approximately, the relationship between this phase shift and the free-running oscillation frequency is presented by (35).

As shown in figure 1.19, when the free-running frequency of the oscillator is varied by the vcontrol voltage of the oscillator, the phase shift Δθ is varied. The phase shift variation is not entirely linear over the locking range. As plotted in figure 1.20 (a), the phase shift is linear within only $\pm 30°$ and nonlinear outside this range [39]. To ensure perfect control of the phase shifter, this nonlinear region is not desirable for the phased array system. In this regard, if the linear phase shift is multiplied by 3, it is possible to obtain a linear phase shift between $\pm 90°$ [22].

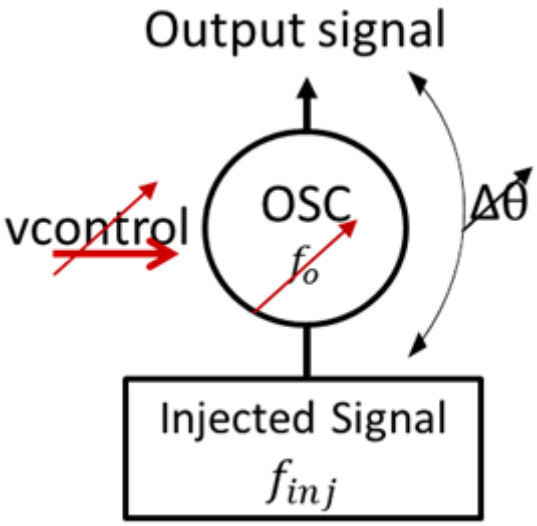


Figure 1.19: Phase variation in an ILO

One of the solutions to obtain the linear phase shift is to use an injection locked triple-push oscillator (ILTPO) instead of an ILO followed by a frequency tripler (figure 1.20(b)). In this thesis, we used an ILTPVCO not only to triple the phase shift but also because the phase shifter needs to operate at 1/3 of the output frequency. Therefore, the ILTPVCO is linearly tuned from -30° to 30° to obtain an effective linear phase shift range from -90° to 90° at the triple-push output. The linearity error calculated in figure 1.21, at ±30°, remains less than 4.46%. Hence the phase shift range will be more linear between ±90°. Furthermore, a full linear phase shift range from -180° to 180° will be obtained by using differential oscillators.

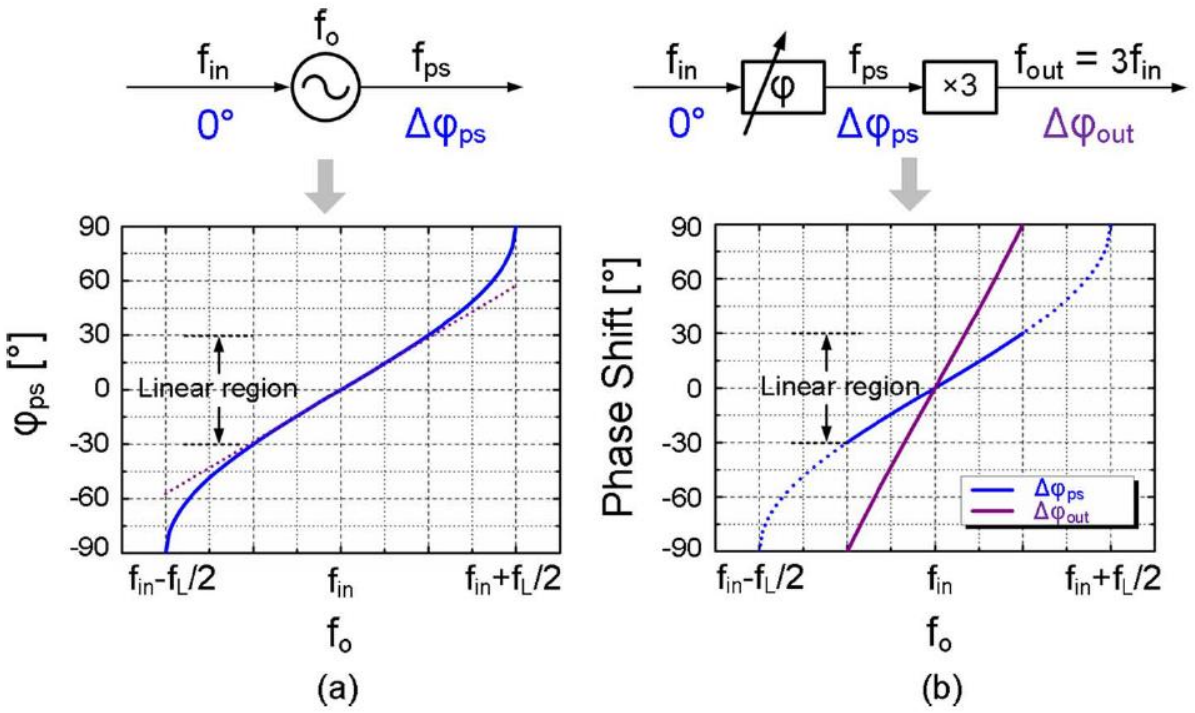


Figure 1. 20: (a) Phase shift variation of an injection locked oscillator, (b) Linear Phase shift variation by using a frequency tripler [22].

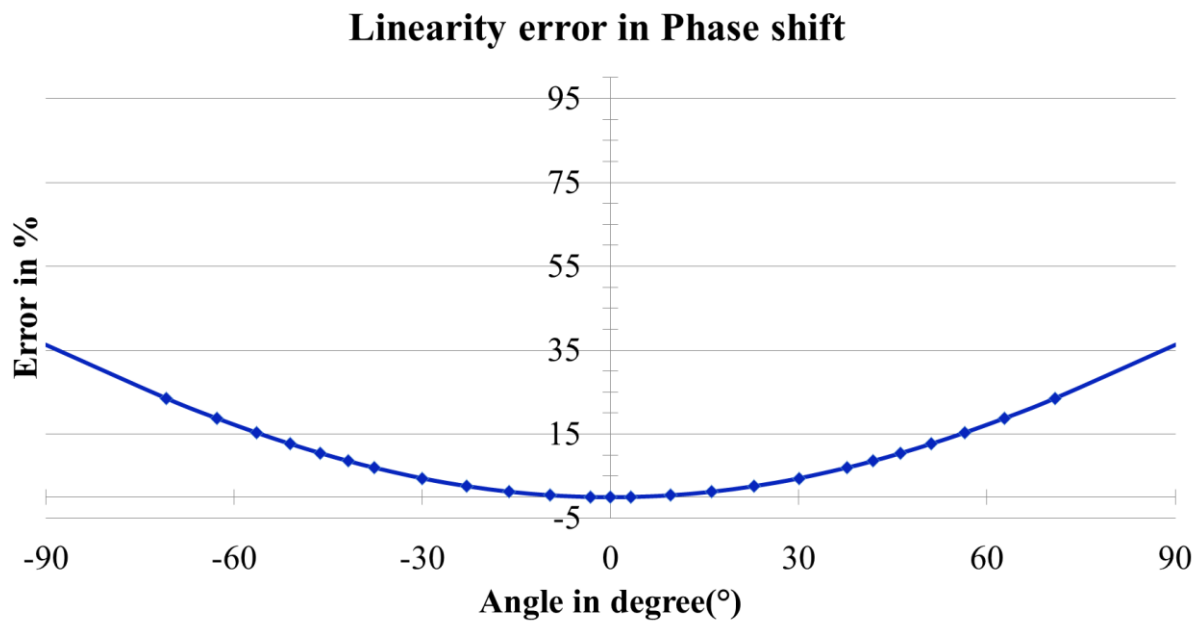


Figure 1.21: Calculated linearity error of the phase shift obtained by injection locking in the oscillator.

3.4 Controlling the shape of the radiation pattern of an antenna array through injection locked oscillator array

As illustrated in section 2.4, the shape of the radiation pattern of the antenna array can be controlled by the varying the phase applied on each element of the antenna array. The approach to steer the radiation pattern of the linear antenna array using injection locked oscillators is illustrated in figure 1.22, where:

- *N* – is the number of the antenna array elements;
- θ – the primary lobe steering angle - is the angle between *z*-axis and the vector that links the origin of the coordinate system with an arbitrary point chosen in the far-field, and *r* is the distance between them;
- *d* – is the distance between two adjacent elements of the array;

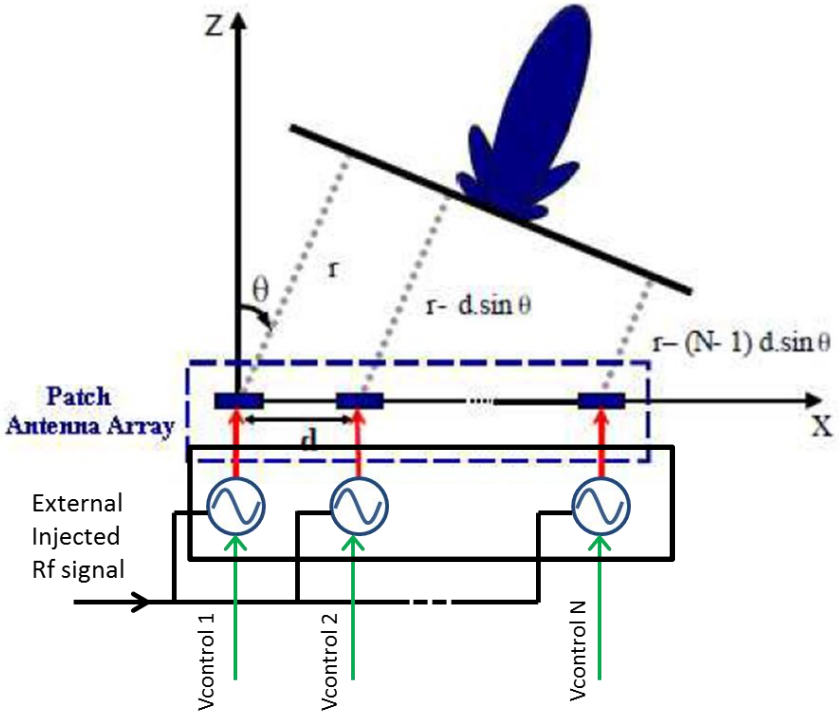


Figure 1.22: Block diagram of an antenna array controlled by an ILOA.

The radiation pattern of the antenna array is successfully controlled when all the oscillators of the control circuit are synchronised at the same time, and they satisfy the desired phase requirement to the elements of the antenna array. The injection locking phenomenon accomplishes both the requirements. The externally injected signal synchronises all the

oscillators to a common injected frequency. The most important and delicate part is to provide the proper phase to the elements of the antenna array. The required phase is provided by changing the free-running frequency of the oscillators while the oscillator is locked by the external signal within the locking bandwidth of the injection locked oscillator.

Linear antenna array has the limitation to scan in the 2-D space, and it is one of the essential requirement for the portable devices to scan the main beam in both elevation and azimuthal directions [42] [43]. In the case of a planar antenna array, ILOAs provides an ease to achieve the required phase on each element of the antenna array. Consider figure 1.23 demonstrating the injection locked planar antenna array. An external injection frequency ω_{inj} synchronises all the oscillators to the same frequency. Now when each oscillator is detuned to provide the required phase relationship between the elements of the antenna array, successful scanning of the beam is achieved. The main advantage of the injection locked oscillators over coupled oscillators is the ease to achieve the required phase shift when the number of elements of the antenna array is increased. Each oscillator can be separately controlled, which is not possible with coupled oscillator arrays [41].

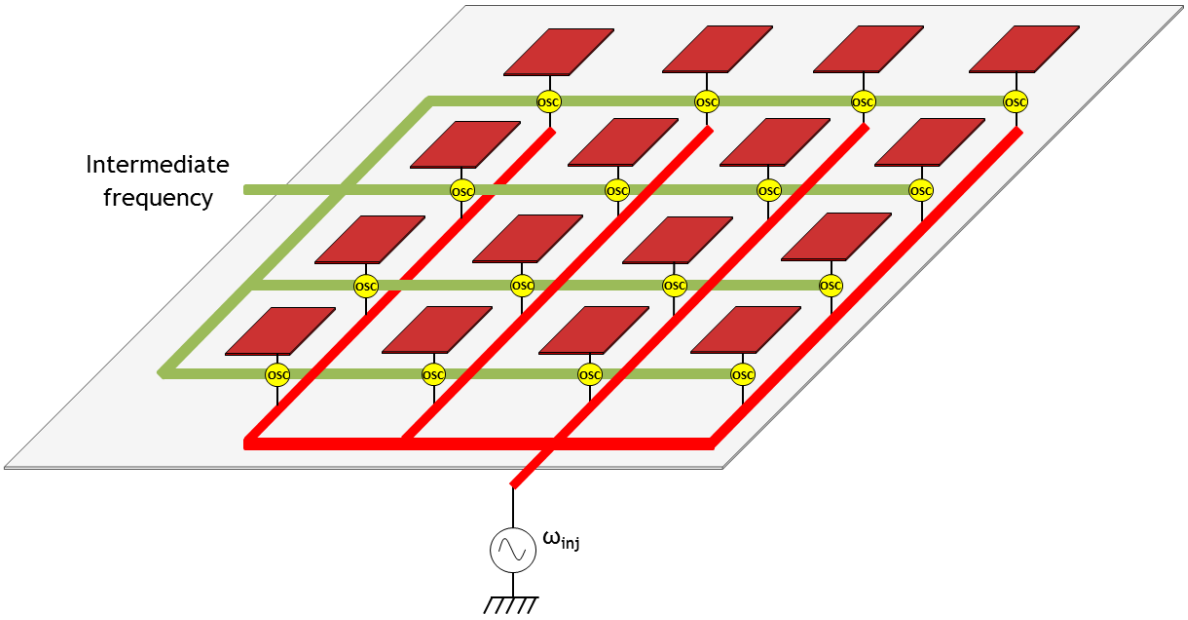


Figure 1.23: Injection locking in a planar antenna array.

In the particular case of the hybrid antenna array, where some radiating elements of the antenna array are deleted/deactivated, the complexity of the commanding is reduced [44]. As shown in Fig 1.24, it is possible to command only some of the radiating elements of the antenna array and provide the required beamforming of the radiation pattern. Injection locking

in hybrid antennas is thus an attractive choice as it reduces the complexity/cost of the circuit and makes the system more robust with better performances.

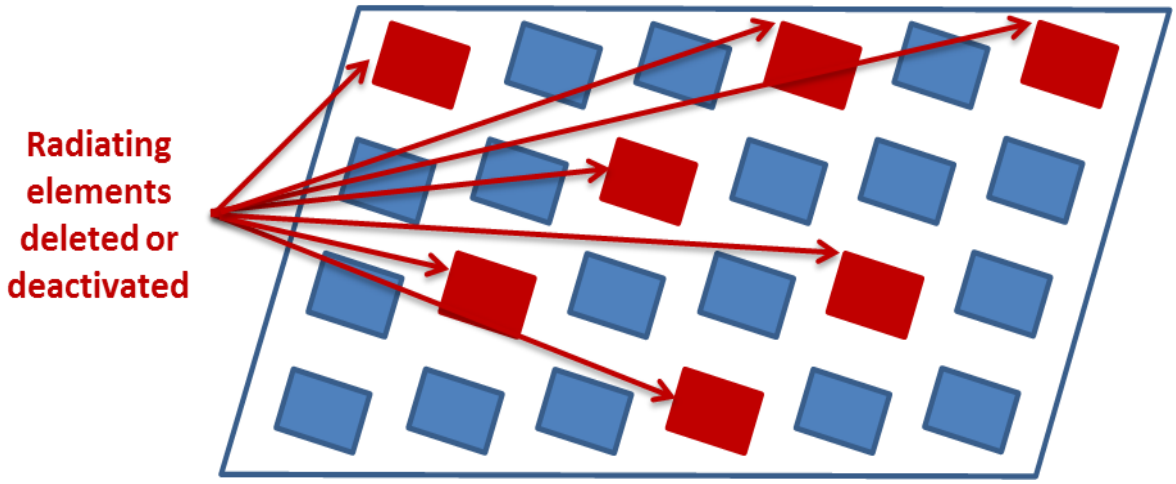


Figure 1.24: Schematic of a hybrid antenna array

4 The objective of the dissertation

The goal of this thesis is to design an active phase shifter, in the millimetre wave domain, for the application of beamforming in 5G technology. When it is associated with an antenna array, this circuit performs beamforming, i.e. it allows the orientation and control of the radiation pattern in the desired direction. In millimetre waves, the ability to steer the beam allows to compensate for the losses due to the increase in frequency. This new circuit ensures a tunable RF phase shift between the input and the output. It is based on an original Injection Locked Triple-Push Voltage Controlled Oscillator (ILTPVCO) at 8 GHz. In these conditions, the frequency of the output signal is at 24 GHz. The objective of this dissertation is to design this fully integrated active RF phase shifter implemented in the QUBiC4X 0.25 µm SiGe:C BiCMOS process of NXP semiconductors.

To achieve this goal, a triple-push differential voltage controlled oscillator is designed at 24 GHz. The design and the implementation of this triple-push VCO are detailed in the second chapter. Post layout simulation results are presented along with the comparison of the triple-push circuit with the state of the art.

The third chapter is dedicated to the active phase shifters. In order to perform the injection locking in the triple-push VCO, a differential 120° tuneable active phase shifter is designed and integrated in the QUBiC4X 0.25 µm SiGe:C BiCMOS process of NXP

semiconductors. This 120° active phase shifter is used to provide the injection locking in the triple-push VCO. A global circuit is designed, combining the 120° phase shifter and the triple-push VCO to control the elements of the antenna array linearly throughout the 360° phase plane (figure 1.25).

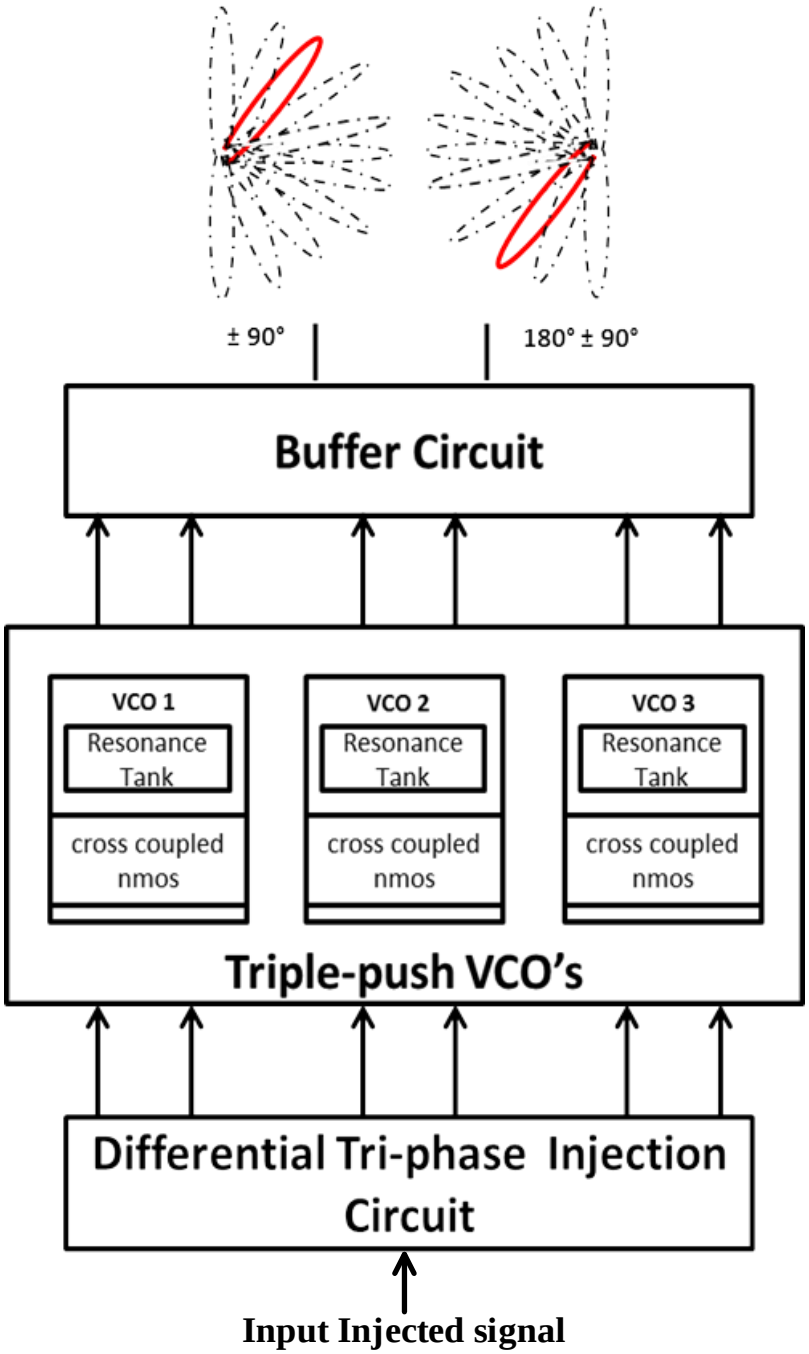


Figure 1 25: The architecture of the proposed active phase shifter.

5 Conclusion

This chapter allows us to introduce the context and framework of this dissertation. In this first chapter, we have briefed the future vision of the 5G technology, its key capabilities, applications and different research challenges from where we obtain the motivation of the thesis. The beamforming of an antenna array is discussed with different techniques to control its radiation pattern. We have reviewed the state of the art of different methods to control the radiation pattern by phase synthesis.

Finally, the objective of the thesis is presented by providing the new architecture of the injection locked triple-push voltage controlled oscillator. This thesis presents the analysis and design of a new 24 GHz active phase shifter, integrated in a BiCMOS SiGe:C 0.25 µm technology for the beamforming application in 5G technology.

Chapter II: Behavioural analysis of triple-push VCO and design of a new triple-push VCO

Table of Contents

Chapter II: Behavioural analysis of triple-push VCO and design of a new triple-push VCO 44

Introduction 48

1. Triple-push Oscillators 49

1.1. Triple-push Oscillator principle 50

1.2. Oscillation modes analysis in a triple-push oscillator 51

1.3. Different architectures of the triple-push 53

2. Design of the differential elementary VCO 55

2.1. Resonance tank design 57

2.2. Active part design 62

2.3. The layout of the VCO 63

3. Design of the differential triple-push VCO 67

3.1. Design of the output stage amplifier and buffer 68

3.2. The layout of the Triple-Push VCO 71

3.3. The Post layout simulation results of the TPVCO 72

4. Conclusion 76

Introduction

In the context of IoTs, thanks to the mm-wave transmissions, 5G technology allow faster data transmission for mobile applications. Such a high data rate (in Gbps) allows significant simplification of connected device management. According to the Cisco IBSG, 50 billion devices will be connected to the internet in 2020 compared to 8 billion people. High-frequency sources are one of the critical requirements in the mm-wave systems and are especially needed for 5G technology. They have remarkable applications in advanced imaging, remote sensing applications, communication systems and radar systems. Also, the requirements for the 5G spectrum are progressively up to 100 GHz in 5G.

Tremendous demand in the application of communication systems has boosted up the attention in wireless architecture and applications. Integrated Voltage Controlled Oscillators (VCOs) are essential building elements in the implementation of a single chip radio in today's communication systems. However, the oscillation frequency of a fundamental frequency oscillator is limited to the maximum frequency of oscillation (f_{max}) of the transistors. Triple-push oscillator is one of the efficient solutions to work at higher frequencies. Triple-push oscillator design consists of three fundamental oscillators operating at 120° phase shift to each other and working at one-third of the desired output signal frequency. The stability of a triple-push oscillator is to operate strictly in odd mode (to obtain the 3rd harmonic) and avoid the even mode, is a critical phenomenon. Hence, in this chapter, we present the design and implementation of a differential triple-push VCO. The chapter starts with the brief theory of the triple-push oscillators and its mode analysis. Different triple-push oscillators around 20-40 GHz designed previously is reviewed, and different architectures of previous triple-push oscillators are analysed. A new architecture of a differential triple-push VCO is proposed here. It consists in operating the coupling through the varactor diodes and separating the output 3rd harmonic from the coupling circuit. The circuit is implemented in the QUBiC4X 0.25 µm SiGe:C BiCMOS process of NXP semiconductors. Finally, the post layout simulation results are presented.

This triple-push VCO will be used to design an active phase shifter for the application of beamforming in 5G technology. A 120° phase-shifting circuit will be used to injection lock the triple-push VCO in order to obtain phase shifting at 24 GHz.

1. Triple-push Oscillators

The increasing demand for the larger bandwidth to support the mobile communications for 5G technology has resulted in demand for the higher operating frequencies in the marketplace. A high-frequency signal can be generated either based on an oscillator operating at fundamental or harmonic frequencies. Due to the low Q-factor, insufficient device gain and higher phase noise at the high frequency of oscillation, typical fundamental oscillators are not recommended at very high frequencies. The VCO doubler provides a quick solution to generate high-frequency signals from oscillators operating at half frequency, but it introduces additional multiplication, filtering and amplification required for complete VCO doubler architecture [45]. A better solution to avoid the above mention problems is to use push-push oscillators or triple-push oscillators. A push-push oscillator, as shown in figure 2.1 (a), is formed by two basic sub oscillators oscillating at a frequency f_0. This topology is generally used to synthesize a double frequency $2f_0$ at the output. To generate the double frequency $2f_0$, the sub oscillator output signals must have the same amplitude but opposite in phase. Consequently, the odd harmonics at the output signal cancel each other, and the even harmonics are added together [46].

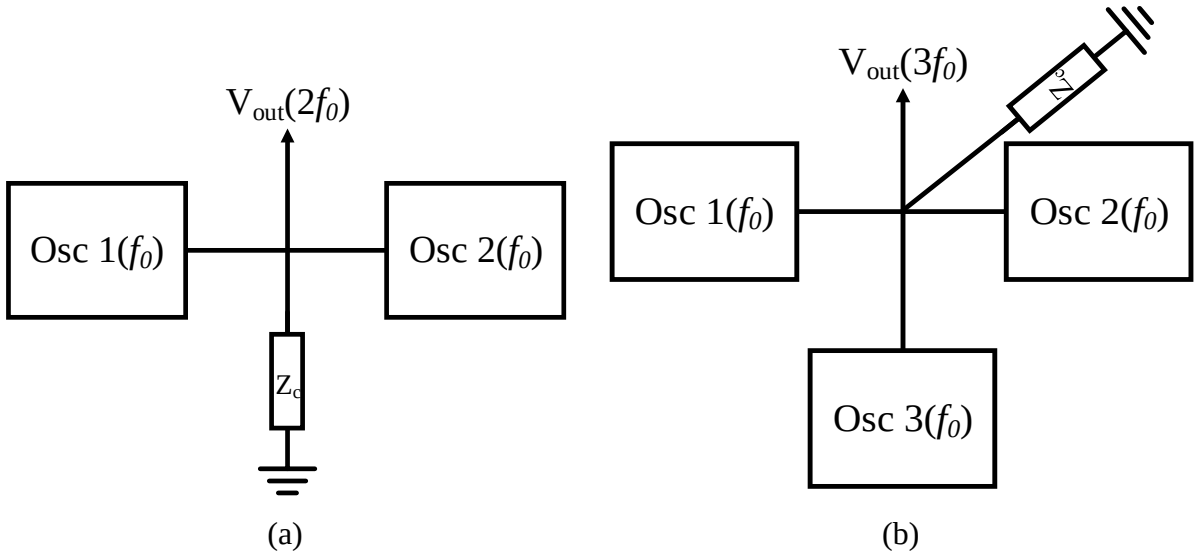


Figure 2.1: Design of (a) Push-push oscillator and (b) Triple-push oscillator

Similarly, in a triple-push oscillator (figure 2.1(b)), three sub oscillators are coupled together where the sub-oscillators operate at the 1/3rd operating frequency. The three sub oscillators have the same amplitude and 120° phase between them. In the following section, a detailed description of the triple-push approach is presented.

1.1. Triple-push Oscillator principle

Triple-push oscillator (TPO) approach was proposed in [47] for the first time. Triple-push oscillator design consists of three fundamental oscillators operating at one-third of the desired output signal frequency. A coupling circuit (active or passive) couples the three VCOs together. The coupling circuit allows synchronising the output signals of the three VCOs at 120° from each other [48]. Consequently, the second harmonics of the three output signals are 240° out of phase, whereas the third harmonics are in phase. By adding the signals of these three VCOs, which is get through the coupling circuit, then, the fundamental and the second harmonic of the three VCOs outputs are suppressed whereas the third harmonic component, i.e., the desired output frequency, is combined in phase as demonstrated by the following equations and illustrated in figure 2.2:

$$V_1(t) = a_1 e^{j\omega_o t} + a_2 e^{2j\omega_o t} + a_3 e^{3j\omega_o t} \quad (1)$$

$$V_2(t) = a_1 e^{j(\omega_o t + \frac{2\pi}{3})} + a_2 e^{j\left(2\omega_o t + \frac{4\pi}{3}\right)} + a_3 e^{j(3\omega_o t + 2\pi)} \quad (2)$$

$$V_3(t) = a_1 e^{j(\omega_o t + \frac{4\pi}{3})} + a_2 e^{j\left(2\omega_o t + \frac{8\pi}{3}\right)} + a_3 e^{j(3\omega_o t + 4\pi)} \quad (3)$$

$$V(t) = V_1(t) + V_2(t) + V_3(t) = 3a_3 e^{3j\omega_o t} \quad (4)$$

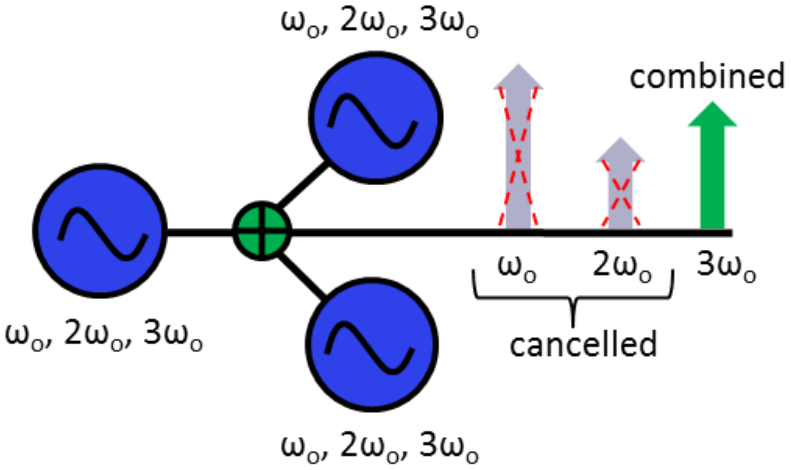


Figure 2.2: Triple-push oscillator operation.

Nevertheless, the amplitude and phase mismatch between the three VCOs outputs have an important impact on the performances of the triple-push VCO. It reduces the output power and lowers the rejection of the fundamental and the second harmonic signals.

1.2. Oscillation modes analysis in a triple-push oscillator

In a triple-push oscillator, either an even mode or odd mode can exist [48]. In the odd mode operation of the triple-push, the fundamental signals of the three oscillators are 120° out of phase. Whereas in even mode operation of the triple-push, the fundamental signals of the three oscillators are in phase. In order to obtain the third harmonic signal, it is absolutely necessary to work in the odd mode. Consider a model of a triple-push VCO operating in the odd mode as shown in figure 2.3(a), where a passive coupling is performed through the varactor diode. To ensure the triple-push operation in odd mode, the three VCOs are coupled through an impedance Rc. Here, the coupling impedance R_c appears as a virtual ground at the coupling node in odd mode. The triple-push oscillator equivalent circuit model in odd mode is shown in figure 2.3(b).

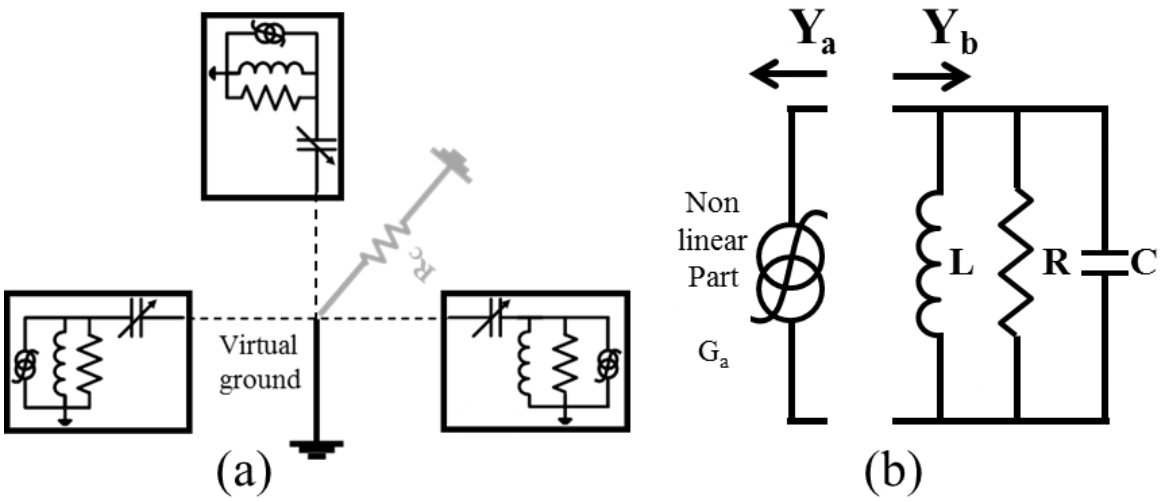


Figure 2.3: Triple-push equivalent circuit model in the odd mode.

$Y_a(\omega)$ and $Y_b(\omega)$ represent the admittances of the active and passive parts, respectively in the odd mode of oscillations. As a consequence, the oscillation startup condition in the odd mode is given by:

$$|R_e(Y_a)| = |G_a| > \frac{1}{R} \tag{5}$$

where $\omega_0=1/(LC)$ is the pulsation of oscillation and G_a is the real part of $Y_a(\omega_0)$.

In the even mode, the output signals of the three oscillators are in phase. Hence, the coupling resistor R_c appears as $3R_c$ at the coupling node because the current through the Rc resistance is the sum of the three currents, as shown in figure 2.4(a). In these conditions, the

triple-push equivalent circuit model in the even mode is shown in Fig. 2.4(b). The coupling resistor in the even mode appears in series with the equivalent capacitor since the coupling is performed through the varactor diode in this design. Hence, we can write:

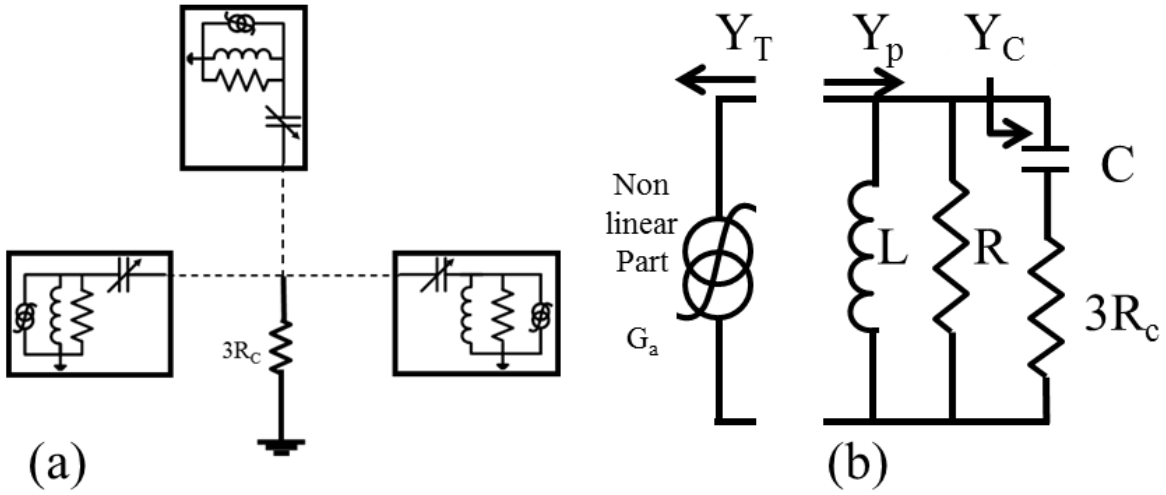


Figure 2.4: Triple-push equivalent circuit model in even mode

$$Z_c(\omega) = \frac{1 + j\omega C 3R_c}{j\omega C} \tag{6}$$

$$Y_c(\omega) = \frac{1}{Z_c} = \frac{j\omega C}{1 + j\omega C 3R_c} \tag{7}$$

$$Y_c(\omega) = \frac{3\omega^2 C^2 R_c}{1 + 9\omega^2 C^2 {R_c}^2} + \frac{jC\omega}{1 + 9\omega^2 C^2 {R_c}^2} \tag{8}$$

$$Y_c(\omega) = A_c(\omega) + jB_c(\omega) \tag{9}$$

$Y_T(\omega)$ and $Y_p(\omega)$ represent the admittances of the active and passive parts in the even mode of oscillations. Thus, the oscillation start-up condition for even mode oscillation is given by:

$$|G_a| > \frac{1}{R} + A_c(\omega_o) \tag{10}$$

$$Y_p(\omega) = \left(\frac{1}{R} + A_c(\omega)\right) + j\left(B_c(\omega) - \frac{1}{L\omega}\right) \tag{11}$$

The triple-push must strictly oscillate in the odd mode to cancel the fundamental and second harmonics. The value of the coupling resistance and negative transconductance of the

oscillator is chosen with outmost care such that the triple-push oscillator operates only in the odd mode (figure 2.5).

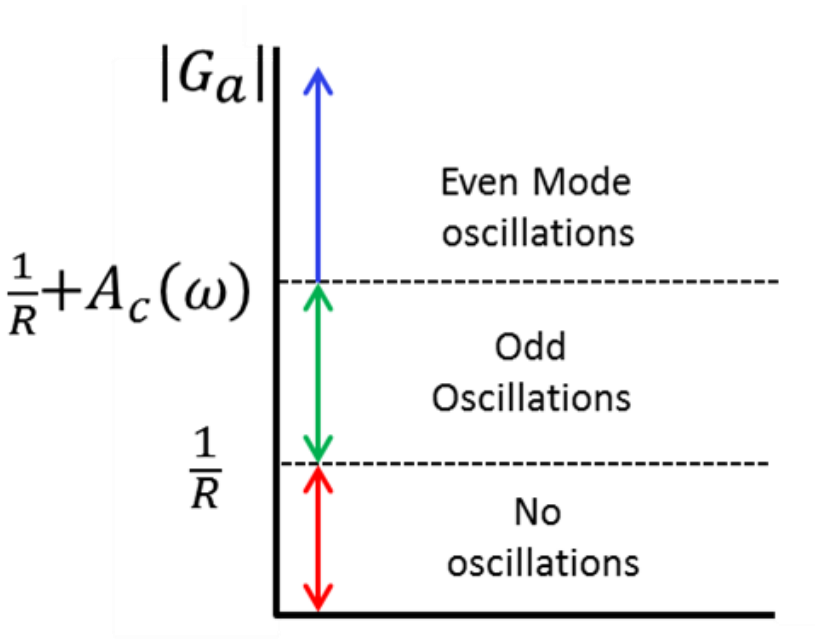
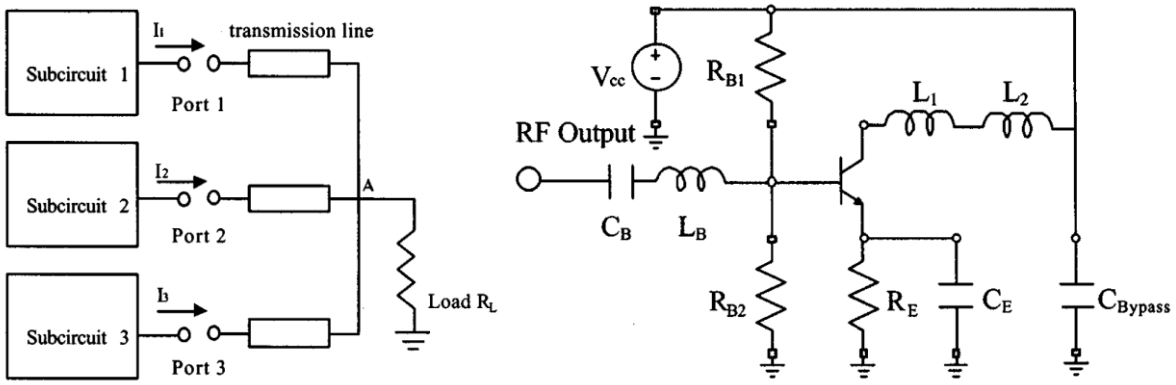


Figure 2.5: Different modes of oscillations for the triple-push oscillator

1.3.Different architectures of the triple-push

In the past, different types of triple-push oscillators architectures have been proposed. Yu-Long Tang and Huei Wang proposed the first architecture as shown in figure 2.6 [47]. They used transmission lines to combine the three single ended sub-oscillators' output to obtain the triple-push behaviour at 4.86 GHz. This was the first-ever triple-push reported in the literature. The rejection of the fundamental and second harmonic were 12.67 dB and 16.17 dB respectively. Later, more triple-push oscillators were fabricated using the same architecture topology to enhance the rejection of the fundamental and the second harmonic signals [45] [48] [49] [50] [51]. Generally, in this architecture, the three fundamental oscillators are coupled using a transmission line and the output is also taken at the same point. This is the major disadvantage of this architecture as the stability of the circuit is complicated. The most important and delicate part to design a triple-push oscillator is to make sure that the output of the three oscillators are at 120° to each other (odd mode). It depends on the oscillation mode through the coupling circuit of the triple-push oscillator. When the buffer circuit is added to increase the output power, the stability of the circuit in odd mode becomes more complicated to obtain.

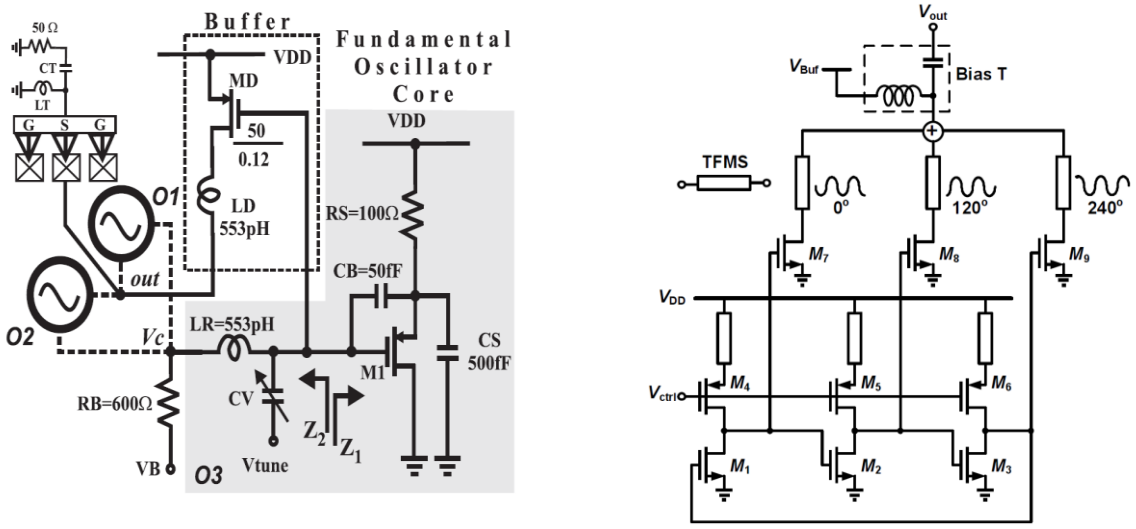


(a) (b)

Figure 2.6: (a)Triple-push architecture by Yu-Long Tang and Huei Wang [47], (b) Architecture of the subcircuit oscillator.

In [52], the authors provide a better solution to separate the coupling circuit from the output circuit. As shown in figure 2.7(a), the three oscillators are coupled at "V_c" and the output is taken through the buffer at "*out*". The stability of the triple-push oscillator in odd mode is guaranteed by the coupling circuit and at the same time, the output of the third harmonics can be increased by the buffer circuit.

However, there is a trade-off between increasing the third harmonic output and the total power consumption. The bias voltage is set to a higher voltage value than the minimum required to enable the driver stage to enhance the output power level. This increase causes the saturation of the signal swing at the fundamental oscillators, wasting some portion of the total DC power consumption and affecting the phase noise performances [53].



(a) (b)

Figure 2. 7: Triple-push architectures (a) by B Çatli and M M Hella [52], (b) by C C Li, C C Chen, B J Huang, P C Huang, K Y Lin, and H Wang [54]

Another impressive triple-push oscillator architecture is using ring oscillators [54] [55] [56]. The advantage of this architecture is that in ring oscillators, the three oscillators are well synchronised at 120° to each other fulfilling the compulsory requirement of the triple-push principle. The thin-film microstrip (TFMS) line is used to combine the three signals in order to extract the third harmonic (figure 2.7(b)). This topology provides the advantage of a wide tuning range. Nevertheless, it is not adapted to our case because when an external injection signal is applied to the triple-push, the three oscillators are not synchronised to 120° to each other anymore and the third harmonics level is reduced.

Hence, we designed here a new differential triple-push oscillator considering the shortcomings of the already existing architectures as mentioned above. We will discuss more in detail the design of the proposed triple-push oscillator in the section 3 of this chapter.

2. Design of the differential elementary VCO

An oscillator is composed of two parts: the active part, which provides the energy to compensate for the tank losses and the passive part, which sets the oscillation frequency.

The LC VCO designed in this thesis is implemented in the QUBiC4X BiCMOS SiGe:C 0.25 µm process developed by NXP Semiconductors. This technology has five levels of metallization with a substrate whose resistivity is 200 Ω.cm. High qualities of passive components such as MIM capacitors are available in this technology and inductors are designed with the highest level of metallisation with a low resistivity of 10.5 mΩ/sq. The available NMOS transistors are capable of operating up to 60 GHz. The LC VCO used in this design is made of a classical NMOS cross-coupled differential topology, as shown in figure 2.8.

The LC tank is made of one symmetric centre-tapped differential inductor and two single ended varactor diodes controlled by the tuning voltage *Vtune*. The cross-coupled NMOS differential pair provides a negative resistance to compensate for the tank losses over the entire tuning range.

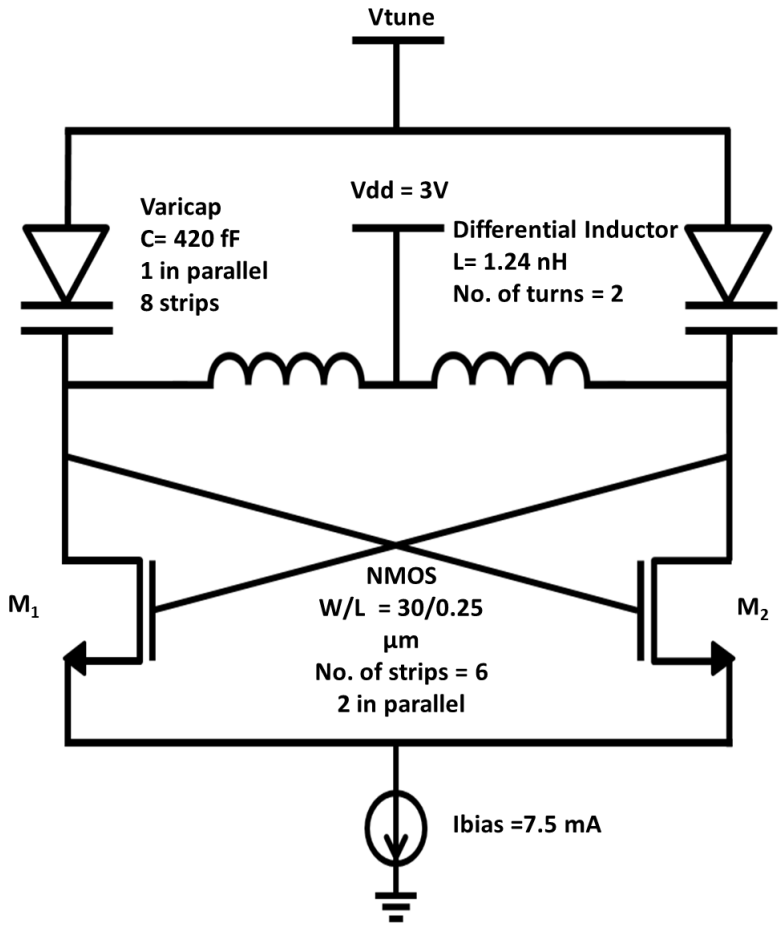


Figure 2.8: Schematic of the differential LC VCO

Consider the small-signal and low-frequency analysis of the LC VCO as shown in figure 2.9. The input of each transistor in the differential pair has been connected to the output of the opposite transistor. The differential voltage is given by:

$$V_{in} = V_{gs1} - V_{gs2} \tag{12}$$

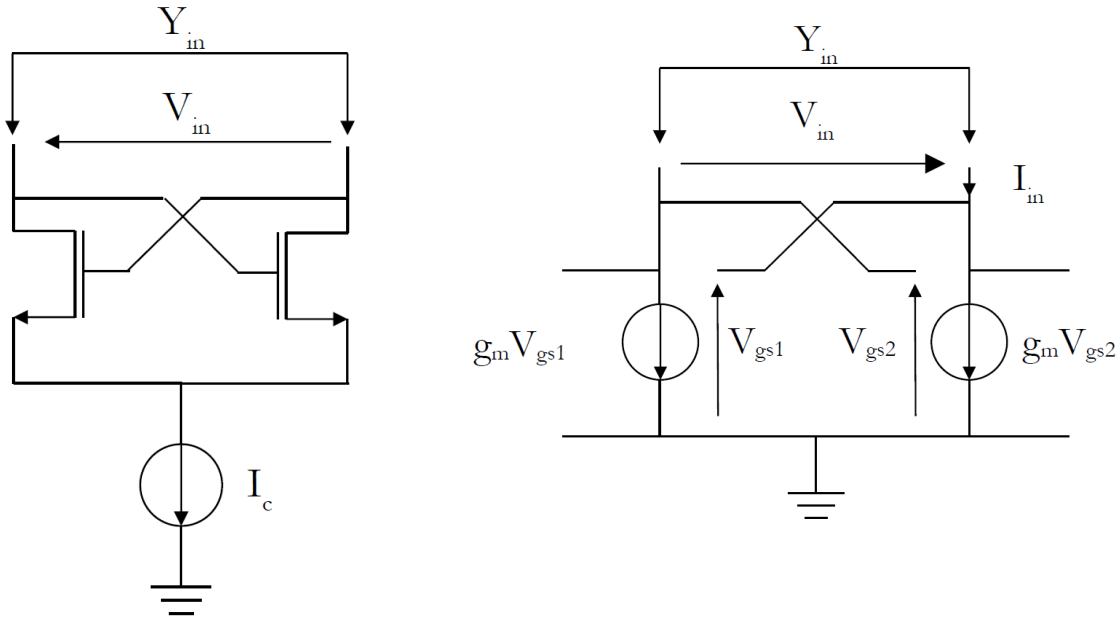
and

$$I_{in} = g_m V_{gs2} = -g_m V_{gs1} \tag{13}$$

Putting (13) in (12), it comes:

$$V_{in} = I_{in}.\left(\frac{-1}{g_m} - \frac{1}{g_m}\right) \tag{14}$$

$$Y_{in} = \frac{-g_m}{2} \tag{15}$$



(a) (b)

Figure 2.9: (a) Admittance Y_{in} presented to the resonance tank, (b) Schematic for the small-signal and low-frequency analysis of the cross-coupled NMOS differential pair.

Hence, this means that to start the oscillations, it is necessary that:

$$g_m > \frac{2}{r_p} \tag{16}$$

where r_p is the parallel equivalent resistance of the resonator.

The LC VCO designed in this thesis comprises of a differential inductor, two single ended varactor diodes and cross-coupled NMOS transistor. The brief description of the passive resonance part is discussed in the following section followed by the active part.

2.1.Resonance tank design

The resonance tank we have chosen in this design comprises a differential inductor and two single ended varactor diodes. The LC tank is designed to resonate at 8 GHz. The values of the inductor and varactor diodes are chosen to obtain a synchronisation over a broad bandwidth around 8 GHz, with a higher third harmonic component in the output signal.

Inductor design

The QUBiC4X library of the NXP Semiconductor design kit provides inbuilt differential inductor models. The differential inductor is an octagonal coil. As shown in figure

2.10, input pins A and B are on the bottom side. The Center Tap can be present or not. This inductor can have several turns, using METAL6/VIA M5_M6/METAL5 for the crossover. Two cells are available: indsymS and indsymSnoCt. Cell indsymS is a differential octagonal inductor with poly shield and Center Tap (CT). Cell indsymSnoCt is a differential octagonal inductor with poly shield and without center Tap.

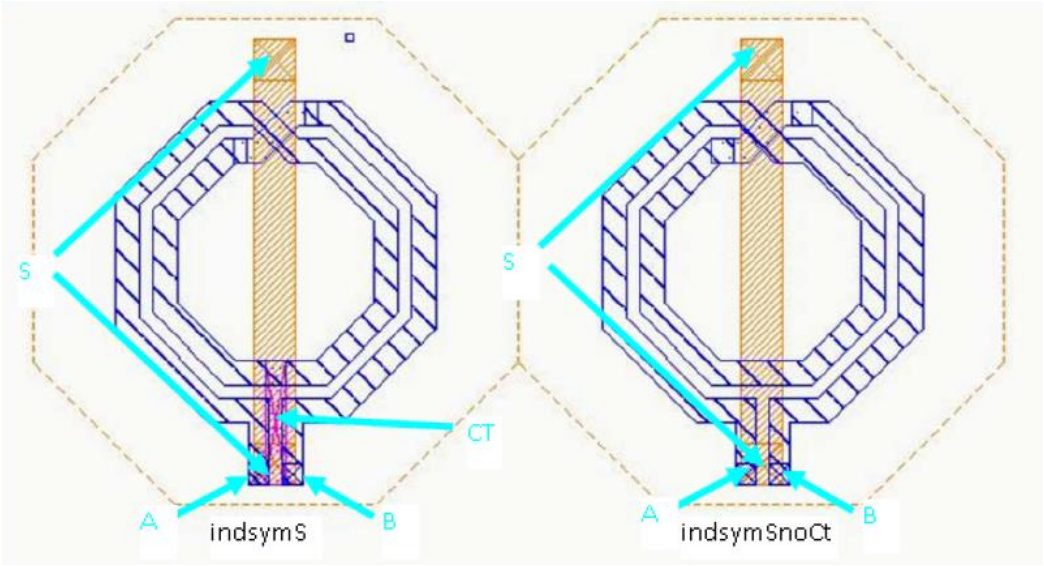


Figure 2.10: Layouts of the shielded octagonal inductors with and without center tap.

The parameters of the inductors are chosen in accordance to obtain the maximum third harmonics when used in the triple-push VCO. The inductance value depends on its geometry, such as the number of turns, the spacing between turns, the diameter of the winding and the width of the winding. The quality factor of the differential inductor is given as [57]:

$$QF_{ind} = \frac{Im(Z_{11} + Z_{22} - Z_{12} - Z_{21})}{Re(Z_{11} + Z_{22} - Z_{12} - Z_{21})} \quad (17)$$

The physical dimensional parameters of the inductor (L= 1.236 nH) used in the design of our LC VCO are presented in Table 2.1.

Table 2.1: Physical characteristics of the Inductor

Inner Diameter of the coil	**150 µm**
Number of windings	**2**
Width of the winding	**10 µm**
Space between the windings	**10 µm**
Space between the pins	**3 µm**
Width of the centre tap pin	**8 µm**

The layout design of the inductor is shown in figure 2.11. The inductor occupies an area of "229.5 x 230.2 μm^2".

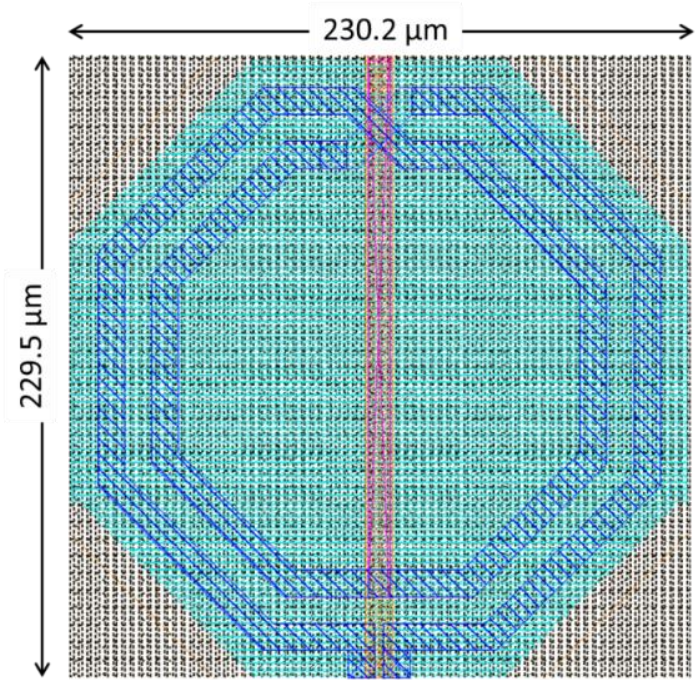


Figure 2.11: Layout view of the octagonal differential inductor in QUBiC4X library

Figure 2.12 shows the variation of the inductance quality factor with respect to the frequency. The quality factor of the chosen inductor is 21.77 at 8 GHz.

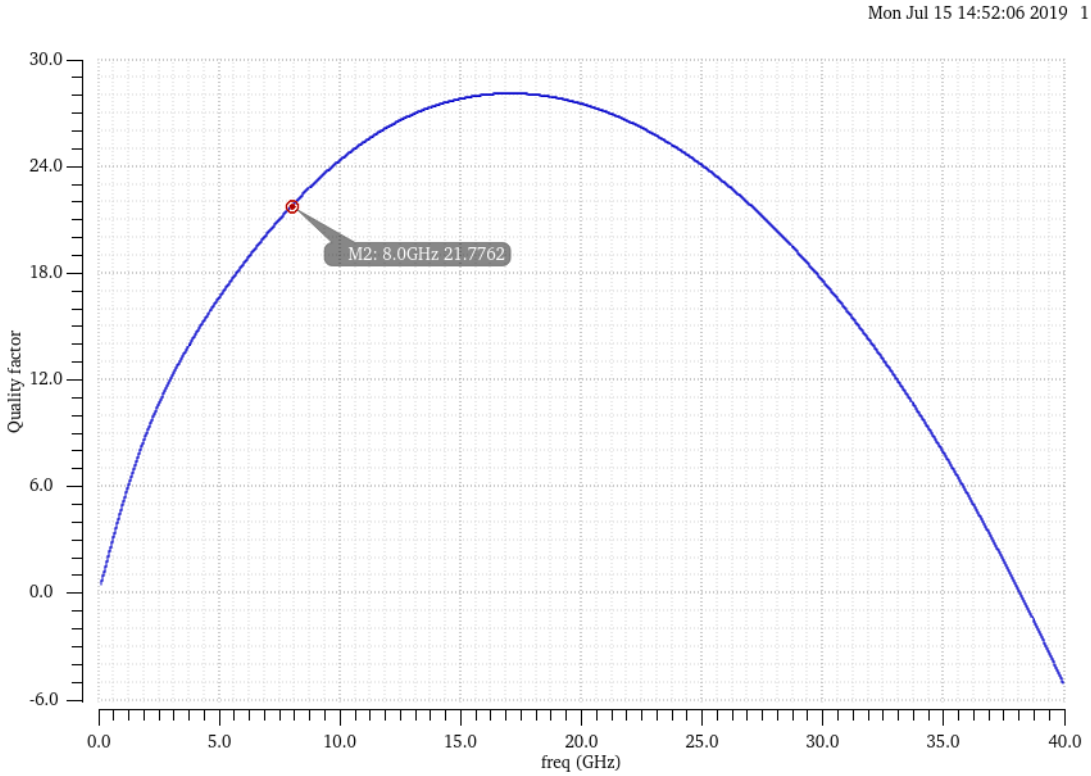


Figure 2.12: The simulated Quality factor of the differential inductor

Varactor diodes design

The varactor diode chosen in this structure is the single ended varactor diode. The choice of the single ended varactor diodes instead of differential diodes is justify by the fact that we will design a triple-push VCO. The advantages of this choice are explained in section 3 of this chapter. The varactor diode used for the design has the following parameters:

- W = 10 µm
- L = 2.025 µm
- Number of strips = 8
- Number in parallel = 1

The dimension of the varactor diode is accordingly chosen so as to obtain an important C_{max}/C_{min} ratio while maintaining the quality factor to a high value. If C_{max}/C_{min} ratio is larger, the transition zone is very steep and therefore the frequency change will take place over a short range of tuning voltage (*Vtune*). With these parameters chosen as mentioned above, the varactor diode has a C_{max}/C_{min} ratio of 2 at 8 GHz. The characteristic C (*Vtune*) is given in figure 2.13 and is obtained using equation (13) taken at f = 8 GHz.

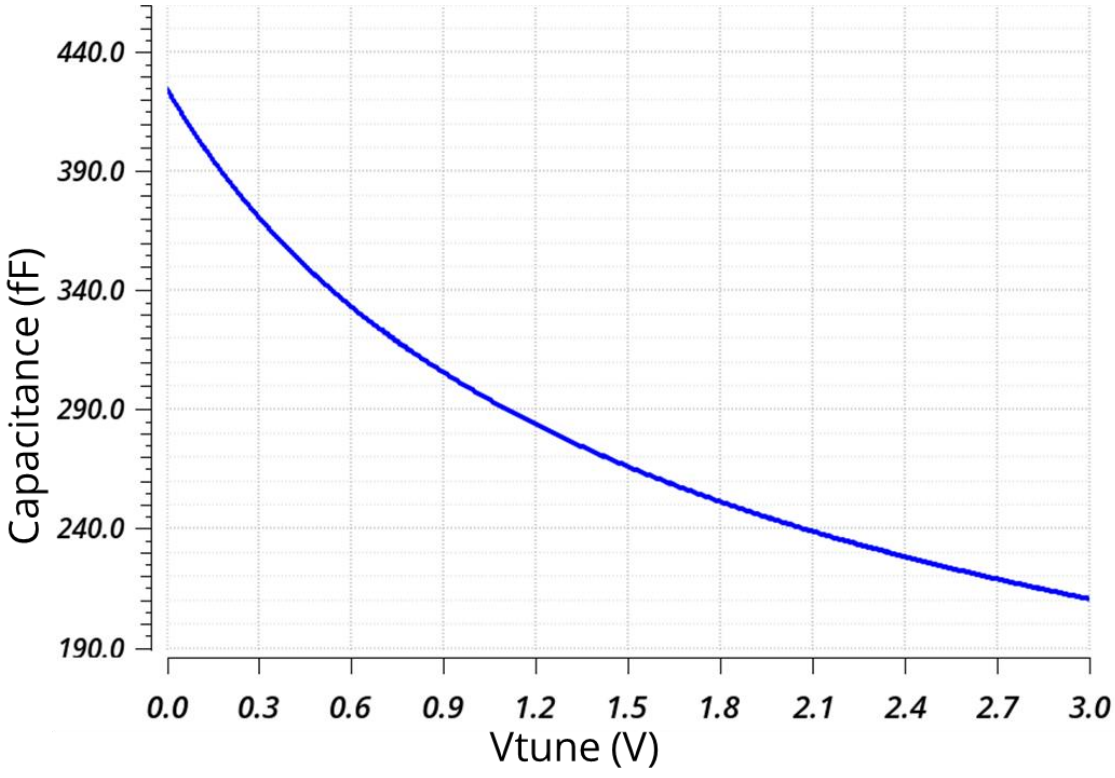


Figure 2.13: Characteristics C(*Vtune*) of the varactor diode @ 8 GHz.

$$C(f)_{|Vtune=[0...3V]|} = \frac{mag(Y)}{2\pi f} \tag{18}$$

The quality factor of this varactor diode is determined as a function of the tuning voltage *Vtune* in figure 2.14 for a frequency of 8 GHz. This characteristic is obtained using equation (19).

$$QF_{|Vtune=[0...3V]|} = \frac{Imag(Y)}{real(Y)} \tag{19}$$

The Quality factor obtained at 8 GHz is equal to 28.5 for *Vtune* = 1 V. Table 2.2 summarises the simulated performances of the varactor diode.

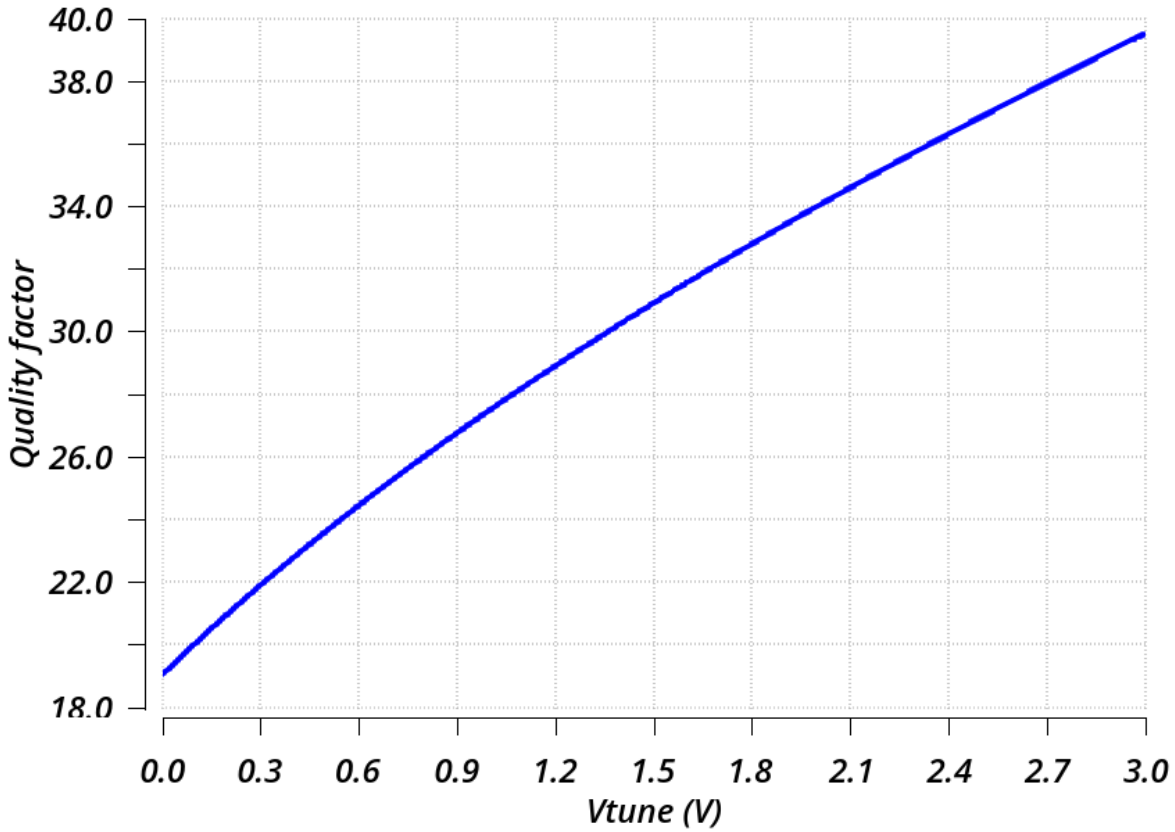


Figure 2.14: The Quality factor of the varactor diode @ 8 GHz.

Table 2.2: Summary of simulated varactor performances

C @ *Vtune* = 1 V [fF]	**290**
Cmax/Cmin	**2**
QF_{var} @ 8 GHz (*Vtune* = 1.0 V)	**28.5**

Quality factor of the resonance tank

The unloaded quality factor of the resonance tank is a function of the quality factor of the inductor (QF_{ind}) and the quality factor of the varactor diode (QF_{var}). It is therefore calculated as:

$$QF_{ind} = \frac{QF_{ind} \times QF_{var}}{QF_{ind} + QF_{var}}$$

Hence the unloaded quality factor of the resonance tank used for this design is 12.34 for *Vtune* = 1 V.

2.2.Active part design

As mentioned in the previous section, the active part of the LC VCO is based on the classical cross-coupled differential NMOS topology. NMOS transistor is preferably chosen over PMOS transistor for their better performances in terms of phase noise [58] and f_T. This topology consists of two identical NMOS M_1 and M_2 equivalent to a negative resistance equal to $-2/g_m$ to compensate for the losses associated with the resonance tank, formed by the differential inductance and two varactor diodes as shown in figure 2.8. In order to ensure the oscillation start-up given by (16), we have chosen an equivalent conductance presented by the active part (gm/2) two times higher than the equivalent tank conductance ($1/r_p$) along with the total parasitics. We can consider this value as a necessary value. Hence, for the given polarisation current, the widths of the two NMOS transistors pairs are chosen equal to 60 µm in order to fulfil the previous conditions. The length of the NMOS transistors is set to 0.25 µm, the minimum length provided by the BiCMOS technology.

For this type of oscillator, a current-controlled circuit is used. This circuit is designed by the conventional NMOS current mirror which provides the required polarisation current (I_{bias}). The architecture of the current mirror is presented in figure 2.15. It consists of an external reference current I_{ref} and the NMOS transistors (T_1 and T_2).

MOS transistors provide high input impedance, hence no leakage current exists. Thus the current transmission between I_{ref} to I_{bias} is almost perfect. The transistor sizes have been chosen to obtain a lower reference current. The reference current (I_{ref}) is then set at 2.5 mA which provides a bias current (I_{bias}) of 7.5 mA for each VCO.

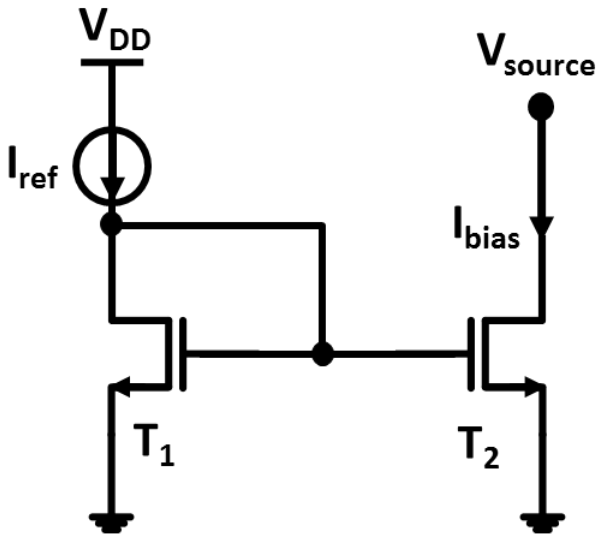


Figure 2.15: Architecture of the current mirror for a single LC VCO.

In addition, an increased grid length of T_1 and T_2 (L =1.5 µm) allows to obtain a higher output resistance R_{DS} and thus to make the polarisation current I_{bias} almost independent of the variation of the V_{DS} voltage. Table 2.3 presents the dimensions of the transistors used in the current mirror.

Table 2.3: Dimensions of the transistors of the current mirror.

Parameters of NMOS	**T_1**	**T_2**
W [µm]	**10**	**10**
L [µm]	**1.5**	**1.5**
Number of transistors in parallel	**10**	**30**

2.3.The layout of the VCO

The differential LC VCO is integrated and implemented in the QUBiC4X 0.25 µm SiGe:C BiCMOS process of NXP Semiconductors. This is an advanced high-speed BiCMOS technology which provides:

- Five layers of metal interconnection with a 5µm thick top metal
- 0.25 µm NMOS and PMOS transistors
- Vertical NPN transistors (both high speed and high voltage versions)
- Mono- and polysilicon resistors, diodes, and capacitors (including a high-density MIM capacitor).

Layout design requires a careful attention in order to minimise the effect of the parasitics. Utmost attention is needed when placing one component next to other components. The guideline of QUBiC4X DRM (design rule manual) is followed to decide the thickness of each metal strip and distance between the different metal layers. In general metal 1 is used for connecting the circuit components to ground. Metal 2 is used to connect all the DC power supplies of the circuit. Metal 3 and Metal 5 are mostly used to connect the RF connections. Metal 6 is used to connect the considerably longer distance RF lines. These specifications are used in general for the robustness of the circuit after fabrication. Figure 2.16 presents the cross-section view of the QUBiC4X technology of NXP semiconductors.

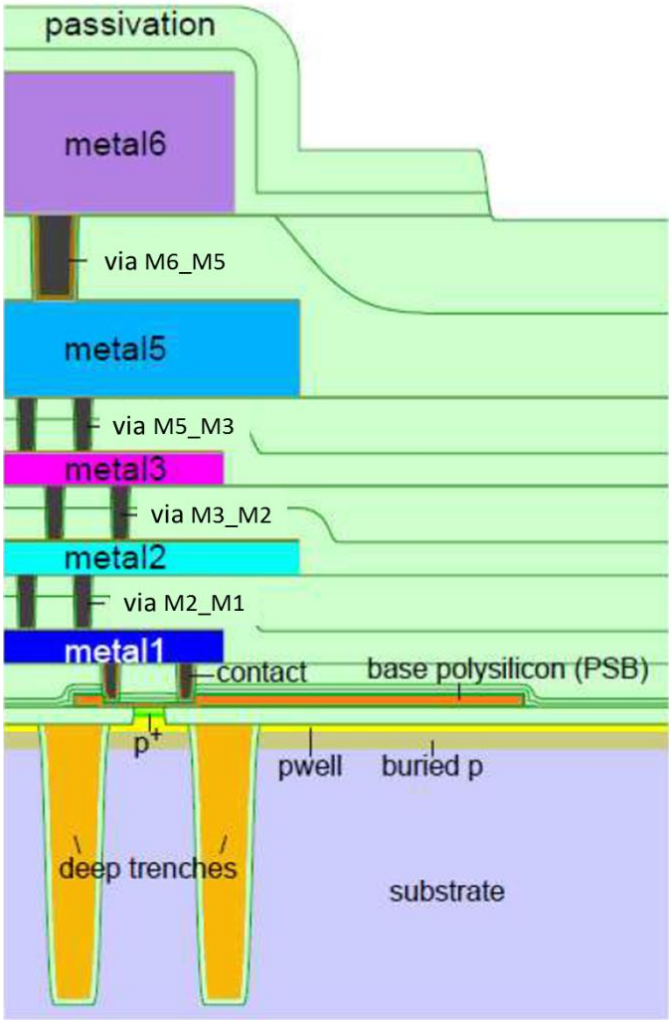


Figure 2.16: Cross-section view of the QUBiC4X technology of NXP semiconductors

The layout of the LC VCO is presented in figure 2.17. Extreme care is taken while connecting the components in order to keep the parasitics elements equal at both the differential outputs. The circuit is consuming 22.65 mW with a power supply of 3 V. The post

layout simulation results show that the frequency of the VCO varies from 7.3 GHz to 8.4 GHz (figure 2.18). The time-domain analysis of the LC VCO layout is simulated up to 500 ns to ensure the steady-state oscillations (figure 2.19).

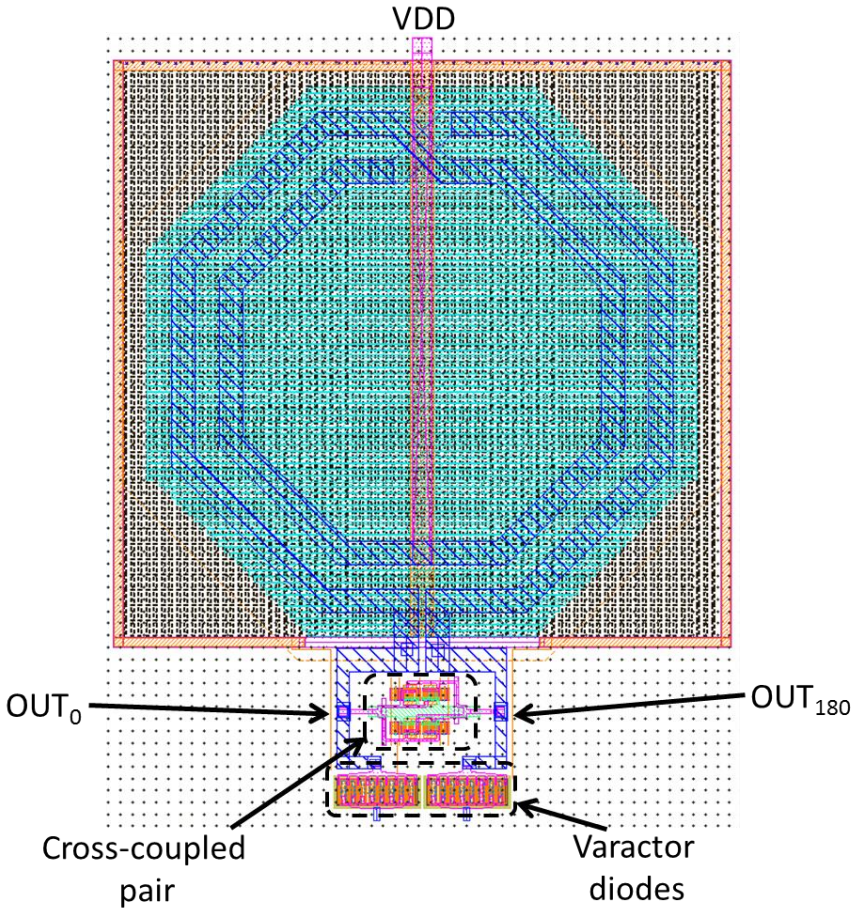


Figure 2.17: Layout of the LC VCO in the cadence design system

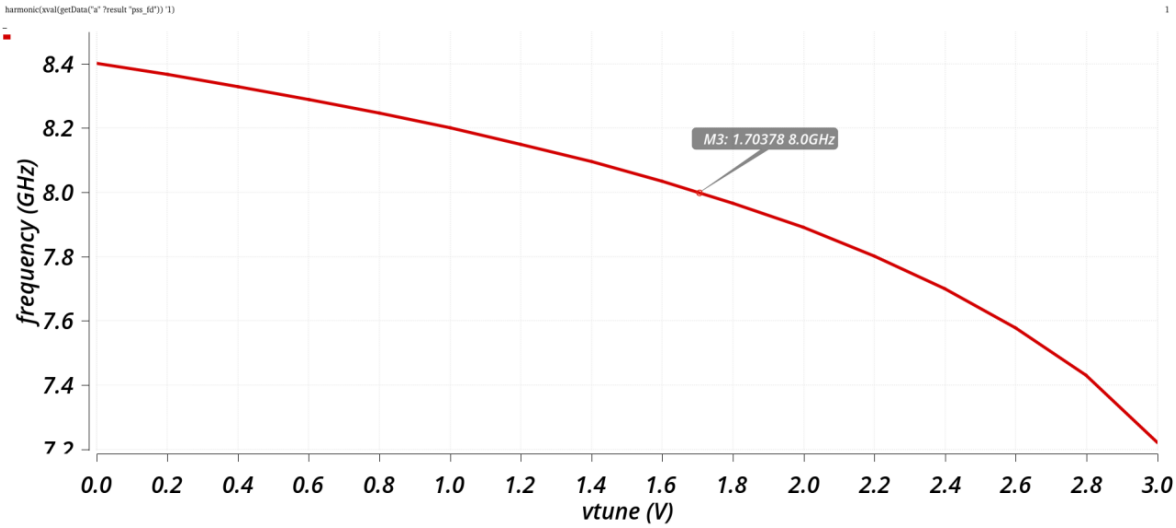


Figure 2.18: Post layout simulation results of the output frequency vs the tuning voltage.

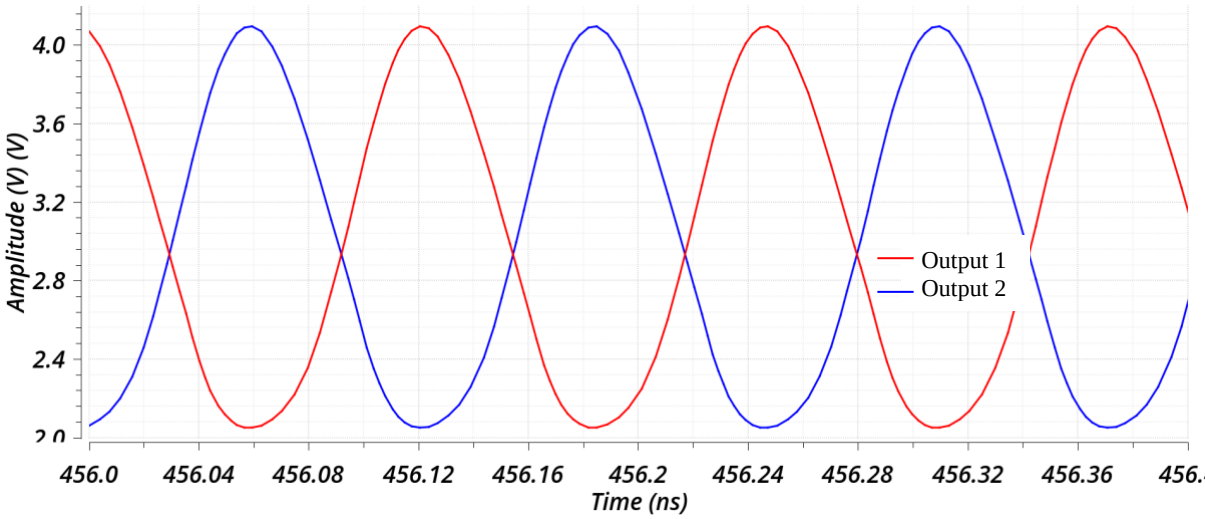


Figure 2.19: Post layout time-domain simulation analysis of LC VCO at 8 GHz for *Vtune*=1.7 V

Finally, figures 2.20 present the phase noise simulation results of the VCO. It shows the phase noise plot for *Vtune* = 1.7 V leading to an oscillation frequency of f_0 = 8 GHz and a current consumption Ibias = 7.5 mA. As can be seen in this figure, the VCO features a phase noise of -84.5 dBc/Hz and -111.7 dBc/Hz at 100 kHz and 1 MHz frequency offset respectively.

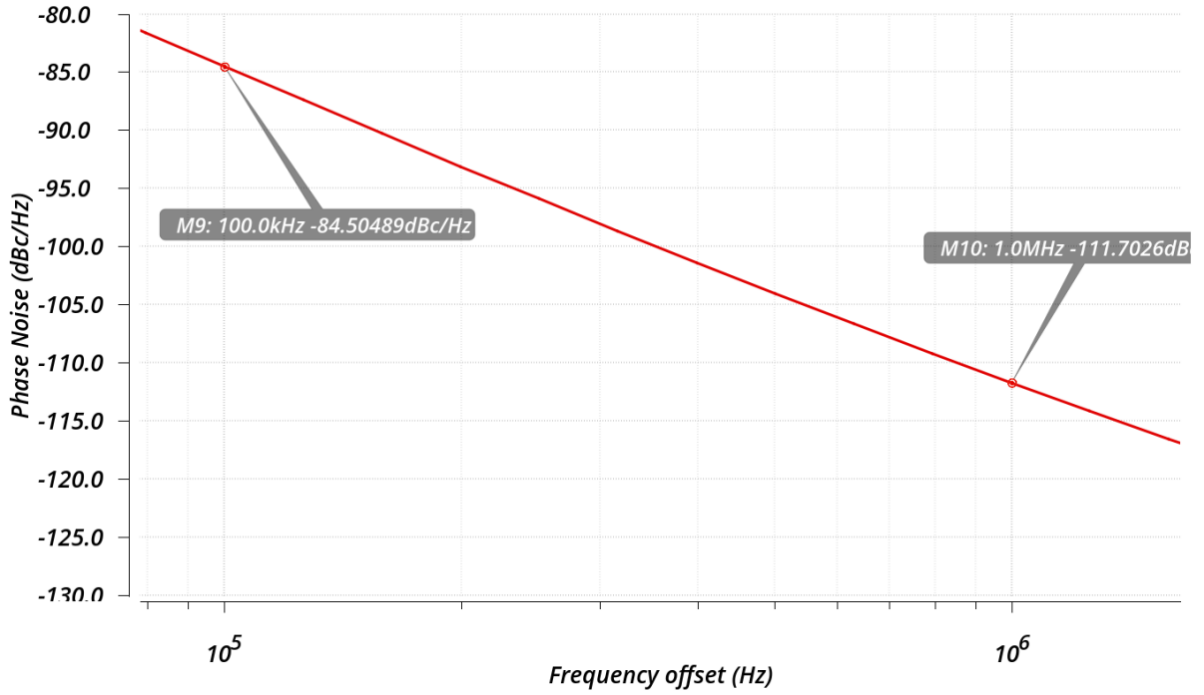


Figure 2.20: Simulated phase noise of the VCO for a tuning voltage of 1.7 V.

3. Design of the differential triple-push VCO

The schematic of the proposed triple-push VCO is presented in figure 2.21. As shown in this figure, an original passive coupling performed via the varactor diodes is proposed.

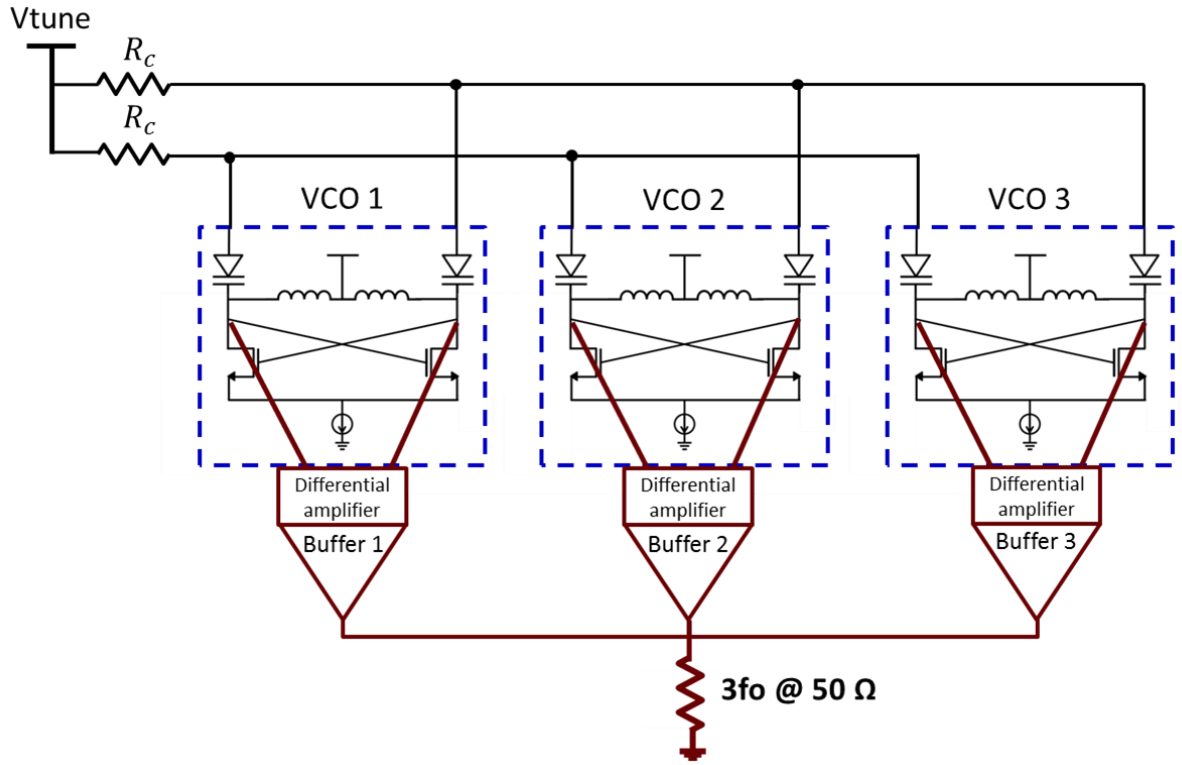


Figure 2.21: Triple-push LC VCO coupled via Varactor diodes.

The main advantages of this topology over coupling through inductor [59] are the following:

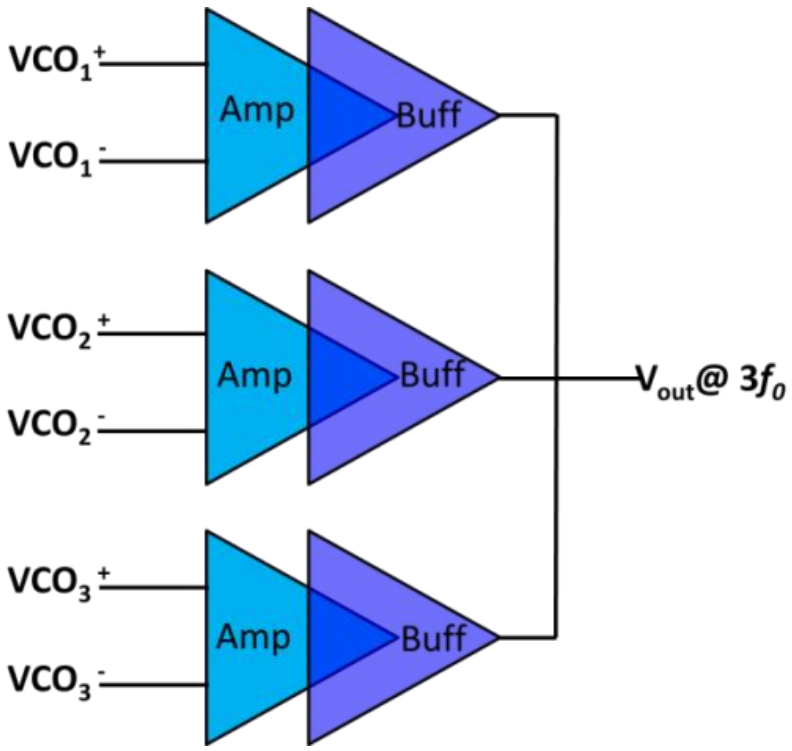
- The coupling circuit is connected separately from the output node of the VCO taken at the drain of the NMOS. The sensitivity of the coupling resistor is important for the triple-push to operate in the odd mode. In these conditions, the isolation between the output of the triple-push and the coupling circuit keeps the coupling resistor value constant.
- The coupling resistor is used both for coupling and biasing the varactor diodes. With the coupling via an inductor, it would not be possible to do that, because the losses due to resistance in series with the inductance would cause the polarisation voltage to drop.

- Moreover, in these conditions, the DC voltage supply is directly applied at the cross connected NMOS differential pair via the tank inductors.

As mentioned above, the output of the triple-push VCO is taken at the junction of the active part and the tank, whereas the coupling is performed via varactor diodes through the resistor R_c. The output signal of each LC VCO is amplified through an output stage made of a differential amplifier designed at 8 GHz and converted to a single ended signal. Finally, the three output signals of the amplifiers are isolated by buffers and added to obtain the third harmonic on a 50 Ω load.

3.1.Design of the output stage amplifier and buffer

The designed triple-push VCO is intended to be associated with an antenna array for transmitting data. In our circuit, we boosted the 3rd harmonic of the output signal of the elementary VCO and then added together to obtain the amplified 3rd harmonic at the output. As shown in figure 2.22, the differential outputs of the VCOs are applied at the input of each differential amplifier (V^+ and V^-).



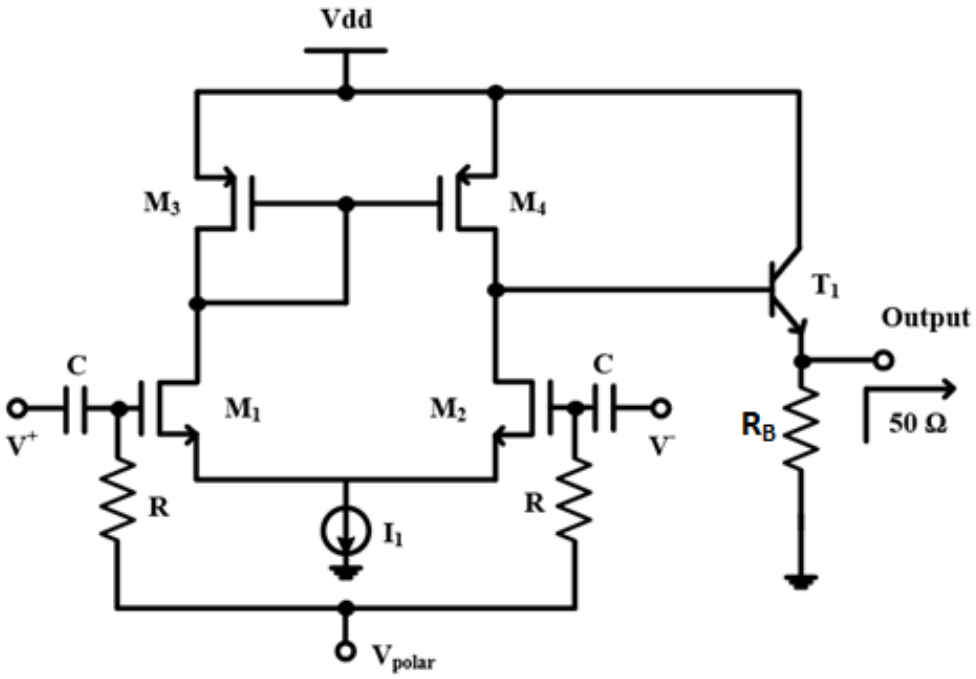


Figure 2.22: Architecture of the differential amplifier and output buffer

Hence, the differential signal from each VCO is converted to a single ended one and the buffer allows the 50 ohms impedance matching. The differential amplifier consists of a differential pair formed by two NMOS transistors (M_1 and M_2) whose size is 20 µm/0.25 µm and an active load formed by two PMOS transistors (M_3 and M_4) of 30 µm/0.25 µm. A tail current I_1 of 2.5 mA is provided to the circuit by the current source. The overall schematic of the current source allowing to bias the triple-push VCO and the three amplifiers is shown in figure 2.23. Table 2.4 presents the sizes and numbers of the transistors of the complete current mirror.

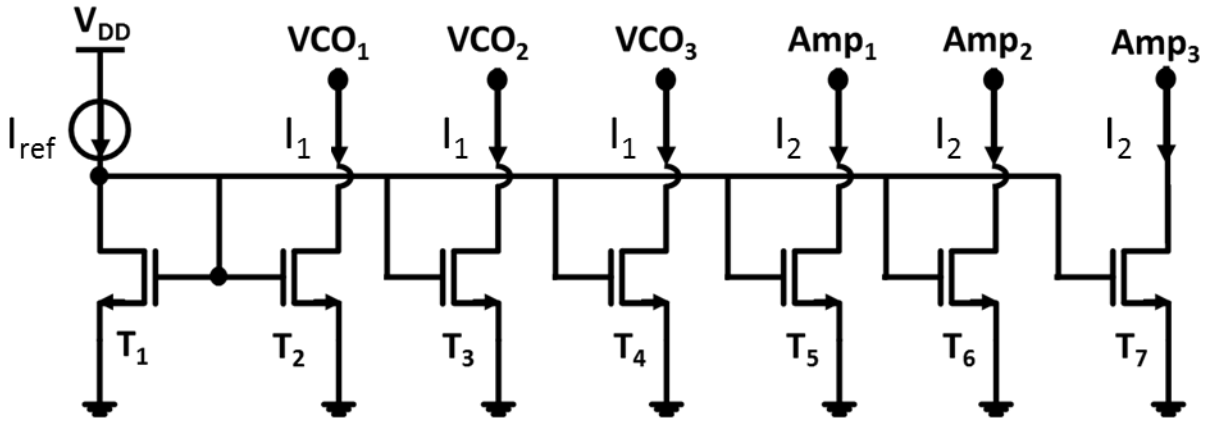


Figure 2.23: Current mirror of the triple-push VCO providing biasing current for the three VCOs and the three output stage amplifiers

Table 2.4: Current mirror transistors' size for the complete triple-push VCO.

Parameters of NMOS	**T_1**	**T_2, T_3, T_4**	**T_5, T_6, T_7**
W [µm]	**10**	**10**	**10**
L [µm]	**1.5**	**1.5**	**1.5**
Number of transistors in parallel	**10**	**30**	**10**

The single ended output signal of the differential amplifier is sent to the buffer in a common collector configuration. The buffer in this configuration has a high input impedance and a low output impedance which helps to match with the 50 ohms load at the output. A small bipolar transistor whose size is 0.5 µm/6.3 µm is chosen, and, in order to obtain the maximum power transfer on 50 ohms, the bipolar transistor is biased by R_B = 500 Ω. Finally, the output of all the three buffers are added in current, and the 3rd harmonic is collected on the 50 ohms load.

3.2. The layout of the Triple-Push VCO

The layout of the proposed 24 GHz triple-push LC VCO integrated and implemented in the QUBiC4X 0.25µm SiGe:C BiCMOS of NXP Semiconductors is presented in figure 2.24. The chip size is 0.9x0.965 mm^2. Under a 3 V power supply voltage, the power consumption is 63.99 mW for the triple-push VCO core (without output buffers) and 113.64 mW for the overall circuit.

The floor plan of the different key blocks of the triple-push VCO is the most critical part of this design. The positions of the inductors of the three VCOs are carefully chosen to reduce the large parasitics. Metal 6 (top metal level in this design kit) is used for coupling with the resistors in order to reduce the effect of the parasitics. It is compulsory for the three large connecting lines to be equidistant from each other to provide the same parasitic elements on the three VCOs. A mismatch would lead to the degradation of the rejection of the fundamental and the second harmonic. The output differential amplifier is biased with a 1.7 V DC supply voltage separately.

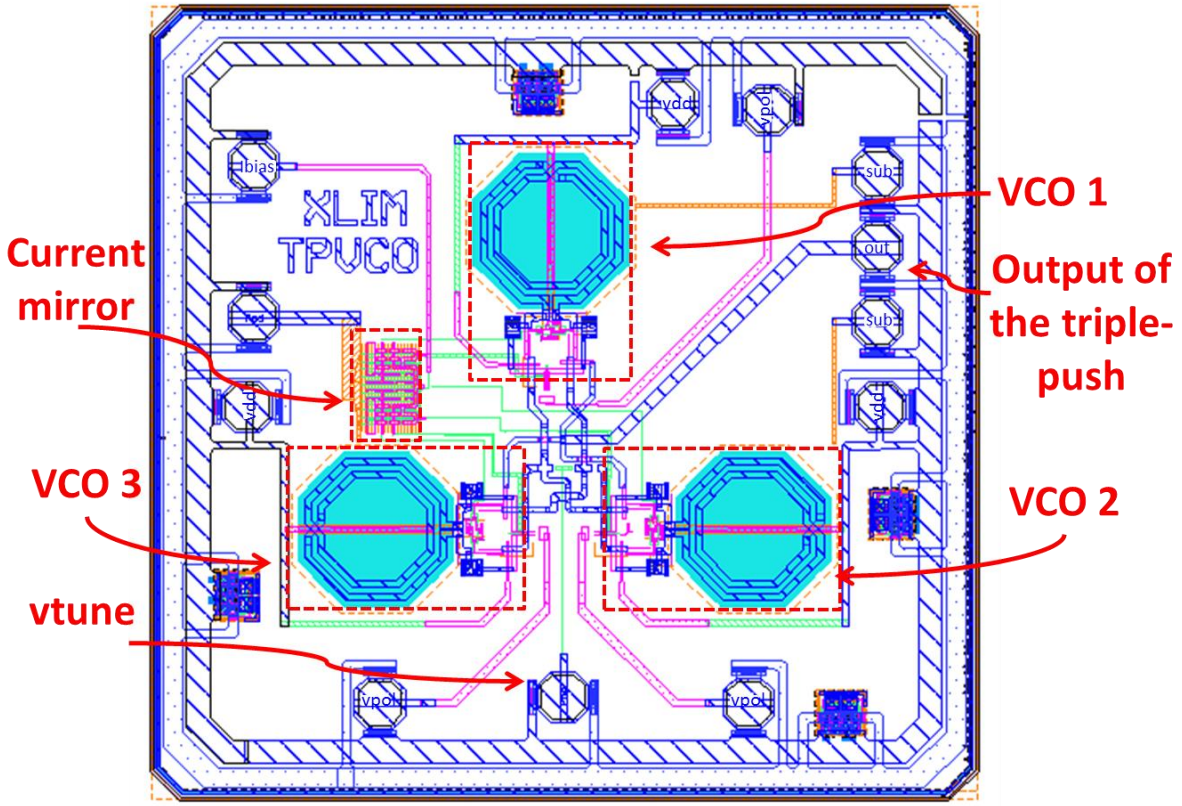


Figure 2.24: The layout of the triple-push VCO implemented in the QUBiC4X 0.25 µm SiGe:C BiCMOS process of NXP Semiconductors.

3.3. The Post layout simulation results of the TPVCO

First of all, a transient analysis is performed with spectre RF in order to verify that the three VCOs are well synchronised. Then, a post layout harmonic balance simulation with an RLC extraction tool is performed. In these conditions, an output power of -5.76 dBm (on 50 ohm load) is found. Furthermore, the proposed triple-push VCO can be tuned from 21.94 GHz to 25.64 GHz with a tuning voltage varying from 0 to 3 V (figure 2.25).

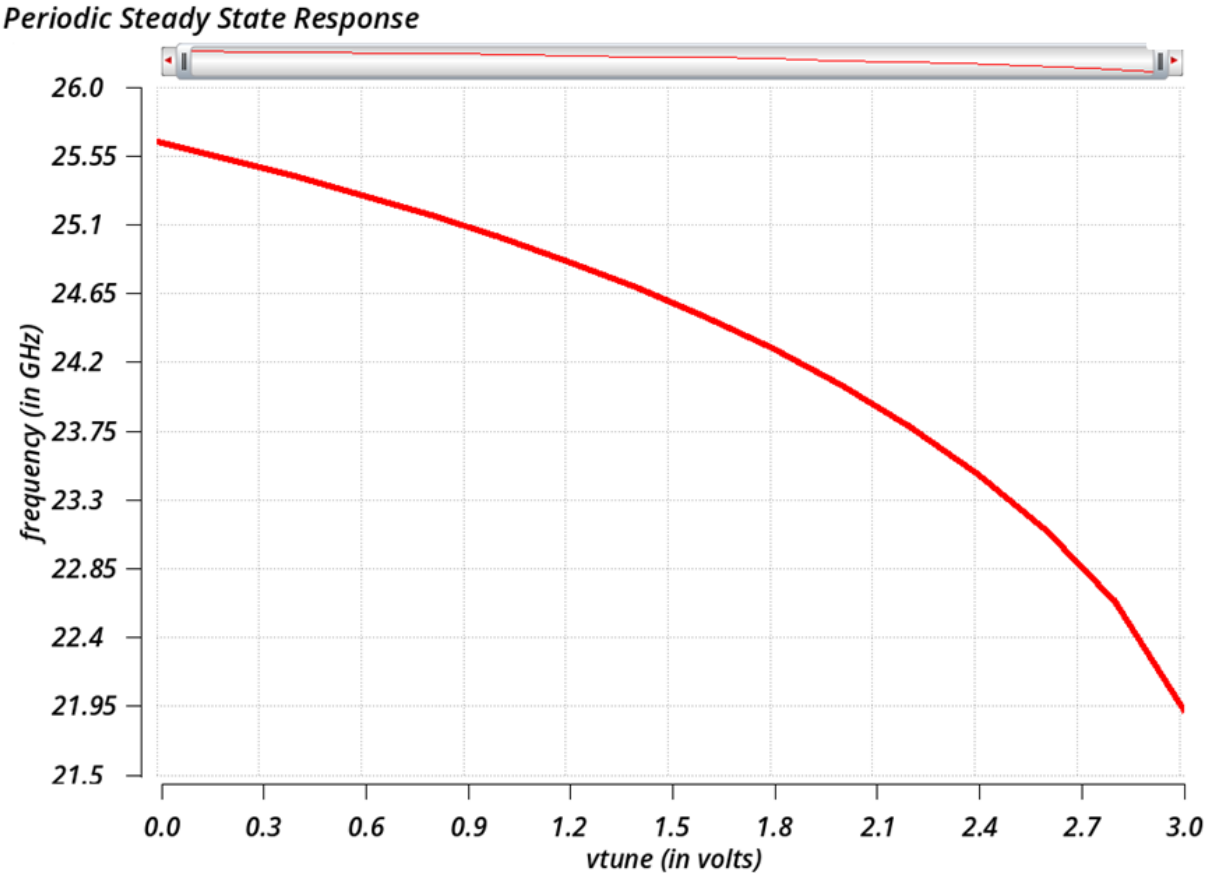


Figure 2.25: Post layout simulation of the output frequency vs the tuning voltage.

Furthermore, the variation of the output power is roughly 0.55 dB over the entire tuning range (figure 2.26). The Fundamental and second-harmonic rejection is more than 25.54 dB and 17.83 dB respectively, over the entire tuning range of 3.7 GHz. A comparison of this work with previously published triple-push oscillators in the 20-30 GHz frequency range is presented in Table 2.5. As can be seen on this table 2.5, the proposed triple-push VCO compares favourably with other published triple-push VCOs oscillating at roughly the same frequency band. The simulated parameters of the proposed triple-push VCO are summarised in Table 2.6. The output waveforms obtained from the post-layout simulation results of the three VCOs are presented in figure 2.27(a). The output signals of the VCO is

purposely distorted by changing the parameter of the cross-coupled NMOS pair and tank circuit in order to extract the maximum third harmonic. The output of the triple-push VCO at 24 GHz is shown in figure 2.27(b). The post-layout transient simulation is well stabilised after 22 nsec.

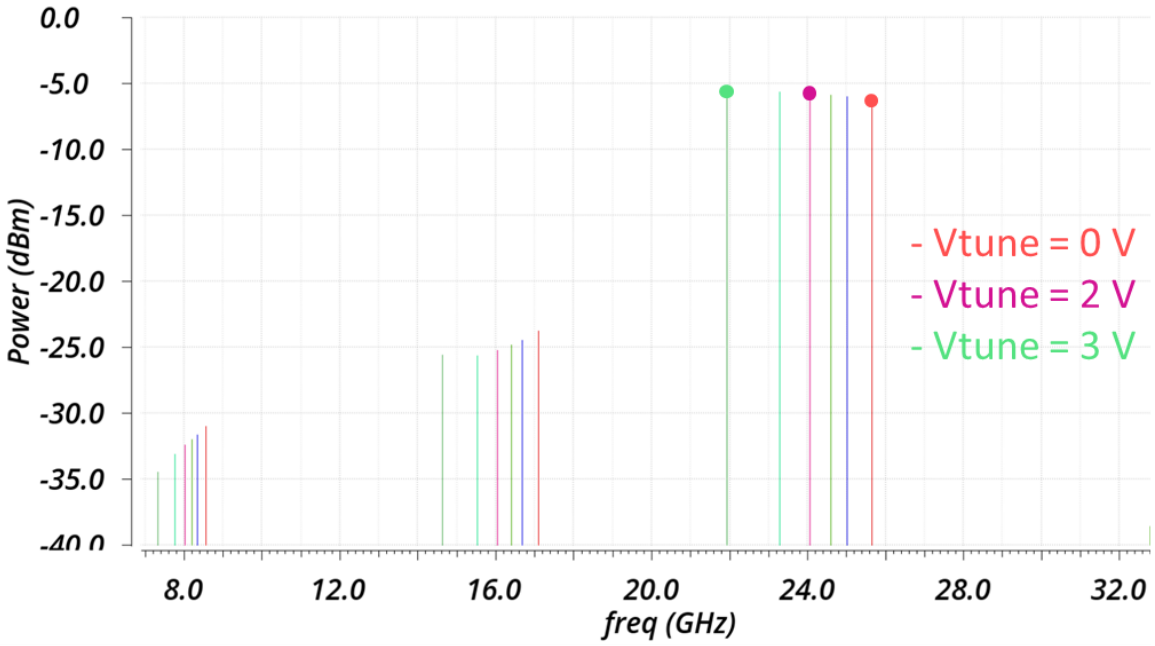


Figure 2.26: Post Layout simulation results of the output power, second harmonics and fundamental as a function of the tuning voltage in CADENCE®.

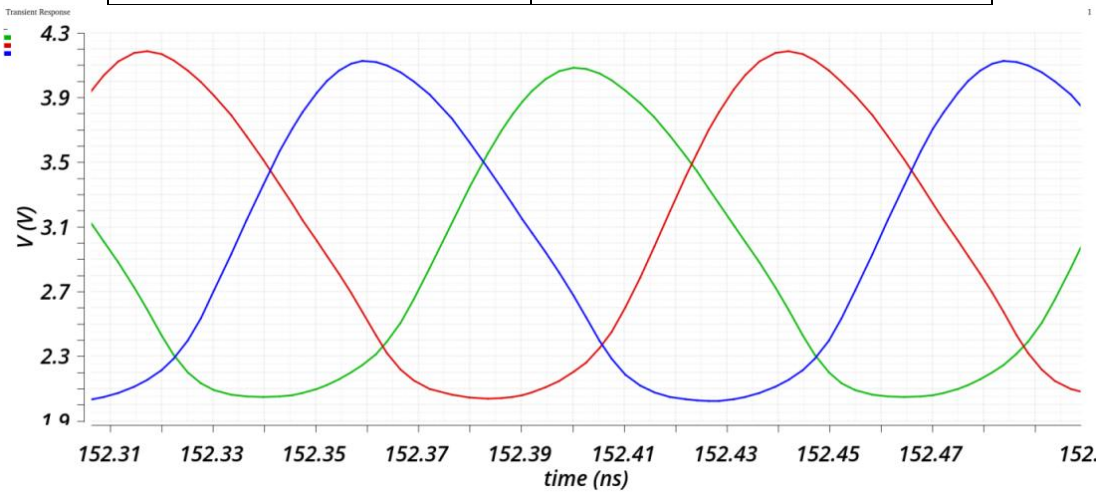
Table 2.5: Comparison with other triple-push VCOs between 20-30 GHz

Ref.	[45]	[49]	[52]	[55]	This work
Frequency (GHz)	28.4	24.6	30	0.2 - 34	24
Fundamental rejection (dB)	5.6	20	18.66	15	27.67
2nd harmonic rejection (dB)	18.6	20	30	15	19.65
Output Power (dBm)	-15.4	-14.8	-12	-16 to -20	-5.76
Power consumption (core in mW)	-	-	10.04	1.2 - 70	63.99

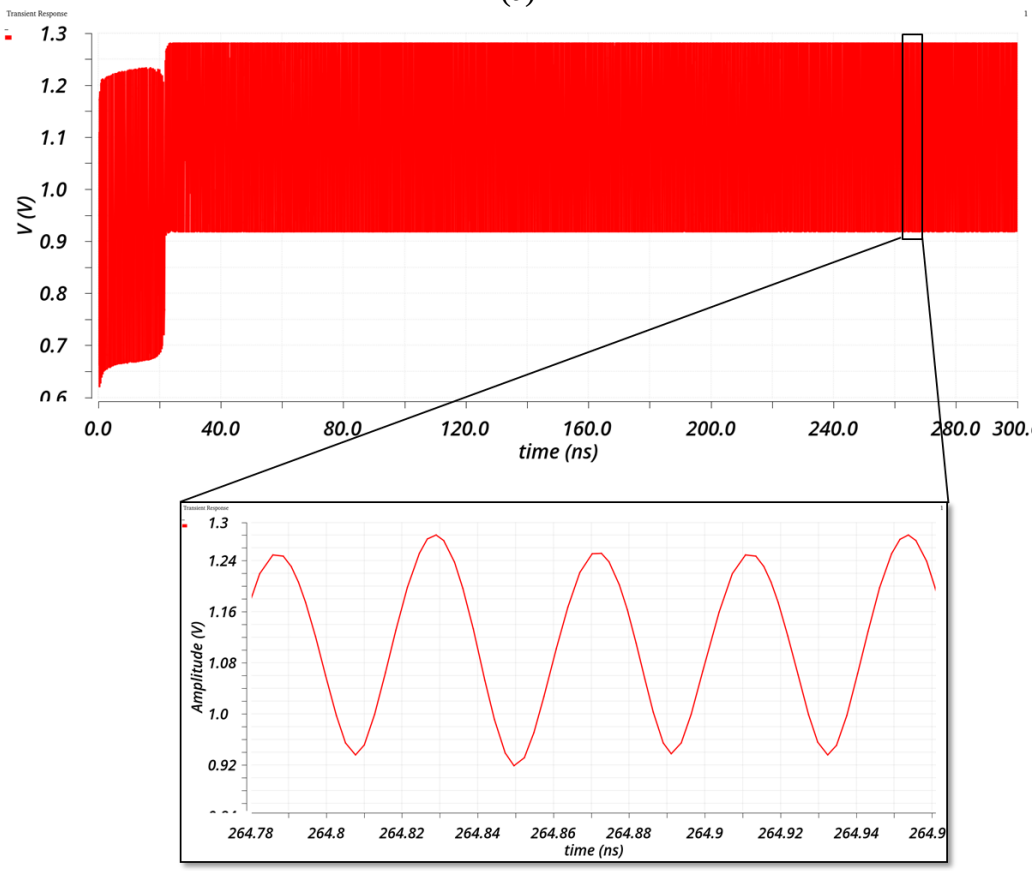
Table 2.6: Summary of the triple-push VCO performances

Parameter	Value
Supply voltage	3 V
Bias Voltage for amplifiers	1.7 V
Power consumption	113.64 mW

Tuning range	**(21.94 – 25.64) GHz**
Output Power	**-5.76 dBm**
Chip Area	**1.227x1.176 mm^2**



(a)



(b)

Figure 2.27: Time-domain post-layout analysis of the triple-push VCO (a) Output of the three VCO at 8 GHz and at 120° to each other, (b) Output of the triple-push VCO in odd mode at 24 GHz for *Vtune* = 2 V

Furthermore, let us remind that, in an integrated circuit, a gradient in the silicon process can lead to a difference between the coupling resistors R_C. Therefore, the rejection of the fundamental and second harmonics can be an issue which would lead to the diminution of the output power at $3.f_0$. So, in order to verify the robustness of our triple-push VCO, post-layout simulations of fundamental and second harmonic rejections according to Process, Voltage and Temperature (PVT) variations are performed. The simulations results are summarised in Tables 2.7, 2.8 and 2.9.

Table 2.7: Rejection of the fundamental and second harmonic as a function of the temperature

Temperature Change	Fundamental rejection	Second harmonic rejection
T = -40° C	**26.5**	**17.5**
T = 27° C	**27.6**	**19.5**
T = 85° C	**26.35**	**19.72**

Table 2.8: Rejection of the fundamental and second harmonic as a function of the supply voltage

Power supply	Fundamental rejection	Second harmonic rejection
Vdd = 2.8 V	**27.4**	**17.28**
Vdd = 3 V	**27.6**	**19.5**
Vdd = 3.2 V	**19.88**	**22.12**

Table 2.9: Rejection of the fundamental and second harmonic as a function of the process variations

Process change	Fundamental rejection	Second harmonic rejection
High_was	**22.75**	**15.298**
Nominal	**27.6**	**19.5**
Low_was	**30.641**	**21.35**

4. Conclusion

In this chapter, a new architecture of a 24 GHz triple-push LC VCO is designed and implemented in the QUBiC4X 0.25 µm SiGe:C BiCMOS process of NXP Semiconductors. The first part of the chapter is devoted to the analysis of the LC VCO design. Then, the theoretical study of the triple-push VCO is briefed. Mode analysis of the triple-push oscillators is presented explaining the condition to ensure an odd mode of operation for the successful triple-push operation. Finally, the post layout simulation results of the triple-push are presented. The post layout simulation results confirm that the circuit delivers a steady and synchronised output signal of -5.76 dBm at 24 GHz. The overall power consumption, including the output buffers, is only 113.64 mW from a 3 V supply voltage. More than 27.67 dB rejection is obtained for the fundamental and more than 19.65 dB for the second harmonic at 24 GHz. The floor plan of the triple-push VCO was done with extreme care as it is the crucial factor for the rejection of the fundamental and the second harmonic.

This triple-push VCO provides the maximum third harmonic output power at 50 Ω in comparison with the previous published triple-push oscillators in the 20-30 GHz frequency range. Also, the fundamental and second harmonic rejection is better in comparison to the other triple-push oscillators in this range. Triple-push oscillators are mostly fabricated at the tetrahedral frequencies, but this triple-push is designed at 24 GHz as it will be used for the design of an active phase shifter circuit for beamforming. In the next chapter, the design of the proposed active phase shifter is presented by using the injection locking phenomenon on the triple-push VCO.

Chapter III: Injection locked triple-push VCO based active phase shifter

Table of Contents

Chapter III: Injection locked triple-push VCO based active phase shifter 78

Introduction 82

1. The Injection locking phenomenon in a triple-push Voltage Controlled Oscillator. 83

2. The 120° phase shifter..... 84

2.1. Design of a new 120° phase shifter at 8 GHz..... 86

2.1.1. Analysis and design of the 60° phase shifters 86

2.1.2. Design of the 120° phase shifter by using differential adders..... 88

2.2. Post-layout simulation results of the 120° phase shifter 92

3. Injection-locked triple-push VCO based RF active phase shifter..... 97

3.1. The architecture of the Injection Locked Triple-push VCO (ILTPVCO)..... 100

3.2. The layout of the IL TP VCO..... 103

3.3. Post layout simulation results..... 104

3.3.1. The performances of the active phase shifter without injection..... 104

3.3.2. The performances of the active phase shifter with injection..... 105

4. Resume of the phase shifter results..... 108

5. Conclusion 110

Final Conclusion 111

List of scientific publications 115

Résumé en français..... 116

References 126

Introduction

The RF phase shifters are highly in demand because they are widely used in applications such as smart antennas, phased array antennas, and Multiple Input Multiple Output (MIMO) systems. In addition, with the advent of 5G technology, many expert groups have proposed a frequency spectrum in the millimetre-wave range of up to 100 GHz or more [60]. Under these conditions, the propagation losses are considerable and the gain provided by the beamforming based on RF phase shifters makes it possible to compensate the losses. In a phased antenna array, the phase shifters can be implemented at different stages: RF, LO, IF or digital baseband [61] [62]. The phase shifter in the LO path has an advantage over the RF path phase shifting as the system performances are not sensitive to the degradation due to the phase shifters. Indeed, the requirement of the phase shifter in terms of noise figure, non-linearity, losses and amplitude mismatching is relaxed because these drawbacks do not have direct impact on the quality of the signal. The objective of this dissertation is to design and implement an active RF phase shifter for a phased antenna array which would be applied in the LO path for the application of beamforming in 5G technology. The main goal is to obtain a linear phase shift from -90° to 90°. Lastly a full linear 360° phase plane can be obtained simply by flipping the outputs.

Therefore, this chapter presents a new architecture of an active RF phase shifter using an Injection Locked Triple-Push Voltage Controlled Oscillator (ILTPVCO). The chapter begins with the introduction of the injection phenomenon in a triple-push VCO. Then, a novel architecture of a tuneable differential 120° phase shifter at 8 GHz and integrated into a 0.25 µm BiCMOS SiGe:C technology is presented with the post-layout simulation results. In the second part, we will present the design and implementation of a new active phase shifter architecture designed with the combination of the 120° phase shifter and the triple-push VCO at a frequency of 24 GHz and fully integrated on a silicon substrate using the 0.25 µm BiCMOS SiGe:C technology of NXP Semiconductors. Then, the post-layout simulation results of the circuit will be presented in order to evaluate the performances of the proposed phase shifter and to validate the concept of this new architecture. Finally, the problems of the parasitic extraction with the Assura module Cadence, which dominates during the implementation of the circuit, will be discussed.

1. The Injection locking phenomenon in a triple-push Voltage Controlled Oscillator

One of the integrable solutions to obtain an active phase shifter is to use an injection-locked VCO (Voltage Controlled Oscillator) [22]. However, as explained in the section 3.3.2 of chapter 1, this solution does not provide a linear phase shift over the entire phase plane (linearity limit is between ±30° with an error of 4.5%). One solution of providing a linear phase shift is to use an Injection-Locked triple-push VCO (figure 3.1). Indeed, with the triple-push, the third harmonic is extracted and we can easily understand that the instantaneous phase is thus multiplied by three and then, the phase shift at $3\times f_{inj}$ will be considered linear between 3 times ± 30° (i.e. ± 90°). In this thesis, we have used differential triple-push VCOs. In brief, injection locking in differential triple-push VCOs then can present a linear phase shift over the entire phase plane thanks to the differential outputs.

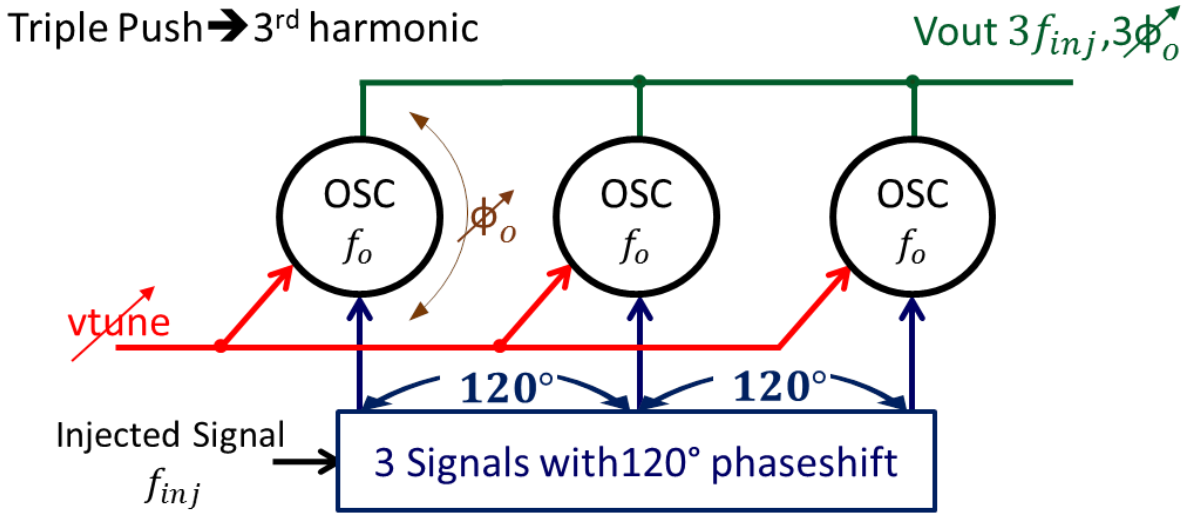


Figure 3.1: The principle of injection locking in a triple-push oscillator

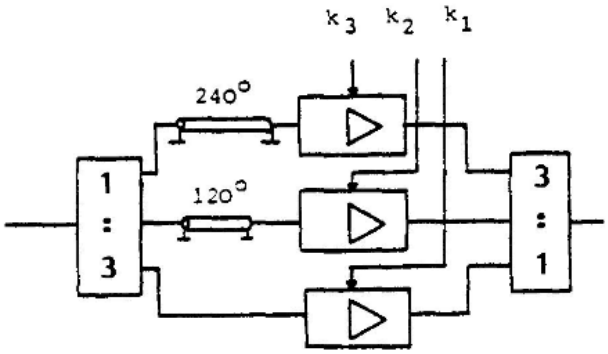
On the other hand, the difficulty consists in injecting three signals out of phase by 120° between each of the oscillators constituting the triple-push VCO. It is in this context that we first designed a new 120° phase shifter. We present here the design and implementation of an integrated circuit that provides three RF signals that are 120° out of phase with each other. In the following section, this innovative 120° phase shifter is proposed and implemented on a silicon substrate using the 0.25 µm BiCMOS SiGe:C technology of NXP Semiconductor.

2. The 120° phase shifter

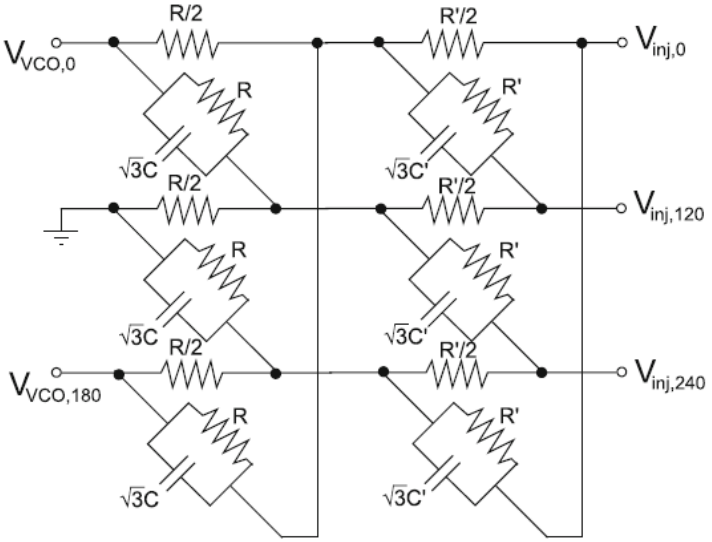
To achieve 120° phase shift signals, in the past, several solutions have been proposed. W. Mielke has used a three-phase shifter circuit using a transmission line and an amplifier to control amplitude and phase for mobile satellite transmissions (figure 3.2(a)). In figure 3.2(b), the authors designed a passive three-phase generation circuit using polyphase filters. This structure presents high losses in the output signals when used at high frequencies. Three-phase generation by ring oscillator is one of the best methods to obtain a 120° phase shift with a minimum phase error (figure 3.2 (c)). However, these circuits can be considered more as multi-phase generators rather than phase shifters since they do not use an injected signal at their input. Besides, with these ring oscillators, the injection of a signal leads to phase and amplitude imbalances.

In these conditions, an innovative architecture of a differential 120° phase shifter can be designed and developed at 8 GHz. This circuit, composed of passive integrated RLC elements, active differential adders, and output buffers, is intended to be integrated into a more complex circuit to provide the differential three-phase signals injected on three VCOs, thus forming a triple-push assembly capable of producing a linear active phase shifter at 24 GHz.

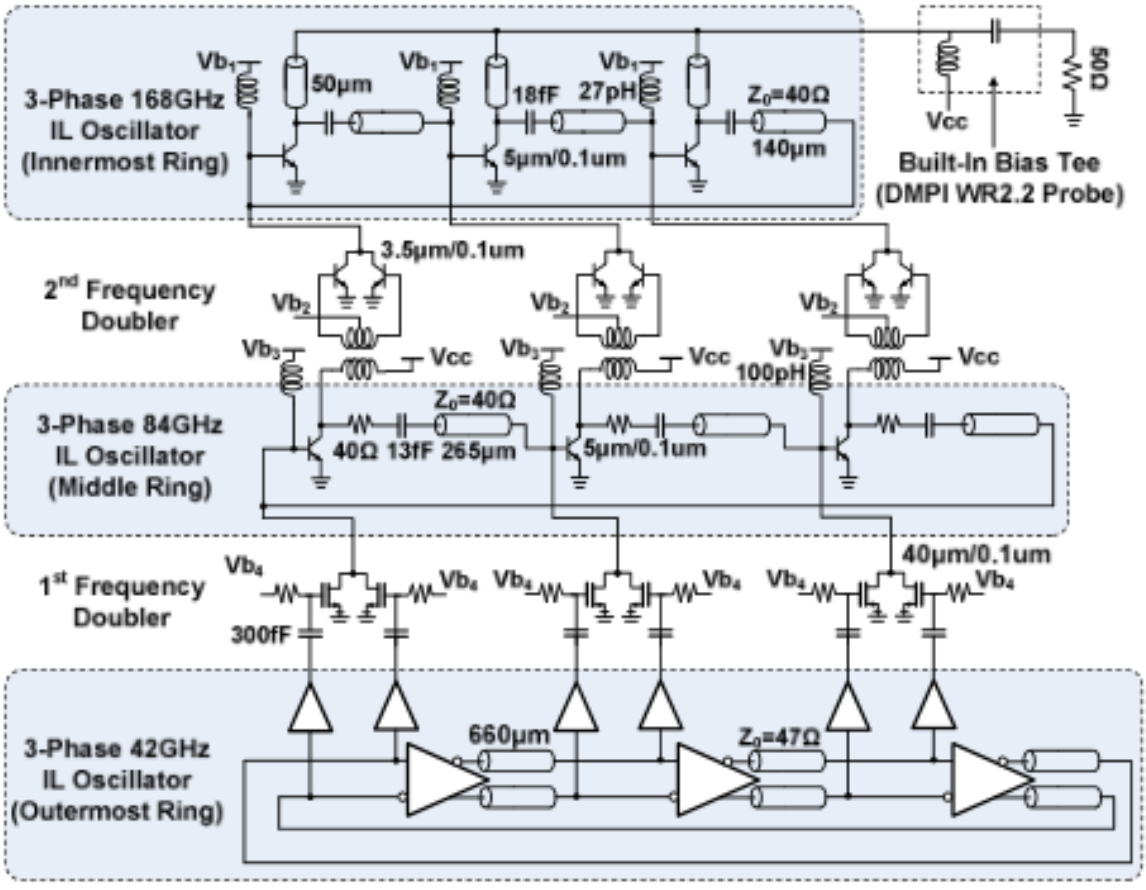
The input of this phase shifter is a single RF signal; however, the output will be three 120° differential signals. Concerning the development of the full circuit, the first step was to design this phase shifter alone. To simplify future measurements, only three 120° signals are provided at the output, while integrated 50 Ω resistors are loaded to their complementary signals. Moreover, for the requirement of frequency agility, thanks to the utilisation of Varicap diodes, this circuit has the advantage of being tunable.



(a)



(b)



(c)

Figure 3.2: Architecture of a 120° phase shifter proposed by (a) W. Mielke [63], (b) Andrea Bevilacqua et Pietro Andreani [64] and (c) T. Chi, J. Luo, S. Hu, and H. Wang [65]

2.1.Design of a new 120° phase shifter at 8 GHz

The block diagram of the differential 120° phase shifter is presented in figure 3.3. Following the input matching network, an integrated balun generates the two differential RF signals from a single ended RF input signal. Then, on each path, a passive circuit providing a 60° phase shift is used. In these conditions, we obtain four signals at 0°, 60°, 180° and 240°. Then combining these signals, it is possible to obtain the three outputs which present a phase shift of 120° between them.

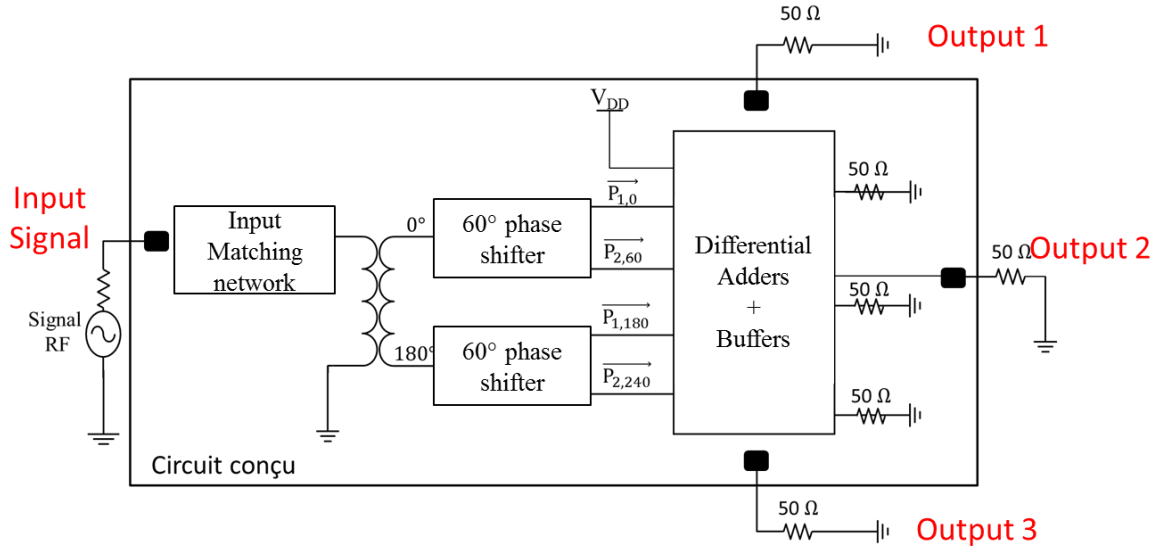


Figure 3.3: complete 120° phase shifter architecture.

2.1.1. Analysis and design of the 60° phase shifters

The first block, called 60° phase shifter, consists of a parallel RC circuit and is associated in series with a parallel RLC resonator block, as shown in figure 3.4. The impedances of these two blocks are respectively noted $Z_1(j\omega)$ and $Z_2(j\omega)$. This combination of components results in the first 60° phase shift between the two signals that are noted $\overrightarrow{P_{1,0}}$ and $\overrightarrow{P_{2,60}}$. The values of these passive RLC components also allows to obtain the same amplitude for these two signals. To calculate these values, $Z_1(j\omega)$ and $Y_2(j\omega)$ are defined as:

$$Z_1(j\omega) = \frac{R}{1 + j\omega RC} \quad (1)$$

$$and \qquad Y_2(j\omega) = \frac{1}{R} + j\omega C + \frac{1}{j\omega L} \tag{2}$$

Then, considering $T(j\omega)$ as the transfer function linking $\overrightarrow{P_{1,0}}$ and $\overrightarrow{P_{2,60}}$, we can write:

$$T(j\omega) = \frac{P_{2,60}(j\omega)}{P_{1,0}(j\omega)} = \frac{Z_2(j\omega)}{Z_1(j\omega) + Z_2(j\omega)} = \frac{1}{1 + Z_1(j\omega)Y_2(j\omega)} \tag{3}$$

$$T(j\omega) = \frac{1}{1 + \frac{R}{1 + j\omega RC}\left\{\frac{1}{R} + j\omega C + \frac{1}{j\omega L}\right\}} \tag{4}$$

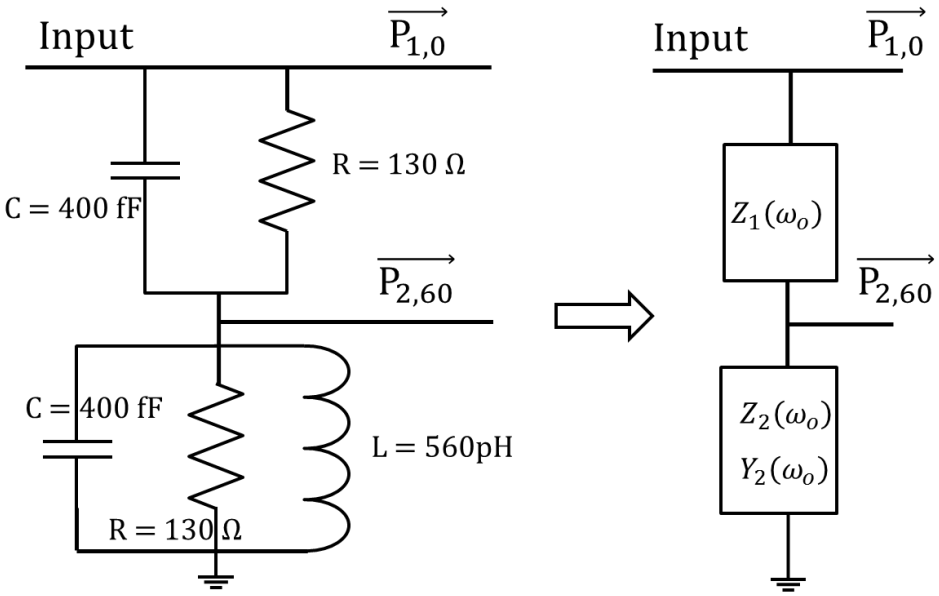


Figure 3.4: Schematic of the 60° phase shifter

$$T(j\omega) = \frac{1 + j\omega RC}{2\left\{1 + j\omega RC\left(1 - \frac{1}{2\omega^2 LC}\right)\right\}} \tag{5}$$

This transfer function is complex and can thus be written as follows:

$$T(j\omega) = a + jb \tag{6}$$

From $T(j\omega)$ and considering that we want to obtain, at the operating pulsation ω_0, a phase shift of 60° and a gain equal to 1 as shown in figure 3.5, one solution is a and b equal respectively to 1/2 and $\sqrt{3}/2$. Therefore, from (6) and (5), we can write:

$$\frac{1 + j\omega RC}{2} = (a + jb)\left\{1 + j\omega RC\left(1 - \frac{1}{2\omega^2 LC}\right)\right\} \tag{7}$$

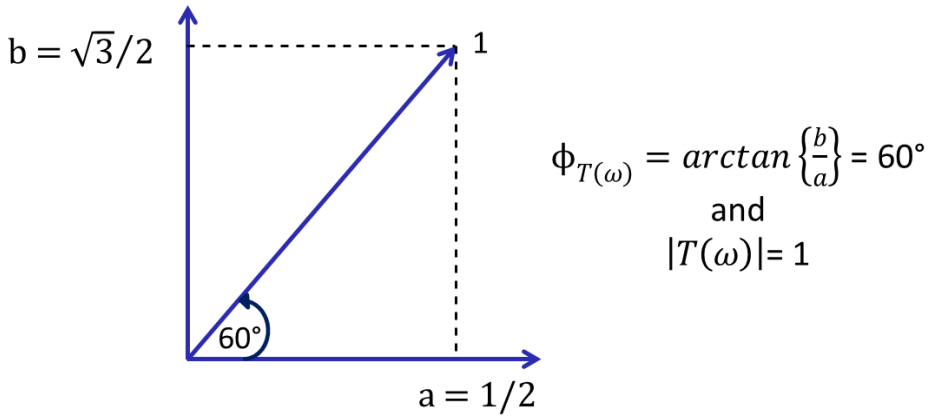


Figure 3.5: Construction of the vector P_2 from the algebraic notation $a + jb$ for a phase of 60° and a module of 1.

By separating the real and imaginary parts and identifying them, we have:

$$\frac{1}{2} = \left\{a - b\omega RC\left(1 - \frac{1}{2\omega^2 LC}\right)\right\} \quad (8)$$

$$\frac{\omega RC}{2} = \left\{a\omega RC\left(1 - \frac{1}{2\omega^2 LC}\right) + b\right\} \quad (9)$$

In these conditions, we obtain the parameters ensuring a phase shift of 60°, when the equalities (10), are respected:

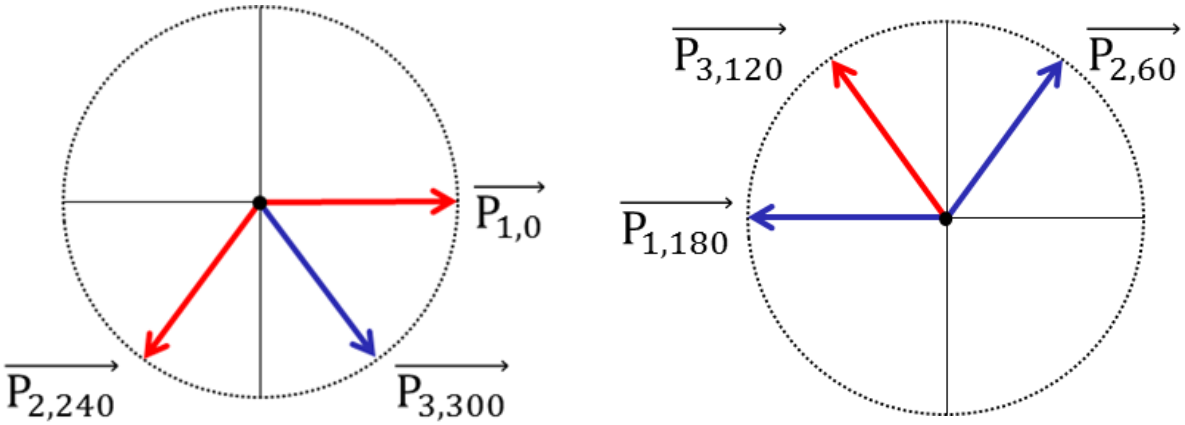
$$\omega_o{}^2 = \frac{1}{2LC} \; and \; R = \frac{\sqrt{3}}{\omega_o C} \quad (10)$$

By considering the above equations, we calculate the values of R, L, and C to obtain a phase shift of 60° between the two signals with the same amplitude at 8 GHz. In these conditions, the values obtained here are L = 0.56 nH, R = 130 Ω and C = 400 fF (figure 3.4).

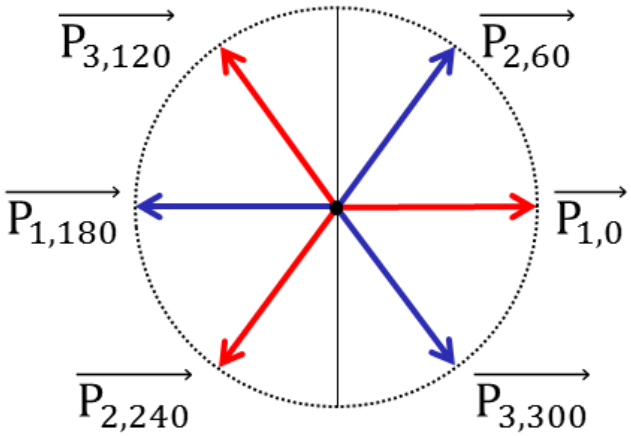
2.1.2. Design of the 120° phase shifter by using differential adders

In order to meet the differential structure, two 60° phase shifters presented previously are used to provide the phases 0°($\overrightarrow{P_{1,0}}$)/60°($\overrightarrow{P_{2,60}}$) and 180°($\overrightarrow{P_{1,180}}$)/240°($\overrightarrow{P_{2,240}}$). Then, differential adders between $\overrightarrow{P_{1,0}}$ and $\overrightarrow{P_{2,240}}$, (and $\overrightarrow{P_{2,60}}$ and $\overrightarrow{P_{1,180}}$) allow adding the two signals vectorially to obtain $\overrightarrow{P_{3,300}}$ = ($\overrightarrow{P_{1,0}}$+$\overrightarrow{P_{2,240}}$) and $\overrightarrow{P_{3,120}}$, as shown in figure 3.6(a). To compensate for the delays generated by the differential adder on $\overrightarrow{P_{3,300}}$ and $\overrightarrow{P_{3,120}}$, then differential adders are also placed on the paths $\overrightarrow{P_{1,0}}$, $\overrightarrow{P_{2,60}}$, $\overrightarrow{P_{1,180}}$ and $\overrightarrow{P_{2,240}}$. All these differential adders are

designed and calibrated to provide the same amplitude on the three output signals. In these conditions, a phase shift of 120° is obtained between $\overrightarrow{P_{1,180}}$, $\overrightarrow{P_{2,60}}$ and $\overrightarrow{P_{3,300}}$ (figure 3.6(b)). Obviously, a phase shift of 120° is also obtained between $\overrightarrow{P_{1,0}}$, $\overrightarrow{P_{2,240}}$ and $\overrightarrow{P_{3,120}}$.



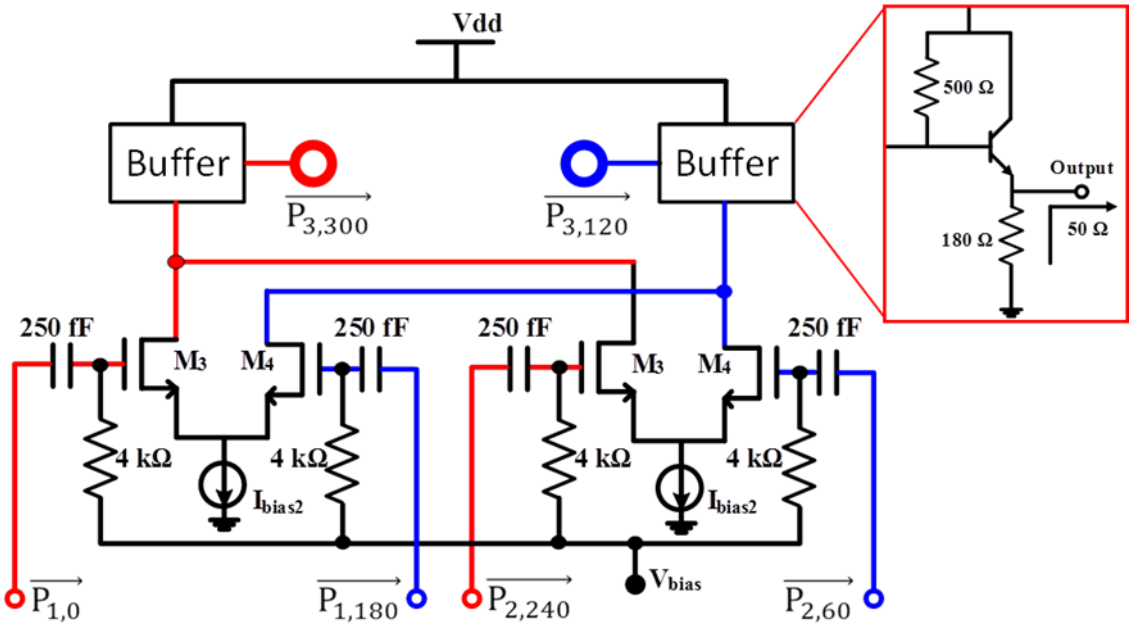
(a)



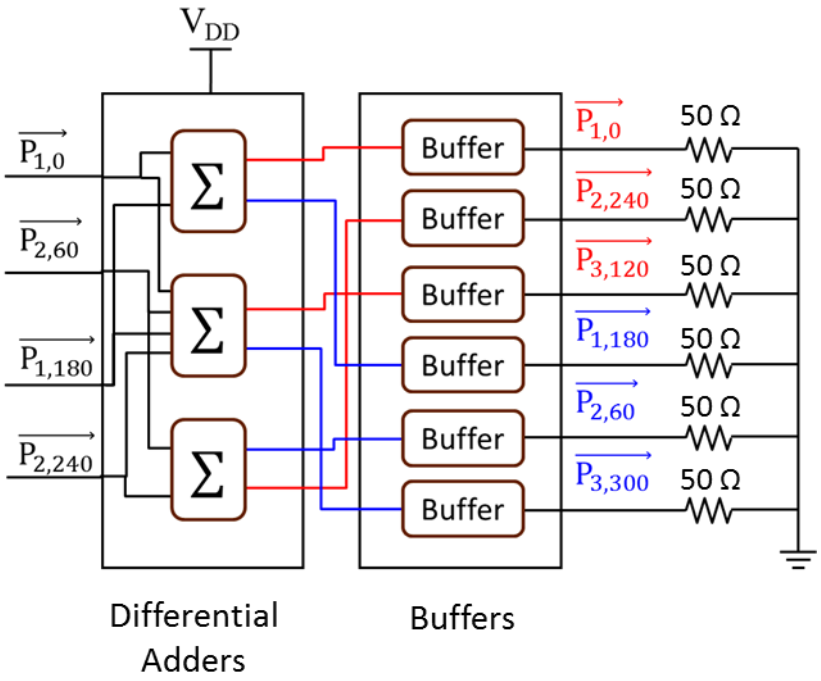
(b)

Figure 3.6: (a) Phase construction of $\overrightarrow{P_{3,300}}$ *and* $\overrightarrow{P_{3,120}}$, (b) Complete phasor diagram.

The architecture of the differential adder is presented in figure 3.7 (a). The differential adders consist of four inputs $\overrightarrow{P_{1,0}}$, $\overrightarrow{P_{2,60}}$, $\overrightarrow{P_{2,240}}$ and $\overrightarrow{P_{1,180}}$. It consists of two pairs of NMOS transistors (M_1, M_2, M_3 and M_4) having the same sizes (30 µm/0.25 µm). A bias current of 2.5 mA is applied at the source of each NMOS pairs.



(a)



(b)

Figure 3.7: (a) Architecture of the differential adder, (b) Block diagram of the three differential adders connected to six output buffers.

An output buffer is designed for 50-ohm impedance matching. The output of the adder bias the buffer in common collector configuration and having a high input impedance and a low output impedance, which allows the impedance matching on 50 ohms load. The size of the buffer's bipolar transistors is 0.5 µm/1.5 µm. Furthermore, in the architecture designed and

presented, in order to make the proposed circuit tunable, a differential varactor diode is used instead of the two fixed capacitors, as shown in figure 3.8. The biasing voltage referred here to as "*Vtune*" reverse biased the differential varicap diode at point X. A 10 kΩ resistor is connected at “point A” to provide a ground in DC mode of operation. A 2 pF coupling capacitor is used to isolate the DC bias voltage of $\overrightarrow{P_{2,60}}$.

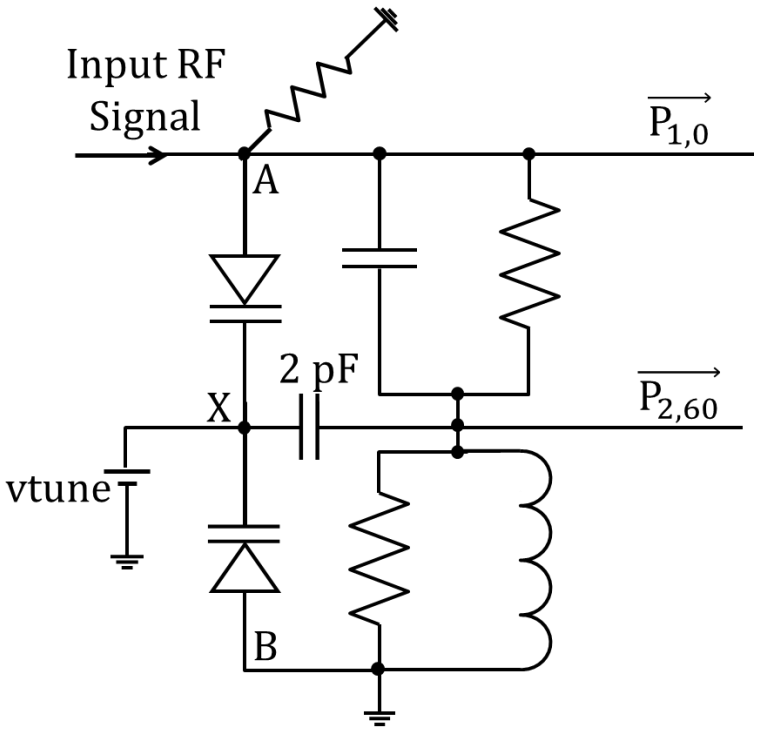


Figure 3.8: Electrical circuit diagram of the 60° phase shifter tunable at 8 GHz.

2.2. Post-layout simulation results of the 120° phase shifter

The layout of the differential 120° RF phase shifter using the BiCMOS SiGe:C 0.25 µm process is designed under the CADENCE® environment and is shown in figure 3.9. The overall chip area is 0.345 mm^2. The total power consumption is 130 mW, for a DC voltage of 3 V, which includes a power of 78 mW consumed by the output stages (50 Ω). The design of the layout is the first step for the implementation of the circuit. Parasitic elements are added if careful attention on the placement of the different components is not taken. Paracitics cannot be avoided, but by carefully placing the components symmetrically, they are minimised and added equally on the differential parts.

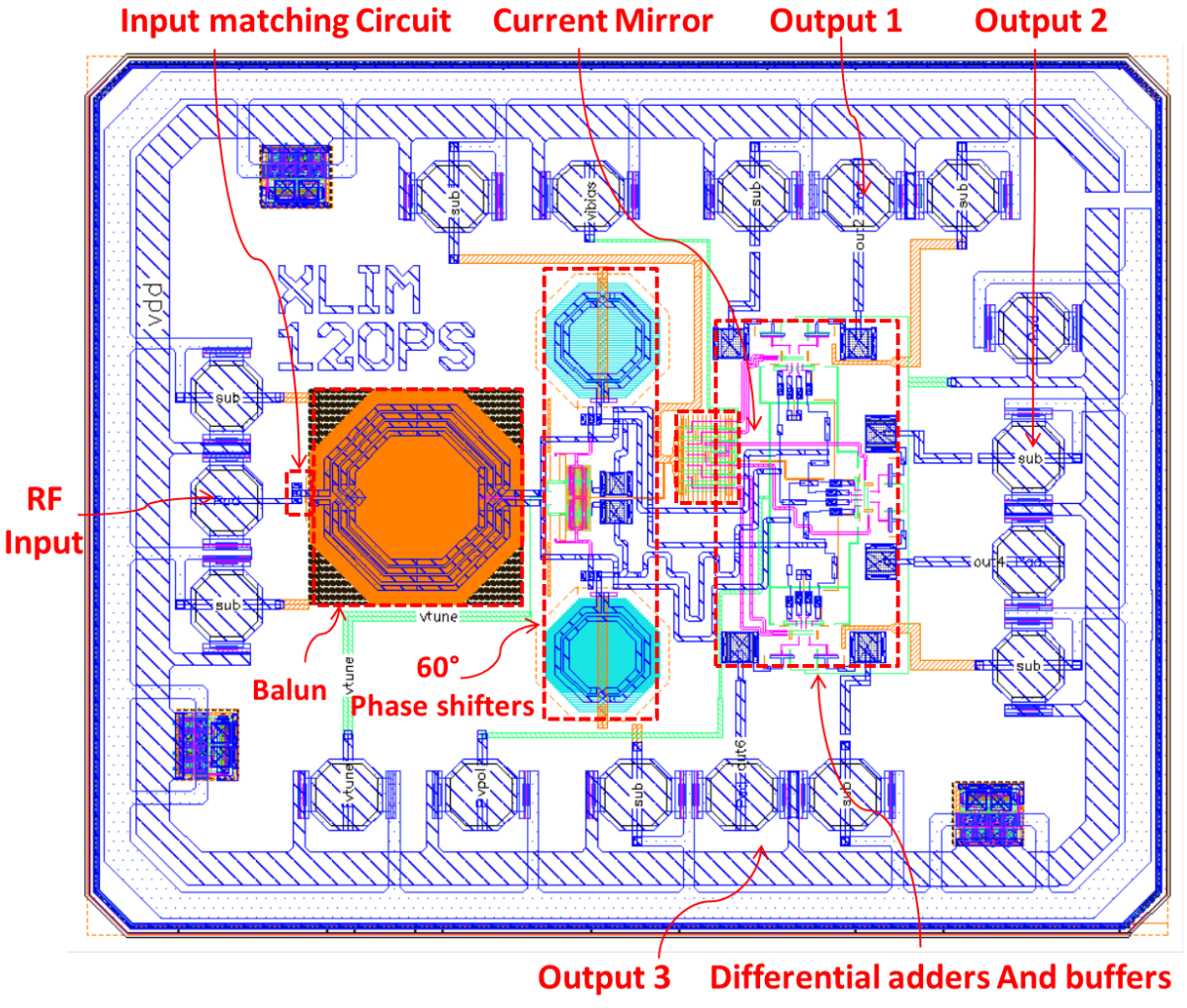


Figure 3.9: The layout of the 120° phase shifter.

During the design of the layout long connecting lines are used at the connections between the 60° phase shifter and the differential adders. Extra parasitic capacitance is added,

which adds additional phase shift. Metal 6 (higher metal level available with this technology) is used to reduce the parasitic effects. The remaining phase and amplitude imbalance were compensated by optimising the capacitance and resistance values in the RLC phase shifter.

The input of this phase shifter is a single RF signal; however, the output is six 120° differential signals. To simplify the measurements, only three 120° signals are provided at the output while integrated 50 Ω resistors are loading their complementary signals. Thanks to the use of varactor diodes, this circuit has the advantage of being tunable over 800 MHz band around 8.1 GHz. A 50 Ω input matching network is designed to match the circuit's input impedance to the source in order to ensure a maximum power transfer. As shown in figure 3.9, a good matching is obtained over a frequency bandwidth of [7.03 GHz, 8.57 GHz] for a frequency operating around 8 GHz.

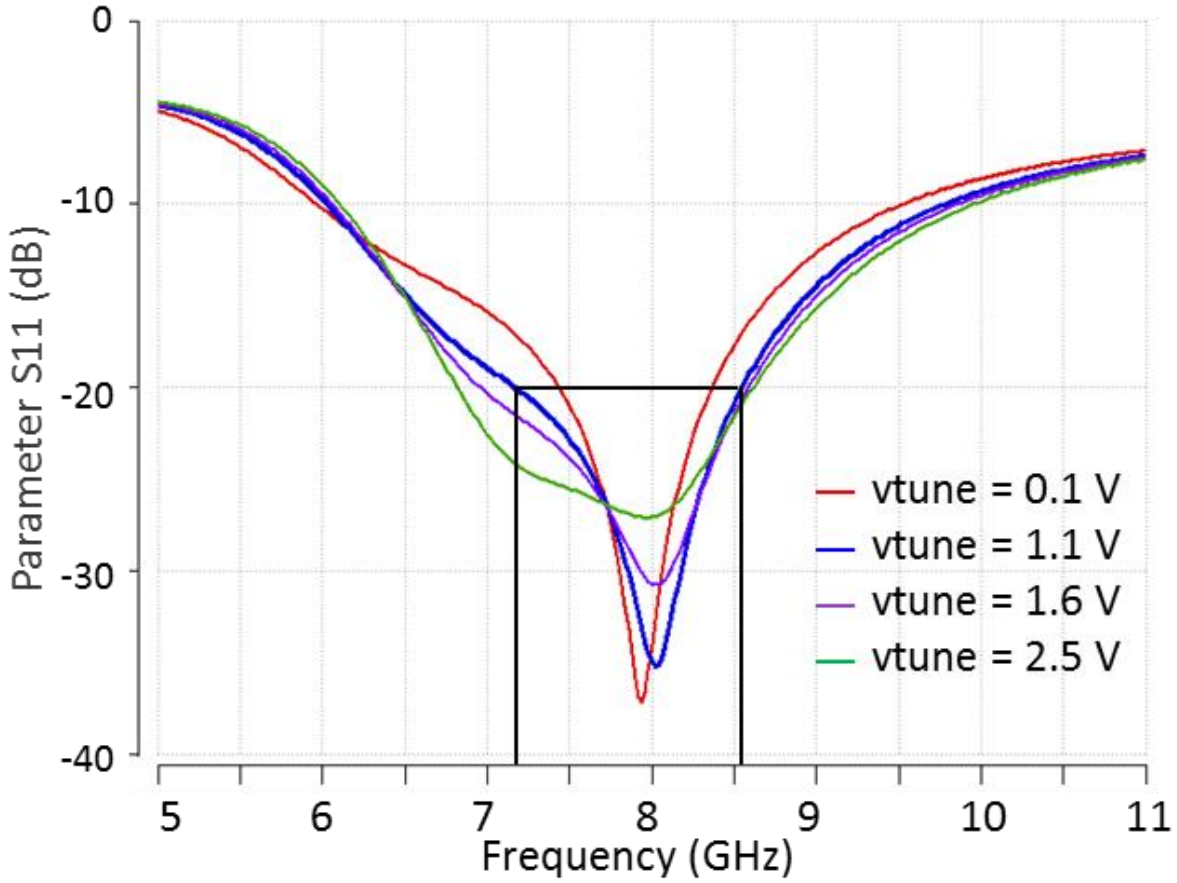


Figure 3.10: Input reflection coefficient (S11).

The results in figure 3.11 show that the circuit is tunable over a bandwidth of 800 MHz thanks to the tuning voltage "*Vtune*" which controls the capacitance presented by the

differential varactor diodes. Furthermore, the phase error between $\overrightarrow{P_{1,0}}$ and $\overrightarrow{P_{2,60}}$ is of the order of 2.75°/100 MHz.

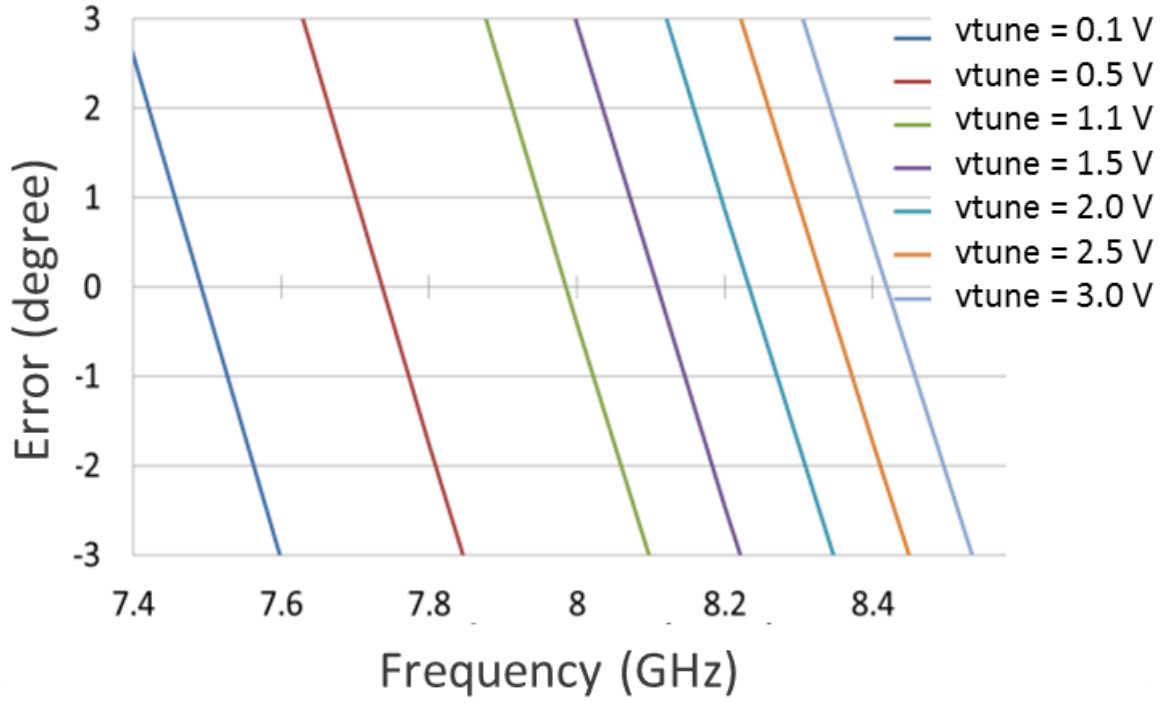


Figure 3.11: Phase error at the output of the 60° phase shifter

Moreover, as expected, the phase shift between the three differential signals at the output of the buffers and adders is 120° at 8 GHz. The phase errors obtained between the output signals $\overrightarrow{P_{1,180}}$, $\overrightarrow{P_{2,60}}$ and $\overrightarrow{P_{3,300}}$ after the extraction of the parasitic components generated by the layout are shown in figure 3.12 for different values of vtune with a resolution of 0.05 Volts. As can be seen on this figure, a maximum error of 3° is found when the frequency varies from 7.7 GHz to 8.5 GHz.

The amplitude error between the three 120° signals is shown in figure 3.13. A maximum error of 2 % between the three outputs at a frequency of 8 GHz is obtained and it remains under 2.5 % over the entire frequency band of the phase shifter.

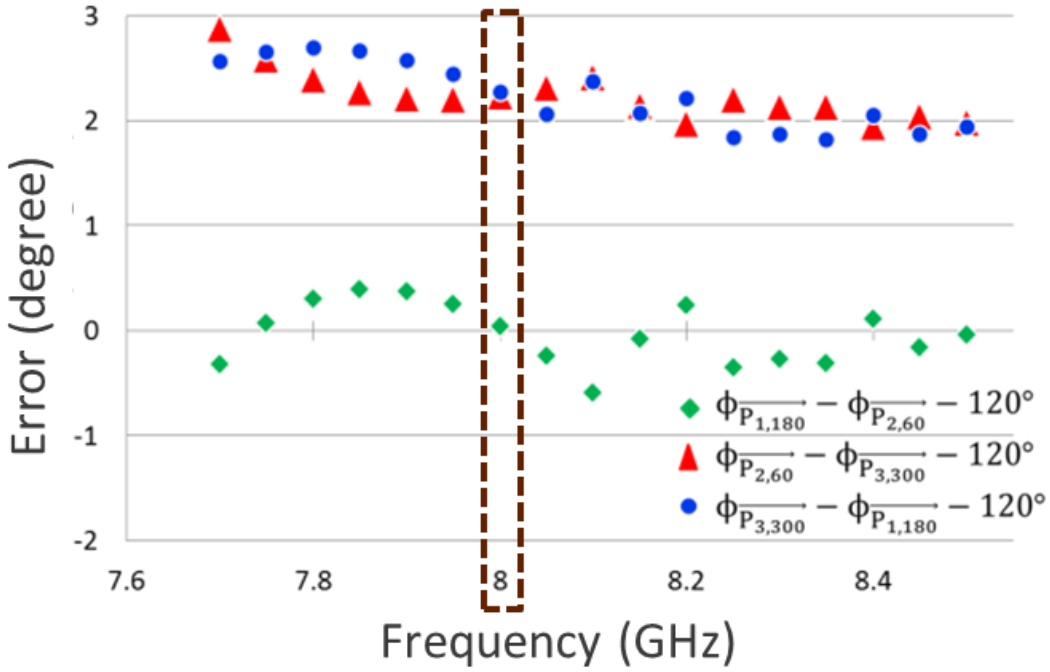


Figure 3.12: Phase errors between the three output signals.

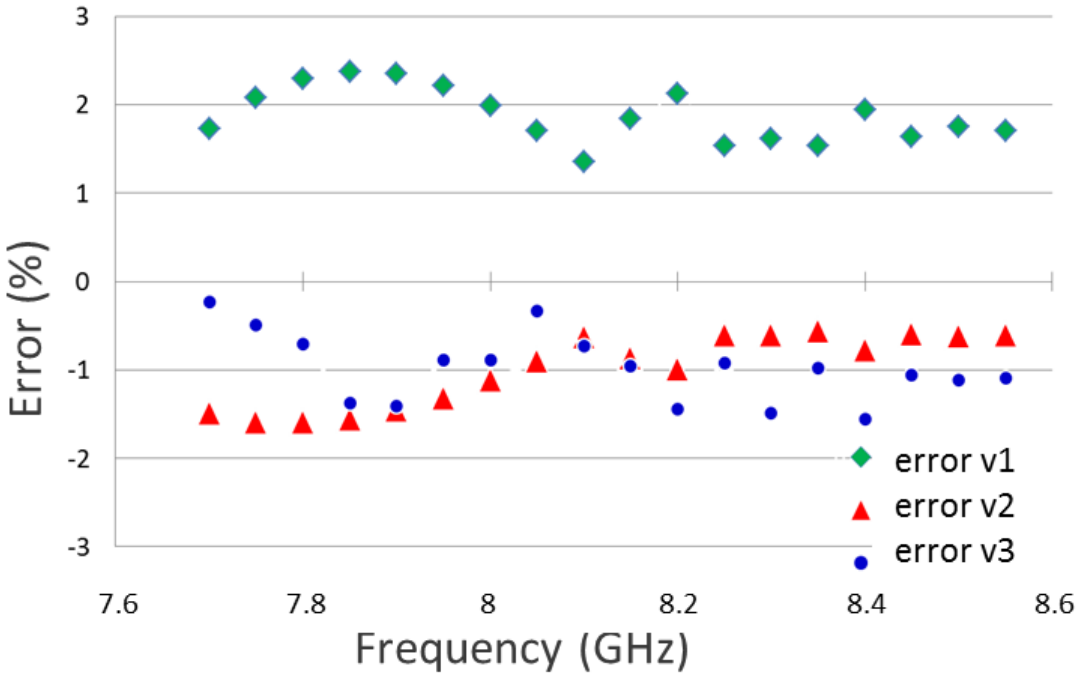


Figure 3.13: Amplitude errors between the three output signals.

The summary of the post layout simulated results and characteristics of the proposed tunable 120° active RF phase shifter is shown in Table 3.1.

Table 3.1: Summary of performances of the differential 120° tunable active phase shifter at 8 GHz.

Parameters	**Values**
Supply voltage	**3 V**
Center frequency	**8 GHz**
DC consumption (buffers)	**78 mW**
DC consumption (global)	**130 mW**
frequency range	**(7.7 GHz - 8.5 GHz)**
Chip area	**0.5x0.69 mm^2**
Phase error	**Less than 3°**
Amplitude error	**Less than 2,5 %**

The post-layout simulation results show a tunable operation over a 10 % frequency band around 8 GHz. Furthermore, the phase error, around 120°, is less than 3° when the frequency varies from 7.7 GHz to 8.5 GHz. The variations in amplitude at this frequency band are less than 2.5 %. This phase shifter is intended to be part of the triple-push Injection-Locked oscillator for beamforming applications at 24 GHz.

3. Injection-locked triple-push VCO based RF active phase shifter

Active phase shifters are important circuits when it comes to the beamforming applications in 5G technology. In chapter 1, the advantage of the beamforming in the millimetre waves has already been overviewed. Also, we have discussed in brief different architectures of the phase shifter using vector modulators, coupled oscillator arrays and injection locked oscillators. Due to the advantage of the linear phase shifting by injection locking in the triple-push oscillator, in this dissertation, active phase shifting is performed by injection locking in a triple-push VCO.

As we saw previously, to steer the beam of the radiation pattern of an antenna array, active phase shifters can be implemented at different stages. Figure 3.14 shows the generation of the active phase shifting at different levels of the phased array transmitter, limited to the case of an array made of two simple elementary antennas. Each of these topologies has advantages and drawbacks as listed below:

- *RF Phase Shifting:* The phase-shifted architecture on the RF path has the advantage of consuming less energy than other architectures given since only one baseband/IF stage is used regardless of the number of elementary antennas in the network [66] [67]. However, if the phase shift losses are not constant as a function of the programmed phase shift, then variable gain amplifiers should be used to prevent degradation on the antenna array radiation pattern. Besides, in order to fully integrate the device on silicon and for high-frequency applications, the design of such low-loss phase shifters can be complex.
- *IF Phase Shifting:* The intermediate frequency is, by definition, lower than the RF frequency, so the design and integration of phase shifters on this path is facilitated. Nevertheless, the value and therefore the size of the passive components required for the design of these phase shifters (inductors, capacitors, transmission lines etc....) is inversely proportional to the frequency, which can lead to a significant increase in the surface area on silicon for the complete system. Moreover, it is easy to understand that this architecture is less interesting than the previous one in terms of consumption since, in this case, an equal number of IF/RF conversion mixers have to be designed for each radiating elements.

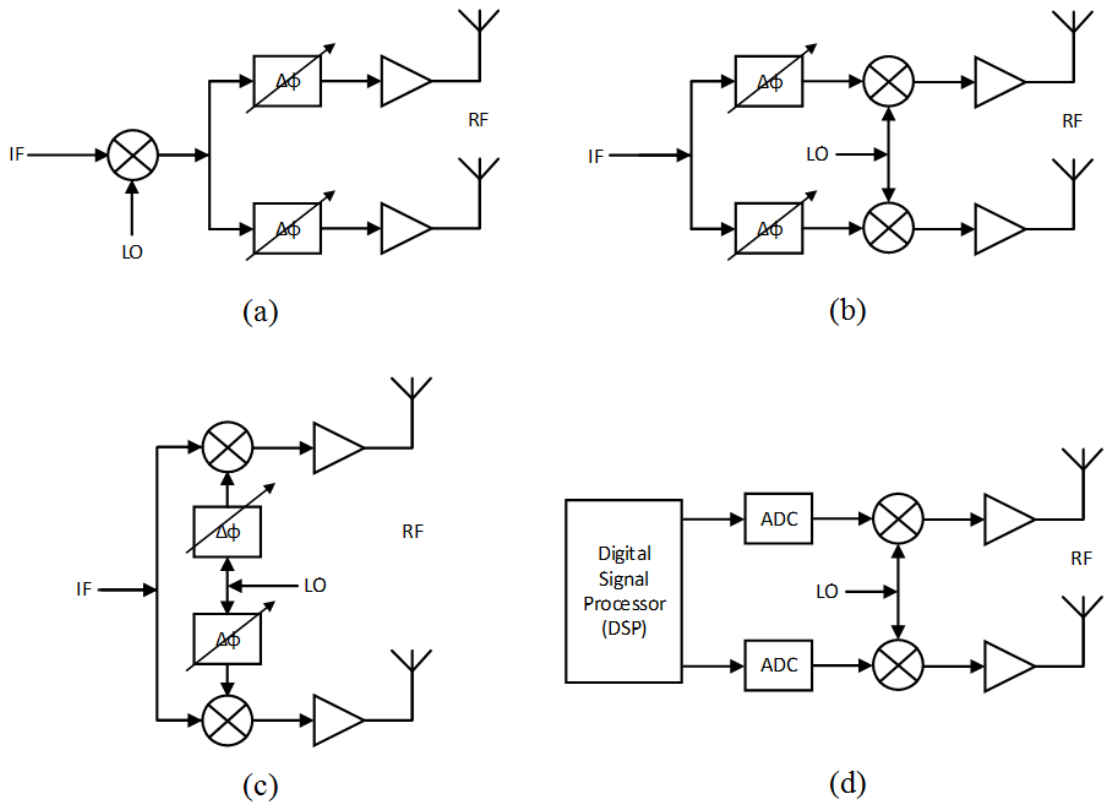


Figure 3.14: Different architectures for implementing the RF phase shift: (a) on the RF path; (b) on the IF path; (c) on the LO path; (d) in the digital baseband

- *LO phase shifting:* Since the best performances of the IF/RF conversion mixer is obtained when it is controlled with a high level LO signal, the LO path control circuits have to operate in saturation. Under these conditions, the sensitivity of the mixer gain to the amplitude variation of the LO signal is low and therefore, the variation in the amplitude of the RF signal for different phase shifts, generated on the LO path, will be negligible [68]. This solution generally presents the best trade-off for a complete integration of the device on silicon.

- *Digital baseband:* The last solution is to generate the baseband phase shift using a digital signal processor. Although this solution offers the greatest flexibility and high phase shift accuracy, the fact remains that the consumption of the complete device can be excessive given that this system is equivalent to N parallel transmitter/receiver (for N radiating elements) not sharing any circuit except the frequency synthesiser. Since multiple mixers and high-speed ADCs are required, so substantial complexity and high-power consumption are resulted in.

In this context, after comparing different topologies to implement the phase shifter, in this dissertation, we choose to apply active phase shifter in LO path due to the fact that this solution provides the best trade-off for a complete integration of the device on silicon. Also, the overall system performances is not sensitive to the performances of the active phase shifter in the LO path. Indeed, in the LO path, the drawback due to noise figure, non-linearity, losses and amplitude mismatches of the phase shifters do not imply a direct impact on the signal quality. The active phase shifter designed in the thesis is a combination of the 120° phase shifter and the triple-push VCO presented previously. The latter is injection locked by the 120° phase shifter. Figure 3.15 presents the architecture of the phased antenna array and the block diagram of the proposed active phase shifter.

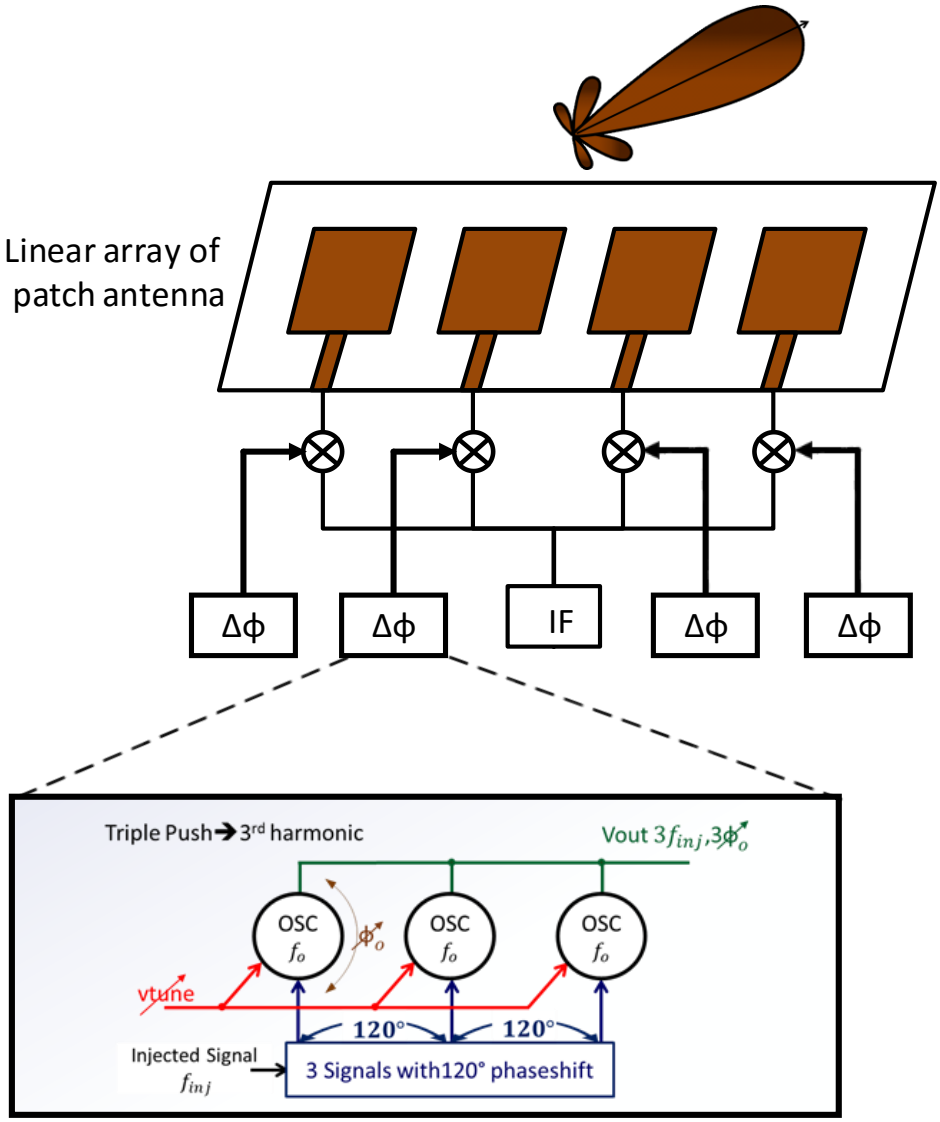


Figure 3.15: The architecture of the phased antenna array for the beamforming application in LO path.

In the next section, the architecture of the injection locked triple-push VCO is presented. The main objective of this combine circuit is to cover the 360° phase shift for the application of beamforming in 5G technology.

3.1. The architecture of the Injection Locked Triple-push VCO (ILTPVCO)

The block diagram of the combine circuit is presented in figure 3.16, combining the 120° phase shifter and the triple-push VCO. At the input, a matching network has been designed to match the input to 50 Ω and thus ensure a maximum power transfer from the injection source to the phase shifter. This matching circuit is based on a capacitive bridge. Then, a balun is used to generate a differential signal from a single ended one. The balun topology is provided by the library of the NXP Semiconductor design kit. This differential signal is then applied to the differential 120° injection phase shifter circuit associated with the triple-push VCO. Thus, the triple-push VCO locked by injection generates a fine and linear phase shift between the injected signal and the output signal of the VCO in the range ±30°, which would provide a linear phase shift of ±90° at the output of the triple-push. Differential amplifiers followed by buffers are used in our design at the output of each VCO. The high input impedance buffer isolates the VCO from the output circuit. The buffers are designed so that the output signal of the triple-push is well matched on 50 Ω. The global circuit is divided into the following blocks:

- Input balun with input matching circuit
- Differential three-phase injection circuit (60° phase shifters and differential adders)
- Triple-push VCO (buffer and amplifier included)

Firstly, the triple-push VCO, presented in chapter 2, is simulated to operate at the center frequency of 24 GHz. Then it is connected to the 120° phase shifter and simulated to observe the phase shift generated by the entire circuit. Synchronising and simulating the combine circuits is a very typical task as we need to make sure that all the steps shown in the following flow chart are respected:

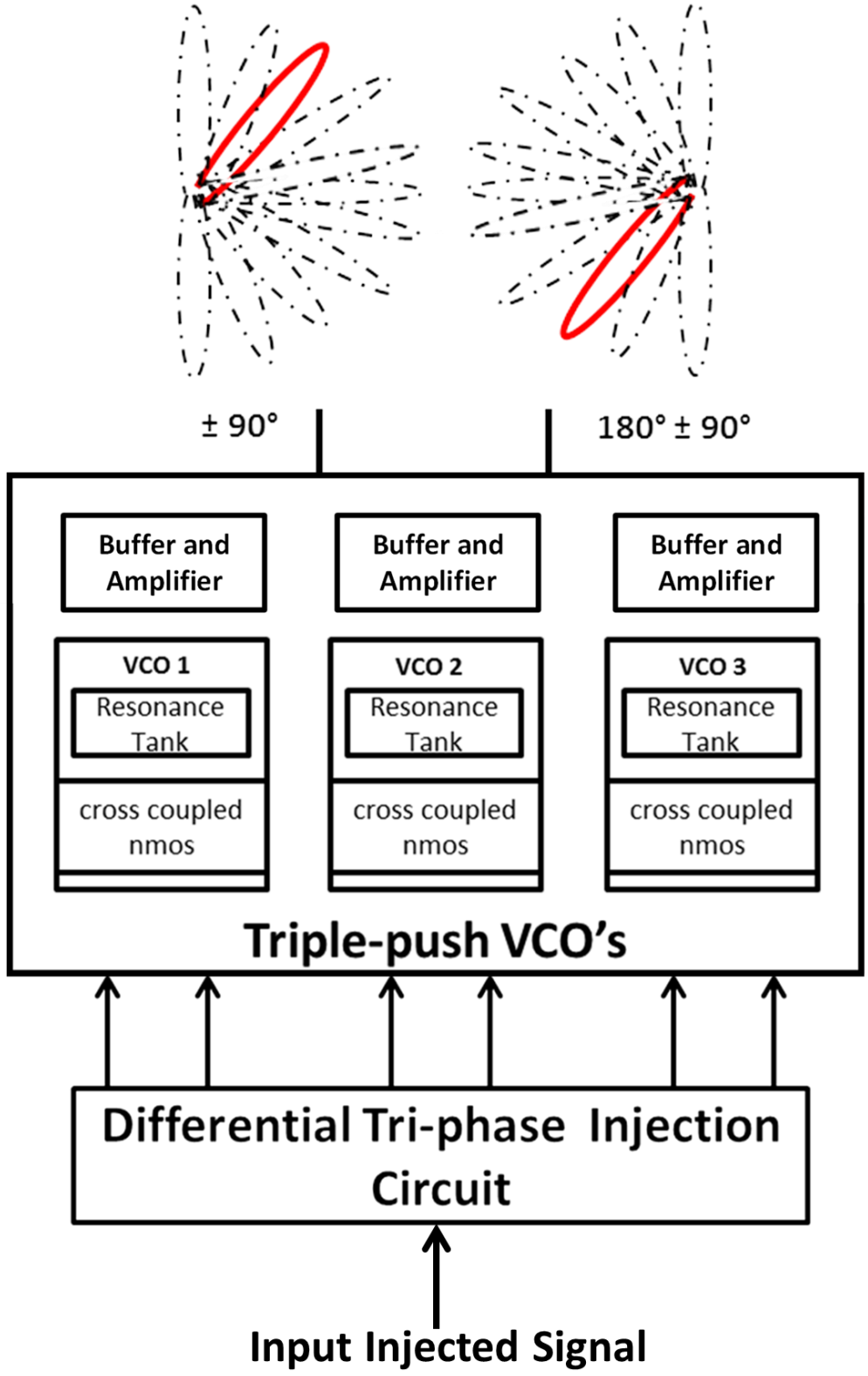
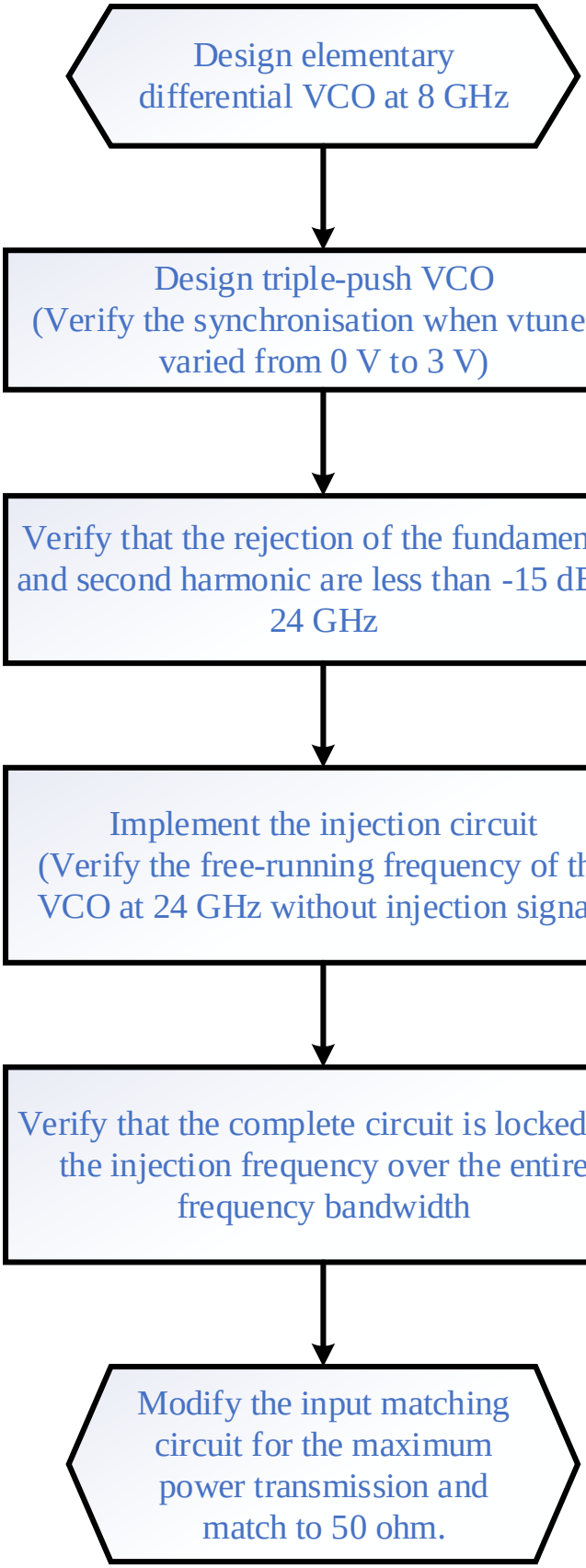


Figure 3.16: Block diagram of the injection locked triple-push VCO.


Design elementary differential VCO at 8 GHz
Design triple-push VCO (Verify the synchronisation when vtune is varied from 0 V to 3 V)
Verify that the rejection of the fundamental and second harmonic are less than -15 dB at 24 GHz
Implement the injection circuit (Verify the free-running frequency of the VCO at 24 GHz without injection signal)
Verify that the complete circuit is locked on the injection frequency over the entire frequency bandwidth
Modify the input matching circuit for the maximum power transmission and match to 50 ohm.

The proposed injection locked triple-push VCO is quite complex and it is also complicated to draw the layout accurately. So, extreme care is taken while drawing the connections of every block. The circuit simulation starts with the synchronisation of the triple-push oscillator along with output buffers. Then, the injection circuit is attached. It is very difficult to be sure of the stability of such a circuit. The CAD tools do not allow to qualify this behaviour. We choose two approaches, one with the time domain simulation for which we simulate up to a duration of 1 µs. Furthermore, another one by simulating with spectre RF with PSS analysis (Periodic Steady State Simulation Analysis). We considered that, when these two simulations give the same results, the results are correct.

3.2. The layout of the IL TP VCO

The layout of the injection locked triple-push VCO using the BiCMOS SiGe:C 0.25 µm process is designed under the CADENCE® environment and is shown in figure 3.17.

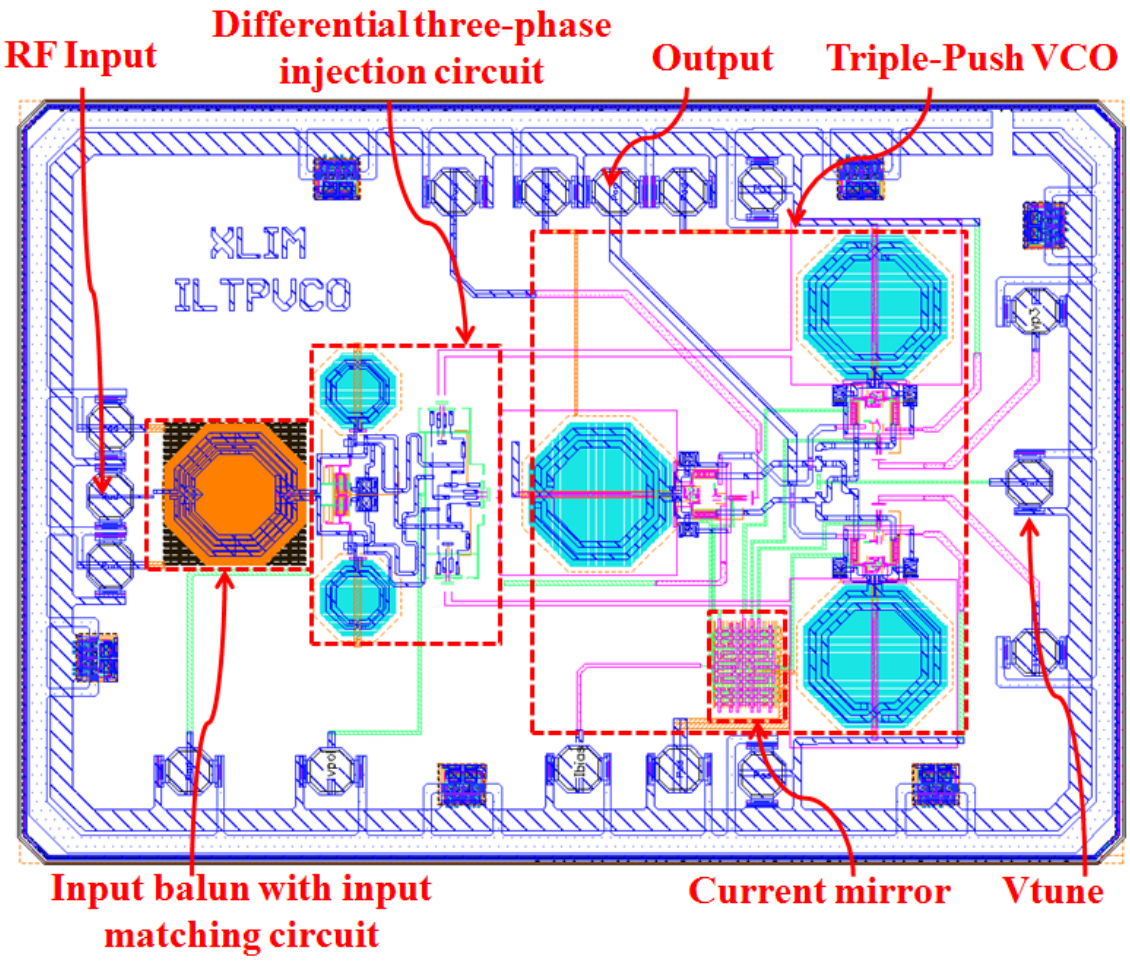


Figure 3.17: The layout of the injection locked triple-push VCO.

The overall chip area is 2.174 mm^2. The input is a single RF signal at 8 GHz and due to triple-push behaviour, the output of the circuit is at 24 GHz.

3.3. Post layout simulation results

First of all, transient analysis is performed with spectre RF in order to verify that the triple-push VCO is working well without injection. Then, a post layout harmonic balance simulation with an RLC extraction tool is made. The total power consumption of the overall circuit is 158.73 mW with a DC voltage of 3 V, which includes 39.12 mW consumed by the buffer stages. Table 3.2 presents the static conditions of the post layout simulation of the global circuit.

Table 3.2: Static parameters of the overall circuit

Parameters	Values
Supply voltage [V]	**3**
Reference current [mA]	**2.5**
Total current consumption [mA]	**52.91**
Power consumed by buffers [mW]	**39.12**
Total power consumption [mW]	**158.73**

3.3.1. The performances of the active phase shifter without injection

Figure 3.18 shows the variation of the free-running oscillation frequency f_0, without injected signal, of the global circuit as a function of the control voltage *Vtune* in the post layout simulation. The circuit oscillates from 20.79 GHz to 24.81 GHz when the *Vtune* of the varactor diode is varied from 0 V to 3 V.

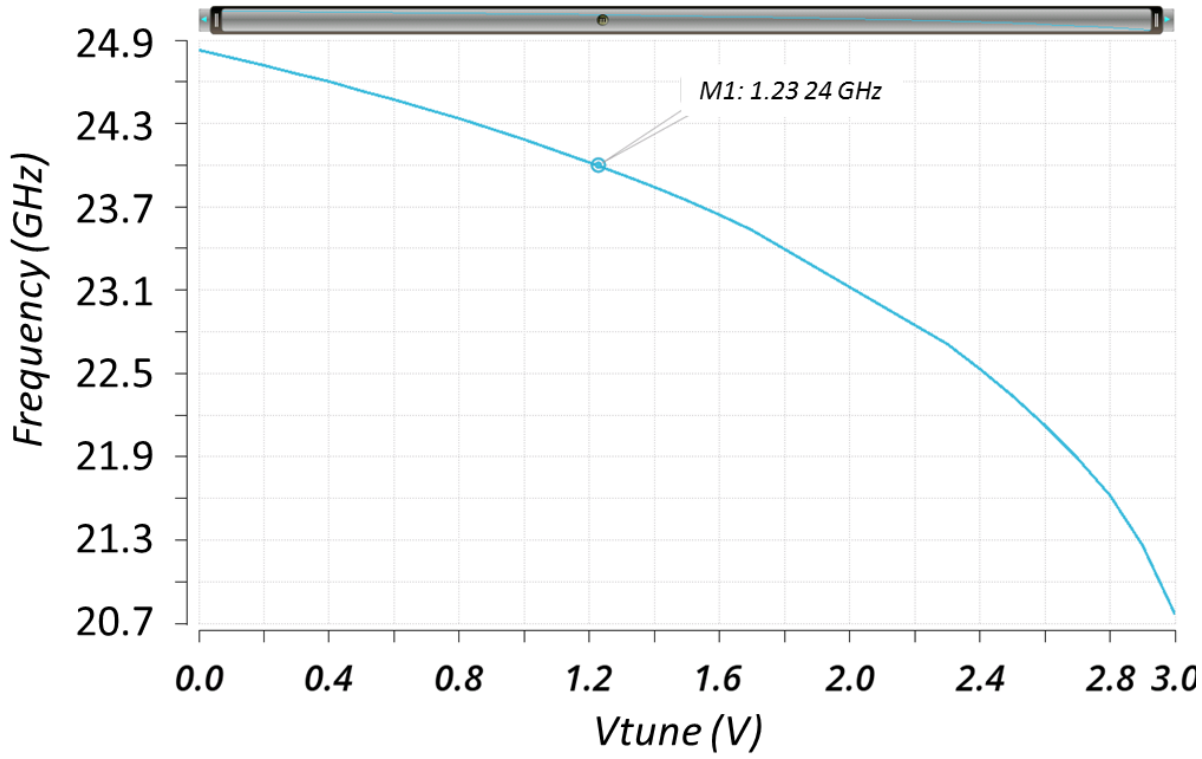


Figure 3.18: Frequency vs *Vtune* for the global circuit without injection.

It should be noted that the output of three differential adders of 120° phase shifter circuit is attached to the drains of the cross-coupled differential NMOS pair of three VCOs respectively.

3.3.2. The performances of the active phase shifter with injection

The input of the injection locked triple-push VCO is a single-ended RF signal at a power Pinj = 5 dBm at 8 GHz. A 50 Ω input matching network is designed to match the circuit's input impedance to the source in order to ensure a maximum power transfer. As shown in Figure 3.19, a matching better than -20 dB is obtained over a bandwidth of [6.96 GHz, 8.5 GHz] for *Vtune* = 0.6 V.

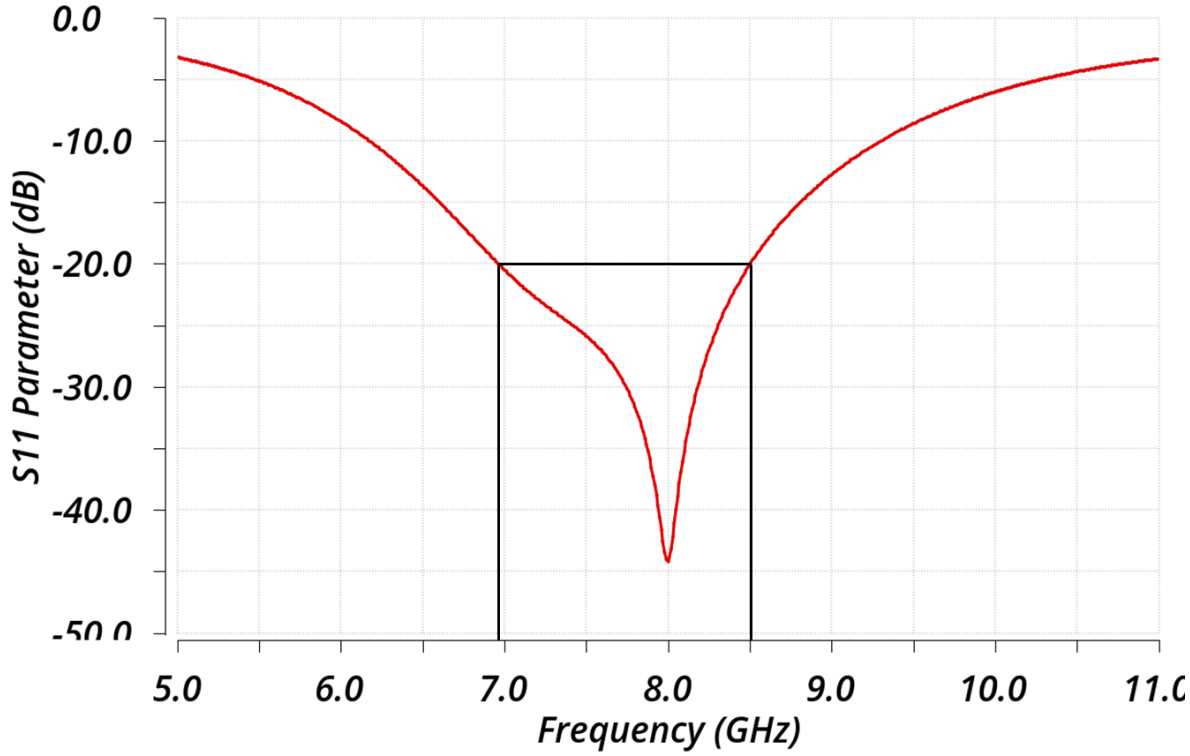


Figure 3.19: Input reflection coefficient (S11)

When the injection signal P_{inj} = 5 dBm is applied, with a frequency f_{inj} = 8 GHz and $\phi_{inj} = 0°$, a phase shift $\Delta\phi = \phi_{inj} - \phi_0$ is obtained by changing the free-running frequency f_0 via *Vtune*. We note that this phase shift $\Delta\phi$, between the injection signal and the output of one VCO, is multiplied by three ($3\Delta\phi$) at the output of the triple-push. The main objective is to obtain a linear phase shift between the injection signal and the output of the VCO within ±30°, which becomes ±90° at the output of the triple-push. The injection locked triple-push VCO is having a frequency variation of 230 MHz to obtain the phase shift of ±90° at the output of the active phase shifter. Figure 3.20 presents the variations of the phase shift obtained between the injection signal and the output signal of one VCO at 8 GHz with respect to *Vtune* in "blue colour". The phase shift obtained at the output of the triple-push at 24 GHz is considered as the reference phase when $\Delta\phi = \phi_{inj} - \phi_0 = 0°$. Now when $\Delta\phi$ is varied the corresponding phase shift at the output of the triple-push VCO is plotted in "red" with respect to *Vtune*. As we can see, the phase shift obtained between the injection signal and the output of one VCO is nearly linear between ±30° and the phase shift variation at the output of the overall active phase shifter is also almost linear between ±90.

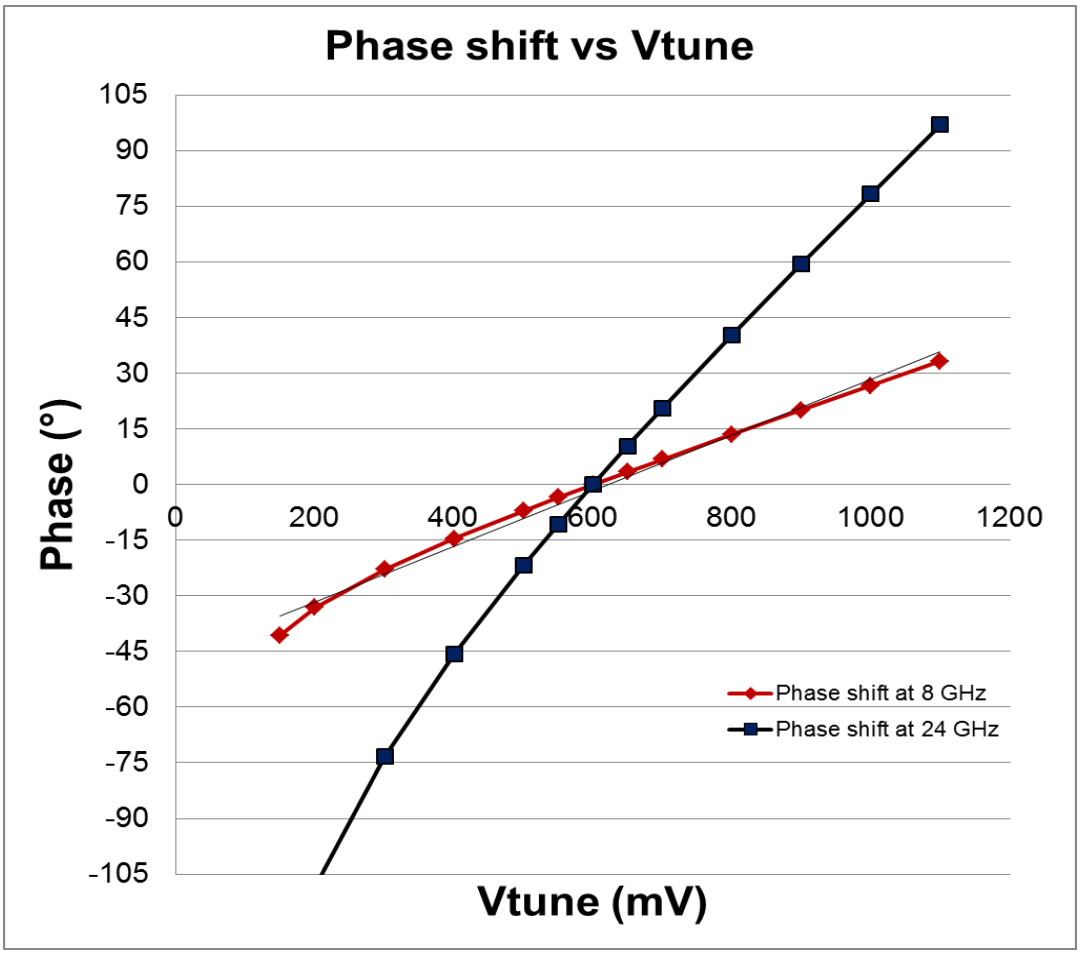


Figure 3.20: Post layout simulation of the phase shift obtained between the injection signal and output of one VCO with respect to *Vtune* and corresponding phase shift obtained at the output of the triple-push VCO

Figure 3.21 shows the variation of the output power vs *Vtune*. The variation of the output power is roughly 0.3 dB over the entire locking bandwidth with a maximum output power of -3 dBm. Table 3.3 summarises the performances of the proposed active phase shifter with post layout results.

Table 3.3: Post layout results of the active phase shifter

	Post-layout
Free running oscillation frequency (GHz)	**20.79 - 24.81**
Injection frequency (GHz)	**8**
Injection power (dBm)	**5**
Phase shift (°)	**180°**
Mean output power at 50 Ω (dBm)	**≈ -3.17**

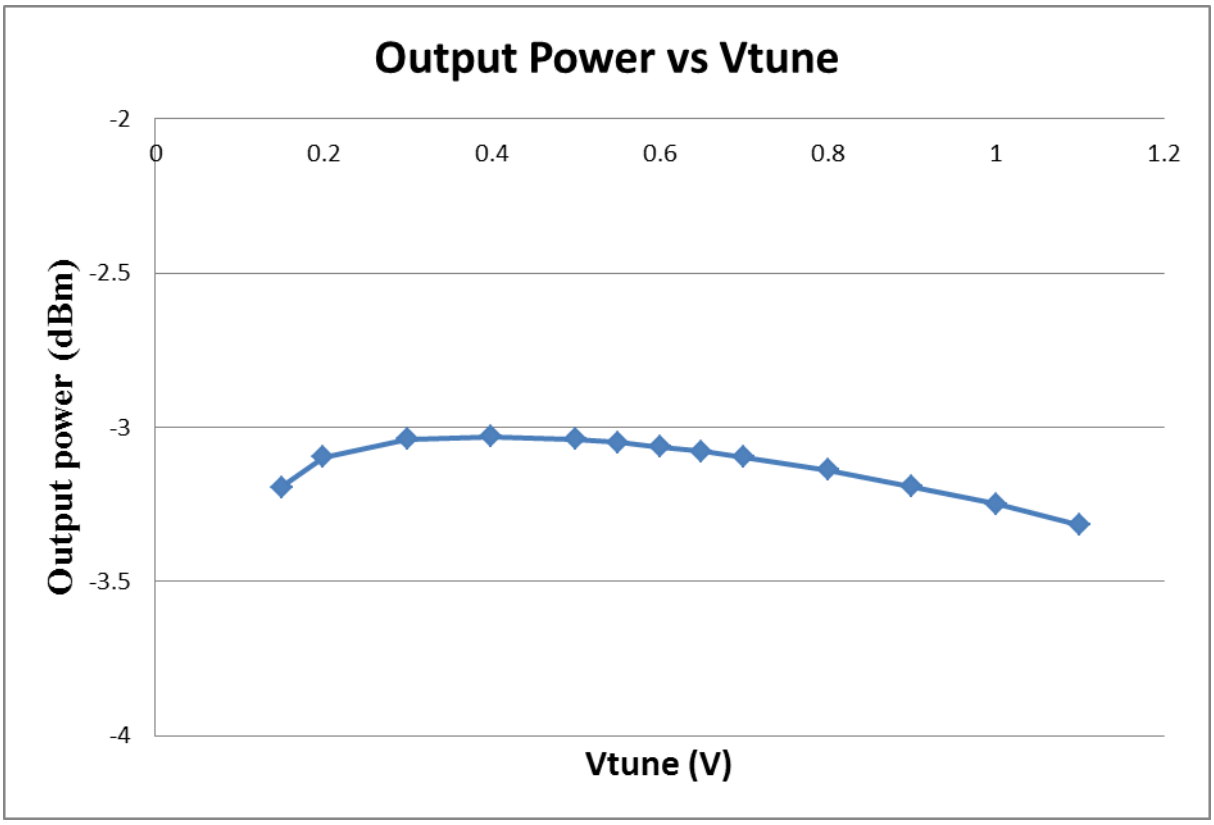


Figure 3.21: Post layout simulation result of the output power with respect to *Vtune*.

4. Resume of the phase shifter results

The performances of the proposed active phase shifter are compared with other recently published works in Table 3.4. The proposed active phase shifter is designed in a low-cost BiCMOS technology. It is to be noted that it is intended to cover 180° (±90°) phase shift range linearly with good performances. This active phase shifter is commanded by a single source (*Vtune* of the triple-push VCO). The phase shift from -90° to 90° is obtained by varying the single voltage *Vtune* of the Injection Locked Triple-Push VCO. This is an important advantage over digitally controlled phase shifters, where the number of commands is more than one (2-bit/4-bit/6-bit etc…). Consequently, the design and calibration would be complex. Moreover, in the case of the digitally controlled phase shifter, additional ADC/DAC converters are required either integrated on-chip or added separately. Furthermore, in our case, a complete 360° linear phase shift range can be obtained by simply flipping the outputs through a phase sign selector. In that case, an additional command will be required for the phase sign selection.

Table 3.4: Comparison of the performances of the developed system with the literature

Parameters	This Work	[22]	[69]	[70]	[71]
Technology	0.25 µm BiCMOS	65 nm CMOS	65 nm bulk CMOS	65 nm CMOS	65 nm CMOS
Nb. of commands	Analog (1)	Analog (4) Digital (4)	Analog (2) Digital (6)	Analog (3)	Analog (2)
Frequency (GHz)	24	42.75 – 49.5	20.3 – 23.4	24/28	24
Phase shift range (°)	±90*/ continuous	±90*	300/ continuous	0-55/ continuous	62/ continuous
Power Consumption (mW)	158	85	84	NR	13
Surface Area (mm^2)	2.174	2.8	0.23	0.98	0.135
Amplitude mismatch (dB)	0.28	± 0.35	NR	NR	±1.15
Supply Voltage (V)	3	1	1.2	-1.9 to 1.5	NR

NR: Not reported

* ± 180° by adding a phase sign selector with an additional command

5. Conclusion

In this chapter, a new architecture of an original active phase shifter is designed at 24 GHz and implemented in the QUBiC4X 0.25 µm SiGe:C BiCMOS process of NXP Semiconductors. Phase control is performed using a triple-push oscillator injection locked by a 120° phase shifter, for a linear phase variation of 180°. The first part of the chapter is devoted to the analysis of injection locking in a triple-push oscillator. Then, an original architecture of a fully integrated differential 120° tunable active RF phase shifter, is presented. The post layout simulation results show tunable operation over a 10 % frequency band around 8 GHz. Furthermore, the phase error, around 120°, is less than 3° when the frequency varies from 7.7 GHz to 8.5 GHz. The variations in amplitude at this frequency band are less than 2.5 %. In the second part, the design and implementation of the full phase shifter at 24 GHz was detailed. Post layout simulation results showed that, with an injected power of 5 dBm, a linear phase shift between -90° and + 90° is obtained. This active phase shifter is intended to be associated with an elementary antenna to subsequently constitute a complete antenna array that can be used for data transmission, for example in 5G technology.

Final Conclusion

Final Conclusion

The work presented in this thesis consists in designing an original integrated circuit in the mm-wave domain for beamforming applications. Associated to an antenna array, beamforming is performed, i.e. it allows the orientation and control of the radiation pattern. An original active phase shifter is thus designed to be implemented on the LO path with the objective to steer the beam in the desired direction. Associated with an antenna array, this phase shift control allows to compensate for the losses due to the unavoidable increase in frequency at millimetre waves. The main objective is to obtain a continuous linear phase shift from -90° to 90°. Thus, this active phase shifter ensures a tunable phase shift between the input and the output. It is based on an original Injection Locked Triple-Push Voltage Controlled Oscillator (ILTPVCO) at 8 GHz. Due to the triple-push behaviour, the operating frequency of the output signal is at 24 GHz. The objective of this dissertation is to present the analysis and design of this fully integrated active phase shifter implemented in the QUBiC4X 0.25 µm SiGe:C BiCMOS process of NXP semiconductors.

This work was organised in 3 chapters, followed by references.

Chapter I, "*Introduction to the research work*", allows us to introduce the context and framework of this dissertation. In this first chapter, we have briefed the future vision of the 5G technology, its key capabilities, the spectrum, applications and different research challenges from where we obtain the motivation of the thesis. The principle and different types of antenna arrays, as well as the main characteristics of linear and planar antenna arrays, are presented first. Then, the different techniques of radiation pattern synthesis are analysed. In addition, a state of the art of the different architectures for implementing phase shifts, used in the literature, is established. Finally, the objective of the thesis is presented by providing the new architecture of the Injection Locked Triple-Push Voltage Controlled Oscillators (ILTPVCO).

Chapter II, "*Behavioural analysis of triple-push VCO and design of a new triple-push VCO*", is devoted to design a new architecture of a 24 GHz triple-push VCO and its implementation in the QUBiC4X 0.25 µm SiGe:C BiCMOS process of NXP Semiconductors.

The first part of the chapter is devoted to the analysis of the LC VCO design and the theoretical study of the triple-push VCO. Thereafter, mode analysis of the triple-push oscillators is presented explaining the condition to ensure an odd mode of operation for the successful triple-push operation. Finally, the post layout simulation results of the triple-push VCO are presented. The post layout simulation results confirm that the circuit delivers a steady output signal of -5.76 dBm at 24 GHz. The overall power consumption, including the three output buffers, is only 113.64 mW from a 3 V supply voltage. More than 27.67 dB rejection is obtained for the fundamental and more than 19.65 dB for the second harmonic.

Chapter III, "*Injection locked triple-push VCO based active phase shifter*", is mainly dedicated to the design of the proposed active phase shifter. A new architecture of an original active phase shifter is designed at 24 GHz and implemented in the QUBiC4X 0.25 µm SiGe:C BiCMOS process of NXP Semiconductors. Phase control is performed using a triple-push VCO injection locked by a primary 120° phase shifter, for a linear phase variation of 180°. The first part of the chapter is devoted to the analysis of injection locking in a triple-push oscillator. This injection in a triple-push oscillator requires the generation of three injected signals with 120° phase shift between them, each of these signals is applied on each elementary VCO. In these conditions, an original architecture of a fully integrated differential 120° tunable active phase shifter, called primary, is described. The post layout simulation results show tunable calibration over a 10 % frequency band around 8 GHz. Furthermore, the phase error, around 120°, is less than 3° when the frequency varies from 7.7 GHz to 8.5 GHz. The variations in amplitude at this frequency band are less than 2.5 %. In the second part of this chapter, the design and implementation of the full active phase shifter at 24 GHz was detailed. Post layout simulation results showed that, with an injected power of 5 dBm, a linear phase shift between -90° and + 90° is obtained. This active phase shifter is intended to be associated with an elementary antenna to subsequently constitute a complete antenna array that can be used for data transmission, for example in 5G technology.

PERSONAL CONTRIBUTIONS

- The study of the beamforming basics using different methods to control the shape of the radiation pattern.

- The state of the art of different methods to control the radiation pattern by phase synthesis. Different architectures using vector modulator, coupled oscillator arrays and injection locked oscillator arrays are discussed in detail.
- Triple-push oscillators and its mode analysis is briefed. Different architectures of previous triple-push oscillators are reviewed.
- The design of a new architecture of a differential triple-push VCO coupled through the varactor diodes and separating the output 3rd harmonic from the coupling circuit is presented.
- The layout design of the triple-push VCO in the QUBiC4X 0.25 µm SiGe:C BiCMOS process of NXP semiconductors and the post layout simulation results.
- The study of the injection locking phenomenon in the triple-push VCO.
- The analysis of a 120° phase shifter and the design of a novel architecture of a differential tunable 120° phase shifter at 8 GHz integrated in the 0.25 µm BiCMOS SiGe:C technology with post layout results.
- The analysis and design of the Injection Locked Triple-Push VCO (ILTPVCO) and its layout in the QUBiC4X 0.25 µm SiGe:C BiCMOS process of NXP semiconductors.
- Post layout simulations of the global circuit.

FUTURE PROSPECTS

- The fabrication of the designed Injection Locked Triple-Push VCO (ILTPVCO) on the QUBiC4X 0.25 µm BiCMOS SiGe process of NXP Semiconductors.
- Improvement of the phase noise figure of the designed triple-push VCO circuit.
- The design of a phased antenna array with the designed injection locked triple-push VCO. The fabricated injection locked triple-push VCO could be associated with a planar or a hybrid antenna array to demonstrate the beamforming feasibility.

List of scientific publications

- **Bhanu Pratap Singh Jadav**, Mariem Kanoun, Jean-Marie Paillot and David Cordeau, “A New 8 GHz Differential 120° Tunable Active Phase Shifter Integrated in a 0.25 µm BiCMOS SiGe:C Technology”, IEEE 26th International Conference on Electronics Circuits and Systems (ICECS) Genova, Italy November 2019.
- **Bhanu Pratap Singh Jadav**, Mariem Kanoun, Jean-Marie Paillot and David Cordeau, “A New 24 GHz Triple-Push Voltage Controlled Oscillator Architecture in 0.25 µm BiCMOS SiGe:C Technology”, IEEE 26th International Conference on Electronics Circuits and Systems (ICECS) Genova, Italy November 2019.
- **Bhanu Pratap Singh Jadav**, Mariem Kanoun, Jean-Marie Paillot et David Cordeau, “Une nouvelle architecture de déphaseur différentiel 120° accordable à 8 GHz intégré en technologie BiCMOS SiGe:C 0,25 µm”, XXI èmes Journées Nationales Microondes (JNM), mai 2019, Caen.
- Mariem Kanoun, **Bhanu Pratap Singh Jadav**, David Cordeau, Jean-Marie Paillot, Hassene Mnif, Mourad Loulou, “Conception et implémentation d’un déphaseur actif à 5.8 GHz, intégré en technologie BiCMOS SiGe:C 0.25 µm, pour la formation de faisceau”, XXI èmes Journées Nationales Microondes (JNM), mai 2019, Caen.
- Mariem Kanoun, **Bhanu Pratap Singh Jadav**, David Cordeau, Jean-Marie Paillot, Hassene Mnif, Mourad Loulou, “A 5.8 GHz Fully Integrated Active Phase Shifter For Energy Beamforming”, Journal Analog Integrated Circuits and Signal Processing (Status: Submitted).
- Mariem Kanoun, **Bhanu Pratap Singh Jadav**, David Cordeau, Jean-Marie Paillot, Hassene Mnif, Mourad Loulou, “A Fully Integrated 5.8 GHz BiCMOS SiGe: C tunable active phase shifter for Beamforming”, IEEE 30th International Conference on Microelectronics (ICM), 2018.

Résumé en français

Très communément appelée « 5G », cette 5éme génération du standard pour la téléphonie mobile et pour les systèmes de communications sans fil va commencer à être déployée dès 2020. L'arrivée de cette technologie « 5G » va considérablement accélérer la transformation de l'industrie des communications sans fil dans le monde entier. Selon un rapport d'Ericsson établi en juin 2019, la 5G devrait atteindre 45% du taux de population et 1,9 milliard d'abonnements d'ici 2024, ceci ferait de cette génération, la plus rapide jamais déployée à l'échelle mondiale.

Dans les années à venir, le partage des données et l'accès à l'information seront possibles n'importe quand et n'importe où pour n'importe qui et n'importe quoi. Ainsi, avec le développement de la norme LTE en combinaison avec de nouvelles technologies d'accès radio (RAT), il sera possible de fournir des débits de données très élevés (typiquement en Gbps), une latence très faible (< 1 ms), une très grande fiabilité (> 99,999 %), une efficacité énergétique et des densités de division extrêmes. La « 5G » permettra d'améliorer la connectivité sans fil des objets portables et favorisera l'évolution des voitures intelligentes, des maisons intelligentes, des processus industriels ainsi que l'automatisation et la diffusion multimédia à très haute vitesse. En bref, l'arrivée de la « 5G » va favoriser le développement rapide du concept de l'Internet des objets (IoT). Les comparaisons des principales capacités de l'IMT « International Mobile Telecommunication system » -2020 (5G) et de l'IMT évolué (4G) sont présentées sur la figure 1.

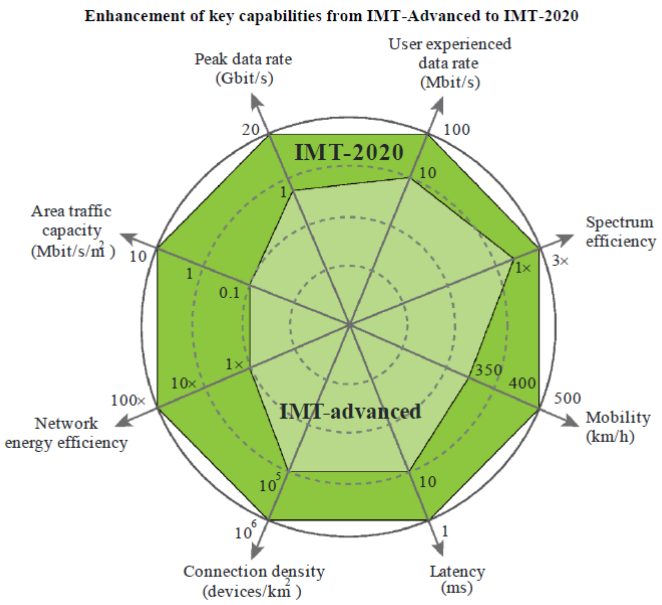


Figure 1: Amélioration des capacités clés des IMT évoluées à IMT 2020.

Afin de supporter l'augmentation de la capacité du trafic et d'assurer des largeurs de bande de transmission nécessaires pour supporter des débits de données très élevés, la technologie « 5G » impose une augmentation significative des bandes de fréquences utilisées pour les communications mobiles. Les axes de recherche dans la « 5G » visent une plage de fréquence comprise entre 300 MHz et 300 GHz.

La « 5G » a besoin d'un nombre important de nouvelles fréquences mobiles harmonisées. Dans ces conditions, du point de vue spectral, pour cette « 5G », il a été défini trois bandes de fréquences clés afin d'assurer une couverture étendue et prendre en considération les différents cas d'utilisation. Les trois bandes de fréquences prévues sont : la bande inférieure à 1 GHz, la bande 1-6 GHz et la bande supérieure à 6 GHz. Une fois la « 5G » déployée en 2020, le défi le plus critique sera de contrôler le trafic massif, en particulier en ondes millimétriques. La transmission des signaux avec un minimum de pertes et d'interférences sera l'un des critères les plus important. Ainsi, l'un des plus grands challenges en termes de recherche dans le domaine de la « 5G » est la formation de faisceau électromagnétique appelée (« beamforming ») et nécessaire à des fréquences d'ondes millimétriques, aussi bien pour les émetteurs que pour les récepteurs. Cette formation de faisceaux permet d'orienter et de contrôler le diagramme de rayonnement dans la direction de transmission souhaitée. Pour cela, un système de commande en phase est associé à un réseau d'antennes afin de gérer la phase du signal appliquée sur chaque antenne élémentaire du réseau. Différents types d'architectures de déphaseurs passifs et actifs existent dans la littérature. Ces déphaseurs peuvent être implémentés sur les voies OL, RF, IF ou en bande de base. Cette thèse se positionne clairement pour une implémentation des déphaseurs sur la voie OL car cette configuration présente, selon nous, plusieurs avantages, notamment en comparaison avec une architecture utilisant des déphaseurs sur la voie RF pour laquelle la qualité du signal est directement impactée par les dégradations dues aux déphaseurs, en termes de facteur de bruit, non-linéarité, ou encore de variation d'amplitudes.

Dans le cadre de ces travaux de thèse, la conception d'une structure originale de déphaseur actif implémenté sur la voie OL pour la formation de faisceau dans le domaine des ondes millimétrique, est détaillée. L'objectif principal est d'obtenir un déphasage linéaire de -90° à 90°. Nous montrerons que le plan de phase complet pourra être couvert en utilisant les sorties différentielles du déphaseur. Ce déphaseur est réalisé à base d'un Oscillateur Contrôlé en Tension (OCT) «triple-push» verrouillé par l'injection d'un signal à 8 GHz. Dans ces conditions, uniquement la composante harmonique de rang trois est conservée et la fréquence

du signal de sortie est donc triplée et égale à 24 GHz. Ce déphaseur actif a été totalement intégré et implémenté avec la technologie bas coût BiCMOS SiGe:C 0,25 µm de NXP Semiconductors.

Ce manuscrit comprend trois chapitres :

Le premier chapitre commence par introduire la vision future de la « 5G », ses applications, le spectre associé à la « 5G » et les différents défis qui doivent être relevés du point de vue recherche. Tout d'abord, le principe et les différents types de réseaux d'antennes ainsi que les principales caractéristiques des réseaux d'antennes linéaires et planaires sont présentés. Ensuite, les différentes techniques de synthèse de diagramme de rayonnement ont été décrites. Par ailleurs, un état de l'art des différentes architectures d'implémentation des déphasages, utilisées dans la littérature, a été dressé. L'accent a été mis, par la suite, sur la technique de synthèse en phase par réseaux d'oscillateurs verrouillés par injection, appelée en anglais « Injection-Locked Oscillator Array » (ILOA). Cette technique est basée sur l'utilisation d'un « d'oscillateur esclave » qui, une fois synchronisé à la fréquence d'injection de « l'oscillateur maître », génère une différence de phase entre le signal injecté (oscillateur maître) et le signal de sortie de « l'oscillateur esclave ». Cette différence de phase est contrôlée en modifiant la fréquence d'oscillation libre de « l'oscillateur esclave » via sa tension de contrôle, nommée ici *Vtune*. Ainsi, pour piloter un réseau antennaire, il suffit de placer un réseau d'oscillateurs esclaves chacun associé à une antenne (ou un groupe d'antennes), tous synchronisés par un signal d'injection, ici le signal d'OL. Le contrôle indépendant des fréquences d'oscillation libres (différents *Vtune*) permet un contrôle indépendant du déphasage entre chaque signal de sortie et le signal injecté. Le schéma de principe d'un réseau d'antennes à commande de phase, où chaque antenne élémentaire est associée au déphaseur actif, est illustré sur la figure 2.

Dans le deuxième chapitre, la conception d'une nouvelle architecture d'OCT différentiel «triple-push» à la fréquence de 24 GHz en technologie BiCMOS SiGe:C 0,25 µm de NXP Semiconductors, est présentée. Cet OCT « triple-push » est formé par l'association de trois oscillateurs identiques fonctionnant chacun à un tiers de la fréquence du signal de sortie désirée. Un circuit passif assure le couplage des trois OCTs et donc la synchronisation des signaux de sortie des trois OCTs. Sous certaines conditions, nous verrons plus tard qu'à la fréquence fondamentale, ces sorties sont déphasées de 120° les unes par rapport aux autres. Par conséquent, les composantes harmoniques de rang deux des trois signaux de sortie sont

déphasées de 240°, tandis que les composantes harmoniques de rang trois sont en phase. Dans ces conditions, en additionnant les signaux de sortie de ces trois OCTs, la composante fondamentale et l'harmonique de rang deux des trois sorties de l'OCT sont supprimées. Par contre, la composante de rang trois, c'est-à-dire la fréquence de sortie souhaitée, est recombinée en phase. Des précautions sont prises, car pour un oscillateur « triple-push », il existe deux modes de fonctionnement : un mode pair ou un mode impair. En mode impair, les signaux de sortie des trois oscillateurs sont déphasés de 120° à la fréquence fondamentale alors qu'en mode pair ces signaux sont en phase. Ainsi, afin d'obtenir la troisième harmonique du signal, il est impérativement nécessaire de travailler en mode impair. Cet aspect est traité dans la première partie de ce chapitre.

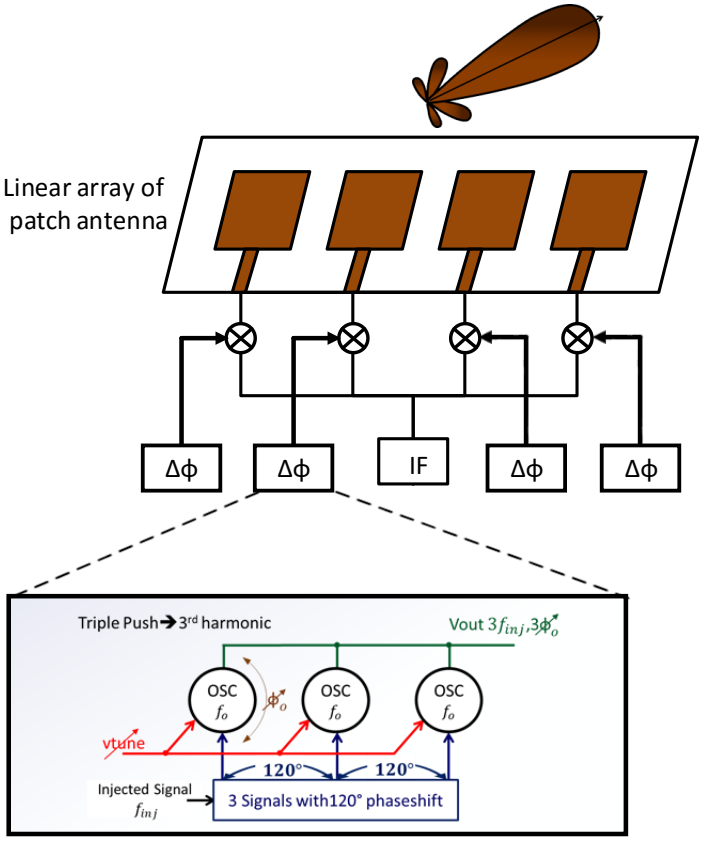


Figure 2: Architecture d'un réseau d'antennes à commande de phase pour la formation de faisceau sur la voie OL

Suite à cette discussion théorique, les conceptions et les implémentations d'un OCT de type LC et d'un OCT « triple-push » sont présentées. Ce dessin des masques a été réalisé avec le plus grand soin car c'est le point crucial pour l'obtention d'un excellent niveau de réjection de la fréquence fondamentale et de la deuxième harmonique. La figure 3 illustre le dessin des

masques de l'OCT « triple-push », intégré et implémenté à la fréquence de 24 GHz avec la technologie BiCMOS SiGe:C 0,25 µm de NXP Semiconductors.

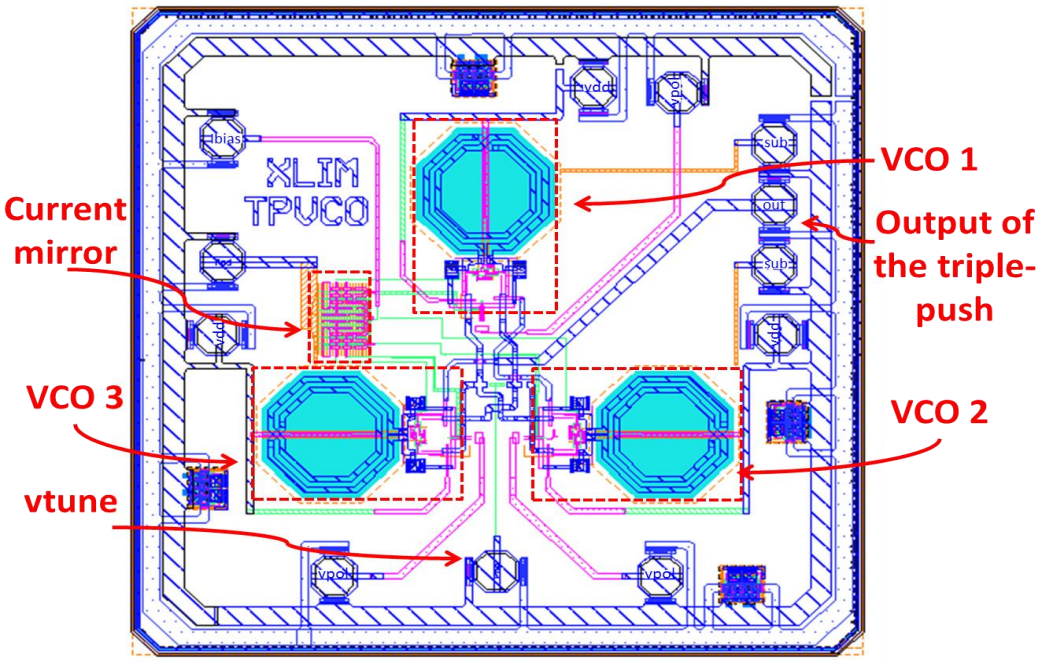


Figure 3: Dessin des masques de l'OCT « triple-push ».

Pour finir ce chapitre, les résultats de simulation « post-layout » du « triple-push » sont exposés. Ces résultats montrent que le circuit est capable de délivrer un signal de sortie stable de -5,76 dBm à la fréquence de 24 GHz. La consommation totale, y compris celle des étages dits « tampons » de sortie, est de 113,64 mW pour une tension d'alimentation de 3 V. Une réjection supérieure à 27,67 dB et à 19,65 dB est obtenue respectivement à la fréquence fondamentale et à la seconde harmonique.

En comparaison avec d'autres travaux récemment publiés dans la gamme de fréquences 20-30 GHz, l'OCT « triple-push » proposé offre le plus fort niveau de puissance de sortie sur 50 Ω à la troisième harmonique. De plus, le circuit conçu permet d'obtenir de meilleures performances en termes de réjection de la fréquence fondamentale et de la deuxième harmonique. Ce « triple-push » est conçu à 24 GHz puisqu'il sert de base à la conception d'un déphaseur actif 24 GHz pour la formation de faisceau. Ce déphaseur étant réalisé à partir d'injection sur un « triple-push », il est donc impératif de concevoir en amont un déphaseur 120°, que l'on peut nommer primaire, capable de distribuer le signal d'origine à 8 GHz sur chacun des OCT constituant le « triple-push ».

Dans le troisième chapitre, la conception et l'implémentation de l'ensemble du déphaseur actif à la fréquence de 24 GHz avec la technologie BiCMOS SiGe:C 0,25 µm de NXP Semiconductors, est détaillée. Rappelons que cet ensemble est constitué de l'OCT « triple-push » et de son circuit d'injection. Le rôle du triple-push est de tripler la phase instantanée afin d'obtenir un déphasage linéaire sur une plage de 180°. Cette injection nécessite d'être appliquée sur chacun des trois OCT du « triple-push » et elle est réalisée à l'aide d'un déphaseur primaire de 120°.

La première partie de ce chapitre a été consacrée à l'étude du phénomène de verrouillage par injection dans un oscillateur « triple-push ». Dans la deuxième partie, la conception d'une architecture originale d'un déphaseur primaire différentiel 120° accordable à 8 GHz est présentée. Le signal appliqué à l'entrée de ce déphaseur est un signal simple accès, par contre, les trois sorties 120° sont différentielles car elles devront par la suite être injectées sur les trois oscillateurs formant le « triple-push ». Ce circuit est composé d'éléments intégrés passifs de type *RLC* et de composants actifs qui assurent les fonctions d'additionneurs différentiels et d'étages «tampons» de sortie. Le dessin des masques de ce déphaseur RF différentiel, réalisé sous l'environnement CADENCE® avec la technologie BiCMOS SiGe:C 0,25 µm de NXP Semiconductors, est illustré sur la figure 4.

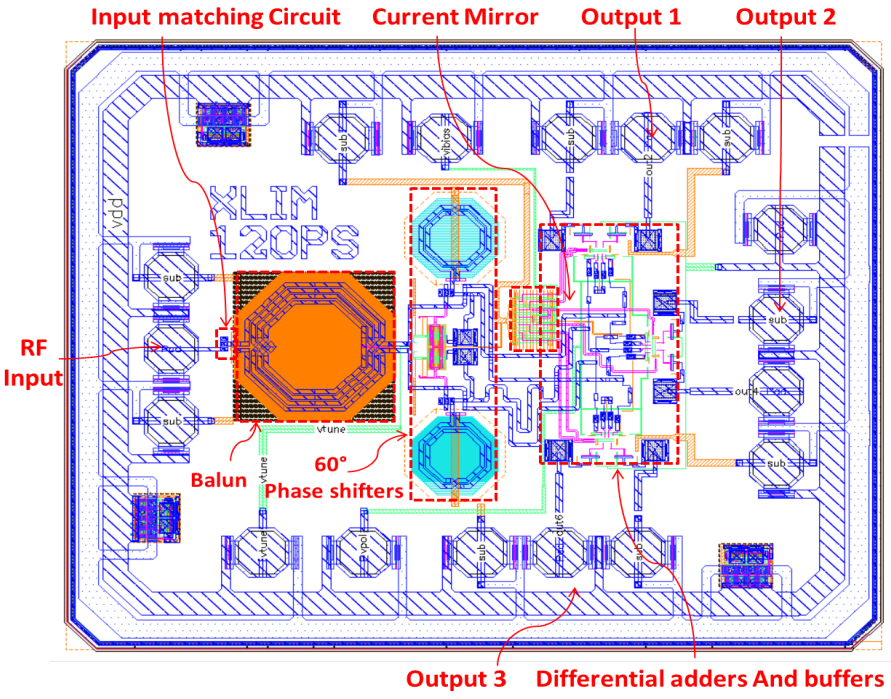


Figure 4: Dessin des masques du déphaseur primaire 120°

Les résultats de simulations « post-layout » montrent un fonctionnement contrôlable sur une bande de fréquences de 10 % autour de 8 GHz assurant ainsi la fonction d'ajustement en fréquence. De plus, l'erreur de phase, autour de 120°, est inférieure à 3° lorsque la fréquence varie de 7,7 GHz à 8,5 GHz. Les variations d'amplitude dans cette bande de fréquences sont inférieures à 2,5 %. Le résumé des différentes performances du déphaseur RF 120° est présenté dans le tableau 3.1.

Tableau 3.1: Bilan des performances du déphaseur différentiel 120° accordable à 8 GHz

Paramètres	**Valeur**
Tension d'alimentation	3 V
Fréquence centrale	8 GHz
Consommation DC (buffers)	78 mW
Consommation DC (globale)	130 mW
Plage de fréquence	(7,7 GHz – 8,5 GHz)
Taille de la puce	0,5x0,69 mm^2
Erreur de phase	Moins de 3°.
Erreur d'amplitude	Moins de 2,5 %

Suite à cette description, la conception et l'implémentation de l'architecture globale du déphaseur actif à la fréquence de 24 GHz sont détaillées. Le schéma de principe de ce circuit déphaseur est présenté sur la figure 5. Ce circuit combine le déphaseur 120° et le circuit OCT «triple-push». A l'entrée, un réseau d'adaptation a été conçu pour adapter l'entrée sur 50 Ω et assurer ainsi un transfert maximum de puissance de la source d'injection vers le déphaseur. Ce circuit d'adaptation est réalisé grâce à un pont capacitif. Ensuite, un « balun » soit un transformateur équilibré 0-180° est utilisé pour générer un signal différentiel à partir d'un signal « single-ended ». La topologie de ce transformateur est fournie par la bibliothèque du design kit de NXP Semiconductors. Ce signal différentiel est ensuite injecté au circuit déphaseur 120° associé à l'OCT « triple-push ». Ainsi, l'OCT « triple-push » verrouillé par injection génère un déphasage fin et linéaire entre le signal injecté et le signal de sortie de l'OCT dans la plage de ±30°. Ceci assure, sur l'harmonique de rang trois, un contrôle continu et linéaire du déphasage dans la plage ±90° à la sortie du circuit global. Des amplificateurs différentiels suivis d'étages « tampons » sont utilisés à la sortie de chaque OCT. En effet, l'étage « tampon » à haute impédance d'entrée permet d'isoler l'OCT de la charge en sortie du

circuit. Ces étages « tampons » sont conçus de telle sorte que le signal de sortie du « triple-push » soit bien adapté sur 50 Ω.

Les résultats de simulations post-layout ont montré qu'avec une puissance injectée de 5 dBm, on obtient un déphasage linéaire entre -90° et + 90° (figure 6). Ce déphaseur actif est destiné à être associé à une antenne élémentaire afin de réaliser un réseau d'antennes à commande de phase pouvant être utilisé pour la transmission de données, par exemple en technologie « 5G ». Les conditions statiques de fonctionnement du circuit déphaseur global ainsi que ses performances obtenues en simulation « post-layout » sont résumées dans les tableaux 2 et 3.

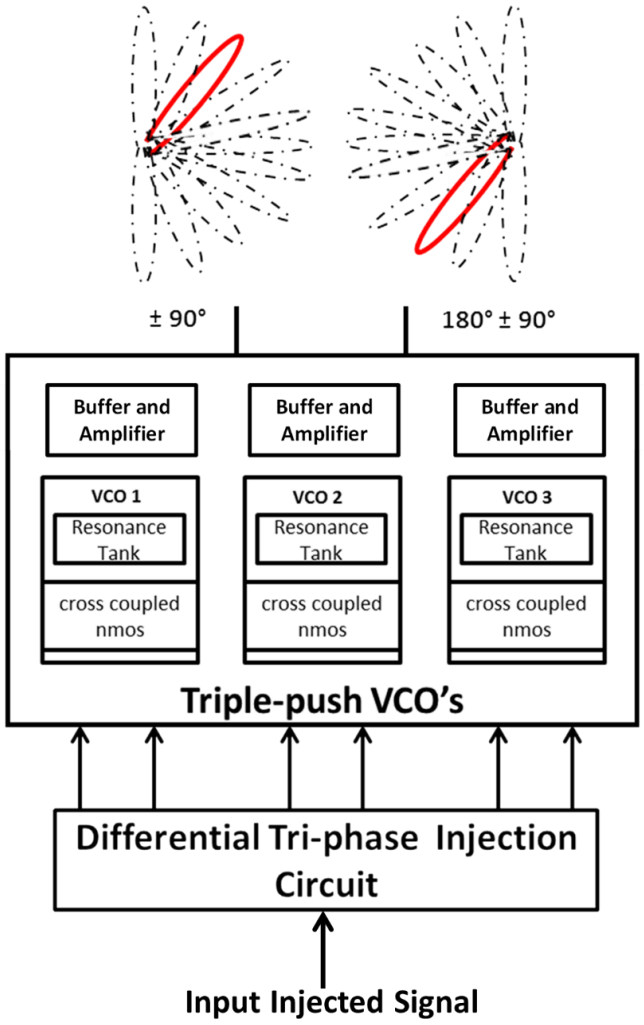


Figure 5 : Schéma bloc de l'OCT « triple-push » verrouillé par injection.

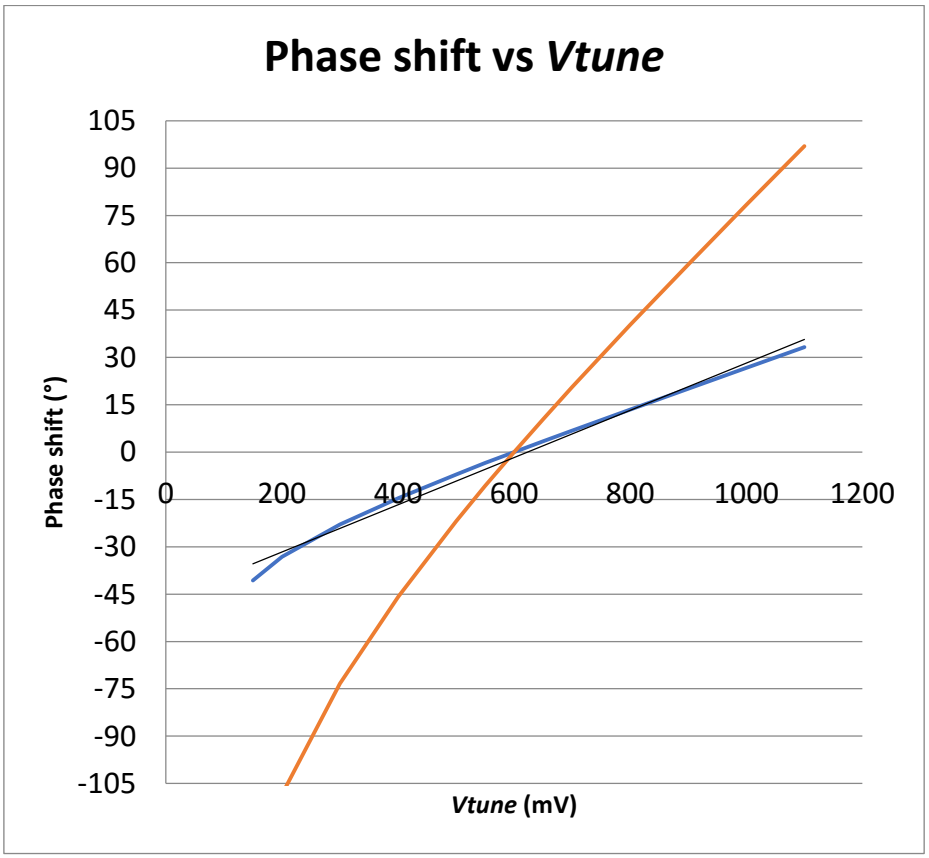


Figure 6: Simulation « post layout » du déphasage obtenu entre le signal d'injection et la sortie d'un OCT en fonction de « *Vtune* » (courbe bleu) et du déphasage obtenu à la sortie de l'OCT « triple-push » (Courbe orange).

Tableau 2: Paramètres statiques de l'ensemble du circuit

Paramètres	Values
Tension d'alimentation [V]	**3**
Courant de référence [mA]	**2,5**
Consommation totale en courant [mA]	**52,91**
Puissance consommée par les buffers [mW].	**39,12**
Puissance totale consommée [mW]	**158,73**

Tableau 3: Résumé des performances du déphaseur actif (simulations post-layout)

	Post-layout
Fréquence d'oscillation libre (GHz)	**20,79 – 24,81**
Fréquence d'injection (GHz)	**8**
Puissance d'injection (dBm)	**5**
Déphasage (°)	**180°**
Puissance de sortie moyenne sur 50 Ω (dBm)	**≈ -3,17**

References

[1] Rysavy Research, “LTE to 5G: Cellular and Broadband Innovation”, White paper of 5G Americas, August 2017 (http://www.rysavy.com).

[2] Afif Osseiran, Jose F. Monserrat and Patrick Marsch, “5G Mobile and Wireless Communications Technology”, Cambridge University Press, 2016.

[3] Ericsson AB, “5G systems - Enabling the transformation of industry and society,” Tech. Rep., Jan. 2017. (https://www.ericsson.com/en/white-papers/5g-systems--enabling-the-transformation-of-industry-and-society)

[4] ITU-R WP5D, “IMT vision–framework and overall objectives of the future development of IMT for 2020 and beyond,” *Int. Telecommunication Union*, Geneva, Switzerland, ITU Recommendation M.2083, 2015.

[5] Ericsson, “Broadband and media everywhere - 5G is here”, 23-May-2016. (https://www.ericsson.com/en/5g/use-cases/broadband-and-media-everywhere).

[6] IEEE 5G, “IEEE 5G AND BEYOND TECHNOLOGY ROADMAP WHITE PAPER”, October 2017 (https://futurenetworks.ieee.org/images/files/pdf/ieee-5g-roadmap-white-paper.pdf).

[7] P. Desai, K. Garcia, and O. Ahmad, “How antenna-on-package design simplifies mmWave sensing in buildings and factories”, *Texas Instruments*, 2019.

[8] Devaki Chandramouli, Rainer Liebhart, Juho Pirskanen, “Wireless Spectrum for 5G," in *5G for the Connected World*”, Wiley, 2019, pp.35-50.

[9] GSMA, “5G Spectrum GSMA Public Policy Position”, July 2019. (https://www.gsma.com/spectrum/wp-content/uploads/2019/09/5G-Spectrum-Positions.pdf)

[10] S. Kumar, G. Gupta and K. R. Singh, "5G: Revolution of future communication technology," *2015 International Conference on Green Computing and Internet of Things (ICGCIoT)*, Noida, 2015, pp. 143-147.

[11] A. Gohil, H. Modi and S. K. Patel, “5G technology of mobile communication: A survey”, 2013 International Conference on Intelligent Systems and Signal Processing (ISSP), Gujarat, 2013, pp. 288-292.

[12] D. Parker and D. Zimmermann, “Phased arrays-Part I: Theory and architectures”, *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, No. 3, pp. 678-687, March 2002.

[13] C. A. Balanis, “Arrays and Smart Antennas”, in *Modern Antenna Handbook*, Wiley, 2008.

[14] G. Clementi, “Conception et caractérisation fréquentielle et temporelle d’antennes réseaux planaires à très large bande passante ”, Thèse de Doctorat, Université de Nice - Sophia Antipolis, 2011.

[15] C. A. Balanis, “*Antenna Theory Analysis And Design, third edition*”, John wiley & Sons. 2005.

[16] N.Y. Tohmé, “Etudes comportementales et réalisation d’un réseau d’oscillateurs couplés et de déphaseurs actifs appliqués à la commande d’un réseau d’antennes linéaire”, Thèse de Doctorat de l’Université de Poitiers, décembre 2009.

[17] N. Fadlallah, “Contribution à l’optimisation de la synthèse du lobe de rayonnement pour une antenne intelligente. Application à la conception de réseaux à déphasage”, thèse de Doctorat de l’Université de Limoges, Mai 2005.

[18] M. Bonnedal, I. Karlsson and K. Van't Klooster, “A dual beam slotted waveguide array antenna for SAR applications”, *1991 Seventh International Conference on Antennas and Propagation, ICAP 91 (IEE)*, York, 1991, pp. 559-562 vol.2.

[19] Li, Bing & Chen, Maggie & Jiang, Nianhua & Fu, Zhenhai & Tang, Suning & Chen, Ray. (2000), “Photonic phased-array antenna system based on detector-switched optical Blass matrix true-time delay steering and heterodyne RF generation”, Proceedings of SPIE - The International Society for Optical Engineering. 4087. 10.1117/12.406340.

[20] F. Hutu, D. Cordeau, and J.-M. Paillot, “2.4 GHz antenna array using vector modulator-based active phase shifters for beamforming”, *IET Microwave Antennas and Propagation*, vol. 5, no. 2, p. 245, 2011.

[21] R. A. York, “Nonlinear analysis of phase relationships in quasi-optical oscillator arrays,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 41, no. 10, pp. 1799-1809, Oct. 1993.

[22] L. Wu, A. Li and H. C. Luong, “A 4-Path 42.8-to-49.5 GHz LO Generation With Automatic Phase Tuning for 60 GHz Phased-Array Receivers,” in *IEEE Journal of Solid-State Circuits*, vol. 48, no. 10, pp. 2309-2322, Oct. 2013.

[23] F. E. Fakoukakis, S. G. Diamantis, A. P. Orfanides, and G. A. Kyriacou, “Development of an Adaptive and a Switched Beam Smart Antenna System for

Wireless Communications", *Journal of Electromagnetic Waves and Applications*, vol. 20, no. 3, pp. 399–408, Jan. 2006.

[24] F. Ellinger and W. Bachtold, "Novel principle for vector modulator-based phase shifters operating with only one control voltage", *IEEE Journal of Solid-State Circuits*, vol. 37, no. 10, pp. 1256-1259, Oct. 2002.

[25] J. Paramesh, R. Bishop, K. Soumyanath and D. J. Allstot, "A four-antenna receiver in 90-nm CMOS for beamforming and spatial diversity," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2515-2524, Dec. 2005.

[26] S. Gueorguiev, S. Lindfors and T. Larsen, "A 5.2 GHz CMOS I/Q Modulator With Integrated Phase Shifter for Beamforming," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 9, pp. 1953-1962, Sept. 2007.

[27] K. Koh and G. M. Rebeiz, "0.13-µm CMOS Phase Shifters for X-, Ku-, and K-Band Phased Arrays," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 11, pp. 2535-2546, Nov. 2007.

[28] Y. Yao, Z. Li, G. Cheng and L. Luo, "A 6-bit active phase shifter for Ku-band phased arrays," *2017 9th International Conference on Wireless Communications and Signal Processing (WCSP)*, Nanjing, 2017, pp. 1-5.

[29] B. Cetindogan, E. Ozeren, B. Ustundag, M. Kaynak and Y. Gurbuz, "A 6 Bit Vector-Sum Phase Shifter With a Decoder Based Control Circuit for X-Band Phased-Arrays," *IEEE Microwave and Wireless Components Letters*, vol. 26, no. 1, pp. 64-66, Jan. 2016.

[30] J. Hu, W. Li, L. He, S. Liu, Y. Xu and J. Gong, "A 65nm CMOS 6–18 GHz full 360° 6-bit phase shifter," *2018 IEEE 18th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, Anaheim, CA, 2018, pp. 51-53.

[31] B. Van Der Pol, "The Nonlinear Theory of Electric Oscillations," *Proceedings of the Institute of Radio Engineers*, vol. 22, no. 9, pp. 1051-1086, Sept. 1934.

[32] P. Liao and R. A. York, "A new phase-shifterless beam-scanning technique using arrays of coupled oscillators," *IEEE Transactions on Microwave Theory and Techniques*, vol. 41, no. 10, pp. 1810-1815, Oct. 1993.

[33] Dorra Mellouli, David Cordeau, Hasséne Mnif, Jean-Marie Paillot and Mourad Loulou, "A Low Phase Noise Fully Monolithic 6 GHz Differential Coupled NMOS LC-VCO", *Frequenz - Journal of RF-Engineering and Telecommunications*, 2016, 70 (1-2), pp.33-38.

[34] D. Cordeau D. Mellouli J-M. Paillot H. Mnif and M. Loulou "A Fully Monolithic 5.8 GHz Low Phase Noise Coupled VCO Network For Phased-Array Systems"

Analog Integrated Circuits and Signal Processing-Springer vol. 82 no. 1 pp. 335-340 2015.

[35] R. A. York, P. Liao, and J. J. Lynch, "Oscillator array dynamics with broadband N-port coupling networks", *IEEE Transactions on Microwave Theory and Techniques*, vol. 42, no. 11, pp. 2040–2045, Nov. 1994.

[36] J. J. Lynch and R. A. York, "Synchronization of Oscillators Coupled Through Narrow-Band Networks", *IEEE Trans.Microw. Theory Tech*, 49 (2) (2001), 237–249.

[37] R. Adler, "A Study of Locking Phenomena in Oscillators," *Proceedings of the IRE*, vol. 34, no. 6, pp. 351-357, June 1946.

[38] L. J. Paciorek, "Injection locking of oscillators," *Proceedings of the IEEE*, vol. 53, no. 11, pp. 1723-1727, Nov. 1965.

[39] N. Ebrahimi, P. Wu, M. Bagheri and J. F. Buckwalter, "A 71–86-GHz Phased Array Transceiver Using Wideband Injection-Locked Oscillator Phase Shifters," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 2, pp. 346-361, Feb. 2017.

[40] B. Razavi, "A study of injection locking and pulling in oscillators," in *IEEE Journal of Solid-State Circuits*, vol. 39, no. 9, pp. 1415-1424, Sept. 2004.

[41] Y. Lo and J. Kiang, "Comparison of Injection-Locked and Coupled Oscillator Arrays for Beamforming," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 4, pp. 1353-1360, April 2015.

[42] S. Bellofiore *et al*., "Smart antenna system analysis, integration and performance for mobile ad-hoc networks (MANETs)," *IEEE Transactions on Antennas and Propagation*, vol. 50, no. 5, pp. 571-581, May 2002.

[43] J. Mondal S. K. Ray M. S. Alam M. M. Rahman "Design smart antenna by microstrip patch antenna array" International Journal of Engineering and Technology vol. 3 no. 6 pp. 675 2011.

[44] A. Oueslati, "Nouveau concept simplifié d'antennes reconfigurables utilisant les couplages inter-éléments : Mise en œuvre d'un réseau hybride ", Thèse de Doctorat, Université de Limoges, 2015.

[45] Y. L. Tang and H. Wang, "Triple-push oscillator approach: Theory and experiments", *IEEE Journal of Solid-State Circuits*, vol. 36, no. 10, pp. 1472–1479, 2001.

[46] F. Ramirez, J. L. Garcia H, T. Fernandez, and A. Suarez, "Nonlinear simulation techniques for the optimized design of push-push oscillators", *IEEE MTT-S*

International Microwave Symposium Digest, 2003, 2003, vol. 3, pp. 2157–2160 vol.3.

[47] Yu-Long Tang and Huei Wang, "A novel triple-push oscillator approach", *2000 IEEE MTT-S International Microwave Symposium Digest (Cat. No.00CH37017)*, 2000, vol. 2, pp. 1201–1204 vol.2.

[48] Jonghoon Choi and A. Mortazawi, "Design of push-push and triple-push oscillators for reducing 1/f noise upconversion", *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 11, pp. 3407–3414, Nov. 2005.

[49] Y. L. Tang and H. Wang, "A 24.6-GHz MMIC HBT Triple-Push Oscillator", *2001 31st European Microwave Conference*, 2001, pp. 1–4.

[50] Po-Yo Chen, Yu-Lung Tang, Huei Wang, Yu-Chi Wang, Pane-Chane Chao, and Chung-Hsu Chen, "A 39-46 GHz MMIC HBT triple-push VCO using cascode configuration", in *Proceedings. IEEE Asia-Pacific Conference on ASIC*, 2002, pp. 61–64.

[51] A. Collado and A. Georgiadis, "Nonlinear Mode Analysis and Optimization of a Triple-Push Oscillator", *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 8, pp. 545–547, Aug. 2008.

[52] B. Catli and M. M. Hella, "A 30-GHz triple-push oscillator on silicon for mm-wave applications", in *2009 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2009, pp. 2037–2040.

[53] B. Catli and M. M. Hella, "Triple-Push Operation for Combined Oscillation/Divison Functionality in Millimeter-Wave Frequency Synthesizers", *IEEE Journal of Solid-State Circuits*, vol. 45, no. 8, pp. 1575–1589, Aug. 2010.

[54] Chao-Chieh Li, Chung-Chun Chen, Bo-Jr Huang, Pin-Cheng Huang, Kun-You Lin, and Huei Wang, "A novel ring-based triple-push 0.2-to-34 GHz VCO in 0.13μm CMOS technology", *2008 IEEE MTT-S International Microwave Symposium Digest*, 2008, pp. 347–350.

[55] Chung-Chun Chen, Chao-Chieh Li, Bo-Jr Huang, Kun-You Lin, Hen-Wai Tsao, and Huei Wang, "Ring-Based Triple-Push VCOs With Wide Continuous Tuning Ranges", *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 9, pp. 2173–2183, Sep. 2009.

[56] Y. Lin, T.-H. Lin, and H.-Y. Chang, "A 42–71 GHz 90 nm CMOS injection-locked voltage-controlled oscillator using bulk injection technique", *2015 10th European Microwave Integrated Circuits Conference (EuMIC)*, 2015, pp. 108–111.

[57] D. Cordeau, “ Etude comportementale et conception d’oscillateurs intégrés polyphases accordables en fréquence en technologies Si et SiGe pour les radiocommunications ”, Thèse de Doctorat, Université de Poitiers, 2004.

[58] J. Mira, “Conception d’oscillateurs contrôlés en tension dans la gamme 2 GHz - 10 GHz, intégrés sur silicium et analyse des mécanismes à l’origine du bruit de phase”, Thèse de Doctorat, Bordeaux 1, 2004.

[59] H. L. Kao *et al.*, “A Ka-band triple push coupled pair VCO using 0.18-μm CMOS technology”, *2011 Eighth International Conference on Wireless and Optical Communications Networks*, 2011, pp. 1–4.

[60] M. Series, “IMT Vision – Framework and overall objectives of the future development of IMT for 2020 and beyond”, *ITU-R*, Sep. 2015.

[61] A. Natarajan, A. Komijani, X. Guan, A. Babakhani, and A. Hajimiri, “A 77-GHz Phased-Array Transceiver With On-Chip Antennas in Silicon: Transmitter and Local LO-Path Phase Shifting”, *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2807–2819, Dec. 2006.

[62] S. Gueorguiev, S. Lindfors, and T. Larsen, “A 5.2 GHz CMOS I/Q Modulator With Integrated Phase Shifter for Beamforming”, *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1953–1962, Sep. 2007.

[63] W. Mielke, “An Active Phase Shifter for Phased Array Applications Providing Amplitude and Phase Control”, *1985 15th European Microwave Conference*, Paris, Frane, 1985, pp. 572–577.

[64] A. Bevilacqua and P. Andreani, “A 2.7-6.1 GHz CMOS local oscillator based on frequency multiplication by 3/2”, *2011 NORCHIP*, Lund, Sweden, 2011, pp. 1–4.

[65] T. Chi, J. Luo, S. Hu, and H. Wang, “A multi-phase sub-harmonic injection locking technique for bandwidth extension in silicon-based THz signal generation”, *Proceedings of the IEEE 2014 Custom Integrated Circuits Conference*, 2014, pp. 1–4.

[66] A. Natarajan *et al.*, ‘A Fully-Integrated 16-Element Phased-Array Receiver in SiGe BiCMOS for 60-GHz Communications’, *IEEE Journal of Solid-State Circuits*, vol. 46, no. 5, pp. 1059–1075, May 2011.

[67] M. Fakharzadeh, M.-R. Nezhad-Ahmadi, B. Biglarbegian, J. Ahmadi-Shokouh, and S. Safavi-Naeini, “CMOS Phased Array Transceiver Technology for 60 GHz Wireless Applications”, *IEEE Transactions on Antennas and Propagation*, vol. 58, no. 4, pp. 1093–1104, Apr. 2010.

[68] S. Emami *et al.*, “A 60GHz CMOS phased-array transceiver pair for multi-Gb/s wireless communications”, *2011 IEEE International Solid-State Circuits Conference*, 2011, pp. 164–166.

[69] M. Egot, B. Martineau, O. Richard, N. Rolland, A. Cathelin, and A. Kaiser, “A 20–23 GHz Coupled Oscillators Array in 65nm CMOS for HDR 60GHz beamforming applications”, 2011 Proceedings of the ESSCIRC (ESSCIRC), 2011, pp. 463–466.

[70] M. L. Carneiro, M. Le Roy, A. Pérennec, R. Lababidi, P. Ferrari, and V. Puyal, “Compact Analog All-Pass Phase-Shifter in 65-nm CMOS for 24/28 GHz on-Chip- and in-Package Phased-Array Antenna”, 2019 IEEE 23rd Workshop on Signal and Power Integrity (SPI), 2019, pp. 1–4.

[71] T. V. Zlotnikov, O. Degani, I. Brouk, and Y. Nemirovsky, “A 45nm CMOS miniature phase shifter with constant amplitude response”, Microelectronics Journal, vol. 42, no. 10, pp. 1143–1150, Oct. 2011.

Abstract

The work presented in this thesis consists in designing an original integrated circuit in the millimetre-wave domain. Associated to an antenna array, this circuit performs beamforming, i.e. it allows the orientation and control of the radiation pattern in the desired direction. In millimetre waves, the ability to steer the beam allows to compensate for the losses due to the increase in frequency. This new circuit ensures a tunable RF phase shift between the input and the output. It is based on an original Injection Locked triple-push Voltage Controlled Oscillator (VCO) at 8 GHz. In these conditions, the frequency of the output signal is at 24 GHz. The objective of this dissertation is to design this fully integrated active RF phase shifter implemented in the QUBiC4X 0.25 µm SiGe:C BiCMOS process of NXP semiconductors. In the first part of this work, the design of this new architecture of a differential «triple-push» VCO at 24 GHz is presented. This «triple-push» VCO consists of three differential VCOs coupled through varactor diodes. The post layout simulation results validate the design methodology with an excellent level of fundamental and second harmonic rejections. Then, a novel architecture of an 8 GHz differential 120° tuneable phase shifter is presented. This phase shifter allows to obtain, from a single-ended input signal, three 120° out of phase signals with the same amplitude. The circuit was implemented on the same process and various post-layout simulation results were reported. Finally, the global circuit is designed and implemented, combining the 120° phase shifter and the «triple-push» VCO. The latter is injection locked by the 120° phase shifter. The post-layout simulations results validate the proposed original approach of the designed circuit and show a linear variation of the phase shift throughout the entire phase plane. This active phase shifter is intended to be associated to an elementary antenna to subsequently constitute a complete antenna array that can be used for data transmission, for example in 5G technology.

Keywords: VCO, «triple-push», millimetre wave frequency, beamforming, active phase shifter, SiGe BiCMOS.

Résumé

Le travail présenté dans cette thèse consiste à développer un circuit intégré original dans le domaine des ondes millimétriques. Associé à un réseau d'antennes, ce dispositif permettra de réaliser de la formation de faisceaux (« beamforming »), c'est-à-dire qu'il permettra d'orienter et de contrôler le diagramme de rayonnement dans la direction désirée. Pour les ondes millimétriques, cette capacité à orienter le faisceau compense par son gain, les pertes dues à la montée en fréquence. Ce nouveau circuit assure un déphasage RF contrôlable entre l'entrée et la sortie. Il est réalisé à base d'un Oscillateur Contrôlé en Tension (OCT) «triple-push» verrouillé par l'injection d'un signal à 8 GHz. Dans ces conditions, la fréquence du signal de sortie est de 24 GHz. L'objectif de cette thèse a été de concevoir ce déphaseur RF actif, totalement intégré et implémenté avec la technologie BiCMOS SiGe:C 0,25 µm de NXP Semiconductors. Dans la première partie de ce travail, la conception de cette nouvelle architecture d'OCT différentiel «triple-push» à la fréquence de 24 GHz est présentée. Nous verrons que l'OCT «triple-push» est constitué de trois OCT différentiels couplés via des diodes varactors. Les résultats de simulations post-layout valident la méthodologie de conception avec un excellent niveau de réjection de la fréquence fondamentale et de la deuxième harmonique. Par la suite, une nouvelle architecture d'un déphaseur différentiel 120° accordable à la fréquence de 8 GHz est présentée. Ce déphaseur permet d'obtenir à partir d'un seul signal d'entrée, trois signaux de même amplitude et déphasés de 120° entre eux. Le circuit a été implémenté et les différents résultats de simulations post-layout obtenus ont été exposés. Enfin, le circuit global a été conçu et implémenté, en combinant le circuit déphaseur 120° et le circuit OCT «triple-push». Ce dernier est verrouillé par injection par le déphaseur 120°. Les résultats de simulations post-layout valident l'approche originale du système conçu et montrent une variation linéaire du déphasage dans tout le plan de phase. Ce déphaseur actif est destiné à être associé à une antenne élémentaire pour ensuite constituer un réseau antennaire complet qui pourra être utilisé pour la transmission de données, par exemple en technologie 5G.

Mots-clés: OCT, «triple-push», onde millimétrique, formation de faisceau, déphaseur actif, BiCMOS SiGe.