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Co-design Methodology of 60 GHz Filter-LNA

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"Le bonheur se résume finalement à de toutes petites choses."
Marc Lévy, L'Horizon à l'envers, 2016

To my family,

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4G – Fourth Generation Mobile Radio.
5G – Fifth Generation Mobile Radio.

AMPS – Advanced Mobile Phone System.

BDMA – Beam Division Multiple Access.

CAD – Computer-Aided Design.
CB – Common Base.
CCI – Co-Channel Interference.
CDMA – Code-Division Multiple Access.
CDMA2000 – also known as C2K or IMT (*International Mobile Telecommunications*) Multi-Carrier.
CE – Common Emitter.
CL – Conversion-Loss.

DRC – Design Rule Check.

EDGE – Enhanced Data Rates for GSM Evolution.
EHF – Extremely High Frequency.
EM – Electromagnetic.
EVDO – Evolution-Data Optimized.

F – Noise Factor.
FBMC – Filter Bank Multi-Carrier.
FDMA – Frequency-Division Multiple Access.
FSPL – Free-Space Path Loss.

GPRS – General Packet Radio Service.
GSG – Ground-Signal-Ground.
GSM – Global System for Mobile Communications.

HBT – Heterojunction Bipolar Transistor.
HDTV – High-Definition Television.
HSPDA – High Speed Downlink Packet Access.
HSUPA – High Speed Uplink Packet Access.

IC – Integrated Circuit.
IEEE – Institute of Electrical and Electronics Engineers.
IF – Intermediate Frequency.
IL – Insertion Loss.
ISM – Industrial, Scientific and Medical.
ITU-R – International Telecommunications Union Radiocommunication Sector.

LDPC – Low-density Parity Check Code.
LNA – Low-Noise Amplifier.
LO – Local Oscillator.

LTE – Long-Term Evolution.
LTE-A – LTE Advanced.
LVS – Layout Versus Schematic.

MIM – Metal-Insulator-Metal.
MIMO – Multiple Input, Multiple Output.
mm-wave – Millimeter-Wave.
MMIC – Monolithic Microwave Integrated Circuit.

NF – Noise Figure.

OFDMA – Orthogonal frequency-division multiple access.
OSI – Open Systems Interconnection.

PDK – Process Design Kit.

RF – Radio Frequency.
RFIC – Radio-Frequency Integrated Circuits.

SC-FDMA – Single-Carrier FDMA.
SNR – Signal-to-Noise Power Ratio.
SOFDMA – Scalable OFDMA.

TDMA – Time-Division Multiple Access.
TL – Transmission Line.

Ultra-HD – Ultra-High-Definition Television.
UMTS – Universal Mobile Telecommunications System.
UWB – Ultra-Wild Band.

VCO – Voltage Controlled Oscillator.
VR – Virtual Reality.

WCDMA – Wideband Code Division Multiple Access.
WIMAX – Worldwide Interoperability for Microwave Access.
WPAN – Wireless Personal Area Network.

Chapter 1

60GHz (ISM) and 5G bands

THE Fifth Generation Mobile Radio (5G) promises faster data transfer ratio and more reliable network services. These promises implementation can be a great technological advance, except for the fact that during the early days of Fourth Generation Mobile Radio (4G) these commitments were already a thing. Back then it was intended that Ultra-Wild Band (UWB) high data transfer rate would be possible using the existing technology at the time, and quickly a bunch of industry consortium and small companies were created with intention of exploring UWB new technologies. At the time the idea of high bit-rate large data transport was shaped with either too slow and power hungry systems (Bluetooth), or designed with ancient technology optimization for long distances (WiFi).

Today, with the 5G hype, portable devices as computers are already a thing and a new wave of multimedia services (like streaming audio/video, and cloud document storage, for example) has arrived. These user end technologies are already mature for use, and hence the necessity of devices and network capable of transmitting a large amount of data and as fast as possible.

In this context of high data transportation is safe to say that the utilization of mm-waves in wireless networks are the next step for the radio technology due long term previsions of telecommunication boundaries [1], [2] and [3], such as: Hyper-populated lower frequency spectrum, possibility of high data rates usage, lower Co-Channel Interference (CCI) due perimeter limitation of transmitted signal in, minimization process of microelectronic circuits, cable-less communication, and more. Of course, these promising technologies inspire both

researchers and industry for new products and applications, despite the fact they have not always the same motivation

To meet these exigences 5G network promises to deliver high efficient and reliable network in terms of services and velocity of data transfers, using a diverse combination of small/large cells protocols. Differently of what was before proposed (in 4G), now the 5G proposition involves new network structure, implicating the use of different techniques and technologies in OSI model media layers (physical, data link, and network layers), such as massive MIMO, different frequency bands and small cells.

The acronym mm-waves is used because its spectrum surrounds the electromagnetic waves with wavelength range between 1 mm to 100 mm – so with the frequency range between 30 to 300 GHz. In the table of the International Telecommunications Union Radiocommunication Sector (ITU-R) radio bands the used nomenclature is Extremely High Frequency (EHF) band, while according to IEEE standard this range comprehend the bands K_a, V, W, and G[1].

There already exists many application with mm-wave usage in, for example, weapon defense systems, security imaging and even in medicine. Also, in telecommunications, the use of 60 GHz band for high-speed microwave data links for point-to-point communication is already licensed in many countries. Additionally 60 GHz freqency band are long used in temporary short-range data links where terrain is flat enough. Furthermore 5G Mobile Networks defines the following requirements that should be fulfilled [4], [5], [6] and [7]:

1. Data rates of tens of megabits per second for tens of thousands of users;
2. Data rates of 100 megabits per second for metropolitan areas;
3. 1 Gbps simultaneously to many workers on the same office floor;
4. Several hundreds of thousands of simultaneous connections for wireless sensors;
5. Spectral efficiency significantly enhanced compared to 4G;
6. Coverage improved;
7. Signaling efficiency enhanced.

[1]The G band is also named *mm* band, generating confusion. In this work the term *mm* is used only as mm-waves with frequency range between 30 to 300 GHz.

The recommendations on commercial spectrum for 5G in Europe to meet commercial deployments in 2020 and to achieve full capabilities by 2025 it to license the 700 MHz, 3.6 GHz and 26 GHz no later than end 2019 [8]. The 26 GHz band (24.25 GHz to 27.5 GHz) is necessary for the very high data rates and capacity foresee by 5G.

Also, lot of work is being performed to benefit the Industrial, Scientific and Medical (ISM) band at 60 GHz which can achieve high data transmission and should be considered within ITU-R and may provide extreme bandwidths for indoor and short-range in 5G applications. Although the band is inappropriate for long distance communication due to atmospheric attenuation, that is of no significance in a short range. Furthermore, federal agencies worldwide have already standardized on the use of 60 GHz spectrum allocation, and several national regulatory agencies have agreed to use unlicensed spectrum at 60 GHz for Wireless Personal Area Networks (WPANs), as shown in Figure 1.1.

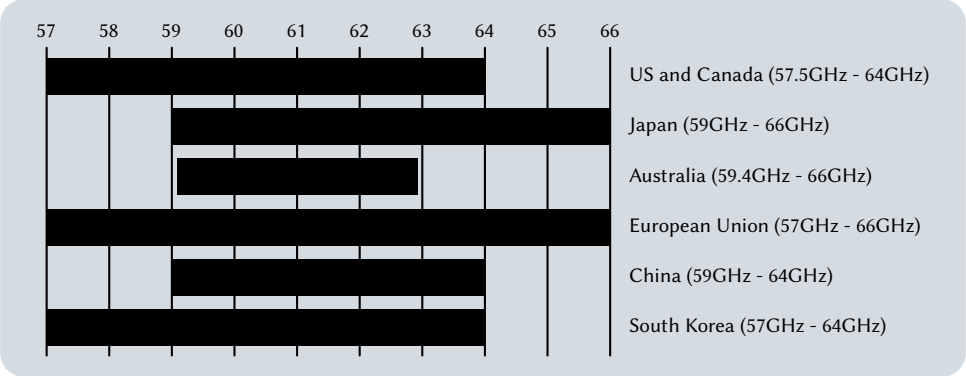


Figure 1.1: 60 GHz ISM band allocation worldwide

At the same time, the mobilization for the 5G mobile networks regulation have started and the prevision for the deployment of the preliminary systems is 2020 with the full working system in 2025. Table 1.1 puts up a not extensive list of specifications showing the evolution of the mobile (cell-phone) radio network. Some values are set for more than one network generation and are represented with gray background cells.

All that said, it is important to notice that although 5G wireless network is our principal motivation, this work is intended to discuss the Radio Frequency (RF) interface for mm-wave and design solutions on the radio receiver side, notably the global design implications of a radio

Table 1.1: A non exhaustive mobile network specifications evolution.

Gen	Access Tech.	Data Rate	Freq. Band	BW	Error Coding	Switching	Applications
1G	AMPS FDMA	2.4 kbps	800 MHz	30 kHz	NA	Circuit	Voice
2G	GSM TDMA	10 kbps	850/ 900/ 1800/ 1900 MHz	200 kHz	NA	Circuit	Voice, Data
	CDMA	10 kbps		1.25 MHz			
2.5G	GPRS	50 kbps		200 kHz		Circuit, Packet	
	EDGE	200 kbps		200 kHz			
3G	WCDMA UMTS	384 kbps	800/ 850/ 900/ 1800/ 2100MHz	5 MHz	Turbo Codes	Circuit, Packet	Voice, Data, Video calling
	CDMA2000	384 kbps		1.25MHz			
3.5G	HSUPA HSPDA	5–30 Mbps		5 MHz		Packet	
	EVDO	5–30 Mbps		1.25 MHz			
3.75G	LTE OFDMA/ SC-FDMA	100–200 Mbps	1.8, 2.6 GHz	1.4 – 20 MHz	Concat. Codes	Packet	Online gaming, HDTV
	WIMAX SOFDMA	100–200 Mbps	3.5, 5.8 GHz (initially)	1.25 MHz			
4G	LTE-A OFDMA/ SC-FDMA	DL 3 Gbps UL 1.5 Gbps	1.8, 2.6 GHz	1.4–20 MHz	Turbo Codes	Packet	Online gaming, HDTV
	WIMAX (Mobile) SOFDMA	100–200 Mbps	2.3, 2.5 and 3.5 GHz (initially)	3.5, 7, 5, 10 and 8.75 MHz (initially)			
5G	BDMA FBMC	10–50 Gbps (expected)	1.8, 2.6 GHz and mm-wave (expected)	will depend on the quantity of channels in use	LDPC	Packet	Ultra-HD Video, VR app.

* Table adapted from [9]

receiver operating for the 5G mm-wave band and including the future 60 GHz ISM band, which happened to be one of the bands of interest to 5G networks. An exhaustive list of papers exists with the intention of mitigate the 5G wireless network problematic, and specific topics discussion can be found in [9], [10] and [6]. Furthermore, we do intend to show that the global system design is not only more beneficial for reducing adaptation problems and used area, but also to improve the overall radio performance.

Finally, the goal of this work is to demonstrate a flux of project for a global design of the receiver side of a transceiver operating in a mm-wave band, and using a silicon substrate. The intention is to bypass intrinsic problems of miniaturization and technology bias, notably the constraints imposed by the silicon substrate, as well as to show the overall amelioration in performance of the system.

1.1 Overview

The objective of this work is to develop a unified design flow methodology of the receiver side on a radio transceiver. This co-design approach aims to minimize the problems encountered with the miniaturization of transistors for high-frequency signal systems. Although it can bring inherent problems to the system, miniaturization is a wanted characteristic not only because it can improve the overall performance of the system (notably selectivity, gain, noise factor, non-linear performance and possibly frequency tuning) but also in semiconductors fabrication process permitting high-speed and low-power transistors to be inexpensive in large scale. Usually, the development of a radio transceiver (both receiver or transmitter) is done with great attention on input/output specifications of impedance[2], and this can limit the system performance due to inter-stage adaptation networks.

The proposed work relaxes the inconvenience of input/output constraints due the capability of a full global design. It is expected that with this approach it could be possible to reduce the design time of the system, and reduce the total area of the circuit; both due the lack of

[2]Historically 50 Ω or 75 Ω are used as interconnection circuit impedance.

adaptation networks for the components of the system.

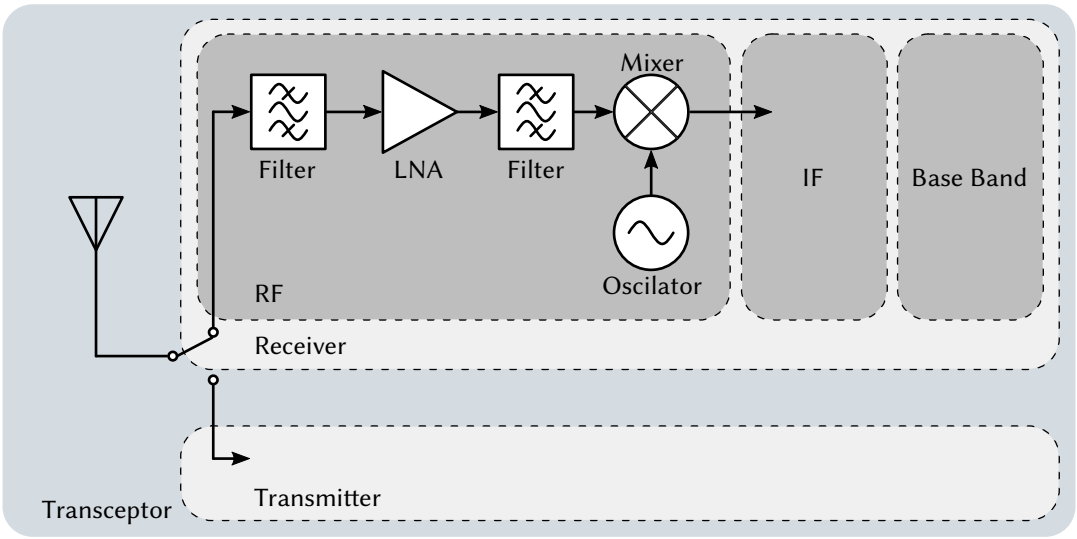


Figure 1.2: A simplified view of a radio transceiver, emphasis in RF part of receiver.

In Figure 1.2 are represented the block diagrams of a radio transceiver, with emphasis in the RF blocks of the reception chain. Each block represents different microwave functions placed on cascade in order to perform the reception task itself. The electromagnetic signal first arrives at the antenna and passes by the switch that selects the reception task. Depending on the system, the arriving signal is first filtered or amplified by the Low-Noise Amplifier (LNA) (suppressing the first filter). After the amplification the second filter in the diagram is normally named as *image filter*, and is used (in the best case) to remove the spurious signal generated by the mixing process.

The mixer[3] and the oscillator blocks works together to outputs the signal *down*-converted[4] and delivers to the Intermediate Frequency (IF) part of the receiver. The Local Oscillator (LO) generates a signal with frequency f_{LO} that is mixed with the output signal from the LNA signal centered in f_{RF}. The output signal of the mixer is then centered in f_{IF}, and the sent to the IF part of the receiver.

[3]The Mixer procedure is better explained in Annex A.4, where investigations on mm-wave mixers using NXP® QuBIC techonology are described.

[4]in this example the signal is down-converted since it is in the receiver side. In such case, the signal should be up-converted in the transmission side.

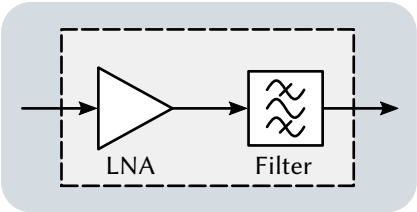


Figure 1.3: LNA and filter acting as a single block.

As the subject of this work we can point two main functions on the chain of reception on a microwave communication system: The LNA and the filter. The main objective is to analyses each one of the two structures and synthesize a block that do both functions at the same time, as in Figure 1.3, and discourage the system-block structure based design.

1.1.1 Known issues

There are some inherent problems that must be faced in order to effectively design for mm-wave in silicon substrate. Here is a list of the principal problems faced during the design and system project for the interest bands on this work.

Even though this issue does not directly affect the design process, it is important to understand this physical difficulty that interferes on a technology level on the 5G application project.

Band attenuation

Even though it does not directly affect the design process, the electromagnetic attenuation in the 60 GHz frequency band is an important issue on the application planning, as shown in 1.4 in both, dry and standard[5] environment as settled in [11]. In spite of the fact that the attenuation can reduce the communication distance, this property can be indeed exploited.

At 60 GHz, the Free-Space Path Loss (FSPL)[6] is approximately 88 dB loss at 10 m, causing a natural space isolation due to the oxygen absorption, what can be an inherent advantage in limited range operation, for example confined areas and/or small cells applications. In 5G

[5] air pressure = 1013.25 hPa, temperature = 15 °C, and water-vapor density = 7.5 g/m^3
[6] FSPL is defined in Appendix A.1

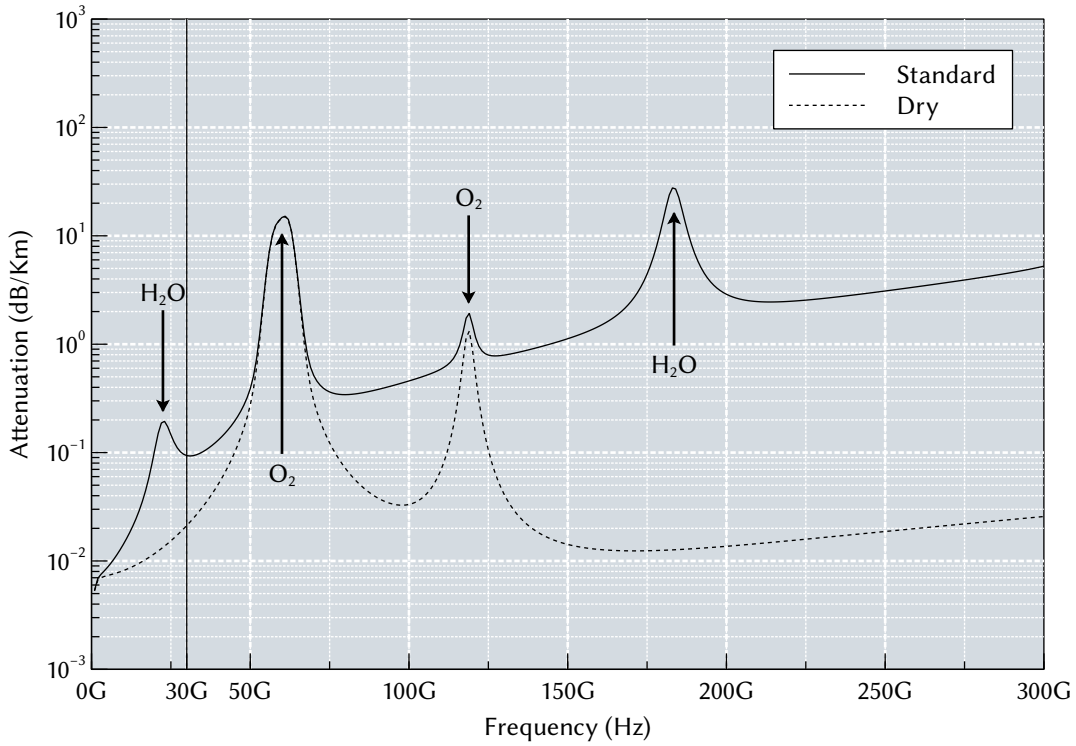


Figure 1.4: Atmospheric attenuation in millimeter band.

network directional propagation is intended to be used to enhance signal transmission and reception through the use of beamforming.

Actually, the standard 801.11ad[7] exploits this characteristic and can delivers high data rate and volume on a small distance radio communication. This permits, for example, to transfer a high-definition video from a portable to a TV (the two equipment must be in compliance with 801.11ad standard).

Transistor models and resistive substrate

In the past RFIC analog design for mm-wave were difficult due the utilization of models that fails to consider complex physical effects. For example energy models were very useful in the past to explain the functioning of transistors, but its use is impraticable today due to the miniaturization and density of transistor in an Integrated Circuit (IC). Great attention was given on this issue during the last two decades [12], [13] and [14]. Figure 1.5, illustrates a

[7]Although the name WiGiG is a current name for this standard this is not an official name.

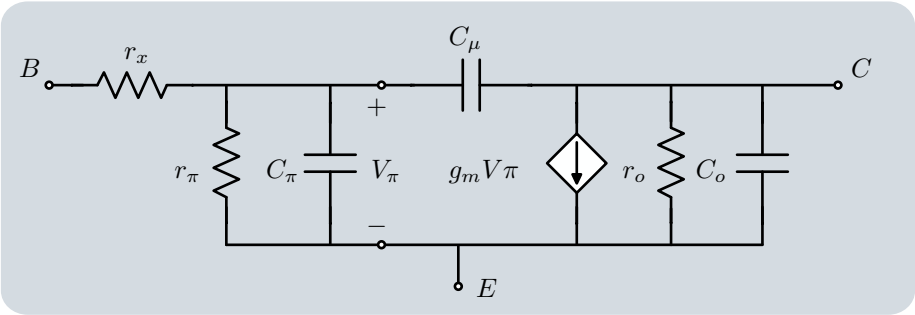


Figure 1.5: A simple model for small signal transistor operation.

simple small-signal model that can be used in handy analysis.

In 1996 the *Compact Model Council* was created with the purpose of standardization of the simulation models and used interfaces, limiting the choice of simulators and the design of new components. A success attempt initiated before that each simulation software used to use proprietary software. In 2013 the council was renamed for *Compact Model Coalition*, which now works under the *Silicon Integration Initiative* (Si2). The models supported by the coalition by the present day are:

1. BSIM3 a MOSFET model developed at the University of California in Berkeley.
2. BSIM4 a more modern version of BSIM3, also from UC Berkeley.
3. PSP yet another MOSFET model. PSP originally from Penn State-Philips, now semiconductor group as NXP Semiconductors is responsible.
4. BSIMSOI a model for Silicon On Insulator MOSFETs.
5. HICUM or HIgh CUrrent Model for bipolar transistors, from Dresden University of Technology, and University of California in San Diego.
6. MEXTRAM a compact model for bipolar transistors designed to model bipolar transistor circuits at high frequencies in Si and SiGe based process technologies. MEXTRAM was originally developed at NXP Semiconductors.
7. ASM-HEMT and MVSG, new standard models for Gallium Nitride (GaN) transistors.

The MEXTRAM model for the HBT (as illustrated in Figure 1.6, obtained in [15]) is planed to support the design of circuits at high frequency in Silicon (Si) and Silicon-Germanium (SiGe) technologies, it is a much more complete (and complex) model compared with Ebers-

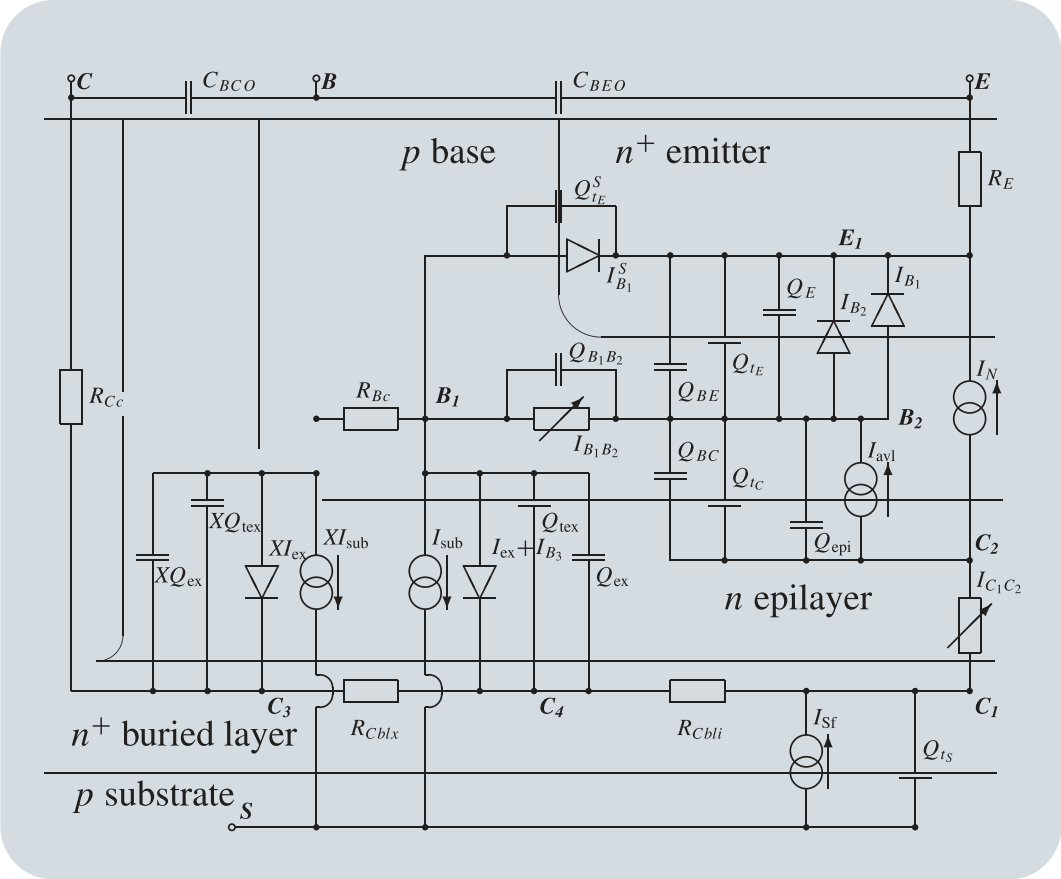


Figure 1.6: Complete MEXTRAM equivalent circuit for the vertical NPN transistor. Modified image from the original rapport from MEXTRAM documentation.

Moll or Spice-Gummel-Poon model for transistors, for example. Both last transistors do not consider accurately the stored charge dynamics, wich determines the transistor high speed performance [16].

Although MEXTRAM models displays good simulation results, the intrinsic lossy silicon substrate introduces finite resistance to ground (which works as current divisor), as marked in red in Figure 1.7, and unwanted paths between close components, some of which can corrupt critical signals. This lossy substrate is a big disadvantage when compared to III-V compound process technologies.

Furthermore, in order to reduce the unwanted effects caused by the lossy silicon substrate (cross-talk, coupling, noise, etc...) simple techniques can be used such as the utilization of a deep trench ring, a ring of highly doped P-substrate connected to the ground, or both (Figure 1.8) around sensitive circuits. These structures are known as guard-rings and can

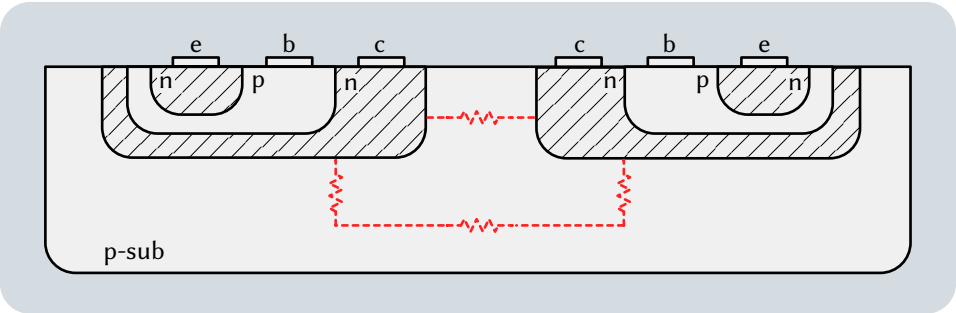


Figure 1.7: Cross-view of two transistors with virtual substrate connections in red.

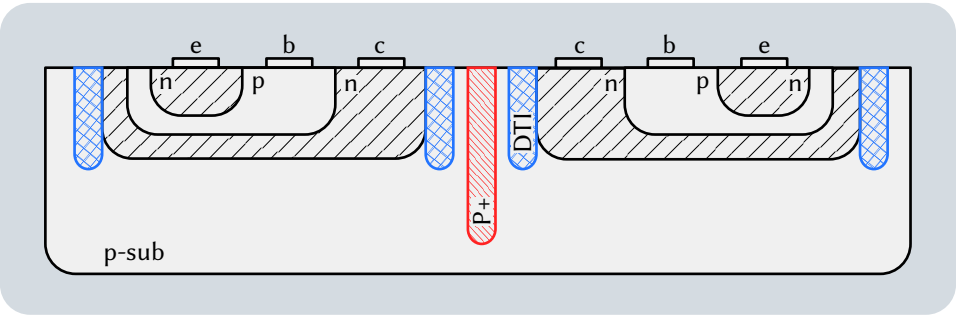


Figure 1.8: Cross-view of two transistors with guard-rings structures.

provide low impedance path to ground for charge generated in the substrate.

The design kit used in this work permits to set automatic guard rings as the component transistor option, although it is not always a good choice to set such parameters automatically, this kind of automation can optimize the design-flow.

Inductance components and the frequency relation

One advantage of commercial design kits is the utilization of pre-modeled components (inductance, capacitance, ...), these components are handful during initial design, but for high frequencies it can ruin the fabricated design, wasting time and money. In mm-wave design, the final dimensions of the circuit have implications in the circuit response due its frequency operation; for example 60 GHz signal has a wavelength of λ=5 mm approximately, so a 500 µm long circuit is 10% of λ, and is near of $\lambda/8$.

It is important to pay attention on miniaturization aspects of mm-wave design specially with inductance and line metal connections, these kind of component can become an unwanted inductance (if not), transmission lines or simply coupling with another component ruining the

entire circuit. One manner to attenuate this limitation is the use of electromagnetic (EM) simulation on critical parts of the circuit.

Electromagnetic simulations can exhibit the diversity of interactions on each circuit component, simulation how each component behaves in the frequency of interest and more. Although the EM simulation gives virtually all information of the circuit physical behavior, its simulation time consuming and parameter setting are enormous drawbacks, what forces the designer to have strong synthesis and analysis circuit background.

1.1.2 Material and Methods

In this work the Qubic design kit from NXP Semiconductors is used, this is a mature 0.25 µm SiGe BiCMOS technology with HBT with f_T that goes up to 180 GHz with interface for Cadence® Virtuoso® and Keysight® ADS® simulation software. The choice of this technology lies on the partnership between NXP Semiconductors and the XLIM University of Limoges.

This technology has as characteristics: Well established and reliable simulation results; well modeled lumped components; six layers of metal with two highest metal layers with low resistive materials; deep trench isolation layer, high velocity bipolar transistors (HBT), MEXTRAM bipolar transistor modeling and highly resistive substrate (due silicon properties).

Measurements were performed at the dependencies of XLIM, with the available instruments at that time. Notably:

1. Microwave Network Analyzer (PNA-X, model N5247A) from Agilent® with frequency band is from 10 MHz up to 67 GHz,
2. A Cascade® micro-handling table,
3. DC and RF probes,
4. A voltage source bank with eight independent sources, and
5. Two cables for mm-wave measurements with 8 dB attenuation at 60 GHz each.

Finally, all measurements were performed at the same room temperature (approximately 27 °C). All data was recorded and later plotted with Veusz (https://veusz.github.io/).

1.2 This work organization

This work is divided in six chapters plus one appendix chapter. The chapters were carefully divided in a way that each chapter can be read separately without lost of comprehension, although there must exist specific parts which these efforts are not well presented. This first chapter is a resume containing the motivations for the development of this work, and also the presentation of the final objectives. Here it is also shown difficulties inherent to the mm-wave design in Silicon. The second chapter is an overview of the design techniques used in this work. It is introduced as a chapter due to the difficulties that were found in order to design and simulate the circuits in mm-wave due to the lack of information in literature.

The third chapter is a discussion about the filtering theory, with emphasis in resonating ring structures working as filters. Furthermore, a meander filter ring structure (with reduced dimensions) is presented in this chapter. Results of fabricated filtering resonators in Silicon are shown and compared with the state-of-the-art.

The reception chain is then firstly examined with the introduction of the LNA in the fourth chapter. In this chapter a revision on the LNA fundamentals is developed. Additionally, results with more than ten years on BiCMOS Silicon LNA design results are presented for comparison purposes.

Finally, both measure and simulation results of the fabricated circuits are examined in the fifth chapter. It would be possible to say that it is the main chapter of this work, because it is the chapter were the discussion about the global system design, with the exemplification of a filtering LNA designed as a single block and working at the 60GHz ISM frequency band. To conclude, the appendix and the bibliography are presented after the fifth chapter.

Chapter 2

Layout techniques for mm-Wave design in silicon

SIMULATION-driven circuit design becomes more and more important in microelectronic industry due to the necessity of fast execution for production. Although the design work-flow changes for different circuits specifications, it is based on a well known and secure design procedure that guarantee error-prone devices. However, new technologies keep tightening design constraints in frequency, consumption size and others, and it turns out that the use of a classical design approach has to be constantly reevaluated due to different problems introduced with the miniaturization of the technology.

In this chapter, an algorithmic method for RFIC design – validated with an LNA design – for mm-wave using Computer-Aided Design (CAD) tools (Cadence® Virtuoso® and ADS® Momentum®) is demonstrated. Information about how to perform with proposed work-flow and further discussion is also suggested in the last section.

2.1 Layout Design Methodology

Classically a LNA design is done taking into consideration the requirements of the reception-chain for a given system transceiver (frequency, bandwidth, consumption, gain, noise, etc.), the objective is therefore to design a circuit that best fits its specifications. To perform this assignment a general design flow is roughly described in [17] and [18], although it is not a closed rule process design can be divided into three steps before production: circuit requirement

identification (which includes schematic analysis and simulation), layout design, and initial fabrication for evaluation. By that, during circuit RFIC LNA design, a not extensive list of tasks the designer have to perform is:

1. System specification:
    - Mitigate specifications and determine which technology should be used, if the case.
    - Determine which topology best fits to specifications.
    - Choose transistor(s) to be used in design that meet required noise, if the case.
    - Adapt the amplifier for noise and gain, in LNA design.
    - Develop a preliminary design of circuit.
    - Compute circuit design to evaluate if it meets specification
2. Layout design
    - Sketch the circuit blueprint.
    - Draw the layout design.
    - Extract circuit from layout design.
    - Compare layout and schematic responses, then determine if design meet specifications.
3. Evaluation tests
    - Measure fabricated circuit and compare with simulation results.

For high-frequency mm-wave design the designer have to care about the wavelength of the RF signal. For mm-wave circuits, lumped element analysis can be inaccurate because the dimensions of the designed circuit can have the same order of magnitude of the signal wavelengths. Consequently, to ensure that the layout performs well the designer has to be familiar with distributed circuit elements and transmission-line theory.

More advanced designs need also that the designer be familiar with CAD software, considering that manual synthesis for complex mm-wave circuits become quickly impracticable primarily due to realization time. Nowadays, CAD software (notably Cadence® Virtuoso® and Keysight® ADS®) offers a great simulation environment to realize fabricated circuits that fit well with simulated results.

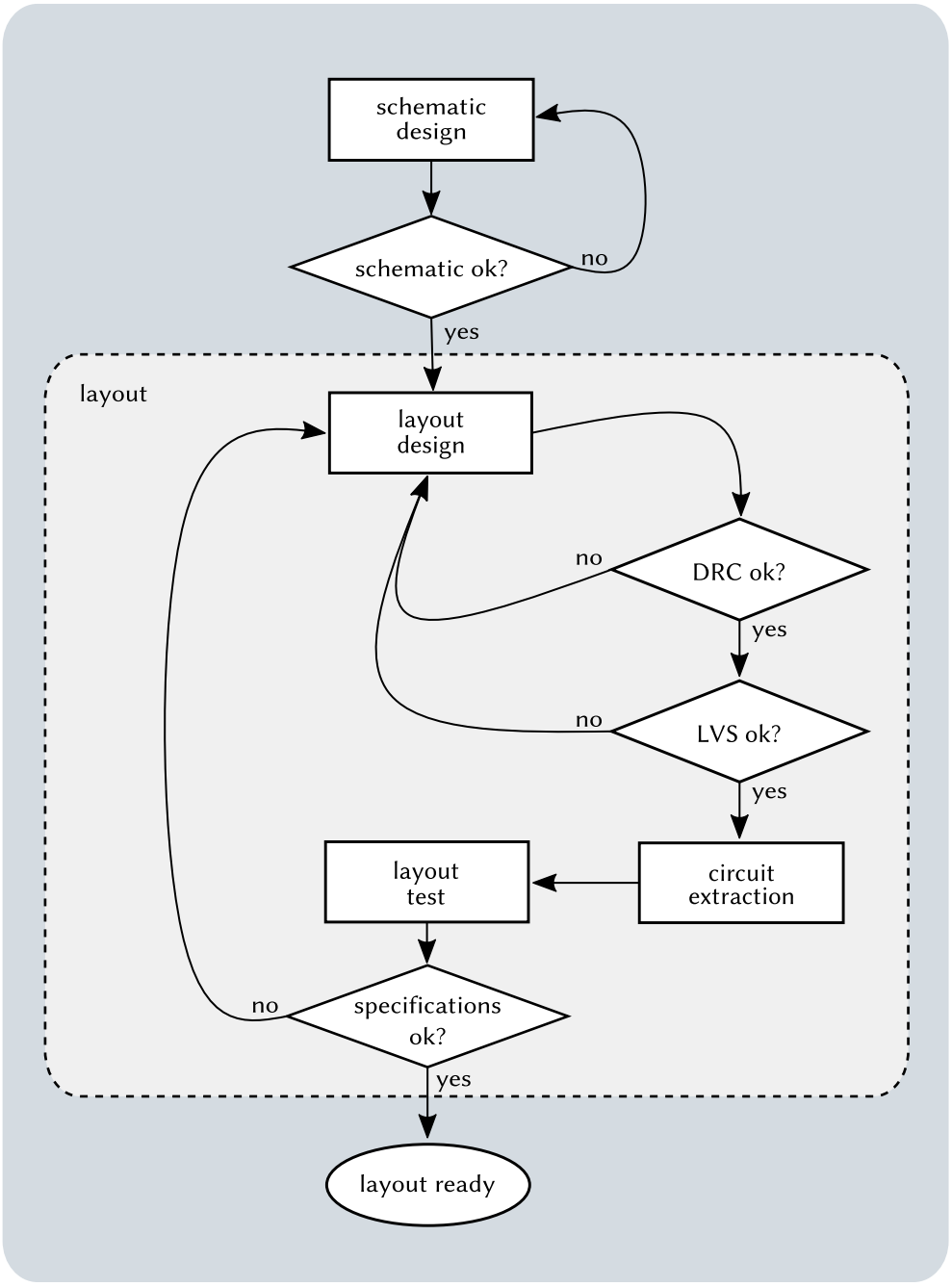


Figure 2.1: Design flow for analog circuit design emphasizing layout design steps.

On the classical design flow approach, it is first set the conditions and requirements of the circuit (technology, topology, transistors, etc.). After, we proceed with the second stage, when the definition and validation of the schematic of the circuit is done. Only then the layout design stage begins, as illustrated in Figure 2.1.

Good layout design practice includes within its firsts steps discussions about the blueprint of the circuit layout. This blueprint has to contain the placement of each component (or each part) of the circuit and it have to be in accordance with the Design Rule Check (DRC) of the technology. The DRC is an operation which assures that the designed layout masks are in conformity with the rules of fabrication. After the circuit is completed the next move is to test the layout against its schematic version; thus the designer knows effectively if all circuit components are present in its layout version. This procedure is called Layout Versus Schematic (LVS) test.

After LVS is completed with no mistakes, the next step is to perform circuit extraction. Circuit extraction is the process of derivation of a schematic version of the layout, with its circuit interferers (intrinsic from layout) taken into account. This action is important because the designer can efficiently test the layout and determine if its response fit with the system design specification. In case the extracted version simulation results are not in accord with what is attended, then corrections must be performed in the layout.

Circuit extraction software can support different modes of layout circuit extraction. A general example is presented in Figure 2.2 where various methods of extractions are shown. In Figure 2.2 R stands for resistive extraction, C for capacitive extraction, L for inductive extraction and K for coupling interference between circuit metal connections, this last is represented with arrows in $RLCK$ extraction.

Note that extraction examples in Figure 2.2 depend on the employed software and its context. For example, a designer wants to extract his layout and decided to use R extraction with 25 µm of circuit division. Assuming that the developed design is a piece of metal measuring 100×10 µm^2, then the parasite extractor can divide the circuit into four resistors with $R=25\times10\times R_{\square}\ \Omega$. In other words, circuit extraction depends on the choice of designer and how the circuit will be

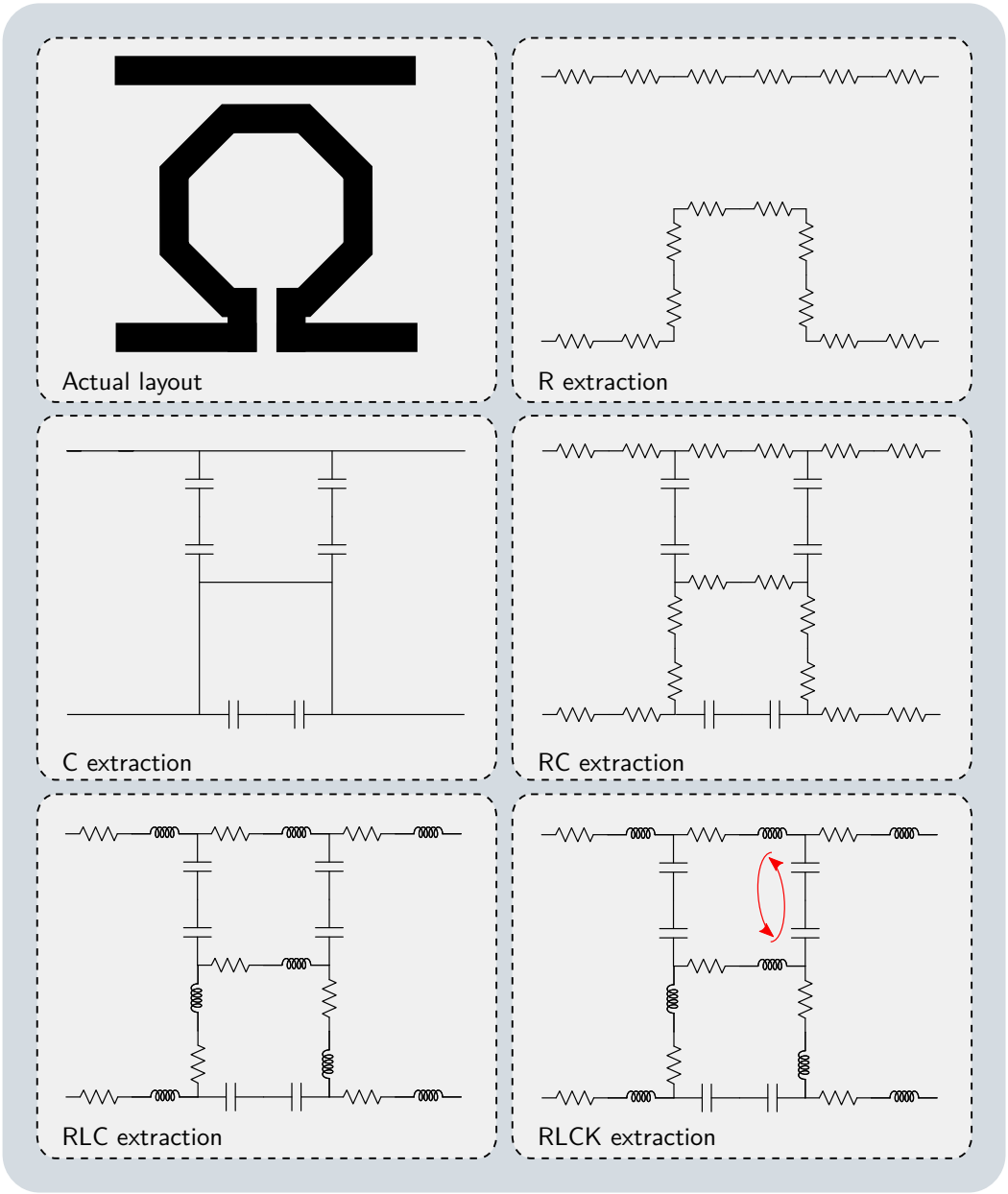


Figure 2.2: Examples of different methods of circuit extraction from layout.

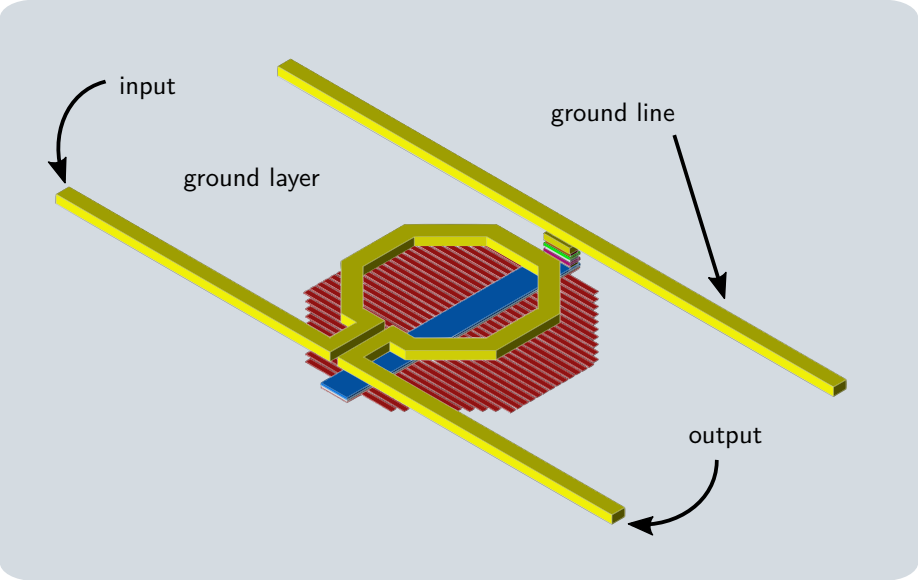


Figure 2.3: Circuit simulated with different extraction methods.

divided by the extractor software.

Parameter setting for extraction is challenging because it is highly dependent on the circuit and its specifications. That means that setting bad extraction parameter values can lead to completely different (and sometimes wrong) results. For example, the layout of Figure 2.3, was simulated to evaluate its S-parameter performance according to different types of circuit extractions. The tools used in this example were ASSURA® QRC for the circuit extractions and Keysight® Momentum® to Electromagnetic (EM) simulation, the schematic response was included in the graph of Figure 2.4 for comparative purposes.

The layout in Figure 2.4 is composed of a one turn octagonal inductance with a line of 100×10 µm^2 on both the input and the output access, a ground line connect to the inductance ground layer. Figure 2.4 illustrates the input impedance results for the circuit with different kinds of extraction, including EM simulation. Inductance value and metal dimensions are not important in this example because we want to stress the difference within the curves response for the same circuit as motivation to investigate different extraction methods.

Simulations can lead to erroneout result interpretations due to its high dependency on the choice of extraction parameters, the fact that the technology component cells are modeled as a black-box, and therefore some parasites are not well modeled, also happens to be a problem

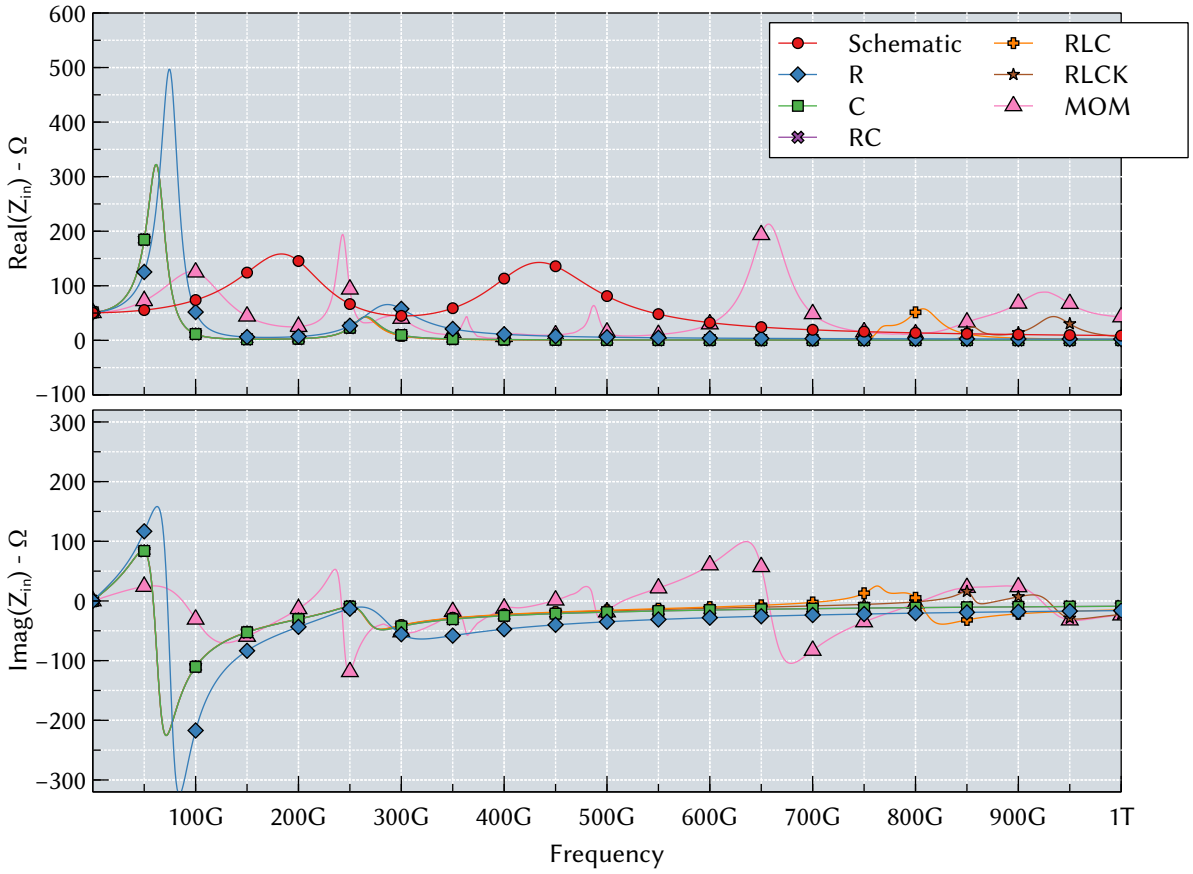


Figure 2.4: Comparison of simulation on input impedance of same circuit and with different extraction types.

because only the connected metal lines have the parasites computed. This way the simulation results rely on the modeled parasitics of each technology component.

Additionally, note that R, C, RC, RLC and RLCK extractions in the example give virtually the same frequency response (Figure 2.4), this result corroborates with the statement that the circuit is better modeled as a distributed-element circuit, because ASSURA® cannot model the interferers of the inductor. Furthermore, EM simulation gives a completely different result. At this point, the only information collected was that no extraction techniques were reliable because none comparison structure was available.

2.2 Investigations on mm-Wave co-design

Because in mm-wave wavelength (30 GHz to 300 GHz) varies between $1\,\text{cm} \leq \lambda \leq 1\,\text{mm}$ in free-space, and silicon design circuit dimensions have usually same order of magnitude (normally hundreds of μm^2), phase change effects cannot be neglected. Also, the dimensions of the circuits designed in this work are bigger than the normal due to the co-design strategy. This means that the full circuit can be designed in a row, and therefore the circuit itself is electrically larger than the isolated circuit components.

Thus it is necessary to analyze different extraction modes to better adapt the design flow to the circuits being projected. Typically, EM modeling is preferred to problems of distributed elements, but different extraction modes have been evolving and worth to be investigated

During the investigation, five circuits were sent to fabrication within three fabrication runs. The circuit sent in the first run was a 60 GHz LNA working on ISM band. After on the second run, two circuits were sent, an octagonal ring resonator filter, and a filtering 60 GHz LNA that uses the octagonal ring filter. Finally, in the last run, we sent a meander version of the filtering 60 GHz LNA and the meander filter itself. The meander ring filter is a smaller version of the ring resonator.

The first circuit (LNA 60 GHz) was realized within a workflow with only RLCK circuit extraction. No EM simulation was performed. This simulation choice was taken because

circuit layout had 750×520 μm^2, therefore with width of about six times smaller than the signal wavelength at 60 GHz in freespace ($\lambda_{@60\,GHz} \approx 5$ mm). Therefore simulated results were expected to be good approximations of circuit response.

Even though RLCK circuit extraction have performed well during s-parameters comparison with measurements (Figure 2.5, left side), frequencies nearby 60 GHz s-parameters begin to deviate. Parameter S_{11}, for example, shows a drop at 60 GHz that not meet simulations. Furthermore, although the measurements and simulation values are not exactly the same, it can be seen that EM modeling follow the same tendency.

In addition, in the right side of Figure 2.5 is shown the absolute error in log scale between different extraction modes and measurement ($E_a = |S_{measure} - S_{simulation}|$), so it is possible to analyze the extraction parameters more systematically, it is seen that although gain (S_{21}) is better represented using RLCK extraction (smaller error), Momentum® modeling error is more constant. For the other parameters (S_{11} and S_{22}) RLCK extraction shows higher error than on EM modeling, while small response drops happen with all extraction methods.

From the S-parameter error calculated due to simulation and measurements (Figure 2.5) we can speculate that, although the error is smaller on RLCK extractinon for frequencies bellow 60 GHz, in the parameter S_{21}, the error with EM extraction have less variation, further the error is even smaller on the other parameters (S_{11} and S_{22}).

The second active circuit set to fabrication was a version of the LNA connected with a filter, hence a filtering LNA that is intended to be a part of this work objective. During the design stage, the circuit was developed cascading the circuits(first stage amplifier, filter resonator, the second and third amplifier resonator connected in cascade). The resonator was electromagnetically simulated because RLCK circuit extraction does not model appropriately the resonant effect of the ring. Also, this simulation workflow was used because the circuit size was 1.34 mm^2, and so it was expected unimportant phase delay along layout realization.

Standing that during simulations it was virtually granted that both structures (resonator and cascode stages) were optimally adapted, and it would be expected that the simulation response of the full circuit was correct. It happens that due to the circuit size and its characteristics,

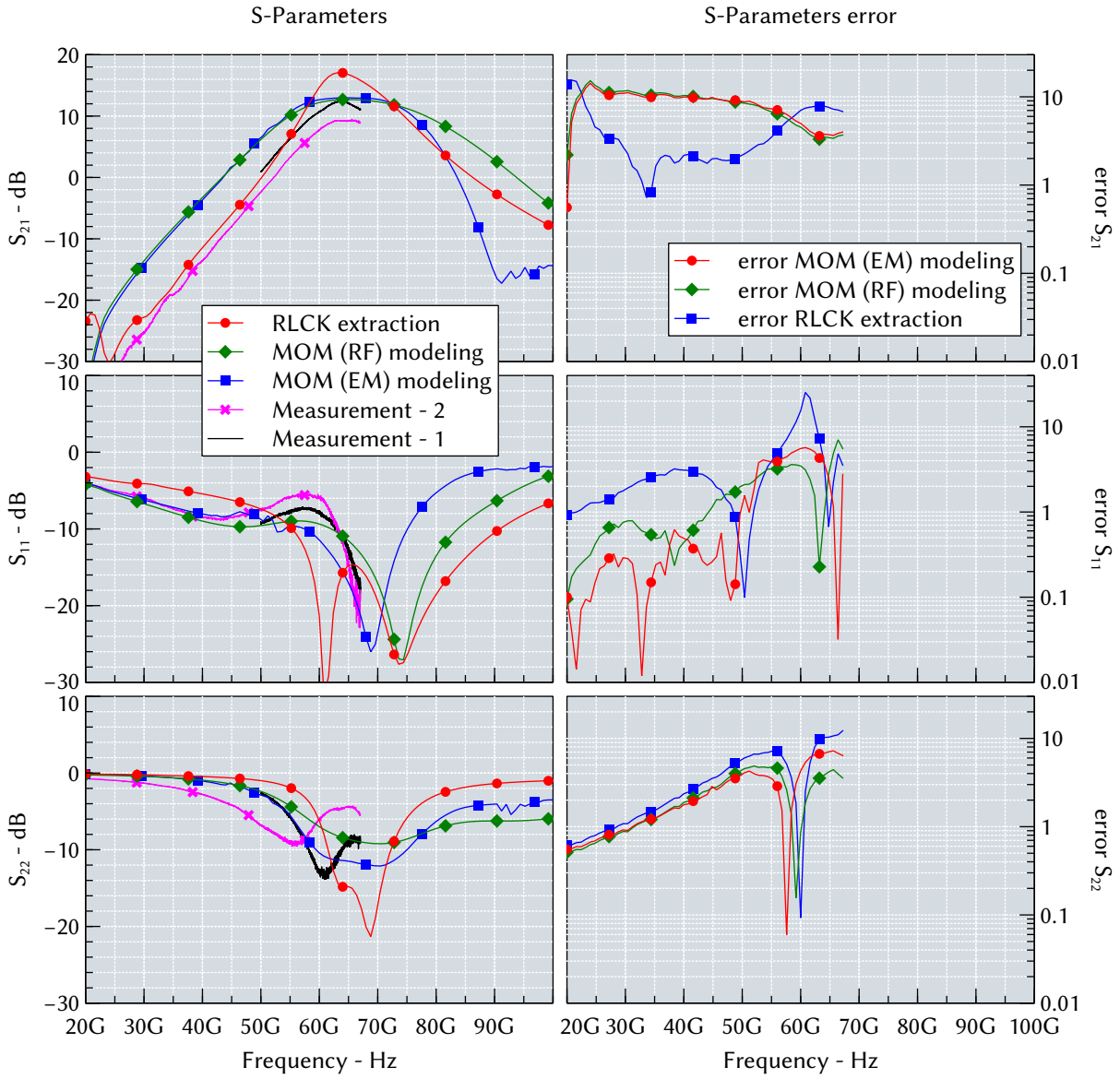


Figure 2.5: Comparison of measured 60 GHz LNA and simulation results in different modes of extraction. First column show s-parameters of measured and simulated structures, second column is the corresponding absolute error of simulations related to the measurement of each s-parameter.

the reference plane is not electrically the same over the IC, what should be taken into account during the design. And therefore, the first version of filtering LNA did not perform as expected[1].

Hence, it is important to take advantage of CAD design in order to evaluate different configurations of the reference plane and better investigate the behavior of the circuit. For example, the second version of filtering LNA (Figure 2.6) was proposed with a more compact version of the resonator filter, and a different topology. Electromagnetic modeling of the full passive part of the circuit was performed in order to describe and optimize its behavior.

EM circuit modeling is performed taking into account all interactions of the circuit parasites. Every connection between passive and/or active component on the circuit is modeled as a Momentum® port in the EM model and further connected to the active parts of the circuit. This way it is also possible to be aware of about the reference plane interactions with the circuit components.

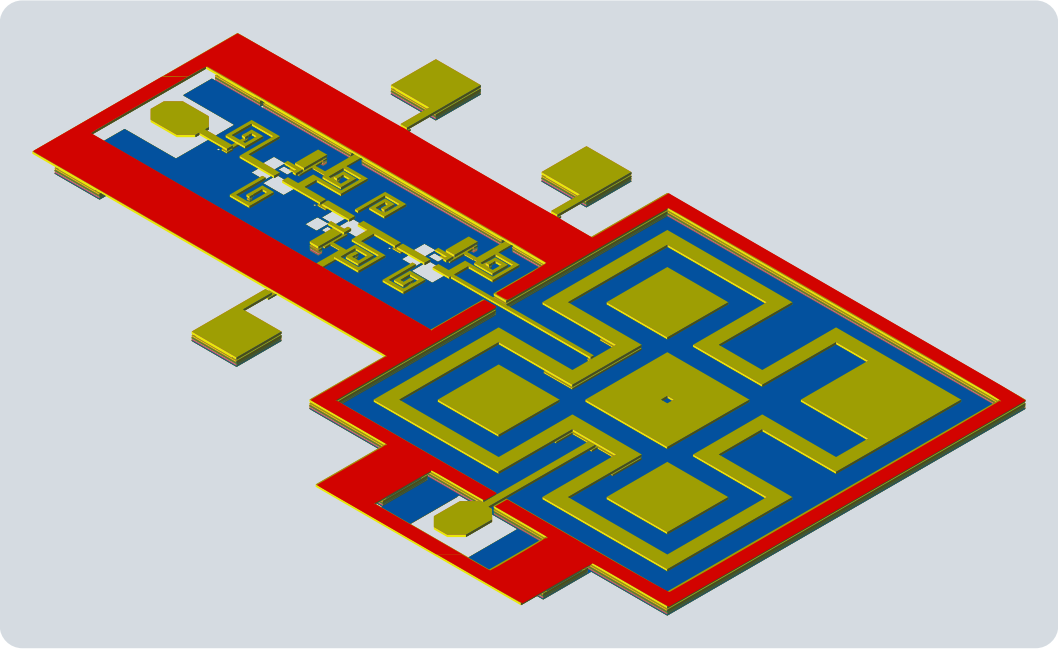


Figure 2.6: Passive section of the second version of filtering LNA design.

In the design of Figure 2.6 all the plane in red and blue is the ground plane (reference) connected with *vias* going from metal one up to metal six. Circuit ground pads are connected using Ground-Signal-Ground (GSG) probes, and therefore reference is not the same all over

[1]Full circuit description is given in chapter 5.

the circuit.

2.2.1 Reference plane influence over design

Reference plane carries out great importance on mm-wave circuit design. That happens because the wavelength of the irradiated signal is of the same order of magnitude of the circuit, as aforementioned. For example, Figure 2.7 illustrates the different responses of the filter resonator used in the second version of the filtering LNA due to different port configuration. Note that the response changes with different ground port positions.

In the upper design of Figure 2.7 red dots mark stacked differential ports configuration, in this configuration both signal and ground ports, are connected on metal six (*yellow*) and metal one (*blue*).

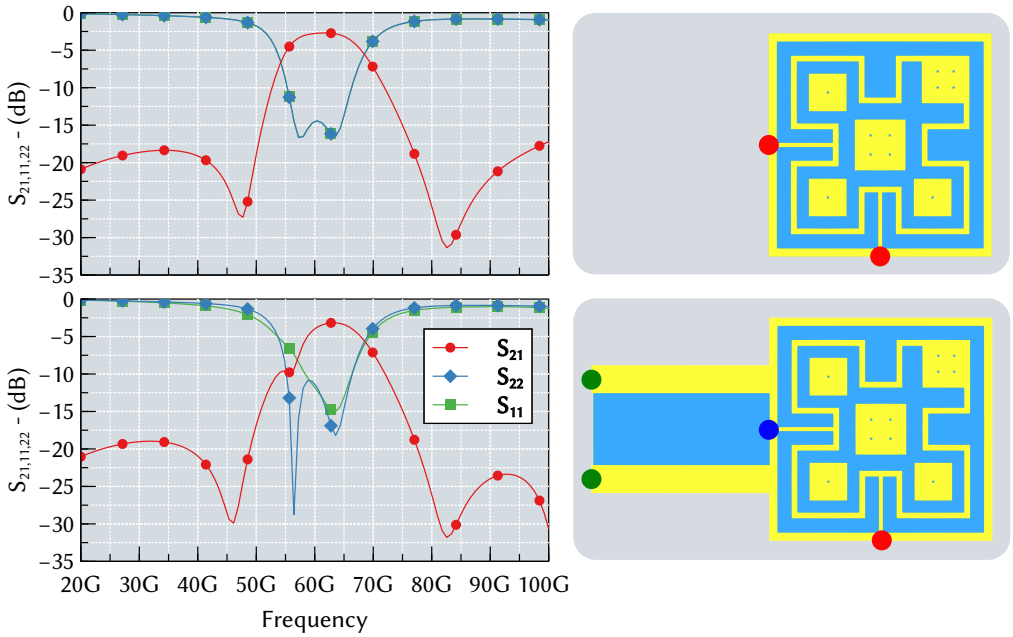


Figure 2.7: Reference plan influence over resonator circuit design.

In the bottom design of Figure 2.7 red dot performs the same way that in the last design, blue and green dots are two parts of the differential port were blue dot is the signal port and green dot is ground port. It is seen that s-parameters differ from last design due to ground ports placement, what influences the filter circuit adaptation to the active part of the circuit, that in this case must be placed before the resonator, and connected to RF input of the filter

(blue dot).

The difference in the simulation response implies that the designer has to perform the simulations according to the circuit connection during usage (measurements). The impact of these steps for co-design methodologies is that: first, the number of EM simulations can grow fast, and therefore the time spent on the design; second, the blueprint of the layout can change during the design, what favors co-design methodologies since in these cases the full circuit is implemented.

2.3 mm-Wave design simulation

Based on the classical design work-flow (Figure 2.1) a different layout design methodology that introduces field analysis concurrently with classical circuit extraction (Figure 2.8) is proposed. In this methodology, two complementary circuits remain after the previously schematic simulation is performed. In the first circuit, on the passive design side, all passive components of the circuit are electromagnetically simulated. In the second, that is the circuit that includes the active design side of the circuit, classical circuit extraction is performed.

On the passive design side of the layout block, as many iterations as necessary of EM simulation are performed, illustrated by the red arrow in Figure 2.8. These iterations are required to find and to reduce mutual interference in design; in this step EM simulation of the complete passive components of the circuit including the reference plan is performed, and then a schematic view with a multi-port s-parameters is generated.

On the active design side, the very same procedure of Figure 2.1 is taken into account. After the schematic simulation is according to the specifications, layout design is performed and so LVS and circuit extraction. Once everything is right with the extracted circuit, then the layout can be used in the next step. Because both circuits are complementary, attention must be given to the blueprint of both passive and active layout structures. These structures have to be designed in a way they connect flawlessly, with no gaps or superposition.

The next step is to create a schematic view with the two connected structures: the extracted

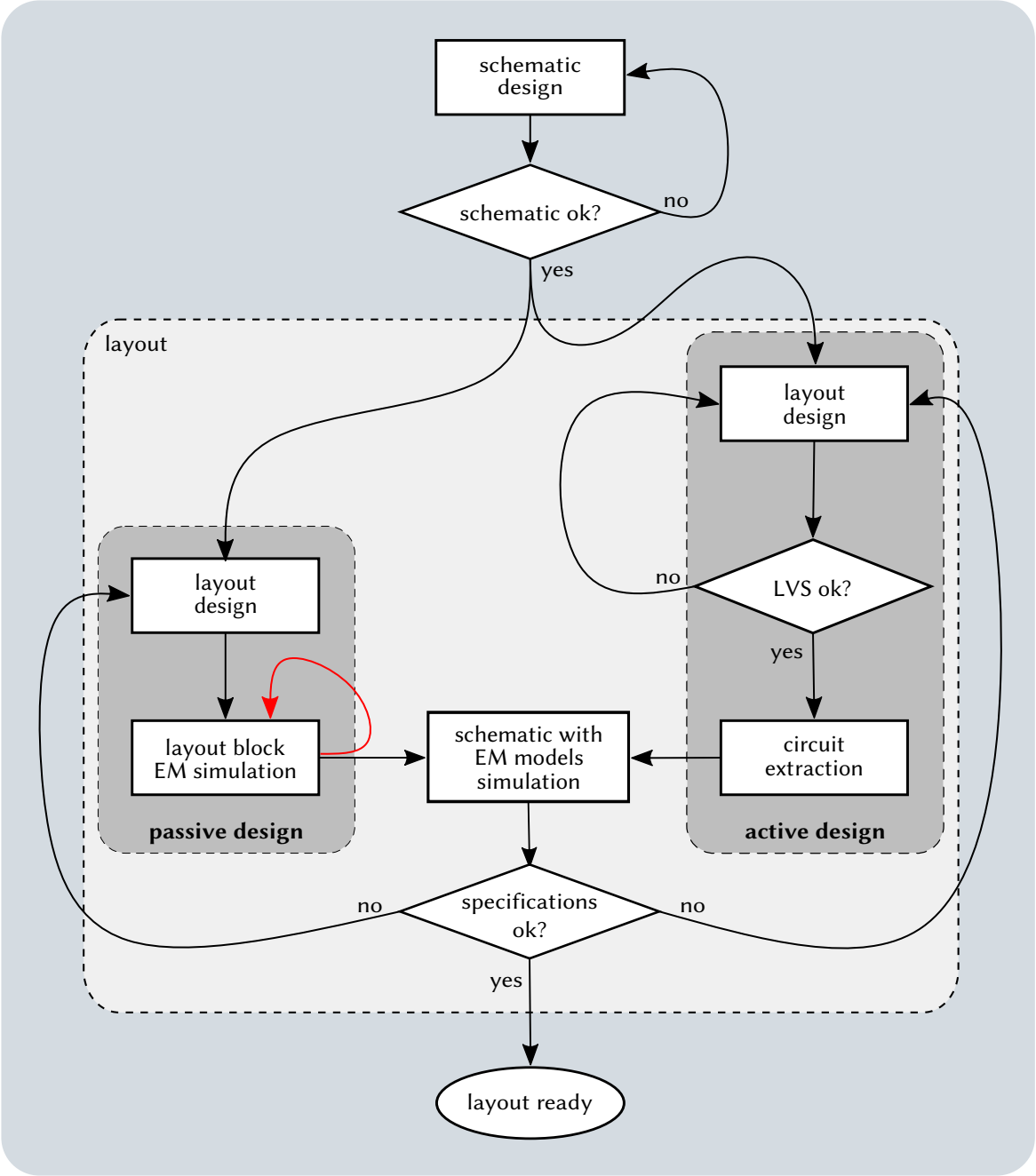


Figure 2.8: Proposed concurrent design flow for analog circuit.

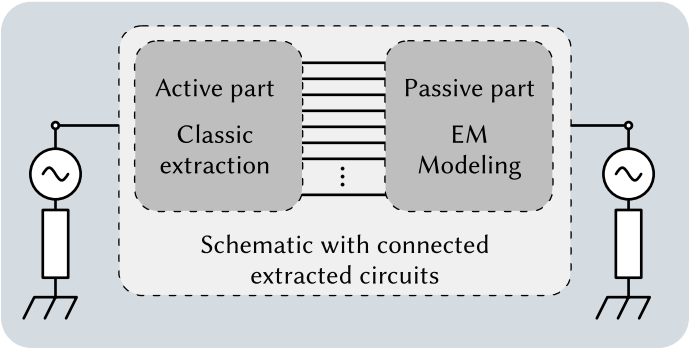


Figure 2.9: Test-bench example for multiple extraction design used in this work.

circuit containing the active models and the electromagnetically simulated circuit. The final layout is the concatenation of layout views (extracted and EM simulated) corresponding to the structures used in the last schematic simulation (Figure 2.9). The final layout do not have an unique extracted view in this method, although the it is formed with all views that are individually electromagnetically simulated or circuit extracted.

This complementary design flow was developed according with the design needs of the circuits proposed in this work (as demonstrated in further sections). It demonstrated to be adapted for mm-wave band design in silicon SiGe:C BiCMOS technology because the models for the active devices included in the Process Design Kit (PDK) includes a high-frequency response. Finally, it is important to be aware that during EM simulation due to its huge use of computer resources computation time can quickly become an enormous constraint.

2.4 Discussion

During the development of this work special attention about the design methodology was taken into account, the idea of documenting the the flux procedure became imperative due to the lack of literature found in the subject of layout techniques. This consideration become even more important if we consider that the use of silicon technologies on mm-wave circuit design is still an emerging process. Therefore, one of the most important contributions of this work are the consiretarions on layout design demonstrated in this chapter.

In that regard, it could be said that the importance of the design methodology was neglected

at first. However, at the time of first measurements we started to discuss about how to accord more attention to the simulation steps in orther to obtain models that better represent the circuit. Originally our difficulty was to compare the simulated results with measurements, since we had not any device to compare and therefore our first fabricated circuit did not met our simulations during measurements.

Imediatelly we noted that more effort had to be given in order to develop a more systematic approach to analog circuit design. We noted that at this point it was important to design a layout that match the electric and magnetic iterations that happens on the physical circuit with reliability.

In this chapter specific attention to the design flux is given to facilitate simulation procedure. It is written in a way so it could be possible to use these procedures in order to design and simulate any mm-wave circuits fabricated in silicon. Finally, this simulation approach can be easily adapted in a co-design environment not only were circuit and devices can be optimized to meet the specifications, but also on a system level where multiple circuits have to be optimized at the same time.

Chapter 3

Ring Resonator Filters

Theory and realization

FREQUENCY filter theory is a long known part of electrical engineering, it is strongly based and dependent on Fourier analysis and circuit response. In addition to be an essential element in a radio frequency transceiver filters also can be found in a variety of applications, from control theory to imaging processing. In radio frequency, they can be used among other tasks to reduce the noise, isolate frequencies or to select a frequency band of interest of a received signal. In this last task, the filter supresses the unwanted part of its input signal, wich can be seen as spurious frequencies.

The unwanted frequencies of a signal can be either generated by exterior and by the circuit itself. Usually, non-linear components are a great source of unwanted signals inside the circuit. Examples of non-linear devices that introduces spourious signals are amplifiers, oscillators, and mixers. On the other hand in a superheterodyne receiver architecture, the received signal is assumed to be a corrupted version of the original signal sent by the transmitter. For that reason, filters are placed in the receiver chain in order to suppress out-band signals added by the channel.

Although filter design is a well-established discipline, analog passive filter integration is difficult in microcircuits due to the lumped devices dimensios. In commercial systems, this complication is commonly solved with the aid of external filter components. Therefore many research fields on filtering devices for microcircuits are still open, and the research on original distributed structures for filtering tasks is one of them.

In classical lumped filter design, general filter masks are used to help during the design procedure. The filter mask is tuned according with the application requirements, only after its creation the filter is synthesized. Examples of different filter masks are illustrated in Figure 3.1.

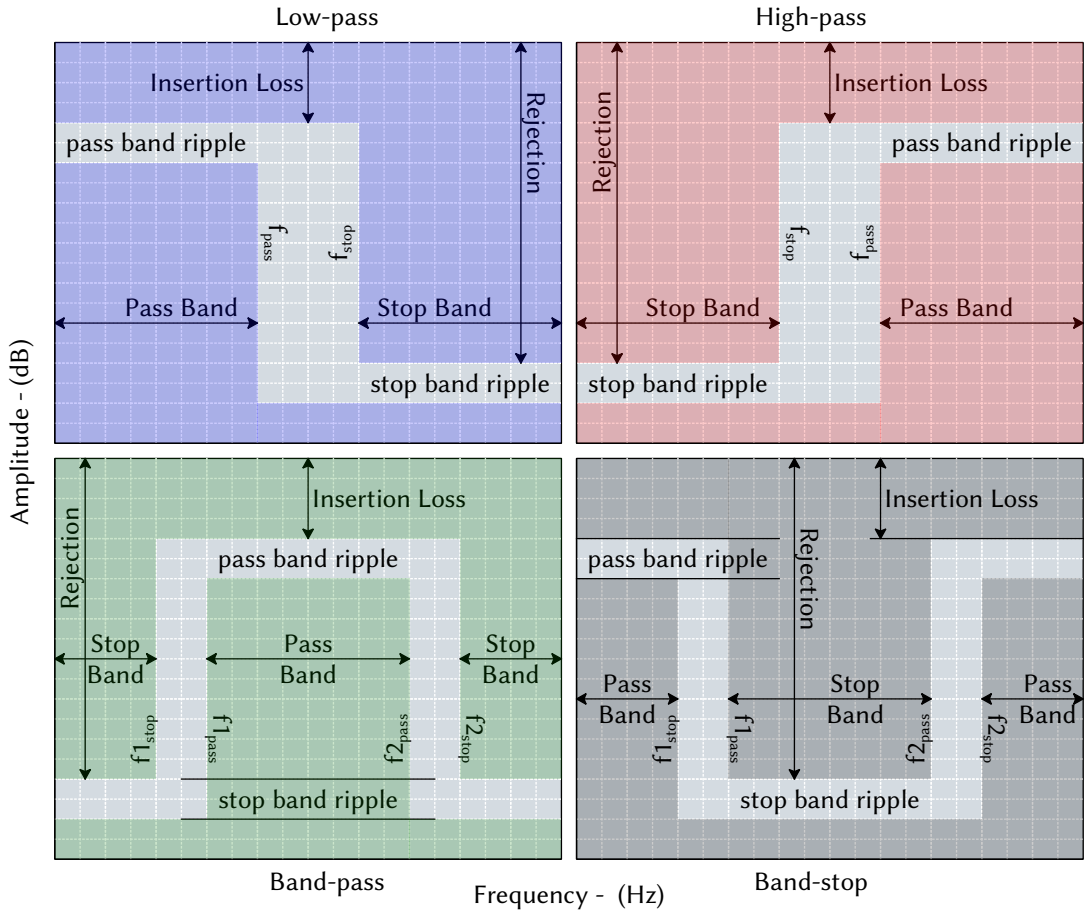


Figure 3.1: Filter mask design examples.

In distributed filter designed, all filter components are meant to be *lumped together* in the same structure. This constructions is conceptually simple, but its synthesis becomes unreliable as the signal frequencies increases. Circuit minimization of silicon structures and integration offers great potential to co-design lumped filters and optimal inter-stage system adaptation. All these benefits brings difficulties that must be outperformed during the design step. In this work, we propose two ring resonator designs to meet mm-wave ISM band at 60 GHz. The proposed structures were proven to be well suited for mm-wave filter design due to its low insertion loss, and its synthesis ease.

One of the first tasks during IC resonator circuit design is extract a model of the designed structure. There are many ways to perform this task, that can be: To use a Transmission Line (TL) equivalent circuit, EM modeling with Maxwell equations or EM simulation of design structure using CAD software. Furthermore, resonator filter structures are usually designed in a way that topology dimensions can influence differently on filter response, and for that reason resonator filter design can be time consuming.

In this chapter we analyze the use of ring resonator structures as mm-wave filters, and illustrate with both designed and fabricated circuits. In the last section the two designed circuits are compared with the mm-wave filter designs found in literature.

3.1 Ring Resonators

A ring resonator is a distributed circuit structure that resonate at certain wavelengths due to an incident signal. For such a simple circuit, however, many complicated variants can be created. For example, by modifying its basic structure such as cutting a slit or adding a notch, cascading two or more rings, connecting the ring with solid-state devices, integrating the ring with multiple inputs and output lines, or many others. Back to the time of the introduction of the ring resonators (about 1960), field analysis was a complicated task due to the lack of processing power. Therefore, diverse distributed models were developed to ease ring resonators analysis. Nowadays, electromagnetic simulations can be performed in order to easily design such resonator structures.

The interest of using ring resonators as a filter lies on the capacity to easily control the modes of resonance of the ring with the changing of the ring size. The ring resonates when an incident signal wave with sufficient power couples efficiently to the ring at some harmonic frequencies. In this context, the resonator attenuates frequencies other than the specific signal lengths of the resonant harmonic frequencies.

3.1.1 Dual mode ring resonator

Dual mode operation on ring resonator is composed of two degenerate modes or splitting resultant frequencies that may be excited by perturbing stubs, notches, or asymmetrical feed-lines.

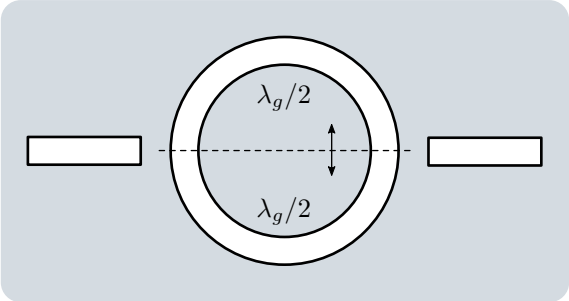


Figure 3.2: Transmission-line model representation of a ring.

For example, suppose the ring can be modeled with two identical transmission lines of size $\lambda/2$ as shown in Figure 3.2. If this ring is excited at the same time and by symmetrical feed-lines, both lines will resonate at the same harmonic frequency, therefore both have the same response. However, if one transmission line is excited differently than the other, or the ring is formed by two different transmission lines, then two different coupled frequency modes exists.

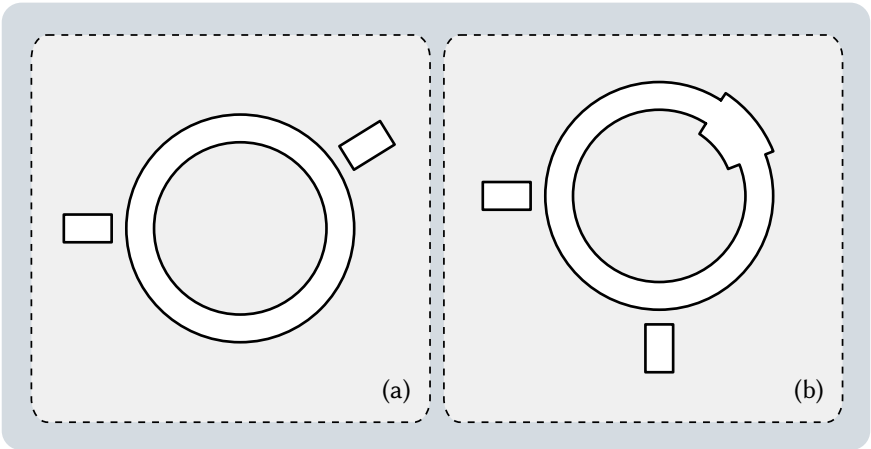


Figure 3.3: Different feed-lines configurations. (a) asymmetric (b) orthogonal feed-line with perturbation.

Utilization of dual mode ring resonator was first introduced by [19] using asymmetric coupling

feed-line. Asymmetric feed-lines can be very difficult to put in an order, on the other hand ring resonator using both orthogonal feed-line and patch perturbation methods demonstrated to be more reliable techniques [20], [21], [22], [23] and [24]. This orthogonal configuration offers a quasi-elliptic function that has two transmission zeroes close to the pass-band. Both asymmetrical and orthogonal feed-lines configuration are illustrated in Figure 3.3.

3.1.2 Ring Filter

Ring resonators have band-pass characteristics, and when connected with proper input and output adaptation network the injected signal can be filtered over the penalty of certain attenuation. Resonator excitation depends on the perturbation used in the ring and the coupling methods.

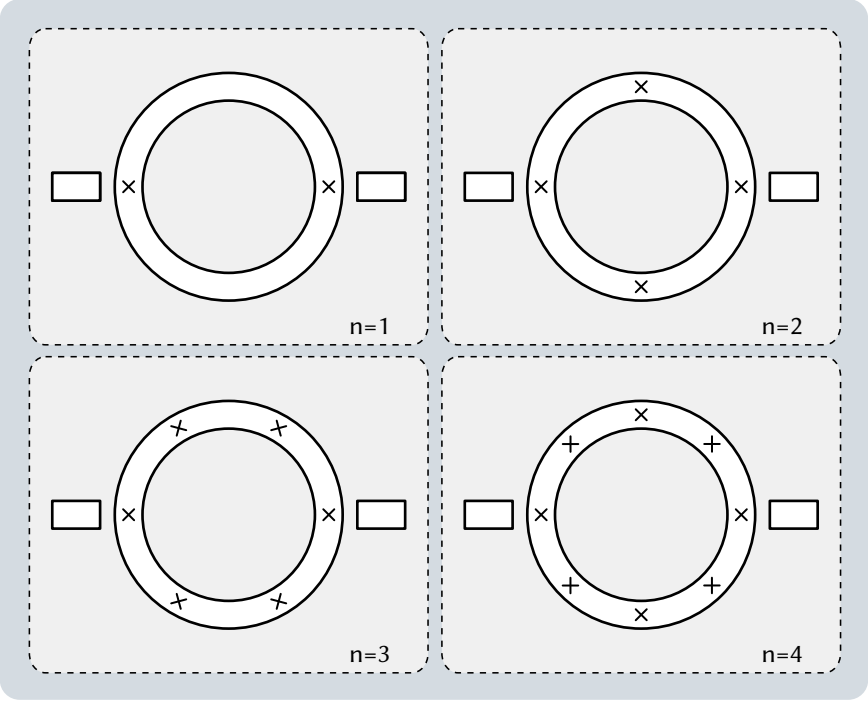


Figure 3.4: Points of maximum field on a generic ring resonator.

Regular resonant modes occur when symmetric (input and output) feed-lines are applied to the ring structure. Figure 3.4 shows the four first modes for a same ring resonator, and the maximum field points are indicated by the crosses. A simple modeling of a ring resonator is a TL formed in a closed loop as shown in Figure 3.2, and the basic circuit consists of

the feed-lines, coupling gaps and the resonator itself. A ring resonator structure can then be expressed by its radius that is related with the resonating modes with a relation that is determined by

$$2\pi r = n\lambda_g, \text{ for } n = \{1, 2, 3, ...\} \tag{3.1}$$

In equation 3.1, r is the mean radius of the ring that is equal the average of the outer and inner radii, λ_g is the guided wavelength, and n is the mode number. Equation 3.1 rules the regular resonant modes of the ring structure. Different resonator modes can be excited with the use of perturbations on the original ring structure as illustrated in 3.5.

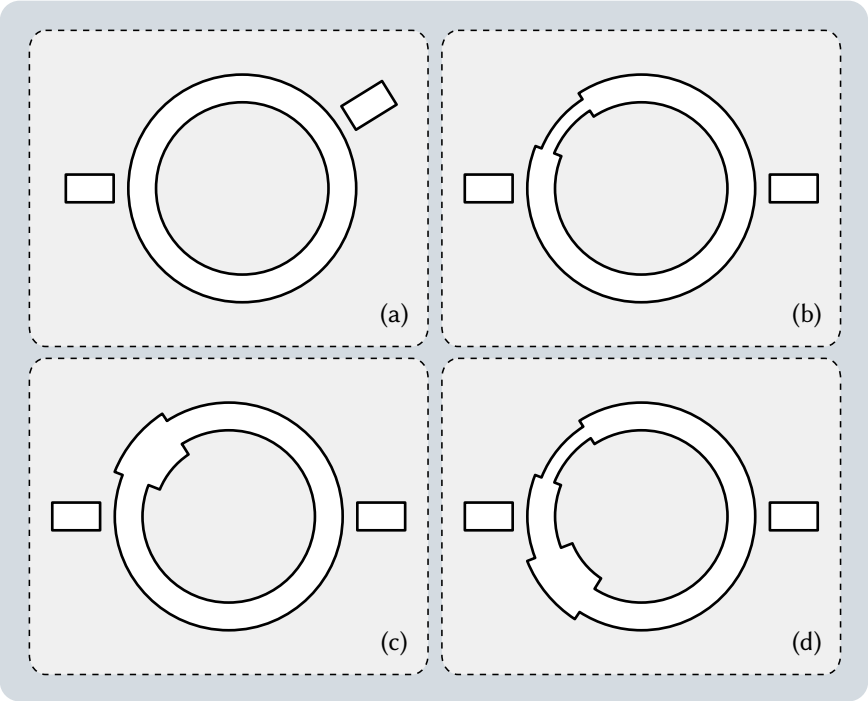


Figure 3.5: Perturbations on a regular ring. (a) Coupled split mode due to asymmetric feed-lines, (b) notch perturbation, (c) patch perturbation and (d) local resonant split node

These perturbations are also called *split resonant modes* because it separates the various modes of interest. Yet from Figure 3.5 they are classified in:

a. Coupled split mode: Generated by asymmetric feed-lines. In this case, the annular angle between feed-lines determines the splitting frequency. It is not an intuitive method and can deliver angular layouts difficult to adapt to design rules.

b. Notch perturbation split mode: Generated with a reduction of width in a section of the ring. This change increases the impedance on section creating a local resonant structure and splits energy of different resonant modes. It can be not appropriated in cases where the width of the annular structure is near design rule bottom boundaries.

c. Patch perturbation split mode: Same as notch perturbation, but here the local structure stores energy of different resonant modes, as a capacitance. In contrast to the last structure, it offers a design possibility when ring width already touches design rules bottom boundaries.

d. Local resonant split mode: Combination of patch and notch perturbation modes.

Another important part of the ring resonator is the feed-line coupling method. Albeit various nomenclatures exist to different coupling methods, it is more convenient to classify as direct coupling and gap coupling. The first happens when feed-line is physically connected to the ring, and the last happens when feed-line is separated from the ring. Coupling gap allows the structure to support only selected frequencies.

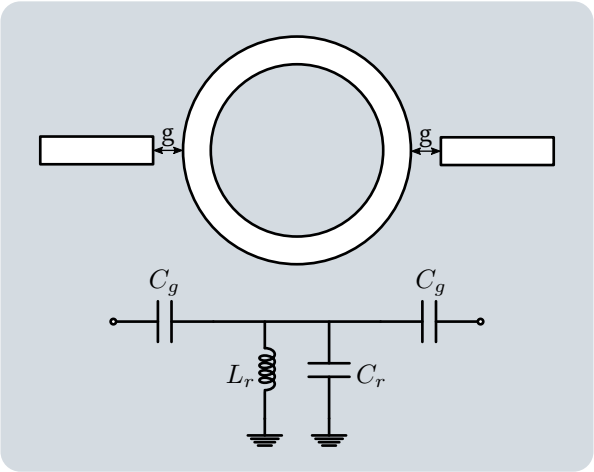


Figure 3.6: Ring resonator equivalent model. Top figure is a two-port resonator connected with gap coupling method to the feed-lines. Below is an equivalent circuit illustrating the gap g as a capacitor C_g, L_r and C_r form an LC network that mimic the ring behavior. This model do not consider the line impedance of the feed-lines.

In Figure 3.6 is shown an equivalent circuit for the ring resonator, where the coupling gap is represented by the capacitors C_g. The size of the coupling gap also affects the performance of resonator. For example with a larger gap less energy is transferred to the ring, therefore

lowering the energy in the resonator field. On the other side, the field on the ring will be more affected when reducing the gap, which can affect filter response. Inspecting the equivalent circuit of Figure 3.6, it is found that S_{21} is given by equation 3.2 as demonstrated in [25].

$$S_{21}|_{\omega=\omega_0} = \frac{2}{2(1+Z_gY) + \frac{Z_g}{Z_0}(2+Z_gY) + YZ_0} \tag{3.2}$$

where

$$\omega_0 = \frac{1}{\sqrt{L_r(C_r+C_g)}} \tag{3.3}$$

$$Z_g = \frac{1}{j\omega_0 C_g} \tag{3.4}$$

$$Y = \frac{j(\omega_0^2 L_r C_r - 1)}{\omega_0 L_r} \tag{3.5}$$

In the model of Figure 3.6 it is seen that the capacitance C_g changes with gap distance g (smaller the g bigger the C_g). Accordingly, Equation 3.4 relates capacitance C_g with S_{21}. Therefore when the value of g decreases, then S_{21} increment. This result is in conformity with our first intuitive assumption. The contrary is also true, if g increase, then C_g decreases and correspondingly S_{21}.

TL models extraction of ring resonators is highly affected by the ability to accurately model the resonator with an equivalent circuit. For example a squared resonator where capacitive accesses are placed at 90° one to other (180° and 270° angles precisely), and with a perturbation (Y_d) at 45°. This ring is modeled using three TL of size $\lambda/4$ and two of size $\lambda/8$ with a perturbation. Albeit these simple assumptions, the equivalent circuit can became quickly untraceable for hand analysis and therefore EM simulation is recommended.

3.2 Filter Resonator state-of-the-art

Ring resonators were first introduced in [26] to measure phase velocity and dispersion characteristics in microstrip lines. During the firsts ten years, most applications were concentrated on measuring the characteristics of discontinuities on microstrip TL. Although sophisticated field analyses were necessary to study the behavior of these structures, distributed models were developed to ease the ring resonators analysis. In the 1980s, applications using ring circuits as antennas, and frequency-selective surfaces emerged. Microwave circuits using rings for filters, oscillators, mixers, baluns, and couplers were also reported. Some unique properties and excellent performances have been demonstrated with the use of ring circuits built in coplanar waveguides and slotlines. Also integration with various solid-state devices was realized to perform tuning, switching, amplification, oscillation, and optoelectronic functions. All this information is better detailed in [25].

The first use of ring resonator as a filter was introduced in [19], when dual mode ring band pass filter study was developed, since then technology evolved and other structures were designed to be used as filters. The influence of gap access in the ring structure and its influence on bandpass filters can be found in [21].

Table 3.1: Comparative of published performances of mm-wave filters.

Paper	Frequency	$Bandwidth_{3dB}$	IL	Surface area	Technology	Year
[27]	60 GHz	50%	−3 dB	–	0.18 µm CMOS	2007
[28]	64 GHz	20%	−4.9 dB	1.71 mm^2	0.18 µm CMOS	2008
[29]	60 GHz	10%	−9.3 dB	–	0.18 µm CMOS	2008
[30]	70 GHz	26%	−3.6 dB	0.44 mm^2	0.18 µm CMOS	2008
[31]	63.5 GHz	38%	−2 dB	–	0.13 µm CMOS	2009
[32]	62 GHz	42%	−2.2 dB	*0.034 mm^2	0.13 µm CMOS	2009
[33]	65.25 GHz	36%	−3.86 dB	*0.076 mm^2	0.18 µm CMOS	2010
[33]	63.5 GHz	28.3%	−4.8 dB	*0.079 mm^2	0.18 µm CMOS	2010
[34]	63 GHz	30%	−3 dB	0.074 mm^2	0.18 µm CMOS	2010

[35]	62 GHz	12%	−2.3 dB	0.49 mm^2	IPD	2010
[34]	60 GHz	20%	−3.1 dB	–	0.18 µm CMOS	2010
[34]	60 GHz	18%	−3.5 dB	–	0.18 µm CMOS	2010
[36]	58 GHz	28%	−3 dB	0.73 mm^2	0.18 µm CMOS	2011
[37]	76 GHz	25%	−4 dB	0.08 mm^2	0.13 µm CMOS	2011
[38]	59 GHz	24.5%	−4.2 dB	0.12 mm^2	90 nm CMOS	2011
[39]	60 GHz	17%	−4.1 dB	0.29 mm^2	0.13 µm CMOS	2012
[40]	60 GHz	30%	−3.5 dB	0.1 mm^2	0.18 µm CMOS	2014
[41]	51 GHz	17.6%	−7.3 dB	0.189 mm^2	0.18 µm CMOS	2014
[42]	60 GHz	33%	−3 dB	0.29 mm^2	0.18 µm CMOS	2014
[43]	61.2 GHz	11.9%	−5 dB	0.32 mm^2	0.25 µm CMOS	2016
[43]	61 GHz	13%	−5.6 dB	0.74 mm^2	0.25 µm CMOS	2016
[44]	59.5 GHz	21.68%	−3.3 dB	0.061 mm^2	0.18 µm CMOS	2017

Asterisks sign (*) marks dimensions without pad.

Integrated filters were recently investigated and great compilation of works up to 2013 can be found in [45], also a list for comparison purposes is given in Table 3.1 containing results of integrated resonator filters published in the last ten years, so it is possible to compare the results of this work with the state of the art. Not all entries are related to ring resonator structures such as [29], [31], [40]. Compact resonator structures can be found in [43], [37], [42] and [44].

3.3 60 GHz resonator filter

The version of ring resonator filter developed in this work is based on [23], [21], [28] and [46], however it uses an octagonal arrangement due to the obligation of fitting with the DRC of the technology, and its shape similarity with a circular ring itself. Its transmission line model is shown in Figure 3.7. The filter is a dual mode ring resonator, and its choice is based on its satisfactory filter response and the simplicity of design. Figure 3.8 illustrates the arrangement

of the circuit resonator and the names of the variables used in the dimensioning of this design.

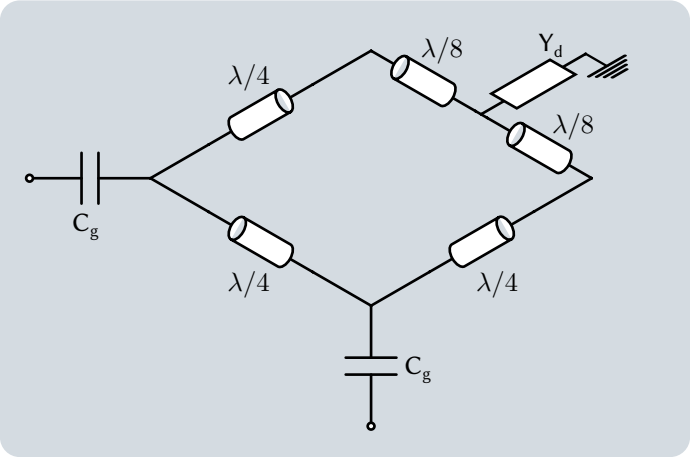


Figure 3.7: Transmission line model of a ring resonator with a perturbation (Y_d).

Each dimension of resonator have an influence on circuit response, diameter $D = 2r \approx \lambda_0/4$ sets the frequency f_0 of the circuit; *w* plays on circuit band (higher *w* implies higher band, limiting band to design rules); *g* affects the filter IL; *d* is the size of perturbation that induces dual mode on ring resonator and adds a higher frequency transmission zero on filter response (also is associated with 90° design), ultimately l_a and w_a are both input/output TL ring adaptation.

Design rules of QuBIC impose the creation of a vertical coupling gap that uses different metal layers in order to couple the feed-lines with the ring. On this technology the minimal distance between two metal-six structures is three micrometers, distance that is not sufficient to good ring coupling (Equation 3.2). Therefore metal-five to metal-six coupling is used as detailed in Figure 3.8. The ring resonator was fully designed in Cadence® Virtuoso® and simulated in Keysight® Momentum® using EM.

A micro-photography of the fabricated circuit is shown in Figure 3.9. The results of simulation and measurements are plotted in Figure 3.10. Circuit layout measures 1180×1180 µm^2 with the pads and 760×760 µm^2 only the ring, filter bandwidth goes from 55 GHz to 66 GHz with attenuation of -4 dB on f_0, and the bandwidth is BW=18 %.

Attention about the timeline of circuits measurements and fabrication. At the time the ring resonator and the first version of LNA filter (with the octagonal resonator) were sent,

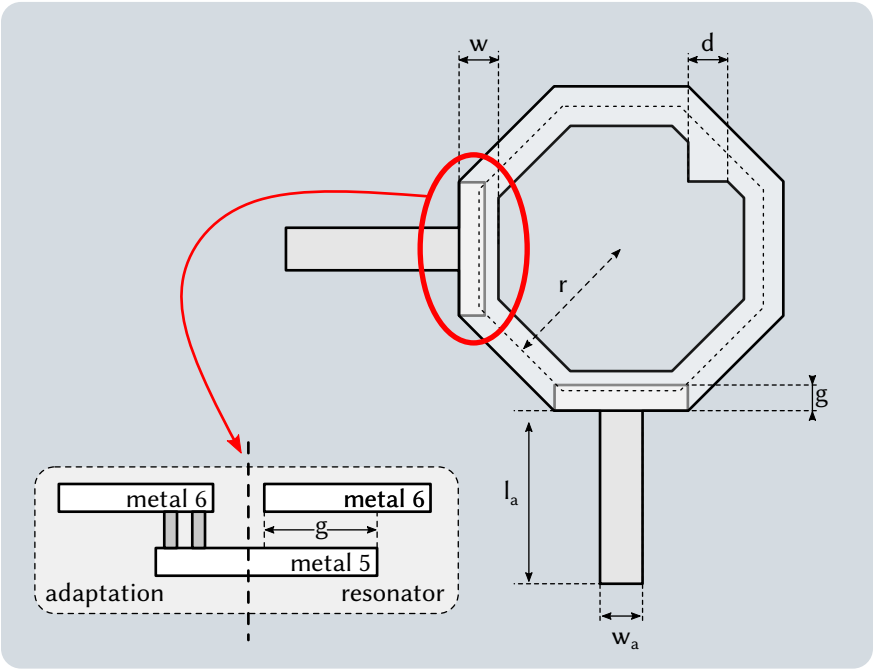


Figure 3.8: Octagonal filter ring resonator design variables.

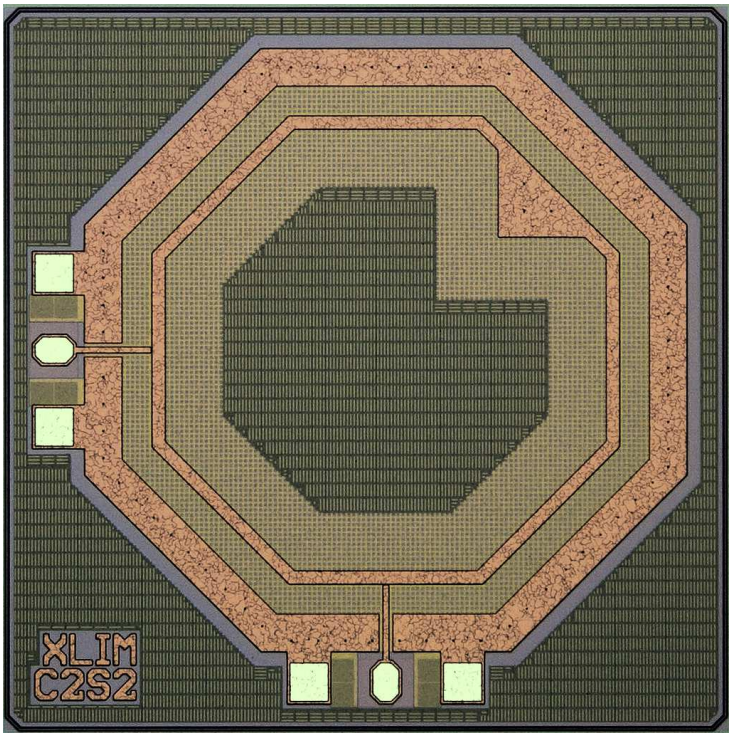


Figure 3.9: Photography of the fabricated 60 GHz ring resonator filter.

the first circuit (LNA) have not arrived and consequently the measurement outcomes were unknown. Therefore it was also unknown if the design workflow used to this design was correct or not. Only after the ring resonator and the Filtering LNA measurements it was possible to

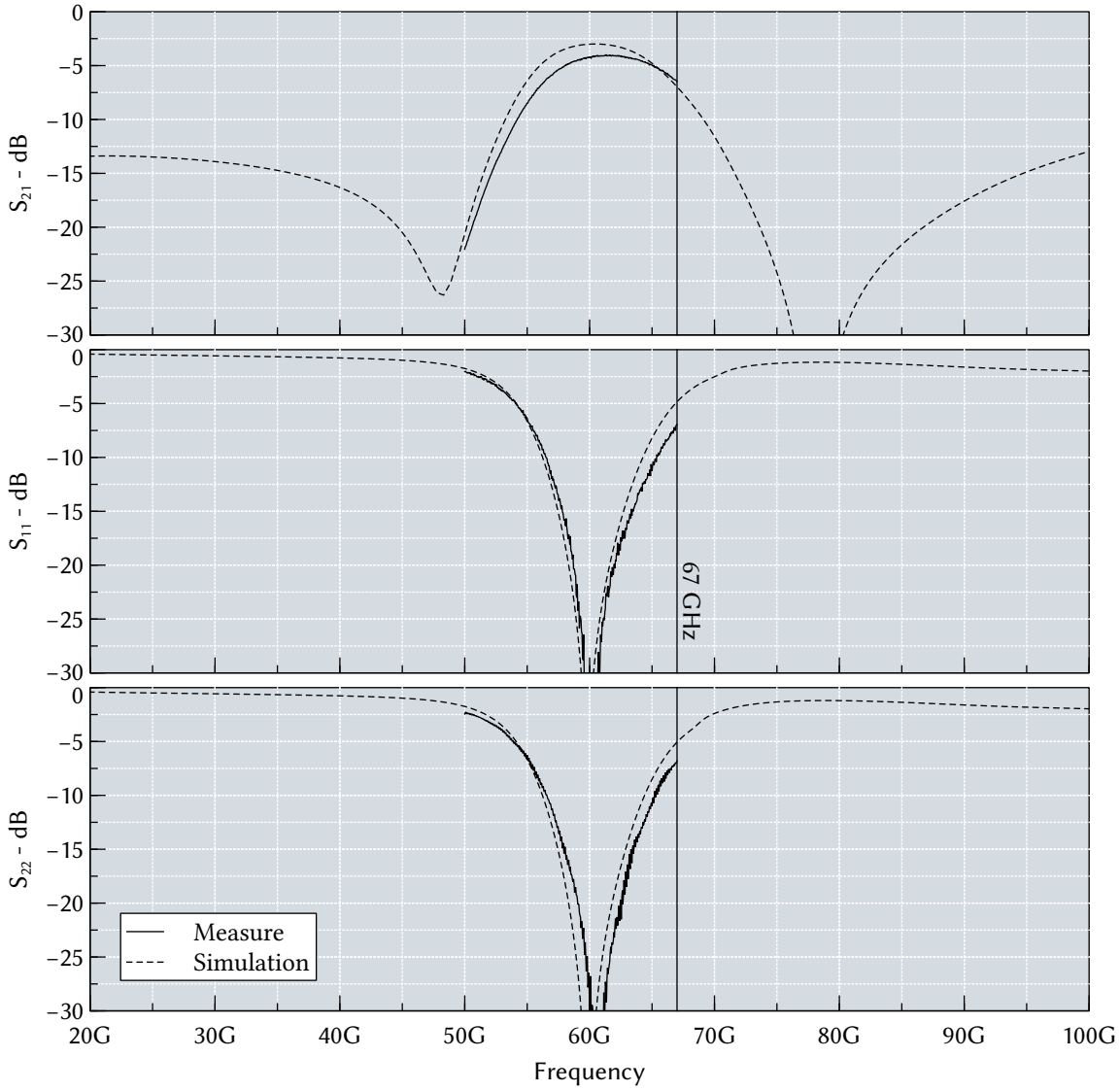


Figure 3.10: Measure and simulation of the octagonal 60 GHz ring resonator filter.

established an algorithmic workflow for mm-wave circuit design.

3.3.1 Meander Loop Ring resonator

A meander loop ring resonator filter is developed in a more compact design when compared with the octagonal version. This structure provides reduction in layout dimensions of almost 60 % (448×448 μm^2 against 760×760 μm^2 in the octagonal version) for the core layout. The full layout (including the pads) happens to have same dimensions of the octagonal ring without pads, 1180×1180 μm^2.

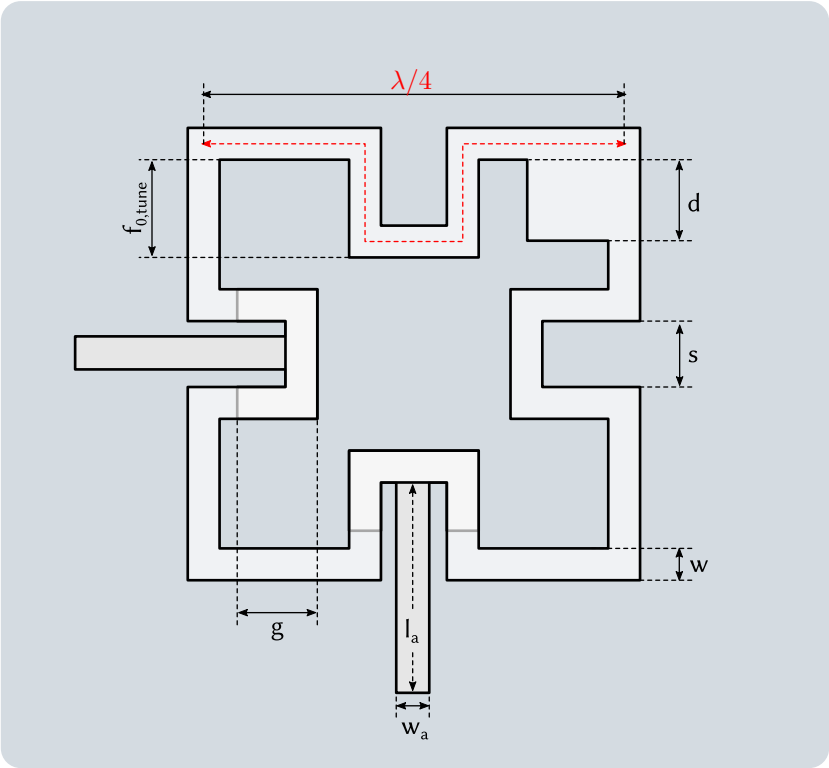


Figure 3.11: Proposed filter ring resonator design variables - version 2.

The reduction in circuit dimensions come with extra complexity in design dimensioning. Albeit this layout is easier to tune in frequency (with $f_{0,tune}$ distance), it is more sensible to variations in filter response due its density. The $f_{0,tune}$ work reducing or increasing the size of side filter dimension, what is proportional with $\lambda/4$ as can be seen in Figure 3.11. Variables d, g, w, l_a and w_a perform the same way here than in the octagonal ring, s must be at last 6 µm (on each side) larger than w_a due NXP® QuBIC layout rules constraints (metal-five to metal-five minimal distance). Same coupling technique is used in this second version, with use of metal-five and metal-six forming the coupling gap capacitance. The measurements were performed in the same testbench of the octogonal filter so the results can be directly compared. Simulated and measured results are shown in figure 3.12.

As a design procedure it is recommended first to find λ for the wanted central frequency f_0, and draw a single side of $\lambda/4$ long with s and $f_{0,tune}$ distances according to design rules; then copy the design to form the four sides. Second draw the patch perturbation with a random value for d and put the accesses, then run EM simulation. After read the results, increase d

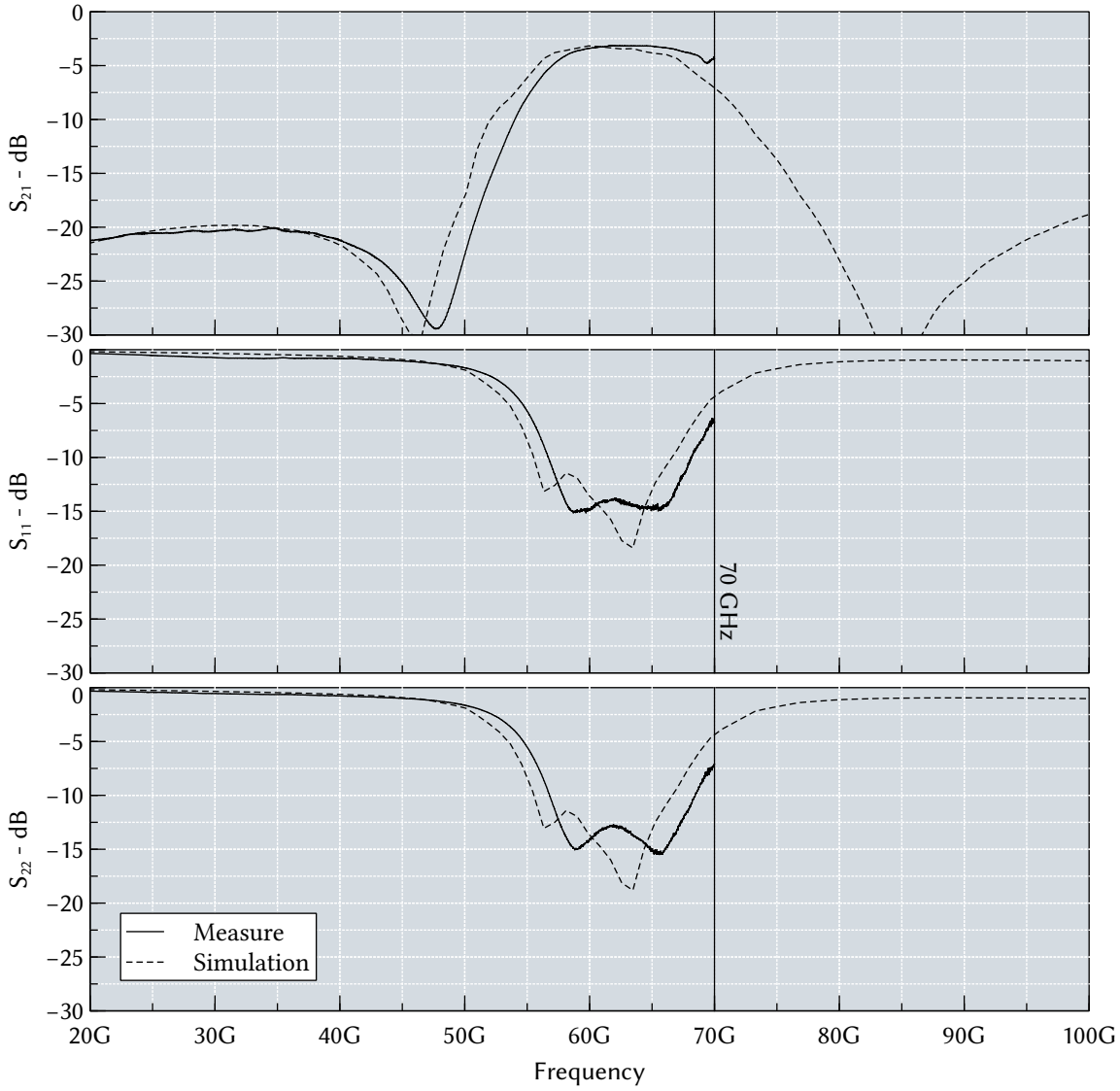


Figure 3.12: Measure and simulation of new version of 60 GHz ring resonator filter - version 2.

if needed, reduce $f_{0,tune}$ if central frequency is higher than f_0, reduce otherwise. For last, to set the bandwidth the w variable is used to influence the width of the ring, and finally the matching network can be changed as needed (for adaptation).

In the Figure 3.13 is presented the micro-photography of the fabricated meander filter, the layout circuit have 760×760 µm^2 without pads, filter bandwidth goes from 55 GHz to 68 GHz with attenuation of −3 dB on f_0=60 GHz, and its the bandwidth is BW=21 %.

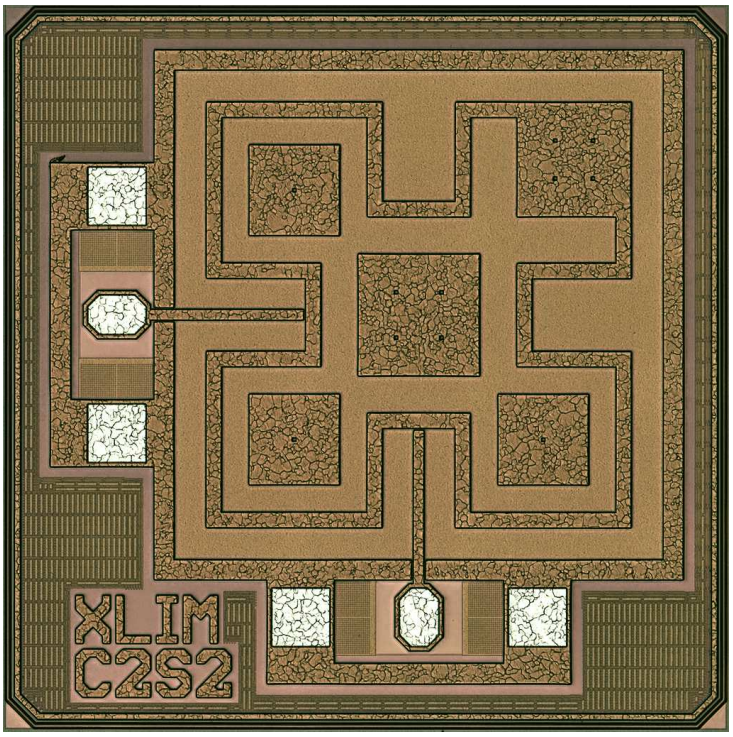


Figure 3.13: Photography of the second version of fabricated 60 GHz ring resonator filter.

3.4 Discussion

Two designs of ring resonator filters were developed and its operation is demonstrated. Both filter structures were separatelly designed as a proof-of-concept and are intended to be used as a blackboxed cell for future circuits as a filtering amplifier.

A significant reduction in the dimension of the filter was noted between the two versions (approximately 60 % on the core design) and with low difference on measured and simulated S-parameters (as can be seen in Figure 3.10 and Figure 3.12). The coupling between the ring and its feed-lines was designed on two different metal layers (Figure 3.8), one alternative would be to use Metal-Insulator-Metal (MIM) layers in order to increase coupling capacitance.

In both designs floating metals stacks were introduced so the designs could respect DRC step. These structures can be seen in Figure 3.9 at the centre of the ring resonator, and in Figure 3.13 as floating squares inside the meander filter. These floating networks have no influence with the results, as stated during exhaustive electromagnetic simulations and confirmed after with the measurements.

A review in the state-of-the-art for resonator filters fabricated in silicon is summarized in Table 3.1, and is used for comparison purposes with the designed structures. The result of simulation and measurements are presented in Table 3.2 for both structures. Also we present Figure 3.14 in order to better compare the IL and bandwidth with the state of the art filters with various different topologies and technologies.

Table 3.2: Ring resonators results.

	Frequency	$Bandwidth_{3dB}$	IL	Surface area	Technology	Year
Octagonal	60 GHz	18%	−4 dB	0.57 mm^2	0.25 µm CMOS	2018
Meander	60 GHz	21%	−3 dB	0.20 mm^2	0.25 µm CMOS	2018

These results place this work side-by-side on the state-of-the-art due both its IL and bandwidth. Furthermore, both designs were tested in a co-design circuit environment and the performed well.

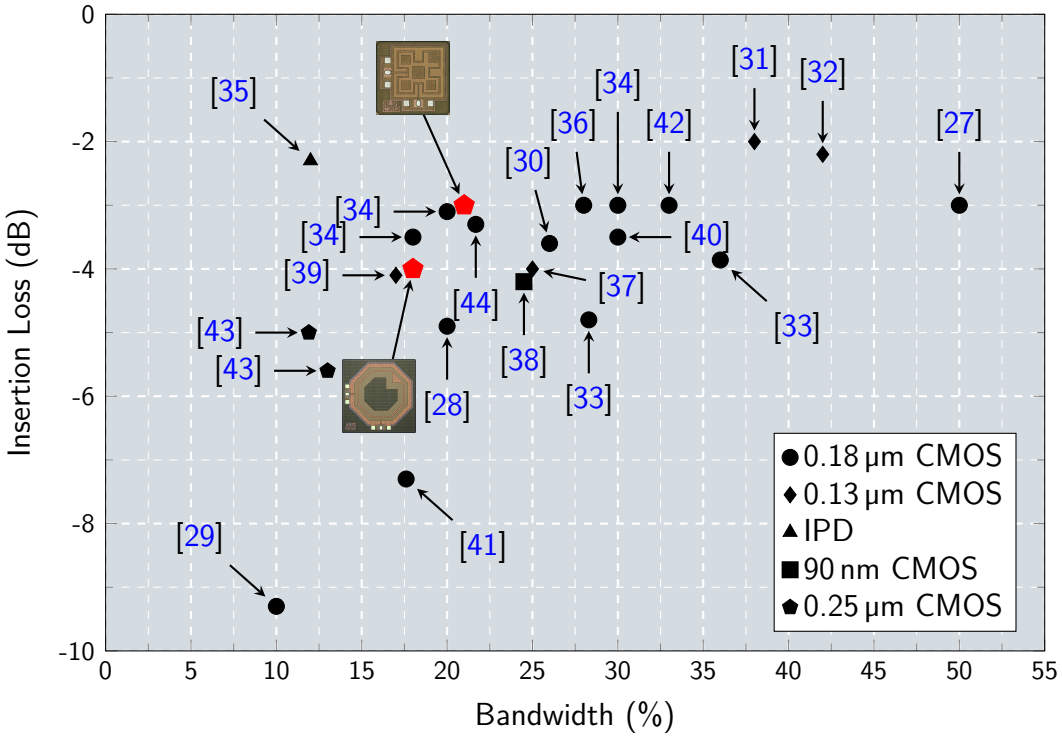


Figure 3.14: Comparison chart of state-of-the-art designs due to IL and bandwidth with the two fabricated designs developed in this work.

Model extraction of circuits was performed in Cadence® Virtuoso® and Keysight® Momentum®, and attention had to be given such as the simulation time do not become impractical due the characterization of EM simulation. All measurements were performed at XLIM in waffle using Cascade Microtech® RF probes connected on a Keysight® PNA-X Microwave Network Analyzer (model N5247A), with commercial up frequency limit of 67 GHz.

Chapter 4

A piece on LNA design fundamentals and state-of-art for mm-Wave

ALL radio receiver system have as main goal to decode the information from a received signal and deliver its information to the next stage. However the output of the transmission channel is normally a corrupted version of the transmitted signal that traveled thoroughout many sources of interference (multipath, co-channel interference, thermal noise. Even the air molecules can become source of interference). One way to eliminate all these spurious signals is to eliminate its sources, task virtually impossible for a system designer.

The other way is to try to amplify only the signal so increasing the Signal-to-Noise Power Ratio (SNR) and granting that the next stages operations be successful. Next, in a *superheterodyne* receiver, before that the received signal can be decoded it needs still to be shifted in frequency. All this signal computation on the receiver system (the amplification and frequency shifting) are performed on its RF stage (Figure 4.1). Essentially the full set of receiver topologies includes the LNA as the first block after the antenna[1].

Friis formula for noise (equation 4.1) indicates that for the RF part using the amplifier as an input system block is the best approach since noise of the first element on a cascade system is dominant. Thereby, a LNA must be conceived to offer a maximal signal gain, and minimum noise, maximizing the signal-to-noise ratio. So accordingly with equation 4.1, the other elements placed after the LNA see their noise contribution divided by the gain of the

[1]Here we make a parenthesis for the Mitola's software defined radio, that is basically a cascaded antenna and an A/D converter connected on a microprocessor.

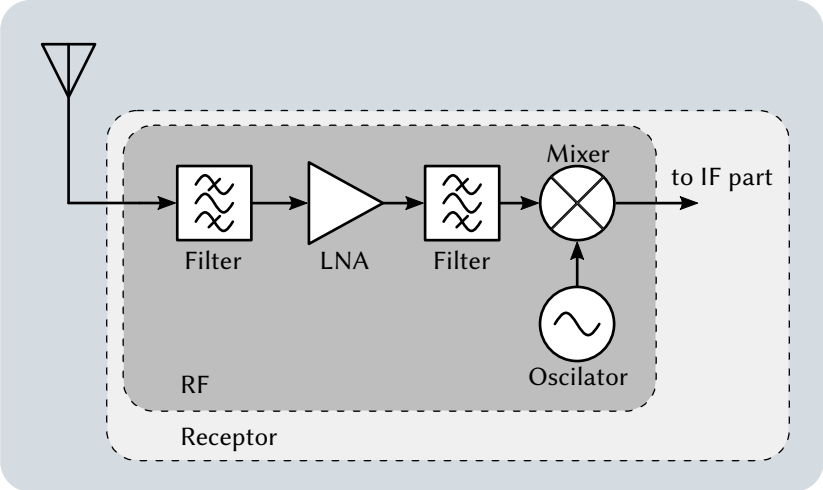


Figure 4.1: Block diagram of the RF stage of the receiver.

preceding stage.

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \cdots + \frac{F_n - 1}{G_1 G_2 \cdots G_{n-1}} \tag{4.1}$$

So one can think that the next logical step is to find an amplifier topology that fits on this corollary, except that many other specifications (linearity, dimension, adaptation, etc...) are necessary and depends on the system, some of which are intrinsic to the transistor. Therefore the choice of the transistor is an important step during design.

4.1 Designing for low noise

This section gives the mathematical background of Noise Figure (NF) and maximum gain (G_{MAX}), two important figure of merit for the low noise RF circuits design. Moreover, the design procedure to grant the optimal choice of the LNA transistor. It is important to know that the NF and Gain are variables dependent of transistor architecture; hence, different NF can be delivered by two transistors of the same area and polarization due different design.

4.1.1 Two-port noise figure

Noise Factor (F) is defined as the Signal-to-Noise Power Ratio of the input signal over the Signal-to-Noise Power Ratio of the output signal when the transistor (here seen as a *two-port device*) is connected to matched sources at standard noise temperature (usually T_0=290 K), as shown:

$$F \triangleq \left(\frac{SNR_I}{SNR_O}\right) \tag{4.2}$$

following the NF is defined as F in dB, as shown in equation 4.3.

$$NF = 10\log(F). \tag{4.3}$$

In order to simplify the noise analysis for a given circuit, it is assumed that the total noise generated by the circuit can be reduced to the noise sources placed at the input of the noiseless two-port device (Figure 4.2), now seen as a cascaded noiseless device with a noisy circuit source and modeled on its ABCD matrix form.

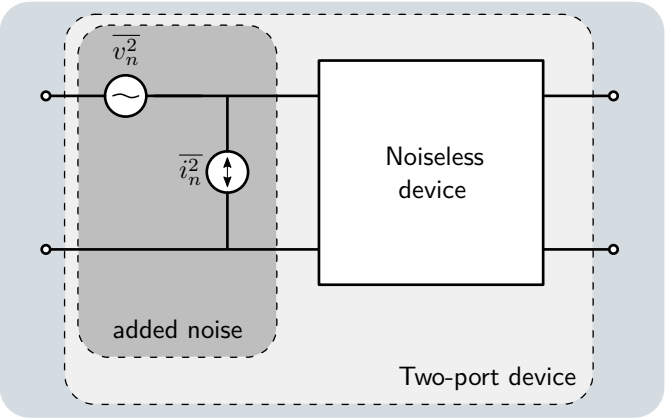


Figure 4.2: ABCD representation of a noisy two-port as a noiseless device and its noise sources components.

Using matrix notation we can describe Figure 4.2 as

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} + \begin{bmatrix} v_n \\ i_n \end{bmatrix} \tag{4.4}$$

were V_1 and I_1 are the voltage and current input referred, V_2 and I_2 output referred, and v_n and i_n referent to added noise sources. The equation 4.4 assumes that the noise sources are uncorrelated, so $\rho(v_n, i_n^*) = \rho(i_n, v_n^*) = 0$. In the case wich noise sources are correlated, its correlation matrix is defined (equation 4.5).

$$[C_A] = \begin{bmatrix} \rho(v_n, v_n^*) & \rho(v_n, i_n^*) \\ \rho(i_n, v_n^*) & \rho(i_n, i_n^*) \end{bmatrix} \tag{4.5}$$

This is an interesting approach because it provides a good understanding about the produced noise with easy algebraic manipulation for circuit noise analysis, because is possible to isolate the added noise from the noiseless two-port device itself. Additionally, it is also possible to describe F with other matrix circuit representations, what leads to more algebraically complicated developments.

Noise figure derivation

As defined in the equation 4.3 the noise factor is found by calculating the noise power in the load Z_L due the noise delivered by the source (v_{ns}) alone, and the noise power in the load due the noise delivered by both, the source (v_{ns}) and the internal (v_n and i_n) noise source. However, since the description of the circuit uses an ABCD matricx, this derivation can be further simplified if the short-circuit noise current i_{sc} is calculated (Figure 4.3). Also it is assumed that the noiseless two-port will not modify the signal-to-noise ratio in this configuration and due its properties we can omit it from analysis.

Noise factor is then seen as the total noise power at the input of the noiseless two-port $i_n$plus i_n over the noise power delivered by the source i_s. Assuming that the noise sources are correlated (as in an HBT), we want to define the correlation between i_n and v_n as the first correlated to the second. Therefore, if

$$i_n = i_{nu} + i_{nc} \tag{4.6}$$

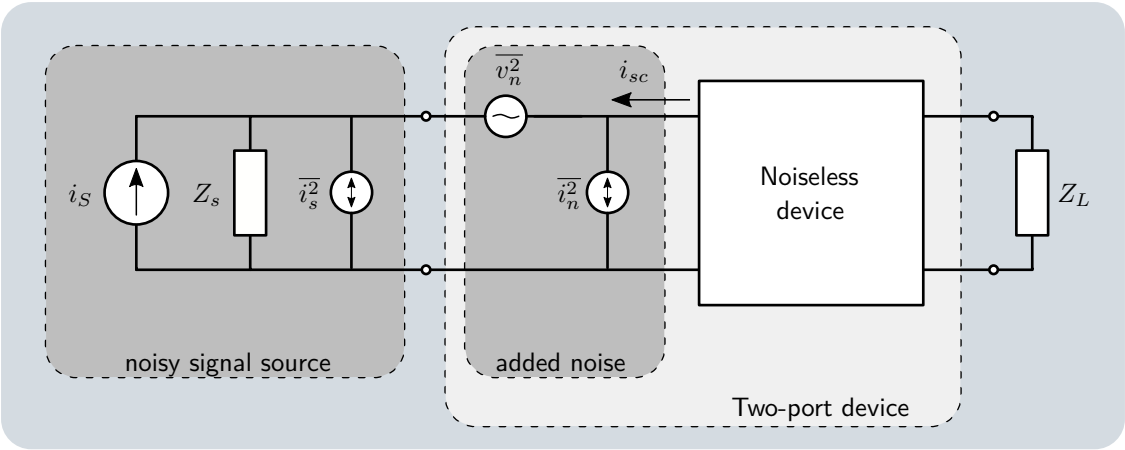


Figure 4.3: Representation of noise sources presents in a system for the noise factor calculation.

where i_{nc} and i_{nu} relates to the correlated and uncorrelated part respectively, and their correlation is given by

$$i_{nc} \triangleq Y_\rho v_n \tag{4.7}$$

where Y_ρ as a complex admittance value; and substituting 4.7 in 4.6

$$i_n = i_{nu} + Y_\rho v_n \tag{4.8}$$

it is found that $i_{sc,tot}$ and $i_{sc,src}$ are

$$i_{sc,tot} = i_s + i_{nu} + (Y_\rho + Y_s)v_n \tag{4.9}$$

$$i_{sc,src} = i_s \tag{4.10}$$

and finally the noise factor is given as

$$F = \frac{\overline{i_{sc,tot}^2}}{\overline{i_{sc,src}^2}} = 1 + \frac{\overline{i_{nu}^2}}{\overline{i_s^2}} + \frac{\overline{v_n^2}|Y_s + Y_\rho|^2}{\overline{i_s^2}} \tag{4.11}$$

In noise theory each resistive component act like a thermal noise source defined by it's

power density [47],[48],[49]:

$$\overline{v_n^2} = 4\mathrm{k}R_n\Delta f \tag{4.12}$$

$$\overline{i_n^2} = 4\mathrm{k}G_n\Delta f \tag{4.13}$$

where k is the Boltzmann constant, Δf if the frequency band of noise (needed for integration for total noise in band) and R_n and G_n that are the noise characteristic resistance and admittance, respectively. Purely complex components (capacitance and inductance) do not contribute to noise, but can confine the noise band.

So, continuing with the analysis, using equations 4.12 and 4.13 in equation 4.11 leads to the noise factor as a function of the noise resistance, noise conductance and noise correlation admittance of two-port device

$$F = 1 + \frac{G_{nu}}{G_s} + \frac{R_n|Y_s + Y_\rho|^2}{G_s} \tag{4.14}$$

and for uncorrelated noise sources, the equation 4.7 reduces to $i_n = i_{nu}$, and therefore

$$F = 1 + \frac{\overline{i_n^2} + \overline{v_n^2}|Y_s|^2}{4kG_s\Delta f} \tag{4.15}$$

From equations 4.14 and 4.15 is possible to deduce that noise depends directly of the input resistance R_n of the two-port, and of the source impedance Y_s. To find the minimal value of noise for a given two-port circuit we differentiate equation 4.14 with respect of G_s and B_s, to find its minimum value.

$$G_{s,opt} = \sqrt{G_\rho^2 + \frac{G_{nu}}{R_n}} \tag{4.16}$$

$$B_{s,opt} = -B_\rho \tag{4.17}$$

and accordingly

$$F_{MIN} = 1 + 2R_n(G_\rho + G_{s,opt}) \tag{4.18}$$

where $Y_\rho = G_\rho + jB_\rho$ and $Y_{s,opt} = G_{s,opt} + jB_{s,opt}$. These three parameters F_{MIN}, R_n and Y_{sOPT} represents all noise presented at the output of the two-port. The equation 4.14 for the noise figure can now be reintroduces as a function of the three noise parameters

$$F = F_{MIN} + \frac{R_n}{G_s}|Y_s - Y_{s,opt}|^2 \tag{4.19}$$

Equation 4.19 shows that the noise factor is highly dependent of R_n, we can think about R_n as an indicator of the sensitivity of the noise figure to noise impedance mismatch in a given frequency. Yet if we express the admittances Y_s and $Y_{s,opt}$ in terms of reflection coefficients

$$\Gamma_s = \frac{1 - Y_s}{1 + Y_s} \tag{4.20}$$

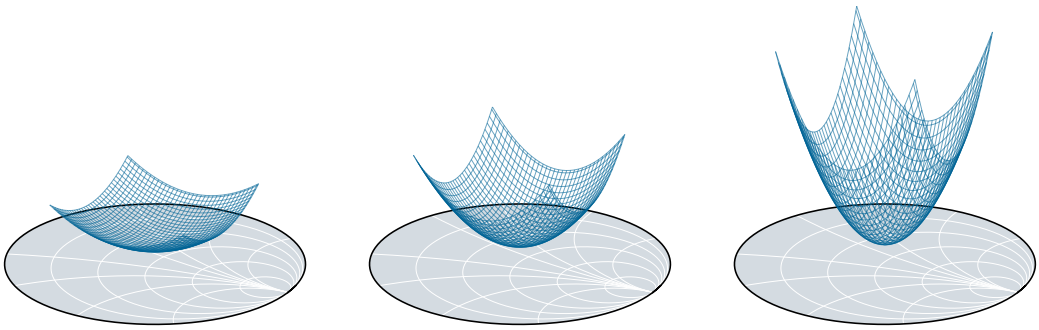
$$\Gamma_{s,opt} = \frac{1 - Y_{s,opt}}{1 + Y_{s,opt}} \tag{4.21}$$

then the equation 4.19 can be rewrite (equation 4.22) and so it is possible to represent the noise-figure in a smithchart.

$$F = F_{MIN} + 4R_n\frac{|\Gamma_s - \Gamma_{s,opt}|^2}{|1 + \Gamma_{s,opt}|^2(1 - |\Gamma_s|^2)} \tag{4.22}$$

Throughout this development (leading to equation 4.19) it is seen that large values of R_n implies that the two-port noise factor will be very sensitive to variations in the value of the source impedance, and vice-versa. Figure 4.4 shows a representation of the R_n influence on the F sensibility, where the F is draw as a function of impedance mismatch, and $R_n = (0.5,\ 1,\ 2)$.

Yet the choice of the transistor must be not only guided by R_n but also by adaptation mismatch because $F = F_{MIN}$ when $Y = Y^*_{s,opt}$. Another factor that will heavily influence the choice of the transistor is linearity, that is after all, an actually limit that is driven by the specification of the general system.



(a) $R_n = 0.5$ (b) $R_n = 1$ (c) $R_n = 2$

Figure 4.4: Variations of R_n values indicating its implication over the noise factor in a two-port device for fixed values of F_{MIN} and $Y_{s,opt}$.

4.1.2 Noise and Gain circles

Now that noise-figure can be easily with equations 4.19 and 4.22 it would interesting during the design specifying the distance between NF and the minimal NF for a given transistor, this distance can be obtained with noise circles. The use of noise circles as a design tool allows to choose the transistor with the minimal distance between NF and minimal NF, indicating that the best transistor is also the easiest to adapt.

To obtain the noise circle for a given transisor, we first fix F and define

$$N = \frac{F - F_{MIN}}{4R_n}|1 + \Gamma_{s,opt}|^2 \tag{4.23}$$

this way the equation 4.19 simplifies to

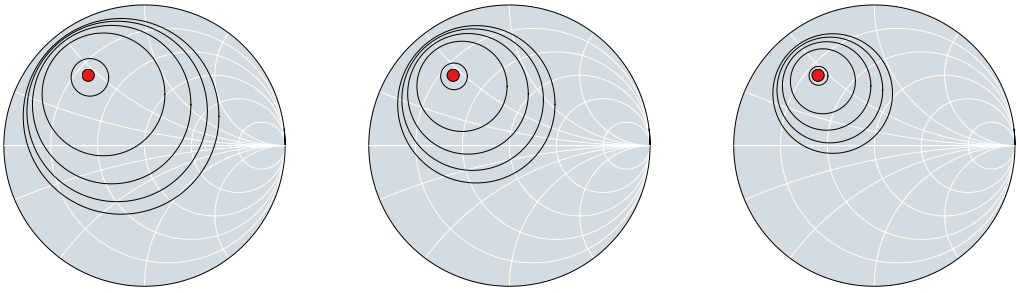
$$N = \frac{|\Gamma_{s,opt} - \Gamma_s|^2}{1 - |\Gamma_s|^2} \tag{4.24}$$

what is then developed to

$$\left|\Gamma_S - \frac{\Gamma_{s,opt}}{N+1}\right| = \frac{\sqrt{N(N+1-|\Gamma_{s,opt}|^2)}}{N+1} \tag{4.25}$$

that is a circle centered at $\Gamma_{s,opt}/(N+1)$, with radius given by the right hand side of the equation. Note that, as expected, the optimum noise figure is a point centered at $\Gamma_{s,opt}$ with

radius zero ($N = 0$). Figure 4.5 is a plot of noise circles for a given two-port circuit with fixed values of noise-factor. Noise circles can be actually defined as a two-dimensional representation of Figure 4.4.



(a) $R_n = 0.5$ (b) $R_n = 1$ (c) $R_n = 2$

Figure 4.5: Influence of R_n in noise circles for fixed values of F_{MIN} and $Y_{s,opt}$ (in red). Each circle represents 1 dB, the inner circle represents F_{MIN}.

Although for the LNA the minimal noise figure is virtually the most important specification during the design, it is still important to maximize the gain of the amplifier. Considering that in an amplifier network the input (Z_{in}) and output (Z_{out}) impedance is hardly the same as the source (Z_s) and load (Z_L), it is imperative the addition of matching networks to adapt the circuit, as in Figure 4.6, where optimal adaptation is given for $\Gamma_s = \Gamma_{in}^*$, and $\Gamma_L = \Gamma_{out}^*$.

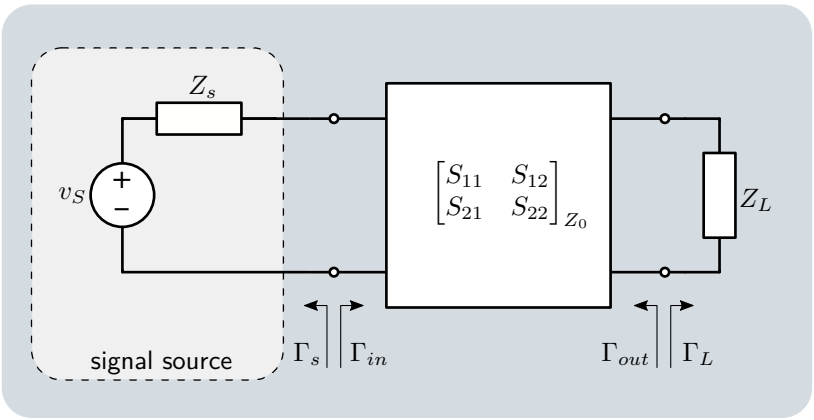


Figure 4.6: Two-port device adaptation.

Therefore, for the gain, we first define the *transducer gain* (G_T) and *available power gain* (G_A)

$$G_T = \frac{P_l}{P_s} = \frac{\text{power delivered to the load}}{\text{power available from the source}} \tag{4.26}$$

$$G_A = \frac{P_{l,max}}{P_{s,max}} = \frac{\text{power available from the two-port}}{\text{power available from the source}} \tag{4.27}$$

also assuming that $|S_{12}| = 0$, the transducer gain expression is simplified to the *unilateral transducer gain* and so in terms of reflection waves it is set as

$$G_T = \overbrace{\frac{1-|\Gamma_s|^2}{|1-S_{11}\Gamma_s|^2}}^{\substack{\text{gain term} \\ \text{associated with} \\ \text{input match}}} |S_{21}|^2 \overbrace{\frac{1-|\Gamma_L|^2}{1-|S_{22}\Gamma_L|^2}}^{\substack{\text{gain term} \\ \text{associated with} \\ \text{output match}}} \tag{4.28}$$

$$= G_s(G_0)G_L \tag{4.29}$$

where $G_0 = |S_{21}|^2$, and $G_s(G_0)G_L$ are the three independent terms of the total unilateral gain, and since the isolation is perfect they have no influence on each other.

Assuming that the load is well matched ($\Gamma_L = \Gamma^*_{out}$), then $G_T = G_A$ and equation 4.28 is rewritten as

$$G_A = \frac{1-|\Gamma_s|^2}{|1-S_{11}\Gamma_s|^2}|S_{21}|^2\frac{1}{1-|S_{22}|^2} \tag{4.30}$$

what eliminates Γ_L dependency in the equation.

Because the noise depends on the input match network (mainly on the source), the input is often mismatched to obtain the best noise figure at the expense of gain. Therefore in design terms, during a LNA design first the input match is performed in order to minimize added noise, then the gain is optimized with the match between the output of two-port with the conjugated load.

Equation 4.30 have the first term still dependent on the input match (S_{11}) because actual power absorbed in the input is not necessarily the same power delivered by source, and depends on the input adaptation network. In such case that input is also adapted, then

$G_A = G_{A,max} = G_{T,max}$, and the equation 4.30 is now given by

$$G_A = \frac{1}{1-|S_{11}|^2}|S_{21}|^2\frac{1}{1-|S_{22}|^2} \tag{4.31}$$

From equations 4.28 and 4.31 it can be said that

$$G_{T,s} = \frac{1-|\Gamma_s|^2}{|1-S_{11}\Gamma_s|^2} \tag{4.32}$$

$$G_{T,L} = \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \tag{4.33}$$

and since it is assumed that $G_{A,s} = G_{T,s,max}$, so

$$G_{A,s} = G_{T,s,max} = \frac{1}{1-|S_{11}|^2} \tag{4.34}$$

$$G_{A,L} = G_{T,L,max} = \frac{1}{1-|S_{22}|^2} \tag{4.35}$$

and setting

$$g_s = \frac{G_s}{G_{s,max}} = \frac{1-|\Gamma_s|^2}{|1-S_{11}\Gamma_s|^2}(1-|S_{11}|^2) \tag{4.36}$$

$$g_L = \frac{G_L}{G_{L,max}} = \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2}(1-|S_{22}|^2) \tag{4.37}$$

for both $0 \leq g_s \leq 1$ and $0 \leq g_L \leq 1$. Then, in order to set g_s (or g_L) equal to a constant and solve that values of Γ_s, we let

$$\Gamma_s = U_s + jV_s \qquad\qquad S_{11} = A_{11} + jB_{11} \tag{4.38}$$

and after some manipulation we obtain the equation for gain circles

$$\left[U_s - \frac{g_s A_{11}}{1-|S_{11}|^2(1-g_s)}\right]^2 + \left[V_s + \frac{g_s B_{11}}{1-|S_{11}|^2(1-g_s)}\right]^2$$

$$= \left[\frac{\sqrt{1-g_s}(1-|S_{11}|^2)}{1-|S_{11}|^2(1-g_s)}\right]^2 \tag{4.39}$$

Equation 4.39 gives a family of circles defined with g_s as a parameter. The circles of radii

$$R_s = \frac{\sqrt{1-g_s}(1-|S_{11}|^2)}{1-|S_{11}|^2(1-g_s)} \tag{4.40}$$

are centered in the real and imaginary part of Γ_s, given by

$$U_s = \frac{g_s A_{11}}{1-|S_{11}|^2(1-g_s)} \tag{4.41}$$

and

$$V_s = \frac{-g_s B_{11}}{1-|S_{11}|^2(1-g_s)} \tag{4.42}$$

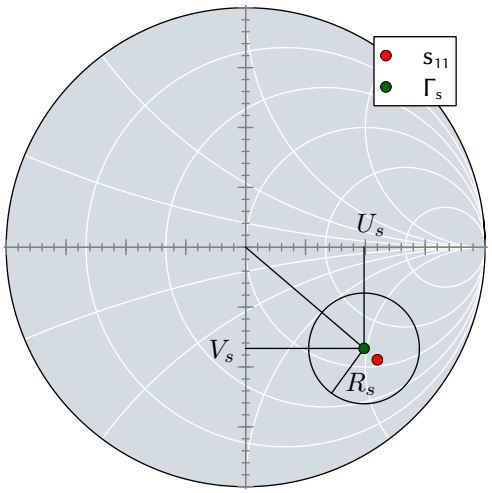


Figure 4.7: Creation of constant-gain circles in the Smith chart.

With the equations 4.40, 4.41 and 4.42 the noise circles from a given amplifier of input s-parameter S_{11}, can be plotted, for example, as follows:

1. First locate S_{11} in the smith-chart and draw a line from the origin to S_{11}, the maximum gain $G_{s,max}$ is delivered when $\Gamma_s = S_{11}^*$. This will be a guideline to the Γ_s different values of the circuit adaptation.

2. Determine the values of G_s for one wanted constant-gain circle, normally G_s is specified as a difference in dB from $G_{s,max}$. So, for example, if a circle of X dB less than $G_{s,max}$ is wanted, then (from equation 4.36)

$$\begin{aligned} g_s &= \frac{G_s}{G_{s,max}} \\ &= \frac{G_{s,max} - X_{dB}}{G_{s,max}} \\ &= 1 - \frac{10^{\frac{X}{10}}}{G_{s,max}} \end{aligned} \tag{4.43}$$

3. Using equations for the constant-gain circles (4.40, 4.41 and 4.42), we find the center of the gain-circles on Γ_s and the radii for each circle for different values of X. On the Table 4.1 (and Figure 4.8) is displayed different Γ_s values for different X values.

Table 4.1: Gain-circles $\Gamma_s = U_s + jV_s$ values for $S_{11} = 0.55 + j0.47$.

$X = G_{s,max} - G_s$	0.4 (dB)	0.8 (dB)	1.2 (dB)	1.6 (dB)
U_s	0.361	0.335	0.304	0.267
V_s	0.308	0.286	0.260	0.228

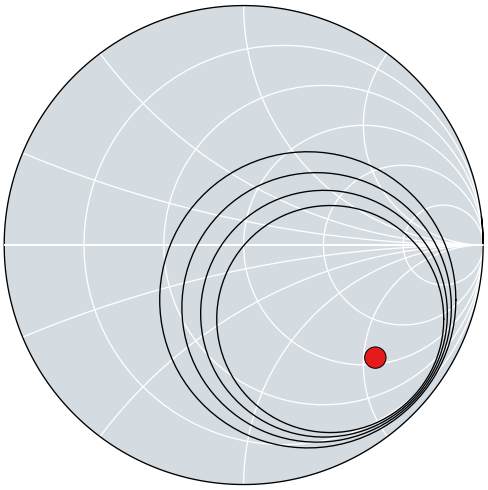


Figure 4.8: Gain-circles $\Gamma_s = U_s + jV_s$ values for $S_{11} = 0.55 + j0.47$. Referent to Table 4.1.

4.2 LNA Topologies

Three topological configurations of amplifiers are preferred for a LNA design: Common Emitter (CE), Common Base (CB) – both using single-transistors by stage, and Cascode. Others LNA configurations are versions of circuits that uses one of these three. For example using multiple stages, differential stages and/or current reuse[2]. Table 5.1 shown a comparison table with the main characteristics for each LNA structure topologies.

The most used single-transistor topology is the common-emitter configuration. In low frequencies this configuration can offer good gain and low noise on silicon substrate (even with MOS transistors, what can be an advantage for mixed-signal design), with low power consumption. However, work with high frequencies is quite difficult not only because the gain decreases when frequency raises, but also because noise increased. Caution have to be taken during layout design in order to understand the impact of each component of circuit on noise figure.

[2]Current reuse is a term with large meaning in literature. One can say, for example that a cascode take advantage of current reuse.

Table 4.2: Amplifier topologies review.

Characteristic	Common-Source	Common-Gate	Cascode
Noise Figure	Lowest	Rises rapidly with frequency	Slightly higher than CS
Gain	Moderate	Lowest	Highest
Linearity	Moderate	High	Potentially Highest
Bandwidth	Narrow	Fairly broad	Broad
Stability	Often requires compensation	Higher	Higher
Reverse Isolation	Low	High	High
Sensitivity to process variation, temperature, power supply, Component tolerance	High	Low	Low

* Table adapted from [50]

Good compromise between gain, noise and adaptation can be achieved with cascode topology. This configuration allows an easier output adaptation than the CE thoroughout a CB transistor that is connected in cascade, increasing the value of r_O in the assembled cascode stage.

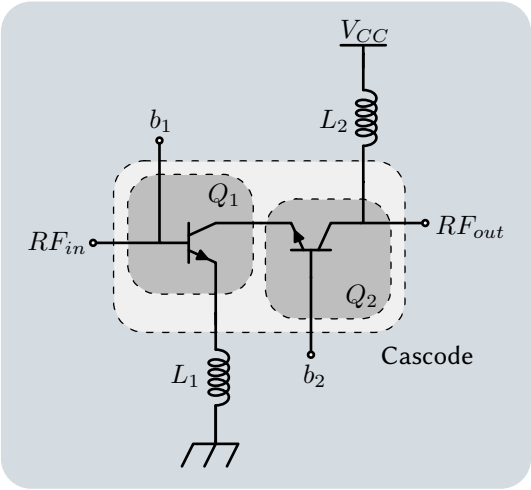


Figure 4.9: Cascode circuit with degeneration and tuning inductance.

In Figure 4.9 is presented the circuit representation of cascode topology, where Q_1 and Q_2 are respectively the CE and CB transistors (here presented with bipolar transistor symbol

diagram). Inductances shown in this circuit works as degeneration network (L_1) and frequency tuner (L_2), b_1 and b_2 connections are polarization networks for each transistor.

Usually for low frequencies a capacitor between the base and collector terminals of Q_1 transistor can be used to flat the gain, thus increasing the band of transistor assembly gain; although, in high frequencies this technique is highly dependent on the used technology, this happens due to the influence of parasitic components on the transistor, and the capacitors dimensions of the design kit.

4.3 LNA state-of-the-art

Many works has been done during the last fifteen years on the subject of 60 GHz LNA, it has happen because the challenges imposed in this frequency, and the real interest to explore this spectrum as a product by industry. In general the firsts works (during the beginning of years 2000) the motivation were to demonstrate that this frequency band usage was possible with RFIC technology and miniaturization. Then, in 2010 the first version of the 802.11ad standard wifi amendment) is published, promoting medium distance access with high data rate using 60 GHz ISM band.

At this time research were conducted to develop full system transmitters on mm-wave, and many work has been published in this topic [51], [52], [53], [54], [55], and [56]. A review with the last years in LNA development is shown in table 4.3 with the main parameters.

Table 4.3: Comparative of published results on different specifications.

	Gain@f_0 (dB)	NF (dB)	P_{1dB} (dBm)	Band	Supply Charge	Technology	Year
[57]	9.6@61.25 GHz	–	–	ND	–	0.25 µm SiGe BiCMOS	2004
[58]	22@52 GHz	–	–	ND	11.4 mA@3.3 V	0.18 µm SiGe	2004
[59]	18@60 GHz	–	–	49 GHz to 71 GHz	30 mA@2.2 V	0.25 µm SiGe BiCMOS	2005

[60]	18@60 GHz	6.8*	–	49 GHz to 71 GHz	30 mA@2.2 V	0.25 µm SiGe BiCMOS	2005
[61]	14.7@60.15 GHz	4.5	-20	ND	6 mA@1.8 V	0.12 µm SiGe Bipolar	2005
[62]	14@65 GHz	–	-12.8	ND	33 mA@2.5 V	0.18 µm SiGe Bipolar	2006
[63]	14@65 GHz	–	–	50 GHz to 94 GHz	–	0.18 µm SiGe BiCMOS	2006
[64]	12.9@61 GHz**	4.6**	–	ND	–	0.13 µm CMOS	2006
[53]	20	6.2	-29	ND	10 mA@2.7 V	0.13 µm SiGe BiCMOS	2006
[65]	14.6@58 GHz	5.5	–	ND	24 mW@1.5 V	90 nm CMOS	2007
[66]	12.5@59.2 GHz*	7.5*	–	58.4 GHz to 60.2 GHz	34 mW@1.2 V	65 nm CMOS	2007
[67]	14.5@59 GHz	4.1	–	57 GHz to 64 GHz	8.1 mW@1.8 V	0.12 µm SiGe BiCMOS	2007
[68]	15@58 GHz	4.4	–	ND	4 mW@1.3 V	90 nm CMOS	2008
[69]	21.4@61.5 GHz	4.3*	-21.2	ND	12.2 mW@1.2 V	0.13 µm SiGe BiCMOS	2009
[70]	9@94.7 GHz	8.6	-14.9	ND	13 mW@3 V	0.13 µm SiGe:C BiCMOS	2010
[71]	18.6@57 GHz	5.7	-14.8	54 GHz to 63 GHz	29mW@1.2V	90 nm CMOS	2010
[72]	15.3@60 GHz	6.2*	-20	57 GHz to 64 GHz	10 mW@3.3 V	0.25 µm SiGe	2010
[73]	18@61 GHz	4.7	–	57 GHz to 67 GHz	28.32 mW@1.2 V	90 nm CMOS	2011
[74]	11.2	4		ND	13.6 mW@2 V	0.13 µm SiGe BiCMOS	2011
[75]	21@60 GHz	5.2	–	55 GHz to 67 GHz	34.22 mW@1.2 V	65 nm CMOS	2012
[76]	14.9@68 GHz	6.8	–	60 GHz to 75 GHz	30.4 mW@1.2 V	32 nm FinFET	2013
[77]	22@60 GHz	5.5	–	58 GHz to 62 GHz	26 mW@1.2 V	65 nm CMOS	2014
[78]	16@60 GHz	5.5	–14.5	57.5 GHz to 62.5 GHz	30 mA@1.2 V	90 nm CMOS	2014
[56]	17.8@60 GHz	5.6	–	54 GHz to 66 GHz	13.2 mW@1.0 V	65 nm CMOS	2014

[79]	23	5.8	–	40 GHz to 67 GHz	25.3 mW	28 nm LP CMOS	2015
[80]	15@60 GHz	3.6	−13.5	52 GHz to 66 GHz	19.96 mW@2.5 V	0.13 µm SiGe	2017
[81]	17.7@67 GHz	7.4	−15.4	54.4 GHz to 90 GHz	19 mW	65 nm CMOS	2017

(*) – simulated results and (**) – approximated values

Smaller CMOS design kits (in the order of tenth of nm) are more disponible, as anticipated by Moore's Law, for analog design; for example 65 nm in 2013 [56] [77], and impressive 28 nm in 2015 [79]. Smaller CMOS transistors mean higher frequencies on the design without the necessity of using bipolar transistors (BiCMOS) in the same design. Unfortunately these technologies are not (still) largely available. Furthermore, the use of NXP® QuBIC in this work is due to the agreement of XLIM with the NXP® semiconductors.

Chapter 5

Realization of a filtering LNA Circuit in mm-wave band of 60 GHz

THE design method presented in previous chapters were assembled in a way to facilitate RFIC circuits design for mm-wave band, these methods were developed in the course of development of the circuits presented in this chapter. Five designed layouts were sent to the foundry within three *fabrication runs*.

The LNA 60 GHz was fabricated in the first fabrication run. At this time our intention was to understand all steps of a circuit fabrication in order to develop a systematic view of the design procedure; also it was important to have a working circuit in order to understand the measurement adversities at mm-wave frequencies. During this first development stage, some problems were mitigated and, although the circuit did not performs as simulations during measurements, the results were satisfactory to review the design procedure and to build up a know-how on mm-wave measurements.

On the second run, two designs were sent to fabrication: A ring resonator filter with central frequency f_0 equal 60 GHz, and a filtering LNA using the same resonator with f_0 equal 60 GHz. This way would both be possible, to evaluate the used design procedure and validate the global RFIC design concept. At this point LNA measurements did not meet with specifications.

The design workflow was then reevaluated (Figure 2.8) and a new version of the filtering LNA and the resonator (with reduced dimensions) were sent to the foundry during the third fabrication run. Measurement results of these last designed circuits illustrates the success in the design method and validate the global RFIC design.

Even if it was supposed to perform the LNA design using the classical approach (which was described in previous chapters), each technology have its peculiarities and deserve attention on the choice of circuit components. This chapter describes the development to the problem of how to choose the transistor for low noise design using NXP® QuBIC technology and to perform good transistor adaptation in mm-wave frequencies. Furthermore, it presents the designs of the five fabricated circuits. Last section compares these designs with the state-of-the-art designs shown in Table 4.3, and discuss some future works possibilities.

5.1 RFIC mm-wave transistor adaptation

Despite the fact that LNA adaptation must performed in a way to offer the specified noise (with the drawback of lowering gain), it was seen in previous chapters that the output charge do not interfere with noise figure when the two-port network is well adapted, therefore in a well designed tuned LNA the transistor output matching network can be adapted to increase gain associated.

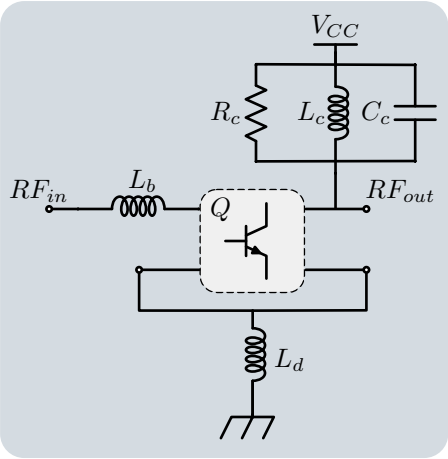


Figure 5.1: Circuit transistor adaptation for RFIC LNA design.

Thus, to adapt the transistor with the minimum noise figure the matching network between the two-port device and its source must be optimized to with minimal contribution to noise while providing *good* match adaptation. In previous chapters it is shown that purely reactive degeneration network – connected as inductance L_d in a two-port network (Figure 5.1) – do not

contribute neither to NF_{MIN} nor to $R_{s,opt}$, however it helps increasing linearity in a common emitter transistor.

5.1.1 Input adaptation

For high-frequencies the small signal equivalent simple model of the intrinsic HBT is illustrated in Figure 1.5, and the corresponding Y-parameter of CE and CB matrices are given by equations 5.1 and 5.2, as seen in [82] and [49].

$$Y_{CE} = \begin{bmatrix} g_\pi + j\omega(C_\pi + C_\mu) & -j\omega C_\mu \\ g_m e^{-j\omega\tau} - j\omega C_\mu & g_o + j\omega(C_o + C_\mu) \end{bmatrix} \tag{5.1}$$

$$Y_{CB} = \begin{bmatrix} g_m e^{-j\omega\tau} + g_o + g_\pi + j\omega C_\pi & -g_o \\ -g_m e^{-j\omega\tau} - g_o & g_o + j\omega(C_o + C_\mu) \end{bmatrix} \tag{5.2}$$

Here the base-emitter resistance (R_π) is ignored because it can be negligible in high-frequencies for this analysis, but the capacitance C_μ is still present. This equivalent circuit is a useful approximation to a first hand-on analysis for circuit design.

Furthermore, the input admittance of a transistor loaded by the admittance Y_L is directly obtained by a two port admittance matrix using

$$Y_{in} = Y_{11} - \frac{Y_{12}Y_{21}}{Y_L + Y_{22}}. \tag{5.3}$$

Finally, for a cascode stage its input admittance can be derived by 5.3 using equations 5.1 and 5.2 from CE and CB stages as

$$Y_{in} = Y_{11,CE} - \frac{Y_{12,CE}Y_{21,CE}}{Y_{22,CE} + Y_{1,CB} - \left(\dfrac{Y_{12,CB}Y_{21,CB}}{Y_L + Y_{22,CB}}\right)} \tag{5.4}$$

Continuing the analysis to capture the characteristics of the extrinsic transistors at mm-wave,

it is necessary to consider parasitic resistances R_b, R_c, and r_E, as illustrated in Figure 5.2.

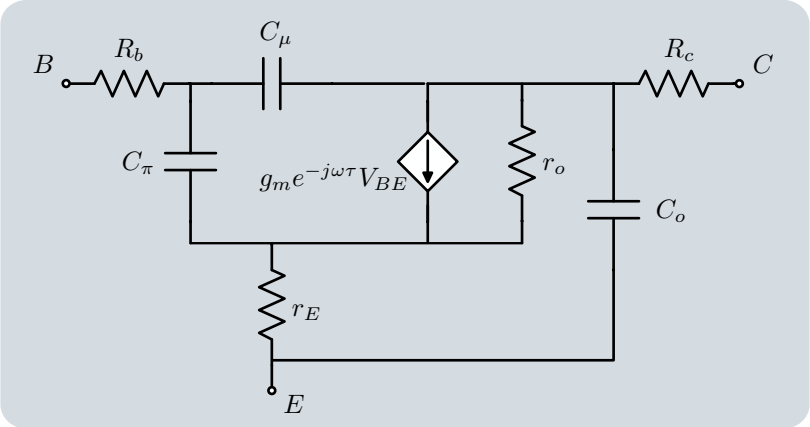


Figure 5.2: Small signal high-frequency equivalent circuit with series parasite resistors.

Although extract the corresponding Y-parameters directly from circuit of Figure 5.2 would be possible the use of feedback theory simplifies the circuit to that of Figure 5.3.

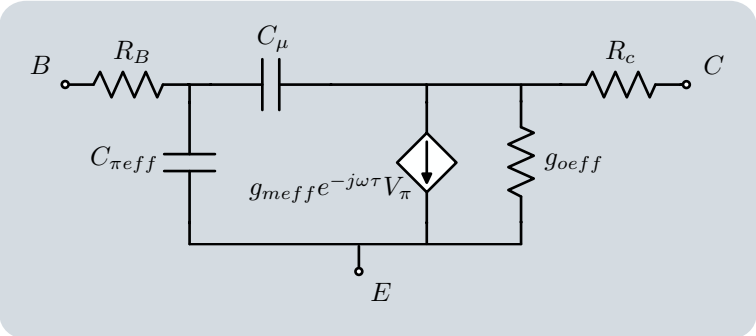


Figure 5.3: Small-signal HBT high-frequency equivalent circuit with parasite resistors.

where $R_B = R_b + r_E$, and

$$g_{meff} = \frac{g_m}{1 + g_m r_E} \tag{5.5}$$

$$g_{oeff} = \frac{g_o}{1 + g_m r_E} \tag{5.6}$$

$$C_{\pi eff} = \frac{C_\pi}{1 + g_m r_E} \tag{5.7}$$

At this point one could deliberately remove C_μ and express the equivalent circuit as a function of the effective cuttoff-frequency (f_{Teff}) and of the effective trans-conductance

(g_{meff}) of the transistor or of the cascode stage itself [49]. In other words, it can be accepted that f_{Teff} includes partially the impact of C_μ during a first *hands-on* analysis; also, despite the fact that this equivalent circuit do not account for the reverse feedback through the C_μ, it is simple and sufficient.

An alternative and more precise analysis would be to use Miller theorem, but since these designs are computer aided, it was not necessary to develop this analysis by hand. The final circuit for input impedance is illustrated in Figure 5.4.

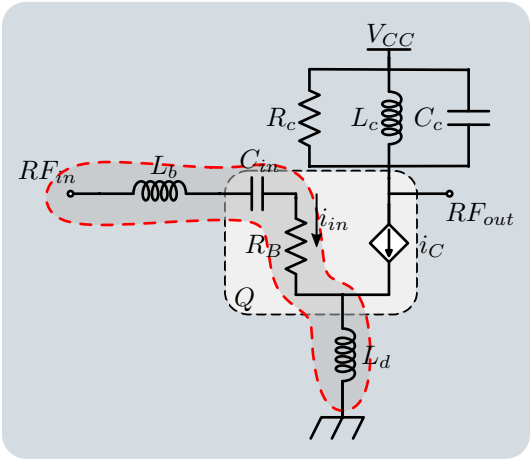


Figure 5.4: Input impedance of a common emitter circuit showing the components of the network.

And because the use of the effective cuttoff-frequency f_{Teff} then, $C_{in} = \dfrac{g_{meff}}{\omega_{Teff}}$ and the current $i_C = \dfrac{f_{Teff}}{jf} i_{in}$ at the source. The role of L_d and L_b are therefore to set the real and imaginary part of input impedance of a tuned common emitter (or cascode) amplifier, as shown in equation 5.8.

$$Z_{in} \approx \underbrace{(R_b + r_E)}_{R_B} + 2\pi f_T L_d + j\left(2\pi f_0 L_d + \omega L_b - \frac{1}{2\pi f_0 C_{in}}\right) \tag{5.8}$$

Equation 5.8 shows that for a given transistor, R_B, f_T, and C_{in} is fixed and the inductance values L_d, and L_b have to be found for the optimal adaptation. It is seen that L_d sets the real part of Z_{in} and should not affect noise figure if purely reactive, what cannot be true in

real design. To conclude, L_b resonate with C_{in} limiting the band of the circuit, and sets the imaginary part input impedance Z_{in}.

The input impedance is then based in the choice the three components: The transistor itself, what defines the resistence R_B and the input capacitance, and L_d and L_b.

5.1.2 Output adaptation

Previously in this work it was demonstrated that in a two-port circuit the load (therefore output adaptation itself) have no impact on NF of the circuit, and for that reason output adaptation is done in a way to match the load, hence increasing the gain.

Equation 4.28 illustrates that maximal trans-conductance gain is achieved if optimal input and output adaptation of circuit is attained. Since we do want to adapt the input to noise, it is interesting to match the output to the load (or the next stage) so reducing signal reflection what increases gain.

In RFIC design, LNA load can be provided by a second amplifier gain stage, a mixer or a phase shifter; in addition, the output of a LNA is capacitive (due C_o capacitance of the transistor intrinsic model). Consequently, the simplest matching network is obtained with an L-section matching circuit consisting of a shunt inductor L_c connected to the V_{CC}, followed by a series capacitor to the load. The RLC circuit from Figure 5.4 can then be reduced to an inductor L_C, and the output series capacitor provides a DC block to next stages.

5.1.3 Designing for low noise in QuBIC using HBT

During the LNA design one of most important and difficult task is the choice of the right transistor. A LNA transistor have to deliver the minimum amount of noise to the circuit (or the noise according to the system specifications), while offering good gain and easy adaptation. In this section is show an structured transistor analysis to choose the optimal transistor for a LNA circuit using NXP® QuBIC technology.

Design with use of a *design kit* optimizes workflow cycle because it uses modeled structures

that otherwise should be measured before, in a full design environment. For example the QuBIC uses the MEXTRAM model for bipolar transistors, which have its parameters set by the Heterojunction Bipolar Transistor (HBT) BNY from the design kit. Figure 5.5 illustrates a BNY transistor with four emitters from QuBIC.

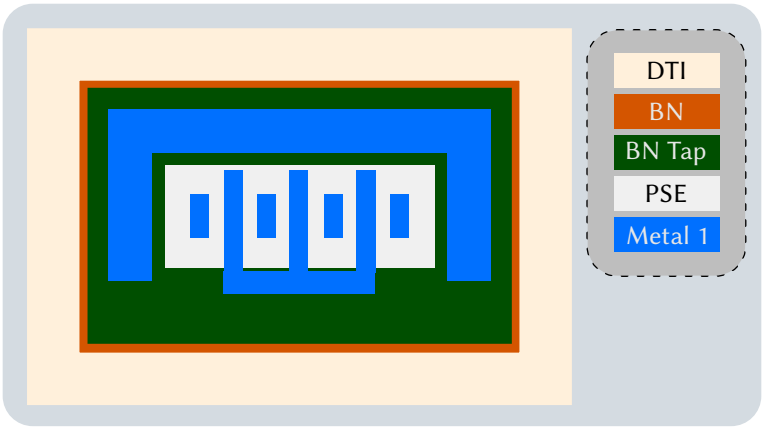


Figure 5.5: Representation of a BNY QuBIC transistor with four emitters.

After the circuit specifications are known, the choice procedure for the correct core transistor that meet these characteristics is taken into account as a delicate task, this task can be better performed with a structured approach. Using NXP® QuBIC design kit it was possible to develop a simulation with the transistor topology size varying, what helped us to comprehend how transistor dimensions impact on the circuit noise, gain and adaptation.

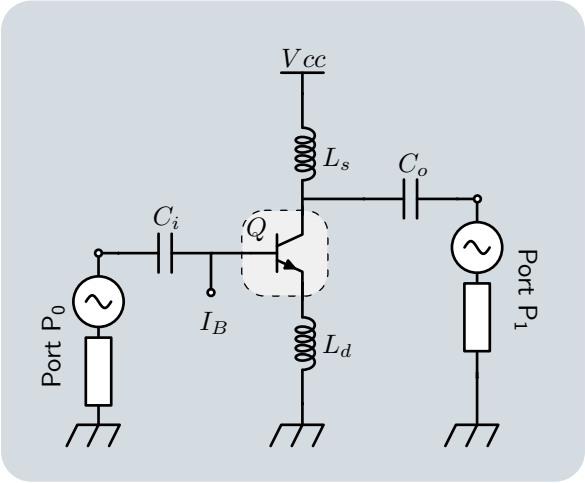


Figure 5.6: Schematic created to extract transistor LNA design characteristics.

Our approach was to simulate a great number of NXP® QuBIC technology transistors (with

different dimensions) for its characteristics. For this, a schematic was developed (see Figure 5.6), so it was possible to obtain the value of NF_{MIN}, maximal trans-conductance gain G_{MAX}, optimal adaptation (Γ_{opt}), and R_n for different transistor dimensions, bias and degeneration inductance; note that it is necessary to simulate these values to a specific frequency (say 60 GHz, for example), and so it is possible to simulate a large number of transistors in a relatively small time. Table 5.1 show the variation on component values, biasing and transistor dimensions that were simulated.

Table 5.1: Amplifier topologies review.

	V_{CC}	I_B	Q_w	Q_l	Q_N	L_d
Min	0.4 V	1 µA	0.3 µm	1 µm	4	80 pH
Step	0.2 V	1 µA	0.2 µm	1 µm	2	10 pH
Max	0.8 V	3 µA	0.7 µm	3 µm	8	100 pH

Where I_B is the base current, Vcc voltage source for the experimented transistor, Q_w, Q_l and Q_N are emitter width, emitter length and the quantity of emitters in BNY transistor Q. It is also important to vary the inductance L_d so it is possible to determine the impact over the transistor stability. Capacitors C_i and C_o works as DC blocks and the value of inductance L_S is not important in this analysis.

What concerns to the simulation time, if we suppose exaggeratedly that the simulation of the parameters of a single transistor takes five seconds to finish, then approximately one hour of simulations are necessary to run all the 729 transistors. Also these simulations can be stored for future designs, reducing the time of this design step.

Figure 5.7 illustrate the variation of R_n with the increase of number of emitters, although I_C is almost equally distributed while *n* varies, Figure 5.8 is the same 5.7, but without the change in R_n size to better understanding on how these transistor are distributed.

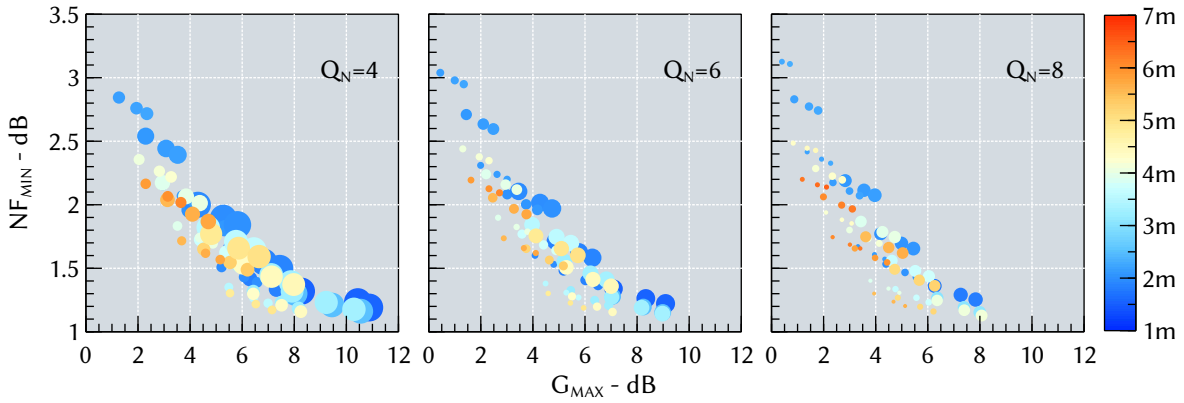


Figure 5.7: Parametric plot of NF_{MIN} versus G_{MAX} for $Q_n = \{4, 6, 8\}$. Consummation (I_C) and noise resistance (R_n) information given by color-map and size respectively (bigger size implies higher R_n). $L_d = 100pH$ is fixed.

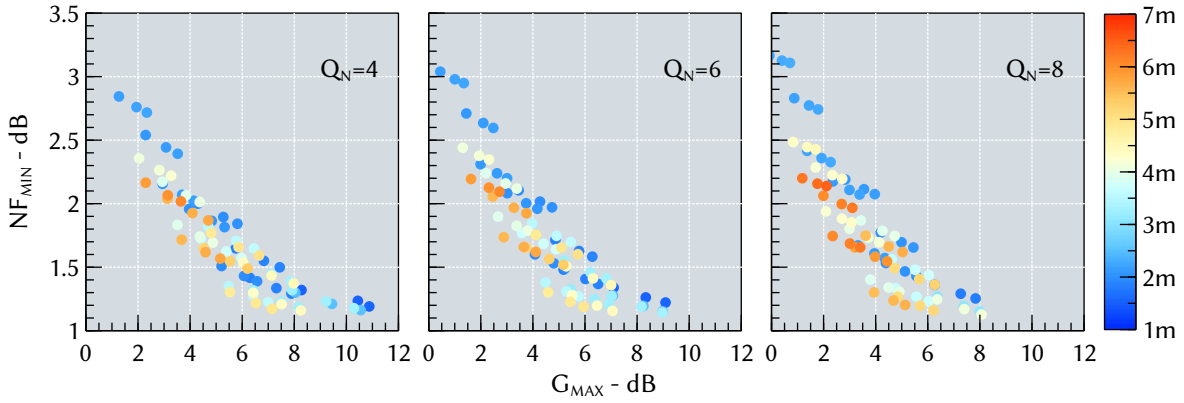


Figure 5.8: Parametric plot of NF_{MIN} versus G_{MAX} for $Q_n = \{4, 6, 8\}$. Consummation (I_C) given in color-map. $L_d = 100pH$ is fixed.

After the simulations are performed, NF_{MIN} of a bipolar[1] transistor can be calculated using equation 5.9 (derived in [49] and [82]).

$$F_{MIN} \cong 1 + \frac{n}{\beta_{DC}} + \frac{f}{f_T}\sqrt{\frac{2I_C}{V_T}(r_E + R_b)\left(1 + \frac{f_T^2}{\beta_{DC} f^2}\right) + \frac{n^2 f_T^2}{\beta_{DC} f^2}}; \tag{5.9}$$

where:

— $n \simeq 1$: collector current ideality factor, approximately equal to one, except under high current injection bias when its value can exceed 1.2;

[1] In this case the word bipolar is used as a generalization that includes HBT.

— β_{DC} : DC gain;

— $V_T = \frac{kT}{q}$: thermal voltage;

— r_E : emitter resistance;

— R_b : base resistance.

But, from Spectre® model files of NXP® QuBIC library BNY transistor has its dimensions mapped to the MEXTRAM model with the emitter resistance (r_e), the constant part of base resistance (r_{bc}), and the constant part of collector resistance (r_{cc}) given by

$$r_e = \frac{re_c^{\,0}}{rm^{\,1}} + \frac{re_{sq}^{\,12}}{w_m(l_m - dle_{re}^{\,0})n_e} \tag{5.10}$$

$$r_{bc} = \frac{rbc_c^{\,1.2}}{n_e}\left(\frac{rbc_{be}^{\,50}\; wbe^{\,0.7}}{n_b(l_b + w_b)} + \frac{rbc_{pe}^{\,150}}{n_b(l_m + w_m)}\right) \tag{5.11}$$

$$r_{cc} = \frac{rce_c^{\,1.1}}{rm^{\,1}} \times \frac{rcc_{plug}^{\,10}}{2l_{col} + w_{col}} \tag{5.12}$$

where variables w_m, l_m, n_e, w_b, l_b and n_b are respectively width, length and number of emitters and base connections for BNY transistor, all crossed variables are dependent of technology and defined in model files for BNY, its values are shown over the arrow; the term $2l_{col} + w_{col}$ in equation 5.12 is the area of collector, l_{col} and w_{col} are given in equations 5.13 and 5.14 where *pitch* is the distance between two emitters.

$$l_{col} = l_e + ddem^{\,0} + dwb^{\,0.3} + leol1^{\,1.2} - (dwb^{\,0.3}/2) \tag{5.13}$$

$$w_{col} = w_e + (ndot^{\,1}n_e - 1)\text{pitch} + 2wcol1^{\,1.2} \tag{5.14}$$

And therefore, for the BNY transistor, NF_{MIN} is dependent of transistor contact dimensions, result that were previously confirmed in Figure 5.7. Equations from 5.10 to 5.14 are highly

dependent of transistor topology and technology[2], but they give a good insight of how R_n changes according to *width* and *length* of transistor contacts. However Figure 5.8 show that current do not increase significantly with transistor size; and yet no information on the adaptation of simulated transistors is given in Figures 5.7 and 5.8.

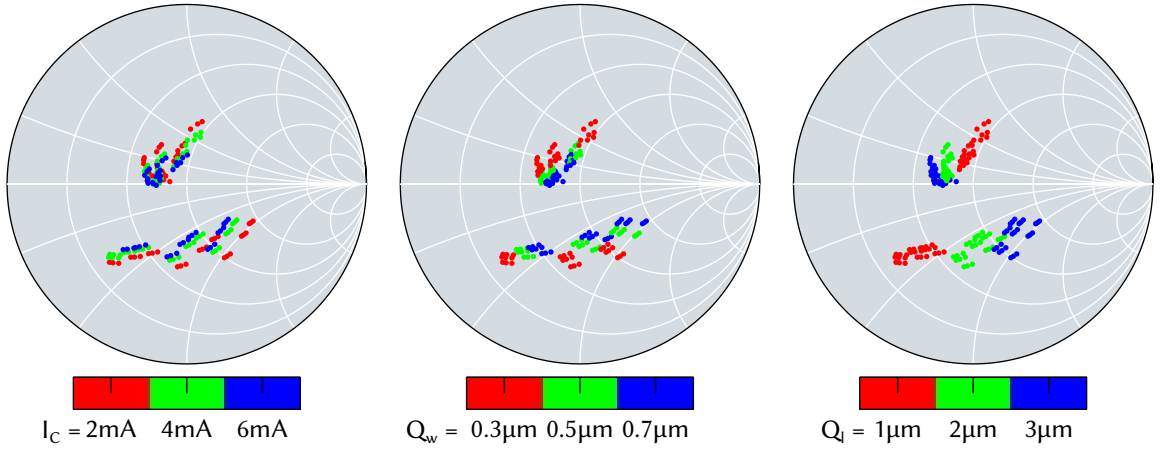


Figure 5.9: Influence of I_C, Q_w and Q_l in the optimal adaptation for gain and noise in a transistor with eight emitters. $L_d = 100pH$ is fixed.

The information on the values for the adaptation of the transistors are obtained with the Smith chart diagram, Figure 5.9 illustrates the diagrams and the influence of Q_w and Q_l in adaptation for $Q_N = 8$, which was chosen because it delivers lower R_n values for a varying V_{CC} and I_B. Q_w influence is smaller than Q_l influence, this last changes significantly the real part of the transistor Γ_{OPT}.

Also, in Figure 5.10 is illustrated the Q_l influence over gain circles and noise circles, the points with same color are transistors with same dimensioning set in the caption. Figure 5.10 illustrate maximal gain ($G_{S,MAX}$), and NF_{MIN} points, where each point being the center of its gain circles (in black) and its noise circles (colored) respectively.

The LNA optimal adaptation is a compromise between gain and noise; and is represented in literature by the zone of interception between both noise and gain circles. Also, if R_S=R_L=50 Ω is assumed, this intersection must be close to the center of Smith chart to an easy adaptation.

For example in Figure 5.10 the circles are plotted with $G_{MAX} - G_A = 0.8$dB and $NF -$

[2]Also the variable names are the same used in NXP® QuBIC library files

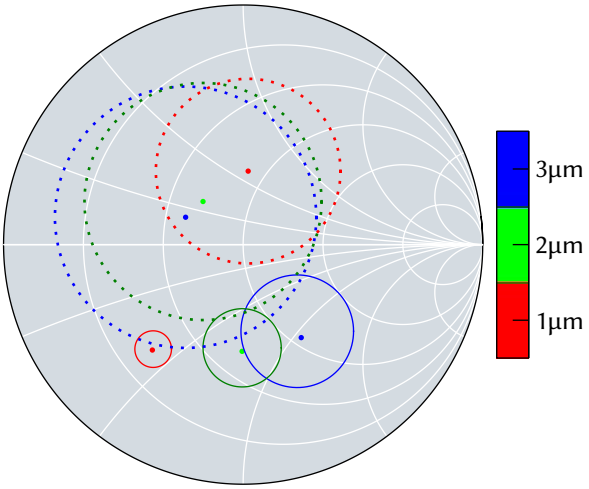


Figure 5.10: Gain circles (in dotted lines) and Noise circles (in solid lines). Points are transistors with $Q_l = \{1\mu m, 2\mu m, 3\mu m\}$, $Q_N = 8$, $Q_w = 0.3\mu m$, $V_{CC} = 0.4$ and $I_B = 0.1\mu A$.

$NF_{MIN} \approx 2$dB. From figure we see that the blue transistor is the easiest to adapt in noise, because it's noise circle is larger, however, its gain is not very good. Both transistors red and green have good gain, but also are more difficult to adapt in noise than blue transistor.

If only the differences $G_{MAX} - G_A$ and $NF - NF_{MIN}$ were important on LNA design, then only this Smith chart would be enough for the transistor choice, however the information of *what is the maximal gain and minimal noise* for each transistor is not present in this context. Therefore, for the choice of transistors in this context it is necessary both the graph of Figure 5.8 indicating the relation of gain G_{MAX}, NF_{MIN} and I_C current; and the Smith chart from Figure 5.10, indicating the optimal adaptation of each transistor.

5.2 Fabricated Low Noise Amplifiers

Three versions of the 60 GHz LNA where sent to fabrication:

1. 60 GHz LNA:

   This is a no filtering version of the circuit;

2. 60 GHz filtering LNA – version 1:

   With the first version the ring resonator (octogonal) as filter block;

3. 60 GHz filtering LNA – version 2:

   With the second version the ring resonator (squared) as filter block.

5.2.1 60 GHz LNA

This circuit represents the first efforts of this work on developing for mm-wave using BiCMOS SiGe:C 0.25mm^2 technology. During the design procedure a simulation to obtain the specifications of the transistor was performed in order to make the optimal choice of components for this LNA.

The topology of the LNA design was defined after a bibliographic analysis on RFIC LNA 60 GHz design, and is summarized in table 4.3 on page 72. For instance, the topology that best fits our purposes, and therefore the chosen topology, was a cascode multistage not differential LNA. Also the interest on this topology was because we could directly compare the results of our design with state-of-art designs.

After that we chose the transistors that attend circuit specifications, yet it is necessary to know how this transistor will perform with a varying I_C control current versus NF, so we can determine the optimal polarization current that grants the smaller (and stable) NF_{MIN}. At this point a schematic simulation were performed to determine NF and the transition frequency f_T versus an injected I_C for a given transistor.

Figure 5.11 illustrate the obtained values of NF and frequency f_T versus current I_C for a transistor chosen by the procedure described in previous section for f_0=60 GHz. This way we can know the extension of that I_C current can vary without interfere in transistor noise performance in a given frequency.

It is implicit in equation 5.9 that noise is a nonlinear function of emitter width w_E via the $I_C(r_E + r_B)$ term. Also, as long as the length-to-width (l_E/w_E) ratio of the emitter stripe is larger than ten, F_{MIN} remains invariant to changes in emitter length and increases almost linearly with frequency [82].

Considering that specifications on this circuit were not severe – because at the design time we did not completely knew the technology and how to perform design adjustments –, we have

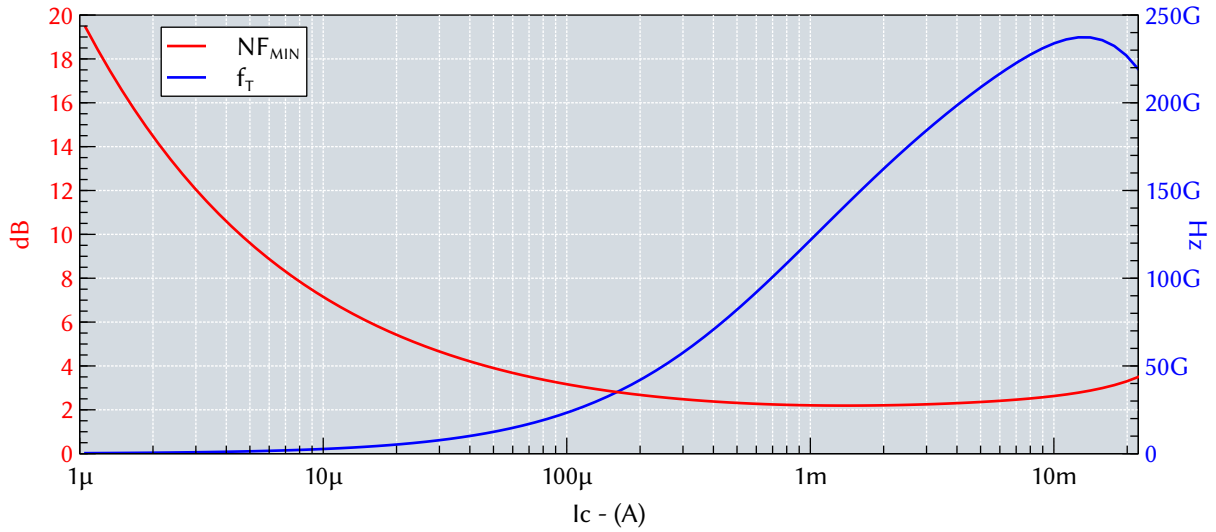


Figure 5.11: NF_{MIN} and f_T versus polar current I_C @ 60 GHz.

chosen to focus on the simulation procedures of passive components, and to develop a sense of the limits of components for the technology. A preliminary version the circuit schematic was developed (Figure 5.12) with use of the same cascode transistors on both stages, in prejudice of circuit linearity. The impedances Z_i, Z_1, and Z_o are generally formed using a capacitor in series so each stage is DC isolated.

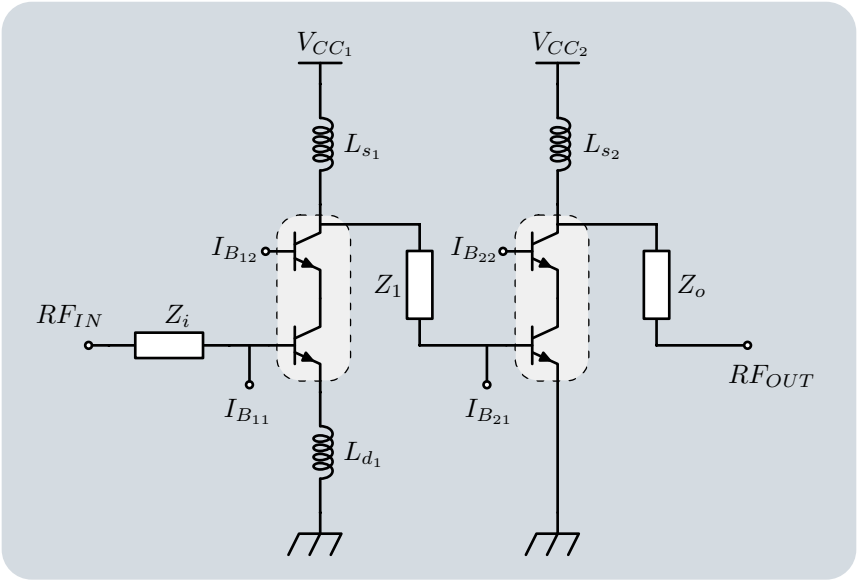


Figure 5.12: 60 GHz LNA schematic.

The circuit layout was developed using the regular design flow (as demonstrated in Figure 2.1), and has approximately 750×520 µm^2 in layout (787×554 µm^2 measured in microscope,

after waffle cutting), stable ($K_f > 1$ and $Bf_1 > 0$), and with gain over 12 dB in measure.

Even though the results are in conformity with literature, it happens that the expected parameters were not attained during measurements. After discussions about what could have happened for the curves do not meet simulations, the first insight was to examine the measurement setup. After all, it was noted the existence of problems in design workflow that was not adapted to mm-wave design at the time.

A comparative table on 0.25 µm SiGe BiCMOS 60 GHz LNA is shown in table 5.2. Lack of equipments for mm-wave measurement in the laboratory prevented that the circuit have its noise measured. Figure 5.13 is the microphoto of the fabricated circuit.

Table 5.2: Comparative table of published results on 0.25 µm SiGe BiCMOS.

	Gain@f_0 (dB)	NF (dB)	P_{1dB} (dBm)	Band	Supply Charge
[57]	9.6@61.25 GHz	–	–	ND	–
[59]	18@60 GHz	–	–	49 GHz to 71 GHz	30 mA@2.2 V
[60]	18@60 GHz	6.8*	–	49 GHz to 71 GHz	30 mA@2.2 V
[72]	15.3@60 GHz	6.2*	-20	57 GHz to 64 GHz	10 mW@3.3 V
This work	12.5@64 GHz	–	–	58.25 GHz to >67 GHz	26 mA@3 V

(*) – simulated results and (**) – approximated values.

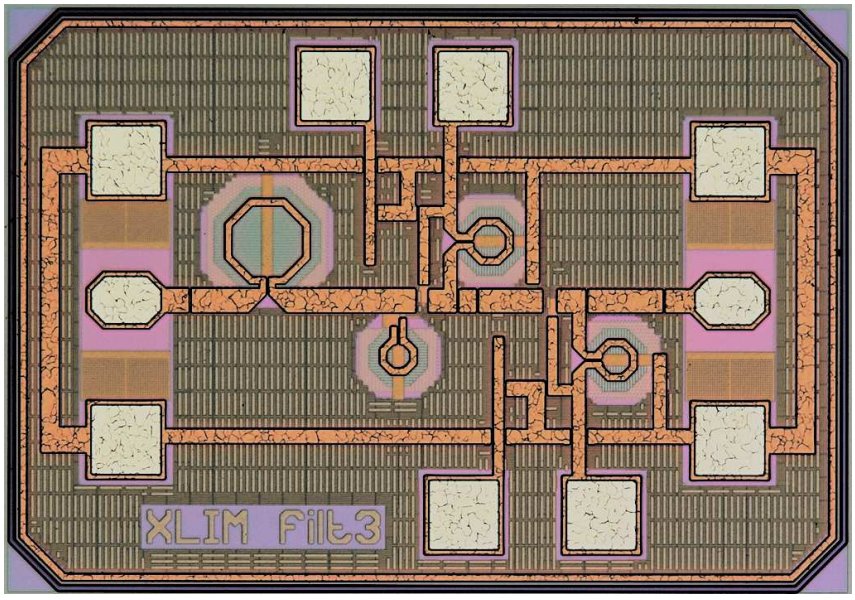


Figure 5.13: Photo of fabricated LNA 60 GHz circuit.

At this point we traced back design errors, and perform a reorganization in the design workflow in a way simulation and measurement results could meet one another (Figure 5.14), using the measurements to control workflow errors, and adapting the simulations.

This reevaluation in design flux of Figure 2.1 allowed to trace back the performed errors in layout design. Subsequently this study permitted that a modified workflow (that includes EM simulation) could be completed, optimizing layout design in simulation time and results.

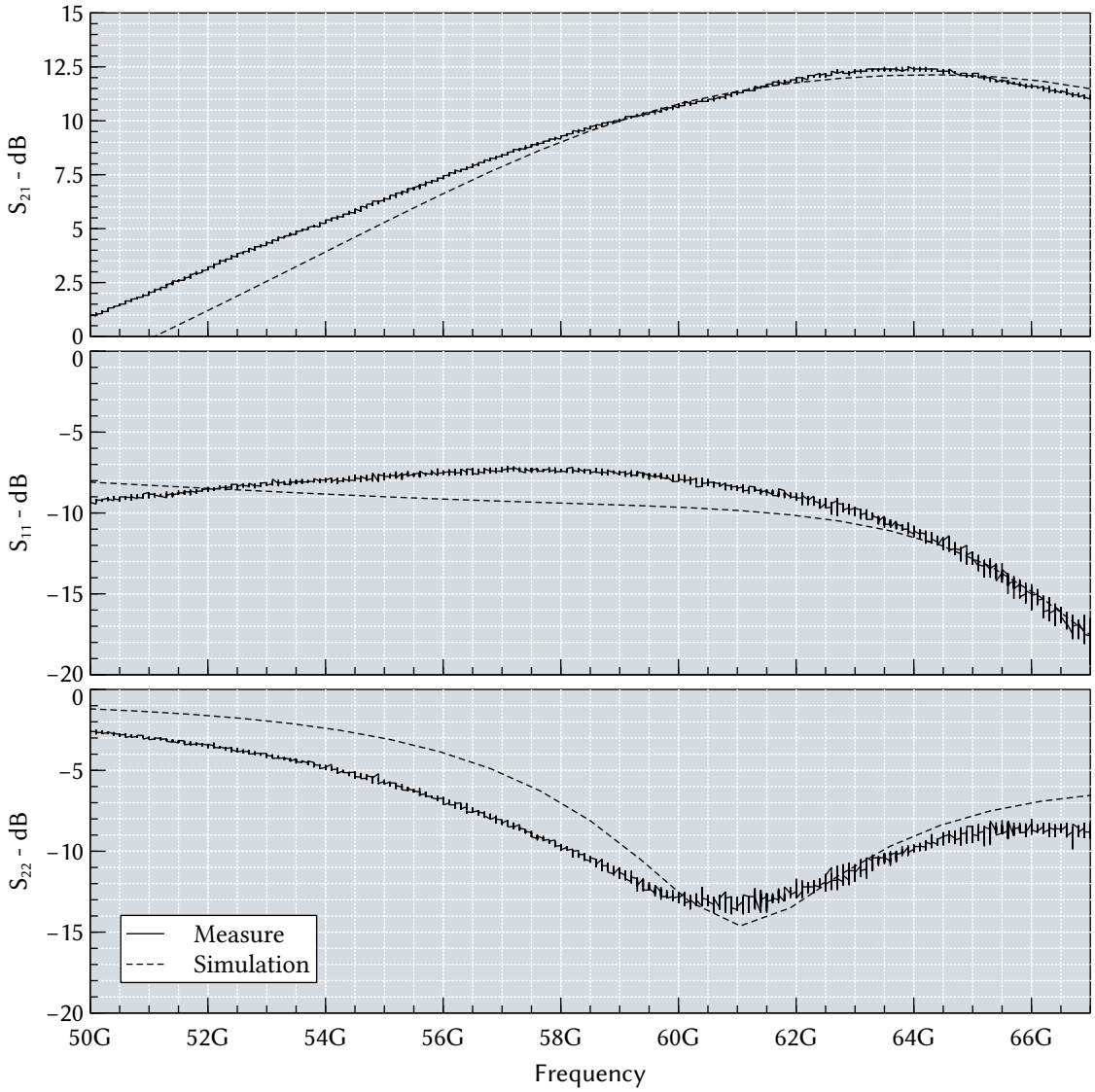


Figure 5.14: Measured and simulated results of LNA 60 GHz.

5.2.2 60 GHz Filtering LNA

For the second and third LNA the design objective was to make use of Monolithic Microwave Integrated Circuit (MMIC) advantages (such: integrated adaptation, same ground plane for multiples devices, CAD software use for design, etc.) while carrying out mitigation process of miniaturization problems.

The challenge was to insert a pre selection filter stage into the project of multiple stage LNA, designing the filter and the LNA at same time. This procedure exploits the design step to reduce circuit interferers in silicon, and integrate block adaption in the system design rather than adapt to a fixed load, or with a matching network outside circuit.

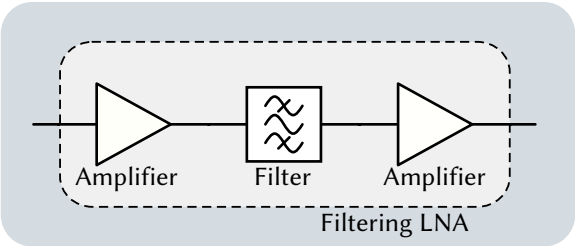


Figure 5.15: Proposed 60 GHz LNA filter topology.

Figure 5.15 illustrates a system design view of the proposed circuit, co-design technique permits to divide component designs to better explore its parameters. For example, comparing Figure 5.15 with the first version of the filtering LNA, the first amplifier on the figure is the first stage of LNA, while the second amplifier is both, the second and third stage (the full LNA is a three stage cascode).

For these designs, the same procedure of the first 60 GHz LNA for the choice of transistors was performed during the design steps. First the transistors are chosen based on noise, gain and adaptation, later its I_C impact in noise variation is defined, so we have the polarization value for the transistor. Furthermore, these steps are performed for each stage, in order to grant linearity and stability.

The Fabricated circuit for the first version of the filtering LNA is presentetd in Figure 5.16, total circuit dimensions are 1193×1123 µm^2, each one of the three LNA stages have a pair control pads, one for V_{CC} and other that controls the current mirror connected in the base of

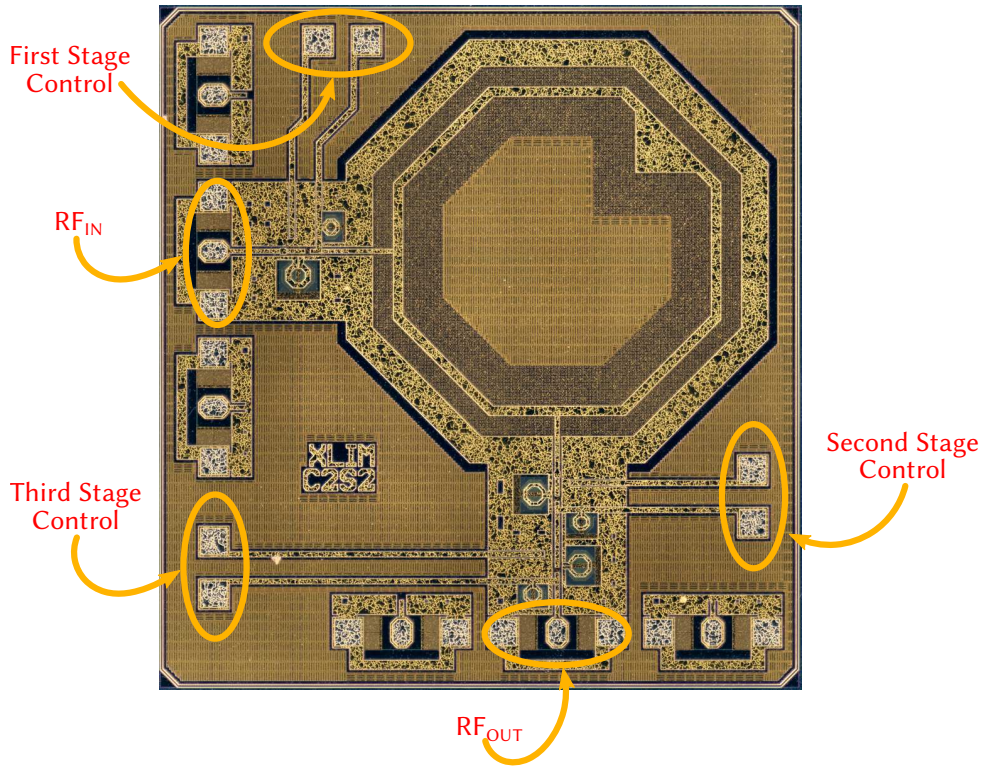


Figure 5.16: Photo of fabricated circuit Filtering LNA 60 GHz.

CE transistor of cascode. The filter performed in this design circuit is the first version of the ring resonator studied in previous chapters, and its operation performance is shown in table 3.2, on page 53.

Also as pointed out before, the first filtering LNA not performed as well as during simulations. After measurements and observations on the design some inaccuracies on the workflow were identified, this helped us to mitigate the design procedure in a way we could tune workflow to mm-wave design.

Figure 5.17 illustrates simulated results of designed LNA circuit when it was sent to fabrication, with the first workflow (without EM simulation). Then, after changing the workflow the simulations to the designed circuit were performed and we found it meet measurements, and validating new modified workflow (Figure 5.18).

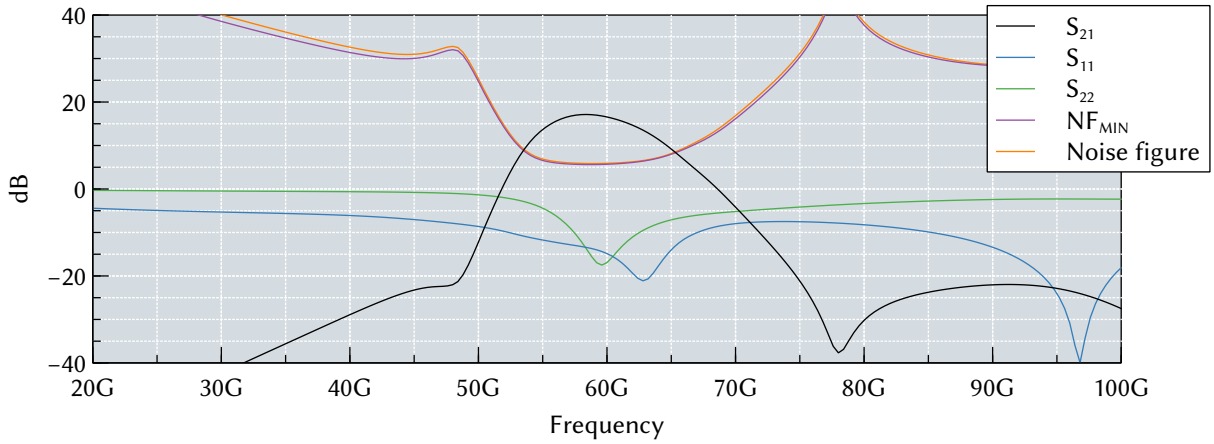


Figure 5.17: Response 60 GHz filtering LNA simulation of circuit layout using classic workflow.

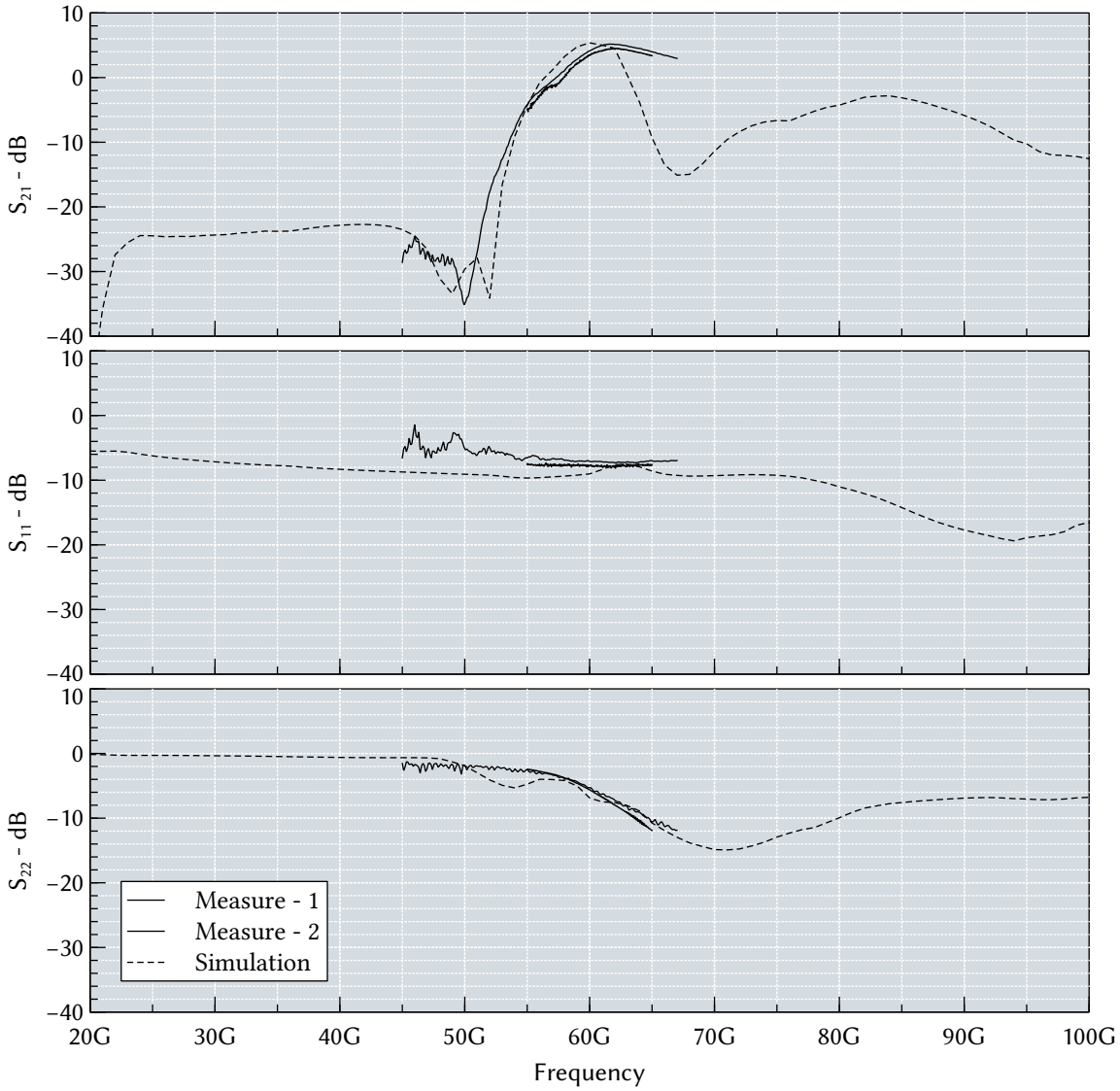


Figure 5.18: Response 60 GHz filtering LNA measure of circuit layout using modified workflow.

During the development of this second version of the filtering LNA, it was decided to ameliorate the resonator filter as well as the schematic of the LNA itself. The first observable change concerns the resonator size, what reduces 32% of the total circuit size, going from 1193×1123 μm^2 in the first filtering LNA to 1200×757 μm^2 in the second version. Figure 5.19 show a microphoto of the fabricated circuit.

Also, the number of pads were reduced because the current mirror that controls the base current I_B of CE transistor of cascode was directly connected to V_{CC} pad throughout a resistance on this version; this modification simplify the bank of measurement, although adds a supplementary difficulty during the design.

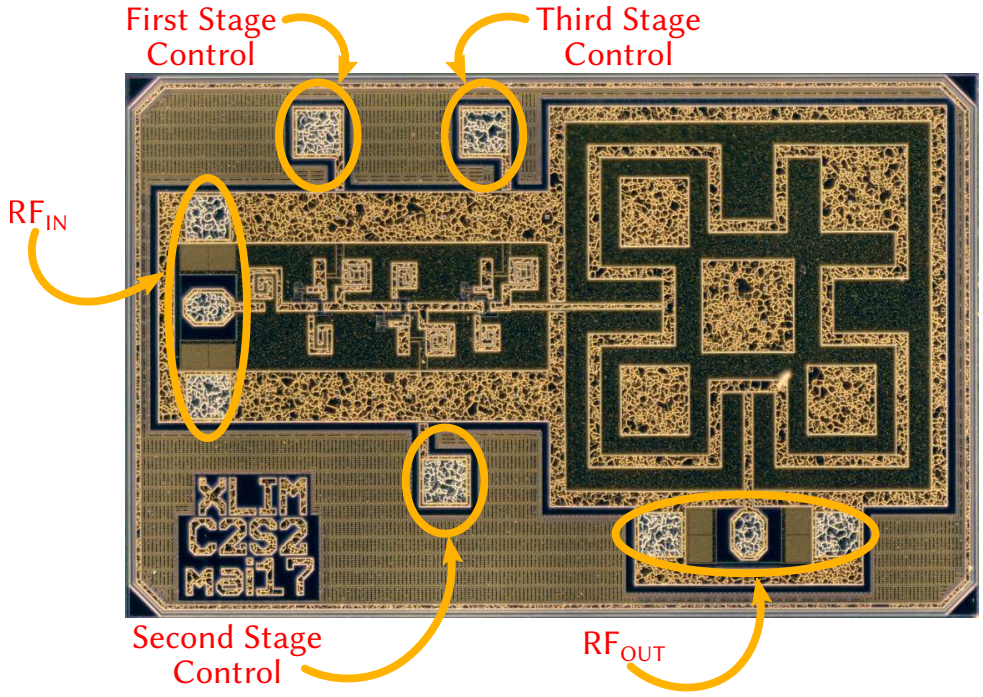


Figure 5.19: Photo of fabricated circuit Filtering LNA 60 GHz second version.

Different of the previous version, in this revision the three stages of the amplifier are placed before the resonator filter, this placement was chosen as an effort to increase gain, considering that IL of filter is approximately −3 dB. Additionally, a ground wall covers the totality of the circuit and the resonator, this is an effort to reduce the effects of the difference on the reference plane off the circuit, therefore reducing amplifier interference to the resonator response.

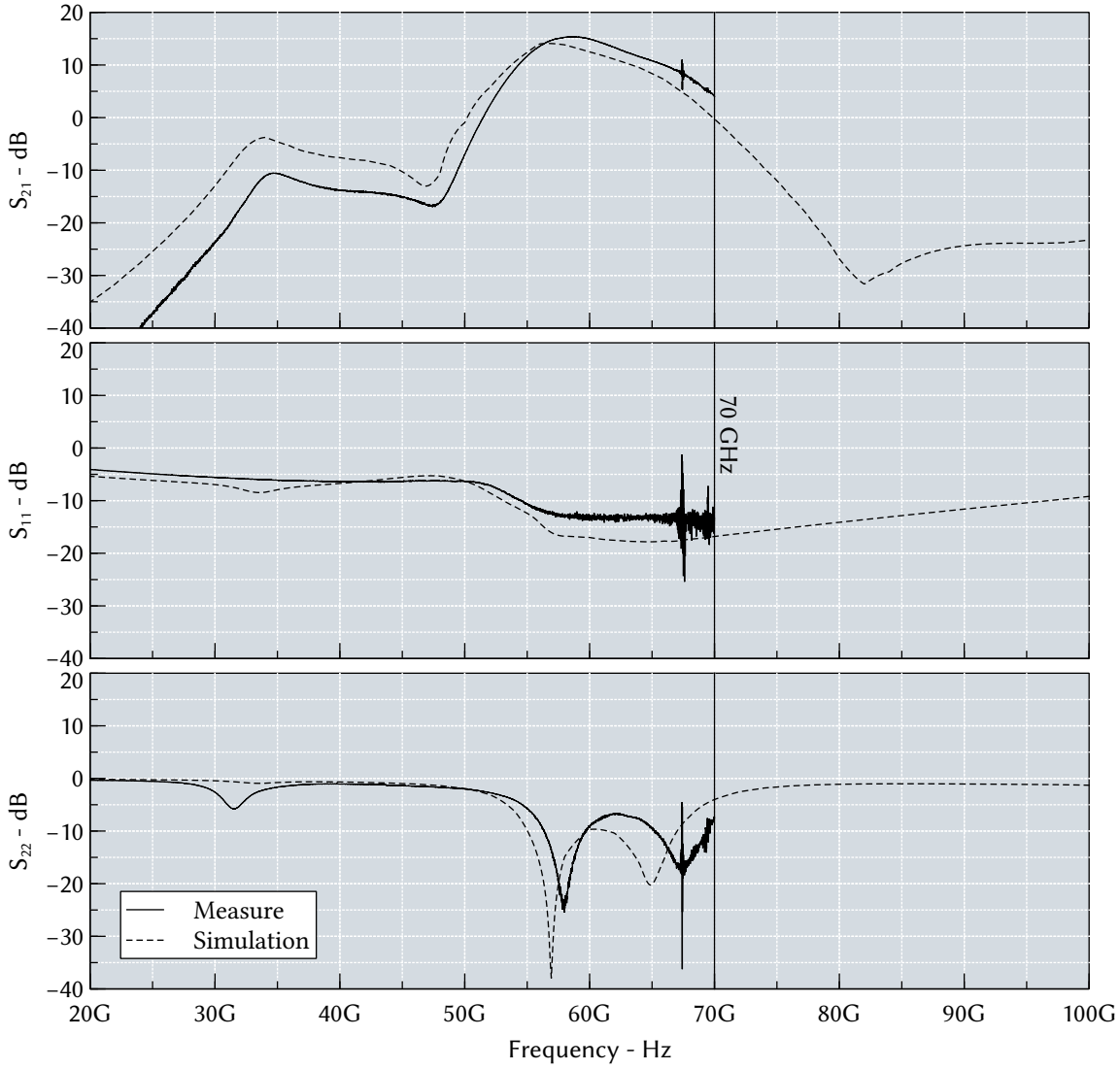


Figure 5.20: Comparative results of 60 GHz filtering LNA second version.

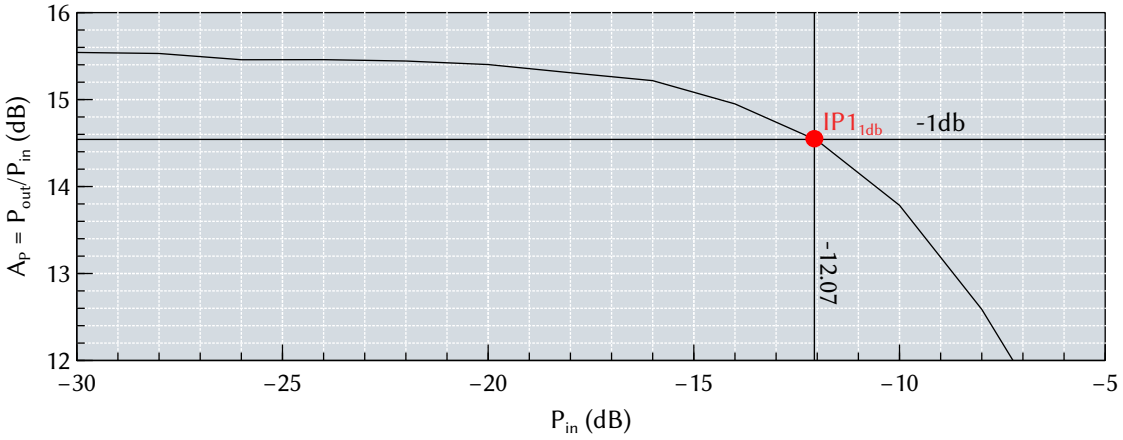


Figure 5.21: Power gain $A_P = P_{OUT}/P_{IN}$ relation at 58.5 GHz.

Measured curves are shown in Figure 5.20 where they are compared to simulation results. Maximum gain is over 15.5 dB@58.5 GHz, bandwidth goes from 55 GHz to 65 GHz centered in 60 GHz. The graph from Figure 5.21 shows the power gain relation at the peak frequency (58.5 GHz), the red circle marks the input referred compression point IP_{1dB}=−12.07 dB.

The power consumption of the circuit was measured stage by stage, the project of this circuit includes current mirrors at each stage so it is possible to control the gain separately. Table 5.3 shows the variation of current I_C and how this variation impacts on the performance of the LNA circuit. For example, for a gain of 14.4 dB the power consumption on each stage (P_1, P_2 and P_3) is 18.1 mW, 17.5 mW, and 22.2 mW respectively with a current $I_{C_{1,2,3}}$=10 mA.

The gain of this LNA is smaller when compared with the circuits of the Table 4.3 for the same power consumption, this result is expected since IL of the resonator is approximately −3 dB. Table 5.3 illustrates the impact of I_C current variation over the LNA gain, this table was obtained varying V_{CC} values on each pad forcing the wanted I_C current.

Table 5.3: Measured power consumption and gain (S_{21}) at 58.5 GHz for the second version of the filtering LNA.

I_C	P_1 – V_{CC}	P_2 – V_{CC}	P_3 – V_{CC}	S_{21} @ 58.5 GHz
5 mA	1.307 V	1.154 V	1.660 V	8.301 dB
7 mA	1.505 V	1.312 V	2.19 V	11.5 dB
10 mA	1.812 V	1.745 V	2.222 V	14.4 dB
12 mA	2.061 V	1.829 V	2.475 V	15 dB
13 mA	2.435 V	2.001 V	2.385 V	15.3 dB

To conclude, Figure 5.22 show the placement of this work LNA designs as a result of its consumption by stage. Although these results do not suggest a favorable result at first, it should be considered that none other LNA presented here is filtering. Also, It should be considered that the power consumption of this work presented here is the sum of the polarization current and the current driven to the polarization circuit of each stage.

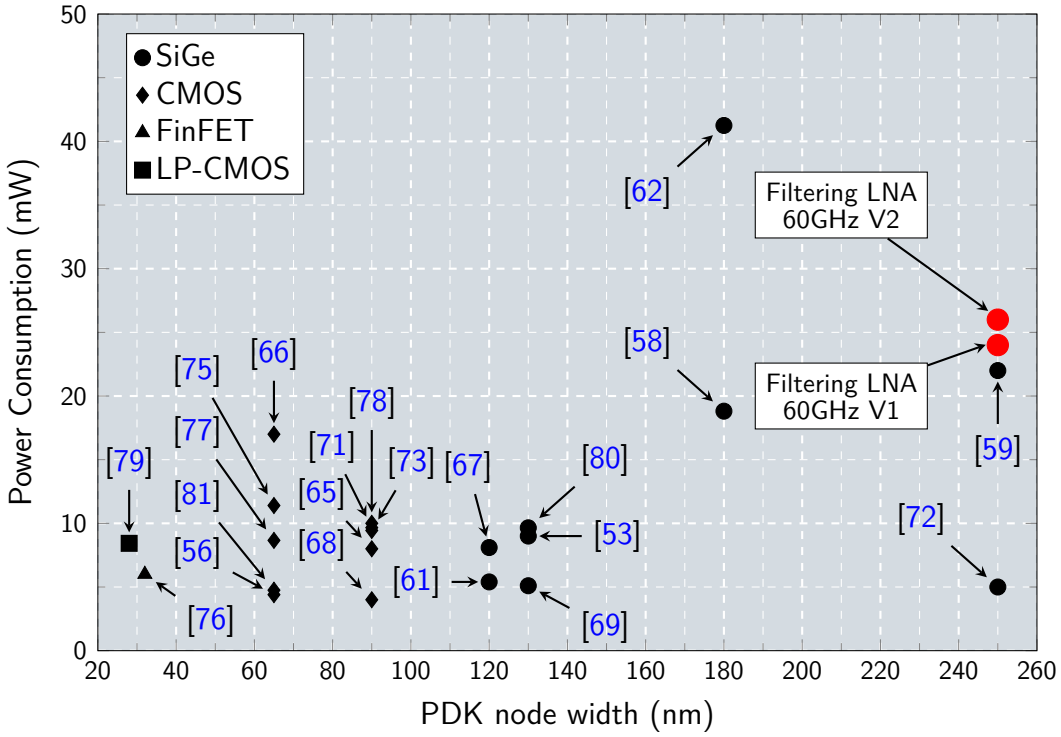


Figure 5.22: Performance comparison on power consumption by stage of a number of amplifiers found in literature. Detailed table with other variables can be found at 4.3.

5.3 Discussion

In the chapter 4 it is shown that a LNA must be conceived to offer a maximum signal gain, and minimum noise, in such a way to maximize the signal-to-noise ratio. To achieve these characteristics in mm-wave has long be proved to be an arduous task. Furthermore, in a system co-design environment, circuit designers have to be capable to visualise each influence of the the overall system. Although the difficulties, such design environment gives to the designer engineer the possibility to change the system on both circuit and component level at the same time.

For these reasons, in this chapter a study of about how to use component specificities of QuBIC transistors to optimize the design topology characteristics is developed, this way to achieve not only the LNA specifications, but also to reduce the dimensions of the fabricated circuits at mm-wave. The opportunity to change component variables (transistor in this case)

allows the designer to ease other design constraints, such as adaptation and circuit dimension.

To achieve dimension optimization we have considered small passive component dimensions, what influence directly the transistor dimensions. A large number of transistor simulations were performed so it could be chosen according *gain*, *noise* and *adaptation*.

During the development of this work three LNA circuits were sent to fabrication, two of them were co-designed in system level with resonator filters (studied in chapter 3) what permited to increment the knowledge on about how to perform during co-design simulations on system level, in this case with the LNA and the ring resonator.

At the time of this writing the second version of the 60 GHz LNA circuit developed in this work perform as well as the others SiGe:C LNA at the same frequency (Table 5.2), but with better attenuation on side frequencies due to the filter ring. Unfortunately It was not possible to measure the circuit noise due to the lack of equipment on the laboratory. We hope that this measure could still be performed on future developments of this work.

Finally, it is important to point out that the transistor choice based on the system specification as performed can be extended to any component or technology, and therefore can be also used in other circuit topologies. Also, for future development it would be interesting to investigate device optimization on both component and physical level, this way reducing the search space of components consequently reducing the simulation time.

Chapter 6

General Conclusion

In a general manner a great ammount of the subject discussed in this thesis is already examined in textbooks, neverthless with the miniaturization of silicon chips new challenges to the designer engineer emerge. Passive structures that could not be fabricated in the past (inductors, capacitors, coupling structures) due to the fabrication process limitations, now can be used to push working frequencies over and over. Also, nowadays transistors have much higher f_T than ten years ago. This context makes it important to step back and explore design subjects on mm-wave and organize its utilization.

This work presents an overview about the design procedures on RF silicon circuits for mm-wave on silicon. In Chapter 2 is presented a description of about how to design reliable layouts for mm-wave analog signals. Meticulous workflow is presented with details on circuit simulation. Simulation results are compared with measurements, what corroborate with the chapter's development.

The history, development and performance of resonator rings are presented in Chapter 3 specially for the use with mm-wave on silicon for filtering purposes. In this step two designs are proposed, as a resonant filter for 60 GHz signal waves. The first version is a octagonal filter with -3 dB of insertion-loss. The second is a meander ring with the same IL, but 60 % less area. Further, a co-design environment using EM simulation for the feedlines coupling is presented. Although these structures are not state-of-the-art *per se*, their overall performance are compared to what is found in literature, and instigate further investigations.

Chapters 4 and 5 presents a detailed co-design procedure on about how to perform for LNA design and the design and analysis of a filtering LNA. The co-design of LNA is both the LNA circuit design and component definition, therefore a custom circuit can be designed in order to be in conformity with the system specifications. Tree LNAs were fabricated and measured. These design met the specifications and demonstrate good performance, what validate the design procedure. Although it were not possible to measure the NF, the meander version of the filtering LNA presented the same gain of the literature but with a passband response, what places this circuit in the state-of-the-art for this technology (SiGe:C 0.25 µm).

Albeit each chapter is intended to be self contained they can refer to each other in some specific passages.

As can be seen through this manuscript, the contribution of this work as to the state-of-the-art lies mainly to the RFIC design for mm-wave. Although great attention has been given to the receptor side of the transceptor (LNA, filter and mixer), some specific aspects to the circuit design have to be taken into account. That said, as this work is driven to circuit simulations the used technology is a restriction. For example, the transistor dimension is imposed by physical models of the technology, also the dimension of the ring resonator is limited due to the height of the metal layer between other things, and finaly the power consumption is due to the technology drive currents. These limitations can be further addressed.

Actually, there are many discussions that were opened by on this work that can gradually be investigated, for example:

1. The circuit oriented transistor parametrization for optimal performance.
2. Use of other CMOS technology in order to reduce filter dimensions.
3. Investigations on the use of smallwave theory in ring resonators.
4. Design of mm-wave Voltage Controlled Oscillator (VCO), and the use of distributed component devices.
5. Investigation on mm-wave mixers.
6. Investigation on adaptation networks for mm-wave mixers.
7. Investigation on distributed devices on Silicon.

What concerns to the knowledge dissemination, the principal result of this work that is still on hold due to limitations on measurements of noise figure at extremely high frequencies. Complementary, this work has been discussed in two publications, as listed bellow:

- MARINHO, R.S.; BARELAUD, B. ; LINTIGNAT, J. ; JARRY, B. – *Conception d'un LNA à 60 GHz en technologie BiCMOS SiGe:C 0.25 µm* – Journées Nationales du Réseau Doctoral en Micro-nanoélectronique, 2016, Toulouse.

- MARINHO, R.S.; BARELAUD, B. ; LINTIGNAT, J. ; JARRY, B. – *Réalisation d'un LNA BiCMOS SiGe :C large bande pour applications millimétriques* – 20èmes Journées Nationales Micro-Ondes, 2017, Saint-Malo.

To finish, this work has evolved from the idea to study general aspects of system design with the receptor side of a RFIC transceptor for 5G as object. Now that 5G is first deployed, and 60 GHz deployment is pushed farther in the future, this work is still more relevant. Most information learnt throughout many iterations on circuit analysis and design, simulation and study is presented in this work.

Appendix

A.1 Free-space path loss

With a point-to-point link it is preferable to calculate the free-space attenuation between isotropic antennas, also known as the free-space basic transmission loss, defined in [11] as:

$$L_{bf}(dB) = 20\log_{10}\left(\frac{4\pi df}{c}\right)$$

where:

L_{bf}: Free-space path loss (dB)

d: is the distance between the antennas, and

λ: is the wavelength of signal in the same unity of d.

For $\lambda = c/f$, we can re-write L_{bf} as

$$\begin{aligned} L_{bf}(dB) &= 20\log_{10}\left(\frac{4\pi df}{c}\right) \\ &= 20\log_{10}(d) + 20\log_{10}(f) - 147.55 \end{aligned}$$

with frequency (f) in hertz and distance (d) in meters.

A.2 Planning the electromagnetic simulation

To the developed circuit in this work using this modified approach (Filtering LNA 60 GHz) measurements were accurate with simulated results, validating the methodology. Notwithstanding, material and method used in this approach have to be pointed out.

CAD design software Cadence® Virtuoso® and Keysight® Momentum® offer good integration between design and EM simulation. It is possible from Virtuoso® first to design and then, following quick procedure, to EM simulate in Momentum® and then to came back to Cadence® Spectre® to perform s-parameter (or other) simulation.

During simulation the designer have to be attentive to EM simulation options given by Momentum®, a bad choice take in the setup time can lead to infinite computation time. Most important setup variables are: simulation mode, and mesh related parameters.

Momentum® offers two simulation modes named *RF mode*, and *microwave mode*. The first one have a small lack of accuracy on results caused by neglected radiation effects; in this mode, as frequency increases and radiation effects become more important, the accuracy of the Momentum® RF models declines smoothly. Second simulation mode is the *microwave mode*, that is based on full-wave electromagnetic functions and take into account the radiation effects of design, and therefore require more memory and processing time.

Mesh related parameters controls the quantity of polygons a simulated circuit will be divided, large quantity of polygons means more calculation therefore more computation time, and vice versa. Most problems related to mesh division is associated with both variables *mesh frequency* and *mesh density*. Say:

- Mesh frequency: Is related with the maximum wave length (λ) simulated. It is a dimensional value of the circuit taken into account during simulation
- Mesh density: This value sets the number of division *Mesh frequency* will have. Minimum polygon length will have *Mesh frequency* over *Mesh density* value.

It can be easily seen that mesh division is highly dependent of circuit layout complexity; for example, Figure A.1 illustrate mesh with different mesh densities calculated with Momentum® software, the actual design measures 45×17 μm^2 and the maximum mesh frequency used in this simulation is 50 GHz. If the layout have many layers, for example, quantity of polygons can increase quickly. And it is a designer competence to find the optimal mesh variables that simulates in a finite time.

One last possibility to optimize simulation without loss of accuracy is the use of via simplification. In this case, if multiple vias are posed side by side, designer can deliberately draw a large polygon on via layer connecting all vias; via connection is a small component and so dimension is usually way smaller than the maximum λ frequency simulated, when it is the case then this modification handle small (or none) influence on the EM modeled circuit while

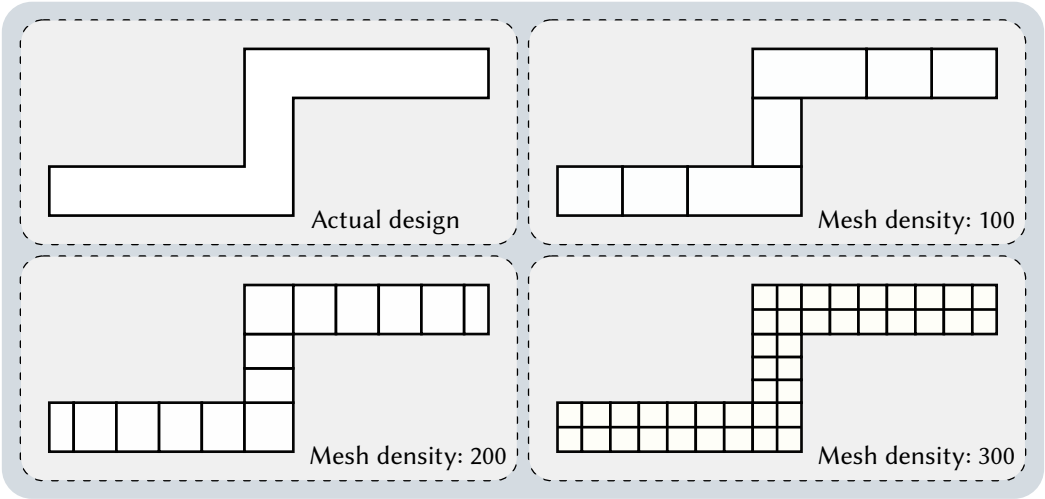


Figure A.1: Mesh density example taken with Momentum® software.

reduce computation time considerably.

Second version of filtering LNA circuit developed in this work would take, for example, less than thirty minutes to completely model full circuit (passive components) without RF and DC pads. In this case the maximal simulated frequency was 60 GHz with a 120 GHz mesh frequency, mesh density equal 10, and RF mode simulation[1]. Via simplification was also settled because some designs contained inductor of the design kit, and in this case large computation time was performed due contact vias between poly layer and metal 1 layer on these inductor designs.

A.3 Matrix transformation table

Table A.1 shows the two port circuit transformation for its $[z]$, $[y]$ and $[ABCD]$ models. In this table $[a]$ stands for $[ABCD]$ matrix.

[1]this configuration was usually taken in previous version of the design, each time design approaches final version these numbers increase.

Table A.1: Transformation matrices

	$[z]$	$[y]$	$[a]$
$[z]$	$\begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix}$	$\frac{1}{\Delta[y]} \begin{bmatrix} y_{22} & -y_{12} \\ -y_{21} & y_{11} \end{bmatrix}$	$\frac{1}{a_{21}} \begin{bmatrix} a_{11} & \Delta[a] \\ 1 & a_{22} \end{bmatrix}$
$[y]$	$\frac{1}{\Delta[z]} \begin{bmatrix} z_{22} & -z_{12} \\ -z_{21} & z_{11} \end{bmatrix}$	$\begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}$	$\frac{1}{a_{12}} \begin{bmatrix} a_{22} & -\Delta[a] \\ -1 & a_{11} \end{bmatrix}$
$[a]$	$\frac{1}{z_{21}} \begin{bmatrix} z_{11} & \Delta[z] \\ 1 & z_{22} \end{bmatrix}$	$\frac{1}{y_{21}} \begin{bmatrix} -y_{22} & -1 \\ -\Delta[y] & -y_{11} \end{bmatrix}$	$\begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix}$

A.4 Large RF band Mixer realization – from mm to cm Waves

Mixers are components capable of translate a given signal in frequency. Although time-invariant linear circuits are normally wanted to perform a large set of RFIC tasks, linear systems cannot operate in frequency, and therefore frequency translation must be performed with a non-linear use of the components.

The operation performed by a given mixer is the time domain multiplication of two signals, which can always be seen as a convolution on the frequency domain. This operation is represented in time domain as in the equation A.1.

$$A\cos(\omega_1 t)B\cos(\omega_2 t) = \frac{AB}{2}\left[\cos(\omega_1 - \omega_2)t + \cos(\omega_1 + \omega_2)t\right] \tag{A.1}$$

This multiplication results in a signal with two different components, one in frequency the $\omega_1 + \omega_2$ and other in the frequency $\omega_1 - \omega_2$. Also, the output signal have its amplitude proportional to the product of the A and B amplitudes. The result of equation A.1 have (in general) two components. One is above the central frequency of the input signal, and the other below the input signal, both frequencies are used depending on the mixer. In the *up-converter* mixer version the interesting signal have frequencies above the frequency of the input signal and is used mainly in transmitters circuits. On the other hand, the *down-converter* version of

mixers are used normally on the receptor side.

This shift in frequency is obtained due to the non-linear reponse of the components used in the mixer circuit. For instance if a sinusoid is applied to such systems, the output generally exhibits frequency components that are integer multiples of the input frequencies, these components are called *harmonics*. This *mixing frequencies* effect happens because the RF signal passes throughout a switch that changes its state at LO frequency generating a *switched* version of the original signal that contains the IF component.

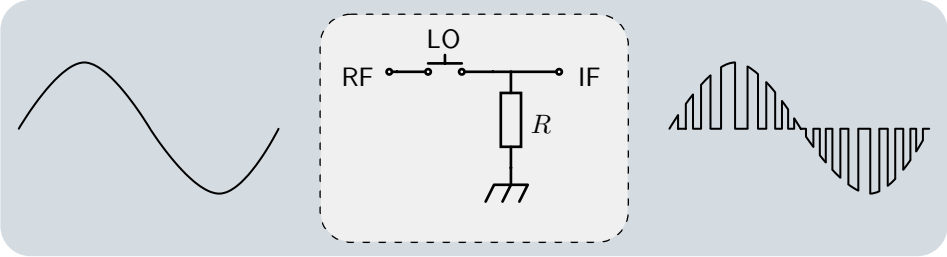


Figure A.2: Input and output waveforms of a given mixer.

In the circuit of Figure A.2, if the LO signal open and closes the switch as a perfect square wave $S(t)$ of period T_{LO}, then, the output voltage can be calculated as $V_{out} = S(t)RI_{RF}$. Therefore, if both RF and LO signals were perfect sinusoidals, the IF output is a perfect representation of equation A.1. However, $S(t)$ is a swithing response with (ideally) fast state changes due the square nature of the signal, what implies a great number of harmonics in the output signal, including the IF frequencies.

A.4.1 Mixer Classification

Due to the nature of the mixer circuit operation, mixers can be designed to convert RF signals to IF frequencies that are above or below f_{RF}. When the mixer is designed to generate IF frequencies that are below f_{RF}, it is called a *down-converter* mixer, and in this complementary case it is called *up-converter*. Although both are used to convert signal frequencies, up-converter mixers are used in the transmitter side of a communication system in order to convert IF signals (usually band-based signals) and deliver RF signals to the power-amplifier. Down-converter

mixers in its turn are used on the receptor side to translate RF frequencies into IF frequencies so they can be processed, as on a superheterodyne receptor.

As the mixer performs the operation stated in equation A.1, it can be used as an *up-converter* or a *down-converter*, depending on the system specifications such the isolation on each port. For example, Figure A.3 ilustrate the signal input/output relation on both mixers.

(a) Down-converter mixer (b) Up-converter mixer

Figure A.3: System level symbol representing up-converter and down-converter mixers.

In some radio systems the signal chain is differential in order to reduce noise interference. In such context, a mixer that accomodates a differential LO signal but single ended RF is called *single-balanced* mixer. On the other hand, if a mixer operates with both LO and RF differential signals, it is called *double-balanced* mixer.

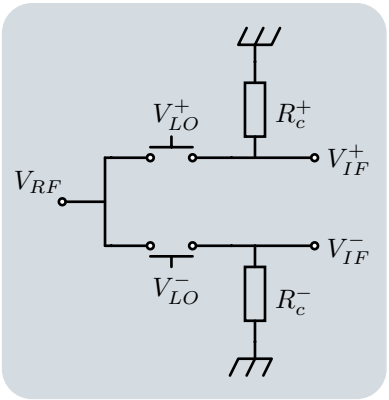


Figure A.4: Single balanced mixer.

The single balanced mixer is an efficient approach whereby two switches are driven by differential LO phases, thus comutating the RF input to the two outputs even with a single-ended RF input, what facilitates the design of subsequent stages. If the circuit is simetric, then it vanidhes the LO-RF feedthrough due its LO signal differential phase.

Although single balanced mixers are good for providing differential output, they suffer from

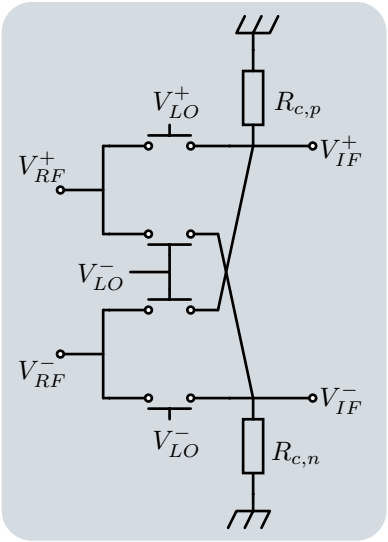


Figure A.5: Double balanced mixer.

significant LO-to-IF feedthrough. In particular, denoting the coupling of V_{LO}^{+} to V_{IF}^{+} by $+\alpha V_{IF}^{+}$, the same happens to its differential network where the coupling of V_{LO}^{-} to V_{IF}^{-} is denoted by $+\alpha V_{IF}-$. Therefore it can be observed that $V_{IF}^{-}V_{IF}^{-}$ contain an LO leakage equal to $2\alpha V_{LO}$.

Finally, active mixers are circuits also used to give gain to the IF signal, and so improving the overall system SNR. On the other hand, if on the context of active mixers we talk about gain, when the mixer do not add gain to the output signal, then it is called *passive* mixer, and the input-output ratio is called Conversion-Loss (CL).

Gilbert Cell

Two single-balanced mixers can be combined to form a double-balanced mixer. Both RF and LO inputs of the mixer are now differential. The active double-balanced current switching mixer is also termed as Gilbert cell mixer as show in Figure A.6.

The LO drive should be large enough to make the differential pair act like current-switching switches. The two single-balanced mixers are connected in anti-paralle1 as far as LO signal is concerned but in parallel for RF signal, therefore, the LO terms are cancelled at the output port. In addition, the interconnection of the outputs causes the drain of the LO quad transistors to act as a vimial gound not only for LO and RF frequencies but also for the even-order spurious frequencies [83]. Hence, no special circuitry is required to provide RF and LO short at the drain

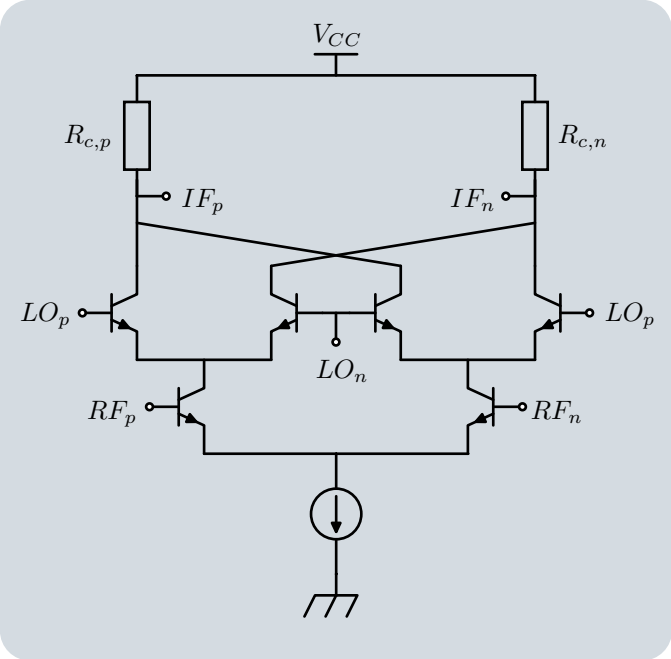


Figure A.6: Gilbert Cell.

of LO quad. Consequently, this mixer provides a high degree of LO-IF isolation easing filtering requirements at the proceeding receiver stages. The major drawback of double-balanced mixer is the higher power consumption, because of twice the number of devices as compared to a single-balanced mixer and also due to the fact that al1 the active devices should remain in saturation region of operation and a current source is ofien necessary for proper biasing. Moreover, mismatches between different devices and signal path lengths limit port-to-port isolation and cancellation of the harmonics at the output IF port,

A.4.2 Parameter Performances

Since mixer are frequency conversion devices, the primary electrical specification is its conversion gain (or conversion loss in case the mixer is passive); along, the signal of interest have $f_0 = f_{IF}$ and the two input are unwanted frequencies at the output, so logically LO-to-IF and RF-to-IF isolation are important to characterize how the mixer signals are suppressed at the inputs and output ports. Other important isolation value is LO-to-RF because it can drive the antenna and radiate. The three mixer isolation main characteristics are described in table A.2.

Table A.2: Parameters of isolation small description and importance.

Isolation Parameter	Importance
LO-to-RF	The large LO signal appearing at the RF port could actually make it to the antenna and radiate, specially if $\|S_{12}\|$ of the LNA is poor.
LO-to-IF	The large LO signal appearing at the IF port may require extensive filtering to ensure that its large amplitude does not overdrive downstream circuits.
RF-to-IF	One of the isolation of lesser importance; filtering usually can minimize this since the RF signal is small.

Many mixer variants exists nowadays although the well known topologies of single and doubled balanced mixers. It happens because the mixing operation ultimately depends heavily on the circuits specifications, and therefore on the circuits surroundings. This statement is way more important if miniaturization is taken into account for high frequency circuits.

Albeit all these existent mixer variants, complex structure (as Gilbert cells) are still preferable since extra transistores can be used with virtually no extra cost, what can improve the mixer circuits performance.

A.4.3 Mixer Implementation

This mixer implementation is based on the Gilbert Cell and uses the same BHT transistors of the LNA prsented in chapter 5, due its high f_T frequency, therefore the same circuit will be used in different system designs independent of the RF frequency. The only drawback to this approach is the input and output adaptation, that is frequency dependant.

Two system structures were designed, the first is the same of the Gilbert cell topology presented in Figure A.6. In the second design we choose to try increase the gain of the mixer adding active charges in the place of the $R_{c,p}$ and $R_{c,n}$ resistors, what would also ease the output adaptation with the increase of the mixer output resistance. Of course that in this last case output impedance shall be carefully evaluated. Figure A.7 show the output power due the local oscilator power input (P_{LO}).

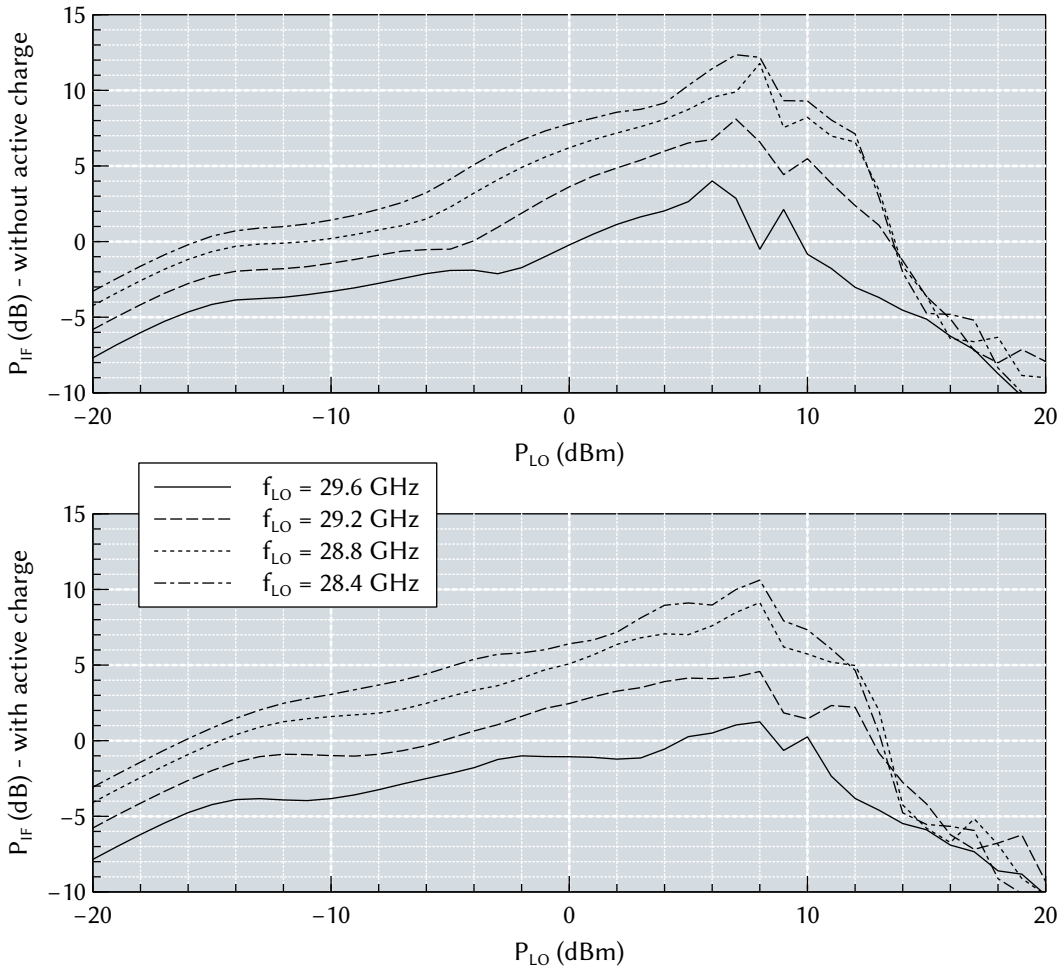


Figure A.7: Mixer conversion-gain due to the local oscilator input power. These graphs illustrates the importance of P_{LO} to the output power signal P_{if}. The frequency of IF output signal is referred to $f_{IF} = f_{RF} - f_{LO}$, where f_{RF}=30 GHz, and f_{LO} varies with 400 MHz step.

As waited, the power gain is higer when f_{LO} is more distant from f_{RF}. For instance, the option to evaluate the influence on parameters of the mixer with the use of an active charge in the gain amplifier is taken. At first, we tried to adapt *pmos* devices as active charge, but the mixer was designed to a fixed voltage drop at the charge component, what imposes that the pmos transistor should have high width, what impact on its f_T affecting the performance of the system. Also, the maximal f_T of *pmos* transistors for QuBIC is around 30 GHz, and therefore bipolar transistors are prefered. Figure A.8 presents the signal power of the output mixer signal with the variation of the input RF signal for a fixed value of P_{LO}=4 dB.

We note that the mixer with the active charge presents a lower band. This can be explained

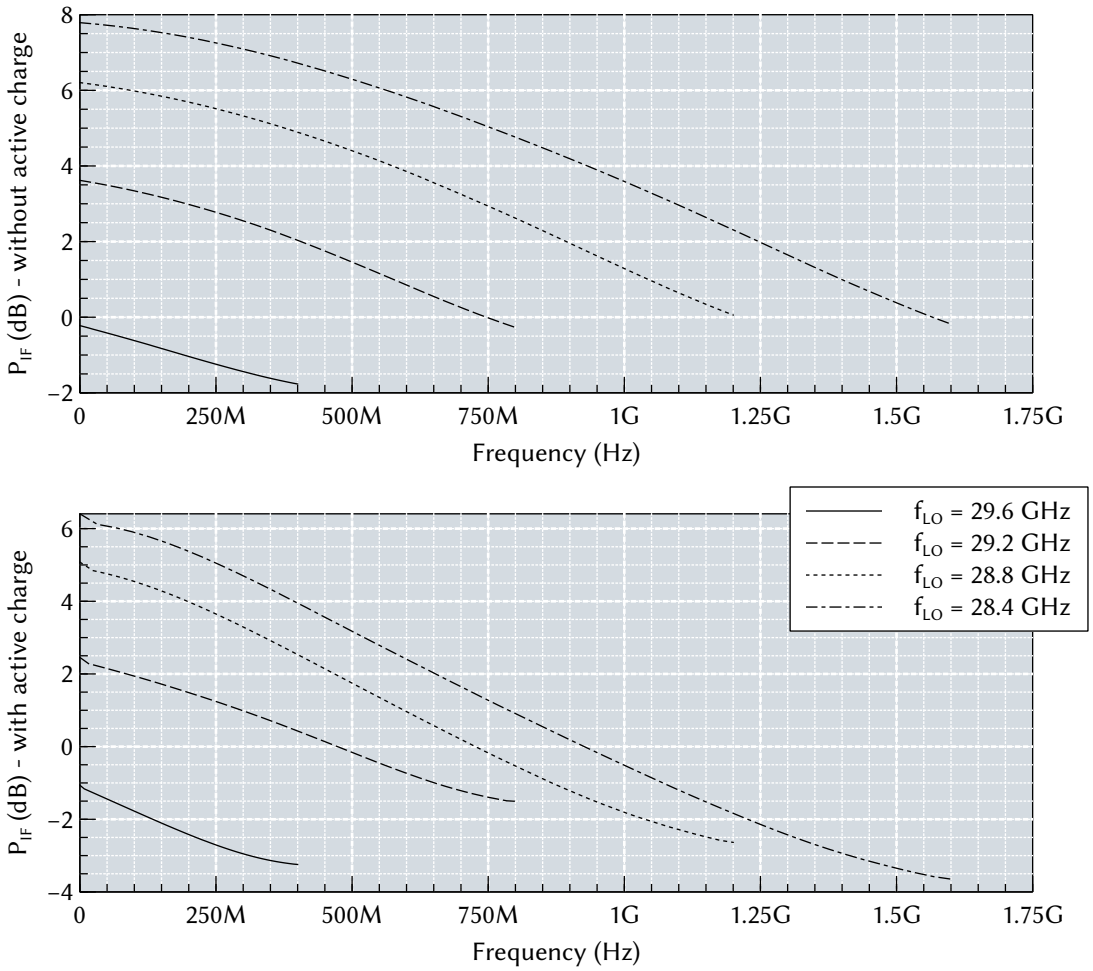


Figure A.8: The conversion-gain due to the RF signal frequency sweep for P_{LO}=4 dBm. The frequency axes are relative to $f_{IF} = f_{RF} - f_{LO}$. Therefore for f_{LO}=29.6 GHz frequency zero at the graph is 400 MHz, for f_{LO}=29.2 GHz frequency zero is 800 MHz, and so on.

due the intrinsic capacitances of the transistor at the charge. Also the gain is smaller when compared with its no active version, what is justified by the mixer output adaptation. More investigation must be performed on transistor sizing for optmization pourposes on mixer design.

Tables A.3 and A.4 shows the isolation for both layouts, although the mixer with resistive charge performs slightly better, both mixers presents good isolation due RF-to-IF and LO-to-IF. Moreover, these Gilbert cell circuits are designed to work with a high frequency shift, from frequencies surrounding 30 GHz to some hundreds of megahertz. This specification have a high influence on the conversion gain of the amplifier because f_{LO} have to be near of f_{RF}.

Figures A.9 and A.10 shows the frequency translation for f_{LO}=29.6 GHz, 29.4 GHz, 28.8 GHz

Table A.3: Simulated values for isolation on the Gilbert cell circuits using resistive charge.

	f_{LO}=29.6 GHz	f_{LO}=29.4 GHz	f_{LO}=28.8 GHz	f_{LO}=28.4 GHz
RF-to-LO	below -20 dB	below -84 dB	below -94 dB	below -85 dB
RF-to-IF	below -70 dB	below -64 dB	below -70 dB	below -48 dB
LO-to-IF	below -70 dB	below -82 dB	below -82 dB	below -84 dB

Table A.4: Simulated values for isolation on the Gilbert cell circuits using active charge.

	f_{LO}=29.6 GHz	f_{LO}=29.4 GHz	f_{LO}=28.8 GHz	f_{LO}=28.4 GHz
RF-to-LO	below -20 dB	below -35 dB	below -75 dB	below -40 dB
RF-to-IF	below -85 dB	below -88 dB	below -81 dB	below -85 dB
LO-to-IF	below -82 dB	below -87 dB	below -72 dB	below -77 dB

and 28.4 GHz for both mixers. In Figure A.10, it can be seen that the active charge mixer in Figure A.10 reduces the gain according to this frequency, what do not corroborate with what is shown in Figure A.8. It happens because of the simulation from this last do not take into account the f_{RF}, and uses only the steady state model of the circuit. On the other hand, Figures A.9 and A.10 were obtained performing transient analysis and taking the Fourier transform of the result.

Further, it is observed that a wideband resistive output is particularly important if it is to achieve the highest dynamic range. This wideband resistance is difficult to obtain with active charges in mm-wave due the filtering carachteristic of the transistor. In order to bypass this difficulty, buffer stages can be used to simulate a high load seen by the mixer with the drawback of current use. For systems with no size constraints, passive components as baluns or transformers can be used. In the case of the proposed circuits if a band of 400 MHz is needed, then both circuits can be used with a small difference on IF signal.

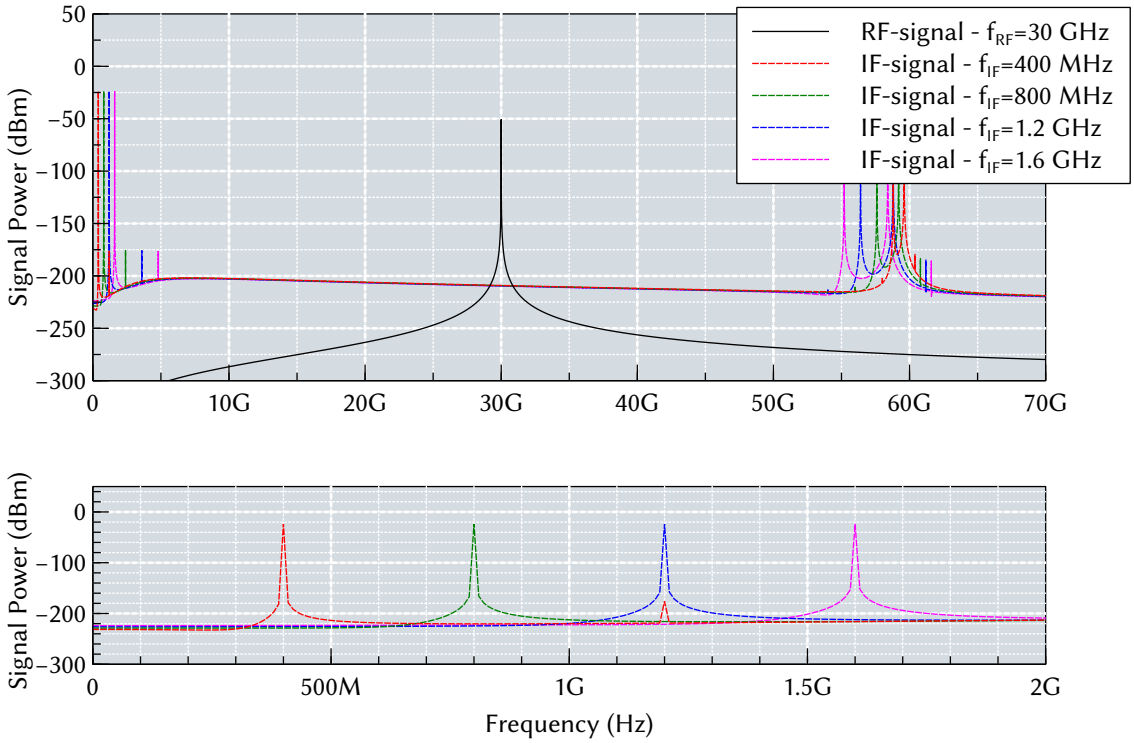


Figure A.9: Frequency mixing generated frequencies for the mixer with output resistors. Bottom graph is a *zoom* to the generated frequencies due f_{LO}={29.6, 29.4, 28.8, 28.4} GHz.

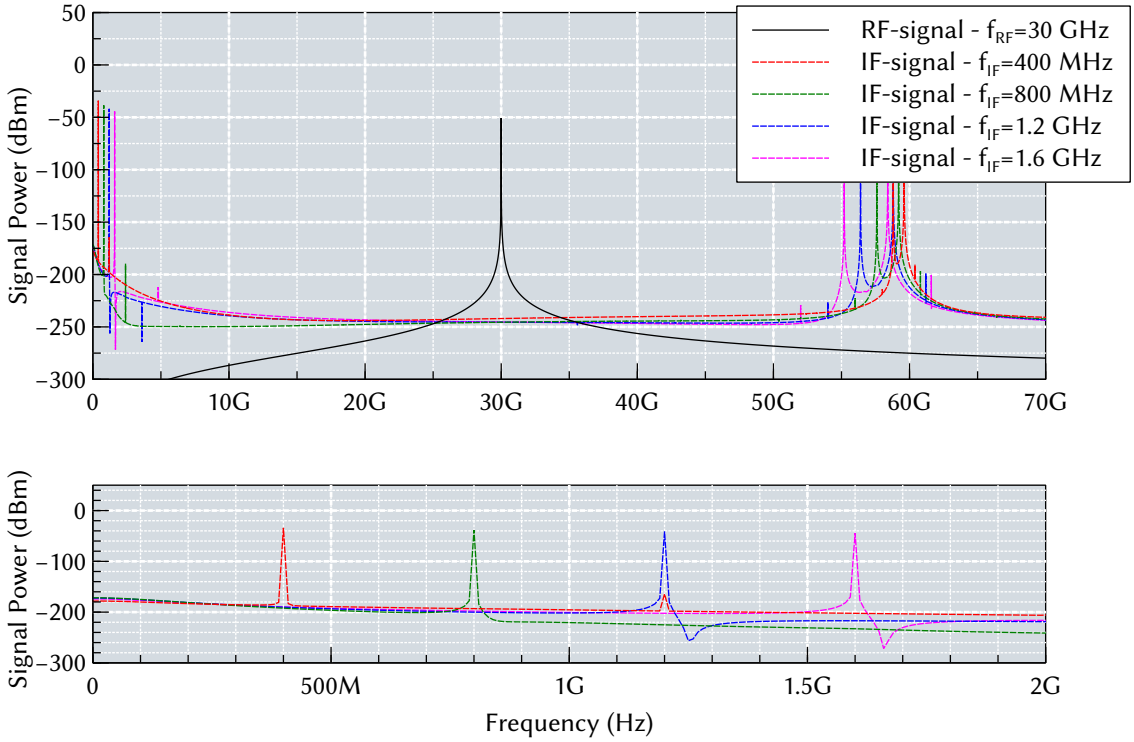


Figure A.10: Frequency mixing generated frequencies for the mixer with active charge. Bottom graph is a *zoom* to the generated frequencies due f_{LO}={29.6, 29.4, 28.8, 28.4} GHz.

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Méthodologie de co-conception d'un Filtre-LNA de 60 GHz

Résumé : Ce travail montre les résultats et discussions à propos du projet partagé des structures pour un récepteur radio-fréquence des ondes millimétriques. Deux structures ont été étudiés : Le LNA et le resonateur en anneau. Ces structures ont été développes en utilisant des nouvelles techniques de projet de circuit micro-électroniques et utilisation des outils CAD. Les circuit ont été fabriqués avec la technologie QuBIC NXP® BiCMOS SiGe:C de 0.25 µm. Les résultats de mesure sont en conformité avec l'état de l'art pour des LNA.

Mots clés : LNA, ondes millimétriques, MMIC, projet de circuit micro-électronique , resonateur en anneau.

Co-design Methodology of 60 GHz Filter-LNA

Abstract: This work presents the results and discussions about shared design (co-design) of structures for a RF receptor in millimetric waves. Two structures were mainly studied: The LNA and the resonator filter. Both structures were developed using novel microelectronic circuit design techniques and with the extensive use of CAD software. The circuits were fabricated using a 0.25 µm BiCMOS SiGe:C QuBIC technology from NXP® semiconductors, and the measurement results are in conformity with the state-of-the-art.

Keywords: LNA, mm-wave, MMIC, circuit layout design, ring resonators.

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