Thèse de doctorat

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ECOLE DOCTORALE SCIENCES ET INGÉNIERIE POUR L'INFORMATION

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Présentée et soutenue par

PoornaKarthik NAKKALA

le 18 Juin 2015

Pulsed I-V and RF characterization and modeling of AlGaN/GaN HEMTs and Graphene FETs

Thèse dirigée par Michel CAMPOVECCHIO et Audrey MARTIN

JURY:

Juan Maria COLLANTES	Professeur, Université de Bilbao	Rapporteur
Cristell MANEUX	Professeur, Université de Bordeaux, IMS	Rapporteur
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Université de Limoges

To my mother and father

To all, I thought about

"We were saying how very important it is to bring about, in the human mind the radical revolution. The crisis is the crisis in consciousness, a crisis that cannot anymore accept the old norms, the old patterns, the ancient traditions, and considering what the world is now, with all the misery, conflict, destructive brutality, aggression and so on. Man is still as he was, is still brutal, violent, aggressive, acquisitive, competitive, and he has built a society along these lines"

—Jiddu Krishnamurti

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General Introduction

Relevant societal issues in which nanoelectronic is expected to give an important contribution are Health, Transport, Security, Energy, Environment, and Communications. Indeed, nanoelectronic will enable the development of smart electronic systems by receiving, storing and transmitting information, usually in digital form to interact with the outside world. We note an increasing request for the development of new components and electronic circuits. During the last years, the miniaturization of integrated circuits and the increase of integration density induce compatibility problems between new materials and current technologies. Therefore, future components, using smaller size going down to nanometer scale, will improve significantly the reliability and the integration of systems. The classical approach of reducing sizes of current technologies seems to reach limits and leads to difficult and complex problems (short channel effect, interconnections, tunnel effect …) so that the features of nanodevices appear to be the key solutions facing the goal of more integration and more complexity.

The research community has been attracted by the potentialities of Graphene materials (high carrier mobility even at room temperature). Graphene appears as a promising candidate to make the future generation of high frequency electronic devices, in particular Field Effect Transistors (FET). One of the main advantages of graphene comes from its planar structure. Such long-sought goal is not conceivable without the required development of measurement and modeling tools well suited to the technological process of nano-components (CNTs, Graphene). The research task and objective target the characterization and the modeling of new graphene nanodevices. Measurement tools will be developed and matched to the characterization of various nanodevices with their specific constraints. Simultaneously, measurements provided by the experimental set-up will be used for the nonlinear modeling process that will be conducted from upstream electrical topologies with a behavioural approach. It is essential to go up to the development of accurate models including the new characteristics of these nanodevices in order to establish a strong link with technological aspects, and to perform feedbacks between technological and characterization processes. Therefore, one of the most important issues of characterization and modeling tools dedicated to nanodevices is to develop the specific expertise required to establish the rules of the feedback between manufacturing and model parameters. The final aim is to efficiently explore performances of such nanodevices as well as to estimate their limits.

On the other hand, Gallium Nitride (GaN) devices have grown into several markets with many performance advantages. A new generation of high power transistor has emerged.

GaN High Electron Mobility Transistors (HEMT) exhibits high power densities coupled with high breakdown voltages, high cut-off frequency as well as high temperature capabilities. Nevertheless, the design of microwave power amplifier remains a difficult task for the wireless communications industry. Despite advantages of GaN technology, designers have to deal with parasitic effects such as thermal effects and especially trapping effects. Even if GaN transistors have matured dramatically over the last few years, the existence of dispersion effects observed in wide-bandgap devices has limited the initial expectations. This study makes a contribution to the understanding of trapping effects in GaN HEMTs. The characterization of microwave power transistors is an important field with many interesting engineering challenges leading to a new interesting topic with the development of model extraction techniques.

In this context, the first chapter introduces thermal and trapping effects that afflicted nowadays III-V semiconductors used for high power RF and microwave applications. Then, an overview of well-established pulsed I-V and [S] parameters measurement techniques developed at XLIM laboratory to characterize III-V compound semiconductors (high frequency and high-power transistors such as GaN HEMTs) is presented. Moreover, the aim of this work is to assess the high-frequency performances of graphene FETs. In this way, DC, pulsed and RF measurement techniques and setups are developed and dedicated to accurate low-current measurements of graphene FETs. This new setup based on the Keithley 4200 semiconductor characterization system (SCS) with an additional pulse measurement unit (PMU-4225) offers specific features of sensitivity and pulse resolution.

The chapter II presents dynamics of trapping effects in AlGaN/GaN HEMTs using specific time-domain pulsed I-V characterizations to determine current collapse (kink effect) and drain lag emission/capture times depending on the electrical history on the device. The trapping phenomenon is affected by electrical history, temperature and maximum drain voltage. The measurement setup and the associated characterization process offer an efficient way to identify and quantify trapping dynamics in AlGaN/GaN HEMTs. These low frequency effects have a great impact on power performances when the device operates with modulated signals and especially under pulsed mode as it is the case in radar applications. An accurate modeling of these trapping effects is of prime importance for efficient circuit designs encountered in telecommunication and radar signals.

The chapter III presents an overview on the physics of graphene 2D atomic crystal structure. Later graphene's basic electronics properties followed by different graphene

synthesis techniques and their pros and cons are discussed. This work was carried out in collaboration with Professor Happy from the IEMN Laboratory at Lille who allowed us thanks to a relevant technological contribution, to characterize and model three types of wafer-scale graphene FETs. DC/Pulsed I-V measurements and high-frequency S-parameters measurements of three different graphene transistors namely, Epitaxial Graphene Nano Ribbon FET (Epi GNR-FET), Epitaxial Graphene FET (Epi G-FET), and Chemical Vapor Deposition Graphene FET (CVD G-FET) have been realized. An equivalent nonlinear circuit model will be presented and validated in a broad range of operating conditions for the three types of graphene FETs. The extraction method of model parameters is based on the characterization of three specific technological structures called PAD, MUTE and FET integrating only the coplanar access structure, the FET without graphene, and the entire graphene FET respectively. The model will only take into account the transport behavior due to n-type carriers (unipolar) above the Dirac point. This nonlinear model has the advantage of an easy implementation in commercial CAD tools.

Finally, conclusions are made and possible new work directions will be discussed and outlined like technological challenges.

I. Development of Pulsed Measurement setup for GaN HEMTs and Graphene FET

I.1 Introduction

High data communication systems have introduced new high spectral efficient modulation techniques and standards such as LTE-A (Long Term Evolution-Advanced) for 4G systems which is demanded by the wireless market. This demand for wireless devices in commercial and military continues to grow and within the market of high power transistors for applications such as phased array antennas, base stations, radars etc... The microwave power transistors are the workhorse of the wireless communication industry. The different transistor technologies that fill these requirements include MESFET, HEMT, HBT, pHEMTs, LDMOS, as they offer high cut off frequencies, high oscillation frequencies and medium and high operating power [1]. These transistors must be measured for experimental evaluation of their microwave performances, in order to identify their optimum operating conditions. For cost effective High Power Amplifier (HPA) design to production cycle, rigorous computer-aided design (CAD) transistor models are essential to reflect real response with increasing power level and channel temperature.

The literature shows that static DC-IV measurements without separating electro thermal (self-heating) and trapping (memory effects) modeling can lead to inaccurate RF models[2]-[3]. The aim of this thesis is to explore and implement pulsed measurements for characterization of RF transistors. In pulsed measurements, depending on the pulse width and duty cycle, the slow process like self-heating and trapping do not have time to occur. Thus it is safe to say that it is similar to RF operation of transistor [4].

The first part of this chapter is dedicated to present the physical significance of dispersion phenomenon namely thermal and trapping effects that are responsible to degrade the RF transistor performances, particularly AlGaN/GaN HEMTs. Later, classical pulsed I-V setup and pulsed measurement techniques previously developed by researchers to characterize and model the medium and high power devices such as GaAs HEMTs, GaAs HBTs, and GaN HEMTs will be presented [5]. But, the brief introduction on AlGaN/GaN HEMT material will be presented later in chapter II as an introduction to our experimental work on these III-N devices.

The second part is dedicated to the development of a pulse setup for graphene FET characterization. In this part, a brief presentation of nano device characterization challenges

will illustrate why such a pulse characterization needs to meet specific requirements on low current measurements at very high sensitivity. This will be done by using a dedicated equipment Keithley 4200-SCS (semiconductor characterization system).

I.2 Thermal effects

Under DC operation, the transistor channel heats up uniformly. But, in the case of modulated information (RF) signal, we may find high amplitude at some time and later time low amplitude. The transistor channel heats up in response to the high amplitude signal. A short time later, the signal returned to some low value, but the channel does not cooled down instantaneously. Due to this change in temperature the transistor parameters and response will be slightly different. For example, the low level signal sees lower gain than expected because of different temperatures. Due to this, the transistor response exhibits memory of the previous signal. The time constants associated with thermal effects are in the range of microseconds to milliseconds so that the thermal time scale is longer than RF period and is closer to the envelope variation of the modulated signal. These long term memory effects can be seen in the AM-AM characteristics of RF power amplifier, as a spread around the mean gain compression curve [6]. In order to perform efficient designs, these thermal effects should be included in the transistor models by implementing a dynamic coupling of electrical and thermal signals. It is clear that the nonlinear model should accurately describe the impact of the time-varying temperature on the device behavior and performances.

We have discussed the importance of apprehending the transistor performance as a function of temperature to model the changes that occur to the material parameters. Apart from ambient temperature, transistors designed for high power densities generate heat as a byproduct of current flowing in and out at the junctions known as “self-heating”. This self-heating degrades the actual performances of the device and therefore it should be carefully characterized to include these thermal effects inside the nonlinear electrical models.

To quantify the amount of self-heating within the device, we need to look at the definition of Power-Added Efficiency (*PAE*) denoted by η in Equation I-1.

$$\eta = \frac{(P_{out} - P_{in})}{P_{dc}} \qquad \text{(I-1)}$$

where P_{in} and P_{out} are the input and output powers, respectively, at the operating frequency while P_{dc} is the supplied DC power.

The amount of power that is not converted from DC to RF is dissipated as heat in the device. The dissipated power P_{diss} is calculated in Equation I-2 from the power-added efficiency η and the DC power P_{dc} :

$$P_{diss} = P_{dc}(1 - \eta) \tag{I-2}$$

In order to represent this self-heating phenomenon inside the nonlinear electrical model, the electro-thermal modeling consists in using the electrical and thermal equivalencies to derive an equivalent circuit for representing self-heating in electrical circuit simulators. The two main parameters of the electro-thermal circuit are the thermal resistance and the capacitance, which are briefly described in the following.

I.2.1 Thermal resistance

By definition, the thermal resistance is the characteristic feature by which the material is opposing heat dissipation and heat conduction. The smaller the thermal resistance value, the smaller the change in temperature due to high thermal conductivity, while higher values of the thermal resistance lead to large increase in temperature.

To quantify the temperature increase as a function of the dissipated power, the thermal resistance has to be defined. Therefore, using Fourier's law [7] as illustrated in Fig I-1, a relationship between the incident heat flux density ϕ on the surface of a homogeneous conductive material and the gradient change ∇T in its local temperature is established as.

$$\Phi = -\mathrm{K}(T).\nabla T \tag{I-3}$$

where T is the temperature in Kelvin (K) and $K(T)$ is the temperature dependent thermal conductivity of the material given in ($W.m^{-1}.K^{-1}$). By integrating the heat flux distribution in Equation I-3 over the surface of incidence, we obtain for a given dissipated power P_{diss}, the steady state solution given in Equation I-4.

$$R_{th} = \frac{\Delta T}{P_{diss}} \tag{I-4}$$

where the resulting factor R_{th} ($K.W^{-1}$) is defined as the thermal resistance of the homogeneous medium.

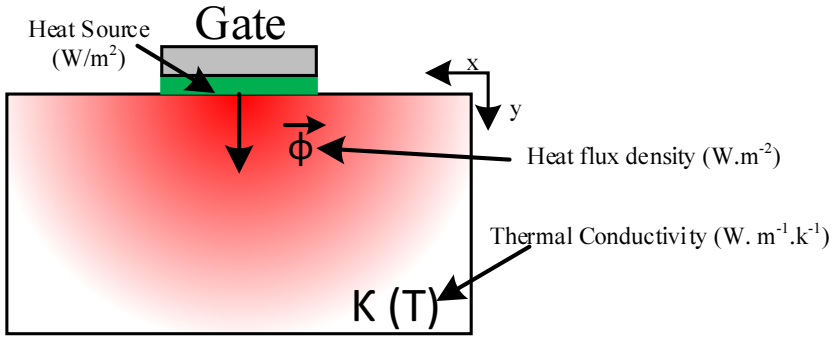

Fig I-1: Heat conduction in semiconductor material.

The steady state thermal expression can be used for any semiconductor device to calculate the thermal resistance of its material layers or the whole thermal resistance of the device. For example, the HEMT device channel temperature T_{ch} can be calculated from the given dissipated power P_{diss} and the reference temperature T_{amb} (ambient temperature). The resulting linear relationship between the channel temperature and the amount of dissipated power is written in Equation I-5 [7].

$$T_{ch} = R_{th}P_{diss} + T_{amb} \quad \text{(I-5)}$$

I.2.2 Thermal capacitance

Similarly, a more general form of Equation I-4 can be obtained for a time varying thermal analysis in semiconductor devices subjected to instantaneous time dependent power dissipation $P_{diss(t)}$. Therefore, the resulting expression for above development in time domain can be reduced to [8]:

$$P_{diss}(t) = \frac{\Delta T_{ch}}{R_{th}} + C_{th}\frac{d}{dt}(\Delta T_{ch}) \quad \text{(I-6)}$$

The first term in Equation I-6 reflects the conductive heat generation as function of channel temperature and thermal resistance, as previously explained. The second term in Equation I-6 reflects the dynamic heat flow due to the heat stored in the semiconductor material. Since this characteristic is directly related to the ability of the semiconductor material

to store heat (defined as heat capacity in materials), the resulting coefficient C_{th} (J.K^{-1}) *is* defined as the thermal capacitance of the semiconductor material. Therefore, the total instantaneous generated heat is the sum of heat flow term $\frac{\Delta T_{ch}}{R_{th}}$ and heat storage term $C_{th}\frac{d}{dt}(\Delta T_{ch})$.

I.2.3 Thermal circuit

By analogy to electrical circuit theory, the formulation of Equation I-6 is similar to the electrical equation describing the current charge and discharge through a RC network. Indeed, when replacing the dissipated power P_{diss} with the current intensity I, and the temperature T with the voltage V, the Equation I-6 reduces to Equation I-7, which calculate the current intensity I flowing through the capacitor C_{th} shunted to ground and the series resistor R_{th}.

$$I = \frac{\Delta V}{R_{th}} + C_{th}\frac{dV}{dt} \qquad \text{(I-7)}$$

This thermal-electrical analogy allows us to replace heat conduction problem as illustrated in Fig I-1 by circuit element analysis with resistors, capacitors and a current source as shown in Fig I-2. Hence, the heat conduction from one surface to another through the different materials can be simultaneously calculated with the electrical performances of the device within a circuit simulator.

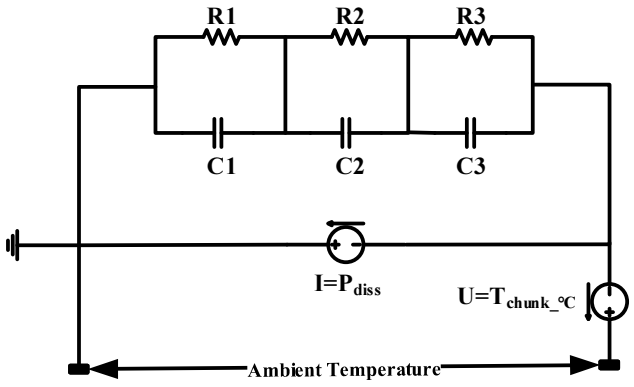

Fig I-2: An example of thermal analogue circuit implemented in a circuit simulator.

Under the transient conditions, the heat conduction is governed by the combination of thermal resistance and thermal capacitance collectively known as thermal impedance. The

$R_{th}.C_{th}$ products give the thermal time constants τ_{th} associated with the different layers stacked in conventional HEMT devices. These thermal time constants are very useful to provide the significant insight into the heating and cooling curves of a device.

I.2.4 Influence of temperature on properties of semiconductors

In the preceding sections, we have briefly discussed the physics of heat conduction to illustrate how equivalent electrical thermal circuits are used to model the heat conduction through stacks of semiconductor materials. Now we focus on the influence of temperature on the properties of semiconductors. A close analysis of the HEMT device behavior shows that its electrical behavior is highly correlated to channel temperature variation. Physical quantities such as energy band gap, carrier mobility, drift velocity, thermal conductivity, and the free carrier density are all temperature dependent. In brief, we show in the following some parameter variations with temperature, which in turn affect the HEMT device operation.

I.2.4.1 Temperature effect on energy band gap

The temperature dependence of energy band gap is given by the semi-empirical relation of Equation I-8 proposed by Varshni [9]. This behavior can be better understood if one considers that the interatomic spacing increases when the amplitude of atomic vibrations increases due to the increased thermal energy. This effect is quantified by the linear expansion coefficient of a material. An increased interatomic spacing decreases the potential seen by electrons in the material, which in turn reduces the size of the energy band gap [10].

$$E_G(T) = E_G(0) - \alpha \frac{T^2}{T + \beta} \qquad \text{(I-8)}$$

where E_G is the energy bandgap, $E_G(0)$ the value at 0 K while α and β are constants. The different parameters E_G, α, β in the Equation I-8 are listed in Table I-1 for different semiconductor materials.

	Germanium	Silicon	GaAs	GaN
$E_G(0)$ [eV]	0.7437	1.166	1.519	3.47
α [eV/K]	4.77×10^{-4}	4.73×10^{-4}	5.41×10^{-4}	7.7×10^{-4}
β [K]	235	636	204	600

Table I-1: Temperature dependent parameters of energy band gap of semiconductors.

The temperature coefficient of the energy band gap (dE_G/dT) is negative for all the semiconductors listed in Table I-1. This is illustrated in Fig I-3, which shows the variation of E_G as a function of the temperature. For example, the energy band gap of GaN and GaAs decreases by around 0.1eV with an increase in temperature from 25°C to 250°C. This in turn leads to a significant decrease of the breakdown voltage and therefore the potential output power decreased with the increase in temperature.

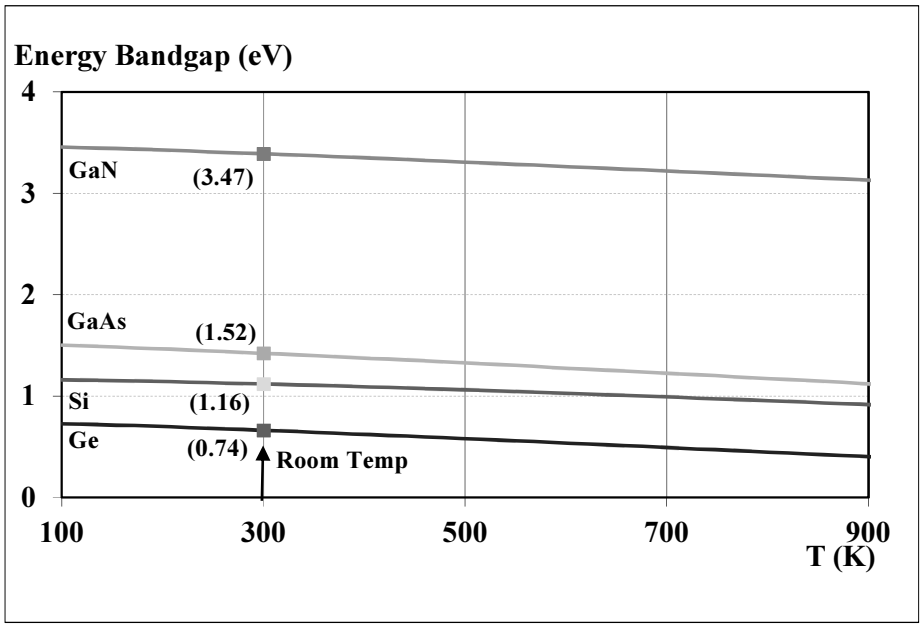

Fig I-3: Variation of energy band gap E_G of different semiconductors versus temperature [10].

I.2.4.2 Temperature effect on carrier mobility

With an increase in temperature, the electron mobility decreases [11] due to the corresponding increase of vibrations in the crystal lattice. This decrease of mobility with temperature is illustrated in Fig I-4 for GaN [12] and GaAs [13] semiconductors. It is observed

that the electron velocity in GaN is less sensitive to temperature than that of GaAs. Hence, GaN devices should be more tolerant to self-heating and clearly more suitable for high temperature operation. A decrease in drift velocity due to decreased saturation electric field is apparent, thereby the current collapses affecting the DC and RF performances of the transistors. Any fluctuations in ambient temperature or any variations in DC and RF power dissipation bring a change in channel temperature affecting the channel current.

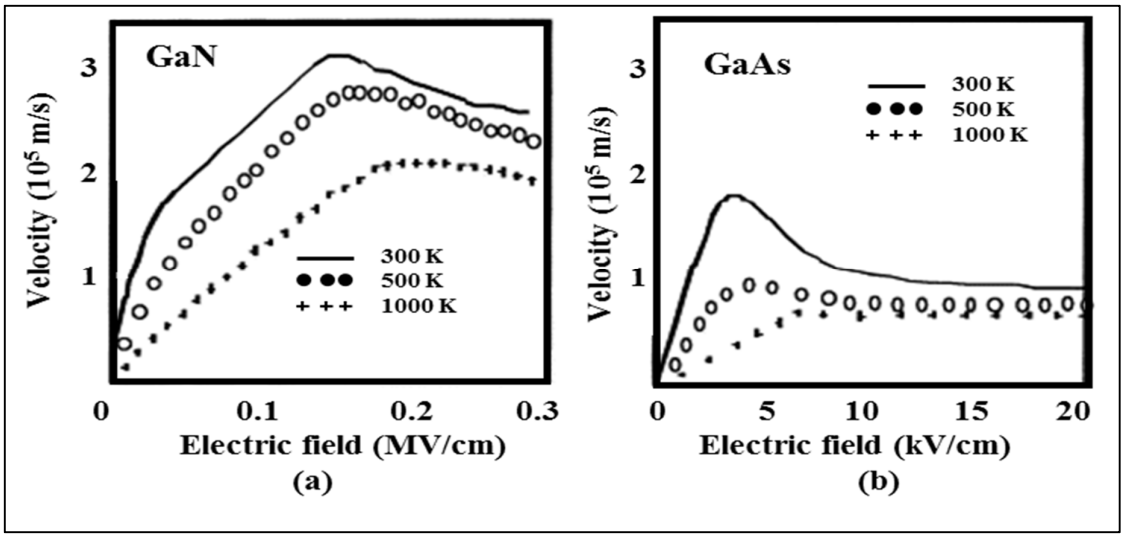

Fig I-4: Velocity characteristics versus Electric field at different temperatures for GaN (a) and GaAs (b) semiconductors [11].

I.2.4.3 Temperature effect on thermal conductivity

One important impact on device behavior is due to the temperature dependency of the thermal conductivity *K (T)*. This term has to be extracted carefully because it is the important parameter in modeling thermal sub-circuit. In literature [14], it is shown that the thermal conductivity decreases with an increase in temperature.

The following Equation I-9 gives the variation of thermal conductivity with temperature.

$$\mathrm{K}(T) = \mathrm{K}_0 . \left(\frac{T}{300}\right)^{-\alpha} \qquad \text{(I-9)}$$

where K_0 is the thermal conductivity of semiconductor material at room temperature (T_{amb} = 300K) and α is a constant. From literature [15], the values of K_0 and α are given in Table I-2 for different semiconductor materials.

	GaAs (Non-Doped)	**GaAs (Highly doped)**	**GaN**	**SiC**
K_0 (W/m.K)	45	30	190	414
α	-1.35	-1.35	-1.35	-1.5

Table I-2: Parameters of the temperature-dependent thermal conductivity (Equation I-9) for different semiconductor materials.

The Fig I-5 illustrates the decrease of thermal conductivity with temperature for GaAs, GaN and SiC semiconductors. This demonstrates the thermal advantage of GaN and SiC materials for heat dissipation but also the importance of modeling the temperature dependence of thermal conductivity for these materials when compared with GaAs.

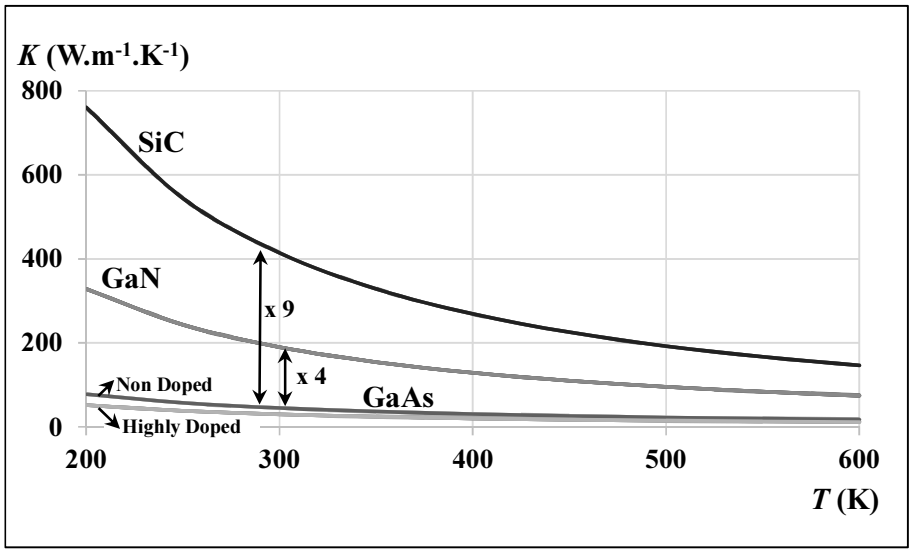

Fig I-5: Variation of the thermal conductivity (K) with respect to temperature (T) for different semiconductor materials (GaAs, GaN and, SiC) [16].

I.3 Trapping effects

The temperature is not the only physical characteristic that can give rise to dispersion effects. Trapping effects in semiconductor materials are also responsible for short and long-term memory effects. These trapping effects can result from material defects, dislocations, lattice mismatch, impurities in the crystal lattice and existence of dangling bond on the surface of transistors that act as trap centers for charge carriers flowing in conduction channel and causes current collapse. Trapping effects were known during the technological developments of several semiconductor devices like GaAs MESFETs and well understood in terms of physical mechanisms, which provide physical basis to model them by designers. Nowadays, HEMT devices replace those preceding technologies in commercial markets due to their superior properties such as high power densities, frequency of operation and better thermal properties. However, HEMT devices are also deeply affected by trapping effects, which hold them down in providing their expected theoretical performances. But, although they suffer from trapping effects, they still demonstrate better performances than previous technologies at RF/Microwave frequencies. Some reasons for these trapping phenomena, which are intrinsic to HEMT technology cannot be solved rapidly. That said, these trapping phenomena are more complex than those observed in GaAs MESFETs and not completely understood. This is the basis to find better ways to characterize these trapping effects, which can be quantified and included in CAD models later used by designers. In this section, we will examine the physical aspects of trapping effects in particular within GaN HEMTs. Later, we will present and discuss the characterization of trapping effects using pulsed I-V techniques that can account for nonlinear dispersion in current.

I.3.1 Physical mechanisms of trapping effects in HEMTs

From solid state physics, the definition of traps are the energy levels presented between the energy band gap of semiconductor materials. From an electrical point of view, these traps are responsible for electrical anomalies such as current collapse, difference between static and dynamic trans-conductance and frequency dispersion of the output conductance [17]-[18]. Indeed, these traps or energy levels have the ability to capture and release free charge carriers at different time constants. For example, GaN HEMTs usually exhibit capture time constants that are in the orders of few nanoseconds and emission time constants in the orders of few

microseconds to seconds or even more. Such time constants induce a delayed response of the channel current to the fast changing electrical command signals (RF/Microwave). The presence and identification of traps in GaAs-based devices have been studied well in recent decades [19]. Specific characterization methods were developed to find the location and the density of traps in the device structure [20], [21]. These works helped to understand the trapping phenomenon or at least reduce their densities during the device fabrication process. In the case of GaN HEMTs, the identification of traps is a very tricky point due to the non-reproducibility of measurements and invalidity in some cases [22]. Many factors can explain these limitations:

- Process: Variation of material qualities during fabrication.
- Electrical: Due to the very high values of electric field in wideband gap materials that can initiate the specific mechanisms, such as the Poole-Frenkel effects[23].
- Dislocation: The high trap densities induced by the lattice mismatched Si or SiC substrates [24].

The Shockley-Read-Hall (SRH) statistics, presented in Equation I-10 for an electron trap, gives the important characteristics of traps; their occupancy factor is determined by the balance between the capture and emission of free electrons.

$$\frac{df_T}{dt} = n.C_n(1 - f_T) - e_n.f_T \tag{I-10}$$

with

$$C_n = \sigma_n.v_{thn} \tag{I-11}$$

where, f_T is the electron occupancy ratio for deep traps, *n,* the electron concentration, σ_n, the electron capture cross-section, and v_{thn}, the electron thermal velocity. The capture rate is given by $(n.C_n)$ whereas the emission rate e_n is determined by the Arrhenius law presented in Equation I-12.

$$e_n = \frac{1}{\tau_{emission}} = A.T^2.e^{\frac{-E_A}{k.T}} \tag{I-12}$$

where A is a constant, T, the temperature, k, the Boltzmann's constant, $\tau_{emission}$, the trapped charge emission time constant, and E_A, the activation energy, respectively.

Thus, the capture rate is proportional to the electron concentration, whereas the emission rate has a strong dependence on temperature. This set of equations brings to conclusion that the emission time constants are several order magnitude longer than the capture

time constants. This peculiar behavior is very important to understand the transistor electrical characteristics under RF drive, under transient conditions and also under steady state operation.

From an electrical point of view when characterizing GaN HEMTs, the traps are separated into two types "Gate Lag" and "Drain Lag". They correspond to the delayed response of the drain current associated with V_{GS} and V_{DS} control voltages, respectively. This can be performed easily since each effect depend only on drain or gate potential. Consequently, in frequency domain, the impact of gate lag is noticeable on trans-conductance (the partial derivative of drain current with respect to gate potential), and the impact of drain lag on the output conductance (the partial derivative of drain current with respect to drain potential).

I.3.2 Drain lag effects

In GaAs MESFETs, the output current is determined by the effective channel thickness, modulated by the gate potential. However, ionized traps [25] are present in the substrate, or in the substrate/channel interface. It is also modulated by the extension of depletion layer into the active region. The injection of free electrons is determined by the drain potential, which mechanism is known as "drain-lag effect" and also "self-backgating" (*the traps act like a pseudo backgate*) [26].

In GaN HEMT's, the phenomenon is quite similar but the output current is modulated by the density of free electrons in the channel. The presence of a 2D electron gas (2DEG) is necessary to compensate the positive (piezoelectric) charge σ^+ at the AlGaN/GaN interface [27]. However, if the ionized traps are located near to the AlGaN/GaN interface, the resultant change is not zero and becomes negative but the equilibrium is kept by maintaining the 2DEG density (n_s) as shown in Equation I-13.

$$\sigma_+ = q.(n_s - Nd^+ + Na^-) \qquad \text{(I-13)}$$

where Nd^+ is the density of ionized donors, Na^-, the density of ionized acceptors, and q, the electron charge.

The schematic of Fig I-6 explains the impact of traps on the 2DEG density (n_s) when a drain pulse is applied. The conduction band diagrams under the gate are shown in three different conditions: (*case 1*) is the initial state, (*case 2*) after a positive pulse, (*case 3*) back to

initial state. It is assumed that there are deep donor and acceptor traps in the buffer, with respective densities *Na* and *Nd* and (*Nd* > *Na*) by imperfect compensation. Hence, to maintain equilibrium, the Fermi energy is pinned (band bending) to donor energy level in the absence of electric field.

$$Nd^{+} = Na^{-} \qquad \text{when E = 0} \qquad \text{(I-14)}$$

On the other hand when the electric field is present (*case 1*), the equilibrium is reached by this Equation I-15.

$$n_s = (\sigma_+)/q + Nd^{+} - Na^{-} \qquad \text{(I-15)}$$

hen the drain voltage is pulsed high (*case 2*), the induced vertical electric field initiates the deep buffer scattering from the 2DEG channel, which can be captured by the donor traps. Hence, the density of ionized donors is reduced to Nd'^{+} and becomes neutral. This modifies the charge equation given in Equation I-16.

$$n'_s = (\sigma_+)/q + Nd'^{+} - Na^{-} \qquad \text{(I-16)}$$

When the drain voltage is pulsed down (*case 3*), opposite happens. The charge equation comes back to Equation I-15 after the slow emission process is finished. This capture-emission process is not symmetrical. The trapping process mainly occurs in the drain gate access regions both in barrier and buffer regions. Consequently, there is an increase in resistance of drain access region and decrease in 2DEG in this region. This increase in resistance is given in Equation I-17. This also explains the knee voltage increase, often observed in the drain lag measurements during pulsed I-V characterizations.

$$R_{access}(\Omega/\square) = 1/(q.n_s.\mu_n) \qquad \text{(I-17)}$$

where μ_n is the electron mobility in the channel, and n_s, the sheet charge density.

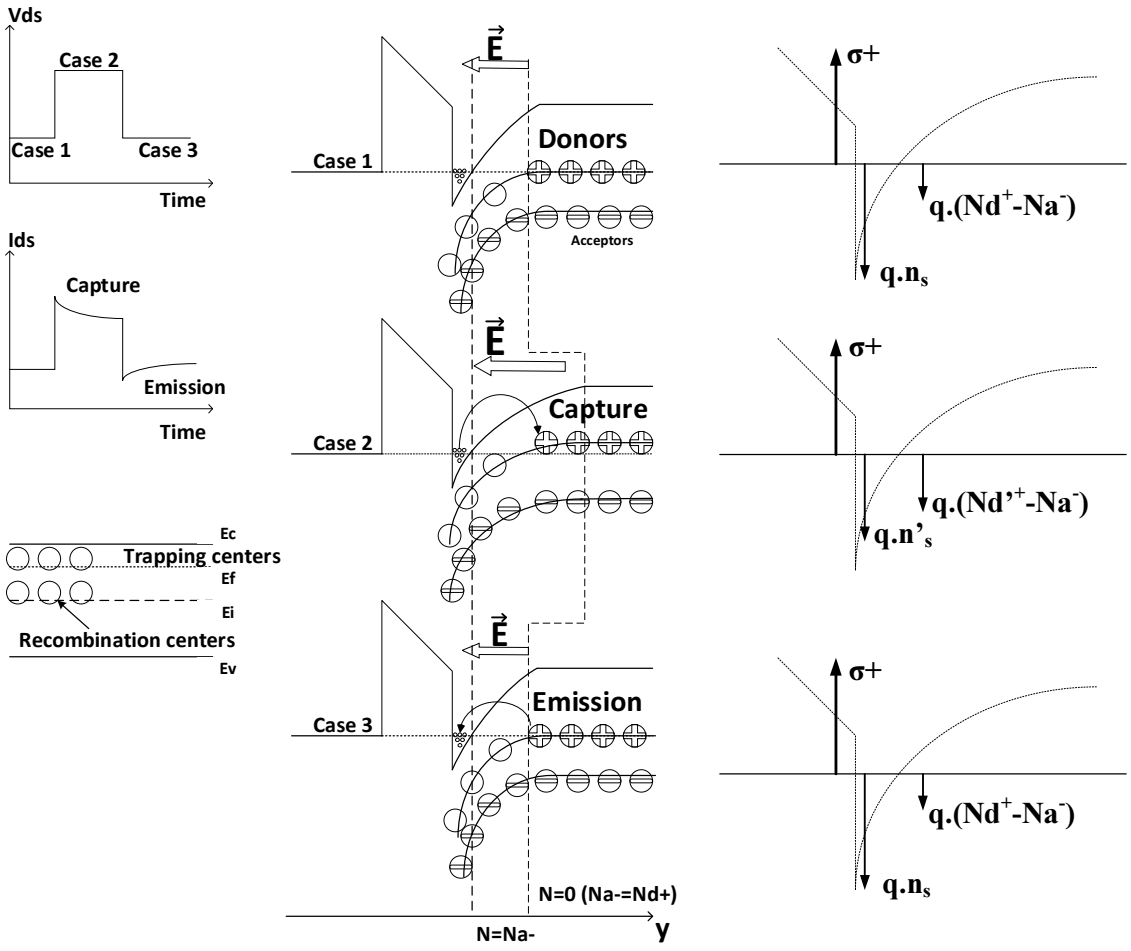

Fig I-6: Description of trapping and detrapping process of traps located in the GaN buffer of HEMT technology ($N_d > N_a$) [16].

I.3.3 Gate lag effects

Gate lag effects are mainly due to the presence of traps at the semiconductor free surface charges present between gate and drain sides. In this region, the electric field is strongest, and the gate can provide free electrons to fill these surface states.

In GaN HEMTs, *Vetury et al* [28] introduced the concept of virtual gate to take into account the gate lag effects. It explains how the probable presence of deep donors at the drain edge of the gate and the neutralization of their charge by trapped electrons is able to reduce the 2DEG density in other words "the origin of current collapse". Fig I-7 shows the schematic illustration of this concept in which a virtual gate acts as a second gate. In the first case of Fig I-7 (*case 1*), the surface donors are ionized, which leads to the presence of 2DEG density, while

in the second case (case 2), the partial occupation of surface ionized donors with electrons results in depletion of 2DEG density [22].

The next sections will illustrate the pulse measurement techniques for the nonlinear modeling of high frequency and high-power devices.

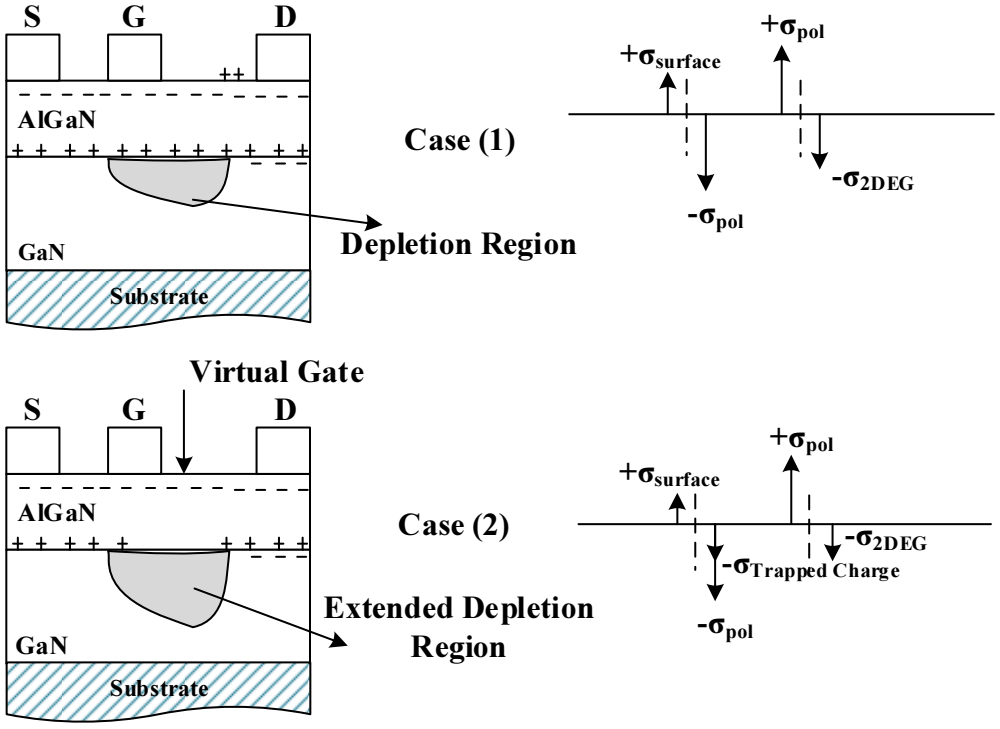

Fig I-7: Concept of virtual gate (case 1) in the presence of ionized donor traps, and (case 2) when traps are charged with a subsequent decrease in 2DEG density [28].

I.4 Pulse measurement techniques for high-frequency and high-power devices

For characterizing high-power AlGaN/GaN HEMT devices, with significant self-heating and trapping effects, several types of device characterizations are required. Characterization's efficiency mainly depends on capturing the nonlinear dispersion in drain current. The pulsed I-V measurement is the most relevant characterization technique compared to conventional DC and CW S-parameter measurements [5][29][30]. Pulsed I-V measurements permit an in-depth characterization of different effects like drain current non-linearity and discrimination of trapping and thermal (self-heating) effects. This section will be focused on the theory and application of these characterization techniques for the nonlinear electrical modeling.

For illustrating the pulsed I-V measurement technique, we considered 2x75µm AlGaN/GaN HEMTs with 0.15µm gate length from III-V Lab, France. These devices were processed on Silicon Carbide (SiC) substrate.

I.4.1 Pulse measurement test bench

A schematic of the pulsed I-V test bench for the characterization of high-power GaN HEMTs is shown in Fig I-8. This set up is used for extracting the nonlinear conductive model of transistors, and also to characterize separately thermal and trapping phenomena. This test bench was developed in XLIM laboratory in Brive. The development of the pulsed I-V setup and the specific measurements dedicated to nonlinear modeling are reported in number of thesis such as [31]–[33].

A state of the art pulsed I-V setup has been developed by the AMCAD Engineering. The AMCAD BILT pulsed I-V system consists of power supplies and input/output measurement units which are embedded in the same hardware. It also consists of two probe heads for the gate and drain access. The purpose of these probe heads is to provide short pulses (down to 200 ns) and also to improve the quality of pulse shape even in the presence of strong drain current variation. The signal is delivered by fast MOSFET switch (10 kV/µs) for the drain probe head and by fast amplifier for the gate probe head. The pulsed I-V measurement units

are synchronized by the pulsed I-V supplies. The trigger is set "internal" for both power supplies and I-V measurement units.

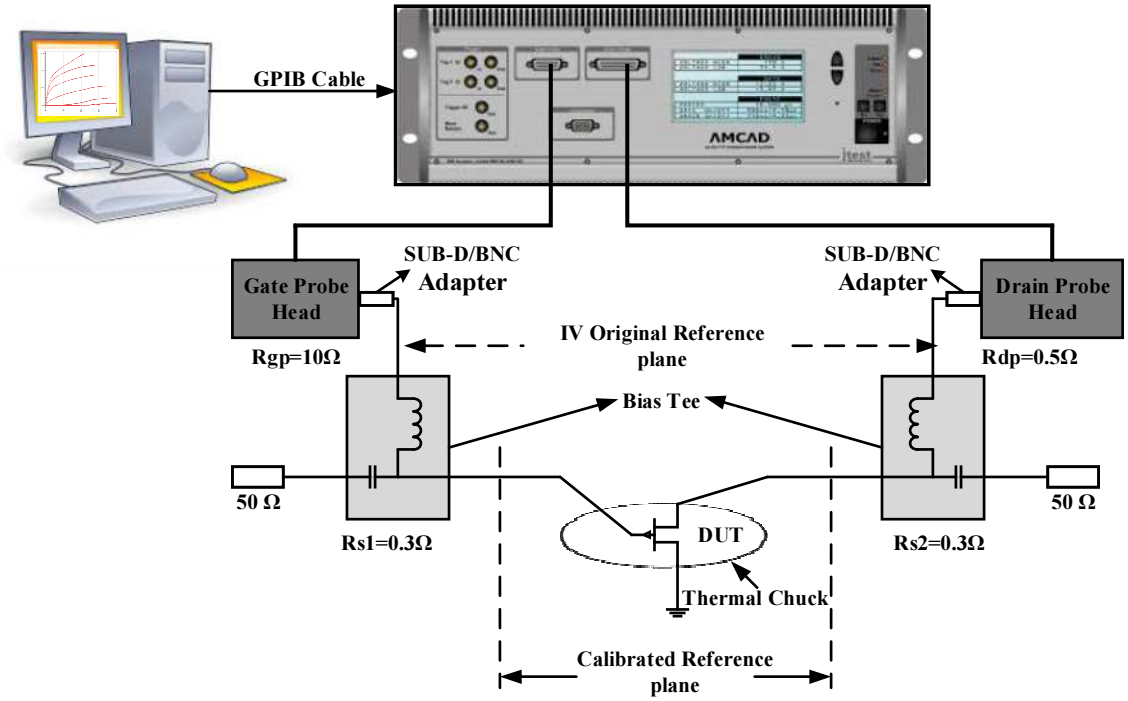

Fig I-8: Schematic of pulsed I-V setup to characterize high-power RF transistors.

An ideal measurement environment would consist of circuits without parasitic components. Unfortunately, the real environment consists of imperfections related to cables, connectors, bias tee... In addition, some resistances can be added between pulse generators and DUT to enable current measurements. In the case of transistor measurements through bias tees, it is recommended to avoid oscillations. The series resistances that exists between the transistor accesses (calibrated reference plane) and the IV original reference plane must be taken into account.

On the contrary to classical high-power pulse pattern generators which have an output impedance of 50Ω, the internal impedance of the I-V probe heads for gate (AM211) and drain (AM221) are small enough (10Ω and 0.5Ω). As a matter of fact, parallel impedances used to decrease the equivalent impedance are not needed anymore. Because of the improved ground connection, there is no need for 500Ω parallel resistances that can be used to improve the ground connection close to the device under test in order to avoid some low-frequency oscillation problems. In addition with the PIV system, some external resistive kits (not shown

in schematic) can be plugged between the gate/drain probe heads and the transistor. The resistive networks are made of series resistances, they are equipped with heat sinker and connection pads for oscilloscope's voltage and current probes. One can choose an alternative measurement system such as an external oscilloscope. In pulse mode, it will decrease the measurement vertical accuracy and measurement speed, but it will increase the horizontal resolution which is limited to 20 ns using the Pulse IV measurement units. That makes this test bench setup versatile.

The main features of the pulsed I-V setup developed by AMCAD:

- 250V/10A pulse generation.
- Pulse width generation down to 200ns.
- All the measurements are easy to perform, store and visualize by IVCAD software [34].
- Embedded measurement units provide simultaneous wide bandwidth and high-accuracy voltage and current measurements:
  - Equivalent to 50 Mega-samples/sec and 10 MHz bandwidth scope for pulse shape monitoring.
  - Fast averaging function providing 16 bit resolution, 0.1% typical measurement accuracy and fast acquisition.
- 4 inch on-wafer probe station equipped with thermal chuck to regulate temperature of devices ranging from -65°C to 200°C.

I.4.2 Pulse measurement principle

The principle of pulsed I-V measurements is illustrated in Fig I-9. It consists of I-V characteristics measured in isothermal conditions at a given quiescent point defined by its quiescent control voltages *Vdsq* and *Vgsq*. The resulting current measured at the quiescent point is given as *Idsq*. Therefore, to characterize the I-V network at this given quiescent bias point, the gate and drain control voltages are pulsed from this quiescent point to new instantaneous values named *Vgsi*, *Vdsi*, *Igsi*, and *Idsi* such as to measure all the I-V characteristic. Now, we will discuss the different conditions that should be satisfied for pulsed I-V measurements.

- The pulse width should be chosen according to the range of measured current. This will give the precision of measurement.

- For low current, large pulse width
- For high current, low pulse width

❖ The duration of pulse period should be larger than pulse width to make sure the device should return to its steady state conditions after each measurement pulse. Thus eliminating self-heating and traps to some level.

❖ Pulse duty cycle must not be large in order to ensure fast and reliable data acquisition with averaging, (A duty cycle of 0.1%-0.5% is usually acceptable).

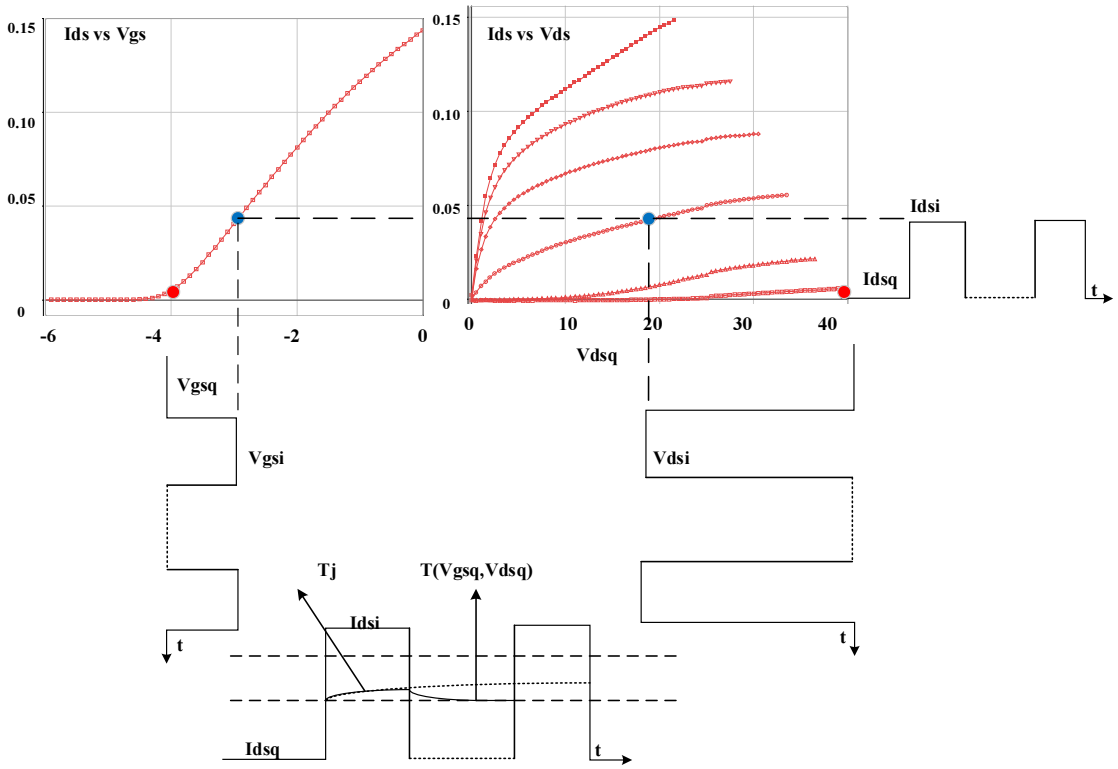

Fig I-9: Principle of pulsed I-V measurement in isothermal conditions.

I.4.3 Pulse characterization of thermal effects

The reduction in self-heating offered by pulse measurements greatly simplifies the process of characterizing the devices at varying temperatures as well. Typical semiconductor devices are so small that it impossible to measure their instantaneous temperature with any kind of probe. Using pulsed I-V measurements [35], the self-heating of the device can be made so insignificant that the internal temperature of the device can be assumed to surrounding ambient temperature and temperature increase due to the dissipated power of the quiescent bias

point. To characterize the device at ambient temperature, simply change the ambient temperature using the thermal chamber or thermal chuck. Once the device has enough time to settle to its new ambient temperature, repeat the pulse measurements at that new temperature.

In order to illustrate some specific device characterization enabled by using the pulsed I-V measurement technique, we present in the next sections the characterization of the on-resistance (R_{ON}) and maximum drain current (Id_{MAX}) variations with respect to temperature. Secondly, we present the simple technique to extract a value of thermal resistance R_{TH}.

I.4.3.1 Temperature dependent parameters

When characterizing the temperature dependence of I-V characteristics, one of the most relevant measurement is the reference pulsed I-V measurement from a cold quiescent bias point ($Vgs = Vds = 0$ V), which gives the temperature independent characteristics at the ambient temperature without the device self-heating. Therefore, the actual temperature is provided by the external thermal chuck and the channel temperature is fixed by this chuck temperature. Actually, in order to avoid self-heating within the pulse, one need to use very short pulses that are difficult to achieve. In the next measurement examples illustrated in this section, we used 600-ns pulse width with 100-µs pulse period giving 0.6% duty cycle. This set of pulse timings will give enough time to recover from temperature transients that occur during the pulses. In any case, this isothermal measurement provides the result close to accurate.

To illustrate the variations of the on-resistance R_{ON} and the maximum drain current *Idss* with temperature, Fig I-10 shows the pulsed I-V characteristic of the 2x75µm AlGaN/GaN HEMT which is measured at a cold quiescent bias point for a pulsed drain voltage *Vds* ranging from 0 to 25 V. This measurement is repeated for different chuck temperatures (25°C, 50°C, 70°C and 100°C).

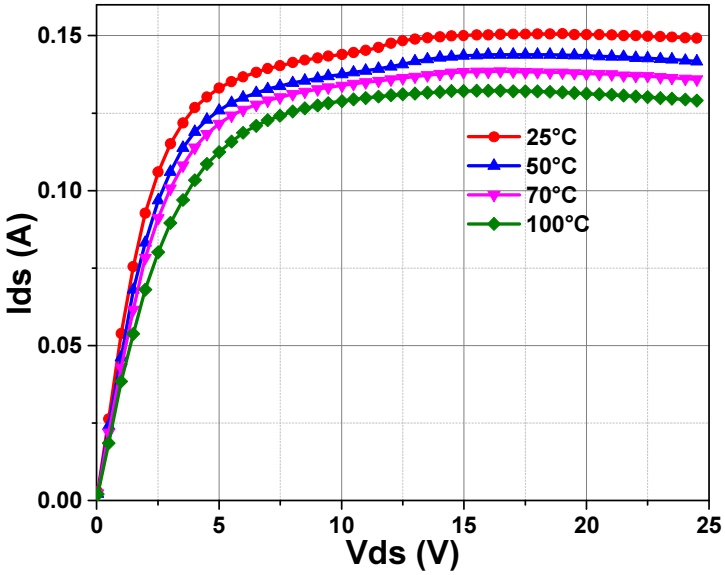

Fig I-10: I-V characteristics of AlGaN/GaN HEMT 2x75x0.15µm² measured at Vgs = 0V with different chuck temperatures pulsed from Vgs = 0V and Vds= 0V.

From the measured results of Fig I-10, the Fig I-11 shows the significant increase of R_{ON} and decrease of the maximum drain current *Idss* with temperature. This is due to the decrease of electron mobility with temperature as explained in the previous section.

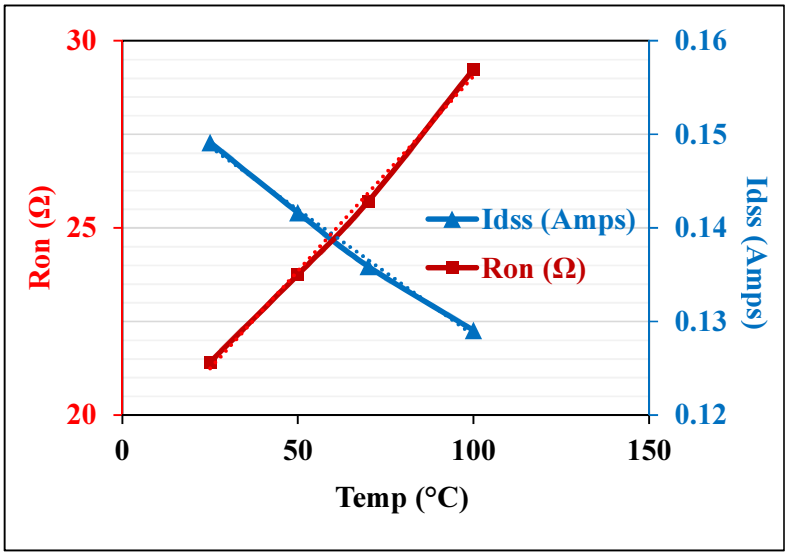

Fig I-11: Extracted Idss (@Vds=25V) and R_{ON} (@Vds=0 to 2V) with respect to different chuck temperatures @P_{Diss}=0W for a 2x75x0.15 µm² AlGaN/GaN HEMT.

From the measured results of Fig I-10, the values of the on-resistance R_{ON} were extracted in the *Vds* range from 0V to 2V while the maximum current values *Idss* were

extracted at 25V of *Vds*. All these values were extracted at the imposed chuck temperature since a cold quiescent bias point was selected for pulsed I-V measurements.

As shown in Fig I-11, the maximum drain current *Idss* exhibits a linear relationship with temperature with a negative slope while the on-resistance R_{ON} also exhibits a linear relationship but with a positive slope. These variations are fitted in the following equations.

$$R_{ON} = 0.1042.T_C + 18.647 \quad \text{(I-18)}$$

$$Ids_{MAX} = -0.0003.T_C + 0.1554 \quad \text{(I-19)}$$

I.4.3.2 Thermal resistance

Several experimental methods have been developed for assessing the thermal resistance of devices. In this section, we present a method [36] based on pulsed I-V measurements, which is illustrated in Fig I-12. At first, the pulsed I-V characteristics are measured at a cold quiescent bias point for the same gate voltage *Vgs*=0V under pulsed conditions (600-ns pulse width and 10-µs pulse period) at different temperatures. In this case, self-heating is negligible and the channel temperature is assumed to be imposed by the chuck temperature. Then, a DC I-V measurement is performed at ambient temperature so that each point of this DC I-V curve corresponds to a different dissipated power. Finally, the crossing points of the DC I-V and the pulsed I-V curves define points at identical channel temperatures. Given the channel temperature, the ambient temperature and the corresponding DC power dissipation (product of drain current and voltage), a value of the thermal resistance *Rth* can be extracted from the equation shown in the inset of Fig I-13. A value of ~35 °C/W was extracted for the measured device. The major drawback of this method is that the results are a mixture of both thermal and

drain-lag effects. This limitation could be reduced by choosing lower values of maximum drain voltage, where traps are not activated.

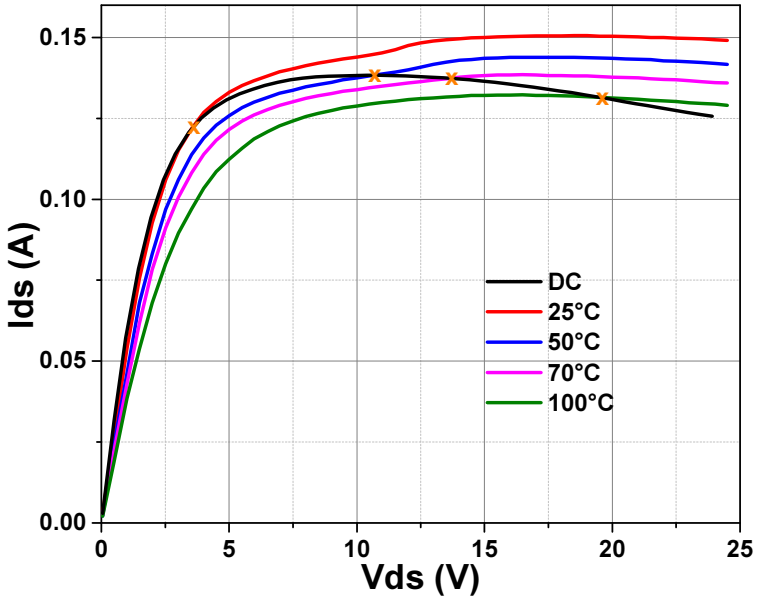

Fig I-12: Extraction of the thermal resistance from a combination of DC and pulsed I-V measurements. The DC I-V curve at Vgs=0V crosses the pulsed I-V curves at different temperatures (25°C, 50°C, 70°C and 100°C) at Vgs = 0V.

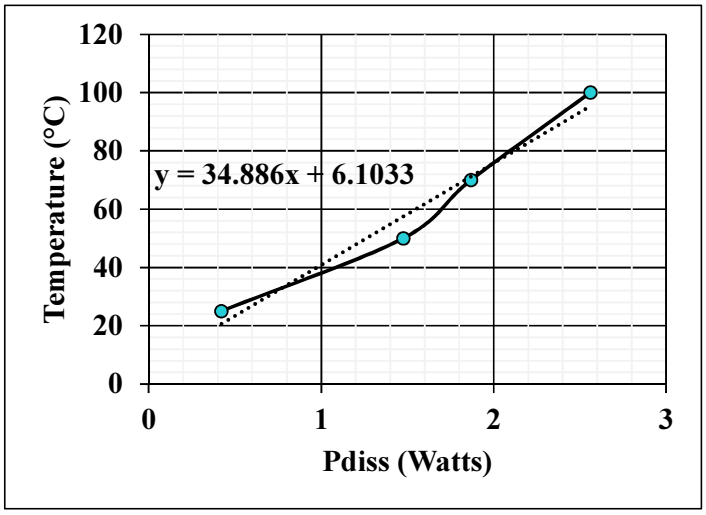

Fig I-13: Temperature versus channel power dissipation where the slope of the linear curve gives an estimated value of thermal resistance R_{TH}=34.9°C/W.

I.4.4 Pulse characterization of trapping effects

The characterization of trapping effects can be based on dedicated pulsed I-V measurements using the test bench setup for high power devices presented in the previous sections. The use of very short pulse widths for pulsed I-V measurement serves as a powerful tool to quantify trapping effects, such as gate lag and drain lag [37]. Indeed, assuming that the trap emission process is longer than the pulse duration whereas the trap capture process is shorter leads to define the necessary pulse conditions where the trap states depend on instantaneous values (*Vgsi*, *Vdsi*) or remain constant at the quiescent bias point (*Vgsq*, *Vdsq*) during the pulses. So, it is possible to define three measurement conditions which play interesting role in the experimental way of quantifying traps.

- **Condition 1 (*Vgsq* = *Vdsq* = 0V):** In this case of quiescent bias point, the gate pulses are negative while the drain pulses are positive in describing the I-V characteristics. The trap capture process is the predominant effect in this case so that all the traps are filled and reach their steady state conditions by the instantaneous voltage levels (*Vgsi*, *Vdsi*). Indeed, the measured I-V characteristics are similar to the DC case, except that there is no self-heating effects because of the very short pulse widths.
- **Condition 2 (*Vgsq* = *Vp*, *Vdsq* = 0V):** In this case of quiescent bias point, both the gate and drain pulses are positive. The trap emission process is the predominant effect in this case. However, when compared to the pulse durations these traps does not have enough time to evolve. Since the quiescent gate voltage *Vgsq* is fixed at pinch-off *Vp*, all the gate-related traps always remain charged and will remain charged during the instantaneous point (*Vgsi*, *Vdsi*).
- **Condition 3 (*Vgsq* = *Vp*, *Vdsq* = Vds_0) :** In this case of quiescent bias point, gate pulses are positive as in the previous case while the sign of drain pulses depends on the values of *Vdsi* which can be lower or greater than Vds_0, i.e. requiring negative or positive pulses, respectively. As in the previous case, the trap emission process is predominant but the I-V characteristics involve both gate-lag and drain-lag effects due to the different signs of the drain pulses. When the instantaneous voltage $Vdsi > Vds_0$, gate lag effects play a major role as in condition 2 while drain-lag effects comes into play when $Vdsi < Vds_0$.

It should be noted that all three conditions have the same thermal conditions that means almost no power dissipation. Thus, these characterizations only involve trap related dispersion.

So, by comparing the measurement results in conditions 1 and 2, one can assess and quantify the gate-lag effects while by comparing measurements in conditions 2 and 3, one can quantify the drain-lag effects. It has been proposed a definition of figure of merit to quantify gate and grain lag effects by their respective influence in terms of power degradation in class A operation. The principle of this comparison is based on the modified voltage and current swings in the 3 conditions and their resulting load-line as it is illustrated in Fig I-14. The figure of merit is calculated as a percentage of gate and drain lag as written in Equations 20 and 21.

$$Gate - Lag(\%) = 1 - \left[\frac{\Delta I'.\Delta V'}{\Delta I.\Delta V}\right] \quad \text{(I-20)}$$

$$Drain - Lag(\%) = 1 - \left[\frac{\Delta I''.\Delta V''}{\Delta I'.\Delta V'}\right] \quad \text{(I-21)}$$

where (ΔI, ΔI′and ΔI′′) are the maximum allowed current swing of Class A operation up to 0V gate voltage in conditions 1, 2 and 3, respectively. In the same manner, (ΔV, ΔV′ and ΔV′′) are the maximum allowed voltage swing of Class A operation around Vds_0 in conditions 1, 2 and 3, respectively.

Indeed, the effects of trapping phenomena on I-V characteristics will directly reflect in limitations of the maximum output power delivered by the device. The formula to calculate the maximum output power P_{OUTmax} of the transistor as a function of ΔI_{max} and ΔV_{max} for Class A operation at a Vds_0 bias voltage is given in Eq 22.

$$P_{OUTmax} = \frac{1}{8}.\Delta I_{max}.\Delta V_{max} \quad \text{(I-22)}$$

where $\Delta V_{max} = 2(V_{ds0} - V_{knee})$ and $\Delta I_{max} = I_{dss} = I_{dsmax}(V_{gs} = 0)$ (I-23)

where all the parameters of these equations are illustrated graphically in the Fig I-14 defining the maximum swings (ΔI, ΔV), (ΔI′, ΔV′) and (ΔI′′, ΔV′′) of the measurement conditions 1, 2 and 3, respectively.

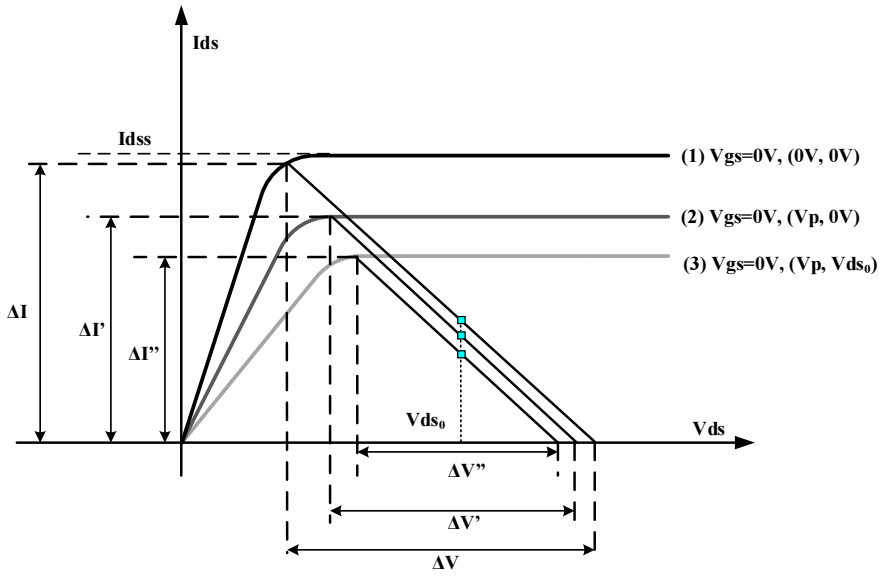

Fig I-14: Schematic explaining how gate-lag and drain-lag effects can be quantified in terms of decrease in power for three different quiescent points, (1):- Vgsq = 0V and Vdsq = 0V, (2):- Vgsq = Vp and Vdsq = 0V and (3):- Vgsq = Vp and Vdsq = Vds_0.

To conclude this analysis of traps by pulsed I-V measurements, we present in Fig I-15 the measured characteristics of the 2x75x0.15µm^2 AlGaN/GaN HEMT in the three conditions of trapping characterization at *Vgs*=0V. The calculated gate-lag and drain-lag percentage are given in Table 1-3.

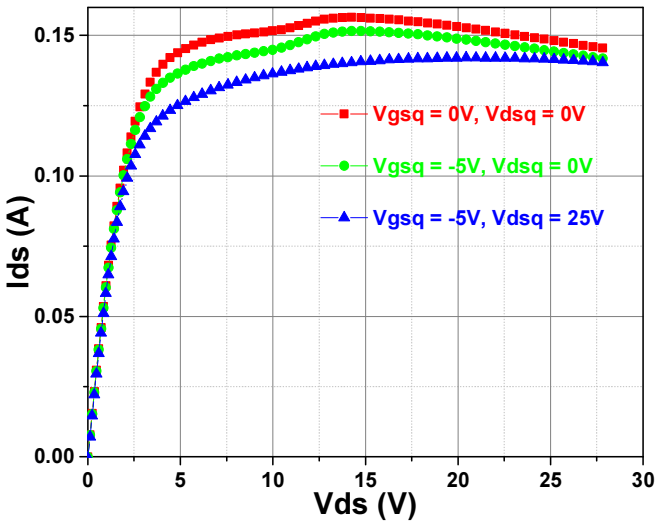

Fig I-15: Measured gate and drain lag effects at Vgs=0V for a 2x75x0.15µm^2 AlGaN/GaN HEMT for three different quiescent points, (1):- Vgsq = 0V and Vdsq = 0V, (2):- Vgsq = Vp and Vdsq = 0V and (3):- Vgsq = Vp and Vdsq = Vds_0.

Gate-lag (%)	Drain-lag (%)
3.3	14.9

Table I-3: Calculated values of gate-lag and drain-lag at Vgs = 0V

I.4.5 Pulsed S-parameter measurements

The principle and characterization techniques of Pulsed I-V measurement as well as the test bench have been discussed in previous sections. This new section deals with the principle of pulsed S-parameters measurements. This feature is included in the whole characterization setup as illustrated in Fig I-16.

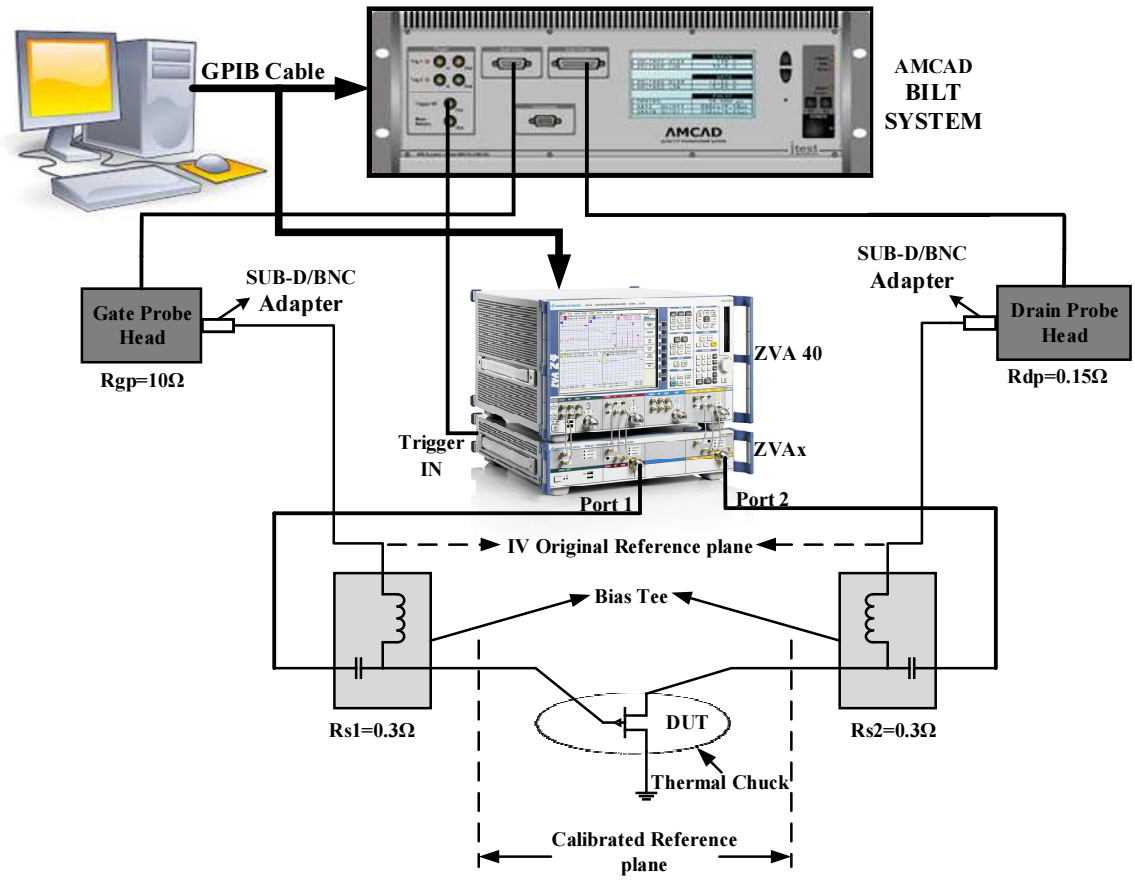

Fig I-16: Schematic of the pulsed measurement setup including pulsed I-V and pulsed S-parameter features to characterize high power RF transistors.

The setup is the same as the previously described test bench for pulsed I-V except that it is coupled to a vectorial network analyzer (VNA), which is able to measure pulsed S-parameters and pulsed load-pull measurements. The additional equipments coupled to the I-V setup are Rohde & Schwarz ZVA40 and ZVAx modules. Each of these modules will be explained along with calibration procedures. The specific bias tee (Agilent 11612A) for the pulsed measurement must be capable of handling low pulse-width, high currents and voltages and support very high frequencies (500ns, 40GHz, 200V and 10A) in pulse mode based on our laboratory experience. Their inductance should be low to avoid distortions on pulses.

This test bench is similar to any classical VNA measurement in continuous mode except the difference in the receiver unit of R&S ZVA 40. The dynamic range is around 65dB in the frequency range of 10MHz to 40GHz. But, when operated in continuous mode (classical VNA), the dynamic range is around 110dB. This decrease in dynamic range from CW to pulsed mode is due to the receiver losses that occur in pulsed mode. This losses are given in Equation I-24 as a function of the pulse-width and the pulse-period.

$$reduction\ (dB) = -20.\log\left[\frac{Pulse\ period}{Pulse\ width}\right] \qquad \text{(I-24)}$$

Specific features of calibration for pulsed S-parameter measurements:

The calibration principle of pulsed S-parameter measurements remains the same as that of the CW mode (SOLT, TRM, etc…). However, if the pulse settings like pulse-width and pulse-period or the calibration is done in CW mode, the calibration will be deteriorated because of the linearity and dynamic range of the receiver's mixer that will not be perfect in all conditions. The other feature that should be taken into account is the RF power level. Indeed, the RF power should be constant over the selected frequency range for small-signal analysis of the DUT. All the losses due to connectors and cables should be nullified and present the same power at the DUT reference plane. If the RF power is too low, it affects the measurement accuracy, while if the RF power is too high, the DUT could generate many harmonics which are undesirable for small-signal linear analysis. Therefore, the accurate calibration requires to control the RF power at each frequency to generate a correction table for the RF source and to present constant power at DUT reference plane over the selected frequency band.

I.4.6 Principle of pulsed S-parameters

The principle of pulsed S-parameter measurements consists of superimposing the RF signal on each instantaneous bias point (*Vgsi*, *Vdsi*) of the pulsed I-V network and perform the acquisition of S-parameters as it is illustrated in Fig I-17.

In usual conditions of instantaneous pulsed bias with superimposed RF signal, the selected pulse width is 800ns for *Vgsi* at the gate port and 600ns for *Vdsi* at the drain port with an identical pulse period of 10µs. The pulsed RF signal is synchronized with the instantaneous I-V pulse using sufficient on-off delays (only 300ns RF pulse-width) to avoid any RF signal during the transients of I-V pulses. As already discussed, the thermal and trap states are fixed by the quiescent bias point (Vgs_0, Vds_0). At each instantaneous point (*Vgsi*, *Vdsi*) of the entire I-V characteristic, a S-parameter file is measured over the frequency bandwidth. Indeed, each of these S-parameter files measured in pulsed mode gives the actual response of the device at the quiescent bias point (Vgs_0, Vds_0). They are used to extract the parameters of a small-signal circuit model as a function of the instantaneous control voltages (*Vgsi*, *Vdsi*). Finally, the reactive and conductive nonlinearities of the nonlinear circuit model at (Vgs_0, Vds_0) will be extracted from both the pulsed I-V and pulsed S-parameter measurements. The nonlinear model in CAD tools, which are close to real operation of the device. The extraction process of model parameters will be discussed briefly in chapter II.

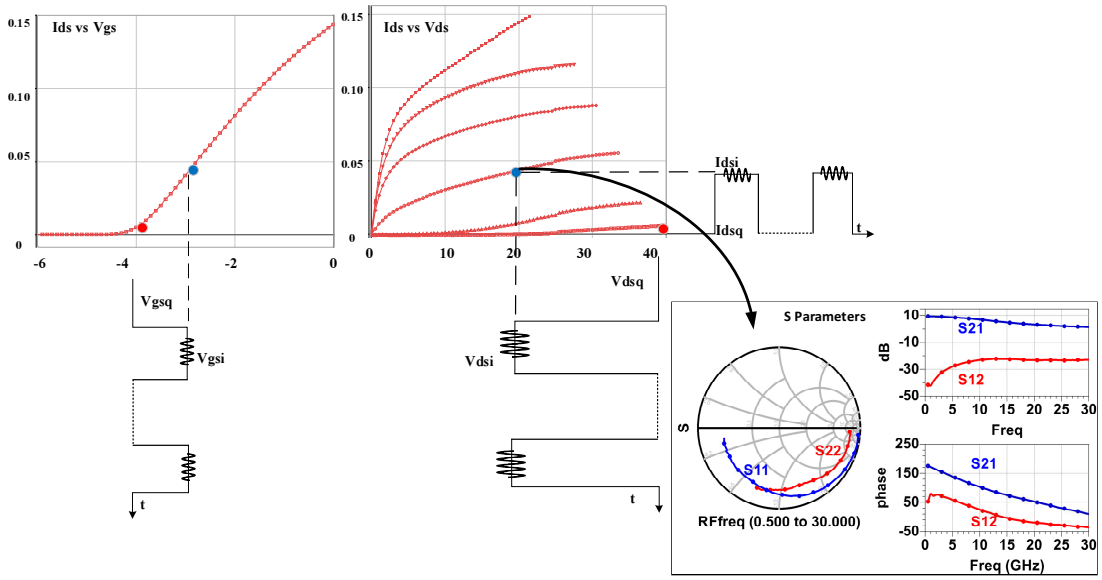

Fig I-17: Principle of synchronized pulsed I-V and pulsed S-parameter measurement.

Usually, in the case of power transistor modeling, the pulsed I-V and pulsed S-parameter measurements are used to extract the nonlinear circuit model and are followed by a load-pull characterization to serve as validation data for the model extraction. Indeed, the measured small signal S-parameters at (Vgs_0, Vds_0) such as S_{11} and S_{22} are used to initialize the load-pull measurement configuration (i.e. input and output optimum load area on the Smith chart). Fig I-18 shows the measured S-parameters of the 2x75x0.15µm^2 AlGaN/GaN HEMT in Class AB (Vds_0=25V, Ids_0= 15mA) up to 35 GHz.

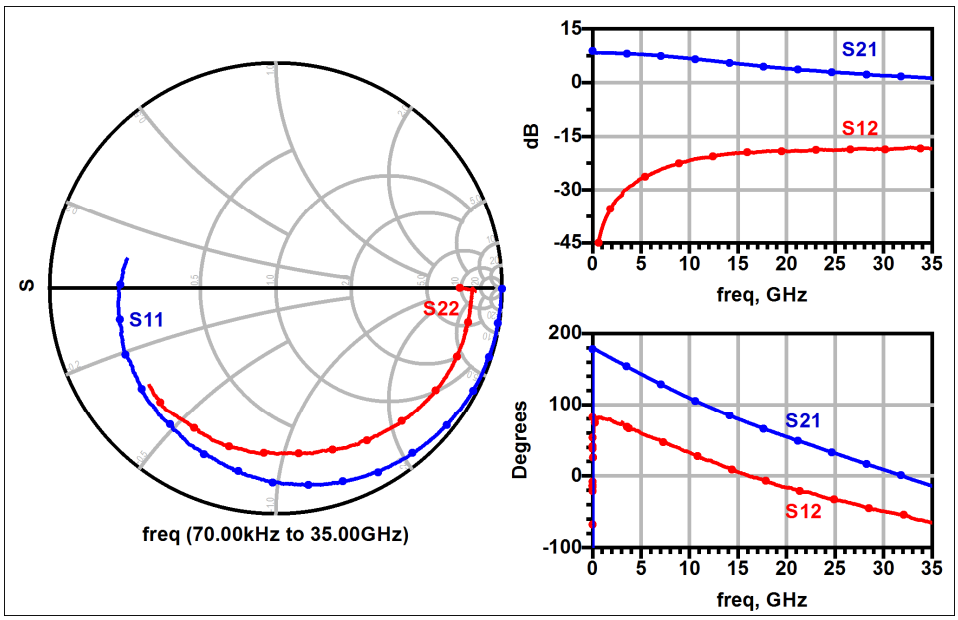

Fig I-18: Measured S-parameters of 2x75x0.15µm^2 GaN HEMT (Vds_0=25V, Ids_0= 15mA).

Moreover, from these S-parameter measurements of Fig I-18, the figure of merits like maximum stable gain (MSG) and maximum available gain (MAG) will be extracted at the frequency of interest to initialize the load-pull configuration. As an example, Fig I-19 and Table I-4 gives the extracted characteristics for the 2x75x0.15µm^2 AlGaN/GaN HEMT at 18GHz.

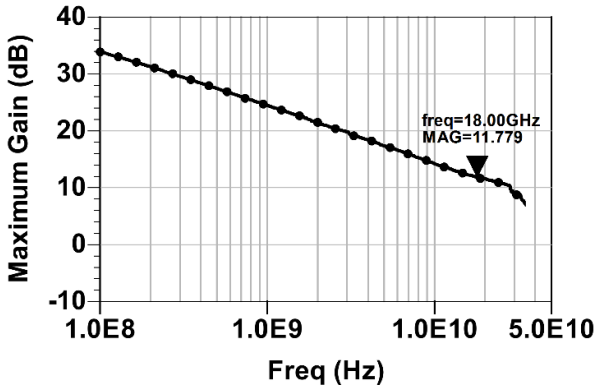

Fig I-19: Maximum gain (dB) of 2x75x0.15µm^2 GaN HEMT (Vds_0=25V, Ids_0= 15mA).

	Transition MSG/MAG (GHz)	**Gain (dB) @18GHz**	$\boldsymbol{Z_{22}^{*}}$ **@18 GHz**
AlGaN/GaN 2x75µm, Lg=0.15µm	28.25	11.78	16.33+54.95.j

Table I-4: Gain and output impedance extracted from S-parameters of 2x75x0.15µm² GaN HEMT (Vds_0=25V, Ids_0= 15mA) for load-pull initialization.

I.5 Pulse setup developed for graphene FET characterization

I.5.1 Introduction

The recent discovery of graphene [38], a single atomic sheet of graphite, has attracted device community to explore the electronic properties of this novel two-dimensional (2D) device material. In graphene, charge transport is different from that of conventional semi-conductors due to its conical energy dispersion near the charge neutrality (Dirac point) in the energy band diagram [39]. This gives rise to some of the very interesting intrinsic properties of graphene. Field-effect mobility as high as 15000 $cm^2/(V.s)$ and Fermi velocity of ~10^8 cm/s have been demonstrated at room temperature [40]. These properties makes graphene a possible candidate for future electronic devices. More detailed explanations of these properties and transport process are given in chapter III, which is dedicated to examples of graphene FET characterization and modeling.

Despite the superior properties of graphene that are frequently quoted like electron/hole mobility compared to other semiconductors, it is not obvious when experimentally compared to narrow band III-V semiconductors at comparable carrier densities, as illustrated in Fig I-20. This is due to very unstable device characteristics that arise in graphene's sensitivity to several environmental factors such as metal contacts, defects, interface charges, contaminants, etc…

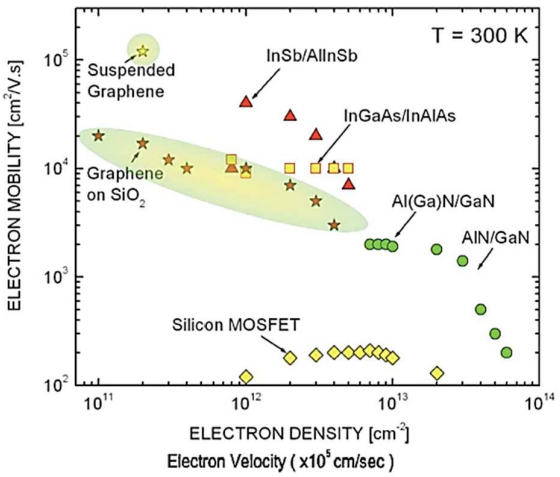

Fig I-20: Electron density and velocity versus electron mobility of different semiconductor materials [41].

The electrical measurements of graphene transistors are not very different from that of semiconductor devices since they are interpreted as current-voltage (I-V) characteristics but a specific attention has to be paid to measurement accuracy due to low I-V levels of nano devices.

I.5.2 Specificities of nano-device characterization

Nanotechnology is the act of manipulating matter at the atomic scale, otherwise known as "nanoscale". In the field of nanotechnology, there are research areas that require electrical characterizations such as nanowires, nano-based materials (Graphene), and electronic devices such as carbon nanotube FETs (CNT-FET), graphene FETs (G-FET), graphene nano-ribbon FETs (GNR-FET) and nano-electro-mechanical switches (NEMS).

The development of electrical measurement tools [42] with very high sensitivity is of prime importance to accurately characterize the electrical properties and performances of new nano-electronic materials and devices such as graphene FETs. First and foremost the instrument sensitivity must be higher because electric current of nano-devices are much lower while they exhibit improved conductivities [43]. There are also many specificities when characterizing nano-scale devices such as, for example, the great complexity to probe down to the device level for failure analysis and other testing.

So, the safe characterization of nano-scale device properties is a very difficult issue. In our case of pulsed electrical characterization, we need to send very short bursts of energy (pulse testing) while keeping a tight control over pulse parameters like pulse-width, rise-time, fall-time and voltage/current levels. Apart from pulse measurement techniques, a specific attention has to be paid to avoid unnecessary source of errors [44]. These features are illustrated in the next sections through the specific measurement setup that we have developed for characterizing graphene FETs.

I.5.3 Pulse measurements

Pulse measurements are simply measurements made with a pulsed source signal. This has been demonstrated by comparing with typical DC measurement, as shown in Fig I-21. To perform a DC measurement, we need to apply a DC signal (typically DC voltage) and then wait for some time. We have to wait long enough time for all the transients due to the DUT and the

test system itself to settle out. Once all these transients settled, the measurement is performed. Measurements are usually made by sigma-delta (∑-Δ) or integrated type analogue to digital converters (ADC). The conversion is done over one or more power line cycles to eliminate noise in the measurement caused by the ambient power line noise that exits in test environment. Multiple measurements can be taken to further increase the accuracy. Using DC measurement technique, measurements may take 100 ms or greater for just one measurement reading.

However, pulse measurement occurs quickly since the test signal is applied for a very brief time before the signal is returned back to the base level. In order to fit the measurements in this very short time, sigma-delta (∑-Δ) ADCs run at sub-power-line interval integration times or even the system uses faster successive approximation register (SAR) type ADCs. By running at higher speeds, the readings from pulse measurements are nosier, compared to readings returned by DC measurements. However, pulse measurements offer other advantages over DC measurements that will be discussed in the following.

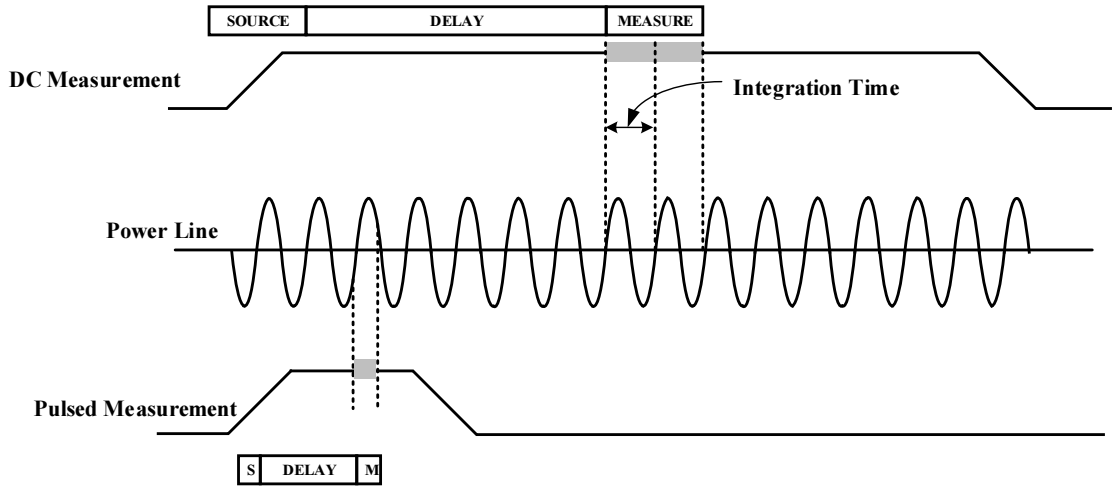

Fig I-21: DC versus pulsed measurement technique.

I.5.3.1 Anatomy of the measurement pulse

Before discussing about the measurement part of the pulse system, we will first discuss about the features of the pulse signal itself. In pulse measurements, the test signal is applied for a brief time and returned to its base level. This application and removal of the test signal relative to time defines the shape of the pulse and each part of the resulting waveform. In the following

sections, we will describe the specific parameters of the pulse signal which are illustrated in Fig I-22 (definitions given by Keithley Instruments, Inc.).

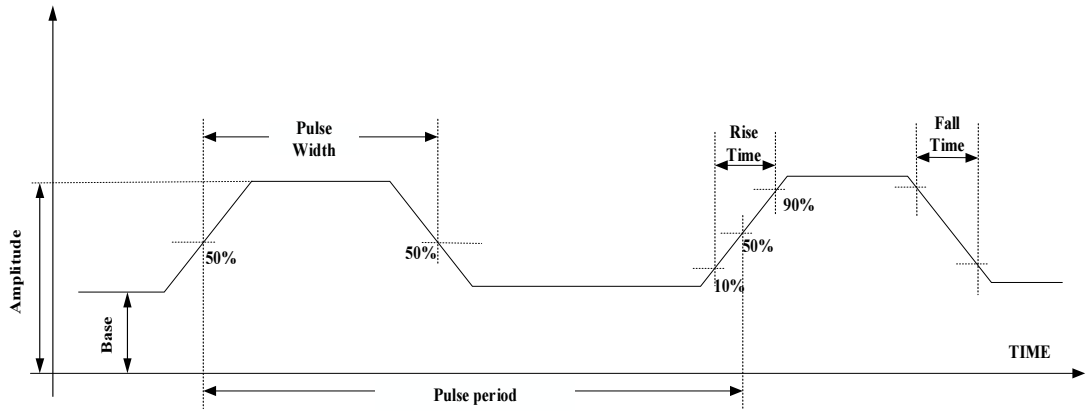

Fig I-22: Time-domain profile of a pulsed measurement signal.

Amplitude and base:

Amplitude and base describe the height of pulses in the waveform. The base describes the quiescent level of the signal waveform that is imposed both before and after the pulse, i.e. the DC offset from the level zero. The amplitude is the level of the signal waveform relative to the base level and its absolute value is base + amplitude.

Pulse-width and pulse-period:

The pulse-width is the time during which the pulse signal is applied. More specifically, the pulse-width is the time duration of the pulse at half maximum. The pulse-period is the time duration of the entire waveform before it is repeated. The duty cycle is the ratio of pulse-width to pulse-period.

Rise and fall times:

The rise and fall times of a pulse are the time durations of low-level to high-level transitions and high-level to low-level transitions, respectively. More specifically, the industry standard to measure transition times is the duration from 10% to 90% of amplitude over the rising edge and vice versa.

I.5.3.2 Pulse measurement techniques

Pulse measurements comes in two types: pulse I-V and transient measurements as illustrated in Fig 1-23. Pulse I-V technique is to gather DC like current versus voltage (I-V) curves using pulses. In pulsed I-V technique, the measurements are taken at the flat top of the pulse, preferably near the end of the pulse before the falling edge. In this technique, the pulse shape is very important as it determines the quality of measurement. If the top of the pulse is not settled when the measurement is taken, the resulting reading will be noisy and incorrect. Sigma-Delta (∑-Δ) and integrated-type ADCs should be configured to perform their conversion over this flat top as much as possible to increase the accuracy and reduce noise [45].

Two techniques [46] of pulse I-V measurement can be employed to improve the accuracy of measurement readings. In the case of adequate pulse width and measurement speed, multiple measurements can be made on the flat top of the pulse and averaged together to generate a single reading. This is known as the "spot mean measurement". This technique uses high-speed summation approximation registers (SAR) ADCs to make measurements. SAR ADCs perform conversions often at a rate of 1µs/sample or faster, sacrificing resolution for speed. At these high speeds, many samples can fit at the pulse top. If even more accuracy is desired, the pulse measurement is repeated several times over several pulses and the readings averaged to get a single reading with even greater accuracy. This is known as "spot mean average measurement".

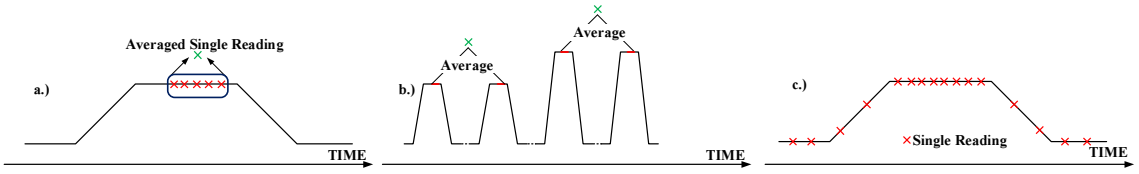

Fig I-23: Pulse measurement technique. a) Pulse "spot mean measurement", b) Pulse "spot mean average measurement" and c) Transient pulse measurement.

The other type of pulse measurement is the transient pulse measurement. Transient pulse measurements are performed by sampling the signal at high speed to create a waveform of the signal versus time. These measurements are often made by oscilloscopes, but it can be also made by traditional DC-measurement equipment with ADCs running at very high speeds. Transient pulse measurements are very useful because they allow us to investigate various device behaviors like self-heating and charge trapping.

I.5.4 Pulse measurement setup

The pulsed I-V measurement setup that we have specifically developed during this work for a highly sensitive characterization of devices is shown in Fig I-24. It associates the Keithley 4200 Semiconductor Characterization System (SCS) with an additional pulse measure unit (PMU-4225). This PMU is available as add-on card. Pulse Measure Unit (PMU) like Source Measure Unit (SMU) combines the capabilities of multiple instruments into one. The PMU combines the capabilities of a pulse generator and a high resolution oscilloscope, simplifying the measurement capabilities over several instruments. This setup has two independent channels capable of sourcing up to (40 V/800 mA). Like any standard pulse generator, all pulse-shape parameters are user-configurable. The pulse widths can be controlled down to 60 ns while rise and fall times can be imposed as small as 20 ns. These excellent features of pulse-shape generation allow us to characterize devices with fast transients. It is also featured with the electrical waveform generation "Segment ARB" (trademark of Keithley Instruments, Inc.) that allows us to source multi-level pulse waveforms.

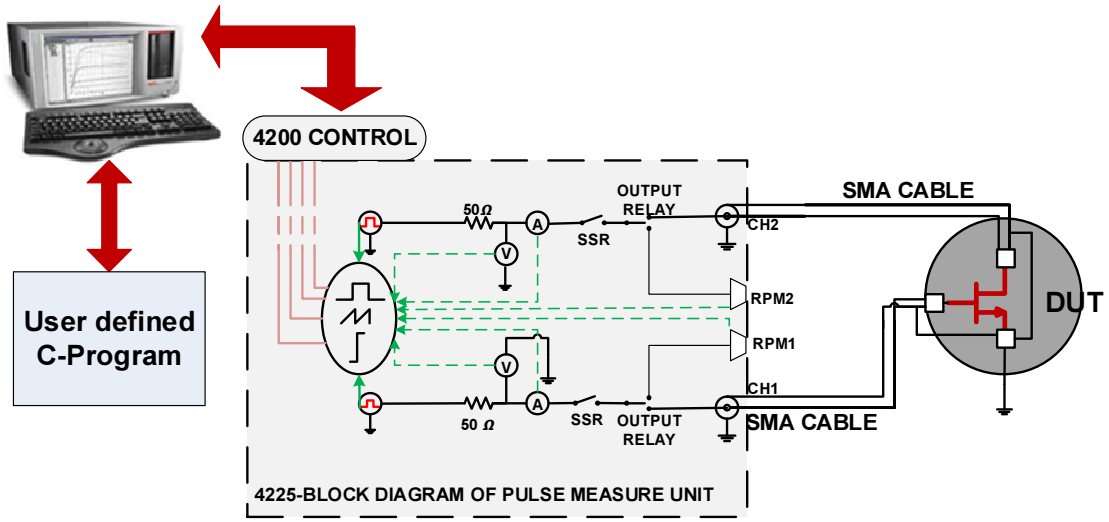

Fig I-24: Pulse measurement setup dedicated to low-current pulsed I-V and transient measurements of transistors.

On the measurement side, each PMU channel is capable of measuring current and voltage using two ADCs (14-bit, 200 Mega-Samples/sec) per channel for a total of four ADCs per card. All of the four ADCs are capable of sampling together synchronously at full speed. In addition, the 4225-PMU has excellent low-current capabilities with a minimum current

range of 100µA or even 100nA with the addition of 4225-RPM (Remote Amplifier/Switch Module) allowing highly accurate characterization even for very small devices.

The photograph of the experimental setup is shown in Fig I-25. The DC and pulsed I-V characteristics are measured by Keithley 4200-SCS whereas the S-parameters measurements are performed by Anritsu VNA (37297D) for DC conditions only. This setup is coupled to on-wafer probe station

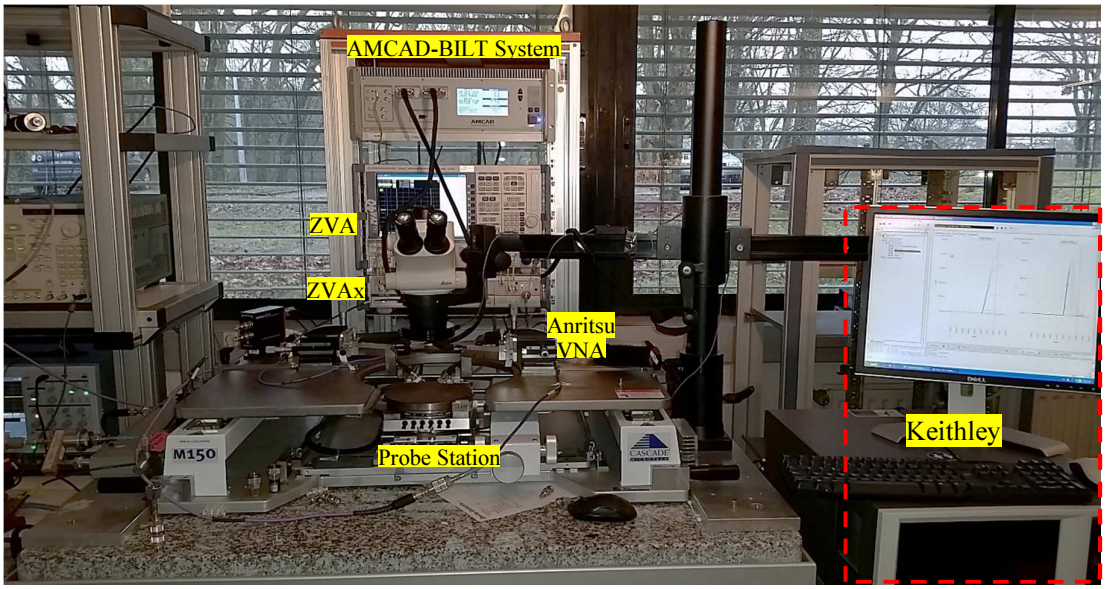

Fig I-25: Photograph of I-V and S-parameters setup.

I.5.5 Features of developed test setup

We detail here some examples of measurements and precautions to show the specificities of Keithley test setup for transient I-V for high power devices over AMCAD-BILT SYSTEM, and nano devices characterization. These examples of measurements are few in many innovative characterizations that we can perform using this developed test bench.

Pulse average:

"Pulse Average" means that each point on I-V characteristics is an averaging of samples taken inside the measurement window of the number of pulses (spot mean average). In reality, to avoid noise on measurement readings one should satisfy the Equation I.25. We cannot have more samples using only one pulse reading. So, in the real systems an average of 10 pulses

gives enough samples to avoid noise [43]. This technique also allows us to keep shorter pulse widths along with pulse averaging and as a consequence we lower the noise on the measurement. But, averaging pulse measurements on a lot of pulses acquisition leads to longer test times. This is due to the limitations of the instrument itself, which has maximum sampling rate of 200 Mega samples/sec and it keeps 1 million points per measurement for each channel and each Current (I) and Voltage (V).

$$Noise\ reduction \propto \frac{1}{\sqrt{no.of\ samples}} \qquad \text{(I-25)}$$

Satisfying this condition, we performed measurements on a 2x75µmx0.15µm^2 AlGaN/GaN HEMT. Measurements are made with the two conditions: 1.) pulse averaging of 15 pulses 2.) pulse averaging of 1000 pulses with a gate pulse width of 800ns, a drain pulse width of 600ns and a pulse period of 10µs for the two conditions respectively. Since the device is stressed in pulse conditions with small pulse width, we can safely say that there is no significant self-heating effect. From the Fig I-26, it is clear that the number of pulses impact the trapping by observing the decrease in current for 1000 pulses compared to 15 pulses. This kind of measurements are interesting and possible with the developed test bench. It justifies the dynamic nature and quantifies the traps states dependency on the number of pulses applied to the DUT. These innovative measurements are not possible with previous developed test bench i.e., AMCAD BILT SYSTEM, because it does not have accurate control over number of pulses. Indeed, the measurements taken by BILT are based on subsampling principle where the number of samples inside the measurement window determines the number of pulses.

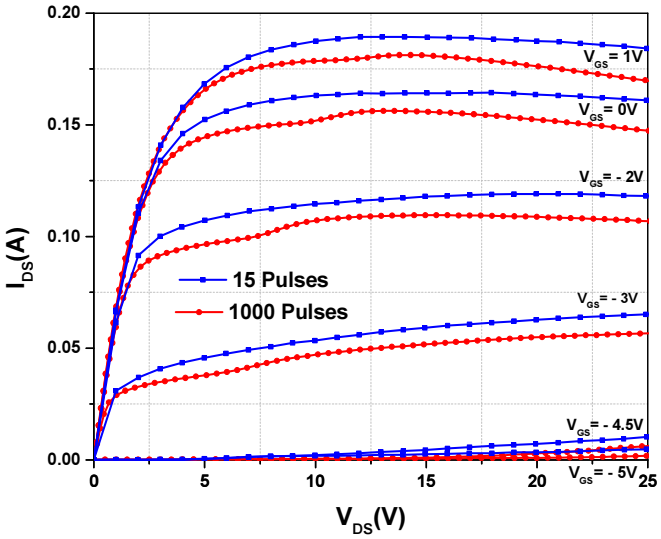

Fig I-26: Example of different pulse averaging measurements.

Current charging effects during pulse transitions:

Previously, we talked about the number of samples inside the measurement window and pulse averaging to avoid noise. However, one should be very cautious to select the region of measure window because it can affect the measurement result. The following Fig I-27 shows the importance of pulse shapes for I-V measurements with Keithley 4200-SCS. In the measurements of Gate/Drain currents, we observed overshoots during the pulse transitions. The recorded current during these transitions is from charging and discharging of cable capacitance and instrument capacitance.

$$I = C * \left(\frac{dV}{dt}\right) \qquad \text{(I-26)}$$

where I is the measured current, C is the capacitance, dV/dt is the slope of voltage during rise (or fall) time.

The Equation I-26 shows that this effect is a function of the capacitance, as well as the dV/dt and illustrated in Fig I-27. Therefore, minimizing the capacitance will reduce this measurement artifact. The cabling is typically the largest contributor to this capacitance. Moreover, this capacitive charging current is primarily a measurement artifact as the current does not flow through the DUT. Note that if a spot mean is taken during the settled portion of the pulse, then this charging does affect the spot mean measurement. So, it is necessary to follow the recommended pulse timings for different I-V measurement ranges shown in Table I-5. In next sections we discuss the consequences of pulse timing violations.

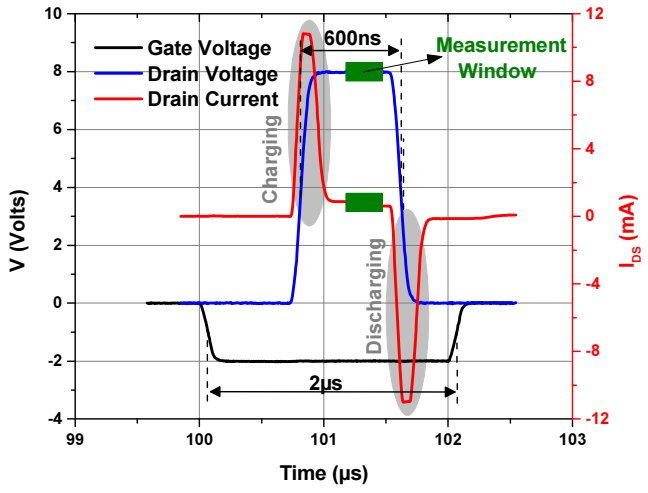

Fig I-27: Cable and source capacitance effects, with Rise Time =100ns, Drain Voltage= 8V, Fall Time =100ns, Gate Voltage= -2V, Period = 1ms and Delay = 0.1ms.

	Current Measurement Ranges	Recommended Min Pulse Width Time	Recommended Min Rise and Fall Times	Recommended Min measurement window	Settling Time
RPM*10V	100 nA	134 µs	1 µs	10 µs	100 µs
RPM 10V	1 µA	20.4 µs	360 ns	1.64 µs	15 µs
RPM 10V	10µA	8.36 µs	360 ns	1 µs	6 µs
RPM 10V	100 µA	1.04 µs	40 ns	130 ns	750 ns
RPM 10V	1 mA	370 ns	30 ns	40 ns	250 ns
RPM 10V	10 mA	160 ns	30 ns	20 ns	250 ns
(A) PMU** 10V	10 mA	160 ns	20 ns	20 ns	100 ns
(B) PMU 10V	200 mA	70 ns	20 ns	20 ns	30 ns
PMU 40V	100 µA	6.4 µs	1 µs	1 µs	4 µs
(C) PMU 40V	10mA	770 ns	100 ns	100 ns	500 ns
(D) PMU 40V	800 mA	770 ns	100 ns	100 ns	500 ns

*RPM: Remote Amplifier/Switch. **PMU: Pulse Monitoring Unit.

Table I-5: Typical Minimum Timing Parameters Based on Voltage and Current Range [46].

Small Pulse Width:

To demonstrate the effect of capacitance, we detail in this paragraph the results obtained from the measurements on 2x75x0.15µm^2 AlGaN/GaN HEMT's I_{DS} versus V_{DS} characteristics which are shown in Fig I-28.

These measurements are performed by varying the pulse widths from 100ns to 1µs. The rise time and fall time are 20ns for all pulse widths. The gate to source voltage (V_{GS}) is equal to -2.5V. The range of Vds is limited to 10V due to the recommended pulse conditions allocated by the instrument itself given in Table I-5[B]. For the measurement accuracy the pulse average is done for 1000 pulses.

Indeed, there are variations in I-V characteristics for different pulse widths and it is more evident when we used 100ns pulse width. This differences cannot come from self-heating or noise because we used small pulse widths and performed pulse averaging. But, this is due to the measurements readings which are taken during the unsettled portion of the measurement window inside pulse. The unsettled portion of pulse is the pulse shape due to cable transients for the reasons given in the before section. To avoid this, we should verify the pulse shape using the waveform capture capability of the 4225 PMU and also minimizing cable lengths. A trade-off is thus needed between very short pulses and resolution.

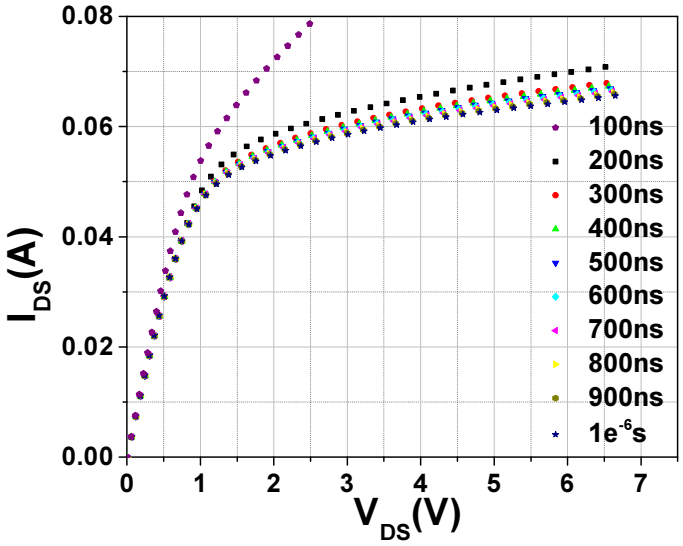

Fig I-28: Different pulse widths effects.

Measurement Range:

To see the effect on measurement ranges using allowed pulsed conditions given in Table I-5[A,C,D] like pulse width, pulse period and number of pulses, we have performed a measurement on discrete commercial JFET 2N4416 [47]. Fig I-29 shows the measurement ranges and their respective I-V curves. It is clear that with the pulsed I-V with 40V-800mA range, we observed very noisy measurement readings. This is due to the measurement resolutions allocated by Keithley 4200 SCS itself. This can be avoided by following the conditions presented in the Table I-5 based on the DUT specifications.

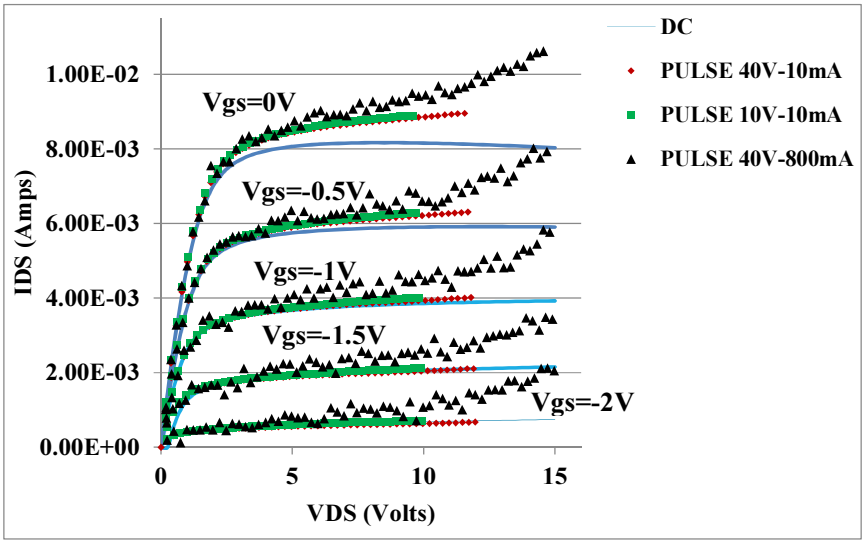

Fig I-29: Different measurement ranges effects.

This transient pulse analysis, highlights that pulse shape determines spot mean values for pulse I-V curves. If the pulse width is too short, a spot mean is still provided. During pulse rise and fall times, the current charges the interconnect and instrument capacitance. Therefore, particular attention is needed on pulse waveform measurement, especially on current measure waveforms.

This will conclude the part on features of developed Keithley setup where we saw some of the innovative measurements using number of pulses, importance of pulse shape when measuring pulsed I-V, and necessary precautions that need to be taken care while doing pulsed I-V measurements by following the recommended measurement conditions given in Table I-5 detailed on pulse widths and measurement ranges.

I.6 Conclusions

In this chapter, we presented the pulsed measurement techniques and setup that have been previously developed at XLIM laboratory for the characterization of medium and high power transistors. Pulsed I-V and pulsed S-parameter techniques have been reviewed as well as the main measurement techniques to characterize thermal and trapping effects. Many of these measurement techniques have been illustrated through the measurement of a $2x75x0.15\mu m^2$ AlGaN/GaN HEMT.

Starting from all this experience on pulsed measurements at XLIM laboratory, we have developed a new setup with specific features of sensitivity and pulse resolution dedicated to high-speed low-current measurements with the aim of characterizing nano-devices such as graphene FETs. However, this new setup will be used in the next two chapters both to investigate trapping effects on high power devices such as GaN HEMTs and to model low-current graphene FETs.

Indeed, the next Chapter 2 will use the features of this setup to investigate the distinct electrical behavior of AlGaN/GaN HEMTs using static and pulsed I-V characterizations under different pulse widths, pulse periods, number of pulses, quiescent bias points. After presenting the GaN HEMT technology, the electron capture/emission phenomena will be experimentally characterized in terms of electrical device's history or stress to illustrate long-term memory effects of AlGaN/GaN HEMT technology.

Finally, the Chapter 3 will use the features of the presented setup to investigate the electrical behavior of graphene FETs and to extract a nonlinear circuit model. This last chapter will start with brief presentation of graphene and its intrinsic properties. Then, the measurement and modeling process will be detailed for different graphene-based FETs such as epitaxial grown graphene nano-ribbon FET (GNR-FET) and CVD transfer based large-area graphene FETs (G-FETs).

II. Pulsed I-V and RF characterizations and nonlinear modeling of AlGaN/GaN HEMT

II.1 Introduction

In the first chapter, the different pulse measurement setups and pulsed measurement techniques dedicated to medium and high power transistors as well as nano-devices were presented. The main dispersion phenomena resulting from thermal and trapping effects that affect the device performances were discussed and particularly for AlGaN/GaN HEMTs.

This second chapter will start by presenting a brief history of microwave transistors in order to highlight the respective advantages of GaN-based semiconductors over its predecessors. Then, the physical properties of AlGaN/GaN HEMT structure and the formation of the 2-dimensional electron gas (2DEG) will be presented to understand the increased performances of such a device architecture. This brief presentation of the HEMT's physical properties will be followed by a review of its nonlinear modeling from pulsed I-V and RF measurements, including the nonlinear electro-thermal and trapping models, which were developed by previous PhD students of XLIM.

In the final part of this chapter, the pulsed setup presented in section V of Chapter-I, which was initially developed for nano-devices, will be used to perform innovative pulsed characterizations of a 2x75µm AlGaN/GaN HEMT with 0.15µm gate length fabricated at 3-5 Lab. These innovative characterizations techniques, such as very short pulses, will be detailed. They were used to observe trapping phenomena and its dependency on various parameters such as temperature, bias voltage and RF power. One of the important characterization technique developed and illustrated in this final experimental is the electrical history measurements. As an example, the results of such electrical history measurements are very useful for pulsed radar applications to quantify pulse to pulse stability. During this experimental study, the major limiting factors of AlGaN/GaN HEMT performances like drain current collapse and kink effect were characterized by specific pulsed I-V measurements.

II.2 GaN-based semiconductors

The development of radar imposed by military emergency during World War II [48] leads to a critical need for new electronics that could handle high power levels at RF and microwave frequencies. Initially, the design of pulsed radar were mainly based on the use of klystrons, travelling wave tubes, and cavity resonators (magnetrons). However, after the invention of the bipolar transistor in 1947, the place of semiconductor devices became more and more important for electronics. Since this date, the Silicon technology started to dominate the electronic world, which can be attributed to the tremendous decrease in device dimensions thanks to Moore's law [49], and therefore the integration of more and more transistors onto a single Silicon chip, i.e. Silicon VLSI (Very Large Scale Integration). Besides Silicon VLSI, however, there were other emerging fields in microelectronics. Among them, one of the prominent field is the radio frequency (RF) electronics with RF transistors as its basic building blocks. The term RF refers to electromagnetic waves at frequencies around and above 1 GHz and has constituted a limit to different device technologies.

In the 1960s, some new semiconductor devices have attracted the interest of circuit designers to be integrated in electronic radar systems as the main RF power amplification components. These new components include GaAs transferred electron devices (TED) or Si and GaAs IMPATT (impact ionization transit time) diodes. The development of RF transistors remains marginal until the 1980s because, unlike Silicon VLSI, there were no mass market driven by civil consumer applications except military. Since the 1980s, many civil applications, such as the satellite television, began to create a consumer market and drive the need for new components. Moreover, during the 1990s, the 2G cellular market revolutionized the communication industry by generating a mass consumer market at RF. Such a market growth of consumer applications at RF and microwave frequencies resulted in great technological developments of semiconductor transistors.

Depending on the specificities of consumer and military applications, there is a choice of semiconductor technologies for RF electronics, unlike VLSI, which is dominated by Silicon. Indeed, for RF and microwave applications, a wide variety of semiconductor materials exists (Si, SiGe, GaAs, InP and wide bandgap materials) associated to various transistor types such as bipolar junction transistor (BJT), heterojunction bipolar transistor (HBT), metal semiconductor field-effect transistor (MESFET), high electron mobility transistor (HEMT),

and metal-oxide-semiconductor field-effect transistor (MOSFET, LDMOS), which have found their respective applications.

Current civil and military applications at RF and microwave frequencies are satisfied by mature semiconductor technologies such as Si, GaAs, and other conventional III-V semiconductors. However, the wide bandgap semiconductors are the most promising technology for the next generation applications. Particularly, the wide bandgap Gallium Nitride (GaN) has attracted attention as the highly promising material for electronic applications because of its excellent transport properties, high critical electric field and thermal stability. Over other highly commercialized semiconductors such as Si and GaAs, GaN-based semiconductors offer five key advantages, which are high operating temperatures, high critical electric field, high current densities, high-speed switching and low on-resistances. A schematic comparison of this five figures of merit is given in Fig II-1.

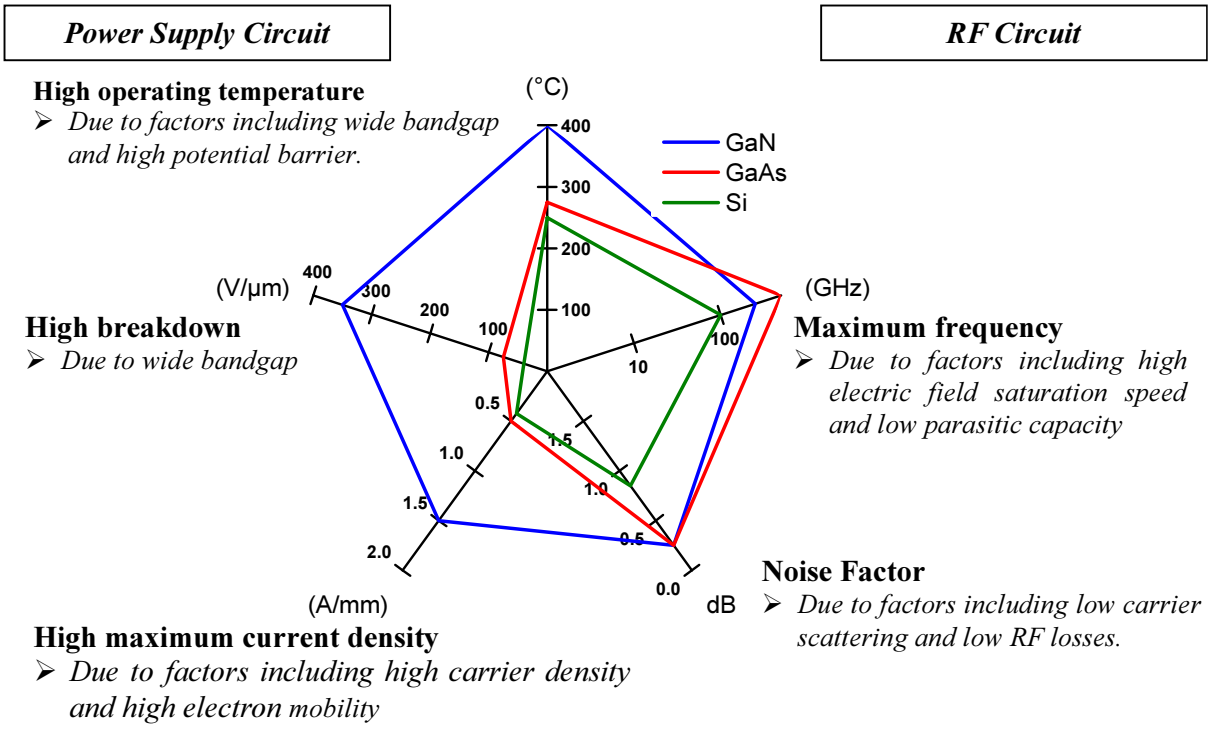

Fig II-1: Comparison of GaN with Si and GaAs semiconductors [50].

Indeed, to achieve high current densities at high operation frequencies, a semiconductor device should demonstrate high carrier mobility (μ) and high saturation velocity (v_{sat}). As an example, the high value of electron mobility μ_n for GaAs (8500 $cm^2.V^{-1}.s^{-1}$) is the decisive

reason for its greater potential to achieve high frequency performances, as shown in the performance of maximum frequency in Fig II-1. However, as also illustrated in Fig II-1, the GaN material demonstrates promising superior performances over its competitors.

In fact, unlike GaAs, a primary drawback of fabricating transistors from bulk GaN is the relatively low value of its electron mobility μ_n (900 $cm^2.V^{-1}.s^{-1}$) but this value is sufficient in the case of transistor types that are specially designed for high power operation. Actually, wide-bandgap semiconductor materials demonstrate relatively low values of electron mobility but very high values of saturation velocity, which are achieved at very high electric fields that they can withstand. Indeed, the levels of mobility and saturation velocity achieved by 2DEG in AlGaN/GaN hetero-junction are very suitable for high-power applications at very high frequencies. As illustrated in Table II-1, AlGaN/GaN HEMTs demonstrate much better values of mobility and saturation velocity than bulk GaN at room temperature. Moreover, due to piezoelectric and spontaneous polarization induced effects, the 2DEG sheet carrier concentration (n_s) of AlGaN/GaN structure is very high (experimental values up to 10^{13} cm^{-2}) in comparison with III-V semiconductors. To conclude this comparison, Table II-1 gives the intrinsic electronic properties for different bulk semiconductors along with realized devices.

	InAs (AlSb/ InAs)	**Si (SiGe-Si)**	**GaAs (AlGaAs/ InGaAs)**	**InP (InAlAs/ InGaAs)**	**4H SiC (-----)**	**GaN (AlGaN/GaN)**	**Diamond**
Bandgap (eV)	0.36	1.1	1.42	1.35	3.26	**3.49**	5.45
Electron mobility (cm^2/Vs)	33000 (25000)	1500 (2800)	8500 (8000)	5400 (10000)	700	**900 (>2000)**	4000
Saturated (peak) electron velocity ($x10^7$cm/s)	(4.0)	1.0 (1.0)	1.0 (2.1)	1.0 (2.3)	2.0 (2.0)	**1.5 (2.7)**	2.8
2DEG sheet electron density (cm^{-2})	$<6x10^{12}$	$2x10^{12}$	$<3x10^{12}$	$<4x10^{12}$	NA	**$1\text{-}2x10^{12}$**	NA
Critical breakdown field (MV/cm)	0.04	0.3	0.4	0.5	2.0	**3.3**	10
Thermal conductivity (W/cm·K)	0.27	1.5	0.5	0.7	4.5	**>2.0**	2.2
Relative dielectric constant (ε_r)	15.1	11.8	12.8	12.5	10	**9.0**	5.5

Table II-1: Comparison of thermal and electronic properties for different semiconductors and heterostructures

II.3 Structure of the GaN material

In order to present the creation of 2DEG in GaN HEMTs induced by spontaneous and piezoelectric polarization, this section will briefly introduce the structure of GaN material.

The Gallium Nitride and other group-III-N crystals exist under different crystalline structures (wurtzite, zinc-blende and rock-salt) [51], [52]. However, under thermodynamically stable conditions of growth, the (Al, In, Ga) N alloys have a crystal structure of wurtzite type. As shown in Fig II-2 in the case of GaN, this crystal structure called wurtzite consists of a hexagonal unit cell, which is defined by three lattice parameters (*a*, *c* and *u*). The lattice parameter *a* (*basal plane parameter*) corresponds to the edge length of the basal plane hexagon while the other lattice parameter *c* (*axial parameter*) corresponds to the height of the unit cell perpendicularly to the basal plane. The interatomic distance is defined by the internal parameter *u*. The ideal equilibrium values of a wurtzite lattice corresponds to an axial ratio $c_0/a_0 = \sqrt{8/3}$=1.633 with an internal parameter u_0=3/8=0.375 in fractional coordinates (units of *c*).

As illustrated by Fig II-2, the GaN wurtzite structure is non-centrosymmetric since it presents two different sequences of atomic layers for Ga and N along the two opposite directions [0001] and [000$\bar{1}$] parallel to the *c* axis. The atoms are arranged in bilayers that are made of two close hexagonal layers with one sub-lattice constituted of cations (Ga) while the other one is constituted of anions (N), thus creating polar faces. The corresponding (0001) and (000$\bar{1}$) faces shown in Figs II.2.a and II.2.b are called Ga-face and N-face, respectively. Since there is no inversion symmetry, a polarity of the crystal exists along the [0001] direction.

Due to the non-centrosymmetric structure of wurtzite lattice together with the large difference in electronegativity between the group-III metal and the nitrogen, these III-N structures exhibit a high level of spontaneous polarization P_{SP} (i.e. without applied strain) [53]. The polarity of the crystal determines the directions of the polarization along the *c*-axis. As illustrated in Fig II-2(a) and II-2(b) for GaN, the spontaneous polarization P_{SP} is pointing from the Ga-face (cation-face) to the substrate while the direction of P_{SP} is inversed for the N-face (anion-face).

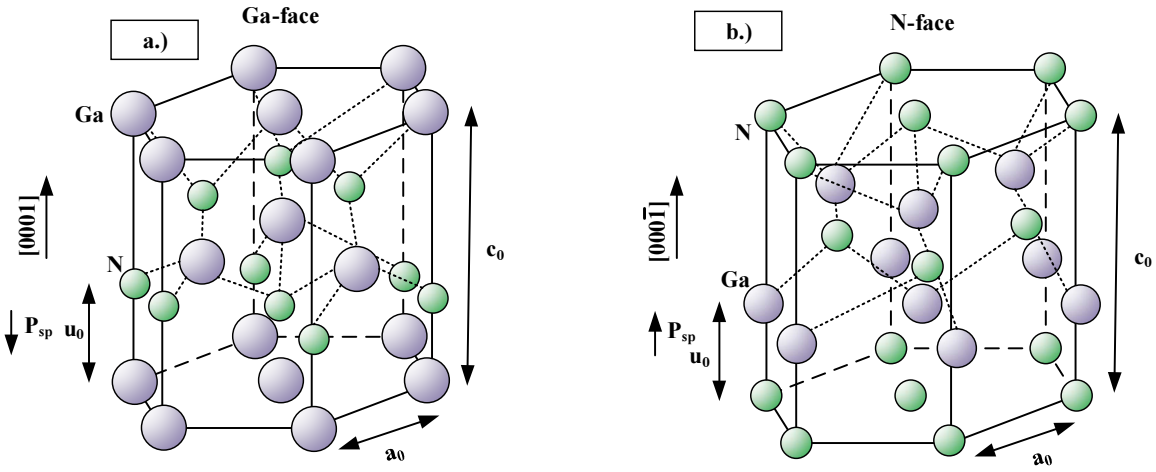

Fig II-2: Illustration of an ideal wurtzite structure of GaN lattice a) Ga-face b) N-face [50].

Moreover, when a strain is imposed to the GaN crystal, the equilibrium structural parameters (*a*, *c*) of the lattice will change so that an additional piezoelectric polarization P_{PE} will result since there is no symmetry of inversion in the wurtzite structure. The piezoelectric polarization P_{PE} of the wurtzite GaN in the direction of the *c*-axis can be written [54] as a function of the structural strain by:

$$P_{PE} = e_{33}\,\varepsilon_z + e_{13}\,(\varepsilon_x + \varepsilon_y) \qquad \text{(II-1)}$$

with $\varepsilon_z = \frac{(c-c_0)}{c_0}$, $\varepsilon_x = \varepsilon_y = \frac{(a-a_0)}{a_0}$ and $\varepsilon_z = -2.\frac{C_{13}}{C_{33}}.\varepsilon_x$ (II-2)

so that finally $P_{PE} = 2\,\frac{(a-a_0)}{a_0}\left[e_{13} - e_{33}\,\frac{C_{13}}{C_{33}}\right]$ (II-3)

where ε_z is the strain along the *c*-axis, (ε_x and ε_y) are the basal-plane strains assumed to be isotropic, (e_{33} and e_{13}) are the piezoelectric coefficients, (C_{33} and C_{13}) are the elastic constants, (a_o, c_o) are the equilibrium values of the lattice parameters (*a*, *c*).

The values of equilibrium lattice parameters, piezoelectric coefficients and elastic constants are compared in Table II-2 for wurtzite structures of AlN, GaN and InN.

	AlN	GaN	InN
a_0 (Å)	3.112	3.189	3.540
c_0 (Å)	4.982	5.185	5.705
c_0/a_0	1.601	1.626	1.612
P_{SP} (C/m^2)	-0.081	-0.029	-0.032
e_{33} (C/m^2)	1.46	0.73	0.97
e_{13} (C/m^2)	-0.6	-0.49	-0.57
C_{33} (GPa)	395	379	182
C_{13} (GPa)	120	70	121
e_{13}-$e_{33}(C_{13}/C_{33})$	-0.86	-0.68	-0.9

Table II-2: Comparison of lattice parameters, spontaneous polarization, piezoelectric and elastic constants of wurtzite AlN, GaN, and InN [54].

In Eq II-3 giving the piezoelectric polarization P_{PE}, it should be noted that the term $(e_{13} - e_{33}\, C_{13}/C_{33})$ is always negative in wurtzite structures of group-III-nitrides since their piezoelectric coefficient e_{13} is always negative while their coefficients (e_{33}, C_{13}, C_{33}) are always positive. Thus, in group-III-nitrides, Eq II-3 shows that the sign of P_{PE} is opposite to the sign of in-plane strain $(a\text{-}a_o)/a_o$ so that the sign of P_{PE} in the [0001] direction is always negative for layers with tensile strain $(a > a_o)$ and positive for layers with compressive strain $(a < a_o)$. Moreover, the spontaneous polarization P_{SP} of group-III-nitrides is always negative in the [0001] direction. The resulting directions of P_{SP} and P_{PE} are illustrated in Fig II-3 for GaN and AlGaN without strain and with compressive or tensile strain.

It should be noted that, in the case of tensile strain applied to layers (Fig II-3b), P_{SP} and P_{PE} are added in the same direction, while in the case of compressive strain (Fig II-3a) P_{SP} and P_{PE} are in opposite directions. The high levels of spontaneous and piezoelectric polarizations P_{SP} and P_{PE} in wurtzite group-III-nitrides are about ten times higher than those observed in III-V semiconductors.

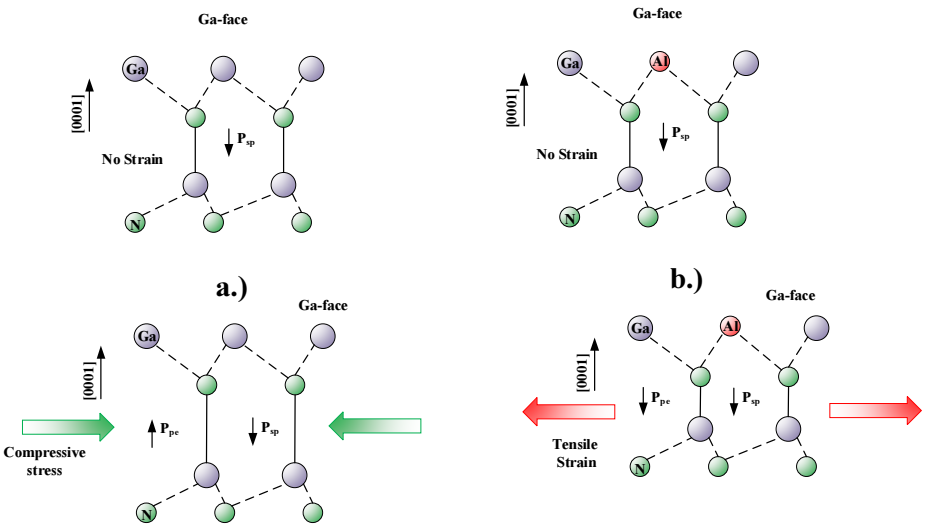

Fig II-3: Directions of spontaneous P_{SP} and piezoelectric P_{PE} polarizations for a) GaN Ga-face compressive strain and b) AlGaN Ga-face tensile strain [50].

II.3.1 2DEG formation

The unique feature of AlGaN/GaN HEMTs is characterized by the channel formation. High levels of polarization at the interface of AlGaN/GaN heterostructure induce a polarization sheet charges σ in the high bandgap AlGaN, which causes the accumulation of attracted mobile carriers (electrons in the case of a positive sheet charge σ) confined in a quantum well along the heterojunction, as shown in Fig II-4. This electron accumulation induced by polarization is called a 2-Dimensional Electron Gas (2DEG). Since the quantum well is located in a non-intentionally doped (nid) region, the confined electrons exhibit very high mobility, which is the key feature of HEMTs.

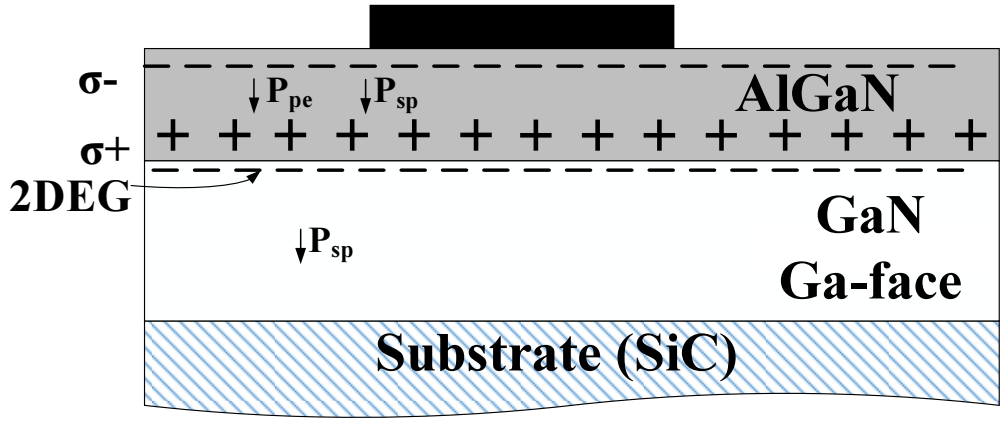

Fig II-4: Polarization and charges in AlGaN/GaN HEMTs [16].

AlGaN/GaN heterostructures are grown along the [0001] direction (*c*-axis) so that the polarization is always perpendicular to the heterostructure interface (Fig II-4). Therefore, the induced sheet charge σ created at the abrupt interface between the top layer (AlGaN) and the bottom layer (GaN) can be written as the change of spontaneous and piezoelectric polarizations across the heterostructure interface.

$$\begin{aligned}\sigma &= P_{TopLayer} - P_{BottomLayer} \\ &= \{P_{SP-AlGaN} + P_{PE-AlGaN}\} - \{P_{SP-GaN} + P_{PE-GaN}\}\end{aligned} \quad \text{(II-4)}$$

In Eq II-4, the piezoelectric polarization P_{PE-GaN} is negligible since the GaN buffer is assumed relaxed without strain. Moreover, the AlGaN layer is under tensile strain so that both piezoelectric $P_{PE-AlGaN}$ and spontaneous $P_{SP-AlGaN}$ polarizations add up with same sign. Therefore, the polarization induced sheet charge σ is expressed

$$\sigma = \{P_{SP-AlGaN} + P_{PE-AlGaN}\} - \{P_{SP-GaN}\} \quad \text{(II-5)}$$

To compensate this sheet charge σ, mobile carriers will be attracted at the interface. In the case of a fairly high band offset of the AlGaN/GaN heterostructure associated to a positive sheet charge ($\sigma > 0$), an accumulation of free electrons will appear at the interface at a sheet carrier concentration of n_s. In the other case of a negative sheet charge ($\sigma < 0$), it will result in hole accumulation. For Ga-face AlGaN/GaN structure, the polarization induces a positive sheet charge ($\sigma > 0$) as illustrated in Fig II-4.

The accumulated electrons are more confined at the interface by the existing difference between spontaneous polarization of GaN and AlGaN. Moreover, the piezoelectric polarization of the AlGaN barrier under tensile strain increases the polarization variation at the interface, and thus the sheet charge σ, and in turn the sheet carrier concentration n_s of the 2DEG.

Indeed, the sheet charge density σ and thus the sheet carrier concentration n_s of the 2DEG at the AlGaN/GaN interface depends on the content x of Aluminium in the $Al_xGa_{1-x}N$ barrier [55], [56]. The maximum sheet carrier concentration can be expressed [25], [28]:

$$n_s(x) = \frac{\sigma(x)}{q} - \frac{\varepsilon_0 \varepsilon_r(x)}{q^2 d}[q\Phi_b(x) + E_F(x) - \Delta E_c(x)] \quad \text{(II-4)}$$

where σ is the polarization induced sheet charge density, q is the electron charge, (ε_0, ε_r) are vacuum and relative permittivity's, d is the thickness of AlGaN barrier, $q\phi_b$ is the

Schottky barrier of the gate contact on top of AlGaN, E_F is the position of Fermi level with respect to the edge of the GaN conduction band energy, $\Delta E_c(x)$ is the offset of conduction band energy at the AlGaN/GaN interface.

The sheet carrier concentration increases with the Al-content but suited values of x are chosen between 0.15 and 0.4. Indeed, lower values of x give too small conduction band offset resulting in bad carrier confinement while higher values increase the lattice and thermal mismatches between barrier and GaN buffer resulting in a high level of structural defects that limit the 2-DEG mobility.

To illustrate the creation of quantum well and 2-DEG at a standard AlGaN/GaN interface, Fig II-5 presents the charge distribution, electric field and band diagram along the heterostructure.

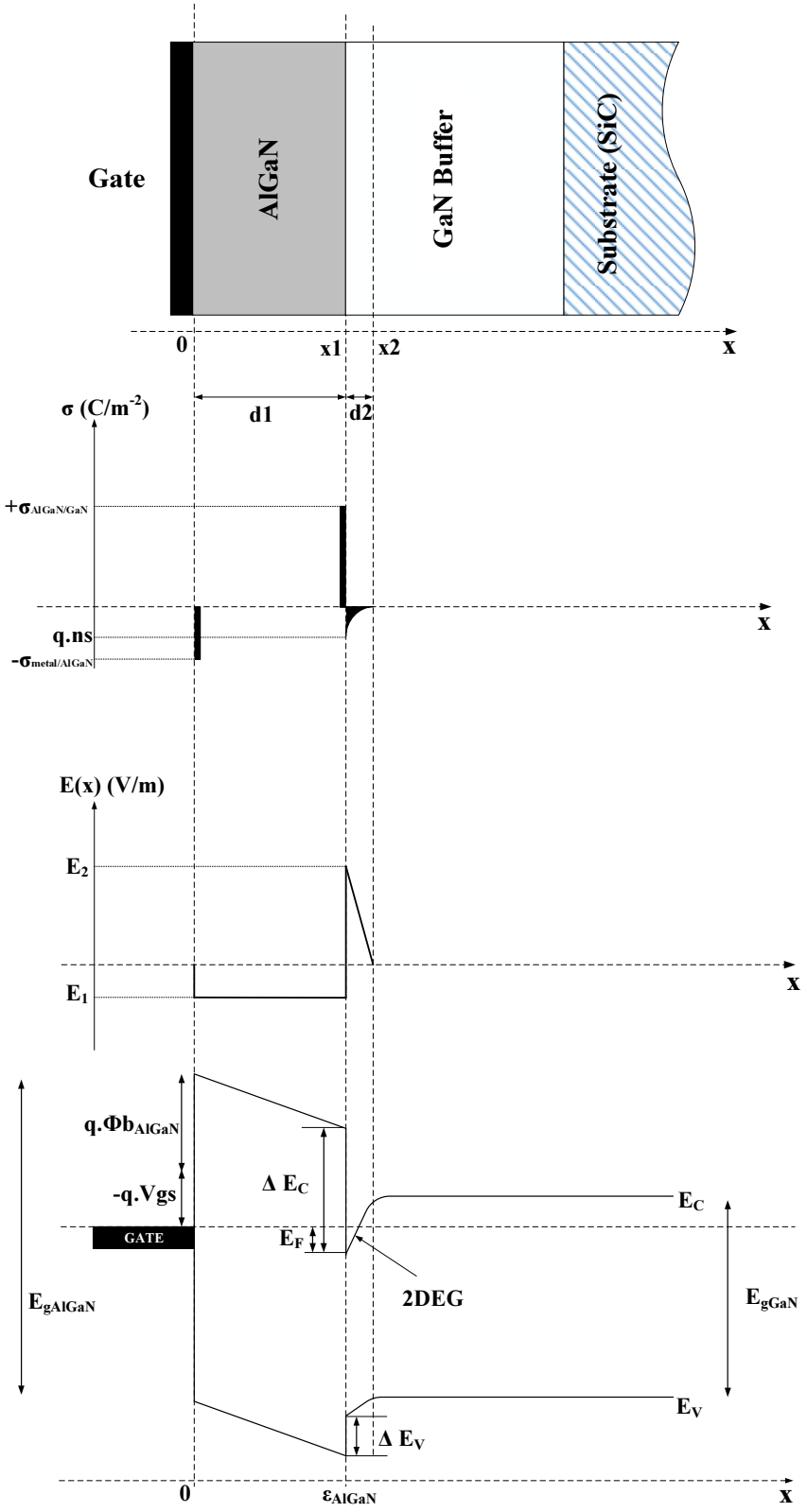

Fig II-5: Charge distribution, electric field and energy band diagram of an AlGaN/GaN HEMT heterostructure [16] .

II.4 Electrical circuit modeling of GaN HEMTs

The electrical circuit modeling of HEMTs or any transistor consists in generating a specific network of lumped circuit elements that represent the fundamental behavior of the device. The aim of electrical modeling is to allow designers to simulate in CAD tools the nonlinear behaviors of the device under complex electrical signals. Such a nonlinear electrical model is highly critical for the design flow. As illustrated in Fig II-6 (a), the electrical topology of the model is often directly correlated to physical entities associated to the extrinsic and intrinsic device structure. The main analytical nonlinear equations of GaN HEMTs presented in this section, and used in this work, are based on previous nonlinear modeling studies at XLIM. These model equations and modeling flow were principally developed to fit the specific large signal operation of high power microwave amplifiers (HPA) in the saturated operation area of I-V characteristics.

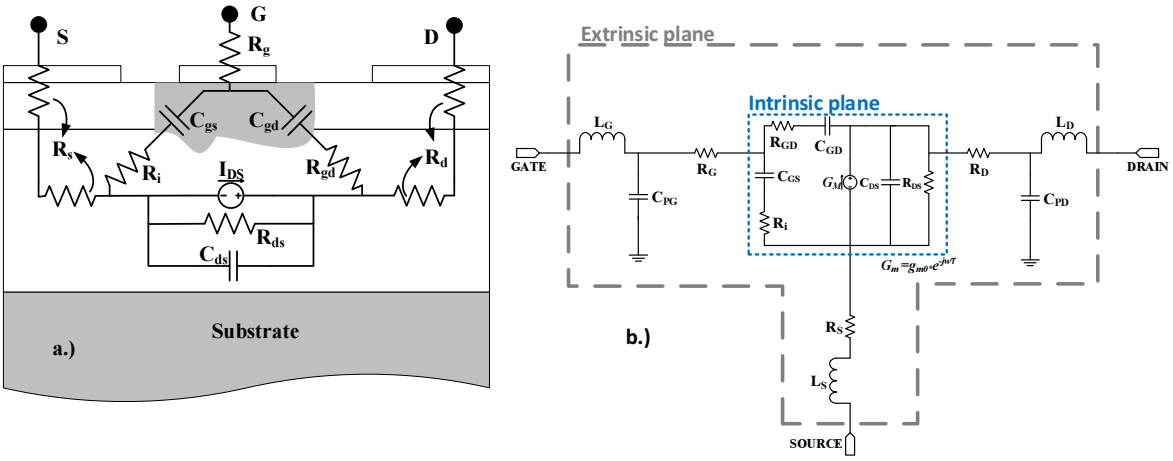

Fig II-6: a.) Cross-section of HEMT device associating a physical origin to each electrical element of the model. b.) Circuit schematic of the small signal HEMT model.

Fig II-6 (b) represents the classical small-signal HEMT model, which is mainly composed of a voltage-controlled current source and passive linear components. This electrical model can be divided into two parts as shown in Fig II-6 (b): the "intrinsic part" of the transistor modeling the active region under the gate and the "extrinsic part" modeling the passive access regions of the device. In the classical HEMT topology, the intrinsic part is represented with a set of 8 intrinsic elements (R_{GD}, R_i, C_{GS}, C_{GD}, C_{DS}, G_M, R_{DS}, and τ) while the extrinsic part is represented with a set of 8 extrinsic elements (R_G, R_D, R_S, L_G, L_D, L_S, C_{PG}, C_{PD}) as shown in Fig II-6 (b).

These 16 elements of the small-signal HEMT model need to be extracted from specific linear measurements of the device when biased at a given operating point. It must be noted that the values of a small-signal model are only valid at a given bias point. The main steps of the modeling process will be discussed in the following section.

II.4.1 Small-signal circuit modeling of HEMTs

The linear model extraction is a crucial step since this model will be the initial basis for the final extraction of a nonlinear model. The extraction process used at XLIM is based on the optimization of extrinsic elements to meet the condition of frequency-independent intrinsic elements as previously published in [57].

Using an initial set of extrinsic values (R_G, R_D, R_S, L_G, L_D, L_S, C_{PG}, C_{PD}), the measured "extrinsic S-parameters" at the extrinsic HEMT access are de-embedded to give the "intrinsic Y-parameters" at the intrinsic reference planes of the transistor. Using these "Intrinsic Y-parameters", the value of each intrinsic element (R_{GD}, R_i, C_{GS}, C_{GD}, C_{DS}, G_M, R_{DS}, and τ) can be analytically calculated at each frequency using the following equations:

$$Cgd = \frac{-Im(Y_{12})}{\omega}\left[1+\left(\frac{Re(Y_{12})}{Im(Y_{12})}\right)^2\right] \quad \text{(III-5)}$$

$$Rgd = \frac{-Re(Y_{12})}{(Cgd.\omega)^2}\left[1+\left(\frac{Re(Y_{12})}{Im(Y_{12})}\right)^2\right] \quad \text{(III-6)}$$

$$Cgs = \frac{Im(Y_{11})+Im(Y_{12})}{\omega}\left[1+\left(\frac{Re(Y_{11})+Re(Y_{12})}{Im(Y_{11})+Im(Y_{12})}\right)^2\right] \quad \text{(III-7)}$$

$$Gd = Re(Y_{12})+Re(Y_{22}) \quad \text{(III-8)}$$

$$Cds = \frac{Im(Y_{12})+Im(Y_{22})}{\omega} \quad \text{(III-9)}$$

$$Ri = \frac{Re(Y_{11})+Re(Y_{12})}{(Cgs.\omega)^2}\left[1+\left(\frac{Re(Y_{11})+Re(Y_{12})}{Im(Y_{11})+Im(Y_{12})}\right)^2\right] \quad \text{(III-10)}$$

$$Gm = \sqrt{(A^2+B^2)(1+Ri^2Cgs^2\omega^2)} \quad \text{(III-11)}$$

$$\tau = \frac{-1}{\omega}.arctan\left[\frac{B+A.Ri.Cgs.\omega}{A-B.Ri.Cgs.\omega}\right] \quad \text{(III-12)}$$

where:

$$A = Re(Y_{21}) - Re(Y_{12}) \quad \text{(III-13)}$$

$$B = Im(Y_{21}) - Im(Y_{12}) \quad \text{(III-14)}$$

Given that the value of each intrinsic element have to be independent of the frequency, the values of extrinsic elements are optimized to meet this requirement using a dedicated optimization algorithm based on the simulated annealing method. Moreover, the values of extrinsic elements have to be bias-independent, which is not the case of intrinsic elements.

Therefore, this extraction process of extrinsic and intrinsic elements can be applied to a set of multi-bias measured S-parameters given that the extrinsic parameters are bias-independent.

II.4.2 Nonlinear circuit modeling of HEMTs

The topology of the intrinsic nonlinear model of current sources that are present in measured I-V characteristics is represented in Fig II-7. This intrinsic static part consists of the access resistances (*Rg*, *Rd*, *Rs*), the main drain current source I_{ds}, the breakdown current source I_{bk}, and the two Schottky gate diodes (I_{gs}, I_{gd}).

When modeling the nonlinear current sources, it should be noted that the values of extrinsic access resistances are already known as explained in the previous section on small-signal circuit modeling. First, the next subsections will give some examples of nonlinear equations that have been developed to fit the behavior of each of these current sources although many other equations have been published in the literature. Later, examples of equations for the intrinsic nonlinear modeling of intrinsic gate capacitances (*Cgs*, *Cgd*) will be reported as well as the specific modeling of critical parasitic phenomena which are thermal and trapping effects. Particularly, trapping model will be discussed in detail.

Finally, all these subsections are intended to provide a brief overview of the complete nonlinear HEMT model which is used at XLIM for large signal analysis and design of GaN HEMT power amplifiers.

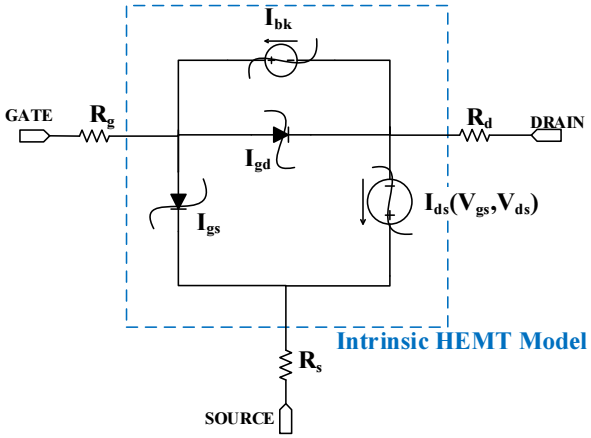

Fig II-7: Intrinsic nonlinear current sources of HEMT.

II.4.2.1 Examples of drain current equation

The fundamental property of FET is described by a voltage-controlled nonlinear current source *Ids*, which is driven by the gate-to-source voltage *Vgs* and the drain-to-source voltage *Vds*. One of the most suited nonlinear equation of *Ids* to fit the I-V characteristics is based on the Tajima equations [58] specifically developed for GaAs FET amplifier. These equations are also well suited to modeling GaN HEMTs.

$$Id_{Tajima} = \frac{Idss}{1-\frac{1-e^{-m}}{m}}\left[Vgsn - \frac{1-e^{-m}}{m}\right]\left[1-e^{-Vdsn(1-a.Vdsn-b.Vdsn^2)}\right] \quad \text{(III-15)}$$

where

$$Vgsn = 1 + \frac{Vgs(t-\tau) - V\varphi}{Vp} \quad \text{(III-16)}$$

$$Vdsn = \frac{Vds}{Vdsp\left(1 + W.\frac{Vgs(t-\tau)}{Vp}\right)} \quad \text{(III-17)}$$

$$Vp = Vp_0 + P.Vdsp + V\varphi \quad \text{(III-20)}$$

One correction term α_{GMGD} is often added to this equation to model the decrease of transconductance in GaN HEMTs [31].

$$Id = Id_{Tajima}.\alpha_{GMGD} \quad \text{(II-18)}$$

where

$$\alpha_{GMGD} = 1 + \beta_{gm}.[Vds + Vdm].[1 + \tanh(Vgs - Vgm)] \quad \text{(II-19)}$$

This equation has 13 parameters (*Idss*, *m*, *a*, *b*, *P*, *Vφ*, Vp_0, *Vdsp*, *W*, *Vgm*, *Vdm*, α_{gm} and β_{gm}). A modified version of the Tajima equation was developed in [16] to model the nonlinear current source in a large operating area such as very large negative drain voltages.

II.4.2.2 Nonlinear gate-to-source and gate-to-drain diodes

As illustrated in Fig II-7, the gate contact is modeled by two diodes that connect gate to source and gate to drain. These current sources represent the gate leakage current for positive gate voltages *Vgs* and *Vgd*, respectively. As an example, the Schottky diode equations are:

$$Igs = Is_{gs}.\left[e^{\frac{q.Vgs}{N_{gs}.k.T}} - 1\right] \quad \text{(III-20)}$$

$$Igd = Is_{gd}.\left[e^{\frac{q.Vgd}{N_{gd}.k.T}} - 1\right] \quad \text{(III-21)}$$

Each diode equation has 2 parameters (Is_{gs} and N_{gs}) and (Is_{gd} and N_{gd}). In the case of GaN HEMTs, the gate-to-drain diode equation has often to be modified as explained in [16].

II.4.2.3 Breakdown current source

As illustrated in Fig II-7, the drain-to-gate breakdown phenomenon is modeled by a current source I_{bk}, which can be simply expressed as an exponential increase of the gate-to-drain current when the breakdown voltage V_{GD} is reached. A soft quasi-exponential function (*exp_soft*) is used to keep an expression well suited for convergence [33], as illustrated below.

$$I_{bk} = Iav_{gd}.\left[exp\_soft(\alpha_{gd}Vds)\right] \quad \text{(III-22)}$$

However, the nonlinear breakdown source is of little or no interest in modeling GaN HEMTs since they have very large breakdown voltages far beyond the operating voltages.

II.4.3 Nonlinear capacitance modeling

The gate-to-source and gate-to-drain capacitances *Cgs* and *Cgd* present a nonlinear dependence on both control voltages *Vgs* and *Vgd*. However, for the sake of simplicity, the

capacitance values are extracted along the ideal operation load-line so that the nonlinear model of *Cgs* and *Cgd* can be reduced to only one control voltage *Vgs* or *Vgd*, respectively. From the multi-bias measured S-parameters, the extracted values of *Cgs* and *Cgd* along the estimated load line can be precisely fitted with hyperbolic tangent equations [59]:

$$C_{gx} = C_0 + \frac{C_1 - C_0}{2}\left[1 + \tanh(a(V_{gx} + V_m))\right] - \frac{C_2}{2}\left[1 + \tanh(b(V_{gx} + V_p))\right] \quad \text{(III-23)}$$

where C_{gx} and V_{gx} stand for the gate-to-x capacitance and voltage, respectively, i.e. (C_{gs} and V_{gs}) or (C_{gd} and V_{gd}). The seven modeling parameters (C_0, C_1, C_2, a, b, V_p and V_m) are different for each of the capacitance model.

II.4.4 Thermal dependence in the model

Temperature dependency and self-heating effect are not negligible in the actual operation of HEMTs. In the first Chapter, we already presented the pulsed setup and discussed the different effects that are caused by thermal effects. In this section, we present some example of equations that have been developed at XLIM [16], [33] to account for the temperature dependence of model parameters in the case of HEMT devices. Isothermal pulsed measurements have shown that in the device's operating area, the temperature has an almost linear impact on the current source *Ids*, the access resistances (*Rs*, *Rd*) and the ideality factors (N_{gs}, N_{gd}) of diodes, except the diode saturation currents that demonstrate an exponential variation. The following equations illustrate the temperature dependence of linear elements and nonlinear equation parameters, which have been presented in the previous section.

Access resistances:

$$Rs = Rs_0.(1 + \alpha_{Rs}.T)$$
$$Rd = Rd_0.(1 + \alpha_{Rd}.T) \quad \text{(III-24)}$$

Current source (Tajima equation in Eq. II-17 and II-20):

$$Idss = Idss_0.(1 + \alpha_{Idss}.T)$$
$$P = P_0.(1 + \alpha_P.T) \quad \text{(III-25)}$$

Gate-to-source and drain-to-source diodes (in Eq. II-23 and II-24):

$$N_{gs} = N_{gs0}.\left(1 + \alpha_{Ngs}.T\right)$$
$$Is_{gs} = Is_{gs0} + Is_{gsT}.e^{\left(\frac{T}{Ts_{gs}}\right)} \quad \text{(III-26)}$$
$$N_{gd} = N_{gd0}.\left(1 + \alpha_{Ngd}.T\right)$$
$$Is_{gd} = Is_{gd0} + Is_{gdT}.e^{\left(\frac{T}{Ts_{gd}}\right)} \quad \text{(III-27)}$$

These temperature-dependent equations allow the designer to account for self-heating effect during nonlinear simulations as soon as the model topology is associated to an electro-thermal circuit that consists of the thermal resistances and capacitances of the device.

II.4.5 Electrical modeling of trapping effects

As already presented in the first Chapter, trapping effects play a not negligible role in GaN HEMT operation with critical parasitic effects on electrical performances. Many of these effects can be characterized through pulsed I-V measurements as presented in Chapter I but the nonlinear circuit modeling is still under development. However, a reference study of dynamic trap circuit modeling was published in [16] [60] by O. Jardel.

The trapping effects are modeled through the modulation of the drain current source by gate and drain stimulus. This modeling is done by adding a new "trap sub-circuit" to the nonlinear circuit model that dynamically modify the actual gate and drain control voltages with respect to trap emission and trap capture process. An example of the drain-lag sub-circuit schematic is presented in Fig II-8. This drain-lag schematic has two input voltages *Vgs* and *Vds* while the output voltage generated by the drain-lag model *Vgs_int* is the actual gate-to-source control voltage of the nonlinear drain current source.

The drain-lag sub-circuit schematic presented in Fig II-8 [60] is mainly composed of two parts. The left part of the schematic operates as an envelope detector that reproduces the asymmetrical time constants of emission and capture process of traps. Depending on the drain voltage variation, the diode will conduct or not so that to define the capture or emission time constants. When the diode conducts (i.e. the drain voltage variation is positive), the current flows through the resistor $R_{capture}$ and charges the capacitor *C* to model the capture process with

the associated time constant $\tau_{capture}$ defined by the product of $R_{capture}$ and C. When the diode is blocked (i.e. the drain voltage variation is negative), the capacitor C discharges through the resistor $R_{emission}$ given that the resistance $R_{emission}$ is much larger than $R_{capture}$. This discharge models the emission process with the associated time constant $\tau_{emission}$ defined by the product of $R_{emission}$ and C. The voltage Vc of the capacitor C is related to the density of trapped charges.

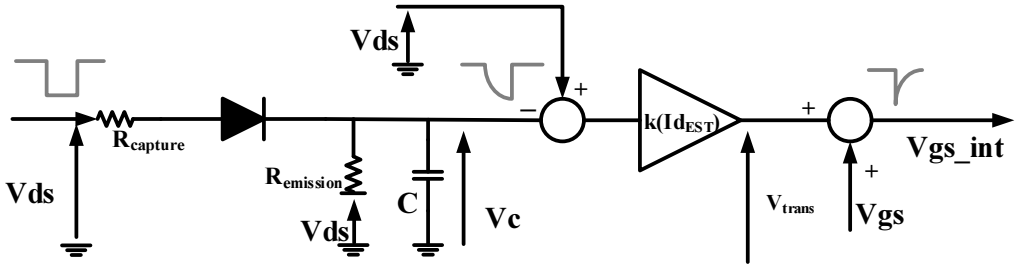

Fig II-8: Drain-lag sub-circuit: the left part synthesizes the equivalent charge of trap while the right part processes the voltages to generate the actual control voltage Vgs_int [60].

Finally, the second part of the drain-lag sub-circuit schematic performs the processing of the capacitor voltage *Vc* in order to generate the actual gate control voltage *Vgs_int* which is modified by the presence of traps. The model equations are given below to process the capacitor voltage *Vc* using the amplification factor *k* [16] shown in Fig. II-8 which is linked to the amplitude of the trap and to the estimated drain current Id_{EST} by:

$$k(Id_{EST}) = krel.Id_{EST}(V_{gs}).A_{DL} \quad \text{(III-28)}$$

with

$$Id_{EST}(V_{gs}) = Gm_{DC}.[V_{gs} - V_{pincement}] \quad \text{(III-29)}$$

where Gm_{DC} and A_{DL} are fitting parameters while *krel* is the sum of each trap contribution $krel_n$ in the case of *n* different trap states.

$$krel = \sum_{1}^{n} krel_n \quad \text{(III-30)}$$

Finally, given the summing and amplifying blocks of the drain-lag sub-circuit schematic in Fig. II-8, the modeling process of the actual gate control voltage *Vgs_int* is defined by the following equation:

$$V_{gs\_int} = V_{gs} + k(Id_{EST}).(V_{ds} - V_C) \quad \text{(III-31)}$$

So that the actual drain current will be expressed as:

$$I_{ds} = f(V_{gs\_int}, V_{ds}) \quad \text{(III-32)}$$

As an example of the drain-lag impact observed in I-V characteristics, the chronogram presented in Fig II-9 [7] shows the internal voltages appearing within the drain-lag model of Fig. II-8 in the case of a nonlinear simulation for a drain voltage pulse from 30V to 10V during a pulse width that is enough large to observe emission and capture process on the simulated intrinsic voltages and drain current. The level of the control voltage *Vgs_int* is mainly determined by the high level of the drain voltage in pulsed conditions. As it can be observed, the drain-lag model allows designers to simulate the current transients and time constants associated to the capture and emission phenomena.

As the drain voltage *Vds* comes from 30V to 10V, the diode of the drain-lag sub-circuit is blocked and the capacitor *C* is discharged through $R_{emission}$ with an associated time constant $\tau_{emission}$. The resulting transients of the carrier emission can be observed in Fig. II-9 on the time-domain internal voltages (*Vc*, *Vtrans*) and the final output voltage *Vgs_int,* which directly shapes the transient of the *Ids* drain current. It can be noted that the gate voltage is very close to pinch-off, in order to avoid self-heating and its related transients.

Moreover, as the drain voltage *Vds* returns from 10V to 30V after enough time to complete emission process, the diode of the drain-lag sub-circuit conducts and the capacitor *C* is charged through $R_{capture}$ with an associated time constant $\tau_{capture}$. The resulting transients of the carrier capture can be observed in Fig. II-9 on the time-domain internal voltages (*Vc*, *Vtrans*) and the final output voltage *Vgs_int,* which directly shapes the transient of *Ids* current.

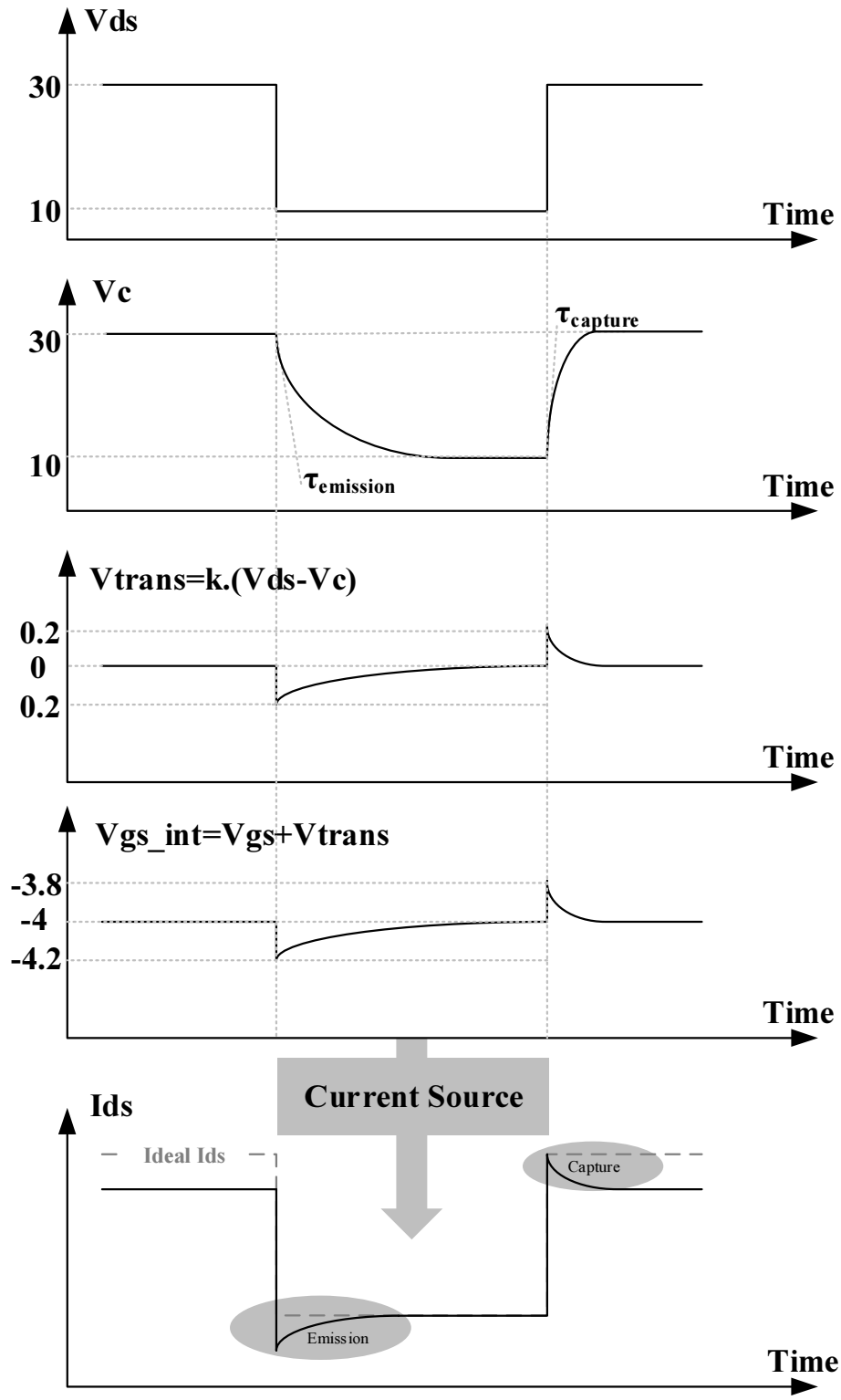

Fig II-9: Chronogram of internal voltages and drain current in the drain-lag sub-circuit model for a negative drain pulse from 30V to 10V [61].

A similar model architecture is adopted for the gate-lag modeling in [7]. The gate-lag sub-circuit is presented in Fig II-10. The main differences with the drain-lag sub-circuit are that the control voltage of the envelope detector becomes *Vgs* instead of *Vds*, the emission resistor is referenced to *Vgs* instead of *Vds*, the diode is reversed, and there is only one input voltage *Vgs* and an output voltage *Vgs_int*. Thus, as the diode is reversed, unlike to the drain-lag model, the emission process of gate-lag is active when the *Vgs* voltage increases while the capture process of gate-lag takes place when the *Vgs* voltage decreases.

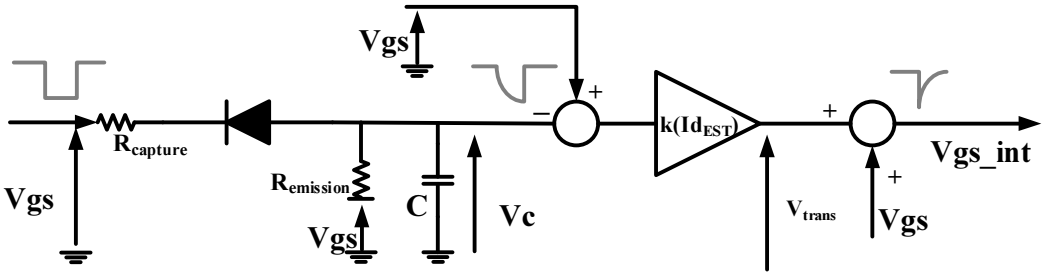

Fig II-10: Gate-lag sub-circuit [60].

Finally, the complete nonlinear model topology is presented in Fig. II-11, which integrates all intrinsic nonlinear capacitances and current sources as well as the gate-lag/drain-lag sub-circuits and the temperature-dependent equations of access resistances, diodes and current source. The only remaining schematic that should be associated to dynamically compute self-heating is the electro-thermal equivalent circuit made of the thermal resistances and capacitances.

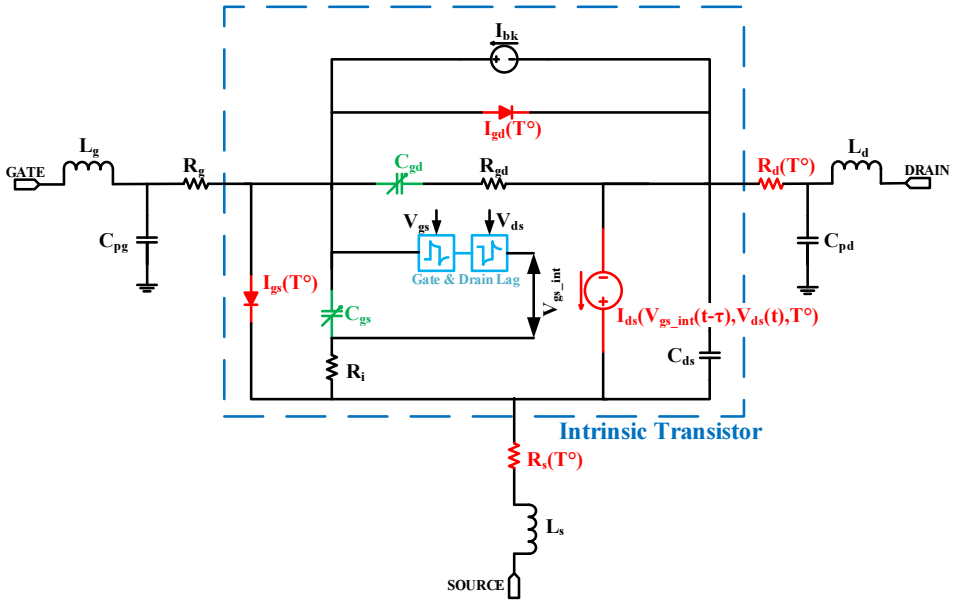

Fig II-11: Nonlinear HEMT model including thermal and trapping effects.

II.5 Kink effect and current collapse

II.5.1 Introduction

GaN HEMT is the most promising candidate for future wireless and radar applications since the intrinsic material properties of GaN like high electron mobility, wide band-gap and high electron saturation velocity give it superiority over its predecessors like Si and GaAs devices. Although these devices are already in the commercial market, especially for power applications, many issues of GaN technology still need to be addressed. Among these, one of the most important issues is the drain current collapse and kink effect that directly affects the output power, gain and RF transitions of microwave devices under pulsed modulated signals.

Similar behavior (kink effect) was already observed and reported for GaAs HEMTs [62] where it is caused by impact ionization, which leads to a sudden rise in drain current. The Fig II-12(a) illustrates the kink behavior of GaAs HEMTs on I-V characteristics. This explanation is not well suited for GaN devices due to their high breakdown voltage although it can be true at very low temperatures [63]. Kink effect in GaN HEMTs is mainly attributed to carrier trapping [64]. The Fig II-12(b) illustrates the kink characteristics of GaN HEMT.

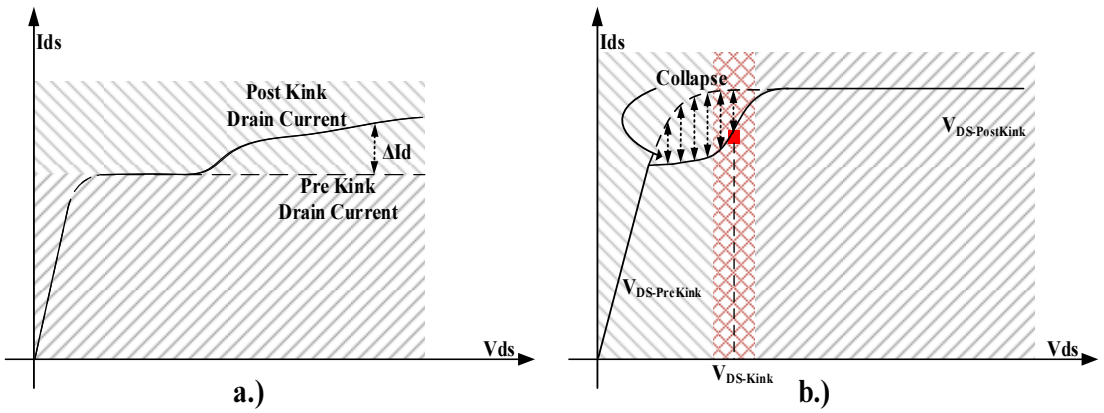

Fig II-12: Schematic of a.) GaAs HEMT Kink Characteristics, b.) GaN HEMT kink Characteristics.

During this work, we performed an experimental investigation on kink effect and trapping dynamics in GaN HEMTs by using the pulsed I-V setup developed in this work.

A series of I-V measurements were performed under DC and pulsed conditions to characterize the influence of key parameters involved in carrier trapping and responsible for current collapse and kink effect. All these measurements were performed with respect to the impact of temperature and drain voltage [65].

II.5.2 Influence of maximum drain voltage

In order to illustrate the impact of the maximum drain voltage $V_{DS\text{-}MAX}$, a set of pulsed I-V measurements associated to different maximum drain voltages were performed on a 2x75µm AlGaN/GaN HEMT of 0.15µm gate-length.

Each pulsed I-V measurement shown in Fig. II-13 is performed at a cold quiescent bias point (V_{DSq} =0V) so that to neglect thermal effect. The gate-to-source voltage V_{GS} is stepped from +1.5V to -3.5V in steps of 1V while the drain-to-source voltage V_{DS} is swept from 0 V to the maximum drain voltage $V_{DS\text{-}MAX}$. Fig. II-13 shows the measured I-V characteristics measured for different set of maximum drain voltages $V_{DS\text{-}MAX}$ of 10V, 20V, 25V, 35V and 40V.

The gate pulse-width was 800ns and the drain pulse-width was 600ns with 10µs period. The value of each *Ids* points in the pulsed I-V characteristics of Fig. II-13 is an average of 1000 measured pulses. The purpose is to stress the device in pulsed conditions with electrical voltages without inducing self-heating. Moreover, as trapping is an asymmetrical process with a fast capture process and a slow emission process, the 10µs period is not long enough to complete the emission process. Hence, it is safe to say that this characterization is unique to quantify trapping effects while eliminating thermal effects.

For $V_{DS\text{-}MAX}$ < 20V in Fig. II-13, no kink effect was visible at all V_{GS} values. However, as $V_{DS\text{-}MAX}$ is increased, the kink effect becomes prominent. This can be explained by the electric field induced by V_{GD} during the former sweep that leads to electrons filling the ionized donor like traps, and thus results in kink for later sweeps. Each set of pulsed I-V characteristics were measured with a time interval of 6 hours during which no potentials were applied for both gate and drain. Therefore, during the first sweep (V_{GS}= +1.5V) of each set of pulsed I-V, we do

not observe significant kink because the time interval of 6hours gives enough time to emit electrons back to the channel. However, this time interval is not sufficient for all $V_{DS\text{-}MAX}$.

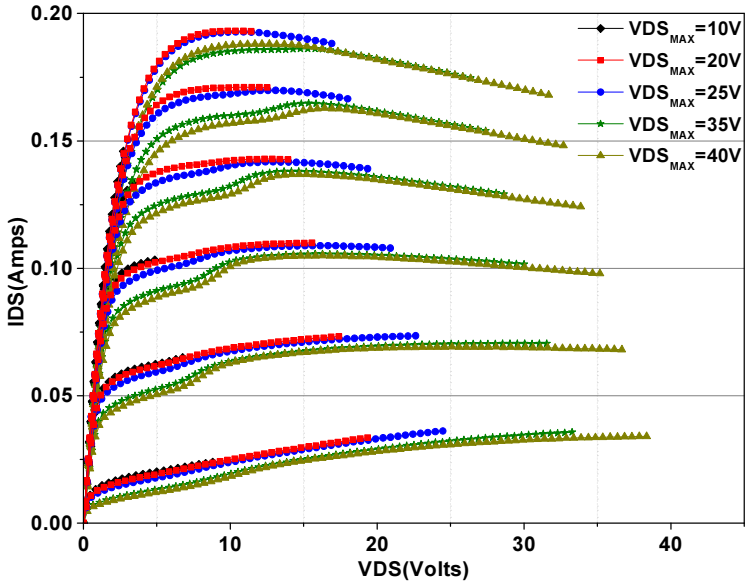

Fig II-13: Influence of the maximum drain voltage ($V_{DS\text{-}MAX}$) on kink effect in the case of a 2x75µm AlGaN/GaN HEMT with Lg = 0.15µm at a cold quiescent bias point.

Since this device is passivated and does not show any impact of illumination on kink, traps in barrier layer and due to surface states can be ruled out.

In the case of $V_{DS\text{-}MAX}$ > 20V in Fig. II-13, the kink effect appears. At a given *Vgs*, as V_{DS} is increased, traps are released by the field-assisted emission process and the current is progressively recovered. It should be noted that the amplitude of current collapse in kink region is much higher in the case of large drain current at positive gate voltages. This is due to a much easier generation of hot electrons during positive gate voltage V_{GS} with large drain current. These hot electrons have enough energy at lower bias value to get out of 2-DEG and are occupied in ionized donor like traps in buffer layer.

From the above discussion, we can conclude that the current collapse increases gradually with $V_{DS\text{-}MAX}$ in the pre-kink region associated to significant field assisted current recovery in post-kink region with $V_{DS\text{-}MAX}$. The trapped electrons demonstrate very large emission time before contributing again in conduction channel. As observed during this measurement process, this emission time constant is in the orders of several hundred minutes. That was the reason to wait for 6 hours between each set of pulsed I-V measurements.

All these measurements show that the most influential parameter on trap activation is the electric field induced by the highest drain voltage $V_{DS\text{-}MAX}$ reached during a pulse sequence, which leads to the drain current collapse.

II.5.3 Shift in pinch off voltage

In order to illustrate the positive shift in pinch-off voltage *Vp* observed in the kink region, Fig II-14 shows the measured transfer characteristics *Ids*(*Vgs*) of the 2x75µm AlGaN/GaN HEMT. During this measurement process, the gate-to-source voltage *Vgs* was swept from -5V to -1V at two constant drain-to-source voltages *Vds* of 5V and 30V. Two different curves were measured before kink and after kink at the respective voltages. The term "before kink" means that the device was swept without any stress voltage while the term "after kink" means that the device was tested after the stress voltage. The voltage values used as stress voltages were a gate-to-source voltage *Vgs* at *Vp* and a drain-to-source voltage *Vds* of 40V.

This positive shift in pinch-off voltage corresponds to the presence of trapped electrons in the buffer region. The shift of *Vp* is less important at *Vds* of 30V than at *Vds* of 5V due to the efficient de-trapping process at the higher bias voltage. This behavior also complements the observed impact of $V_{DS\text{-}MAX}$ on kink and de-trapping process at higher drain bias voltage, which was discussed in the previous section.

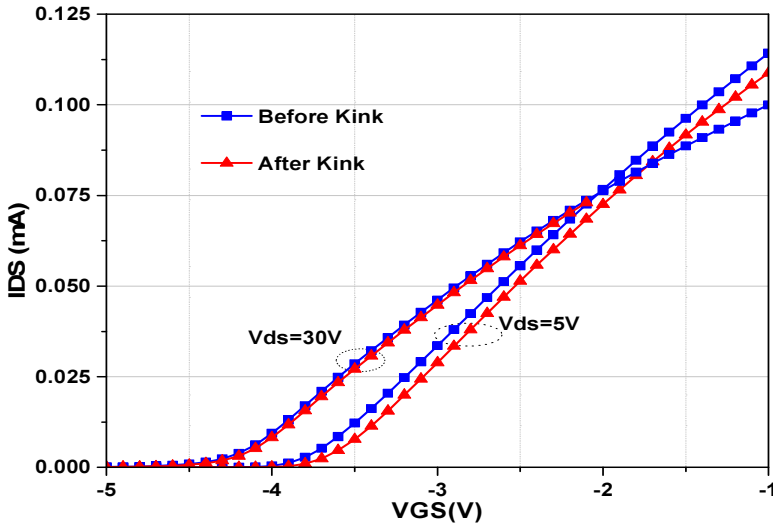

Fig II-14: Transfer characteristics of 2x75µm AlGaN/GaN HEMT at Vds of 5V and 30V before kink (no-stress) and after kink (stressing the device at Vds = 40V).

II.5.4 Impact of temperature

Kink effects in GaAs or InP HEMTs have been widely reported [66], [66], [66]. They are considered as sudden rise in the drain current at a certain V_{DS} voltage that results in high drain conductance G_D and transconductance g_m compression, leading to reduced voltage gain and linearity. In these devices, the kink effect is mainly caused by the impact ionization [67]. However, it is not the case in AlGaN/GaN HEMTs since impact ionization is difficult to observe due to their wide bandgap and low impact ionization rates.

To study the kink effect at different temperatures, the pulsed I-V characteristics were measured with a thermal chuck coupled to the pulsed setup to master the ambient temperature. The temperature is set by the thermal chuck since all pulsed I-V measurement of the kink effect were performed at a cold quiescent bias point to have no significant self-heating. In Fig. II-15(a), the measured I-V curves at different temperatures (-50 to 100ºC) clearly show the drain current collapse at low V_{DS} voltages and its subsequent recovery at higher V_{DS} voltages. The drain current collapse occurs at low V_{DS} values denoted as V_{DSKink}. This is induced by the high electric field of former instantaneous bias points at high drain voltages $V_{DS\text{-}max}$ that activate traps, which are subsequently filled at low V_{DS}, and lead to the decrease in drain current.

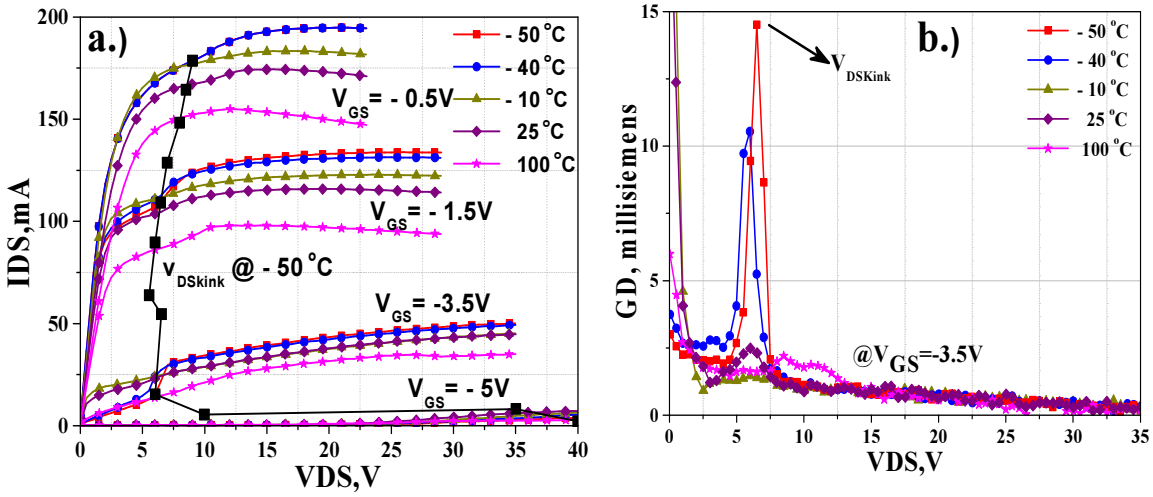

Fig II-15: Pulsed I–V curves at a cold quiescent bias point with temperatures set by the thermal chuck from −50 to 100°C: Drain current IDS (a) and output conductance GD (b).

The impact of temperature on kink effect can be visualized more clearly in Fig. II-15(b) where the output conductance G_D is plotted versus V_{DS} at a constant gate voltage V_{GS} of -3.5V. Indeed, the peak value of G_D occurs at V_{DSKink}. It can be observed that the kink effect is maximum at the lowest temperatures and tends to disappear with increasing temperature, as observed up to -10ºC. However, beyond this temperature of -10ºC, the kink reappears around room temperature and begins to disappear again at higher temperatures because of de-trapping due to thermal emission. From these measurements, we can conclude that the temperature dependence of kink effect is non-monotonic.

II.5.5 Impact of sweep directions of the drain voltage

This section illustrates the impact of directions (increase or decrease) of variation of the drain voltage V_{DS} on the de-trapping of electrons in the kink region. Fig II-16 shows a measured I-V characteristic of de-trapping process and kink effect at a constant gate voltage V_{GS} and different temperatures when the direction of the V_{DS} sweep is reversed. These measurement results also illustrate that trapping and de-trapping process are temperature dependent because the observed magnitude of the current collapse due to kink effect is quite different at each operating temperature.

The pulsed I-V measurements of Fig. II-16 were performed at a cold quiescent bias point while the temperature was successively set by the thermal chuck at -20°C, 10°C, 25°C, 40°C and 100°C. The pulse timing parameters were a gate pulse-width of 800ns and a drain pulse-width of 600ns with 10µs period. In Fig II-16, the instantaneous gate voltage V_{GSi} was kept at –2V for all temperatures. Before starting measurements at each temperature, the device was stressed for few seconds at a maximum drain voltage V_{DS} of 25V with a gate voltage V_{GS} at pinch-off value Vp.

Then, the measurement process starts by sweeping the drain voltage V_{DS} from 0V to 25V (direction left to right) and then from 25V to 0V (direction right to left). During the first sweep direction from 0V to 25V, all the ionized donor like traps are occupied by electrons due to the pre-stress voltage at 25V, and thus the current collapse occurs at lower bias voltages. However, this is no longer the case when the sweep direction is reversed from 25V to 0V. As the sweep starts from high V_{DS} value, it results in field assisted de-trapping process so that the kink effect is no longer visible in Fig. II-16 for the sweep direction from 25V to 0V.

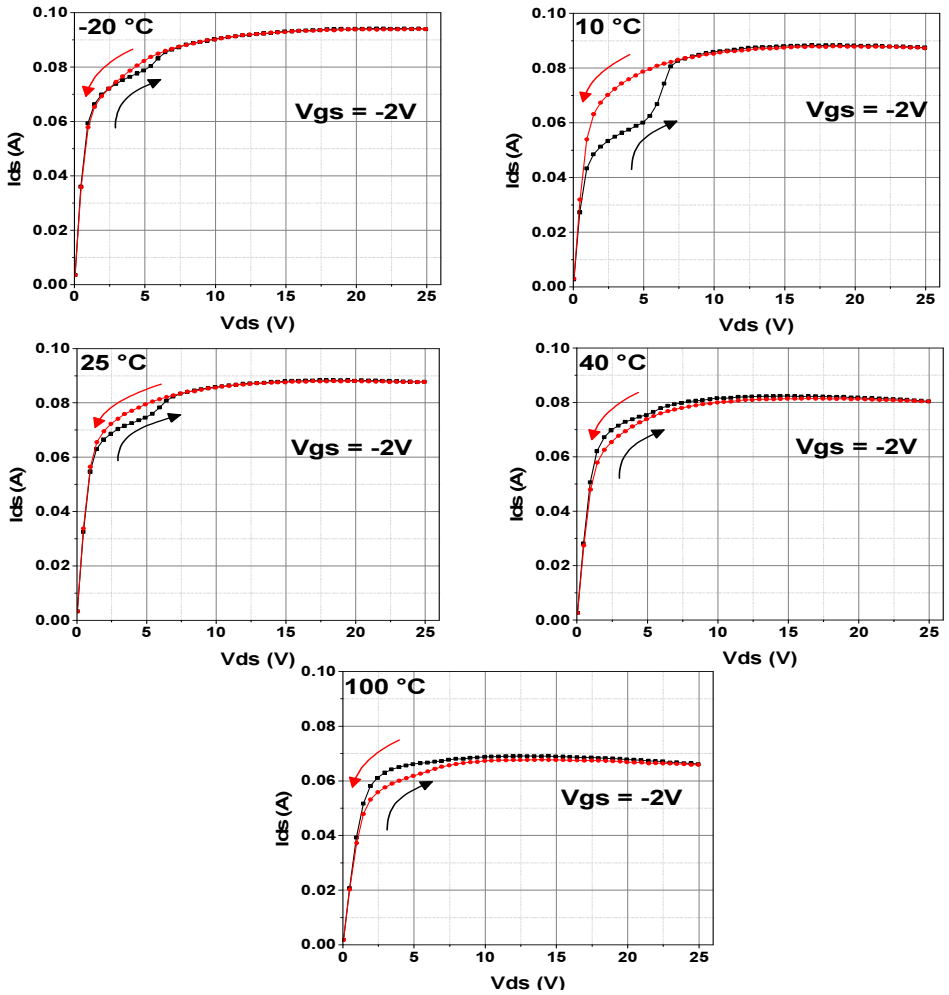

Fig II-16: Measured impact of the sweep direction of Vds on kink effect at different temperatures (-20°C → 100°C) for Vgs =-2V.

The important observation for the measurement is the temperature dependence on the current collapse magnitude in the kink region. As observed in Fig. II-16, the magnitude of current collapse is maximum at 10°C. At the highest temperatures of 40°C and 100°C, there is no visible kink effect but it still remains a difference between the two sweep directions of V_{DS}.

It is clear that the magnitude of current collapse observed in the first sweep direction is temperature-dependent but follows a non-monotonic dependency. Usually this phenomenon should be monotonic with temperature. This non-monotonic behavior observed at -20°C could be a measurement artifact due to the very small current collapse observed. In order to be sure, this should be confirmed by performing measurements at other relevant temperatures for example at -30 °C. It should be also noted that in the case of second sweep direction, the results in kink free characteristics are not temperature-dependent.

II.5.6 Electrical history measurements

In this section, two different measurement procedures are presented to characterize drain current collapse and drain lag in terms of magnitude, electrical history and recovery times. As previously reported [68] and illustrated, the drain current collapse at low V_{DS} values is only observed after a high drain voltage was applied. Moreover, the amount of current collapse depends on both the high drain voltage V_{DSmax} applied during former sweeps and the electrical history of the device. These phenomena are due to carrier trapping either in AlGaN barrier, GaN buffer or in both regions with short capture times and long emission times.

II.5.6.1 Current collapse

The pulsed I-V measurement setup presented in Chapter I (Fig. I-8) was used to perform these electrical history measurements. It associates the Keithley-4200 characterization system with a Pulse Monitoring Unit (PMU-4225) to allow as short as 70ns pulse widths with 10% duty cycle. To properly measure such a short pulse width, short cables and compensation techniques are required to reduce the transient effects. In this section, two different measurement procedures are presented to characterize drain current collapse and drain-lag in terms of magnitude, electrical history and recovery times.

In the first measurement procedure, the amount of current collapse and the drain current recovery times are characterized at room temperature both in DC and pulsed modes as shown in Fig. II-17 and Fig. II-18, respectively. The test procedure starts by a first I-V measurement run in which V_{DS} voltage is swept from 0 to $V_{DS\text{-}MAX}$. Subsequently, the same measurement is repeated after waiting different time intervals during which no voltages are applied, as shown in Fig. II-17(a) and Fig. II-18(a) in DC and pulsed modes, respectively. The selected time intervals under relaxed conditions vary from 0 to around 2 hours. In pulsed mode, the quiescent bias point is set to $V_{GSq} = V_{GSq} = 0$ V while in both modes the instantaneous gate bias voltage is constant at $V_{GSi} = -2.5$V. During the first run without electrical history, it is observed that no current collapse occurs at low V_{DS} but, as the V_{DS} value becomes higher, the high electric field activates trap centers. Therefore, in the subsequent sweeps, the current collapse is observed due to captured carriers in the trap centers activated by previous sweeps. The density of trap centers and their location depends on the electric field induced by $V_{DS\text{-}MAX}$ in former sweeps while the current recovery is obtained at $V_{DS\text{-}Kink}$.

From Fig. II-17(b) and Fig. II-18(b), it can be observed that the emission times are very high in the order of several minutes or even more. From these results, it is clear that captured carriers are released at different time constants.

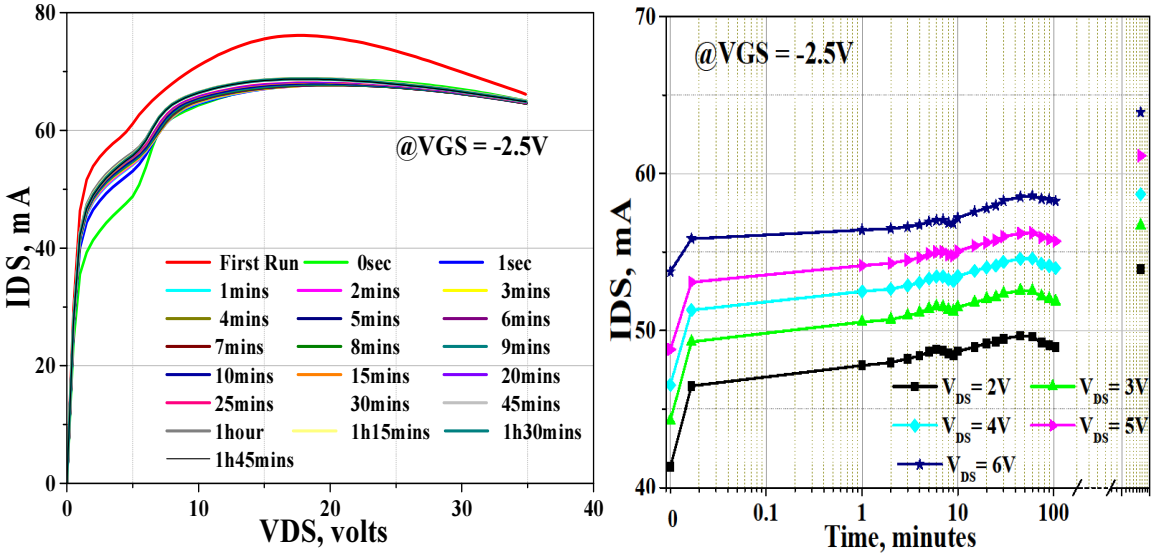

Fig II-17: DC I-V drain curves at V_{GS} = -2.5V at different time interval (a), and time delay to recover initial current value of first run (b)

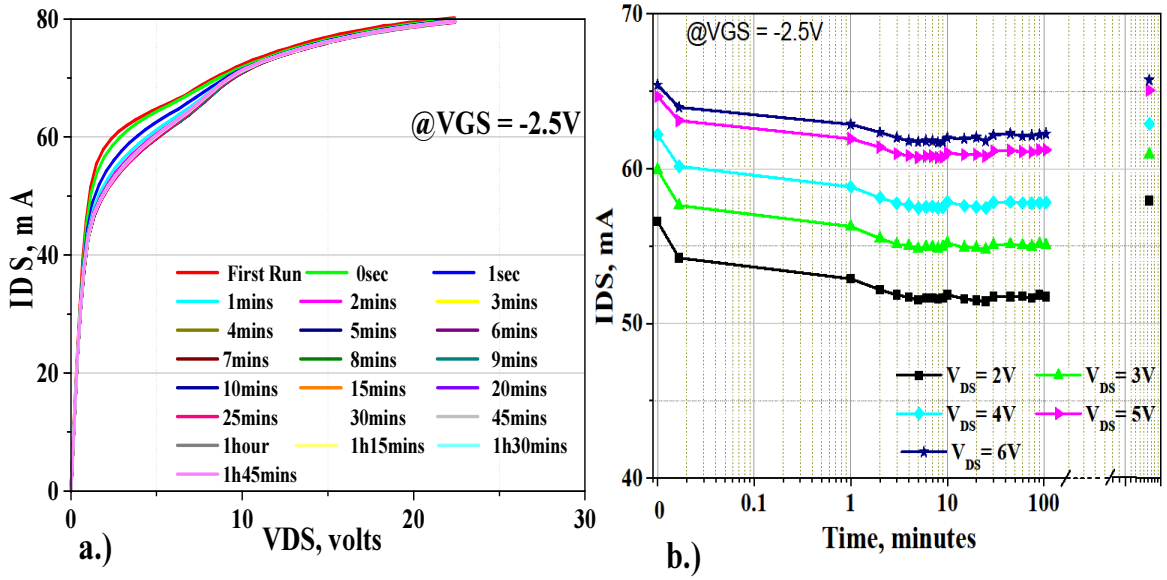

Fig II-18: Pulsed I-V drain curves at V_{GS} = -2.5V at different time interval (a), and time delay to recover initial current value of first run (b)

A significant difference is observed between measurements in DC and pulsed modes. In Fig. II-17(a) and Fig. II-17(b), the DC mode shows an immediate and maximum current collapse occurring right after the first run of the V_{DS} sweep, whereas the current collapse is lower in the subsequent delayed sweeps. This reflects that some of the traps are emptied during the different time intervals as shown by the slopes of Fig. II-17(b).

In Fig. II-18(a) and Fig. II-18(b), the pulsed mode shows a current collapse occurring and increasing gradually after the first measurement run of the V_{DS} sweep. This reflects that new carriers are captured at different time intervals according to the electrical history of the device as shown by the slopes of Fig. II-18(b).

These DC and pulsed I-V measurements demonstrate that, once activated, the kink effect can remain for several minutes, even without applied voltages. The observed differences between measurements in DC and pulsed modes can be explained by their different thermal conditions. In pulsed mode, the cold quiescent bias point at $V_{GSq} = V_{DSq} = 0$V associated with short pulse widths of 400ns and low duty cycle of 10% ensure that no self-heating effects exist, whereas it is not the case in DC mode.

II.5.6.2 Drain lag

In the second measurement procedure of this study on the impact of electrical history on trapping behavior, the impact of $V_{DS\text{-}MAX}$ on the amount of drain-lag and the recovery times of current within the pulses are characterized at room temperature in pulsed mode as shown in Fig. II-19. To this end, the bias point is set to a quiescent gate voltage V_{GSq} of −6V lower than V_P and four separate I-V measurements are performed at different quiescent drain voltages V_{DSq} varying from 0 to 30V in steps of 10V, whereas the same instantaneous bias point is used at a gate voltage V_{GSi} of −2.5V and a drain voltage V_{DSi} of 5V. As the quiescent point (V_{GSq}, V_{DSq}) is cold since V_{GSq} is lower than the pinch-off voltage V_P, there are no thermal effects in the case of short enough instantaneous pulses.

Fig. II-19 shows the time-domain I-V pulse response of a long pulse with 90ms pulse-width in order to illustrate the measured emission times within the pulse, which are in the orders of tens of milliseconds, even though a small thermal effect cannot be eliminated in this case of long pulses. However, the same behavior was observed in the case of very short pulses of 70ns, but without allowing to observe the emission times. One important conclusion of measurements

observed in Fig. II-19 is that the immediate decrease of drain current due to carriers captured in the first nanoseconds is roughly proportional to the level of the initial quiescent level V_{DSq} when it exceeds the instantaneous value V_{DSi}. This is due to the high electric field induced by V_{DSq} associated to the fast fall times of current. Such a short capture time in the orders of nanoseconds cannot be observed in the curve. However, the long pulse case presented in Fig. II-19 allows us to demonstrate that the recovery times of drain current within the pulse are in the orders of tens of milliseconds.

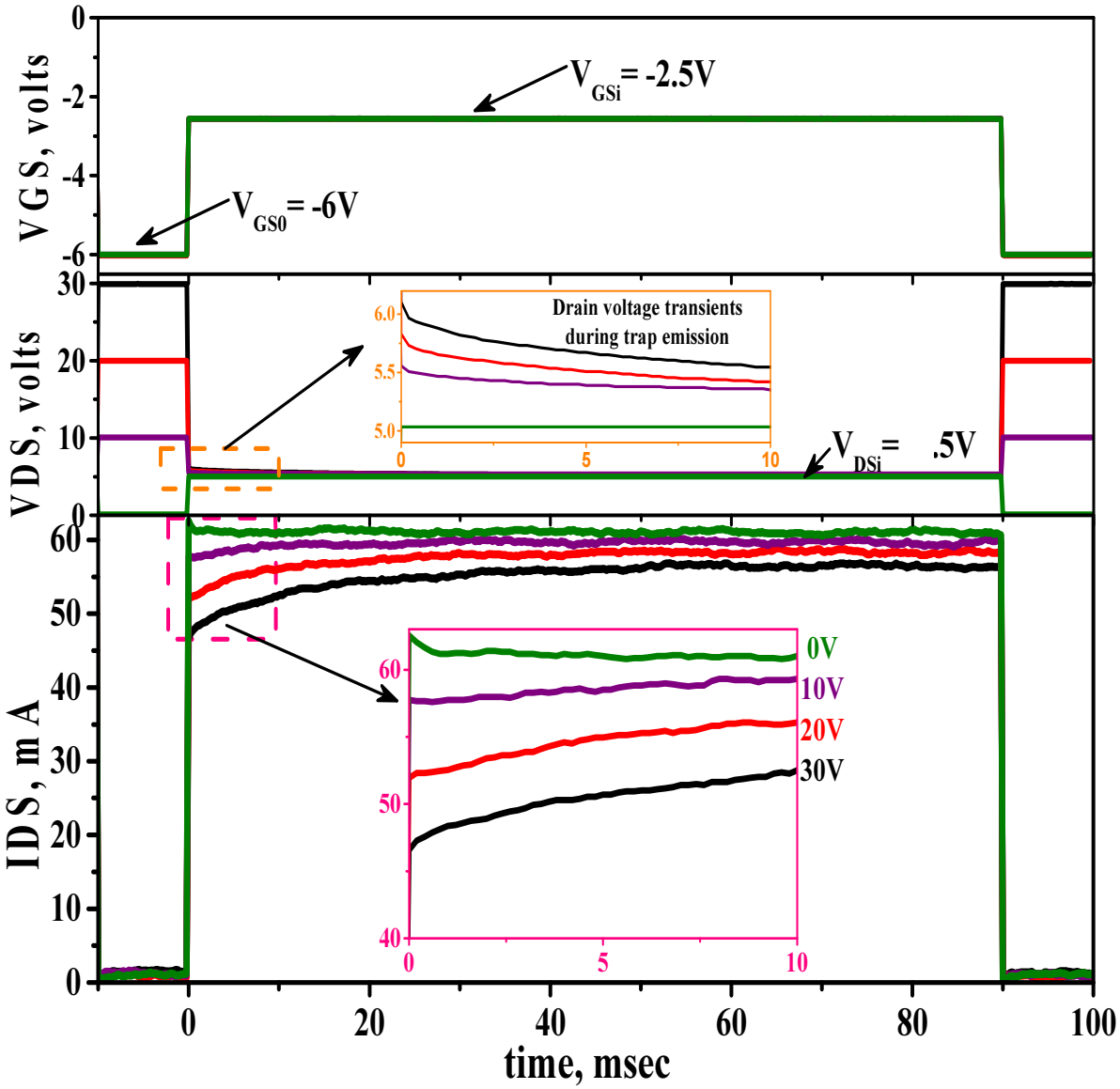

Fig II-19: Time-domain drain current affected by drain-lag at the same instantaneous bias point (V_{GSi}=-2.5V, V_{DSi}=5V) in the case of a cold quiescent bias point (V_P, $V_{DS\text{-}MAX}$) for an initial drain voltage $V_{DS\text{-}MAX}$ of 0, 10, 20 and 30V.

In this section, two specific measurement procedures were presented to quantify the impact of traps on *I-V* characteristics. Measurement results demonstrate that the electrical history induced by quiescent and instantaneous bias points, along with the resulting thermal effects, play a major role in current collapse and drain-lag, and thus on high-frequency electrical performances.

II.6 Pulsed RF measurements

II.6.1 Pulsed RF measurement setup

The pulsed I-V measurements presented in the previous sections illustrate the importance of measuring the transients of drain currents with respect to voltages, i.e. electric field and temperature. Such measurements also outlined the asymmetry of trap capture and emission phenomena through their very different scale of time constants. These effects need to be taken into account in high-frequency large signal operation when the device is excited with large RF voltages. For example, many high power devices are used in pulsed RF operation and also in applications where high peak-to-average-power-ratio are common. All dispersive effects such as trapping and thermal effects, and thus the resulting shift in device characteristics presented in the previous section have to be considered in CAD tools. So, to check the model validity under large signal conditions, these simulations have to be compared with measurements. This section presents the pulsed RF load-pull setup and some pulsed measurement results for varying pulse characteristics.

The pulsed RF load-pull setup based on SWAP X402 is shown in Fig II-20. It is a sampler-based nonlinear vector network analyzer (NVNA) developed by VTD [69] which consists of four independent and synchronized RF sampler-based receivers that convert RF signals into intermediate frequency. The stable clock, which is driving the four samplers, is generated by a stable local oscillator (LO). The LO is phase-locked to a stable reference that is shared with the RF source and with the analog to digital converter (ADC) clock. Using one shot measurements, all the wave data are acquired coherently by the receiver at the fundamental and harmonics frequencies. Thus, the time-domain current and voltage waveforms versus time as well as the load line cycles can be determined at the reference planes using robust algorithms.

Power performances in pulsed RF mode such as the output power, input power, gain and power added efficiency are characterized.

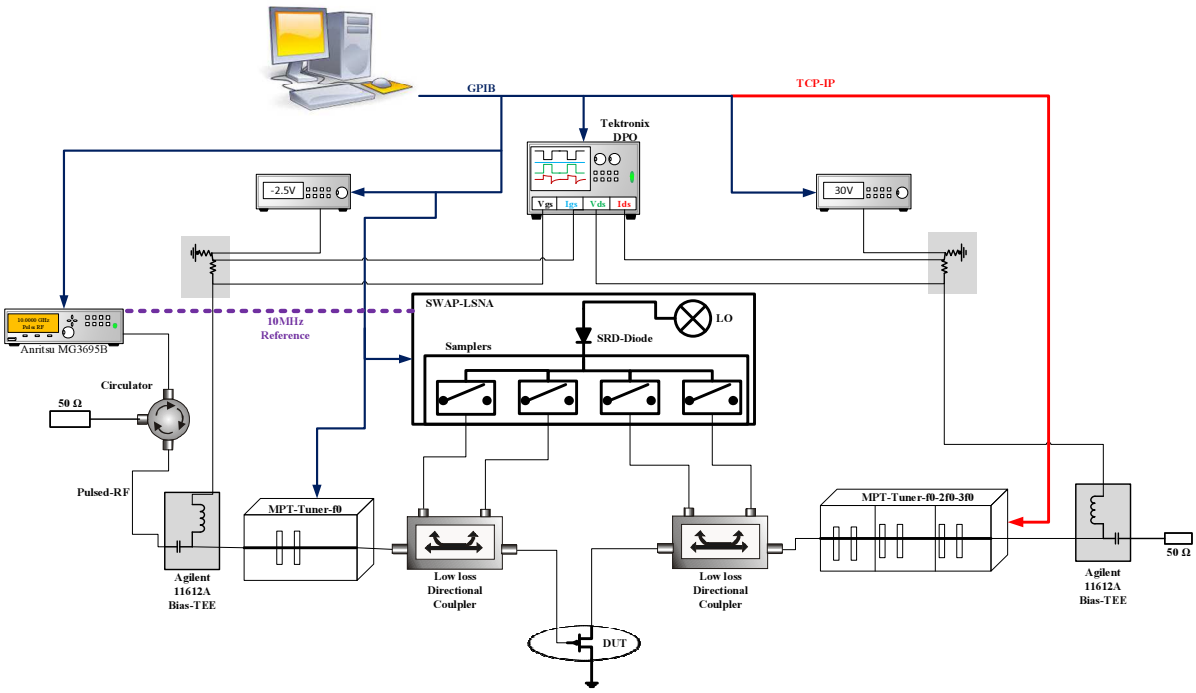

Fig II-20: Pulsed RF load-pull measurement setup using nonlinear vector network analyzer.

The pulsed RF signal is delivered by a pulsed RF signal generator Anritsu MG3695B. The transients on gate and drain currents are captured by the Tektronix Digital Phosphor Oscilloscope (DPO) shown in Fig II.20. The current and voltage probes of the instrument are used to capture the current and voltage transients in pulsed RF conditions during RF_{ON} and RF_{OFF} states. The multi-purpose tuners (MPT) from the company "FOCUS microwave" are used for source- and load-pull impedance matching. The source tuner is operates at fundamental while the load tuner is capable for matching up to three harmonics.

II.6.2 Impact of pulsed RF on drain current

In this section, we present pulsed RF measurements for different timing parameters of RF pulses at varying RF powers and bias conditions. In these examples of measurement results, the device is excited with fundamental pulsed RF signal and the source tuner is kept at 50 Ω whereas the load impedance is only matched at fundamental without tuning at second and third harmonics. Fig II-21 illustrates these measurement results of the 2x75µm AlGaN/GaN HEMT

with the *Ids* current transients captured by the DPO oscilloscope. The control over pulse parameters, RF power and bias voltages are captured and controlled through the GPIB interface with the SWAP X402 system software.

Impact of the RF pulse width on drain current transients:

Fig II.21 (a) and (b) illustrates the impact of the RF pulse width *PW* on the trap capture and emission phenomena [70]. During these measurements, the transistor was biased at -3V of gate voltage and 30V of drain voltage. The pulse repetition period *PRP* was kept constant at 250 µs and the RF pulse width *PW* was successively set to 5µs, 10µs, 20µs, 35µs, 50µs, and thus the duty cycle varied from 2% to 20%. The resulting transients of drain current captured at each pulse width are superimposed on the same time axis in Fig II.21 (a) and (b). In Fig II.21 (a), all pulses are superimposed on the same time axis and aligned with the rising edge of pulses whereas the time axis of Fig II.21 (b) is aligned with the falling edges of RF pulses. Whatever the value of the pulse width *PW*, Fig II.21 (a) demonstrates that the magnitude of current collapse observed at the end of RF pulses remains unchanged. This measurement results suggest that the same density of traps are occupied whatever the pulse width. Moreover, it can be observed that the capture behavior is very fast with an associated capture time constant that could be in the orders of picoseconds to nanoseconds. Moreover, whatever the pulse width *PW*, the pulse repetition period *PRP* of is high enough to observe the complete recovery of the drain current level with respect to the emission time constant. Fig II.21 (b) demonstrates that the recovery time does not depend on the RF pulse width.

Impact of the pulse repetition period on drain current transients:

Fig II.21 (c) illustrates the impact of the pulse repetition period on the current recovery time with respect to the emission time constant of traps. In this measurement, the transistor was biased at -3.5 V of gate voltage and 30 V of drain voltage. The pulse width *PW* of the RF signal was fixed at 20µs while the pulse repetition period *PRP* was varied from 50µs to 250µs in steps of 50µs. It can be observed that the pulse repetition period of 50µs and 100µs are not long enough to complete the current recovery with respect to the emission time constant. This problem can be outlined at the very beginning of the current curve in Fig II.21 (c) where only the highest *PRP* values of 200µs and 250µs allow the current to recover the same value of 27mA whatever *PRP,* whereas the lowest *PRP* values

of 50µs and 100µs does not allow the complete current recovery and demonstrate lower and different values of recovered current. Such a measurement is very important to quantify the emission time constant. Therefore, it can be observed that the amplitude of current collapse increases with increasing pulse repetition period until the pulse period reaches the required value to allow the complete current recovery.

Impact of the RF power on drain current transients:

Fig II.21 (d) illustrates the impact of the RF power level on capture and emission times, which in turn affect the gain of GaN HEMT at medium or high RF powers [7]. In these measurements, the transistor was biased at -3.5 V of gate voltage and 30 V of drain voltage. The pulse width *PW* of the RF signal was fixed at 75µs while the pulse repetition period *PRP* was set to 250µs. The RF power was varied from medium to large signal operation corresponding to 5dBm and 10dBm input powers, respectively. In Fig II.21 (d), both power levels demonstrate a decrease of the drain current during the RF pulse. This effect can be also observed when the drain current value is plotted against the RF power [7]. Indeed, as long as the RF power is low, there is no change in the drain current but as the RF power reaches a given moderate power, a decrease of the drain current is observed. As also illustrated in Fig II.21 (d), the recovery time of the drain current through the trap emission process can be observed when the RF pulse is finished.

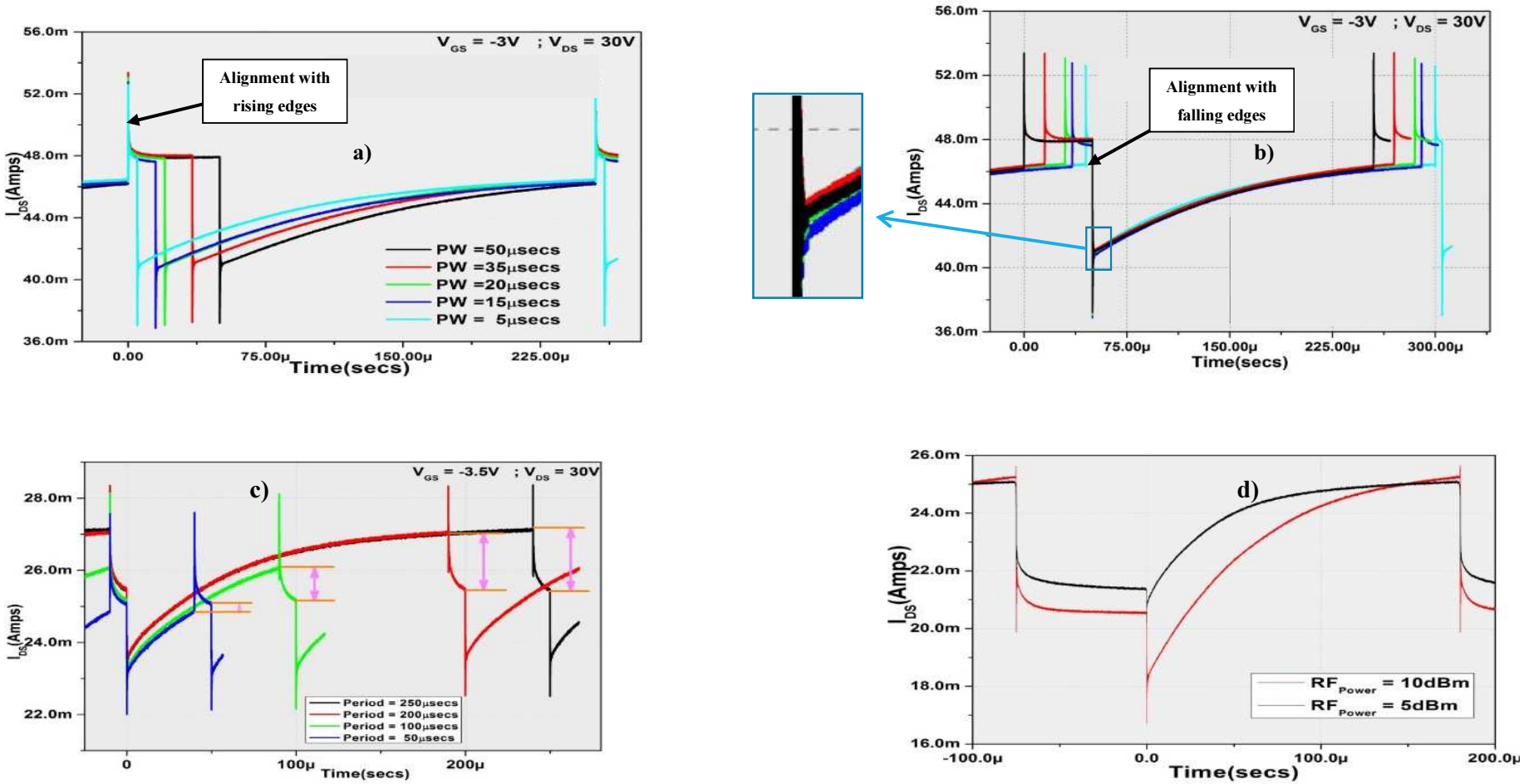

Fig II-21: Pulsed RF measurements of drain current: a) and b) variable pulse width PW of (5µs, 10µs, 20µs, 35µs, 50µs) with 250µs of pulse period, c) variable pulse periods PRP of (50µs, 100µs, 200µs, 250µs) with 20µs of pulse width, d) variable input RF power (5dBm, 10dBm).

II.7 Conclusions

In this chapter, to illustrate the advantages of GaN-based semiconductors over its predecessors, we have presented the physical properties induced by the wurtzite lattice of GaN and group-III-nitride crystals which exhibit high levels of spontaneous and piezoelectric polarizations. Indeed, the unique feature of AlGaN/GaN HEMTs is characterized by the channel formation which is called a 2-Dimensional Electron Gas (2DEG) induced by the specific polarization properties of the heterostructure.

Then, we have presented a brief synthesis of the nonlinear modeling flow of AlGaN/GaN HEMTs with a particular emphasis on the specific nonlinear circuit modeling techniques that have been developed at XLIM lab. These modeling techniques are mainly based on specific DC and pulsed I-V measurements as well as RF measurements. Such a nonlinear modeling flow includes the equations of nonlinear circuit elements and the nonlinear electro-thermal and trapping models developed at XLIM.

The final part of this chapter was devoted to an innovative pulsed characterization technique we have performed on a 2x75µm AlGaN/GaN HEMT with 0.15µm gate length fabricated at III-V Lab. These innovative characterizations aimed to study the dynamics of trapping effects in AlGaN/GaN HEMTs using specific pulsed I-V and pulsed RF characterizations. The current collapse (kink effect) and the impact of drain lag emission/capture time constants were experimentally characterized with respect to the electrical history of the device. It was demonstrated that the electrical history of the device induced by the quiescent and instantaneous bias points, along with the thermal effects, play a major role in the phenomena of current collapse and drain-lag. The pulsed measurement setup and the proposed characterization procedure present an efficient way to identify and quantify trapping dynamics in AlGaN/GaN HEMTs that have a great impact on power performances when the device operates with modulated signals and especially under pulsed mode as it is the case for radar applications.

These characterization results can be used to develop and improve a dedicated nonlinear model of GaN HEMTs integrating the dynamics of trapping effects and their effect on high-frequency electrical performances.

III. DC and High-Frequency Characterization and Modeling of Graphene FET

III.1 Introduction

The "Moore's Law" [49] was stated in 60's by Gordon Moore, the head of Intel corporation at that time. It was an empirical observation of the components that can be built on an integrated circuit and their cost, which means that the computing power doubles every 18 months. Intel made the first CPU with 2300 transistors and a clock speed of 0.7 MHz comparing with today's average CPU that contain few billion transistors and reach clock speeds over 4GHz, which is achieved by scaling down of device dimensions. Eventually, there is a limit to this aggressive scaling down of devices (More Moore) [71] due to the limitations set by the laws of thermodynamics and quantum mechanics which give how much computing power one can produce with silicon. This is due to the two main problems 'heat' and 'leakage current' that's why silicon-era will eventually come to an end. This is the motivation to explore for the non-silicon based materials.

In addition, new technologies like graphene (Beyond CMOS) [71] has emerged as a new discovery and it is given much attention by researchers because of its unique structural, electrical and mechanical properties [72]. According to 2013 International Technology Roadmap for Semiconductors (ITRS) [73] in emerging research materials, graphene transistors might have an opportunity to replace Silicon only after 2021. At the moment, all the research efforts are put towards graphene preparation that can be qualified as a high yield method. Recent progress on graphene synthesis [74], [75] led to the availability of graphene samples for the broad examination of electronic properties [76].

Graphene is a single layer of two dimensional carbon atoms arranged in a regular hexagonal pattern. Prior to its demonstrated existence by *Geim et.al* in 2004 [38], physicists strictly believed that the two dimensional atomic-crystals were unstable and cannot exist in free state. Graphene ever since has attracted tremendous attention and research interests due to its exceptional physical properties such as high electron mobility, thermal conductivity and excellent mechanical strength. Graphene also exhibits strong ambipolar electric field effect and quantum hall effect. In addition, graphene is highly transparent [77] with 2.3% absorption of visible light and thermal conductivity measured [78] at room temperature is higher than 3000 $W(m.K)^{-1}$ for single layer of graphene. Graphene also possess excellent mechanical strength [79]. Measurements have shown that graphene has breaking strength (1.0 T Pa) of over 100 times greater than the steel film of the same thickness indicating one of the strongest material

ever measured. In Table III-1, the graphene electrical properties are compared to other conventional semiconducting materials and Fig III-1 shows the properties and an overview of graphene applications.

Characteristics	Silicon	AlGaAs/ InGaAs	InAlAs/ InGaAs	InSb	Copper	Graphene
Electron mobility at 300K ($cm^2/V·s$)	1500	8500	5400	80000	300-400	**> 100000**
Peak electron velocity ($\times 10^7$ cm/s)	1.0 (1.0)	1.3 (2.1)	1.0 (2.3)	5-7	1	**7-10**
Thermal conductivity (W/cm·K)	1.5	0.5	0.7	0.15	3.5	**48.4-53**

Table III-1: Graphene properties compared to other materials.

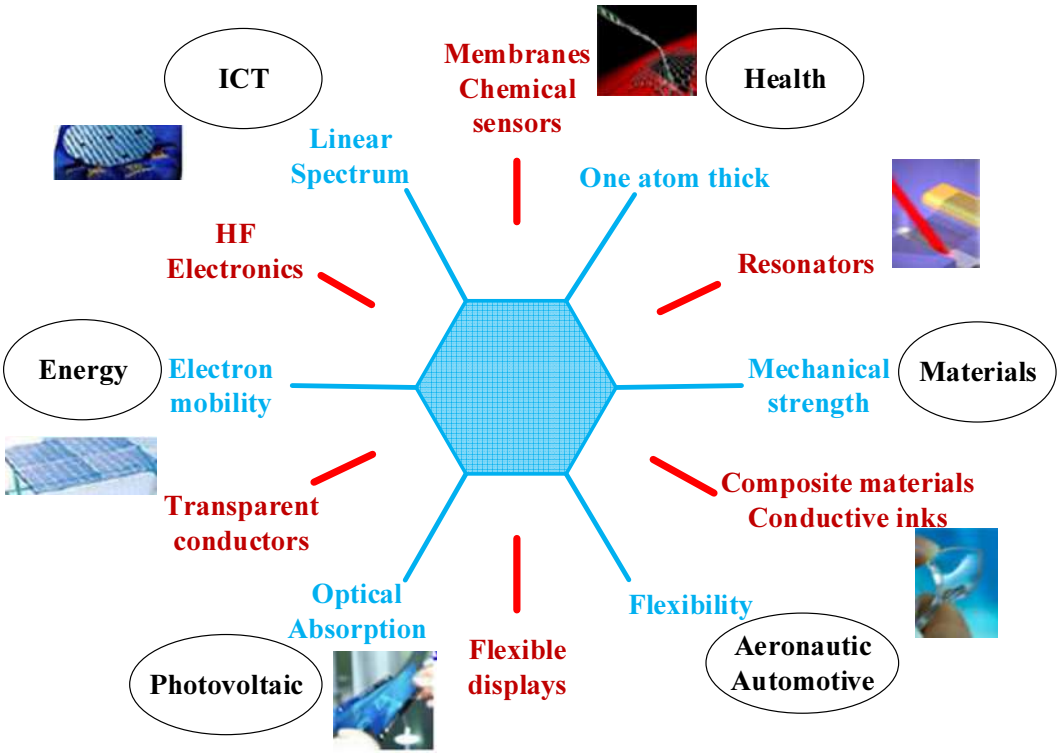

Fig III-1: Graphene properties and overview of applications [80].

Graphene is a zero-bandgap semiconductor, or semimetal. The zero-bandgap means that graphene cannot be switched from conductive state to non-conductive state. The zero-bandgap is the major obstacle for the synthesis of graphene transistors. Thus opening a bandgap without compromising other properties, is one of the active research areas in graphene. But, the target is to explore the performance of graphene transistors in both logic and RF applications. However, the zero band gap of large area graphene is not an issue in all applications. Most recently researchers in Switzerland [81] showed new 2D material $MoSe_2$ material superior to Silicon and Graphene based digital logic. At the moment, graphene needs to compete against the more mature technologies such as III-V semiconductors. According to "A roadmap for graphene" [82] forecasts, III-V compound semiconductors will no longer be able to obtain the required cutoff frequency f_t of 850GHz and maximum oscillation frequency f_{max} of 1.2THz. Researchers at IBM already reported [83] graphene based RF transistors with f_t of 300GHz and the reported [84] f_{max} is around 44GHz. The goal for graphene transistors is to obtain f_t of 850GHz and f_{max} of 1.2 THz by 2021 according to graphene flagship in the WorkPackage4 (WP4) of "High-frequency electronics". There is a possibility to extend the f_t until 1THz but the f_{max} is still at a low value which can be improved by obtaining current-saturation in graphene transistor and by improving semiconductor process to reduce gate resistance.

The aim of this thesis is to assess the RF behavior and potential of graphene-based transistors. This chapter will report DC and RF measurements performed on graphene FETs and the electrical modeling approach developed in this work. Three types of graphene FETs were studied, all of which were fabricated by the IEMN laboratory, Lille, France. The first two types of graphene FET were fabricated with SiC evaporation and the second with Chemical Vapour Deposition (CVD). This chapter is divided into four sections. First, graphene physics and electrical properties were detailed and followed by brief discussion on graphene synthesis. Then the measurement results on DC behavior of three different technologies of graphene FETs will be presented. Finally, the de-embedding methods and the RF measurements on GNR-FET are presented, leading to development of HF-model. The validity of the HF-model is checked by comparing measurements with simulations.

III.2 Graphene physics

Electronic configuration of an isolated carbon atom which has four valence electrons in the outer s-p shell arranged in their lowest energies, two electrons in 2s orbital and the remaining two electrons are occupied each in $2p_x$ and $2p_y$ leaving $2p_z$ orbital empty (Fig III-2(a)). When carbon atoms come close to form a crystal, one of the 2s electron is excited to $2p_z$ orbital from the energy gained from the neighboring nuclei (Fig III-2(b)), this in turn has an effect in lowering the overall net energy of the system. This is followed by subsequent bonding's between the 2s and 2p orbitals shown in Fig III-2(c). The mixing of different atomic orbitals is called hybridization, and the new orbitals formed are called hybrid orbitals as shown in Fig III-2.

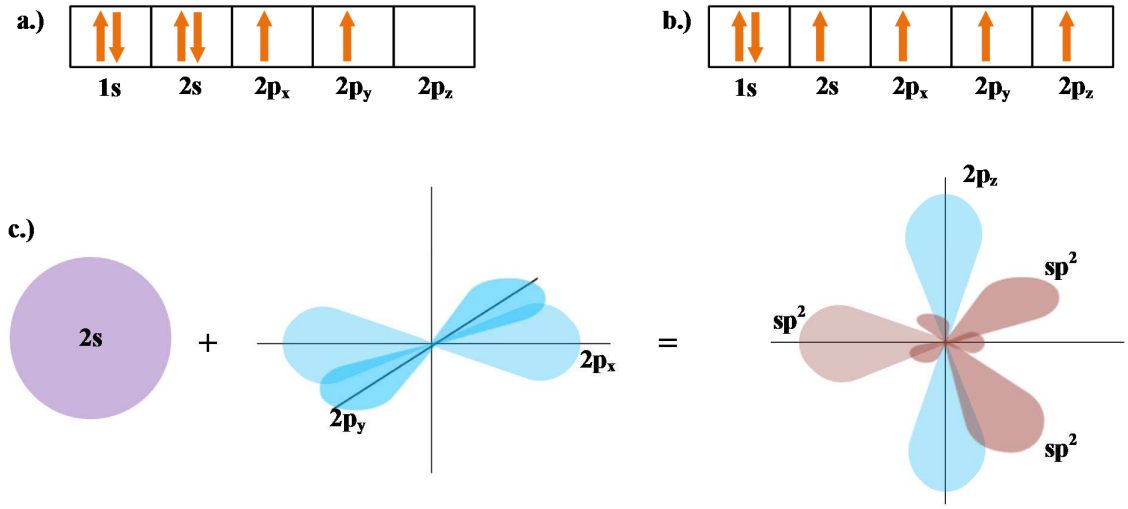

Fig III-2: Electronic configuration and their relative spin (a) element carbon (b) Graphene, the 2s and two electrons of 2p orbitals interact covalently to form three sp^2 hybrid orbitals (c) sp^2 orbital illustration [85].

The way in which these hybridization found their stable structures with suitable atomic bonding properties leads to the carbon allotropes shown in the Table III-2.Graphene is the basis of all other carbon allotropes. As illustrated in Fig III-3, wrapping the graphene into a sphere produces Fullerene [86], folding graphene into a cylindrical structure produces a carbon nano tube [87] and last by arranging planar graphene sheets on top of one another produces graphite. Besides, by cutting the graphene into ribbons gives us the graphene nano ribbons used in GNR-FETs.

As illustrated in Fig III-2(c), the 2s orbital interacts with only two of the three available 2p orbitals resulting in three sp2 hybrid orbitals leaving one uninvolved $2p_z$ orbital. The three sp^2 interactions results in three sigma (σ)-bonds, which are the strongest type of covalent bond. The remaining $2p_z$ orbital forms pi (Π)-bond, where the electron cloud is distributed normal to the plane connecting carbon atoms. The $2p_z$ electrons are weakly bonded to the nuclei making them relatively delocalized. These delocalized electrons determines the conduction properties of graphene.

Allotrope	**Structure**	**Hybridization**	**Electronic properties**
C60 Fullerene	Spherical	sp^2	Semiconductor
Carbon nano tube	Cylindrical	sp^2	Metal or Semiconductor
Graphene	Planar	sp^2	Semi Metal

Table III-2: Allotropes of Carbon [85].

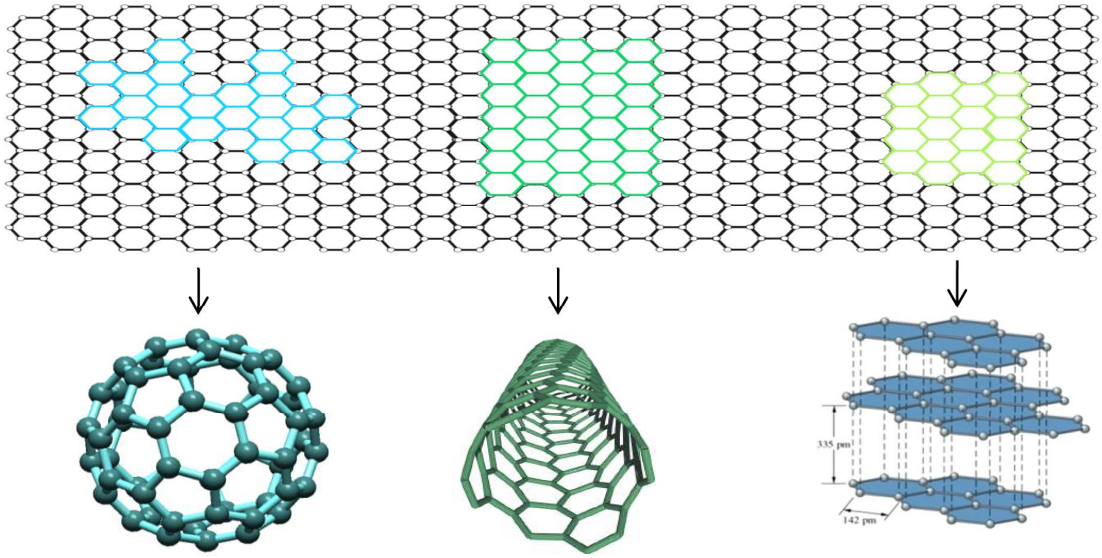

Fig III-3: Carbon allotropes a.) Fullerene b.) Carbon nano tube c.) Graphite [85].

III.2.1 The graphene lattice

Graphene is a two-dimensional material with a honeycomb lattice as illustrated in Fig III-4. Due to the two dimensional nature of graphene, only two primitive unit vectors a_1 and a_2 are required to construct the entire lattice and these vectors are given in Equation III-1. The carbon-carbon length is $a_{c\text{-}c} \sim 1.42$ Å and lattice constant is $a = \sqrt{3}a_{C-C} = 2.46$ Å. The graphene Bravais lattice has a basis of two atoms, indicated as A and B, is shown in Fig III-4. These atoms contribute with a total of two Π-electrons per unit cell to the electronic properties of graphene.

The basis vectors $\overrightarrow{a_1}$ and $\overrightarrow{a_2}$ of the graphene lattice are:

$$\overrightarrow{a_1} = \left(\frac{\sqrt{3}a}{2}, \frac{a}{2}\right), \qquad \overrightarrow{a_2} = \left(\frac{\sqrt{3}a}{2}, -\frac{a}{2}\right) \tag{III-1}$$

With $|\overrightarrow{a_1}| = |\overrightarrow{a_2}| = a$. The nearest neighbor vectors describing the type A atom bonded to its three nearest neighbors are given in Equation III-2.

$$\overrightarrow{R_1} = \left(\frac{a}{\sqrt{3}}, 0\right), \qquad \overrightarrow{R_2} = -a_2 + \overrightarrow{R_1} = \left(-\frac{a}{2\sqrt{3}}, -\frac{a}{2}\right),$$
$$\overrightarrow{R_3} = -a_1 + \overrightarrow{R_1} = \left(-\frac{a}{2\sqrt{3}}, \frac{a}{2}\right), \tag{III-2}$$

With $|\overrightarrow{R_1}| = |\overrightarrow{R_2}| = |\overrightarrow{R_3}| = a_{C-C}$

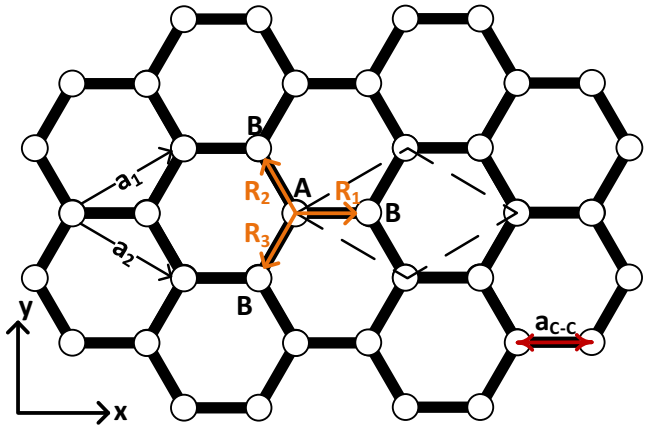

Fig III-4: The lattice structure of graphene is a honeycomb lattice [85].

The Fourier transform of the spatial wave function of the direct lattice results in the reciprocal lattice of graphene shown in Fig III-5 and the reciprocal lattice is again an hexagonal lattice. The reciprocal lattice vectors are given in Equation III-3.

$$\overrightarrow{b_1} = \left(\frac{2\pi}{\sqrt{3}a}, \frac{2\pi}{a}\right), \qquad \overrightarrow{b_2} = \left(\frac{2\pi}{\sqrt{3}a}, -\frac{2\pi}{a}\right), \tag{III-3}$$

with $\left|\overrightarrow{b_1}\right| = \left|\overrightarrow{b_2}\right| = 4\pi/\sqrt{3}a$. The Brillouin zone is a primitive unit cell of the reciprocal lattice shown as shaded region in Fig III-5 with sides of length $b_{BZ} = \left|\overrightarrow{b_1}\right|/\sqrt{3} = 4\pi/3a$ and area equal to $8\pi^2/\sqrt{3}a^2$.

There are three key locations of high symmetry in Brillouin zone when discussing the dispersion of graphene. In Fig III-5, these locations are identified by convention as the Γ-point, the M-point, and the K-point. The Γ-point is at the center of the Brillouin zone, and the vectors describing the location of the other points with respect to the zone center Γ are given by:

$$\overrightarrow{\Gamma \mathrm{M}} = \left(\frac{2\pi}{\sqrt{3}a}, 0\right), \qquad \overrightarrow{\Gamma \mathrm{K}} = \left(\frac{2\pi}{\sqrt{3}a}, \frac{2\pi}{3a}\right), \tag{III-4}$$

with $\left|\overrightarrow{\Gamma M}\right| = 2\pi/\sqrt{3}a$, $\left|\overrightarrow{\Gamma K}\right| = 4\pi/3a$, $\left|\overrightarrow{MK}\right| = 2\pi/3a$.

There are six K-points and six M-points within the Brillouin zone. The Brillouin zones are used to describe and analyze the electron energy in the energy band structure of crystals. The unique solution for the energy bands of crystalline solids are found within the Brillouin zone and the dispersion is plotted along the high symmetry directions.

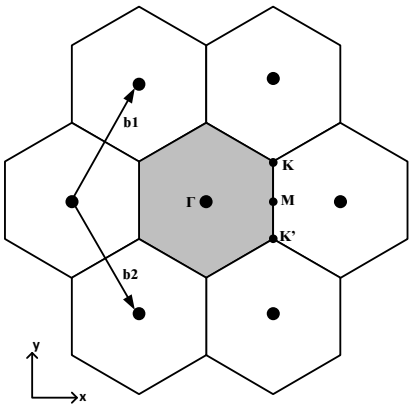

Fig III-5: The reciprocal lattice and possible choice for the first Brillouin zone with the high symmetry points labeled as Γ, M, and K located at the center, midpoint of the side, and the corner of hexagon respectively [85].

III.2.2 Graphene electronic band structure

The 3D plot of the ab-initio energy dispersion of graphene is shown in Fig III-6. Throughout the Brillouin zone the conduction and valence bands of graphene touch at four points which are known as "Dirac Points". This will give rise to zero energy bandgap at the Fermi energy. Indeed, the upper half of the energy dispersion plot in Fig III-6 is the conduction band and the lower half is the valence band. Due to the zero energy bandgap, graphene is considered as semi-metal or zero-bandgap semiconductor, in contrast to a regular metal, where E_F is typically inside the conduction band, and also in contrast to a semiconductor where E_F is located in the finite energy bandgap.

The zero bandgap results in linear energy-momentum dispersion relation, which means that an electron has a zero effective mass (massless Dirac fermions) at these Dirac points and behaves more like a photon than a conventional massive particle whose energy-momentum dispersion is parabolic. This has a direct result that the charge carriers obey the Dirac equation. Under applied electric or magnetic fields or presence of impurity atoms, the Fermi energy will be shifted from its equilibrium value of 0 eV. The deviation of E_F from its equilibrium value is often used in determining the strength of the field or concentration of impurity atoms (doping profile) of graphene.

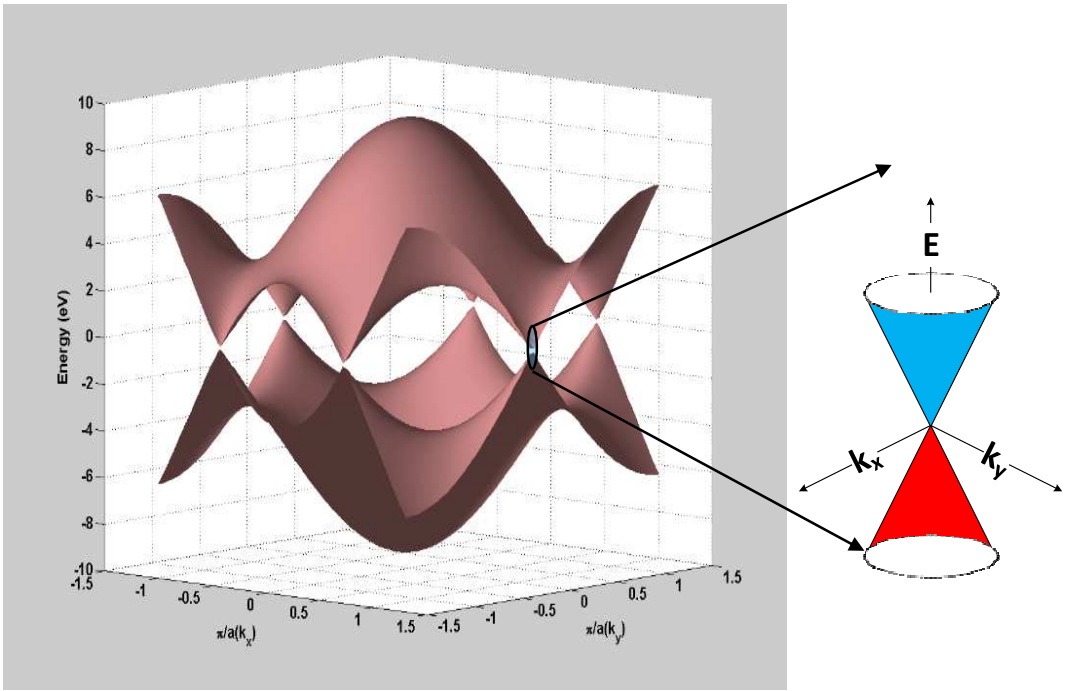

Fig III-6: The ab-initio band structure of graphene [85].

III.3 Graphene synthesis

In this part, we will present briefly the different graphene synthesis techniques. The preparation of graphene is divided into two methods illustrated in Fig III-7 namely, top-down approach (from graphite) and bottom-up approach (from carbon precursors).

In top-down approach, there are two synthesis types: First and foremost the most famous synthesis type is micromechanical exfoliation of graphite ("Scotch Tape" or peel-off Method) for which Novoselov and Geim [38] won noble prize in 2010 for their ground breaking experiments on graphene. The second synthesis type is the creation of colloidal suspensions from graphite oxide or Graphite Intercalation Compounds (GICs) [88] [89].

In bottom-up approach there are three synthesis types; First type is Chemical Vapour Deposition (CVD) of hydrocarbon [90], second type is epitaxial growth on electrically insulating surfaces such as Silicon Carbide (SiC) [91] and, third type is total organic synthesis [92].

In next sections the micromechanical exfoliation, CVD and epitaxial methods will be presented.

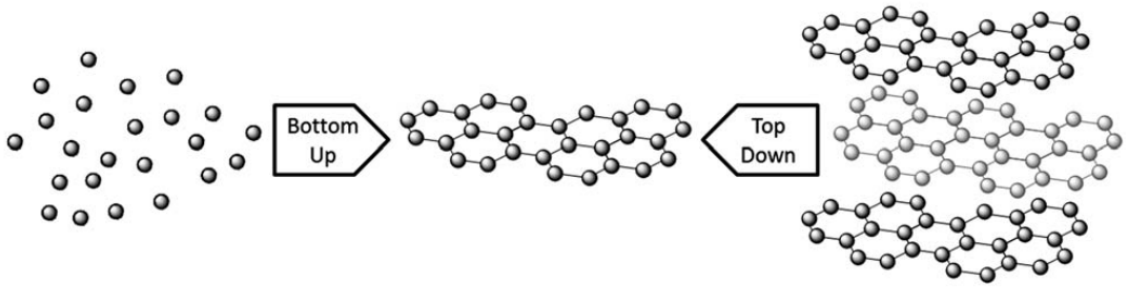

Fig III-7: A schematic of 'bottom-up' and 'top-down' graphene synthesis [93].

III.3.1 Micromechanical exfoliated graphene

"Micromechanical exfoliation" or the so called "Scotch Tape" method is probably the straightforward and well-known technique to produce graphene. A piece of bulk graphite is repeatedly peeled off using adhesive tape to detach layers of graphene. Then, the remained multiple layers of graphene on the tape are transferred on desired substrates. For example, the first report of isolating graphene onto insulating SiO_2 substrate was made by Geim et.al. in

2004 [38]. The transferred graphene layers differs in size and thickness. The invisible graphene flakes become visible on SiO_2 substrate [94]. Raman spectroscopy or Atomic Force Microscopy (AFM) can also be used to find out if the graphene flakes are single, few- or multilayers. This method has huge disadvantages in terms of controllability and moreover, the finding of graphene on the substrate is labor intensive. The only advantage of this method is to produce highly pure graphene with almost no defects. However, this method is not easily scalable to industrial and commercial levels.

III.3.2 Graphene by Chemical Vapour Deposition (CVD)

Chemical Vapour Deposition is one of the most promising techniques [95] to grow thin films of graphene on substrate by decomposing gaseous compounds. Graphene has been grown with CVD on metal substrates, such as nickel (Ni) and copper (Cu). First the Ni sample is heated with a filament or plasma. Later the Ni is exposed to a gas mixture of H_2, CH_4, and Ar at a high temperature of ~1000 °C. Then, the methane decomposes onto Ni, and hydrogen evaporates, and finally, the carbon diffuses into Ni. After the Ni is cooled down in Ar atmosphere, graphene layers are grown on the surface. The obtained graphene layers are then transferred to a substrate using polymer support. The advantages of this technique is the control of shape and number of graphene layers. Hence, the number of layers is controlled by Ni thickness and the shape is obtained by the patterning of the Ni layer. The disadvantage of CVD technique is the graphene layers transfer to a substrate, which is somewhat difficult and may degrade the quality of the layer and may lead to folding of the layer. However, CVD synthetized graphene has larger grain size. Researchers are optimistic about extending CVD growth to silicon wafer sizes. Growing graphene with CVD is an attractive solution, because it is highly compatible with existing semiconductor industry processes

III.3.3 Epitaxial graphene

Graphene can be prepared by annealing the SiC crystal at high temperature (1200 °C) in Ultrahigh Vacuum (UHV) [96]. During annealing process, Si atoms will evaporate and leave behind carbon-rich surface. The advantage of this method is that no transfer of the graphene layer is needed to another dielectric substrate because of wide-bandgap SiC substrate. Indeed,

graphene is grown on hexagonally stacked SiC {0001} substrate and top gated FETs can be fabricated.

The graphene layer has different properties based on which face of crystal is grown [97]. For example, graphene grown on Si-face (0001) results in unintentional doping and graphene grown on C-face ($000\overline{1}$) SiC consists of rotational disorder and misalignment with respect to substrate. As a consequence of weak coupling with the substrate graphene grown on C-face has higher mobility than on Si-face and has less doping. There are several pros and cons for this method; the high temperature process and the substrate itself are very expensive, and it is not be suitable for large scale manufacturing.

III.3.4 State-of-the-art of graphene transistor

In the previous section, we discussed the different techniques of graphene synthesis. These different methods yield varying quality of graphene, especially concerning the carrier mobility and homogeneity of the material across the substrate. Besides, the most suitable methods of graphene synthesis will depend on the intended applications. Substantial efforts have been carried out to improve G-FET performances and to overcome its related technical challenges. All these technological efforts in graphene synthesis are intended to find replacement for CMOS "Beyond CMOS" as well as to include more functionalities into the devices "More-than-Moore" [71]. So, here we will detail some of the state of the art of graphene performances of graphene transistors based on different graphene synthesis techniques presented in the previous section.

As an example, a graphene field effect transistor fabricated using mechanical exfoliated graphene demonstrated a high mobility in the order of 8000 $cm^2(V.s)^{-1}$ [38]. On the other hand, an intrinsic cutoff frequency f_T of 300GHz for a gate length Lg of 144nm achieved using exfoliated material [98]. The drawback of exfoliated graphene is uneven films, and unsuitability for large-scale production.

Graphene can also be grown by CVD on metal such as Nickle (Ni) and Copper (Cu). The advantages of this method are large area production and graphene transfer to wide variety of substrates. Examples of published electron mobilities for CVD graphene grown on Ni and Cu are in the range of 1000 $cm^2(V.s)^{-1}$ [90] and 4000 $cm^2(V.s)^{-1}$ [99]. The highest intrinsic

cutoff frequency f_T of 300 GHz was reported for a graphene grown on copper with a gate length Lg of 40 nm [83].

Epitaxial grown graphene offers advantages of the most even films and large scale area. The difficultly of this method is to control morphology and adsorption energy and its high temperature process. Epitaxial grown graphene exhibited mobilities up to 3000 $cm^2(V.s)^{-1}$ on the Si face with a reported intrinsic cutoff frequency f_t of 350 GHz [83] at a gate length Lg of 40nm.

Table III-3 shows the main extrinsic and intrinsic figures of merit reported for some of the different graphene technologies.

Ref	Year	Technology	Graphene layers [width (µm)]	Gate type	Gate length (µm)	G_M (mS/µm)	G_D (mS)	f_t (GHz)		f_{max} (GHz)
								Extrinsic	Intrinsic	
Meric [100]	2008	Exfoliated	One [2.5]	Top gate	0.5	0.11	x	x	14.7	< 1
Lin [101]	2009	Exfoliated	One [~20]	Top gate	0.36	0.08	x	2.6	4	x
					0.15	x	x	26	x	x
Liao [98]	2010	Exfoliated	One [2.5]	Nano wire	0.144	1.27	x	2.4	300	x
					0.182	x	x	1.9	168	x
					0.21	x	x	1.6	125	x
Lin [102]	2010	Epitaxial	One or two [x]	Top gate	0.24	0.15	x	100	x	10
					0.55	x	x	53	x	14
Moon [103]	2011	Epitaxial	One [12]	Top gate	2	0.195	x	4.1	x	11.5
Wu [83]	2012	CVD	One [20]	Bottom gate	0.04	x	x	x	300	44
		Epitaxial	One [20]	Top gate	0.04	x	x	x	350	42
Meric [104]	2013	CVD	One [30]	Bottom gate	0.5	x	x	7.2	x	2.6
Wei [105]	2014	CVD	One [12]	Bottom gate	0.1	0.07	x	10.2	15.5	12
					0.2	0.15	x	8.1	13.5	8
					0.3	0.066	x	2.9	5.5	2.5
IEMN [106] [107]	2014	Epitaxial-GNR	Several [12]	Top gate	0.3	0.61	1.5	3.5	9.5	x
					0.5	0.44	4.6	1.5	2.6	x

Table III-3: State of the art graphene transistors for different technologies.

In particular, the maximum cut off frequency f_t is one of the most important performance which is used to quantify the internal speed of these devices and its potential for high frequency operation. It is clear that having same gate length does not always give the same performances, because these transistors mainly depend on the quality of synthesized graphene

and interface between oxide/substrate and graphene. It should be noted that very high intrinsic f_t are often extracted and reported but these values are extremely dependent on the actual values of extrinsic parameters. However, the maximum oscillation frequency f_{max} is also of prime importance because it is used to quantify the graphene FET's ability to amplify power for high frequency applications. This critical figures of merit is often not given for reported transistors. In conclusions, even though the figures of merit are compatible to universal figures of merit of silicon transistors with same gate length, these graphene transistors suffer from the fabrication related issues making them to not totally obtain extraordinary intrinsic properties.

III.4 Graphene field effect transistors

In this section, we present the graphene transistors that were characterized during this work. The pulsed I-V and RF measurements were carried out on three different devices fabricated by IEMN laboratory at the University of Lille. The main geometrical parameters of characterized devices are given in Table III-4.

- Graphene Nano Ribbon FET (GNR FET)
- Graphene FET (GFET)
  - T-shaped gate (top gated)
  - Bottom gate (on the same plane as graphene)

	Substrate (Name)	Technology	Gate Location (Type)	Measured Device Dimensions			
				Gate length Lg (nm)	Source to Drain Distance Lsd (µm)	Width W (µm)	Ribbon width RW (nm)
Epi-Graphene Nano Ribbon	Silicon Carbide (SiC156)	Epitaxial Grown	Top (-)	500	1.6	12	300
Epi-Large Area Graphene	Silicon Carbide (SiC422)	Epitaxial Grown	Top (T-Gate)	170	0.6	12	x
CVD-Large Area Graphene	Silicon (Si09)	CVD Transfer	Bottom (-)	200	0.7	12	x

Table III-4: Measured graphene transistors and device dimensions.

III.4.1 Epitaxial GNR-FET technology

The main technological details of the first device type, which is a dual gate GNR FET in a coplanar access fabricated at IEMN laboratory are outlined in the following. The few-layers graphene was obtained by thermal decomposition of Si-face of semi-insulating SiC-4H substrate [108], [109]. Fig III-8 shows a Scanning Electron Microscope (SEM) image of the GNR-FET, which has 12µm gate width and 500nm gate length.

As illustrated in Fig III-9, the active part consists in two arrays of twenty 300nm-wide graphene ribbons equally spaced by a distance of 300nm, while the source to drain separation of 1.6µm. The source/drain metal contacts were realized by standard lift-off process with Ni/Au (50nm/300nm). The GNR array [106], [110] was patterned by e-beam lithography and a 5nm-thick Al_2O_3 oxide layer was deposited using the lift-off process. Finally, the two gates lying on the parallel graphene nano ribbons were realized with a length of 500nm.

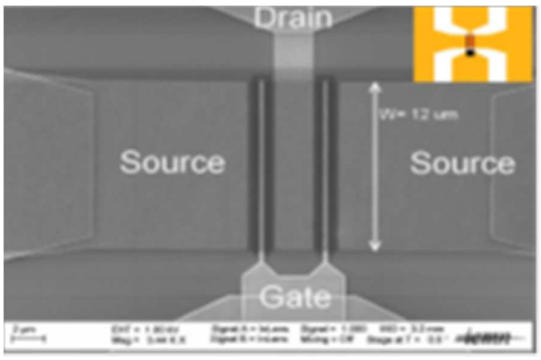

Fig III-8: SEM image of the fabricated top-gated GNR FET [110].

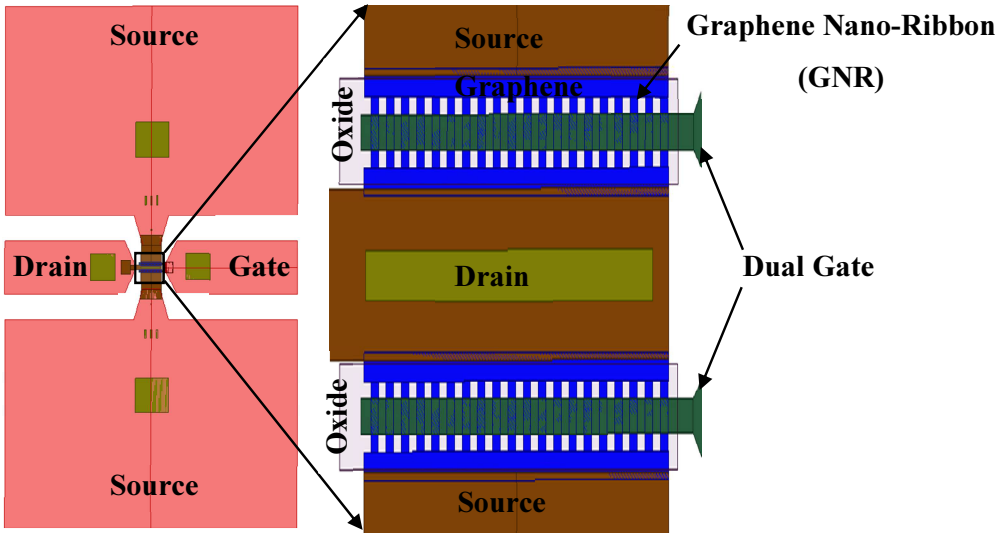

Fig III-9: Coplanar GSG configuration of GNR FET and zoomed channel region.

III.4.2 Epitaxial G-FET technology

Regarding the second device type, epitaxial graphene was synthesized on the Si face of semi insulating 4H-SiC wafer by thermal decomposition in an Ultra-High Vacuum (UHV) chamber where the substrate was heated close to 1150° C leading to desorption of the silicon atoms. This graphitization is detailed in [111]. The number of layers and the quality of the graphene were characterized by Raman spectroscopy. The number of layers was estimated to be around 4 layers. The GFET [112], [107] was fabricated with a T-shaped gate in order to reduce the gate access resistance. First, the channel region was patterned by e-beam lithography and then the graphene was isolated by Reactive Ion Etching (RIE). The source and drain contacts of Ni/Au were obtained by e-beam evaporation metal deposition and standard bilayer lift-off.

When fabricating the GFET, the choice of gate oxide is a vital material of the resulting improved device performances. After the deposition of 2 nm of Al which was left to oxidize in air as a seed layer to facilitate dielectric nucleation, 10 nm of Al_2O_3 were deposited by Atomic Layer Deposition (ALD) at 300° C to be used as a high-k gate dielectric. The ALD was preferred to deposit the gate oxide according to its precision in controlling the film thickness and uniformity [113]. Researchers at IEMN employ a standard tri-layer resist E-beam lithography to realize the T-shaped gates. Finally, coplanar accesses were realized to the source and drain contacts. Fig III-10 (a) shows a scanning electron microscope (SEM) image of a dual-channel graphene RF transistor with a ground-signal-ground coplanar pad which has been designed for suitable for RF measurements. Fig III-10 (b) shows a cross section of a 170nm T-shaped gate.

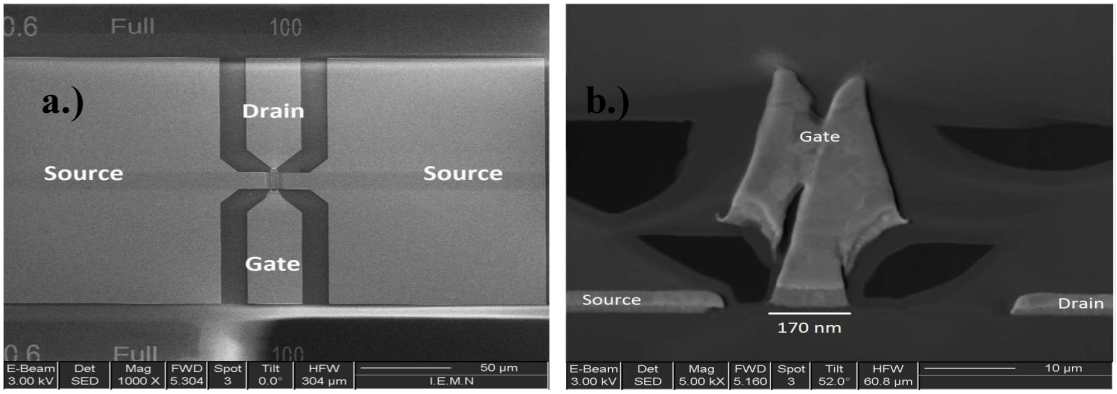

Fig III-10: a.) Scanning electron microscope (SEM) image of a GSG coplanar access of full device. b.) Focused Ion Beam (FIB) image of the cross section of T-shaped gate [112].

III.4.3 CVD transfer bottom gate G-FET technology

The third device type is based on graphene growth on metal substrates (Cu, Ni etc.) by Chemical Vapour Deposition (CVD), which is a highly suitable method for large scale production [97], [114]. Here we present briefly the technological process steps of IEMN laboratory [115]. Monolayer graphene with scale of 2×2cm was grown by using CVD on Cu foil at 1050°C, with $Ar/H_2/CH_4$ at respectively 10/1/2 sccm (standard cubic centimeter per minute) flow by keeping system pressure at 10 Torr throughout the graphene growth experiment. A wet chemical transfer process [105] was carried out as shown in Fig III-11(b).

The bottom gates were realized by e-beam evaporation of Al depositing 40 nm followed by standard lift-off process illustrated in Fig III-11(a). After air exposure of back gates for more than 10 hours, a self-limited natural oxidation leads to a layer of Al_2O_3 with thickness of ~3nm. Next, graphene was deposited onto pre-patterned back gates by implementing transfer procedure [105]. Later, graphene was patterned for isolation defined by e-beam lithography and released by O_2 plasma etching. Evaporation and lift-off process have been used to form source and drain (Ni/Au, 20nm/30nm) with 1µm separation. In this work, we characterized devices with gate width of being 12µm and gate length of 200nm. The SEM image of the active device part with two-fingered bottom gate, which was designed with suitable coplanar access structure for RF measurements, is presented in Fig III-12 at different scales.

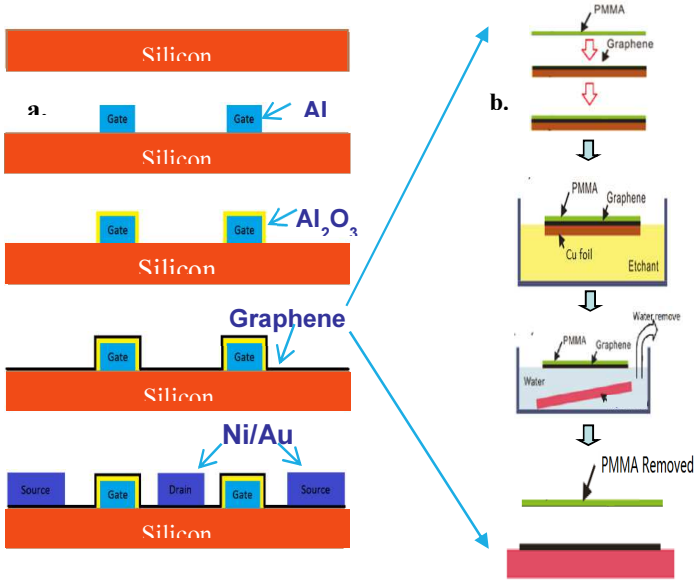

Fig III-11: Schematic of a.) the device fabrication process and b.) the graphene transfer process [105].

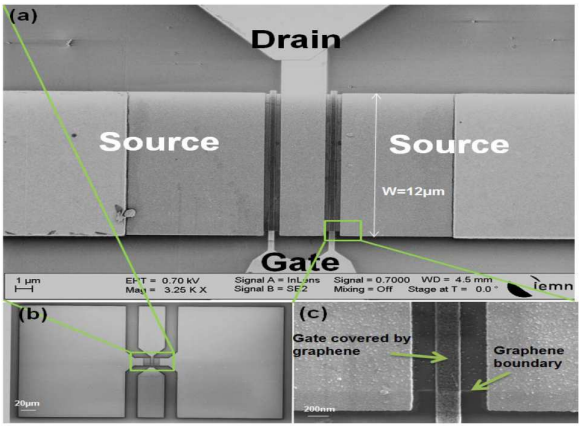

Fig III-12: Scanning electron microscopy (SEM) of a.) active region b.) GSG coplanar structure c.) an enlargement of bottom gate and graphene channel [105] .

III.5 Graphene electrical characterization

III.5.1 Ambipolar effect

Graphene exhibits ambipolar electric field effect such that the Fermi level can be shifted into the conduction or valence bands by applying an electric field giving rise to conduction by either holes or electrons carriers. Thus, in graphene material, the charge carriers in the 2-D channel can switch from electrons to holes with a Dirac point characterizing the transition limit. This is illustrated in the measurement of Fig III-13 in the case of a CVD transfer GFET with gate length Lg of 200nm. The carrier concentration can be as high as 10^{13} cm^{-2} in a good sample under ambient condition. Mobility can exceed 15,000 cm^2/Vs, more than 10 times higher than silicon. The room temperature mobility currently limited by surface roughness and impurities [116] but still can be improved. An important observation is that graphene exhibits a minimum conductivity near the Dirac point where the carrier concentration vanishes.

The longitudinal resistance of a graphene layer on Si substrate as function of bottom gate voltage is shown in Fig III-14 for a CVD transfer G-FET with gate length Lg of 200nm. The plot shows the ambipolar properties of graphene which conducts when either electrons or holes are induced into the material. Note that large slope on either side of the peak shows the fast decrease in resistance, when the magnitude of gate voltage increases. This is due to the advantage of high carrier mobility in graphene and these measurements were made at room temperature.

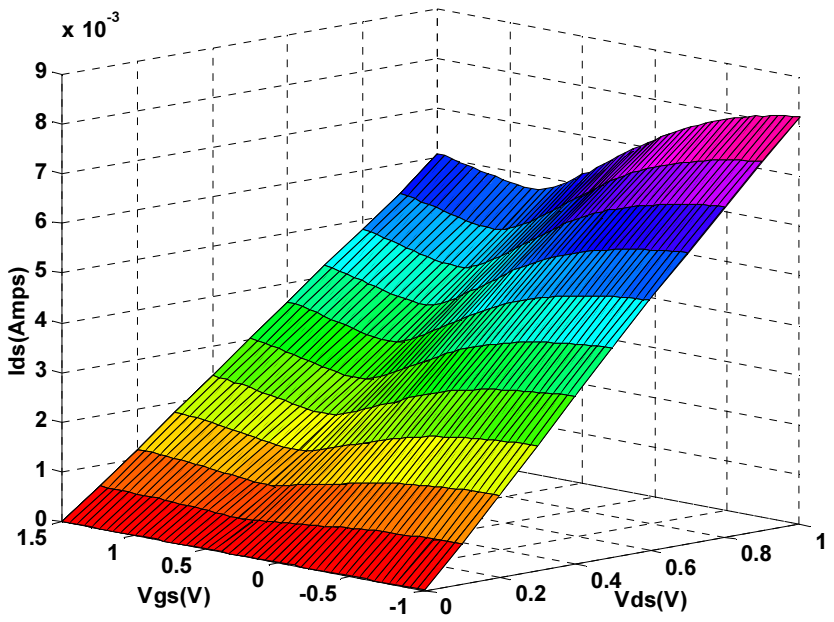

Fig III-13: Transfer characteristics of CVD Transfer G-FET Lg=200nm, W= 12µm, Lsd=0.7µm.

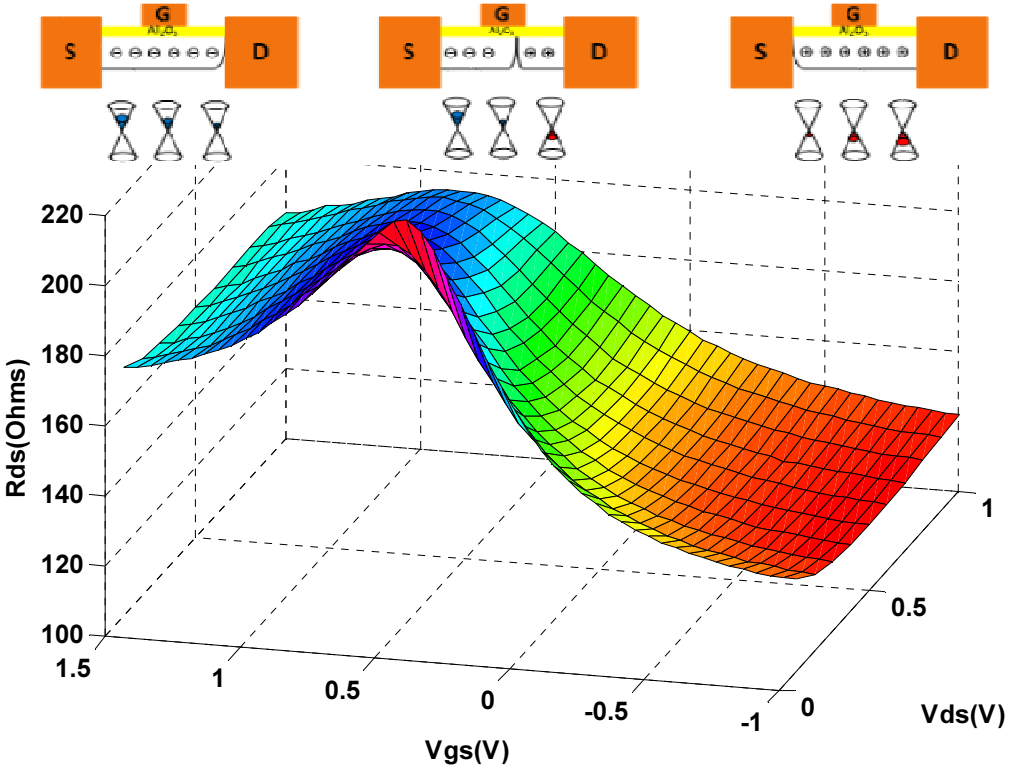

Fig III-14: Resistance versus gate voltage and drain voltage characteristics of CVD Transfer G-FET Lg=200nm, W= 12µm, Lsd=0.7µm.

III.5.2 DC characterization

This section is dedicated to the DC measurement results of the Epitaxially grown Graphene Nano Ribbon FET and Graphene FET (Epi GNR-FET, Epi G-FET) and the CVD transfer Graphene FET (CVD G-FET). As described in *Chapter I, Section I.5.4,* the measurement setup based on the *Keithley 4200-SCS* was used to characterize DC and pulsed I-V behaviors of these transistors.

The measured current and transconductance characteristics (I_{DS} and G_m versus V_{GS}) of the GNRFET are shown in Fig III-15 for V_{GS} varying from -7V to 0V at a fixed V_{DS} voltage of 1V. The patterning of graphene to fabricate narrow ribbon and thus GNRFET is one of the most usual technological method suggested for opening a gap in the graphene and increase the on/off current ratio although it leads to significant degradation of mobility. As high as 400meV bandgap have been reached using very narrow graphene ribbons. However, as already mentioned, the characterized GNRFET has a ribbon width RW of 300nm, which is too large so as to open a bandgap. The energy gap is conversely proportional to the ribbon width of graphene. The graphene has to be patterned in very narrow ribbons of sub-20nm width so as to expect the opening of an energy gap.

The measurements of Fig III-15 was performed at very high negative values of gate voltage so as to locate the Dirac point corresponding to the ambipolar transition point. As observed in Fig III-15, the null value of transconductance was found at -5.45V of V_{GS} voltage. This negative shift of the Dirac voltage is due to the fact that graphene growth on Si face of SiC substrate induced n-type doping. After the first Vgs sweep of this measurement up to high negative gate voltages, the characterized GNRFET was destroyed so that the next measurements on GNRFETs will be limited to lower magnitudes of gate voltage.

The measured transfer characteristics of the drain current I_{DS}, the transconductance G_m and the drain resistance R_{DS} versus V_{GS} are compared in Fig III-16 for the three different technologies of graphene FETs reported in this study. It can be observed that the top gated epitaxially grown GNRFET and GFET are n-type doped, whereas the bottom gated CVD transferred GFET is p-type doped. In the last case of the CVD GFET, we can observe both p-type and n-type conduction properties on both sides of the Dirac point. The doping type is determined by finding the location of the Dirac point with respect to the zero gate voltage for each technology.

As already observed in Fig III-16, the Dirac point measured for top gated GNR-FET devices are found at high negative values (V_{DIRAC} < -5V). It means that graphene channel will conduct when the gate is zero-biased and it is often advantageous when we need low series resistances for graphene FETs [102]. In Fig III-17(a), the Vgs voltage of GNRFET was kept higher than -3V so as to not destroy the device as it was the case in Fig III-16 to find the Dirac point. Indeed, if the Vgs voltage is decreased below -3V to locate the Dirac point, the gate oxide would be damaged. The deposition of oxide layer on the graphene is an important issue of graphene FET technology since the particular atomic structure of graphene makes very difficult to grow an oxide layer with high quality and mastered thickness. In graphene FET technology, one of the most critical issue is related to the quality of dielectric interface to the graphene channel that greatly impact the intrinsic conduction properties of the graphene channel. Indeed, many technology research activities are focused on the improvement of the graphene-dielectric interface such as the use of hexagonal Boron Nitride (h-BN) [117] as the gate dielectric instead of silicon dioxide (SiO_2).

However, the first Vgs sweep of Fig III-15 allowed us to locate the Dirac point at fixed Vds voltage. After that the device was damaged at the gate region so that Fig III-16 only represents the n-type properties of the characterized GNR-FET.

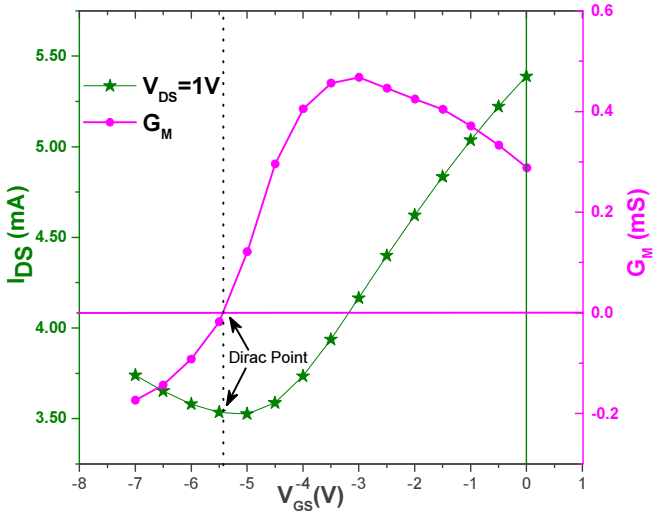

Fig III-15: Measured DC transfer characteristics of the GNR-FET at a fixed V_{DS} voltage of 1V measured dirac point at V_{GS}=-5.45V of dual-gate GNR-FET Lg=500nm, Rw=300nm, Lsd=1.6µm and, W=12µm.

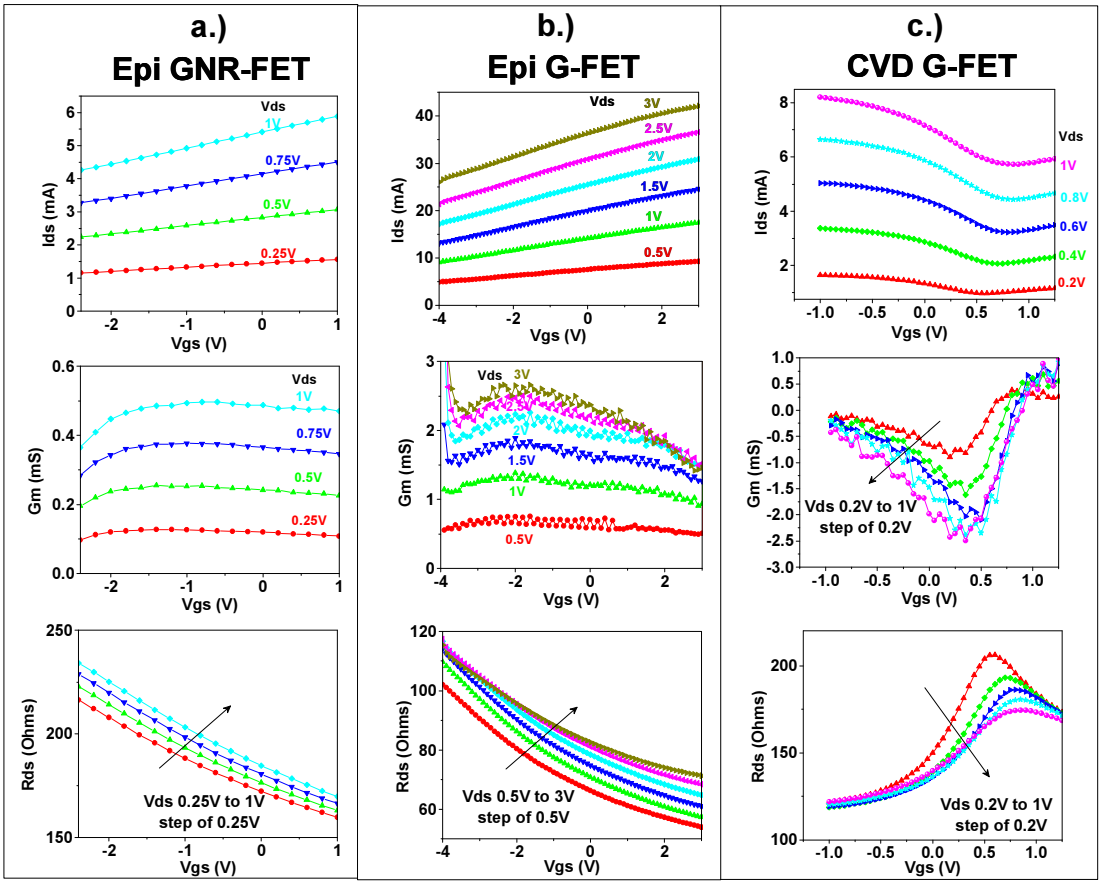

Fig III-16: Transfer characteristics of a.) GNR-FET Lg=500nm, RW= 300nm, Lsd=1.6µm. b.) G-FET Lg=170nm, W= 12µm, Lsd=0.6µm. c.) CVD Transfer G-FET Lg=200nm, W= 12µm, Lsd=0.7µm.

Lastly, the CVD G-FET transfer characteristics are shown in Fig III-16(c) with a Dirac point between 0.5 and 1V of gate voltage. This device shows the complete ambipolar behavior of graphene FETs. The left side of the graphs in Fig III-16(c) is due to p-type (holes) carriers, and the right side is due to n-type (electrons) carriers based on the gate voltage polarity. In the drain resistance characteristic (R_{DS} versus Vgs) of Fig III-16(c), it can be observed that the source to drain resistance (R_{DS}) decreases with increasing Vds voltage around the Dirac point while it has no significant change with Vds in the region away from the Dirac point.

To give complementary insights, Fig III-17 compares the DC measurements of I-V characteristics for the three different graphene transistors. Figures III-17 (a) and (b) show the I-V measurements of GNR-FET and G-FET synthesized by epitaxial process. The current level is increased in Epi G-FET compared to GNR-FET. This difference is due to the larger area of graphene in the G-FET, whereas there are only nano ribbons in GNR-FET. The measured

maximum current for Epi G-FET was around 40mA due to improvements in graphene synthesis techniques. The robust oxide technology used in T-gate Epi G-FET technology allowed us to stress it during measurements for broad range of V_{GS} values (-4V to 3V) and V_{DS} values up to 3V. Figure III-17 (c) shows the I-V measurements of CVD G-FET where it can be observed a crossover point at V_{DS} equal to 0.65V between the I-V curves at constant V_{GS} values (0.5V and 1V). This crossover point represents the ambipolar effect of the device. For V_{DS} values less than 0.65V, the dirac point is close to the V_{GS} value of 0.5V while for V_{DS} values greater than 0.65V, the dirac point is close to the V_{GS} value of 1V. It should be noted that these values indicate p-type doping in the device.

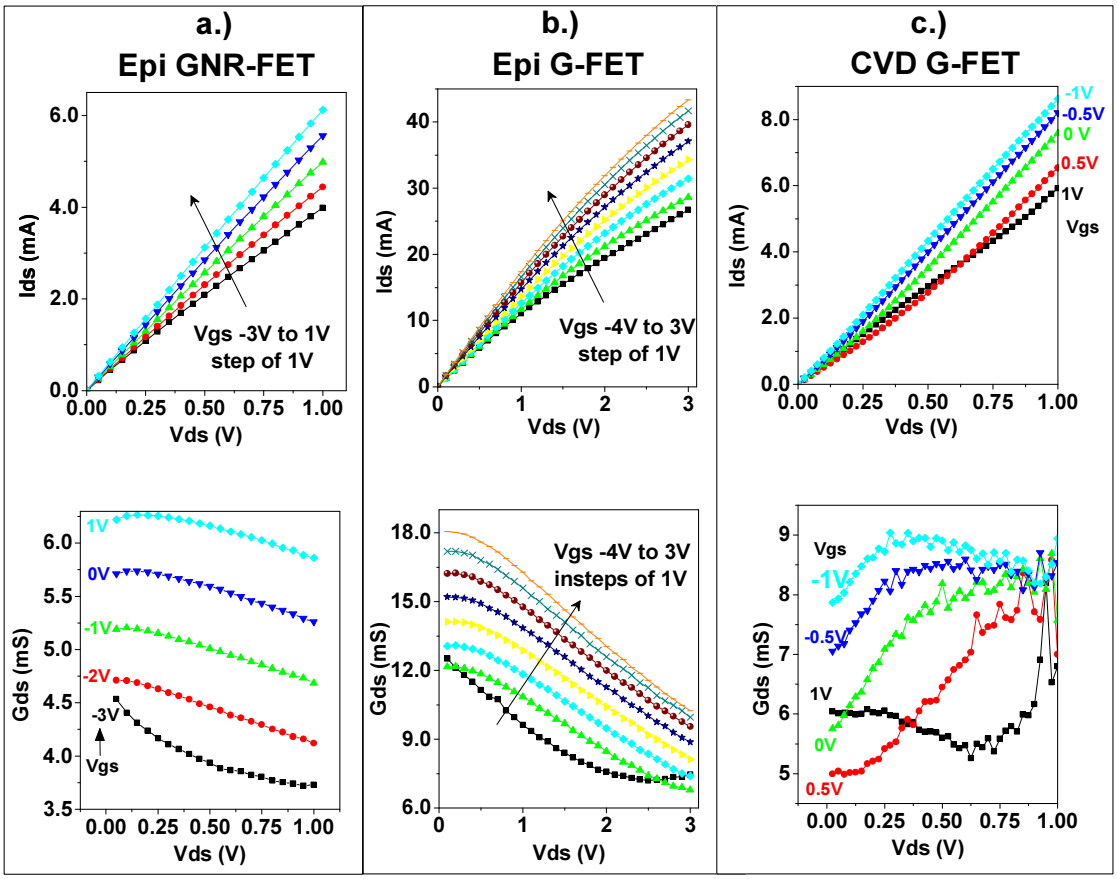

Fig III-17: DC IV characteristics of a.) GNR-FET Lg=500nm, RW= 300nm, Lsd=1.6µm. b.) G-FET Lg=170nm, W= 12µm, Lsd=0.6µm. c.) CVD Transfer G-FET Lg=200nm, W= 12µm, Lsd=0.7µm.

The drain conductance G_{DS} of the three devices are shown in the bottom graphs of Fig III-17. The Epi G-FET has very high values of drain conductance, which correspond to low drain to source resistances R_{DS} when compared to other two technologies. This is due to the decreased access length with source to drain distance Lsd of 0.6µm but also improved graphene

synthesis. The reported behavior in the literature [118] on repeatability and unchanged G-FET performance was also observed in the measurement on Epi G-FET. The other two technologies Epi GNR-FET and CVD G-FET did not demonstrate the same level of repeatability during DC I-V measurements. This can be due to the presence of trap states near gate region or due to graphene substrate interaction or technological immaturity. In conclusion, Epi G-FET graphene technology has proven trap free characteristics for DC measurements and technological maturity in terms of stability and robustness for future electronic applications. However, the Epi G-FET device demonstrated measurement problems during probing for multi-bias S-parameter measurements so that the section devoted to device modeling will be illustrated through the example of GNRFET measurements while the modeling results of the two other devices will be reported in the appendices of the manuscript.

III.5.3 Pulsed IV Characteristics

In addition to the previously reported DC I-V measurements, pulsed I-V measurements have been carried out using Keithley 4200-SCS equipped with Pulse Module Unit (4225-PMU) for highly accurate measurement at very low current levels. The timing parameters of the pulsed I-V measurement were 500ns pulse width and 0.5% duty cycle. As an example, Fig III-18 compares DC and pulsed I-V measurements in the case of the GNR-FET for a V_{GS} sweep from -3V to 0V with a step of 1V. The observed differences in Fig III-18 between DC and pulsed I-V characteristics are decreasing as V_{GS} moves away from the Dirac point. There is no significant difference between DC and pulsed I-V at zero-biased gate voltage V_{GS}. The observed differences cannot be attributed to thermal effects but presumably to trapping effects localized in the oxide-channel and/or the substrate-channel interfaces.

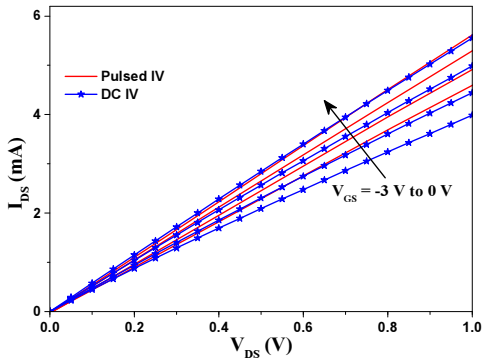

Fig III-18: Measured DC/Pulsed I-V characteristics of the GNR-FET of dual-gate GNR-FET L_g=500nm, R_W=300nm, L_{SD}=1.6µm and, W=12µm.

III.6 Modeling process of the GNR FET

III.6.1 Nonlinear drain current source

Many research activity is actually focused on the technological developments of high performance graphene FETs for high frequency applications. These researches include improved graphene synthesis and dielectric/graphene interfaces. On the other hand, these technological developments have to be accompanied by physics-based and/or CAD-compatible modeling. During this period of technological improvements, the modeling of current-voltage I-V characteristics as well as high-frequency performances are of prime importance. On the one hand, physics-based models [119] are essential for their direct link with technology and device optimization, while on the other hand, simpler compact electrical models [120] [121] fully compatible with measurements and CAD tools are required for the assessment of HF performances and the investigation of future analog high-frequency circuit applications. Indeed, only few analog high-frequency graphene-based circuits have been demonstrated and particularly resistive mixers [122] along with noise and linearity assessment [123] [124]. Therefore, the physics-based models and the compact electrical models have to be jointly developed for offering in-depth insights of the different graphene materials and dielectric types but also investigating circuit applications [125] to project the future graphene-based high frequency electronics.

Regarding the modeling of the drain current source characteristics, although few reported models are based on the ballistic transport theory in the graphene channel, most of the nonlinear modeling works on graphene FETs are based on the drift-diffusion model. However, when compared to the classical analysis of drift-diffusion in semi-conductors, the zero bandgap properties of graphene require a slightly different approach to solve the potential and charge variation along the graphene channel. Finally, most of the nonlinear models aim to be fully compatible with high-frequency circuit CAD tools such as ADS so that realistic assumptions are made to derive analytical model equations from their complex integral forms.

In the literature, most of the current-voltage characteristics of graphene FETs are described by field-effect model and diffusive carrier transport [126] [127]. Therefore, the drain current equation is derived from the resolution of the integral form of the drift equation.

$$I_{DS}(x) = e\frac{W}{L}\int_0^L n(x)v(x)dx \qquad \text{(III-5)}$$

where *e* is the electron charge, *W*, the width of graphene sheet, *L*, the channel length, $n(x)$, the carrier concentration along the channel and $v(x)$, the drift velocity. The variable *x* is the position along the graphene channel varying from 0 to *L*.

The carrier concentration along the graphene channel is given by:

$$n(x) = \sqrt{n_o^2 + \left(\frac{C_G}{e}\right)^2 (V_G - V(x) - V_0)^2} \qquad \text{(III-6)}$$

where n_o is the intrinsic carrier concentration, C_G, the effective gate capacitance per unit area , V_G, the gate voltage, $V(x)$, the potential along the channel and V_0, the Dirac voltage.

At large drain voltage values, if the device demonstrates saturating I-V characteristics in this high-field operating region, the drift velocity is assumed to be saturated at the v_{sat} value.

$$v(x) = \frac{\mu E}{1 + \frac{\mu E}{v_{sat}}} \qquad \text{(III-7)}$$

where v_{sat} is the saturation velocity in the graphene layer, μ, the low-field carrier mobility and, *E,* the electric field. It should be noted that the saturation velocity v_{sat} depends on the carrier concentration.

Many published models are based on the resolution of the preceding drift equations so that to derive an analytical form of the current equation fully compatible with CAD tools [128] [129]. However, it remains very difficult to obtain an analytical physics-based model which is able to represent the ambipolar behavior close to the Dirac point.

Since the measured I-V characteristics of Fig III-19 for the epitaxial GNR FET were limited to a gate voltage Vgs above -3V and drain voltage Vds below 1V so as to prevent breakdown, only the n-type I-V characteristics of the GNR-FET was actually characterized. Thus, the measured I-V characteristics demonstrated a simple behavior with an associated limited ratio of about 1.7 between on/off currents since the ribbon width is too large to open an energy gap. Indeed, the drain current did not show any saturating characteristics. Therefore, a polynomial equation was used to extract a straightforward nonlinear model of the nonlinear current source $I_{DS}(V_{GS}, V_{DS})$ covering only the measured n-type operating region far away from

the Dirac point. The comparison between the extracted model and measurement of the output characteristics I_{DS}-V_{DS} and I_{DS}-V_{GS} is presented in Fig III-19 with a good agreement.

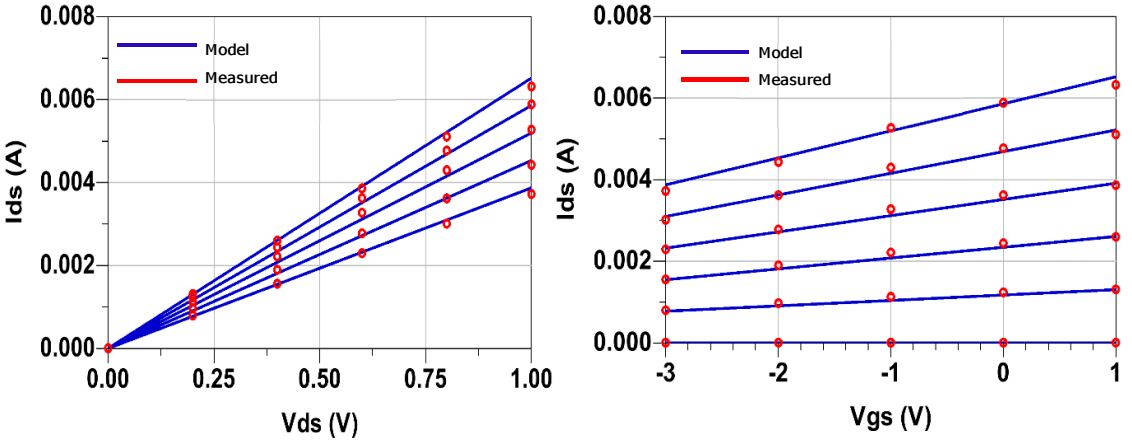

Fig III-19: Comparison between measured and modeled transfer characteristics I_{DS}-V_{DS} and I_{DS}-V_{GS} for the dual-gate GNR-FET L_g=500nm, R_W=300nm, L_{SD}=1.6µm and W=12µm.

III.6.2 High-frequency characterization and modeling

III.6.2.1 De-embedding of extrinsic elements

In order to model the small-signal response of graphene FETs, the device is modeled through an electrical circuit topology that is fully compatible with CAD tools. The lumped circuit element model we have used for graphene transistors is represented in Fig III-20. This circuit topology can be separated in two main parts detailed in the following figure. The first part integrates the extrinsic bias-independent equivalent circuit elements modeling the passive access structure of the device whereas the second part integrates the intrinsic equivalent circuit elements modeling the active intrinsic device.

To derive consistent element values for the intrinsic device, the modeling process starts first by de-embedding the extrinsic bias-independent elements. In the case of classical semiconductor FETs, the characterization of extrinsic elements such as pad capacitances and access resistances and inductances can be performed by using the “cold FET” method [130]. The cold FET measurements are performed at a zero drain voltage under pinched-off channel and the gate operating in forward conduction, which is not possible for graphene transistors. Thus, in order to more accurately separate the determination of extrinsic parasitic elements from the intrinsic elements, two dedicated technological structures were fabricated on the same

wafer as the graphene FETs for the de-embedding process. These two test structures are called PAD and MUTE.

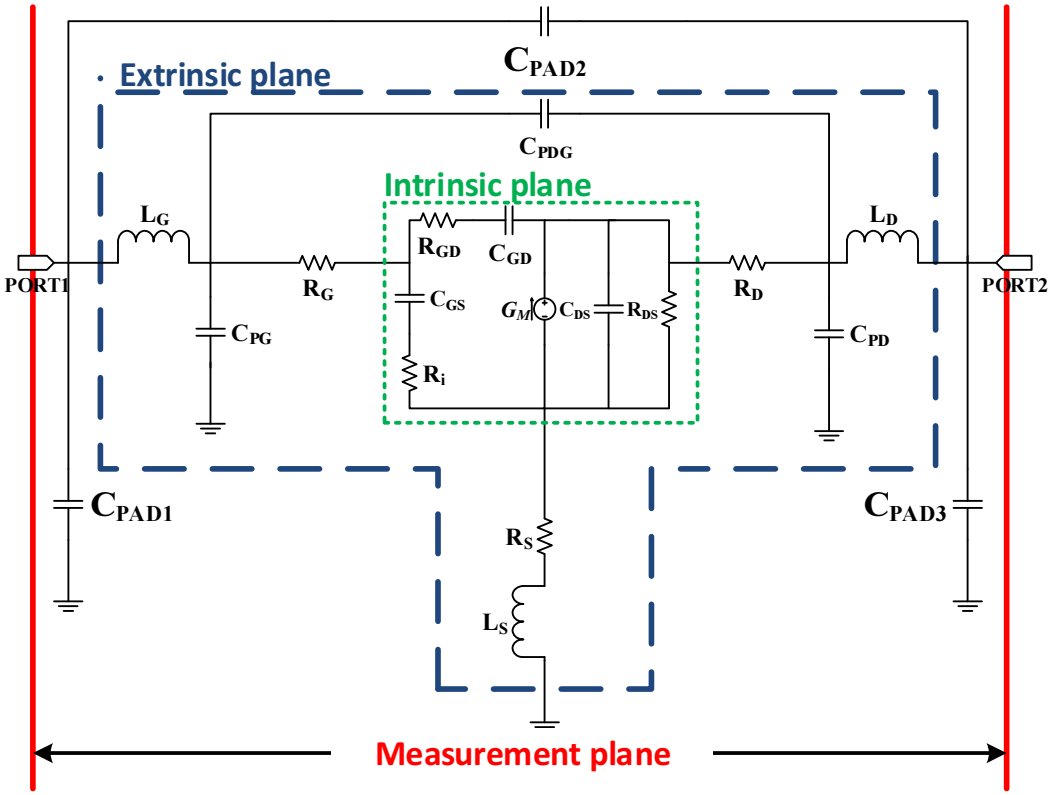

Fig III-20: Small signal equivalent circuit model of the GNR-FET.

The first structure called PAD only integrates the coplanar access structures without integrating the GNRFET between them which remain as open-ended structures. The second structure called MUTE is exactly the same as the processed GNRFET except that the graphene nano ribbons are not integrated in the active channel region.

The two dedicated structures PAD and MUTE are shown in Fig III-21 with their associated equivalent electrical models. The electrical model of the PAD structure is represented by three access and coupling capacitances (C_{PAD1}, C_{PAD2}, C_{PAD3}) in Π network configuration. The electrical model of the MUTE structure not only integrates the PAD capacitances but also the three extrinsic capacitances (C_{PG}, C_{PD}, C_{PDG}) in Π network configuration.

However, these PAD and MUTE structures does not include the contact and access resistances. Since, both de-embedding structures are in open-ended configuration the extraction

of series element (R_G, L_G, R_D, L_D, R_S, L_S) is not possible. In most cases, in the considered frequency domain, due to the very small dimensions of the device, the parasitic inductances are negligible. On the other hand, series resistances such as contact resistances are determined by TLM measurements (Transmission Line Measurement). The required TLM test structures were also fabricated on the same substrate and will be presented in the next section.

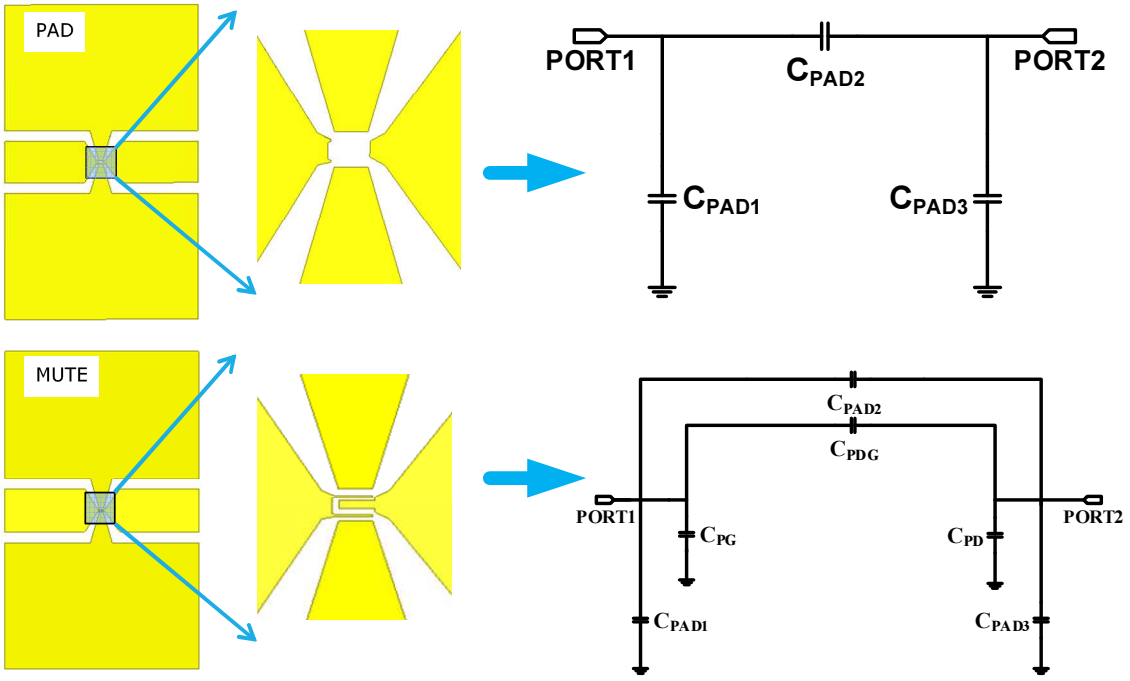

Fig III-21: De-embedding structures and models called PAD and MUTE.

Therefore, high-frequency S-parameters measurements of the PAD and MUTE test structures are measured within the frequency bandwidth. The flowchart represented in Fig III-22 details the extraction process of extrinsic capacitances. First, the three pad capacitances (C_{PAD1}, C_{PAD2}, C_{PAD3}) are analytically extracted versus frequency from measured S-parameters of the PAD structure converted into Y-parameters. In a second de-embedding step, given the previous extracted values of PAD capacitances, the three extrinsic capacitances (C_{PG}, C_{PD}, C_{PDG}) are analytically extracted versus frequency from measured S-parameters of the MUTE structure converted into Y-parameters. The analytical calculation of these extrinsic capacitances are shown in the flowchart of Fig III-22 as a function of measured Y_{PAD} and Y_{MUTE} parameters at each frequency. It should be noted that these extracted capacitances must remain constant versus frequency in order to validate the equivalent circuit models of PAD and MUTE structures.

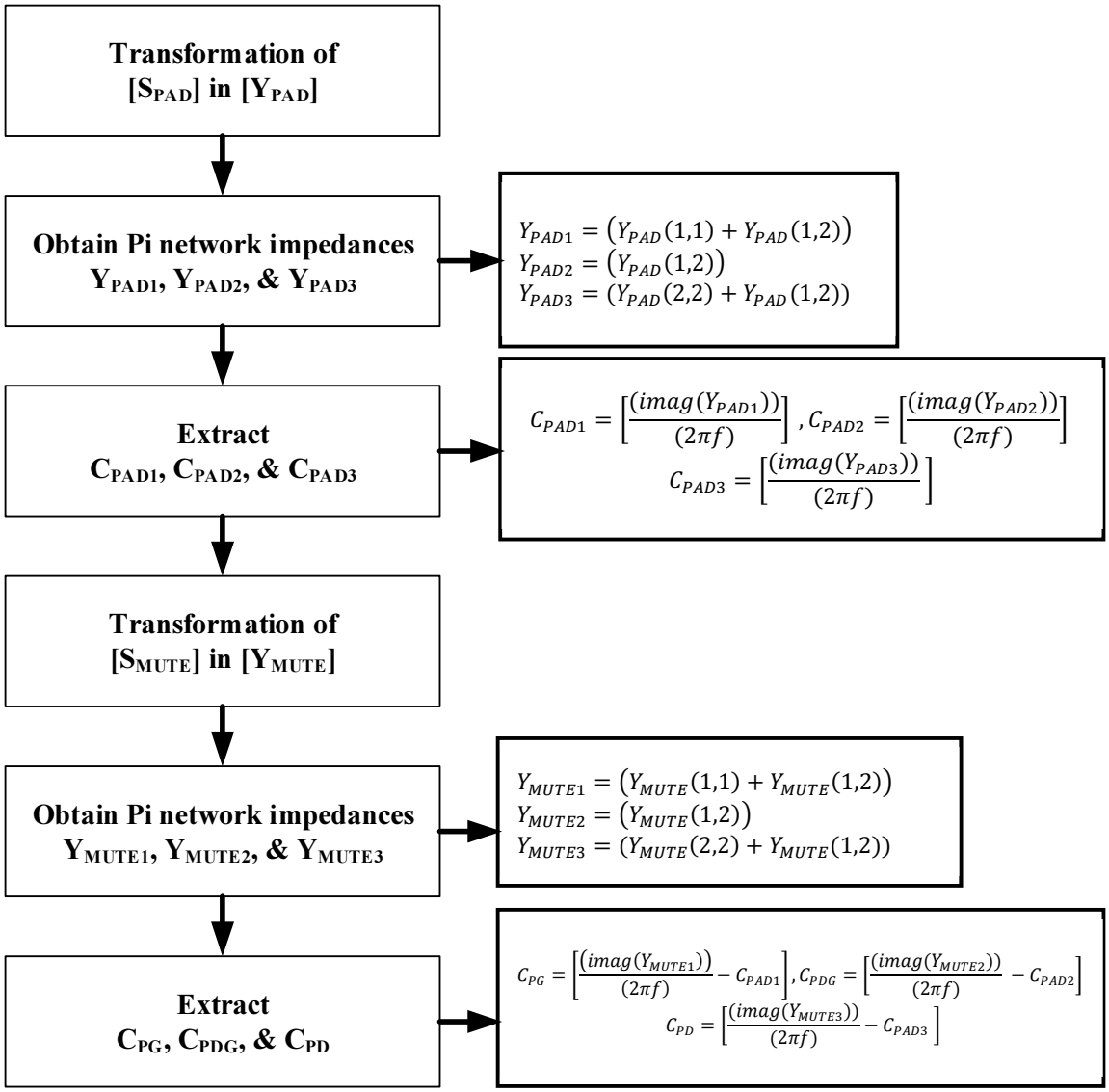

Fig III-22: Flowchart for De-embedding structures PAD and MUTE.

The analytical value of extrinsic capacitances extracted from S-parameter measurements of PAD and MUTE test structures are shown in Fig III-23. It should be noted that the extracted values of extrinsic pad capacitances (C_{PAD1}, C_{PAD2}, C_{PAD3}) remain quite constant over the frequency band, demonstrating the accuracy of the PI-network model and allowing us to determine accurate average values. Although the extracted values of extrinsic capacitances (C_{PG}, C_{PD}, C_{PDG}) are noisier with higher uncertainties since they combine two different measurements, accurate average values can be determined as shown in Fig III-23.

In order to check the overall accuracy of extrinsic capacitance and equivalent circuit models for PAD and MUTE test structures, both equivalent models were implemented in ADS

for S-parameter simulations. Fig III-24 shows the comparison in amplitude and phase between measured and simulated S-parameters of PAD and MUTE structures from 1 GHz to 20 GHz. Except some slight phase differences in S_{12} and S_{21} parameters over 10 GHz, a very good agreement is verified for both dedicated de-embedded structures.

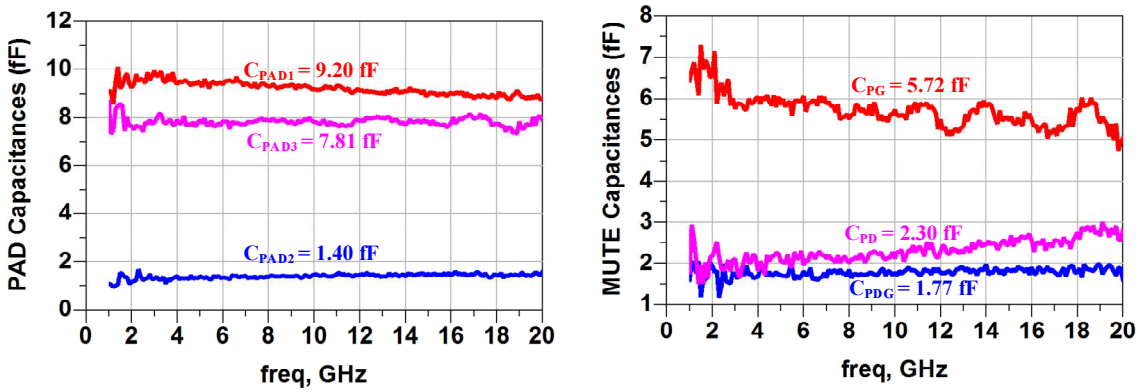

Fig III-23: The extrinsic capacitances determined from measured S-parameters of de-embedding structures (PAD and MUTE) in [1-20 GHz] frequency band.

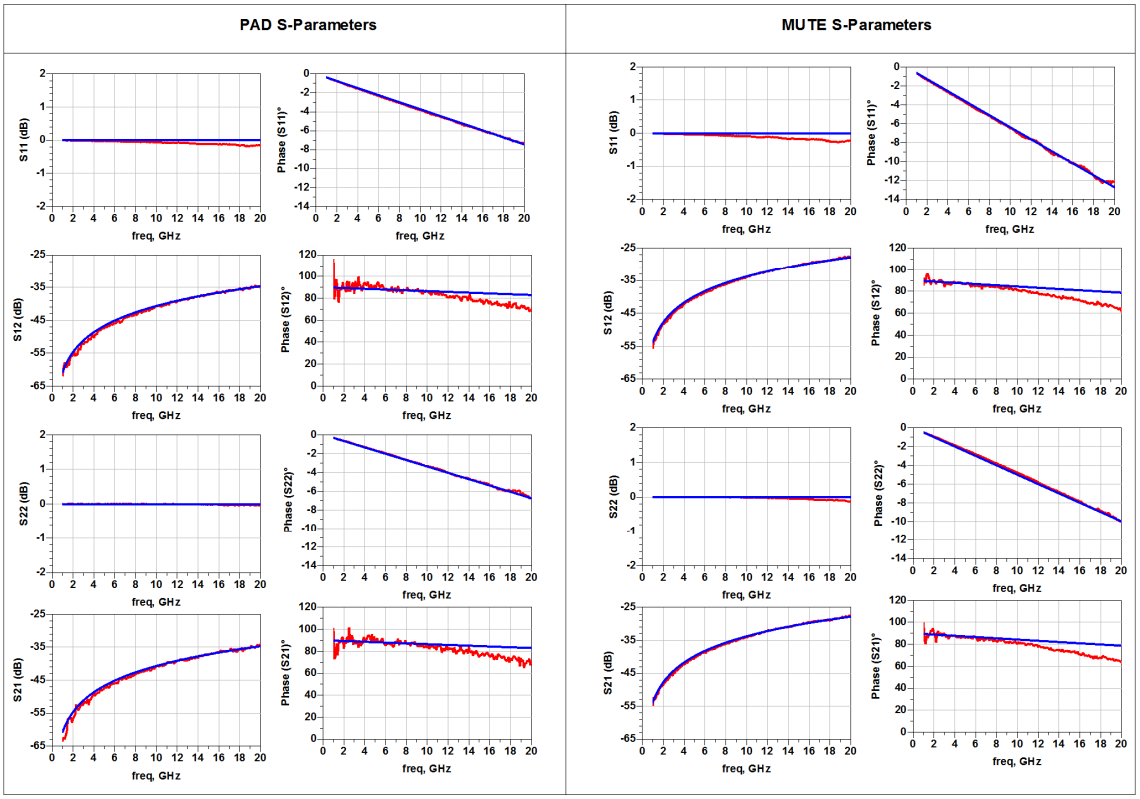

Fig III-24: Comparison of simulated (blue) and measured (red) S-parameters of PAD and MUTE test structures over the [1-20] GHz frequency band.

III.6.2.2 Contact resistance

In order to measure contact and sheet resistances, test patterns were designed by IEMN for TLM (Transmission Line Measurement) on the same wafer. The typical schematic of a TLM test pattern is shown in Fig III-25. Typically, to determine the contact resistance between a metal and a semiconductor, a TLM structure consists of a series of metal-semiconductor contacts separated by different semiconductor lengths d of constant width W.

As shown in Fig III-25, in the case of a graphene TLM pattern, the current flows from the first metal/graphene contact, then through the graphene sheet, and finally into the second metal/graphene contact. Therefore, the total measured resistance R_T represents the sum of twice the metal/graphene contact resistance R_C and the graphene resistance R_{gr} between contacts.

$$R_T = R_C + R_{gr} + R_C = \left(\frac{R_S}{W}\right) d + 2R_c \qquad \text{(III-8)}$$

where R_C is the contact resistance, R_S is the sheet resistance while (d, W) are the length and width of the graphene sheet, respectively.

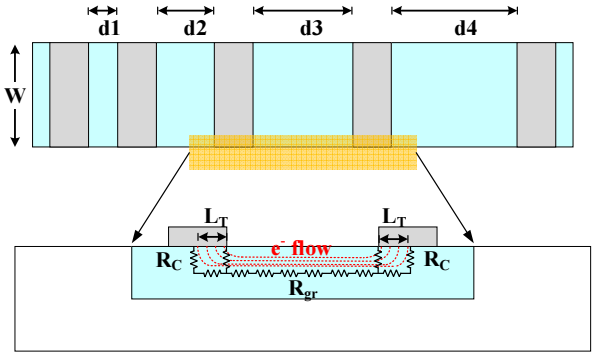

Fig III-25: Schematic of TLM structure.

As the TLM structure is measured for different separation distances d between metal leads, Equation III-10 shows that the plot of total resistance R_T versus d should be linear. The slope of this line is the ratio (R_S / W) whereas the y-axis intercept point is twice the contact resistance $2R_C$. This is illustrated in measurements of Fig III-26 in order to graphically determine the sheet resistance and the contact resistance.

In TLM measurements, the transfer length L_T (Fig III-26) is another parameter regarding contact quality since the current flow is not uniform along the contact in planar

configuration. Indeed, the current is large at the edge of the contact and decreases along the contact to be null at the far edge. This is known as "current crowding" in planar technology so that the transfer length L_T is defined as the average length that electrons travel in the graphene sheet beneath the contact before flowing into the metal lead. This in turn defines ($L_T \times W$) as the effective contact area S_C and the transfer length L_T is defined by

$$R_C = R_S\left(\frac{L_T}{W}\right) = R_S\left(\frac{{L_T}^2}{WL_T}\right) = R_S\left(\frac{{L_T}^2}{S_C}\right) \longrightarrow L_T = \sqrt{\frac{R_C\, S_C}{R_S}} = \sqrt{\frac{\rho_C}{R_S}} \qquad \text{(III-9)}$$

with the contact resistivity ρ_c expressed by

$$\rho_C = R_C\, S_C = R_S {L_T}^2 \qquad \text{(III-10)}$$

Therefore, from Equations III-10 and III-11, the total resistance R_T can be expressed as a function of the (R_S/ W) ratio, the sheet length d, and the transfer length L_T

$$R_T = \frac{R_S}{W}(d + 2L_T) \qquad \text{(III-11)}$$

Thus, the plot of the measured total resistance R_T versus the sheet length d can also be used to determine the transfer length L_T at the x-axis intercept point which corresponds to (-$2L_T$) value. This is illustrated in measurements of Fig III-26.

The contact and sheet resistivity of graphene with metal Ni/Au (50nm/300nm) stacking were determined by TLM measurements on 65um-wide test patterns using various graphene lengths from 5 to 20 um integrated on the same substrate. The plot of the total resistance R_T versus graphene length d is shown in Fig III-26 with the extraction of the slope, x- and y-axis intercept points which in turn give the sheet resistance R_S, the contact resistance R_C and the transfer length L_T, respectively. Finally, the extracted values from a TLM test pattern give a contact resistance R_C of 4.5 Ω, a transfer length of 0.19 µm, a contact resistivity ρ_c of 5.6 10^{-7} Ω.cm^2 and a sheet resistance of 1560 Ω/sq for the synthesized graphene [131]. Here is an example of contact resistance extraction from TLM measurements although these measurements have to be examined over all the wafer locations to check its uniformity that may be very different because of surface inhomogeneity.

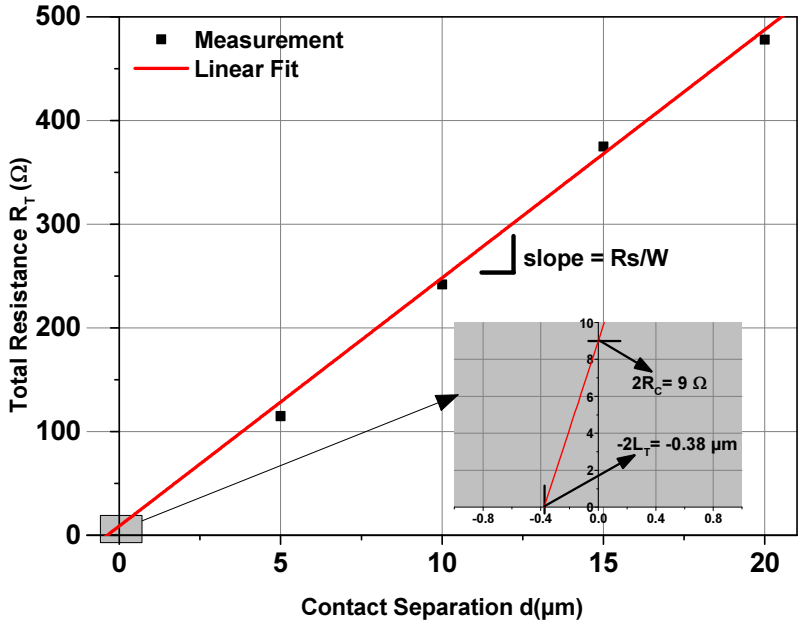

Fig III-26: TLM measurement graph with linear approximation [131].

III.6.2.3 HF characterization and parameter extraction

To assess the high frequency performances of graphene FETs, microwave S-parameter measurements were performed from 500 MHz to 20GHz using a vectorial network analyzer (VNA Anritsu 37297D) and on-wafer SOLT calibration.

The entire small-signal electrical model of the graphene FET is shown in preceding Fig III-20. The coplanar PAD and MUTE test structures integrated with the GNRFET were simultaneously characterized to be used for the equivalent circuit modeling of extrinsic and intrinsic model parameters. The extraction method and measurement results of the bias-independent PAD and MUTE structures are already reported in Fig III-22 to Fig III-24.

The extraction method of model parameters in Fig III-20 is based on the optimization of extrinsic access elements (R_G, L_G, R_D, L_D, R_S, L_S) except the values of extrinsic capacitances (C_{PAD1}, C_{PAD2}, C_{PAD3}, C_{PG}, C_{PD}, C_{PDG}) that were already extracted from MUTE and PAD measurements. It should be noted that the R_D and R_S values are rather low compared to those found in literature. This modeling process is based on the direct extraction method used for circuit modeling of field-effect [57]. Indeed, each optimization step corresponds to a given set of all extrinsic model parameters, and thus the intrinsic Y-parameters can be determined from

extrinsic measured S-parameters by matrix de-embedding using extrinsic parameter values. Then, each of the eight intrinsic parameters (C_{GS}, C_{GD}, C_{DS}, g_M, G_{DS}, R_i, τ, R_{GD}) can be analytically expressed at each frequency in terms of intrinsic Y-parameters using the well-known equations of FET electrical models [130]. The error function of extrinsic parameter optimization is linked to the variation of analytically extracted intrinsic elements over the frequency band since they have to be frequency-independent.

Table III-5 show the model parameters of the considered GNRFET extracted from S-parameter measurements at 1V of V_{DS} and -2V of V_{GS}. It can be noted that the high-frequency values of g_M and G_{DS} are consistent with the DC values extracted in Fig III-17 and III-18.

PAD Capacitances			**Extrinsic elements**								
			GATE			**DRAIN**				**SOURCE**	
C_{PAD1} (fF)	C_{PAD2} (fF)	C_{PAD3} (fF)	R_G (Ω)	L_G (pH)	C_{PG} (fF)	C_{PDG} (fF)	R_D (Ω)	L_D (pH)	C_{PD} (fF)	R_S (Ω)	L_S (pH)
9.2	1.4	7.8	1.3	7	5.7	1.7	4.2	9	2.3	4.2	4

Intrinsic elements									
V_{DS}=0V, V_{GS}=-2V		V_{DS}=1V, V_{GS}=-2V		C_{GS} (fF)	R_i (Ω)	C_{GD} (fF)	R_{GD} (Ω)	C_{DS} (fF)	T_{au} (psec)
g_M (μS)	G_{DS} (mS)	g_M (μS)	G_{DS} (mS)						
0.1	5.9	440	4.6	12.3	135	15.4	184	0.1	0.1

Table III-5: Circuit model parameters at VDS=1V and VGS=-2V of the dual-gate GNRFET (Lg=500nm, RW=300nm, LSD=1.6μm, W=12μm) from 0.5 to 20 GHz.

As an example of model agreement, Fig III-27 compares simulated and measured S-parameters at a constant gate voltage of -2V in the case of 0 and 1V drain voltage. In this case, the simulation implements the nonlinear GNRFET model where all electrical model parameters of Table III-5 are considered bias-independent except the transconductance g_M and drain conductance G_{DS} which are replaced by the polynomial nonlinear current source $I_{DS}(V_{GS}, V_{DS})$.

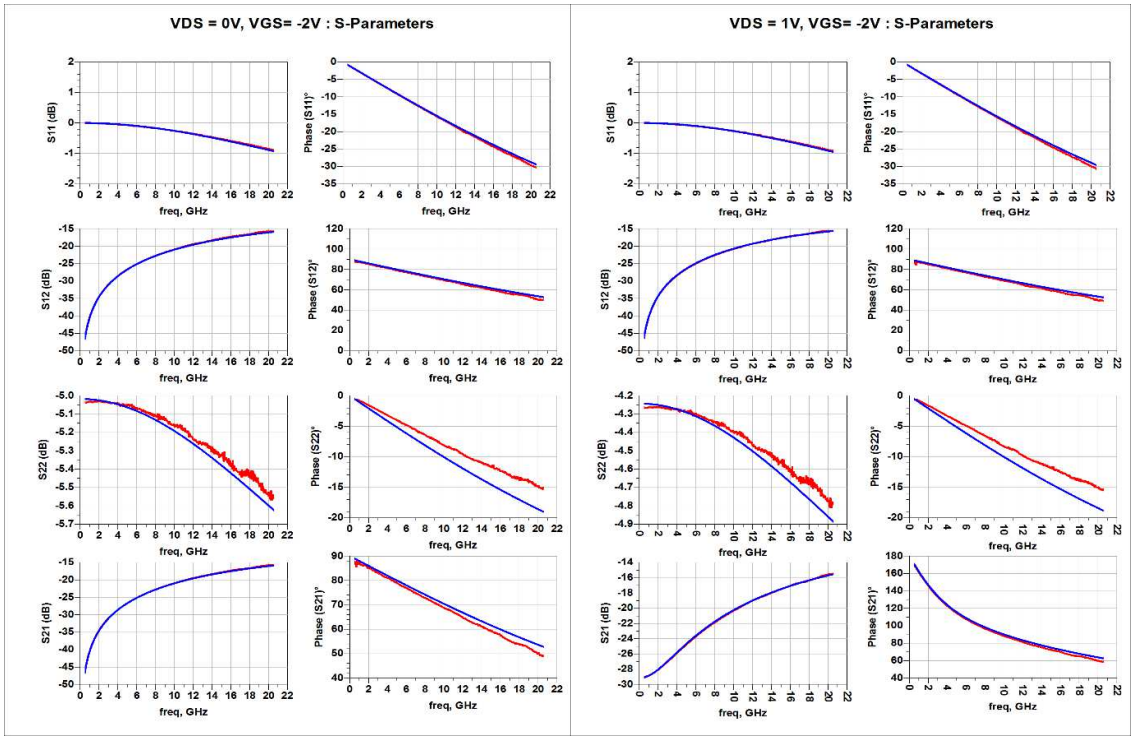

Fig III-27: Comparison of simulated (blue) and measured (red) S-parameters at a fixed gate voltage V_{GS} = -2V and two drain voltages (V_{DS} = 0V and 1V) for the dual-gate GNRFET.

The end of this section compares multi-bias S-parameter measurements and circuit simulations of the GNRFET model integrating the polynomial nonlinear current source. Fig III-28 compares measured and simulated S-parameters in the frequency range 0.5-20 GHz at V_{DS}=0V and V_{DS}=1V for V_{GS} varying from -3V to 1V. The observed impact of the gate voltage V_{GS} on S_{22} is consistent with the one observed on R_{DS} variations in the measured I-V curves of Fig III-17 since the drain channel resistance R_{DS} of the GNRFET decreases as V_{GS} moves away from the Dirac point. However, the drain channel resistance R_{DS} depends on both bias voltages.

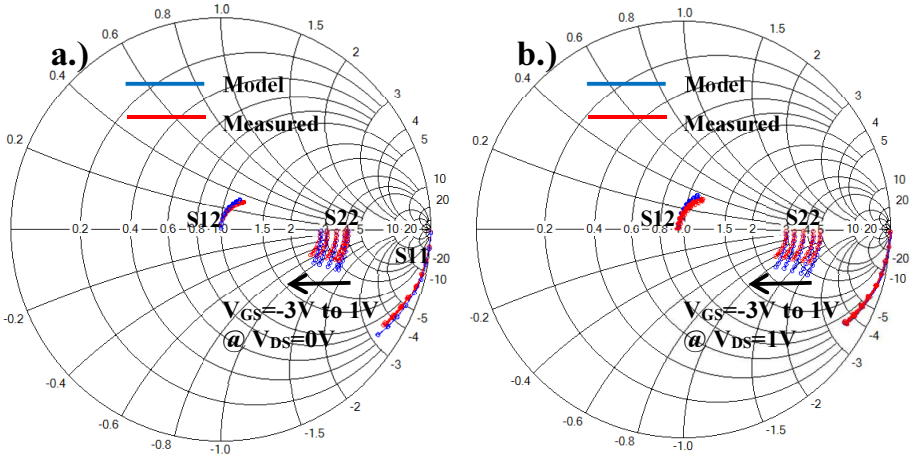

Fig III-28: Comparison of simulated and measured S-parameters at two fixed drain voltages VDS = 0V (a) and VDS = 1V (b) when VGS is varied from -3V to 1V in steps of 1V for the dual-gate GNRFET

III.6.3 Figures of merit for high frequency applications

The potentiality of graphene transistors for high-frequency electronics is one of the most important development axis of graphene-based FETs. The high-frequency performances of any microwave transistor are usually assessed by two main small-signal figures-of-merit, which are the maximum oscillation frequency f_{max} and the transition frequency f_t. The different technological process and graphene materials compete internationally to achieve both wafer-scale graphene integration and record cutoff frequencies. In this competition, the mechanically exfoliated graphene has always presented impressive frequency performances but both wafer-scale epitaxial graphene and CVD grown graphene have also demonstrated their great potentialities with cut-off frequencies f_t above 300 GHz for sub-50nm gate lengths and maximum oscillation frequencies above 40 GHz.

Although the cutoff frequency f_t is typically used to compare high frequency performances of graphene FETs, the maximum oscillation frequency f_{max} is an important figure-of-merit to assess potentialities for high-frequency analog applications since it is the highest operating frequency beyond which a transistor is not able to amplify power. The maximum oscillation frequency f_{max} is defined as the frequency at which the unilateral power gain is unity or 0dB. The unilateral power gain is also called the Mason's unilateral gain (MUG) which is expressed as a function of small-signal S-parameters by

$$MUG = \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)} \quad \text{(III-12)}$$

It can be noted that in some publications, the maximum oscillation frequency f_{max} is referred to the frequency at which the maximum available gain (MAG) decreases to unity. The two frequency results and definitions are not significantly different.

Although it is recognized that high-frequency applications require both high f_{max} and f_t, the graphene FETs are benchmarked against their performances in terms of cutoff frequency. In most of the published papers, only the cutoff frequency f_t is mentioned. The cutoff frequency f_t is defined as the frequency limit where the current gain drops to unity or 0dB. The short-circuit current gain is expressed as a function of small-signal S-parameters by

$$h_{21} = \frac{-2S_{21}}{(1-S_{11})(1+S_{22}) + S_{12}S_{21}} \quad \text{(III-13)}$$

In the case of the GNRFET of 500nm gate length presented in this section, Fig III-30 shows the comparison between measured and simulated current gains and extrinsic cutoff frequencies at a fixed drain voltage of 1V and two gate bias of -2V and 0V. The relatively low values of f_t for this first generation devices is mainly related to the gate length of 500nm and the f_{max} value is not significant in this case. However, higher f_t values are reported in the appendices for the two other characterized devices of this work while very high f_t have also been reported by IEMN for up-to-date graphene FETs. The Fig III-29 also gives the intrinsic current gain and cutoff frequencies deduced from de-embedded S-parameters using modeled extrinsic elements. Due to the great values of extrinsic parasitic elements, there is an important discrepancy between the intrinsic and extrinsic f_t values. It can be noted that the comparison of graphene materials and device technologies regarding only the intrinsic value of cutoff frequency should be always related to the extrinsic f_t since this difference can be very large according to the retained values of extrinsic elements.

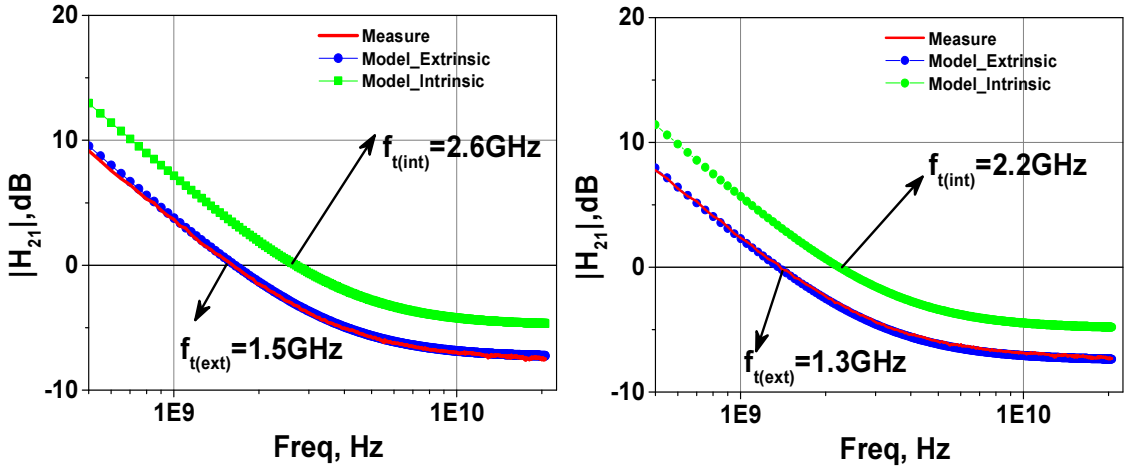

Fig III-29: Measured/Simulated ft and intrinsic ft at V_{DS}=1V for two gate bias: V_{GS}= -2V (left graph) and V_{GS}= 0V (right graph) of dual-gate GNR-FET (L_g=500nm, R_W=300nm, L_{SD}=1.6µm, W=12µm).

III.7 Conclusions

In this chapter, we presented the main physical characteristics and electronic structure of graphene explaining its great conduction properties for fabricating high-speed devices in terms of mobility, saturation velocity and current density. State-of-the-art performances of graphene-based FETs were presented along with the main synthesis technique of graphene material, among which are the mechanical exfoliation and wafer-scale epitaxial graphene or CVD grown graphene.

This work on graphene FET characterization and modeling has benefited from the graphene FET technologies developed at the IEMN laboratory of Lille. Thanks to this cooperation, we have characterized three types of graphene-based FETs which are a CVD grown graphene FET (CVD-GFET) of 200nm gate length and epitaxially grown on SiC GNRFET and GFET with gate lengths of 500nm and 170nm, respectively. This chapter described these three types of graphene FET devices with their measured DC/pulsed I-V behaviors and respective doping properties.

Thereafter, the high-frequency equivalent circuit modeling of devices is illustrated through the example of the GNRFET while the modeling results of the two other devices are given in appendices for the sake of readability. The equivalent circuit model of graphene FETs and the different steps of the modeling process based on DC/Pulsed I-V measurements and high-frequency S-parameter measurements are described. Since the "cold-FET" method, which is typically used for parasitic extraction of FETs, cannot be used for graphene FETs, two dedicated on-chip de-embedding structures called PAD (only coplanar access) and MUTE (FET structure without graphene) were fabricated on the same wafer as graphene FETs to enable an accurate extraction of extrinsic parasitic model elements. Then, the remaining model parameters are extracted from the optimization of unknown access elements coupled to an analytical determination of intrinsic parameters. This nonlinear compact model has the advantage of an easy implementation in commercial CAD tools. The electrical model consistency has been checked through the comparison of measured and simulated multi-bias S-parameters for several graphene-based devices. The presented nonlinear model was focused on the n-type device behavior away from the Dirac point because of device reliability during measurements. Indeed, although the nonlinear FET model may only consider one conduction type for the CAD of most of the high-frequency integrated applications, specific model

enhancements in terms of accounting Dirac point need to be included in future electrical models. However, one of the critical issue is to develop fully compatible CAD models.

As a conclusion, graphene material presents impressive potentialities for high-frequency applications but this new technology is still facing great technical challenges for wafer-scale FET integration. Some of the critical issues in graphene FET technology are related to the interfaces between graphene and its supporting substrate as well as between graphene and its gate dielectric insulator, which both affect the intrinsic electrical transport properties of the graphene channel and particularly its actual carrier mobility. The quality of 2D graphene materials along with the choice and engineering of dielectric and substrate interfaces to the graphene are still subject to intensive technological developments to improve wafer-scale graphene FET technology.

General Conclusions

The first chapter of this thesis was focused on the presentation of different DC, pulsed and RF measurement techniques and setups required to characterize high frequency high-power transistors such as GaN HEMTs and high-frequency characteristics of nano-transistors such as graphene FETs. Pulsed I-V and RF measurement setups were already developed at XLIM for modeling very high power RF transistors. However, as this thesis was also focused on the high-frequency characterization of graphene FETs, a great part of this work consisted of developing a new DC/pulsed I-V and S-parameter measurement setup dedicated to accurate low-current measurements of nano-devices. This new setup is based on the Keithley 4200 semiconductor characterization system (SCS) with an additional pulse measure unit (PMU-4225). Some shortcomings of present day characterization techniques are also outlined in this first chapter.

In Chapter II, the measurement set-up and associated characterization procedures are presented for time-domain pulsed I-V characterizations of trapping dynamics in AlGaN/GaN HEMTs. Accurate nonlinear electrical CAD models are required for efficient circuit designs dedicated to high power applications at microwave frequencies under complex modulated signals. In order to determine the electrical parameters of such a nonlinear model, many specific characterizations are needed. Actually, most of the existing nonlinear models do not account for trapping dynamics which have a critical impact on modulated signals. Our research group published a new nonlinear model [68] that integrates the effect of trapping time constants in AlGaN/GaN HEMTs. In this thesis, through new capabilities of the developed setup, we implemented new techniques of time-domain pulsed IV measurements by which it is possible to assess the different trapping time constants associated with the safe operating areas on I-V network (ohmic, pinch-off and saturation). The measurement procedure for determining the influence of temperature, electrical history and their mutual interaction on trapping phenomena are illustrated in this chapter. Taking advantage of the set-up capabilities to reach very short and very long pulse widths, thermal and trapping effects can be discriminated. This characterization method provide an efficient way to assess the different thermal and trapping time constants for the nonlinear modeling task that are of great interest, especially in the case of pulsed waveforms such as in radar applications. The perspectives of this work are numerous in terms of characterizing high power AlGaN/GaN HEMTs for future high-power multi-functions pulsed radar and communication applications as well as providing consistent nonlinear models taking into account the dynamics of traps. The characterization procedure of trapping dynamics and electrical history are dedicated to the nonlinear modeling of

AlGaN/GaN HEMTs and its impact on high power applications in the context of modulated signals and complex pulsed radar sequences.

Finally, the chapter III discusses the graphene physics along with the high-frequency characterization and circuit modeling of wafer-scale graphene FETs. With this aim in view, a new DC/pulsed I-V and S-parameter measurement setup dedicated to accurate low-current measurements of nano-devices was developed and is reported in chapter I. In complement, this work benefited from a close cooperation with Professor Happy of the IEMN laboratory at Lille who allowed us to characterize and model three types of wafer-scale graphene FETs, which are epitaxially grown on SiC (GNRFET, GFET) and a CVD grown graphene FET. In this last chapter, these three types of graphene FETs are described. An equivalent circuit model is presented along with the different modeling steps based on DC/Pulsed I-V measurements and high-frequency S-parameter measurements. The nonlinear model consistency has been checked through the comparison of measured and simulated multi-bias S-parameters for several graphene-based devices. Indeed, although the nonlinear FET model may only consider one conduction type for the CAD of most of the high-frequency integrated applications, specific model enhancements in terms of accounting Dirac point need to be included in future electrical models.

There are several downsides concerning the wafer-scale fabrication of high-frequency graphene FETs. One of the most relevant issues are the improvement of synthesized graphene quality along with the engineering and choice of the dielectric and substrate interfaces to graphene, which affect the intrinsic transport properties, induce surface trap densities that lead to shift in Dirac point, and degrade the gate control on channel modulation. Indeed, all these technological challenges are subject to an intensive coordinated research activity within the frame of the "Graphene Flagship", which is a very high scale research consortium supported by the European Union. In this context, the suited technologies for fabricating stable single-atom-thick to few-atom-thick layers of 2D materials are investigated along with research activities on "Beyond Graphene Materials" such as oxides (e.g., vanadium pentoxide V_2O_5), silicene, transition metal di-chalcogenides TMD (e.g., molybdenum sulfide MoS_2), and nitrides (e.g., hexagonal boron nitride h-BN). Many of other 2D materials are at a very initial phase of theoretical research activities

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Relevant publications

JOURNAL:

[1] **P. NAKKALA, A. MARTIN, M. CAMPOVECCHIO, S. LAURENT, P. BOUYSSE, E. BERGEAULT, R. QUÉRÉ, O. JARDEL, AND S. PIOTROWICZ,** ***"Pulsed characterization of trapping dynamics in AlGaN/GaN HEMTs,"*** *Electronics Letters, vol. 49, no. 22, pp. 1406–1407, Oct. 2013.* This article has following corresponding article: in brief.

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[3] **R. QUERE, T. REVEYRAND, P. BOUYSSE, P. NAKKALA, A. MARTIN, O. JARDEL, J.-M. NEBUS, E. BERGEAULT, AND M. CAMPOVECCHIO,** ***"Impact des effets de pièges sur la dynamique grand signal des transistors à effet de champ sur Nitrure de Gallium,"*** *in Journées Nationales Micro-ondes (JNM), pp. 1-3, 2013.*

[4] **P. NAKKALA, N. MENG, A. MARTIN, M. CAMPOVECCHIO, AND H. HAPPY,** ***"Characterization and circuit modeling of Graphene Nano Ribbon field effect transistors,"*** *in IEEE MTT-S International Microwave Symposium Digest, no. V, pp. 1–4, 2014.*

[5] **P. NAKKALA, A. MARTIN, M. CAMPOVECCHIO, H. HAPPY, M. S. KHENISSA, M. M. BELHAJ, D. MELE, I. COLAMBO, E. PALLECCHI, AND D. VIGNAUD,** ***"High frequency characterization and compact electrical modelling of Graphene Field Effect Transistors,"*** *in 44th European Microwave Conference, pp. 1452–1455, 2014.*

A. Appendix on Epi GFET

The measurement and modeling results of Appendix A concerns a dual gate epitaxial GFET (Epi GFET) with 170nm gate length, 12µm gate width and 0.6µm drain-to-source separation. Epitaxial graphene of the channel was synthesized on the Si face of a semi-insulating SiC substrate. The gate oxide is a high-κ dielectric Al_2O_3 of 10nm thickness deposited by atomic layer deposition.

- **I-V Measurements**

Fig A-1 shows the DC measurements of I-V transfer characteristics along with extracted trans-conductance G_m and drain-to-source conductance G_{ds} for *Vgs* varying from -4 to 3V and *Vds* varying from 0 to 3V. The Dirac point is located at far negative gate voltage demonstrating the n-type doping of the device.

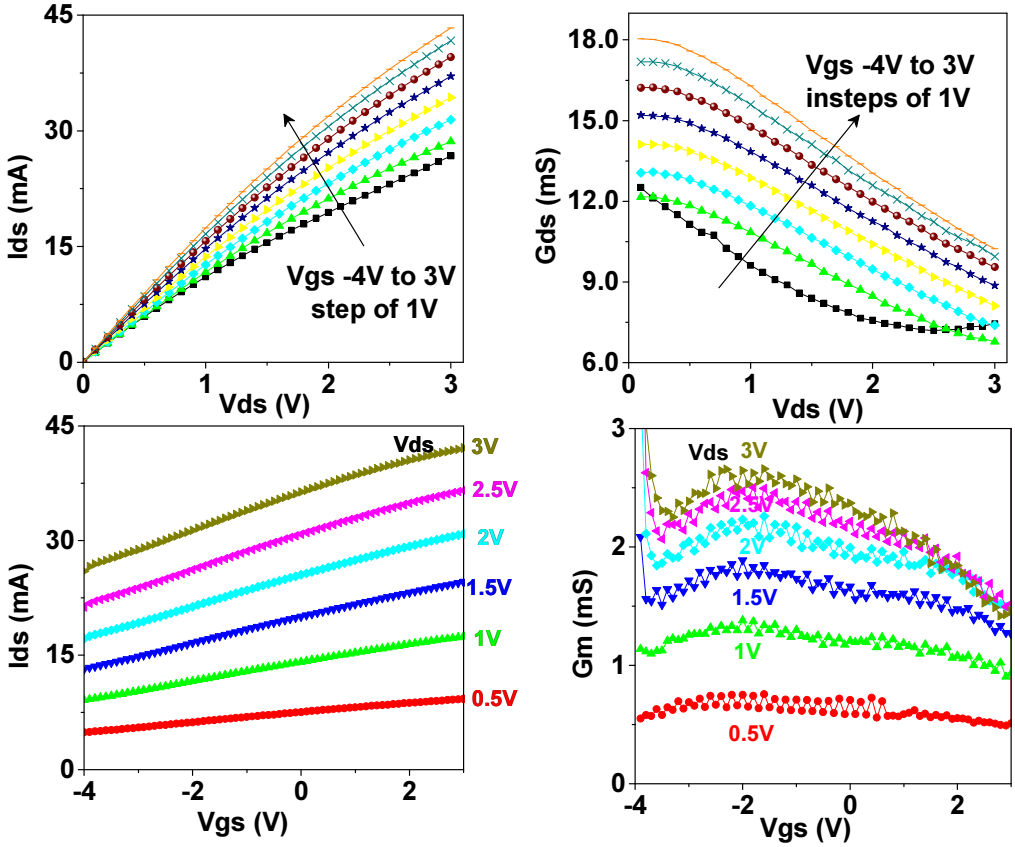


Fig A-1: DC measurements of (Ids-Vds), (Ids-Vgs), (Gds-Vds) and (Gm-Vgs) transfer characteristics for the Epi GFET (Lg=170nm, W= 12µm, Lsd=0.6µm).

The same I-V measurements were performed during multi-bias S-parameter measurements and are compared with a polynomial current equation in Fig A-2. The standalone DC I-V measurements and multi-bias S-parameter I-V measurements were identical, which demonstrates a stable behavior of this device under repetitive characterizations.

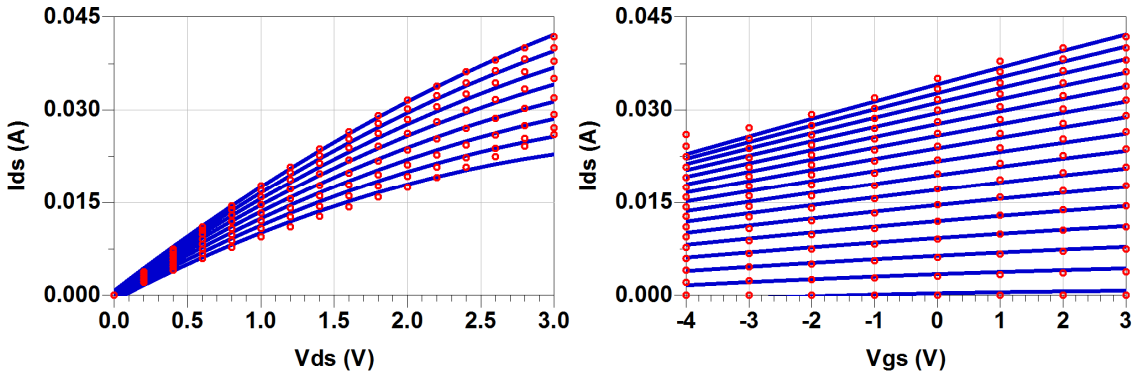


Fig A-2: Comparison between measured and modeled (IDS-VDS) and (IDS-VGS) transfer characteristics for the dual-gate Epi GFET (Lg=170nm, LSD=0.6µm, W=12µm).

- **S-parameter measurements and modeling results:**

From high-frequency S-parameter measurements of on-chip de-embedding structures and GFET devices, the equivalent circuit model of the GFET have been extracted following the modeling process described in section III.6.2. The extracted model parameters of the GFET are listed in Table A-1. Over the frequency range 0.5-35 GHz, the Fig A-3 compares multi-bias S-parameter measurements and simulations of the Epi GFET using the linear model elements associated with the polynomial nonlinear current source for V_{gs} varying from -4 to 3V in steps of 1V and V_{ds} varying from 0 to 3V in steps of 0.2V.

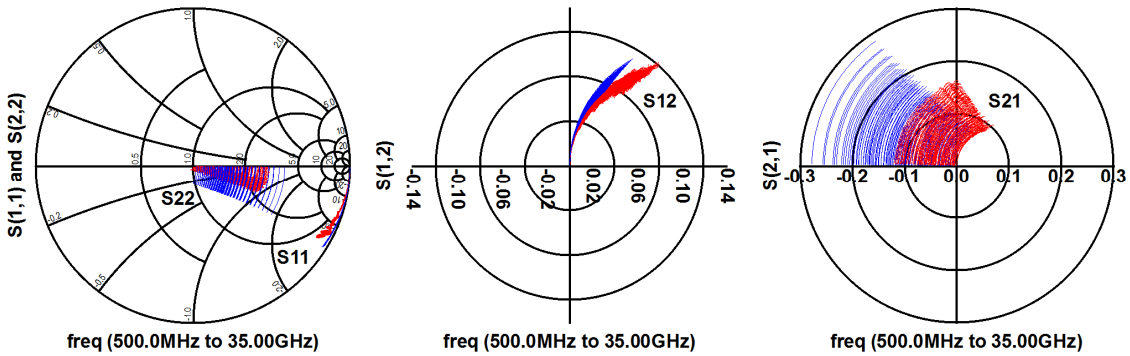


Fig A-3: Comparison of simulated (blue) and measured (red) multi-bias S-parameters over the [1-35] GHz frequency band for Epi GFET (Lg=170nm, LSD=0.6µm and, W=12µm).

PAD Capacitances			**Extrinsic elements**								
			GATE			**DRAIN**				**SOURCE**	
C_{PAD1} (fF)	C_{PAD2} (fF)	C_{PAD3} (fF)	R_G (Ω)	L_G (pH)	C_{PG} (fF)	C_{PDG} (fF)	R_D (Ω)	L_D (pH)	C_{PD} (fF)	R_S (Ω)	L_S (pH)
9.2	1	7.8	1.5	35	5.7	2.9	5	65	2.3	5	20

Intrinsic elements							
V_{DS}=3V, V_{GS}=-1V		C_{GS} (fF)	R_i (Ω)	C_{GD} (fF)	R_{GD} (Ω)	C_{DS} (fF)	T_{au} (psec)
g_M (mS)	G_{DS} (mS)						
1.6	9	3.87	85	3	152	7.5	0.1

Table A-1: Extracted Parameters at (Vds=3V, Vgs=-1V) of the dual-gate Epi GFET.

The measured and simulated S-parameters over the 0.5-35 GHz band are compared in Fig A-5(a) at 3V of *Vds* and -1V of *Vgs*. The extrinsic and intrinsic current gains deduced from measured and de-embedded S-parameters are shown in Fig A-5(b) demonstrating an intrinsic transit frequency of 38.5 GHz.

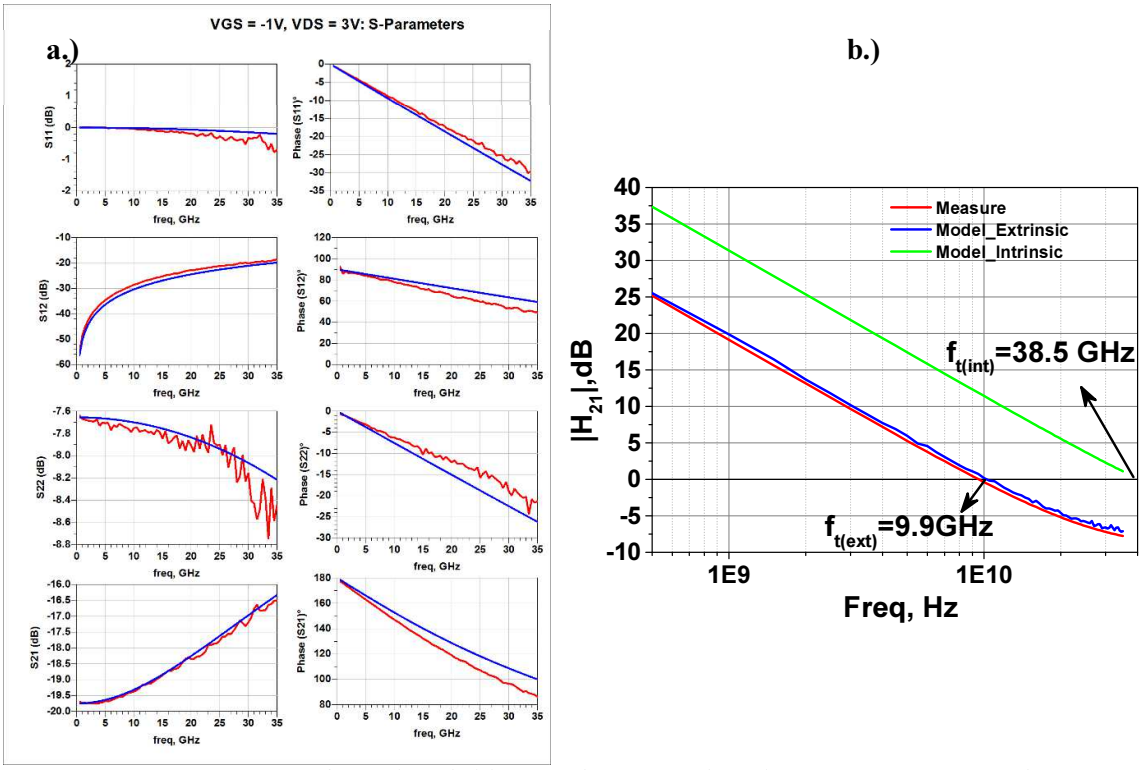


Fig A-4: a.) Comparison of simulated (blue) and measured (red) S-parameters at (Vds= 3V, Vgs=-1V), b.) Measured vs simulated transit frequency ft of the dual-gate Epi GFET.

B. Appendix on CVD GFET

The measurement and modeling results of Appendix B concerns a dual gate CVD-grown graphene FET (CVD GFET) with 200nm gate length, 12µm gate width and 0.7µm drain-to-source separation. CVD-grown graphene on Cu was transferred on Si/SiO_2 substrate. The gate oxide is a high-κ dielectric Al_2O_3 of 3nm thickness.

- **I-V measurements**

Fig B-1 shows the DC measurements of I-V transfer characteristics along with extracted trans-conductance G_m and drain-to-source conductance G_{ds} for *Vgs* varying from -1 to 1V and *Vds* varying from 0 to 1V. The Dirac point is located at a positive gate voltage of ~0.5-1 V demonstrating the p-type doping of the device.

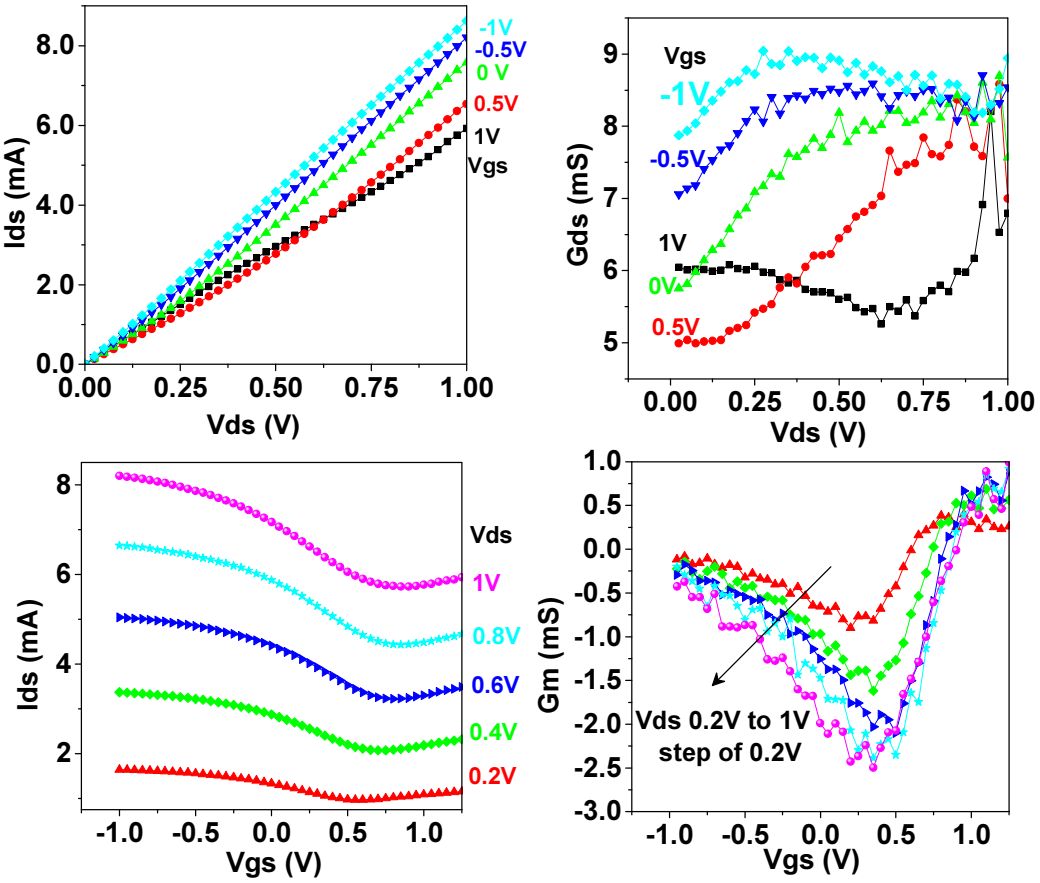


Fig B-1: DC measurements of (I_{ds}-V_{ds}), (I_{ds}-V_{gs}), (G_{ds}-V_{ds}) and (G_m-V_{gs}) transfer characteristics for the CVD GFET (Lg=200nm, W= 12µm, Lsd=0.7µm)

The same I-V measurements were performed during multi-bias S-parameter measurements and are compared with a polynomial current equation in Fig B-2. When comparing the standalone DC I-V measurements of Fig B-1 and multi-bias S-parameter I-V measurements of Fig B-2, the Dirac point cannot be observed in Fig B-2 as it was the case in Fig B-1. This is likely related to repetitive measurement timings that lead to a shift of the Dirac point.

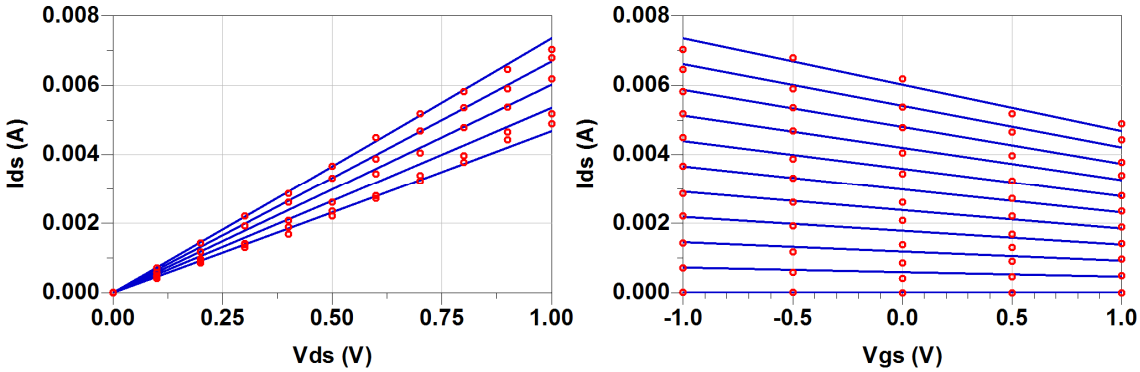


Fig B-2: Comparison between measured and modeled (I_{DS}-V_{DS}) and (I_{DS}-V_{GS}) transfer characteristics for the CVD GFET (Lg=200nm, W= 12µm, Lsd=0.7µm).

- **S-parameter measurements and modeling results:**

From high-frequency S-parameter measurements of on-chip de-embedding structures and CVD GFET devices, the equivalent circuit model of the CVD GFET have been extracted following the modeling process described in section III.6.2. The extracted model parameters of the CVD GFET are listed in Table B-1. Over the frequency range 0.5-35 GHz, the Fig B-3 compares multi-bias S-parameter measurements and simulations of the CVD GFET using the linear model elements associated with a polynomial nonlinear current source for V_{gs} varying from -1 to 1V in steps of 0.5V and V_{ds} varying from 0 to 1V in steps of 0.1V.

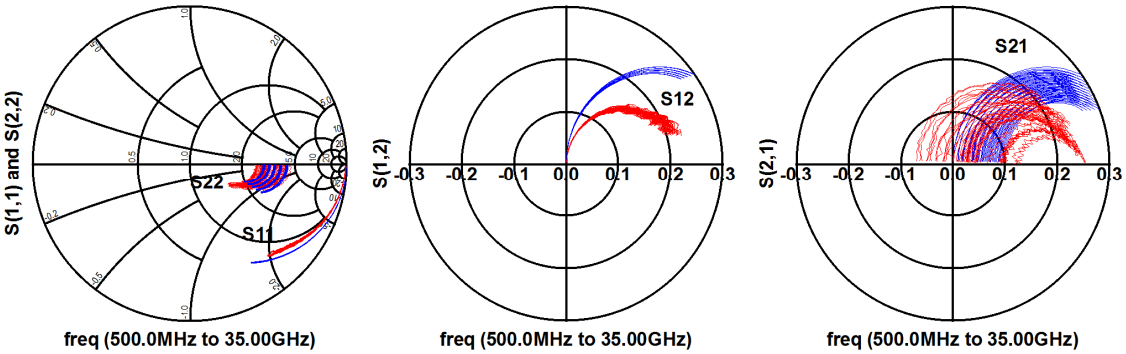


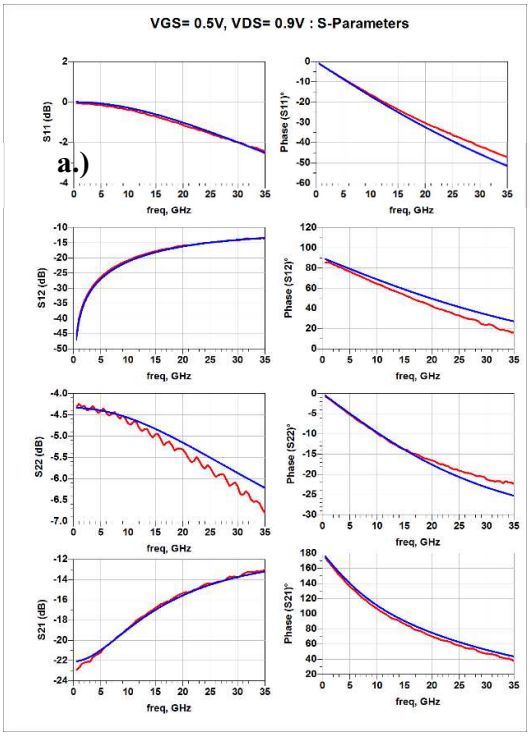
Fig B-3: Comparison of simulated (blue) and measured (red) multi-bias S-parameters of over the [1-35] GHz frequency band for CVD G-FET L_g=200nm, L_{SD}=0.7µm and, W=12µm.

PAD Capacitances			**Extrinsic elements**								
			GATE			**DRAIN**				**SOURCE**	
C_{PAD1} (fF)	C_{PAD2} (fF)	C_{PAD3} (fF)	R_G (Ω)	L_G (pH)	C_{PG} (fF)	C_{PDG} (fF)	R_D (Ω)	L_D (pH)	C_{PD} (fF)	R_S (Ω)	L_S (pH)
9.1	1	9.2	1.3	40	1.1	2.6	2	85	1.2	2	30

Intrinsic elements							
V_{DS}=0.9V, V_{GS}=0.5V		C_{GS} (fF)	R_i (Ω)	C_{GD} (fF)	R_{GD} (Ω)	C_{DS} (fF)	T_{au} (psec)
g_M (mS)	G_{DS} (mS)						
1	5	19.7	65	14.3	204	0.1	0.1

Table B-1: Extracted Parameters at (Vds=0.9V, Vgs=0.5V) of the CVD GFET.

The measured and simulated S-parameters over the 0.5-35 GHz band are compared in Fig B-5(a) at 0.9V of *Vds* and 0.5V of *Vgs*. The extrinsic and intrinsic current gains deduced from measured and de-embedded S-parameters are shown in Fig B-5(b) demonstrating an intrinsic transit frequency of 5 GHz.



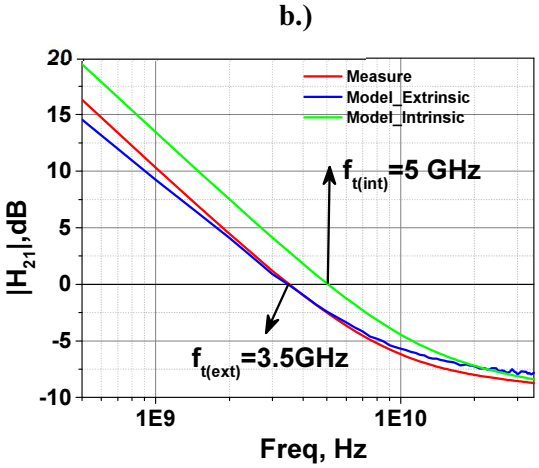


Fig B-4: a.) Comparison of simulated (blue) vs measured (red) S-parameters at (Vds = 0.9V, Vgs=0.5V), b.) Measured vs simulated transit frequency ft of the CVD GFET.

Pulsed I-V and RF characterization and modeling of AlGaN/GaN HEMTs and Graphene FETs

SUMMARY

The aim of this work is to assess the potentialities of Graphene Field Effect Transistors (G-FET) as well as to put in evidence dispersive effects of AlGaN/GaN High Electron Mobility Transistors (HEMTs). The main experimental results of this study have been obtained through the development of an advanced characterization set-up.

The main objective for characterization of AlGaN/GaN HEMTs was to develop innovative characterization techniques such as very short pulses and electrical history measurements. Dedicated time-domain pulsed I-V measurements have been performed in order to characterize and model the time dependent trapping phenomena in such devices. The current collapse (Kink effect) and drain lag are directly related to quiescent and instantaneous bias points as well as thermal effects which play a prominent role. This method provides an efficient way to assess the different thermal and trapping time constants for the nonlinear modeling.

The second aspect of this research work was the characterization of several graphene-based devices in order to assess the potentialities of such transistors and to derive a nonlinear device model. DC and high frequency characterization were performed. Specific test structures fabricated for accurate de-embedding at high frequencies along with the nonlinear model extraction were detailed in this work. This electrical model consistency has been checked through the comparison of measured and simulated multi-bias S-parameters. For this new material with outstanding electrical properties and promising capabilities, material and technological process are still subject to intensive research activities to improve high frequency graphene FET performances.

Keywords: *GaN, Graphene, HEMT, GNR-FET, G-FET, Pulsed I-V characterization, HF characterization, Trapping effects, Modeling.*

RÉSUMÉ

Ces travaux de recherche se rapportent à l'évaluation des potentialités des transistors à base de graphène ainsi que la mise en évidence des effets dispersifs sur les transistors HEMTs en technologie Nitrure de Gallium. Les principaux résultats issus de ces travaux sont obtenus suite au développement d'un banc de caractérisation spécifique.

L'objectif principal pour la caractérisation des transistors en technologie AlGaN/GaN a été de développer des techniques innovantes de caractérisation. Des mesures IV et RF impulsionnelles ont été réalisées afin de caractériser et modéliser les phénomènes de pièges. Cette méthode fournit un moyen efficace d'évaluer les constantes de temps thermiques et de pièges pour la modélisation non linéaire. Ces mesures illustrent ainsi l'impact des effets de pièges sur le comportement dynamique grand signal des transistors GaN.

Le second aspect de ces travaux de recherche est axé sur la caractérisation de différents composants à base de graphène afin d'extraire un modèle non linéaire. Des caractérisations DC et HF ont été réalisées. Des structures spécifiques de test ont été fabriquées pour la technique de « de-embedding » permettant l'extraction du modèle non linéaire. La cohérence du modèle électrique a été vérifiée via une comparaison des paramètres S mesurés et simulés. Il est primordial de construire des modèles performants prenant en compte les nouvelles caractéristiques de ces dispositifs dans le but d'établir un lien fort entre les aspects technologiques et systèmes afin d'améliorer les performances HF des transistors à base de graphène.