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Characterization and modeling of devices and amplifier circuits at millimeter wave band

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“When you can measure what you are speaking about, and express it in numbers, you know something about it; but when you cannot measure it, when you cannot express it in numbers, your knowledge is of a meager and unsatisfactory kind”

Lord Kelvin, 1883

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Abstract

Interest in millimeter-wave device characterization and modeling is growing rapidly as numerous radio frequency (RF) applications are migrating to higher frequencies. In particular, the electrical characterization needs a large number of steps to extract the device characteristics such as measurement, de-embedding, extraction and curve fitting. However, the successful implementation of the accurate models depends on how researchers resolve the new set of challenges and constraints associated to these steps. To address some of these challenges, I present my work on the characterization and modeling of RF models at millimeter-wave band.

In this regard, I looked more closely at some of the important limitations caused by the increase of frequency from device and circuit points of view. The goal is the investigation of two approaches for on-wafer measurements of individual device (device level) and on-wafer measurements of the same device in a basic circuit (circuit level). The approach of characterizing at device level is based on the standard characterization method previously developed by NXP modeling engineers. I have brought improvements in parameters extraction by optimization of the test structures. The approach of characterizing at circuit level is based on a new method to extract the small signal equivalent circuit using matching networks in characterization test structures. This method proposed here makes the DUT impedances carefully match the characteristic impedances of the measurement equipment. The matching network parasitics are included in the de-embedding test structures (dummies) and are eliminated by the conventional de-embedding steps. In results, the transmission of the signal from the source to the DUT is increased while the parameters extraction accuracy is improved. The developed method allowss the BiCMOS 0.25μm compact models validation at circuit level in mm-Wave band and provides accurate parameter extraction in a narrow band.

The developed method is implemented and verified on two MOS test modules and two bipolar test modules both fabricated in BiCMOS 0.25 technology of NXP Semiconductors. The measurements are carried out up to 50GHz and 110GHz, for respectively MOS and bipolar modules. The verification results demonstrated that the new test structure significantly outperformed the conventional method in measurement accuracy specifically in very high frequency (30 GHz for MOS structures and 60/95GHz for bipolar structures). It was also demonstrated that the conventional method accuracy can be increased by optimization of the test structures (example for the small single loop inductors characterization).

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List of symbols

BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BJT	Bipolar Junction Transistor
BSIM	Berkeley Short-Channel IGFET Model
CMC	Compact Model Council
CMOS	Complementary Metal Oxide Semiconductor
CPW	CoPlanar Waveguide
DUT	Device Under Test
GSG	Ground Signal Ground
HCI	Hot Carrier Injection
ICCAP	Integrated Circuit Characterization and Analysis Program
ISS	Impedance Standard Substrate
LNA	Low Noise Amplifier
LRRM	Line-Reflect-Reflect-Match
MEMS	Micro-Electro-Mechanical-Systems
MEXTRAM	Most EXquisite TRAnsistor Model
mm-wave	Millimeter wave
MPW	Multi Project Wafer
NBTI	Negative-Bias Temperature Instability
NF	Noise Figure
pCells	Parameterized Cells
PSP	Penn State Philips
Qubic	QUality BIpolar Cmos
S-parameters	Scattering parameters
SOLT	Short-Open-Line-Thru
SMTA	Smart Matched Test Structure
SSC	Small Signal Characterization
TDDB	Time Dependent Dielectric Breakdown

TRM	Thru-Reflect-Line
VNA	Vector Network Analyzer

Chapter 1: An introduction to millimeter wave characterization and modeling

Chapter 1 An introduction to millimeter wave characterization and modeling

1.1. Challenges for RF applications in the millimeter wave band

Semiconductors have been used for millimeter-waves since the 1970s. As silicon process technology continue to progress, analog, digital, and mixed analog/digital radiofrequency applications, became very proactive for semiconductor commercial industry success. These applications are an integral part of telecommunication applications (automotive radar, high speed wireless communication, passive and active imaging systems, and fast measurement equipments, etc) including market and services, progressing in a spectacular manner. Operating at millimeter-wave frequencies [30-300GHz] can promise a lot of interest such as, acquiring additional spectrum with larger bandwidth allocations, mitigation of the electromagnetic spectrum that saturates gradually, high data rate communication, and accommodate new applications.

Figure 1 : Evolution of RF applications in the electromagnetic spectrum

The millimeter-wave band is one of the innovative solutions that have surfaced to increase spectrum usage efficiency. Figure 1 summarizes the evolution of some RF applications in the electromagnetic spectrum. The possibility of using CMOS technology for high frequency generate a lot of interest in automotive radar [22-29GHz], license free band [59-66GHz], automotive collision radar [77GHz],

autonomous cruise control [94GHz], and non-ionic imaging [100-300GHz]. The evolution of these RF applications comes thanks to the evolution of advanced technologies. New technologies offer several advantageous options for application specifics. For example, a better radiation resistance is obtained using the SOI technology (Silicon On Insulator), a high electron mobility of transistors and low-loss substrate can be obtained by using the GaAs technology (Gallium Arsenide), a significant output power delivered using the GaN technology (Gallium nitride), and a moderate cost is obtained with SiGe technology (Silicon Germanium).

The silicon germanium (SiGe) process is also one of a silicon process suitable for high frequency circuits allowing fabrication of high frequency bipolar junction transistors. Recent Micro-electro-mechanical-systems (MEMS) processing enables high quality devices desirable for analog circuits. BiCMOS technology for RF purposes allows designing of mixed signal applications. This refers to the standard process technology for which analog circuits such as amplifiers and mixers are built. The key driver is the cost reduction from CMOS-bipolar integration in the same chip, as we bear in mind that reduced cost was the main driver in using silicon technology for RF in the first place. BiCMOS technology combines the bipolar and CMOS devices in the same chip, the bipolar transistor offers the circuit designers additional speed and current drive capability, while the CMOS devices continue to provide the high density, low power consumption, and low costs. Recent developments in BiCMOS increased the transition frequency (f_T) to achieve values of 350GHz. Such transistors allow BiCMOS technologies to be used for circuits in mm-wave band.

In the current version of the International Technology Roadmap for Semiconductors (ITRSs), the scaling of the metal-oxide-semiconductor field-effect transistor (MOSFET) is projected to the year 2016 when the channel length should be 16nm as shown in Figure 1 [1]. Progressive development in the process

of fabricating transistors with reduced surface contributed to a wider use of advanced technologies. Such developments allow CMOS technologies to be used for mm-wave band applications.

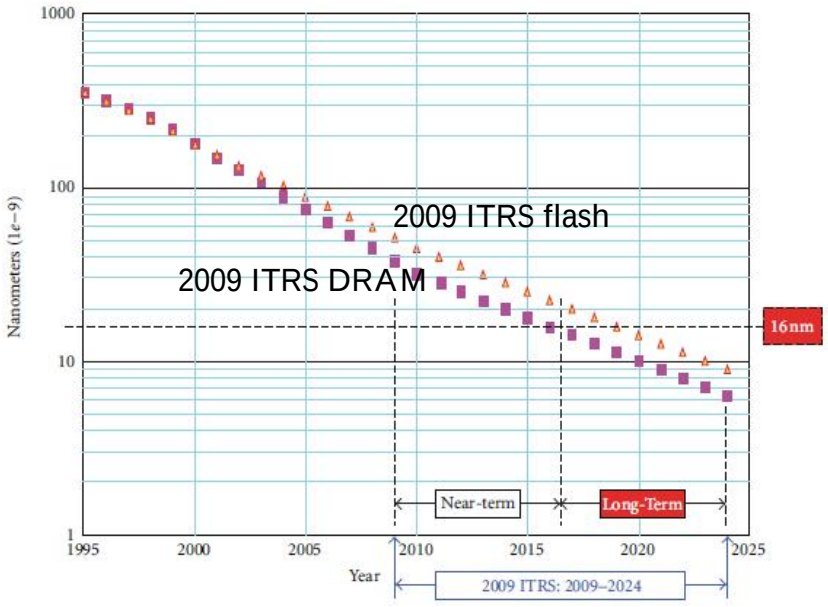

Figure 2 : ITRS prediction [1], the scaling of the MOSFET

However, CMOS technologies in mm-wave ranges, has some associated difficulties. Scaling requirements demand a lower supply voltage which restricts the use of certain conventional circuit topologies. In literature, to design applications in mm-wave range, the improvement of fabrication technologies, the characterization, and the design techniques are the goal of multiple research activities. The characterization and design techniques are the focus of this dissertation. The electrical characterization discussed in this thesis includes measurement and extraction of the device characteristics in order to obtain the parameters of device models. A large number of steps are needed to extract device parameters such as measurements, de-embedding, extraction and curve fitting [2-6]. In the case of analog circuits, several iterations are also required to meet the specifications, because they face some difficulties related to design complexity associated to some device characterization and measurement

limitations [2], [3-4], [7-12]. Therefore, it is important to have appropriate techniques to reach the best accuracy in parameter extractions, models validations, and design cycles.

1.2. BiCMOS 0.25µm advanced-high speed technology

The technology used for these studies is the NXP Semiconductors Qubic4Xi technology. The QubiC (Quality Bipolar CMOS) process features a rich set of devices for high frequency mixed-signal designs. It consists of a BiCMOS 0.25µm process with a transition frequency (f_T) of a NPN bipolar transistor of 180GHz. The BiCMOS technology combines the manufacturing of bipolar and CMOS devices on the same chip for mixed, digital, and analog circuits. The bipolar transistor offers the speed of circuits, while the CMOS devices ensure the low power consumption [13].

The NXP semiconductors' BiCMOS technology is an advanced high-speed technology, characterized by high resistivity silicon substrates to overcome the parasitic substrate effects, thicker metallization and stacked of multiple metal layers to reduce the conductor dissipation. The Qubic4Xi is an enhancement of the Qubic4X version dedicated to micro-wave applications. The QUBiC4Xi is specifically designed to meet the needs for high frequency applications in the wireless, broadband communications, networking and multimedia markets. With multiple process nodes available, QUBiC4Xi allows optimal technology selection based on functionality, integration, and performance requirements. It contains up to 5 metal layers, in which the highest is about 3 microns thick. These features allow preferment inductors manufacturing (quality factor more then 20 for 500pH inductors). The metal 6 is about 3 microns and metal 5 is about 2 microns thick. The Qubic4XI layer thicknesses and dielectric constants "back-end" is shown in Figure 3. The highest metals are thicker and less resistive (metal 5 and metal 6) to reduce the conductor dissipation.

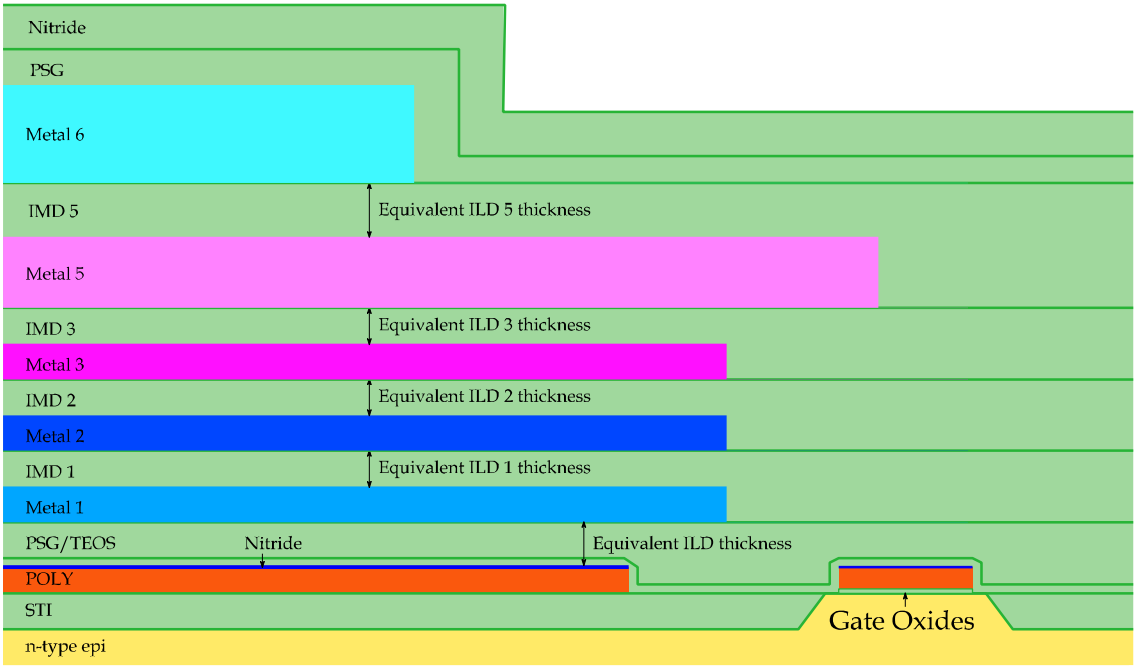

Figure 3 : Qubic4Xi layer thicknesses and dielectric constants «Back-end»

The bipolar transistors are optimized for either ultra-high-speed or high-voltage-robustness. Both devices show excellent RF and low power performances. The sectional view of the NPN transistor is shown in figure 4 [13]. The basic architecture is similar to the original concept [14]. For this generation emphasis was placed on the base link region, the emitter-base spacer in particular as shown below.

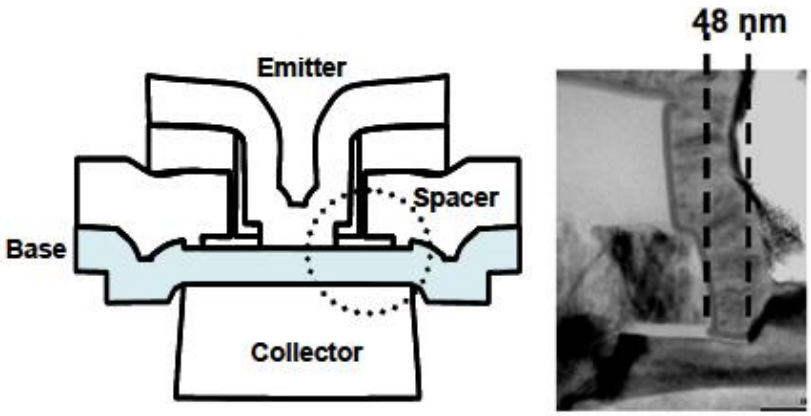

Figure 4 : Schematic cross section of the NPN device [13]

BiCMOS technologies provide the best performance/cost. The validation is performed with characterizations based on available model measurements. Compact models for BiCMOS technology are used in NXP semiconductors to simulate the high frequency behavior of the library components.

1.3. Challenges for RF characterization of advanced devices

In the Semiconductor industry, the shrinking line widths, scalable device sizes and the requirement for higher frequency operation have put more and more pressure on accurate device characterization [2-4]. The demand in RF applications emphasizes the need for accurate and valid models, since any application at high frequency is only as good as its models. For the last decade, the mm-wave band has attracted more and more attention of RF field researchers and has presented a particular interest for countless telecommunication applications (automotive radar, high speed wireless communication, medical imaging systems, etc). This frequency band has become increasingly attractive for multiple reasons such as the electromagnetic spectrum saturation (frequencies < 30GHz), and the emergence of systems that require wide frequency bands which simply are not available in the frequency band below to 30GHz.

Today, obtaining accurate device measurements at mm-wave frequency becomes the major challenge for the modeling engineers while characterizing models at these frequencies [4], [7-8]. Several compact models have already been developed for digital, analog, and RF applications [5-6]. These compact models (ex. BSIM, PSP, MEXTRAM etc.) available in design kit libraries are recurrently characterized up to a few tens of gigahertz [7]. The characterization procedures have inaccurate at higher frequencies for multiple reasons. In literature, we can find several de-embedding techniques [5], [7], [10]. The impact of the unwanted parasitics on device characterization is substantially reduced after subtracting them, but the equivalent-circuit methods may not work well, and the accuracy of

the device under test (DUT) characteristics is always insufficient [6], [8]. As it is known also at high frequencies, parasitics from the probe pads and interconnections have significant impacts on the RF on-wafer measurements [10]. Indeed, the test structure parasitics, the inaccuracy of test equipments, and the effects of measurement environment, always let the measurement accuracy still an extreme concern for device characterization of both passive and active components. All this creates discrepancies between the foundry models and the measurements [4], [7-8].

Standard test structure is composed of probe pads, input and output interconnections, and intrinsic device. The input and output interconnections are removed from the raw measurements by de-embedding. The device characteristics are measured in a large band (e.g. up to 50GHz or 110GHz). However, at higher frequencies (in mm-wave range), the devices (e.g. MOS transistors) lead to measurement inaccuracies due to an important measurement attenuation signal and due to low input and output impedances when the device is connected in common source configuration [11-12].

In this context, this research work focuses on developing appropriate methodologies to overcome these mm-wave limitations and to initiate a novel characterization method at circuit level. As known at these frequencies, special care must be taken for such a characterization in order to avoid measurement and de-embedding errors, and in order to take account of these effects in the device characterization. At the same time, to save time in measurement. The attempt is to find a solution through a constructive investigation of the circuit level layout and model. This involves compact model verifications and validations, small signal characterization, and test structure improvements [11-12].

1.4. State of the art models

The specifications of accuracy of compact models are becoming more restrictive as circuit operating frequencies increase and when the device sizes continue to scale down with concomitant increase of chip density of analog and mixed-signal circuits. The increase of accuracy in modeling of intrinsic passive and active devices becomes an important topic to extend the models validity at mm-wave frequencies and requires the modeling of the backend series resistive and inductive parasitics, and of parallel parasitic capacitances [4].

The compact models are defined as a generic set of equations describing the physical behavior of a device [5-6]. These equations are based on a set of parameters extracted from measurements after curve fitting, scaling or direct calculation. Apart from extracted parameters, a compact model contains indirect parameters related to their use in advanced circuit simulators [15] for correctness, smoothing etc. A general-purpose state-of-the-art compact model of active devices consists of about 300–400 equations and 150–400 parameters containing physical information about the device (e.g., oxide thickness and doping level) and compensating for the simplified description of the physical of semiconductor devices [16].

Previously in electronics, simple voltage and current equations could be sufficient to describe the precision of a device behavior. Nowadays, the evolution of the modern circuits is driven by product cost which is obtained by size reduction. The size scaling lead to complicate characterization and modeling, and this complexity challenges the compact model to describe all the operation regions of the device with an acceptable accuracy more than ever before. The accuracy requires the models to take into account different types of effects related to small geometries, such as passive / active connection complexity, measurement errors, de-embedding errors, etc. In addition to this the models should cover the

high frequency operation region for devices used for designs operating in these regions [15].

The Berkeley Short-channel IGFET Model (BSIM) from the device group of the University of California at Berkeley [17] is an example broadly used model for transistor simulations. The BSIM4 is the extension of BSIM3 Model, ant it offers better smoothing in current derivative and discontinuities in the transition region between sub threshold and moderate inversion of the Ids–Vgs curve. The discontinuities which the older models (Berkeley Model 1, 2, and 3) failed to describe and corrected by the last version. However, for operating frequencies in mm-wave range, the standard BSIM model is not longer reliable.

One of the MOS models also widely used in industry is the MOS Model 11 which is an industry-based model, developed as the successor of MOS model 9 at Philips Research laboratories [18]. Several important physical effects have been included in this model, such as: mobility reduction, bias-dependent series-resistance, velocity saturation, drain-induced barrier lowering, static feedback, channel length modulation, self-heating, etc. The MOS model 11 is especially intended for analog and RF circuit design, because he describes accurately the electrical distortion behavior and gives an accurate description of the noise behavior of the MOSFETs. MOS Model 11 provides a model for the intrinsic transistor and the gate/source and gate/drain overlap regions. But in terms of extrinsic RC parasitics the MOS Model 11 doesn't take into account this features.

In 2005, the PSP (Penn State Philips) model was selected as the first surface-potential-based MO industry standard compact model by the compact model council (CMC). The channel surface potential expressed in terms of the terminal voltages. The PSP model is developed by Philips research laboratories and the Pennsylvania State University [16]. It was reviewed to get more accuracy with special emphasis to features of interest to digital, analog and RF designers [19].

Although the PSP compact model is reviewed and have a higher content of physical meaning, the curve-fitting techniques and careful selection of the model parameters extracted from measurements still play essential roles in the development of compact MOSFET models.

1.5. Characterization methods used in this study

In this section, the standard test structure characterization which concerns the single device characterization is discussed, and then the characterization at circuit level procedure is presented. After that a discussion on research and industry needs of high frequency valid models is introduced.

1.5.1. Standard test structure characterization

A typical Small-Signal Characterization (SSC) and modeling flow is shown in figure 5. The SSC flow is illustrated on the left side of the figure. The characterizations (S-parameter measurements) are made on RF test structures including the device under test and the probe pads using a Vector Network Analyzer (VNA). The parasitic contribution of probe pads is subtracted by de-embedding step and an equivalent circuit is extracted from the de-embedded S-parameters. On the right, is presented the model used for simulations making the interface between the technology (process) and the circuit application. This compact model is extracted from AC/DC measurements.

In mm-wave range the parameters of the equivalent circuit are sensitive to the robustness of test structure design, the accuracy of S-parameter measurements (compliancy with the HF signals), and equivalent circuit definition/distribution.

The test structure design can have an impact on the measurement accuracy of device under test due to parasitics of the connection between signal pad and the device under test, coupling between probe contact area and the boundary of the pad, the capacitance between S and G (e.g. associated dielectric loss), etc.

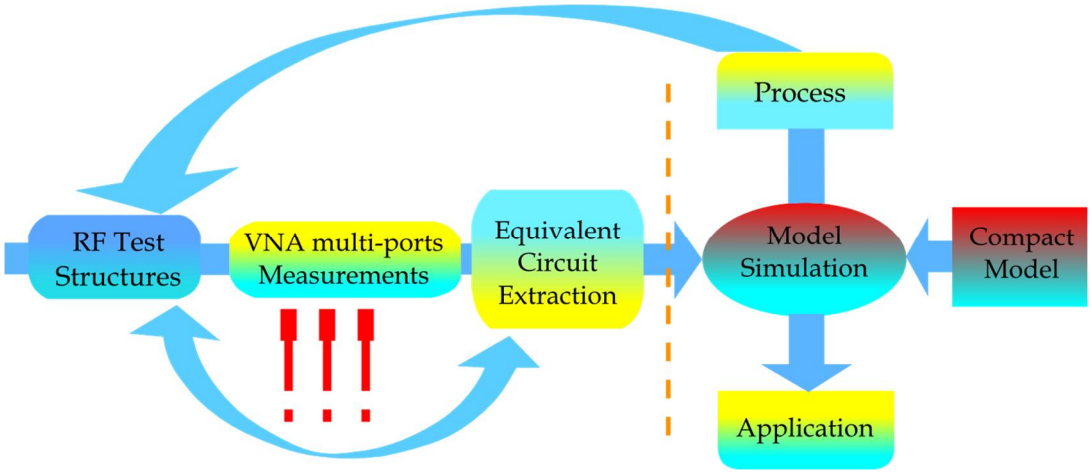

Figure 5 : RF characterization and modeling flow

The parasitics generates loss of measurement signal from the signal pad to the device under test. This loss is taken into account in de-embedding step. The de-embedding methodology and its associated dummies are also related to the design of the RF test structure and play an important role on measurement accuracy.

The accuracy of the S-parameter measurements can be affected by the VNA calibration and by bad contacts between probes and on-silicon pads. Very high or very low impedances of devices under test (compared to the 50 Ohms characteristic impedance of VNA) push the instrument to lower accuracy [11-12].

The definition / distribution of the equivalent circuit is not in agreement with the architecture of the device or with the physical mechanisms which define its operation. As example, at high frequency the gate losses can be only modeled when the gate capacitance and channel resistance are distributed in several segments (Non-Quasi-Static effect) [6-11], [20].

All these reasons can lead to specific mm-wave frequencies measurements inaccuracies. To illustrate an example of extracted parameter variations of a passive device, the quality factor of a small octagonal inductor (with an inner

diameter of 130µm, track width of 5µm) is shown in figure 6. It was extracted from measurements and simulated in Momentum simulator (EM simulator).

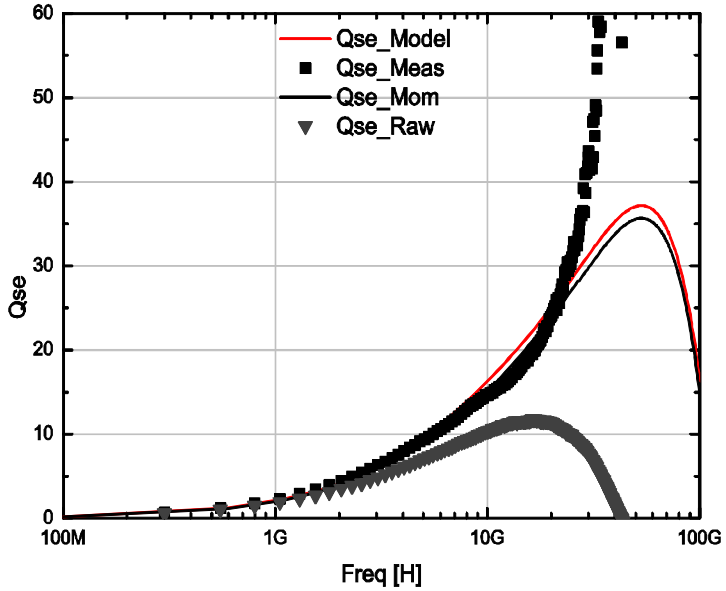

Figure 6 : Small octagonal inductor quality factor simulated and measured

The Q factor extracted from S-parameter measurements shows a remarkable deviation from the simulated Q factor starting from 30GHz after de-embedding. The raw measurements (without de-embedding) do not show this weird behavior after 30GHz. That proves the de-embedding step has a strong impact on extracted characteristics.

For active devices, a MOSFET 20µmx0.25µm transistor fabricated in BiCMOS0.25µm technology in this example, the parameters extracted from small signal measurements are based on equivalent circuits as illustrated in Figure 7. The equivalent circuit is composed of the extrinsic elements ($L_{g,d,s}$, $R_{g,d,s}$, and $C_{pg,dpd}$) and the intrinsic elements ($C_{gs,gd,ds}$, $R_{i,gd,ds}$, and g_m). Inaccurate equivalent circuit definition generates extraction variations as shown in figure 8 for reflection S22 parameter. The substrate network (R_{sub}, and C_{sub}) has been found as the root cause for such variations (discrepancies between simulations

and measurements) by [3]. The simulated real part output impedance differs from measured as shown in [3].

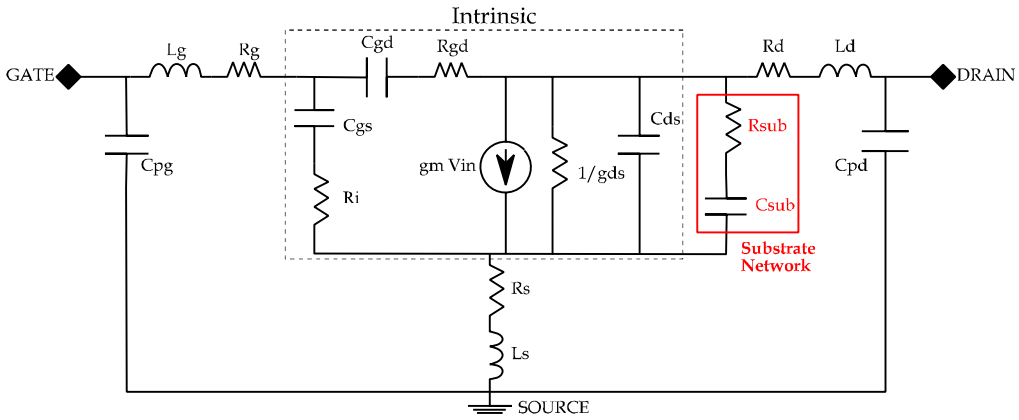

Figure 7 : MOSFET Small-signal equivalent circuit with substrate network

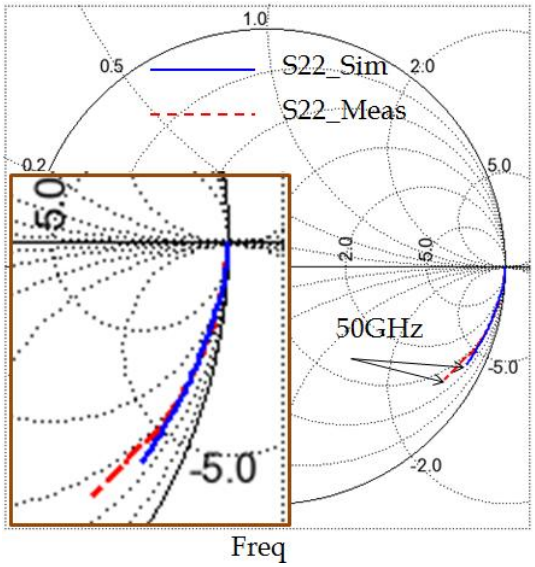

Figure 8 : Output impedance difference due to inaccurate substrate network

The substrate network added in the small signal equivalent circuit of the MOSFET allows to the equivalent circuit simulations to reproduce measurements over all frequency range. For those reasons, the investigation of improvements of de-embedding techniques and of dummy test structure design is required to overcome the influence of the high frequency effects, and obtain accurate broad band measurements.

1.5.2. Characterization at circuit level

As the small signal characterization of active devices is usually made in common source/emitter configuration, the device in its test structure can be seen as an amplifier. At mm-wave range, the characteristics of device under test (e.g. MOS transistors) which are sensitive to the robustness of test structure design, to the accuracy of S-parameter measurements, and to the equivalent circuit definition/distribution, become dominated by the test structure parasitics. This leads to signal attenuation transmitted from the probe tips to the DUT. Moreover, the input and output impedances of MOS devices connected in common source configuration are lower than to the VNA characteristic impedances. This is particularly true for small advanced technologies device [11-12].

To overcome these limitations, we propose a novel method for circuit level characterization, called, matched test structure architecture (SMTA). This method makes the DUT impedances carefully match to the characteristic impedances of the measurement equipment. The matching network parasitics are included in the de-embedding test structures (dummies) and are eliminated by the conventional de-embedding steps. The methodology is proposed in order to simplify measurements into a narrow band of interest and to save time in measurement.

The SMTA characterization approach can be summarized as follows; firstly this method improves the modeling at high frequencies by considering the extrinsic part of the device, for inductors, interconnect lines, and active devices. Secondly it improves the extraction precision. In figure 9, is shown the GSG test structure used for MOS transistor characterization. Figure 9 (a) shows the conventional test structure with simple interconnect lines and figure 9 (b) shows, the transistor under test pre-matched to 50 Ohms (impedance of measurement equipment). The matched test structure increases the transmission gain of the transistor in the

frequency band of interest [11-12] and then improves the modeling SSC extraction accuracy.

The matching of the transistor connected in GSG probe pads allows the extraction of parameters (e.g. C_{gs} and g_m for a MOS transistor). These parameters are the same in equivalent circuit given in figure 7. But they are extracted in a narrow band centered at higher frequency. Thus, the measurements provide results (e.g. a resonance frequency) that are a combination of the equivalent circuit parameter and of the matching network.

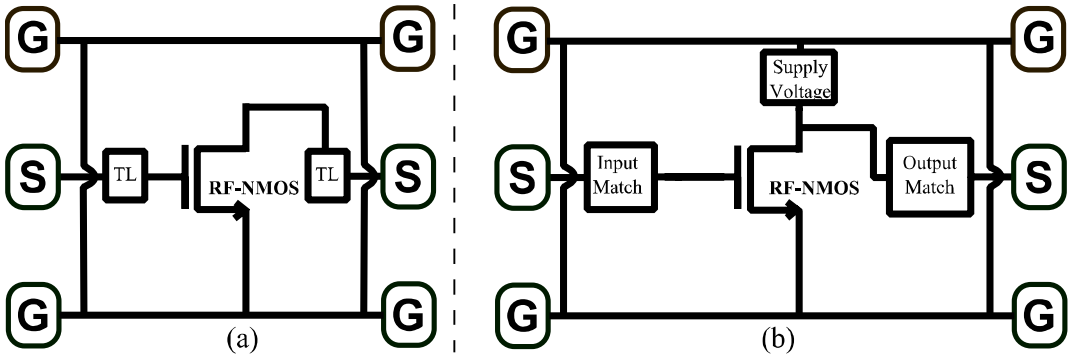

Figure 9 : (a) Schematic of conventional test structure, (b) Schematic of the matched test structure

This technique allows first, the measurements of devices in a reduced frequency band (e.g. mm-wave range), and secondly it allows the verification of the characteristics extracted by standard methodology (broad band measurements without 50Ω matching). The characteristics of active devices (MOS and Bipolar) but also of the passive components (inductors used in the matching network) can be extracted individually and validated at higher frequencies in a large band.

As an example, and like shown in figure 10, in the case of the common source SMTA MOS amplifier, all of the amplifier performances such as, input and output impedances and the low frequency gain are dependent on the SSC parameters of the transistor.

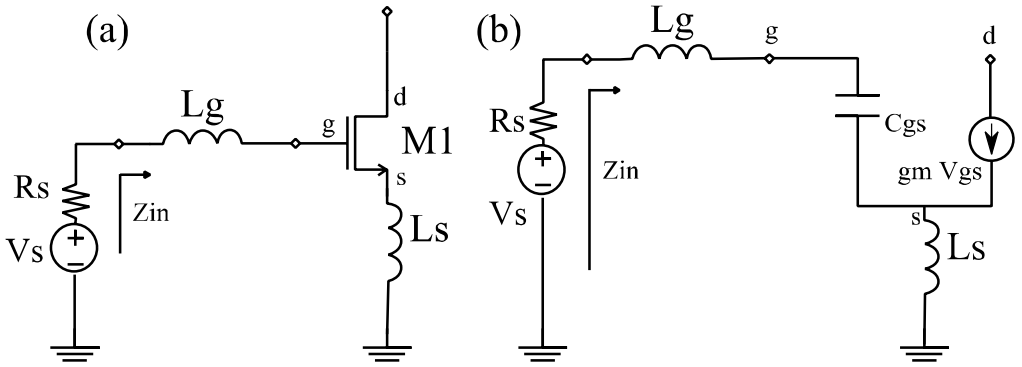

Figure 10 : RFMOS transistor matched with Lg & Ls (a), and small signal equivalent circuit (b)

In the SMTA, the input impedance Z_{in} of the MOS transistor represented in figure 10, with inductive source degeneration is given by:

$$Z_{in}(w) = R_{in} + jwC_{in} \tag{1.1}$$

$$Z_{in} = \frac{L_s g_m}{C_{gs}} + j\left((L_s + L_g)2\pi f_{c1} - \frac{1}{C_{gs}2\pi f_{c1}}\right) \tag{1.2}$$

Where, L_s is an inductance in series with MOS transistor source, and L_g is added in series with the gate. The input impedance Z_{in} depends on the input capacitance accuracy and the matching network which could be inductors or inductors and capacitors characterized in single mode characterization.

The low frequency gain is given approximately by:

$$A_v \approx \frac{g_m}{g_{ds}} \tag{1.3}$$

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \tag{1.4}$$

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}} \tag{1.5}$$

With an ideal behavior, $g_{ds} = 0$, the output impedance real part is approximately by:

$$R_{out} = \frac{1}{g_{ds}} \tag{1.6}$$

The matching network allows the matching of the low impedance of the device under test to be aligned to 50 Ohms of the VNA in a given bandwidth. The matched test structure allows by this the maximum transfer of signal, delivered from source to the device under test.

1.6. Research and industry needs for high-quality valid models

Semiconductor companies have made significant efforts during recent years to secure future availability of high-quality compact models. NXP Semiconductors make it through proprietary in-house developments and university research. By initiating and suggesting new topics to be included in models based on the most important needs identified by IC designers. As device size becomes smaller, device reliability due to degradation with operation time, as well as device variability due to process variations, the modeling process becomes increasingly hard.

Here are listed some of the topics NXP is doing to improve the accuracy of models:

- Matching modeling: Characterization of the pair devices to extract small electrical performance differences over a large group.
- Model reuse: DC model parameters are reused when model verification is realized in small signal equivalent circuit (eg. for MOS model).
- Verification of “Golden” active and passive devices using PCM (Process Control Module) measurements. Comparison of component simulations (nominal, corners) with the PCM measurement results is made in order to control the performance of the device with respect to the manufacturing specifications.
- Post-processing simulations are made obtainable by the use of the models of the PCM measurements. PDV (Process Design Variable) parameters are first extracted from PCM measurements. Through this transformation, the

modeling engineers and circuit designers are able to simulate their components or integrated circuits using the electrical characteristics of a wafer site for the wafer silicon or die (plural dice or dies).

- RF modeling: accurate gate resistance modeling (MOS devices; several types of gate resistances contribution are extracted over temperature); substrate network modeling (MOS transistors); non-quasi-static effects (resistance put in series with gate to source and gate to drain capacitances); etc
- Extraction of RLCk back-end parasitics: RLCk parasitic extractions are made for “layout view”.
- Noise and variability (1/f noise, thermal noise, layout-dependent effect)
- self-heating of devices
- Reliability models to include NBTI (Negative-bias Temperature Instability), HCI (Hot Carrier Injection), and TDDB (Time Dependent Dielectric Breakdown) effects.

1.7. Millimeter wave measurements and characterization

The characterization procedure allows model extraction and validation. Both depend on the accuracy of measurements (DC and small-signal measurements). Accurate measurement of devices provides correct circuit performance predictions [20], [21]. Hence, the interest of giving more attention for appropriate on-wafer measurements.

1.7.1. GSG test Structure

The size of devices (i.e. transistor) of an advanced high speed technology is just a few micrometers. The intrinsic devices (front-end) could not be contacted directly using RF probe pads. Moreover, up to the top of active devices, there are several layers of metallization (back-end). The GSG pad is defined as a probe pads on-wafer, the interconnect lines between the probe pads and the device under test (front-end) connected by the vias stack as is shown in figure 11. The

impact of these elements is subtracted by de-embedding from the high measurement frequencies and will be explained in the section 1.6.3. De-embedding is the next step after the calibration of the VNA. There are different methods with different complexities of de-embedding depending upon the measurement needs, the design of the DUT, model parameters to be extracted, and the frequency range. Different methods are used upon the device type: passives (inductors, capacitors, and resistors), and active devices (transistors, diodes, etc.).

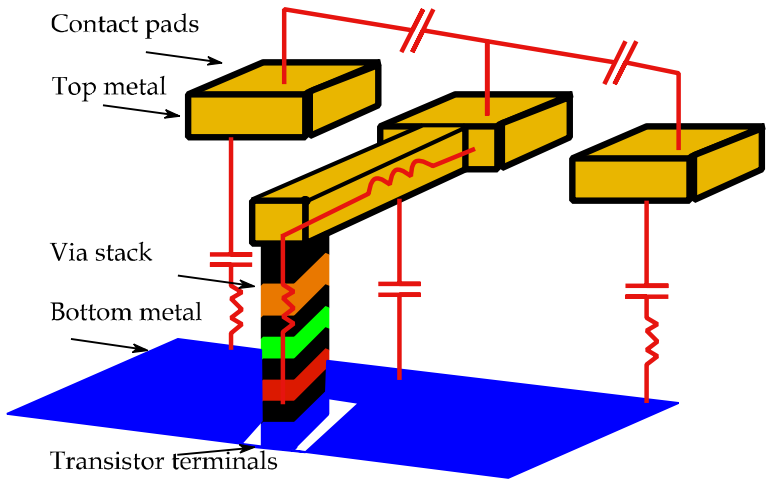

Figure 11 : An example of GSG pad with simplified representation of parasitic elements

1.7.2. Measurements platform

The measurement setup can be composed by on-wafer test structures and RF probe station. Both can have an impact on the device under test, and for a characterization of the intrinsic device an appropriate calibration and de-embedding procedures are required to extract the impact of measurements setup. In this study, measurements are made using the following platform:

1) Vector Network Analyzer (VNA). The VNA is used for measurement of S-parameters. The VNA measures the amplitude and the phase of two ports incident and reflected waves that are used to calculate the scattering

parameters (S-parameters) of the device under test (DUT) [22]. In our study, high frequency on-wafer measurements are carried out with an Agilent 8364B network analyzer (50GHz) and Agilent 8510C network analyzer (110GHz) with ground-signal-ground (GSG) probes.

2) RF probe station for maintaining the (8" inch) wafer under test and probe petitioners that sustain the GSG probe pads on each component [22]. The probes used are the GSG probe pads provided by Cascade Microtech with a pitch of respectively, 125µm (50GHz) and 100µm (110GHz).
3) ICCAP (Integrated Circuit Characterization and Analyses Program) is used for measurements, control, and data acquisition.

Measurement accuracy can be impacted by the network analyzer uncertainties such as the imperfections coming from each unit of the VNA, losses in cables, interconnects and probe pads, etc, known as the systematic errors. Error generated by the noise of the test equipments known as the random errors and the temperature variation errors known by the drift errors.

The accuracy of the measurements depends on the test equipments calibration techniques and on the procedure of removing the pad and metallization parasitic and moving the reference plane to the edge of the device under test (DUT) itself.

1.7.2.1. Calibration methods

The calibration method consists of a systematic, random, and drifts errors correction from the instrument hardware using standards made on alumina substrate (figure 12). These standards are certified, and allow measurements up to 50GHz and 110GHz depending on the VNA and probe tips used. This type of calibration allows moving the reference plane at the end of the probe tips, and the reference impedance is equal to the VNA impedance which is equal to 50Ω. The most common calibration methods that allow the correction of the first error

type (systematic, random, and drift errors) are: the SOLT (Short-Open-Load-Thru) [23], TRL (Thru-Reflect-Line) [24], LRM (Line-Reflect-Load) [24] and LRRM (Line-Reflect-Reflect-Match) [25]. In our study, on-wafer LRMM/SOLT calibration methods are used. The calibration standards are made on alumina substrate (ISS Impedance Substrate Standard).

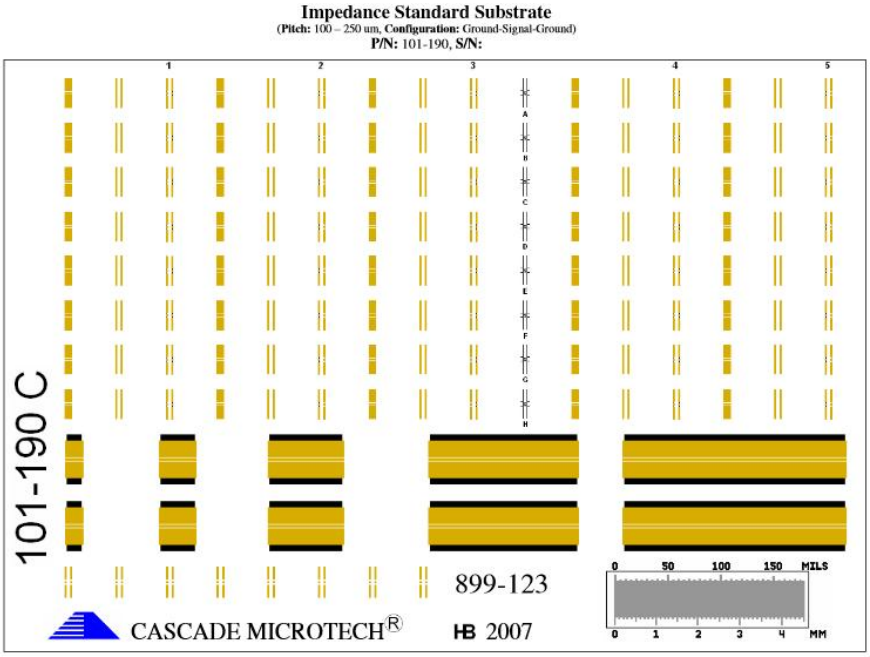

Figure 12 : Calibration substrate used for calibration

The reference planes are defined in tips probe plane by the calibration of the vector network analyzer (VNA). The network analyzer calibration kits include documentation indicating the accuracy of standards. The measurements of calibration standards are stored directly in the network analyzer memory and used for corrections. Figure 13 shows the typical platform used for measurements of the device under test and shows the calibration and de-embedding reference planes in S-parameters measured. An accurate subtraction of these parasitics requires a good understanding of calibration and de-embedding methods. The platform is composed by VNA, the probe station, cables, and wafer probes.

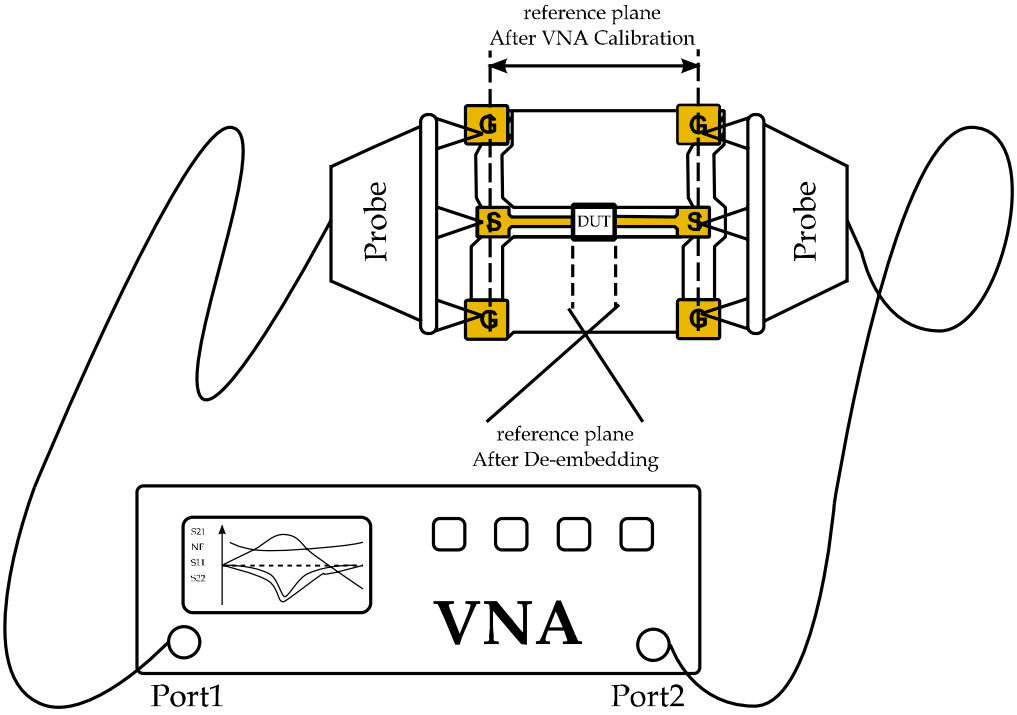

Figure 13 : Calibration and de-embedding reference planes in S-parameters measured

TRL (Thru- Reflect-Line)

In figure 14, are shown layouts of the TRL standard for calibration on a silicon-wafer. The standard is composed of a two CPW (CoPlanar Waveguide) lines (a and c) and a reflective device (b). The thru and the line have a characteristic impedance of a nearly 50Ω (Z_{LINE} = 50Ω), and the reflect standard can be an open or a short circuit.

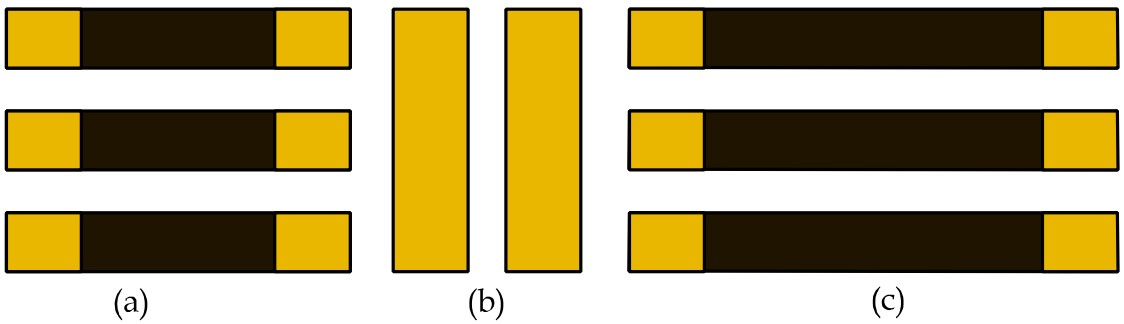

Figure 14 : Layout of calibration standard for TRL calibration: (a). thru, (b). reflect, and (c). line

The Thru line is described by the scattering matrix: $S_T = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}$. The reference plan is in the center of the line on condition that reflect standard is symmetrical. The calibration condition requires that the characteristic impedance of the thru line Z_{LINE} be fully matched with the reference impedance ($Z_{ref} = 50\Omega$), i. e. $S_{11} = S_{22} = 0$.

The Line of known length is characterized by the matrix: $S_L = \begin{pmatrix} 0 & e^{-\gamma L} \\ e^{-\gamma L} & 0 \end{pmatrix}$, where L is the difference between the physical length of the two lines. The line propagation constant (γ) is directly extracted by algorithm and the diagonal elements S_{11} and S_{22} equal to zero by definition, so then it is possible to move the reference planes along the line and the reference impedance equal to the reference impedance of the transmission line.

The reflect standard consists of a high reflection coefficient in each port. It can be an open or a short it's characterized by: $S_R = \begin{pmatrix} \Gamma & 0 \\ 0 & \Gamma \end{pmatrix}$.

SOLT (Short-Open-Line-Thru)

The SOLT calibration is perhaps the most common of all manual VNA calibration techniques. Figure 15 shows a simplified calibration substrate with short, open (open is performed by lifting the probe in air), line, and thru standards.

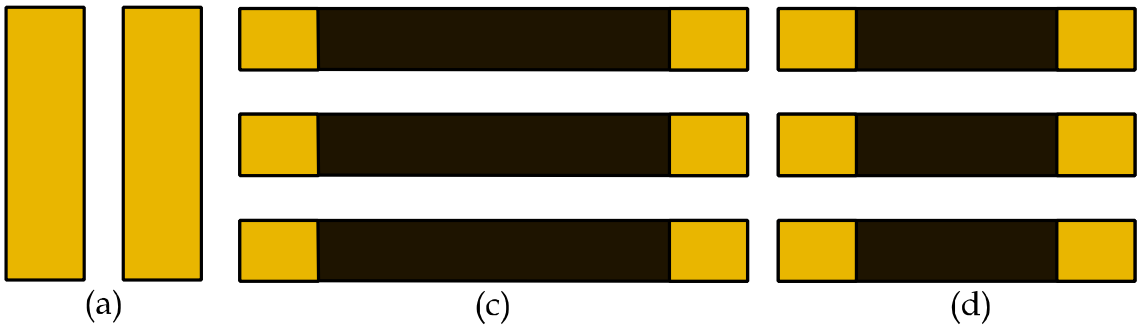

Figure 15 : Layout of calibration standard for SOLT calibration: (a). short or open, (b) line, and (c). thru

LRRM (Line-Reflect-Reflect-Match)

The LRRM method is based on four calibration standards: a thru line (a), two pure reactance pairs (b), and a pair of matches (c). The line standard and the resistance of the match standard need to be exactly known, the reactances of the match and lossless open and short standards are found using their raw-parameter measurement data [25]. Figure 16, depicts the corresponding test structures.

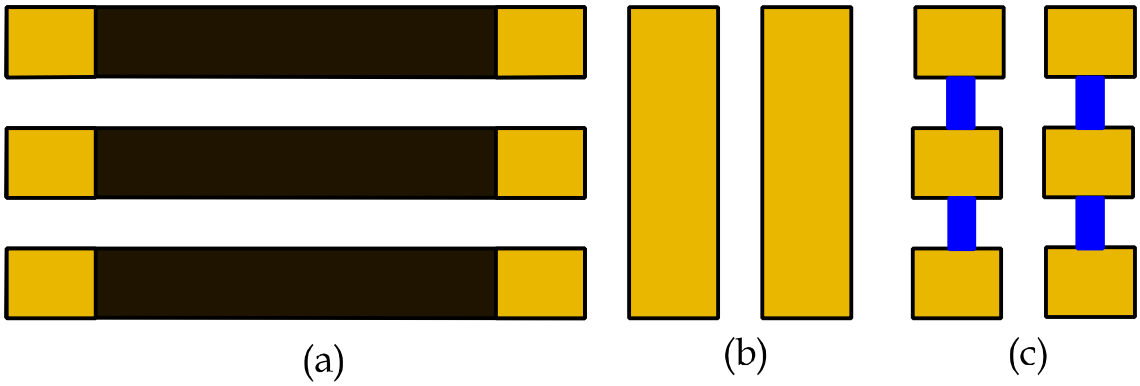

Figure 16 : Layout of calibration standard for LRRM calibration: (a). line, (b). reflect, and (c) match

The essential difference of this method with respect to the TRL method is that it uses a perfectly two matched loads to set the value of the reference impedance (50Ω). The matched load is described by: $S_T = \begin{pmatrix} 0 & 0 \\ 0 & 0 \end{pmatrix}$, each matched load is the reference for the port where it is connected.

For the LRRM calibrations, the reference impedance is determined solely by the definition of the match (load) standard, therefore it is important that the behavior of the match be understood.

Figure 17 shows a simple load model. As position of the tips varies, the capacitance across the resistor stays nearly constant, while the inductance changes significantly due to the change in the length of the current path. Because the resistor is 50 ohms and wC and wL are both small, the capacitance will behave to first order as negative series inductance. Thus the capacitance may be accounted for by the inductor, leaving simply a variable inductor in series with

the resistor. The value of this inductance includes differences between the reference reactances of the load and the thru standards.

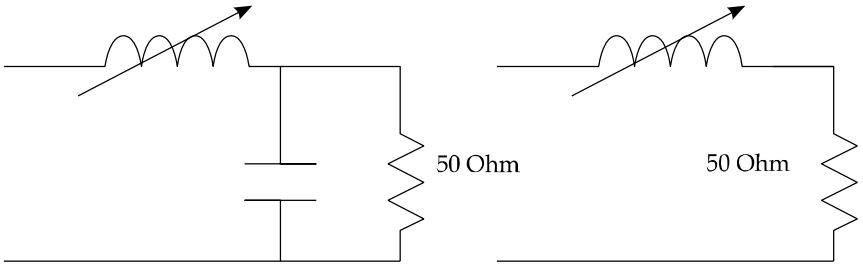

Figure 17 : Simple load model

The line-reflect-reflect-match (LRRM) calibration method is one of the most accurate calibration methods for an eight-term error network. It is valued for its relative insensitivity to small errors in probe placement that are inherent in microwave and mm-wave probing.

1.7.2.2. De-embedding techniques

The de-embedding allows extraction of the intrinsic device performances, removing parasitic of the probe pads and metallization from raw S-parameters measured. The de-embedding moves the reference plane the end of probes to the edge of the device under test (DUT, intrinsic device). On-wafer RF test structures are usually realized by placing the device under test (DUT) between probe pads, with either ground–signal (GS/SG) or ground–signal–ground (GSG) RF probes [26]. Several de-embedding techniques have been proposed over the years [7], [26-28]. The industry two-step “open-short” de-embedding method introduced in 1991 [28], is one of the most used for the high frequency characterization. A new “three step de-embedding” [26] and “open-open-thru-short” [29] de-embedding techniques have been proposed, showing an increase of the accuracy of the figures of merit obtained for the single-loop inductor and high-speed bipolar transistor.

These methods provide correction through the use of specific on-wafer structures, typically, “open”, “short”, “load”, and/or “thru” dummy structures. In mm-wave range, special care must be made in order to avoid mismatch between measurement parasitics of dedicated test structures (dummies) and of the passive/active device under test. The verification of these de-embedding techniques [26], [29] is realized in frequency band up to tens of gigahertz.

A. De-embedding for transistors

In this study, the open-short method has been successfully used to de-embed the pads and interconnects [29]. Figure 18 shows the layouts of a transistor under test and of dummies used for de-embedding.

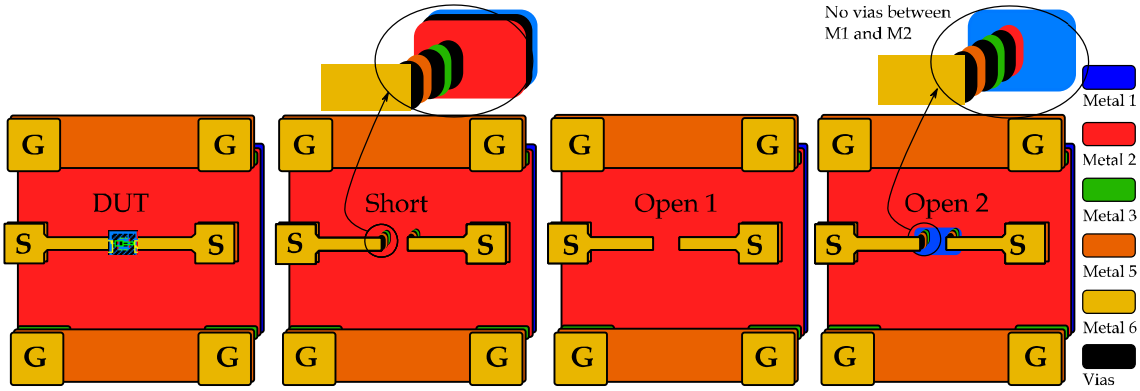

Figure 18 : Illustration of the transistor under test, short, open1, and open2 dummies test structures for de-embedding of S-parameter measurements

Dummies are laid out similar to the DUT, the short is obtained by connecting the extremity of the top metal to the ground metal (metal 1), the open 1 is obtained by removing the via stack between metal 1 and metal 2, and open 2 is realized by shorting the top metal to the metal 2. Dummies are measured in the same series as the DUT.

The pads and the interconnections are realized in the top metal (metal 6) and the front-end device is in the bottom metal (metal 1). In the short and open dummies test structures used for de-embedding shown in figure 18. The short removes the inductive and resistive effects of the pads and the interconnections from

measurements represented by the series parasitic elements in figure 19, while the open removes the capacitance parasitic of the device toward the substrate represented by the parallel elements in the same figure.

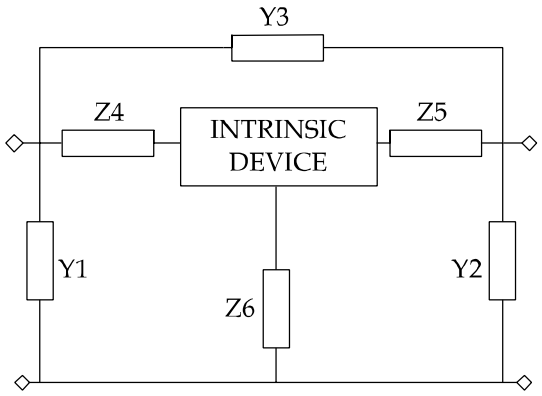

Figure 19 : Equivalent circuit representation of the open-short de-embedding

In this method, the parallel extrinsic elements are subtracted by the open dummy structure as follows:

$$Y_{DUT} = Y_{DUT\_raw} - Y_{Open} \tag{1.9}$$

$$Y_{Short} = Y_{Short\_raw} - Y_{Open} \tag{1.10}$$

The series parasitic are then removed by the short dummy structure as follows:

$$Y_{tran} = ((Y_{DUT})^{-1} - (Y_{Short})^{-1})^{-1} \tag{1.11}$$

This method is widely used due to its simple dummy structure and calculations. However, its accuracy decreases with the frequency and becomes unsatisfactory above already 40 GHz.

For these reasons, modeling engineers at NXP use a more adequate de-embedding technique developed by [10], which is a three-step (short-open1-open2) version of the four-step approach introduced in [30]. This method takes into account the top down parasitics.

The parasitics in the three-step de-embedding approach [26], are modeled as assumed in the figure 20, a special open2 dummy pattern (open2) has been added

for active device to extract the vertical interconnections between the interconnection line in top metal and the front-end device [10]. These vertical interconnections have considerable impact on the de-embedded measurements at high frequencies due to the complexity of the back-end (capacitive interaction of the signals with substrate as well as non-negligible inductive effect of vertical vias).

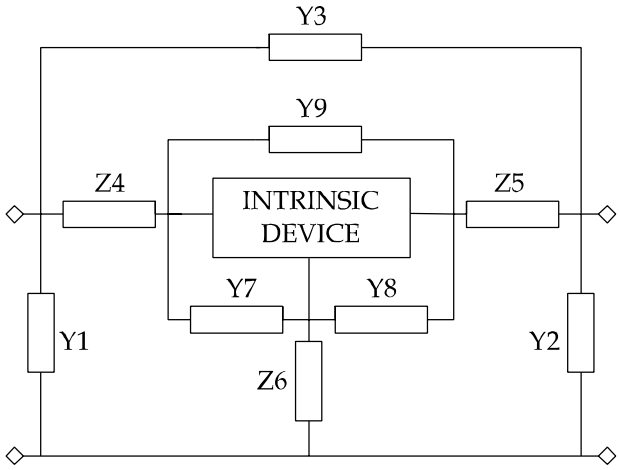

Figure 20 : Equivalent circuit representation of three-step de-embedding

In this method, the intrinsic device Y-matrix is given by Y^{INT} and the extrinsic device Y-matrix is given by Y^{DUT}. $Y^{open-in}$ is describing the open 2 Y-matrix and the $Y^{open-ex}$ the open2 Y-matrix. They are related as follows:

$$Y^{DUT} = \left(\left(Y^{INT} + Y^{open-in}\right)^{-1} + Z^{short}\right)^{-1} + Y^{open-ex} \tag{1.12}$$

$$Y^{open-ex} = \begin{pmatrix} Y_1+Y_3 & -Y_3 \\ -Y_3 & Y_2+Y_3 \end{pmatrix} \tag{1.13}$$

$$Z^{short} = \begin{pmatrix} Z_4+Z_6 & Z_5 \\ Z_5 & Z_5+Z_6 \end{pmatrix} \tag{1.14}$$

$$Y^{open-in} = \begin{pmatrix} Y_7+Y_9 & -Y_9 \\ -Y_9 & Y_8+Y_9 \end{pmatrix} \tag{1.15}$$

For the open and the short dummies, where $Y_{open}^{INT} = 0$ and a "short where$Y_{open}^{INT} = 0$ (using this method on a four port system, for the short structure $V_i = 0$ and for the open structure $I_i = 0$, giving $Y_{open}^{INT} = \frac{I_i}{V_i} = 0$ and $Y_{open}^{INT} = \frac{V_i}{I_i} = 0$), one obtains:

$$Y^{OPEN} = \left(\left(Y^{open-in}\right)^{-1} + Z^{short}\right)^{-1} + Y^{open-ex} \quad (1.16)$$

$$Y^{SHORT} = \left(Z^{short}\right)^{-1} + Y^{open-ex} \quad (1.17)$$

It is easily seen that once $Y^{open-ex}$ is known, one can find the other two unknown matrices Z^{short} and $Y^{open-in}$. Using the information provided by the open and short dummy structures. A straightforward solution here is to add a "pad" dummy structure, which only contains the probe pads and is especially designed to directly measure $Y^{open-ex}$ through

$$Y^{PAD} = Y^{open-ex} \quad (1.18)$$

After that we can recover the intrinsic device using

$$Y^{INT} = \left(\left(Y^{DUT} - Y^{open-ex}\right)^{-1} - Z^{short}\right)^{-1} - Y^{open-in} \quad (1.19)$$

Previous works at NXP [10], demonstrated the practical benefits of adding a load dummy structure to the industry standard "open" and "short" dummy structures.

B. De-embedding for passives

Within NXP Semiconductors "open-short" and/or "open-short-load" de-embedding are used for inductor characterizations [10]. The representation of de-embedding layouts test structures is given en figure 21.

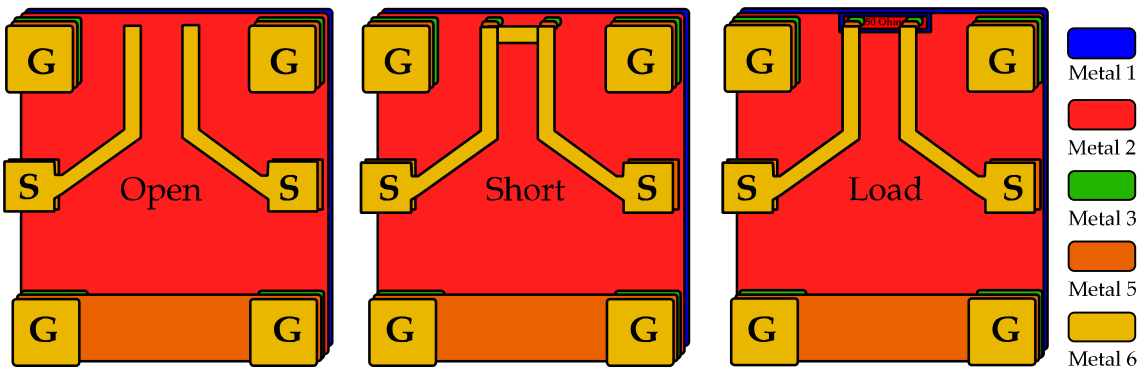

Figure 21 : GSG test structures used in "open-short-load" de-embedding

The measurement of the open standard is obtained by disconnection of the inductor from the test structure. The short standard is implemented by connecting the interconnection lines (metal transporting the signal) to the ground plane (GND). The load parasitic obtained after “open short” de-embedding and subtracted from inductor measurement after “open short” de-embedding.

Several modeling and characterization techniques have been proposed to characterize inductors, capacitors, and interconnect lines [31-33]. The S-parameters are often used to characterize the response of the passive components at mm-wave band. The Z and/or the Y parameters converted from the S-parameters measured allow the extraction of the Π and/or T circuit model [35]. Extension to multi-port can also be done for microwave passive networks [36]. A direct de-embedding “open short” is usually sufficient to obtain accurate results from the raw measurements [10]. From measured data and from the electromagnetic simulation (EM), equivalent circuits for passive devices are driven. A part the measurements accuracy, an accurate electromagnetic modeling plays also an important part in determining the robustness of passive structures under a wave excitation, but the setup should be always determined properly. Some products such as Momontum from Agilent offer a simulation environment that integrates directly into a Layout tool from Cadence.

1.7.3. Small signal model for RFMOS transistor

The characterization and modeling of active devices at very high frequencies is made using the measurement of the scattering (S-) parameters. The accuracy of the S-parameters data hinges on reliable measurements of the device and de-embedding structures. The small signal equivalent circuit (SSEC) has been an effective approach to analyze the behavior of the device. As shown in Figure 22, the SSEC of a RFMOS device can be divided into multiple parts: probe pads, metal interconnections, extrinsic and intrinsic parts.

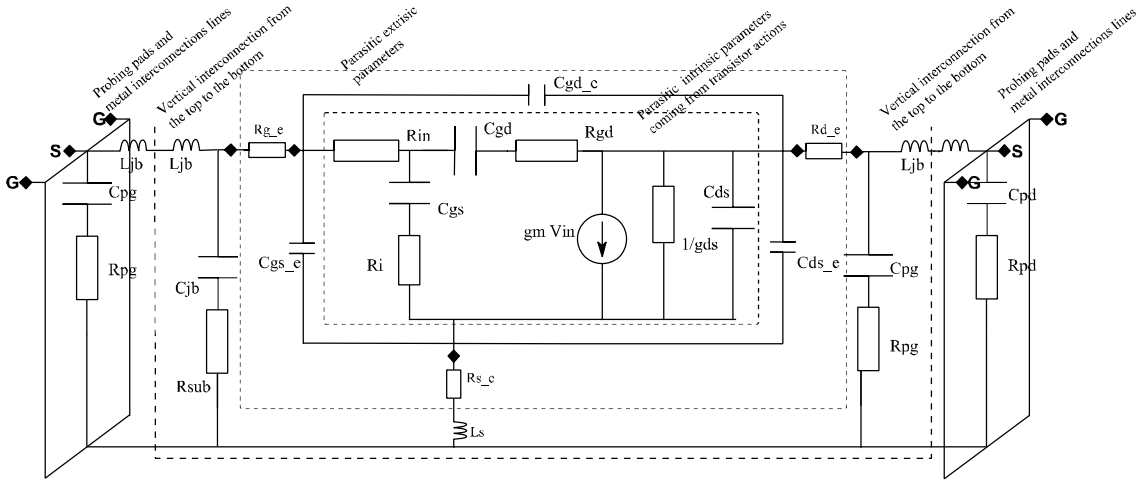

Figure 22 : Small signal high frequency equivalent circuit of RFMOS transistor

The extrinsic part consists of parasitic resistances and capacitances located around the channel of the transistor (R_{g_e}, R_{s_e}, R_{d_e}, C_{gs_e}, C_{ds_e}, and C_{gd_e}), at gate, source and drain terminals. The intrinsic part is the familiar small signal equivalent circuit of the RFMOS (R_{in}, R_i, R_{gd}, R_{ds}, C_{gs}, C_{gd}, C_{ds}, C_{gd}, and g_m). After de-embedding (de-embedding is the procedure to remove probing pads and vertical interconnection shown in the equivalent circuit of 11) only the intrinsic part and the extrinsic part will remain. The intrinsic part will be detailed in the chapter 2. The extrinsic capacitances are given in π configuration in Y-matrix by:

$$Y_e = \begin{bmatrix} jw(C_{gs\_e} + C_{gd\_e}) & -jwC_{gd\_e} \\ -jwC_{gd\_e} & jw(C_{ds\_e} + C_{gd\_e}) \end{bmatrix} \quad (1.7)$$

The extrinsic resistances are given in T configuration in Z-matrix by

$$Z_e = \begin{bmatrix} (R_{g\_e} + R_{s\_e}) & R_{s\_e} \\ R_{s\_e} & (R_{d\_e} + R_{s\_e}) \end{bmatrix} \quad (1.8)$$

1.8. Research goals and the organization of the dissertation

The primary goal for this dissertation is to explore techniques for designing a matched test structures for accurate characterization at millimeter wave range. To reach this goal, mm-wave circuits have been designed with a dual role: extract

device characteristics and validate models at circuit level. From the device point of view, the standard test structures are used and various active and passive devices have been analyzed and/or optimized. On the circuit side, several matched test structures are designed and implemented to investigate the compact models accuracy and the RF parameter extractions. Some novel techniques of extraction at circuit level have been proposed and implemented.

The other goal of this research work concerns the study of new methodologies for device/circuit characterization and developing certain design techniques for mm-wave circuit.

Along the manuscript, various topics covering the measurements, the characterization of inductors, of RFMOS, of bipolar transistors, and of matched test structures are presented.

The goal of the first chapter is to introduce the general context and to give the importance of modeling and characterization at device and at circuit level in millimeter wave.

The concepts of matched test structure and circuit level characterization, are presented in the second chapter

The aim of the third chapter is to explore the matched test structure using the bipolar transistors. This is followed by a discussion about results and comparison between standard and proposed techniques.

Finally, chapter 4 concludes the dissertation and proposes some perspectives for future research work.

1.9. Summary

In this chapter, methods used for mm-wave modeling and characterization are discussed. Challenges for RF application and RF characterization are brought to

attention with some examples from literature. The performance of mm-wave devices can be addressed based on different ways. An investigation on de-embedding schemes, test structures improvements, and characterization at device level are discussed. The following chapters will expand on the issues discussed in this chapter.

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Chapter 2: Design of circuits for validation of RF device models at circuit level

Chapter 2 Design of circuits for validation of RF device models at circuit level

2.1. Introduction

Device performance in millimeter-wave frequencies is often under the influence of the layout parasitics. As the frequency band of interest increases, the RF modeling engineers must deal simultaneously with multiple characterization, modeling, and design constraints [1]. Several iterations in test structures optimization, measurements, extractions, and de-embedding are typically followed in modeling and measurement flow to meet the modeling goals. These iterations, however, can become measurement and time prohibitive. As a result, the measurement and characterization errors are accumulated and the device may not longer meet some performance specifications [1-3].

In this chapter, we look more closely at some of the important limitations caused by the increase of frequency from device and circuit points of view. The study is realized by using of the both approaches, device level characterization and circuit level characterization. The approach of characterizing at device level is based on the standard characterization method previously developed by NXP modeling engineers with improved test structures. The approach of characterizing at circuit level is doubly original; firstly its tries to explain the high frequency limitations of devices, by analyzing the whole elements such as inductors, interconnect lines, and transistors. Secondly it allows the extraction of a few model parameters from circuit measurements. For example, this is possible by matching a transistor under test to 50 Ohms (impedance of measurement equipment) improving by this its transmission gain in the frequency band of interest [4-5].

The chapter covers also high frequency design constraints such as the prediction of the interconnect lines contribution between two passive devices, between

passive and active devices, and existing solutions to overcome difficulties related to the parasitic existing in layout.

2.2. Challenges for single-loop RF inductors characterization

Planar spiral inductors with typical values of a few hundred Pico henries (pH) fabricated on high resistivity substrates allow peak quality factor Q around 30 at frequency of few tens gigahertz [2-6]. At NXP several compact models (ex. LSIM3) are available. However, in term of measurements, it was found that impedance of inductors is quite difficult to extract with accuracy using conventional de-embedding methods for a small and single-loop (one turn) inductors [3]. The model has to describe self inductance, DC resistance, and quality factor versus frequency also in the millimeter wave range (small inductor). Our interest for small inductors in this section is based on the fact that the self resonance frequencies higher than about 20 GHz can only be achieved by inductances lower than 1 nH. The design community expresses then a strong interest for small inductors (with high self resonance frequency) to make millimeter wave circuits.

Since the inductor is the one of the widely used component when implementing LNAs or VCOs, the performance of these circuits will depend on its quality factor model accuracy [7]. In the figure 23 is shown the single ended (SE) inductance of a 1nH octagonal inductor. It's easy to see that the inductance is constant up to certain frequency which equal in general to the third of the resonance frequency. We may even say that, above this frequency, the inductance increases very fast with the increase of the frequency.

To obtain a large band where the inductance value is constant it is necessary to dispose of inductor with high resonance frequency and the best way to increase this resonance frequency is to optimize the inductor geometry and make it smaller.

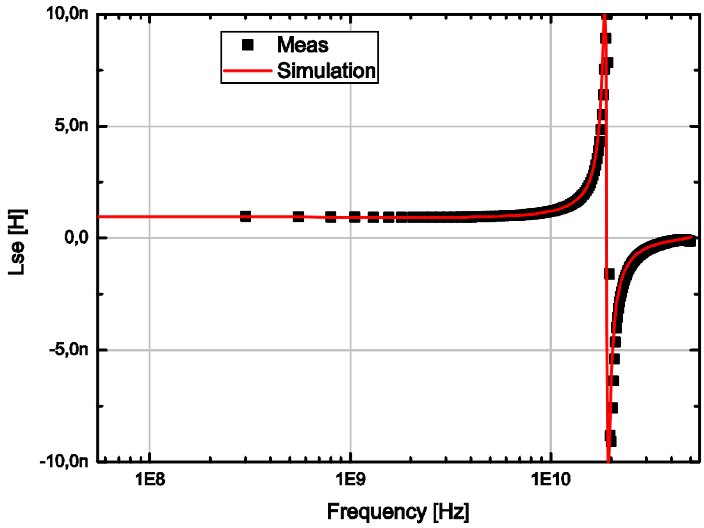

Figure 23 : Self inductance of a 1nH octagonal inductor

2.1.1. Octagonal inductors

The inductors used in this study are fabricated with NXP Semiconductor BiCMOS technology. They have an octagonal shape with symmetrical geometry (their characteristics are independent from which input port the inductor is analyzed with respect to a central tap connection to allow the design of differential circuits).

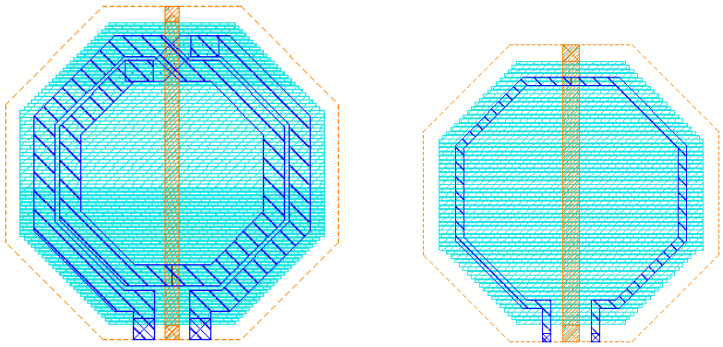

Figure 24 : Layout of the octagonal inductors with a 0.25µm BiCMOS technology, two turns (left) and single-loop (right). The ground shield consists of the polysilicon bars perpendicular to the symmetry plane of the inductor

The 0.25µm BiCMOS technology uses five metallization layers. The spiral is built by using the thick top metal layer (metal 6 that is 3 µm thick and that has a sheet resistivity of 10 mΩ) with higher conductivity to reduce the resistivity of the metal tracks and to increase the quality factor of the integrated inductors. The

ohmic losses in the substrate due to electrical coupling are avoided by using a patterned ground shield, to provide a short circuit to ground.

In figure 24 are shown the layouts of two octagonal inductors fabricated in 0.25µm BiCMOS. These devices together with the third one (not shown in figure 24) are analyzed in this chapter and their dimensions are given in table 1. The first inductor is a two turn inductor with a value of 1.04nH, the inductor 2 is the two turn inductor with a value of 668pH, and the inductor 3 is the single-turn with a value of 360pH.

Inductor	L (pH)	Din (µm)	Width (µm)	N. tours	Separation of metal (µm)
1	1039	130	15	2	3
2	668	79	5	2	3
3	360	130	5	1	0

Table 1 : Geometrical parameters of octagonal inductors

2.1.2. Inductor test structures for on-wafer measurements

The on-wafer test structure (TS) makes the interconnection between the device under test (DUT) and the probes. This interconnection is necessary due to the difficulty to built probe tips small enough to directly connect to the DUT. The measurements of the device in a test structure allow the extraction of the electrical models after subtraction of TS contribution. Figure 25, shows the dummy test structures (open, short, load) used for the characterization of the integrated inductors.

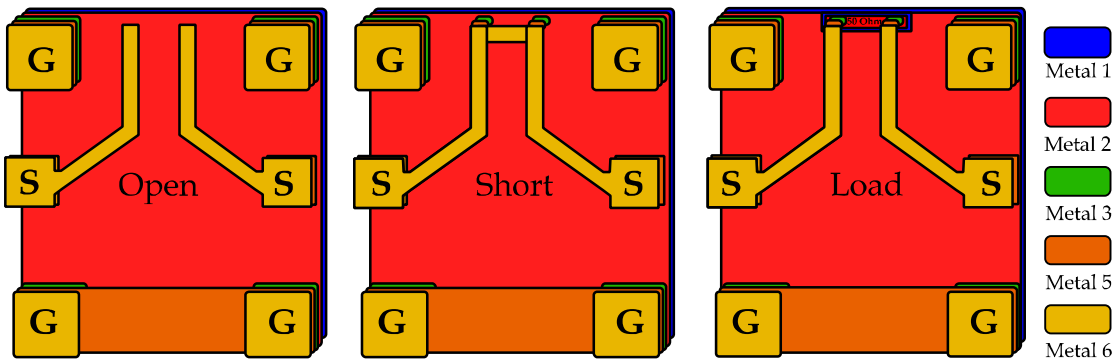

Figure 25 : On-wafer test structures in two ports configuration

A key point is the way we subtract the test structure contribution from the whole contribution (DUT+ST). For this purpose, within NXP Semiconductors the "open-short-load" methodology [2] has been found as the most accurate for the extraction of the TS contribution. The short dummy is obtained by connecting the top metal to the down metal at the end of the interconnection line (GND). The "load" is obtained by the interconnection of (50 Ohms) resistors at the end on the test structure interconnections.

2.1.3. Modeling of inductors

Two port S-parameter measurements are made in the 100MHz to 50GHz range after the Line-Reflect-Reflect-Match (LRRM) [8] calibration using Agilent 8364B vector network analyzer with the Cascade Microtech Infinity co-planar GSG RF-probes. The S-parameters measured are obtained after de-embedding of the test structure parasitics after "open-short-load" de-embedding. To evaluate the compact model and measurement accuracies, Momentum simulator (Agilent) has been used. The one spiral inductor contribution has been subtracted from the EM simulations of the inductor plus TS. From EM simulation methodology point of view, all vias were simplified and two pins in M6 "edge pins" have been added at the extremity of inductor connections. The substrate is defined using default substrate available in BiCMOS design package. The inductors dimensions are summarized in table 1. The SE self inductance, quality factor measured and simulated for the inductor with two turns (inductor number 1 in table 1) are shown in figure 27 over the 100MHz to 50GHz frequency range.

The compact model of octagonal inductors used for simulation is the lumped LSIM model available in NXP design package. A description of the model is given in [9]. The extraction of inductors characteristics from small signal simulations and measurements (S-parameter sets) are made based on lumped π-equivalent circuit.

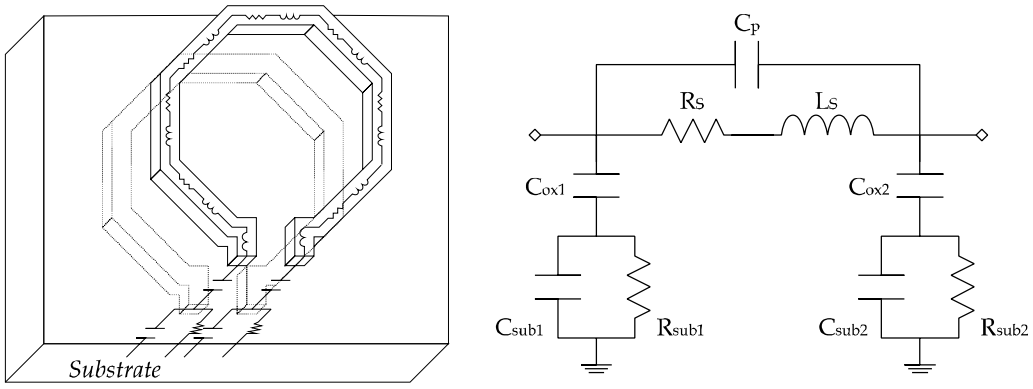

Figure 26 : Two port π-model

The use of the equivalent circuit allows the extraction of the Single Ended (SE) inductance and quality factor, which are calculated (from Y-parameters) with equations (2.1) and (2.2), respectively:

$$L_{se} = \frac{Imag(1/Y_{11})}{2\pi freq} \tag{2.1}$$

$$Q_{se} = \frac{-Imag(Y_{11})}{Re(Y_{11})} \tag{2.2}$$

The quality factor (Q) of the inductor is determined by the geometry and fabrication process [10]. This criterion is the ratio of the inductance impedance value over its resistance equivalent losses. It is obtained from the admittance parameters (Y) after transformation of S-parameters (eq. 2.2).

The π configuration model is often used to extract simple model from measurements. It uses ideal components like; C_p is the capacitance between coils, R_s is the ohmic losses of the metal track, L_s models the inductance of the coil. C_{ox}, C_{sub}, and R_{sub} are respectively, the oxide capacitance, substrate capacitance, and substrate resistance. Such a model is less accurate and is not used in this study.

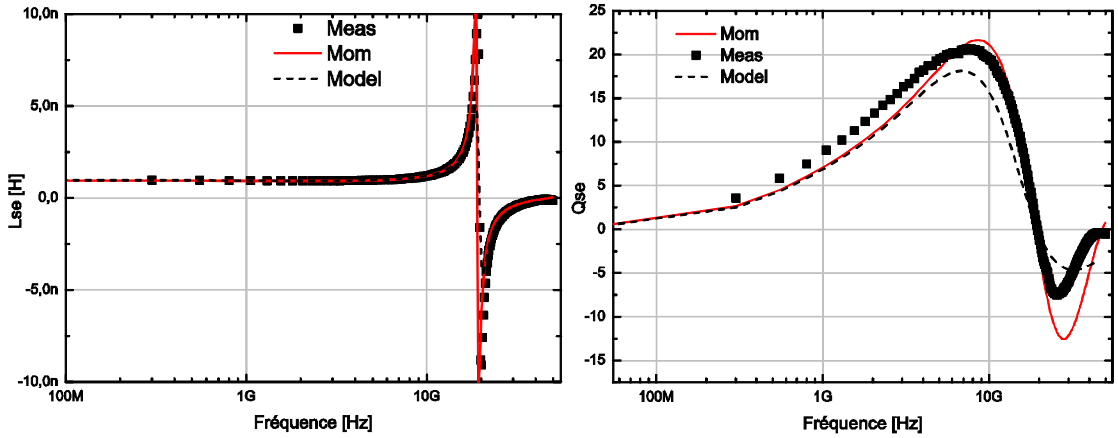

Figure 27 : Self inductance (left) and quality factor (right) of a two turns octagonal inductor

Since the inductors characterized are used in a single ended mode LNAs, the model has to give an excellent description of the single mode impedance mainly defined by the self inductance and the quality factors versus frequency. The self inductance is extracted from S-parameter simulations and measurements using the equation (eq. 2.1). As shown in figures 27, the simulation is in good agreement with the measurement. The broadband verification plots indicate that a good qualitative agreement between measured and modeled self inductance and quality factors over frequency is obtained.

The self inductance and the quality factor of the single-loop inductor (inductor number 3 in table 1) are shown in figure 28.

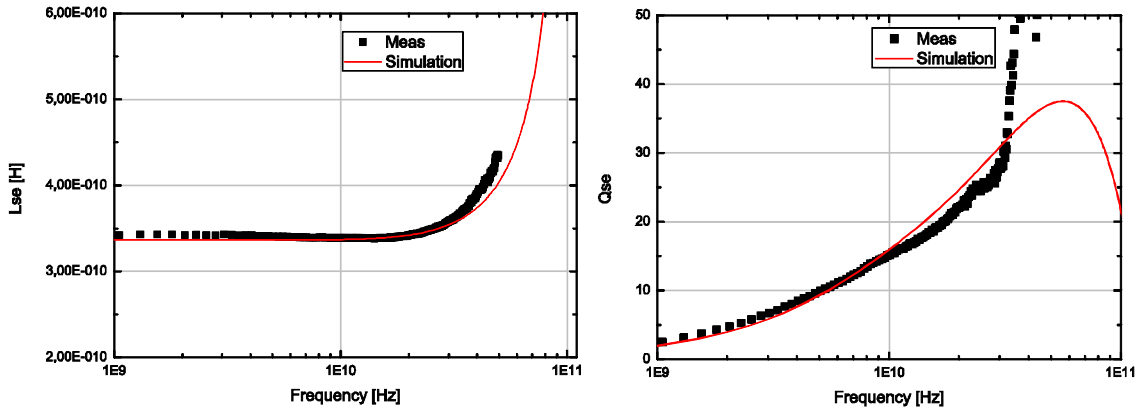

Figure 28 : Self inductance (left) and quality factor (right) of single-loop octagonal inductor

Due to the small size of the inductor, we notice that the measurements show a different behavior than simulations at millimeter wave frequency (above 35GHz). This behavior is weirder for the quality factor. The reason of this inaccuracy is due to the de-embedding and measurement errors [3]. The small inductors are difficult to characterize because of their intrinsic impedances which are dominated by the test structure parasitics. The resistance of the inductor is highly dependent of the frequency.

As it can be seen in figure 28 and as mentioned before, when the inductor is small in term of sizes (single-turn inductor) the quality of the measurements is affected. This issue has also been observed in bibliography [2-3]. To diminish the contribution, a solution consists in designing inductor with the smallest interconnects lines width. This is the matter of the next section.

2.1.4. New test structure for single-loop inductor characterization

One of the fundamental properties of an interconnect line in a test structure is that generates a magnetic field. This alternating field penetrates into the conductive substrate and induces a voltage difference, which in turn generates a current. This phenomenon diminishes the energy in the conductor, decreasing at the same time the quality of the transmitted signal. Moreover capacitive coupling between the conductors and the substrate is another negative effect since, depending on the amount of capacity and the measurement frequency, a portion of the transmitted energy will be stored in these capacitors.

To ensure that discrepancies between measurement and simulation are caused by the test structure, the old test structure was optimized on a new MPW (Multi Project Wafer). In the new test structure, the width of the interconnect lines (from the signal pads to the inductor under test) and the area of signal pad are reduced. The new test structure proposed is shown in figure 29. From the figure, there is noticeable difference between the old and the new test structures. The width of

the interconnect lines are reduced to the minimum width allowed by the technology.

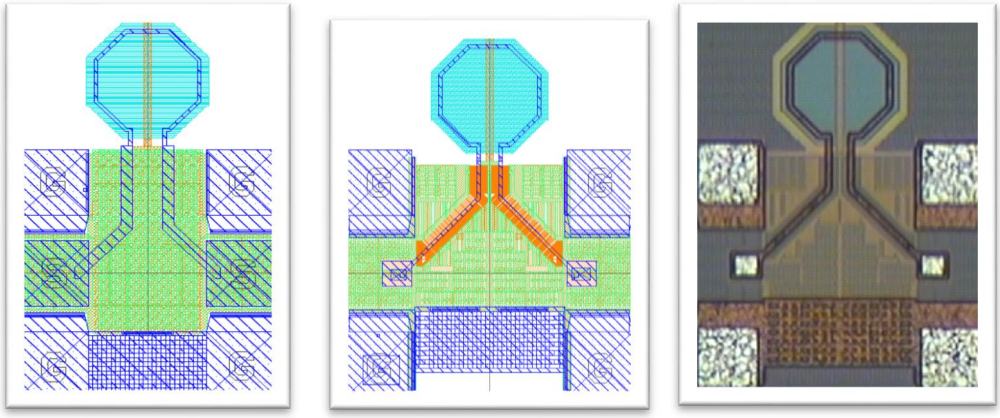

Figure 29 : Old test structure (left) and new test structure (middle and right)

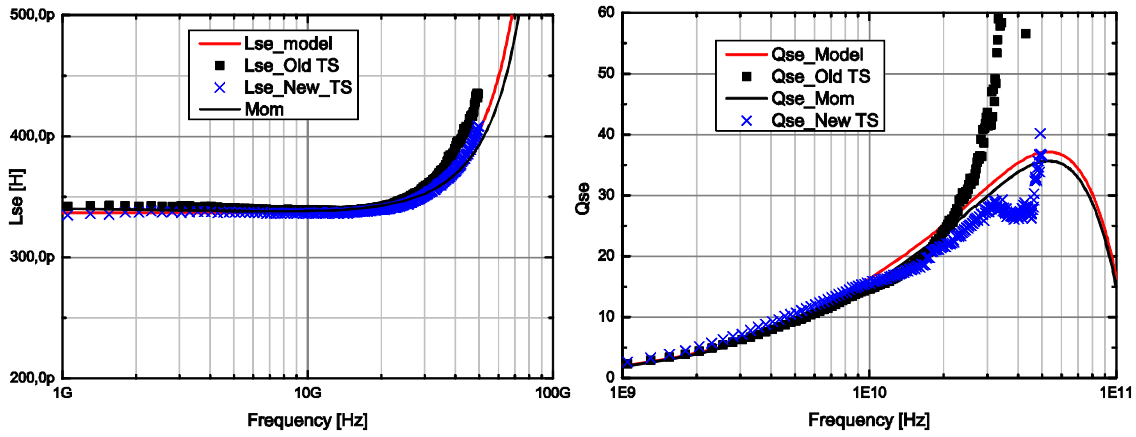

Figure 30 : Self inductance (left) and quality factor (right) of single-loop octagonal inductor

The results obtained using these new test structures are shown in figure 30. As shown in the figure, the measurements obtained using the new test structure show a behavior closer to compact model and EM simulations (for the inductance number 3 in table 1). The inductor number 2 in table 1 has been also characterized using the new test structure. The results show a better agreement between measurement and simulation than the standard test structure. The results of measurements and compact model simulations are shown in figure 32 for the SE self inductance and the quality factor.

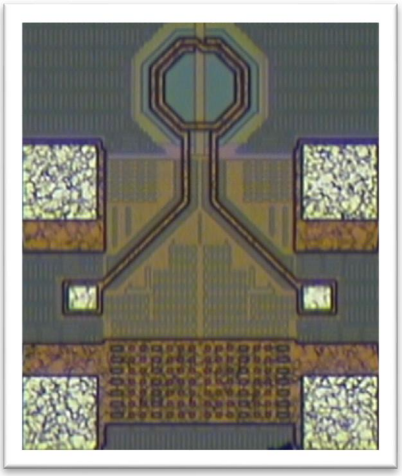

Figure 31 : Photograph of the inductor 2 in the new test structure

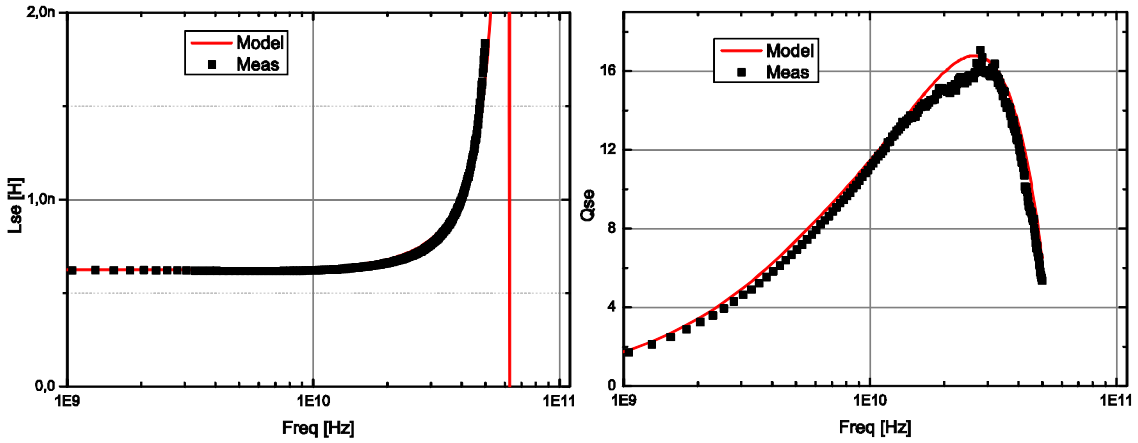

Figure 32 : Self inductance (left) and quality factor (right)

2.1.5. Conclusion

In this section, it has been shown that the optimizing of RF test structure allows better characterization of small inductors in mm-wave range. The inductor measurement accuracies are analyzed in order to obtain an appropriate extraction / verification of the model needed for circuit-level simulations.

2.3. RFMOS modeling and characterization

Along this section, the steps followed to extract parameters of the RFMOS transistor from the S-parameter measurements are presented. The extraction procedure presented here underline the important parameters needed to develop circuit design. The characterization methodology (presented in section 2.3) is

discussed. The RF characterization and verification are realized for RFMOS (20µm / 0.25µm) fabricated in 0.25µm BiCMOS technology.

2.3.1. Small signal equivalent circuit of RFMOS transistor

The high frequency small signal behavior of a MOS transistor can be predicted using an equivalent circuit as shown in figure 33. This equivalent circuit is extracted (capacitances, resistances, transconductance, and output conductance) after de-embedding of test structure parasitics (probe pads, interconnection lines, and vertical interconnection from the top to the bottom). Similar equivalent circuits have been published in [11]-[16].

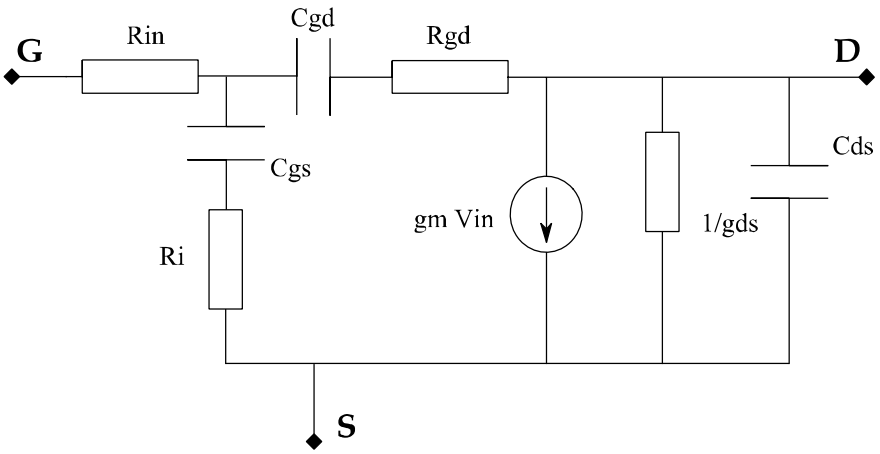

Figure 33 : Small signal equivalent circuit of the RFMOS transistor

In figure 33, g_m is the transistor transconductance which allows the control the output current when a voltage is applied to the gate. g_{ds} is the output conductance, R_i , R_{in} and R_{gd} are intrinsic resistances in series with intrinsic capacitances. The C_{gs} is the gate-source capacitance, C_{ds} is the drain-source capacitance, and C_{gd} is the gate-drain capacitance.

2.3.2. DC modeling

The DC characterization consists on a set on-wafer measurement that is used to extract the input/output transistor behavior [16]. The DC compact model has been extracted based on several MOS transistor geometries. However, the

dimensions of the transistor under test in RF range are different than those used for DC extraction. For this reason, first the verification of model accuracy in DC is made. Drain current, conductance, and transconductance are measured and simulated both in drain voltage and gate voltage sweeps.

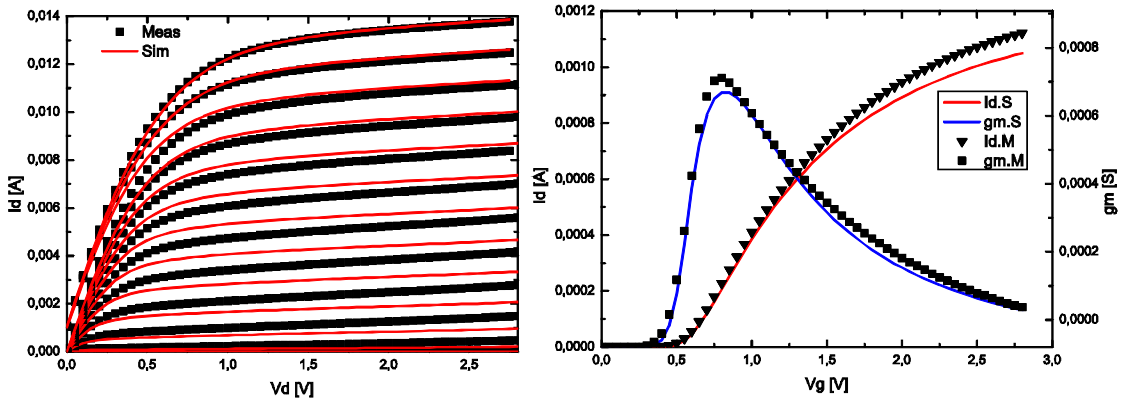

Figure 34 : Example of measured and simulated output characteristics (Ids-Vds), input characteristic (Ids-Vgs), and transconductance for a 20x0.25µm NMOS transistor

The output I_{ds}-V_{ds} and input I_{ds}-V_{gs} curves of 20µm / 0.25µm transistor measured and simulated are shown in Figure 34. They present a good agreement between measurements and simulations without optimization after DC parameter extraction. The measurements over the wafer for different dies are not presented here and show a negligible variation (after verification of a few dies). The DC measurement uncertainty is in general related to contacts and cables.

2.3.3. AC modeling

The AC measurements allow the extraction of the small signal equivalent circuit by measuring the S-parameters of the transistor. The equivalent circuit used to extract the different characteristics is shown in figure 33. The S-parameters are measured from 100MHz to 50GHz. The gate of the transistor is connected to the input RF port and the drain was connected to the output RF port, whereas the source was grounded.

After de-embedding and extrinsic elements subtraction, the intrinsic elements are obtained. In this study a conventional open1 (dummies without DUT), open 2

(all the metallization have been shorted from the top metal 6 up to metal 2) and short (all the metallization have been shorted from metal 6 up to metal 1) de-embedding technique was used to subtract the parasitics of the test structures. Based on S-parameters converted to Y-parameters, the SSEC parameters extracted are shown in Figure 35. The intrinsic parameters are extracted using the equations bellow [14]:

$$C_{gs} = Im\left(\frac{Y_{11}+Y_{12}}{w}\right)\left(1 + \left(\frac{Re(Y_{11}+Y_{12})}{Im(Y_{11}+Y_{12})}\right)^2\right) \quad (2.3)$$

$$C_{dg} = Im\left(\frac{-Y_{12}}{w}\right)\left(1 + \left(\frac{Re\,Y_{12}}{Im\,Y_{12}}\right)^2\right) \quad (2.4)$$

$$C_{ds} = Im\left(\frac{Y_{12}+Y_{22}}{w}\right) \quad (2.5)$$

$$g_m = \left|(Y_{21} + Y_{12})\left(1 + \frac{Re(Y_{11}+Y_{12})}{Im(Y_{11}+Y_{12})}\right)\right| \quad (2.6)$$

$$R_{gd} = \frac{1}{C_{dg}w}\,\frac{Re\,Y_{12}}{Im\,Y_{12}} \quad (2.7)$$

$$R_i = \frac{1}{C_{dg}w}\,\frac{Re(Y_{11}+Y_{12})}{Im(Y_{11}+Y_{12})} \quad (2.8)$$

The small-signal elements are determined by direct extraction from the de-embedded results using the above analytical equations which are derived from real and imaginary parts of the Y-parameters. The small-signal equivalent circuit used is that shown in figure 33.

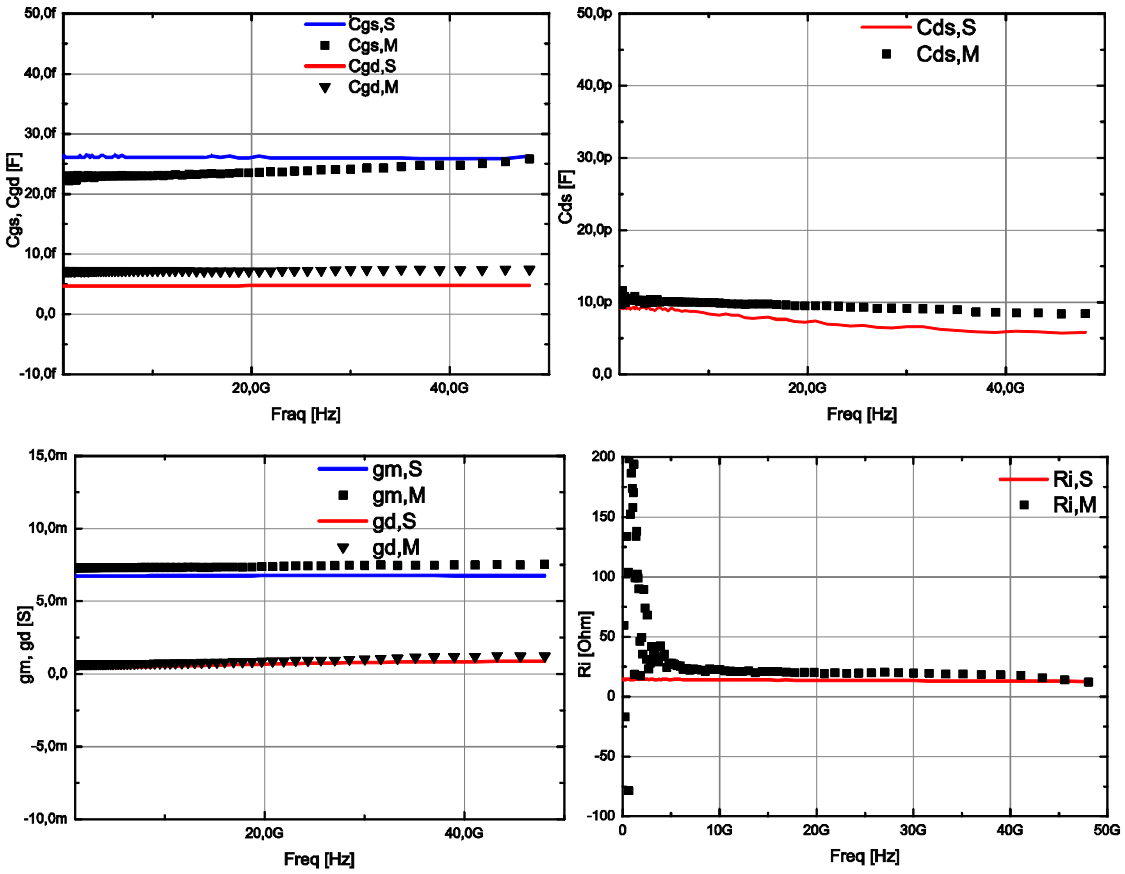

Figure 35 : The extraction of intrinsic small signal parameters of the 20µmx0.25µm RFMOS transistor

From the Figure 35, the transistor measured exhibits nearly flat curves along the frequency band for all parameters. The results show that the extracted parameters remain almost constant with frequency. This demonstrates that the extraction method is accurate and reliable. The values of the small signal equivalent circuit parameters have been deduced from these curves. They are extracted from measurements at 1GHz and summarized in Table 2.

C_{gs}	C_{ds}	C_{dg}	g_m	g_d	R_{in}	R_i
23 fF	9pF	5fF	7.3 mS	0.4 mS	28 Ω	12 Ω

Table 2 : Small equivalent circuit parameter extracted values

AC extraction accuracy is known to be more sensitive to measurement uncertainties than DC characterization because of the environment effects.

The g_m extracted from the S-parameter measurements and from DC measurement match very well, verifying the validity of the equivalent circuit and the extraction method. There are two main ways to evaluate and confirm the validation of the small signal equivalent circuit parameters extracted. Firstly as previously mentioned and as illustrated in figure 35, the intrinsic extracted parameters, are invariables over frequency, secondly the comparison between measured and simulated S-parameters.

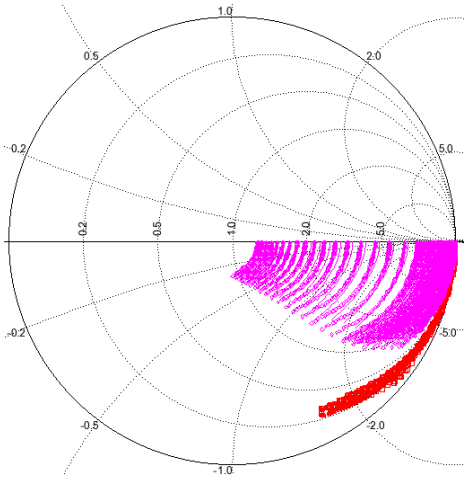

Figure 36 : The S11 (red) and S22 (pink) parameters measured and simulated

Smith chart allows faster and accurate evaluation of the model accuracy by comparison of the simulated and measured characteristics. The figure 36 compares the S-parameters simulated and measured of the 20µmx0.25µm transistor in the 100MHz-50GHz frequency range.

2.3.4. Parameter extractions for high frequency ICs design

At millimeter-wave frequencies, the impact of extrinsic parasitics is more significant when looking to S-parameter plots. The capacitive parasitics are more significant because of the layout consideration (back-end). Consequently, it is critical to accurately model the layout of the back-end device. In traditional microwave design the common approach is to use device parameters extracted in the calculation of impedance matching (ex. Matching network) [16], [19]. This

approach is very accurate and takes into accounts all the distributed effects associated to the intrinsic device operating. While this method is sufficient for small signal circuit design applications, the accuracy of the calculation hinges on the transistor parameters to be used [16], [24]. In RF designs, it should not only to predict exactly the transistor behavior, but it should also to predict the layout effects. These elements are extracted in our study since the size of the transistor is smaller and also in order to take into account the metallic connections from the active zone of the transistor to the reference planes of connections. For those reasons, a small signal equivalent model given below is used to extract parameters used in linear circuit applications [16].

The circuit given in figure 33 can be simplified to that of figure 37 by using local series-series feedback [15] by absorbing the resistances R_{in} and R_i in the gate-source capacitance C_{gs}. The capacitance C_{gd} has been neglected. The C_{in} from the modified circuit is:

$$C_{gs} = \frac{C_{in}}{1+g_m(R_{in}+R_i)} \tag{2.9}$$

$$C_{in} = C_{gs}(1 + g_m(R_{in} + R_i)) \tag{2.10}$$

$$C_{ds} = \frac{C_{out}}{1+g_m(R_{in}+R_i)} \tag{2.11}$$

$$C_{out} = C_{ds}(1 + g_m(R_{in} + R_i)) \tag{2.12}$$

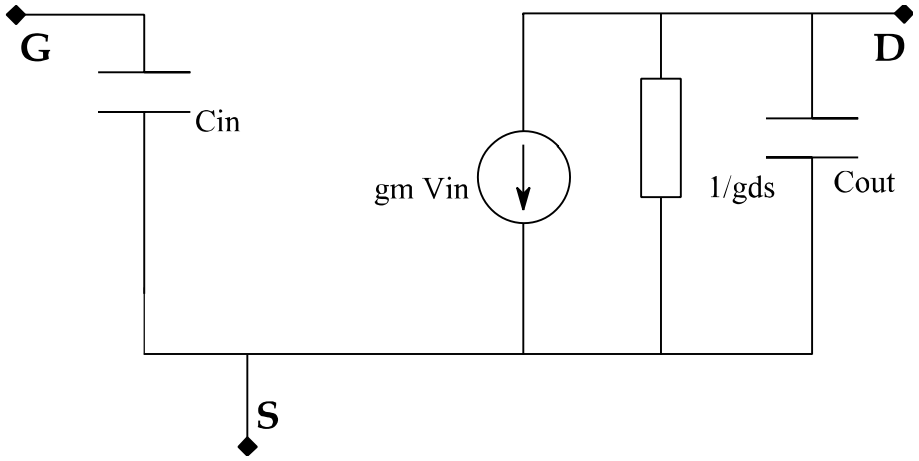

Figure 37 : Simplified small signal equivalent circuit of the RFMOS

Based on the equivalent circuit shown in figure 37 and based on equations (2.13, 2.14), the extraction of the capacitances can be established directly from the imaginary part of the Y-parameters:

$$C_{in} = Im\left(\frac{Y_{11}}{w}\right)\left(1 + \left(\frac{Re\,Y_{11}}{Im\,Y_{11}}\right)^2\right) \tag{2.13}$$

$$C_{out} = Im\left(\frac{Y_{22}}{w}\right) \tag{2.14}$$

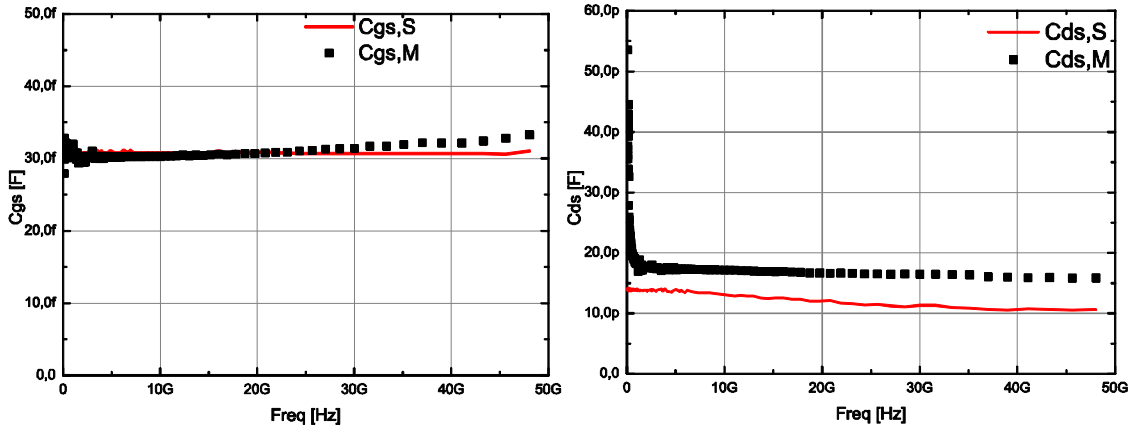

Figure 38 : The extraction of the input and output capacitances

Figure 38 shows the capacitance C_{in} extracted (equal to 32fF@1GHz) which is equal to C_{in} calculated by equation 2.10 and which differs from the C_{gs} extracted from figure 35 by 7fF (this difference corresponds to C_{gd} which is not included in

this simplified small signal equivalent circuit). This information is very useful for the linear circuit performances design. The main objective of this modification is to simplify the input impedance of the transistor and thus simplify the input impedance matching of the transistor (presented in section 2.3).

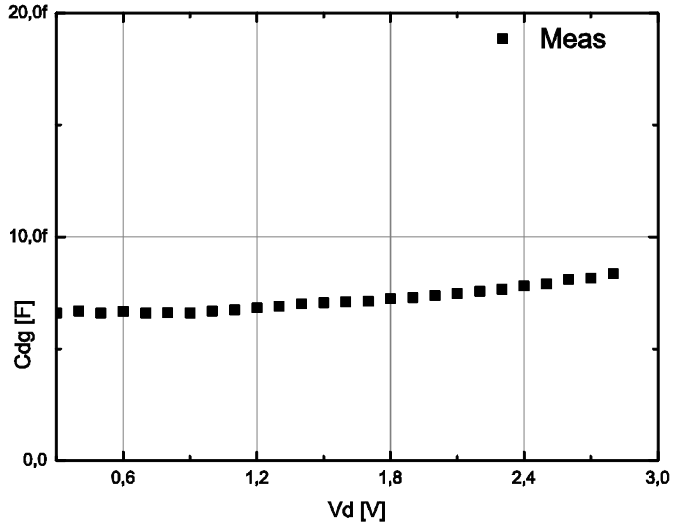

Figure 39 : The gate to drain capacitance Cgd, Vd =2.8V

From figure 39, the value of C_{gd} =7fF is extracted. It can be seen the input capacitance C_{in} and output capacitance are:

$$C_{in} = C_{gs} + C_{gd} \quad (2.15)$$

$$C_{out} = C_{ds} + C_{gd} \quad (2.16)$$

From now and for convenience, we consider C_{in} as the new C_{gs} with a value of 32fF and the C_{out} as the new C_{ds} with a value of 16fF.

2.4. Matched test structure design for on-wafer characterization

The characterization at circuit level can be achieved by the characterization of more than one component into RF pads. Compared to the characterization at device level, the characterization at circuit level includes the standard test structure for RF characterization (probe pads, input and output interconnections, intrinsic device as shown in figure 40 (a)) and multiple devices with the interconnection between them shown in figure 40 (b). The transistor is characterized and measured in a large band (e.g. up to 50GHz or 110GHz) [13-

19]. However, at higher frequencies (in mm-wave range), the transistor characteristics (e.g. Small signal characteristics are more sensitive) are impacted by measurement inaccuracies due to an important attenuation of the measured signal and due to low input and output impedances when the device is small in term of sizes and connected in common source configuration [17], [18].

Nowadays, it's more complicated to improve the accuracy of parameters extracted from measurement at device level since the size of transistors continues decreasing. So, it seems necessary to investigate more than one component into RF probe pads in order to seek solutions for discrepancies coming from high frequency effects, de-embedding errors, and the measurement equipment. The characterization at circuit level could provide a way to overcome the high frequency effects.

The methodology proposed in this section focuses on the matching of the transistor under test in order to enable a better transmission of the measurement signal (from probe) to the intrinsic device and improve its transmission gain at the desired frequency. The method takes advantage of few inductive devices to make a matching network between RF pads and the transistor as it is shown in figure 40 (b).

2.4.1. Methodology of impedance matching of a transistor under test

The matching of the transistor connected in GSG probe pads allows the extraction of C_{gs} and g_m parameters of the equivalent circuit of a MOS transistor under 50Ω matching conditions in frequency band centered at higher frequency [18]. Thus, the measurements provide results (e.g. a resonance frequency) that are a combination of the equivalent circuit parameter and of the matching network. This technique allows first, the measurements of devices in a reduced frequency band (e.g. mm-wave range), and second it allows the verification of the characteristics extracted by standard methodology (broad band measurements

without 50Ω matching). The characteristics of active devices (MOS and Bipolar) but also of the passive components (inductors used in the matching network) can be extracted and validated at higher frequencies in a broad band. This section presents the way the test structures are designed and the methodology used to extract the characteristics of equivalent circuit from the measurements of a smart matching test structure.

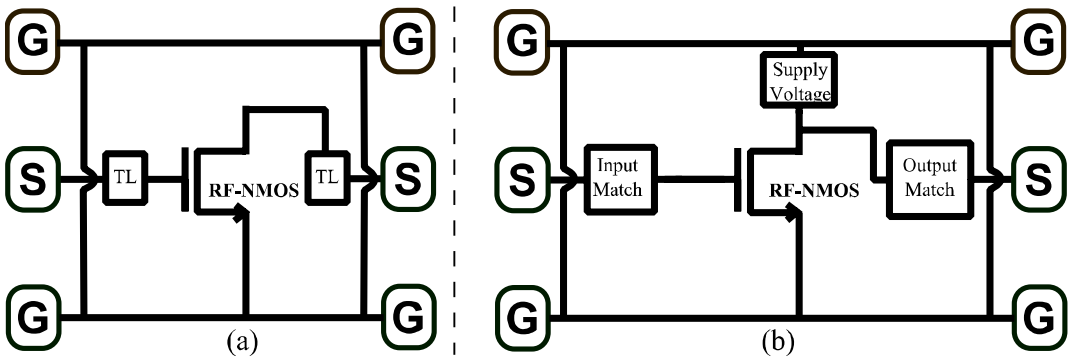

Figure 40 : (a) Schematic of conventional test structure, (b) Schematic of the matched test structure

The extraction of small signal equivalent circuit parameters has been performed by an appropriate matching of on-wafer measurement setup. This improvement concerns a better choice of the test structure (probe pads and interconnections) in order to match the active device to the 50Ω impedance of the probes. The matching has been realized by replacing the straight interconnection lines by a complex matching network (e.g. using inductors).

The methodology proposed in this section allows the definition of measurement references by the use of a smart matching of the transistor connected in GSG probe pads in common source (CS) configuration. A module with transistor matching includes standard transistor test structures and matched transistor test structures as it follows:

- A smart matching transistor architecture (SMTA) integrated between GSG probe pads; that includes passive and active devices (e.g. inductors) and carries out the matching network;
- The passive and active devices that are used in SMTA, and which will be individually characterized;

Dummies for de-embedding (simple or complex methods can be used depending on interconnection complexity and the measurement planes).

2.4.2. Definition of the Smart Matched Test Architecture (SMTA)

The definition of SMTA depends on the type of the device to be characterized respectively MOS or bipolar transistors. For the MOS transistor, the gate source capacitance (C_{gs}) and the transistor transconductance (g_m) are extracted from the measurements of single MOS test structure (without matching network, characterization presented in section 2.2). The values of C_{gs} and g_m depends on transistor sizes. The input impedance Z_{in} of the MOS transistor represented in figure 41, with inductive source degeneration is:

$$Z_{in} = \frac{L_s g_m}{C_{gs}} + j\left((L_s + L_g)2\pi f_{c1} - \frac{1}{C_{gs}2\pi f_{c1}}\right) \quad (2.17)$$

Where, L_s is an inductance in series with MOS transistor source, and L_g is added in series with the gate. Based on this equation, a resonance frequency is obtained when the imaginary part is 0. Thus, the SMTA allows the measurement of S-parameters of transistor matched to 50Ω around a resonance frequency given by f_{c1}. First, the L_s inductance is calculated from the real part of Z_{in} that has to be 50Ω ($L_s = \frac{50 \cdot C_{gs}}{g_m}$). At higher frequencies, the C_{gs} capacitance, that has small value (e.g. $\cdot C_{gs}$=32fF for a 20µmx0.25µm transistor), makes the transistor impedance very low and leads to measurement inaccuracies. L_s Adds “a real part” contribution to the overall impedance seen from the transistor gates that matches

to 50Ω. The input impedance is purely resistive at the resonance frequency fc1 (see eq. 2.17).

Second, with gm and C_{gs} extracted from single transistor measurements, with Ls calculated as presented above, and f_{c1} chosen upon measurement range needs, L_g is calculated from the imaginary part of equation 2.17. It aligns the series resonance frequency with the desired frequency of operation f_{c1} ($L_g = \frac{1}{C_{gs}\cdot(2\pi f_{c1})^2} - L_s$).

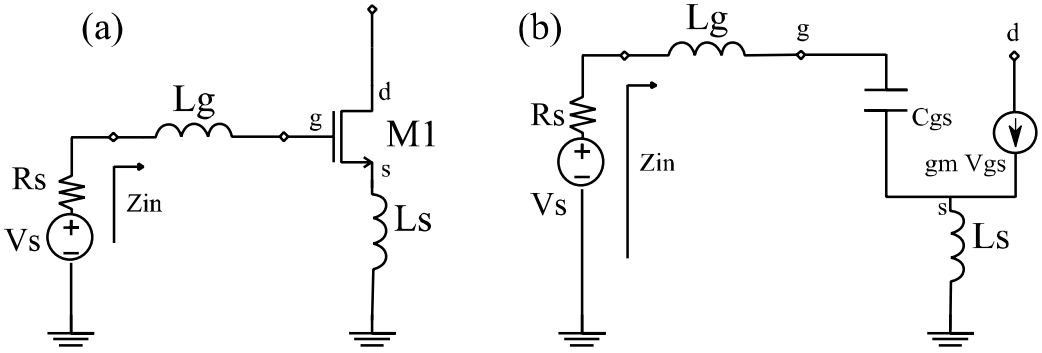

Figure 41 : MOS Transistor matched with Lg & Ls (a) and small-signal equivalent circuit (b)

The MOS SMTA S-parameters measurement (with L_s and L_g) allows the extraction of MOS $C_{gs\_extracted}$ capacitance at resonance frequency of the SMTA (f_{c1_meas}). However, L_{g_meas} and L_{s_meas} inductances have also to be measured separately. Furthermore, the $C_{gs\_extracted}$ capacitance can be extracted from MOS SMTA with L_{g_meas} and L_{s_meas} test structure using these equations:

$$C_{gs\_extacted} = \frac{1}{2\pi f_{c1\_meas}{}^2 (L_{s\_meas} + L_{g\_meas})} \quad (2.18)$$

$$g_{m\_extacted} = \frac{50 * C_{gs\_extacted}}{L_{s\_meas}} \quad (2.19)$$

The test structure of MOS with matching inductors (SMTA) has been integrated in GSG test structure in the same module as the MOS transistor, inductors, and dummies.

2.4.3. SMTA module for characterization of two RFMOS transistors

Using the method presented in previous sub-section, a test module including MOS transistors, a first SMTA with 2 stages, and matching inductors have been fabricated in a BiCMOS 0.25µm technology. High frequency on-wafer measurements are carried out. The S-parameters of MOS transistors (with and without network matching) and of matching inductors on test module are measured from 100MHz to 50GHz frequency range.

The SMTA schematic is shown in figure 42. It consists of two stages; the first stage has been matched for MOS characterization as explained in section 2.3.2. It provides an input impedance matching at 50Ω. The second stage is added for higher transmission gain and better output impedance matching. However, the first stage matching is realized as explained above and allows the extraction of the $C_{gs\_extacted}$ capacitance and $g_{m\_extacted}$ transconductance. The f_{c1} frequency is chosen close to the transistors cut-off frequency f_T (35GHz) that is equal to 32GHz. The source inductance L_s is calculated from the real part of the classical matching technique given in equation (2.17). Its simulated value is equal to 220pH. After setting the value of L_s, the gate inductance L_g (565pH), is calculated. It should be noted that the interconnect parasitcs can have a non-negligible impact on central frequency drift (f_{c1}). In this SMTA design, the impedances L_{in} and L_{g2} are added in order to include the impact of parasitics. The approximate values of the interconnect line inductances are calculated first by the following equation [20], and confirmed by the Momentum simulation:

$$L_{interc} = \frac{\mu_0}{2\pi} L \left[ln\left(\frac{2L}{W+T}\right) + 0.50048 + \frac{W+T}{3L} \right] \qquad (2.20)$$

Where, L is the interconnect length, W is the interconnect width and T is the interconnect thickness. It can be seen from the zoom shown in figure 42 that L_g is the sum of L_{in}, L_{g1}, and L_{g2} and resonates with the intrinsic capacitance of the transistor C_{gs} at the chosen frequency f_{c1}.

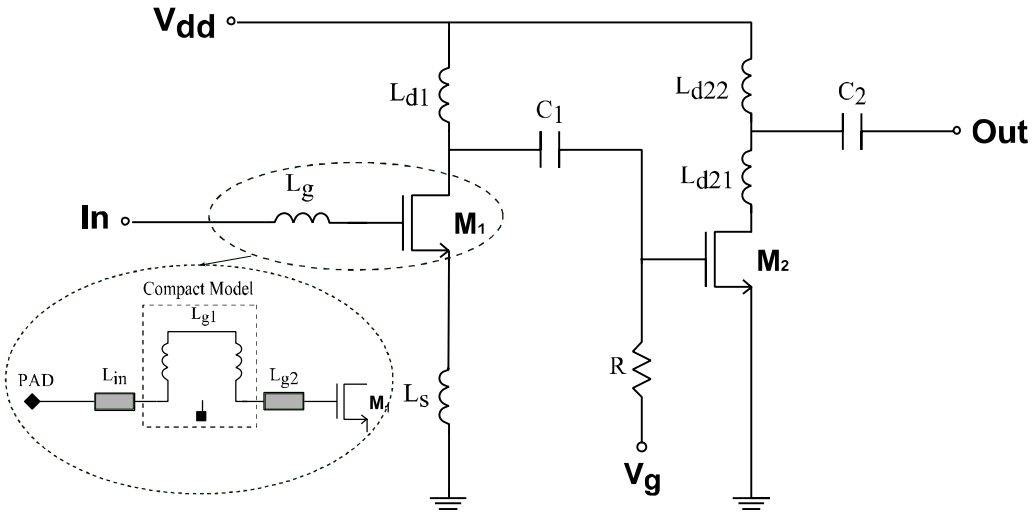

Figure 42 : Schematic of the 30GHz single-ended LNA

2.4.4. SMTA results and parameters extraction

The measured and simulated value of the inductance L_g, which is composed by L_{g1} connected to the interconnect lines presented in figure 42 by parasitic impedances (L_{in}, L_{g1} and L_{g2}) is shown in figure 43. The sub-section composed by L_{g2}, L_{in}, and L_{g1} is measured separately on silicon and simulated using the Momentum simulator. The simulated sub-section value was used in the calculation of the matching network (the value of the whole L_g presented to the gate of the transistor is fixed to resonate at the desired frequency), and the measured sub-section value is used in the calculation of the parameters extracted from the smart matched transistor architecture ($C_{gs\_extracted}$ and $g_{m\_extracted}$).

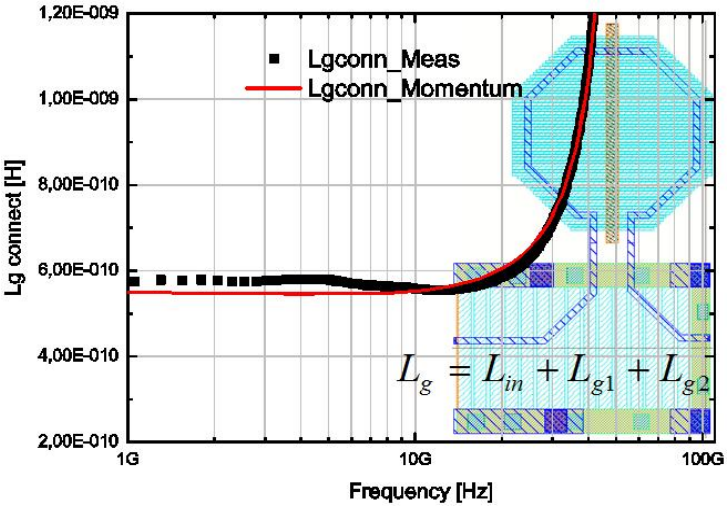

Figure 43 : The self-inductance of the Lg sub-section used for matching of the transistor

The measurements of the module (inductors and SMTA) allow the extraction of f_{c1_meas} frequency (the operating frequency of the S-parameters measured) and of the inductance measured L_{g_meas} presented in figure 43. The four measured and simulated S-parameters are represented in figure 44. The f_{c1_meas} frequency is extracted from S21 parameter measured peak and is close to 30GHz. The measurements of the inductors allow the calculation of the gate-source capacitance $C_{gs\_extracted}$ using equation 2.18 (L_g=585pH and L_s=245pH extracted from measurement and layout view, respectively) that gives a $C_{gs\_extracted}$ capacitance equal to 33.5fF. The $g_{m\_extracted}$ is extracted using the equation 2.19 with a value extracted equal to 7 mS. These values are closer to previous MOS transistor characterizations (see table 3).

The top-level simulations of the circuit are performed with SpectreRF and are compared in the same figure with measurements (figure 45). S-parameters are obtained by the simulation of post layout view that includes RLCk parasitic (k is the mutual coupling). The layout parasitic are taken into account by using the Partial Element Equivalent Circuit (PEEC) method available in QRC extraction tool of NXP design kit developed with Cadence and verified up to 50GHz.

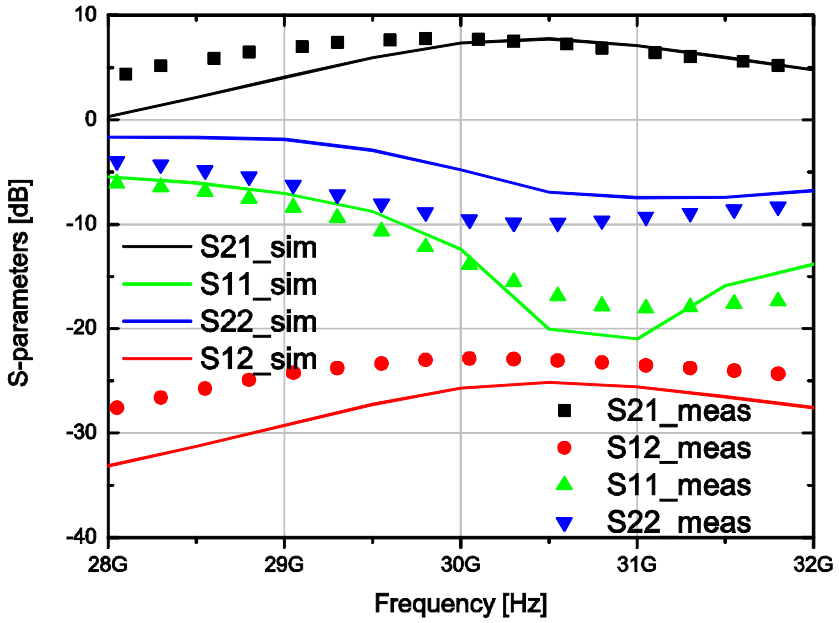

Figure 44 : Measured and simulated of S-parameters of the SMTA

The SMTA with 2 stages show a peak gain of 8 dB at the central frequency of f_{c1} = 30GHz and fits simulation quite well. The input (S11) and output return losses (S22) measured are better than -10dB, indicating quite good input/output matching at fc1. A shift towards high frequency is observed in simulation with respect to measurement, caused by the approximation of the interconnect parasitics inductance values. The S12 is better than -25dB indicating that parasitic coupling through the silicon substrate is very small. The stability factor (k) measured is larger than 2.5 and delta is smaller than 1, showing that SMTA is unconditional stable (see figure 45).

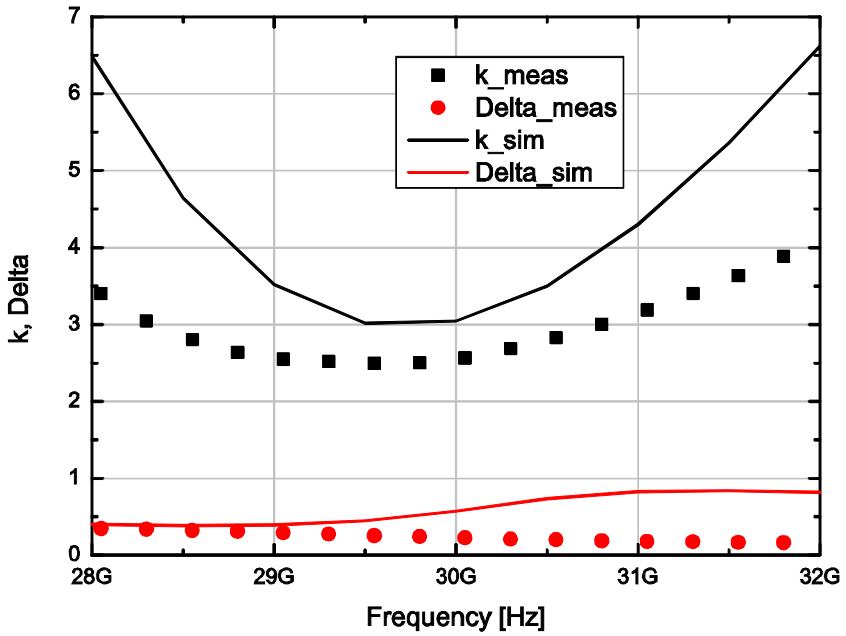

Figure 45 : Measured and simulated stability factors of the 30 GHz LNA

The most common stability factors (k and Δ which are directly calculated from S-parameters) ensure unconditional stability when k is above 1 and Δ is between 0 and 1.

Parameter extractions accuracy of the device is crucial when it comes to their use in specific blocks such as low noise or power amplifiers. To maximize the performance of the circuit, it was crucial to consider the correct parameters extracted and the criteria of optimization. For instance, from this study and when the layout does not add considerable extra capacitance parasitics (taken into account in QRC extraction), the gate-source capacitance extracted ($C_{gs\_extracted}$) and the transconductance extracted ($g_{m\_extracted}$) determined by equation 2.18 and 2.19, respectively, will not be much affected by the layout effects and the impedance matching calculation values remain correct in a mm-wave frequency.

The parameter values extracted from device level characterization and circuit level characterization are shown in table 3.

Calculation		Device level extraction				Circuit level extraction	
L_{s_cal}	L_{g_cal}	L_{s_extr}	L_{g_extr}	g_{m_extr}	C_{gs_extr}	g_{m_extr}	C_{gs_extr}
220 pH	565 pH	245 pH	585 pH	7.3 mS	32 fF	7 mS	33.5 fF

Table 3 : Comparison of parameters extracted from device characterization and circuit level characterization

The values from circuit level extraction are close to previous MOS level transistor characterization. The results validate the equations used for extraction from circuit level. That means also that under certain accurate measurement at device level and under a good choice of the design techniques (circuit level), the design kit of 0.25µm BiCMOS mature technology show good circuit performances and could be used to design a preferment circuit at millimeter wave frequency.

2.4.5. Conclusion

In this section, a novel methodology for high frequency characterization up to mm-wave range and small signal equivalent circuit extraction is proposed. This methodology allows the definition a smart 50Ω matched test structure for the characterization of transistors in GSG probe pads. The method is validated on a test module based on RFMOS transistor fabricated in BiCMOS 0.25µm technology from NXP Semiconductors. The results of matched RFMOS transistors at 30GHz are presented and show good agreement between measurements / extractions and calculations.

2.5. SMTA verification using two RFMOS with a double gate width

This section, presents a 24GHz Amplifier circuit demonstrator designed and fabricated in the same process than the SMTAs (0.25µm BiCMOS mature technology from NXP Semiconductors). The demonstrator is designed in order to evaluate the effect of the interconnect lines on impedance matching. The matching methodology is improved by considering the interconnect lines (from the Layout view) in the matching networks using RLC extraction. Schematic circuit simulations and measurements are used to evaluate the amplifier circuit performances.

2.5.1. Equivalent circuit for interconnect lines

The interconnections between passive / active devices in RF circuit designs are key challenging for designers when it comes to millimeter wave frequency. The octagonal inductors offer smaller dimensions and well defined analytic solutions that speed up the design (ex. Amplifier impedances matching), but are more difficult to connect in “layout” and susceptible to coupling discrepancies in the design performances. High frequency CMOS devices which require quite high quality factor are primarily limited by passive devices [21-22]. The interconnect lines can therefore add resistive, capacitive, and inductive parasitic in the whole circuit. As a result, these parasitics may deteriorate the circuit performances, due to both the high frequency significant effects. The parasitic (L, R, C) can be modeled based on the electromagnetic (EM) simulations using an elementary equivalent circuit as shown in figure 46. In the interconnect lines equivalent circuit, the series inductance and resistance are represented by L and R respectively. The capacitances between the signal line and the ground metals are considered with the capacitors C1 and C2. The extraction of the equivalent circuit is realized for each interconnection between two RF devices (e.g. inductor and MOS transistor) of the design shown in figure 49. The extracted values for each interconnect line are given in table 4.

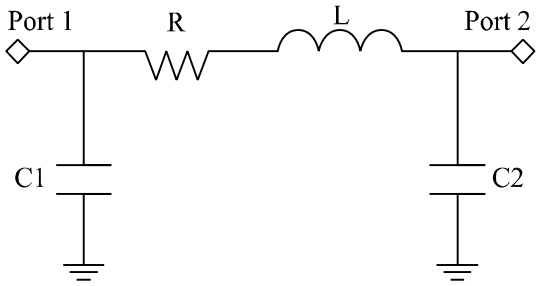

Figure 46 : Predictive interconnect equivalent circuit on single-Pi configuration

Designing high performance CMOS circuits is more difficult in high frequency applications [24-25] due to interconnections and back-end complexity. From design methodology point of view, the interconnections between all devices are considered as inductive impedances and are accounted in the matching impedances of the designed circuit. So, the interconnect lines are connected to single-loop inductors to form the input/output impedances matching. As shown in figure 49, the impedances $L_{g1}$and L_{g2} of the interconnect lines ($IL_{g1}$and IL_{g2}), are added in the input impedance matching. The L'_g inductance (see eq. 2.21) is considered as the sum of L_{g1}, L_g, and L_{g2} which resonates with the intrinsic capacitance of the transistor T1(C_{gs}) at desired frequency f_{c1} (idem for input/output and inter stage impedances matching). The interconnect line between the input pad and the octagonal inductor (L_g) is shown in fig 47 using the L_{g1} inductance.

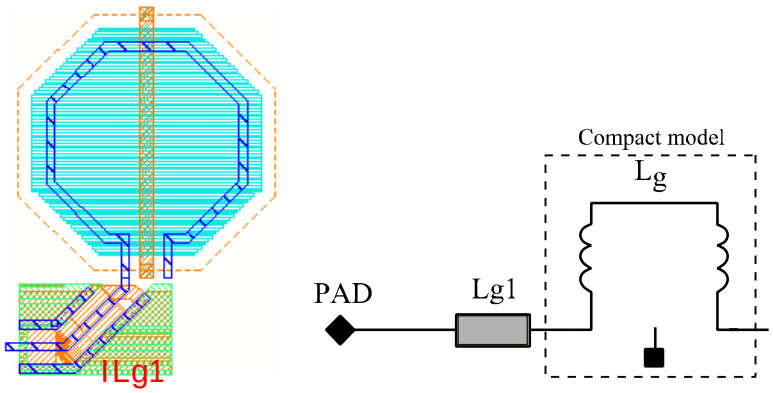

Figure 47 : Interconnection between input pad and compact model inductor. All interconnections are included in simulation

The parameters of the interconnect lines used in demonstration design and their associated values are summarized in table 4. The values depend on the length of the interconnect lines.

Interconnect lines	L (pH)	R (Ω)	C1 (fF)	C2 (fF)
ILg1	96.0	0.842	7.11	4.14
ILg2	75.0	0.181	3.70	1.60
ILs1	54.0	0.160	3.00	3.00
ILd1	48.0	0.160	3.02	3.02
ILis	108	0.866	5.60	6.54
ILin2	41.0	0.144	2.60	2.60
ILd11	80	0.144	2.64	2.60
ILd22	57	0.180	3.02	3.02
ILout	164	0.900	8.80	10.9

Table 4 : Summary of interconnect line parameters

From the table 4, it can be seen that the interconnect lines have an equivalent inductance values of a few tens of picoHenries, values which are non-negligible when it comes to millimeter-wave impedance matching designs.

To validate the equivalent circuit proposed for the interconnect lines, the S-parameters obtained with EM simulation and obtained by the simulation of the extracted equivalent circuit are compared. In figure 48 are shown the S-parameters simulated with Momentum simulation of the interconnect line (ILg1) compared to the simulation of the proposed (RLC) model. The EM simulation and the equivalent circuit simulation match very well up to 50GHz. A set of probe pads has been also simulated with Momentum and used to extract pad parasitics. Pad capacitances are used in the hierarchical schematic shown in figure 49 to obtain the behavior of the entire amplifier without de-embedding.

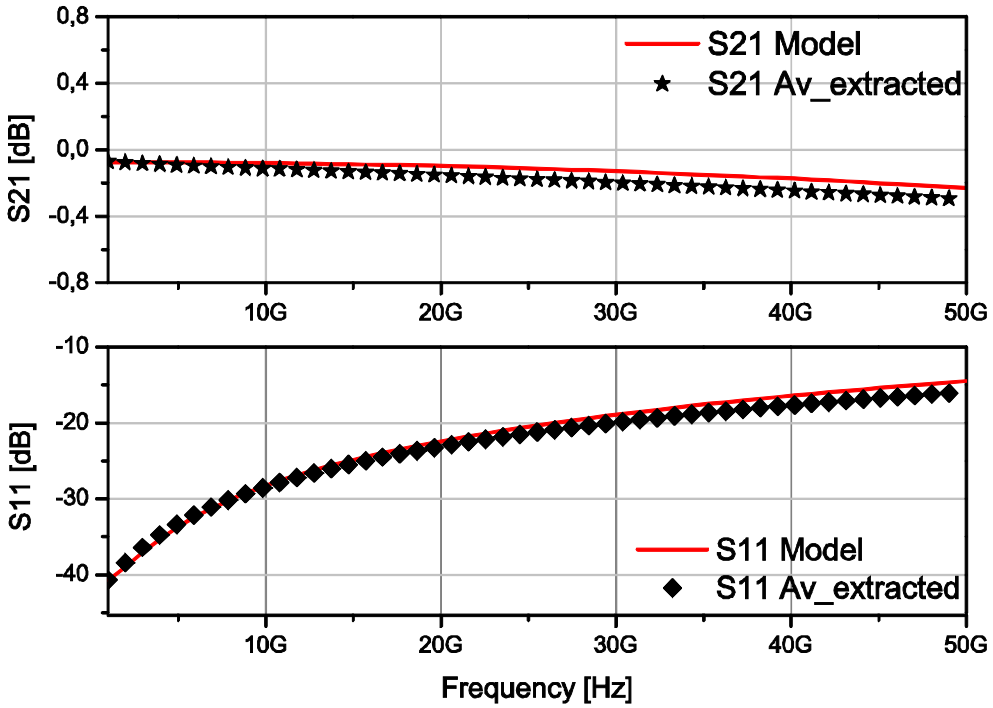

Figure 48 : S11 and S21 parameters of the interconnect lines equivalent circuit

2.5.2. Influence of the interconnect lines in the matching network

The schematic of the two stages cascaded circuit amplifier is shown in figure 49. The circuit has been implemented in the 0.25µm Technology of NXP Semiconductor's. The two cascaded stages architecture are selected here for getting better performances, considering also that small transistors (40µmx0.25µm) are used and 50Ω input and output matching condition must be satisfied. The second stage is then added for higher transmission gain and better output impedance matching. The values of C_{gs} and g_m depends on transistor sizes. Their values were extracted from the single transistor characterization. The input impedance Z_{in} of the MOS transistor represented in figure 49, with inductive source degeneration is:

$$Z_{in} = \frac{L'_s g_m}{C_{gs}} + j\left((L'_s + L'_g) 2\pi f_{c1} - \frac{1}{C_{gs} 2\pi f_{c1}} \right) \quad (2.21)$$

Where, L'_s is an inductance in series with MOS transistor source, and L'_g is added in series with the gate. Based on this equation, a resonance frequency is obtained when the imaginary part is 0. Thus, the amplifier allows the measurement of S-parameters of transistor matched to 50Ω around a resonance frequency given by f_{c1}.

First, the L'_s inductance is calculated from the real part of Z_{in} that we want to attain as close as possible the VNA characteristic impedance of 50Ω ($L'_s = \frac{50 \cdot C_{gs}}{g_m}$). At higher frequencies, the C_{gs} capacitance of T1, that has a small value (C_{gs}=64fF for 40µmx0.25µm transistor), makes the transistor input impedance very low and leads to measurement inaccuracies. To avoid this low input impedance, L'_s is added with "a real part" contribution to the overall impedance seen from the transistor gate that matches to 50Ω. Thus, the input impedance is purely resistive at the resonance frequency fc1 (see eq. 2.21).

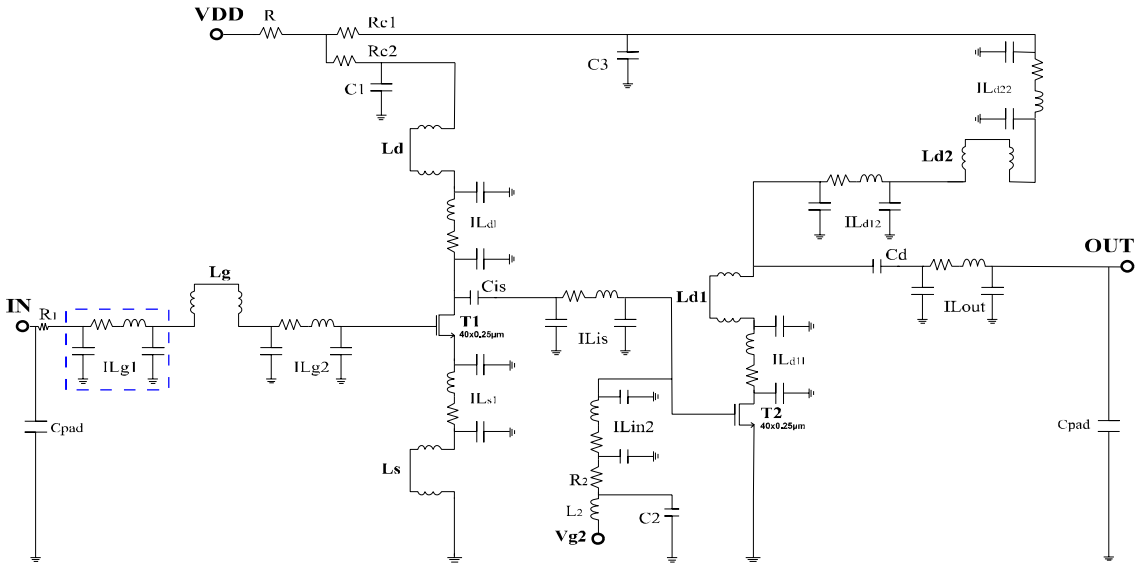

Figure 49 : Schematic of the 24GHz single-ended circuit demonstrator

Second, with gm and C_{gs} which are previously extracted from single transistor measurements for the 40µmx0.25µm transistor, with L'_s calculated as presented above, and f_{c1} chosen upon the measurement range needs, L'_g is calculated from

the imaginary part of eq.2.21. L'_g is equal to $L'_g = \frac{1}{C_{gs}\cdot(2\pi f_{c1})^2} - L'_s$. The L'_g inductance can be also calculated using the Smith Chart technique [23] after setting the value of $L'_s$and using commercial simulators (e.g. SpectreRF tool from ®Cadence). The effect of parasitic resistances and parasitic capacitances at transistor level, between gate, source, and drain terminals and between interconnect lines and the substrate are taken into account by the simulation of the "extracted view" of transistor "layout" with its interconnections. The extraction of the transistor is realized using the RLCk extraction (k is the mutual inductance) available in QRC extraction tool of NXP design kit developed with Cadence and verified up to 50GHz. In this extraction the signal, power, and ground nets are explicitly extracted, resulting in a matrix that captures also the magnetic couplings (the transistor intrinsic model is not extracted by the tool, the transistors are defined as a pCell).

The stability characteristic of the amplifier is given by K and Δ [24]:

$$K = \frac{1+|\Delta|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{12}||S_{21}|} \quad (2.22)$$

Where, $\Delta = S_{11}S_{22} - S_{12}S_{21}$. The amplifier is unconditional stable for $K > 1$ and $|\Delta| < 1$. The stability factors are shown in figure 51, indicating unconditional stability of the amplifier circuit.

Prior to the detailed circuit design, a tradeoff study between different transistor sizes was carried out. The f_{c1} frequency (24 GHz) is chosen quite close to the transistor cut-off frequency f_T which is equal to 35GHz.

2.5.3. SMTA performance results

High frequency on-wafer measurements are carried out with an Agilent 8364B network analyzer with ground-signal-ground (GSG) probes. On-wafer LRRM calibration is used. The S-parameters of CMOS circuit amplifier are measured from 100MHz to 50GHz. The simulations of the circuit are performed with

SpectreRF and are compared in the same figure (figure 50) with measurements. S-parameters are obtained by the simulation of hierarchical schematic circuit shown in figure 50. The layout parasitics at transistor level are taken into account by using the RLCk extraction.

The amplifier achieves a peak gain of 11 dB, and input (S11) and output return losses (S22) measured are better than -12dB, indicating good input/output matching at the working frequency (fc1). A shift towards the high frequency is observed in simulation with respect to the measurement of S11. The S12 is better than -23dB indicating that the parasitic coupling through the silicon substrate is very small. The measured NF is about 7.6 dB at 24GHz. The stability factor (k) measured is larger than 1.9 and delta is smaller than 1 (see figure 51), showing that the amplifier is unconditional stable [24].

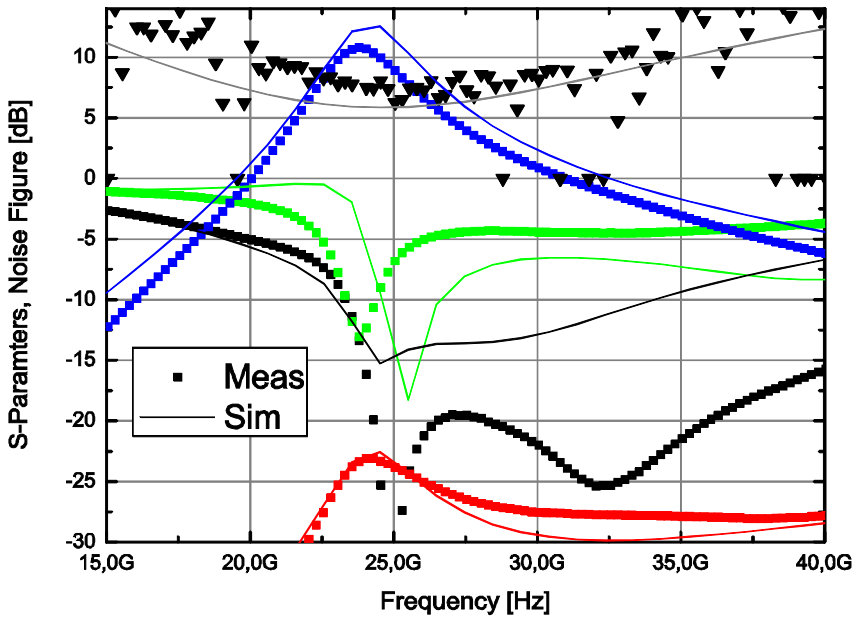

Figure 50 : Measured and simulated S-parameters of the circuit demonstrator

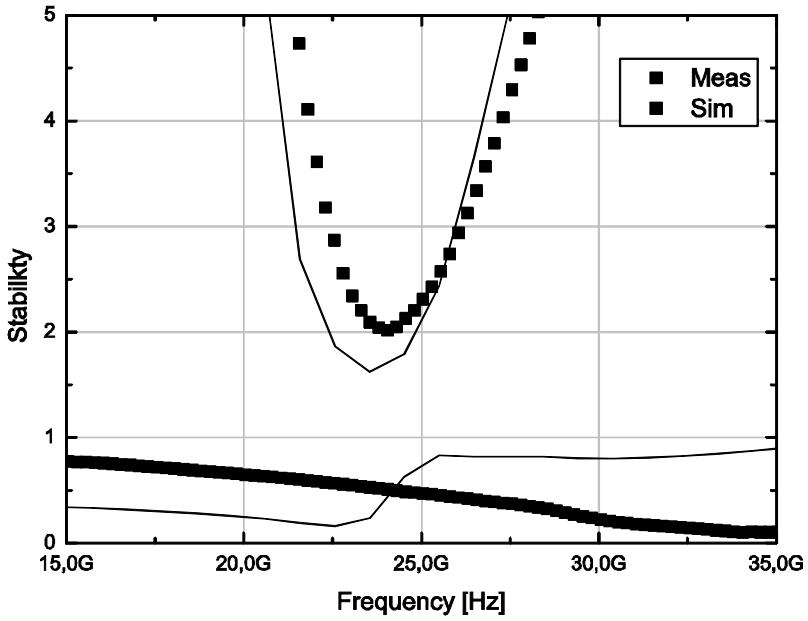

Figure 51 : Measured and simulated stability factor of the circuit demonstrator

2.5.4. Conclusion

In this section, A 24 GHz circuit demonstrator for high frequency model validation is proposed. This circuit demonstrator is based on a modified impedance matching networks that allows high simulation accuracy at frequency close to MOS transistor f_T. The interconnect lines are used together with octagonal inductors to calculate / simulate the matching networks of the demonstrator. The results of the circuit, showing good agreement between measurements and simulations at 24GHz, demonstrate the accuracy of device models above 20GHz.

2.6. Summary

In this chapter, the MOS and inductor characterization at device and circuit levels are presented. The approach of characterizing at device level is based on the NXP available method with improvements of test structures in order to obtain more accuracy at higher frequencies.

The characterization at circuit level is a new methodology dedicated to high frequency characterization up to mm-wave range and small signal equivalent circuit extraction in reduced frequency band. The approach followed in this chapter allowed first, understanding of the high frequency limitations of devices at circuit, by analyzing the whole elements such as inductors, interconnect lines, and transistors. Secondly it allows the extraction of some parameters from circuit measurements. This is possible by matching a transistor under test to 50 Ohms (impedance of measurement equipment). The transmission gain of the common source transistor is improved in the frequency band of interest. The method is validated on a test module based on RFMOS transistor fabricated in BiCMOS 0.25µm technology from NXP Semiconductors. The results of matched RFMOS transistors at 30GHz are presented and show good agreement between measurements/extractions and calculations (e.g. for C_{gs}).

In the last part of this chapter, A 24 GHz circuit demonstrator for high frequency range is also proposed for model validation. This demonstrator is based on a modified impedance matching networks which include the interconnect lines together with the octagonal inductors to obtain accurate simulations. The results of the circuit at 24GHz are presented and show good agreement between measurements and simulations. The design demonstrates then the design kit validity at micro and millimeter wave frequencies.

2.7. References

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Chapter 3: Methodology for improved extraction of bipolar equivalent circuit from measurements at mm-wave band

Chapter 3 Methodology for improved extraction of bipolar equivalent circuit from measurements at mm-wave band

3.1. Introduction

This chapter presents the characterization and modeling of the bipolar and matched bipolar transistors. DC and RF characterization of bipolar transistor is detailed. The extractions are performed using RF test structures where the emitter and the substrate are connected to the ground. The parameters of the Mextram model are extracted directly from the measured data [1].

3.2. Mextram equivalent circuit for vertical NPN transistor simulation

Within NXP Semiconductors, we use the Mextram 504 Compact model for bipolar transistor modeling. The Mextram model equivalent circuit for the vertical NPN transistor is shown in figure 52 [2]. It describes the various currents and charges which are the main part of the model and form the equivalent circuit. The currents are presented through the common resistances, diodes, and controlled current sources. The charges are presented by the various depletion and diffusion capacitances. The intrinsic part of the transistor is presented by the bleu dashed lines square in the figure and the exterior part is the extrinsic transistor.

In the Mextram, the main current is presented by the controlled source current given by I_N, where the depletion charges Q_{tE} and Q_{tC} and the diffusion charges Q_{BE} and Q_{BC} are included in current equation (See Appendix A, DC model). The total base current has a bottom and sidewall contribution. The ideal base current is presented by a diode and given by I_{B1}, and the I_{B1}^{S} (extrinsic part) is the ideal base current follow through the sidewall (the pn-junction between base and emitter is not only present at the intrinsic region bellow the emitter, a part of the I_{B1} will fellow through the sidewall). The non-ideal forward base current originates from the combination in the depleted base-emitter region is given by

IB2. The reverse base current, is affected by high injection and partitioned over the two external base-collector branches (B1 and C4). It is given by Iex and IB3 is the non-ideal reverse base current originates from the combination in the depleted base-collector region. The current fellow in the case of forward bias in the substrate-collector is the current Isf.

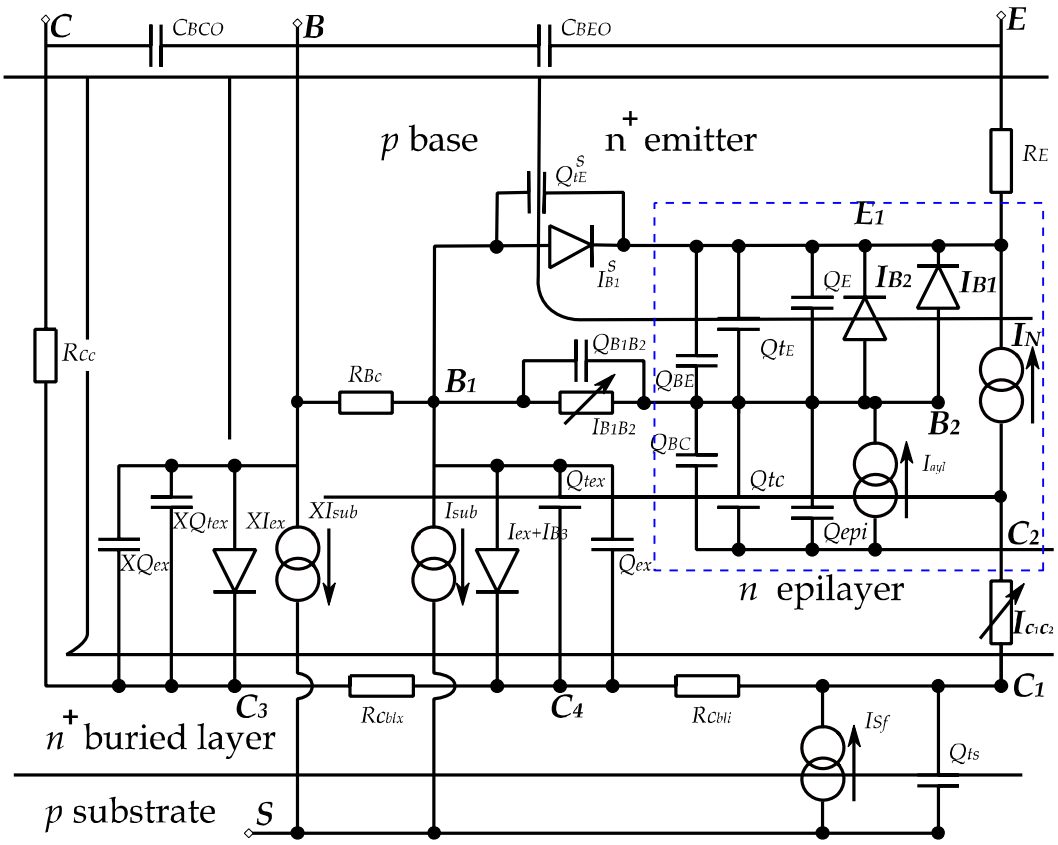

Figure 52 : The complete Mextram equivalent circuit for the vertical NPN transistor

The model contains constant, series resistors at the base, emitter and collector terminals, R_{Bc}, R_E, and R_{Cc}, respectively. The resistances of the buried layers underneath the transistor are represented by two constant, temperatures dependent resistances R_{Cblx} and R_{Cbli} [3]. The base resistance is divided in a constant part R_{Bc} and a variable part given by $I_{B_1B_2}$.

The model has two overlap constant capacitances. C_{BEO}, which is the base-emitter overlap capacitance and C_{BCO}, which is the base-collector overlap

capacitance. The noise is included in various branches of the model. All resistances have a thermal noise (R_E, R_{Bc}, R_{Cc}, R_{Cblx}, R_{Cbli}, R_{Bv}), all diodes like currents have shot-noise (I_N, I_{B1}, I_{B1}^s, I_{B2}, I_{B3}, I_{ex}, XI_{ex}, I_{sub} and XI_{sub}), and all base current also have flicker-noise (1/f noise) (I_{B1}, I_{B1}^s, I_{B2}, I_{B3}, I_{ex} and XI_{ex}) modeled with a pre-factor K_f and a power A_f (See appendix A, DC model).

The Mextram is very accurate for bipolar transistor simulations and it contains many features that the widely Gummel-Poon model lacks [4]. In this section, the objective is not to introduce the physical origins of the Mextram model but only to use it as medium when discussing some model components (ex. capacitances) effects which will be discussed later in the chapter. The equivalent circuit we use for small signal equivalent circuit characterization (discussed in section 3.4.2) is only a simplification of the full Mextram model presented in figure 52.

3.3. Measurement and simulation setups used for characterization

The vertical NPN transistors fabricated in BiCMOS 0.25µm process from NXP Semiconductors are characterized and modeled. The transistors measured are NPN type transistors (emitter width W of 0.3µm, length L of 1um, and number of emitters respectively, E =20 and 5). Table 5 summarizes DC and RF measurement setups and conditions used to characterize the bipolar transistors. Most of the parameters are extracted from the DC measurements and high frequency measurement (S-parameters, in practice always converted to the Y parameters)). Available templates are used with several DC and RF measurement setups to characterize the DC and RF characteristics of the transistor. The setups available to extract the transistor parameters are implemented under:

- Forward measurements: the forward junction bias is increased while keeping the collector-emitter voltage constant. The reverse junction bias is constant. Quantities like Gummel plots and the input inductances are measured. The forward measurements are realized using the Gummel_dc setup given in table 5.

- Output characteristic measurements at least at three constant values of the base current. The output characteristic is extracted from the Current_dc setup given in table 5.
- Cbe depletion capacitance from special (off-state) S-parameter measurements. Measurements are done at 3.5GHz fixed frequency over a range of base-emitter voltage from -1V to 0.4V, with a step of 10mV. The collector-emitter voltage is set to zero.
- Cbc depletion capacitance is determined in similar way as the measurement of Cbe capacitance. The collector–emitter voltage is swept and the base-emitter voltage is set to zero.
- S-parameter setup measures the S-parameters in common emitter configuration in the forward operation regime. The measurements are performed with a frequency sweep for all bias voltages.
- Measurements over a large range of collector, base, and emitter conditions and over the frequency range, respectively for DC and RF characterizations.

Measurement setups	Vc [V]	Vb [V]	Ic [A]	Ib [A]	Freq [Hz]	S-par
Gummel_dc	1	0.2→1 step 10mV	m	m		
Vaf_Vce	0.3→2.5V step 100mV	0.6→0.7V step 50mV	m	m		
Current_dc	-0.3→1V step 100mV	m	m	(1,2,3)*Ae		
Cbe_ac	0	-1→0.4 (50mV)			3.5G	m
Cbc_ac	-1→0.4 (50mV)	0			3.5G	m
S-parameters_0	0	0			500M-110G 220pts/Dec	m
S-parameters	1	0.77			500M-110G 220pts/Dec	m
Bias_dc	0.5→2.5 (500mV)	0.7→1 (31pts)	m	m		m
Bias_ac	0.5→2.5 (500mV)	0.7→1			500M-110G 220pts/Dec	m
Freq_bias_ac	1	-1→0.4 (50mV)	m	m		
Cbe_Cbc_60GHz	0.5	0.7→1(50mV)			60G	m

Table 5 : Setups of DC and RF measurement and bias ranges used for bipolar and matched bipolar characterization

To extract the transistor parameters it's important that the measurements are realized over a large range of collector, base and emitter bias conditions. For most

of the conditions given in table 5, the S-parameters are measured allowing Y-parameters calculation and then small signal equivalent circuit extraction. At higher frequencies, Y-parameters describe the behavior of the internal structure of the device under test. Y-parameters are also the base for estimation of specific designs parameters.

3.4. Single Transistor (ST) characterization and extraction

RF characterization and verification have been realized for bipolar transistor within 0.25µm BiCMOS technology. High frequency on-wafer measurements are carried out with an Agilent 8510C network analyzer with ground-signal-ground (GSG) probes. On-wafer SOLT / LRRM calibration and open-short de-embedding method are used. The S-parameters of the bipolar transistors are measured from 100MHz to 110GHz.

The bipolar transistors have been successfully characterized at device level and at circuit level. Most of the characteristics like Gummel plots, forward and reverse current gain, output curves, depletion capacitances, fT and fmax are extracted from measurements and compared with the simulation of the compact model.

3.4.1. ST measured and simulated DC characteristics

The DC characterization allows verification of dispersion of DC characteristics over wafer due to process variations. The DC parameter extractions have been first performed from the on-wafer measurements. In the DC setups shown in table 5, several procedures have been implemented to allow the extraction of quantities like current gain Ic / Ib, Gummel plots, base and emitter resistances, etc. The description of extraction procedures of bipolar transistor implemented under ICCAP can be found in [5-6]. Figure 53 shows measured and simulated DC characteristics of the bipolar transistor (W0.3L1E20).

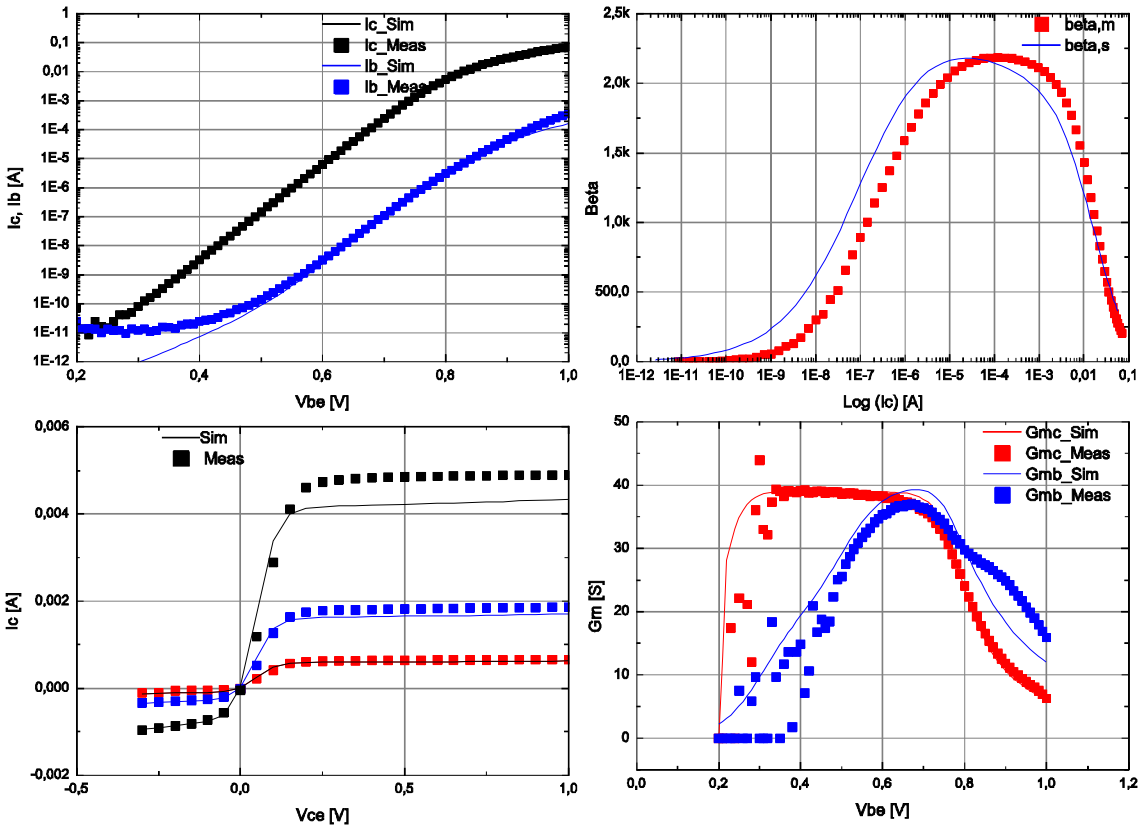

Figure 53 : Examples of measured and simulated DC characteristics

The Gummel plots (Ic, Ib) as a function of the base-emitter bias for Vbe [0.2V→1V, step of 10mV] and for Vbc=0V are presented on the top left of figure 53. Higher base current at Vbe close to 1V has been observed in measurement compared to simulation due to base and emitter resistances. An offset is also observed for low values of Vbe due the base-emitter diode recombination effect "knee effect". The collector saturation current Is of the intrinsic transistor has also been extracted from measurements. The extraction is realized at small values of Vbe when the series resistances may be neglected.

The plot on the top rights of the figure represents the measured and simulated current gain (Hfe=Ic/Ib) of the transistor. The measured gain at high current levels is significantly higher as simulated. The knee current I_K of the Mextram model can be tuned to fit the measurements of the current gain [1]. From the forward current gain Ic/Ib the ideal and non-ideal base current components are

extracted. From the decrease of the gain at the medium current levels (Vbe=0.6-0.7 V) the reverse Early voltage is extracted.

The output characteristic measured for three values of the base current is given on the bottom left of the figure 53. The measured results fit quite well with the simulation mainly in the quasi-saturation region. The collector resistance can be tuned for better fit in hard saturation and normal regions. The reverse gain is extracted from the output characteristics where Vce is negative. The Knee current is extracted from the collector current where Vce is sufficient high to be in the normal (flat) region.

The plot on the bottom rights shows the normalized input conductance Gm/I=dI/dV/I of the base and collector current. A strong increase of the Gm/I of the base current at Vbe slightly above 0.8V can be noticed.

The base and emitter resistance extracted from Ning-Tang method [4] is given in figure 54. The resistance named in the plot (Rin) contains base and emitter resistance contributions.

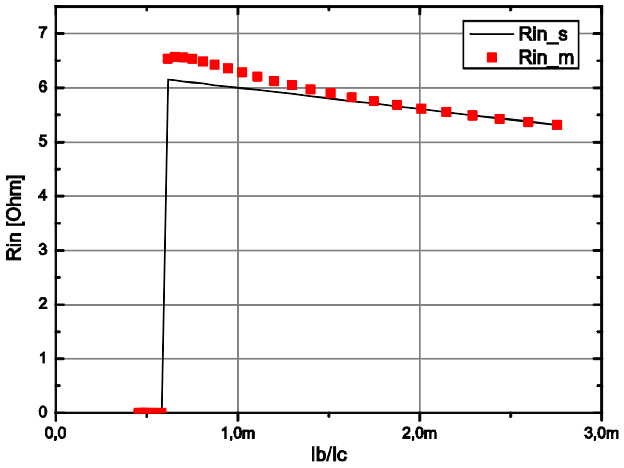

Figure 54 : Measured and simulated base and emitter resistances

The influence of the resistance is a factor of current gain since the collector current goes through the emitter resistance.

3.4.2. ST small signal equivalent circuit extraction

The small signal equivalent circuit of the bipolar transistor used for characterization for bipolar in mm-wave range is shown in figure 55.

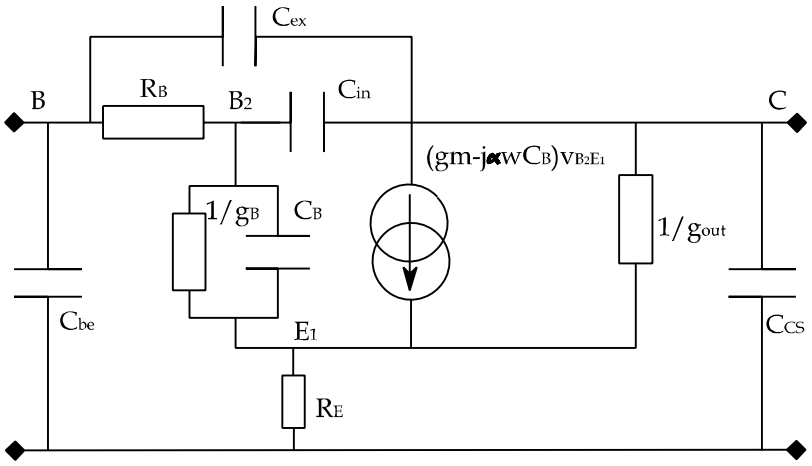

Figure 55 : Small signal equivalent circuit of the bipolar transistor

g_m is the intrinsic transconductance of the transistor, g_b is the conductance of the base, typically close to g_m/β [2], where β is the current gain. C_{be} is the extrinsic base-emitter capacitance, C_{in} is the base-collector depletion capacitance of the intrinsic transistor and C_{ex} is the base-collector depletion capacitance of the extrinsic transistor. Due to base-charge partitioning [2] a fraction α of the diffusion charge is not allocated to the emitter node, but to the collector node (the integral charge is composed by depletion charges Q_{tE} and Q_{tC} and the diffusion charges Q_{BE} and Q_{BC}, see figure 52). As a result, the effective transconductance is given by $g_{m,eff}$, with $g_{m,eff} = g_m - \alpha jwC_B$. In the Mextram 504 α is taken constant $\alpha=1/3$. V_{B2E1} is the internal base-emitter voltage.

Y -parameters of the bipolar W0.3L1E20 transistor as function of frequency are shown in figure 56. All imaginary parts have a linear variation with the frequency. The real part of Y21 is nearly constant. The real part of Y22 shows a small offset between measurements and simulations. This offset is due to the output conductance [2]. These curves are used to show the frequency dependency and to verify the high frequency model.

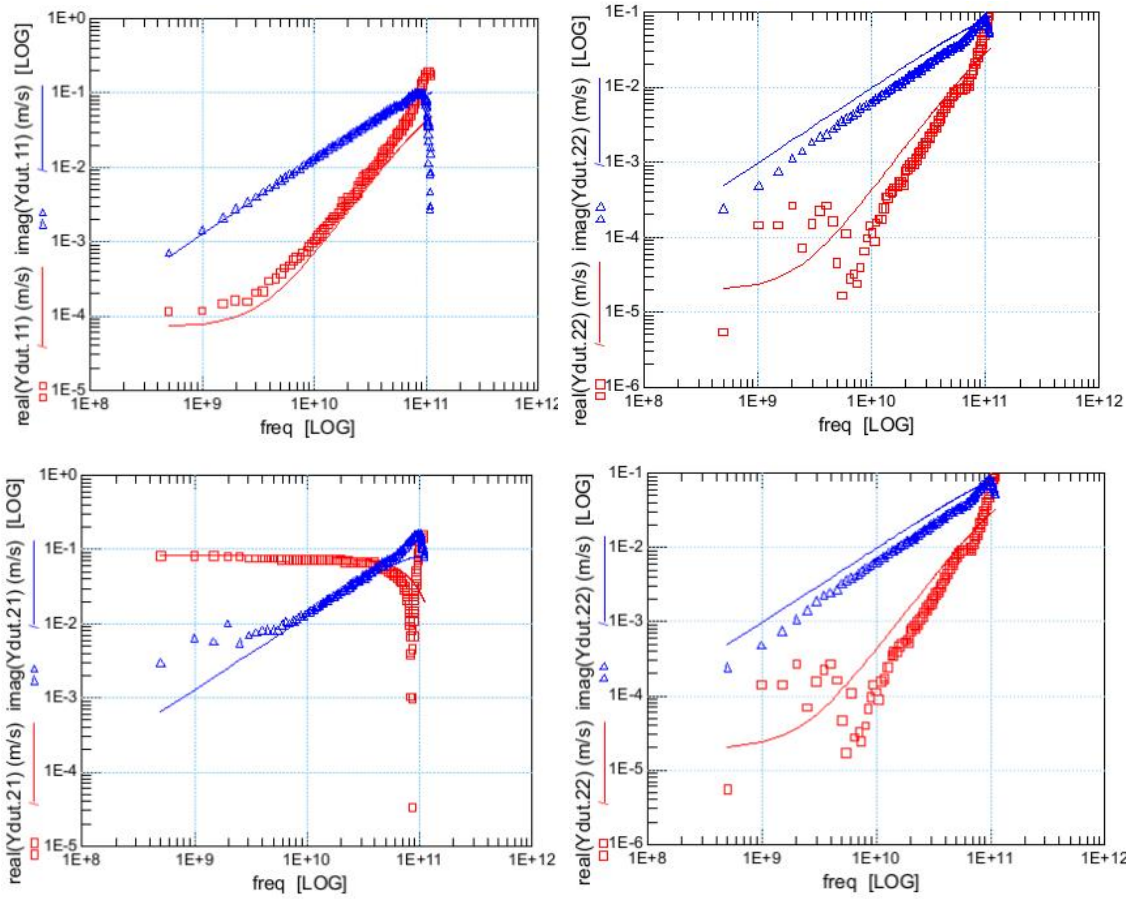

Figure 56 : Imaginary (bleu) and real part (red) of the four Y parameters Y11, Y22, Y21 and Y12

The base and emitter resistances are calculated from the RF measurements using the improved circle impedance method presented in [7]. The extracted resistances are presented in figure 57 versus Ic current.

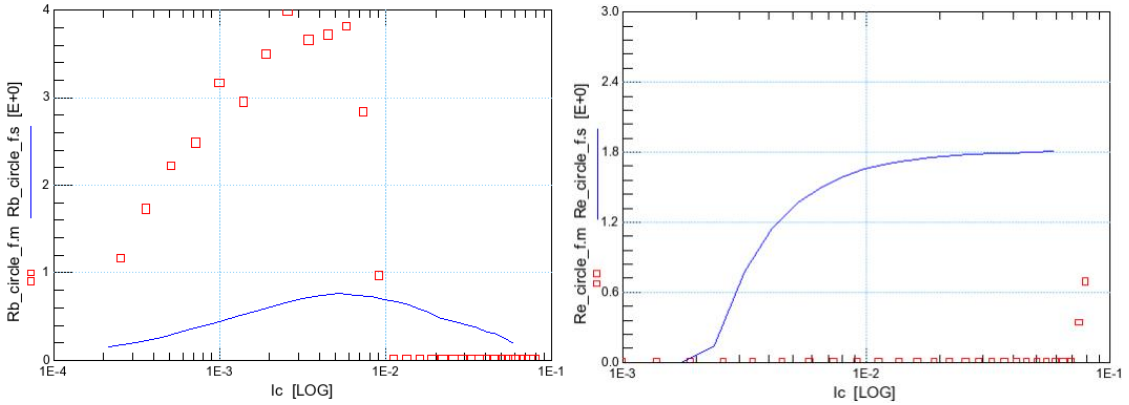

Figure 57 : Measured and simulated base and emitter resistances

The capacitances of the transistor are extracted from Y-parameter measurements. First, the cold-state measurements (i.e the transistor is off state; all junctions are reverse or very limited forward biased) are used to extract the depletion capacitances. Then, the on-state measurements are used to extract the depletion and diffusion capacitances. After de-embedding of the measured S-parameters [8], the Y-parameters used to extract the capacitances by means of these equations [4]:

$$C_{bc} = C_{in} + C_{ex} = \frac{-Imag\,(Y_{12})}{w} \tag{3.1}$$

$$C_{be} = \frac{Imag\,(Y_{11}+Y_{12})}{w} \tag{3.2}$$

$$C_{sc} = \frac{Imag\,(Y_{22}+Y_{12})}{w} \tag{3.3}$$

The base-emitter C_{be} and the base-collector C_{bc} capacitances extracted from the cold-state Y-parameters of the DUT are shown in figure 58.

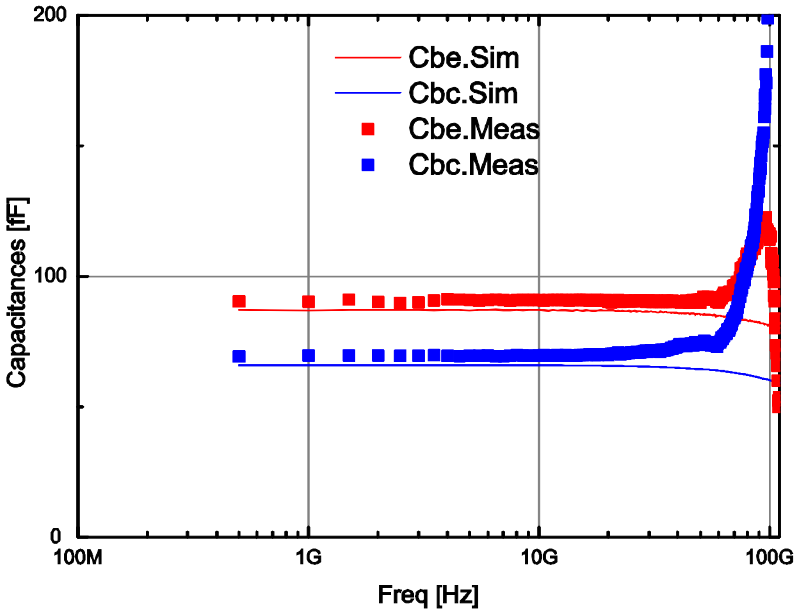

Figure 58 : Measured (markers) and simulated (line) depletion capacitances of W03L1E20 transistor for cold-state measurements

These measurements shown in figure 58 are performed versus frequency without bias (cold-state). From the figure, it can be seen that for higher frequencies, resonance appears at frequency higher than 60GHz. The capacitances extracted here remain constant up to 60GHz. Indeed it is common understanding that the compact model parameters of a device such as, for instance, its capacitances should be constant over the wide frequency range. The frequency choice for using of the small signal equivalent circuit in the design should be the lowest frequency that still has an acceptable noise level.

It should be noted that all the simulated capacitances have been obtained from the physical compact model simulations and compared to the measured capacitances. The equations (3.1, 3.2, and 3.3) are also used for the on-state Y-parameters measured of the DUT for Vbe=0.77V and Vce=1V. With biasing of the transistor, the contribution of the diffusion capacitances is also added to the depletion capacitances. In figure 59, the measured and simulated C_{be} and C_{bc} capacitances are presented. The capacitances are constant up to 60GHz.

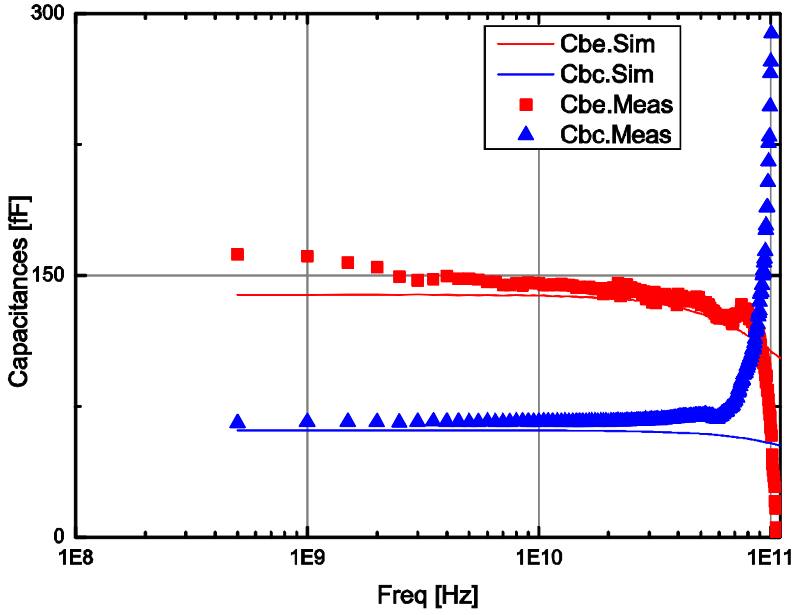

Figure 59 : Measured (markers) and simulated (line) depletion capacitances of W03L1E20 transistor for on-state measurements.

The C_{be} and C_{bc} capacitances are extracted over a range of base-emitter voltage [-1V→0.4V, step 10mV for Vce=0]. Figure 60 compares extracted C_{be} and C_{bc} capacitances from measurement and simulation at 3.5GHz.

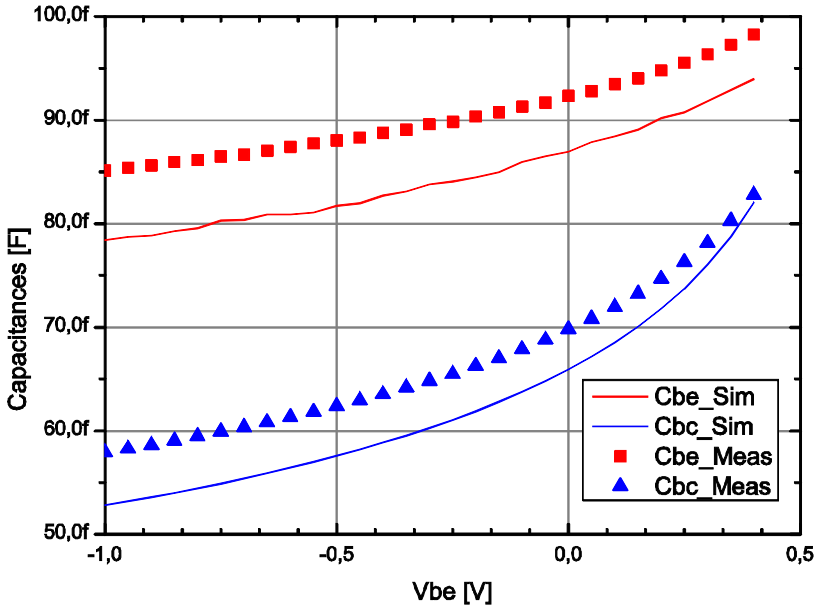

Figure 60 : Measured (markers) and simulated (line) base-emitter and base-collector capacitances extracted at 3.5GHz

The identification of the diffusion contribution from extracted capacitance is more difficult to obtain. However, the overall capacitance gives an indication of model accuracy which is very useful for designers. The C_{be} and C_{bc} capacitances shown in figure 60 can be used to estimate the depletion capacitances at low frequencies. This extraction is realized to show the capacitance bias dependency.

The extraction of capacitances at very high frequency is similar to that of the extraction at low frequency. Figures 61 and 62, illustrate the C_{be} and C_{bc} capacitances as a function of base-emitter voltages V_{be} [0.7 to 1V, step 0.1V]. The capacitances are extracted at a constant frequency of 60GHz. In this extraction, for more accuracy, the base-emitter voltage is swept from 0.7 V to 1 V instead of -1 to 0.4V in low frequency. The reason is that the diffusion voltage is between 0.5 and 1 V [1], this voltage determine the cross-over between junction charges and stored charges.

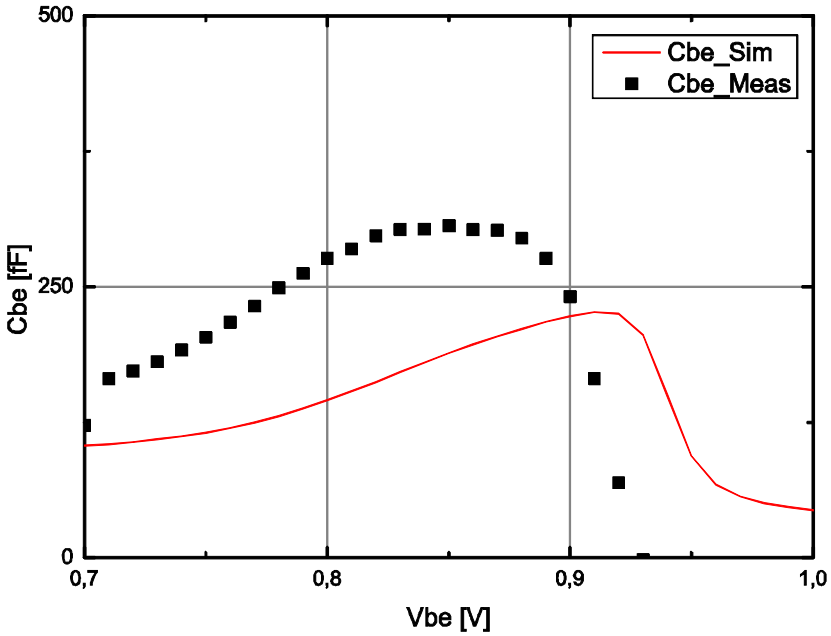

Figure 61 : Measured (markers) and simulated (line) base-emitter capacitance at 60GHz

From figure 62, it can be noticed that an increase in base-emitter voltage leads to a decrease of capacitance caused by an increase of electron density. This changes the charge distribution and consequently also the capacitance. Not that the reduction of capacitance is only visible in the measurements.

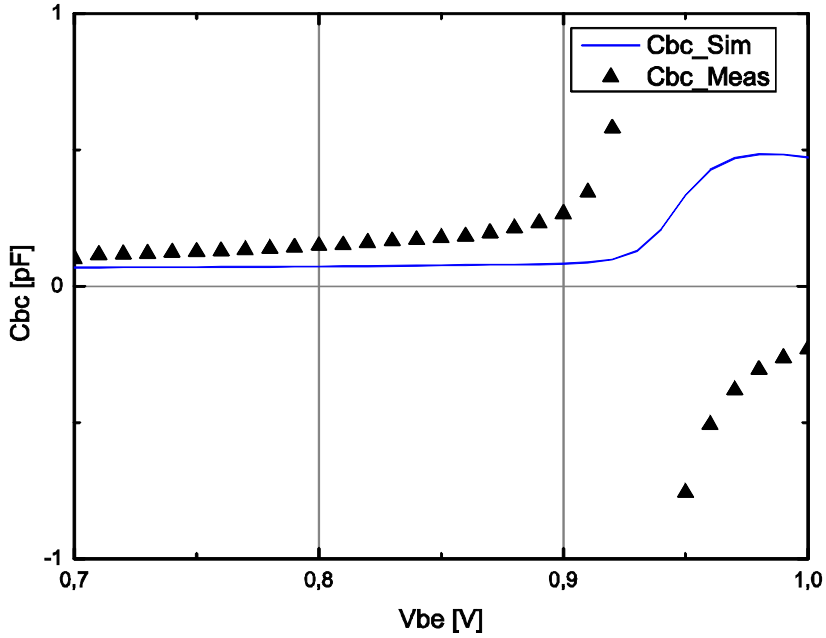

Figure 62 : Measured (markers) and simulated (line) base-collector capacitance at 60GHz

The capacitances extracted in on-state at 3.5 and 60GHz are key parameters for circuit design. The extractions led to the conclusion that the capacitance extracted at the bias chosen for the circuit at 60GHz is the more accurate for achieving input impedance matching (see section 3.5.2). For example, the base-emitter capacitance of 115fF has been extracted at Vbe=0.75V and will be explained more in detail in the SMTA design.

3.5. Smart matched bipolar transistor structure (SMTA) design and characterization

The method of impedance matching of a transistor under test used for MOS transistor presented in chapter 2 has been tested out for a bipolar transistor. The bipolar transistor (W0.3L1E20) is connected to GSG probe pads and matched to 50 Ohms within common emitter configuration. The measurements of the SMTA allow the extraction of the equivalent circuit parameters (e.g. capacitances). These capacitances are determined at high frequency band (60GHz). Therefore, the accuracy of simulations is improved using a better extraction method for capacitances. The module used to characterize the bipolar transistor includes the single transistor characterization set up and the SMTA set up.

3.5.1. SMTA design tradeoff

DUTs are always placed in test structures. Therefore, the test structures should be robust and have minimum influence on the characteristics of the device under test. Users of test structures must verify that the test structure contribution is accurately subtracted by de-embedding.

In this context, the test structure should satisfy the following specifications:

1. Surface area of pads must be minimized to provide minimal pad parasitic capacitances and / or must be considered in the matching network;
2. Measurements reference place must be located as close as possible to the terminals of the DUT;
3. Definition of the device terminals should be well defined for characterization (input and output of the intrinsic device, metal level best choice top or middle);
4. Additional implementation of elements (dummies) for quantitative verification of the calculation accuracy;
5. Dummy structures must be located near to the DUT.

3.5.2. Design and implementation of the SMTA

As the small signal characterization of active devices is usually made in common source/emitter configuration, the device in its test structure can be seen as an amplifier. The new SMTA proposed is composed by the DUT and the input/output matching networks. The purpose of this new structure is to amplify the signal received from VNA in the mm-wave band of interest and thus to improve the model extraction. The first step in this design procedure is to select the collector current (Ic). Ic is extracted from the single transistor characterization in order to obtain maximum transition frequency (fT). Then, the base and collector inductances are calculated in order to bring the circuit gain into narrow frequency band (resonance).

Once the bias and the transistor size are selected, the base and collector inductances (matching network) can be calculated using the Smith Chart [9] to provide input/output impedances matching to 50 Ohms. However, we can also calculate the matching network using the equivalent impedance calculation. For example, the value of the inductance in series with the base of the transistor, Lb can be given by equation (3.4):

$$L_b = \frac{1}{C_{be}(2\pi f_c)^2} \tag{3.4}$$

Where, Lb and Cbe have conjugate impedances to the frequency fc taken equal to 60GHz. The input/output pad parasitic capacitances affect the matching networks. The signal pads capacitances in this case are included in the matching networks and calculated using the matching conditions. Once the base inductor is calculated (Lb was determined to be 67 pH with Cbe=115fF and Fc=60GHz), the remaining portion of the input matching network, Cpb is calculated. The input/output pad capacitors are created between top layers (M5-M6) and the third metal layer.

Equation 3.5 can be used to calculate this capacitance [10]:

$$C_{pb} = A.C_a + P.C_p \quad (3.5)$$

Where, A is the metal area of metal 5 and metal 6, C_a is the parallel plate capacitance between metal 5 and metal 3. P is the perimeter of metal 5 and metal 6, and C_p is the perimeter capacitance.

The remaining portion of this design requires an output matching network meeting the requirements of gain and bandwidth. Figure 63 depicts the schematic and the photograph of the designed bipolar matched structure with total area of 425µm x 340µm including bond pads.

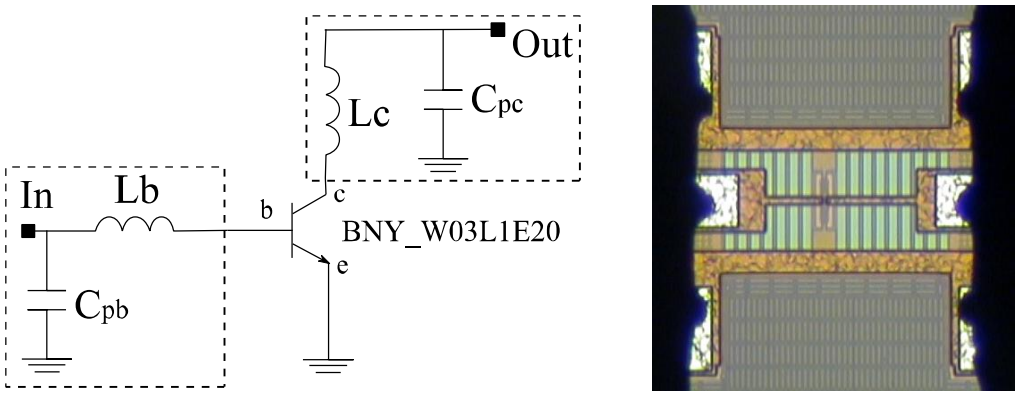

Figure 63 : Schematic and photograph of the bipolar matched structure

The matched test structure is fabricated within the GSG on-wafer probe pads. The input signal contact pad measures 60µm x 75µm, while the output signal contact pad measures 60µm x 65µm.

3.5.2.1. S-parameters measured and simulated results

The matched test structure characterization is carried out with an Agilent 8510C network analyzer with ground-signal-ground (GSG) probes. The matched test structure is measured on-wafer with SOLT / LRRM calibration. The S-parameters of the matched bipolar transistors are measured in the range frequency from 100MHz to 110GHz and are shown in figure 64. The measured S-parameters presented here are the de-embedded results from the raw measured data using open and short pads.

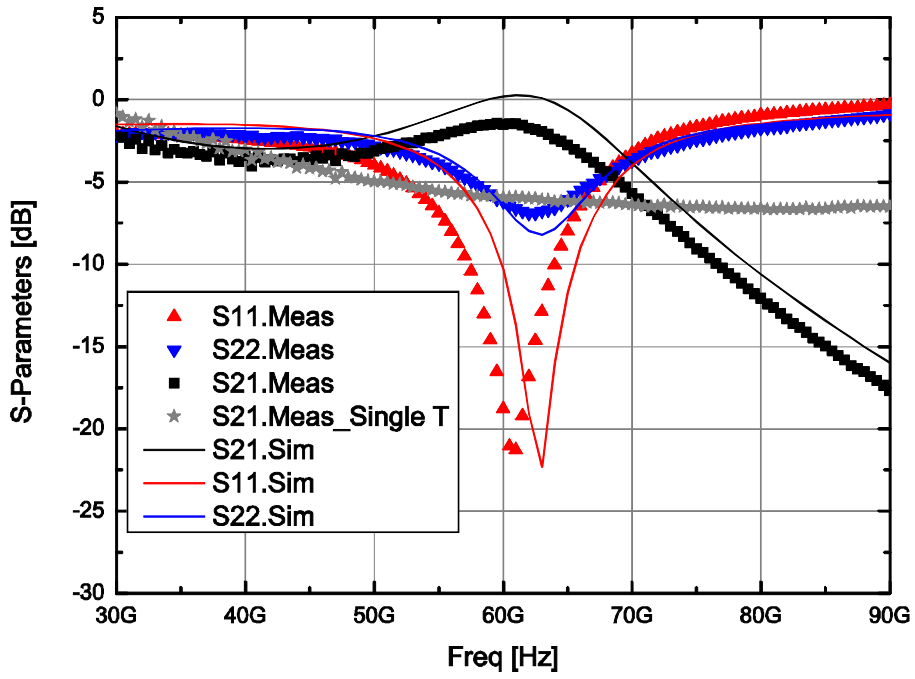

Figure 64 : Matched test structure S-parameters measured and simulated

In figure 64, the transmission gain S21-parameter measured for the single transistor is shown. In the same figure, the S-parameters measured and simulated for the SMTA matched are also shown. A good agreement between measured and fitted curves for the compact bipolar transistor for each parameter is obtained. SMTA reflection parameters S11 and S22 show good input/output matching. As expected, the gain S21 of SMTA is improved from -6dB to -1.5dB the gain S21 of the single transistor. This method slightly increases the silicon area but reduces the time and the extraction flexibility for de-embedding and measurements.

3.5.1. Cbe extraction from the S-parameters of the SMTA

The measurement of the bipolar SMTA allows the extraction of Cbe transistor parameter directly from the measured S-parameters. The $C_{be\_extracted}$, is extracted at the resonance frequency of the SMTA (f_{c_meas}) using equation (3.6). L_{e_meas} is neglected as the emitter node is connected directly to the ground and L_{b_meas} is

the inductance of the input short test structure. This method is developed in our previous study detailed in [11].

$$C_{be\_extracted} = \frac{1}{2\pi {f_{c_{meas}}}^2 (L_{b\_meas} + L_{e\_meas})} \quad (3.6)$$

$$C_{be\_extracted} = \frac{1}{2\pi (60.10^9)^2 (67.10^{-12} + 0.1^{-12})} \quad (3.7)$$

$$C_{be\_extracted} = 114fF \quad (3.8)$$

The $C_{be\_extracted}$ calculated from the measured L_{b_meas} and f_{c_meas} is equal to 114fF. The value calculated is very close to the base-emitter capacitance extracted from the single transistor characterization which was used for the calculation of the matching network in the beginning of the SMTA design procedure.

3.5.2. SMTA characterization and extraction

The similar DC / RF measurements and bias ranges that were used to characterize the single bipolar transistor discussed in section 3.4.2 are repeated for the characterization of the SMTA using the same setups (template). The same DC characterization results as for the single transistor presented in sub-section 3.4.1 are obtained. The DC results are not shown again in this sub-section. For comparison, only the RF characterization results are presented ahain.

3.5.3. SMTA small signal equivalent circuit extraction (ST/SMTA results comparison)

The bipolar under test in the new matched test structure is characterized using the same conditions as for the single transistor characterization. The goal is to perform comparison between extractions and thereby check the improvement of characteristics extractions (discrepancy between measurement and simulation) achieved using the SMTA. The comparison realized for capacitances. The Cbe and Cbc extracted capacitances from respectively, transistor and SMTA measurements and simulations are shown in figure 65 over the frequency range

up to 80GHz. The capacitances extracted from SMTA measurements show different values after 40GHz compared to ST measurements. They are in agreement with the simulations (with best agreement at 60GHz).

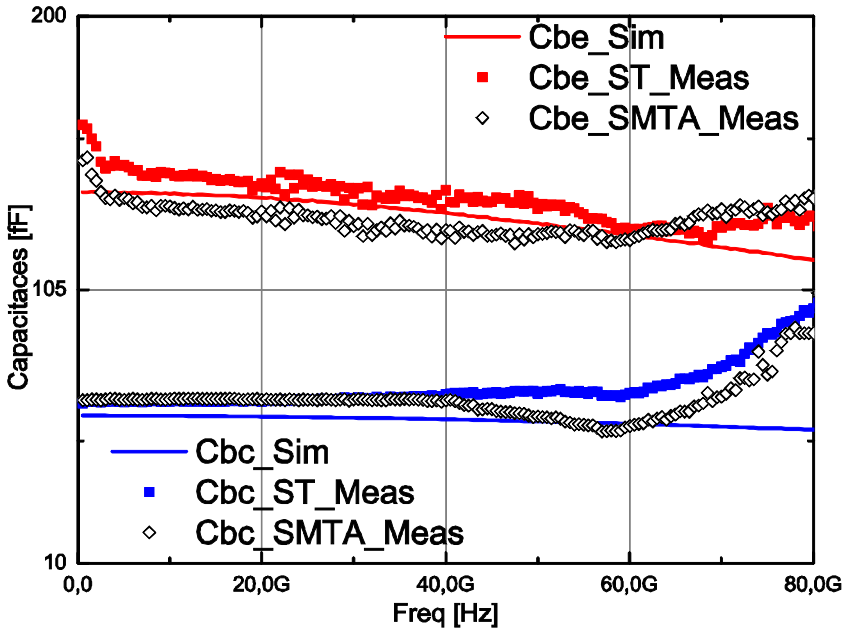

Figure 65 : Measured and simulated capacitances over the frequency range

The base-emitter depletion and the base-collector capacitances extracted using the new test structure over base-emitter biasing are shown in figure 66 and 67, respectively, and compared to those extracted from the single transistor characterization mode presented in section 3.4.2.

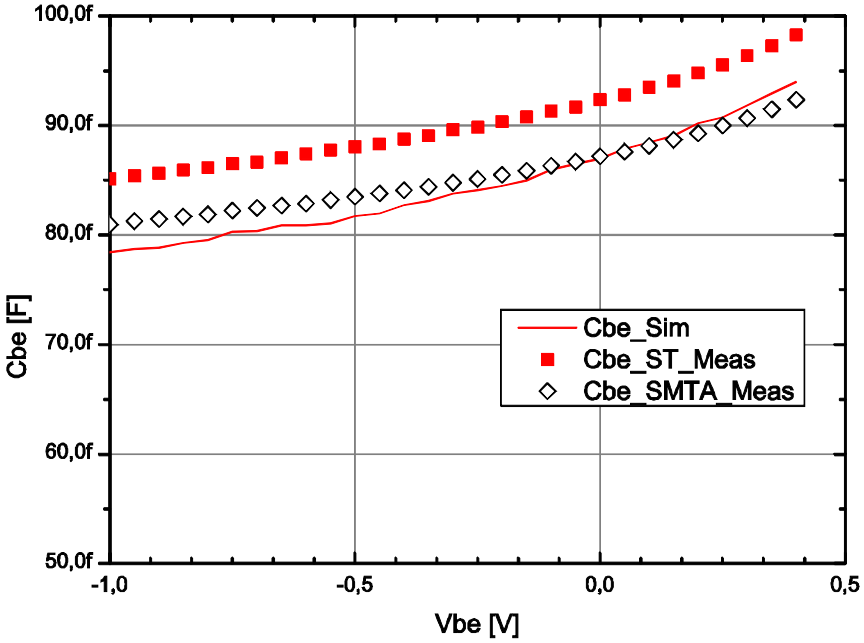

Figure 66 : Measured (markers) and simulated (line) base-emitter capacitance at 3.5GHz

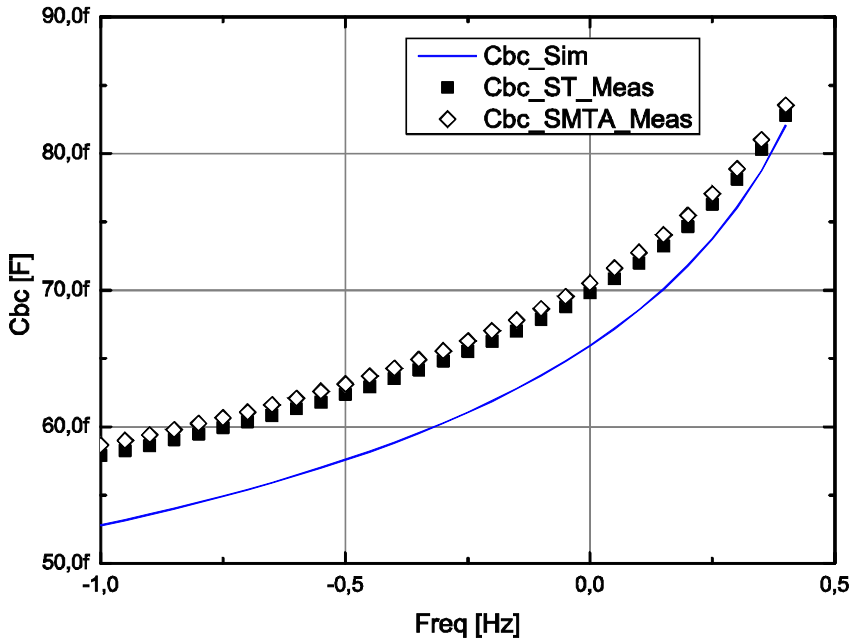

Figure 67 : Measured (markers) and simulated (line) base-collector capacitance at 3.5GHz

The measured and simulated Cbe and Cbc capacitances shown in figure 66 and figure 67 are extracted at the frequency of 3.5GHz. The capacitances extracted

from the SMTA measurements show a shift of 5fF for Cbe with respect to the measured capacitances extracted from the ST measurements.

The procedure used for the extraction of capacitances at 3.5GHz also used at 60GHz. Figures 68 and 69 illustrate the capacitances C_{be} and C_{bc} as a function of Vbe [0.7 to 1V, step 0.1V].

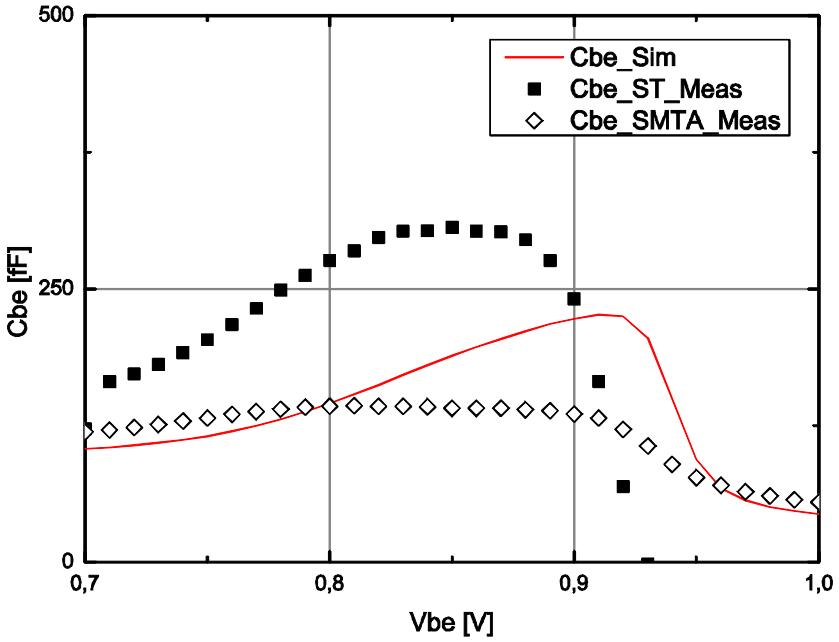

Figure 68 : Measured (markers) and simulated (line) base-emitter capacitance at 60GHz

C_{be} extracted from measurements of SMTA shows a behavior over Vbe closer to simulations as shown in figure 68. The value of C_{be} is improved at 0.85V by more than 35% compared to the measurement obtained from the single transistor characterization at 60GHz (See table 6 in section 3.5.3.1). The simulation over base-emitter voltage is better predicted at very high frequency. The same observation can be noted also for the C_{bc} capacitance in figure 69.

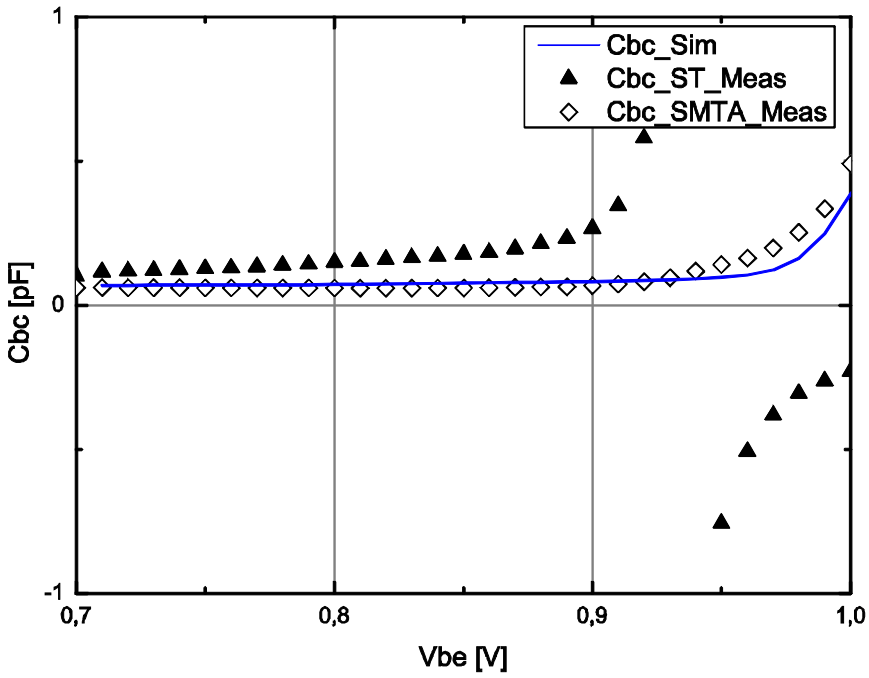

Figure 69 : Measured (markers) and simulated (line) base-collector capacitance at 60GHz

The values extracted at 60GHz from SMTA measurements are more suitable for design of circuits at this frequency.

3.5.3.1. Summary of capacitances extraction (ST/SMTA)

The table 6 summarizes the capacitances extracted from the single transistor and the matched test structure characterization. The table compares the dispersion between extracted capacitance values from both methods ST/SMTA extractions and the model simulation values. The relative error between measurements and simulations with respect to simulation is calculated using equation (3.9)

$$Relative\ error = \frac{Sim}{Sim-Meas} * 100 \qquad (3.9)$$

For the capacitances extraction, the measurements are realized over a large range of collector, base and emitter bias conditions as explained above. The capacitances values summarized in table 6 are taken for one base-emitter and one collector-emitter voltages. The setup A represents the capacitances extracted

from the figure 65 (measured over the range of frequency) for Vbe=0.77V and Vce=1V, the setup B enables the extraction of the capacitances at one constant frequency (3.5GHz) for Vbe=0.4V and Vce=0V (figure 66 and 67), and the setup C is used for extraction of the capacitances at 60GHz for Vbe=0.77V and Vce=0.5V (figure 68 and 69).

Setup	[A] Vb=0.77V, Vc=1V Capacitances over frequency, extraction at 60GHz			[B] Vb=0.4V and Vc=0V Capacitances extraction at 3.5GHz			[C] Vb=0.77V and Vc=0.5V Capacitances extraction at 60GHz		
	Sim	Meas_ST	Meas_SMTA	Sim	Meas_ST	Meas_SMTA	Sim	Meas_ST	Meas_SMTA
Cbe	115fF	126fF	122fF	94fF	98fF	93fF	115fF	232fF	130fF
Error % Sim		14.5	1.7%		4%	1%		50.43%	11.5%
Cbc	59fF	69fF	58fF	82fF	83fF	83.5fF	70fF	134fF	61fF
Error % Sim		8.7%	5.7%		1.2%	1.8%		48%	14.75%

Table 6 : Summary of the extracted capacitances

The capacitances extracted from measurements of the new test structure SMTA (depicted in the table on blue background) show a lower relative errors with respect to the simulations when are compared to those extracted from the single transistor measurements. This accuracy improvement at mm-wave frequencies could be a solution to the limitations related to the increase of measurement frequencies and the decrease of the size of transistors (decrease of their impedances). Accurate equivalent circuit, more attention to calibration and de-embedding steps, as well as multiple measurement and calculation steps are required to improve characterization accuracy. The DUT carefully matched the characteristic impedances Z_0 of the VNA are a promising solution to provide proper transmission of the signal between probes and devices under test.

3.5.4. Very high frequency (95GHz) SMTA for characterization and extraction

To validate and assess the accuracy of the proposed method, additional matched test structures are fabricated and placed on the test chip. In this section, the matched test structure for a bipolar W03L1E5 is presented. The matched test structure is designed with input/output impedance matching realized using inductors from the 0.25µm BiCMOS library. The SMTA is optimized to match 50 Ohms impedance at 95GHz frequency. The matching network is found using the approach presented in the previous section.

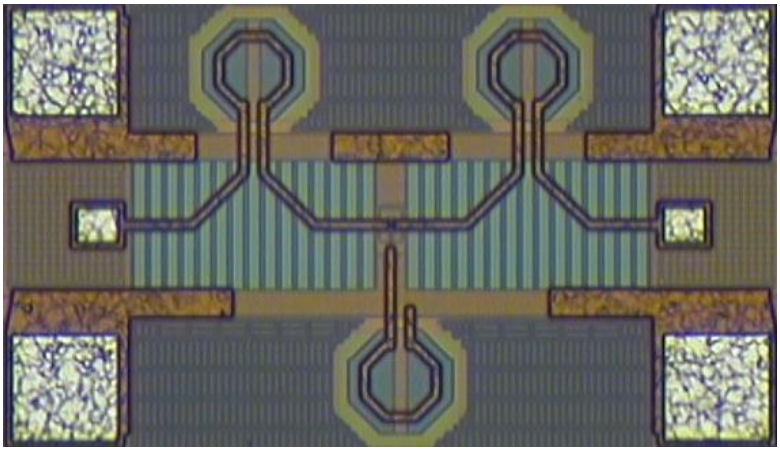

Figure 70 : Photograph of the bipolar matched structure

For de-embedding reasons, the test structure is symmetric and the device is in the center of the test structure. The open-short de-embedding procedure is used to subtract the extrinsic components modeled as parallel-series configuration. The SMTA is modeled including pads, input/output interconnects and intrinsic device. Usually, in the conventional characterization method, the emitter port transistor is connected directly to the ground (common emitter configuration). With the matched test structure, the emitter port transistor is connected the ground through an emitter inductor (common emitter configuration). The inductor is de-embedded by the use of dedicated dummies.

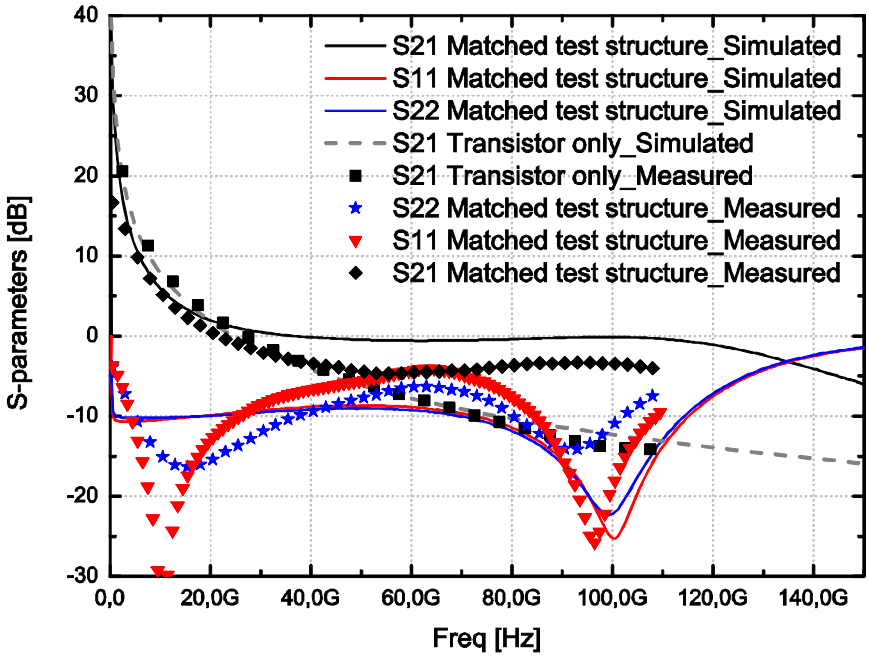

Figure 71 : Matched test structure S-parameters measured and simulated

The measurements of the SMTA given in figure 71 show a good agreement with simulations of available compact models after carefully integration of matching networks up to 110GHZ. The measured transmission gain (S21) of the SMTA (-2.5dB) is improved by 10dB comparing to the measured transmission gain of the single transistor which is -12.5dB. However, the advantage of SMTA is the improvement of the bipolar input/output impedances seen from the VNA and accordingly of the transistor transmission gain. This improvement could offer more accuracy during the extraction of the small signal equivalent circuit parameters in mm-wave range.

3.6. Conclusion

The SMTA with bipolar transistors demonstrates an improvement of parameter extraction when using the matching network elements followed by the simple two steps de-embedding. The matching network is used to match the DUT to the impedance matching of the VNA (50 Ohms) and to improve the transmission gain of the DUT at a desired frequency band. It was proved that the matching network can be removed by a simple de-embedding. The comparison with the

compact model simulations and the single transistor characterization showed SMTA potential.

3.7. References

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Chapter 4: Conclusion and further research

Chapter 4 Conclusion and further research

4.1. Conclusion

Presently, extracting the wafer-level S-parameters of DUTs for characterization and modeling of advanced devices consists of taking into account the de-embedding test structures parasitics, the measurement environment, extraction and curve fitting procedures. This approach has some remain limitations, such as limited accuracy at mm-wave frequencies and its complexity that increases with the increase of the small signal equivalent circuit extraction.

This work proposed a new method to extract the small signal equivalent circuit using matching networks in characterization test structures. This method is based on the DUT input and output impedances that are carefully matched to the characteristic impedances of the measurement equipment. The measurement reference plan can be set close to the DUT as in the standard test structure but it is dependent on the input / output matching network size. The matching network is included in the de-embedding test structures (dummies) and can be eliminated by the conventional de-embedding steps. The advantages are the transmission of the signal from the probes to the DUT improvement and the parameters extraction with more accuracy. The developed method enables the BiCMOS 0.25µm compact models validation in circuit level in mm-wave band and enables accurate parameter extraction in a narrow band at very high frequencies.

The developed method is implemented and verified on two CMOS test modules and two bipolar test modules from BiCMOS 0.25µm technology of NXP Semiconductors. The experiments are carried out up to 50GHz and 110GHz, respectively for CMOS and bipolar modules. The verification results demonstrate that the SMTA can lead to more accuracy for Cbe and Cbc capacitances extraction at 60GHz than the measurement of the unmatched transistors.

The key contribution of this work is to initiate characterization and extraction of small signal equivalent circuit at very high frequency. The main advantage of of the SMTA is to allow the characterization of S-parameters in a reduced band centered at mm-wave frequencies. The device behavior is made more robust for on-wafer characterizations in a reduced band with higher gain, lower noise, and matched input/output impedances. Therefore, the SMTA has three significant advantages:

1. Improving the transmission of the measurement signal from the probes to the device under test
2. The calibration and measurements are made in narrow band with gain in characterization time
3. Increasing of the parameters extraction accuracy and accordingly the extraction of SSEC parameters

Previously, there were several attempts to improve the silicon small signal equivalent circuit accuracy at device level by improving de-embedding techniques and some other improvements such as fabricating calibration standards together with the DUT. Since then, it has become a common understanding in industry that it was generally difficult to achieve more accuracy at device level. Investigating de-embedding techniques leads to several solutions to the characterization issues but always needs more and more dummy test structures as well as multiple measurement and calculation steps, with as result, additional sources of errors. Fabricating calibration standards together with the DUT also raises additional calibration challenges and the non-ideal characteristics of standards limit the accuracy.

Based on detailed analysis, this work proposed another way of characterizing based on exploring techniques at circuit level. It also includes the analysis of the test structure design, accuracy of S-parameter measurements, the small signal

equivalent circuit definition / distribution, and, finally the verification of compact models.

4.2. Further research

Going beyond the original scope of this research work, some aspects of the matched test structures could be subject of further investigation. In particularly topics such as additional test structure analysis, characterization over multiple impedance matching bands, and de-embedding test structures evaluation.

4.2.1. Additional test structure analysis

As discussed in chapter 3, advanced characterization technique as well as device parameter extraction at millimeter wave band demand improvement of the transmission of the measurement signal from the source to the device under test, and demand also measurements over a large biasing and a large measurement conditions. The verification of the SMTA design in different frequency bands and the evaluation of accuracy of SSEC in different bands will be subject for further improvements.

4.2.2. Characterization over multiple impedance matching bands

Modeling, parameter extraction, and model verification require several measurements of the same DUT. Adopting the same test structure, such as for matched test structure developed in this chapter, makes the requirement for device modeling more challenging. Another possible and useful area of development in this research is the development of a parameterization methodology for implementation of matching networks, and thereby uses different SMTAs over different frequency band.

4.2.3. De-embedding test structure

Crosstalk and parasitic coupling of signals inside the test structure have an impact. An overall behavior of devices measured on-wafer was well predicted and considered in this study. De-embedding strategies that allow the subtraction

of matching networks at SMTA central frequency should be investigated in order to obtain more flexibility in matching impedances definition and subtraction.

Appendix

Appendix A Introduction to the Mextram 504 compact model

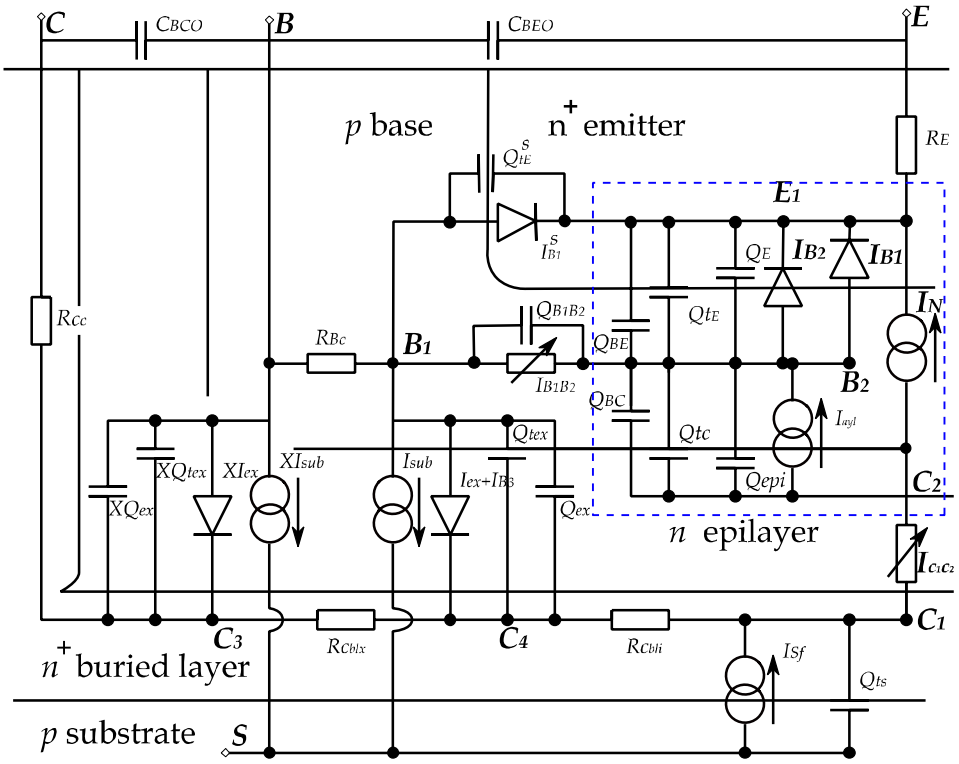
A. Introduction to the Mextram 504 compact model

Within NXP Semiconductors, we use the Mextram 504 compact model for vertical bipolar transistor simulations. The Mextram level 504 is an advanced compact model developed as the successor of the first Mextram level 503 putted in the public domain in 1994. The Mextram is very accurate for bipolar transistor simulations. It gives an excellent description of vertical bipolar transistor in all kinds of process and contains many features that the widely-used Gummel-Poon model lacks. It has been improved by changing some of the formulations of model level 503. For instance the Early voltages were calculated from other parameters, whereas, in 504 are now calculated as separate parameters. In order also, to make much smoother the behavior of the model characteristics, improvements, have been made in the description of the epilayer.

In Mextram almost of all parameters have a physical meaning and this makes the parameter extractions more difficult. Therefore NXP modeling engineers have tried in Mextram 504 to remove as much as possible this interdependence without losing the physical basis of the model. In the fall of 2004, Mextram was elected as a world standard transistor model by the *Compact Model Council (MCP)*. The complete model that has been revised is shown in the figure below, which in its other versions has already discussed in for instance. Most of the Mextram parameters can be extracted from, DC and S-parameter measurements. It is important to mention that the Mextram transistors can be put in parallel, so no extensive geometrical or process scaling rules are needed.

In this appendix, we only introduce the physical origins of the Mextram model (active transistor), without giving the detailed overview. The model describes the various currents and charges. These currents and charges are described by the

various elements shown as resistances, capacitances, diodes and current sources. These elements connect the internal and external nodes.



The full Mextram equivalent circuit for the vertical NPN transistor

DC Model

The main current

In the Mextram, the generalization of the integral charge control relation is used to take into account the depletion charges Q_{tE} and Q_{tC} and the diffusion charges Q_{BE} and Q_{BC} on the main current, the relation is:

$$I_N = I_s(e^{v_{B2E1}/kT} - e^{v_{B2C2}/kT})\frac{1}{qB} \qquad \text{(A.1)}$$

Where, I_N is the main current, I_s is the main saturation current, q is the unit charge, $\frac{kT}{q}$ is the thermal voltage (V_T), v_{B2E1} and v_{B2C2} are the internal junctions node voltages. $I_s(e^{v_{B2E1}/V_T}) = I_f$, is the forward part of the main current and $I_s(e^{v_{B2C1}/V_T}) = I_r$, is the reverse part of the main current.

The normalized base charge is given by:

$$q_B = \frac{Q_{B0}+Q_{tE}+Q_{tC}+Q_{BE}+Q_{BC}}{Q_{B0}} \quad \text{(A.2)}$$

Where, Q_{B0} is the base charge at zero bias. The normalized base charge can be given as a product of the early effect (describing the variation of the base width given by the depletion charges) and a term which includes high injection effects. The Early effect term is:

$$q1 = \frac{Q_{B0}+Q_{tE}+Q_{tC}}{Q_{B0}} = 1 + \frac{V_{tE}\,(v_{B2E1})}{V_{er}} + \frac{V_{tC}\,(v_{B2C1},I_{C1C2})}{V_{ef}} \quad \text{(A.3)}$$

The voltages V_{er} and V_{ef} are the forward and reverse early voltages. The voltages V_{tE} and V_{tC} describe the curvature of the depletion charges as function of junction biases, but not their magnitude:

$$Q_{tE} = \left(1 - XC_{jE}\right).C_{jE}.V_{tE} \quad \text{(A.4)}$$

$$Q_{tC} = \left(1 - XC_{jC}\right).C_{jC}.V_{tC} \quad \text{(A.5)}$$

The total normalized base charge is

$$q_B = q_1\left(1 + \frac{1}{2}n_0 + \frac{1}{2}n_B\right) \quad \text{(A.6)}$$

Where n_0 and n_B are the electron densities in the base at the emitter edge and at the collector edge.

$$n_0 = \frac{4I_f/I_k}{1+\sqrt{1+4I_f/I_k}} \quad \text{(A.7)}$$

$$n_B = \frac{4I_r/I_k}{1+\sqrt{1+4I_r/I_k}} \quad \text{(A.8)}$$

I_k is the Knee current

Forward base current

The total base current has a bottom and a sidewall contribution. The separation is given by the factor XI_{B1} which can be determined by analyzing the maximum current gain of the transistor with different geometries.

$$I_{B1} = (1 - XI_{B1})\,\frac{I_S}{\beta_f}\left(e^{v_{B2E1}/kT} - 1\right) \quad \text{(A.9)}$$

$$I_{B1}^{S} = XI_{B1}\,\frac{I_S}{\beta_f}\left(e^{v_{B1E1}/kT} - 1\right) \quad \text{(A.10)}$$

I_{B1} is the ideal base current, I_{B1}^{S} is the ideal base current fellow through the sidewall (the pn-junction between base and emitter is not only present at the intrinsic region bellow the emitter, a part of the I_{B1} will fellow through the sidewall), and β_f is the ideal forward current gain.

The non-ideal forward base current originates from the combination in the depleted base-emitter region.

$$I_{B2} = I_{Bf}(e^{v_{B2E1}/m_{Lf}V_T} - 1) \quad \text{(A.11)}$$

When recombination is the main contribution we have $m_{Lf} = 2$, I_{Bf} is the saturation current of the non-ideal forward base current and m_{Lf} is the non-ideality factor of the non-ideal base current.

Reverse base current

The reverse base current, similar to I_{B2}, is affected by high injection and partitioned over the two external base-collector branches (with parameter X_{ext}). It uses the electron density n_{Bex} in the external region of the base

$$I_{ex} = \frac{1}{2\beta_{ri}} I_k n_{Bex}(v_{B1C4}) \quad \text{(A.12)}$$

The current XI_{ext} is calculated in similar way using the density X_{nBex} (v_{BC3}). β_{ri} is the ideal reverse current gain and X_{ext} is a partitioning factor of the extrinsic regions.

The non-ideal reverse base current originates from the combination in the depleted base-collector region.

$$I_{B3} = I_{Br} \frac{e^{v_{B1C4}/V_T} - 1}{e^{v_{B1C4}/2V_T} + e^{v_{Lr}/2V_T}} \quad \text{(A.13)}$$

It is meant to describe the transition from ideality factor 1 ($v_{B1C4} < v_{Lr}$) to ideality factor 2 ($v_{B1C4} > v_{Lr}$). I_{Br} is the saturation current of the non-ideal base current and v_{Lr} is the cross-over voltage of the non-ideal reverse base current.

Avalanche current

In Mextram the avalanche current is given by:

$$I_{avl} = I_{C1C2}\, G\, (v_{B1C1,} I_{C1C2}) \qquad \text{(A.14)}$$

Where the generation factor, related to the multiplication factor, G = M – 1, is a function of bias and current.

Substrate current

In Mextram the substrate current is modeled as:

$$I_{sub} = \frac{2I_{ss}\left(e^{v_{B1C1}/V_T}-1\right)}{1+\sqrt{1+I_s e^{v_{B1C1}/V_T}/I_{ks}}} \qquad \text{(A.15)}$$

It describes the holes going from the base to the substrate. The current that runs in the case of forward bias in the substrate-collector is not modeled in the physical way, since this should not happen anytime. There is only a single current I_{sf} to alert a designer to this wrong bias situation.

Resistances

The model contains constant, series resistors at the base, emitter and collector terminals, R_{Bc}, R_E, and R_{Cc}, respectively. The resistances of the buried layers underneath the transistor are represented by two constant, temperatures dependent resistances R_{Cblx} and R_{Cbli}. The base resistance is divided in a constant part R_{Bc} and a variable part given by $I_{B_1B_2}$.

AC Model

Overlap capacitances

The model has two overlap constant capacitances. C_{BEO} which is the base-emitter overlap capacitance and the C_{BCO} which is the base-collector overlap capacitance.

Depletion capacitances

The base-emitter depletion capacitance C_{tE} is partitioned in a bottom and a sidewall component by the parameter XC_{jE}

$$C_{tE} = \frac{dQ_{tE}}{dv_{B2E1}} = (1 - XC_{jE}) \frac{C_{jE}}{(1 - v_{B2E1}/v_{d_E})^{P_E}} \quad \text{(A.16)}$$

$$C_{tE}^{S} = \frac{dQ_{tE}^{S}}{dv_{B1E1}} = XC_{jE} \frac{C_{jE}}{(1 - v_{B1E1}/v_{d_E})^{P_E}} \quad \text{(A.17)}$$

C_{jE} is the zero bias emitter base depletion capacitance, v_{d_E} is the emitter base buit-in voltage, P_E is the emitter base grading coefficient, and XC_{jE} is the fraction of the BE depletion capacitance not under the emitter (sidewall fraction).

The base-collector depletion capacitance C_{tC} underneath the emitter takes into account the finite thickness of the epilayer and current modulation:

$$C_{tC} = \frac{dQ_{tC}}{dv_{junc}} = XC_{jC}\, C_{jC} \left((1 - X_p) \frac{f\,(I_{C1C2})}{(1 - v_{junc}/v_{d_C})^{P_C}} - X_p \right) \quad \text{(A.18)}$$

$$f\,(I_{C1C2}) = \left(1 - \frac{I_{C1C2}}{I_{C1Ch2} + I_{hC}}\right)^{mC} \quad \text{(A.19)}$$

The capacitance depends on the junction voltage v_{junc} that is calculated using the external base-collector bias minus the voltage drop over the epilayer, as if there were no injection. The current modulation (Kirk effect) has its own 'grading' coefficient mC and uses the parameter I_{hC} from the epilayer model.

Diffusion charges

The base-emitter and base-collector diffusion charges are given in term of normalized electron densities n_0 and $n_B$discussed earlier. The base transit time determines the zero bias base charge $Q_{B0} = \tau_B I_k$. Also the early effect is included via q_1

$$Q_{BE} = \frac{1}{2} q_1\, Q_{B0}\, n_0 \quad \text{(A.20)}$$

$$Q_{BC} = \frac{1}{2} q_1\, Q_{B0}\, n_B \quad \text{(A.21)}$$

Note τ_B is the base transit time. The n_0, n_B are almost proportional to I_c / I_k. The diffusion charges are therefore almost independent of the knee current, and so in the transit time.

The emitter diffusion charge Q_E is given by:

$$Q_E = \tau_E I_S \left(e^{v_{B2E1}/m_\tau V_T} - 1\right) \left(\frac{I_S}{I_k}\right)^{1/m_\tau - 1} \quad \text{(A.22)}$$

τ_E is the minimum delay time of emitter diffusion charge and m_τ is the non-ideality of the emitter diffusion charge. The actual transit time corresponding to this charge is a function of the current. When $m_\tau > 1$ it has a minimum which is for a transistor without quasi-saturation occurs at $I_c \approx I_k$. The formulation above is such that the minimum is approximately by τ_E. Note that this charge Q_E is not a part of the collector current description. In contrast to the (normalized) depletion and base diffusion charges.

Excess phase shift

Excess phase shift represents the distributed high frequency effects in the vertical direction. This is modeled in Mextram using base-charge partitioning.

Noise Model

In the Mextram, noise is included in various branches of the model:

All resistances have a thermal noise (R_E, R_{Bc}, R_{Cc}, R_{Cblx}, R_{Cbli}, R_{Bv}).

All diode like currents have shot-noise (I_N, I_{B1}, I_{B1}^s, I_{B2}, I_{B3}, I_{ex}, XI_{ex}, I_{sub} and XI_{sub}).

All base current also have flicker-noise (1/f noise) (I_{B1}, I_{B1}^s, I_{B2}, I_{B3}, I_{ex} and XI_{ex}) modeled with a pre-factor K_f and a power A_f. In Mextram the non ideal forward base current has its own pre-factor K_{fN} and a fixed power 2.

Self-heating Model

To describe the self-heating we need to consider two things: what is the dissipated power and what is the relation between the dissipated power and the increase in temperature. The total dissipated power is a sum of the dissipated power at each brunch of the equivalent circuit.

B. Parameter Extraction

The accuracy of circuit simulation depends not only on the performance of the transistor model itself, but also on the model parameters used. Most of the parameters are extracted from the measured data (depletion capacitances (CV), terminal currents versus voltages (DC), and high frequency measurement (S-parameters, in practice always converted to the Y parameters)).

The extraction of the Mextram model parameters are based on the model implemented in the characterization and analysis program IC-CAP of Agilent. Several templates are available with several DC and RF measurement setups to characterize the DC and RF performance of the transistor. With these setups measurements and simulations could be done to perform all kind of parameter extractions. Procedures are coded to extract quantities like current gain ic/ib, early voltages, cut off frequency fT, maximum frequency for voltage gain fA, maximum oscillation frequency Fmax, base, emitter, and collector series resistances. The Mextram parameter extraction strategy allows the extraction of:

- Parameters related to the depletion capacitances (Cbe, Cbc, Csc)
- Forward and reverse early voltage
- Temperature scaling parameters of the collector and base current (temperature dependency of Ic and Ic/Ib)
- Base, emitter, and collector resistances
- The cut off frequency fT, maximum oscillation frequency Fmax and maximum frequency of voltage gain fA are used to extract the transit time

parameters. Fmax is sensitive to the base resistance and the part of Cbc underneath the emitter (parameter XCjc).

- Temperature scaling parameters are extracted.

The global parameters are modified step by step in the model code. After each modification the setup used to extract the parameter is simulated for all devices. From each device a typical quantity (like capacitance at zero bias, Ic and Hfe at Vbe=0.7 Volt, maximum fT, Fmax etc.) is taken and plotted as a function of the emitter perimeter over area (1/Le+1/We). After a limited number of iterations (2-3) a good model overlay with the measured data is obtained. The simulation of a dedicated setup for all devices and plotting the requested quantity is highly automated. The developed model source code can be used directly for implementation in a Process Block without major modifications. This makes that the procedure is time effective and not susceptible to all kind of rework afterwards.

C. References

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Abstract

This thesis deals with the study of innovative solutions for small signal characterization at millimeter wave frequency. After a state of the art in this field and following to several characterizations at device level, a new test structure “new approach” is designed, fabricated, and characterized. The approach of characterizing at circuit level is based on a new method to extract the small signal equivalent circuit using matched test structures. This method proposed here makes the DUT impedances carefully match the characteristic impedances of the measurement equipment. In results, the transmission of the signal from the source to the DUT is improved while the parameters extraction accuracy is improved. The developed method enables the BiCMOS 0.25µm compact models validation in circuit level in mm-Wave band and enables accurate parameter extraction in a narrow band at higher frequencies. The verification results demonstrated that the new test structure significantly outperformed the conventional method in measurement accuracy specifically in very high frequency. Some aspects of the matched test structure could be subject of further investigation. In particularly topics such as, characterization over multiple test structure geometries and de-embedding test structure losses.

Key-words:
Millimeter waves, RF characterization, RF test structures, S-parameters, RF circuit.

Résumé

Ces travaux de thèse portent sur l’étude des solutions innovantes de caractérisation destinées à l’amélioration de la précision du schéma équivalent petit signal à des fréquences d’ordre millimétrique. Après un état de l’art dans ce domaine et suite à plusieurs caractérisations au niveau composant, une nouvelle structure de test “nouvelle approche” est conçue, réalisée et caractérisée. Cette approche est basée sur une nouvelle méthode d’extraction du schéma équivalent petit signal à partir d’une structure adaptée. Cette méthode réalise une adaptation des impédances du transistor sous test aux impédances des équipements de mesure. Comme résultats, la transmission du signal antre la source et le composant sous test ainsi que la précision de la mesure des paramètres extraits sont améliorés. La méthode développée permet la validation des modèles compacts des composants fabriqués en technologie BiCMOS 0.25µm au niveau circuit. Les mesures réalisées ont montré une bonne amélioration de l’extraction entre un transistor sous test seul et un transistor sous test adapté. La méthode d’investigation proposée permet l’extraction des modèles à des très hautes fréquences avec une meilleure précision. Cette thèse ouvre donc des perspectives pour la caractérisation en bande millimétrique notamment caractérisation des structures adaptées en impédances et de méthodes de de-embedding dédiées à ces dernières.