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SUMMARY

This work was performed in the frame of collaboration between the Laboratory on Plasma and Energy Conversion (LAPLACE), University of Toulouse, and the Second University of Naples (SUN). This work was supported by Rongxin Power Electronic Company (China) and concerns the use of multilevel converters in High Voltage Direct Current (HVDC) transmission.

For more than one hundred years, the generation, the transmission, distribution and uses of electrical energy were principally based on AC systems. HVDC systems were considered some 50 years ago for technical and economic reasons. Nowadays, it is well known that HVDC is more convenient than AC for overhead transmission lines from 800 - 1000 km long. This break-even distance decreases up to 50 km for underground or submarine cables.

Over the twenty-first century, HVDC transmissions will be a key point in green electric energy development. Due to the limitation in current capability of semiconductors and electrical cables, high power applications require high voltage converters. Thanks to the development of high voltage semiconductor devices, it is now possible to achieve high power converters for AC/DC conversion in the GW power range.

For several years, multilevel voltage source converters allow working at high voltage level and draw a quasi-sinusoidal voltage waveform. Classical multilevel topologies such as NPC and Flying Capacitor VSIs were introduced twenty years ago and are nowadays widely used in Medium Power applications such as traction drives. In the scope of High Voltage AC/DC converters, the Modular Multilevel Converter (MMC), proposed ten years ago by Professor R. Marquardt from the University of Munich (Germany), appeared particularly interesting for HVDC transmissions.

On the base of the MMC principle, this thesis considers different topologies of elementary cells which make the High Voltage AC/DC converter more flexible and easy suitable respect to different voltage and current levels. The document is organized as follow.

Firstly, HVDC power systems are introduced. Conventional configurations of Current Source Converters (CSCs) and Voltage Source Converters (VSCs) are shown. The most attractive topologies for VSC-HVDC systems are analyzed.

The operating principle of the MMC is presented and the sizing of reactive devices is developed by considering an open loop and a closed loop control. Different topologies of elementary cells offer various properties in current or voltage reversibility on the DC side. To compare the different topologies, an analytical approach on the power losses evaluation is achieved which made the calculation very fast and direct.

A HVDC link to connect an off-shore wind farm platform is considered as a case study. The nominal power level is 100 MW with a DC voltage of 160 kV. The MMC is rated considering press-packed IGBT and IGCT devices. Simulations validate the calculations and

also allow analyzing fault conditions. The study is carried out by considering a classical PWM control with an interleaving of the cells.

In order to validate calculation and the simulation results, a 10kW three-phase prototype was built. It includes 18 commutation cells and its control system is based on a DSP-FGPA platform.

RESUME

Les travaux présentés dans ce mémoire ont été réalisés dans le cadre d'une collaboration entre le LAboratoire PLAsma et Conversion d'Énergie (LAPLACE), Université de Toulouse, et la Seconde Université de Naples (SUN). Ce travail a reçu le soutien de la société Rongxin Power Electronics (Chine) et traite de l'utilisation des convertisseurs multi-niveaux pour le transport d'énergie électrique en courant continu Haute Tension (HVDC).

Depuis plus d'un siècle, la génération, la transmission, la distribution et l'utilisation de l'énergie électrique sont principalement basées sur des systèmes alternatifs. Les systèmes HVDC ont été envisagés pour des raisons techniques et économiques dès les années 60. Aujourd'hui il est unanimement reconnu que ces systèmes de transport d'électricité sont plus appropriés pour les lignes aériennes au-delà de 800 km de long. Cette distance limite de rentabilité diminue à 50 km pour les liaisons enterrées ou sous-marines.

Les liaisons HVDC constituent un élément clé du développement de l'énergie électrique verte pour le XXIème siècle. En raison des limitations en courant des semi-conducteurs et des câbles électriques, les applications à forte puissance nécessitent l'utilisation de convertisseurs haute tension (jusqu'à 500 kV). Grâce au développement de composants semi-conducteurs haute tension et aux architectures multicellulaires, il est désormais possible de réaliser des convertisseurs AC/DC d'une puissance allant jusqu'au GW.

Les convertisseurs multi-niveaux permettent de travailler en haute tension tout en délivrant une tension quasi-sinusoïdale. Les topologies multi-niveaux classiques de type NPC ou « Flying Capacitor » ont été introduites dans les années 1990 et sont aujourd'hui couramment utilisées dans les applications de moyenne puissance comme les systèmes de traction. Dans le domaine des convertisseurs AC/DC haute tension, la topologie MMC (Modular Multilevel Converter), proposée par le professeur R. Marquardt (Université de Munich, Allemagne) il y a dix ans, semble particulièrement intéressante pour les liaisons HVDC.

Sur le principe d'une architecture de type MMC, le travail de cette thèse propose différentes topologies de blocs élémentaires permettant de rendre le convertisseur AC/DC haute tension plus flexible du point de vue des réversibilités en courant et en tension. Ce document est organisé de la manière suivante.

Les systèmes HVDC actuellement utilisés sont tout d'abord présentés. Les configurations conventionnelles des convertisseurs de type onduleur de tension (VSCs) ou de type onduleur de courant (CSCs) sont introduites et les topologies pour les systèmes VSC sont ensuite plus particulièrement analysées.

Le principe de fonctionnement de la topologie MMC est ensuite présenté et le dimensionnement des éléments réactifs est développé en considérant une commande en boucle ouverte puis une commande en boucle fermée. Plusieurs topologies de cellules élémentaires sont proposées afin d'offrir différentes possibilités de réversibilité du courant ou de la tension du côté continu. Afin de comparer ces structures, une approche analytique de

l'estimation des pertes est développée. Elle permet de réaliser un calcul rapide et direct du rendement du système.

Une étude de cas est réalisée en considérant la connexion HVDC d'une plateforme éolienne off-shore. La puissance nominale du système étudié est de 100 MW avec une tension de bus continu égale à 160 kV. Les différentes topologies MMC sont évaluées en utilisant des IGBT ou des IGCT en boitier pressé. Les simulations réalisées valident l'approche analytique faite précédemment et permettent également d'analyser les modes de défaillance. L'étude est menée dans le cas d'une commande MLI classique avec entrelacement des porteuses.

Enfin, un prototype triphasé de 10kW est mis en place afin de valider les résultats obtenus par simulation. Le système expérimental comporte 18 cellules de commutations et utilise une plate-forme DSP-FPGA pour l'implantation des algorithmes de commande.

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Nell'ultimo secolo, la generazione, la trasmissione, la distribuzione ed il consumo di energia è stato principalmente basato su sistemi in corrente alternata (AC). I sistemi di tipo HVDC si sono resi attrattivi negli ultimi 50 anni per una serie di ragioni di natura tecnica ed economica. Oggi, è ben noto che le connessioni HVDC sono più convenienti rispetto a quelle AC per distanze superiori a linee comprese tra 800 – 1000 km. Questa distanza di soglia si riduce quando si parla di trasmissioni sottomarine.

Nel ventunesimo secolo, le trasmissioni HVDC saranno un punto chiave anche per lo sviluppo e l'integrazione con il preesistente sistema elettrico delle energie rinnovabili. A causa della limitazione in corrente dei dispositivi semiconduttori e dei cavi di trasmissione, l'impiego di alte potenze si traduce nell'impiego di convertitori ad alte tensioni. Grazie alo sviluppo di dispositivi semiconduttori, è oggi possibile ottenere conversioni AC/DC per alte potenze dell'ordine dei GW.

Per diversi anni, i convertitori Multilivello di tipo sorgente di tensione, in letteratura noti come voltage source converters (VSC), consentono di lavorare ad alti livelli di tensione e di imporre una forma d'onda di tensione al lato AC pressoché sinusoidale. Le classiche topologie come NPC e Flying Capacitors ti tipo VSI sono state introdotte circa venti anni addietro ed oggi sono generalmente utilizzate in applicazioni di media potenza come gli azionamenti delle macchine elettriche. Per la conversione AC/DC ad alta tensione, il convertitore modulare multilivello (MMC), proposto circa dieci anni fa dal professore R. Marquardt della Università di Monaco (Germania), è sembrato particolarmente attrattivo ed interessante per le trasmissioni HVDC.

Partendo dalla struttura HVDC, si sono considerate all'interno del lavoro di differenti topologie di celle elementari che rendono il convertitore più flessibile e più facilmente adattabile rispetto ai differenti livelli di tensione e corrente.

Il lavoro di tesi si è svolto secondo il seguente ordine:

in primis, i sistemi HVDC sono stati introdotti. Le configurazioni convenzionali basate sui convertitori a sorgente di corrente (CSC) e quelle basate sui convertitori a sorgente di tensione (VSC) sono state descritte. In entrambi i casi il principio di funzionamento sul quale si basa il trasferimento di potenza è stato descritto. Parallelamente è stato effettuato uno studio sullo stato dell'arte dei semiconduttori impiegati nella elettronica di potenza e sono state tratte

valutazioni sui meglio adattabili alle connessioni HVDC. Si è evinto dedotto che l'orientamento delle trasmissioni HVDC è basato sulla conversione VSC. Per tale motivo ha analizzato le topologie multilivello più attrattive.

I principi di funzionamento dell'MMC sono stati studiati e il dimensionamento dei componenti reattivi è stato proposto considerando due differenti approcci a seconda del controllo ipotizzato per il sistema. Nel corso del suo studio si è inoltre evinto che differenti topologie di celle elementari offrono varie proprietà reversibilità di corrente o di tensione sul lato DC. Al fine di comparare le differenti topologie, si è proposto un nuovo approccio analitico per lo studio delle perdite ha reso il calcolo veloce e diretto.

In tale ambito una nuova struttura multilivello è stata introdotta. Tale topologia è stata pensata per sistemi AC/DC basata su raddrizzatori a ponte di diodi. Tali sistemi infatti sono composti da trasformatori di rete di tipo ZigZag configurati in tal modo da compensare le componenti continue della corrente introdotte dal raddrizzatore a ponte lato AC. La topologia proposta nel lavoro di tesi è pensata per rimpiazzare i vecchi raddrizzatori obsoleti e poco versatili con una struttura multilivello capace di avere un impatto armonico ridotto ed un funzionamento a quattro quadranti in termini di potenza.

In una fase successiva gli studi sono stati validati attraverso una campagna di simulazioni. Il caso considerato è quello di un sistema HVDC-VSC multiterminal chiamato ad interfacciare un parco eolico off-shore sito in Cina. La potenza del sistema è di 100 MW con una tensione DC di 160 kV. Il convertitore MMC è stato dimensionato considerando dei dispositivi IGBT di tipo press-Pack e dei dispositivi IGCT. Le simulazioni hanno validato le simulazioni anche in condizioni di fault. Lo studio del controllo per il sistema è stato effettuato in prima battuta considerando la classica modulazione PWM. Tale modulazione è stata implementata sfasando le portanti tra le celle che compongono la struttura.

Al fine di validare lo studio e i risultati di simulazione, un prototipo trifase da 10 kW è stato realizzato. Tale prototipo è formato da 18 celle di commutazione di tipo semplici. Il sistema di controllo è stato implementato grazie una piattaforma basata su logica DSP-FPGA.

RESUME DE LA THESE EN LANGUE FRANÇAISE

Chapitre I : Les systèmes HVDC

Ce chapitre présente les systèmes pour le transport d'énergie électrique en courant continu à haute tension (HVDC) et souligne leur rôle clé dans le développement des énergies renouvelables.

Ces 40 dernières années, les systèmes HVDC ont été développés pour le transport de l'électricité compte tenu des considérations techniques et économiques suivantes :

- Par rapport aux systèmes en courant alternatif, la transmission en courant continu, malgré le coût additionnel des sous-stations de conversion, est économiquement intéressante pour des distances supérieures à 800 km dans le cas des lignes aériennes et 50 km pour les lignes enterrées ou sous-marines (Figure I-1).
- Les systèmes en courant continu permettent les interconnexions entre des réseaux hétérogènes qui peuvent être asynchrones entre eux, et/ou à fréquences différentes.
- L'amélioration constante de la technologie des dispositifs semi-conducteurs a permis d'atteindre des niveaux de puissance de l'ordre du GW.

Nous illustrons la description des principes de connexion HVDC en faisant référence aux principales installations actuelles. Deux principaux types de connexion HVDC sont utilisés. Celles basées sur des convertisseurs AC/DC de type onduleur de courant (CSC) et celles basées sur des convertisseurs AC/DC de type onduleur de tension (VSC).

Avant d'entrer dans les détails de fonctionnement de ces liaisons HVDC, nous décrivons les principaux dispositifs semi-conducteurs disponibles sur le marché et employés pour les applications « haute tension ». Nous donnons en particulier une description détaillée des technologies en boitier pressé (*press-pack)*, qui peuvent être considérées comme les meilleures candidates pour la mise en œuvre de semi-conducteurs en haute tension et fort courant.

Nous donnons ensuite une description des convertisseurs CSC à base de thyristors et présentons les principes de réglage de la puissance. Du fait que les thyristors ne présentent pas de problèmes de mise en série directe, les convertisseurs peuvent atteindre des tensions de l'ordre de 500 kV. Bien que simple et robuste, la topologie de type CSC ne permet pas un contrôle indépendant des puissances active et réactive et absorbe également des courants non sinusoïdaux qui nécessitent des dispositifs de filtrage occupant 20 à 30% de la superficie totale d'une sous-station (Figure I-42).

Les convertisseurs de type VSC commandés en modulation de largeur d'impulsion (MLI) sont basés sur des semi-conducteurs à amorçage et blocage commandées (IGBT ou IGCT). Les topologies HVDC-VSC permettent d'effectuer le transport d'énergie en courant continu en offrant, vis-à-vis des réseaux AC, des réglages indépendants des puissances active et réactive . La mise en série directe d'IGBT étant très délicate, la tension reste aujourd'hui limitée à 320 kV pour une topologie classique à trois niveaux de tension par bras.

Nous décrivons ensuite des topologies multiniveaux qui sont adaptées à la haute tension. Par rapport aux structures classiques, elles peuvent garantir une forme d'onde quasi sinusoïdale en réduisant les harmoniques et en permettant une réduction des éléments de filtrage. Parmi ces topologies multiniveaux, nous présentons le principe de base du convertisseur modulaire multiniveaux (MMC) qui sera développé dans la suite de la thèse. Cette structure consiste en la mise en série de blocs élémentaires identiques (Figure I-62). Elle est aujourd'hui préférée aux structures traditionnelles car elle garantit une modularité en termes de production industrielle et n'a théoriquement pas de limite supérieure pour la valeur de la tension DC puisqu'il est toujours possible d'ajouter des blocs élémentaires en série.

Chapitre II : Le convertisseur modulaire multiniveaux (MMC)

Nous étudions dans ce chapitre le convertisseur AC/DC modulaire multiniveaux. Le circuit triphasé est formé de la connexion de deux bras par phase (Figure II-1). Chaque bras impose la moitié de la tension DC ainsi que la tension AC. Chacun des bras conduit également un tiers du courant DC et la moitié du courant AC. La combinaison des deux bras nous permet d'obtenir les courants et tensions AC et DC nécessaires au transfert de puissance par la liaison DC. Après une première analyse du fonctionnement, nous proposons un modèle moyen de la structure (macro modèle) afin de simplifier l'étude de dimensionnement. Ce modèle ne prend pas en considération les effets des harmoniques dus aux dispositifs de commutation mais garantit une plus grande rapidité dans les simulations, les calculs étant simplifiés. L'étude est en outre valable quelle que soit la topologie des blocs élémentaires et considère une commande MLI classique avec entrelacement des porteuses.

Nous effectuons une analyse préliminaire des courants et tensions du convertisseur. Du point de vue des harmoniques de courant, outre les composantes DC et AC, chacun des bras conduit une composante au double de la fréquence fondamentale (Figure II-9). Cette composante découle de l'équilibrage énergétique entre les deux bras qui composent chaque phase. La minimisation de cette composante jouant un rôle fondamental dans le dimensionnement des éléments de filtrage, nous étudions par la suite deux possibilités liées au pilotage de la structure. Des simulations sur un système de 100 MW composé de 64 convertisseurs élémentaires par bras valident l'étude.

Dans le premier cas, nous adoptons un contrôle de la structure qui ne permet pas de supprimer l'harmonique de second ordre du courant de bras. La limitation de son amplitude est alors effectuée exclusivement par les composants passifs. Ainsi, en augmentant la capacité du condensateur de chaque bloc élémentaire et l'inductance série de chaque bras, l'amplitude de cet harmonique peut être diminuée. Pour ne pas limiter la plage de réglage du convertisseur à cause des valeurs élevées de l'inductance de bras, nous proposons alors d'utiliser deux inductances couplées par phase. Elles sont couplées de manière à présenter une valeur élevée vis-à-vis de l'harmonique de courant d'ordre deux tandis qu'une valeur faible est présentée vis-à-vis de la composante fondamentale de courant. Cette approche requiert bien entendu une structure plus coûteuse mais un circuit de contrôle plus simple.

Le second cas considère une commande plus complexe capable de contrôler chaque courant de bras de façon à obtenir la référence désirée à la fréquence fondamentale tout en

supprimant la composante de rang deux. Dans ces conditions, le dimensionnement des composants passifs est réduit puisque seul l'harmonique de courant à fréquence fondamentale est considéré. La complication du contrôle n'est pas aujourd'hui un problème grâce au large choix de dispositifs numériques de commande disponibles sur le marché. Ainsi, avons-nous privilégié ce cas dans la suite du travail de thèse.

Chapitre III : Nouvelles topologies de convertisseurs modulaires multiniveaux.

Dans ce chapitre, nous proposons et étudions et différentes topologies pour le convertisseur modulaire multiniveaux afin d'obtenir différentes propriétés en termes de réversibilité de tension ou de courant.

La première topologie considérée pour réaliser un bloc élémentaire est une simple cellule de commutation. C'est celle qui est utilisée dans la version de base du MMC (Figure III-5). Cette topologie est bidirectionnelle en courant et unipolaire en tension. Pour cette raison, en cas de court-circuit sur le côté *DC*, le système multiniveaux n'est pas en mesure de limiter le courant ce qui risque de détruire les semi-conducteurs. Seules les cellules bipolaires sont en mesure de limiter le courant en cas de court-circuit sur le côté *DC*. Dans ce but, nous introduisons le pont asymétrique et le pont complet. La première structure (Figure III-8) est bipolaire en tension mais unidirectionnelle en courant. Cette topologie rend le MMC peu adaptée au réglage de la puissance réactive mais dans le cas où le facteur de puissance est unitaire, cette topologie étant unidirectionnelle en courant, le système effectue l'inversion de la puissance en inversant la tension DC, ce qui est typique des CSC à thyristors. Pour cette raison, une telle structure peut être utilisée pour le remplacement immédiat des convertisseurs à thyristors. Par la suite, nous considérons également le pont complet (Figure III-11). Assurément, cette structure est la plus flexible car elle est simultanément bidirectionnelle en courant et en tension, mais par rapport aux deux précédentes elle exige le double de composants semi-conducteurs.

Dans ce chapitre, nous présentons une approche analytique pour le calcul des pertes dans les semi-conducteurs. Elle permet par la suite une évaluation directe et rapide du rendement du convertisseur AC/DC. Jusqu'à présent, dans la littérature, une telle approche n'avait pas été proposée pour le MMC car la forme d'onde du courant dans les semi-conducteurs rend le calcul des pertes très complexe.

A la suite de la validation des formules analytiques par des simulations avec les modules de calcul de pertes du logiciel PSIM, nous effectuons une comparaison du rendement du système en considérant l'utilisation des trois topologies mise en avant ci-dessus. La comparaison est effectuée pour une puissance de 100 MW et une tension DC de 160 kV. En termes de rendement, la structure à simples cellules est la moins dissipative. Les deux autres à base de cellules bipolaires présentent des pertes plus élevées car elles requièrent au final plus de composants semi-conducteurs. Bien que ces topologies permettent au système de mieux gérer les conditions de court-circuit DC, une baisse même minime au niveau du rendement (de l'ordre 0,5%) est difficilement acceptable compte tenu des niveaux de puissance mis en jeu.

Nous présentons ensuite une nouvelle structure modulaire multiniveaux (Figure III-28) de convertisseur AC/DC. Contrairement à la version traditionnelle, cette topologie adopte pour

chaque phase une seule branche de blocs élémentaires et une seule boucle de contrôle du courant. D'autre part, celle-ci est connectée avec le réseau alternatif triphasé à travers un transformateur zig-zag. Le dimensionnement des composants réactifs et des semi-conducteurs est identique à la version de base. A titre d'exemple, nous proposons cette nouvelle structure pour remplacer les anciens redresseurs à base de diodes ou thyristors (Figure III-30). Nous développons ce remplacement en conservant le même transformateur de ligne et ainsi les mêmes niveaux de courant et tension. Nous effectuons les simulations en considérant un système de 10 MVA.

Chapitre IV : Commande MLI pour les convertisseurs modulaires multiniveaux

Nous développons dans ce chapitre le contrôle pour les structures MMC en considérant une modulation (commande MLI classique avec entrelacement des porteuses). A chaque fois, les simulations valident l'étude en considérant un système de 100 MW avec une tension de 160 kV sur le côté continu et côté alternatif un fonctionnement à facteur de puissance unitaire en mode onduleur ou redresseur.

La commande pour convertisseurs modulaires multiniveaux proposée dans ce chapitre comporte trois boucles de contrôle (Figure IV-3) :

- Le contrôle du courant assure que chaque courant de branche ait les bonnes valeurs des composantes AC et DC nécessaires pour obtenir la puissance requise. Après avoir établi les équations électriques du MMC triphasé, nous exprimons les grandeurs électriques dans un repère tournant dq synchronisé sur le réseau alternatif. Une fois les équations établies dans ce nouveau repère, nous effectuons la synthèse des régulateurs PI de manière à ce que le système soit stable, capable de suivre la consigne de courant à la fréquence fondamentale et de supprimer la composante harmonique de courant de rang 2.
- En amont du contrôle de courant il faut assurer l'équilibre des énergies stockées dans les condensateurs. Compte tenu de la puissance mise en jeu côté continu, cette partie du contrôle adapte la puissance active afin de maintenir constantes les tensions sur les condensateurs des blocs. A cet effet un correcteur PI, dont nous donnons la synthèse, assure pour les branches positive et négative le contrôle de la valeur moyenne des tensions condensateurs.
- Dans une branche du convertisseur, les tensions sur chaque bloc peuvent être déséquilibrées à cause des dispersions sur les valeurs des composants passifs et des pertes différentes dans les semi-conducteurs. Pour cela, dans le but de réguler chaque tension condensateur à la valeur désirée, nous prévoyons un contrôle local basé sur un correcteur proportionnel qui agit sur le signal modulant au niveau de chaque bloc élémentaire. Des simulations, basées sur un convertisseur ayant des branches avec des pertes par blocs différentes, valident l'efficacité de ce réglage.

Chapitre V : Prototype de convertisseur modulaire multiniveaux de 10 kW.

Afin de valider les résultats de calcul et de simulation, nous avons réalisé un prototype à puissance réduite. La structure inclut 18 cellules de commutation, elle est prévue pour fonctionner avec une tension DC de 600 V pour une puissance nominale de 10 kW (Figure V-

1). Cette maquette a été conçue et réalisée au LAPLACE. Le contrôle est implanté sur une plateforme DSP-FPGA.

Nous testons une première configuration conformément à la Figure V-5. Nous considérons une branche unique par phase avec une charge RL triphasé de 4 kW en série, le tout est alimenté par une source de tension continue de 600 V. Après avoir étudié les boucles de contrôle et réalisé des simulations préliminaires, nous effectuons les tests en boucle fermée. Cette configuration a été initialement choisie car nous savons que la structure MMC classique, à deux branches par phase, peut difficilement limiter le courant en condition de défaut. Ainsi, la présence de la charge RL en série dans chaque branche limite « naturellement » le courant et permet sans danger la mise au point des chaines de mesure des signaux et la validation de la synthèse des régulateurs.

La bonne correspondance entre les résultats expérimentaux et les simulations nous permet alors d'aborder le fonctionnement dans une configuration MMC classique mais dans un premier temps avec un contrôle en boucle ouverte (Figure V-20) sur une charge RL triphasée de 5 kW.

Des simulations en boucle fermée avec un contrôle en boucle fermée dans un repère dq valident ensuite la synthèse des correcteurs pour le système de 10 kW (Figure V-16). Les simulations sont effectuées sur une charge RL triphasée (Figure V-20). Il nous reste à effectuer les tests en boucle fermée sur la maquette.

Conclusions et Perspectives

Aujourd'hui, les connexions HVDC constituent un élément de réponse aux besoins énergétiques mondiaux croissants. La technologie multiniveaux, associé au développement de semi-conducteurs haute tension contrôlés au blocage, va permettre aux convertisseurs de type onduleur de tension (VSC) de devenir la topologie la plus employée dans les systèmes HVDC. Toutefois, grâce aux avantages découlant de la facilité de mise en série des thyristors, les structures CSC restent encore mieux adaptées aux tensions élevées. A court terme, l'écart entre les deux topologies pourrait se réduire de manière significative grâce aux performances offertes par les thyristors blocables de type IGCT. Ces composants en boitier pressé présentent par rapport aux modules classiques plusieurs avantages : En cas de court-circuit dans une cellule, il n'y a pas de risque d'explosion du boitier et la structure monolithique de l'IGCT (*single wafer*) est plus adaptée pour l'encapsulation en boitier pressé qu'un ensemble de petites puces IGBT.

Ce travail de thèse a porté sur des topologies convertisseurs modulaires multiniveaux. Pour les études préliminaires, nous avons proposé un « macro modèle », indépendant de la topologie des blocs élémentaires, qui a permis une analyse directe du fonctionnement et des simulations plus rapides.

Le dimensionnement du convertisseur a été effectué pour deux stratégies de contrôle. La première considère seulement un contrôle de la composante fondamentale du courant de sortie mais entraîne la circulation d'un harmonique de rang deux dans les branches du circuit. La mise en œuvre d'inductances couplées dans les branches du convertisseur pourrait

constituer une bonne solution pour limiter ce courant mais dans la gamme de puissance visée (GW), une telle technologie augmenterait les coûts de manière considérable. En revanche, la seconde approche, consiste à contrôler le courant dans chacune des branches mais requiert un système de contrôle plus performant basé sur une commande en dq. A cette condition, la composante harmonique de courant de rang deux est supprimée, ce qui permet de minimiser le volume et donc le coût des éléments réactifs.

L'emploi des différentes topologies de bloc élémentaire rend le MMC plus flexible en termes de réversibilité en tension et en courant. En termes de pertes, à niveaux de puissance et de tension continue identiques, la simple cellule est la plus intéressante. Cependant, les autres topologies qui fournissent une tension de sortie bipolaire (pont asymétrique et pont complet) rendent la structure apte à limiter le courant en cas de court-circuit côté continu.

La commande MLI classique avec entrelacement des porteuses permet une réduction de la fréquence de commutation ce qui minimise les pertes dans les semi-conducteurs. Toutefois cette technique de modulation présente une limite inférieure en fréquence de commutation de l'ordre de 200 Hz. Quand le nombre de niveaux est très élevé, la modulation de la tension en « marches d'escalier » peut être très intéressante. Une étude de cette technique de modulation (marge d'escalier) sera développée prochainement. En effet, il nous reste à analyser l'impact de cette stratégie de modulation sur le dimensionnement des éléments réactifs et les pertes dans les semi-conducteurs pour la comparer à la commande MLI classique avec entrelacement des porteuses.

Différents aspects pourraient rendre le pont asymétrique intéressant dans les applications HVDC. En effet, par rapport à la structure classique, pour une même amplitude relative d'ondulation de tension, la capacité du condensateur de chaque bloc peut être réduite. De plus, comme le système effectue l'inversion du flux de puissance par le changement de polarité de la tension DC, cette topologie peut être employée pour remplacer les structures CSC dans des sous-stations HVDC avec l'avantage de travailler à facteur de puissance unitaire.

La nouvelle structure à une seule branche par phase (single loop) proposée dans le chapitre III permet un contrôle plus simple. Elle ne requiert pas d'inductances en série dans les branches puisqu'elle utilise directement l'inductance de fuite du transformateur dont le secondaire doit être couplé en zigzag pour annuler la composante continue du flux dans les colonnes. De plus l'isolement du transformateur est dimensionné uniquement pour la tension du réseau alternatif. Ceci n'est pas le cas de la configuration classique du MMC où, en plus de la composante alternative de tension, le transformateur doit supporter une tension d'isolement continue égale à la moitié de la tension sur le lien *DC* (composante homopolaire). Au-delà de ces considérations, et de manière plus générale, l'utilisation de cette nouvelle structure pourrait être intéressante pour remplacer d'anciens redresseurs à diodes ou à thyristors, en apportant les avantages découlant de la structure VSC.

Un prototype de 10 kW a été développé au laboratoire LAPLACE. Afin d'interfacer le circuit de puissance avec le système de contrôle, un ensemble de cartes « Interface Hardware » a été réalisée. Cet ensemble de cartes adapte les niveaux des signaux provenant des capteurs du prototype aux niveaux des tensions d'entrée du dispositif de commande. Il permet aussi le

filtrage du bruit pour les signaux analogiques. En ce qui concerne les signaux numériques de commande en provenance du dispositif de contrôle, ceux-ci sont transmis aux cellules de commutation via des fibres optiques.

Avant de démarrer les essais en puissance, une procédure préliminaire de test a été effectuée. Tous les capteurs ont été calibrés et toutes les connexions de la chaine de mesure ont été vérifiées. Enfin, l'interconnexion des masses de tout le système a été effectuée petit à petit afin d'éviter tout problème de compatibilité électromagnétique (CEM).

Les résultats expérimentaux avec une commande MLI classique avec entrelacement des porteuses ont été obtenus pour la structure à boucle simple et la structure classique. Le bon fonctionnement des boucles de contrôle a permis de valider le modèle du système et la synthèse des régulateurs.

Prochainement, ce prototype permettra d'une part de tester la structure à une branche par phase avec le transformateur à secondaire couplé en zigzag et d'autre part le fonctionnement en boucle fermée avec la commande en dq puis la modulation en « marche d'escalier ».

RIASSUNTO DETTAGLIATO DELLA TESI IN LINGUA ITALIANA

Capitolo I: A proposito di HVDC

Questo capitolo tratta i sistemi HVDC (le transport d'énergie électrique en courant continu Haute Tension) andandone ad evidenziare il ruolo chiave che hanno nel campo della trasmissione dell'energia elettrica attraverso la consultazione di circa 40 riferimenti bibliografici.

L'adozione di sistemi HVDC negli ultimi 40 anni ha avuto un ruolo fondamentale per i sistemi di trasmissione per una serie di considerazioni tecniche ed economiche.

- Rispetto ai sistemi di trasmissione AC, trasmettere in corrente continua, nonostante il costo addizionale dovuto alle sottostazioni di conversione, inizia a diventare conveniente per distanze maggiori di 800 km per linee aeree e 50 km per linee sottomarine (Figure I-1).

- Il continuo miglioramento delle tecnologie dei dispositivi semiconduttori essendo al cuore delle tecnologie HVDC

- Sistemi in corrente continua consentono interconnessioni tra reti eterogenee che possono essere asincrone tra loro e/o a frequenza diversa.

Una descrizione sui principi di connessione HVDC è stata illustrata facendo riferimento alle principali installazioni attualmente esistenti ciascuna delle quali in grado di gestire potenze dell'ordine dei GWs.

Due tipi di connessione HVDC sono utilizzate. Quelle basate su convertitori AC/DC di corrente (CSC) e quelle basate su convertitori AC/DC di tensione (VSC). I lavori presenti nella letteratura corrente fino ad oggi si sono sempre focalizzati sulla topologia dei convertitori, in questo lavoro una delucidazione esaustiva sul concetto di trasferimento di potenza di tipo HVDC sia per strutture CSC che VSC è stata data.

Prima di scendere nel dettaglio i principali dispositivi semiconduttori disponibili sul mercato ed impiegati per le alte tensioni sono stati descritti attraverso la consultazione di circa venti riferimenti bibliografici. Lo studio ha messo in luce le varie evoluzioni dei dispositivi dandone un'ordine di grandezza sulle tensioni e correnti nominali sostenibili per ciascuno di essi. Inoltre una descrizione dettagliata della tecnica presspack è stata data giacché tale tecnologia può essere considerata la meglio candidata per l'utilizzo e l'impiego di dispositivi semiconduttori nelle alte potenze.

Una descrizione dei convertitori CSC basati su tiristori è stata fornita al fine di rendere meglio comprensibile l'approccio adottato per lo scambio di potenza per queste strutture. Grazie al fatto che i tiristori non presentano problemi di connessione diretta in serie, i sistemi CSC-HVDC riescono a raggiungere tensioni dell'ordine dei 500 kV. Ovviamente la topolgia non consente il controllo indipendente della potenza attiva e reattiva ed inoltre esibisce un

contenuto armonico in corrente tale da richiedere dispositivi di filtraggio che occupano il 20-30 % della superficie totale di una sottostazione (Figure I-42).

Una descrizione dei convertitori VSC modulati PWM (MLI) basati su dispositivi di commutazione controllabili sia in apertura che in chiusura (IGBT) è stata fornita. Dopodiché la trasmissione di energia HVDC basata su convertitori VSC è stata illustrata. Le topologie VSC riescono ad effettuare il trasferimento di potenza attiva e reattiva in maniera indipendente. D'altro canto per topologie classiche a due livelli si riesce al massimo ad operare a 320 kV a causa dei problemi dovuti alla messa in serie di dispositivi IGBT.

Le topologie VSC sono state prese in considerazione nel lavoro. In particolare una descrizione delle strutture multilivello è stata data grazie alla loro capacità di lavorare ad alte tensioni. Tali topologie rispetto a quelle tradizionali riescono a garantire una forma d'onda quasi sinusoidale riducendo il contenuto armonico e permettendo una riduzione degli elementi di filtraggio. All'interno delle topologie multilivello la struttura modulare multilivello (MMC) è stata presentata nel capitolo e studiata nel lavoro di tesi. Tale struttura consiste nella messa in serie di convertitori elementari (Figure I-62) normalmente identici (per questo modulare). Tale struttura è stata preferita a quelle tradizionali giacché garantisce una modularità in termini di produzione industriale e non ha limitazioni superiori sul valore della tensione DC poiché è possibile sempre aggiungere convertitori elementari in serie.

Capitolo II: Strutture modulari multilivello

La struttura modulare multilivello è stata studiata in questo capitolo. La configurazione trifase per questa struttura è formata dalla connessione di due rami per fase (Figure II-1). Ogni ramo impone metà della tensione DC e la tensione al lato AC. Ciascun ramo inoltre conduce un terzo della corrente DC e la metà della corrente AC. La combinazione tra i due rami fa si che si ottengano le correnti e tensioni AC e DC necessarie al trasferimento di potenza richiesto. Per l'analisi un modello medio della struttura è stato estratto (macro modello) al fine di semplificare le considerazioni preliminari. Tale modello non considera gli effetti delle armoniche dovuti ai dispositivi di commutazione ma garantisce una maggiore velocità nelle simulazioni poiché semplifica i calcoli. Lo studio inoltre è stato ottenuto indipententemente dalla scelta della topologia per il convertitore elementare e considerando una phase shifted sinusoidal PWM (commande MLI classique avec entrelacement des porteuses). La potenzialità dello studio, oltre alla semplificazione della comprensione, sta nel fatto che tale struttura è stata resa altamente flessibile e versatile in termini di tensioni e correnti gestite.

In una analisi preliminare correnti e tensioni del sistema sono state analizzate. Dal punto di vista armonico di corrente, ciascun ramo, oltre alle componenti DC ed AC conduce una componente AC al doppio della frequenza fondamentale che rimane all'interno della struttura (corrente circolante in Figure II-9). Questa componente deriva dal bilanciamento energetico tra i due bracci che compongono ogni fase. La soppressione di tale componente gioca un ruolo fondamentale nel dimensionamento dei componenti reattivi che è stata effettuata considerando due casi.

Il primo caso considera un sistema controllato in maniera tale per cui non si è in grado di sopprimere l'armonica di II ordine della corrente di ramo. Per tale motivo la compensazione è

effettuata in maniera hardware. Al crescere del condensatore posto in parallelo a ciascun convertitore elementare e dell'induttore di ramo tale armonica si riduce. Per problemi di controllabilità del sistema dovuti ad elevati valori dell'induttore di ramo una nuova configurazione di tipo tripolare per l'induttore è stata proposta nel lavoro. Tale induttore è configurato in maniera tale da imporre una elevata induttanza di ramo al fine di sopprimere la II arminica nella corrente ed una ridotta induttanza di uscita garantendo la controllabilità del sistema. Tale approccio ovviamente richiede un hardware più costoso ma un controllo più semplice.

Il secondo caso considera un controllo leggermente più complesso capace di controllare ciascuna corrente di ramo in maniera tale da ottenere il riferimento desiderato alla armonica fondamentale di corrente e di sopprimere anche la corrente circolante nel ramo alla seconda armonica della fondamentale. In tali condizioni il dimensionamento dei componenti passivi si riduce giacché solo l'armonica di corrente a frequenza fondamentale è considerata. La complicatezza del controllo non è un problema al giorno d'oggi grazie alla vasta scelta di dispositivi di controllo disponibili sul mercato. Per questo motivo è stato preferito in questo lavoro di tesi. Per tutti i casi, simulazioni su un sistema da 100 MW composto da 64 convertitori elementari per ramo hanno validato lo studio.

Capitolo III: Nuove topologie multilivello per sottostazioni HVDC

In questa parte del lavoro nuove configurazioni per la struttura modulare multilivello sono state studiate e proposte. Ciò è avvenuto andando a cambiare di volta in volta la topologia del convertitore elementare. Disporre di differenti topologie ha reso la struttura MMC più versatile e flessibile nei confronti dei livelli di tensione e corrente.

La prima topologia considerata come convertitore elementare è la cella semplice che rappresenta la versione base dell'MMC. Questa topologia è bidirezionale in corrente ma unipolare in tensione. Per tale motivo in condizioni di fault DC il sistema multilivello non è in grado di limitare la correne di corto circuito rischiando di danneggiare i dispositivi semiconduttori. Solo celle bipolari sono in grado di meglio limitare la corrente in condizioni di fault DC. A tale scopo il ponte asimmetrico ad H ed il ponte intero ad H sono stati considerati. La prima struttura (Figure III-8) è bipolare in tensione ma unidirezionale in corrente. Per tale motivo l'impiego di questa topologia rende la struttura MMC poco adatta a scambi di potenza reattiva. In condizioni di fattore di potenza unitario, essendo tale topologia unidirezionale in corrente, il sistema effettua l'inversione della potenza tramite l'inversione della tensione che è tipico dei sistemi CSC. Per questo motivo tale struttura può essere anche utilizzata per il rimpiazzo immediato di convertitori basati su tiristori. Infine tra le celle bipolari anche il ponte ad H è stato considerato (Figure III-11). Ovviamente tale struttura è la più flessibile delle prime due essendo anche bidirezionale in corrente ma esige il doppio dei componenti.

In questa parte un approccio analitico per il calcolo delle perdite nei dispositivi è stato dato. Tale approccio ha reso la valutazione della efficienza del sistema diretta veloce. Tale approccio era stato evitato in letteratura giacché la componente continua della forma di

corrente nei dispositivi, dovuta alla struttura MMC, rendeva il calcolo delle perdite molto complesso. Nel presente lavoro invece la formalizzazione analitica delle perdite è stata formalizzata e validata.

A valle della validazione delle forme analitiche tramite il software PSIM un confronto sul rendimento del sistema è stato effettuato considerando l'uso delle tre topologie evidenziate sopra. Il confronto è stato effettuato a parità di potenza (100 MW) e di tensione DC (160 kV). In termini di rendimento la singola cella è la meno dissipativa. Le altre due celle bi-polari hanno un incremento delle perdite giacché richiedono un incremento dei componenti, tali perdite non sono accettabili per i livelli di potenza gestita. Ovviamente tali topologie permettono al sistema di gestire meglio le condizioni di faults.

Successivamente nel capitolo una nuova struttura modulare multilivello è presentata (Figure III-28) chiamata Raddrizzatore a singola semionda. Per ogni fase questa topologia adotta un solo ramo rispetto alla versione tradizionale. D'altro canto si interfaccia con la rete attraverso un trasformatore zig-zag. Il dimensionamento dei componenti reattivi e dei dispositivi semiconduttori è lo stesso della versione base. Al fine di validare lo studio del macromodello questa nuova struttura è stata proposta per rimpiazzare i vecchi raddrizzatori basati su diodi o tiristori (Figure III-30). Il rimpiazzo è stato sviluppato conservando lo stesso trasformatore di linea e dunque gli stessi livelli di corrente e tensione. Simulazioni sono state effettuate considerando un sistema da 10 MVA.

Capitolo IV: Un nuovo controllo PWM per le strutture modulari multilivello

Un nuovo controllo per le strutture MMC è stato sviluppato in questo capitolo considerando una modulazione (commande MLI classique avec entrelacement des porteuses). Volta per volta simulazioni hanno validato lo studio considerando un sistema da 100 MW con una tensione DC di 160 kV. Le simulazioni sono state inoltre fornite per condizioni di funzionamento a fattore di potenza unitario in modalità inverter e raddrizzatore.

Il controllo dei sistemi MMC in letteratura hanno sempre cercato di sopprimere la seconda armonica di ramo della corrente in maniera parallela al controllo tradizionale. Ci sono numerosi lavori che adottano tale sistema rendendo il controllo alquanto complesso sia alla comprensione che all'implementazione [49]-[51].

Il controllo tipico per i sistemi multilivello è costituito da tre cicli di controllo fondamentali (Figure IV-3).

- Il controllo di corrente , assicura che ciascuna corrente di ramo abbia i giusti valori per le componenti AC e DC necessare ad ottenere la potenza richiesta. L'approccio per tale controllo è stato effettuato tramite una sovrapposizione degli effetti. Dopo aver impostato le equazioni caratterizzanti il sistema è stata effettuata una trasformazione delle grandezze nel sistema di riferimento ad assi rotanti DQ. Una volta definite le equazioni, la sintesi dei regolatori PI è stata effettuata in maniera tale rendere il sistema in grado di inseguire la corrente desiderata e sopprimere la seconda armonica di corrente (corrente di ricircolo) nei margini di stabilità.

Il sistema di controllo proposto nel lavoro di tesi è lineare ed, attraverso la taratura dei regolatori, agisce in maniera tale da sopprimere anche la seconda armonica a frequenza fondamentale di corrente. L'innovazione sta nel fatto che il tutto è effettuato attraverso un singolo ciclo senza l'aggiunta di loops addizionali adottati in [50]-[51].

- A monte del controllo di corrente è posto il bilancio di energia di ramo. Tale parte di controllo regola la potenza attiva necessaria a mantenere tutte le tensioni sui condensatori di ramo costanti al valore desiderato. La sintesi dei regolatori PI è stata fornita.

- Ciascuna cella di ramo può essere sbilanciata a causa delle differenti tolleranze dei componenti passivi, conduzioni diseguali e/o perdite differenti nei dispositivi semiconduttori ed infine differenti risoluzioni dei sensori. Per questo motivo al fine di bilanciare ogni cella al valore di tensione desiderato, un controllo locale è stato previsto definito come il bilancio della tensione di cella. Un correttore proporzionale per ogni convertitore elementare è stato adottato e sintetizzato. Tale controllo in maniera indipendente dai due precedenti agisce direttamente sull'indice di modulazione. Simulazioni in condizioni di celle sbilanciate hanno validato lo studio.

Capitolo V: Il prototipo MMC da 10 kW

Al fine di validare i risultati analitici e simulativi un prototipo a potenza ridotta è stato realizzato. Tale struttura include 18 celle di commutazione di tipo semplice (simple cell), una tensione DC di 600 V ed una potenza nominale di 10 kW (Figure V-1). Il prototipo è stato progettato e realizzato presso il LAPLACE. Inoltre al fine di effettuare i test sperimentali il controllo è stato implementata tramite piattaforma DSP-FPGA. I livelli di potenza e di tensione scelti per il prototipo sono abbastanza alti per una rispetto a quelli adottati in letteratura per la sperimentazione da laboratorio di sistemi MMC.

Una prima configurazione in modalità single loop è stata testata (Figure V-5). In particolare solo un ramo per fase si è considerato con in serie un carico RL da 4 kW. Il tutto in parallelo alla sorgente DC. Dopo la sintesi del controllo e simulazioni preliminari, sono stati effettuati tests a ciclo chiuso. Questa è una configurazione intermedia che ha un duplice scopo. È noto che la classica struttura MMC è poco capace di limitare la corrente di ramo in condizioni di faults, per questo motivo non è stata preferita come prima prova. La presenza del carico RL in serie al ramo infatti limita la corrente nel ramo garantendo lo stesso un set-up delle catene di segnale e la validazione della sintesi dei regolatori in condizioni di sicurezza. È definita configurazione intermedia giacché a causa delle proprietà unipolari della cella semplice al carico viene imposta anche una componente DC all'interno del ramo. In ogni caso la buona corrispondenza tra simulazioni e prove sperimentali hanno reso il passaggio alla configurazione con trasformatore zig-zag immediato.

In un secondo step la struttura MMC a ciclo aperto è stata considerata (Figure V-20). Simulazioni preliminari a ciclo chiuso con un controllo nel sistema di riferimento rotante DQ hanno validato la sintesi dei controllori per il sistema da 10 kW (Figure V-16). Le simulazioni sono state effettuate imponendo la rete al lato AC. Il sistema è stato dunque testato in

modalità raddrizzatore e inverter a fattore di potenza unitario. Successivamente prove sperimentali a ciclo aperto sono state effettuate imponendo al sistema un carico RL di circa 5 kW (Figure V-20) al fine di validare la giusta modulazione e il corretto dimensionamento dei componenti reattivi (condensatori ed induttori). Resta da effettuare ovviamente il passaggio dei test a ciclo chiuso per la struttura MMC.

Conclusioni e Prospettive

Al giorno d'oggi le connessioni HVDC sono una buona risposta alla fabbisogno energetico mondiale che è sempre più crescente. Le topologie multilivello stanno rendendo i Voltage source converters (VSC) tra i più impiegati nei sistemi HVDC. Lo sviluppo dei dispositivi semiconduttori controllati in fase di spegnimento ed impiegati per alte tensione hanno reso queste strutture molto interessanti. D'altro canto grazie ai vantaggi derivanti dalla facilità della messa in serie di tiristori, le strutture CSC gestiscono meglio le alte tensioni. Nel prossimo futuro, il divario tra le due topologie verrà decisamente ridotto grazie alle prestazioni offerte dai dispositivi IGCT sia nella fase di accensione che di spegnimento. L'inscatolamento a pressione (press pack) porta inoltre una serie di vantaggi rispetto ai moduli classici specialmente in condizioni di emergenza dove c'è il rischio di esplosione. La struttura a singolo tassello (single wafer) rende l'IGCT più adatto per l'inscatolamento a pressione rispetto all'IGBT. Per queste ragioni l'IGCT sembra essere il dispositivo più attrattivo in applicazioni VSC-HVDC.

Il lavoro di tesi è stato focalizzato sui convertitori modulari multilivello. Per studi preliminari il "macromodello" ha consentito valutazioni dirette e simulazioni più veloci. Inoltre ha reso il modello indipendente dalla particolare topologia.

Il dimensionamento del sistema è stato effettuato attraverso due approcci di controllo. Il primo considera solo un controllo sulla corrente di uscita AC che determina una considerevole seconda armonica nel ramo. L'induttore tripolare accoppiato potrebbe essere una buona soluzione al fine di limitare questa corrente ma nel campo delle applicazioni di alta potenza, la particolarità dell'hardware accresce i costi in maniera considerevole. Il secondo approccio invece consiste nel controllo della corrente di ciascun ramo, inoltre esso richiede un sistema di controllo più efficiente basato sul sistema di riferimento rotante DQ. Sotto questa condizione la seconda componente armonica della corrente è cancellata andando a ridurre i costi degli elementi reattivi.

L'impiego di differenti topologie come convertitore elementare rende l'MMC più flessibile in termini di reversibilità di tensione e corrente. In termini di perdite a parità di potenza e tensione DC, la cella semplice è più conveniente. Le altre topologie però che forniscono una tensione bipolare (HB asimmetrico e ponte ad H) rendono la struttura capace di limitare la corrente di corto circuito in caso di fault DC.

La commande MLI classique avec entrelacement des porteuses porta ad una riduzione della frequenza di switching e dunque riduce le perdite nei dispositivi. Certamente questa tecnica di modulazione presenta un limite inferiore sulla frequenza di switching. Quando il numero dei livelli è molto elevato la modulazione stai case (marge d'escalier) può essere molto interessante per strutture multilivello. Uno studio della modulazione (marge d'escalier) sarà

presto sviluppato. Infatti rimane da fare una investigazione sugli effetti della modulazione nei confronti del dimensionamento di elementi reattivi e nei confronti delle perdite nei dispositivi rispetto alla (commande MLI classique avec entrelacement des porteuses).

Differenti aspetti potrebbero rendere il ponte asimmetrico ad H interessante nelle applicazioni HVDC. Se questa topologia è scelta, il condensatore di cella potrebbe essere ridotto a parità di ampiezza di oscillazione della tensione. Siccome il sistema effettua l'inversione del flusso di potenza tramite il cambiamento della polarità della tensione DC, questa topologia può essere impiegata per rimpiazzare strutture CSC per sottostazioni HVDC con il vantaggio di lavorare a fattore di potenza unitario.

La struttura nuova a controllo unico (single loop) proposta nel capitolo III permette un controllo più semplice. La topologie non richiede il doppio induttore poiché utilizza l'induttore parassita posto in serie al trasformatore accoppiato zig-zag. l'accoppiamento del trasformatore richiede più rame di un classico avvolgimento. L'isolamento del trasformatore deve essere effettuato solo per la tensione AC. Questo non è il caso della classica configurazione per l'MMC dove il trasformatore deve sostenere un isolamento DC pari alla metà della tensione sullo DC link (sequenza omopolare). Oltre a queste considerazioni, l'uso di questa nuova struttura potrebbe essere interessante per rimpiazzare i vecchi raddrizzatori garantendo i vantaggi derivanti dalle strutture VSC.

Un prototipo da 10 kW è stato sviluppato nel laboratorio LAPLACE. Al fine di interfacciare il circuito di potenza con il sistema di ptototipazione rapida, una piattaforma di schede piazzate sulla struttura chiamata "Hardware di Interfaccia" è stata realizzata. Questo hardware adatta i livelli dei segnali provenienti dai sensori del prototipo verso il livello delle tensioni di ingresso del dispositivo di pototipazione rapida. Inoltre tale hardware fornisce il filtraggio del rumore per i segnali analogici. Anche per i segnali digitali provenienti dal dispositivo di prototipazione, una conversione elettro-ottica è stata fornita dall'hardware di interfaccia al fine di controllare le celle.

Prima di avviare le prove in potenza, una procedura preliminare è state eseguita. Tutti i sensori sono stati calibrati e la giusta connessione della catena di segnale è stata verificata. Infine l'ottimizzazione della configurazione delle masse di tutto il sistema è stata effettuata passo dopo passo al fine evitare tutti i probleme dovuti alla compatibilità elettromagnetica (EMI)

Risultati sperimentali in (commande MLI classique avec entrelacement des porteuses) sono stati ottenuti per la struttura a singolo ciclo e quella classica. Il buon funzionamento dei cicli di controllo ha validato il modello del sistema e la sintesi dei regolatori.

Prossimamente, questo prototipo permetterà di testare la struttura a singolo ciclo con il trasformatore zig-zag, il funzionamento a ciclo chiuso nel sistema di riferimento dq e la modulazione a (marge d'escalier).

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Chapter I. **HVDC SYSTEMS**

This chapter presents the HVDC systems by pointing out the key role that they play in the field of electrical energy transmission. After a chronological description of the penetration of the HVDC system in the transmission grid scenario, the most employed structures are depicted and their advantages/drawbacks are described. A comparison is achieved between the Current Source Converter and Voltage Source Converter based HVDC. Nowadays, regarding economic and technical considerations VSC-HVDC systems are most popular. Then, this work focuses on the topology based on Modular Multilevel Converters (MMCs) which is more and more often chosen for VSC-HVDC power stations

I.1 About HVDC

The world energy consumption is expected to increase by more than 54% every ten years [1]. Moreover, population growth and the development of "new economies" require energy sharing that has to keep in step to guarantee electrical grid voltage stability.

On the other hand, the Kyoto protocol to the United Nations framework convention on climate change defined the ways and the constraints of regulating energy production. Those in attendance at this meeting considered renewable energy sources as a good way to achieve the goal.

Since the beginning of the 21st century, many countries have chosen to deregulate the electricity sector. This has created a more flexible mix of energy sources by encouraging higher efficiencies, particularly with the introduction of private investments in the energy market.

In the scenario of electrical energy transmission growth, HVDC systems seem to best meet the purposes given. As affirmed in [1], thanks to their inherent power flow control capability and asynchronous feature, HVDC systems associated with flexible AC transmission systems (FACTS) are spreading all over the world.

In the last 40 years, HVDC has played a key role in transmission systems with a series of economic and technical considerations:

- As shown in Figure I-1, compared to AC transmission systems, HVDC transmission systems become more convenient for a distance depending on the line technology (around 800 km for overhead line and 50 km for underground or

submarine cables). Despite the fact that HVDC converter stations are expensive, the transmission line requires a reduced number of conductors which approximately leads to a reduction of one third of the cost.

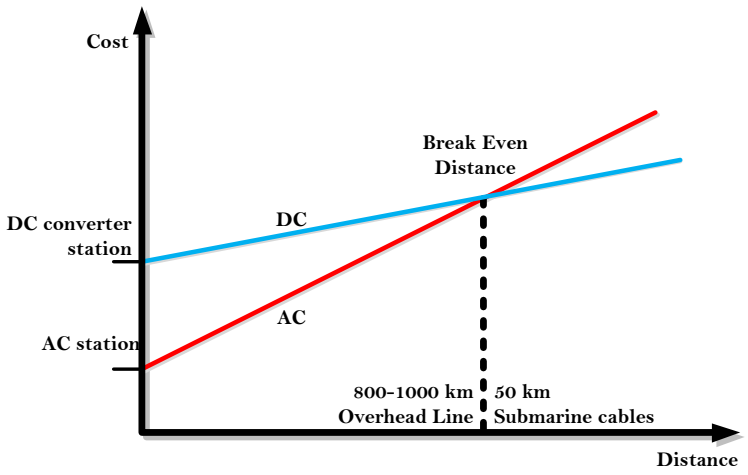


Figure I-1 - Estimation of the coasts for AC and DC transmission

- The ever-increasing improvements in power electronics devices, more particularly in the field of turn-off controlled semiconductors, are at the heart of HVDC technologies [2].
- HVDC systems allow interconnections between miscellaneous grids which can be asynchronous or with different operating frequencies. They facilitate integration of renewable sources like wind farms or photovoltaic plants.

Until 2005, according to [3], the total power installed in HVDC systems was around 55 GW, amounting to 1.4% of the worldwide installed generation capacity. The curve shown in Figure I-2 shows the trend of the main installations achieved in the world since 1970. In the next years, 48 GW of HVDC installed stations are expected by China alone. A detailed overview on the existing project can be further found in [4].

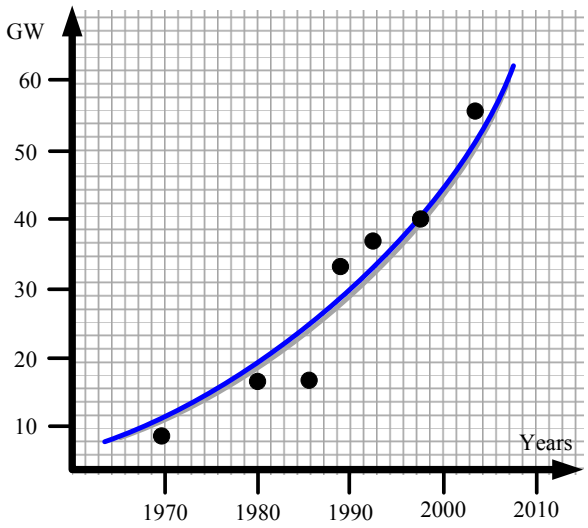


Figure I-2: Power provided by HVDC transmissions

I.2 HVDC Connection Systems

I.2.1 The concept of a HVDC connection

The evolution of the solid state devices essentially made possible the concept of the AC/DC conversion. The mercury arc valves were replaced by solid-state devices named thyristors since 1970s. The first thyristor employment was the Eel River in Canada based on Line-Commutated Converter (LCC), which was built by General Electric and went into service in 1972 [5]. Since that time onwards, the thyristor LCCs or Current Source Converters (CSCs) have been continuously diffusing and developing for HVDC applications, like the transmission systems for which the basic configuration is shown in Figure I-3. The typical CSC based HVDC connection assumes in steady state that the power flow is regulated by changing the sign of the averaged value of the voltages (V_{out1} *and* V_{out2}) imposed on the DC line. The system is adopted for high power levels, beyond 1 GW, for installations like the Itapiu system in Brazil (6.3 GW) [6], or the longest power transmission that links Xiangjiaba to Shanghai [7].

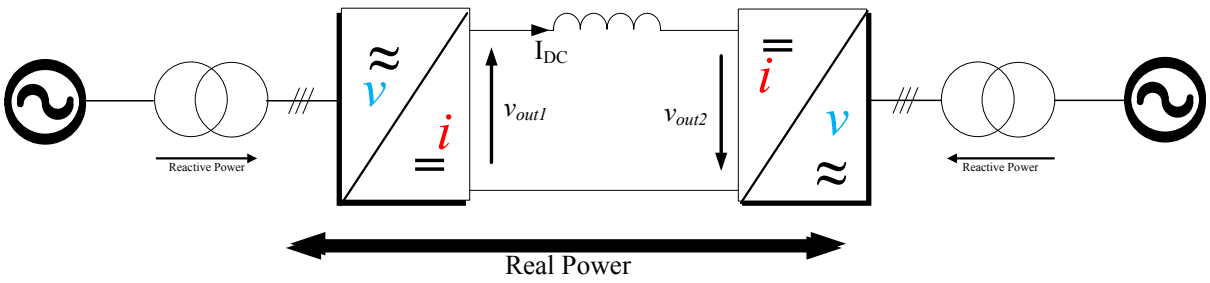


Figure I-3 - CSC-HVDC system base lay out

In TABLE I-1 examples of existing CSC-HVDC connections are listed. The table gives an idea of the power, level voltages and the transmission distances insured by these systems.

Project Name	***Completation Year***	***Power Rating***	***DC voltage***	***Covered Distance***	***Maker***	***Semiconductor devices***
France England	1986	2 GW	±270 kV	70 km	Alstom Grid	Thyristors
Shin-Shinano Sakuma	1993	0,3 GW	±125 kV		Mitsubishi	Thyristors
Norway Netherland	2008	0,7 GW	±450 kV	580 km	ABB®	Thyristors
Xiangjiaba Shanghai	2010	7.2 GW	±800 kV	1900 km	ABB®	Thyristors

TABLE I-1: Example of Existing CSC-HVDC connections

The huge DC voltage that these converters can reach is allowed thanks to the direct series connection of the thyristors. More detailed descriptions on the devices are given in the next section. Just to give an idea of the huge physical structure, an example in series connection of 336 thyristors such as the Shin-Shinano substation is given in Figure I-4. Another example is also given in Figure I-5. It corresponds to the substation located in France (Les mandarins) of the France – England HVDC interconnection.



Figure I-4: thyristor tower for the frequency converter on Shin-Shinano side



Figure I-5: Thyristor tower of the France-England connection on the french side

However, the development of high rated fully controllable switches, which are described in the next section, such as insulated gate bipolar transistors (IGBTs) and gate-commutated

thyristors (IGCTs) let the Voltage Source Converters (VSCs) be an attractive alternative to the CSCs for HVDC applications.

The level of power afforded for these systems goes hand in hand with the evolution of the VSC topologies and the voltage which the semiconductor device is able to sustain. A basic configuration of these connections is shown in Figure I-6. In steady state the power flow is regulated by changing the sign of the averaged value of the currents imposed on the DC line. The first VSC-HVDC installation, which consolidated the success of these systems, was the HVDC Hellsjön–Grängesberg (Sweden) from ABB, called HVDC Light [8]. It is a PWM-controlled system built at the beginning of 1997 [1]. The power rating is about 3 MW with a voltage of 10 kV. Many other installations are listed in [9].

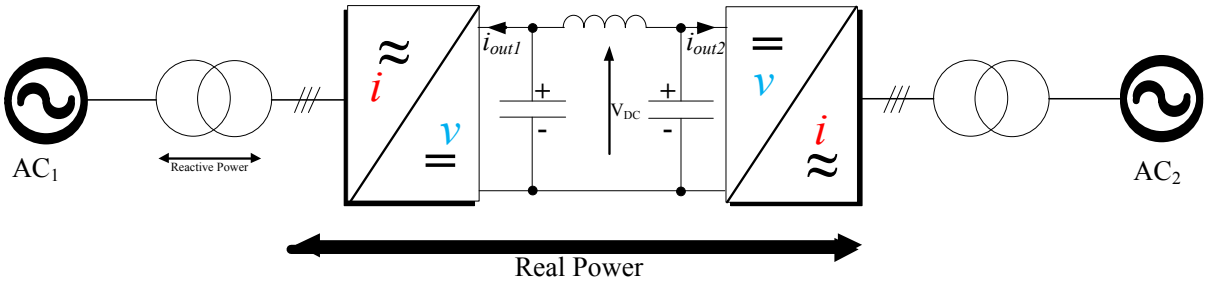


Figure I-6 - VSC-HVDC system base layout

First VSCs for HVDC applications were two-level inverters while three-level inverters (Neutral Point Clamped topology) were introduced later. To sustain the huge voltage the installations are composed by series connected IGBTs. ABB is the only maker which provides this configuration (Figure I-7 and Figure I-8) [10]. The configuration allows each VSC to sustain maximum 320 kV with a maximum power rating at one GW.



Figure I-7: Typical series valve tower of ABB

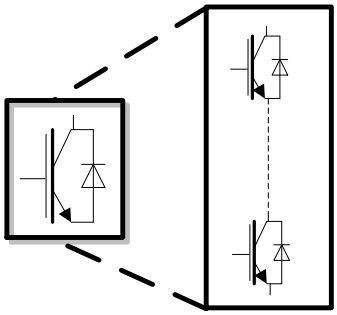


Figure I-8: IGBTs Series connected lay-out

The last generation of multilevel VSC for HVDC applications is the Modular Multilevel Converter (MMC or M2C), introduced by Marquardt and Lesnicar in 2002, [11]. The first application of MMC for HVDC was the Trans Bay Cable in San Francisco, California, powered by Siemens in November 2010, [12]. Another example of VSC HVDC connection based on MMC topology is the France-Spain interconnection "INELFE" [13] (Figure I-9). The connection is achieved with a DC voltage of ±320 kV and involves two converters of 1 GW each one. In Figure I-10 is depicted a typical tower provided for a phase of the MMC. An overview of a typical MMC based substation for HVDC connections is shown in Figure I-9.

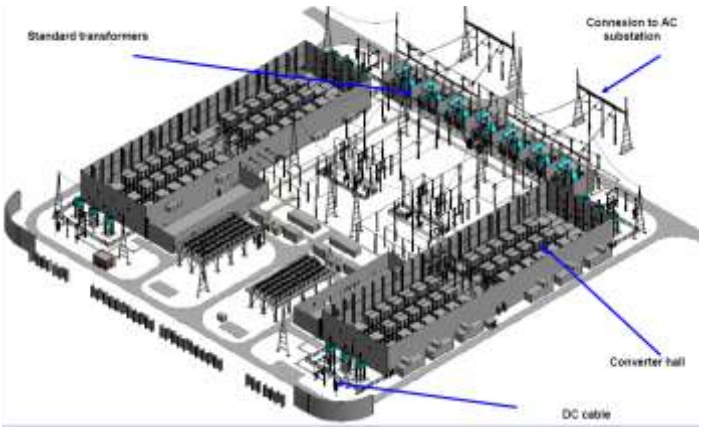


Figure I-9: Lay out of a HVDC sub-station based on MMC topology proposed by SIEMENS



Figure I-10: typical MMC tower of a phase based on IGBT and proposed by SIEMENS

In [1] is affirmed that the CSC-HVDC systems, also called "classic HVDC", can be considered as mature technologies today [14]-[18]. Advantages include their natural ability to limit the currents in fault conditions on the DC link. In the past, the inability of VSC structures to limit DC currents under fault conditions limited their adoption. Of course the CSC-HVDC connections allow the system working at higher DC voltages such as ±500 kV. This because the series connection of thyristors is well mastered. Today, for these reasons, only Ultra HVDCs are based on thyristor converters [16].

A more detailed description of the problems which the series connections of IGBTs lead is given in [18]. There are many reasons which justify the success of VSC structures. We can mention new developments in circuit breakers (CB), in control systems which are able to regulate the DC voltages not also in ordinary conditions [19]. Moreover systems which allow

the power reversibility through the changing of the current direction require a less expensive cable technology than the others [20] (CSC-HVDC systems allow the change of the power flow through the changing of the DC voltage polarity).

I.2.2 HVDC Configurations

Different configurations of HVDC systems can be determined according to the particular application and the project considered. The main configuration lay outs are shown in this section. Then the methods to regulate the power flow are described for CSC and VSC systems.

Back-to-back systems are composed of two converter stations. The conversion takes place in the main location, and these systems are not suitable for long-distance transmission. The block diagram depicted in Figure I-11 shows AC/DC conversion. This facilitates the connection between asynchronous grids. This kind of connection is also known as a unipolar system.

Unipolar systems can be employed also for submarine connections by using the ground to return current. On the other hand many problems can be led from this kind of employment [9].

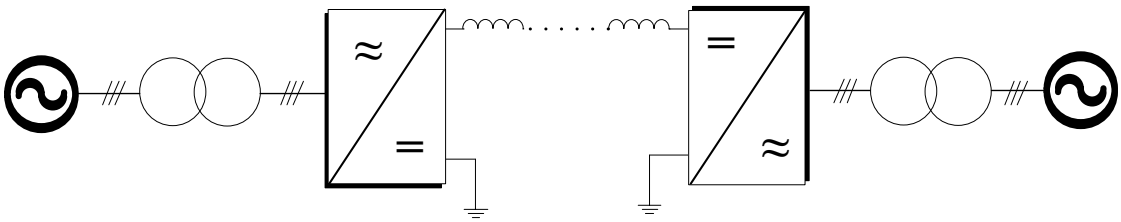


Figure I-11 – B2B HVDC system

One of the most used configurations is as shown in Figure I-12. These systems are mainly employed to transmit power in overhead lines. Also called bipolar systems, these are composed of two unipolar structures. Usually the double structure can be considered to be a redundancy. Of course if one of the two converters turns off, half part of the total power can be guaranteed on the line [9]. This structures use the ground as potential reference.

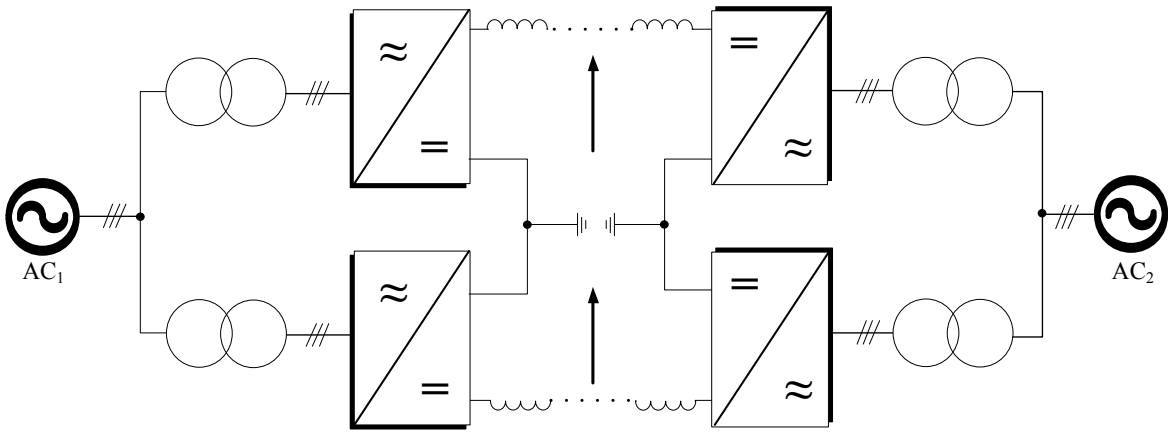


Figure I-12: Bipolar system

By connecting more than two sets of converters, it is possible to arrange multi-terminal connections Figure I-13. For the particular depicted configuration converters, if CSC based connections are considered, 1 and 3 operate as rectifiers while converter 2 can operate as inverter. By mechanically switching the connections of a given converter, other combinations can be achieved [9]. For VSC based connections the switch is not necessary due to the sign of the DC voltage is kept.

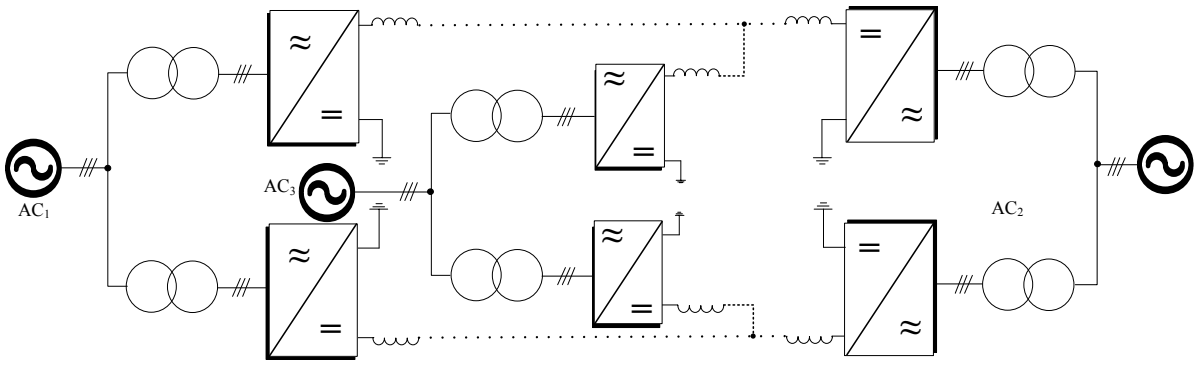


Figure I-13: Multi-terminal connection

I.2.3 Semiconductor devices for HVDC systems

Despite the huge cost of devices employed for the medium and high power applications, this kind of application covers only a much reduced part of the semiconductor total market [21] as shown in Figure I-14. The distribution and the trend of the semiconductors in power electronic field are reported in Figure I-15. The description indicates the manufacturer and places the semiconductor devices according to voltage and current rating.

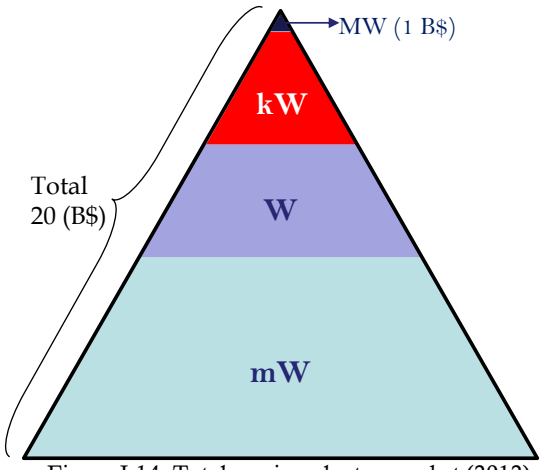


Figure I-14: Total semiconductor market (2012)

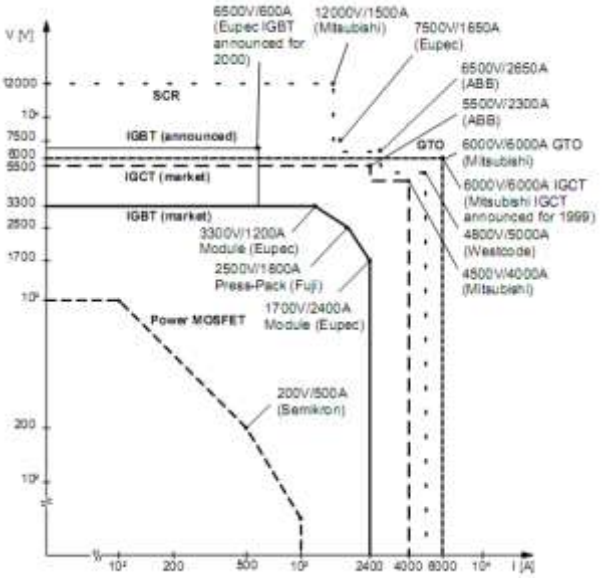


Figure I-15: Distribution and trend for semiconductor devices in power electronic field [22]

An investigation on the most used semiconductor devices was provided for the HVDC connection's field. For each device the operating range was given in terms of managed power, moreover advantages and drawbacks which decided the replacement of one respect to one another were highlighted.

In [23] is affirmed that the device manufacturers have developed different technologies for addressing the demand for an increasing reliability and lifetime. In this context, the device packaging assumes a critical role. Several manufacturers prefer power modules with bonded interconnections even though these bonding wires and solder layers are susceptible to thermo-mechanical stress and ultimately failure when subjected to power cycling. In the high power electronic, particularly in HVDC field, a consolidated packaging structure is the press contact assembly technology [24] called Press-pack (PP). This technology achieves the conduction on the power side of the semiconductor junction through pressure contact surfaces. This leads to eliminate bonding wires and solder layers; it offers an improved power cycling lifetime [23]. According to the type of device, different technologies were developed by the makers such as single wafer (Figure I-16) PP or multi-die device PP (Figure I-17).

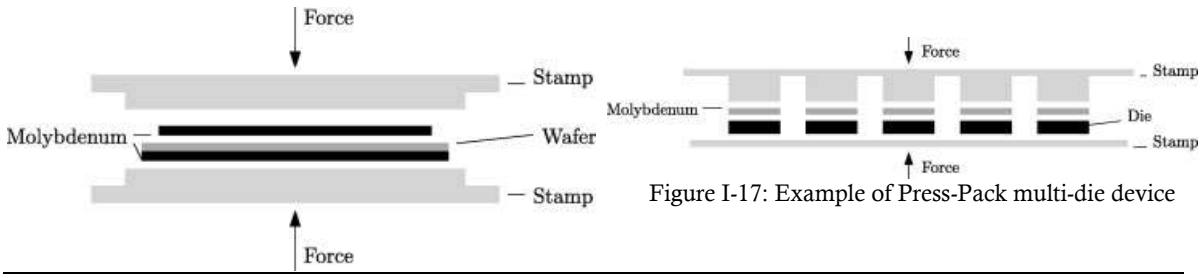


Figure I-17: Example of Press-Pack multi-die device

Figure I-16:Cross section of a press-pack single wafer (monolithic)

Typical frame assemblies are provided for the single wafer press-pack and for multi die device in Figure I-18 and Figure I-19.



Figure I-18: Press-pack single wafer tower by ABB®

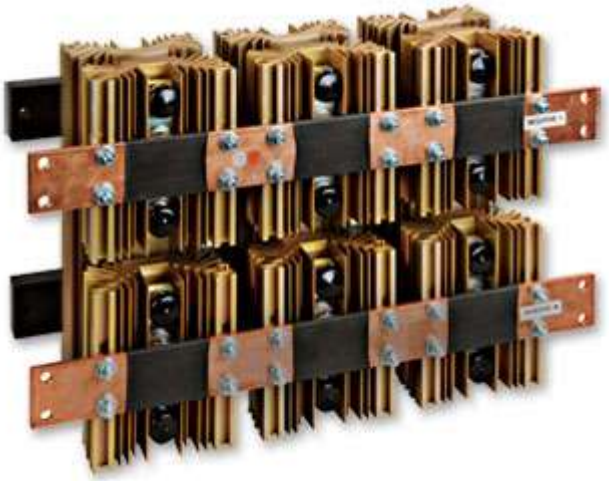


Figure I-19: Assembled Press-Pack multi-die device

I.2.3.1 Diode

For HVDC connections the fast diodes for the free-wheeling and the clamping ones are used according to the topology. The operating voltage range for the single device is about 1-10 kV. Moreover these devices can reach currents of 2-7 kA. The device is almost composed by a monolithic junction even for Press-Pack structures.

Problems due to the reverse recovery are well treated in literature especially for the free willing diodes. Unexpected problems are caused by this phenomenon such as overvoltage and HF oscillations which lead to EMI problems. The most frequent problems are the "Snappy Recovery" (Figure I-20-a) and "Reverse Recovery Dynamic Avalanche" (Figure I-20-b). The study of these phenomena were been consolidated in [26] which showed that under adverse combinations of high commutating di/dt, large circuit stray inductance, low forward current and low junction temperature, it is likely that all fast power diodes produce excessive voltage spikes due to snappy recovery.

One of the last high voltage diode technology is proposed by [26] and exhibits soft recovery performance under all operating conditions. This diode structure is capable of providing the necessary charge for soft recovery behavior by employing the new Field Charge Extraction (FCE) technology. More detailed aspects are treated in [21]-[27].

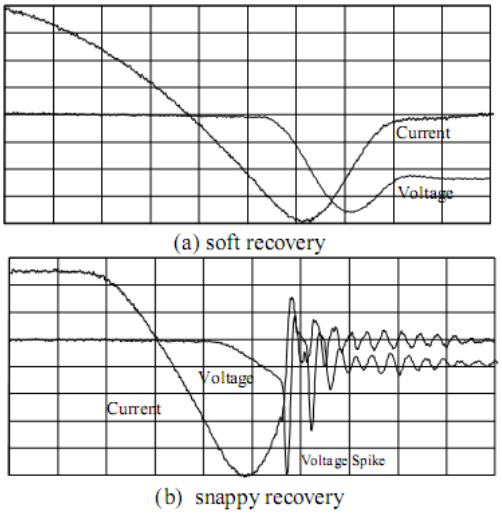


Figure I-20: Reverse recovery voltages and current in the diodes (ABB®)

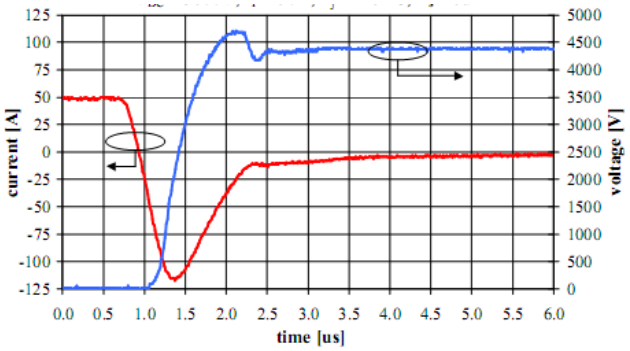


Figure I-21: Reverse recovery voltage and current in the FCE diode

This FCE diode provided a new performance for high voltage fast recovery diodes and it can be considered as the most employed in applications based on fully-controlled semiconductor devices such as VSCs.

I.2.3.2 Thyristor

These devices that can sustain voltages in the range of 10kV are matched for HVDC applications. On the market it can be found devices which can conduct current levels up to 5kA. Nevertheless, the thyristor is not a fully controllable switch. For HVDC applications, this device is usually provided in a Press-Pack single wafer structure (monolithic) (Figure I-22). Evolutions of power rating and wafer dimension versus time are reported in Figure I-23.



Figure I-22: Typical commercial thyristors (Infineon®)

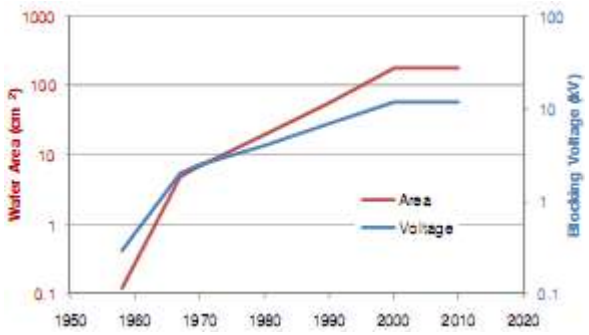


Figure I-23: The most powerful semiconductor type

Thyristors can reach very high voltage levels, they are very fast during turn-on and they don't show overvoltage problems in series connection [28]-[22].

I.2.3.3 IGBT

The Insulate Gate Bipolar Transistor was introduced in 1981 combining a MOS gate with a bipolar transistor for high voltage sustaining and simple gate driving. Actually on the market there are devices which can sustain a voltage up to 6.5 kV and switch a current up to 750 A.

This device thanks to the MOS gate can be controlled with a small power level. Moreover the MOS structure, distributed over the entire chip, allows full area conduction of the bipolar transistor.. For high high voltage and high current applications modules are based on multi-chip substrates (Figure I-24). The bi-directionality in current is guaranteed by the reverse diode which is included in the structure. An example of multi-chip packaging is given in Figure I-25. In many cases the fault of this component due to over-current makes the device always opened, which leads to an explosion [29]. For series connection of these devices, an external mechanical switch or a semiconductor device are always added to by-pass the broken device [30].

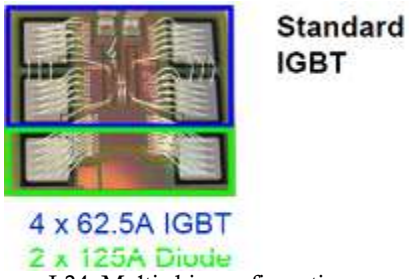


Figure I-24: Multi chip configuration proposed by ABB



Figure I-25: External package proposed by ABB for a multi chip configuration

For HVDC applications also the Press-Pack could be adopted. Nevertheless, as discussed in [23] the single wafer construction cannot be directly transferred to the manufacturing of IGBTs. Indeed, it is still not feasible to produce a large IGBT wafer for high power applications due to the fine pattern of the IGBT cell structure. To overcome this technological limitation, the press-pack housing for IGBT was developed as a multi-die device. Nowadays two Press Pack technologies can be found on the market [22], [31].

- Direct Pressure

Proposed by Toshiba and Westcode, the system consists of several chip stacks each composed of an IGBT die, supporting molybdenum disks and a chip frame to align these disks. The external lids are also achieved with multi-blocks (stamps) transferring the external force to the individual IGBT stacks [22].

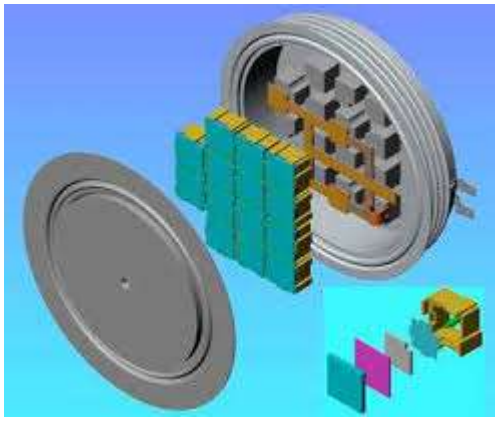


Figure I-26: 3D lay out of a Direct pressure IGBT (Westcode)

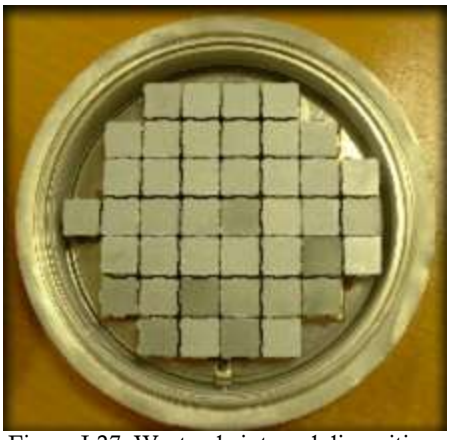


Figure I-27: Westcode internal disposition of a IGBT

In [23] it was proved that the press-pack package shows excellent performances in terms of reliability and thermo mechanical-behaviors. On the other hand, according to the structure lay-out shown in Figure I-28, the direct transmission of the pressure to the single chip requires a calibration of the strength with high resolution due to the fragile structure of the single chip. Moreover an unbalanced distribution of the pressure among the chips directly decreases the reliability.

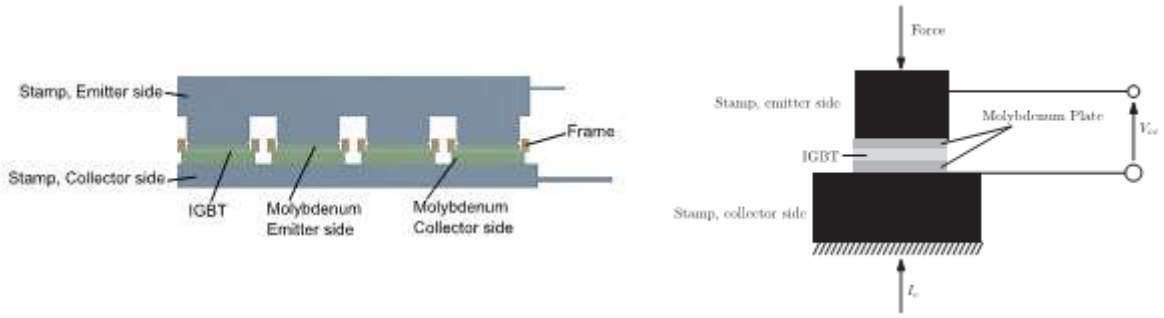


Figure I-28: Lay out of the IGBT in the frame

- Indirect pressure

This technology was introduced by ABB that is the only maker, the structure is also called Press Pack Indirect (PPI). As reported in [32] - [33] a module consists of a number of parallel connected subassemblies, called "sub-modules" inside a rigid frame. As reported in Figure I-29, when the module is mechanically clamped, each of the press-pins is subject to a force $F=c\Delta x$, where c is the spring constant and Δx is the travel distance. The surplus force, exceeding the sum of all forces on the chips, is sustained by the rigid frame. In this way, the difference in the force on the chips no longer depends on the pressure homogeneity in the stack, but only on internal tolerances of spring constant and travel distance, which can be accurately controlled.Thus, even long stacks, with their inherent problem of having

inhomogeneous pressure distribution across the PPI, become easy to assemble. In Figure I-30 a typical press-pack made by ABB and a tower of series connected IGBSs are reported.

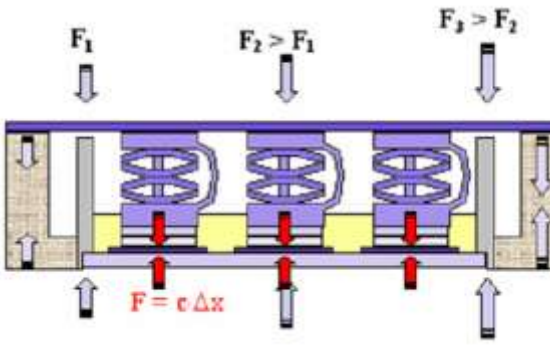


Figure I-29: Three IGBT chips with an individual press-pin each

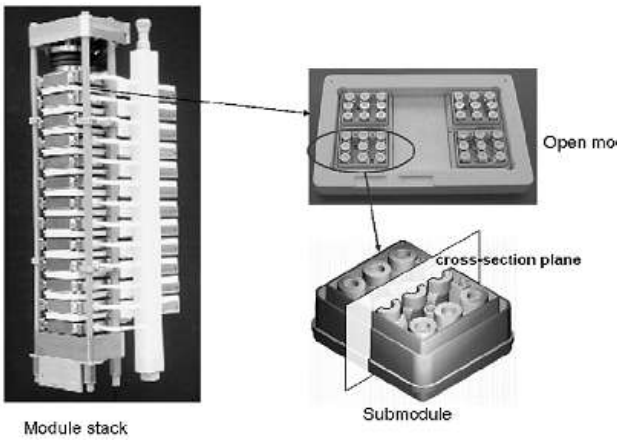


Figure I-30: Pictures of a module stack, an open individual module, and a sub-module inside the module

It' is well known that the Press-Pack IGBT modules proposed by ABB have a good resistance to the thermal cycling and allow a stable short circuit in fault conditions [34].

The indirect pressure of the construction presents better performances in case of high number of series connected devices. The homogeneous pressure distribution guarantees improvements in terms of thermal behaviors and gives to the structure a good robustness toward the vibrations. The modular structure leads to a good efficiency in terms of industrial production.

I.2.3.4 IGCT

The Integrated Gate-Commutated Thyristor is exclusively used for very high power applications such as medium voltage drives or wind turbine converters in the multi-megawatt range. These devices can turn-off up to 6 kA under 4.5 kV. In the future, this device could be the best candidate for HVDC systems based on VSCs. In the world-wide, there are only three production sites which are located in Japan (Mitsubishi), in Switzerland (ABB) and in Czec Republic (ABB). The IGCT presents a Monolithic structure (Figure I-31) always in press pack packaging as shown in Figure I-32.



Figure I-31: 4" IGCT (5.5 kA/4.5 kV) (ABB)



Figure I-32: 6" IGBT wafer

As reported in [35] in the conducting state, an IGCT is a regenerative thyristor switch like a SCR or a GTO as illustrated in Figure I-33. In the blocking state, the gate cathode junction is reverse-biased and is effectively "out of operation" so the resultant device is that of Figure I-34.

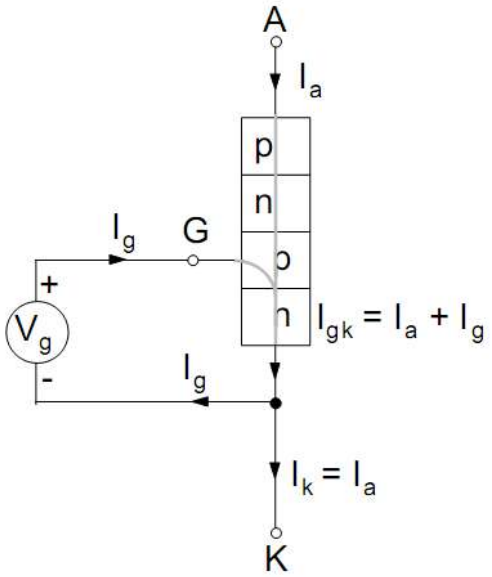


Figure I-33: Lay out in conduction mode for the IGCT

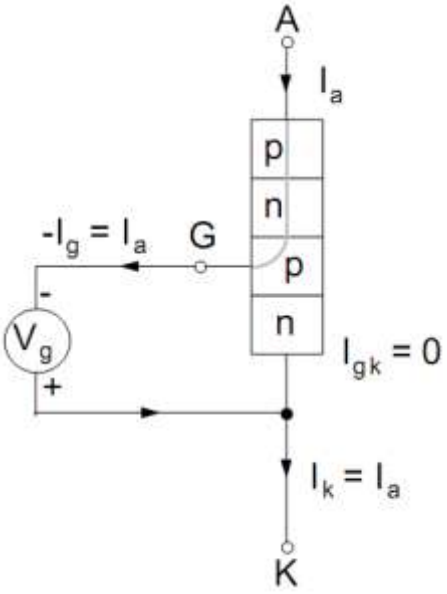


Figure I-34: Lay out of the IGCT in blocking mode

Figure I-33 and Figure I-34 also represent the conducting and blocking states of GTOs with one major difference, namely that the IGCT can transit from a state to other one instantaneously [35]. A typical turn off phase for an IGCT device is shown in Figure I-35. . The IGCT technology allows eliminating the GTO zone [28] so the device becomes a transistor prior having to sustain any blocking voltage. Because turn-off occurs after the device has become a transistor, no external dv/dt limitation is required and the IGCT may operate without snubber as does a MOSFET or an IGBT [35].

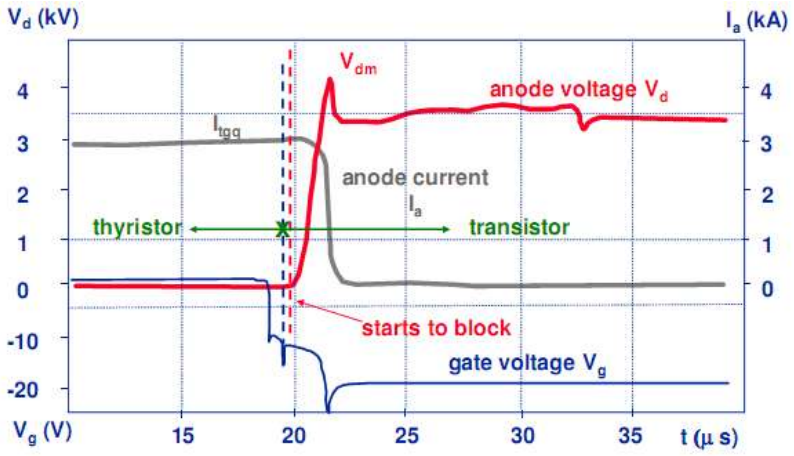


Figure I-35: Typical currents and voltages for a IGCT in turn off mode

More detailed aspect in terms of devices presents on the market and their dimension, operative voltage and current are highlighted in [35].

Of course at the moment of its introduction the IGCT required a more complicated production costs. Actually the IGCT can be considered very simple because of the development of the makers. This device is affirmed on the market also for its availability because there are not many things that fail its [35]. Moreover about its junction aspects the IGCT is not sensitive to dv/dt and di/dt problems [35].

I.2.4 CSC-Phase controlled converters

CSCs are the most affirmed structures in the field of HVDC systems [19]. The basic converter is depicted in Figure I-36, this is a classical 6-pulse topology.

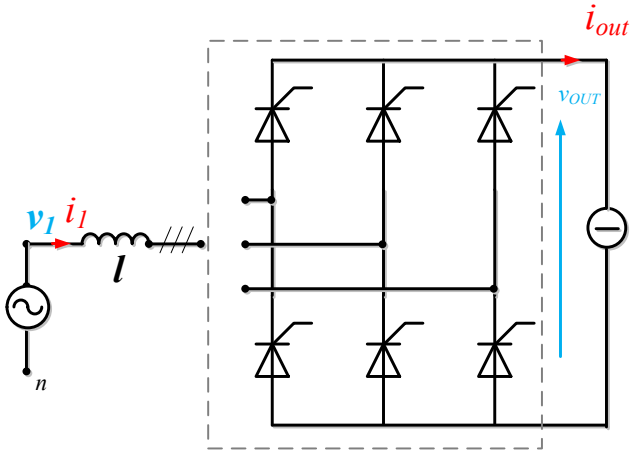


Figure I-36: Rectifier bridge based on phase-controlled thyristors

Typical voltage waveforms are presented in Figure I-37. The DC waveform depends on the line-to-line AC voltages. The average value on the DC voltage (2) can be fixed by controlling the turn-on angle of the semiconductor devices respect to the line-to-line voltage.

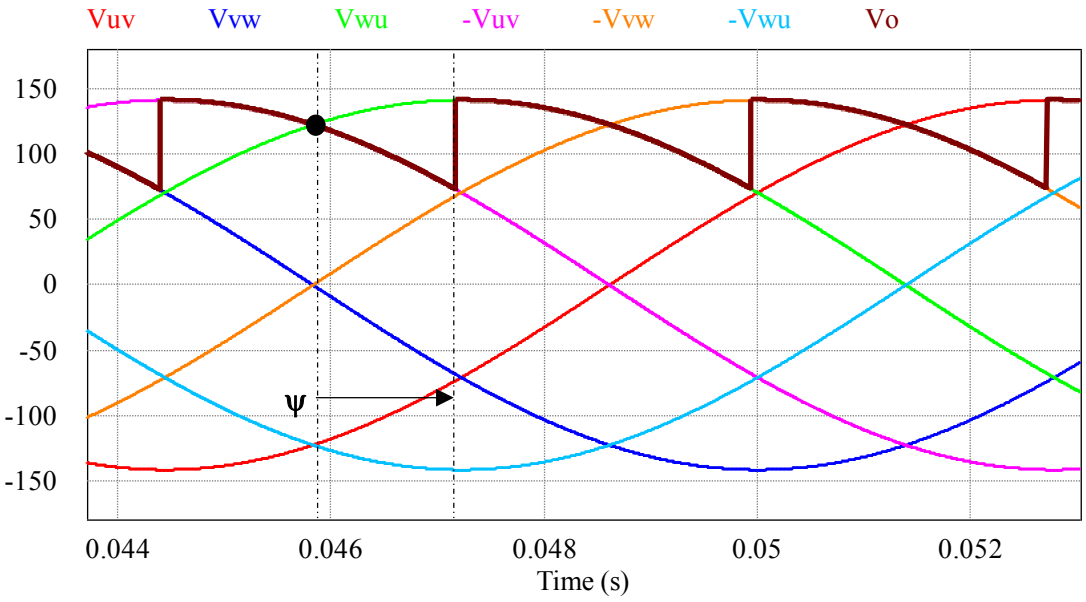


Figure I-37: Line to line voltage waveforms for the 6-pulse converter

The relationship between the turn-on angle and the amplitude of the DC voltage imposed by this system is described in Figure I-38.

$$v_1 = V\sqrt{2}.\sin(\omega_0 t) \qquad (1)$$

$$< V_{OUT1} >= \frac{3}{\pi} V\sqrt{6}.\cos\psi \qquad (2)$$

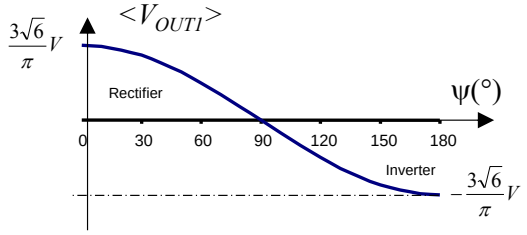


Figure I-38: DC voltage regulation according to the phase angle

The turn-on angle ψ determines also the phase between the current and the line-neutral voltage. A typical current waveform of a 6-pulse thyristor converter is depicted in Figure I-39. At high current level, the inductance on the ac-side *l* cannot be ignored. In fact for a given angle ψ, the current commutation takes a significant commutation interval δ which influences also the maximum negative limit on the DC voltage [36].

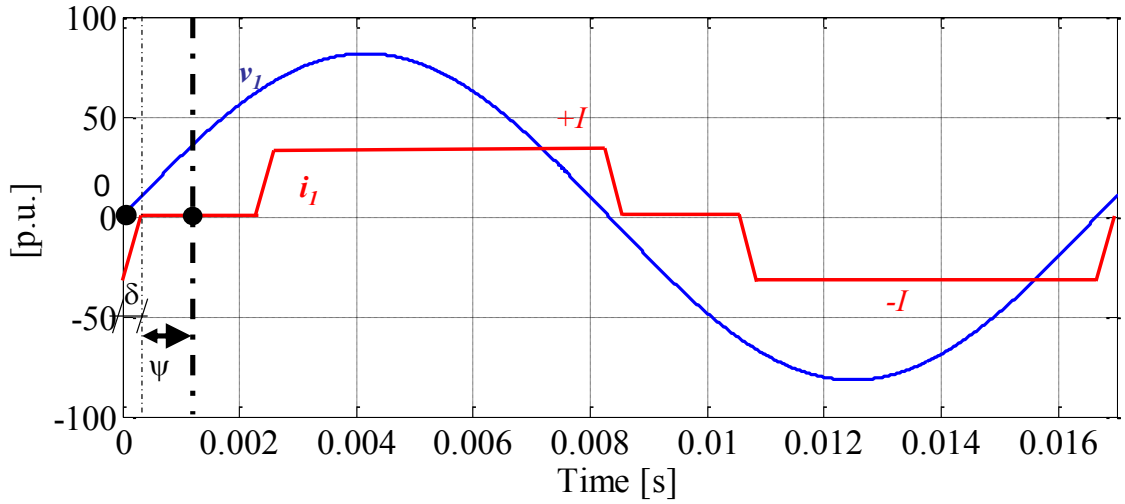


Figure I-39: Typical input current waveform for a 6-pulse rectifier compared with the AC phase voltage

The AC current waveform can be decomposed in a Fourier series (3). The fundamental component shows a phase shift respect to the phase voltage. This means that the regulation of the DC voltage determines the active (4) and reactive power (5) transmission.

$$i_1 = \frac{2\sqrt{3}}{\pi} I.\left[sin(\omega.t - \psi) + \sum_{h=1}^{\infty} \frac{1}{6h \pm 1}.sin[(6h \pm 1)(\omega.t - \psi)] \right] \quad (3)$$

$$P = \frac{3\sqrt{6}}{\pi} V.I.\cos\psi \quad (4) \qquad Q = \frac{3\sqrt{6}}{\pi} V.I.\sin\psi \quad (5)$$

The typical spectral content is shown in Figure I-40. Nevertheless, it is well known that the harmonic spectrum can be improved by interleaving thyristor commutations with multi-winding transformers to achieve 12-pulse or 24-pulse rectifiers [36]-[37].

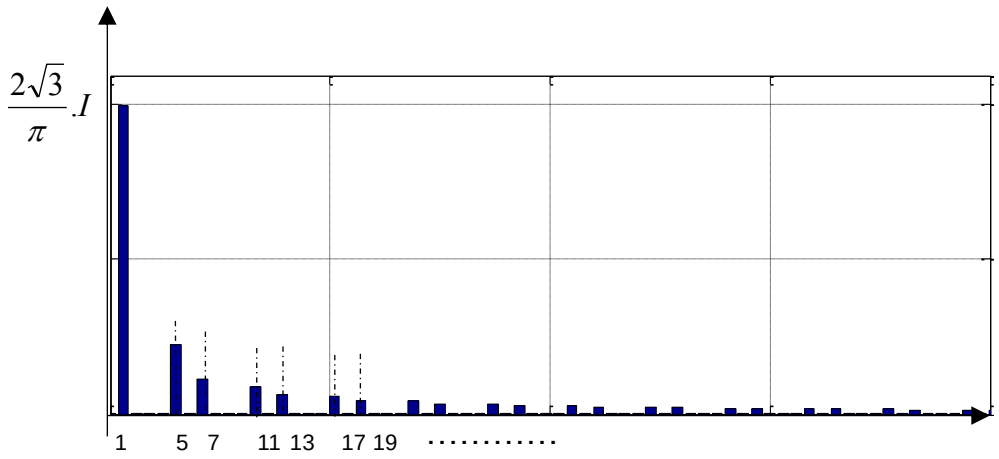


Figure I-40: Harmonic content for a 6 pulse thyristor rectifier

The presence of the AC line inductor limits the voltage capability of the converter depending on the line current as (6).

$$< v_{OUT} >= \frac{3}{\pi} V\sqrt{6}.\cos\psi - \frac{3}{\pi}\ell.\omega.I \tag{6}$$

The output characteristic of the converter is given in Figure I-41. The curves are marked for different values of ψ. For values ψ greater than 90°, the system works in inverter mode (4th quadrant). In this case there is an extinction time interval, t_{inv}, during which the voltage across the thyristor is negative and beyond which it becomes positive. Time interval t_{inv} should be greater than the thyristor minimum turn-off time t_q. Otherwise, the thyristor will prematurely turn-on, leading to a loss on the current control which can be destructive.

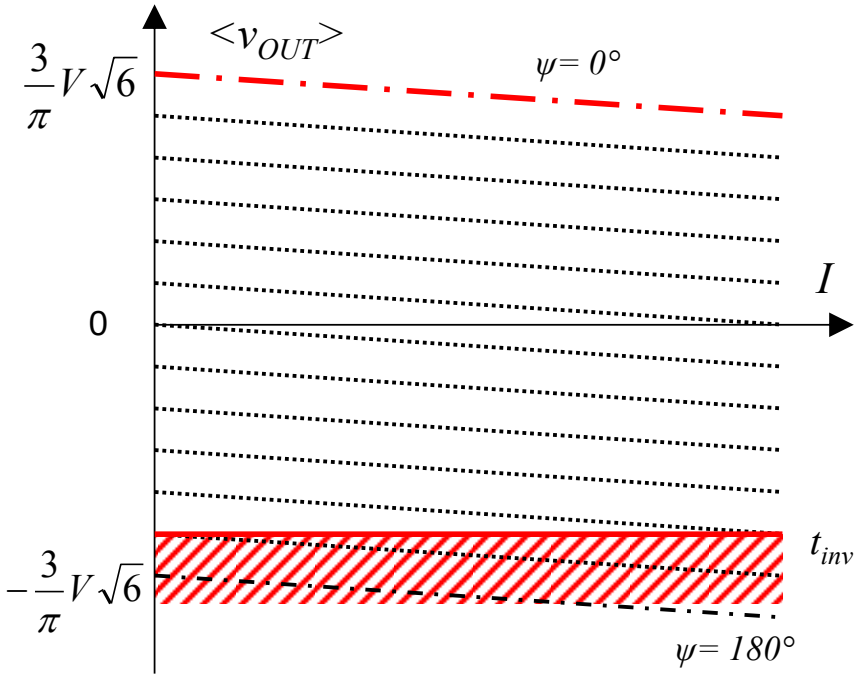


Figure I-41: DC voltage capability vs AC current

The current drawn by the power station has to be filtered by LC shunt circuits tuned on the typical frequencies of the low rank harmonics [38]. These filters take-up 20-30 % of the surface employed for the substation which is not negligible. As example, Figure I-42 shows the "field" of LC filters associated to the AC/DC converter station of the France-England connection (2 GW).



Figure I-42: LC shunt filters at « Les Madarins » converter station in France - England Interconnection

I.2.5 CSC-HVDC SYSTEMS

In this section is shown the operating principle for the converters which characterize the CSC-HVDC link. The basic connection is composed by a voltage rectifier which provides the power necessary to the transmission line through the DC current imposition. The regulation is achieved through the phase angle ψ_1.

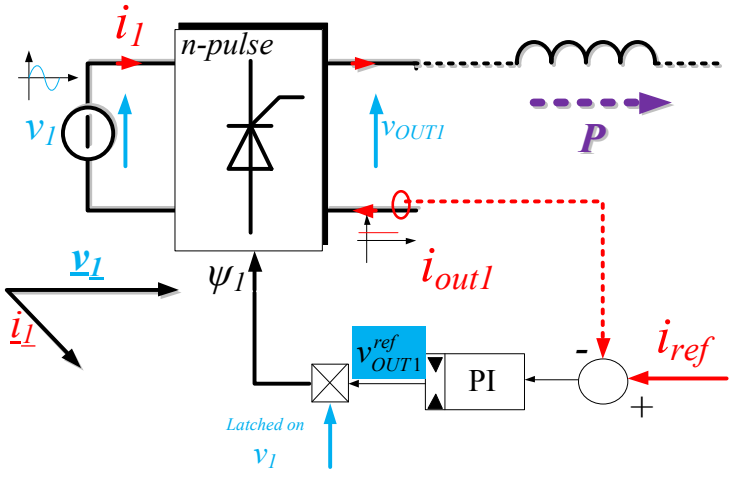


Figure I-43: Basic HVDC connection based on CSC systems

By considering the reference current the converter which is in rectifier mode works on the red characteristic in Figure I-44. The operating power diagram is shown in Figure I-45 and it is important to note that the control of the active power affects the input reactive power.

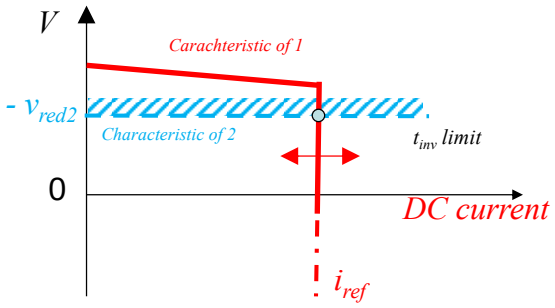


Figure I-44: I-V diagram for the two converters

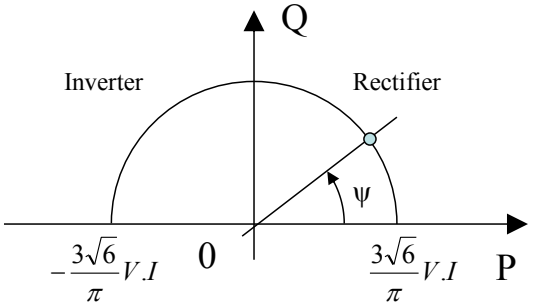


Figure I-45: PQ diagram

The converter which gets the power and works in inverter mode is depicted in Figure I-46. The converter must regulate the voltage phase angle ψ_2 to operate at the minimum turn-off time t_{inv} and then limit the reactive power received. As shown in Figure I-44, the operating point is given by the intersection of characteristics for the first converter (in red) and the receiver converter (in blue).

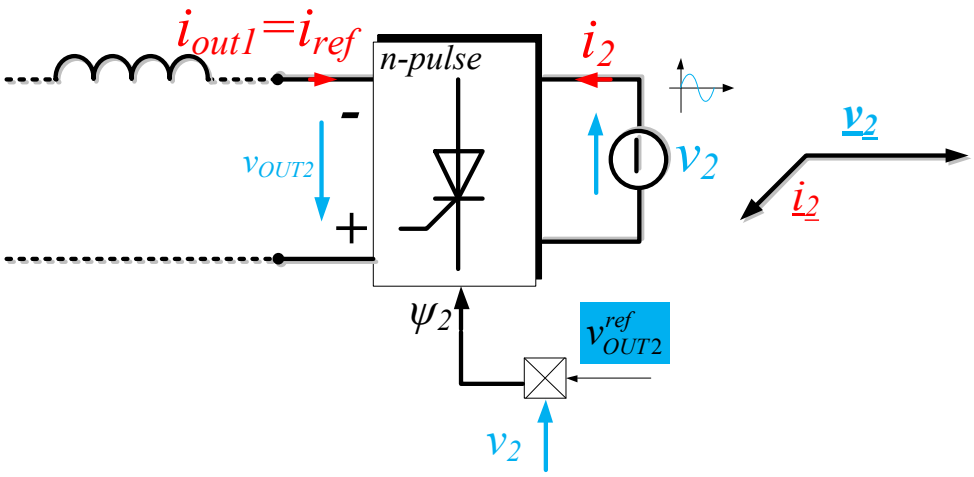


Figure I-46: thyristor converter in inverter operation

To change the direction of the power flow it is necessary that the two converters switch the roles. This means an inversion of the DC voltage polarities.

I.2.6 VSC-PWM based AC/DC converters

In this section, after a brief review on the VSC SPWM converters the principles of the HVDC transmission are explained. The so-called Voltage Source Converter based on the Sinusoidal Pulse Width Modulation allows the AC/DC conversion (and vice-versa) by regulating the active and the reactive power independently. The basic structure for the

conversion is shown in Figure I-47. If the AC voltage is imposed the power flow is regulated via duty cycle α which determines the sign of the current.

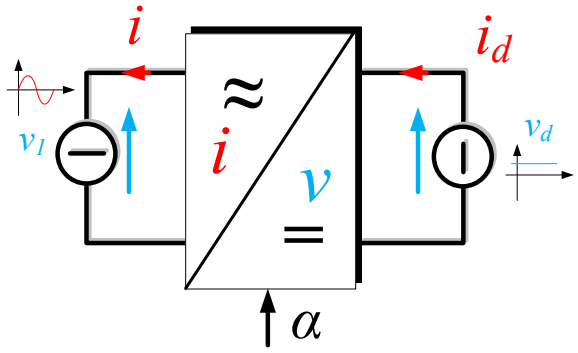


Figure I-47: basic structure for the AC/DC conversion based on VSC systems

The basic control diagram for a 3-phase VSC is depicted in Figure I-48. A generator synchronized on the grid voltage v_s determines the AC current reference which is composed by active and reactive components. The duty cycle α determines the voltage v_r which draw the desired AC current via inductor L [39].

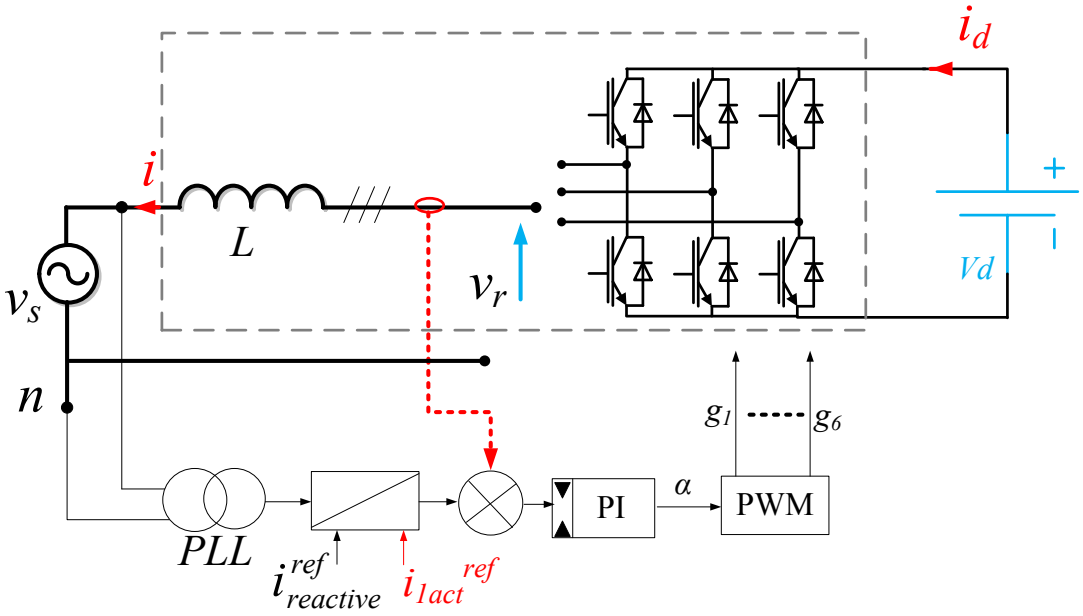


Figure I-48: Diagram of the control for a VSC PWM converter

According to the duty cycle variation the pulse width modulation is determined as shown in Figure I-49. The phase voltage waveform imposed by the three phase converter on the AC side reaches values between $-2/3V_d$ and $+2/3V_d$ [37]. The fundamental component can reach maximum amplitude equal to $V_d/2$.

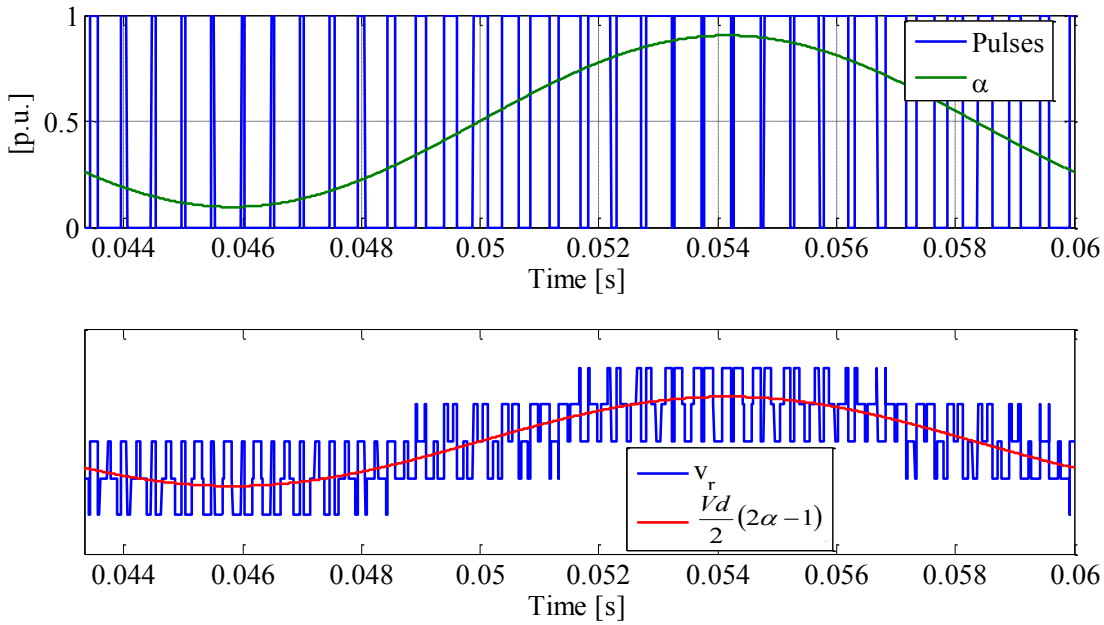


Figure I-49: switch pulses and duty cycle; phase voltage imposed by the converter and its fundamental component waveform

Inductor L determines the current waveform according to the single phase equivalent circuit in Figure I-50.

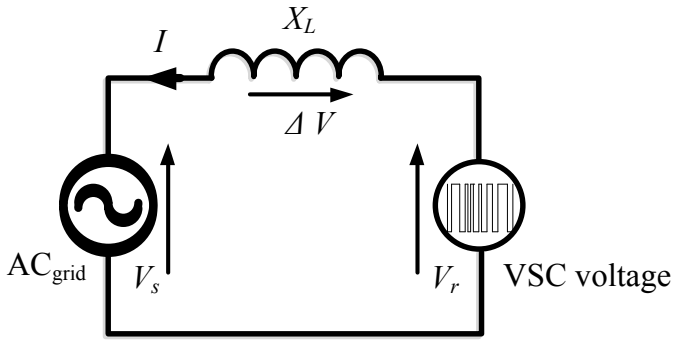


Figure I-50: Single phase Equivalent circuit VSC-HVDC connection

Amplitude and phase φ of the current depends on the active and reactive powers provided to the grid. (Figure I-51).

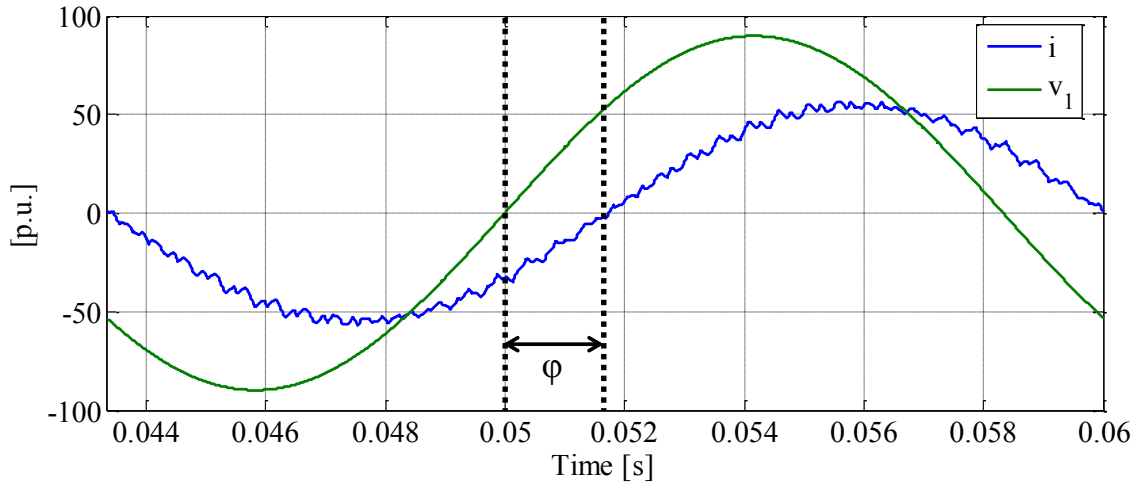


Figure I-51: AC current and grid voltage

As it is shown in Figure I-52, the line current waveform shows a spectrum which has inter-harmonics centered on the multiple of the switching frequency [40] *h* is the ratio between switching frequency and fundamental frequency).

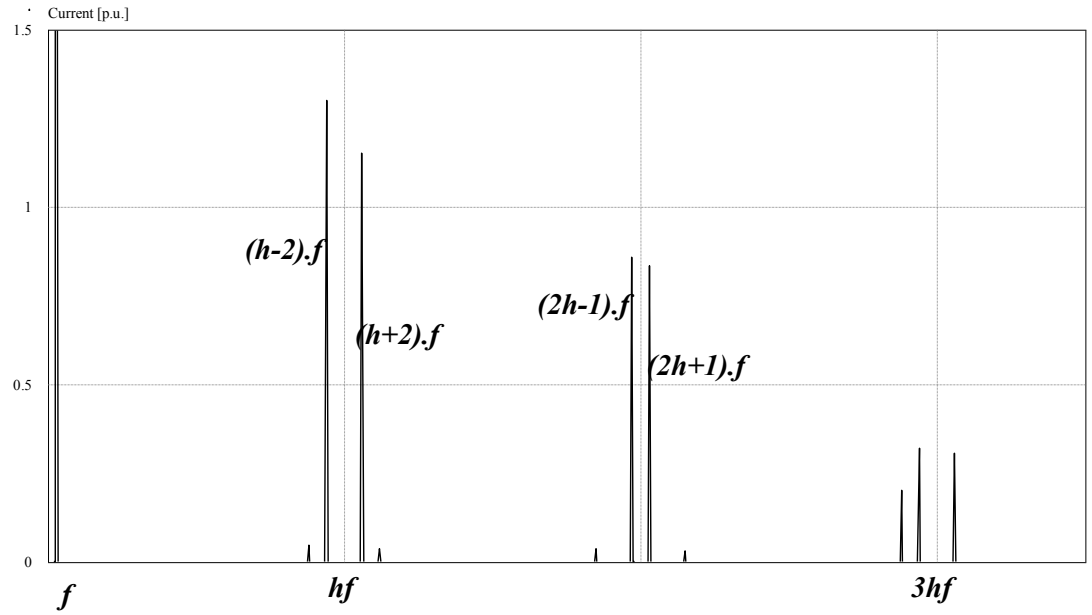


Figure I-52: AC current harmonic spectrum for a PWM VSC structure

Due to the unidirectional DC voltage, the direction of the power flow regulated on the AC side leads on the DC side to a change on the sign of the current averaged value. An example of positive averaged value of the DC current is shown in Figure I-53. Each converter imposes the desired DC voltage through the averaged value of the DC current.

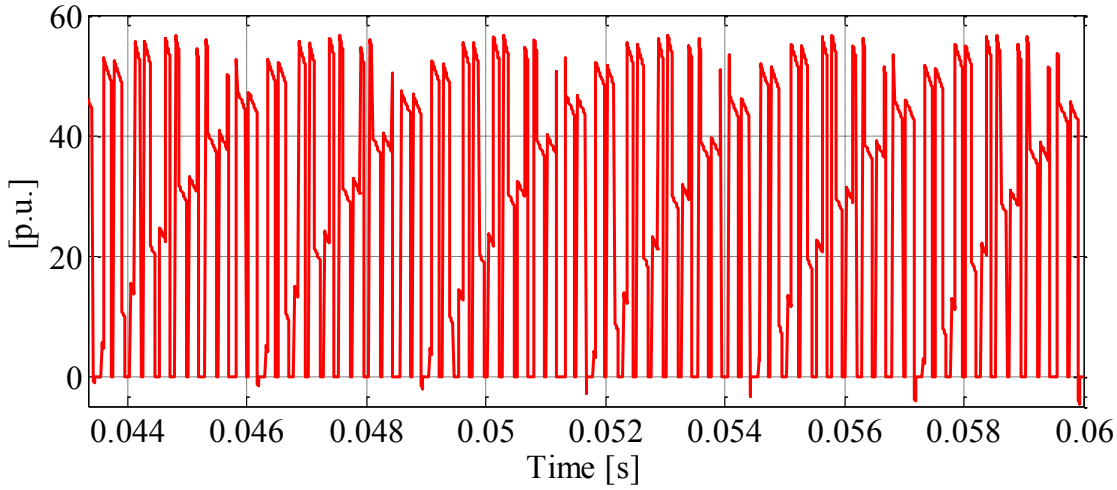


Figure I-53: i_d current

Regarding the single phase equivalent circuit at the fundamental frequency (Figure I-50), the corresponding vector diagram converter is given in Figure I-54. The DC voltage determines the output voltage limit of the converter as marked on black ring while the AC current the limit (red ring) is fixed by the semiconductor devices. Then the area corresponding to the intersection of the two rings gives the operative range of the DC/AC converter. According to the references made in Figure I-50 the sign of the power flow is also determined.

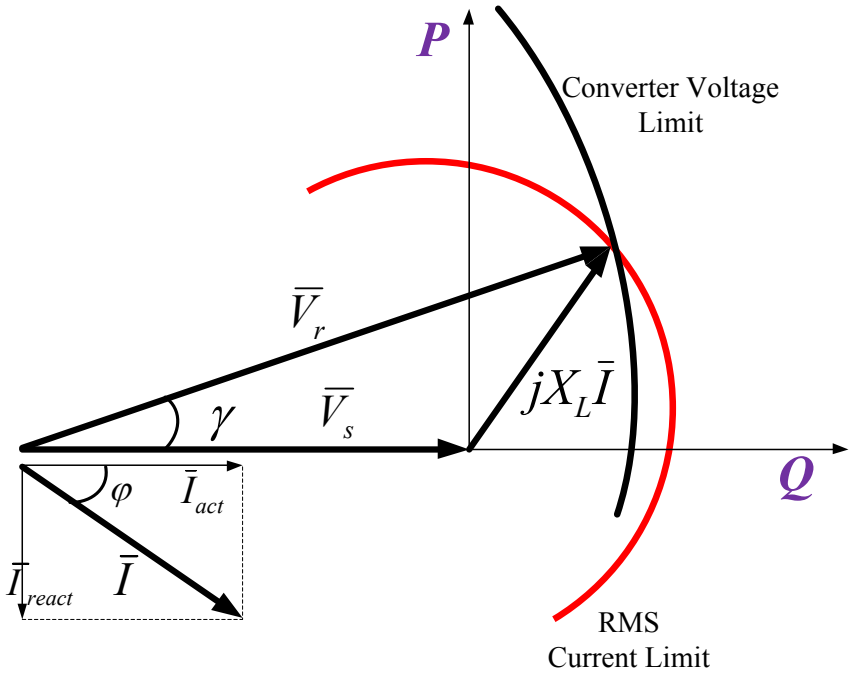


Figure I-54: Fresnel diagram for a AC/DC VSC structure

The synchronous reference frame is tuned on the voltage grid v_1. By varying the amplitude and the phase γ of V_r the vector jX_LI is placed to achieve the desired active (7) and reactive (8) power.

$$P = 3\frac{V_S V_r \sin\gamma}{X_L} \quad (7) \qquad Q = 3V_S\frac{V_r\cos\gamma - V_S}{X_L} \quad (8)$$

In the next section the principle of control to achieve the power sharing is provided for the HVDC link based on VSC structures.

I.2.7 VSC-HVDC systems

The basic lay out of a VSC-HVDC link is highlighted in Figure I-55. The approach supposes that the power is transferred from the source 1 (on the left) to the source 2 (on the right).

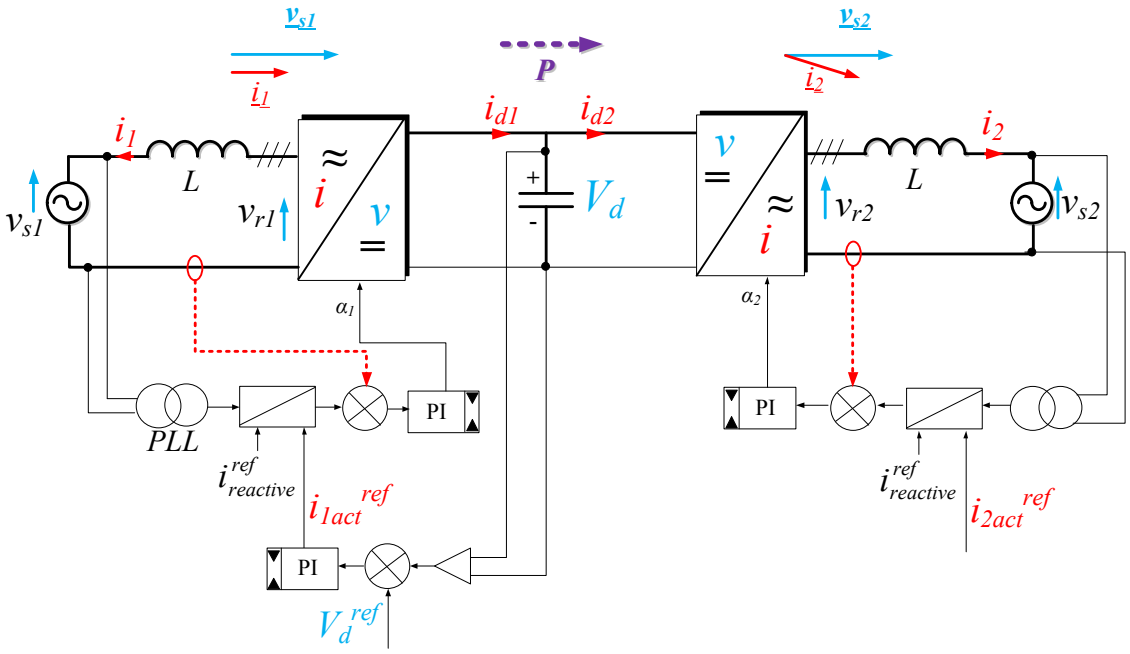


Figure I-55: simple control strategy for a VSC based HVDC connection

The two terminals share the same voltage on the DC link. The receiver converter (right) draw the currents in grid2 which fixes the active power level. To balance the DC voltage, the converter 1 absorbs the required active power on grid 1. The reactive power controls on each

side are completely independent. The stability of the DC voltage is ensured by the first converter. The DC voltage control generates the reference for the active part of the current necessary to keep the required DC voltage.

According to the claims made up to this point, VSC-HVDC systems can be chosen rather than CSC-HVDC ones because of a series of factors, such as:

- Failures of the commutations due to AC network disturbances that could be avoided.
- Independent managing of the active and reactive power.
- The use of modulations such as PWM, which guarantees frequency very low harmonic distortion on the currents. The AC filter size can be greatly reduced.

That is why in the following section, multilevel VSC topologies, able to operate in high voltage applications, are considered.

I.3 VSC-HVDC multilevel topologies

Due to the limited current capability of the cables and semiconductor devices, HVDC systems require converters able to operate on around a hundred volts. In Figure I-56, the main topologies of voltage source inverters are reminded.

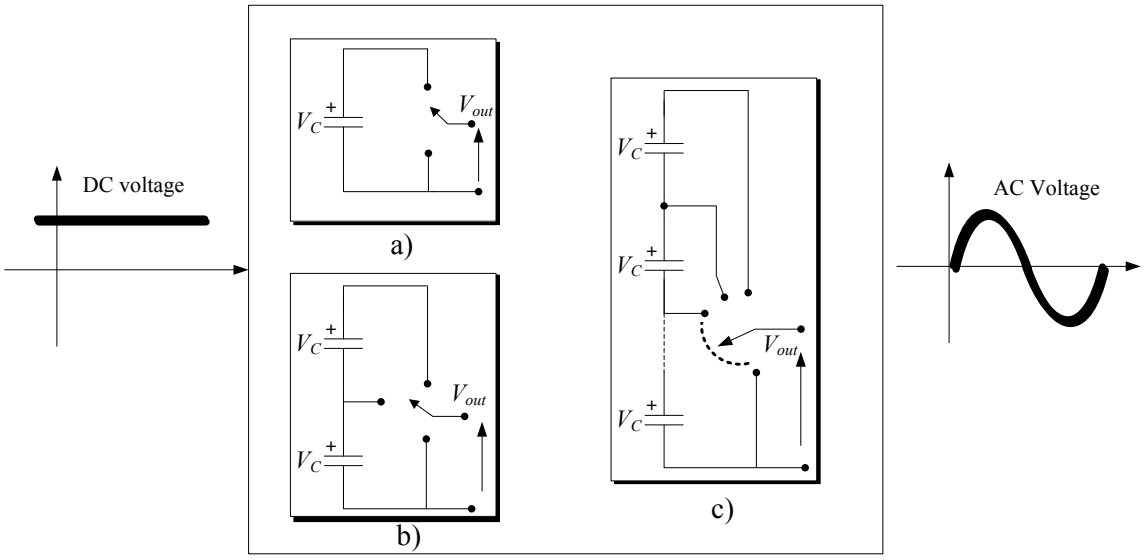


Figure I-56: Basic schema of VSC topologies for a simple one a), 2-VSI b), and a multilevel topology c)

The simplest VSC topology is the two-level, three-phase bridge [40]. If this solution is adopted, many series-connected IGBTs are used to compose one device as shown in Figure I-57. As treated previously there is just one manufacturer available on the market for this solution.

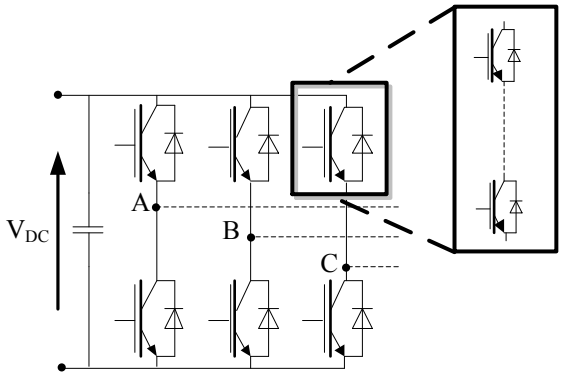


Figure I-57: VSI 2-level topology for high voltage employment

The connection of series devices leads to output voltage waveforms, which show high dv/dt, which is a main constraint for transmission line transformers. Moreover, for high-power converters, the switching frequency is very low due to power losses and the limitations of the semiconductor device. To keep the harmonic impact under the limit imposed by the standards, an AC filter is necessary.

The use of multilevel converters enables work at a high-voltage level, with a high-waveform quality. The main feature of these converters is that they draw a quasi-sinusoidal voltage waveform from several levels obtained from flying capacitors (like flying cap converters) [42] connected to each commutation cell.

In multilevel structures, due to the interleaved modulation technique, it is possible to achieve a series of advantages [42] - [43], such as:

- Quasi-sinusoidal AC voltage waveform
- Low harmonic impact
- Reduced costs for the filtering elements
- Possible direct connection to the MV grid
- Reduction of semiconductor losses due to a very low single-switching frequency per device

An overview is given in the next section on the multilevel topologies candidate to be employed for high-power transmission.

I.3.1 Neutral Point Clamped (NPC)

One of the topologies which literature started to consider is the NPC [43]. In Figure I-58, a three-level version is shown, but it is possible to add the components and place them correctly to increase the number of levels.

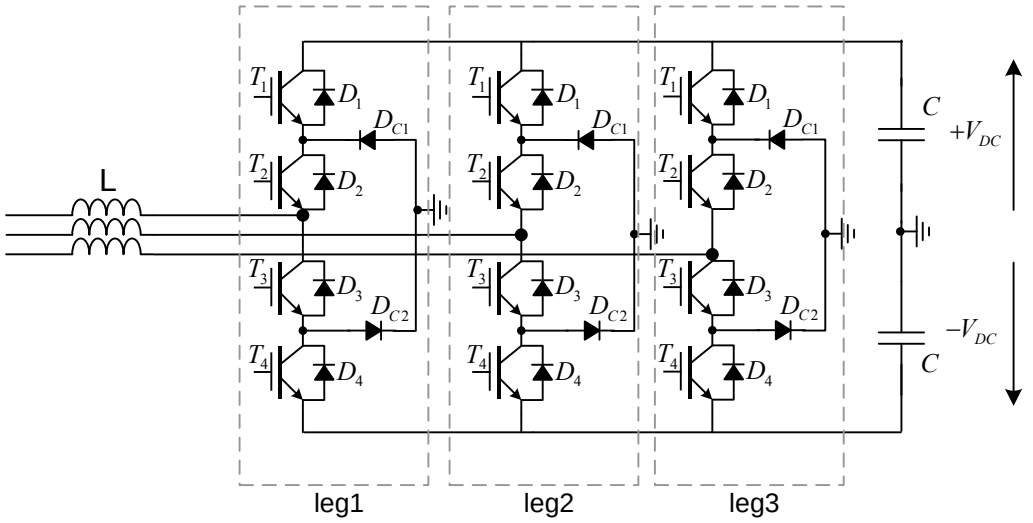


Figure I-58: Three-level three-phase NPC topology

The component which characterizes this topology is the diode necessary to clamp the switching voltage to the half level of the DC bus, which is split into three levels by two series of connected bulk capacitors. In this topology, the middle point is also called the neutral point, outlined in Figure I-58 as the ground. By increasing the number of levels, the voltage which the diodes have to sustain rises. If the voltage rating of each diode is kept, more devices are necessary for the whole voltage. For this reason, if the number of voltage levels that the system can impose is N, $(N-1)^2$ diodes are necessary. For high-DC voltages, the system becomes less convenient due to the huge number of diodes.

I.3.2 Flying capacitor

Another multilevel topology which is suitable for high-power applications is the Flying Capacitor structure with N imbricated cells (Figure I-59). The output inductor value is calculated to limit the output current ripple at the equivalent switching frequency. [44] The FC topology includes N-1 flying capacitors, and the operating voltage of each cell is V_d/N [44]. One drawback of this topology is the stored energy in the flying capacitors close to the DC bus (voltage and energy increase with index i). However, it is possible to connect capacitors in the series to sustain high voltage, but it is not certain that the voltage will be equally shared between them.

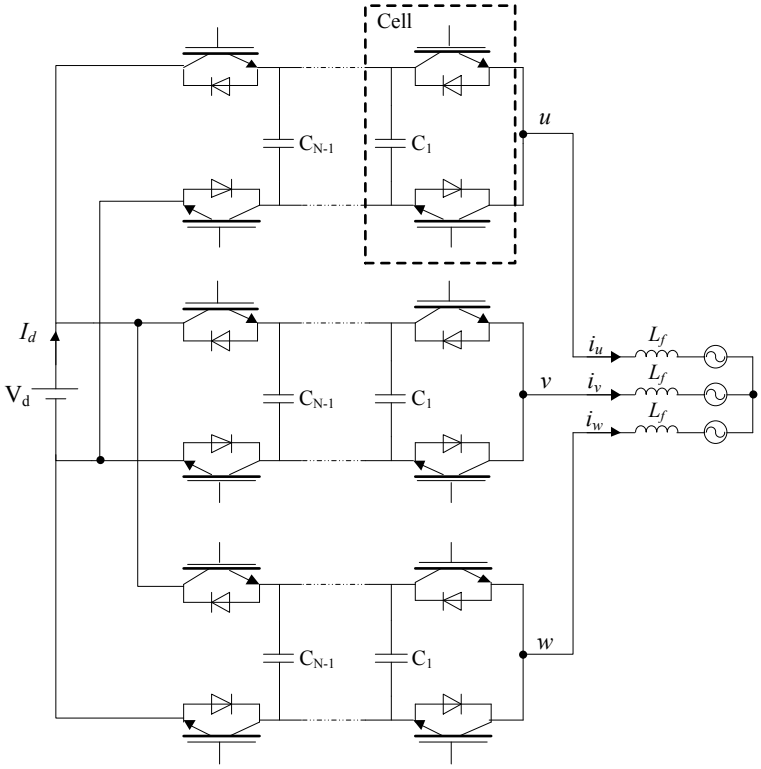


Figure I-59: Three-phase flying capacitor converter

The two topologies analyzed present a better reduction in the harmonics. Despite the improvements which they are able to reach, these kinds of multilevel converters present a series of limitations/drawbacks. For this reason, they did not succeed in these HV-application demands [47].

- Not suitable for the industrial series production (thanks to the modular construction in order to enable scaling to different power and voltage levels, using the same hardware [48])
- Unwanted EMI disturbances generated by a very high slope (di/dt) of the arm currents
- The DC bulk capacitor stores a huge quantity of energy which leads to damages under faulty conditions
- The stored energy of the concentrated DC capacitor at the DC-Bus results in extremely high surge currents and subsequent damage if short circuits at the DC-Bus cannot be excluded
- Harmonics on the AC current must always be suppressed

I.3.3 Cascaded Multilevel Inverters

These structures are characterized by a series connection of elementary converters that are normally identical, as shown in Figure I-60. Each cell corresponds to a voltage level. According to the particular modulation technique, it is possible to achieve the desired voltage waveform according to the imposed reference (Figure I-61).

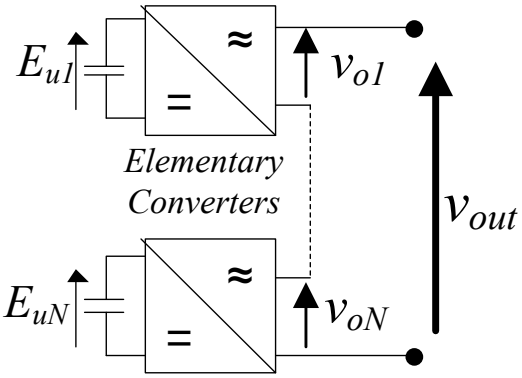


Figure I-60: Cascaded multilevel stage

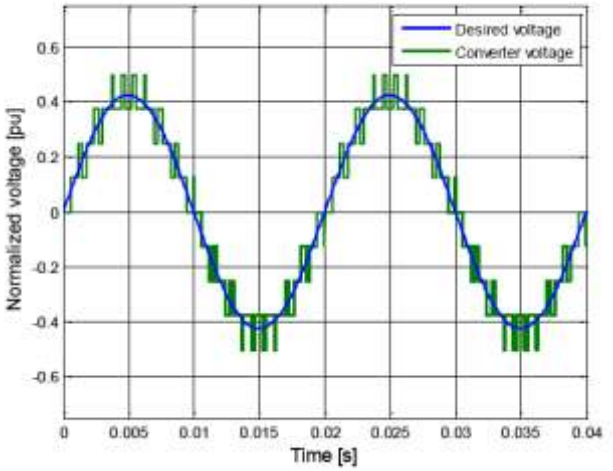


Figure I-61: Example of multilevel waveform

With respect to the traditional topologies, cascaded structures ensure the modularity of the system by ensuring series industrial production. Due to the modularity, they do not present upper-DC voltage limits. In fact, it is possible to add more series cells to sustain the desired voltage.

A topology which has been affirmed in the last decade is the Modular Multilevel Converter. This structure is more and more often chosen for VSC-HVDC power stations [45].

The converter is a composition of series-connected elementary cells (Figure I-62). This converter offers the possibility to regulate the active and reactive power independently. Each phase is composed by two groups of elementary cells (1..N and N+1…2N), called branches. Each branch conducts the half-phase current. As affirmed in [47], "At first glance, when being compared to conventional VSC or multilevel VSC, the new topology offers several features which may seem strange or definitely wrong". Thanks to a series of advantages listed above, the next chapter pays attention to the main topology and sizing aspects for this structure:

- Each arm conducts half current and in continuous conduction mode
- Arm inductances contribute to limit faulty conditions
- The bulk capacitor is not necessary because there are two terminal cells
- Each capacitor cell voltage can be controlled very slowly with respect to the current regulator
- The DC link voltage can be controlled by the converter

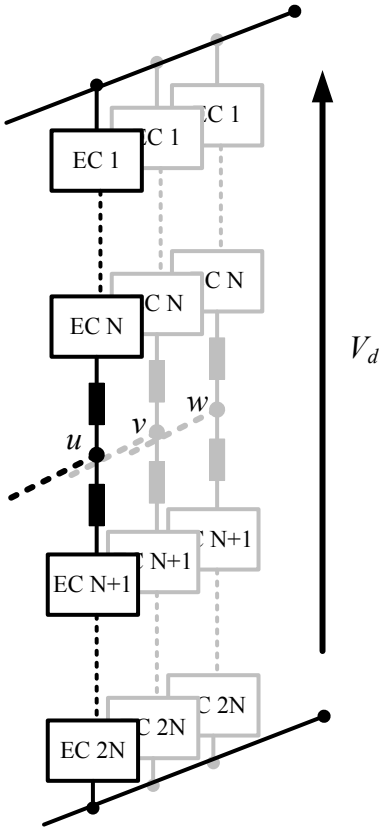


Figure I-62 : Modular Multilevel Converter base schema

I.4 Conclusions

The development of semiconductor turn-off devices and the success of the multilevel topologies in recent years have made VSC-HVDC structures the most employed in HVDC systems.

CSC structures can manage high voltages because are composed by thyristor rectifiers. This device does not suffer the series connection. On the other hand, VSC structures can control the active and reactive power independently. Moreover the SPWM based structures make the filtering stage very small respect to the CSC. VSC structures allow also islanded operation.

Compared to the traditional multilevel structures, Cascaded multilevel converters, due to their modularity, are matched to series industrial production. Moreover they do not present upper-DC voltage limits. In fact, it is possible to add more series cells to sustain the desired voltage.

Chapter II. **MMC systems**

In the first part of this chapter a macro model is provided for the MMC structure. The so-called averaged model facilitates considerations and investigations without taking into account the effects of the harmonics at the switching frequency, making the study fast and direct. Sizing parameters are provided for the reactive elements (branch inductors and cell capacitors) for two different approaches. A first approach supposes a current control, which acts directly on the AC output current (one current control per phase). Under this condition, a new configuration is also proposed for the branch inductor in order to improve the system performances. The second approach proposes two current loops per phase, each of which acts on the current of each inductor. For both approaches, simulations are performed to validate the study.

The considered structure in the work is depicted in Figure II-1. Each phase of the system is composed by two branches. Each branch is a connected series of N elementary cells (EC) and the branch inductor L. Each phase contains 2N elementary cells. At the top are the negative branches (n), and at the bottom are the positive ones (p).

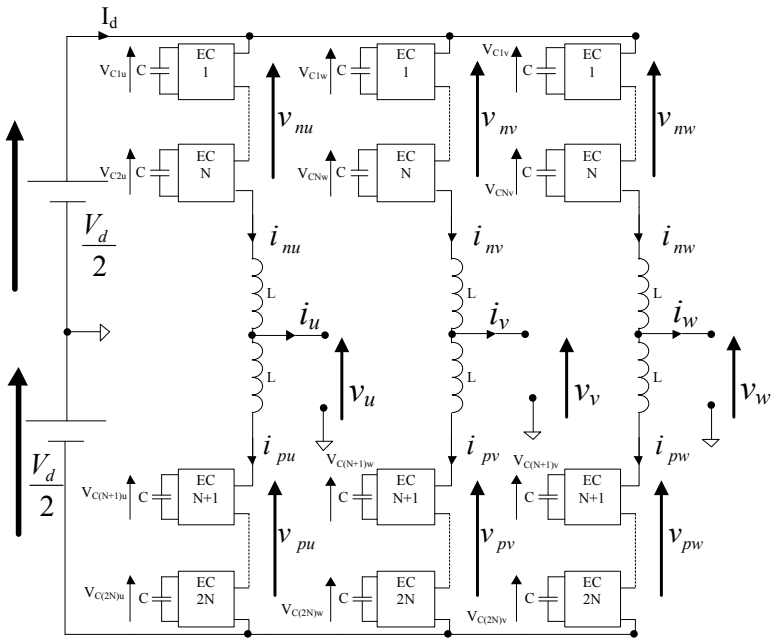


Figure II-1: Modular Multilevel Converter in three-phase configuration

II.1 The Macro Model

To make preliminary considerations and gain an easier understanding of the system, a model at low frequency was extracted. A Sinusoidal Pulse Width Modulation (SPWM) is assumed. This approach does not consider the switching contribution on the spectral content for the voltages and currents of the system. Moreover, this approach makes the study of the MMC structure independent from the particularly topology of the series connected elementary converters.

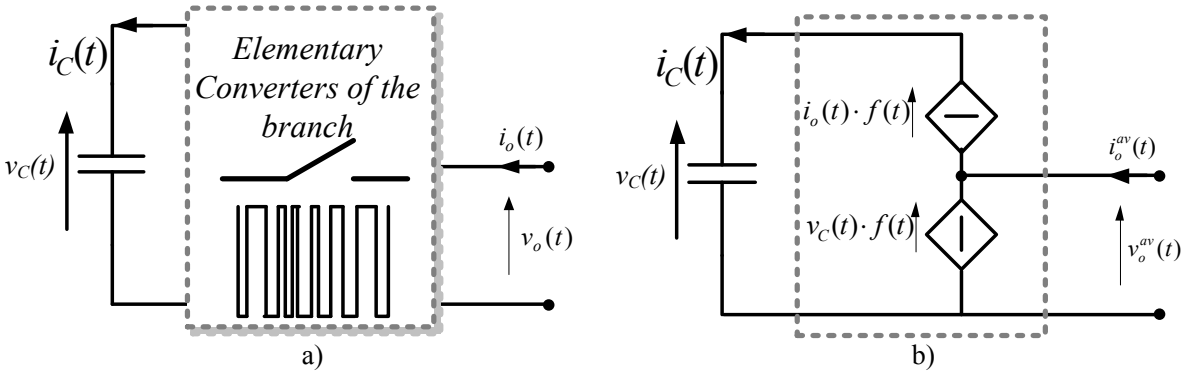


Figure II-2: Low-frequency model b) of an elementary switching cell a)

Each commutation cell can be seen as a 2-port device (Figure II-2 a)). The input side is characterized by the voltage and current for the cell capacitor. The output side carries out the voltage cell and the branch inductor. The relations between currents and voltages of the cell are at (1) and (10), respectively, where *f*(t) is the modulation function, depending on the modulation signal and the topology of the elementary converter. Thus, the averaged model of the cell is depicted in Figure II-2 b).

$$i_C(t) = i_o^{av}(t)\cdot f(t) \tag{9}$$

$$v_o(t) = v_C^{av}(t)\cdot f(t) \tag{10}$$

By starting from the diagram given in Figure II-1, it is possible to extract the equivalent averaged circuit (Figure II-3) valid for the MMC system; the equations which characterize the structure don't consider the particularly topology of the elementary converter. Moreover each capacitor resumes the total capacitance for the N converters which compose the branch. The equivalent value is C/N.

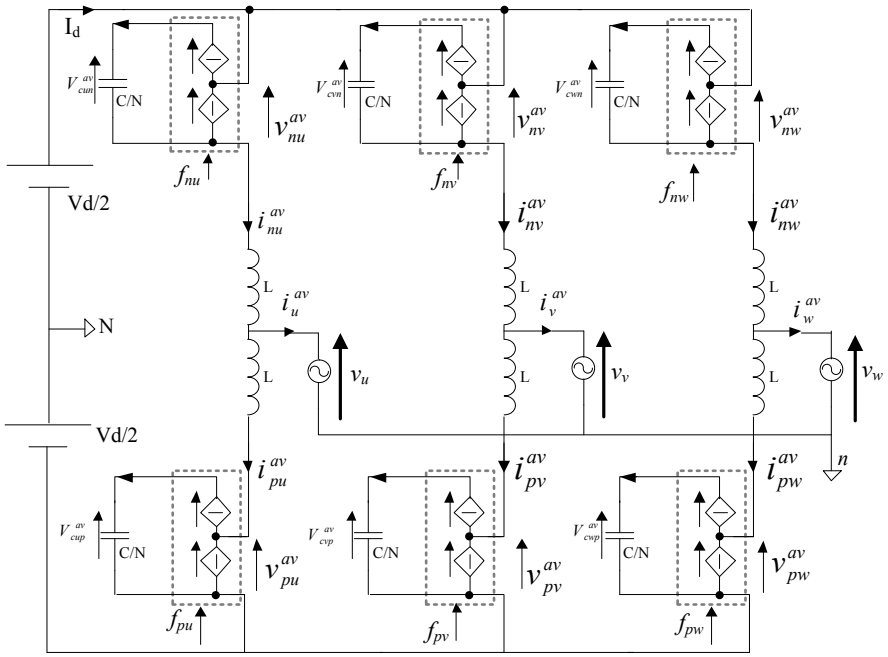


Figure II-3: Averaged model for the MMC

To make the study not-dependent from the particular topology, definitions on the nomenclature about the functions has to be given in Table II-1.

Table II-1: Elementary converters function definition

f(t)	Function which multiplied for the averaged cell gain gives the averaged voltage waveform of the cell output
k(t)	AC part of *f(t)*
α(t)	Averaged value of the switching function. (for a unipolar elementary converter f(t)=α(t); for a bipolar elementary converter α(t)=(1±f(t))/2)

All of the considerations were made just for one phase. Each branch imposes a voltage (11) which is the equivalent sum of the output voltage of each series' connected cell. Moreover each cell imposes a voltage depending on the modulation function and the voltage capacitor. By supposing the voltages on the capacitors for all the cells of the branch equal between them and the same for all the modulation functions, each branch imposes the voltage in (12) According to the diagram shown in Figure II-3, the phase voltage is achieved in by neglecting the voltage drop on the branch inductor L (13). Branch currents determine the current in the phases (14).

$$\begin{aligned} v_{nu}^{av}(t) &= \sum_{j=1}^{N} V_{ju}^{av}(t) \\ v_{pu}^{av}(t) &= \sum_{j=1}^{N} V_{ju}^{av}(t) \end{aligned} \quad ; V_{ju}^{av}(t) = f_j(t) V_{cj}^{av} \tag{11}$$

$$\begin{cases} v_{nu}^{av} = V_{Cn}^{av} \cdot f_n(t) \\ v_{pu}^{av} = V_{Cp}^{av} \cdot f_p(t) \end{cases} \tag{12}$$

$$v_u(t) = \frac{v_{pu}^{av}(t) - v_{nu}^{av}(t)}{2} \tag{13}$$

$$i_u(t) = i_{nu}(t) - i_{pu}(t) \tag{14}$$

The instantaneous and averaged voltage waveforms are compared in the next section. This facilitates better understanding of the difference between the two models.

II.1.1 Macro model validation

The typical voltages and currents of an MMC system are considered to demonstrate the reliability of the macro model. The simulation results are reported in p.u., because the particular case study is shown after the sizing considerations achieved in the next sections. The switching frequency for the single cell is 450 Hz for the instantaneous model. The voltage and currents of the instantaneous model are compared to the averaged ones. Moreover, considerations for the spectral content are achieved to show the frequency limits of the model with respect to the instantaneous one.

In Figure II-4, a typical voltage waveform of the capacitor of the elementary converter is shown. The instantaneous model seems to match well with the averaged one. This is consolidated also by the spectral content comparison in Figure II-5.

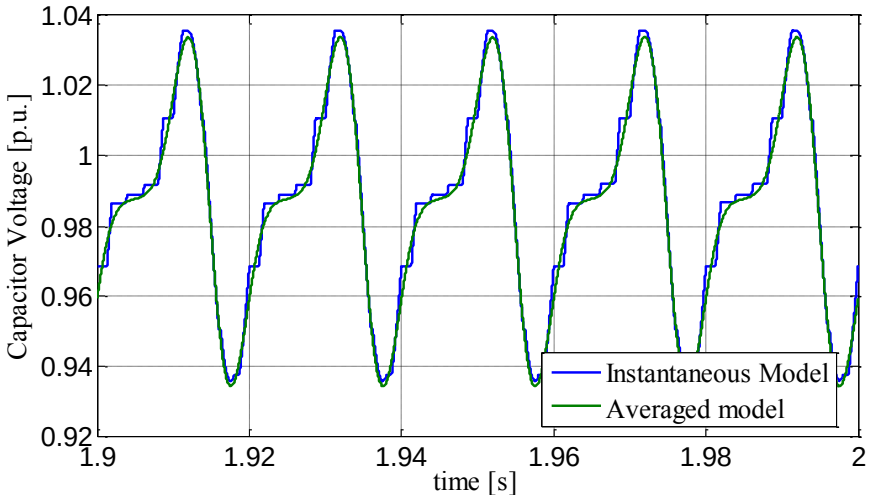


Figure II-4: Instantaneous and averaged model comparison of a voltage on a cell capacitor

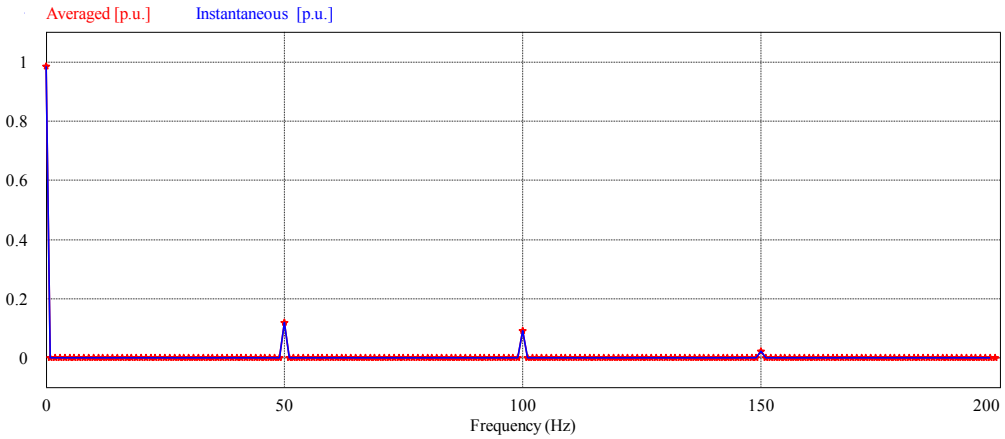


Figure II-5: Spectral content comparison of a capacitor voltage for a cell

A more evident matching between the two models is shown by considering the output voltage of the elementary cell (10) in Figure II-6. In this case, the matching between the two models is more evident in their low-frequency spectral content compared in Figure II-7. The averaged model is not able to take into account the switching frequency.

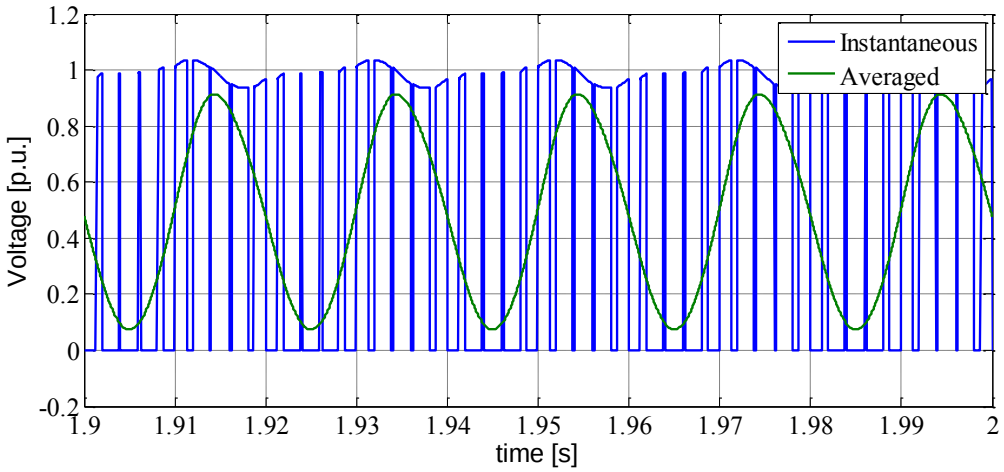


Figure II-6: output voltage imposed by an elementary cell; comparison between instantaneous model and averaged model

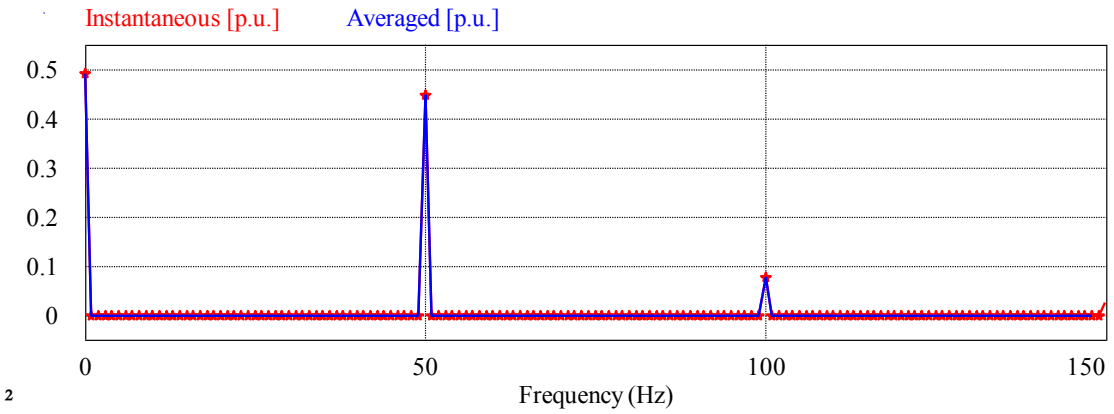


Figure II-7: Spectral content comparison for the output cell voltage

The macro model is very useful in making all preliminary considerations about the reactive element sizing and testing the control. The model implementation is very direct, and the simulations are very fast because the switching frequency is not considered for the time step choice. By now, if it is not specified, all the simulations are performed by considering the averaged model.

Before the sizing approach proposition, the elementary cell topology is defined in the next section. The single cell characterizes the MMC base structure [49] by considering a SPWM. A more detailed study on the choice of the cell topology is achieved in chapter III. In this chapter the study in given for the averaged model if the adaptation of the instantaneous one is not specified.

II.1.2 Study of the MMC basic structure

The basic version of the MMC structure is composed by single cells (Figure II-8). The modulation signal given in (15) considers ω_0 to be the fundamental frequency and $cos(\varphi)$ the power factor. Negative and positive branches have duty cycle (16) and (17), complementary between them.

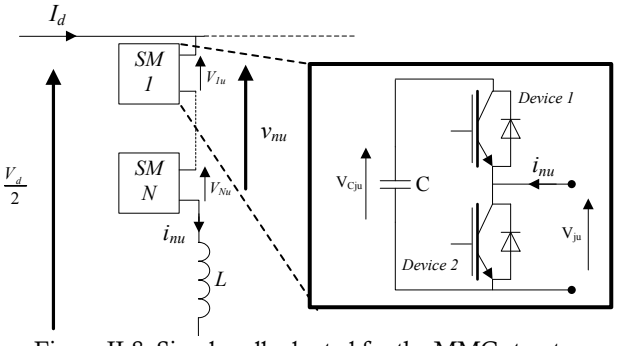


Figure II-8: Simple cell adopted for the MMC structure

$$k(t) = M\sin(\omega_0 t + \varphi)\,;\, 0 < M < 1 \quad (15)$$

$$f_n = \alpha_n = \frac{1 - k(t)}{2} \quad (16)$$

$$f_p = \alpha_p = 1 - f_n(t) \quad (17)$$

From the assumptions given for the elementary cells in (1) and (10) and based on consideration for the modulation ratio assumed for the single cell, the branch voltages and currents for the u-phase are carried out in (18) and (19), the positive part is symmetrical to the negative one. The presence of a second harmonic component is confirmed in the works [50]-[14] and is highlighted as follows.

$$\begin{cases} v_{un}(t) = \frac{1}{2}V_d\left(1 - M\sin(\omega_0 t - \varphi)\right) + \frac{V_{2f}}{2}\sin(2\omega_0 t - \varphi) \\ v_{up}(t) = \frac{1}{2}V_d\left(1 + M\sin(\omega_0 t - \varphi)\right) + \frac{V_{2f}}{2}\sin(2\omega_0 t - \varphi) \end{cases} \tag{18}$$

$$\begin{cases} i_{un}(t) = I_0 + \frac{I_1}{2}\sin(\omega_0 t) + I_{2f}\cos(2\omega_0 t - \varphi) \\ i_{pn}(t) = I_0 - \frac{I_1}{2}\sin(\omega_0 t) + I_{2f}\cos(2\omega_0 t - \varphi) \end{cases} \quad I_0 = \frac{I_d}{3} \tag{19}$$

Each branch current is composed of three terms:

- The DC component, which follows the flow shown in Figure II-9 a)
- The AC component at the fundamental frequency; according to the flow depicted in Figure II-9 b), each branch conducts half of the phase output current
- The second harmonic component, which is kept in the branches (Figure II-9 c)) and represents the energy balance between the negative and the positive branch for each phase [49]-[14]. Moreover, this component doesn't flow on the DC side because it is a negative sequence.

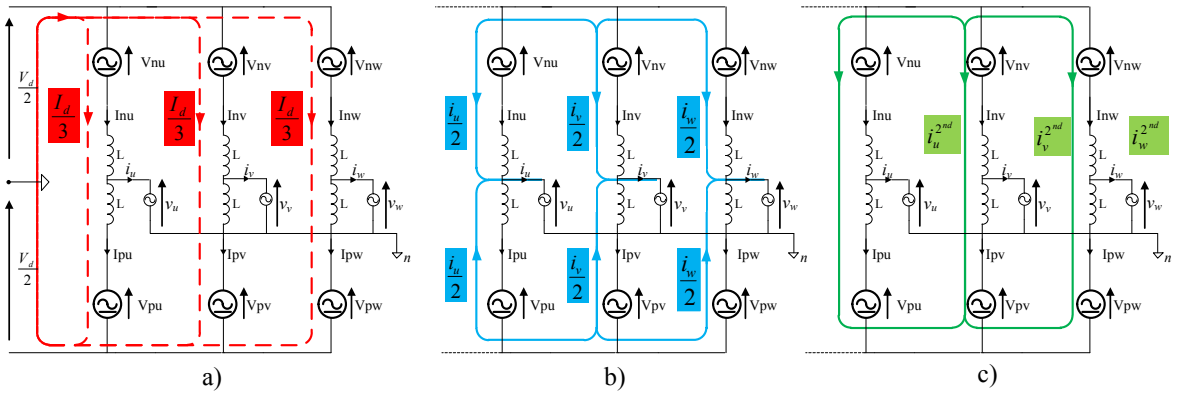


Figure II-9: Current flow in the MMC structure

The study of the system was conducted by making two different assumptions according to the considered control approach to the AC current. The two cases are described below:

• The output AC current imposition permits control of the system by considering the AC output current i_u. In this case, it is not possible to regulate the branch currents composed also by the 2nd harmonic component, which has to be considered in the study (Figure II-10). In this hypothesis, a method for the passive components sizing is given and, upon consideration for a case study, simulations were achieved.

• The branch current imposition operates directly on the branch currents i_{nu} and i_{pu} and supposes the AC voltage imposed on the AC output side. In this case, it is possible to achieve the AC output current desired and to suppress the second harmonic components (Figure II-11). Sizing parameters are given in the study, and one more time, the simulation results validated the study.

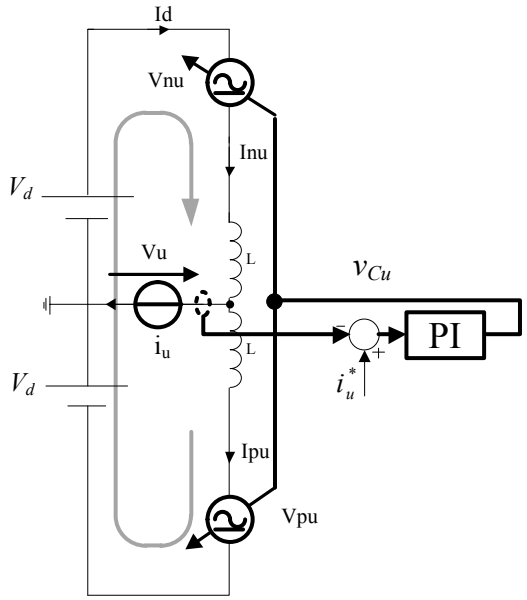


Figure II-10: MMC elementary circuit by imposing the AC output current

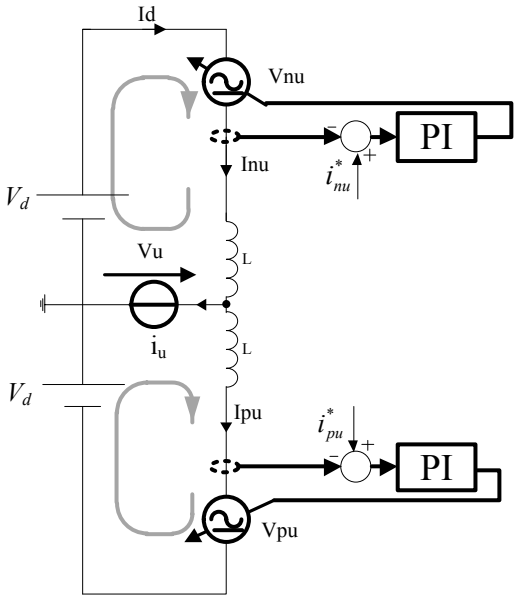


Figure II-11: MMC elementary by imposing each branch current

II.2 Output current imposition

In this section, the circuit presented in Figure II-10 is studied. The sizing parameters were achieved by starting from considerations made in (18) and (19). Evaluations gave the dependence of voltages and currents on the branch inductors and cell capacitors.

By suppressing the current source (Figure II-10), the amplitudes of the 2nd harmonic components of the branch voltages and currents are reported in (20) [49].

$$I_{2f}(t) = -\frac{V_{2f}}{4\omega_0 L}\sin(2\omega_0 t + \frac{\pi}{2} - \varphi) = I_{2f}\cos(2\omega_0 t - \varphi) \tag{20}$$

The capacitor current $i_c(t)$ is

$$i_{cn}(t) = i_{un}(t) \cdot \frac{1}{2}(1 - M\sin(\omega_0 t - \varphi))$$

$$i_{cn}(t) = \frac{I_0}{2} - \frac{I_0 M}{2}\sin(\omega_0 t - \varphi) + \frac{I_1}{4}\sin(\omega_0 t) - \frac{MI_1}{4}\sin(\omega_0 t - \varphi)\sin(\omega_0 t) + \\ + \frac{I_{2f}}{2}\cos(2\omega_0 t - \varphi) - \frac{MI_{2f}}{2}\cos(2\omega_0 t - \varphi)\sin(\omega_0 t - \varphi)$$

By using the Werner formulas:

$$i_{cn}(t) = \frac{I_0}{2} - \frac{I_0 M}{2}\sin(\omega_0 t - \varphi) + \frac{I_1}{4}\sin(\omega_0 t) - \frac{MI_1}{8}\cos(\varphi) + \frac{MI_1}{8}\cos(2\omega_0 t - \varphi) + \\ + \frac{I_{2f}}{2}\cos(2\omega_0 t - \varphi) - \frac{MI_{2f}}{4}\sin(3\omega_0 t - 2\varphi) + \frac{MI_{2f}}{4}\sin(\omega_0 t)$$

The current capacitor has also a third harmonic component thus, the capacitor current is achieved in (22) according to (21).

$$i_{cn}(t) = i_{cn}(t)_0 + i_{cn}(t)_{1st} + i_{cn}(t)_{2nd} \tag{21}$$

$$i_{cn}(t)_0 = \frac{I_0}{2} - \frac{MI_1}{8}\cos(\varphi)$$

$$i_{cn}(t)_{1st} = \frac{1}{4}\left(I_1 - 2I_0 M\cos(\varphi) + I_{2f}M\right)\sin(\omega_0 t) + \frac{I_0 M}{2}\sin(\varphi)\cos(\omega_0 t)$$

$$i_{cn}(t)_{2nd} = \frac{1}{8}(MI_1 + 4I_{2f})\cos(2\omega_0 t - \varphi) \tag{22}$$

$$i_{cn}(t)_{3rd} = \frac{MI_{2f}}{4}\sin(3\omega_0 t - 2\varphi)$$

The fundamental current component is sufficient to generate the second harmonic component. Moreover, according to (23), to keep a constant DC component of the capacitor voltage, the DC component of the capacitor current has to be equal to zero, so it is possible to achieve a relationship between the I_1 and I_0 in (24).

It is possible to verify that the amplitude of the third harmonic for the capacitor voltage can be neglected with respect to the other ones. Thus the capacitor voltage (25) and the total branch voltage (26)-(27) can be obtained.

$$V_{cn}(t) = \frac{V_d}{N} + \frac{1}{C}\int i_{cn}(t)dt \tag{23}$$

$$I_0 = \frac{MI_1}{4}\cos(\varphi) \tag{24}$$

$$V_{cn}(t)_0 = \frac{V_d}{N}$$

$$V_{cn}(t)_{1st} = \frac{1}{\omega_0 C}\frac{I_1 M^2}{8}\cos(\varphi)\sin(\varphi)\cdot\sin(\omega_0 t) - \frac{1}{\omega_0 C}\frac{1}{4}\left[I_1\left(1-\frac{M^2}{2}\cos^2(\varphi)\right)+I_{2f}M\right]\cdot\cos(\omega_0 t) \tag{25}$$

$$V_{cn}(t)_{2nd} = \frac{1}{2\omega_0 C}\frac{1}{8}(MI_1 + 4I_{2f})\sin(2\omega_0 t - \varphi)$$

$$V_{un} = N\left[V_{cn}(t)\cdot\frac{1-M\sin(\omega t-\varphi)}{2}\right] \tag{26}$$

$$V_{un}(t)_0 = \frac{V_d}{2} - \frac{NM}{8\omega_0 C}\left[\frac{I_{2f}M}{2} + I_1\frac{2-3M^2\cos^2(\varphi)}{4}\right]\sin(\varphi)$$

$$V_{un}(t)_{1st} = \left\{\begin{array}{c} M\left[\frac{I_1 MN\cos(\varphi)\sin(\varphi)}{16\omega_0 C} - \frac{V_d\cos(\varphi)}{2}\right]\sin(\omega_0 t) + \\ +\left[\frac{MV_d\sin(\varphi)}{2} - \frac{MN(4I_{2f}+MI_1)}{64\omega_0 C} - N\frac{I_{2f}M + I_1\left(1-4M^2\cos^2(\varphi)\right)}{8\omega_0 C}\right]\cos(\omega_0 t)\end{array}\right\} \tag{27}$$

$$V_{un}(t)_{2nd} = \frac{N}{16\omega_0 C}\left[\frac{4I_{2f}+I_1 M}{2} + M(MI_{2f} + I_1\frac{2-M^2\cos^2(\varphi)}{2})\right]\sin(2\omega_0 t-\varphi) + \frac{I_1 M^3 N\cos(\varphi)\sin(\varphi)}{8\omega_0 C}\cos(2\omega_0 t-\varphi)$$

By fixing the apparent power of the system, V_d and therefore N, I_1, and M and varying the power factor, the variation of the amplitude of $V_{un}(t)_{2nd}$ is not very sensitive to its second term, so it is possible to rewrite $V_{un}(t)_{2nd}$ as (28).

The amplitude of the 2nd harmonic component of the current is therefore extracted in (29).

$$\left|\frac{V_{un}(t)_{2nd}}{2\omega L}\right| = I_{2f} \qquad with \qquad |V_{un}(t)_{2nd}| \approx \frac{N}{16\omega_0 C}\left[\frac{4I_{2f}+I_1 M}{2} + M(MI_{2f} + I_1\frac{2-M^2\cos^2(\varphi)}{2})\right] \tag{28}$$

$$I_{2f} \approx I_1\frac{M^3 N\cos^2(\varphi) - 3MN}{2NM^2 - 64LC\omega^2 + 4N} \tag{29}$$

This study permits evaluation of the 2nd harmonic amplitude of the branch currents and voltages from the knowledge of the power rate of the system, V_d and therefore N, I_1, and M.

II.2.1 Cell capacitor

The value of the capacitor is extracted according to the ripple amplitude of the voltage at low frequency. By considering equation (25), the components of the voltage do not depend

only on the capacitor value but also on the I_{2f} , whose extraction is in (29). The evaluation of the capacitor becomes a non-linear problem.

For this reason, the evaluation of the cell capacitor was achieved by implementing the formulas given previously in an iterative procedure shown in the flow chart in Figure II-12.

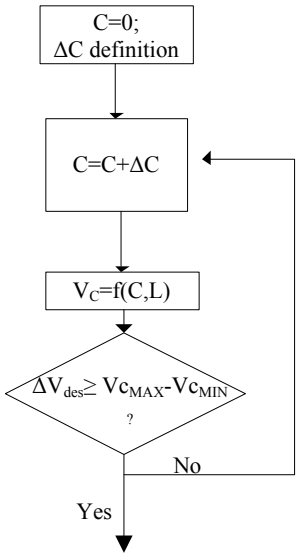


Figure II-12: Iteration method for the capacitor evaluation

II.2.2 Branch inductor

When the second harmonic component in the current is considered, it is necessary to define a limit range within which the branch inductor has to be defined.

The inferior limit is given by the ripple amplitude of the branch current due to the commutations of the devices. By assuming a sinusoidal pulse width modulation and considering that all of the cells are interleaved between them, the maximum amplitude of the branch current ripple is ΔI_{MAX}. In (30) is reported the inferior limit of the inductor.

$$L > \frac{Vd}{8N^2 f_c \Delta I_{MAX}} \tag{30}$$

The second harmonic component of the branch current contributes to increase the total rms value. If this component is considered, an oversizing of semiconductor devices and the copper of the inductor must be taking into account. According to (29), to limit the amplitude of the

second harmonic component of the branch current, it is necessary to increase the value of the inductor.

If the inductor value is significant, its voltage drop at the fundamental frequency could become very great. Usually, the voltage drop on the inductor, ΔV_L, has to be kept under a small percentage of the AC voltage to ensure the controllability of the system at network frequency (31).

$$L < 2\frac{\Delta V_{LMAX}}{\omega_0 I_1} \tag{31}$$

II.2.2.1 Considerations

The only way to limit the branch second harmonic both for the voltage and the current is to size the reactive elements as big as possible. For the current controller, it is not possible to operate on this component, which flows only in the branch (look the grey loop in Figure II-9).

The dynamic response of the equivalent internal current loop has to be studied. To extract the equivalent capacitor of each branch the relationship between the output voltage of the $v_{un/p}$ (32) and the branch current $i_{u(n/p)}$ (33) of the averaged branch shown in Figure II-3, if the averaged duty cycle of the cell is considered equal to ½. The branch capacitance is extracted in (38) and for the phase is (39).

$$\frac{C}{N}\frac{dv_{Cu}}{dt}(t) = \frac{1}{2}i_{un}(t) \tag{32}$$

$$v_{Cu} = 2 \cdot v_{un} \tag{33}$$

$$\frac{4C}{N}\frac{dv_{un}}{dt}(t) = i_{un}(t) \tag{34}$$

$$C_{eq} = \frac{4C}{2N} \tag{35}$$

The equivalent circuit of the loop depicted in Figure II-10 is achieved in Figure II-13 for the small signal approximation.

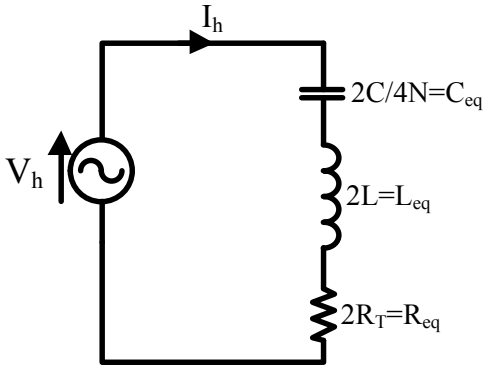


Figure II-13: Equivalent RLC circuit of a single phase

$$H(j\omega) = \frac{I}{V} = \frac{j\omega C_{eq}}{1 - \omega^2 L C_{eq} + j\omega R_{eq} C_{eq}} \tag{36}$$

$$\omega_r = \frac{1}{\sqrt{L_{eq} C_{eq}}} \tag{37}$$

$$\xi = \frac{R}{2}\sqrt{\frac{C_{eq}}{L_{eq}}} \tag{38}$$

The RLC circuit includes the capacitor, which represents the equivalent capacitance in the phase; then there are the negative and the positive inductors and the resistance, which resumes the dissipative part of the semiconductors and the copper losses. The system is studied like a typical second-order circuit of which the transfer function is (36).

According to the particular application, it is possible to achieve some consideration for the bode diagram of the magnitude (Figure II-14), particularly about the frequency resonance (37) and the damping factor (38).

If the considered system has to sustain high voltages, the number of cell capacitors N can be considered huge. If the typical value of the cell capacitor is around mF [51], the C_{eq} is relatively small. Thus, in most cases the frequency resonance f_r is greater than the fundamental frequency. Moreover, the branch inductor is around mH if the second harmonic has to be attenuated [50]. This leads to a dumping factor (38) smaller than 1. For these reasons, the fundamental frequency of the system is placed in the positive slope of the magnitude curve (Figure II-14). This means a further increase for the amplitudes of greater harmonics.

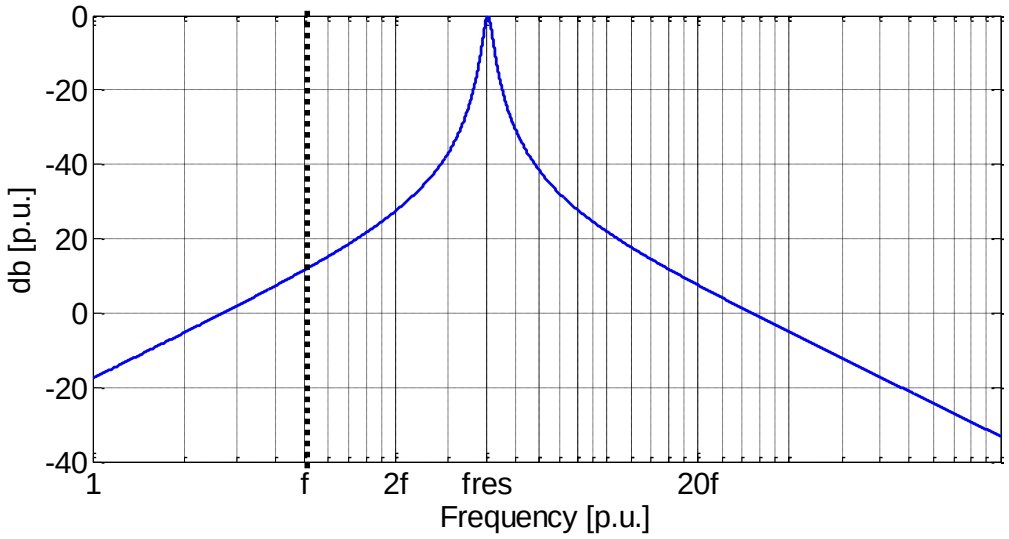


Figure II-14: Bode diagram of a RLC circuit for a typical high voltage system

With these considerations, for this control approach the inductor sizing has to respect the condition on the resonant pulsation given in (38).

$$\omega_r = \frac{1}{\sqrt{L_{eq}C_{eq}}} < \omega_0 \tag{39}$$

This condition requires an increment of the mathematical product on the denominator. The chance to increment the value of the capacitor is greatly reduced because of the physical size of this element which is included on each elementary converter. It is not possible to further increment the branch inductor because of the voltage drop condition (31) at the fundamental frequency. For these reasons, in the next section is given a new configuration of the inductor which can better manage the two contrasting conditions given until now.

II.2.2.2 Coupled inductors

The aim of this configuration is to achieve an inductor which offers a small series impedance to respect the condition (31) and a high impedance at $2.f_r$ to meet the condition (39). Considerations start from the classical configuration of the 4-port model of a transformer depicted in Figure II-15. The equations which characterize the real transformer are shown in (40).

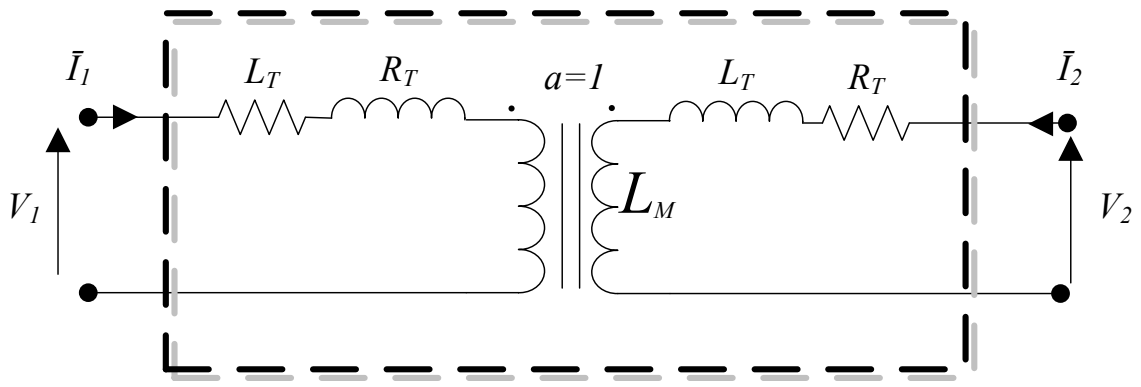


Figure II-15: 2-port model of a transformer

$$\begin{aligned} \bar{V}_1 &= \left[j\omega\left(L_T + L_M\right) + R_T\right]\cdot \bar{I}_1 + j\omega L_M \bar{I}_2 \\ \bar{V}_2 &= j\omega L_M \bar{I}_1 + \left[j\omega\left(L_T + L_M\right) + R_T\right]\cdot \bar{I}_2 \end{aligned} \tag{40}$$

If the transformer is connected in the configuration depicted in Figure II-16, it can be considered a tripolar component of which equations are reported in (41) and (42).

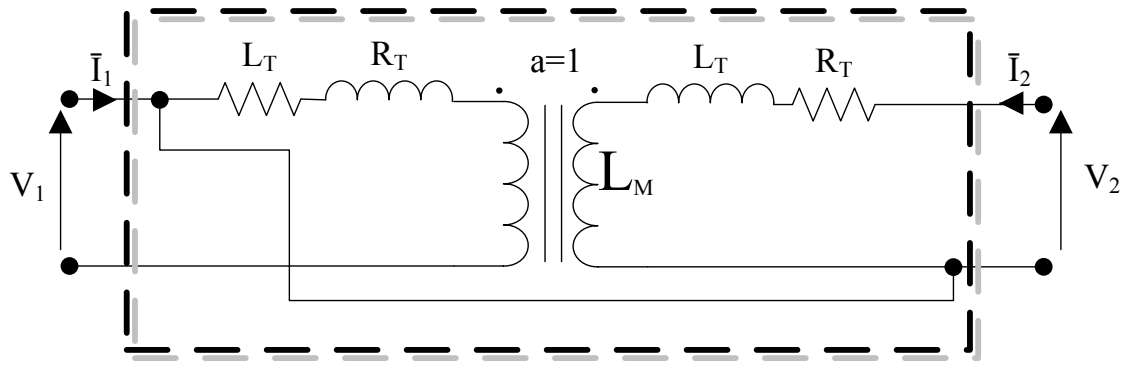


Figure II-16: transformer model in tripolar configuration

$$\begin{aligned} \bar{V} &= \bar{V}_1 + \bar{V}_2 \\ \bar{I} &= \bar{I}_1 + \bar{I}_2 \end{aligned} \tag{41}$$

$$\begin{cases} R = 2R_T \\ L = 2L_T + 4L_M \end{cases} \Rightarrow \bar{V} = (R + j\omega L)\bar{I} \tag{42}$$

The reactive element provides results that can be considered a simple connected inductor series element for which the schema is shown in Figure II-17. This circuit has a series inductor which has four times the magnetization inductance L_M and output impedance L_T, which typically is very low as described in (43).

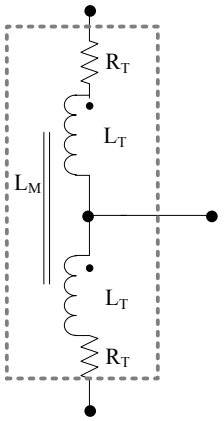


Figure II-17: Equivalent tripolar element of the coupled transformer

$$\begin{cases} R = 2R_T \\ L = 2L_T + 4L_M \end{cases} \Rightarrow \bar{V} = (R + j\omega L)\bar{I} \tag{43}$$

The coupled transformer requires more complicated building costs; on the other hand it presents an equivalent branch inductance which is four times that of the classical version. This can be achieved if the magnetization inductance is sized with the same number of turns of the simple branch inductor.

II.2.3 Simulations

After the choice of the system power rate, in this section, simulations performed validated the sizing parameters given above. Moreover, the improvements through the coupled reactor are shown.

A HVDC link to connect an off-shore wind farm platform is considered as a case study. The nominal power level is 100 MW, with a DC voltage of 160 kV. The MMC is rated considering press-packed IGBT. The study is carried out by considering a classical PWM control with an interleaving of the cells.

All of the simulations are performed by considering the macro model. The reference structure is depicted in Figure II-3, and it considers just six averaged cells (one per branch), each of which resumes the N interleaved instantaneous cells. Each capacitor corresponds to the whole capacitance of each branch and has to sustain the DC voltage V_d.

II.2.3.1 MMC system with classical branch inductor

The main parameters of the system are given in Table II-2.

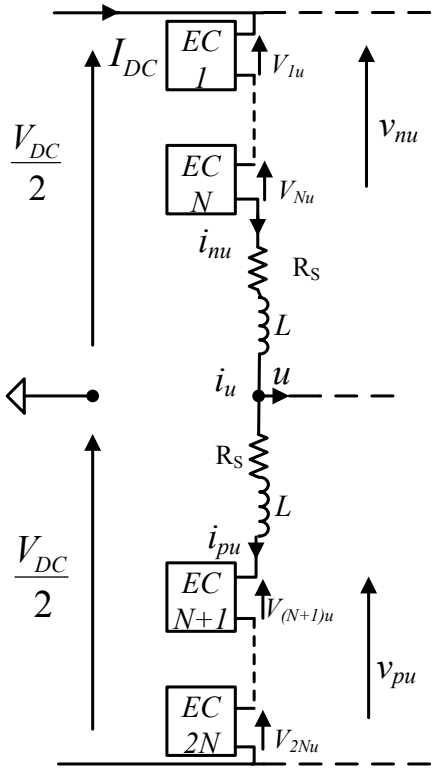


Figure II-18: Case study system

Table II-2: system power rate

System Power Rate	
Nominal power	100 MW
Phase to phase Grid voltage V_{ll}	83 kV
V_d	160 kV
Number of sub-modules	N=64
Voltage capacitor	2.5 kV
Inductor resistance R_S	60 mΩ

In this case, an inductor equal to 50mH was chosen, and a cell capacitor of 7mF is picked to achieve a voltage ripple around the 10%. According to condition (39), a resonance frequency of 34 Hz was chosen. In Figure II-19, the capacitor voltages are reported only for a single phase. The chosen capacitor keeps the ripple amplitude under the imposed value.

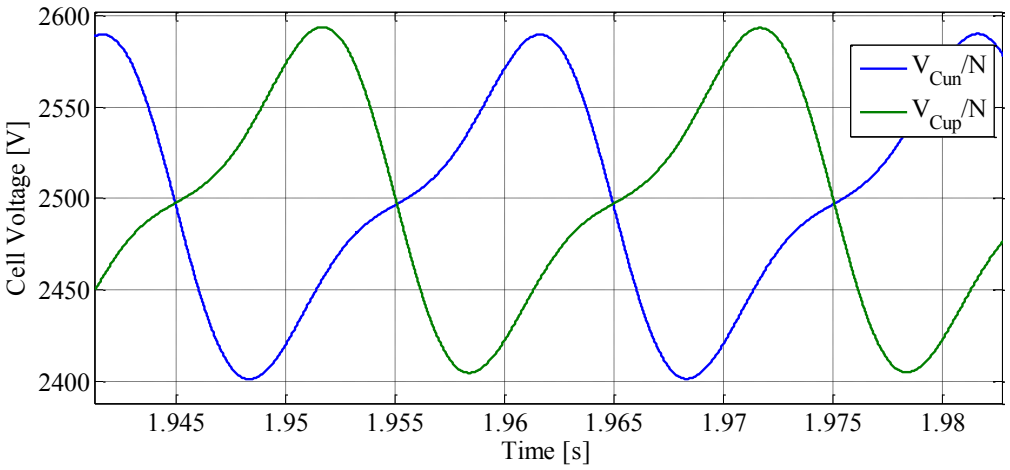


Figure II-19: Cell voltage normalized on the number of cells

The currents flowing (Figure II-20) in the branch inductors have a limited second harmonic component around 10%, as shown in Figure II-21. Moreover, other harmonics are not amplified, so condition (39) is met.

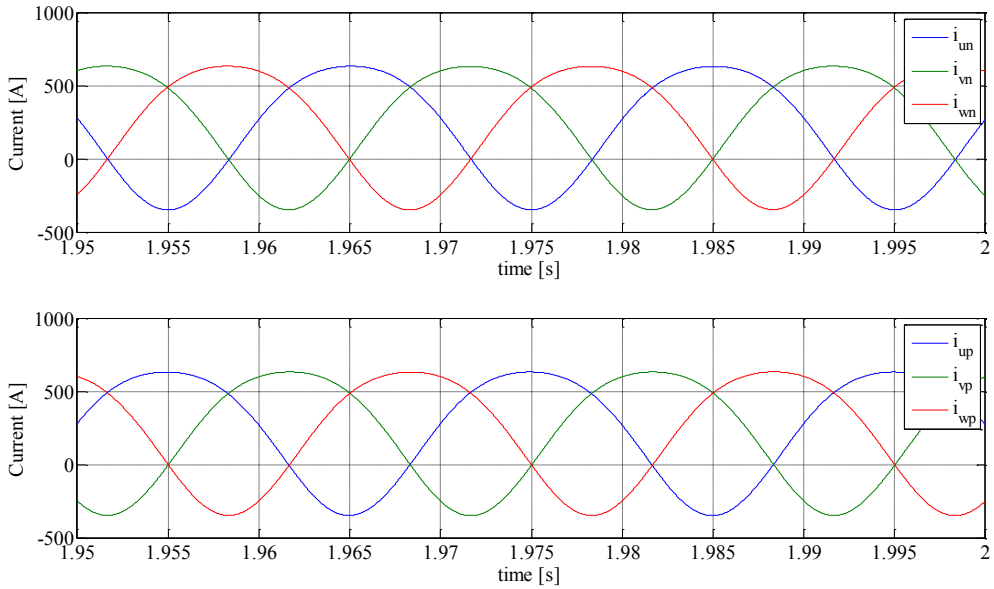


Figure II-20: branch currents

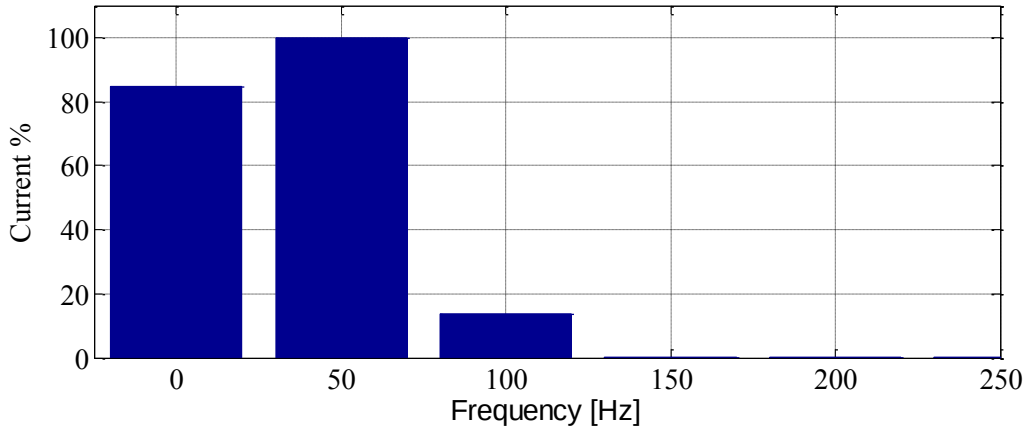


Figure II-21: Spectral content of the branch current in percentage with respect to the fundamental component

The huge inductor value makes the system unable to meet condition (31). Figure II-22 reports a huge voltage drop on the inductor, which could cause the system to lose the current controllability. Under these assumptions, the system is not able to quite match all of the conditions imposed in the previous section.

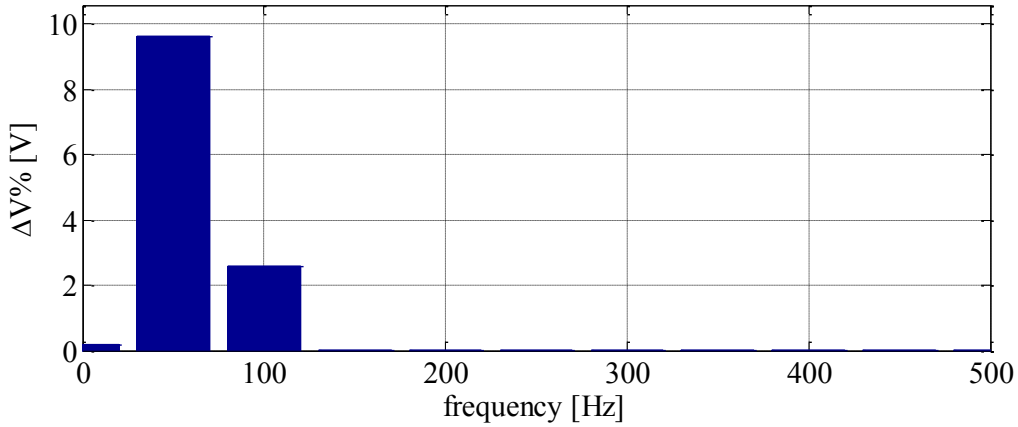


Figure II-22: Percentage spectral content of the voltage drop on the branch inductor

In the next paragraph, the interphase transformer is employed for the MMC structure. This reactor is called to replace the traditional branch inductor to overcome the contrasting conditions given before.

II.2.3.2 Coupled transformer for MMC structure

The interphase transformer is chosen with a magnetization inductor L_M of 25 mH. The inductor L_T candidate to define the series voltage drop V_L at the fundamental frequency is chosen to be 20 times smaller than the previous one. A cell capacitor of 6mF is proposed always to achieve a voltage ripple around the 10% mark. By considering condition (39), the resonance frequency of the circuit is 36 Hz.

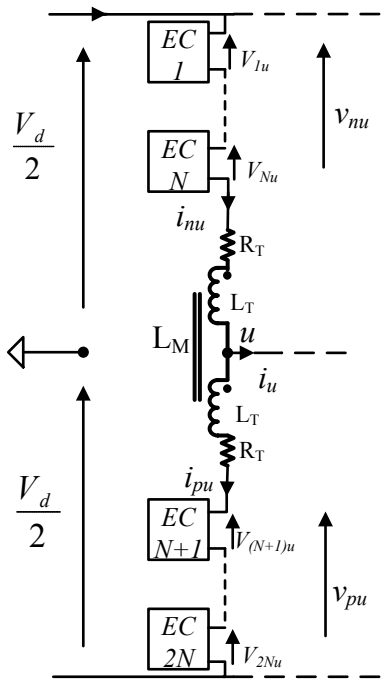


Figure II-23: MMC phase with coupled inductors

Table II-3: Reactive elements sizing

Cell Capacitor	6 mF
L_T @ ΔI_{MAX}	2.5 □ H
L_M	25 mH

Figure II-24 reports the capacitor voltages. The chosen capacitor keeps the ripple amplitude under the imposed values.

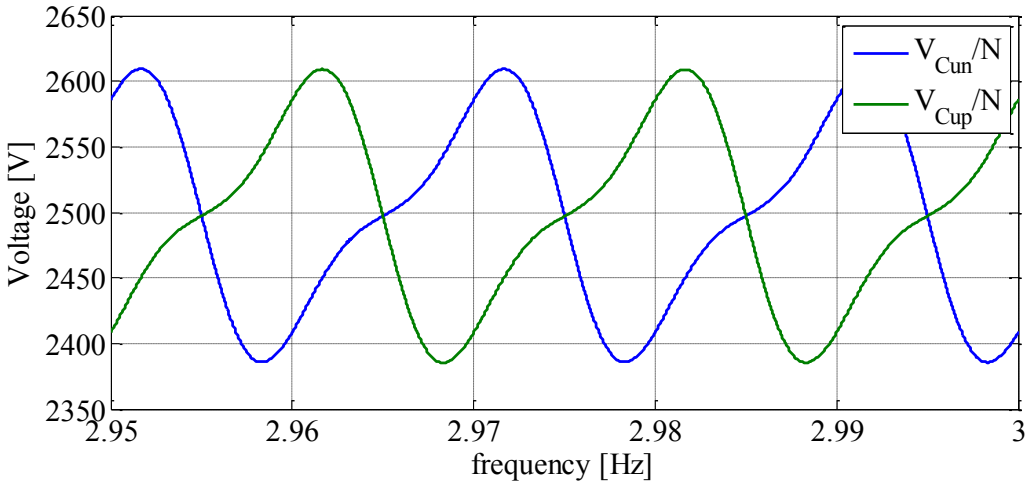


Figure II-24: Cell voltage normalized on the number of cells

Also, in this case, the branch inductors (Figure II-25) are able to limit the second harmonic component as shown in Figure II-21. Moreover, other harmonics are not amplified so that condition (39) is met.

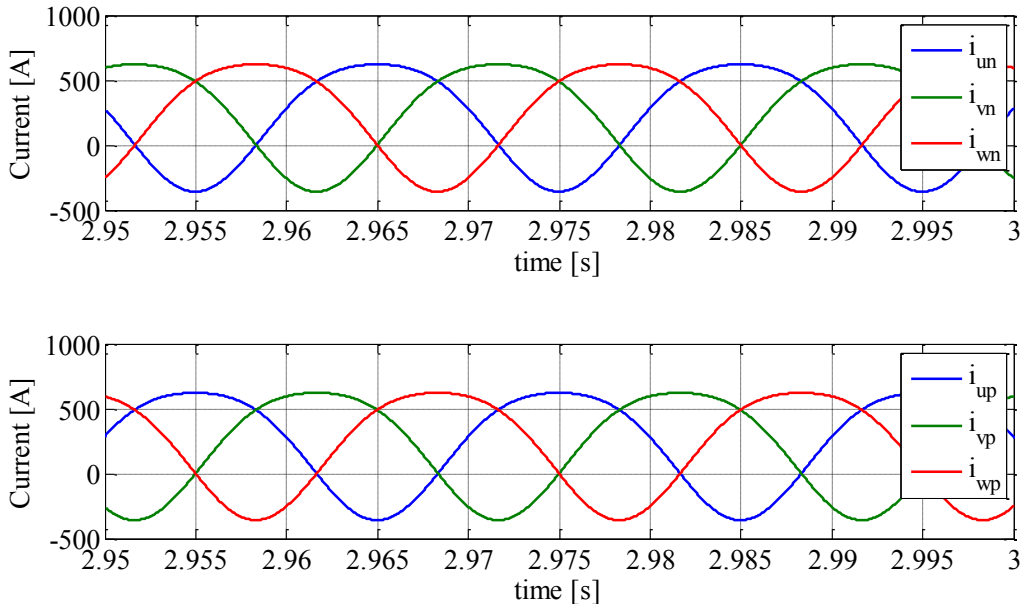


Figure II-25: Branch currents

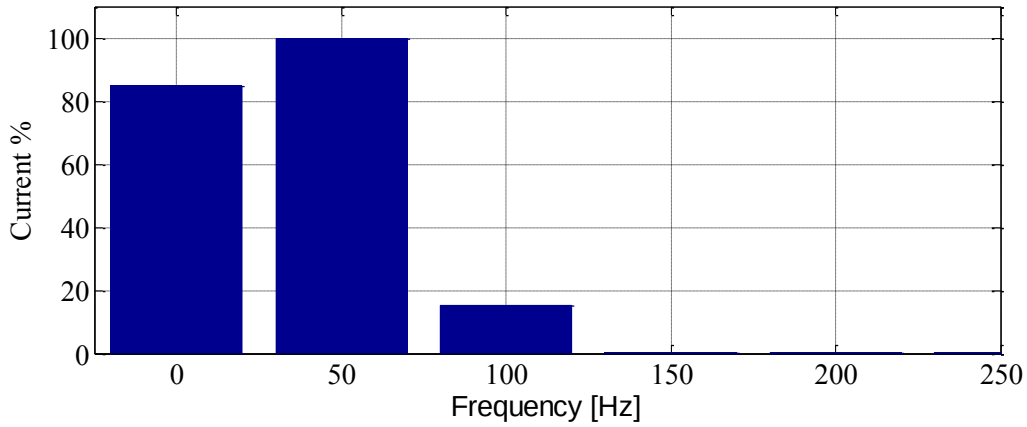


Figure II-26: Spectral content of the branch current in percentage with respect to the fundamental component

The employment of coupled inductors (interphase transformer) better manages the tradeoff between the frequency response condition affirmed in (39) and a low-voltage drop on the series inductor L_T depicted by (31). Figure II-27 reports the voltage drop with respect to the phase voltage amplitude provided for the classical branch inductor employment and the coupled inductors employment. The amplitude of the voltage drop is reduced about ten times that of the classical version.

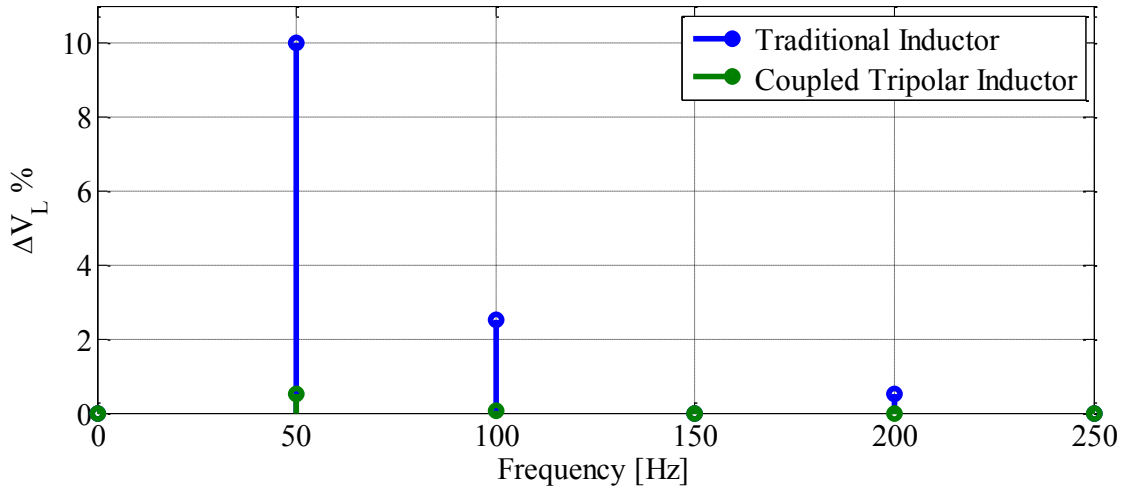


Figure II-27: Comparison of the harmonic content of the voltage drop on the traditional branch inductor of the previous case and the series inductor L_T

For MMC structures, the use of the coupled transformer better manages the hard trade-off between the controllability of the system and the dynamic response. If this approach is adopted, the interphase transformer employment is suggested. In this application, only one current control loop is necessary with respect for other traditional approaches. On the other hand, more complex hardware is necessary.

II.3 Branch current imposition

For this approach, there are two controls per phase that operate directly on the branch currents i_{nu} and i_{pu} , and the AC voltage is imposed on the AC output side. In this case, it is possible to achieve the AC output current desired and to suppress the second harmonic components (Figure II-11). A detailed description of the control is proposed in Chapter IV. Thus, the voltages $v_{(n/p)u}$ (44)-(45) and the currents $i_{(n/p)u}$ (46)-(47) are reported without the second harmonic component. As evaluated in (21) the current has a DC component which is related to the fundamental one to keep constant the voltage capacitor in the cell. A clearer understanding on the components of the branch currents can be achieved by looking Figure II-9.

$$u_{nu}(t)=\frac{V_d}{2}\left(1-m(t)\right);\ u_{pu}(t)=\frac{V_d}{2}\left(1+m(t)\right) \tag{44}$$

$$u_u(t)=\frac{u_{pu}(t)-u_{nu}(t)}{2}=\frac{V_d}{2}m(t); \tag{45}$$

$$i_{nu}(t) = \frac{MI_1}{4}\cos(\varphi) + \frac{I_1}{2}\sin(\omega_0 t)$$
$$i_{pu}(t) = \frac{MI_1}{4}\cos(\varphi) - \frac{I_1}{2}\sin(\omega_0 t) \quad (46)$$

$$i_u(t) = i_{nu}(t) - i_{pu}(t) = I_1 \sin(\omega_0 t) \quad (47)$$

II.3.1 Sizing

The value of capacitor C is chosen to limit the voltage ripple at the fundamental frequency ΔV_C provided by (25) and with a neglected second harmonic component. The maximum ripple amplitude is achieved in a pure reactive operating mode, when *sin(φ)=1.* So the capacitor evaluation in this case is a linear problem and can be extracted from (48)..

$$C = \frac{I_1}{2\omega_0 \Delta V_C}; V_C = \frac{V_d}{N} \quad (48)$$

II.3.1.1 Considerations on the arm inductor

For systems with high power and high voltage, the number of sub modules employed becomes very large. For this reason, the equivalent switching frequency is very high if interleaved modulations are implemented. This allows a very low switching frequency f_{sw} for each device, which leads to a significant reduction in the switching losses. At this condition, the branch inductor value, which is calculated from (30), is very low for a huge number of cells. The second harmonic suppression in the branch is not considered, because it is automatically managed by the current control loop. Problems due to the dynamic response no longer exist because the control approach is different. On the other hand, the branch inductor plays a key role in the limitation of short circuit currents under faulty conditions. For this reason, a low branch inductor means huge short circuit currents. If a branch current control approach is considered, the choice of this reactive element is achieved in order to limit the short circuit current. This aspect is taken into account in V.II.

For a limited number of sub modules, usually the branch inductor value given by (30) succeeds in managing a limited short circuit current, too.

II.3.2 Simulations

According to the considerations provided previously, an inductor equal to 10 mH was chosen, the ripple amplitude of the current is kept around 7% (Figure II-28). Only in this case instantaneous model is considered to achieve the current ripple. A cell capacitor of 6mF is considered to achieve a voltage ripple around 10% of the DC value (V_d/N). Simulations are

performed by considering the averaged model shown in Figure II-3. The capacitor voltages reported in Figure II-29 just for a single phase show that the amplitude of the voltage ripple is kept under the imposed value.

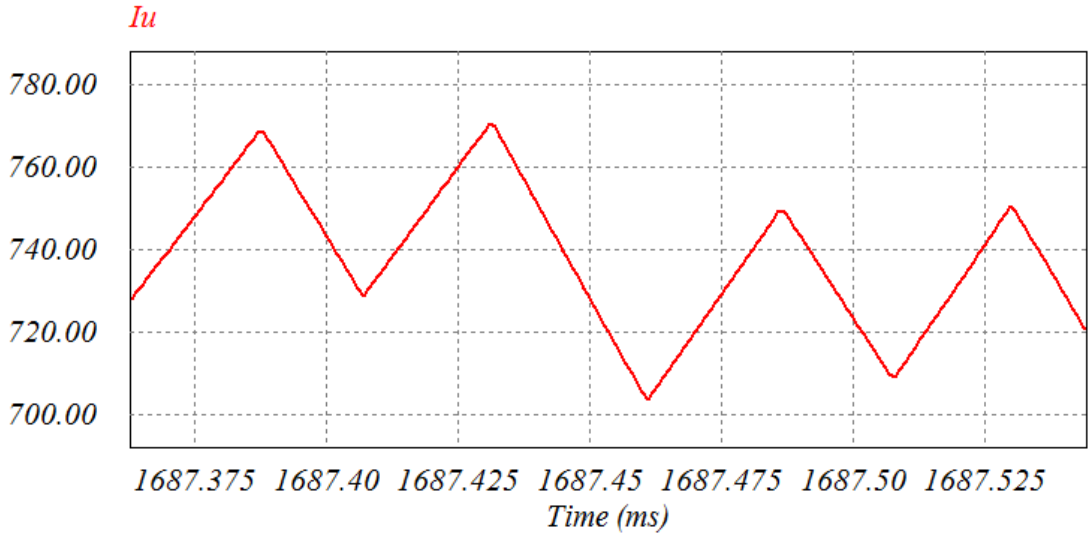


Figure II-28: Current ripple on the phase current from the instantaneous model

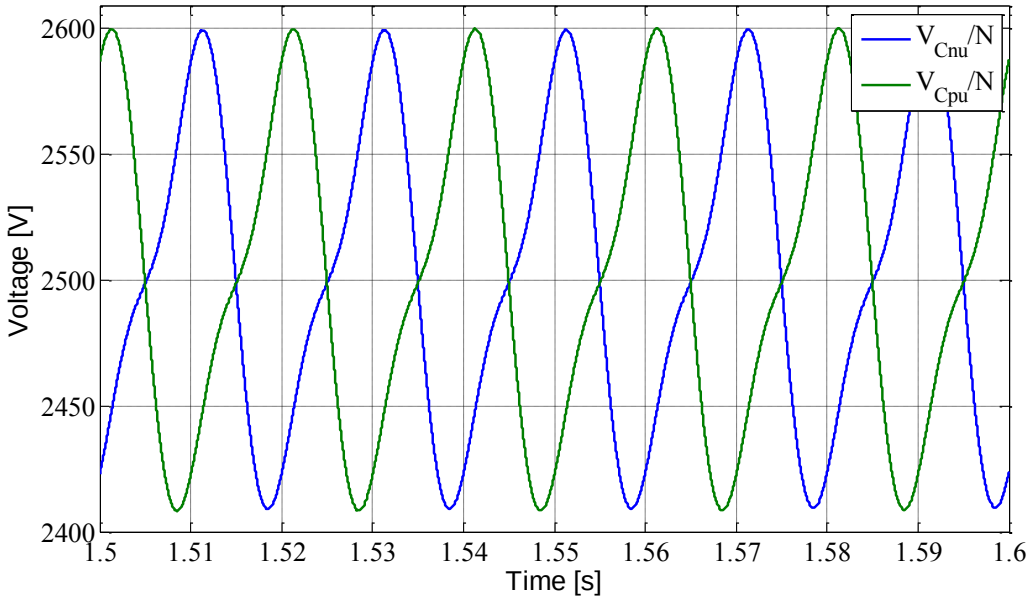


Figure II-29: Voltage capacitor normalized on the number of cells

The currents flowing in the branch inductors (Figure II-30) can be considered sinusoidal. The second harmonic component is reduced and can be considered negligible with respect to the fundamental.

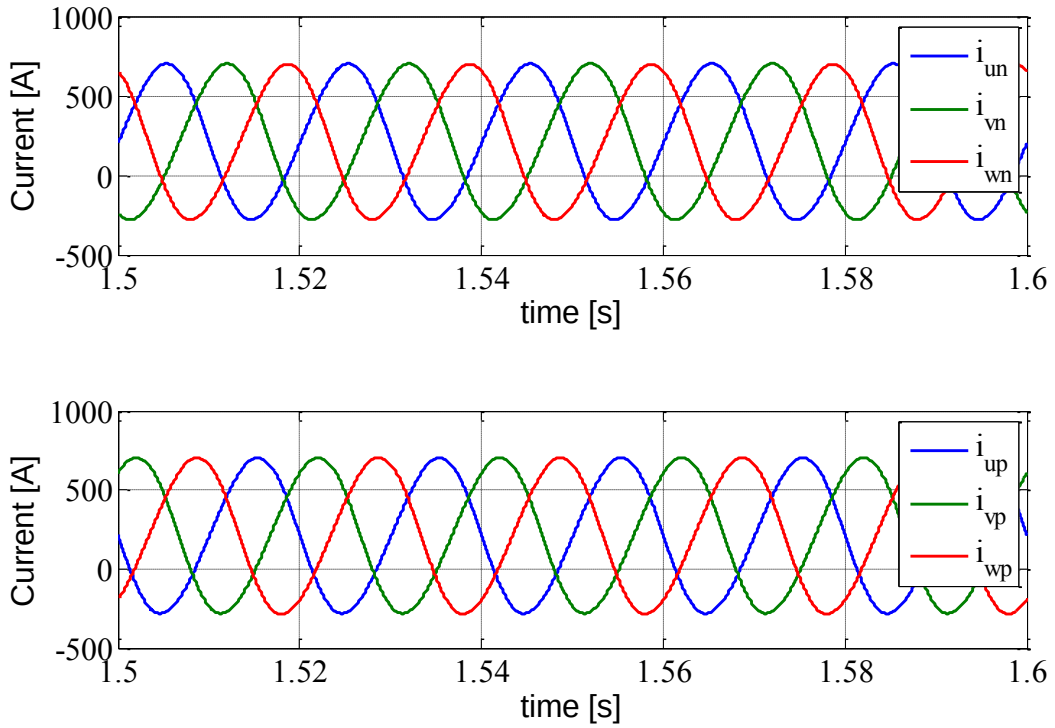


Figure II-30: Branch currents

The second harmonic component is greatly reduced if compared to the previous case (output current imposition) as shown in Figure II-31. The current control loop in the branch directly limits the component.

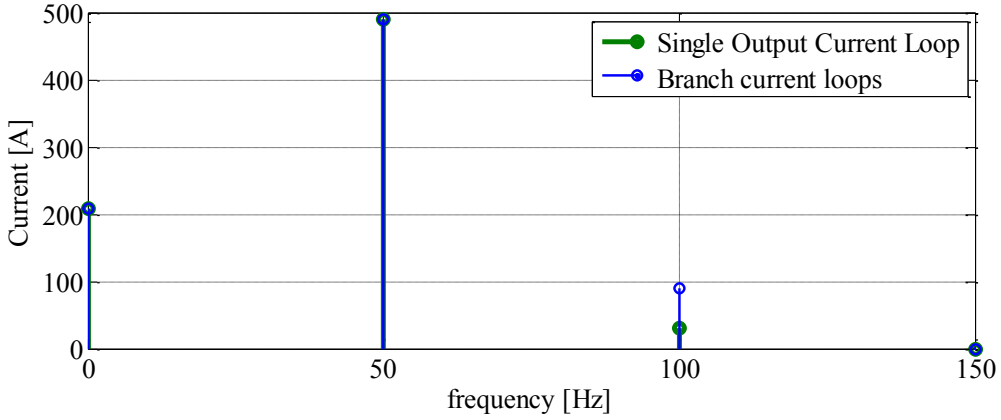


Figure II-31: Comparison of the branch current -harmonic content

II.4 Conclusions

The macro-model makes the preliminary evaluations direct and allows for very fast simulations. The control of the AC output current can lead to a huge second harmonic of the fundamental component in the branch current and an amplification of the greater harmonics. The simple approach of the control has to be compensated by hardware which becomes more complicated and expensive. On the other hand, the second approach facilitates the employment of more simple hardware. Of course, it requires a slightly more complicated control that is not a problem today thanks to the large choice of control devices available on the market. For these reasons, the second control approach was chosen herein the thesis.

Chapter III. **New multilevel topologies**

A topological study is consolidated and extended in this chapter on three different cell topologies. The study of each cell is achieved, and their employment for the MMC structure is treated. For each cell, topology advantages and limits are discussed in terms of current and voltage. By fixing the nominal power of the system and the DC link voltage, the cells are studied and compared in terms of current and voltage on the AC output. It is shown that also improvements on the rating of the reactive elements can be achieved if other topologies are chosen as the elementary cell with respect for the basic cell employed. An analytic approach for the power losses evaluation is given. The losses in the semiconductor devices are evaluated for each topology.

In the second part of this chapter a new multilevel structure is presented. For each phase this topology adopts just one branch and interfaces itself with the grid through the zig-zag transformer. The new structure is compared with the MMC one in terms of sizing. Moreover the so-called multilevel Half wave structure is proposed in order to upgrade the old three phase rectifiers based on diodes/thyristors. The upgrating is achieved by keeping the same grid transformer and therefore the voltage and current levels. Simulations are performed in order to validate the study and evaluate the advantages.

III.1 Elementary converters for the MMC Structure

The choice of the elementary converter depends on the current and voltage which the MMC system has to conduct and to impose. A series of preliminary considerations on the power flow and the control approach are necessary to determine the voltage and current waveforms. As it was introduced in the previous chapter, the branch current control approach is chosen.

For VSC-HVDC systems, as discussed in the chapter I, the grid voltage is imposed so the power flow is regulated through the current regulation as shown in the base circuit reported in Figure III-1. The basic control for an MMC structure is depicted in Figure III-2 according to the choice made in previous section. To simplify the representation, only one phase is depicted; the considered phase voltage and current are shown in (49)-(50). The averaged model is considered for the analysis, and the controlled sources (v_{nu} and v_{pu}) resume the N series connected converters.

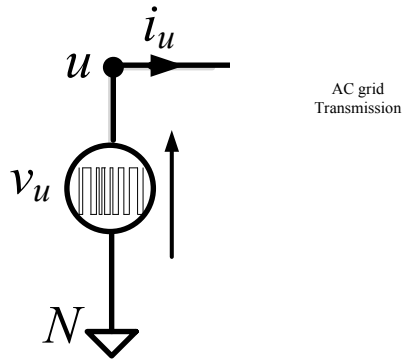


Figure III-1: AC side of the DC-AC transmission

$$i_u = \sqrt{2} I \sin(\omega_0 t) \quad (49)$$

$$v_u = \sqrt{2} V \sin(\omega_0 t - \varphi) \quad (50)$$

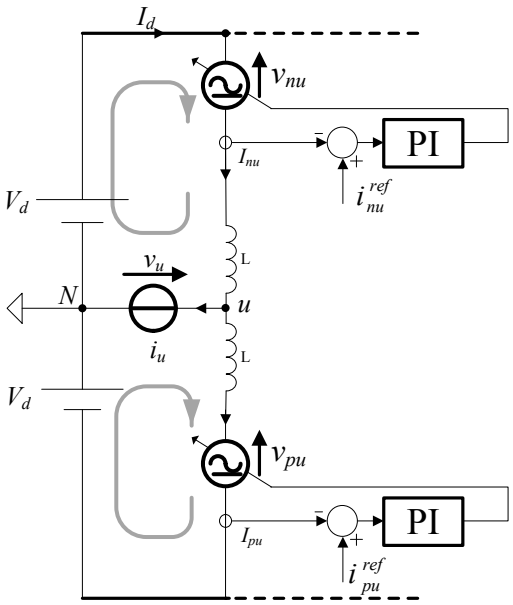


Figure III-2: Current regulation for the power flow provided for a MMC structure

Considerations regarding voltages and currents are given by splitting the circuit in the AC and DC part (principle of superposition). The study is performed only for one phase.

According to the AC circuit of the MMC structure (Figure III-3), the branch currents (51) and voltages (53) are provided. This is valid if the branch inductors have the same value and a negligible voltage drop. For the DC part of the system (Figure III-4), each branch conducts the third part of the DC current (52) because of the three phases. The controlled voltage source in the branch must balance the DC link voltage according to (54).

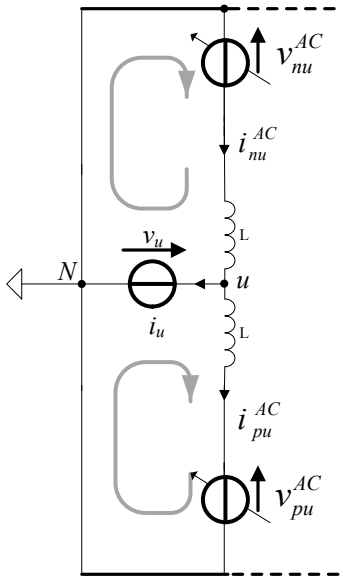


Figure III-3: AC circuit of the MMC structure

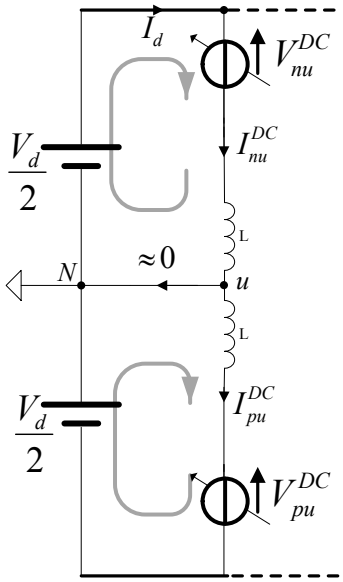


Figure III-4: DC circuit of the MMC structure

$$\begin{cases} i_{nu}^{AC} = \dfrac{i_u}{2} \\ i_{pu}^{AC} = -\dfrac{i_u}{2} \end{cases} \quad (51) \qquad \begin{cases} I_{nu}^{DC} = \dfrac{I_d}{3} \\ I_{pu}^{DC} = \dfrac{I_d}{3} \end{cases} \quad (52)$$

$$\begin{cases} v_{nu}^{AC} \approx -v_u \\ v_{pu}^{AC} \approx v_u \end{cases} \quad (53) \qquad \begin{cases} V_{nu}^{DC} = \dfrac{V_d}{2} \\ V_{pu}^{DC} = \dfrac{V_d}{2} \end{cases} \quad (54)$$

To balance the AC and the DC sides, each branch must conduct the currents in (55) and impose the voltages in (56).

$$\begin{cases} i_{nu} = \dfrac{i_u}{2} + \dfrac{I_d}{3} \\ i_{pu} = -\dfrac{i_u}{2} + \dfrac{I_d}{3} \end{cases} \quad (55) \qquad \begin{cases} v_{nu} = -v_u + \dfrac{V_d}{2} \\ v_{pu} = v_u + \dfrac{V_d}{2} \end{cases} \quad (56)$$

The active and the reactive power on the AC side are reported in (57).

$$\begin{aligned} P_{AC} &= 3VI\cos(\varphi) \\ Q &= 3VI\sin(\varphi) \end{aligned} \quad (57)$$

On the DC side the active power is achieved in (58).

$$P_{DC} = V_d I_d \tag{58}$$

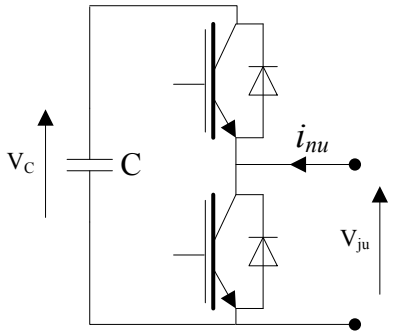
From a power balance between the DC and AC side the (59) is carried out.

$$V_d I_d = 3VI\cos(\varphi) \tag{59}$$

In the next three sections, different topologies for the elementary converters are presented as candidates to be employed for MMC structures. Limits and advantages are highlighted for each topology. The approach supposes that each branch voltage is the equivalent sum of the N series converters as depicted in the previous section. The averaged model was considered for the study to make the analysis fast and direct. Moreover, a sinusoidal pulse width modulation is supposed.

III.1.1 Single Cell

This is the base cell topology used for MMC structures. This cell presents two transistors with anti-parallel diodes (Figure III-5). This topology allows the imposition of a monopolar voltage and the conducting of a bi-directional current. The study is provided for the negative part of the system; considerations on the positive part are directly deducted for symmetry.



- Monopolar voltage
- Bi-directional current

Figure III-5: Single cell topology

This structure can impose only a positive voltage as shown in Figure III-6. If the considered branch voltage is (56), the condition (60) must be met. The voltage on the cell capacitor V_C must make the system able to reach all the voltage levels required as depicted by (61).

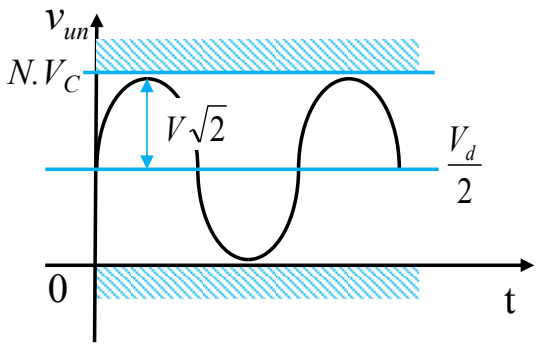


Figure III-6: Averaged voltage waveform if the single cell is considered

$$V\sqrt{2} \le \frac{V_d}{2} \tag{60}$$

$$N \cdot V_C = 2.\frac{V_d}{2} \tag{61}$$

So the modulation signal is reported in (62) if the value of M is considered maximum 1.

$$\hat{k}(t) = \frac{2\sqrt{2}V}{V_d}\sin(\omega_0 t - \varphi)\,,\ M = \frac{2\sqrt{2}V}{V_d} \tag{62}$$

The power balance in (59) is considered between the AC and the DC side to carry out the current waveform. The relationship between the AC and the DC currents is performed if the AC voltage amplitude in (62) is considered. The current waveform is shown in Figure III-7 by employing the single cell for an MMC structure.

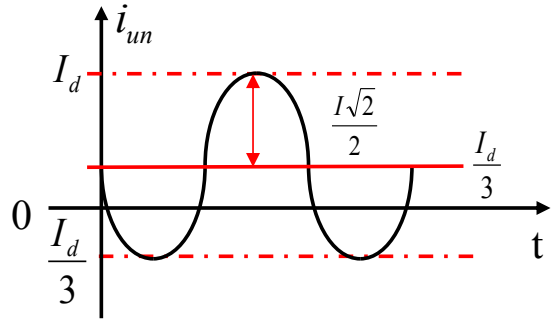


Figure III-7: Averaged current waveform if the single cell is considered

$$I_d = \frac{3}{4}M\sqrt{2}I\cos(\varphi) \tag{63}$$

This balance is also necessary to ensure a constant dc voltage across the capacitor. The right power balance also indicates a constant voltage capacitor in the cell and therefore the right energy balance in the branch.

III.1.2 Asymmetrical H-bridge

This topology guarantees the bipolar voltage, but it can only conduct a unidirectional current. The considered circuit is shown in Figure III-8.

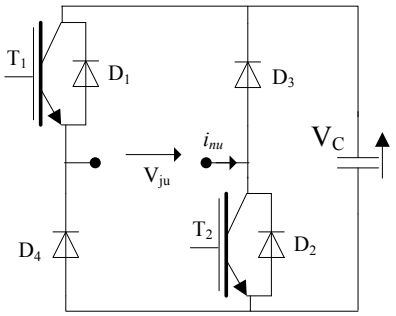


Figure III-8: Asymmetrical H-bridge topology

- Bi-polar voltage
- Monodirectional current

For this topology, the branch current has to be kept as expressed in (64). This condition leads to a balance between the AC and DC components of the currents carried out in (65).

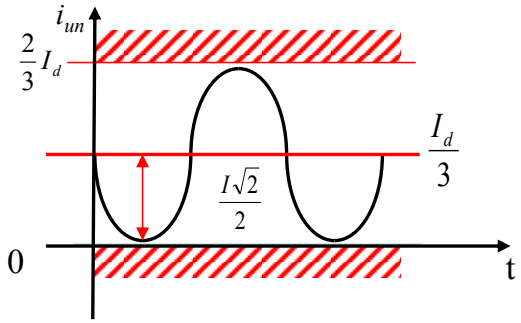


Figure III-9: Averaged current waveform if Asymmetrical H-converter is considered

$$i_{un}(t) = \frac{I_d}{3} + \frac{\sqrt{2}}{2} I \sin(\omega_0 t + \varphi) \geq 0 \qquad (64)$$

$$\frac{3}{2} I\sqrt{2} \leq I_d \qquad (65)$$

The choice of a current with a high DC component increases the rms value. This means an oversizing of the semiconductor devices. To optimize the semiconductor choice, the balance (65) is chosen so that the DC component is equal to the AC one. Under this condition, by substituting (65) in the power balance (60), the relationship between the AC and DC voltages is achieved in (66). This means that the use of the asymmetrical HB-topology is not suggested for reactive power compensations because of the high DC link voltage levels required. Then, the following study was performed only with the unit power factor.

$$\hat{V} = \frac{V_d}{\cos\varphi} \qquad (66)$$

The voltages imposed by each branch are expressed by (67) where N is the number of elementary converters per branch. The total number of elementary converters has to be chosen according to (68) where f is the modulation signal.

$$\begin{aligned} v_{un}(t) &= N \cdot \hat{V}_{ju} = \frac{V_d}{2} - V_d \sin(\omega_0 t) \\ v_{up}(t) &= N \cdot \hat{V}_{ju} = \frac{V_d}{2} + V_d \sin(\omega_0 t) \end{aligned} \tag{67}$$

$$\begin{aligned} \hat{f}(t)_n &= \frac{V_d}{NV_C}\left(\frac{1}{2} - \sin(\omega_0 t)\right) \\ \hat{f}(t)_p &= \frac{V_d}{NV_C}\left(\frac{1}{2} + \sin(\omega_0 t)\right) \end{aligned}, \quad M = \frac{V_d}{N \cdot V_C} \tag{68}$$

To ensure a linear SPWM modulation the peak value of *f(t)* has to be less than 1. The ratio between the number of elementary converters and the DC voltage is carried out in (69).

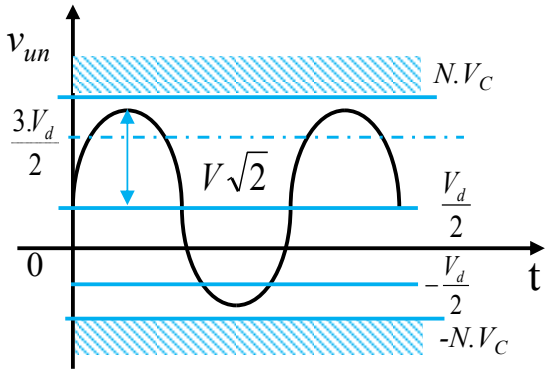


Figure III-10: Averaged voltage waveform if asymmetrical H-bridge topology

$$N \cdot V_C \geq \frac{3}{2} V_d, \tag{69}$$

In this case, the voltage level NV_C , which enables the system to reach the maximum amplitude of the branch voltage, is 1.5 times that of the DC voltage. This means a 50% increase for the number of elementary converters per branch with respect to the employment of the simple cell. On the other hand, considerations on the sizing capacitor make this topology more attractive.

III.1.2.1 The capacitor of the Asymmetrical H topology and the AC current

The voltage imposed by the Asymmetrical H-topology is double that of the simple one. By fixing the values of the DC voltage and the system power rate, the active power is provided for the single elementary converter (70) and for the asymmetrical H bridge topology (71). In the comparison between the two powers in (72), it is shown that, if the asymmetrical H bridge

topology is employed, half of the current is necessary to achieve the same power, also decreased by M.

$$P_{AC} = \frac{3}{2\sqrt{2}} M_{SC} \cdot V_d \cdot I_{SC} \tag{70}$$

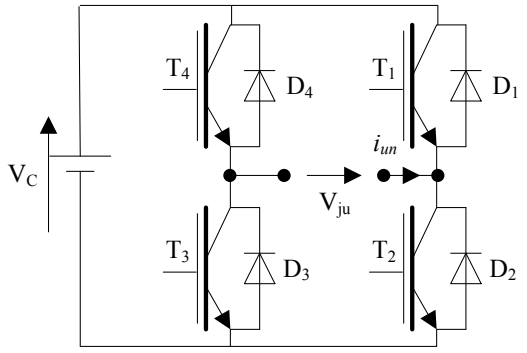
$$P_{AC} = \frac{3}{\sqrt{2}} V_d \cdot I_{AH} \tag{71}$$

The amplitude of the voltage ripple on the capacitors depends on the AC current (48). Thus, to achieve the same amplitude of voltage ripple, at parity of capacitor voltage of the elementary converter, less than half of the capacitance is necessary in terms of single cell use (72).

$$I_{AH} = M_{SC} \frac{I_{SC}}{2} \rightarrow C_{AH} = M_{SC} \frac{C_{SC}}{2} \tag{72}$$

III.1.3 H-bridge

The so-called four-quadrant converter can manage the bi-directional propriety in the current of the single cell, and it can impose a bi-polar voltage as the asymmetrical H-bridge topology. On the other hand, the H-bridge topology requires double the components of the others, four transistors and four diodes, as depicted in Figure III-11.



- Bi-polar voltage
- Bi-directional current

Figure III-11: H-bridge topology

In (73) the voltage condition to respect is reported. The equivalent sum of the output voltages waveform is highlighted in Figure III-12.

$$\frac{V_d}{2} < V\sqrt{2} \tag{73}$$

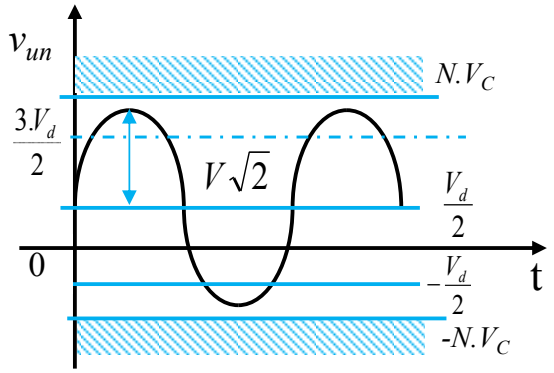


Figure III-12: Averaged output voltage of the H-bridge converter

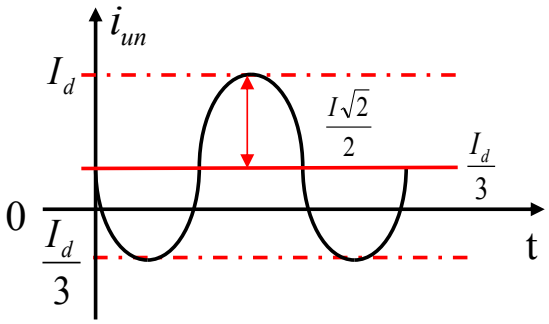


Figure III-13: Averaged current waveform in the H-bridge converter

In (74), the current condition's waveform is highlighted in Figure III-12.

$$\frac{I\sqrt{2}}{2} \le \frac{2}{3} \cdot \frac{I_d}{\cos\varphi} \tag{74}$$

Under ordinary operative conditions, the H-bridge structure is not necessary for the MMC systems. On the other hand, if this cell is configured like a single cell, the bi-polarity can be used in the case of DC fault, which is addressed in the chapter V.

III.2 Efficiency for multilevel structure

Regarding the power level, 1% of losses is not negligible (1 GW correspond to 10 MW of losses). For this reason many semiconductor producers consider efficiency as an 'alternative fuel'. Thus, the power losses evaluation is not a secondary problem. The monitoring of the losses becomes more attractive for high-voltage applications when the number of devices is very high.

In this chapter, the modular multilevel structure is studied in terms of efficiency. An investigation on the power losses in semiconductor devices is carried out by taking into account the previously described cells. An analytical approach was given for each case. After fixing the nominal power and the DC voltage for the converter, the efficiency of the system is evaluated for each kind of employed cell. The analytical results are validated by simulations performed by PSIM software.

III.2.1 The analytical approach

A three-phase balanced operation is assumed and then only one elementary converter is considered. The current in the devices should be carefully determined and the definition of the conduction intervals is fundamental to evaluate conduction and switching losses [52]-[55]. Conduction losses (76) are evaluated by considering a piece-wise linear approximation of the forward characteristic (75) r_0 is on state resistance and V_0 the voltage threshold) [56]. Averaged and RMS values are calculated according to expressions (77) and (78) where α is the duty cycle of the control signal. Assuming $\theta=\omega_0 t$, θ_2-θ_1 is the conduction angle of the devices.

$$V_{T/D} = r_{T/D0} I_C + V_{T/D0} \tag{75}$$

$$P_{T/D}^{cond} = r_{T/D0} \left(I_{T/D}^{rms} \right)^2 + V_{T/D0} I_{T/D}^{avg} \tag{76}$$

$$I_{D/T}^{avg} = \frac{1}{2\pi} \int_{\theta_1}^{\theta_2} i(t)\alpha(t) d\theta \tag{77}$$

$$I_{T_1}^{rms} = \sqrt{\frac{1}{2\pi} \int_{\theta_1}^{\theta_2} i(t)^2 \alpha(t) d\theta} \tag{78}$$

For the calculation of the switching losses, we considered, for the energy curves given by the manufacturer datasheets, a second order approximation [56]. Coefficients a_{dev}, b_{dev} and c_{dev} in (79) come from this approximation.

$$P_{T/D}^{sw} = \frac{f_{sw}}{2\pi} \int_{\theta_1}^{\theta_2} \left(a_{dev} \cdot i^2(t) + b_{dev} \cdot i(t) + c_{dev} \right) \cdot \frac{V_i}{V_{ref}} d\theta \tag{79}$$

Conduction and switching losses extracted in this section suppose a commutation frequency much higher than the fundamental frequency [56].

III.2.2 System rating

In Table III-1 the nominal power and the devices are defined. Moreover from the semiconductor datasheet the linear coefficients of the conduction curve and the coefficients of second order of the energy curve are shown. The number of cells, AC output current and voltages are extracted according to the cell topology chosen for the system.

Table III-1: Case study

POWER CONVERTER S = 100 MVA	
DC voltage V_d	160 kV
Cell voltage	2.5 kV
Switching frequency f_{sw} = 200 Hz	
IGBT COEFFICIENTS @ V_{CC}=2.8 kV	
TRANSISTOR TOSHIBA"S6X06B"	**DIODE EUROPEC "D 1331 SH"**
r_{T0}=1.3mΩ; V_{T0}=1.5 V	r_{D0}=1.3mΩ; V_{D0}=1.1V
$a_{on}+a_{off}$=-15n; $b_{on}+b_{off}$=12.1m; $c_{on}+c_{off}$=-2.4m	a_{rec}=-2μ; b_{rec}=5.2m c_{rec}=0.57

III.2.3 Single cell& Full H-Bridge

The performed study is valid for both the single and for the full H-bridge cell. This last one in ordinary conditions is configured like a single cell. The bipolar voltage is provided only for faulty conditions. The losses of both the switching and conduction depend on the duty cycle and on the current in the device. The RMS and the average values of the current in the devices are carried out in this section.

III.2.3.1 Current calculation

As it was shown in Figure III-14, for the study the negative branch is chosen. All capacitor voltages are considered with a constant value $V_C=V_d/N$ moreover for the current we consider a waveform without ripple at the switching frequency. For the H-bridge cell (Figure III-15), in normal operation, the device 3 is always on while the device 4 is always off. In terms of power losses, devices 1 and 2 are analyzed according to the analytical method adopted for the simple cell. In normal condition the device 4 is always opened while the device 3 conducts always without commutations.

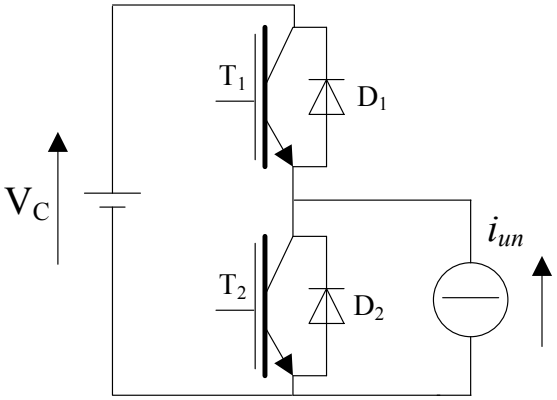


Figure III-14: Single cell configuration

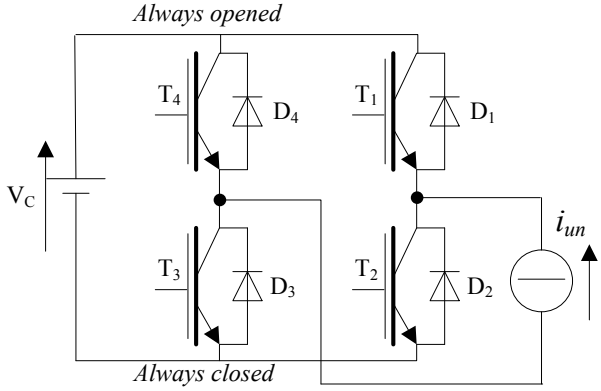


Figure III-15: H-bridge configuration

The duty cycle is given by (80).

$$\alpha_n(t) = \frac{1-k(t)}{2} \;;\; \alpha_p(t) = 1-\alpha_n(t) \tag{80}$$

In Figure III-16, the modulation signal *f(t)* and the current in a cell of the negative branch i_{nu} (46) are reported. Due to the current waveforms, the conduction interval of the devices depend on the sign of cos(φ). The DC component of the current determines different losses between the two switches of the cell.

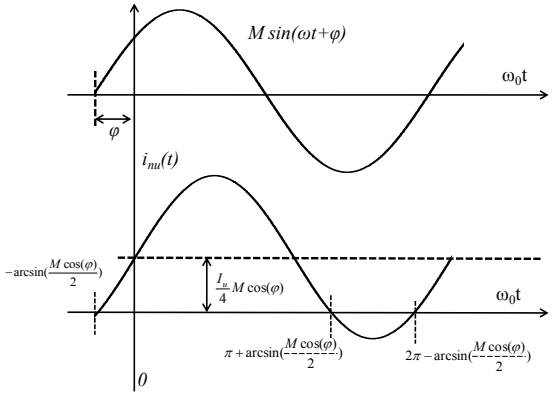


Figure III-16: Modulation signal and cell current

TABLE III-2 – Conduction intervals of the devices

Dev.	Conduction Interval $[\theta_1 ; \theta_2]$	Current	Mod. index
T_1	$[\pi+asin(Mcos(\varphi)/2) ; 2\pi-asin(Mcos(\varphi)/2)]$	$i_{un}(t)$	$\alpha_n(t)$
D_1	$[-asin(Mcos(\varphi)/2); \pi+asin(Mcos(\varphi)/2)]$	$i_{un}(t)$	$\alpha_n(t)$
T_2	$[-asin(Mcos(\varphi)/2); \pi+asin(Mcos(\varphi)/2)]$	$i_{un}(t)$	$\alpha_p(t)$
D_2	$[\pi+asin(Mcos(\varphi)/2) ; 2\pi-asin(Mcos(\varphi)/2)]$	$i_{un}(t)$	$\alpha_p(t)$

TABLE III-2 gives for each device the conduction interval and the associated current. The current averaged values were evaluated by solving integrals (77) and (78) according to TABLE III-2. The results are given in expressions (81), (82) and (83).

$$I_{T_1}^{avg} = I_{D_1}^{avg} = \frac{I_1}{16\pi}\left(4 - M^2\cos^2(\varphi)\right)\sqrt{1-\frac{M^2\cos^2(\varphi)}{4}} \tag{81}$$

$$I_{T_2}^{avg} = \frac{I_1}{16\pi}\left[\begin{array}{l}\left(4+\mathrm{M}^2\cos^2\varphi\right)\sqrt{1-\dfrac{M^2\cos^2(\varphi)}{4}}+ \\ 2M\cos(\varphi)\cdot\left(2\cdot a\sin\left(\dfrac{M\cos(\varphi)}{2}\right)+\pi\right)\end{array}\right] \tag{82}$$

$$I_{D_2}^{avg} = \frac{I_1}{16\pi}\left[\begin{array}{l}\left(4+\mathrm{M}^2\cos^2\varphi\right)\sqrt{1-\dfrac{M^2\cos^2(\varphi)}{4}}+ \\ 2M\cos(\varphi)\cdot\left(2\cdot a\sin\left(\dfrac{M\cos(\varphi)}{2}\right)-\pi\right)\end{array}\right] \tag{83}$$

In a similar way, integral (78) allows calculating current RMS value for each device. The results are given from expression (84) to expression (87)

$$I_{T_1}^{rms} = \frac{I_1}{4}\sqrt{\frac{1}{12\pi}\left\{\begin{array}{l} 6\pi + \left(6M^2\cos^2\varphi - 12\right)\cdot a\sin\left(\frac{M}{2}\cos(\varphi)\right) + \\ \left(2M^3\cos^3\varphi - 2M\cos(\varphi)\right)\cdot\sqrt{1-\frac{M^2\cos^2\varphi}{4}} - \\ 3M^2\pi\cos^2(\varphi) \end{array}\right\}} \tag{84}$$

$$I_{D_1}^{rms} = \frac{I_1}{4}\sqrt{\frac{1}{12\pi}\left\{\begin{array}{l} 6\pi - \left(6M^2\cos^2\varphi - 12\right)\cdot a\sin\left(\frac{M}{2}\cos(\varphi)\right) - \\ \left(2M^3\cos^3\varphi - 2M\cos(\varphi)\right)\cdot\sqrt{1-\frac{M^2\cos^2\varphi}{4}} - \\ 3M^2\pi\cos^2(\varphi) \end{array}\right\}} \tag{85}$$

$$I_{T_2}^{rms} = \frac{I_1}{4}\sqrt{\frac{1}{12\pi}\left\{\begin{array}{l} 6\pi + \left(12+18M^2\cos^2\varphi\right)\cdot a\sin\left(\frac{M}{2}\cos(\varphi)\right) + \\ \left(2M^3\cos^3\varphi + 34M\cos(\varphi)\right)\cdot\sqrt{1-\frac{M^2\cos^2\varphi}{4}} + \\ 9M^2\pi\cos^2(\varphi) \end{array}\right\}} \tag{86}$$

$$I_{D_2}^{rms} = \frac{I_1}{4}\sqrt{\frac{1}{12\pi}\left\{\begin{array}{l} 6\pi - \left(12+18M^2\cos^2(\varphi)\right)\cdot a\sin\left(\frac{M}{2}\cos(\varphi)\right) - \\ \left(34M\cos(\varphi) + 2M^3\cos^3\varphi\right)\cdot\sqrt{1-\frac{M^2\cos^2\varphi}{4}} + \\ 9M^2\pi\cos^2(\varphi) \end{array}\right\}} \tag{87}$$

$$g_1 = \frac{1}{2\pi}\int_{-a\sin\left(\frac{M|\cos\varphi|}{2}\right)}^{\pi+a\sin\left(\frac{M|\cos\varphi|}{2}\right)}\left(a_{dev}\cdot i^2(t) + b_{dev}\cdot i(t) + c_{dev}\right)\cdot\frac{V_C}{V_{ref}}d\theta =$$

$$= \left[\begin{array}{l} a_{dev}\frac{I_1^2}{16}\left(\begin{array}{l} 2\pi - \left(4+2M^2\cos^2\varphi\right)\cdot\left|a\sin\left(\frac{M}{2}\cos(\varphi)\right)\right| - \\ 6M\left|\cos(\varphi)\right|\cdot\sqrt{1-\frac{M^2\cos^2\varphi}{4}} + M^2\pi\cos^2(\varphi) \end{array}\right) + \\ b_{dev}\frac{I_1}{4}\left(2M\cos(\varphi)\cdot a\sin\left(\frac{M}{2}\cos(\varphi)\right) + 4\sqrt{1-\frac{M^2\cos^2\varphi}{4}} - M\pi\left|\cos(\varphi)\right|\right) + \\ c_{dev}\left(\pi - 2\cdot\left|a\sin\left(\frac{M}{2}\cos(\varphi)\right)\right|\right) \end{array}\right]\frac{V_C}{V_{ref}} \tag{88}$$

$$g_2 = \frac{1}{2\pi}\int_{\pi+a\sin\left(\frac{M|\cos\varphi|}{2}\right)}^{2\pi-a\sin\left(\frac{M|\cos\varphi|}{2}\right)}\left(a_{dev}\cdot i^2(t) + b_{dev}\cdot i(t) + c_{dev}\right)\cdot\frac{V_C}{V_{ref}}d\theta = \tag{89}$$

$$\begin{bmatrix} a_{dev}\dfrac{I_1^2}{16}\left(\begin{matrix}2\pi+\left(4+2M^2\cos^2\varphi\right)\cdot\left|a\sin\left(\dfrac{M}{2}\cos(\varphi)\right)\right|+\\ 6M\left|\cos(\varphi)\right|\cdot\sqrt{1-\dfrac{M^2\cos^2\varphi}{4}}+M^2\pi\cos^2(\varphi)\end{matrix}\right)+ \\ b_{dev}\dfrac{I_1}{4}\left(2M\cos(\varphi)\cdot a\sin\left(\dfrac{M}{2}\cos(\varphi)\right)+4\sqrt{1-\dfrac{M^2\cos^2\varphi}{4}}+M\pi\left|\cos(\varphi)\right|\right)+\dfrac{V_C}{V_{ref}} \\ c_{dev}\left(\pi+2\cdot\left|a\sin\left(\dfrac{M}{2}\cos(\varphi)\right)\right|\right) \end{bmatrix}$$

$$P_{T_1}^{sw}=\frac{f_{sw}}{2\pi}g_2\wedge\begin{cases}a_{dev}=a_{on}+a_{off}\\ b_{dev}=b_{on}+b_{off}\\ c_{dev}=c_{on}+c_{off}\end{cases}\ P_{D_1}^{sw}=\frac{f_{sw}}{2\pi}g_1\wedge\begin{cases}a_{dev}=a_{rec}\\ b_{dev}=b_{rec}\\ c_{dev}=c_{rec}\end{cases} \tag{90}$$

$$P_{T_2}^{sw}=\frac{f_{sw}}{2\pi}g_1\wedge\begin{cases}a_{dev}=a_{on}+a_{off}\\ b_{dev}=b_{on}+b_{off}\\ c_{dev}=c_{on}+c_{off}\end{cases}\ P_{D_2}^{sw}=\frac{f_{sw}}{2\pi}g_2\wedge\begin{cases}a_{dev}=a_{rec}\\ b_{dev}=b_{rec}\\ c_{dev}=c_{rec}\end{cases} \tag{91}$$

$$P_{T_1}^{sw}=\frac{f_{sw}}{2\pi}g_2\wedge\begin{cases}a_{dev}=a_{on}+a_{off}\\ b_{dev}=b_{on}+b_{off}\\ c_{dev}=c_{on}+c_{off}\end{cases}\ P_{D_1}^{sw}=\frac{f_{sw}}{2\pi}g_1\wedge\begin{cases}a_{dev}=a_{rec}\\ b_{dev}=b_{rec}\\ c_{dev}=c_{rec}\end{cases} \tag{92}$$

$$P_{T_2}^{sw}=\frac{f_{sw}}{2\pi}g_1\wedge\begin{cases}a_{dev}=a_{on}+a_{off}\\ b_{dev}=b_{on}+b_{off}\\ c_{dev}=c_{on}+c_{off}\end{cases}\ P_{D_2}^{sw}=\frac{f_{sw}}{2\pi}g_2\wedge\begin{cases}a_{dev}=a_{rec}\\ b_{dev}=b_{rec}\\ c_{dev}=c_{rec}\end{cases} \tag{93}$$

The unsymmetrical current waveform makes the calculation more complicated compared to a classical Voltage Source Inverter. Knowing the RMS and averaged values of the currents the conduction losses can be easily evaluated considering expression (76). Switching losses are calculated by considering integral (79) and conduction intervals depicted in TABLE III-2. It is possible to define functions g_1 and g_2 as reported in (88) and (89). Nevertheless, switching losses change according to the sign of $cos(\varphi)$ as it is shown in expressions (90) to (93).

III.2.3.2 Case study

The power losses evaluation was performed in different operating modes: inverter and rectifier at unit power factor and reactive power compensation. By keeping the same semiconductor devices, analytical calculations were validated by PSIM software. According to the analysis of the cell topology, the parameters in TABLE III-3 are extracted to carry out the power required by the system (Table III-1).

I_u [rms]	693 A
V_{ll} [rms]	83 kV
α_{MAX}	0.925
N	64

TABLE III-3 – system parameters if the single cell or the H-bridge cell are used

III.2.3.3 Results for Single Cell

As it is shown in Figure III-17 and Figure III-18, in the unit power factor operation the MMC presents a strong dispersion of the power losses between the devices as expected from the previous section. In the reactive power compensation, the currents in the branches of the MMC become symmetrical and the losses calculation is then equivalent to a classical VSI, moreover the inductor case is the same of the capacitor case (Figure III-19).

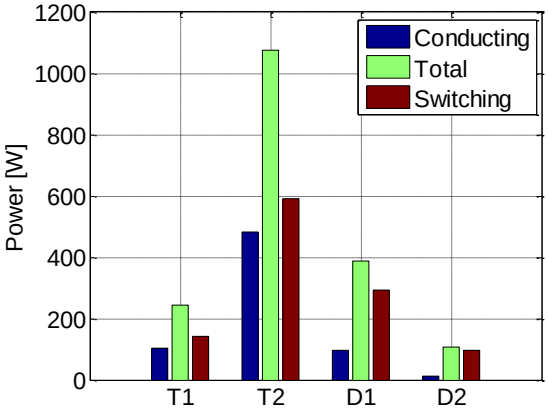


Figure III-17: Cell power losses for MMC in Inverter operating mode

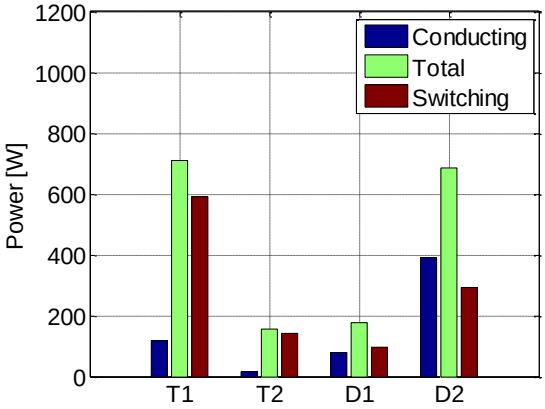


Figure III-18: Cell power losses for MMC in Rectifier operating mode

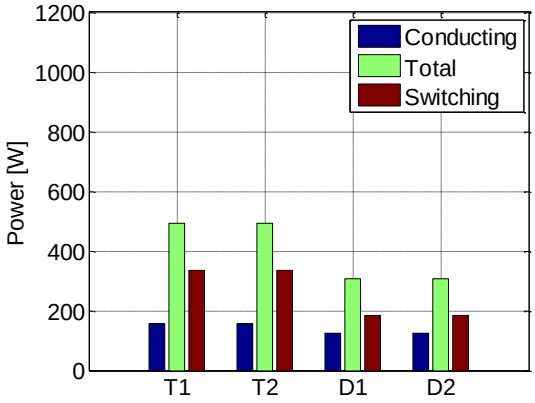


Figure III-19:Cell power losses for MMC in reactive operating mode

III.2.3.4 Results for the full H-bridge

Analytical results are reported in Figure III-20 to Figure III-22. For the switching devices 1 and 2 the power losses evaluation was performed as in the elementary cell. Just conduction losses for S_3 are added.

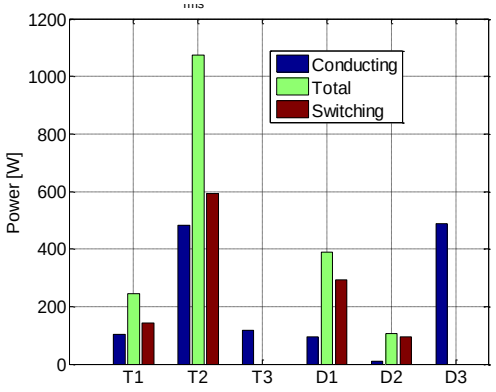


Figure III-20: Cell power losses for MMC in Inverter operating mode

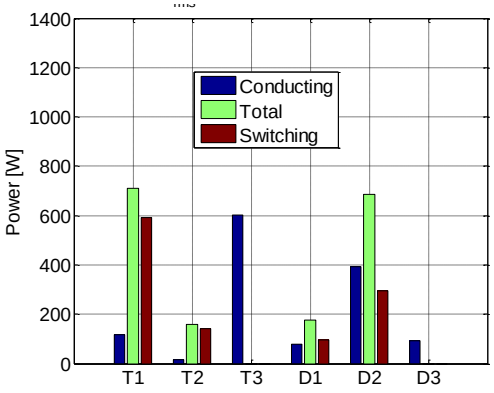


Figure III-21: Cell power losses for MMC in Rectifier operating mode

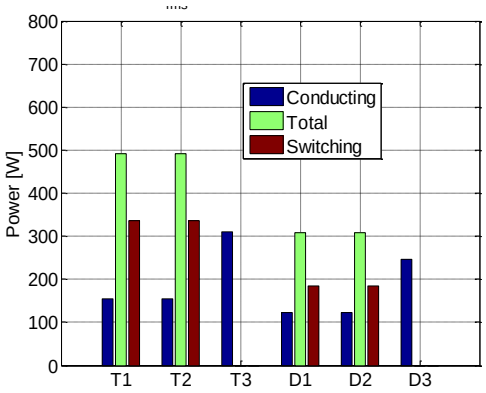


Figure III-22: Cell power losses for MMC in reactive operating mode

The addition of semiconductor devices makes the full H-bridge more expensive in terms of losses. For this reason an investigation on the total losses of this cell respect to the simple cell was carried out. In Figure III-23 and Figure III-24 the increases are shown.

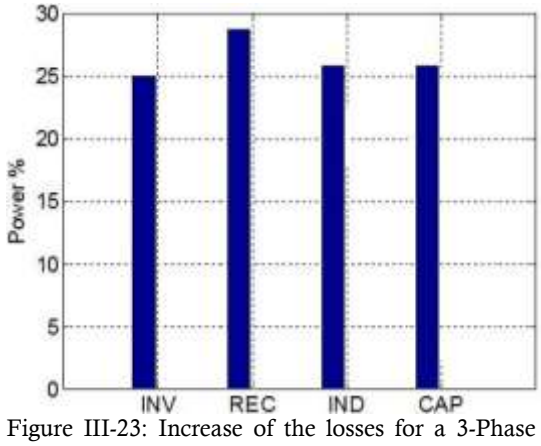


Figure III-23: Increase of the losses for a 3-Phase system by using full H bridge cells respect to a classical system

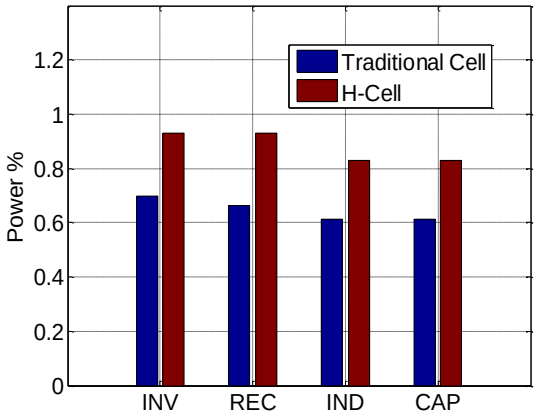


Figure III-24: Total losses comparison for a 3-phase system by considering the classical cell and the full H bridge cell

III.2.4 Asymmetrical H-Bridge

With respect to the previous topologies, the asymmetrical H-Bridge solution shows different current waveforms in semiconductor devices and different modulation ratios.

Due to the symmetry, just the negative branch is considered; the reference circuit is reported in Figure III-25. The current has only one direction as in (94). For this reason, diodes D_1 and D_2 in nominal operating condition are not used. For each pair of devices, in (95) and (96) are reported the modulation ratio necessary for the calculation of RMS and average currents.

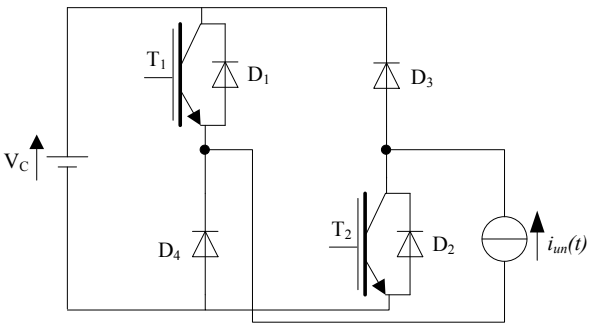


Figure III-25: Asymmetrical H-Bridge employed for the negative branch

$$i_{un}(t) = \frac{\hat{I}}{2}\left(1+\sin(\omega_0 t)\right) \quad (94)$$

$$\alpha_n(t) = \frac{1}{2}\left[1+M\left(\frac{1}{2}-\sin(\omega_0 t)\right)\right] \quad D_3,D_4 \quad (95)$$

$$\alpha_n'(t) = 1-\alpha_n'(t) = \frac{1}{2}\left[1-M\left(\frac{1}{2}-\sin(\omega_0 t)\right)\right] \quad (96)$$

T_1,T_2

III.2.4.1 Current calculation

According to (77), the average value of the devices is extracted in (97), while the RMS values are reported in (98) and (99). According to the current direction, shown in Figure III-25, only T_1, T_2, D_3 and D_4 are conducting.

$$I_{D/T}^{avg} = \frac{1}{2\pi}\int_0^{2\pi} i_{un}(t)\cdot\alpha(t)d\theta = \frac{\hat{I}}{4} \tag{97}$$

$$I_{D}^{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_{un}^2(t)\cdot\alpha_n(t)d\theta} = \frac{\hat{I}}{2}\sqrt{\frac{1}{2}\cdot\left(\frac{3}{2}-\frac{M}{4}\right)} \tag{98}$$

$$I_{T}^{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_{un}^2(t)\cdot\alpha_n^{'}(t)d\theta} = \frac{\hat{I}}{2}\sqrt{\frac{1}{2}\cdot\left(\frac{3}{2}+\frac{M}{4}\right)} \tag{99}$$

According to (78) the switching losses can be expressed by (100).

$$P_{sw}^{T/D} = f_{sw}\cdot\left[a\cdot\frac{3}{8}\hat{I}^2 + b\cdot\frac{\hat{I}}{2} + c\right]\cdot\frac{V_C}{V_{CC}} \tag{100}$$

To calculate the total losses, an equivalent case study with same power rating and same DC voltage level was considered (see Table III-1). According to the asymmetrical H-bridge properties, the AC voltage value is increased with respect to a topology using simple cells (66).

III.2.4.2 Results

As we said before, the power losses evaluation was performed only for a unit power factor. By keeping the same semiconductor devices and ratings (Table III-1), analytical calculations were validated by PSIM software by making rating adaptations in TABLE III-4 due to this kind of topology.

I_u [rms]	295 A
V_{ll} [rms]	121 kV
α_{MAX}	0.925
V_C	2.5 kV
N	113

TABLE III-4 – System parameters

Losses for this elementary converter are balanced between the components as shown in Figure III-26. Of course the total losses are the double (Figure III-27) respect to the single cells due to the number of elementary converters necessary for the employment of this topology.

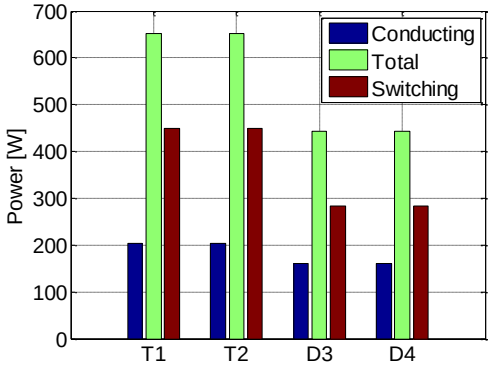


Figure III-26: Single elementary converter losses

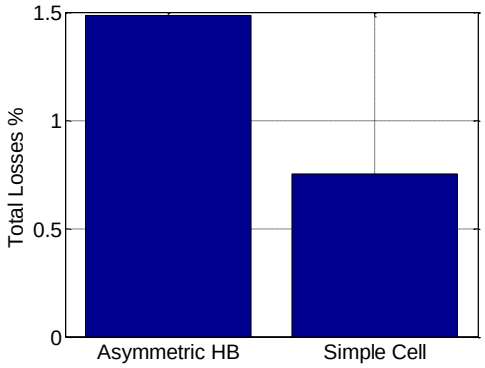


Figure III-27: Total losses percentage comparison with the single cell

III.3 Conclusions

The MMC structure by Professor R. Marquardt is based on single-cell topologies. This cell cannot impose negative voltages; thus, in the case of DC faults, only the branch inductor can limit the current. The asymmetrical H-bridge topology needs the same number of devices per elementary converter. It can impose a bi-polar voltage that better limits the over-currents in faulty conditions. Moreover, at the parity of power sizing and capacitor voltage, this topology allows a reduced value of the capacitance. On the other hand, the number of elementary converter is around the double rather than the single cell use; moreover, this topology is not suitable for reactive power compensations. Of course this topology can be employed for CSC based applications where the power reversibility is achieved with the DC voltage reversibility. If the four-quadrant operation is required with a good limitation of over-currents, then the use of the H-bridge cell is suggested. Moreover, this cell causes the MMC structure not to depend on the voltage and current levels; this aspect is well consolidated in the next section. Of course, the employment of double the components increases the costs. The power reversibility with this topology can be achieved with both the DC voltage and the DC current.

The analytical power losses study makes the evaluation fast and direct. It was not easy to carry out the formulas due to the DC component in the device's current. If the DC voltage value is maintained, the Asymmetrical H-bridge is not so convenient in terms of power losses, despite the lower RMS AC current. This is because, in the Asymmetrical H-bridge, each device conducts during the whole period. Nevertheless, if this cell is employed, a reduced capacitor value can be achieved. Finally, the 25% increasing losses with respect to the single-cell employment is not acceptable for the HVDC employments which usually require almost 1% of the total losses (including losses in the reactive elements). For many other applications with a relatively reduced power the full H-bridge topology is recommended, because it can be employed like a single cell in ordinary operating conditions, and it can limit the current in faulty operating conditions.

III.4 New Modular Multilevel Half Wave topology with zigzag transformer

As shown previously, each branch of the MMC structure has a DC and AC component in the voltage and current. The combination of two branches per phase makes possible the right power transferring of the two components according to the assumptions made in the previous chapter and the circuit diagrams given in Figure III-3 and Figure III-4.

The proposed structure requires just the upper part of the MMC structure as shown in Figure III-28. This configuration absorbs on the AC side currents with a DC zero sequence. To avoid the saturation of the magnetic core a secondary winding with a zig-zag configuration is used [57]-[58]. Thanks to this coupling, secondary voltages are balanced while the DC zero sequence current is canceled on the primary side.

On each phase, several DC/AC cells (converters) are connected in series. Output currents i'_u ,i'_v and i'_w are imposed by three independent control loops which provide a Pulse Width Modulation to the DC/AC converters (101). The phase voltage is chosen according to (102)

$$i'_u = \frac{I_d}{3} + \hat{I}\cos(\omega_0 t - \varphi)\ ;\quad i'_v = \frac{I_d}{3} + \hat{I}\cos(\omega_0 t - \varphi - \frac{2}{3}\pi)\ ; i'_w = \frac{I_d}{3} + \hat{I}\cos(\omega_0 t - \varphi + \frac{2}{3}\pi) \tag{101}$$

$$v'_u(t) = \hat{V}\sin(\omega_0 t) \tag{102}$$

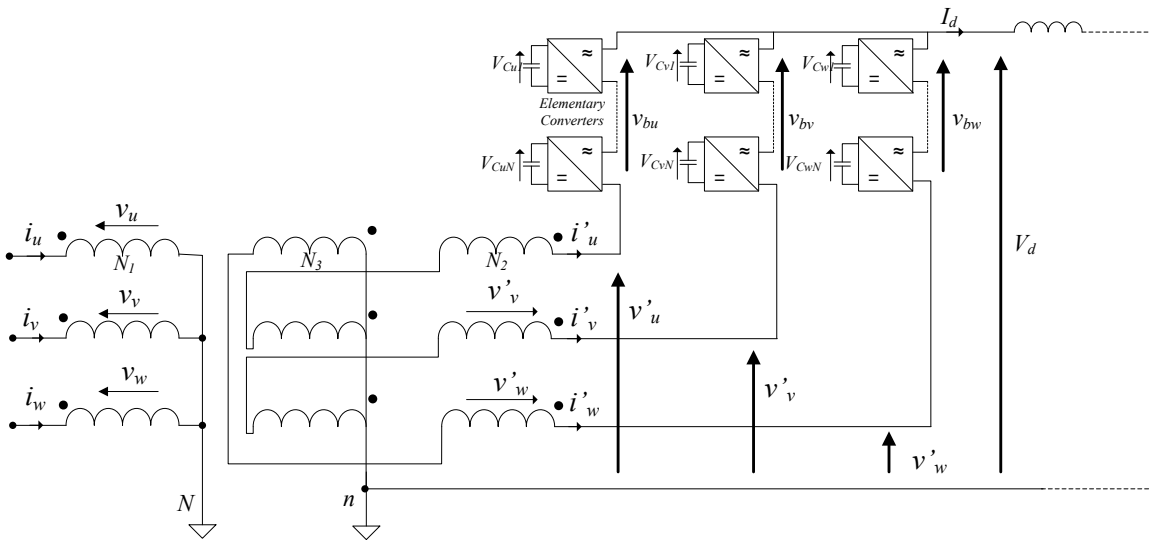


Figure III-28 – Upgraded AC/DC converter

From Figure III-28 the averaged model presented in Figure III-29 is developed and valid at the fundamental frequency. By neglecting the voltage drop across the leakage inductor of the transformer L_S, voltage $\overline{V}_{bu}$ can be expressed by (103).

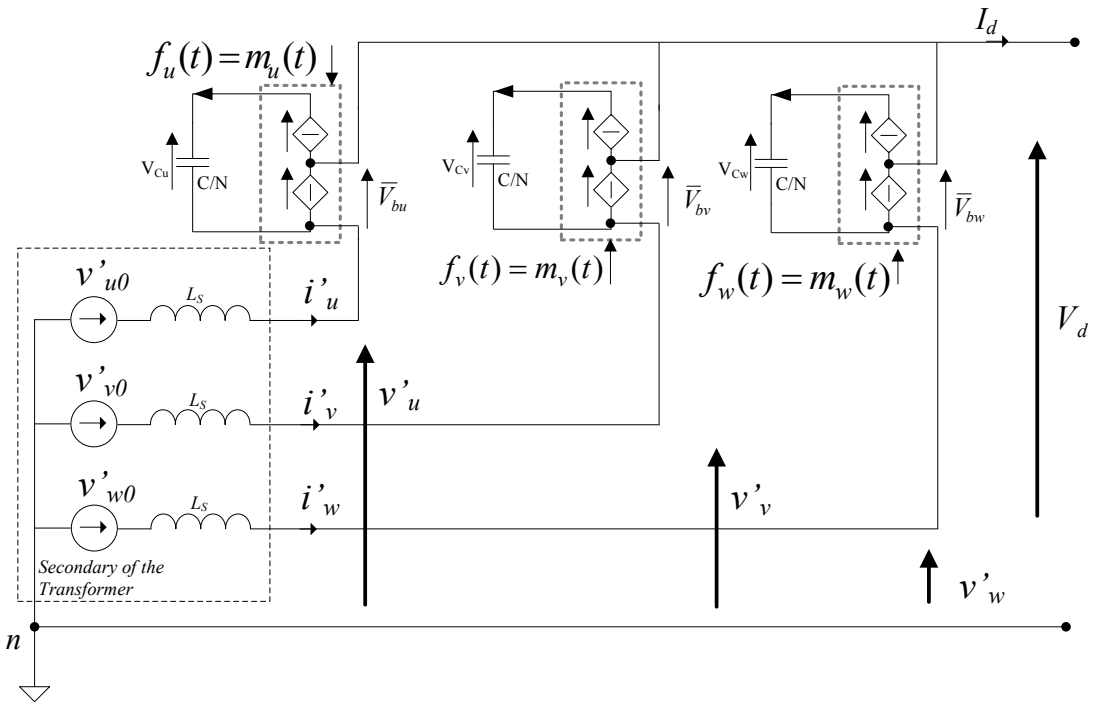


Figure III-29 - Simplified circuit on the AC side with averaged model of the Half Wave multilevel converter

$$\overline{V}_{Bu}(t) \approx V_d - \hat{V}\sin(\omega_0 t) \tag{103}$$

Each elementary converter has to conduct the third part of the DC current and the AC current necessary to achieve the power required if a unitary transformation ratio is provided for the zig-zag transformer.

By considering the same capacitor voltages V_C and the same DC current, if V_d is the DC voltage for the traditional structure a fast comparison in terms of sizing can be achieved for the same cell topology (Single Cell). Moreover for the zig-zag transformer a unitary transformation ratio N_1/N_2 is chosen.

The voltage imposed by each branch is evaluated in (108) to keep a unipolar voltage; the modulation signal is so extracted in (109).

$$\overline{V}_{Bu}(t) \approx V_d \cdot \left(1-\sin(\omega_0 t)\right) \tag{104}$$
$$\widehat{f}(t)\cdot N \cdot V_C = V_d\left(1-\sin(\omega_0 t)\right) \tag{105}$$

The sizing comparison in Table III-5 highlights that for the modular multilevel Half Wave the double of the cells per phase are necessary respect to the classical MMC. The sources V_{bx} in

fact have to sustain all the DC voltage. Moreover the half of the current is imposed on the AC side because the AC voltage is the double respect to the classical MMC structure.

	MMC	Multi HW with zig-zag	Ratio Multi HW/MMC
Number of cells	$2.N = 2.\frac{V_d}{V_C}$	$N = 2.\frac{V_d}{V_C}$	1
AC rms voltage	$V = M.\frac{V_d}{2\sqrt{2}}$	$V = M.\frac{V_d}{\sqrt{2}}$	2
AC rms current	$I = \frac{P}{3.V}$	$I = \frac{P}{3.V}$	½

Table III-5: Comparison on the sizing of the classical MMC structure and the Multilevel Active Front End

In many cases the new structure can be used to replace systems where there is a pre-existent zig-zag configuration such as the application chosen as case study in the next section.

III.4.1 3 MMC Half Wave topology to upgrade obsolete diode/thyristor rectifiers

In this section a particular association of AC/DC multilevel converters is proposed to update classical 3-pulse diode or thyristor rectifiers. The approach is made by keeping the pre-existing transformer and voltage values both on the AC and DC side.

The use of 3-pulse diode or thyristor rectifiers can be considered one of the first structures to achieve a AC/DC conversion. In literature, it is well known that the simplicity of this topology leads to a series of drawbacks [59].

Due to current waveforms show on the AC side, these rectifiers present a poor power factor. Due to severe constraints on Power Quality, these kinds of topologies are associated to harmonic filters which increase the complexity of the conversion system [60]. Moreover half wave rectifiers show a DC current component on the three phase currents that influences the transformer rating. At this effect, a transformer with a zigzag coupling can be used [59].

Nowadays, in the frame of Medium and High Power applications, new requirements on power quality lead to draw a quasi-sinusoidal current waveform with a four quadrant operation. For this reason, classical diode/thyristor rectifiers are obsolete and should be replaced. With the view to save money, it is necessary to update the traditional topology by keeping the same transformer and the same output voltage level. Nevertheless, active front end solutions based on multilevel voltage source inverters [61] are not suitable to control the DC voltage in the same conditions as a thyristor rectifier (the average output voltage is always lower than the input voltage).

III.4.1.1 Three phase half wave rectifier

The 3 pulse bridge rectifier presented in Figure III-30 absorbs on the AC side currents with a DC zero sequence as shown in Figure III-31-a [62].To avoid the saturation of the magnetic core a secondary winding with a zig-zag configuration is used [57]-[58]. Thanks to this coupling, secondary voltages are balanced while the DC zero sequence current is canceled on the primary side as it is shown in Figure III-31-b.

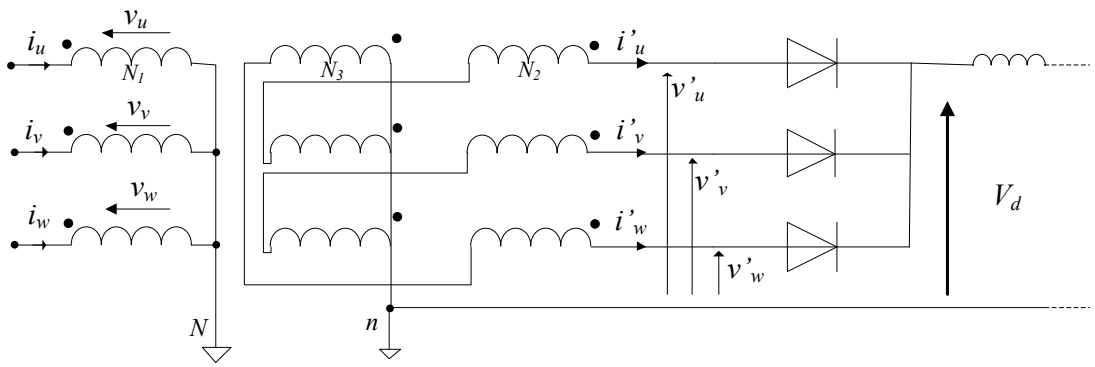


Figure III-30: Three phasehalf bridge rectifier with zigzag transformer.

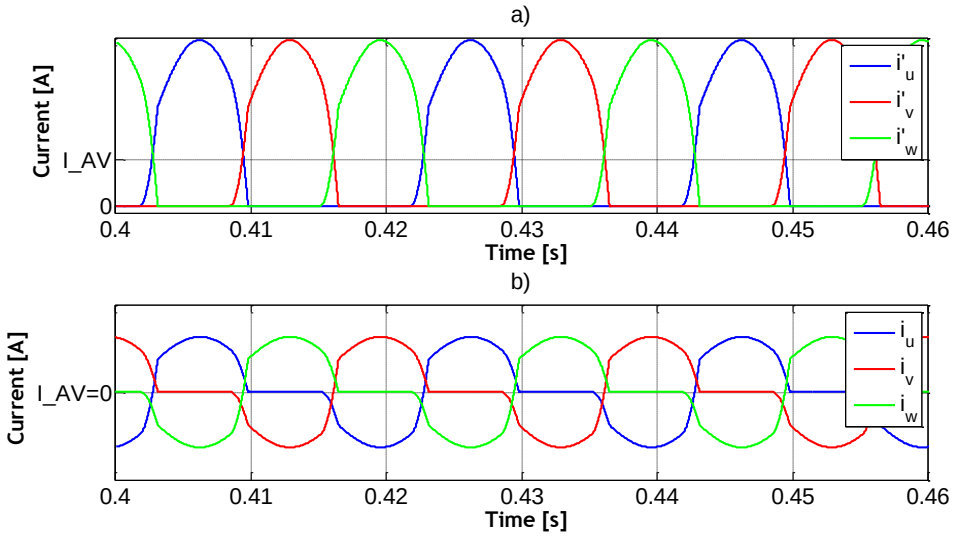


Figure III-31 – AC Current waveforms at secondary side (a) and primary side (b) of the transformer

III.4.1.2 The case study

In a half wave three phase rectifier, voltages on AC and DC side are respectively defined by expressions (106) and (107) by considering the averaged circuit in Figure III-29. Thus, the upgraded system has to be able to manage the power with the same voltage level. So the branch voltage (108) and the modulation signal (109)-(110) are evaluated.

$$v'_u(t) = \hat{V}\sin(\omega_0 t) \tag{106}$$

$$\overline{V}_d = \frac{3\sqrt{3}}{2}\hat{V} \tag{107}$$

$$\overline{V}_{Bu}(t) \approx V_d - \hat{V}\sin(\omega_0 t) \text{ with } V_d = \hat{V}\frac{3\sqrt{3}}{2\pi} \tag{108}$$

$$\hat{f}(t)\cdot N\cdot V_C = \hat{V}\left(\frac{3\sqrt{3}}{2\pi} - \sin(\omega_0 t)\right) \tag{109}$$

$$\frac{\hat{V}}{N\cdot V_C}\left(\frac{3\sqrt{3}}{2\pi} - 1\right) \le m(t) \le \frac{\hat{V}}{N\cdot V_C}\left(\frac{3\sqrt{3}}{2\pi} + 1\right) \tag{110}$$

To keep constant the capacitor voltage on each elementary converter, the power level has to be the same on DC and AC side (111). This statement leads to a direct relation between I_d and $\hat{I}$ (112). Thus, expression (112) shows that the current waveform has positive and negative values requiring a converter topology bidirectional in current.

$$P_{DC} = P_{AC} \quad with \quad \begin{cases} P_{DC} = V_d I_d \\ P_{AC} = 3\dfrac{\hat{V}\hat{I}}{2}\cos(\varphi) \end{cases} \tag{111}$$

$$I_d = \frac{\pi}{\sqrt{3}}\hat{I}\cos(\varphi) \tag{112}$$

As discussed in the previous section, the multilevel AC/DC converter has to be based on four quadrants elementary converters as depicted in Figure III-11.

Left column of TABLE III-6 shows the main parameters considered for the multilevel converter rating. Considering 4.5 kV IGBTs or IGCTs devices and according to (109).The switching frequency is fixed to 350 Hz and the value of the capacitor is calculated to achieve a voltage ripple under 2%.

DC link		**POWER CONVERTER S_N = 10 MVA**	
DC Link Voltage (V_d)	10 kV	Transformer secondary voltage V'_{ll}	23 kV
Zigzag Transformer		DC capacitor voltage V_C	2.6 kV
Magnetization Inductance L_M	12 H	Number of Cells per phase N	10
Total Leakage Inductance	12.7 mH	Cell Capacitor	10 mF
Winding Resistance	0.7Ω	Switching Frequency	350 Hz
Turn ratio $N_1/N_2 = N_1/N_3$	3.76		

TABLE III-6 – Converter Rating

To validate this study a model based on the time-domain simulation tool PSIM was developed. Simulation results are presented below. In Figure III-32-a, the multilevel voltage waveforms imposed by the converters are shown. As it was highlighted in expression (108), the DC offset makes these waveforms unsymmetrical.

Figure III-32-b show capacitor voltages and validate the choice of the capacitor value which guarantees a voltage ripple of 2%.

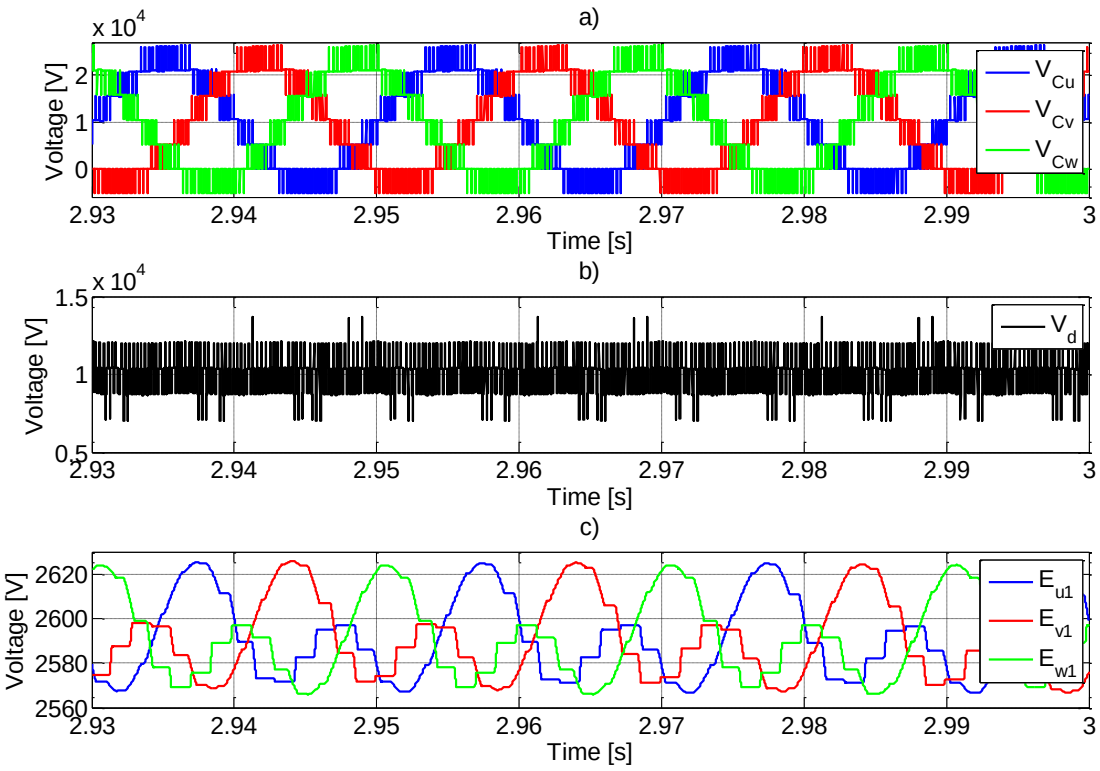


Figure III-32: Simulation Results – Voltage waveforms.

Figure III-33-a show the secondary current waveforms with a DC component. As expected, the primary current waveforms presented in Figure III-33-b are quasi-sinusoidal with a very low harmonic distortion.

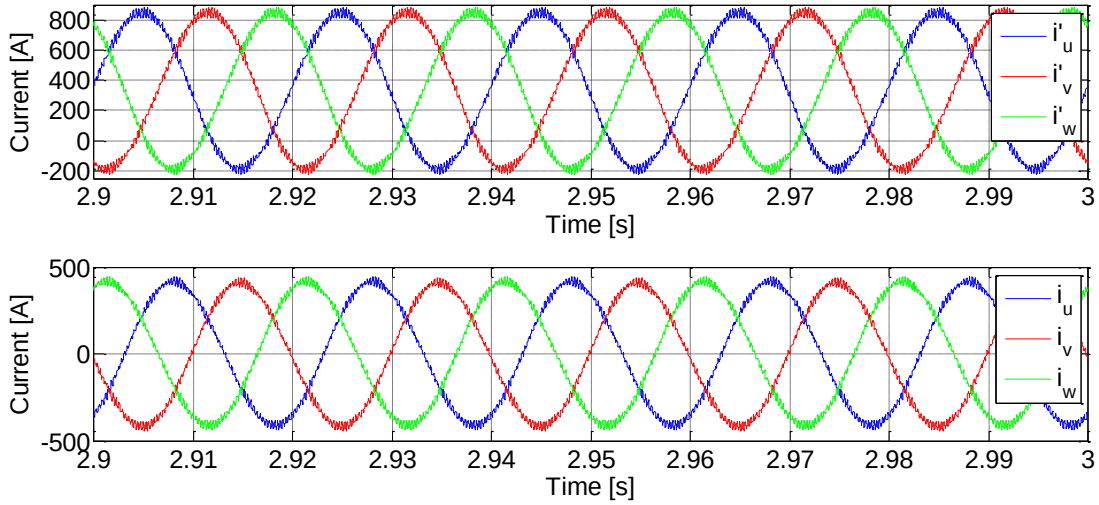


Figure III-33 – Simulation Results – Current Waveforms

Improvements on the AC side in terms of current are shown in Figure III-34. The single loop topology allows achieve negligible fundamental greater harmonics. This leads to a big reduction of the filtering elements.

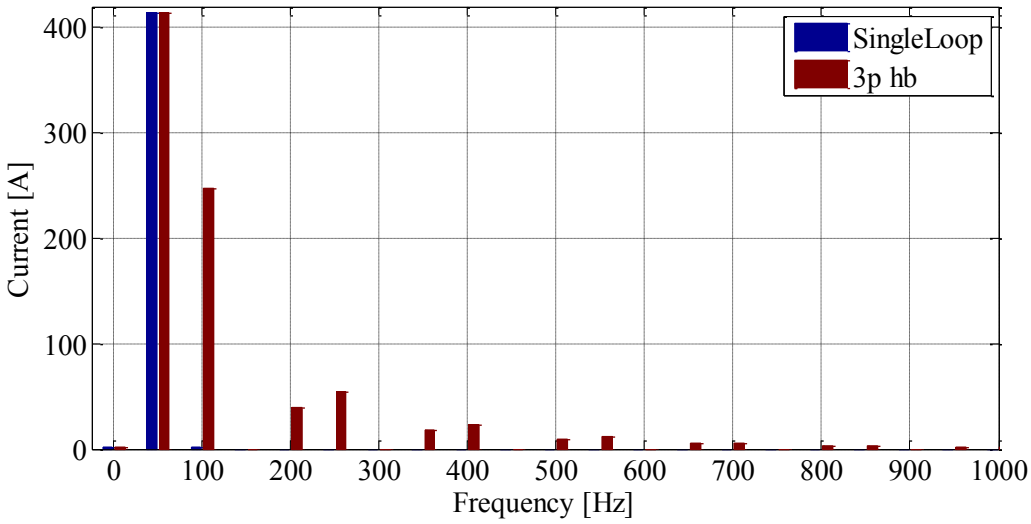


Figure III-34: comparison spectral content of the phase current

III.4.2 Conclusions

In terms of sizing the MMC Half Wave structure is the same respect to the MMC, of course the new topology does not require the branch inductor because it utilizes the leakage inductance of the zig-zag transformer. In a classical MMC structure the transformer has to sustain a DC insulation equal to the half of the DC voltage. This is not the case for the new topology, a classical insulation is sufficient.

The multilevel converter proposed to upgrade old rectifiers seems attractive. It draws on the AC side quasi-sinusoidal current waveforms. Furthermore, thanks to the cascaded H Bridge, a four quadrant operation can be achieved on the DC side. Nevertheless, the number of required devices could be very expensive. On the other hand, changing the transformer turns ratio could be a cheaper solution requiring a lower number of semi-conductor devices for the same output voltage.

Chapter IV. **PWM Control for Modular Multilevel Converter**

A control strategy for modular multilevel structures is proposed in this chapter. The scenario of the modulations techniques is described considering Phase Shift Modulation PWM.

In a classical VSI, the control imposes the desired output currents and keeps a constant voltage on the DC link. For multicellular structures the right balance among the voltages of each elementary converter is necessary, too.

For PS-PWM employment, the control for multilevel structure is carried out through three main control loops which are described hereafter. The regulators are defined and synthetized for each control loop. A system of 100 MW composed by 64 elementary converters per branch is considered as a case study for which sizing parameters were provided in the second chapter. Simulations were performed to validate the control strategy by ensuring the right set-up of the regulators. The chosen simulation environment is MATLAB-PSIM.

IV.1 Introduction

In the last decade the attention of research and development for modulation techniques have played a key role for multilevel structures [39], [70]-[71]. The goal was to extend traditional techniques to multilevel cases. The control of multilevel structures requires more complex strategies to drive more semiconductor devices. On the other hand, benefits can be derived from managing multiple degrees of freedom (the availability and redundancy for instance).

The development and the detailed description of the main modulation techniques in the frame of the multilevel structures are well defined in [72]. The diagram in Figure IV-1 depicts the scenario. In this work the study of modulation techniques is focused on Phase Shifted PWM, derived from the extension to multilevel structures of the traditional PWM technique.

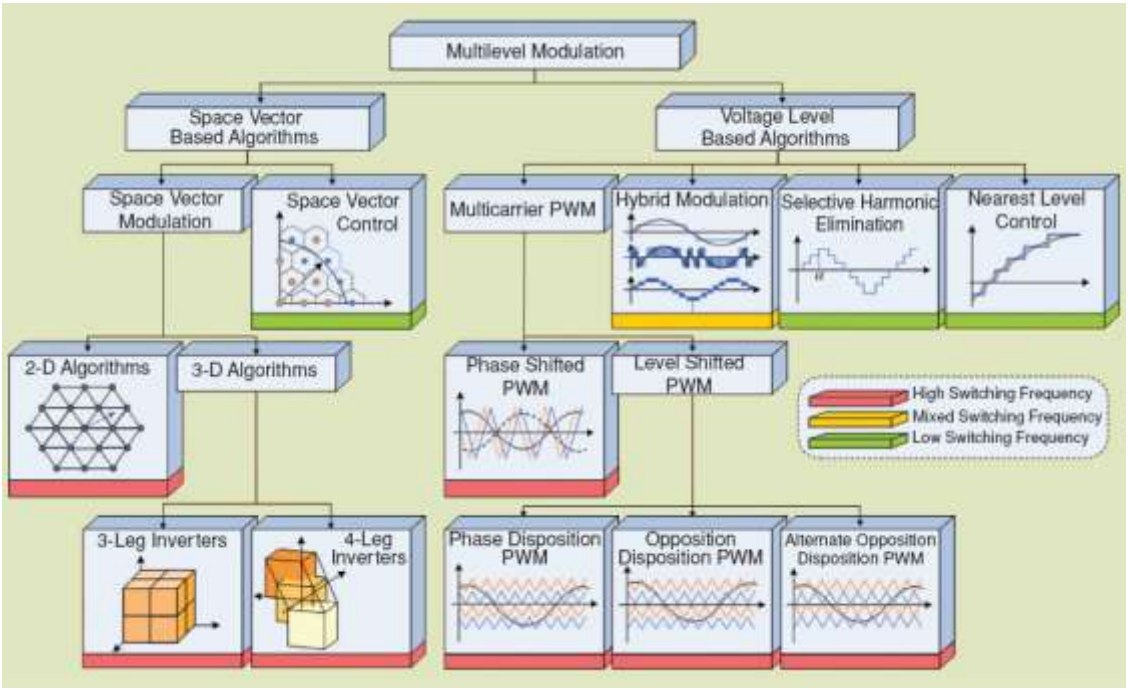


Figure IV-1: Scenario of the modulation techniques for multilevel structures [72]

The strategy adopted in this work for multi-cell topologies associates each carrier to a particular elementary converter or power cell to be modulated independently using sinusoidal PWM respectively. The modulation provides also an even power distribution among the cells. For a converter with N cells, a carrier phase shift of 360◦/N is introduced across the cells to generate the quasi-sinusoidal output waveform [73].

IV.2 Principle of the Phase shifted PWM for MMCs

One more time the averaged model of the structure shown in Figure IV-2 is proposed in order to make the preliminary study fast and direct. The subscript "av" in the formulas is neglected to better visualize the equations. The instantaneous model is used only if specified.

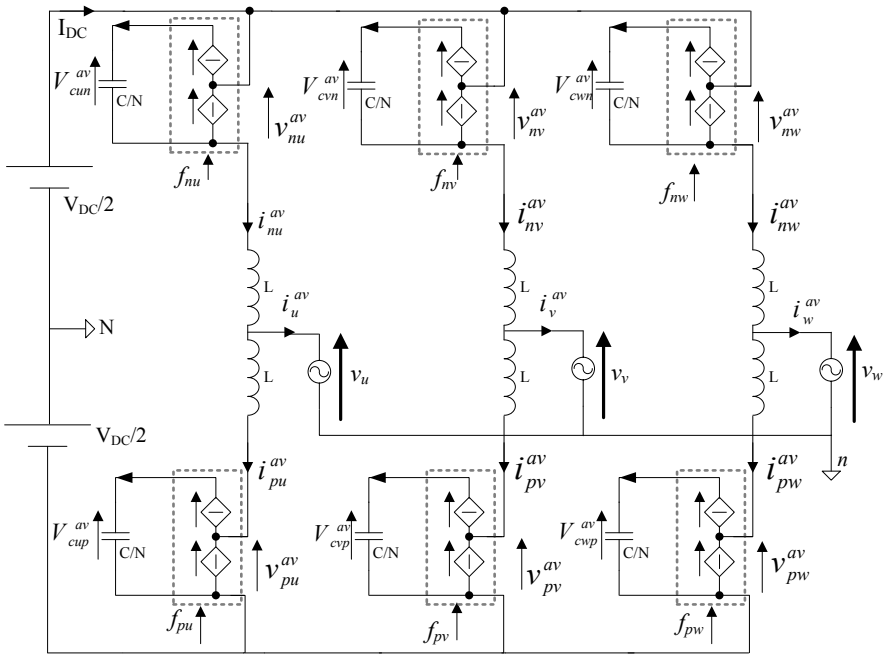


Figure IV-2: Averaged model for a MMC structure

The control for SPWM modulated multilevel structures has to ensure that:

- The system is able to impose the desired current to achieve the required power
- In each phase the capacitors are on the desired voltage level
- The voltages among the capacitors of each elementary converter are balanced between them.

The unbalancing can be caused by different tolerances of passive components, unequal conduction and switching losses in the semiconductor devices or signal imbalance and resolution issues inherent in the control circuit including voltage/current sensors [63].

For these reasons the control approach needs three controllers which are arranged according to the diagram in Figure IV-3.

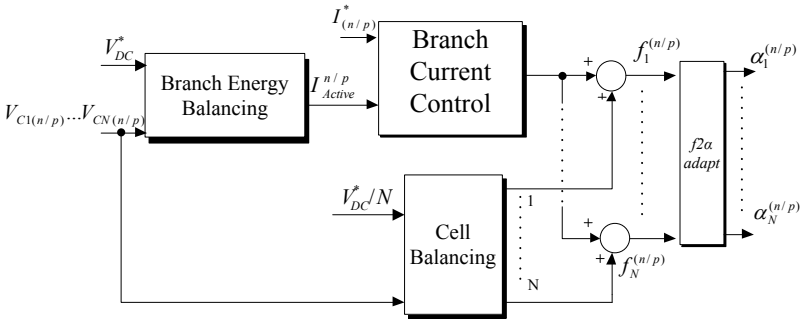


Figure IV-3: SPWM Control approach for a multicellular structure

The energy balancing and the current control follow the classical cascaded disposition of the VSC based structures. The energy balancing provides the required active power, through a current reference, in order to keep the capacitors charged.

In ideal conditions where all the cells of the system are equal and balanced, with the same losses and with sensors with the same characteristics, the cell balancing control could be neglected. This control only regulates the voltage of each capacitor around the right level, which is just reached by the energy-balancing controller. Thus this loop adjusts the voltage on the capacitor by directly interfering on the modulation signal.

The control approach does not depend from the particular topology of the elementary converter. The scaling between *f(t)* and the duty cycle *α(t)* is immediate.

Each controller of Figure IV-3 was presented and developed for the MMC structure. Moreover simulations were performed to validate the study on the 100 MW system presented in the previous chapters and recalled in Table II-2. The system was sized according to the considerations carried out in section II.3. For a better understanding the averaged model was considered.

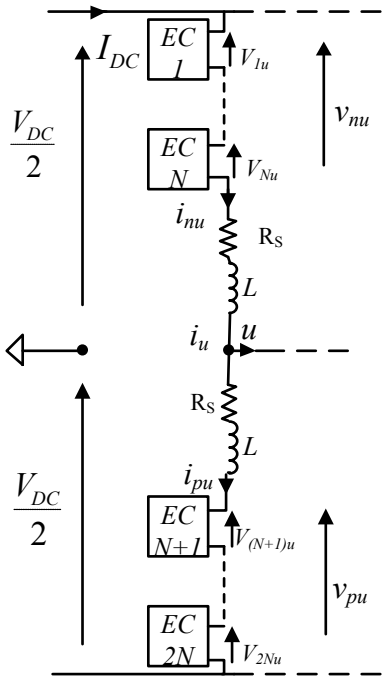


Figure IV-4: Case study system

Table IV-1: system power rate

System Power Rate	
Nominal power	100 MW
Phase to phase Grid voltage V_{ll}	83 kV
V_d	160 kV
Number of sub-modules	N=64
Branch inductor L	10 mH
Cell Capacitor C	6 mF
Voltage capacitor	2.5 kV
Cell switching frequency	200 Hz
Inductor resistance R_S	60 mΩ

IV.2.1 Current control loop

The study supposes that the averaged model of the MMC (shown in Figure IV-2) is connected on the AC side with a balanced (16) and symmetrical three-phase grid (114).

$$v_u(t) = \sqrt{2}V\sin(\omega_0 t) \qquad v_v(t) = \sqrt{2}V\sin\left(\omega_0 t - \frac{2}{3}\pi\right) \qquad v_v(t) = \sqrt{2}V\sin\left(\omega_0 t + \frac{2}{3}\pi\right) \quad (113)$$

$$i_u(t) = \sqrt{2}I\sin(\omega_0 t - \varphi) \quad i_v(t) = \sqrt{2}I\sin\left(\omega_0 t - \frac{2}{3}\pi - \varphi\right) \quad i_w(t) = \sqrt{2}I\sin\left(\omega_0 t + \frac{2}{3}\pi - \varphi\right) \quad (114)$$

As discussed in the second chapter the superimposition approach facilitates the study and allows for easier understanding.

In Figure IV-5 the control strategy for the AC part of the system is depicted. The system supposes that there is not DC current for the symmetry condition. The structure can be seen as two independent STATCOMs (negative and positive).

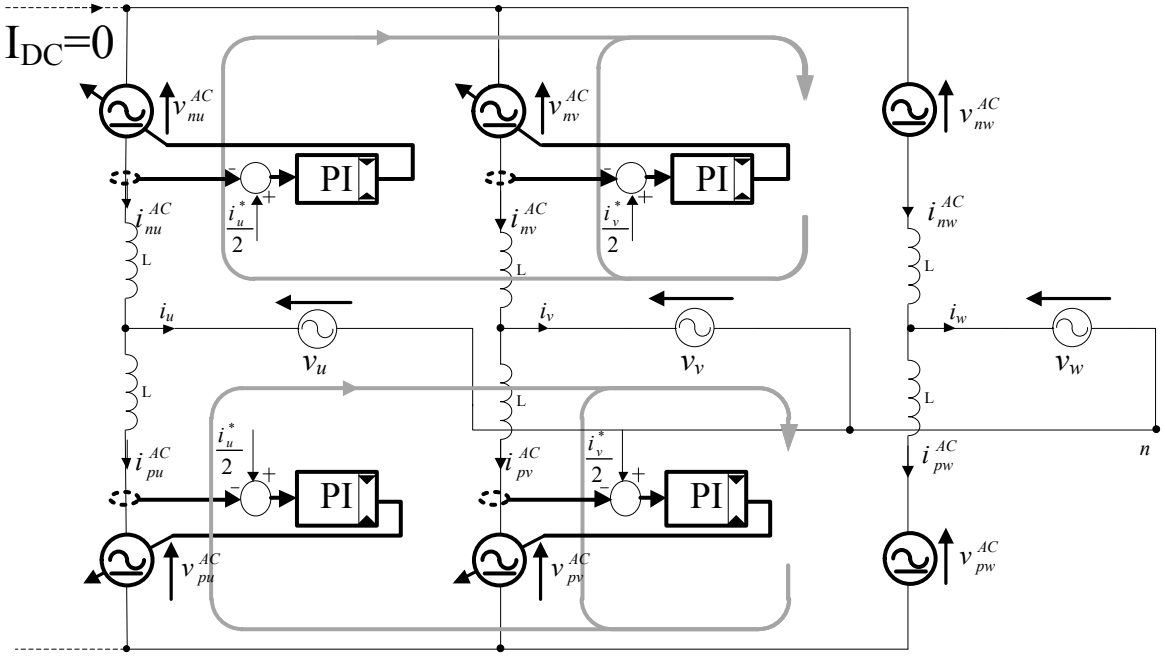


Figure IV-5: Control approach for the AC part for a MMC structure

Each voltage of the branch generator can be regulated to impose the required current through the branch inductor. The AC part of the current for each branch is required to be the half of the phase current.

According to the symmetry conditions one of the branch currents per STATCOM depends on the other ones as written in (115).

$$i_{nw}^{AC} = -\left(i_{nv}^{AC} + i_{nu}^{AC}\right) \qquad i_{pw}^{AC} = -\left(i_{pv}^{AC} + i_{pu}^{AC}\right) \tag{115}$$

This means that for each STATCOM just two branch voltage generators can be controlled according to the simplified schema shown in Figure IV-6 for the negative part and in Figure IV-7 for the positive part.

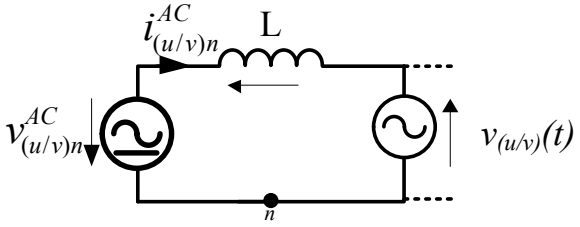


Figure IV-6: Simplified circuit for the negative part of the structure

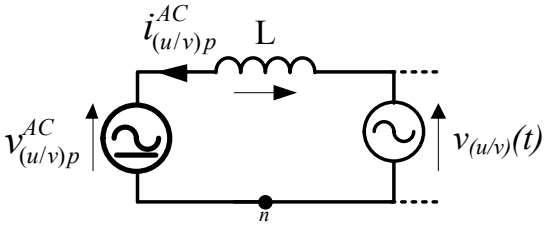


Figure IV-7: Simplified circuit for the positive part of the structure

For each part the equations (116) and (117) are achieved by considering the branch inductors without copper losses.

$$\begin{cases} L\dfrac{d}{dt}i_{nu}^{AC}(t) = -(v_{nu}^{AC}(t) + v_u(t)) \\ L\dfrac{d}{dt}i_{nv}^{AC}(t) = -(v_{nv}^{AC}(t) + v_v(t)) \end{cases} \quad (116) \qquad \begin{cases} L\dfrac{d}{dt}i_{pu}^{AC}(t) = -v_{pu}^{AC}(t) + v_u(t) \\ L\dfrac{d}{dt}i_{pv}^{AC}(t) = -v_{pv}^{AC}(t) + v_v(t) \end{cases} \quad (117)$$

In order to control the AC part of the MMC structure it is necessary to respect the four equations independently.

The control strategy for the DC part of the structure is shown in the layout in Figure IV-8.

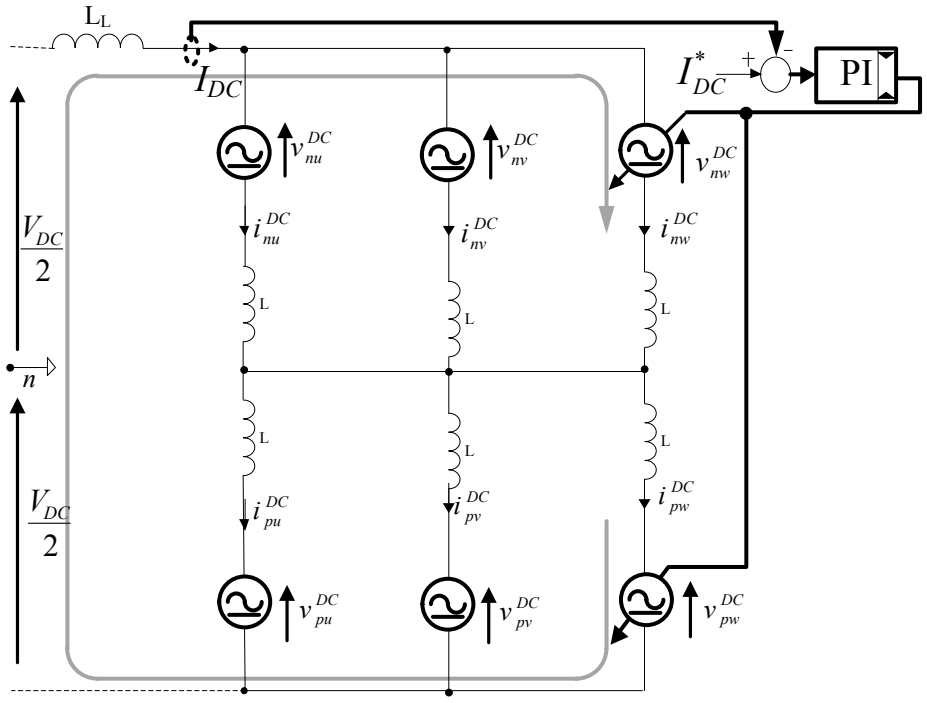


Figure IV-8: Current control loop for the DC part of the MMC structure

The *u* and *v* current controls are supposed to work well. The control must provide just the balance in (118). The current loop in Figure IV-8 is achieved in (120). Since the two controlled generators are driven by the same loop the (120) is developed into (121).

$$I_{DC} = i_{u(n/p)}^{DC}(t) + i_{v(n/p)}^{DC}(t) + i_{w(n/p)}^{DC}(t) = i_{u(n/p)}(t) + i_{v(n/p)}(t) + i_{w(n/p)}(t) \quad (118)$$

$$\frac{I_{DC}}{3} = i_{u(n/p)}^{DC}(t) = i_{v(n/p)}^{DC}(t) = i_{w(n/p)}^{DC}(t) \tag{119}$$

$$v_{wn}^{DC}(t) + v_{wp}^{DC}(t) = V_{DC} - L_L \frac{d}{dt} I_{DC} - \frac{2L}{3} \frac{d}{dt} I_{DC}; v_{wn}^{DC}(t) = v_{wp}^{DC}(t) \tag{120}$$

$$2v_{wn}^{DC}(t) = 2v_{wp}^{DC}(t) = V_{DC} - \left(L_L + \frac{2L}{3} \right) \frac{d}{dt} I_{DC} \tag{121}$$

Finally for the current control, the branch generators have to be driven to comply with the five equations summarized in (116), (117) and (121).

IV.2.2 dq0 reference frame

The advantages coming from the control implemented in the dq0 reference frame with respect to the time domain are well known and described in the literature [64], [65]. In this section the control approach represented in the dq0 reference frame is shown and then simulations are performed to validate this study.

During the steady state of the system the currents in the branches are thereby extracted in (122) for the negative part and in (123) for the positive part of the system.

$$\begin{cases} i_{nu}(t) = i_{nu}^{AC}(t) + \dfrac{I_{DC}}{3} \\ i_{nv}(t) = i_{nu}^{AC}(t) + \dfrac{I_{DC}}{3} \\ i_{nw}(t) = i_{nu}^{AC}(t) + \dfrac{I_{DC}}{3} \end{cases} \tag{122}$$

$$\begin{cases} i_{pu}(t) = i_{pu}^{AC}(t) + \dfrac{I_{DC}}{3} \\ i_{pv}(t) = i_{pu}^{AC}(t) + \dfrac{I_{DC}}{3} \\ i_{pw}(t) = i_{pu}^{AC}(t) + \dfrac{I_{DC}}{3} \end{cases} \tag{123}$$

According to the park transformation the dq0 components are evaluated according to (124) and (125) [66].

$$\begin{cases} \begin{bmatrix} i_{dn}(t) \\ i_{qn}(t) \\ i_{0n}(t) \end{bmatrix} = \dfrac{2}{3} \begin{bmatrix} \sin(\omega_0 t) + \sin(\omega_0 t - \frac{2}{3}\pi) + \sin(\omega_0 t + \frac{2}{3}\pi) \\ \cos(\omega_0 t) + \cos(\omega_0 t - \frac{2}{3}\pi) + \cos(\omega_0 t + \frac{2}{3}\pi) \\ 1/2 \quad 1/2 \quad 1/2 \end{bmatrix} \cdot \begin{bmatrix} i_{nu}(t) \\ i_{nv}(t) \\ i_{nw}(t) \end{bmatrix} \end{cases} \tag{124}$$

$$\begin{cases} \begin{bmatrix} i_{dp}(t) \\ i_{qp}(t) \\ i_{0p}(t) \end{bmatrix} = \dfrac{2}{3} \begin{bmatrix} \sin(\omega_0 t) + \sin(\omega_0 t - \frac{2}{3}\pi) + \sin(\omega_0 t + \frac{2}{3}\pi) \\ \cos(\omega_0 t) + \cos(\omega_0 t - \frac{2}{3}\pi) + \cos(\omega_0 t + \frac{2}{3}\pi) \\ 1/2 \quad 1/2 \quad 1/2 \end{bmatrix} \cdot \begin{bmatrix} i_{pu}(t) \\ i_{pv}(t) \\ i_{pw}(t) \end{bmatrix} \end{cases} \tag{125}$$

The dq0 components of the current for each part (negative and positive) of the MMC are so extracted in (126). Of course, the *dq* components depend on the AC part of the branch currents because the second part of the sum is equal to zero.

To perform the current control loop the dq0 transform of the derivate has to be carried out according to (116), (117) and (121). For this reason the derivate in the time domain for (124) and (125) are achieved in (126). The 0 components are evaluated by considering the (118) and (119)

$$\begin{aligned}
&\frac{d}{dt}i_{(n/p)d} = \frac{2}{3}\left[\frac{d}{dt}i^{AC}_{u(n/p)}\sin(\omega_0 t) + \frac{d}{dt}i^{AC}_{v(n/p)}\sin(\omega_0 t - \frac{2}{3}\pi) + \frac{d}{dt}i^{AC}_{w(n/p)}\sin(\omega_0 t + \frac{2}{3}\pi)\right] + \\
&+\frac{2}{3}\left[\omega_0 i^{AC}_{u(n/p)}\cos(\omega_0 t) + \omega_0 i^{AC}_{v(n/p)}\cos(\omega_0 t - \frac{2}{3}\pi) + \omega_0 i^{AC}_{w(n/p)}\cos(\omega_0 t + \frac{2}{3}\pi)\right] \\
&\frac{d}{dt}i_{(n/p)q} = \frac{2}{3}\left[\frac{d}{dt}i^{AC}_{u(n/p)}\sin(\omega_0 t) + \frac{d}{dt}i^{AC}_{v(n/p)}\sin(\omega_0 t - \frac{2}{3}\pi) + \frac{d}{dt}i^{AC}_{w(n/p)}\sin(\omega_0 t + \frac{2}{3}\pi)\right] + \\
&-\frac{2}{3}\left[\omega_0 i^{AC}_{v(n/p)}\cos(\omega_0 t) + \omega_0 i^{AC}_{v(n/p)}\cos(\omega_0 t - \frac{2}{3}\pi) + \omega_0 i^{AC}_{w(n/p)}\cos(\omega_0 t + \frac{2}{3}\pi)\right] \\
&\frac{d}{dt}i_{(n/p)0} = \frac{1}{3}\left[\frac{d}{dt}i_{u(n/p)} + \frac{d}{dt}i_{v(n/p)} + \frac{d}{dt}i_{w(n/p)}\right] = \frac{1}{3}\frac{d}{dt}I_{DC}
\end{aligned} \tag{126}$$

In order to achieve a better visualization, (126) was rearranged in the form of (127) for the negative part of the system and (128) for the positive one.

$$\begin{cases}
\frac{d}{dt}i_{nd}(t) = \left[\frac{di^{AC}_n}{dt}\right]_d + \omega_0 i_{nq} \\
\frac{d}{dt}i_{nq}(t) = \left[\frac{di^{AC}_n}{dt}\right]_q - \omega_0 i_{dn}
\end{cases} \tag{127}$$

$$\begin{cases}
\frac{d}{dt}i_{pd}(t) = \left[\frac{di^{AC}_p}{dt}\right]_d + \omega_0 i_{pq} \\
\frac{d}{dt}i_{pq}(t) = \left[\frac{di^{AC}_p}{dt}\right]_q - \omega_0 i_{pd}
\end{cases} \tag{128}$$

The obtained equations show the dependency between the d and q components, as described in [63]-[65]. So the results in (116) and (117) and (121) in the dq0 reference frame become (129) and (130).

$$\begin{cases}
L\frac{d}{dt}i_{nd}(t) - \omega_0 L i_{nq} = -(v_{nd}(t) + v_d(t)) \\
L\frac{d}{dt}i_{nq}(t) + \omega_0 L i_{nd} = -(v_{nq}(t) + v_q(t)) \\
(L_L + \frac{2L}{3})\frac{d}{dt}I_{DC}(t) = V_{DC} - 2v_0(t)
\end{cases} \tag{129}$$

$$\begin{cases}
L\frac{d}{dt}i_{pd}(t) - \omega_0 L i_{pq} = -v_{pd}(t) + v_d(t) \\
L\frac{d}{dt}i_{pq}(t) + \omega_0 L i_{pd} = -v_{pq}(t) + v_q(t) \\
(L_L + \frac{2L}{3})\frac{d}{dt}I_{DC}(t) = V_{DC} - 2v_0(t)
\end{cases} \tag{130}$$

Evaluations showed that the d and q components of the current are coupled between them [64]. In the next section d and q components are decoupled to simplify the regulator synthesis.

IV.2.2.1 The regulator synthesis

In order to test only the current control loop, the system in Figure IV-9, the averaged branch, is considered by substituting the capacitor with a voltage source.

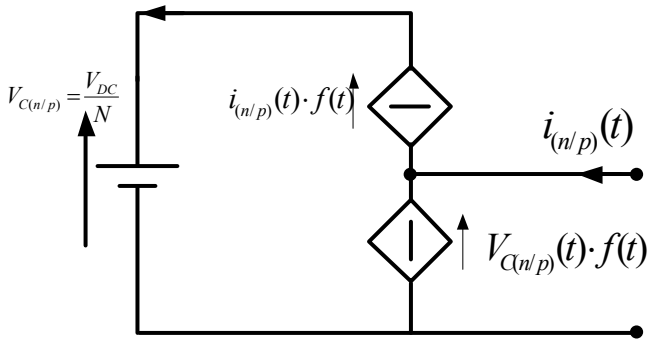


Figure IV-9: Averaged model of the MMC branch to test the control loop

The PLL adopted is the Feed Forward q-PLL which generates the direct component synchronous reference frame. The chosen q-PLL was consolidated in [68] for its fast and robust latching.

As described before the dq current controls are performed for the positive and negative part of the structure. According to (129) and (130) the decoupling layouts are achieved in Figure IV-10 for the negative part and in Figure IV-11 for the positive part.

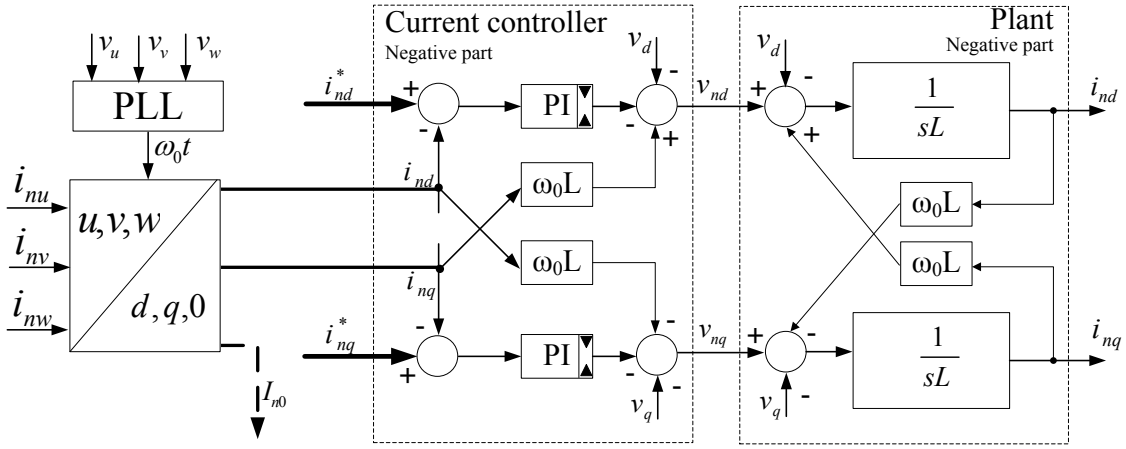


Figure IV-10: Layout of the control for the negative part in dq0 reference frame

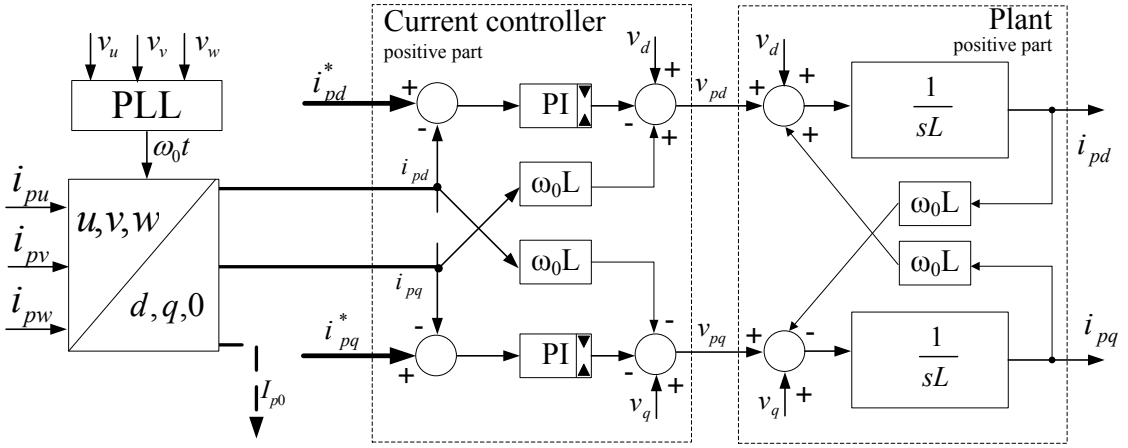


Figure IV-11: Current controller plant in dq0 reference frame for the positive part of the structure

After the decoupling the d and q components can be independently treated as depicted in Figure IV-12 and Figure IV-13 [69].

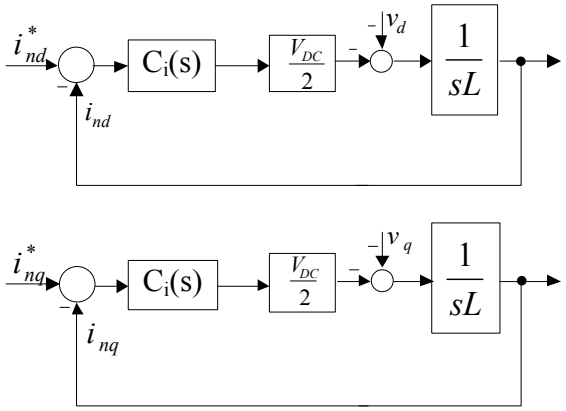


Figure IV-12: Current loops for the negative part after the de-coupling

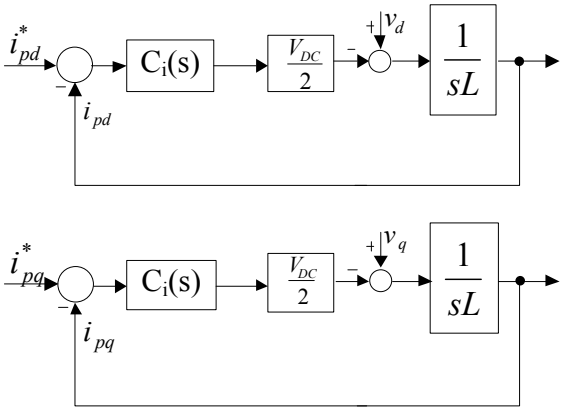


Figure IV-13: Current loops for the positive part after the de-coupling

In the dq0 reference frame, the control of the fundamental component means controlling a constant variable in the time domain. Moreover, a second harmonic component due to the circulating currents, treated in the second chapter, has to be suppressed (Figure II-9). In dq0 this component becomes the fundamental one.

The PI regulator (131) is synthetized according to the open loop transfer function shown in (132). The gain *ki* is evaluated in order to achieve a crossing frequency ten times the fundamental component while the time constant *Ti* is defined to achieve a phase margin of 60° in order to guarantee the stability.

$$C_i(s) = k_i \cdot \frac{1+sT_i}{sT_i} \tag{131}$$

$$Hi(s) = k_i \cdot \frac{V_C}{2} \cdot \frac{1}{sL} \frac{1+sT_i}{sT_i} \tag{132}$$

$$\begin{cases} \left|Hi(s)\right|_{\omega_C} \approx k_i \cdot \dfrac{V_C}{2} \cdot \dfrac{1}{\omega_{Ci} L} \\ \angle Hi(j\omega_{Ci}) = a\tan\left(\dfrac{\pi}{3}\right) \Rightarrow \sqrt{3} \approx \omega_{Ci} T_i \end{cases} \quad with \quad \begin{array}{c} \omega_{Ci} \le 2\pi(10 \cdot f_0) \\ \omega_{Ci} i T_i >> 1 \end{array} \tag{133}$$

The layout of the 0 component control is defined in Figure IV-14 by implementing the third equation of (129) or (130).

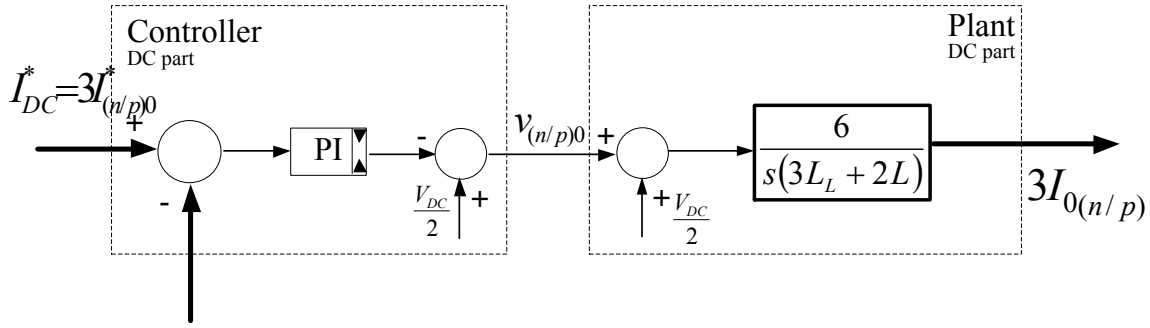


Figure IV-14: Current controller plant for the 0 component of the structure

The layout of the control loop is depicted in Figure IV-15.

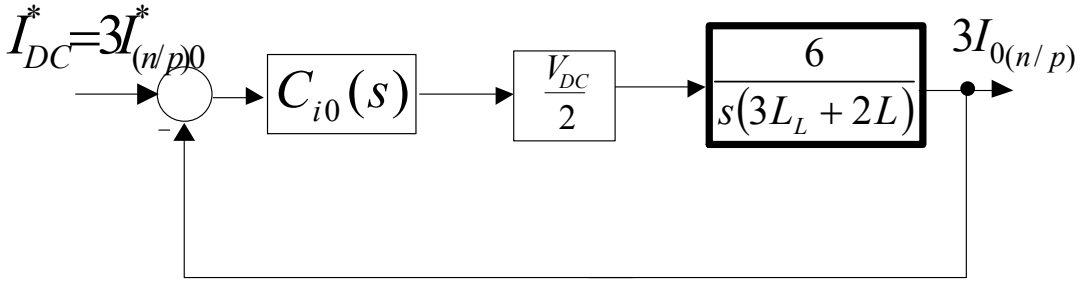


Figure IV-15: Control loop for the 0 component

The regulator (134) makes the system able to follow the power required, for this reason; the dynamic proprieties of the open loop transfer function (135) are slower than the current loop. Therefore, the cutting frequency is around 10 Hz while the time constant is chosen to guarantee the stability (136).

$$C_i(s) = k_{i0} \cdot \frac{1+sT_{i0}}{sT_{i0}} \tag{134}$$

$$Hi_0(s) = k_{i0} \cdot V_{DC} \cdot \frac{6}{s(3L_L+2L)} \frac{1+sT_{i0}}{sT_{i0}} \tag{135}$$

$$\begin{cases} |Hi(s)|_{\omega_C} \approx k_{i0} \cdot V_{DC} \cdot \dfrac{6}{\omega_C(3L_L+2L)} \\ \angle Hi(j\omega_{Ci0}) = a\tan\left(\dfrac{\pi}{3}\right) \Rightarrow \sqrt{3} \approx \omega_{Ci}T_{i0} \end{cases} \quad with \quad \begin{matrix} \omega_{Ci0} \le 2\pi \cdot 15 \\ \omega_{Ci0}T_{i0} >> 1 \end{matrix} \tag{136}$$

IV.2.2.2 Simulations

The current control loops are validated via simulations by considering the averaged system with the main parameters listed in Table II-2.

The simulations are performed according to the power excursion in Figure IV-16, from inverter to rectifier operating mode always at unit power factor. The dq currents measured in the system seem to match quite well with the references. The stability and the crossing frequency imposed by the regulators guarantee the stability and good shape of the waveforms.

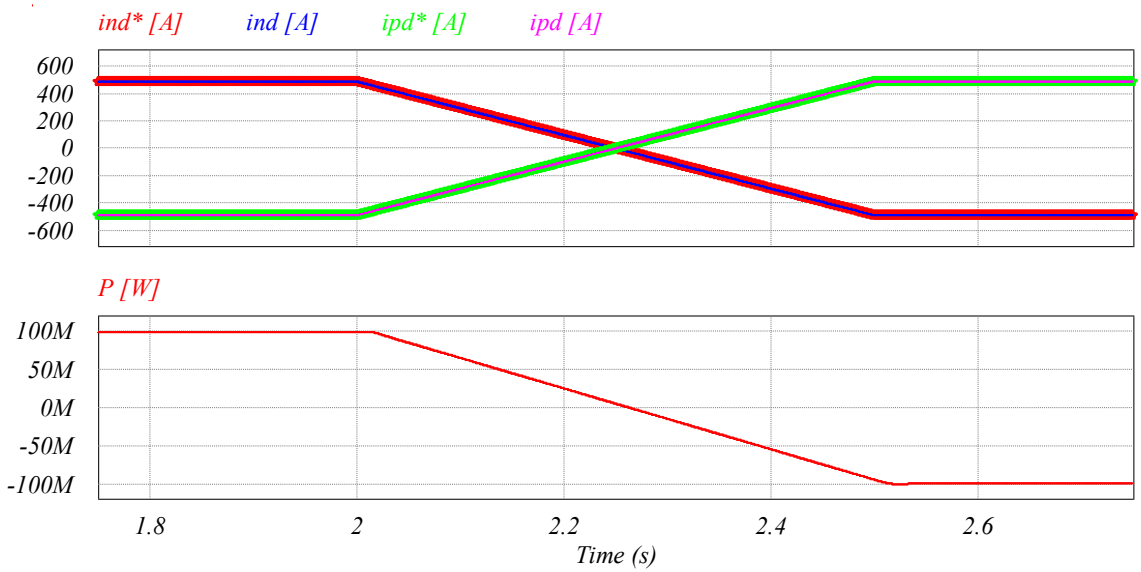


Figure IV-16: d-currents with the references and active power

In Figure IV-18 and Figure IV-18 the good synthesis of the regulators is validated even for the q component which is imposed to zero and for the 0 component which is the third part of the DC current.

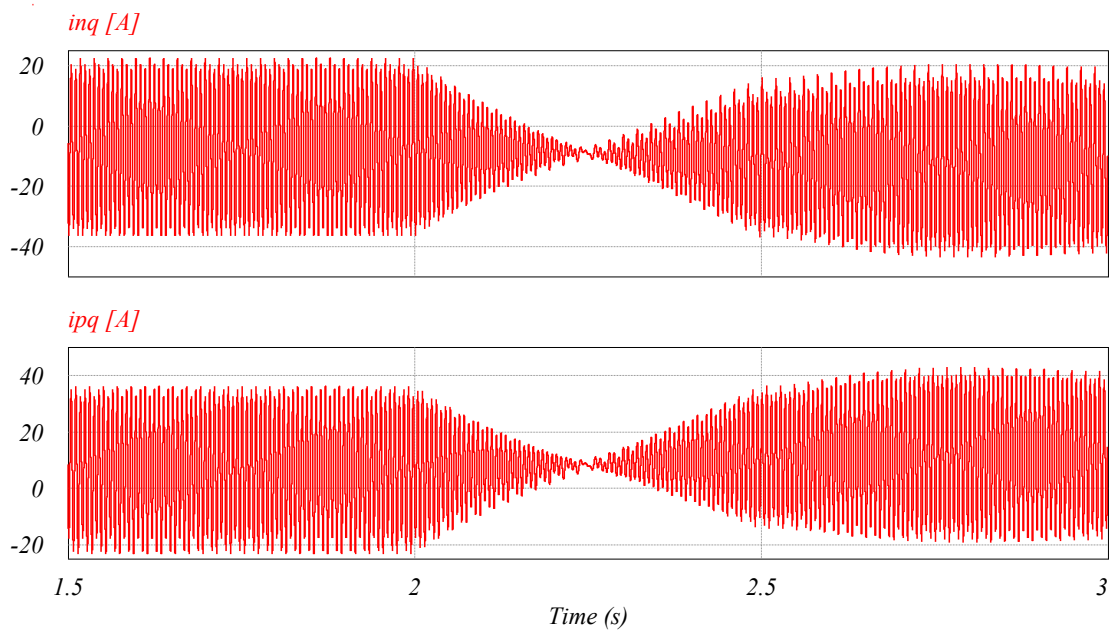


Figure IV-17: Components for q-currents

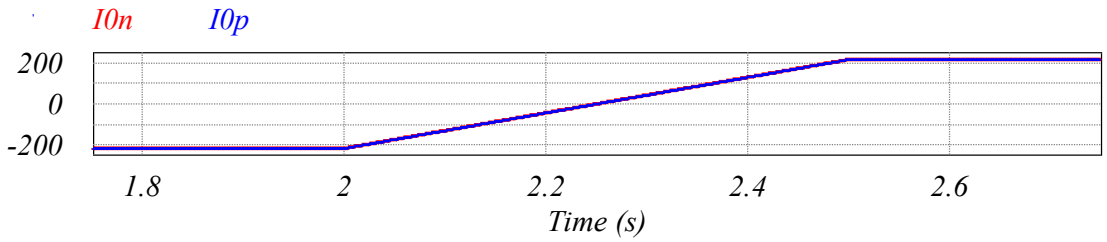


Figure IV-18: q0-current references and measurements

Finally the u, v, w current components in the branches are reported for the two parts of the system. As verified before, the 0 component regulator was also very well synthesized.

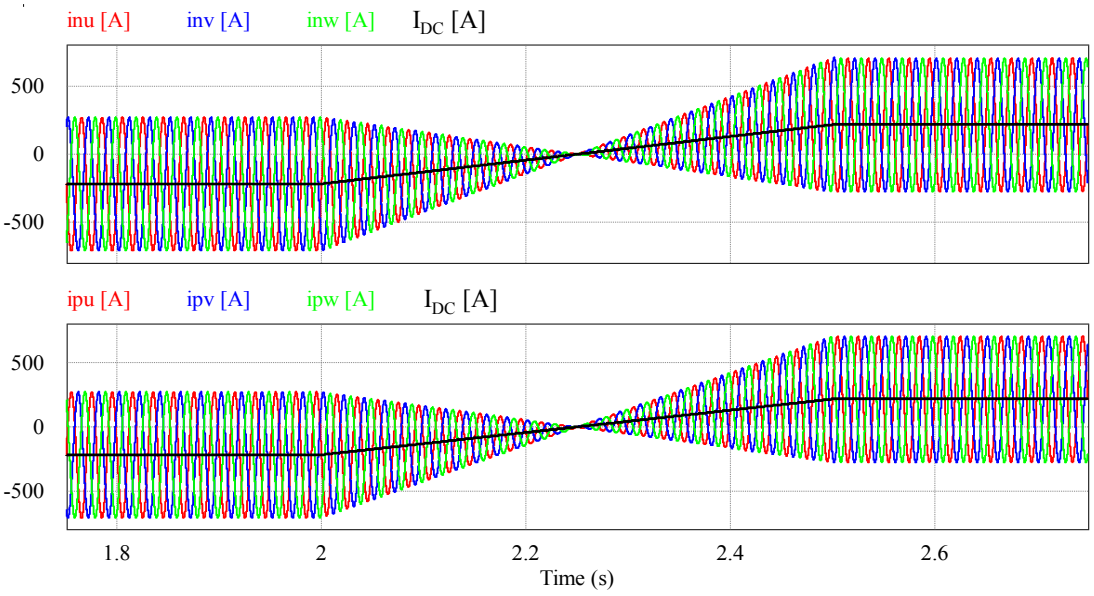


Figure IV-19: u, v, w current components in the branches and continuous current

IV.2.3 Branch energy balancing

This part of the control regulates the active power necessary to keep the capacitor voltages on a required level. The averaged system in Figure IV-2 is considered. For each part of the system (positive and negative) the DC mean capacitor voltage of the three branches $V_{Cn/p}$ is given by (137).

$$\overline{V}_{Cn} = \frac{1}{3}\left(V_{Cnu} + V_{Cnv} + V_{Cnw}\right); \overline{V}_{Cp} = \frac{1}{3}\left(V_{Cpu} + V_{Cpv} + V_{Cpw}\right) \tag{137}$$

In the *dq0* reference frame, considering the PLL latched on the phase voltage, the active and reactive powers, managed by each part of the structure, are achieved in (138). The achieved balance affirms that the active power depends only on the direct component of the AC current and of the AC voltage. The AC voltage is imposed by the grid. The control of the active power is achieved by the regulation of the direct component of the current.

$$\begin{cases} P_{AC(n/p)} = 3\left(v_d i_{(n/p)d} + v_q i_{(n/p)q}\right) \\ Q_{(n/p)} = 3\left(v_d i_{(n/p)q} - v_q i_{(n/p)d}\right) \end{cases} = \begin{cases} P_{AC(n/p)} = 3 v_d i_{(n/p)d} \\ Q_{(n/p)} = 3 v_d i_{(n/p)q} \end{cases}; \tag{138}$$

Assuming that the negative and positive parts of the structure are balanced between them, the active power is shared in the structure according to the (139). The equivalent capacitance

of each branch is considered as discussed in the second chapter (C/N) by taking into account the AC in (138) and the balance (139) becomes the (140).

$$P_{DC} = P_{ACn} + P_{ACp} + 2\frac{C}{N}\frac{d}{dt}\overline{V}_{C(n/p)}(t)\cdot\overline{V}_{C(n/p)}(t)\,;\, P_{ACn} = P_{ACp} = \frac{P_{AC}}{2} \tag{139}$$

$$P_{DC} - 6v_d i_{(n/p)d} = C\frac{d}{dt}\overline{V}^2_{C(n/p)}(t) \tag{140}$$

A constant value of the capacitor voltage requires a current with a null DC component as discussed in the second chapter. Hence, we have a direct relationship between the DC and AC currents of the system recalled by (24) in the dq0 reference frame. AC and DC current components in the system are dependent.

$$i_0 = \frac{Mi_d}{4}\cos(\varphi) \tag{141}$$

IV.2.3.1 Design of the controller

The synthesis was developed by considering the layout in Figure IV-20 valid for the negative and the positive structure according to the (140). The gain of the loop was fixed by considering v_d equal to the peak value of the voltage (16).

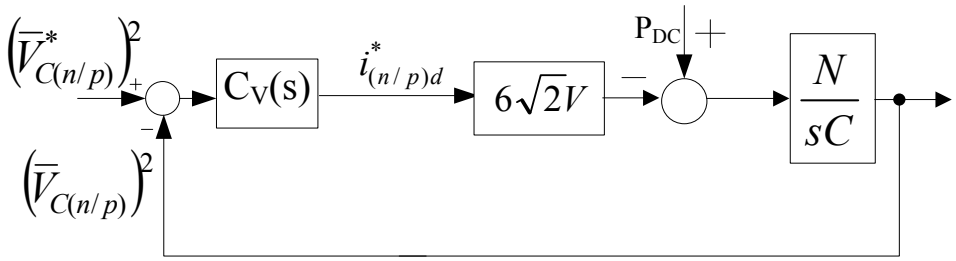


Figure IV-20: Branch energy control loop

By considering the voltage regulator (131), the open loop transfer function of the system is reported in (143). The control system guarantees the right energy balancing, for this reason the PI regulator is chosen to achieve a low crossing frequency and by ensuring the stability (144).

$$C_v(s) = k_v \cdot \frac{1+sT_v}{sT_v} \tag{142}$$

$$Hv(s) = k_v \cdot 6\sqrt{2}V. \frac{N}{sC} \frac{1+sT_v}{sT_v} \tag{143}$$

$$\begin{cases} |Hi(s)|_{\omega_C} \approx k_v \cdot 6\sqrt{2}V. \dfrac{N}{\omega_{Cv}C} \\ \angle Hv(j\omega_C) = a\tan\left(\dfrac{\pi}{3}\right) \Rightarrow \sqrt{3} \approx \omega_{Cv}T_v \end{cases} \quad with \quad \begin{matrix} \omega_C \approx 2\pi 10 \\ \omega_{Cv}T_v >> 1 \end{matrix} \tag{144}$$

IV.2.3.2 Simulations

Simulations were carried out in order to verify the good synthesis of the energy balancing regulators. The main parameters of the system are reported in Table II-2. Simulations are performed by considering the power excursion in Figure IV-21, keeping a null reactive power.

The direct components of the current references are generated by the voltage control as depicted by the macro-layout for of the control in Figure IV-3.

By requiring a DC current of 650 A (necessary to achieve 100 MW), the voltage controllers generate the right reference by ensuring the right level of the d-component for each branch current (24) for the two parts of the structure (Figure IV-21).

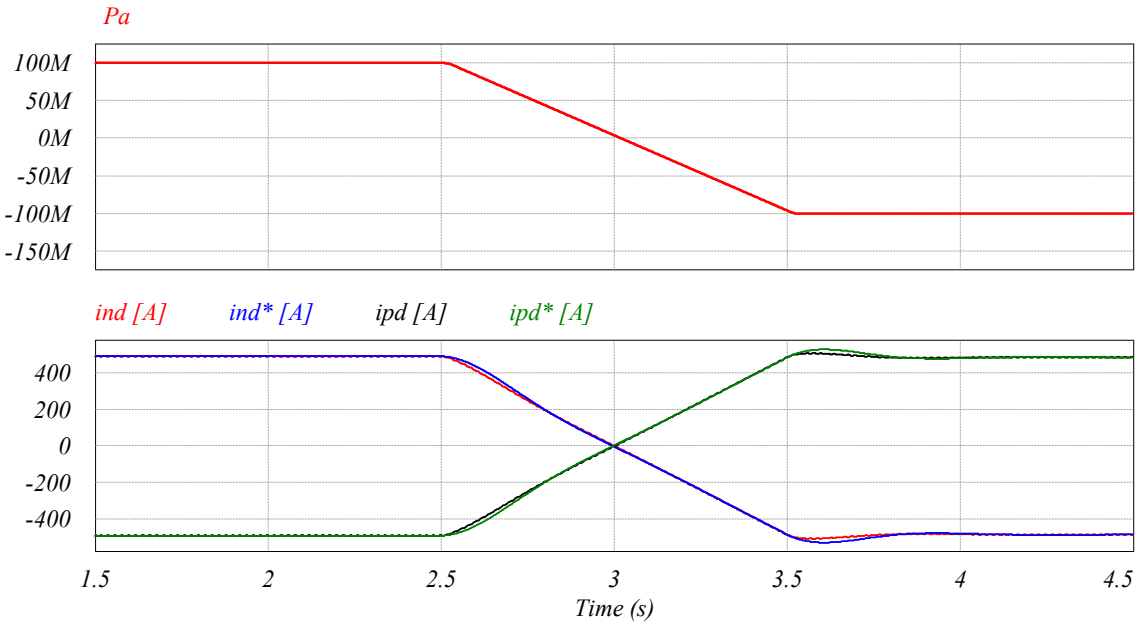


Figure IV-21: Output of the energy balancing controller and direct component of the current for the negative and positive part; power flow

The voltage value on the averaged cell capacitors is kept constant as shown in Figure IV-22.

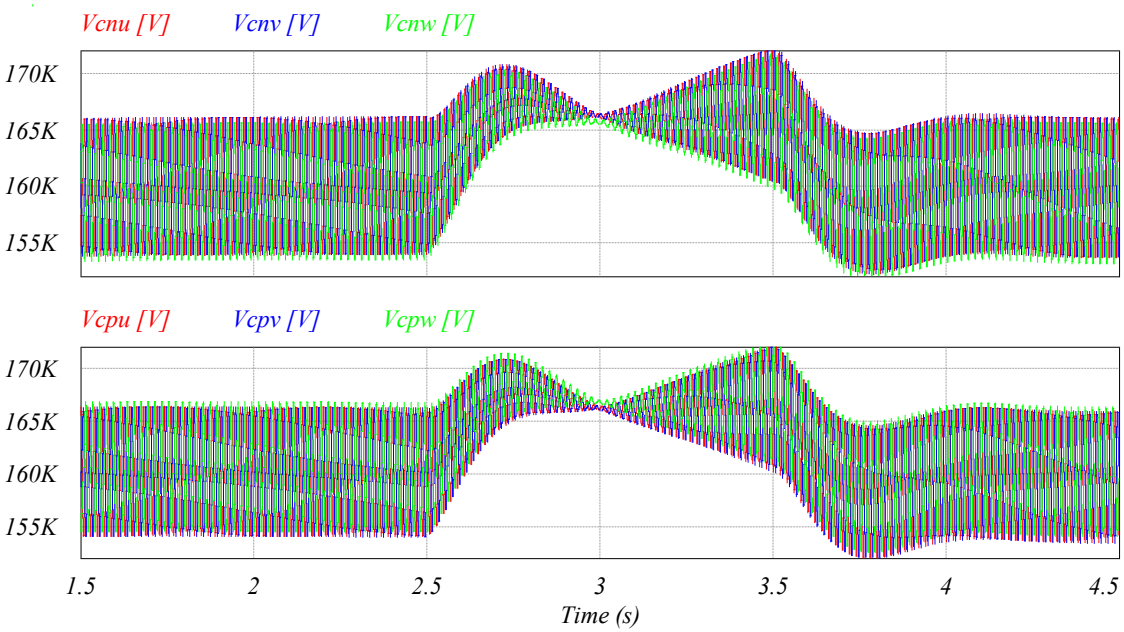


Figure IV-22: Averaged capacitor voltages

IV.2.4 Cell voltage balancing

To balance each cell on the desired voltage value a proportional corrector is chosen as was described in [63]. For each branch the controllers are achieved according to Figure IV-23. The control adds an offset dα to the duty cycle imposed by the previous controller and it is placed according to the control plant in Figure IV-3. Because the balance locally interferes on the single cell it is necessary to take in account the direction of the current. In this way, according to the references imposed in Figure IV-2, if the current is positive and the voltage of the cell capacitor is low, the regulator increases the time in which the capacitor is connected to the branch until when is reached the required value and vice-versa.

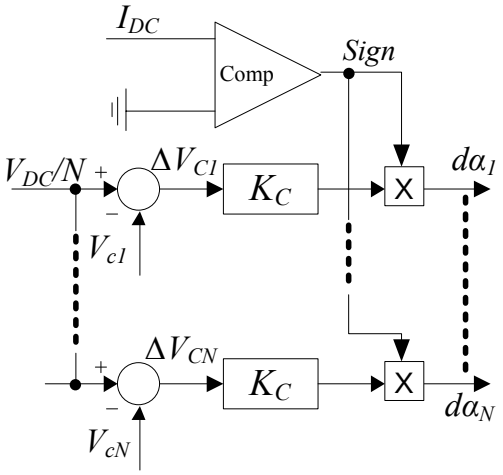


Figure IV-23: Capacitor voltage balancing diagram in a branch

The constant of the regulator k_C (145) is evaluated to achieve at most 5% of the maximum value of the duty cycle where ΔVCi is the amplitude of the capacitor voltage determined by the value of the capacitance of the cell (6 mF to achieve 10% of voltage ripple).

$$\frac{k_C \cdot \Delta V_{Ci}}{\alpha_{\max}} \approx 5\% \tag{145}$$

IV.2.4.1 Simulations

To perform the simulations, the instantaneous model in Figure IV-4 was considered. More details are reported in Table II-2. A resistance is imposed in parallel (2.5 kΩ) for a cell capacitor in order to unbalance its voltage V_{C1u} to 2375 V. On the other hand the energy balancing loop forces the voltage on another cell of the same branch, in this case V_{Cu2} , to increase up to 2625 V in order to reestablish the balance. The simulation view in Figure IV-24 starts with the cell balance enabling.

According the sign of the current, Figure IV-24 shows the intervention of the first regulator $d\alpha_{1u}$ in order to decrease the voltage amplitude by considering a positive DC current. The opposite intervention, for a less voltage amplitude, is carried out for V_{C2u} by $d\alpha_{2u}$. The same results, starting from the same capacitor voltage value, for a negative DC current are shown in Figure IV-25.

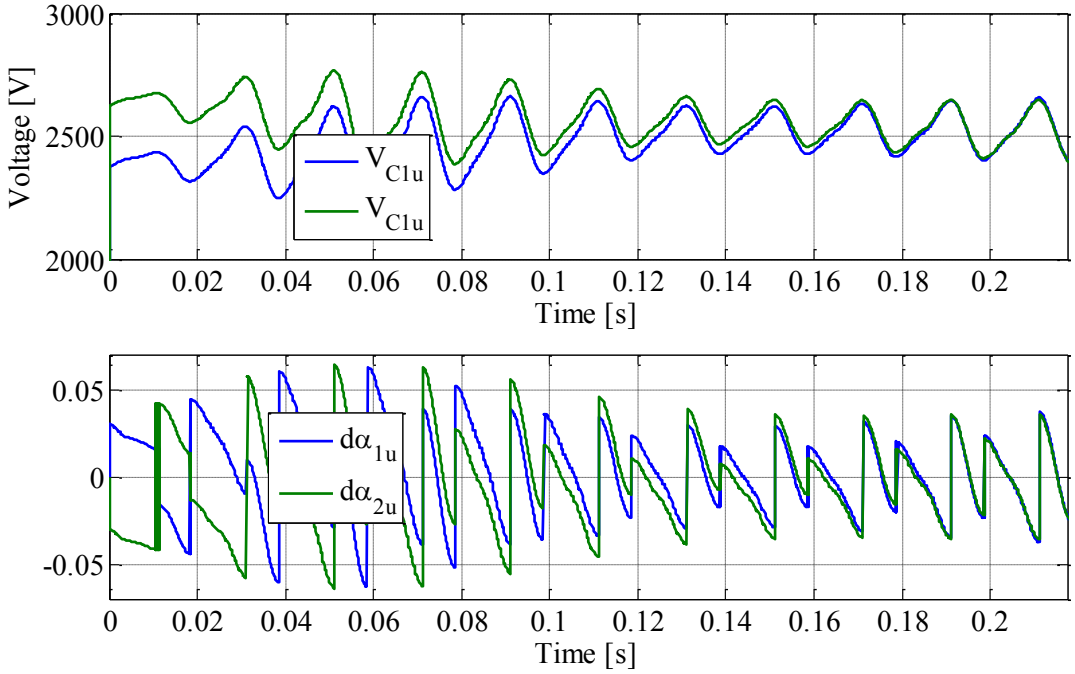


Figure IV-24: Capacitor voltages and outputs of the cell balancing regulator dα for a positive DC current

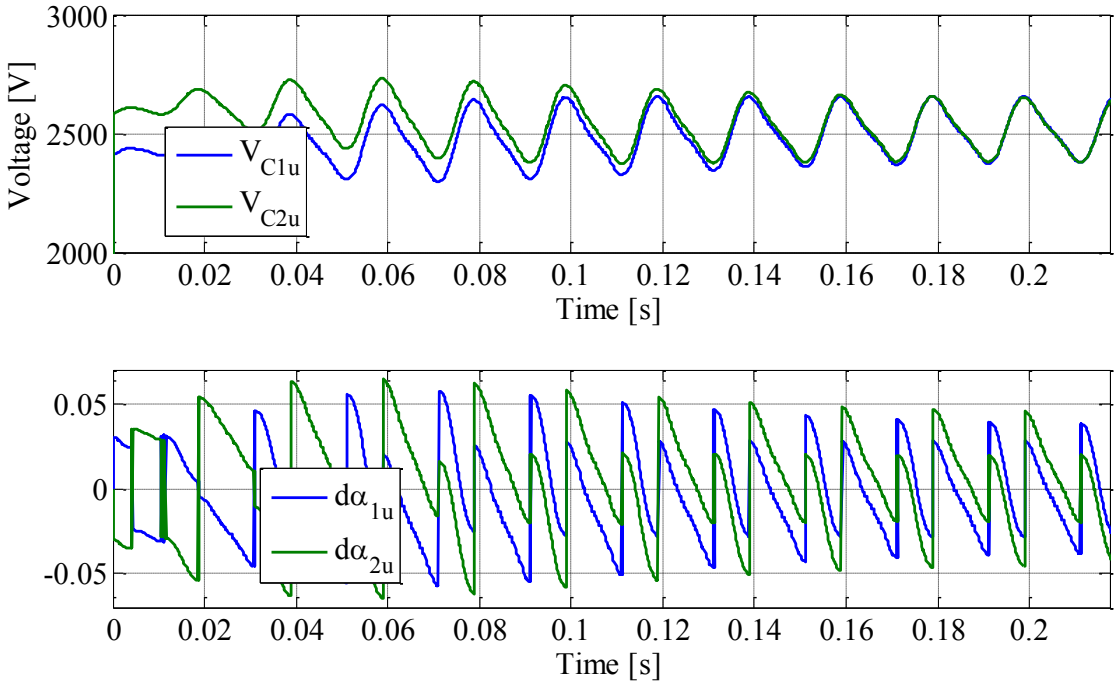


Figure IV-25: Capacitor voltages and outputs of the cell balancing regulator dα for a negative DC current

IV.3 Conclusions

For multilevel structures a very low switching frequency can be obtained for each elementary converter due to the phase shifted carriers of the PWM modulation. For a high number of levels however there is an inferior limit of the switching frequency per switching device. In fact the averaged value of the capacitor current of the elementary converter has to be kept at zero. This is guaranteed for a switching frequency not less than 200 Hz. This means that at current parity, the device losses can't be further reduced.

For staircase based modulations, particularly when the number of levels is very high, the equivalent switching frequency can be further reduced up to 90 Hz [75]. This improves performances of the devices in terms of losses.

For both the modulation techniques a centralized control is necessary. This means that all the signals of the system, currents and capacitor voltages, must be connected to a central controller. For a high number of levels a very complex hardware is required to wire each capacitor voltage to the central controller and, vice-versa, to wire the driving signal from the controller to the switching devices. For these reasons the trend could be to provide a central controller which manages just the control of the currents and each cell provides itself with voltage, maybe according the surrounding ones.

Chapter V. The 10 kW modular multilevel prototype

In order to validate the sizing of the components and the control approach a three phase prototype of 10 kW was made. The structure is composed of 18 elementary cells. Each cell is sized to sustain a 200 V capacitor voltage. IGBTs were chosen as switching devices.

The converter is configured to test the single loop structure proposed in the third chapter and then, to validate the control loop in the dq0 reference frame and described in the previous chapter.

In a first step, the converter was configured in a single loop structure using for each branch a RL load in series to the elementary cells. This is an intermediate configuration, which serves a double purpose. The classical MMC is well known for its much-reduced capability of limiting the branch current in faulty conditions [76]-[77] so it was not preferred for a first test. The RL series connected load instead limits the current in the branches by guaranteeing the setup of the signal chains and the validation of the synthesis of the regulators in safety conditions. Moreover, this configuration reinforced the study of the single loop topology for which experimental results are presented.

In a second step, the classical MMC is tested in open loop conditions and experimental results are reported.

V.1 The prototype configuration

The prototype was developed at the LAPLACE laboratory. It is a 10 kVA three-phase modular multilevel converter composed of 18 switching cells. On this basis each branch has 4 voltage levels (0, V_{DCcell}, $2V_{DCcell}$, $3V_{DCcell}$). Otherwise for a single loop configurations, two branches are directly in series and 7 voltage levels can be achieved (0, V_{DCcell}, …, $6V_{DCcell}$). A diagram of the converter is shown in Figure V-1. The layout also shows the installed voltage and current sensors. The rating data is summarized in TABLE V-1.

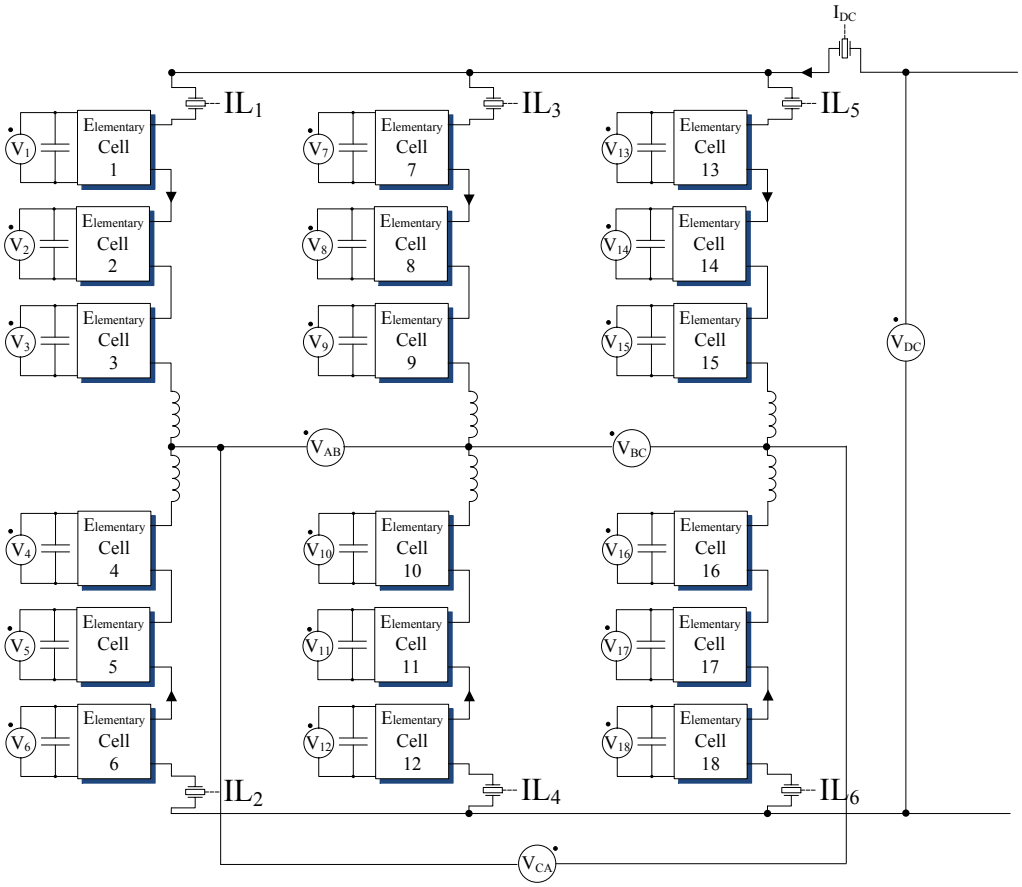


Figure V-1: Layout of the prototype

10 kW system		***The Power supply***	
Power Rate	10kVA	Model	TDK-Lambda ® Genesys
V_{DC}	600V	Power	5 kW
V_{DCcell}	200V	DC max. out voltage	600 V
L	5mH	DC max. out. current	8.5 A
C	2mF		
Cell f_{sw}	2kHz		
IGBT IRGP35B60PDPBF 60A 600V – TO 247 Case			

TABLE V-1: 10 kW system parametres

The power supply can reach up to 5 kW that is the half of the power rating of the system. This value is sufficient to achieve the preliminary tests which concern the set-up of the sensor chains and the validation of the control loops.

V.1.1 Reactive elements design

The design was achieved according to the considerations carried out in Chapter II. The value of the inductor L is chosen in order to limit the current ripple in the branch at switching frequency. Particularly, for this prototype a maximum current ripple of 10% was allowed.

v_u is the phase voltage imposed by the converter on each phase. Equation (146) considers a maximum modulation index M of 0.9.

$$V = 0.9\frac{V_{DC}}{2\sqrt{2}} = 190V \tag{146}$$

The rms current on the AC side at fundamental frequency can be expressed as (147) where P is the power of the converter.

$$I = \frac{P}{3V} = 17.5A \tag{147}$$

As previously evaluated, the inductor must respect the balance in (148), for practical reasons an inductance L=5 mH was chosen with a rating of 20 A

$$L > \frac{V_{DC}}{4N^2 f_c \Delta I_{\max}} = \frac{600}{8 \cdot 3^2 \cdot 2000 \cdot 2.4} = 3.4mH \tag{148}$$

A capacitor of 2 mF was chosen as it limits the voltage ripple at fundamental frequency under 10%.

Each cell is designed to require an optical signal for the driving of the semiconductor devices. The design of the frame, the PCB of the single cell, the arrangement of the sensors and the power supply for the signal management are described in Appendix A.

The final frame for the power side of the converter is shown in Figure V-2.



Figure V-2: Power Hardware frame

V.1.2 Hardware In the Loop configuration

In this section a description is given on the most important parts of the system, which allows the control implementation and tests.

As shown in Figure V-3, the configuration, besides the multilevel prototype, is composed of a HIL box, which allows implementing the control system through a PC. The HIL box accepts analogical signals and sends digital signals to the prototype through the interfacing hardware designed for the purpose.

The interfacing hardware allows managing the signals in two directions. In one direction it processes and adapts the analog signals coming from the prototypes' sensors for the HIL box input. In the other direction the interfacing hardware converts the digital drivers coming from the HIL box in optical signals to control the cells. A more detailed description of these components is given in Appendix A.

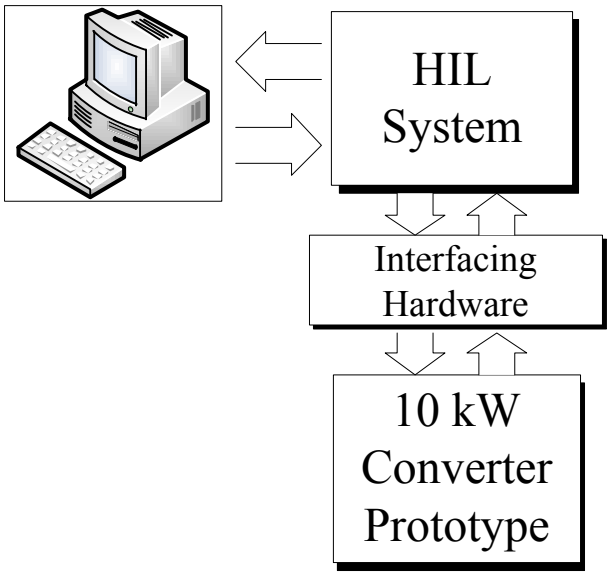


Figure V-3: HIL configuration Lay out

The final assembly of the system with a passive RL load is shown in Figure V-4.

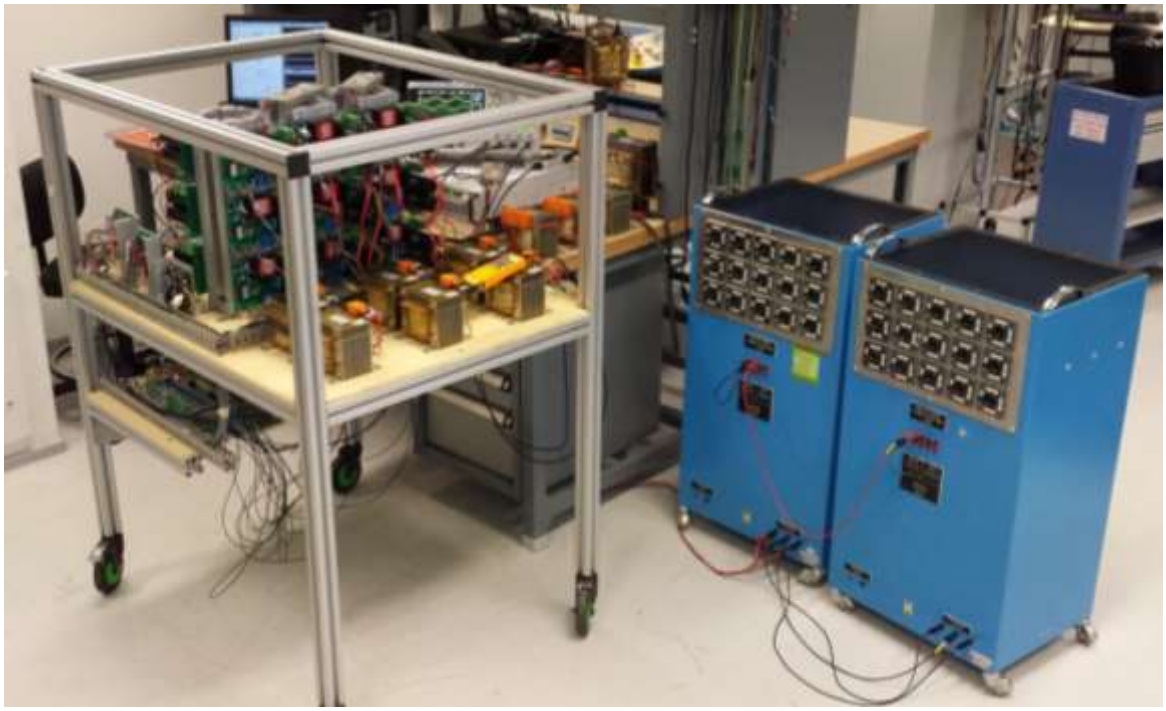


Figure V-4: Final assembly for the system

In the next section the modular structure is configured in single loop modality. A passive load is connected to the system. After a brief explication of the load choice, the control approach is shown and the synthesis of the regulators is carried out. Experimental results are used to validate the study.

V.2 Single Loop Configuration

The structure is organized as shown in Figure V-5. Due to the unipolar proprieties of the single cell this system imposes also a DC component on the load. For this reason this arrangement can be considered a preliminary configuration before connecting the zig-zag transformer introduced in Section III-2.

The configuration was useful to set-up the sensors and to confirm the good correspondence between the simulations and the experimental results with respect to the regulator synthesis. For the tests, a 4 kW three-phase load was used.

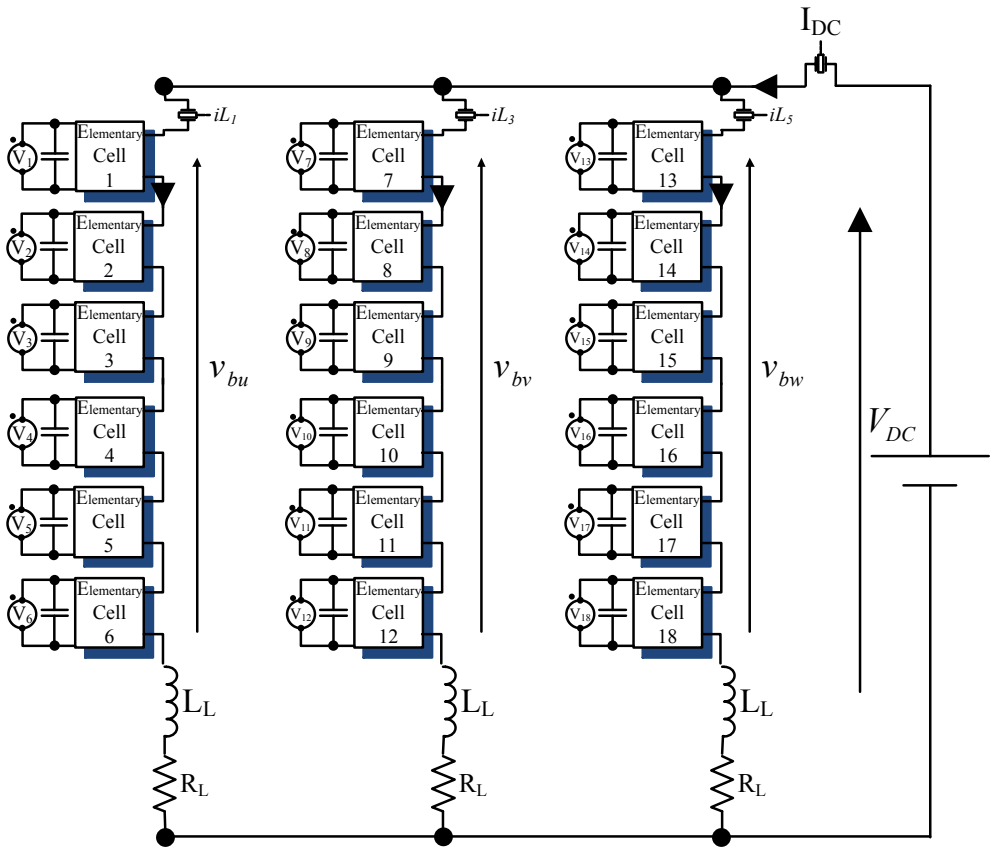


Figure V-5: Prototype in Single Loop Configuration

In order to evaluate the value of the resistance R_L to achieve the fixed power, the branch currents (149) and voltages (150) are defined by neglecting the voltage drop on the inductor.

$$\begin{cases} i_{L1} = \dfrac{I_{DC}}{3} + I\sqrt{2}\sin(\omega_0 t - \varphi) \\ i_{L3} = \dfrac{I_{DC}}{3} + I\sqrt{2}\sin(\omega_0 t - \varphi - \dfrac{2}{3}\pi) \\ i_{L5} = \dfrac{I_{DC}}{3} + I\sqrt{2}\sin(\omega_0 t - \varphi + \dfrac{2}{3}\pi) \end{cases} \quad (149) \qquad \begin{cases} v_{bu} = V_{DC} - V\sqrt{2}\sin(\omega_0 t) \\ v_{bv} = V_{DC} - V\sqrt{2}\sin(\omega_0 t - \dfrac{2}{3}\pi) \\ v_{bw} = V_{DC} - V\sqrt{2}\sin(\omega_0 t + \dfrac{2}{3}\pi) \end{cases} \quad (150)$$

The power of each branch is balanced according to (151) (in each cell AC and DC power must be balanced according to III.1), so the balance for the total active power is given by (152). By considering a SPWM modulation and the relationships achieved in Chapter II for the single cell, *M* is considered the amplitude of the modulation index.

$$P_{DC}^{cell} = -P_{AC}^{cell} = -VI; V = \frac{V_{DC}}{2\sqrt{2}}M \quad (151)$$

$$V_{DC} \cdot I_{DC} = 3P_{cell} + 3 \cdot R_L \frac{I_{DC}^2}{9} + 3 \cdot R_L I^2 + 3 \cdot VI \Rightarrow V_{DC} \cdot I_{DC} = +3 \cdot R_L \frac{I_{DC}^2}{9} + 3 \cdot R_L I^2 \quad (152)$$

By taking in account (151), in (153) the value of I is reported.

$$I = \sqrt{2}\frac{I_{DC}}{3M} \quad (153)$$

By substituting (153) in (152), (154) is achieved.

$$V_{DC} = R_L I_{DC}\left(\frac{1}{3} + \frac{2}{3M^2}\right);\ R_{eq} = R_L\left(\frac{1}{3} + \frac{2}{3M^2}\right) \quad (154)$$

So the control matches the impedance through the variation of *M* in order to achieve the required power.

In this case R_L is defined by the resistor bench available in the laboratory which allows up to 4 kW operating power. According to the relationships achieved before, TABLE V-2 reports the main operating parameters. The inductor L_L was chosen to test the good current ripple around the 5%.

Single loop system parameters	
Operating power	4 kW
V_{DC}	600 V
R_L	40 Ω
R_{eq}	90 Ω
I_{DC}	6.7 A
M	0.6
L_L	5 mH
Number of cells N per branch	6

TABLE V-2: system parameters for the single loop configuration

In the next section the control approach is described and the synthesis of the controller is carried out.

V.2.1 The control

A simple *u, v, w* frame is considered and a superposition approach is used to simplify the study. By considering the averaged model, the DC current loops are shown in Figure V-6 while the AC loops are reported in Figure V-7.

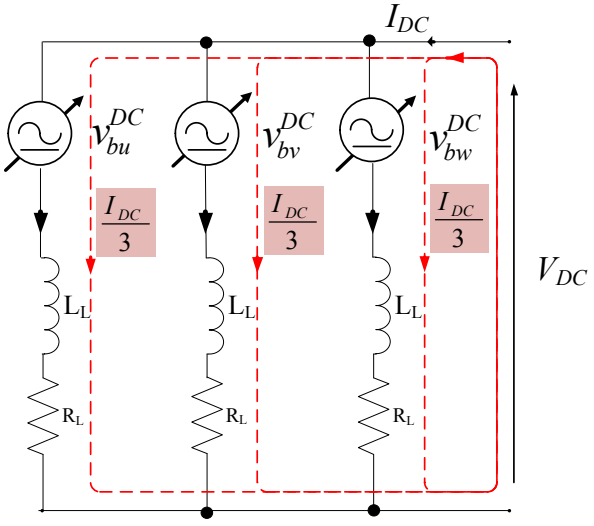


Figure V-6: Layout of the DC part of the system

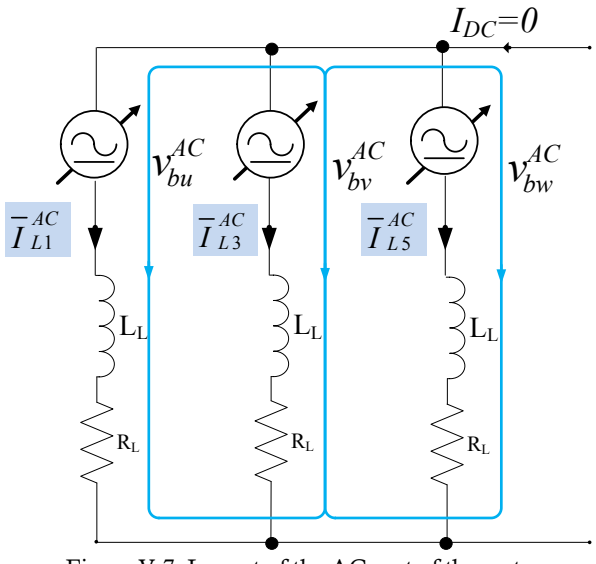


Figure V-7: Layout of the AC part of the system

By considering the single cell topology the voltage imposed by each branch is reported in (155) according to the averaged system in Figure V-8 for a generic phase (*u, v* or *w*). On the DC approach, the branch imposes the voltage to balance the DC side according to (156). The AC voltage value is determined by the modulation index M given in (157). The voltage on the equivalent capacitor is provided by (158).

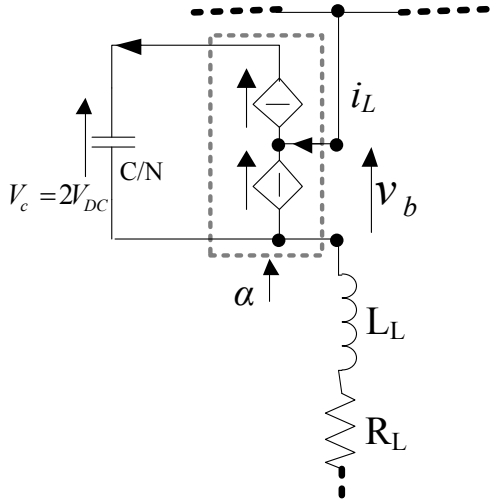


Figure V-8: Averaged model of the branch cells

$$v_b = \frac{NV_C}{2} \cdot \left(1 + M \sin(\omega_0 t)\right) \quad (155)$$

$$v_b^{DC} = V_{DC} \Rightarrow NV_C = 2V_{DC} \quad (156)$$

$$v_b^{AC} = M \cdot NV_C \sin(\omega_0 t) \quad (157)$$

$$V_C = \frac{1}{N}\sum_{j=1}^{N} V_{Cj} \quad (158)$$

According to the control strategy for the multilevel structures depicted in Figure IV-3 (previous chapter) PI regulators are synthetized.

The current control loop is highlighted in Figure V-9, where in this case the gain of the system is $2V_{DC}$. The PI regulator is synthetized in order to achieve a crossing frequency of 1 kHz while the time constant is defined to achieve a phase margin of 60° in order to guarantee the stability.

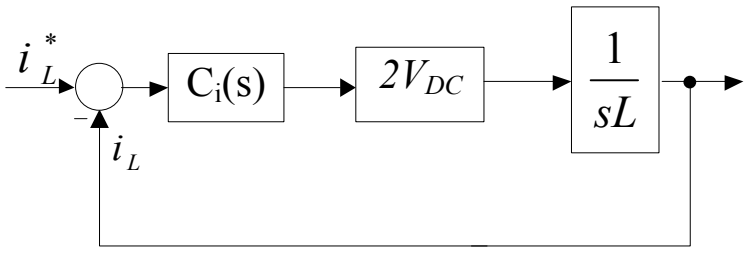
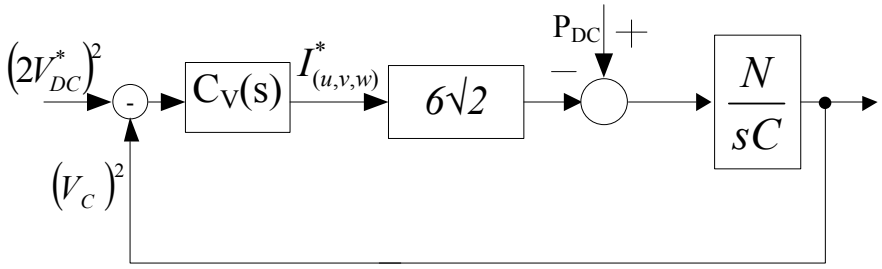


Figure V-9: Current control loop

The branch energy balancing generates the active reference current necessary to keep a total voltage on the capacitors of $2V_{DC}$ where C/N is the equivalent capacitance of each branch. The PI regulator is chosen to achieve a low crossing frequency by ensuring the stability.



By considering the instantaneous model, the same strategy already described in the previous chapter was adopted to keep a constant voltage of $2V_{DC}/N$ on each cell capacitor. This because the cell voltage balancing is a parallel loop which depends neither from the current nor from the branch energy balancing loops but it directly interferes on the modulation index. One more time each cell capacitor has 200V voltage.

V.2.2 Simulations

For the single loop system previously described, TABLE V-2 reports the main parameters and its layout is highlighted in Figure V-5.

The levels imposed by the cells (Figure V-10) in the system are limited to 5 levels because the modulation index M is equal to 0.6. The maximum number of levels 7 is reached for a value of M almost equal to 1.

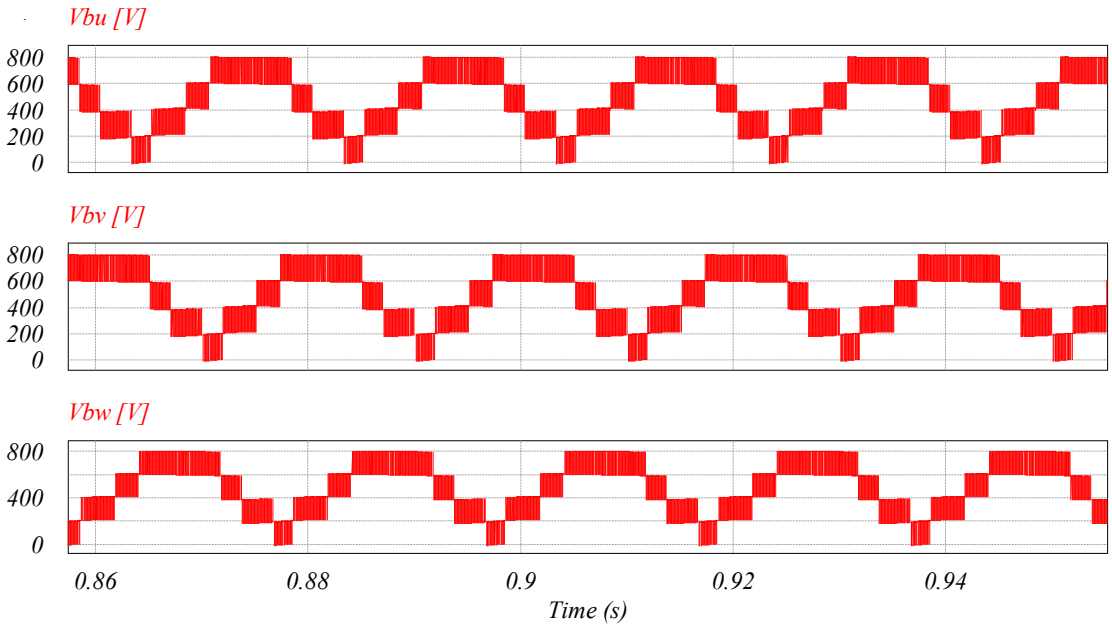


Figure V-10: Voltage imposed by each branch

The currents in the branches and the DC current are shown in Figure V-11. The current ripple, kept below the desired value, confirms the right evaluation of the branch inductor.

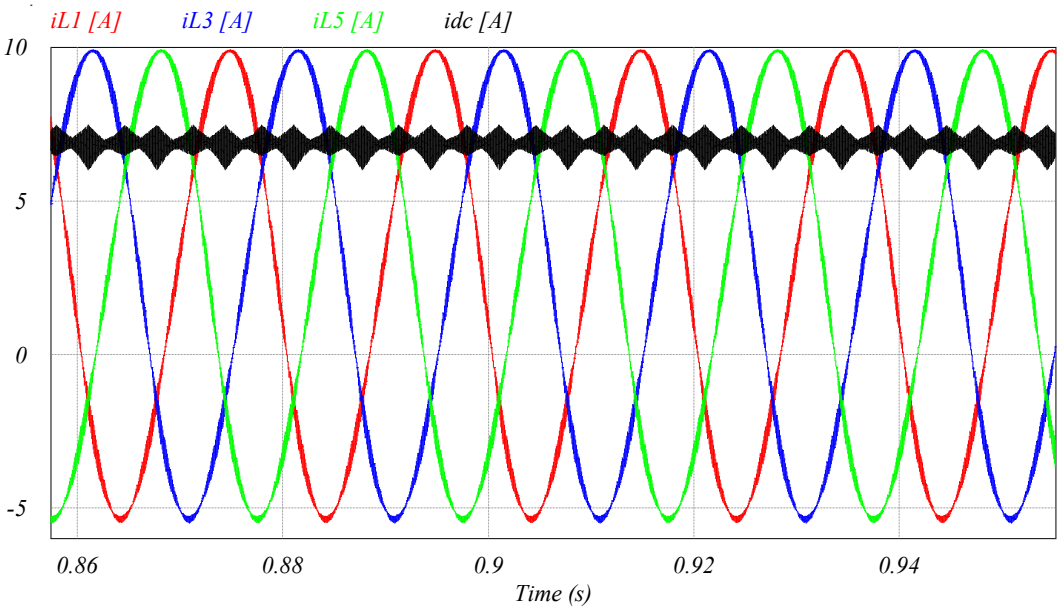


Figure V-11: Branch currents and DC current

The voltage on the cell capacitors kept at the desired value validates the single cell balancing as shown in Figure V-12.

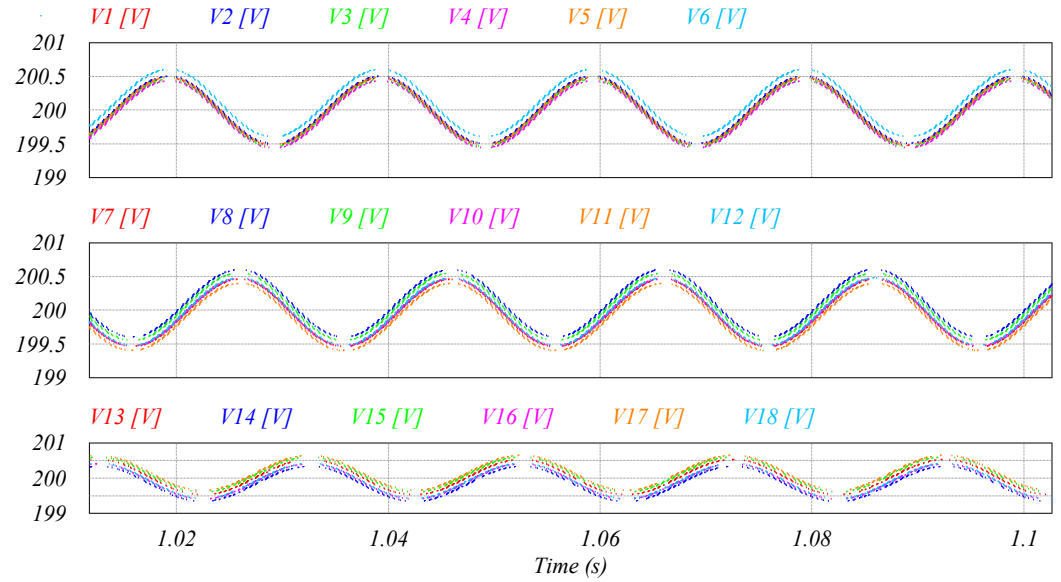


Figure V-12: Voltages on the cell capacitors

The performed simulations validate the study for this configuration of the system. Experimental results are reported in the next section.

V.2.3 Experimental results

The tests confirm the good operation of the sensor chains and the good synthesis of the regulators. The acquisitions are displayed by considering a time scale of 5ms/div.

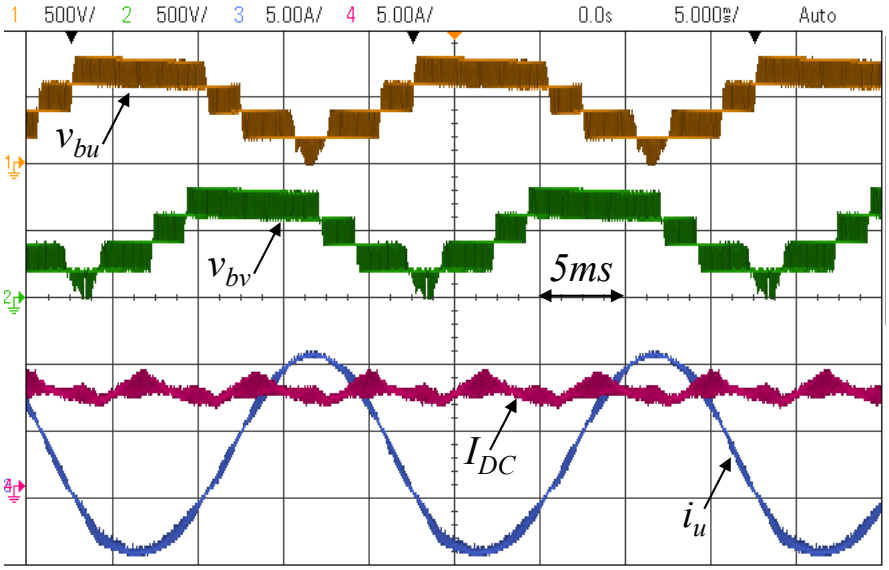


Figure V-13: Branch voltages and currents on DC side and phase u.

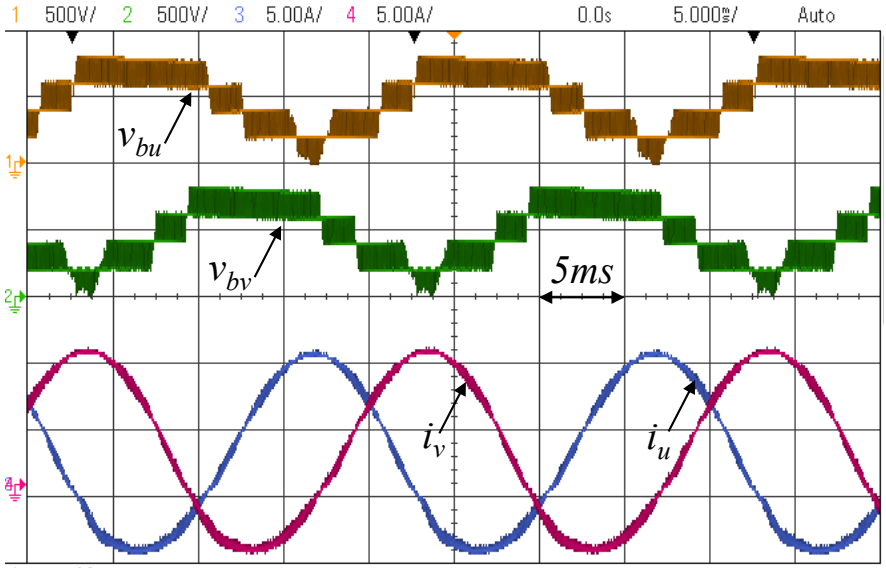


Figure V-14: Branch voltages and currents

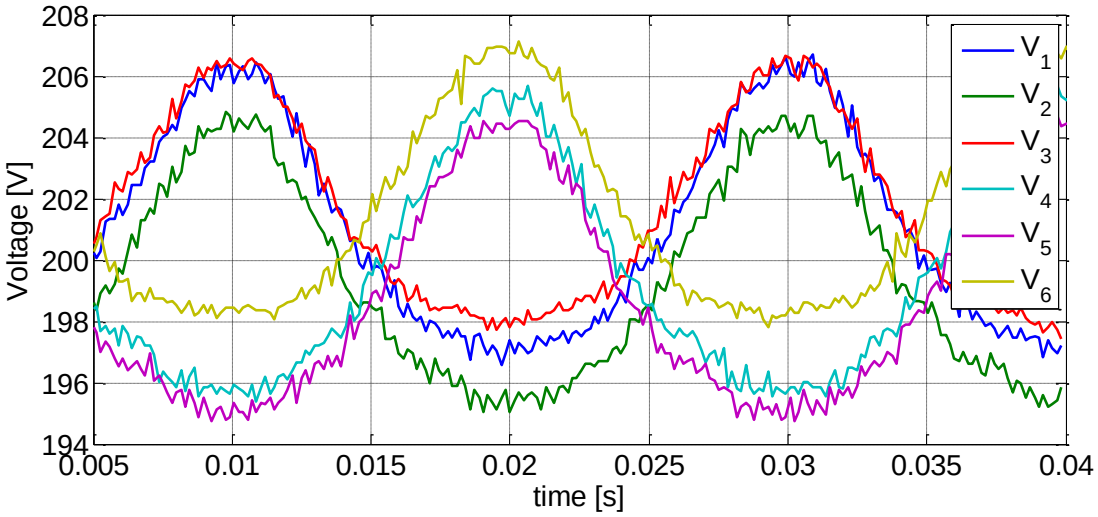


Figure V-15: Cell capacitor voltages

The experimental results seem to match quite well with the simulations. The voltages imposed by the branches confirm one more time the correct phase shift between the carriers. Moreover all the levels are not reached because the amplitude of the modulation index is around 60%. The achieving of the power required validates the good choice of gains for both the regulators for the energy balancing and current loops. The stability of the system is guaranteed by the phase margin which validates the values of the time constants. Finally the parallel loop for the cell voltage balancing interferes without influencing the stability.

V.3 MMC configuration

The MMC configuration of the prototype is considered. For the simulations in closed loop, the multilevel structure is connected to a three-phase voltage source (Figure V-16). For the experimental results, an open loop control is considered with a RL load (Figure V-20).

V.3.1 Simulations in Closed Loop operation

Because of the network connection the simulations were performed for the full 10kW power system of which parameters are reported in V.1. An excursion is carried out at unity power factor by leading the system during operation from inverter to rectifier mode.

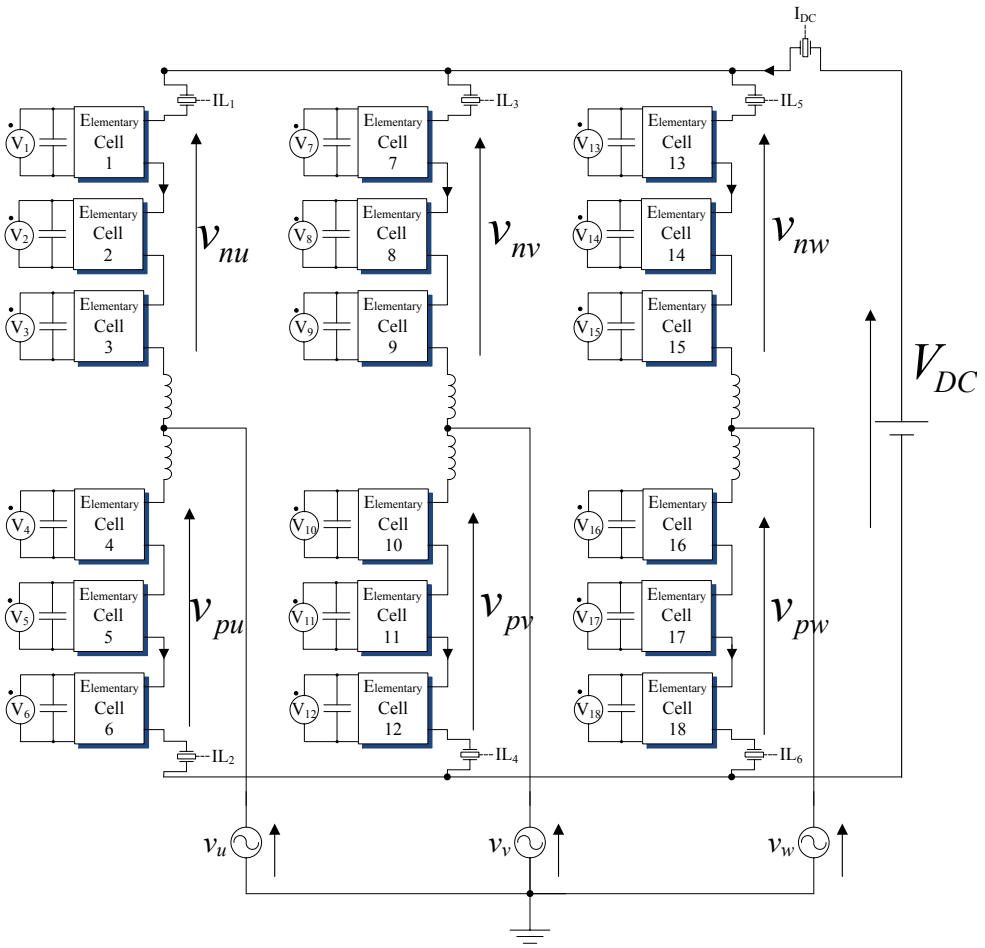


Figure V-16: MMC system configured for the simulations

The u, v, w currents are shown in Figure V-7. During the excursion the stability of the system is maintained. Also the stability of the DC current confirms the good synthesis of the current regulators. Moreover the right active power is required by the regulator synthetized for branch energy balancing loop.

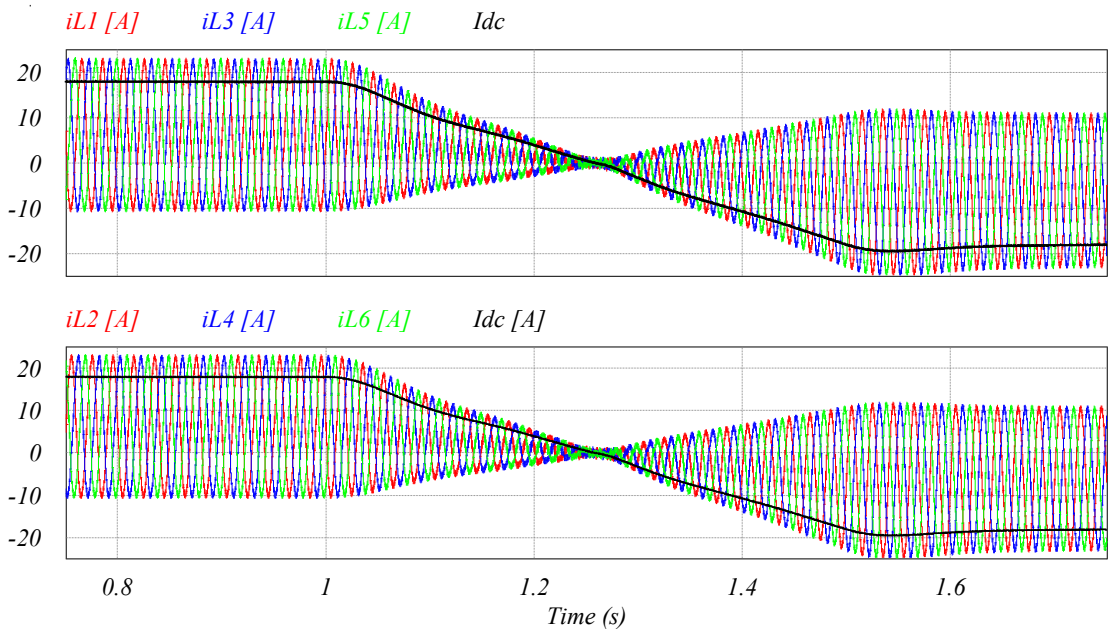


Figure V-17: Branch currents and DC current

The branch voltages in Figure V-18 show how all the four switching levels are reached. This validates the good phase delay between the SPWM modulation carriers.

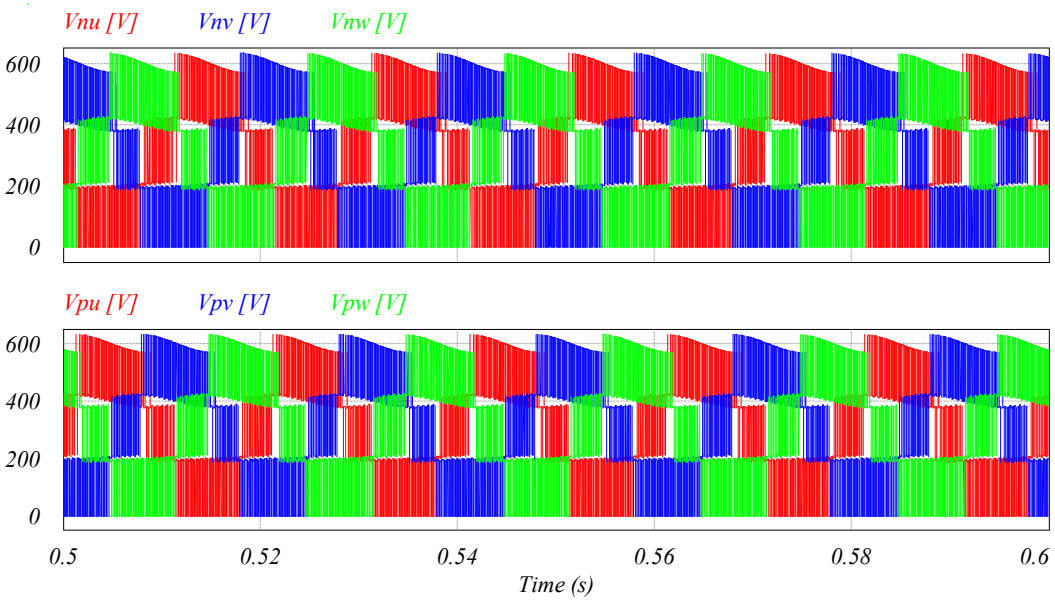


Figure V-18: Voltages imposed by the branches

Finally the averaged voltages on the cell capacitors are kept on 200 V. This validates the balancing of the single cell voltage.

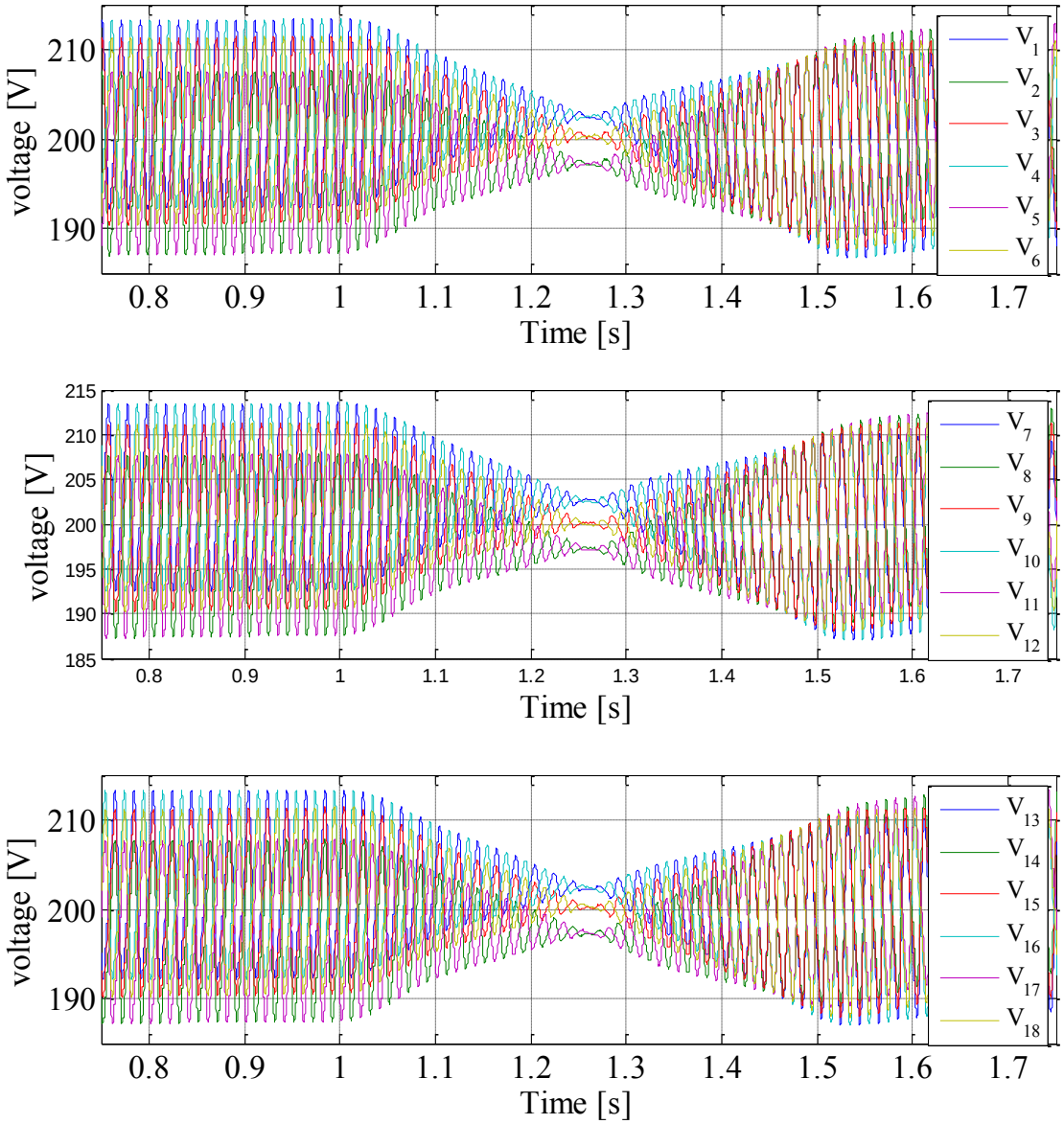


Figure V-19: Voltages on the cell capacitors

V.3.2 Open Loop-Tests

The tests were carried out for the maximum capability of the power supply (5 kW). The MMC configuration is connected to the RL load according to the layout shown in Figure V-20. The resistive load is composed of two 4 kW test benches in parallel to achieve the power

necessary for the tests. The final resistance star configured has a 40 Ω value in order to achieve 4.8 kW.

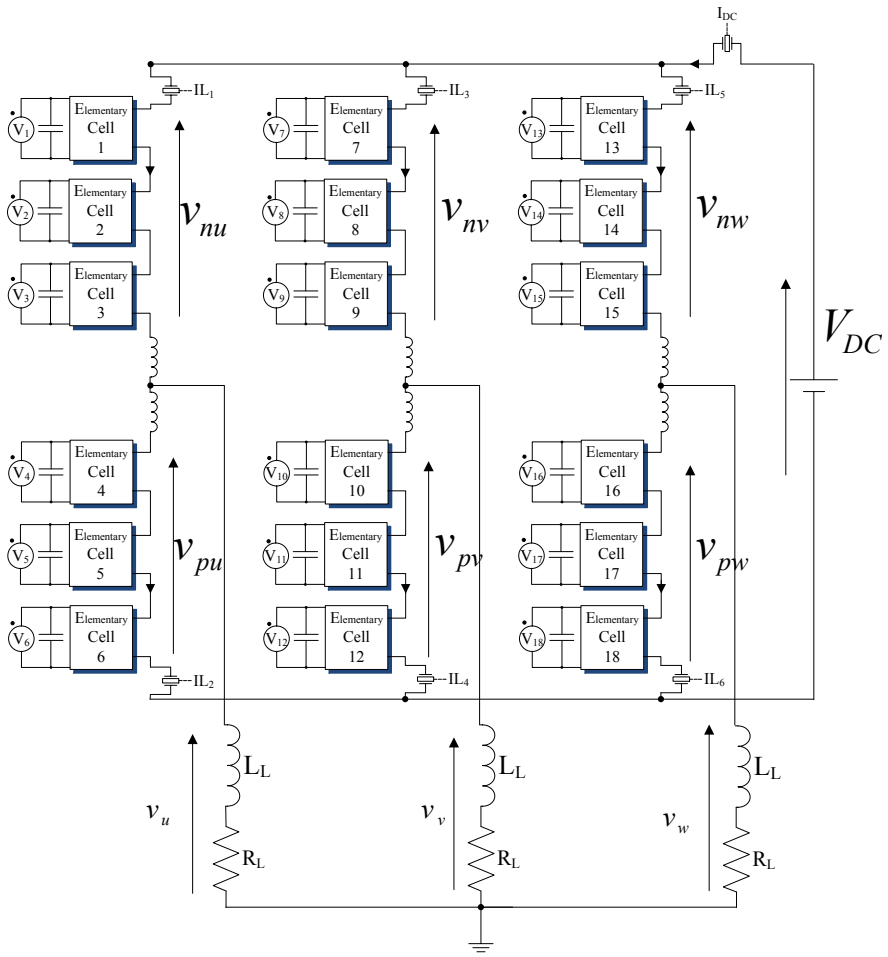


Figure V-20: MMC system configured for the experimental tests

The currents in the negative branches are depicted in Figure V-21. In open loop each branch current presents a DC and a second harmonic component of the fundamental. .

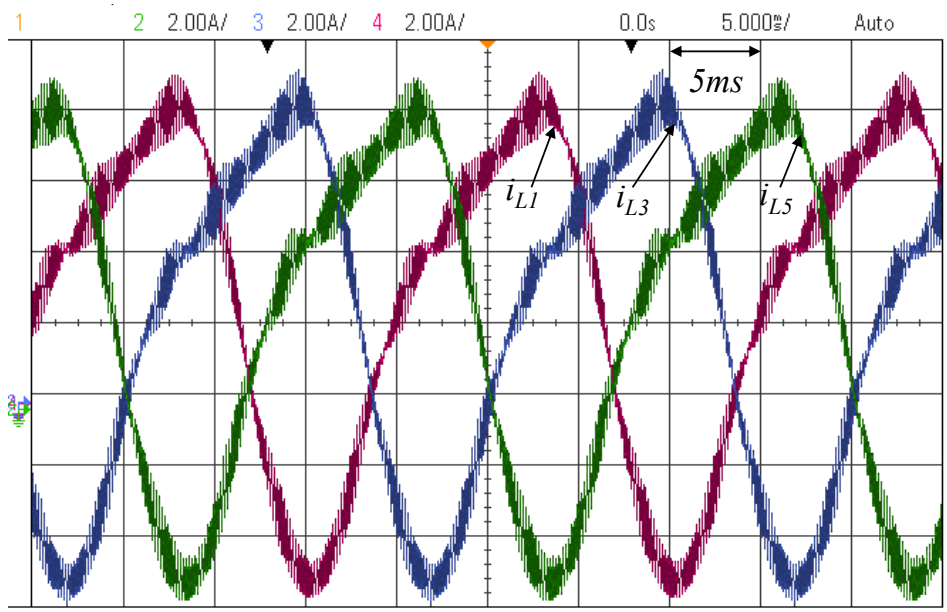


Figure V-21:Negative branch current

As shown in Figure V-22, the currents in the negative and positive branches are in phase opposition in terms of fundamental component. Also the sum between them is reported according to the references shown in Figure V-20. The sum has a DC and a second harmonic component which has to be suppressed by the closed loop control.

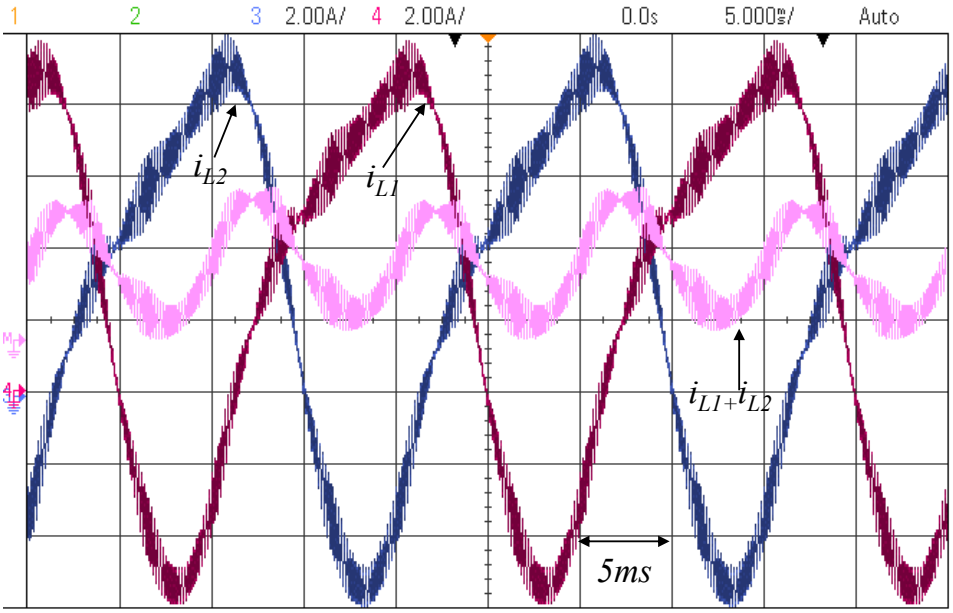


Figure V-22: Negative, positive branch current and the sum

The value of the DC current around 8A confirms an operating power of the system around 4.8 kW (Figure V-23). The output AC currents (Figure V-23) have a sinusoidal waveform. This means that both the components DC and second harmonic are kept in the branch for each phase. The current ripple is further reduced because of the phase shift modulation technique. In fact the group of carriers for the cells of the positive part is phase shifted respect to the group of the negative part.

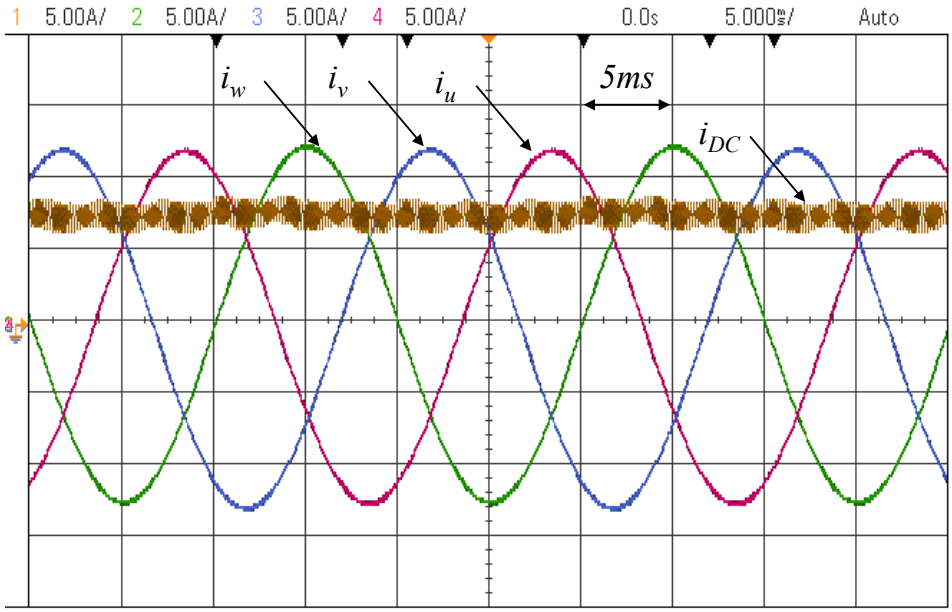


Figure V-23: Output AC currents and DC current

The 4 voltage levels achieved for the branch voltages validate the correct phase shift among the carriers of each cell (Figure V-24).

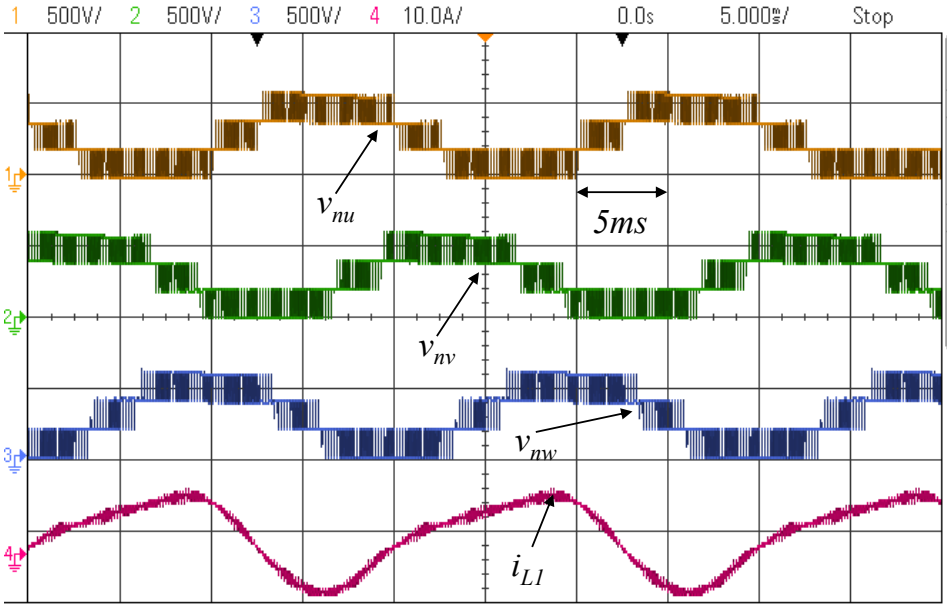


Figure V-24: Negative branch voltages and current in the negative branch

Figure V-25 shows the positive and negative branch voltages for the u-phase. As expected the voltages have the same DC component. The AC components complement each other at the fundamental frequency.

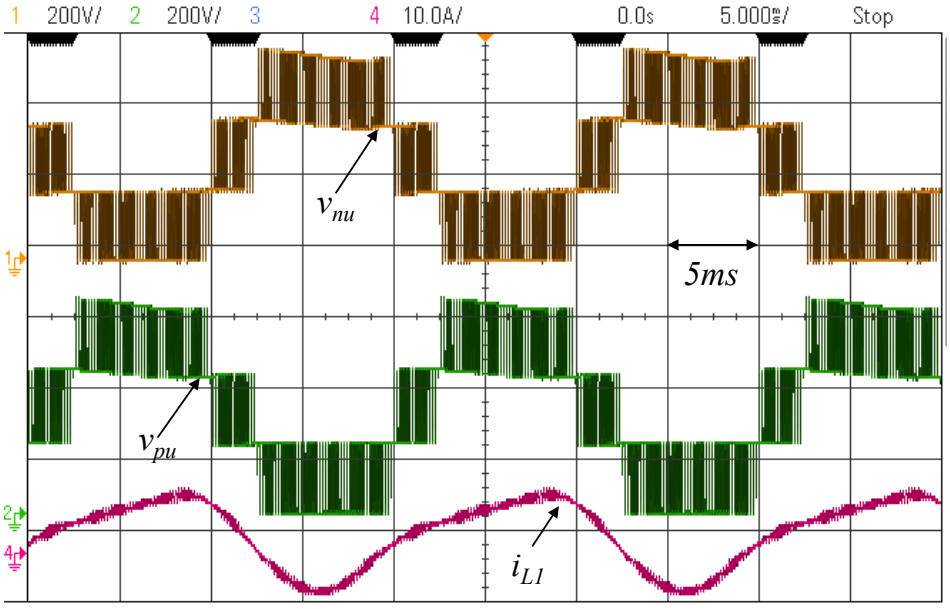


Figure V-25: Negative and positive branch voltages, branch current

The zoom of Figure V-25 shown in Figure V-26 validates the right phase shift between the cells of the negative branch and the cells of the positive branch. Furthermore, the current ripple amplitude confirms the right sizing of the branch inductors which guarantees a current ripple under 10% (the inductor is rated for a current of 20 A).

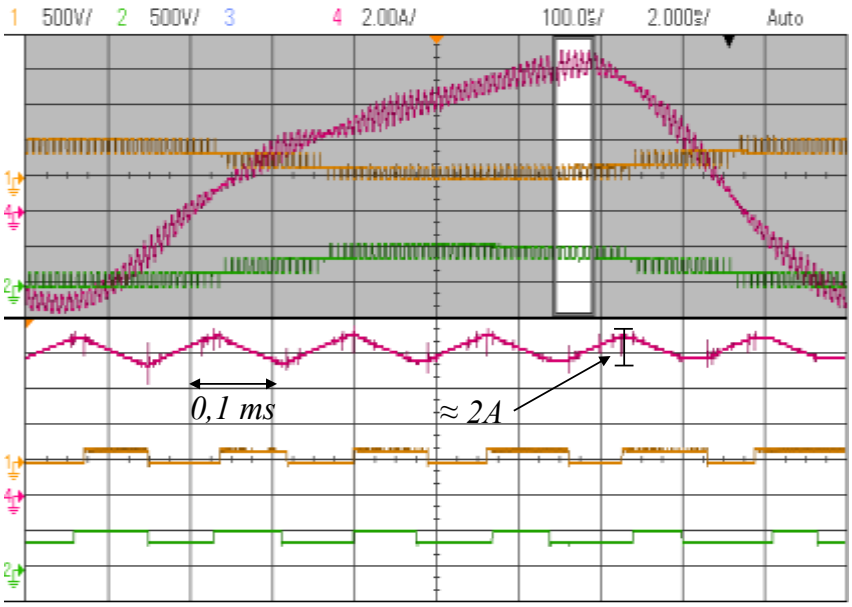


Figure V-26: Zoom on voltage and current waveforms

Finally some capacitor voltages are shown in Figure V-27. The voltages are balanced between them, they have the same DC component value of 200 V.

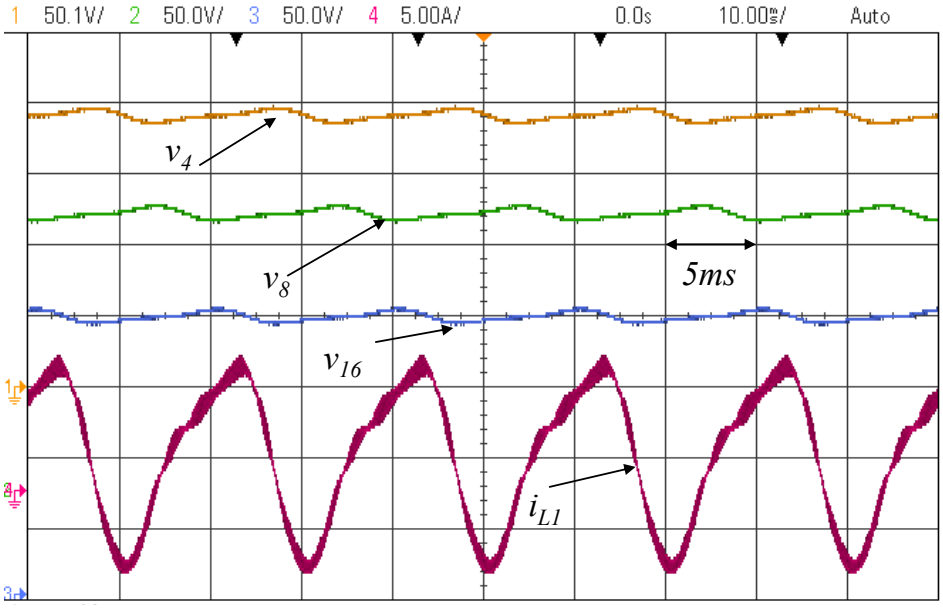


Figure V-27: Capacitor voltages and branch current

V.4 Conclusions

Experimental validations for the single loop structure will allow an immediate transition to the configuration with the zig-zag transformer. The closed loop tests ensured the good correspondence between the sensors and the input analog signals to the controller (HIL Box). Moreover, each output modulation signal coming from the controller drives the right device. The wiring of the switching signals by optical fiber considerably reduced the EMI problems.

The stability of the tested closed loop system validates the reliability of the simulation results by confirming the right synthesis of the regulators. This aspect will facilitate the closed loop tests for the MMC structure. Of course this case is always more dangerous just because the branch inductor limits the current in emergency conditions (divergence of the control, faults etc). These tests will be performed in the coming month.

Conclusions & Future Prospects

Nowadays HVDC connections are an appropriate answer to the more and more increasing world energetic demand. Multilevel topologies are going to make VSC converters the most employed in HVDC systems. The development of high voltage controlled turn-off devices made these structures very attractive. On the other hand because of advantages coming from the easily series connections of thyristors, CSC structures can better manage high voltages. In the near future, the gap between VSC and CSC structures will be much reduced thanks to the performances offer by IGCT devices in terms of on-state current rating and blocking voltage. The press packaging leads a series of advantages respect to the classical modules especially in fault condition where there is a risk of explosion. The single wafer feature makes the IGCT more suitable for the press pack packaging respect to the IGBT. For these reasons the IGCT seems to be the most attractive device in VSC-HVDC applications.

This thesis focused on the VSC based Modular Multilevel Structure. For preliminary studies the "macro-model" allowed direct evaluations and very fast simulations especially as this model is not dependent on the elementary converter topology.

The rating of the system was carried out through two control approaches. The first considers just a control on the AC output current which leads to a huge second harmonic current in the branch. We showed that Coupled inductors could be a good solution to limit this current but in the field of high power applications, the particularity of this hardware increases absolutely the cost. Thus, the second approach consists in a control of each current in the branch, despite it requires a more efficient control system based on a dq reference frame. Under this condition the second harmonic component of the current is cancelled which cut down the rating of the passive components.

The employment of different topologies as elementary converter made the MMC more flexible in terms of voltage and current reversibility. In terms of losses at parity of power and DC voltage, the simple cell is more convenient. Unlike topologies which provide bipolar voltage (Asymmetrical HB and full H-bridge) make the structure able to limit the short-circuit current in case of fault on the DC link.

The Phase Shifted PWM led to a reduction of the switching frequency and then the semiconductor losses. Of course this modulation technique presents an inferior limit on the switching frequency. When the number of levels is very huge the staircase modulation could be very attractive for multilevel structures. A study of the staircase modulation for the MMC structure is going to be soon developed. In fact an investigation on the influence of the modulation versus the rating of the reactive elements and versus power losses of the devices compared to the PS PWM left to be done.

Few aspects could make the Asymmetrical HB attractive in terms of HVDC applications. If this topology is chosen, the cell capacitor can be reduced at parity of voltage ripple amplitude.

Since the system achieves the inversion of the power flow by changing the polarity of the DC voltage, this topology can be employed to replace CSC based HVDC power stations with the advantage of a unit power factor operation.

The new single loop structure proposed in chapter III allows an easier control system. The topology does not require the double branch inductor because it uses the leakage inductor of the zig-zag coupling transformer. Although this coupling requires more copper than a classical winding, the insulation of the transformer has to be rated only for the AC voltage. This is not the case of a classical MMC arrangement where the transformer has to sustain a DC insulation half of the DC voltage (DC zero sequence component). Beyond these considerations, the use of this new structure could become very attractive to upgrade old rectifiers by guaranteeing advantages coming from VSC structures.

A 10 kW prototype was developed in the LAPLACE laboratory. In order to interface the power circuit with the Hardware In the Loop system a boards console placed on the frame called "Interfacing Hardware" was achieved. The interfacing hardware adapts the voltage levels of the signals coming from the sensors of the prototype to the input voltage level at of the HIL box. Moreover it provides also the noise filtering for the analogical signals. Even for the output digital signals coming from the HIL box an electric-optical conversion is provided by the Interfacing Hardware to control the cells.

Before starting the power tests, a preliminary procedure was carried out. All the sensors were calibrated and the good wiring of the signal chain was verified. Finally the optimization of the grounding configuration of all the system was improved step by step in order to avoid EMI problems.

Experimental validations in SPWM were achieved for the single loop topology and the classical structure. The good operation of the control loops validated the system modeling approach and the regulator synthesis.

In the near future, this prototype will allow testing the single loop structure with the zig-zag transformer, the closed loop operation in a dq frame and the staircase modulation.

APPENDIX A - The Prototype: Design & Development

A.1 The Elementary cell

In this section the elementary switching cell of the MMC converter prototype is described. A simple scheme is reported in Figure A - 1.

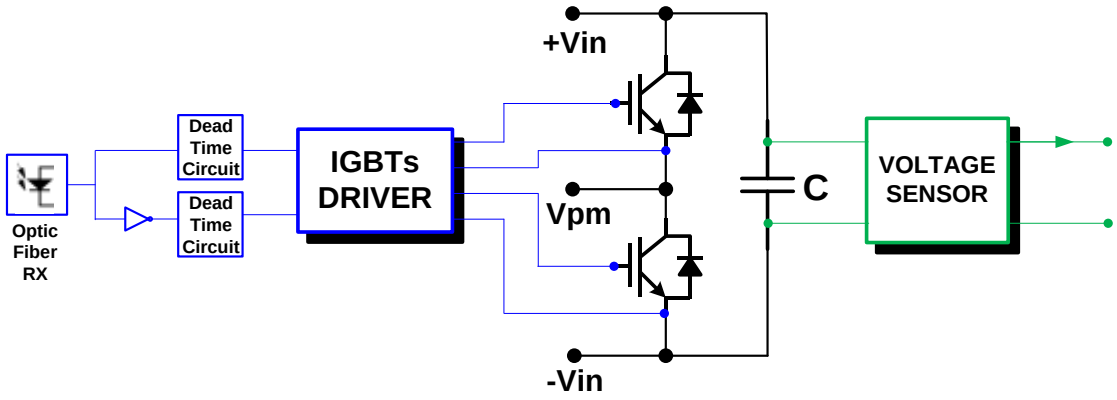


Figure A - 1: Scheme of the elementary switching cell

Each of the 18 switching cell is composed by the following main components:

- 2IGBT IRGP35B60PDPBF 60A 600V – TO 247 Case
- 1 IGBTs Driver CONCEPT 2SC0108T
- 1 Voltage sensors
- 1 Capacitor 2mF (2x1mF) (450V)
- 1 optic fiber receiver for switching signal
- Power supply TRACO TMS 15215

The elementary switching cell is equipped by a single optic fiber receiver. On the cell, a logic circuit generates the 2 complementary switching signals for the BOT and the TOP IGBT. Moreover, a circuit for managing the dead time is present. Particularly this is designed to give a dead time of 2μs.

Each cell is equipped by a LEM voltage sensor that measures the capacitor voltage. The LEM sensor gives the measure in current. It is designed to give 25mA for a measured voltage of 200V.

All the electronics on the PCB is supplied by a TRACO connected to the 230V 50Hz network.

Figure A - 2 shows the dimensions of the cell PCB with the components disposition. Moreover Figure A - 3 and Figure A - 4 report the TOP and BOTTOM layers of the PCB. The final realization for the cell is reported in Figure A - 5.

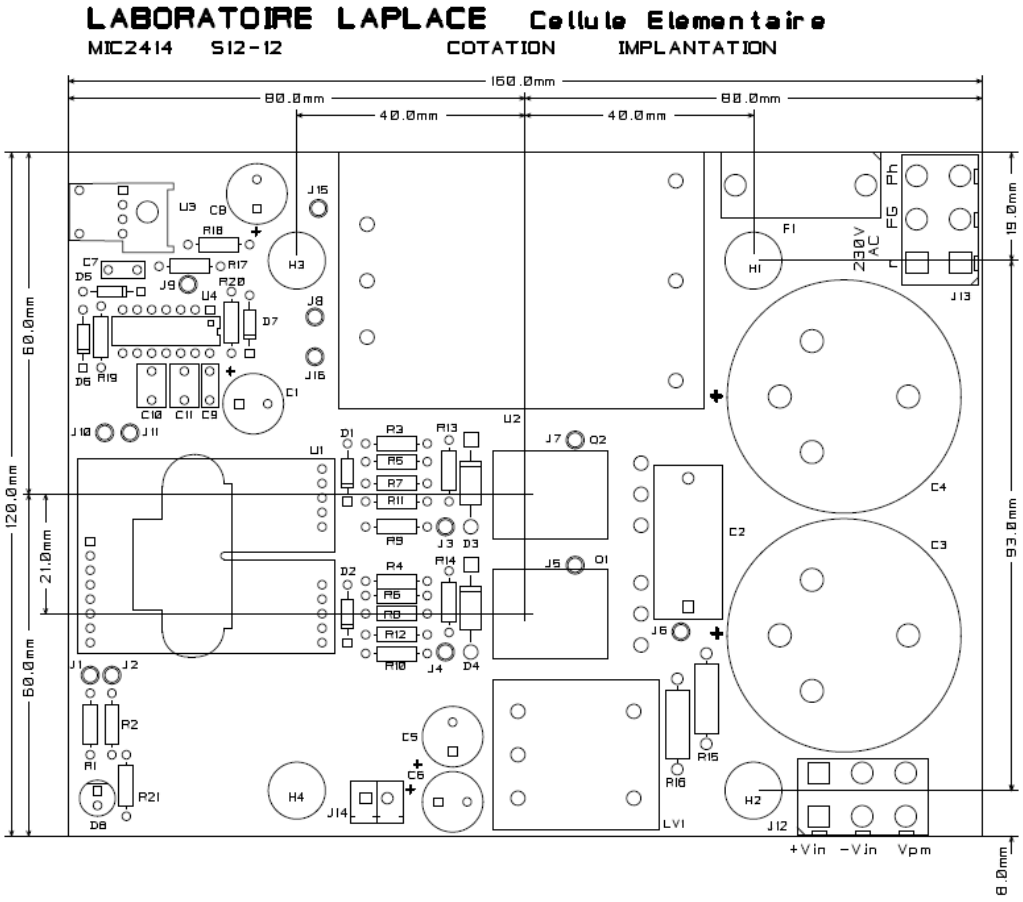


Figure A - 2: Disposition of components on the cell

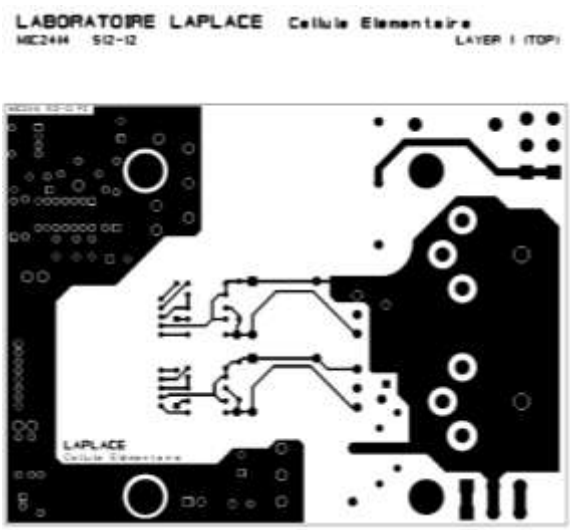


Figure A - 3: PCB Top layer

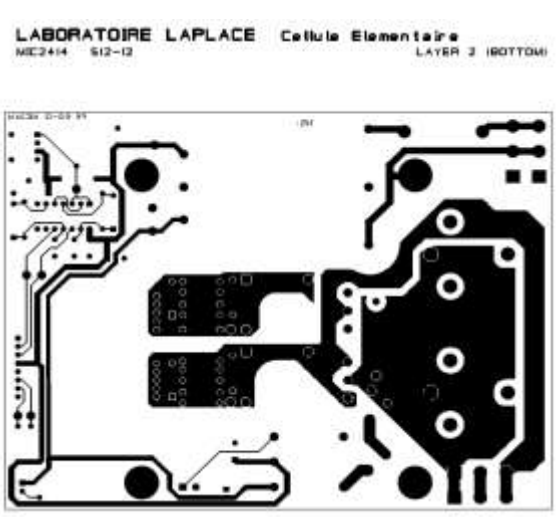


Figure A - 4: PCB Bottom layer

The cells are posed in group of 3 on a single heat sink. Finally the heat sink are assembled in group of 3 forming a matrix of cells 3x3 as shown in the picture of Figure A - 2.



Figure A - 5: Photo of a cell



Figure A - 6: Cells on the heatsinks

V.4.1 Measurement Cards

Each board is equipped with a voltage sensor and two current sensors, to achieve all the required measurements four boards were installed. Adaptation and filtering stages are achieved by the acquisition cards which are detailed below. The reference circuit for the measurements achieved on the prototype is reported in Figure A - 7

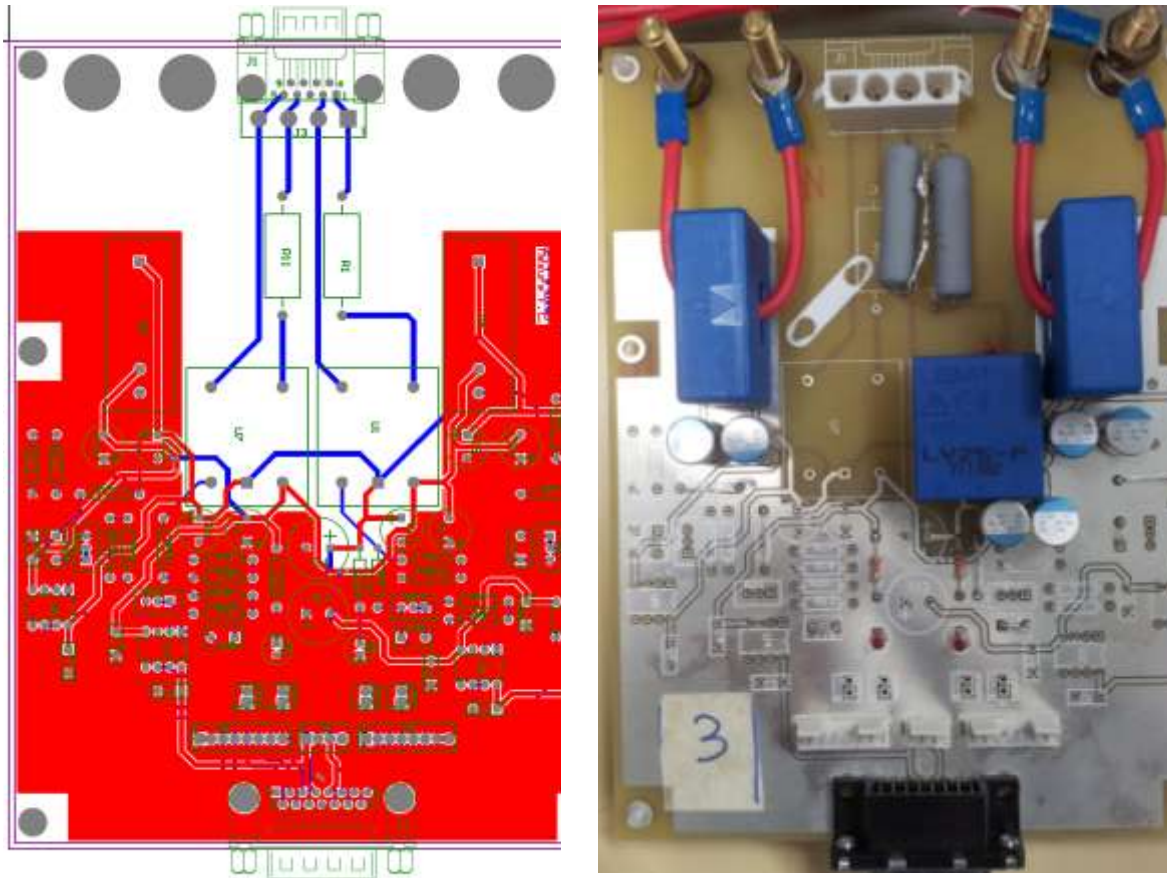


Figure A - 7: Measurement card lay-out and its definitive realization

A.2 The Frame

From Figure A - 8 to Figure A - 10 few views of layout of the frame prototype are reported. The detailed description of the power stage with the elementary cells features was given in R-1. Capacitor voltages and branch currents are provided by sensors (LEM) and measurement cards adapt output sensor voltages to the hardware inputs.

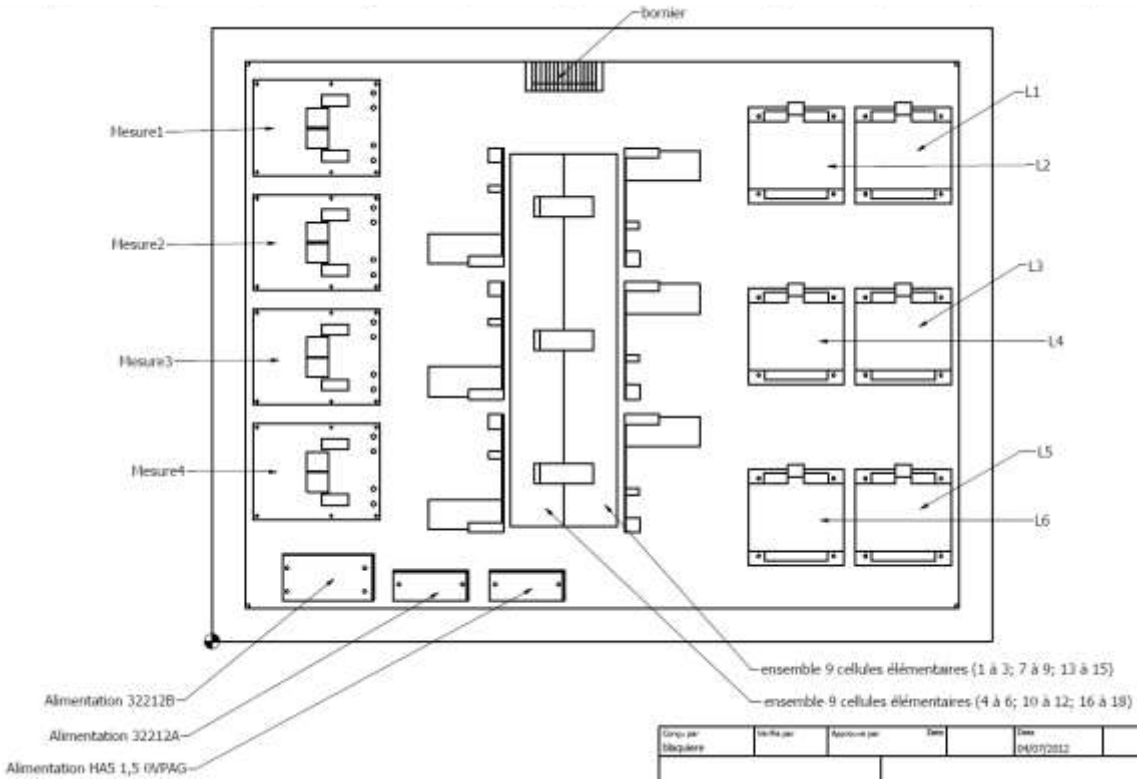


Figure A - 8: Top view of the frame

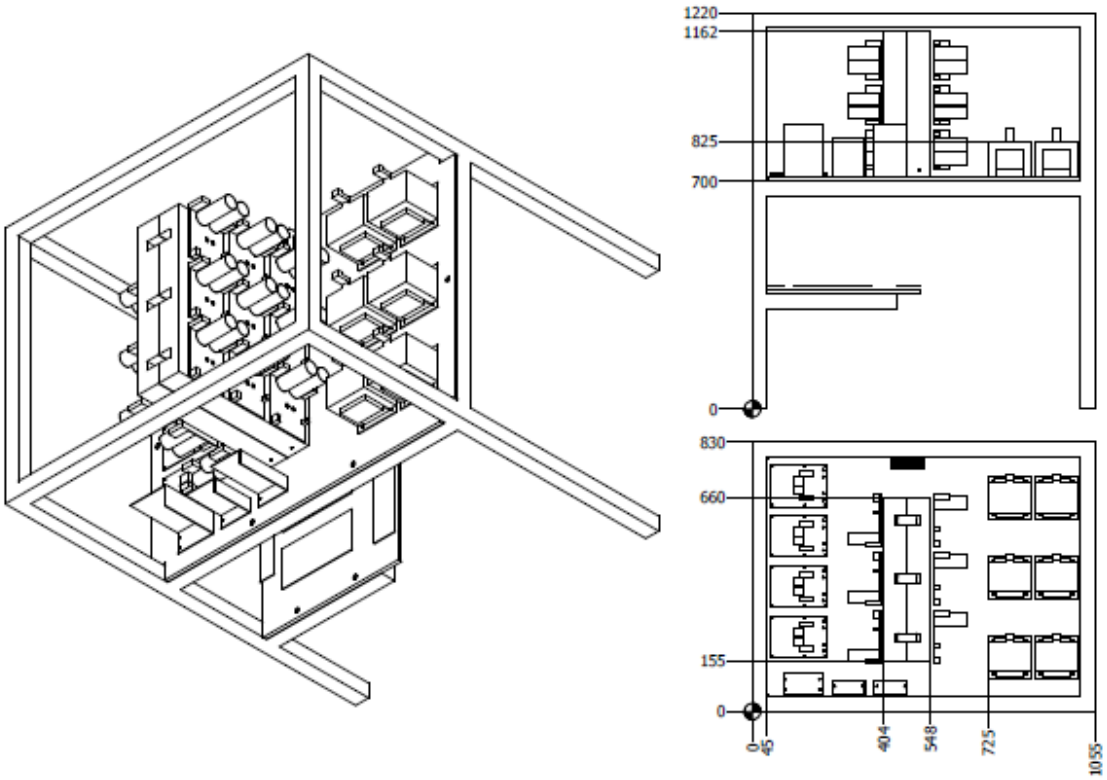


Figure A - 9: View of the design for the frame

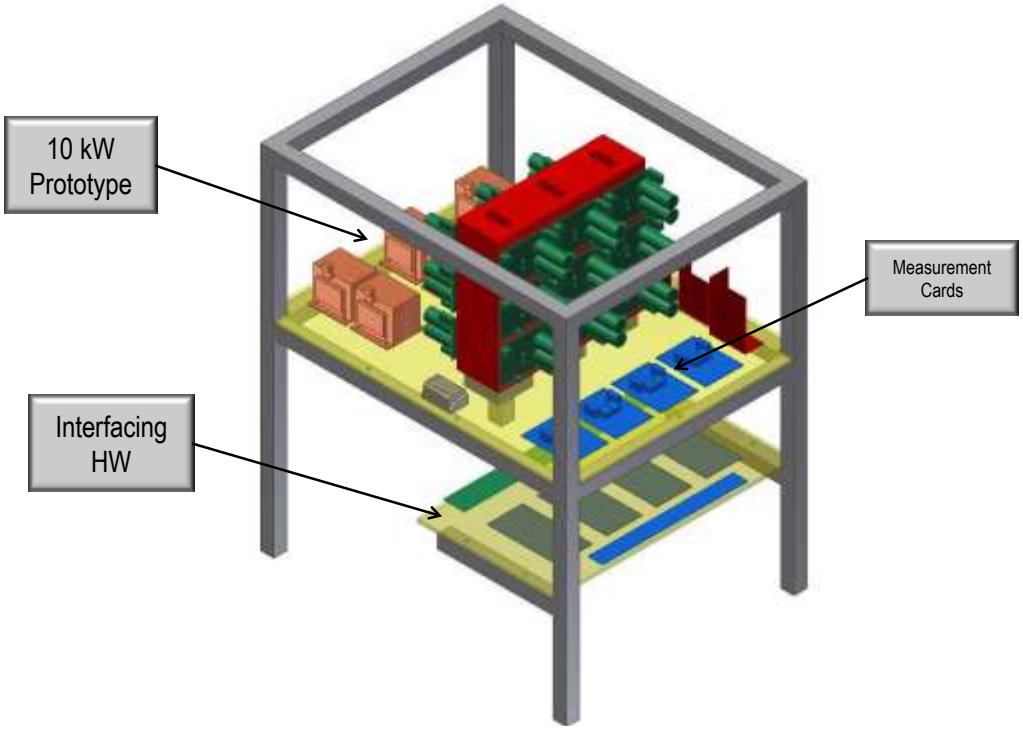


Figure A - 10: CAD design of the system

The interfacing hardware platform shown in Figure A - 11 is composed by sorting card which provides to adapt the analogical signals coming from the acquisition cards, sorted in groups of four, to the DB37 connector. Moreover the digital signals coming from the DB37 connector are divided in groups of eight signals which are converted in optical signals by the optical emitter.

In the next paragraphs each board of the interfacing platform is described.

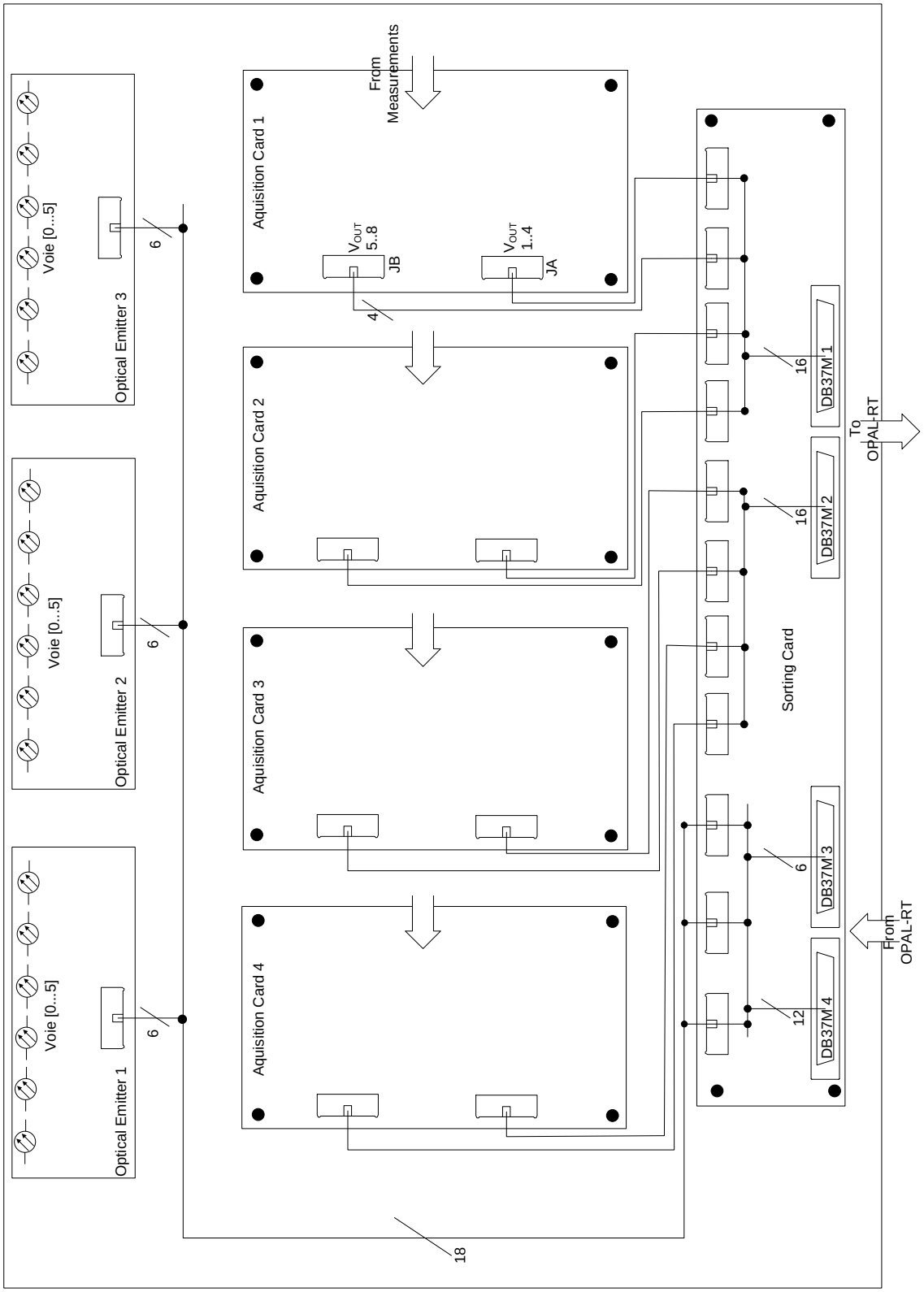


Figure A - 11: Interfacing Hardware platform

A.1.1 Acquisition Card

Each board allows adapting the signals coming from the measurement cards to the right level [±15V] for the analog input side of the OP5340 for the OPAL-RT frame. Each card is able to process eight signals by eliminating the noise whit tunable high frequency active filters. To process 29 analog measurements four acquisition cards are employed. The PCB circuit and its final layout are depicted in Figure A - 12.

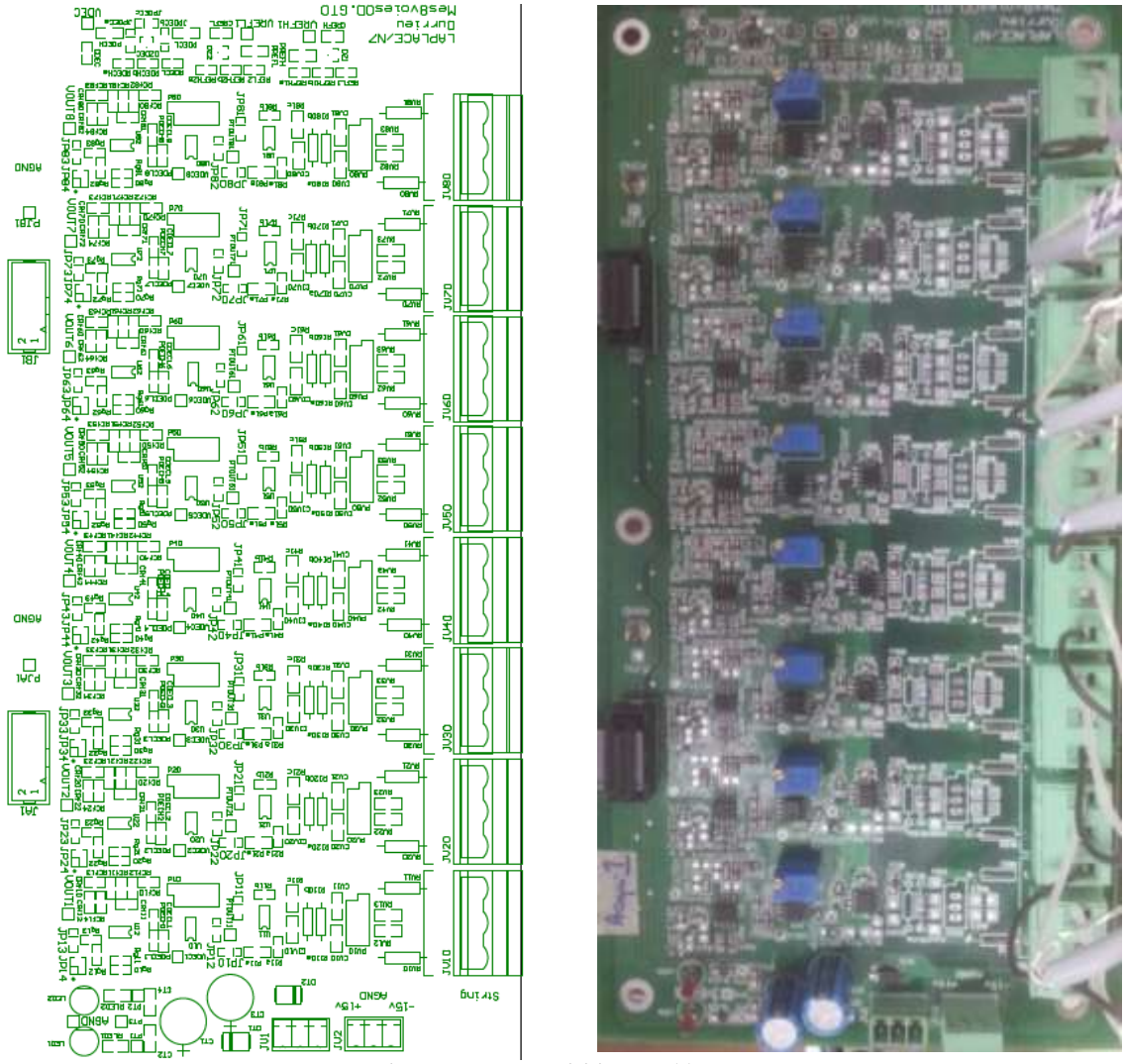


Figure A - 12 Acquisition card layout.

A.1.1 Optical emitter

The digital signals coming from the OPAL-RT provides the ON/OFF state of the semiconductor devices. The signals are arranged in three groups, one per phase. The output card OP5354 of OPAL-RT puts out [0, +5 V] signals.

Each optical emitter is designed to convert in optical signal up to eight electrical inputs. In the configuration adopted for the prototype just six ways are cabled (Figure A - 13) which corresponds to the number of cells per phase of the MMC prototype.

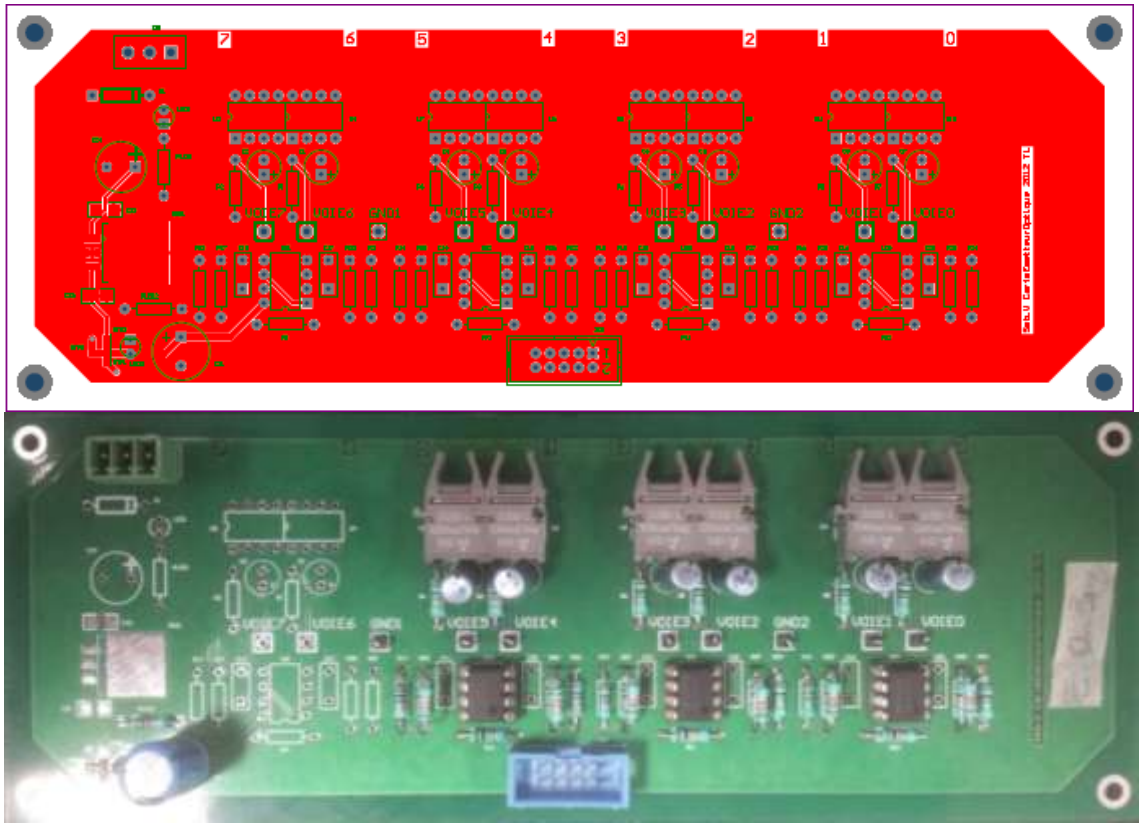


Figure A - 13: Optical emitter layout

For the interfacing hardware two tables are provided. One table is provided for the analogical signal and another one for the digital signals. Each table reports the correspondences, by considering the levels of connection per signal. The levels are:

– OPAL-RT number channel

– Number of the way on the card
– Number of the card
– Name of the voltage/current measured

A.2 HIL Box

The device chosen for the prototyping is the OPAL-RT 5600, which permits to achieve the following performances.

- Model-Based design and virtual Prototyping
- Control Prototyping and testing
- Embedded Control
- Data Logging

The OP5600 is a complete simulation system capable of operating with either Spartan 3 or Virtex 6 FPGA platforms. It is designed to be used either as a desktop (or shelf top) or as a more traditional rack mount. It contains a powerful Target Computer and a flexible high-speed Front End Processor and a signal conditioning stage. The new design makes it easier to use with standard connectors (DB37, RJ45 and mini-BNC) which avoid input/output adaptors and allow quick connections for monitoring. The front of the chassis provides the monitoring interfaces and monitoring connectors, while the back of the chassis provides access to the FPGA monitoring connections, all I/O connectors, power cable and main power switch.

Inside, the main housing is divided into two sections, each with a specific purpose and connected only by a DC power cable and a PCIe cable:

In its standard configuration, the lower part of the chassis contains a powerful target computer that can be connected to a network of simulators or can have a stand-alone capability. The target computer includes the following features:

– ATX motherboard with up to 12 cores
– 6 DRAM connectors
– 250 Mb hard disk
– 600 W power supply
– PCIe boards (up to 8 slots, depending on the configuration).

The main features of the system are reported in [78].

A.3 PIN tables

The connections about the interfacing hardware are sorted according table A-1 for the analogic signals.

PIN DB37M_1	Aq. Card				Signal Name	OPAL-RT		PIN DB37M_2	Aq. Card				Signal Name	OPAL-RT	
	Number	Connector Name	HE_10 N°Pin	Signal Name		Channel	Gr. 1 Sec. A		Number	Connector Name	HE_10 N°Pin	Signal Name		Channel	Gr. 1 Sec.B
1	2	JB	3	Vout 5	V10	0		1	4	JB	3	Vout 5	IL6	0	
2	2	JB	5	Vout 6	V11	1		2	4	JB	5	Vout 6	VCA	1	
3	2	JB	7	Vout 7	V12	2		3	4	JB	7	Vout 7		2	
4	2	JB	9	Vout 8	V16	3		4	4	JB	9	Vout 8		3	
5	2	JA	3	Vout 1	V15	4		5	4	JA	3	Vout 1	IL3	4	
6	2	JA	5	Vout 2	V4	5		6	4	JA	5	Vout 2	IL4	5	
7	2	JA	7	Vout 3	V5	6		7	4	JA	7	Vout 3	VBC	6	
8	2	JA	9	Vout 4	V6	7		8	4	JA	9	Vout 4	IL5	7	
9	1	JB	3	Vout 5	V8	8		9	3	JB	3	Vout 5	IL1	8	
10	1	JB	5	Vout 6	V9	9		10	3	JB	5	Vout 6	IL2	9	
11	1	JB	7	Vout 7	V13	10		11	3	JB	7	Vout 7	VAB	10	
12	1	JB	9	Vout 8	V14	11		12	3	JB	9	Vout 8		11	
13	1	JA	3	Vout 1	V1	12		13	3	JA	3	Vout 1	V17	12	
14	1	JA	5	Vout 2	V2	13		14	3	JA	5	Vout 2	V18	13	
15	1	JA	7	Vout 3	V3	14		15	3	JA	7	Vout 3	IDC	14	
16	1	JA	9	Vout 4	V7	15		16	3	JA	9	Vout 4	VDC	15	
DB37M Pins 20..35=AGND on Acq. Card															

TABLE A-1

The connections about the interfacing hardware are sorted according table A-2 for the digital signals.

PIN DB37M_4	Emetteur optique			OPAL-RT		Elementary Cell	PIN DB37M_3	Emetteur optique			OPAL-RT		Elementary Cell
	Number	HE_10 N°Pin	Signal Name	Channel	Gr. 2 Sec. B			Number	HE_10 N°Pin	Signal Name	Channel	Gr. 2 Sec. B	
1	1	9	Voie 7	0			1	3	9	Voie 7	16		
2	1	8	Voie 6	1			2	3	8	Voie 6	17		
3	1	7	Voie 5	2		1	3	3	7	Voie 5	18		13
4	1	6	Voie 4	3		2	4	3	6	Voie 4	19		14
5	1	5	Voie 3	4		3	5	3	5	Voie 3	20		15
6	1	4	Voie 2	5		4	6	3	4	Voie 2	21		16
7	1	3	Voie 1	6		5	7	3	3	Voie 1	22		17
8	1	2	Voie 0	7		6	8	3	2	Voie 0	23		18
9	2	9	Voie 7	8			9						
10	2	8	Voie 6	9			10						
11	2	7	Voie 5	10		7	11						
12	2	6	Voie 4	11		8	12						
13	2	5	Voie 3	12		9	13						
14	2	4	Voie 2	13		10	14						
15	2	3	Voie 1	14		11	15						
16	2	2	Voie 0	15		12	16						
DB37M Pins 20..35,37=GND on E.O. card; DB37M Pin 18= +5V on E.O. card													

TABLE A-2

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