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Capacitance spectroscopy in hydrogenated amorphous silicon Schottky diodes and high efficiency silicon heterojunction solar cells

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Abstract

In this thesis, research on a-Si:H Schottky diodes and a-Si:H/c-Si heterojunctions is presented with the focus on the capacitance spectroscopy and information on electronic properties that can be derived from this technique.

Last years a-Si:H/c-Si heterojunctions (HJ) have received growing attention as an approach which combines wafer and thin film technologies due to their low material consumption and low temperature processing. Compared to conventional crystalline silicon (c-Si) technologies, HJ solar cells benefit from lower fabrication temperatures (around 200°C) thus reduced costs, possibilities of large-scale deposition, better temperature coefficient and lower silicon consumption (thinner wafers can be used due to excellent passivation quality). In this area impressive results were achieved by Sanyo Electric with the so called a-Si/c-Si Heterojunction with Intrinsic Thin layer (HIT) solar cell. This technology showed excellent surface passivation and the highest power conversion efficiency. The most recent record efficiency belongs to Panasonic with 24.7% for a cell of practical size (100 cm^2 and above) : was obtained.

There are several key properties of a-Si:H/c-Si heterojunctions that should be addressed when fabricating a high efficiency device. Firstly, the density of states (DOS) in the bandgap of a-Si:H is of particular importance since bandgap defects determine the band bending and space charge in a-Si:H, favor the trapping and recombination of free carriers and thus also have an impact on transport of the carriers and their collection on the contacts. Secondly, determination of band offsets between a-Si:H and c-Si is of crucial importance since they govern the carrier transport across the junction and determine the band bending in c-Si. The aim of this thesis is to provide a critical study of the capacitance spectroscopy as a technique that can provide information on both subjects: DOS in a-Si:H and band offset values in a-Si:H/c-Si heterojunctions.

In Chapter 1 a description of hydrogenated amorphous silicon is presented with the focus on its application in photovoltaic devices. Chapter 2 recalls the basics of *p-n* junctions and the fundamental principles of the capacitance vs voltage (*C-V*) technique. Possibilities and limitations of *C-V* measurements and admittance spectroscopy are addressed as well. The depletion approximation is recalled since it plays a very important role in the description of a junction and may be a reason of erroneous interpretations of the capacitance measurements.

In Chapter 3, capacitance spectroscopy in a-Si:H Schottky diodes is investigated. Our interest is concentrated on the simplified treatment of the temperature and frequency dependence of the capacitance that allows one to extract the density of states at the Fermi level in a-Si:H Schottky diodes. To our knowledge no critical assessment of this treatment has been carried out. We focus on the study of the reliability and validity of this approach applied to a-Si:H Schottky barriers with various magnitudes and shapes of the DOS. Several structures representing *n*-type and undoped hydrogenated amorphous silicon Schottky diodes are modeled with the help of numerical simulation softwares. We show that the reliability of the studied treatment drastically depends on the approximations used to obtain the explicit analytical expression of the capacitance in such an amorphous semiconductor.

In the second part of the chapter, we study the possibility of fitting experimental capacitance data by numerical calculations with the input a-Si:H parameters obtained from other experimental techniques. With slight corrections of parameters describing the DOS distributions a very good reproduction of experimental capacitance data is obtained. We conclude that the simplified treatment of the experimentally obtained capacitance data together with numerical modeling is a valuable tool to assess some important parameters of the material with no need in any additional knowledge on the DOS of a studied sample.

In chapter 4, we study the capacitance spectroscopy of a-Si:H/c-Si heterojunctions with special emphasis on the influence of a strong inversion layer in c-Si at the interface. Firstly, we focus on the study of the frequency dependent low temperature range of capacitance-temperature dependencies of a-Si:H/c-Si heterojunctions. The theoretical analysis of the capacitance steps in calculated capacitance-temperature dependencies is presented by means of numerical modeling. It is shown that two steps can occur in the low temperature range, one being attributed to the activation of the response of the gap states in a-Si:H to the small signal modulation, the other one being related to the response of holes in the strong inversion layer in c-Si at the interface. The experimental behavior of *C-T* curves is discussed.

In the second part of Chapter 4, the quasi-static regime of the capacitance is studied. We show that the depletion approximation fails to reproduce the experimental data obtained for (p) a-Si:H/(n) c-Si heterojunctions. Due to the existence of the strong inversion layer, the depletion approximation overestimates the potential drop in the depleted region in crystalline silicon and thus underestimates the capacitance and its increase with temperature. A complete analytical calculation of the heterojunction capacitance taking into account the hole inversion layer is developed. It is shown that within the complete analytical approach the inversion layer brings significant changes to the capacitance for large values of the valence band offset. The experimentally obtained *C-T* curves show a good agreement with the complete analytical calculation and the presence of the inversion layer in the studied samples is thus confirmed. The application of capacitance measurements in the derivation of the band-offsets is discussed by comparing experimentally and analytically obtained *C-V* dependencies at different temperatures. The discussion of the influence of the c-Si surface inversion layer on the *C-V* profiles is provided as well. We demonstrate that due to the existence of the strong inversion layer, the derivation of the band offsets from *C-V* measurements leads to erroneous results.

Résumé

Les travaux développés dans cette thèse sont dédiés à l'étude des propriétés électroniques de diodes Schottky de silicium amorphe hydrogéné (a-Si:H) et d'hétérojonctions entre silicium amorphe hydrogéné et silicium cristallin, a-Si:H/c-Si au moyen de spectroscopies de capacité de jonctions.

Parmi les technologies photovoltaïques à base de silicium, les cellules solaires à hétérojonction a-Si:H/c-Si ont reçu un intérêt croissant car cette nouvelle technologie a un fort potentiel d'amélioration du rendement photovoltaïque et de réduction de coûts. Par rapport aux cellules photovoltaïques classiques à homojonctions, les cellules à hétérojonctions bénéficient des avantages de dépôt des couches amorphes à grande échelle et à des températures faibles, autour de 200°C (procédés de dépôt par décomposition assistée par plasma de gaz précurseurs), d'un meilleur coefficient de température, et d'une consommation plus faible de silicium (des plaques plus minces peuvent être utilisées en raison de l'excellente qualité de passivation de surface par le a-Si:H). A partir de cette technologie à hétérojonctions, la société japonaise Panasonic a réalisé en 2013 une cellule de grande surface (>100 cm^2) possédant un rendement de conversion record de 24,7%.

Lors de la fabrication des cellules solaires à haut rendement plusieurs paramètres d'une hétérojonction a-Si:H/c-Si doivent être considérés.

Premièrement, la densité d'états (DOS, Density Of States) dans le gap du a-Si:H est d'une grande importance car il s'agit de défauts qui :

- déterminent la courbure des bandes et la charge d'espace dans le a-Si:H ;
- favorisent le piégeage et la recombinaison de porteurs libres ;
- influencent le transport des porteurs libres jusqu'aux contacts et leur collecte.

Deuxièmement, la détermination des désaccords des bandes entre la couche amorphe et la couche cristalline est indispensable puisque ceux-ci contrôlent le transport à travers la jonction et déterminent la courbure des bandes dans c-Si, ce qui va notamment influencer la recombinaison des porteurs sous lumière, donc la tension de circuit ouvert des cellules. Cette thèse a pour but d'étudier la spectroscopie de capacité comme technique d'analyse de paramètres clés pour les dispositifs à hétérojonctions de silicium : la densité d'états dans le a-Si:H et les désaccords des bandes entre a-Si:H et c-Si.

Dans le premier chapitre de ce manuscrit, nous présentons une description du silicium amorphe axée sur son application dans le domaine du photovoltaïque.

Dans le deuxième chapitre nous rappelons les éléments de base de la théorie sur la jonction p-n

ainsi que les principes de la technique couramment désignée *C-V* (capacité-en fonction de la tension). Nous abordons aussi les potentiels et les limitations des mesures *C-V* et de la spectroscopie d'admittance. A ce stade, un rappel est effectué sur l'approximation courante consistant à déterminer l'extension de la zone de charge d'espace de la jonction et sa capacité en négligeant les contributions des deux types de porteurs libres (dénommée quelquefois approximation de déplétion, par transposition de sa désignation anglo-saxonne), car elle joue un rôle important dans la description d'une jonction et elle peut être à l'origine de fausses interprétations des mesures de capacité.

Le troisième chapitre est dédié à l'étude de la capacité de diodes Schottky. Nous nous concentrons sur un traitement simplifié de la capacité en fonction de la température et de la fréquence reposant sur une expression analytique obtenue par une résolution approchée de l'équation de Poisson. Ce traitement permet en principe d'extraire la densité d'états au niveau de Fermi dans le a-Si:H et la fréquence de saut des électrons depuis un état localisé au niveau de Fermi vers la bande de conduction, mais il n'a jamais été critiqué sur la base d'une comparaison avec un calcul numérique complet. En appliquant ce traitement simplifié à la capacité calculée sans approximation à l'aide de deux logiciels de simulation numérique, nous montrons que sa fiabilité et sa validité dépendent fortement de la distribution des états localisés dans la bande interdite du a-Si:H et de la position du niveau de Fermi. Globalement, le traitement permet toujours d'obtenir l'ordre de grandeur de la densité d'états au niveau de Fermi, mais la fréquence de saut peut être sur-estimée de plusieurs ordres de grandeur

Nous montrons également que le calcul numérique de la capacité, à partir de paramètres du matériau obtenus par d'autres techniques de caractérisation, permet, moyennant de légers ajustements de ces paramètres, de bien reproduire les données mesurées expérimentalement, en particulier la dépendance de la capacité en fonction de la température et de la fréquence..

Dans le chapitre 4 nous abordons l'étude de la capacité des hétérojonctions entre a-Si:H de type p et c-Si de type n, et nous mettons particulièrement en avant l'existence d'une couche d'inversion forte à l'interface dans le c-Si, formant un gaz bidimensionnel de trous. Dans une première partie, nous présentons une étude par simulation numérique de la dépendance de la capacité en fonction de la température, pour laquelle un ou deux échelons peuvent être mis en évidence à basse température. Leur analyse montre qu'un des ces échelons est attribué à l'activation de la réponse de la charge dans le a-Si:H, qui peut dépendre à la fois du transport et du piégeage/dépiégeage d'électrons au niveau de Fermi, alors que l'autre, présentant une énergie d'activation plus grande, est lié à la modulation de la concentration des trous dans la couche d'inversion forte, lorsque celle-ci existe (i.e. pour des valeurs suffisamment élevées du désaccord de bande de valence). On présente ensuite une discussion de résultats expérimentaux. Si un échelon de capacité peut quelquefois être détecté, son énergie d'activation reste toujours plus faible que celle observée dans les simulations pour la modulation du gaz de trous. Une interprétation basée sur des mécanismes de transport par effet tunnel et par saut dans le a-Si:H est proposée pour expliquer ce désaccord entre résultats expérimentaux et simulation numérique, celle-ci n'intégrant pas ce type de mécanismes. Nous mettons par ailleurs en évidence un comportement quasi statique de la capacité montrant une augmentation significative avec la température.

Ce régime quasi-statique de la capacité fait l'objet d'une discussion dans la deuxième partie du chapitre 4. Nous mettons en relief le fait que l'approximation de la zone de déplétion ne permet pas de reproduire cette augmentation de la capacité en fonction de la température. Du fait de l'existence de la couche d'inversion forte, la chute de potentiel dans la zone de déplétion du c-Si est plus faible que la valeur déterminée par le calcul attribuant toute la chute de potentiel à la zone de déplétion. Par conséquent, cette approximation conduit à sous-estimer la capacité ainsi que son augmentation avec la température. Nous présentons alors un calcul analytique complet qui tient compte à la fois de la distribution particulière du potentiel dans le a-Si:H, et des trous dans le c-Si dont la contribution à la concentration totale de charges n'est pas négligeable dans la couche d'inversion forte. Le calcul analytique complet permet de bien reproduire les résultats expérimentaux de capacité en fonction de la température; ceci confirme la présence de la couche d'inversion forte dans les échantillons étudiés. On présente enfin une discussion sur l'application de la technique *C-V* pour la détermination des désaccords des bandes, ainsi que la comparaison des courbes capacité-tension obtenues expérimentalement et analytiquement à différentes températures. Nous précisons ainsi aussi l'influence et l'importance de la prise en compte de la couche d'inversion forte dans l'analyse des mesures *C-V.*

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1 a-Si:H and its applications

1.1 Description of the a-Si material

Silicon in its amorphous state (a-Si) was first obtained by Bertzelius at the beginning of the 19th century [1], but until the 1960s it was not used as a semiconductor. Amorphous silicon without hydrogen was prepared in those days by thermal evaporation or sputtering [2]. This unhydrogenated material was highly defective, which inhibited its use as a useful semiconductor.

In 1965 it was discovered that deposition of amorphous silicon employing glow discharge as the deposition technique yielded a material with much more useful electronic properties [3,4]. Some years later, Fritsche and co-workers in Chicago confirmed that a-Si produced from a glow discharge of SiH_4 contains hydrogen [5,6]. In 1975 a boost in research activities occurred when it was shown that hydrogenated amorphous silicon (a-Si:H) could be *n*- or *p*-type doped by introducing phosphine (PH_3) or diborane (B_2H_6) in the plasma [7]: a variation of resistivity of more than 10 orders of magnitude could be reached by adding small amounts of these dopants.

This discovery immediately initiated the research on practical amorphous silicon devices. Carlson and Wronski at RCA Laboratories started in 1976 with the development of photovoltaic devices [8]. The first *p-i-n* junction type solar cell was reported by the group of Hamakawa [9,10]. In 1980, Sanyo was the first to fabricate market devices: solar cells for hand-held calculators [11]. Application of a-Si:H in field effect transistors [12-14] is based on the capability to deposit and process a-Si:H over large areas. Combining the photoconductive properties and the switching capabilities of a-Si:H has yielded many applications in the field of linear sensor arrays, e.g. 2D image sensors, position-sensitive detectors of charged particles, X-rays, gamma rays, and neutrons [15-18]. The photovoltaic applications of a-Si:H will be discussed in details in Section 1.3.

1.1.1 Atomic structure

The disorder of the atomic structure is the main feature which distinguishes amorphous from crystalline materials. Hydrogenated amorphous silicon is a disordered semiconductor whose optoelectronic properties are governed by the large number of defects present in its atomic structure. The amorphous nature arises from the absence of long-range order in the lattice of the material. The first few nearest neighbor distances are separately distinguished, but the correlation between atom pairs disappears after a few interatomic spacings [19]. One can describe the disorder by the atom pair distribution function, which is the probability of finding an atom at a distance r from another atom. A perfect crystal is completely ordered to large pair distances, while an amorphous material only shows short-range order. Because of the short-range order, material properties of amorphous semiconductors are similar to their crystalline counterparts. The covalent bonds between the silicon atoms in a-Si:H are similar to the bonds in crystalline silicon.

Amorphous semiconductors are often described as a continuous random network (CRN) [20,21], that is shown in Fig.1.1. The periodic crystalline structure is replaced by a random network in which each atom has a specific number of bonds to its closest neighbors (the coordination). The random network easily incorporates atoms of different coordination, even in small concentration. This is in marked contrast to the crystalline lattice in which impurities are generally constrained to have the coordination of the host because of the long range ordering of the lattice. This difference is most distinctly reflected in the doping and defect properties of a-Si:H.

In the ideal CRN model for amorphous silicon, each atom is fourfold coordinated, with bond lengths similar (within 1 % [22]) to that in the crystal. In this respect, the short range order (< 2 nm) of the amorphous phase is similar to that of the crystalline phase. Amorphous silicon lacks long-range order because the bond-angles deviate from the tetrahedral value.

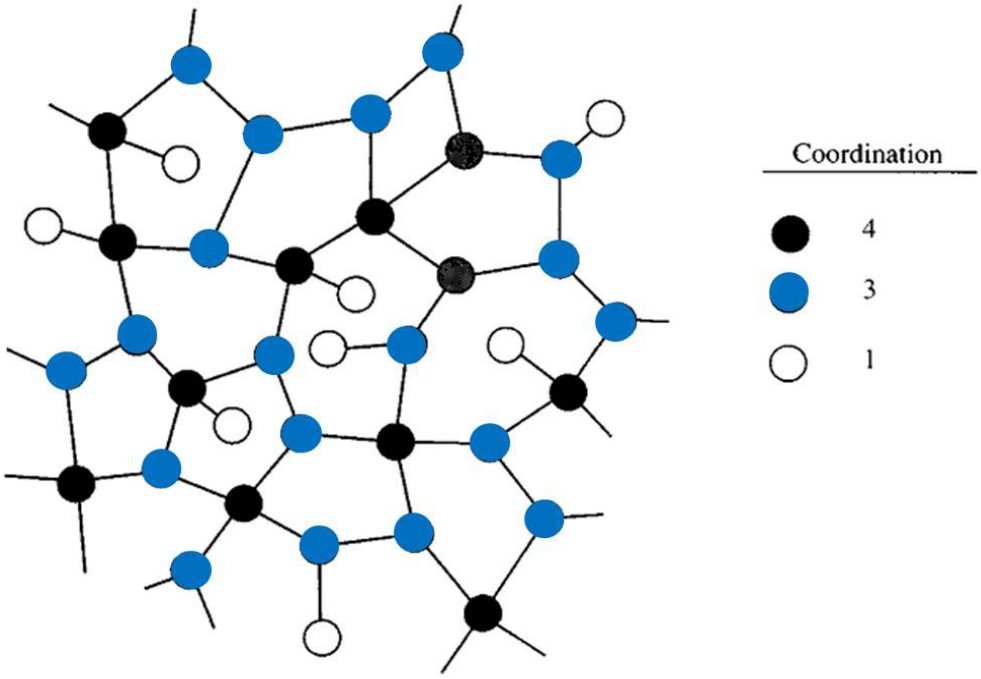

Fig.1.1. An example of a continuous random network containing atoms of different bonding coordination (from [19]).

The continuous random network may contain defects, but the concepts of interstitials or vacancies applicable for crystalline materials are not valid here. Instead, in the CRN one uses the coordination defect when an atom has too few or too many bonds. In a-Si:H, dangling bonds arise when a silicon atom has too few bonds to satisfy its outer sp3 orbital. It is the common view that the dominant defect in amorphous silicon is a threefold-coordinated silicon atom. This structural defect has an unpaired electron in a non-bonding orbital, called a dangling bond. Pure amorphous silicon has a high defect density of the order of 10^{20} cm^{-3}, which prevents photoconductance and doping. The special role of hydrogen with regard to amorphous silicon is its ability to passivate defects by providing for electrons to the dangling bonds. Hydrogenation to a level of ~ 10 at.% reduces the defect density by four to five orders of magnitude.

1.1.2 Electronic structure and properties

The structural disorder influences the electronic properties in several different ways. The similarity of the covalent silicon bonds in crystalline and amorphous silicon leads to a similar overall electronic structure - amorphous and crystalline phases of the same material tend to have comparable band gaps. The disorder represented by deviations in the bond lengths and bond angles broadens the electron distribution of states and causes electron and hole localization as well as strong scattering of the carriers. Structural defects such as broken

bonds have corresponding electronic states which lie in the band gap. There are also phenomena which follow from the emphasis on the local chemical bonds rather than the long range translational symmetry. The possibility of alternative bonding configurations of each atom leads to a strong interaction between the electronic and structural states and causes the phenomenon of metastability.

One of the fundamental properties of a semiconductor or insulator is the presence of a band gap separating the occupied valence band from the empty conduction band states. Since according to the free electron theory, the band gap is a consequence of the periodicity of the crystalline lattice, in the past there were considerable debates over the reason that amorphous semiconductors had a band gap at all. It was stated by Weaire and Thorpe [23] that the bands are most strongly influenced by the short range order, which is the same in amorphous and crystalline silicon and the absence of periodicity is a small perturbation.

The preservation of the short-range order results in a similar electronic structure of the amorphous material compared to the crystalline one: bands of extended mobile states are formed (defined by the conduction and valence band edges, E_C and E_V) separated by the energy gap, E_g, more appropriately termed "mobility gap". The long-range atomic disorder broadens the densities of energy states, resulting in band tails of localized states that may extend deep into the band gap. Coordination defects (dangling bonds) result in electronic states deep in the band gap, around mid-gap. As electronic transport mostly occurs at the band edges, the band tails greatly determine the electronic transport properties. The deep defect states determine electronic properties by controlling trapping and recombination.

In crystalline semiconductors the energy bands are described by energy-momentum (*E-k*) dispersion relations that arise from Bloch solution for the wavefunction of the electronic states. This solution to Schrödinger's equation does not apply to an amorphous semiconductor because the potential energy of an atomic structure is no longer periodic. A weak disorder potential results in only a small perturbation of the wavefunction and has the effect of scattering the electron from one Bloch state to another. The strong scattering causes a large uncertainty in the electron momentum, so that it is not a good quantum number and is not conserved in electronic transitions.

The loss of *k*-conservation is one of the most important results of disorder and changes much of the basic description of the electronic states. Some consequences of the loss of *k*-conservation are:

- The energy bands are no longer described by the *E-k* dispersion relations, but instead by a density-of-states distribution *N(E)*. Also the electron and hole effective masses must be redefined as they are usually expressed from the curvature of *E(k).*
- The conservation of momentum selection rules does not apply to optical transitions in amorphous semiconductors. Consequently, the distinction is lost between a direct and an indirect band gap, in which transitions from the highest-energy state in the valence

band to the lowest-energy state in the conduction band are forbidden by momentum conservation. Instead transitions occur between states which overlap in real space. This distinction is most obvious in silicon which has an indirect band gap in its crystalline phase but not in the amorphous phase.

- The disorder reduces the carrier mobility because of the frequent scattering and causes the much more profound effect of the wavefunction localization.

1.1.3 Density of states in the band gap

The loss of momentum conservation in the electronic transitions results in the replacement of the energy-momentum band structure of a crystalline semiconductor by an energy-dependent density of states (DOS) distribution, *N(E).* It is convenient to divide *N(E)* into three different energy ranges: the main conduction and valence bands, the band tail regions close to the band edges, and the defect states in the forbidden gap. Our interest is concentrated on the two latter since electronic defects reduce the photosensitivity, suppress doping and impair the device performance of a-Si:H. They control many electronic properties and are centrally involved in the substitutional doping process.

Defects are described by three general properties. First is the set of electronic energy levels of different charge states. Those defects with states within the band gap are naturally of the greatest interest in understanding the electronic properties because of their role as traps and recombination centers. Second is the atomic structure and bonding of the defect, which determine the electronic states. Finally, the defect reactions describe how the defect density depends on the growth and on the treatment after growth.

The first arising question is the definition of a defect in an amorphous material. In a crystalline material any deviation from an ideal lattice would be considered as a defect, naming a vacancy or an interstitial atom. By analogy with the crystal one can define a defect in an amorphous material as a deviation from the ideal amorphous network where all the bonds are satisfied. This approach gives an idea of a coordination defect in which an atom has a distinctly different bonding state from the ideal. In ideal a-Si: H all the silicon atoms are four-fold coordinated and all the hydrogen atoms are singly coordinated. An example of a coordination defect where the bonding state is different from the ideal one is the three-fold coordinated silicon with a dangling bond. This type of defect therefore has the distinguishing characteristic of either a paramagnetic spin or an electric charge, which sets it apart from the electronic states of the ideal network.

As it was already mentioned above, in common with most other covalent amorphous semiconductors, the overall shapes of the valence and conduction bands of a-Si: H are hardly different from a smoothed crystalline density of states. The most significant difference between the crystal and amorphous phases comes at the band edges where the disorder creates

a tail of localized states extending into the gap. The width of the tail depends on the degree of disorder and on the bonding character of the states. The localized tail states are separated from the extended band states by the mobility edge [24].

Information on band tails is generally obtained from photoemission and absorption data [25-28]. The photoemission data provide some direct information on the density of states *N(E)* in the band tails, but the results are limited by the low sensitivity and energy resolution of the experiment. The density of states can be determined only to about 5-10% of the peak density in the band, with an energy resolution of 0.05-0.1 eV, after careful correction for the experimental resolution. Both band edges are found to have an approximately linear energy dependence of *N(E)* over an energy range of about 0.5 eV from the band edges and down to a density of about $3 \cdot 10^{21}$ $cm^{-3}eV^{-1}$. The density of states deep in the band gap of good quality a-Si:H is no more than 10^{15}—10^{16} cm^{-3} eV^{-1}[19], so that another 5-6 orders of magnitude of sensitivity are needed to describe the band tails properly.

A typical density of states consists of the following terms [29]:

1. a free electron conduction band DOS for $E \geq E_C$:

$$N(E) = \frac{1}{2\pi^2}\left(\frac{2m_e}{\hbar^2}\right)^{3/2}(E - E_C)^{1/2} \tag{1.1}$$

2. a free hole valence band DOS for $E \leq E_V$:

$$N(E) = \frac{1}{2\pi^2}\left(\frac{2m_h}{\hbar^2}\right)^{3/2}(E_V - E)^{1/2} \tag{1.2}$$

3. a conduction band tail for $E < E_C$:

$$N_{CbT}(E) = N(E_C)\exp\left(-\frac{E_C - E}{k_B T_C}\right) \tag{1.3}$$

4. a valence band tail for $E > E_V$:

$$N_{VbT}(E) = N(E_V)\exp\left(-\frac{E - E_V}{k_B T_V}\right) \tag{1.4}$$

5. a Gaussian shaped deep defect band centered at E_{mGauss} with a width w_{Gauss} and state density at maximum N_{0m}:

$$N_{DD}(E) = N_{0m}\exp\left(-\frac{(E - E_{m\,Gauss})^2}{2w_{Gauss}^{\;2}}\right), \tag{1.5}$$

where $\hbar$ is the normalized Planck constant, m_e ans m_h are the effective masses of an electron and a hole respectively, N_C and N_V are densities of states in the conduction and valence band respectively, T_C and T_V are characteristic temperatures that define the slope of the tails, E_V and E_C are the valence band edge and conduction band edge energies respectively, $N(E_V)$ and $N(E_C)$ are the state densities at the corresponding band edges.

The most commonly used model for the DOS in the gap is the one introduced by Mott and Davis [30]. Compared to the typical DOS, they introduced two deep defect Gaussian distributions instead of a single one. Thus, according to this model the density of states in the band gap is written in the following way:

$$N(E) = N(E_C)\exp\left(-\frac{E_C - E}{k_B T_C}\right) + N(E_V)\exp\left(-\frac{E - E_V}{k_B T_V}\right) + N_{0m1}\exp\left(-\frac{(E - E_{mGauss1})^2}{2w_{Gauss1}^2}\right) + N_{0m2}\exp\left(-\frac{(E - E_{mGauss2})^2}{2w_{Gauss2}^2}\right) \quad (1.6)$$

An example of the density of states distribution according to the model of Mott and Davis is presented in Fig.1.2.

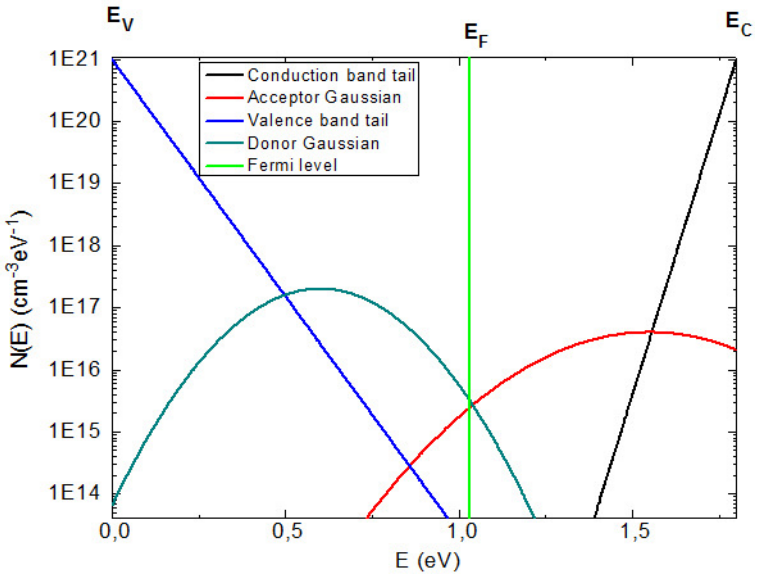

Fig.1.2. Density of state distribution in the gap of amorphous silicon introduced by Mott and Davis.

1.1.3.1 Dangling bonds

As it was mentioned above, the main coordination defect in amorphous silicon is the three-fold coordinated silicon with a dangling bond. The Pauli exclusion principle states that each quantum level of the defect may be occupied by up to two electrons, so that a defect with a single level can exist in three charge states depending on the position of the Fermi energy, as illustrated in Fig.1.3. Indeed, a dangling bond (DB) being a coordination defect can be positively charged (D^+), neutral (D^0), or negatively charged (D^-) if occupied by zero, one, or two electrons, respectively. This kind of defect is described in the energy domain by two

levels E_{DB} and $E_{DB}+E_{cor}$, where E_{cor} is the correlation energy. The sign and the value of the correlation energy depend on the material considered. It is generally accepted that the correlation energy is negative in chalcogenide glasses such as a-As_2Se_3, whereas it is positive in tetrahedrally bounded amorphous semiconductors such as a-Si:H [31,32]. Figure 1.3 illustrates the energy position of DB in the band gap and the position transitions to the conduction and valence bands.

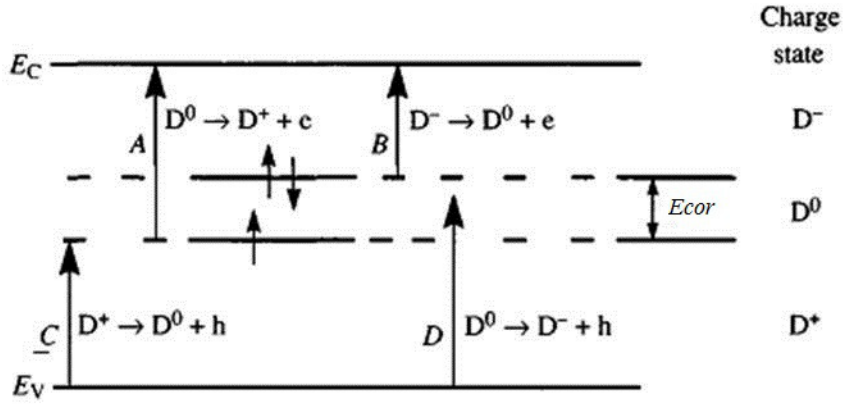

Fig.1.3. The one-electron and two-electron energy levels of a defect and the four possible transitions to the conduction and valence bands. The charge state is indicated when the Fermi energy lies in the different energy ranges. The defect is assumed to be neutral when singly occupied, with a positive correlation energy, E_{cor} (from [19]).

The electronic energies of the first and second electrons are not the same because of electron-electron interactions. The two electrons repel each other with a Coulomb interaction which is absent in the singly occupied state. The energy levels are split by the correlation energy,

$$E_{cor} = \frac{q^2}{4\pi\varepsilon\varepsilon_0 r_e}, \tag{1.7}$$

where q is the elementary charge, $\varepsilon\varepsilon_0$ is the dielectric constant of the material, r_e is the effective separation of the two electrons and so is roughly the localization length of the defect wavefunction. As a rough estimate of the Coulomb interaction E_{cor} = 130 meV for r_e = 10 Å.

The DB states play an essential role in the material properties and they are included in almost all the models developed as an explanation for the experimental results performed on amorphous or glassy semiconductors. For instance, their influence on the steady-state photoconductivity has been widely studied [33,34]. These states are also involved in the thermal equilibrium processes observed in a-Si:H [35,36], as well as in the light-induced

metastabilities known as the Staebler-Wronsky effect.

However, the inclusion of the dangling bonds states into analysis is complicated. They are mainly considered as discrete levels [18] instead of distributions of states, and, apparently because of the complexity of the calculation linked to their specific statistics, they are often treated as monovalent states [38] by means of well-known statistics such as the one extensively studied by Simmons and Taylor [39].

Combination of experimental results from the modulated photocurrent technique and results from numerical modeling have shown [40,41] that a distribution of DB centers exhibiting a positive correlation energy roughly behaves as two distributions of monovalent states whereas a distribution of DB centers with a negative correlation energy roughly behaves as a single distribution of monovalent states. An important property of the DB states with a positive correlation energy is that they can give a significant response in the trapping- and release-limited regime even if their ground-energy level is below the Fermi level.

1.2 Growth of a-Si:H

The fabrication of a-Si:H films with improved properties (low defect density, higher carrier mobility, enhanced stability,etc.) has led to explore a large number of deposition methods and, within each of them, the effects of each process parameter [42].

A wide range of deposition techniques have been developed, which can be divided into two main categories: 1) those based on a physical process such as evaporation and sputtering; and 2) those based on chemical processes, known under the generic term of chemical vapour deposition (CVD).

Amorphous silicon films produced by evaporation of a silicon target or by sputtering in the absence of hydrogen exhibit a high density of defects which make them useless for electronic applications. In contrast, the films produced by the dissociation of hydride gases have a low defect density which allows doping [43]. It took a few years to recognize the fundamental role of hydrogen in the passivation of silicon dangling bonds and thus in reducing the density of defects in the gap of the semiconductor.

Different methods have been used to dissociate the gas precursors, all variants of a CVD process: HOMOCVD, PECVD, PHOTOCVD, etc. Thin films of hydrogenated amorphous silicon are mainly deposited by Plasma Enhanced Chemical Vapour Deposition (PECVD) technique, among which different excitation modes and geometry of the reactor have been

explored [19,44]. RF (13.56MHz) glow discharge is the most widely used deposition technique because it combines low temperature operation, thanks to the plasma dissociation, and the possibility of scaling-up the size of the substrates. Plasma is defined as an ionized gas that is macroscopically neutral. The ionization of the gas atoms and molecules is achieved by providing energy to the system either thermally, optically or electrically. The most common way for thin film deposition is an electrical discharge between two electrodes. In a-Si:H deposition silane is the most common source even though other hydrides (Si_2H_6, Si_3H_8) [45], fluorides (SiF_4,Si_2F_6) [46], chlorides ($SiCl_4$, SiH_2Cl_2) [47], SiH_3F and SiH_2F_2 [48] source gases have been used.

Figure 1.4 shows a schematic diagram of a parallel-plate PECVD reactor. Besides its simplicity, this type of reactor also benefits from the advantages associated to the plasma processes [49]:

i) Deposition is possible even at room temperature since the dissociation of the gas precursors is produced by collisions with high energy electrons.

ii) Dense and smooth films can be fabricated considering that ions are accelerated towards the substrate and thus can bring energy to the growth zone.

iii) The wide range of gas precursors can be used which allows to produce thin films of various compostion: a-Si:H, a-SiGe:H, a-SiC:H, a-SiO_x, etc. Moreover these films can be made *p*-type or *n*-type by adding either diborane or phosphine to the gas mixture and can be easily stacked on top of each other by changing the flow of gases into the reactor.

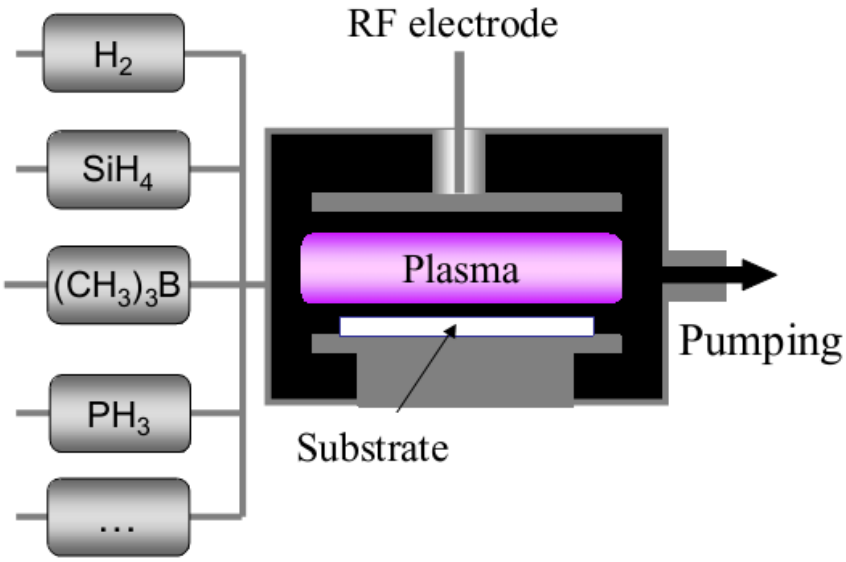

Fig.1.4. Schematic diagram of a plasma enhanced chemical vapor deposition reactor. It consists of a gas handling system, a vacuum system, a RF power electrode and a substrate holder, which is usually heated to ~ 200 °C (from [49]).

Let us now consider briefly main processes that take place in the gas phase. Once SiH_4 is injected in the reactor and the power is applied to the RF electrode, electrons are accelerated by the electric field and gain enough energy to dissociate SiH_4. The primary reactions between electrons and silane can be of different types: dissociation, ionization, attachment, etc. The relative importance of each reaction depends on the energy of the electrons, which is a function of the electric field (from which they gain energy) and their mean free path, which depends on the total pressure. The results of the primary reactions are the radicals and ions responsible for a-Si:H deposition [50]. One should also consider secondary reactions that are interactions of the products of primary reactions mainly with the silane molecules. The degree of dissociation in most silane plasmas for a-Si:H deposition is typically 10%.

Gas phase processes are important because they determine the nature of the reactive species contributing to a-Si:H deposition. However, a-Si:H growth cannot be considered just as a condensation of radicals on the substrate. Indeed, while the radicals and ions responsible for a-Si:H deposition are highly hydrogenated, a-Si:H films contain ~10% hydrogen. Thus cross-linking reactions must take place at the film surface or in a growth-zone [51]. The growth model is schematically shown in Fig.1.5.

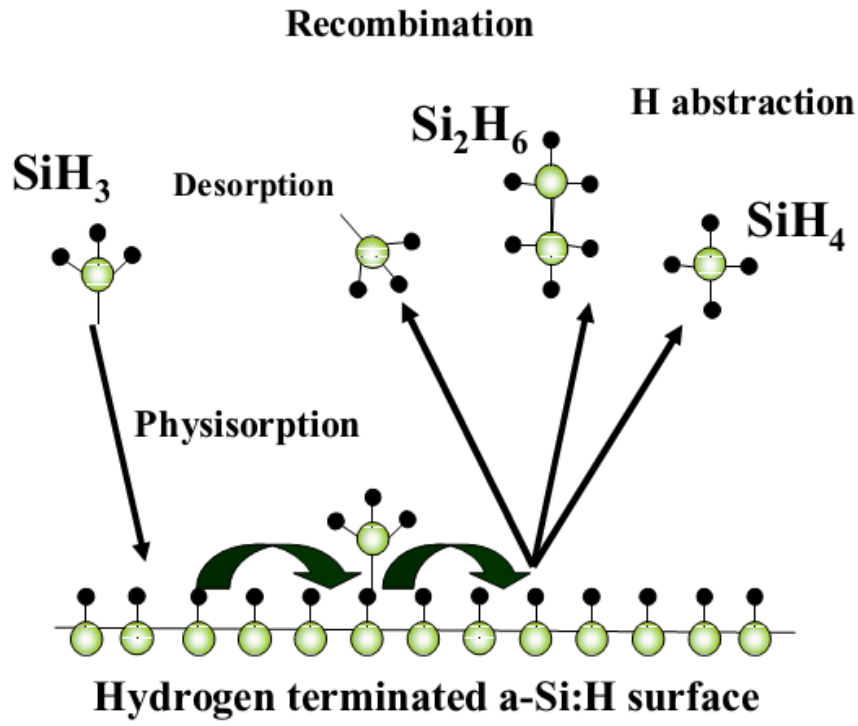

Fig.1.5. Standard view for the deposition of device quality a-Si:H thin films based on the interaction of SiH_3 radicals with a hydrogen terminated silicon surface (from [49]).

The radicals produced in the plasma reach the film surface via diffusion through the sheath (transition region between the plasma and the reactor walls) and land on a hydrogen terminated silicon surface. Because of the low deposition temperature (~ 200 °C) the radical is expected to be adsorbed rather than to form a chemical bond since the thermal energy is not sufficient to break Si-H bonds. The physisorption and diffusion of the radicals along the surface are the processes defining the growth of a film. During this diffusion process SiH_3 may undergo various reactions: 1) highly probable desorption of SiH_3; 2) recombination with another SiH_3 to produce a Si_2H_6 molecule; 3) abstraction of a hydrogen atom producing a SiH_4 molecule and leaving a surface dangling bond available for the next SiH_3 to form a chemical bond; and 4) formation of a chemical bond with a silicon dangling bond at the surface, leading to deposition.

The optimization of a-Si:H growth has been one of the main subjects in this field. The effects of different plasma conditions, reactor geometry, excitation frequency and dilution of the silane on a-Si:H properties have been widely studied [52]. The difficulty of optimizing a-Si:H growth is related to the fact that these parameters are correlated. Indeed, the important aspects for the growth are the rate of production of reactive species, their interaction during their diffusion to substrates and their reactions at the growing surface.

Increasing the RF power, for example, increases the dissociation rate and therefore the

deposition rate. However, the higher dissociation may result in a change in the species involved in the growth because of an increasing importance of secondary reactions [53].

The dilution of silane in inert gases (argon, helium, xenon) can affect the electron distribution function, the rate of silane dissociation and therefore the deposition rate [54]. While inert gases do not play a role in the reactions taking place at the film surface or in the growth-zone, the use of hydrogen dilution strongly modifies them. The use of hydrogen dilution has been reported as an excellent way to improve a-Si:H properties [55]. A high concentration of hydrogen causes the deposited films to become crystalline rather than amorphous. The crystallite size is small, often less than 100 Å, so that the material is termed microcrystalline silicon (μc-Si) [56,57].

The growth of a-Si:H thin films by the dissociation of gas precursors in a glow discharge is a complex process in which gas phase reactions as well as surface reactions have to be considered. In-situ diagnostic techniques of the plasma phase and of the growing film provide valuable information to understand the growth mechanisms and help to optimize the deposition conditions. These in-situ techniques are complemented by ex-situ characterization methods providing complementary information on the optical and electronic properties of the films.

1.3 Photovoltaic applications of hydrogenated amorphous silicon

Although amorphous silicon has poorer electronic properties than crystalline silicon, it offers the important technical advantage of being deposited inexpensively and uniformly over a large area. The applications are therefore almost entirely in situations in which either a large device or a large array of devices is needed. The technology which has received the most attention is the photovoltaic solar cell - large scale power production obviously depends on the ability to cover very large areas at a low cost. Input and output devices such as displays, photocopiers and optical scanners also take advantage of the large area deposition capability.

1.3.1 Amorphous silicon solar cells

The photovoltaic effect was first observed in amorphous silicon in 1974 at RCA Laboratories [58]. The amorphous silicon films were grown by the dc glow-discharge decomposition of silane (SiH_4). Both Schottky-barrier and *p-i-n* devices were fabricated but the conversion efficiencies were limited to less than 1% mainly because of poor contacts. By 1976 the efficiency of the *p-i-n* structure had been improved to 2.4% [59], and in 1977 an

efficiency of 5.5% was obtained in a small (2 mm^2) Schottky-barrier device [60]. In particular, it was becoming clear that hydrogen was playing an important role in assuring the good semiconducting properties of amorphous silicon and that the films were actually silicon - hydrogen alloys (a-Si:H) [5,61].

Continued optimization of the deposition conditions led to efficiencies as high as 6.1% in *p-i-n* cells (1.19 cm^2) by 1980 [62]. An efficiency of 6.3% was reported for a small (4.2 mm^2) metal - insulator- semiconductor (MIS) device fabricated from a glow discharge in SiF_4 and H_2 [63]; the film used in this MIS device was a silicon-hydrogen-fluorine alloy (a-Si:H:F).

One of the key advances in the development of a-Si:H alloys for solar cells was the discovery that the bandgap can be changed by varying the incorporation of hydrogen. Moreover, as in the case of the crystalline materials, the bandgap of a-Si-based alloys can be varied by alloying with carbon or germanium. In 1981 an efficiency of 7.5% was obtained for a *p-i-n* structure (3.3 mm^2) in which the *p* layer was a boron-doped silicon-carbon-hydrogen alloy (a-Si:C:H) [64]. A further improvement in conversion efficiency to 8.5% was obtained in 1982 with a stacked junction structure (9 mm^2) that utilized an amorphous silicon-germanium-hydrogen alloy (a-Si:Ge:H) in the back junction of three stacked *p-i-n* junctions [65]. Up to now a record efficiency of 10.1% has been achieved in a *p-i-n* structure (1 cm^2) deposited on doped LPCVD-ZnO in Oerlikon Solar Lab in Neuchatel [66].

The operation of all solar cells is based on common physical principles. However, since efficient a-Si based solar cells rely on material properties distinctly different from those of crystalline silicon, the basic cell structures are somewhat different. In order to take advantage of the excellent properties of the intrinsic (undoped) a-Si:H and a-Si:Ge:H materials, *p-i-n* and *n-i-p* heterojunction cell structures are used rather than the classic *n-p* junction structures in crystalline silicon [67]. However due to the short lifetime in the highly defective doped materials the photogenerated carriers in the doped layers are not collected and do not contribute to the cell photocurrents.

The fabrication of a *p-i-n* cell begins with the deposition of a *p*-type 'window layer' on the transparent conductive oxide (TCO). An a-Si:H intrinsic layer (*i*-layer) is deposited to form the bulk absorber region of the cell. The final step in forming the single-junction *p-i-n* cell is the *n*-layer deposition.

In order to minimize optical absorption the *p*-type window layers used in high efficiency cells are thin (~10 nm). In order to maximize the cell efficiency it is necessary to achieve a high V_{oc} (open circuit voltage) using a very thin *p*-layer. If the *p*-layer is too thick the device performance will be adversely affected by the loss in the photocurrent due to the higher absorption in the thick *p*-layer.

Most of the important differences in the physics of a-Si based solar cells and crystalline silicon solar cells origin from the most fundamental difference in the materials - the large density of localized gap states in a-Si:H. In a-Si solar cells, absorbed light in the *i*-layer will create electrons and holes, and the collection of these photogenerated carriers is assisted by the internal electric field. Due to the short carrier lifetimes associated with the localized gap states, the photogenerated carriers in a-Si based cells must be collected primarily as a drift current, not as a diffusion current as is the case of crystalline silicon solar cells. These gap states impose significant constraints on the cell performance since a large density of photogenerated carriers can be trapped in these states. The native and light-induced defects in a-Si *p-i-n* devices negatively affect the carrier collection in two ways - they act as recombination centers and also shield the electric field produced by the doped layers – which changes the electric field distribution in the *i*-layer.

Open-circuit voltages in the amorphous cells just as in crystalline solar cells are determined by the quasi-Fermi level splitting, which depends on the density of photogenerated carriers and the band gap (E_g); this in turn leads to the well-known dependence of V_{oc} on E_g. Large values of the built-in potential (V_{bi}) are desirable not only in that they can limit the quasi-Fermi level splitting but also because they determine the electric field across the *i*-layer, which is important in the collection of the photogenerated carriers.

The short circuit current densities (J_{sc}) are determined by the collection of carriers photogenerated in the *i*-layer, which depends on its optical absorption and thickness as well as the ability to extract them from the cell. The amount of absorbed sunlight can be readily increased by making the *i*-layers thicker. However, field-assisted carrier collection is also sensitive to thickness, which results in a negative effect on carrier collection. This adversely affects not only J_{sc}, but generally has an even larger negative effect on the fill factor, since the internal fields are significantly reduced under load (forward bias). The challenge is not only to maximise the optical absorption, such as by increasing the thickness of the *i*-layer, but also to improve carriers collection to reach high values of the fill factor. A major breakthrough in achieving this result is obtained with optical enhancement based on textured substrates and reflectors [68]. This optical enhancement effect greatly increases the already high optical absorption at longer wavelengths so that significantly higher quantum efficiencies can be obtained at these wavelengths without any increase in the cell thickness. The development of tandem a-Si:H/a-SiGe:H and triple a-Si:H/a-SiGe:H/a-SiGe:H cell structures allows not only a larger fraction of the incident sunlight to be absorbed, but also allows this increased absorption to be achieved with thin intrinsic absorber layers.

Today amorphous silicon represents 3% of global photovoltaic market, being the leader in the thin film solar cells technology. The improving of these cells can be performed in several areas [69]:

- further optimization of the tandem-junction thin-film deposition process;

- modification of the current processes used to texturize the transparent conductive oxides (TCOs), which will improve the light-trapping efficiency and thus overall efficiency of the cell;

- the development of materials to support the transition to nanostructured silicon, including silicon nanowires and silicon-based quantum dot absorbers, which if successful could provide a path to efficiencies above 15%.

1.3.2 Amorphous silicon / crystalline silicon heterojunction solar cells

Wafer-based crystalline silicon solar cells are still dominating in the photovoltaic market with an overall share of 87% (2011), and feature a high module efficiency varying from 18% to 24% [70]. The crystalline silicon (c-Si) technologies are characterized by high temperatures processes: diffusion of dopants or annealing after ion implantation. The formation of the back surface field (BSF) layer requires high temperatures as well. Hence the fabrication of crystalline silicon solar cells is an energy consuming and consequently high cost process. The amorphous silicon production, on the contrary, does not require high temperatures. Thus, thin-film silicon solar cells based on hydrogenated amorphous silicon (a-Si:H) and hydrogenated microcrystalline silicon (μc-Si:H) are promising candidates for low-cost PV technology due to their low material consumption and low temperature processing in comparison to wafer-based c-Si solar cells. Moreover, thin-film silicon solar cells can be fabricated on a range of substrates, including flexible metal foils [71]. In order to realize reliable devices characterized by high efficiency of conventional c-Si and low cost that of a-Si:H, an approach has been developed on the basis of amorphous/crystalline silicon heterojunction solar cells (SHJ), which combines wafer and thin film technologies [71].

In this area impressive results were achieved by Sanyo Electric with the so called a-Si/c-Si Heterojunction with Intrinsic Thin layer (HIT) solar cell [72,73]. This technology showed excellent surface passivation (open circuit voltage (V_{oc}) values of around 730 mV) and a conversion efficiency of 23.7% was obtained for a cell size of 100.4 cm^2 [74]. Moreover, Sanyo has also achieved very high efficiencies in mass production: 20% efficiency at the cell level, and 18.3% at the module level [75,76]. The latest world record efficiency of 24.7% belongs to Panasonic achieved as well on HIT type solar cell of practical size (100 cm^2 and above) [77].

To compare with conventional crystalline silicon solar cells the world record belongs to the research group from the University of New South Wales with 25% efficiency achieved on

c-Si with the so-called PERL (passivated emitter rear locally diffused) [78]. Similarly, the high efficiency "point contact" technology from SunPower exhibits an impressive performance of 24.2% [79] on production size wafer of 155.1 cm^2 area.

The design of the silicon heterojunction solar cell is based on an emitter and back surface field (BSF) that are produced by low temperature growth of ultra-thin layers of amorphous silicon on both sides of a thin crystalline silicon wafer-base, typically of the order of 200 µm thick, where electrons and holes are photogenerated. The low temperature a-Si:H deposition lowers the thermal budget in the production of the cell, and at the same time will allows for high throughput production machinery.

The idea of silicon heterojunctions solar cells was first published in 1974 by Walther Fuhs and coworkers [80]. However, it turned out that to obtain the V_{oc} potential > 700 mV inherent to the heterojunction concept, it is mandatory to include additional, very thin (less than 10 nm thick) undoped – so called intrinsic – a-Si:H buffer layers between the wafer and the doped (emitter or BSF) a-Si:H layers. The reason has been already mentioned above - the defect density in a-Si:H increases strongly with doping, and this leads to an increase in interface defect density at the a-Si:H/c-Si junction, leading to enhanced recombination and to lower V_{oc}. This finding was patented by Sanyo in 1991. After formation of the a-Si:H/c-Si heterojunction, the cell is contacted using a ~80 nm thin transparent conductive oxide (TCO) layer and a metal grid on the front. A scheme of a HIT cell is presented in Fig.1.6. The TCO is typically InO doped with Sn (ITO) or ZnO doped with Al. Often, a TCO is also used to form a dielectric mirror on the back side of the cell.

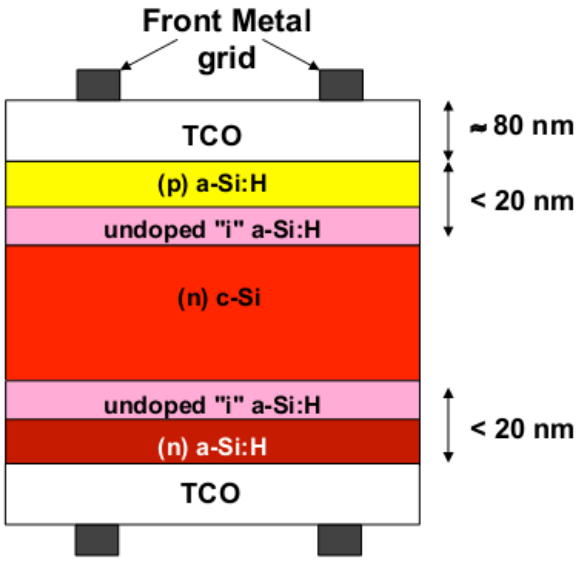

Fig.1.6. Schematic structure of the Sanyo HIT solar cell.

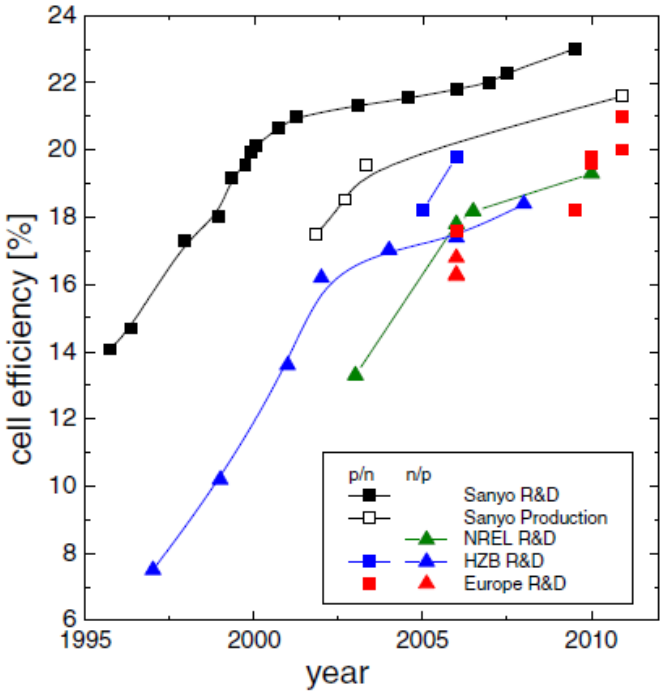

Fig.1.7. Development of a-Si:H/c-Si heterojunction cell efficiency vs. time. Both (n) a-Si:H/(p) c-Si (p/n in the legend) and (p) a-Si:H/(n) c-Si cell (n/p in the legend) structures are shown (from [72]).

The reported cell efficiencies have developed accordingly: Fig.1.7 provides an overview on the progress over time, where the distinction is made between (n) a-Si:H/(p) c-Si type cells and the "canonical" (p) a-Si:H/(n) c-Si structure as used by Sanyo. There is evidence for the gap in cell efficiencies between the two doping sequences due to differences in fundamental device physics (carrier mobilities, band offsets). Furthermore, it is apparent that the Sanyo HIT cell has a significant lead on the reported cell efficiencies.

Inspired by the impressive results of Sanyo many research centers worldwide have been focused on the development of HJ solar cells. In the USA, the National Renewable Energy Laboratory (NREL) reported a 19.3% efficiency on *p*-type c-Si wafers using hot-wire CVD (HWCVD) instead of PECVD for a-Si:H deposition [75]. In Europe, Roth & Rau obtained V_{oc} values up to 735 mV and conversion efficiencies of 21.9% on 4 cm^2 and 20.3% on 149 cm^2 [81]. In Ecole Polytechnique Fédérale de Lausanne (EPFL) in the Photovoltaics-Laboratory (PV-Lab) Neuchatel, high open-circuit voltages have been obtained on both types of float zone (FZ) wafers: up to 735 mV on *n*-type, and 726 mV on *p*-type. The best V_{oc} measured on Czochralski (CZ) *p*-type wafers was only 692 mV, whereas it reached 732 mV on CZ *n*-type. The highest aperture-area certified efficiencies obtained on 4 cm^2 cells are 22.14% (V_{oc} = 727 mV, FF = 78.4%) and 21.38% (V_{oc} = 722 mV, FF = 77.1%) on *n*- and *p*-type FZ wafers, respectively, proving that heterojunction schemes show comparable performance on high-quality *p*-type as on *n*-type wafers. This is the highest efficiency ever reported for a full

silicon heterojunction solar cell on a *p*-type wafer, and the highest V_{oc} on any *p*-type crystalline silicon device [82].The National Institute of Solar Energy (INES) in France, that provided samples studied in this work, is conducting research on a-Si:H/c-Si heterojunction solar cells since 2006. INES has reached one of the highest efficiencies in Europe on large area (148cm^2) *n*-type c-Si wafers and solar cells with up to 20.4% and 720 mV of V_{oc} (21% and 732mV on 105 cm²) have been reported [83].

In most heterojunction silicon solar cells, an undoped a-Si:H layer ((i) a-Si:H) is used as a surface passivation layer, and this layer has been considered essential to achieve high performance. However, Helmholtz Zentrum Berlin (HZB) prepared high quality heterojunction solar cells without an intrinsic a-Si:H passivation layer [84]. They demonstrated that smoothing procedures after additional texturing and cleaning resulted in improved surface uniformity and an improved overall device performance. Without an intrinsic a-Si:H passivation layer in the solar cell, HZB achieved efficiencies as high as 19.8% on surface-textured wafers. However, a doped a-Si:H layer cannot passivate the surfaces of c-Si wafers as well as an undoped a-Si:H buffer layer [85]. Consequently, the interface defect-state density is expected to be high, resulting in a relatively low V_{oc}.

Over the last decade, there have been many encouraging results on developing alternative concepts based on a-Si:H/c-Si heterojunctions for high efficiency cells: no undoped buffer layer and lowering of the doping levels in the emitter and BSF, use of *p*-type *c*-Si substrates (the HIT cell is produced on *n*-type material), use of other materials than a-Si:H like a-Si:H/μc-Si stacks, a-SiC:H, etc.

Besides all the experimental research, simulation studies of the performance of heterojunction silicon solar cells are very important in order to understand the operation of the solar cells and to optimize the design of solar-cell structures. The AFORS-HET (**A**utomat **FOR S**imulation of **HET**erostructures) software developed by HZB in Germany has been widely used for the simulation study of heterojunction silicon solar cell. It will be referred later in this work.

1.4 Aim of this work

In this thesis, research on a-Si:H Schottky diodes and a-Si:H/c-Si heterojunctions is presented with the focus on the capacitance spectroscopy and information on electronic properties that can be derived from this technique.

After an introduction on the basics of *p-n* junctions, the fundamental principles of

capacitance technique are presented as well as its applications in studying Schottky barriers. Possibilities of *C-V* measurements and admittance spectroscopy are addressed in Chapter 2.

In chapter 3, capacitance spectroscopy in a-Si:H Schottky diodes is investigated. First, dynamics of capture-release processes from the defect states in the band gap is described in order to provide a deep comprehension of the origin of a capacitance signal in a Schottky barrier formed on an imperfect semiconductor. Explicit derivation of capacitance in such a barrier is given and a simplified treatment of the capacitance-temperature (*C-T*) dependencies suggested by Cohen and Lang [86] is described. The possibilities of the capacitance technique to determine the density of states (DOS) at the Fermi level, the position of the Fermi level and the attempt-to-escape frequency are studied using numerical modeling of a-Si:H Schottky diodes. A particular interest is devoted to the critical assessment of the mentioned treatment that, to our knowledge, has not been carried out. A discussion on the validity of the model suggested in Ref.[86] when applied to different cases is presented. In the second part of the chapter, a comparison of the experimental capacitance data with the modeling is carried out. The objective of this part is to study the possibility of fitting the experimental data by numerical calculations with the input parameters obtained from other experimental technique. A comparison of the parameters derived from the treatment of the experimental *C-T* data and the introduced into simulation for best fitting of the latter is provided as well.

In chapter 4, a theory on a-Si:H/c-Si heterojunctions such as band diagram analysis and electronic properties, namely the existence of an interfacial inversion layer, is presented. First, we focus on the study of the frequency dependent low temperature range of capacitance-temperature dependencies of a-Si:H/c-Si heterojunctions. The analysis of the low-temperature steps in capacitance-temperature dependencies is presented. These steps are attributed to the different processes taking place in the amorphous layer: the response of the gap states to the ac modulation in the bulk and in the inversion layer at the interface and the transport of charge. The origin of these steps is studied by means of numerical modeling. In the second part of the chapter, a quasi-static regime of capacitance signal is studied. A complete analytical calculation of capacitance of the heterojunction is developed. A comparison with the depletion approximation calculations is given and the limitations of the latter are discussed. The application of capacitance measurements in the derivation of the band-offsets is studied. Experimental and analytically obtained *C-V* dependencies are compared. The influence of the inversion layer at the interface on the *C-V* profiles is assessed. Finally, this work concludes with a summary of the main results and gives some prospects for future studies.

1.5 References

[1] Mary Elvira Weeks, "*Discovery of the Elements*", Kessinger Publishing Reprints, 2003.

[2] J. Tauc, ed. "*Amorphous and Liquid Semiconductors*", Plenum, New York, 1974.

[3] H. F. Sterling and R. C. G. Swann, *Solid State Electronincs*, vol. 8, p. 653, 1965.

[4] R. C. Chittick, J. H. Alexander, and H. F. Sterling, *Journal of Electrochemical Society*, vol. 116, p. 77, 1969.

[5] A. Triska, D. Dennison, and H. Fritzsche, *Bulletin of the American Physical Society*, vol. 20, p. 392, 1975.

[6] H. Fritzsche. In: *Proceedings of the 7th International Conference on Amorphous and Liquid Semiconductors*, Edinburgh, p. 3, 1977.

[7] W. Spear and P. LeComber, *Solid State Communications*, vol. 17, p. 1193, 1975.

[8] D. E. Carlson and C. R. Wronski, *Applied Physic Letters*, vol. 28, p. 671, 1976.

[9] H. Okamoto, Y. Nitta, T. Yamaguchi, and Y. Hamakawa, *Solar Energy Materials*, vol. 3, p. 313, 1980.

[10] Y. Hamakawa, *Materials Research Society Symposium Proceedings*, vol. 609, A17.2.1, 2000.

[11] Y. Kuwano, T. Imai, M. Ohnishi, and S. Nakano. In: *Proceedings of the 14th IEEE Photovoltaic Specialists Conference*, p. 1408, 1980.

[12] P. G. LeComber, W. E. Spear, and A. Ghaith, *Electronics Letters,* vol. 15, p. 179, 1979.

[13] A. J. Snell, K. D. MacKenzie, W. E. Spear, P. G. LeComber, and A. J. Hughes, *Applied Physics,* vol. 24, p. 357, 1981.

[14] M. J. Powell, B. C. Easton, and O. F. Hill, *Applied Physic Letters*, vol. 38, p. 794, 1981.

[15] R. L. Weiseld, *Journal of Non-Crystalline Solids*, vol. 164, p. 771, 1993.

[16] T. C. Chuang, L. E. Fennel, W. B. Jackson, J. Levine, M. J. Thompson, H. C. Tuan, and R. Weiseld, *Journal of Non-Crystalline Solids*, vol. 97-98, p. 301, 1987.

[17] L. E. Antonuk, C. F. Wild, J. Boundry, J. Jimenez, M. J. Longo, and R. A. Street, *IEEE Transactions* on *Nuclear Science*, NS-37, p. 165, 1990.

[18] C. van Berkel, N. C. Bird, C. J. Curling, and I. D. French, *Materials Research Society Symposium Proceedings*, vol. 297, p. 939, 1993.

[19] R. A. Street, "*Hydrogenated amorphous silicon*", Cambridge Solid State Science Series, 1991.

[20] W. H. Zachariasen, *Journal of American Chemical Society*, vol. 54, p. 3841, 1932.

[21] D. E. Polk, *Journal of Non-Crystalline Solids*, vol. 5, p. 365, 1971.

[22] M. A. Paesler, D. E. Sayers, R. Tsu, and J. G. Hernandez, *Physical Review B*, vol. 28, p. 4550, 1983.

[23] M. F. Thorpe and D. Weaire, *Physical Review Letters*, vol. 26, p.1581, 1971.

[24] N.F. Mott, "The mobility edge since 1967", *Journal of Physics C: Solid State Physics*, vol. 20, p. 3075, 1987.

[25] B. Abeles, C. R. Wronski, T. Tiedje, G. D. Cody, *Solid State Communications*, vol. 36, p. 537, 1980.

[26] G. D. Cody, B. Abeles, C. R. Wronski, R.B. Stephens, B. Brooks, *Solar Cells*, vol. 2, p. 227, 1980.

[27] R. Hulthen, *Physica. Scripta,* vol. 12, p.342, 1975.

[28] D. T. Pierce, W. E. Spicer, *Physical Review B,* vol. 5, p.3017, 1972.

[29] L. Ley: "Electronic structure". In: Tim Searle (ed) "*Properties of amorphous silicon and its alloys*", The Institution of Electrical Engineers, London, 1998.

[30] E. A. Davis et N. F. Mott, *Philosophical Magazine B*, vol. 22, p. 903, 1970.

[31] D. Adler, *Physical Review Letters*, vol. 41, p. 1755, 1978.

[32] J. K. Lee and E. A. Schiff, *Physical Review Letters*, vol. 68, p. 2972, 1992.

[33] F. Vaillant and D. Jousse, *Physical Review B*, vol. 34, p. 4088, 1986.

[34] H. Okamoto, H. Kida, and Y. Hamakawa, *Philosophical Magazine B*, vol. 49, p. 231, 1984.

[35] R.A. Street, J. Kakalios, C. C. Tsai, and T. M. Hayes, *Physical Review B*, vol. 35, p. 1316, 1987.

[36] M. Meaudre, P. Jensen, and R. Meaudre, *Philosophical Magazine B*, vol. 63, p. 815, 1991.

[37] E. Morgado, *Philosophical Magazine B*, vol. 63, p. 529, 1991.

[38] S. Lee, M. Gunes, C. R. Wronski, N. Maley, and M. Bennet, *Applied Physic Letters*, vol. 59, p. 1578, 1991.

[39] J. G. Simmons and G. W. Taylor, *Physical Review B*, vol. 4, p. 502, 1971.

[40] C. Longeaud and J. P. Kleider, "General analysis of the modulated-photocurrent experiment including the contributions of holes and electrons", *Physical Review B*, vol. 45, p.11672, 1992.

[41] C. Longeaud and J. P. Kleider, "Trapping and recombination via dangling bonds in amorphous and glassy semiconductors under steady-state conditions: Application to the modulated photocurrent experiment", *Physical Review B*, vol. 48, p. 8715, 1993.

[42] P. Roca i Cabarrocas: "Preparation". In: Tim Searle (ed) "*Properties of amorphous silicon and its alloys*", The Institution of Electrical Engineers, London, 1998.

[43] M. Stutzmann, D. K. Biegelsen, R. A. Street, *Physical Review B*, vol. 35, p.5666, 1987.

[44] R. A. Street, *Philosophical Magazine B*, vol. 60, p.213, 1989.

[45] J .Robertson, *Physical Review B*, vol. 31, p.3817, 1985.

[46] R.A. Street, J. Kakalios, T. M. Hayes, *Physical Review B*, vol. 34, p.3030, 1986.

[47] M. Stutzmann, *Philosophical Magazine B*, vol. 53, p.L15, 1986.

[48] F.J. Kampas, P. E. Vanier, *Physical Review B*, vol. 31, p. 3654, 1985.

[49] P. Roca i Cabarrocas: "Deposition Techniques and Processes Involved in the Growth of Amorphous and Microcrystalline Silicon Thin Films". In: Wilfried G.J.H.M. van Sark, Francesco Roca, Lars Korte (eds.) "*Physics and Technology of Amorphous-Crystalline Heterostructure Silicon Solar Cells"*, Springer-Verlag Berlin Heidelberg, 2012.

[50] J. P. M. Schmitt, *Journal of Non-Crystalline Solids*, vol. 59-60, p. 649, 1983.

[51] B. A. Scott, J. Reimer, P. A. Longeway, *Journal of Applied Physics*, vol. 54, p. 6853 1983.

[52] W. Luft, Y. S. Tsuo "*Hydrogenated Amorphous Silicon Deposition Processes*". Ed. A. M. Hermann, Marcel Dekker Inc., NewYork, 1993.

[53] J. R. Doyle, D. A. Doughty, A. Gallagher, *Journal of Applied Physics*, vol. 68, p. 437, 1990.

[54] J. C. Knights, R. A. Lujan, M. P. Rosenblum, R. A. Street, D. K. Biegelsen, J. A. Reimer, *Applied Physic Letters*, vol. 38, p. 331, 1981.

[55] X. Xu, J. Yang, S. Guha, *Journal of Non-Crystalline Solids*, vol. 198-200, p.60, 1996.

[56] N. Layadi, P. Roca i Cabarrocas, B. Drevillon, I. Solomon, *Physical Review B*, vol. 52, p.5136, 1995.

[57] S. Hamma, P. Roca i Cabarrocas, *Journal of Applied Physics*, vol. 81, p.7282, 1997.

[58] D. E. Carlson, U.S. Patent 4,064,521, 1977.

[59] D. E. Carlson and C. R. Wronski, *Applied Physic Letters*, vol. 28, p. 671, 1976.

[60] D. E. Carlson, *IEEE Transactions on Electron Devices,* vol. 24, p. 449, 1977

[61] G. A. N. Connell and J. R. Pawlik, *Physical Review B,* vol. 13, p. 787, 1976.

[62] D. E. Carlson, *Solar Energy Materials,* vol. 3, p. 503, 1980.

[63] A. Madan, J. McGill, W. Czubatyj, J. Yang, and S. R. Ovshinsky, *Applied Physic Letters,* vol. 37, p. 826. 1980.

[64] Y. Tawada, M. Kondo, H. Okamoto, and Y. Hamakawa. In: *Proceedings of the 16th IEEE Photovoltaic Specialists Conference, San Diego,* vol. 15, p. 245, 1981.

[65] G. Nakamura, K. Sato, H. Kondo, Y. Yukimoto, and K. Shirahata. In: *Proceedings of the 4th European Community Photovoltaic Solar Energy Conference, Stressa. Italy,*. p. 616, 1982

[66] Benagli S., Borrello D., Vallat-Sauvain E., Meier J., Kroll U., Hötzel J., Spitznagel J., Steinhauser J., Castens L., Djeridane Y., "High-efficiency amorphous silicon devices on LPCVD-ZNO TCO prepared in industrial KAI-M R&D Reactor", *24th European*

Photovoltaic Solar Energy Conference, Hamburg, September 2009.

[67] David E. Carlson, C. R. Wronski: Amorphous Silicon Solar Cells. In: Tom Markvart and Luis Castafier (Eds.) "*Practical Handbook of Photovoltaics*", Elsevier Science Ltd. Oxford, 2003.

[68] E. Yablonovitch, and G. D. Cody, "Intensity enhancement in textured optical sheets for solar cells", *IEEE Transactions on Electron Devices*, vol. 29, p. 300, 1982.

[69] http://www.renewableenergyfocus.com/view/1131/amorphous-silicon-will-continue-to-dominate-thin-film-pv-market/

[70] http://www1.eere.energy.gov/solar/sunshot/pv_crystalline_silicon.html

[71] Miro Zeman and Dong Zhang: "Heterojunction Silicon Based Solar Cells". In: Wilfried G.J.H.M. van Sark, Francesco Roca, Lars Korte (eds.) "*Physics and Technology of Amorphous-Crystalline Heterostructure Silicon Solar Cells*", pp. 13-43, Springer-Verlag Berlin Heidelberg, 2012

[72] T. Mishima, M. Taguchi, H. Sakata, E. Maruyama, "Development status of highefficiency HIT solar cells", *Solar Energy Materials and Solar Cells*, vol. 95, p. 18, 2011.

[73] T. Kinoshita, D. Fujishima, A. Yano, A. Ogane, S. Tohoda, K. Matsuyama, Y. Nakamura, N. Tokuoka, H. Kanno, H. Sakata, M. Taguchi, and E. Maruyama, "The approaches for high efficiency HIT solar cells with very thin (<100µm) silicon wafer over 23%". In: *Proceedings of the 26th European Photovoltaic Solar Energy Conference and Exhibition,* Hamburg, Germany, pp. 871-874, 2011.

[74] Q. Wang, M. R. Page, E. Iwaniczko, Y. Xu, L. Roybal, R. Bauer, B. To, et al, "Efficient heterojunction solar cells on p-type crystal silicon wafers", *Applied Physic Letters*, vol. 96, p. 013507, 2010.

[75] N. Nakamura, M. Ouchi, K. Ibi, and Y. Watabe. "New approaches to mass production of heterojunction silicon solar cells". In: *26th European Photovoltaic Solar Energy Conference and Exhibition*, Hamburg, Germany, p. 2194, 2011.

[76] HIT photovoltaic module (September 2012). http://panasonic.net/energy/solar/hit/

[77] http://panasonic.co.jp/corp/news/official.data/data.dir/2013/02/en130212-7/en130212-7.html

[78] J. Zhao, A. Wang, M. A. Green, "24.5% efficiency silicon PERT cells on MCZ substrates and 24.7% efficiency PERL cells on FZ substrates", *Progress in Photovoltaics*, vol. 7, p. 471, 1999.

[79] P. J. Cousins, D. D. Smith, H. C. Luan, J. Manning, T.D. Dennis, A. Waldhauer, K. E. Wilson, G. Harley, G. P. Mulligan, "Gen III: improved performance at lower cost". In: *35th IEEE Photovoltaic Specialists Conference*, Honolulu, 2010.

[80] W. Fuhs, K. Niemann et J. Stuke, "Heterojunctions of amorphous silicon and crystalline single crystals", in *Tetrahedrally bonded amorphous semiconductors,* p. 345–350, 1974.

[81] D. Bätzner, Y. Andrault, L. Andreetta, A. Buechel, W. Frammelsberger, C. Guerin et al.

"Characterisation of Over 21% Efficient Silicon Heterojunction Cells Developed at Roth & Rau Switzerland". In: *26th European Photovoltaic Solar Energy Conference and Exhibition*, Hamburg, Germany, p. 1073, 2011.

[82] A. Descoeudres, Z. Holman, L. Barraud, S. Morel, S. De Wolf and C. Ballif, ">21% Efficient Silicon Heterojunction Solar Cells on n- and p-Type Wafers Compared", *IEEE Journal* of *Photovoltaics,* vol. 3, p. 83, 2013.

[83] D. Muñoz, T. Desrues, A.-S. Ozanne, N. Nguyen, S. D. Vecchi, F. Souche et al. « Progress on high efficiency standard and interdigitated back contact silicon heterojunction solar cells". In: *26th European Photovoltaic Solar Energy Conference and Exhibition*, Hamburg, Germany, p. 861, 2011.

[84] L. Korte, E. Conrad, H. Angermann, R. Stangl, M. Schmidt, "Advances in a-Si:H/c-Si Heterojunction Solar Cell Fabrication and Characterization", *Solar Energy Materials & Solar Cells*, vol. 93, p. 905, 2009.

[85] S. De Wolf, S. Kondo, "Nature of doped a-Si:H/c-Si interface recombination", *Journal of Applied Physics*, vol. 105, p. 103707, 2009.[86] J.D. Cohen and D.V. Lang, "Calculation of the dynamic response of Schottky barriers with a continuous distribution of gap states", *Physical Review B*, vol.25, p.5321, 1982.

[86] J.D. Cohen and D.V. Lang, "Calculation of the dynamic response of Schottky barriers with a continuous distribution of gap states", *Physical Review B*, vol. 25, p. 5321, 1982.

2 Application of capacitance spectroscopy in semiconductors

Capacitance spectroscopy has been widely used for semiconductors characterization [1-5] and essential information on their electronic properties can be obtained from these measurements: doping concentration, density of states in band gap, barrier height, etc.

In this chapter we will address basic theory on the depletion capacitance of a *p-n* junction and a simple heterojunction: a Schottky diode. The possibilities of admittance spectroscopy and capacitance-voltage techniques will be recalled.

2.1 Basic concepts of a *p-n* junction

A *p-n* junction is a device formed by a *p*-doped and a *n*-doped regions of the same semiconductor. We assume that the doped regions are uniformly doped and that the transition between the two regions is abrupt as it is shown in Fig.2.1(a). We will refer to this structure as an abrupt *p-n* junction. In *p-n* junctions, which one side is distinctly higher-doped than the other, only the low-doped region needs to be considered, since it determines the device characteristics. Such a structure is referred as one-sided abrupt p^+-*n* (or *p*-n^+) junction.

Since the work function of the *p*-type material is larger than the *n*-type, the electrostatic potentials must be smaller on the *n*-side than the *p*-side, thus an electric field is established at the junction [6]. This difference on the work functions results in a step in the conduction and valence band edges as it can be seen from the band diagram presented in Fig.2.1(c) Carriers diffuse across the junction leaving behind a layer of fixed charge on either side. Equilibrium is established when diffusion of majority carriers across the junction is balanced by the drift of minority carriers back. At this point the Fermi levels of the *p*- and *n*-type layer are equal. The junction region is depleted of both electrons and holes and there is always a barrier to majority carriers and a low resistance path to minority carriers.

Let us assume high quality, crystalline semiconductor layers and that the junction has no interface states. Then this junction consists of three regions: a neutral *p*-type region, a charged

region around the junction – the space charge or depletion region, and a neutral *n*-type region as it is shown in Fig.2.1(a). In order to obtain the width of the depleted region some approximations are made. First, the depletion approximation assumes that the depletion region is precisely defined, ends abruptly, and is fully depleted of free carriers. Within neutral regions, the majority carriers have their equilibrium value and only variations in the minority carrier density determine the current. The second approximation is that the recombination rates in the neutral regions are linear in the minority carrier density. This allows analytic solutions to be found.

We define the *p-n* junction as a layer of *p*-type material with a doping density N_A for $x<0$ which adjoins a *n*-type layer with a doping density N_D for $x>0$, with a perfect interface at $x = 0$. Let us now define the built-in or diffusion potential in equilibrium, V_d, as it is shown in Fig.2.1(b) and 2.1(c).

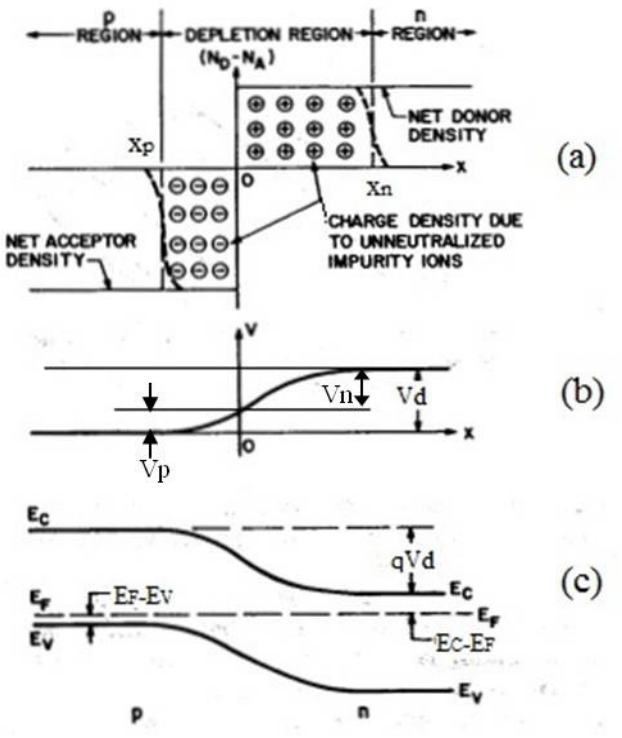

Fig.2.1. Abrupt p-n junction in thermal equilibrium. (a) Space-charge distribution. The dashed lines indicate the majority carrier distribution tails. (b) Potential variation with distance where V_d is the diffusion potential. (c) Energy-band diagram (from [7]).

First, the equations defining the carrier concentrations and the positions of the Fermi level referred to the valence band edge E_V on the *p*-side (δ_p) and to the conduction band edge E_C on the n side (δ_n):

$$n_i^2 = n_0 p_0 = N_C N_V \exp\left(-\frac{E_g}{k_B T}\right) \tag{2.1}$$

$$(E_C - E_F) = \delta_n = k_B T \ln\left(\frac{N_C}{n_0}\right) \tag{2.2}$$

$$(E_F - E_V) = \delta_p = k_B T \ln\left(\frac{N_V}{p_0}\right), \tag{2.3}$$

where n_i is the intrinsic carrier density, E_g is the band gap, N_C and N_V are the effective conduction and valence band densities, respectively, n_0 and p_0 are the equilibrium electron and hole concentrations, respectively. Since $n_0 \sim N_D$ and $p_0 \sim N_A$ we obtain for the diffusion potential:

$$qV_d = E_g - (\delta_n + \delta_p) = kT \ln\left(\frac{N_C N_V}{n_i^2}\right) - \left[k_B T \ln\left(\frac{N_C}{n_0^2}\right) + k_B T \ln\left(\frac{N_V}{p_0^2}\right)\right] \approx k_B T \ln\left(\frac{N_A N_D}{n_i^2}\right), \tag{2.4}$$

The depletion width can be obtained after solving Poisson's equation for both sides of the junctions. Here we present only the well-known expression for the depletion width w for a two-sided abrupt junction [7]:

$$w = x_n + x_p = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)V_d} \tag{2.5}$$

where ε_s is the dielectric permittivity of the semiconductor, x_p and x_n are the depletion widths in p- and n-side respectively. The repartition of V_d between the two layers through V_n and V_p depends on the relative doping density: more of V_d is dropped in the layer which has the lower doping density and the wider depletion width. Then, for a one-sided abrupt junction, Eq.(2.5) reduces to:

$$w = \sqrt{\frac{2\varepsilon_s}{qN_B}V_d} \tag{2.6}$$

where N_B is N_D or N_A (donor or acceptor impurity concentrations) depending on whether $N_A >> N_D$ or vice versa. A more accurate result for the depletion width can be obtained if one considers the majority carrier contribution in addition to the dopants concentration. Eq.(2.6) is then written

$$w = \sqrt{\frac{2\varepsilon_s}{qN_B}(V_d - 2k_BT/q)} = L_D\sqrt{2(\beta V_d - 2)} \tag{2.7}$$

where $\beta=q/k_BT$ and L_D is the Debye length defined by:

$$L_D = \sqrt{\frac{\varepsilon_s k_B T}{q^2 N_B}} \tag{2.8}$$

In Eq. (2.7), the correction factor $2kT/q$ appears because of the two majority-carriers distribution tails.

Let us now consider a *p-n* junction under applied bias. If a forward bias V_a is applied to the *p* side, then the bias across the depletion region is reduced to $V = V_d - V_a$. The depletion width is then reduced in proportion to $(V_d - V_a)^{1/2}$. Similarly, if the junction is reverse biased, the potential drop increases and the depleted layer becomes thicker:

$$w = \sqrt{\frac{2\varepsilon_s}{qN_B}(V_d + V_a - 2k_BT/q)} = L_D\sqrt{2(\beta V_d + \beta V_a - 2)} \tag{2.9}$$

Now we will focus on the definition of the capacitance of a *p-n* junction.

2.2 Two types of capacitance: differential and depletion capacitance

Two types of capacitances are associated with a diode junction. The first one, known as the diffusion capacitance, is proportional to the diode current. Therefore this capacitance is dominant under forward-biased conditions. The second one, known as the depletion capacitance, is a weak function of the applied voltage and is notably dominant under reverse-biased conditions.

2.2.1 Diffusion capacitance

Capacitance is the ability of a body to store an electrical charge. Any object that can be electrically charged exhibits capacitance. A common form of energy storage device is a

parallel-plate capacitor. The basic equation for the capacitance of a parallel-plate capacitor is defined by $C = \varepsilon A/d$, where ε is the permittivity of the dielectric (insulator) between the plates of area A separated by a distance d. The differential capacitance (per unit area) is written as $C = dQ/dV$, where dQ is the charge variation with a voltage variation dV.

In a forward-biased diode, minority carriers are injected into both sides of the junction [8]. These minority carriers diffuse from the junction and recombine with the majority carriers. The electron charge stored in the *p*-region and the hole charge in the *n*-region can be expressed as

$$Q_n = I_n \tau_n, \;\; Q_p = I_p \tau_p \tag{2.10}$$

where I_n and I_p are electron and hole currents at the junction, τ_n and τ_p are the mean minority carrier lifetimes. Assuming $\tau = \tau_n = \tau_p$ and knowing that diode current is $I_d = I_p + I_n$ the total excess minority carrier charge at the junction is $Q_d = I_d\tau$. The origin of the capacitance lies in the injected charge stored near the junction outside the transition region. It is convenient to introduce an incremental capacitance, defined as the rate of change of injected charge with voltage, called diffusion, or storage, capacitance. Supposing that τ does not depend on the potential, the diffusion capacitance can then be written as [8]:

$$C_{dif} = \frac{dQ}{dV} = \frac{\tau dI_d}{dV} = \tau \frac{d}{dV}\left[I_0 \exp\left(\frac{V}{\eta V_T} \right) \right] = \frac{\tau I}{\eta V_T} \tag{2.11}$$

where V_T is thermal potential that equals kT/q, η is the ideality factor and is a function of current with a value between 1.0 and 2.0.

As one can see, the diffusion capacitance C_{dif} is proportional to the mean carrier lifetime τ and to the diode biasing current I. The diffusion capacitances may reach very large values as it can be seen in Fig.2.2, where depletion and diffusion capacitance are presented as a function of the applied voltage.

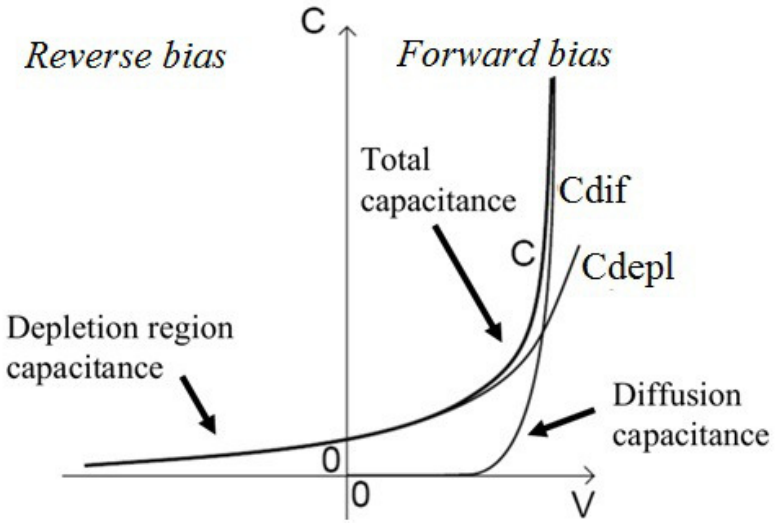

Fig.2.2. Depletion (C_{depl}), diffusion (C_{dif}) and total capacitance as a function of applied voltage.

2.2.2 Depletion Capacitance

As it was recalled in the beginning of this chapter, in a *p-n* junction there exists a space-charge region that stores a charge $Q = q \cdot (N_D - N_A) \cdot w$. The variation of the applied voltage modulates the space charge width w. As a result, the charge Q in the space charge region changes with respect to the applied voltage as it is shown in Fig.2.3.

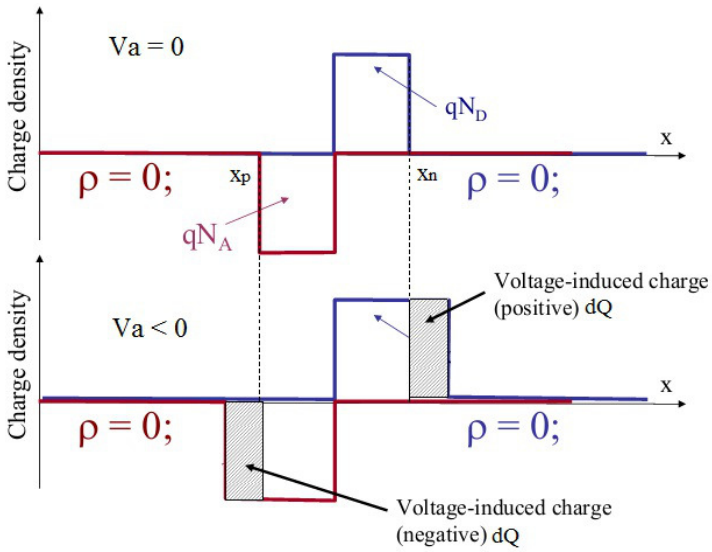

Fig.2.3. Charge density of a p-n junction at equilibrium and under an applied reverse bias V_a.

Then the depletion-layer capacitance per unit area A is defined as [7]

$$\frac{C}{A} = \frac{dQ}{dV} \tag{2.12}$$

where dQ is the incremental increase in charge per unit area upon an incremental change of the applied voltage dV.

For one-sided abrupt junctions, the capacitance per unit area A is given by:

$$\frac{C}{A} = \frac{dQ}{dV} = \frac{d(qN_B w)}{d\left[\left(\frac{qN_B}{2\varepsilon_s}\right)w^2\right]} = \frac{\varepsilon_s}{w} \tag{2.13}$$

One can see that Eq.(2.13) is the same as for a plain capacitor with the distance w between the plates. Using Eq.(2.7) the capacitance is rewritten as:

$$\frac{C}{A} = \frac{\varepsilon_s}{\sqrt{2}L_D}\left(\beta V_d \pm \beta V_a - 2\right)^{-1/2} \tag{2.14}$$

The ± sign is for the reverse- and forward-bias conditions, respectively. One should also note that Eqs.(2.13)-(2.14) are obtained considering that the doping concentrations N_D and N_A (indicated as N_B) are constant and do not vary with the distance.

2.3 Capacitance –voltage technique

We will present here the capacitance-voltage technique and discuss on its possibilities to characterize semiconductors' Schottky diodes and *p-n* junctions.

2.3.1 Doping concentration

The capacitance-voltage (*C-V*) technique relies on the fact that the width of a reverse-biased space-charge region of a semiconductor junction device depends on the applied voltage.

The *C–V* profiling method has been used with Schottky barrier diodes using deposited

metal, mercury, and liquid electrolyte contacts, *p-n* junctions, MOS capacitors, MOSFETs, and metal-air-semiconductor structures [9,10].

Above we provided essential theory on a *p-n* junction. Here let us consider a metal-*p*-type semiconductor junction. By joining a *p*-type semiconductor with a work function Φ_p to a metal of smaller work function $\Phi_p > \Phi_m$, an electric field in a layer close to the interface is established. This situation resembles a *p-n* junction where a *n*-type semiconductor is substituted by a metal. The established field will drive holes into the bulk of the semiconductor and electrons to the interface, thus effecting charge separation. The metal-semiconductor contact presents a lower resistance path for electrons and a barrier for holes. This type of junction is known as a Schottky barrier. The band diagram of a Schottky barrier of a semi-infinite semiconductor of *p*-type is presented in Fig.2.4. The space charge region exists as well in a Schottky barrier with the width *w* defined by Eq.(2.6) with the value of acceptor concentration N_A in the denominator:

$$w = \sqrt{\frac{2\varepsilon_s}{qN_A} V_d} \tag{2.15}$$

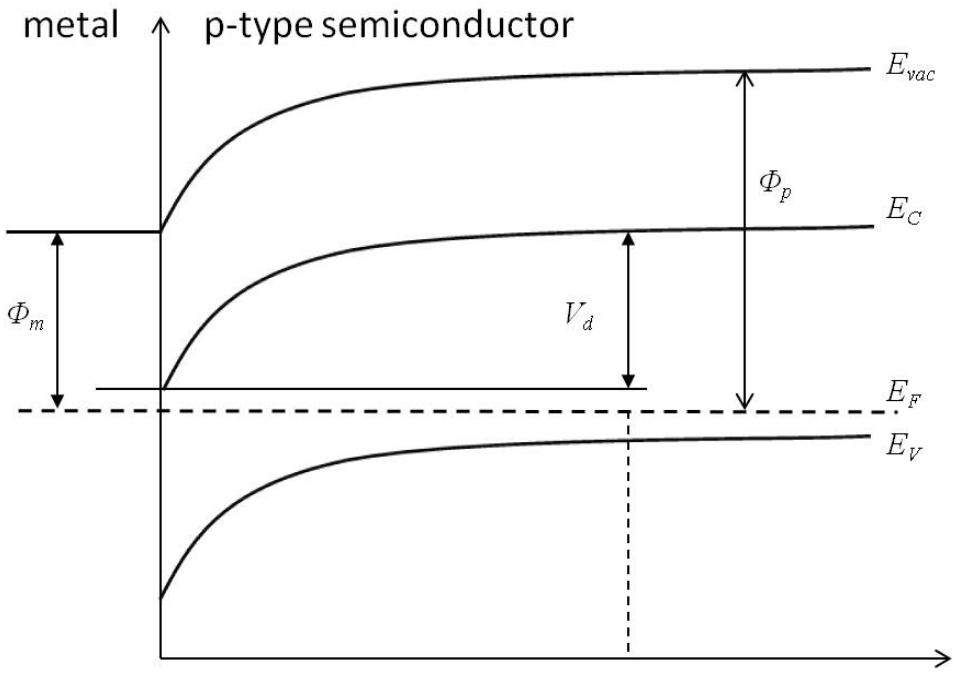

Fig.2.4. Band diagram of the metal - p-type semiconductor junction at equilibrium. Semiconductor and metal work functions, Φ_p and Φ_m, the diffusion potential, V_d, are indicated.

As for the case of a *p-n* junction the differential or small signal capacitance is defined by

$$\frac{C}{A} = \frac{dQ_m}{dV} = -\frac{dQ_s}{dV} \tag{2.16}$$

where Q_m and Q_s are the metal and semiconductor charges. The negative sign accounts for *negative* voltage in the semiconductor space charge region (negatively charged ionized donors) for *positive* charge on the metal (reverse bias) . The capacitance is determined by superimposing a small-amplitude ac voltage v on the dc voltage V. The ac voltage frequency is typically 10 kHz to 1 MHz with 10 to 20 mV amplitude, but other frequencies and other voltages can be used [11].

The ac voltage increasing from zero to a small negative voltage adds a charge increment dQ_m to the metal contact. The charge increment dQ_m must be balanced by an equal semiconductor charge increment dQ_s for overall charge neutrality. The semiconductor charge is given by:

$$Q_s = qA\int_0^{\infty}(p - n - N_A)dx \approx -qA\int_0^{w} N_A dx \tag{2.17}$$

where p and n are hole and electron density, respectively. Within the depletion approximation we suppose $p \approx n \approx 0$ in the depletion region. Another assumption is that all acceptors are ionized.

The charge increment dQ_s appears due to a slight increase in the space charge region width.

$$\frac{C}{A} = -\frac{dQ_s}{dV} = q\frac{d\int_0^{w} N_A dx}{dV} = qN_A\frac{dw}{dV} \tag{2.18}$$

The term dN_A/dV was neglected, assuming N_A does not depend on voltage.

The capacitance of a reverse-biased junction, when considered as a parallel plate capacitor, is given in Eq.(2.13). Differentiating Eq. (2.13) with respect to voltage and substituting dw/dV into Eq.(2.18), we obtain:

$$N_A = -\frac{C^3}{q\varepsilon_s A^2 \frac{dC}{dV}} = \frac{2}{q\varepsilon_s A^2 \frac{d\left(1/C^2\right)}{dV}} \tag{2.19}$$

Note that the area A of the device must be known precisely since it appears as A^2 in Eq. (2.19).

The doping density thus can be obtained from the slope dC/dV of a C–V curve or from the slope $d(1/C^2)/dV$ of a $1/C^2$ –V curve. For a Schottky barrier diode there is no ambiguity in the depletion width since it only spreads into the substrate. Space-charge region spreading into the metal is totally negligible. Equations (2.17), (2.18) and (2.19) can also be used in the case of a one-sided p-n junction, *i.e.*, p^+-n or n^+-p junctions. If the doping density of the heavily doped side is 100 or more times higher than that of the lowly doped side, then the space charge region spreading into the heavily doped region can be neglected. If that condition is not met, the equations must be modified [12]. The corrections, though, are difficult to obtain. It has been proposed that no unique doping density profile can be derived from C–V measurements under those conditions [13]. If the doping density profile of one side of the junction is known, then the profile on the other side can be derived from the measurements [14].

For the derivation of Eq. (2.13) we used the depletion approximation, which neglects minority carriers and assumes total depletion of majority carriers in the space-charge region to a depth w and perfect charge neutrality beyond w. This is a reasonably good approximation when the space charge region is reverse biased and when the substrate is uniformly doped. Furthermore, we used the acceptor ion density at the edge of the space-charge region as the incremental charge variation. The ac probe voltage exposes more or less ionized acceptors at the space-charge region edge. But the charges that actually move in response to the ac voltage are the mobile holes, not the acceptor ions. Hence, the differential capacitance-voltage profiling technique determines rather the carrier density, not the doping density. What is actually measured is an apparent or effective carrier density, which is neither the true carrier density nor the doping density. In many cases the apparent doping density is approximately the majority carrier density. Then, Eq. (2.19) (holes are majority carriers) becomes:

$$p(w) = -\frac{C^3}{q\varepsilon_s A^2 \frac{dC}{dV}} = \frac{2}{q\varepsilon_s A^2 \frac{d\left(1/C^2\right)}{dV}} \tag{2.20}$$

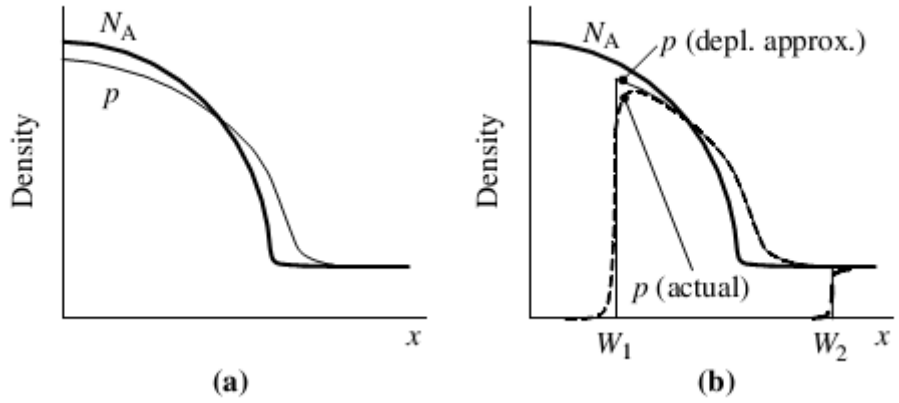

Fig.2.5. Schematic representation of the doping and majority carrier density profiles of a non-uniformly doped layer. (a) zero-biased junction, (b) reverse-biased junction showing the doping density profile, the majority carrier profiles in the depletion approximation and the actual majority carrier profiles for two reverse-bias voltages (from [11]).

The use of the majority carrier density rather than the doping density in the profile equations is an important point and has been the subject of many discussions [15-20]. The concept of a non-uniform acceptor doping density profile was demonstrated in Ref. [11]. The acceptor doping density is shown by the thick curve in Fig.2.5(a). The majority hole density profile shown by the light line differs from the doping density profile even in thermal equilibrium. Some of the holes diffuse from the highly doped region to the lowly doped region and an equilibrium profile is established as a result of both diffusion and drift. The steeper the doping gradient is, the more p and N_A differ from one another.

The majority carrier density deviation from the doping density is governed by the intrinsic Debye length L_D, which was already introduced above and, in more general case, is written as follows

$$L_D = \sqrt{\frac{k_B T \varepsilon_s}{2q^2 n_i}} \tag{2.21}$$

L_D is a measure of the distance over which a charge imbalance is neutralized by majority carriers under steady-state or equilibrium conditions.

When a space-charge region is formed in a reverse biased Schottky diode, the carrier distribution becomes that in Fig.2.5(b). We show the majority carrier distribution expected from the depletion approximation for depletion widths *w1* and *w2*, corresponding to two different reverse-bias voltages. The actual majority carrier distribution is also shown. The two differ considerably and it is seen from these curves that the doping density profile is not what

is measured by differential capacitance profiling. It is also not evident that it is the majority carrier distribution that is measured. It has been shown by detailed computer calculations that what is actually measured is an effective or apparent majority carrier density profile that is closer to the true majority carrier density profile than to the doping density profile [21]. The doping density profile, the majority carrier density profile, and the effective majority carrier density profile are identical for uniformly doped substrates, but not for non-uniformly doped substrates due to the built-in electric field that induces the diffusion of majority carriers to the region of the lower dopant concentration.

The Debye length sets a limit to the spatial resolution of the measured profile. This Debye length problem arises because the capacitance is determined by the movement of majority carriers and the majority carrier distribution cannot follow abrupt spatial changes in doping density profiles. Detailed calculations show that if a doping density step occurs within one Debye length, the majority carrier and the apparent densities agree rather well with one another, but both differ appreciably from the true doping density profile [21]. For a more gradual transition, the majority carrier density agrees quite well with the apparent densities. Moreover, the agreement of the latter with the doping density profile is also quite reasonable.

2.3.2 Barrier height

Let us now address the question of obtaining the barrier height value from *C-V* measurements. The band diagram of a Schottky barrier diode on an *p*-type substrate is recalled in Fig.2.6. The barrier height of ϕ_{B0} is shown in Fig.2.6 as well.

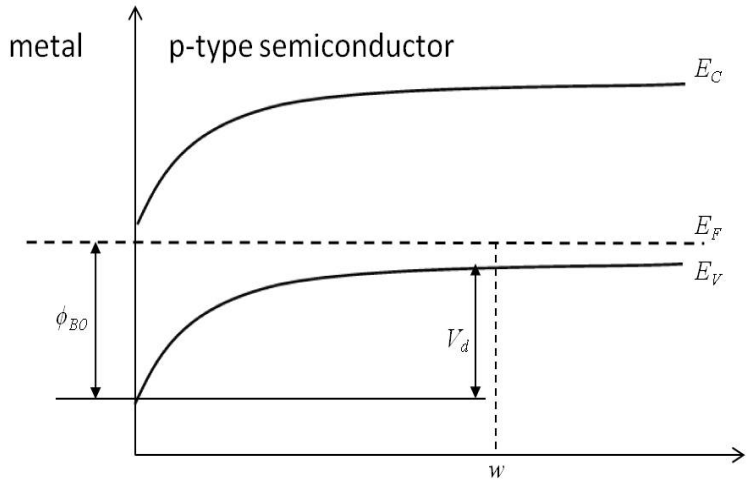

Fig.2.6. Band diagram of a Schottky barrier diode on a p-type substrate at equilibrium with indicated diffusion potential V_d and the barrier height ϕ_{B0}.

The capacitance per unit area of a Schottky diode shown in Fig.2.6 and under reverse-bias conditions is given by Eq.(2.14). Replacing L_D by its expression given in Eq. (2.8), we can write:

$$\frac{C}{A} = \frac{\varepsilon_s}{\sqrt{2}L_D}\left(\beta V_{bi} + \beta V_a - 2\right)^{-1/2} = \sqrt{\frac{q\varepsilon_s N_A \beta}{2(\beta V_d + \beta V_a - 2)}} \tag{2.22}$$

where $\beta = q/k_B T$, V_a is the applied reverse-bias voltage. The diffusion potential is related to the barrier height by:

$$\phi_{B0} = V_d + (E_F - E_V)^{bulk} \tag{2.23}$$

as seen in Fig.2.6. The position of the Fermi level in the bulk of the semiconductor is defined as $(E_F\text{-}E_V)^{bulk} = (k_B T/q)\cdot\ln(N_V/N_A)$, where N_V is the effective density of states in the valence band. Plotting $1/(C/A)^2$ versus V_a gives a curve with the slope $2/[q\varepsilon_s N_A]$, which intercepts the V_a - axis at $V_{int} = -V_d + k_B T/q$.

The barrier height is determined from the intercept voltage by

$$\phi_{B0} = -V_{\text{int}} + (E_F - E_V)^{bulk} + {k_B T}/{q} \tag{2.24}$$

A typical $(C/A)^{-2}$ versus V_a plot of a diode is shown in Fig.2.7. From the slope $2/[q\varepsilon_s N_A]$ we find a doping concentration $N_A = 2\cdot 10^{16}$ cm^{-3} and the barrier height $\phi_{B0} = 0.74$ V can be obtained from Eq. (2.24).

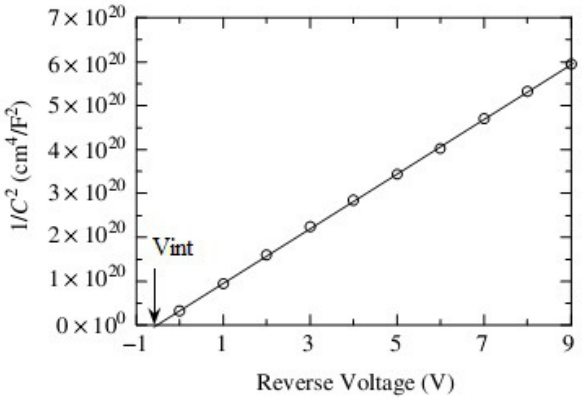

Fig.2.7. Plot $1/C^2$ vs applied reverse voltage of a Schottky diode on an n-type semiconductor.

2.4 DOS in the band gap from capacitance measurements

Capacitance or, more generally, admittance measurements are particularly suited for probing bulk and interface properties of a junction diode-like device. The small signal capacitance is sensitive to carrier capture and emission from trap states, related to the charge response δQ to a small change of voltage δV. A number of experimental techniques have been developed to exploit this sensitivity and try to map out the sub-bandgap density of states. The most broadly applied ones are capacitance–voltage (*C-V*) profiling, admittance spectroscopy [22-26], and deep level transient spectroscopy (DLTS) [27]. These techniques are widely used for the characterization of Schottky barriers, *p-n* junctions, metal-insulator-semiconductor (MIS) structures and devices based on these structures.

The electronic states associated with defects and impurities are typically divided into two broad categories: "shallow" and "deep" states, corresponding, respectively, to centers with extended electronic wavefunctions, and those that are strongly localized [28]. The techniques discussed here are designed to detect nonradiative transitions involving deep states. Deep states act as traps and recombination centers, reducing the minority carrier mobility, and in some cases pinning the Fermi energy deep in the gap. The electrical activity and even the physical nature of deep states can be complex.

Much effort has been done to extend junction capacitance techniques to accurately measure properties of sub-bandgap states density, characteristic of imperfect materials. This includes early work by Losee [29] to treat generally the effect of gap states on admittance in Schottky devices as well as experimental and numerical studies by Cohen and Lang [27, 30] to treat the case of continuous densities of states.

In this section we will enlighten the influence of the defects on the *C-V* measurements. Then a brief description of the principles of capacitance spectroscopy and DLTS technique will be presented. Capacitance spectroscopy measurements performed on a-Si:H Schottky diodes will be described in details in Chapter 3.

2.4.1 The influence of deep defects on *C-V* profiles

Admittance or capacitance measurements generally begin with a simple *C-V* evaluation of the diode, including whether significant shunt current exists, whether the layer is fully depleted, and a rough estimate of doping density.

The diode capacitance is traditionally analyzed using the depletion approximation. Although this approximation may not be very accurate for thin-film semiconductors, which can have significant densities of deep states, it is still a useful starting point for the discussion of admittance measurements. As it was discussed in the previous section, *C-V* measurements can give a one-dimensional profile of the doping density, with a spatial resolution characterized by the Debye screening length L_D. However, the relatively large density of deep

states in thin-film semiconductors can make it impossible to find the free carrier density using *C-V* measurements.

The deep states may adjust their charge state to the dc bias conditions, which results in artifacts such as curvatures of plotted data in the *C-V* profiles that no longer obey Eq. (2.14). The relative contributions of the different states to the space charge change with applied voltage have the result that the $1/C^2$ slope is dominated by the shallow states at low applied bias *V* with the deep states contributing increasingly at high *V*.

The deep-level effect on *C-V* relationship has been examined by many authors [30-32]. Sah and Reddi investigated the effect of deep gold acceptors on both the high and low frequency reverse bias C-*V* relationships in silicon p^+-*n* step junctions. Their model applies equally well to a Schottky barrier. Roberts and Crowell derived an expression for the low-frequency Schottky barrier *C-V* relationship for a distribution of spatially uniform donor and acceptor impurity levels. With knowledge of the impurity distribution they showed how the intercept on the voltage axis of the low frequency $1/C^2$ versus *V* relationship may be interpreted to give the true value of the diffusion potential. In addition authors showed how the low and intermediate frequency capacitances may be used in an appropriate bias range to find both the energy levels and trapping times of the predominant deep levels. When one or more deep level impurities are present in concentrations near that of the shallow impurities it was indicated that the impurity profile deduced from the usual *C-V* relationship can be seriously in error, even at modulation frequencies such that the deep levels cannot respond.

Significant research has been devoted to the study of frequency dependencies of *C-V* data. Balberg [33] developed a way of interpreting frequency dependent *C-V* characteristics by obtaining analytic-explicit expressions for the dependence of the capacitance on bias, frequency and temperature. This dependence indicates how to derive the state distribution from experimental *C-V* measurements under deep depletion conditions, which seem to be the only ones for which a unique interpretation is possible. The deep depletion regime is reached when quasi-intrinsic level of the semiconductor E_i crosses E_F at the interface.

2.4.2 Admittance spectroscopy

As it was discussed above the diode capacitance is traditionally analyzed using the depletion approximation.

However, when energy levels are present deeper in the band gap, then the depletion approximation no longer necessarily holds true, and carrier capture and emission from these states must also be considered.

Admittance spectroscopy has several advantages for the probing of defect levels:

relatively shallow and fast levels are seen, quasi-equilibrium conditions are maintained, the technique is spectroscopic, there is a peak observed for each energy level, the peak height is related to the number of centers (weighted according to level depth). It was shown by Losee [29] that measurements of the capacitance (C) and conductance (G) components of the junction admittance at two (or more) frequencies as a function of temperature provide a spectroscopy of defect levels (principally majority-carrier traps) yielding energies, types, concentrations, and majority-carrier capture coefficients.

The differential capacitance of the sample originates from its response to a small voltage perturbation, δV. In the small signal approximation the condition $\delta V < kT/q$ should be met. Typical values of applied ac-voltage V_{ac}, around 30 mV, do not strictly satisfy this requirement, which may slightly impact the data [34,35]. The resulting change in the band bending causes a change in trap state occupation at the location x_ω, where a trap level E_t crosses the Fermi level E_F at an angular frequency ω, as illustrated in Fig.2.8. Thus, traps contribute to the capacitance in two ways: (i) traps modify the space charge density and therefore the depletion width w, and (ii) in the vicinity of x_ω, the traps may be able to change their charge state dynamically, following the ac voltage, and contributing to $\delta Q/\delta V$.

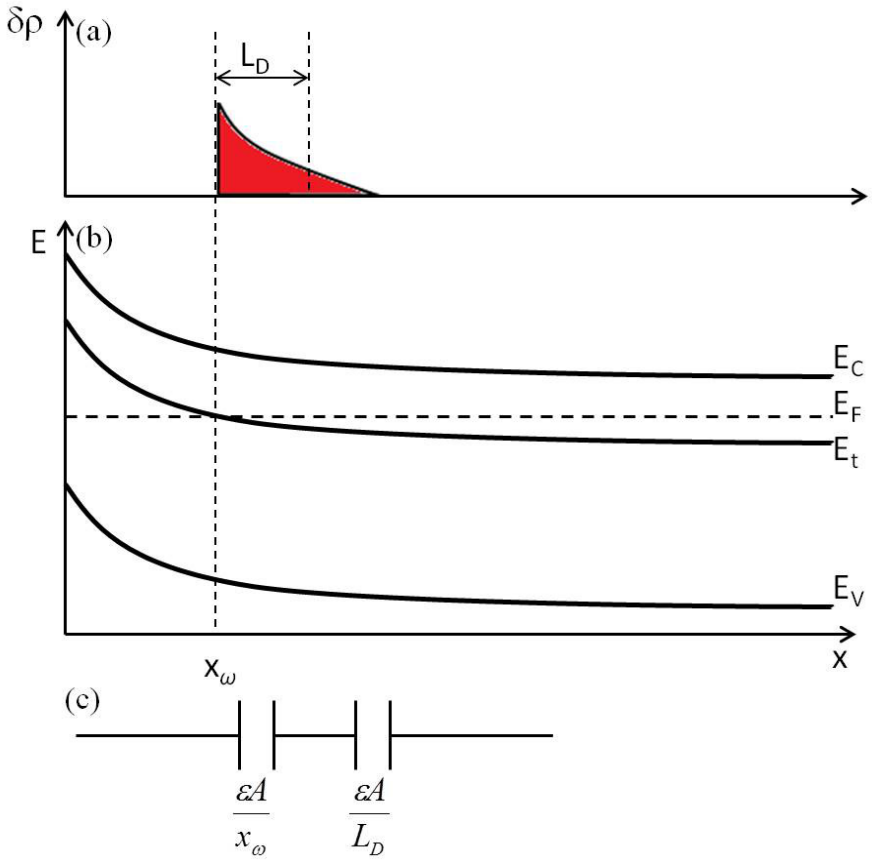

Fig.2.8. (a) ac space charge density, δρ, (b) energy band diagram of a n-type Schottky barrier showing the space charge contribution under reverse bias, (c) the equivalent capacitance derived from the sharp cut-off model.

In Chapter 3 the total capacitance will be derived explicitly. Here we provide the resulting formula:

$$\frac{C}{A} = \frac{\varepsilon}{x_\omega + L_D^{a-Si:H}}, \tag{2.25}$$

where $L_D^{a\text{-}Si:H}$ is the Debye length in a-Si:H that characterizes the density of states (DOS) at the Fermi level in the band gap $N(E_F)$ and namely can be written as:

$$L_D == \sqrt{\frac{\varepsilon}{q^2 N(E_F)}} \tag{2.26}$$

Measurement of the sample admittance as a function of applied ac frequency and temperature is named admittance spectroscopy (AS). This technique can yield the thickness of the film, the position of the Fermi energy in the bulk, the energetic position of dominant defect bands that occur between the Fermi energy and mid-gap, and an estimation of the density of those states. In contrast to both the DLTS and *C-V* techniques, in AS a ramp of frequency (or temperature) is applied to cross the transition frequency where the traps start to respond.

When the temperature is too low, or the frequency is too high, then there is no time for states to respond to the applied ac voltage, and a condition called freeze-out occurs. Under these conditions, the capacitance response will be that of the dielectric layer, $C = \varepsilon A/d$, where d is the distance between the top and back contacts. Increasing the temperature, T, or decreasing the frequency, f, eventually leads to a step in a *C-T* curve. Steps in C correspond to peaks in conductance G/ω, due to their causal relationship.

As T is increasing or f decreasing, trap states start to respond. The turn-on temperature T_0 determines the turn-on temperature for trap response at a certain frequency. When $T = T_0$, the occupation of the state can follow the ac voltage, and its charge state will change at the location x_ω. This causes x_ω to move closer to the interface and C to increase as shown in Fig.2.9(a). Consequently the deeper a trap state lies the higher T_0 is. In the same way, when measuring the capacitance at a given temperature T and changing ω from high to low values there will be a turn-on frequency ω_0. Both ω_0 and turn-on temperature T_0 are linked via

$$2\nu_n \exp\left(-\frac{E_a}{k_B T_0}\right) = \omega_0 \tag{2.27}$$

The term ν_n is the attempt-to-escape frequency defined by:

$$\nu_n = \sigma_n v_{th} N_C, \tag{2.28}$$

where σ_n is the electron capture cross section, v_{th} is the thermal velocity of free electrons and N_C is the effective DOS in the conduction band.

While the G/ω peaks can be a good way to observe the position of the capacitance step, they can be masked by the leakage conductance in some samples. Similar peaks can also be obtained from the derivative of capacitance with respect to frequency (or temperature) as illustrated in Fig.2.9(b).

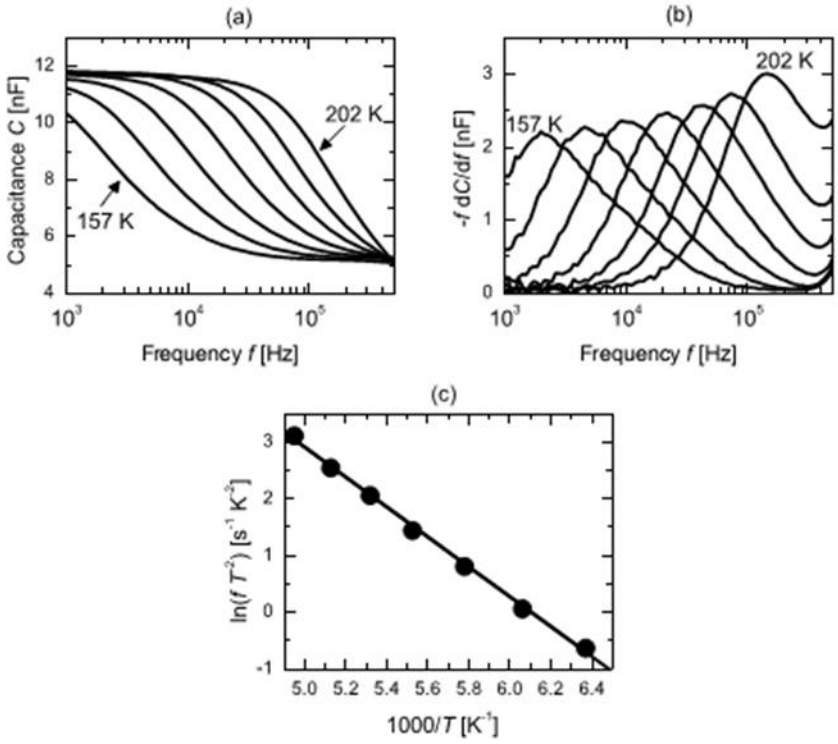

Fig.2.9. (a) Admittance spectroscopy (AS) raw data for a CIGS device. (b) The AS data showing the characteristic peak frequencies at each temperature. (c) Arrhenius plot of each peak (from [36]).

The (ω_0, T_0) data points from each capacitance step can then be plotted on an Arrhenius plot; typically $\ln(\omega/T^2)$ is plotted as a function of $1000/T_0$ as shown in Fig.2.9(c). From Eq. (2.27) the slope yields the activation energy E_a that is considered to be equal to the position of the Fermi level referred to the corresponding band edge, while the intercept gives the attempt-to-escape frequency.

Many authors addressed the possibility of the deriving information on the DOS from the admittance measurements. The pioneer was Losee who showed how to obtain the trap energy level and capture cross-section of a defect state from the plot $\omega T_p^{-3/2}$ vs $1/T_p$ where T_p corresponds to the peak in conductance. Viktorovitch and Moddel [26] focused on the analysis of the frequency dependence of both the conductance and the capacitance of Schottky devices at $V=0$ in order to deduce the depletion width and the DOS in the region of the Fermi level. Archibald and Abram [37] presented calculations to describe the electrical behavior of a-Si:H Schottky barrier in an admittance experiment as well as two simple procedures to find the distribution of gap states. Archibald and Abram introduced previously omitted cases of large reverse bias where minority carrier effects become important and heavily doped regions where there is non-negligible free-carrier charge.

Several simplified approaches have been developed in order to obtain the DOS in the band gap from *C-T* measurements [30,38]. In the next chapter we will particularly focus on the treatment of the capacitance data suggested by Cohen and Lang in 1982 [30].

2.4.3 Transient measurements

The early capacitance vs time (*C-t*) and current vs time (*I-t*) measurements and methods were developed by Sah and his students [39,40]. The initial implementation was time-consuming and tedious because the measurements were single-shot measurements. The power of emission and capture transient analysis was only fully realized when automated data acquisition techniques were adopted. The first of these was Lang's dual-gated integrator or double boxcar approach named deep-level transient spectroscopy (DLTS) [27].

DLTS distinguishes between deep and shallow states by the time-dependent release of the electrons. A forward bias is applied to the Schottky barrier to collapse the depletion region and fill all the traps. When a reverse bias is subsequently applied, the depletion layer is initially wide, but its thickness decreases with time to its steady state value as carriers are released from traps. The change in the depletion layer at a given time *t* reflects the number of traps of binding energy $kTln(\omega_0 t)$ within the depletion region. The density of states is therefore derived from the transient capacitance. The calculation of *N(E)* from the data is straightforward, as it must account for the distribution of states and the voltage dependence of the space charge layer [27]. Deep states are detected only down to the middle of the gap, because deeper states are filled by electrons from the valence band faster than they are excited to the conduction band.

DLTS experiments are performed by measuring either the temperature dependence of the capacitance at a fixed time after the application of the reverse bias or the time dependence at a constant temperature [41].

In the measurement process the steady-state diode reverse bias is disturbed by a voltage pulse. This voltage pulse reduces the electric field in the space charge region and allows free carriers from the semiconductor bulk to penetrate this region and recharge the defects causing their non-equilibrium charge state. After the pulse, when the voltage returns to its steady-state value, the defects start to emit trapped carriers due to the thermal emission process. The variation of the device space charge region capacitance in time is described bythe capacitance transient *C-t*. When observing a repetitive transient through varying the sample temperature, a peak appears in the capacitance versus temperature plot. Such a plot is a DLTS spectrum (see Fig.2.10).

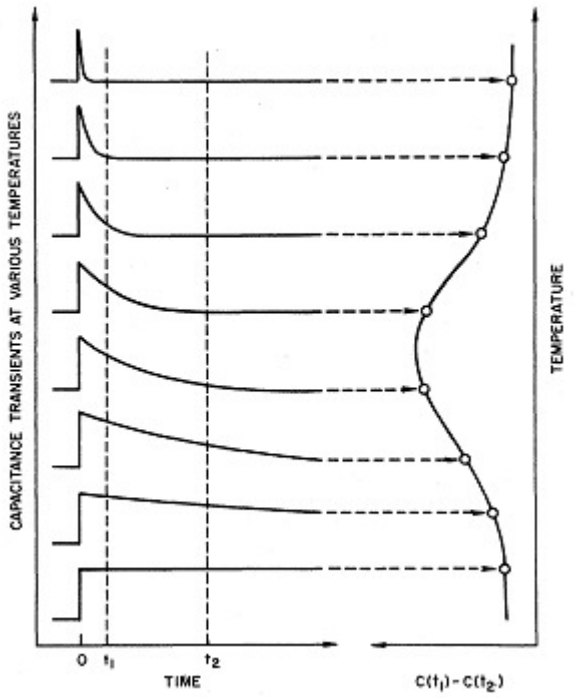

Fig.2.10. Basic principle of the DLTS technique for emission from a discrete trap level. DLTS spectrum, i.e. capacitance difference $C(t_1)$-$C(t_2)$ versus temperature plot, is presented on the right (from [27]).

Suppose that the *C-t* waveforms in Fig.2.10 are sampled at times $t = t_1$ and $t = t_2$ and that the capacitance at t_2 is subtracted from the capacitance at t_1, $\Delta C=C(t_1)-C(t_2)$. Such a difference signal is a standard output feature of a double boxcar instrument. The temperature is slowly scanned while the device is repetitively pulsed between zero and reverse bias. There is no difference between the capacitance at the two sampling times for very slow or for very fast transients, corresponding to low and high temperatures. A difference signal is generated when the time constant is of the order of the gate separation t_2-t_1, and the capacitance difference passes through a maximum as a function of temperature, as shown in Fig.2.10. This is the DLTS peak. ΔC exhibits a maximum ΔC_{max} at temperature T_1. The time constant τ_{max} corresponding to the maximum of DLTS signal is given by:

$$\tau_{\max} = \frac{t_2 - t_1}{\ln\left(\frac{t_2}{t_1}\right)} \tag{2.29}$$

The energy scale of a DLTS spectrum is related to the thermal activation energy of the detrapping process. The electron thermal-emission rate e_n for a particular trap level with the energy E_t from the conduction band edge is defined by

$$e_n = v_n \exp\left(-\frac{E_C - E_t}{k_B T}\right) \tag{2.30}$$

where v_n is the attempt-to-escape frequency. In the small signal limit, the time constant of the

exponential capacitance transient due to this trap is inverse to the thermal-emission rate e_n.

The concentrations of the different deep levels in the case of discrete defect levels are in nearly all cases directly related to the respective magnitudes of the peaks in the DLTS spectrum. In the small-signal $(\Delta C/C<<1)$ large bias $(V_A>>E_g/q)$ limit, the relationship between the magnitude of the capacitance transient ΔC associated with a trap of concentration N_t is

$$\frac{\Delta C}{C} \cong 2\frac{N_t}{N_s} \tag{2.31}$$

where C is the overall capacitance of the depletion layer and N_s is the net shallow-level traps concentration.

From raw DLTS data only general characteristic of the density of state distribution *N(E)* is obtained. Authors provided for a detailed procedure of obtaining the DOS profile from DLTS measurements. It is a fitting procedure of the initial *N(E)* taken from DLTS spectrum by numerical methods [30]. The first approximate *N(E)* is used as the trial function for numerical DLTS simulation program. Then the shape, magnitude and the band gap of *N(E)* are adjusted so that numerically calculate DLTS spectra agree with the experimental one.

2.5 Conclusions

In this chapter we recalled the basic theory on *p-n* junctions and Schottky barriers. The depletion approximation that plays a very important role in the description of a junction was presented.

The two types of capacitance were introduced. Our attention is focused on the depletion capacitance since it allows one to derive essential information on a studied junction. The *C-V* technique is widely used to obtain the doping density and the barrier height of a junction. However, it was shown that there exists a lot of discussion on the accuracy of the derivation of these parameters. For the case of the non-uniformly doped samples the *C-V* technique provides rather for a majority carrier density than the doping density. It is worth emphasizing that the derivation of the parameters from *C-V* measurements is based on the depletion approximation that is not valid in certain cases, as we will discuss in Chapter 4.

The admittance spectroscopy and DLTS measurements were described considering their application for extracting the density of states in the band gap of a semiconductor. In Chapter 3 and Chapter 4 the capacitance spectroscopy of a Schottky diode formed on a-Si:H and a a-Si:H/c-Si heterojunction will be thoroughly discussed.

2.6 References

[1] H. Okushi, Y. Tokumaru, S. Yamasaki, H. Oheda, T. Tanaka, *Japanese Journal of Applied Physics*, vol. 20, p. L549, 1981.

[2] H. Okushi, *Philosophical Magazine B*, vol. 52, p. 33, 1985.

[3] A. V. Gelatos, J. D. Cohen, *Applied Physic Letters*, vol. 47, p. 412, 1985.

[4] J. P. Kleider, D. Mencaraglia, Z. Djebbour, *Journal of Non-Crystalline Solids*, vol. 114, p. 432, 1989.

[5] J. Reynaud, J. P. Kleider, D. Mencaraglia, *Journal of Non-Crystalline Solids*, vol. 187, p. 313, 1995.

[6] Jenny Nelson, "*Physics of Solar Cells*", Imperial College Press, London, 2003.

[7] S. M. Sze, "*Physics of semiconductor devices*", 2nd edn. John Wiley & Sons, New York, 1981.

[8] B. M. Wilamowski, "Semiconductor Diode". In: *Industrial Electronics Handbook, vol. 1 – Fundamentals of Industrial Electronics,* 2nd Edition, pp. 8-1 to 8-15, CRC Press, 2011.

[9] J. Hilibrand and R.D. Gold, "Determination of the Impurity Distribution in Junction Diodes From Capacitance-Voltage Measurements", *RCA Review*, vol. 21, p. 245, 1960.

[10] E. H. Nicollian and J. R. Brews, "*MOS (Metal Oxide Semiconductor) Physics and Technology*", Wiley, 1982.

[11] R. Schroder, "*Semiconductor material and device characterization*", Wiley-Interscience, 2006

[12] R. Decker, "Measurement of Epitaxial Doping Density vs. Depth," *Journal of Electrochemical Society*, vol. 115, p. 1085, 1968.

[13] L. E. Coerver, "Note on the Interpretation of *C–V* Data in Semiconductor Junctions", *IEEE Transactions on Electron Devices*, vol. 17, p. 436, 1970.

[14] H. J. J. DeMan, "On the Calculation of Doping Profiles from C(V) Measurements on Two-Sided Junctions," *IEEE Transactions on Electron Devices*, vol. 17, p. 1087, 1970.

[15] D.P. Kennedy and R.R. O'Brien, "On the Measurement of Impurity Atom Distributions by the Differential Capacitance Technique," *IBM Journal of Research and Development*, vol. 13, p. 212, 1969.

[16] M. Nishida, "Depletion Approximation Analysis of the Differential Capacitance-Voltage Characteristics of an MOS Structure with Nonuniformly Doped Semiconductors", *IEEE Transactions on Electron Devices,* vol. 26, p. 1081, 1979.

[17] D.J. Bartelink, "Limits of Applicability of the Depletion Approximation and Its Recent Augmentation," *Applied Physic Letters,* vol. 38, p. 461, 1981.

[18] H. Kroemer and W.Y. Chien, "On the Theory of Debye Averaging in the *C–V* Profiling of Semiconductors", *Solid-State Electronics*, vol. 24, p. 655, 1981.

[19] C.P. Wu, E.C. Douglas and C.W. Mueller, "Limitations of the CV Technique for Ion-Implanted Profiles", *IEEE Transactions on Electron Devices,* vol. 22, p. 319, 1975.

[20] J. Voves, V. Rybka and V. Trestikova, "C–V Technique on Schottky Contacts — Limitation of Implanted Profiles," *Applied Physics*, vol. A37, p. 225, 1985.

[21] W.C. Johnson and P.T. Panousis, "The Influence of Debye Length on the *C–V* Measurement of Doping Profiles", *IEEE Transactions on Electron Devices,* vol. 18, p. 965, 1971.

[22] J. Beichler, W. Fuhs, H. MeIl, H.W. Welsch, *Journal of Non-Crystalline Solids*, vol. 35-36, p. 587, 1980.

[23] P. Viktorovitch, "Bulk and surface states analysis in a-Si:H by Schottky and MIS tunnel diodes capacitance and conductance measurements", *Journal of Applied Physics*, vol. 52, p.1392, 1981.

[24] A.L. Jung, J.S. Luo, X. Yao, Ch. Lin, Y. W. Yang, D. Adler, *Journal of Non-Crystalline Solids,* vol.57, p. 241, 1983.

[25] T. Tiedje, C. R. Wronski, J. M. Cebulka, *Journal of Non-Crystalline Solids,* vol. 35-36, p. 743, 1980.

[26] P. Viktorovitch, G. Moddel, "Interpretation of the conductance and capacitance frequency dependence of hydrogenated amorphous silicon Schottky barrier diodes", *Journal of Applied Physics,* vol. 51, p. 4847, 1980.

[27] D.V. Lang, J.D. Cohen, JP. Harbison, "Measurement of the density of gap states in hydrogenated amorphous silicon by space charge spectroscopy", *Physical Review B,* vol. 25, p. 5285, 1982.

[28] H. Feichtinger, "Deep centers in semiconductors". In: W. Schroter (ed.), *Electronic Structure and Properties of Semiconductors*, VCH Publishers, New York, pp. 143–195, 1991

[29] D. L. Losee, "Admittance Spectroscopy of Impurity Levels in Schottky Barriers", *Journal of Applied Physics,* vol. 46, p. 2204, 1975.

[30] J.D. Cohen and D.V. Lang, "Calculation of the dynamic response of Schottky barriers with a continuous distribution of gap states", *Physical Review B,* vol. 25, p. 5321, 1982.

[31] G. 1. Roberts and C. R. Crowell, "Capacitance Energy Level Spectroscopy of Deep-Lying Semiconductor Impurities Using Schottky Barriers", *Journal of Applied Physics,* vol. 41, p. 1767, 1970.

[32] C. T. Sah and V. G. K. Reddi, *IEEE Transactions on Electron Devices,* vol. 11, p. 345, 1964.

[33] I. Balberg, "Relation between Distribution of States and the Space-Charge Region Capacitance in Semiconductors", *Journal of Applied Physics,* vol. 58, p. 2603, 1985.

[34] A.V. Los and M.S. Mazzola, "Semiconductor impurity parameter determination from

Schottky junction thermal admittance spectroscopy", *Journal of Applied Physics,* vol. 89, p. 3999, 2001.

[35] A.V. Los and M.S. Mazzola, "Model of Schottky junction admittance taking into account incomplete impurity ionization and large signal effects", *Physical Review B,* vol. 65, p. 165319, 2002.

[36] Uwe Rau, Daniel Abou-Ras, Thomas Kirchartz, *Advanced Characterization Techniques for Thin Film Solar Cells*, Wiley-VCH, Weinbeim, 2011.

[37] I. W. Archibald and R. A. Abram, "More theory of the admittance of an amorphous silicon Schottky barrier", *Philosophical Magazine B*, vol. 54, p. 421, 1986.

[38] T. Walter, R. Herberholz, C. Muller, H.W. Schock, "Determination of defect distributions from admittance measurements and application to Cu(In,Ga)Se_2 based heterojunctions", *Journal of Applied Physics*, vol. 80, p. 441, 1996.

[39] C.T. Sah, L. Forbes, L.L. Rosier and A.F. Tasch Jr., "Thermal and Optical Emission and Capture Rates and Cross Sections of Electrons and Holes at Imperfection Centers in Semiconductors from Photo and Dark Junction Current and Capacitance Experiments", *Solid-State Electronics*, vol. 13, p. 759, 1970.

[40] C.T. Sah, "Bulk and Interface Imperfections in Semiconductors," *Solid-State Electronics*, vol. 19, p. 975, 1976.

[41] N. M. Johnson, *Applied Physic Letters,* vol. 42, p. 981, 1983.

3 Capacitance spectroscopy of a-Si:H Schottky diodes

This chapter is dedicated to the capacitance spectroscopy of hydrogenated amorphous silicon (a-Si:H) Schottky diodes. Firstly, theoretical development on capture-release processes and ac-signal capacitance spectroscopy will be presented.

Secondly, the possibilities of the capacitance technique to determine the density of states (DOS) at the Fermi level, the position of the Fermi level and the attempt-to-escape frequency will be discussed using numerical modeling. We will particularly focus on the treatment of the capacitance data suggested by Cohen and Lang in 1982 [1]. The authors presented a straightforward procedure to obtain the density of states at the Fermi level from *C-T* data. Up to our knowledge no critical assessment of this treatment has been carried out on a-Si:H Schottky diodes. We will examine the validity of the model suggested in Ref.[1] when applied to different cases. Namely, we will consider undoped and *n*-type a-Si:H with different shapes of the DOS in the band gap.

Finally, the comparison of simulation results and experimental data will be carried out.

3.1 Theoretical development

In this section we present the theory on capacitance of a a-Si:H Schottky diode.

3.1.1 Dynamics of capture and emission processes

The band diagram of a perfect single crystal semiconductor consists of a valence band and a conduction band separated by the band gap, with no energy levels within the band gap. When the periodicity of the single crystal is perturbed by foreign atoms or crystal defects,

discrete energy levels are introduced into the band gap. Such defects are commonly called generation-recombination (*G-R*) centers or traps. *G-R* centers lie deep in the band gap and are known as deep energy level impurities. For single crystal semiconductors like silicon, germanium, and gallium arsenide, deep level impurities are usually metallic impurities, but they can be crystal imperfections, such as dislocations, stacking faults, precipitates, vacancies, or interstitials.

Deep level defects act as recombination centers when there are excess carriers in the semiconductor and as generation centers when the carrier density is below its equilibrium value as in the reverse-biased space-charge region of *p-n* junctions or Schottky barriers.

Capture and emission processes at a trap level with density N_t at an energy E_t have been defined in Shockley-Read statistics [2] and are illustrated in Fig.3.1: (1) capture of an electron from the conduction band, this process is characterized by a recombination rate R_n, (2) emission of an electron from the trap to the conduction band, this process is characterized by a generation rate G_n, (3) emission of a hole from the trap to the valence band (characterized by a generation rate G_p) (4) capture of a hole from the valence band (characterized by a recombination rate R_p). These are the only four possible events between the conduction band, the impurity energy level, and the valence band. Thus, a recombination event consists in the sum of processes (1) and (4): the capture of both carriers at the trap level. A generation event is the sum of processes (2) and (3): the emission of carriers towards corresponding bands. The trapping event is described as the capture of a carrier (either (1) or (4)) followed by its emission to the band from which it came (either (2) or (3). Impurities are frequently referred to as traps, regardless of whether they act as recombination, generation, or trapping centers.

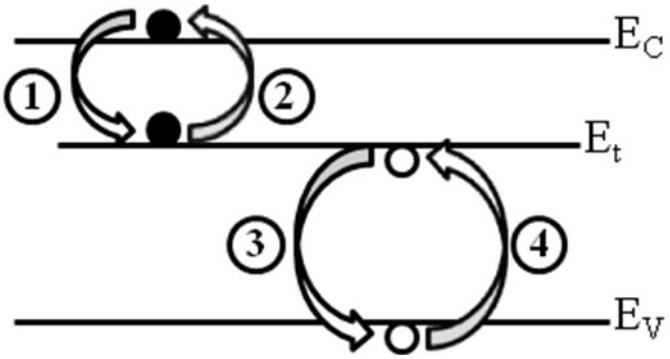

Fig.3.1. Capture-release processes of an electron (1 and 2) and a hole (3 and 4).

Whether an impurity acts as a trap or a *G-R* center depends on E_t, the location of the Fermi level in the band gap, the temperature, and the capture cross-sections of the impurity. Generally the impurities with energies near the middle of the band gap behave as *G-R* centers, whereas those near the band edges act as traps. Generally the electron emission rate for

centers in the upper half of the band gap is higher than the hole emission rate. Similarly the hole emission rate is generally higher than the electron emission rate for centers in the lower half of the band gap such that one emission rate dominates, and the other can frequently be neglected. With impurities being charged or neutral, and with electrons or holes emitted or captured, any measurement that detects charged species can be used for their characterization, *i.e.*, capacitance, current, or charge measurements.

Now, let us consider a mathematical description of the described processes. If a trap level is characterized by a density N_t, then the density of occupied defects is $n_t=N_t f_{oc}$ and the density of unoccupied defects is $p_t=N_t(1-f_{oc})$, where f_{oc} is the occupation probability function.

For the capture and emission processes described above, the recombination and generation rates can be written as (1) $R_n=c_n n p_t$, (2) $G_n=e_n n_t$ (3) $G_p=e_p p_t$ (4) $R_p=c_p p n_t$ where n and p are densities of electrons and holes respectively, c_n and c_p are capture coefficients, e_n and e_p are emission rates of electrons and holes respectively. The f_{oc} function can be then written as follows:

$$f_{oc} = \frac{c_n n + e_p}{c_n n + e_n + c_p p + e_p} \tag{3.1}$$

At thermal equilibrium with no net flow of electrons and holes between conduction and valence band, the emission rates of electrons ($e_n(E)$) and holes ($e_p(E)$) from a state at the energy E toward the conduction band and valence band can be written:

$$e_n = c_n n \exp\left(\frac{E_t - E_F}{k_B T}\right) \tag{3.2}$$

$$e_p = c_p p \exp\left(\frac{E_F - E_t}{k_B T}\right) \tag{3.3}$$

and Eq. (3.1) gives:

$$f_{oc} = \frac{1}{1+\dfrac{e_n + c_p p}{e_p + c_n n}} = \frac{1}{1+\exp\left(\dfrac{E_t - E_F}{k_B T}\right)} \tag{3.4}$$

It is noteworthy that the occupation function f_{oc} is the Fermi occupation function. Hence

this expression is eligible only in low-temperature approximation.

Under small ac bias signal, the occupation function and the electron and hole densities can be separated into two components indexed dc for the steady-state component and ac for the alternative component. Thus, n, p and f_{oc} can be written as:

$$n = n^{dc} + n^{ac} \exp(i\omega t)\,, \tag{3.5}$$

$$p = p^{dc} + p^{ac} \exp(i\omega t)\,, \tag{3.6}$$

$$f_{oc}(E) = f_{oc}^{dc} + f_{oc}^{ac} \exp(i\omega t)\,, \tag{3.7}$$

where ω is the angular frequency, i is the purely imaginary number such that $i^2 = -1$.

According to the Shockley-Read statistics, the occupation function is given by:

$$\frac{\partial f_{oc}(E)}{\partial t} = c_n n + e_p - f_{oc}(E)\left(c_n n + c_p p + e_n + e_p\right) \tag{3.8}$$

which gives, using Eqs. (3.5), (3.6) and (3.7):

$$f_{oc}^{dc}(E) = \left(c_n n_{dc} + e_p(E)\right)\tau(E)\,, \tag{3.9}$$

and

$$f_{oc}^{ac}(E) = \frac{c_n n_{ac}\left(1 - f_{oc}^{dc}(E)\right) - c_p p_{ac} f_{oc}^{dc}(E)}{i\omega + 1/\tau(E)}\,, \tag{3.10}$$

where $\tau(E)$ is defined by:

$$\tau(E) = \frac{1}{c_n n^{dc} + e_n(E) + e_p(E) + c_p p^{dc}} \tag{3.11}$$

$\tau(E)$ can also be written as:

$$\tau = \frac{f_{oc}^{dc}(E)}{c_n n^{dc} + e_p(E)} = \frac{1 - f_{oc}^{dc}(E)}{c_p p^{dc} + e_n(E)} \tag{3.12}$$

Then, using Eq. (3.12), the ac component of the occupation function is given by:

$$f_{oc}^{ac}(E) = f_{oc}^{dc}(E)(1 - f_{oc}^{dc}(E)) \frac{\dfrac{c_n n^{ac}}{c_n n^{dc} + e_p(E)} - \dfrac{c_p p^{ac}}{c_p p^{dc} + e_n(E)}}{1 + i\omega\tau(E)} \tag{3.13}$$

If we consider the case where electrons are the majority carriers (we neglect hole densities p^{ac} and p^{dc}) and where the Fermi level lies above midgap, therefore the term $c_n n^{dc} >> e_p$ (we neglect exchanges with the valence band), and Eq.(3.13) reduces to:

$$f_{oc}^{ac} \approx f_{oc}^{dc}(\mathrm{E})\,(1 - f_{oc}^{dc}(E)) \frac{n^{ac}}{n^{dc}} \frac{1}{1 + i\omega\tau(E)}, \tag{3.14}$$

with

$$\tau = \frac{1}{c_n n_{dc} + e_n(E)} \tag{3.15}$$

The capacitance C being related to the response of gap states to the small ac bias signal, it can be observed in Eq. (3.14) through the term $f_{oc}^{dc}(E)\ (1 - f_{oc}^{dc}(E))$ that a significant contribution to the capacitance can only be obtained for the gap states crossing the Fermi level $(E=E_t=E_F)$, where the time response τ_F is given by:

$$\tau_F = \frac{1}{2e_n(E_F)} \tag{3.16}$$

3.1.2 Band diagram and capacitance of a Schottky diode

As it was mentioned in the previous chapter capacitance techniques are rather applicable to doped a-Si:H. However, we shall also consider the case of undoped a-Si:H with typical Fermi level position E_C-E_F = 0.7 eV and the band gap E_g = 1.7 eV. The latter can be regarded as a slightly doped *n*-type a-Si:H. Thus we consider the Schottky barrier formed on an *n*-type semiconductor.

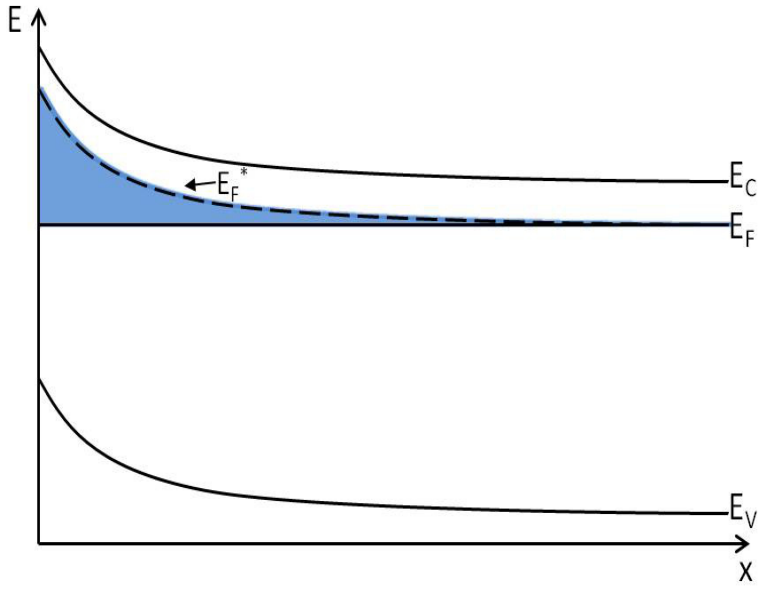

Fig.3.2. Schematic energy band diagram at equilibrium of a n-type Schottky barrier: only the states in the hatched area contribute to the static space charge. E_C and E_V are the conduction and valence band edges, respectively; E_F is the Fermi level; E_F is the level parallel to E_C and is equal to the bulk Fermi level in the neutral bulk region.*

Fig.3.2 shows a schematic energy band diagram of such a structure. We assume that neutral bulk conditions are met at the right-hand side of the figure. Only the states situated in the hatched area contribute to the space charge because, due to the band bending, these are the states that have changed their occupancy compared to the neutral bulk region. These states are located between the Fermi level E_F and the level E_F*, defined as the level parallel to the conduction band edge E_C, and equal to the bulk Fermi level in the neutral bulk region.

Let us consider this system under small inverse polarization as illustrated in Fig. 3.3. Apart from a narrow region close to the interface, the space charge density can be mainly divided into two regions. These are separated by the abscissa x_i* defined as the point where the bulk Fermi level crosses the level E_i* that corresponds to the energy where the emission frequency of electrons towards the conduction band, e_n, equals the emission frequency of holes towards the valence band, e_p. This level is close to midgap. Below this level states are filled by electrons from the valence band faster than they are excited to the conduction band. Thus levels lying below E_i* cannot be detected by small signal variation. For $x > x_i$*, the gap states occupancy is determined by the bulk Fermi level E_F that corresponds to the quasi-Fermi level for trapped electrons. For $x < x_i$*, states are essentially full below E_i* and empty above, and E_i* plays the role of the quasi-Fermi level with an occupation function, however, slightly different from the usual Fermi-Dirac form. The space charge density is constant for $x < x_i$* and is written

$$\rho_i^* = qN_i^*, \tag{3.17}$$

where N_i^* is the integral of the density of states (DOS) between the bulk Fermi level and E_i^*

$$N_i^* = \int_{E_i^*}^{E_F} N(E)dE \tag{3.18}$$

This is because all gap states lying between E_F and E_i^* are unoccupied in this region, while being occupied in the bulk. For $x > x_i^*$, the space charge density decreases with increasing x, corresponding to less gap states being unoccupied.

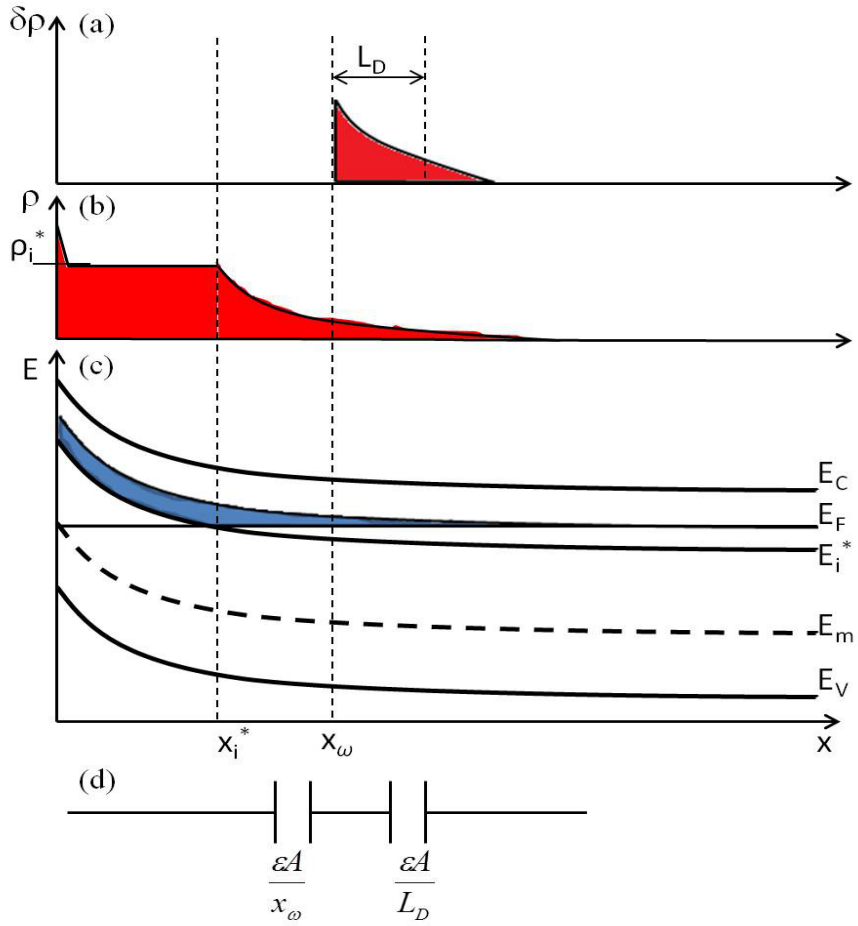

Fig.3.3. (a) ac space charge density, δρ, (b) static space charge density, ρ, (c) energy band diagram of a n-type Schottky barrier showing the space charge contribution (hatched area) under reverse bias. The energy levels are indicated: E_i^* is the energy level where $e_n = e_p$, (d) the equivalent capacitance derived from the sharp cut-off model.

The states which energy level crosses E_F at a certain distance x from the junction change their occupation and thus can be probed by admittance measurements. These levels are the levels lying deeper than the bulk Fermi level whose energy position in the neutral bulk is between E_F and E_i*. The response of these states crossing the Fermi level at a certain abscissa x is determined by the release time τ:

$$\tau(x) = \frac{1}{2e_n(E_F)} = \frac{1}{2\nu_n \exp\left(-\frac{(E_C - E_F)(x)}{k_B T}\right)} \tag{3.19}$$

where ν_n is the attempt-to-escape frequency, $(E_C\text{-}E_F)(x)$ is the position of the Fermi level referred to the conduction band edge E_C at the distance x. The pre-exponential factor ν_n is defined by:

$$\nu_n = \sigma_n v_{th} N_C \tag{3.20}$$

where σ_n is the electron capture cross section of states, v_{th} is the thermal velocity of free electrons and N_C is the effective DOS in the conduction band.

The denominator in Eq.(3.14) puts the limitation on the product of time response τ and angular frequency ω. In order to have a response of states to the ac modulation $\omega\tau$ should be low enough, suppose $\omega\tau < 1$. A cut-off abscissa x_ω for the response of gap states is defined using the mentioned condition:

$$\tau(x_\omega)\omega = 1 \tag{3.21}$$

$$2\nu_n \exp\left(-\frac{(E_C - E_F)(x_\omega)}{k_B T}\right) = \omega \tag{3.22}$$

Thus one can define that the response takes place when $\omega\tau(x_\omega) < 1$ at an angular frequency ω and temperature T of the measurement. The ac space charge density has a characteristic width equal to the Debye length L_D (see Fig.3.3(a)) that is representative of the DOS at the Fermi level:

$$L_D = \sqrt{\frac{\varepsilon}{q^2 N(E_F)}} \tag{3.23}$$

Taking into account that Eq. (3.19) expresses a rapidly varying function with the abscissa x, an abrupt cut-off model can be introduced to rapidly derive the main behavior of the dynamic response of the device to the ac modulation. This means that the states crossing E_F with an abscissa smaller than x_ω cannot follow the ac modulation, whereas those with an abscissa greater than x_ω will follow it instantly. Here we use the sharp cut-off approximation by ignoring the fact that there are the intermediate states around x_ω that respond only partially to the modulation. Thus here are two regions contributing to the total capacitance: at the left of x_ω, the device behaves as a pure dielectric medium with the contribution of $\varepsilon A/x_\omega$, whereas at the right of this cut-off abscissa, the localized states contribution to the total capacitance is written as $\varepsilon A/L_D$, ε being the dielectric permittivity of the active layer and A the junction area.

A simple picture of the equivalent capacitance of the device is shown in Fig.3.3 (d) and the total capacitance can be written:

$$\frac{C}{A} = \frac{\varepsilon}{x_\omega + L_D} \tag{3.24}$$

Looking at the temperature dependence of the characteristic response time (Eq. (3.20)), it appears that τ increases with decreasing temperature, so that the cut-off abscissa x_ω also increases since more states become unable to respond on the time scale imposed by the measurement frequency. At low temperatures no states follow the modulation and the measured capacitance equals the geometric dielectric layer capacitance $C=\varepsilon A/d$, where d is the thickness of the semiconductor layer. This is the lowest capacitance of this layer. At a given frequency ω_0 there will be a certain turn-on temperature T_0 at which states lying at the Fermi level in the bulk start responding to the ac signal. In the similar way, at a given temeperature T_0 if one scans a wide range of frequency there will be a turn-on frequency ω_0 at which the onset of the response of gap states appears. T_0 and ω_0 are linked through:

$$2\nu_n \exp\left(-\frac{(E_C - E_F)_{bulk}}{k_B T_0}\right) = \omega_0 \tag{3.25}$$

Increasing the temperature leads to a movement of the cut-off abscissa towards the junction and an increase of the capacitance until x_ω reaches x_i*. At this stage, all the states that could potentially respond are actually responding, and a further increase in temperature does not lead to an increase of the gap states response since the occupancy of gap states for $x< x_i$* is independent of the Fermi level and cannot be modulated by the bias modulation. Therefore the variation of C with T just above turn-on is related to the DOS at the bulk Fermi level, $N(E_F)$.

3.1.3 The simple treatment *K-T* of the *C-T* data

It was shown [1] that if one considers the following term that we assign as *K:*

$$K(T) = C^2(T)\left[\frac{dC}{dT}\right]^{-1}, \tag{3.26}$$

it is possible to obtain directly the magnitude and the slope of the density of states at the Fermi level. Indeed, if we consider capacitance defined in Eq.(3.24) at a turn-on frequency ω_0, it can be written:

$$\frac{dC}{dT} = -\frac{\varepsilon A}{\left(x_{\omega_0} + L_D\right)^2}\frac{dx_{\omega_0}}{dT} \tag{3.27}$$

Using Eqs.(3.22) and (3.25) we can write:

$$\left(E_C - E_F\right)(x_{\omega_0}) = k_B T \ln\frac{2\nu_n}{\omega_0}, \tag{3.28}$$

and

$$\left(E_C - E_F\right)_{bulk} = \left(E_C - E_F\right)(x=\infty) = k_B T_0 \ln\frac{2\nu_n}{\omega_0} \tag{3.29}$$

The difference of the two last equations is written as follows

$$E_C(x_{\omega_0}) - E_C(\infty) = k_B(T - T_0)\ln\frac{2\nu_n}{\omega_0} \tag{3.30}$$

$$q\left[V(\infty) - V(x_{\omega_0})\right] = k_B(T - T_0)\ln\frac{2\nu_n}{\omega_0}, \tag{3.31}$$

where $E_C(\infty) = -qV(\infty)$. Using the definition of the Debye length as a distance where the electric field diminishes by a factor of $1/e$, we can then rewrite Eq.(3.31):

$$q[V(\infty)-V(0)]\exp\left(-{}^{x_{\omega_0}}\!/_{L_D}\right)=k_B(T-T_0)\ln\frac{2\nu_n}{\omega_0} \tag{3.32}$$

Then we define $x_{\omega 0}$ explicitly as

$$x_{\omega_0}=L_D\ln\left[\frac{q[V(\infty)-V(0)]}{k_B(T-T_0)\ln\frac{2\nu_n}{\omega_0}}\right] \tag{3.33}$$

Differentiation of $x_{\omega 0}$ with respect to temperature gives

$$\frac{dx_{\omega_0}}{dT}=-\frac{L_D}{T-T_0} \tag{3.34}$$

Substituting $dx_{\omega 0}/dT$ in Eq.(3.27) we obtain for the term K defined by Eq.(3.26)

$$K(T)=C^2(T)\left[\frac{dC}{dT}\right]^{-1}=\frac{T-T_0}{L_D}, \tag{3.35}$$

Indeed, around T_0 the onset of the capacitance is due to the response of states at the bulk Fermi level, so that a linear temperature dependence of $K(T)$ should be revealed, with a slope equal to the inverse of L_D.

From the intercept value with the abscissa axis of the K-T curves one can obtain a range of T_0 values at different angular frequencies ω. Tracing Arrhenius plot in ω vs $1000/T_0$ coordinates allows one to obtain the activating energy $(E_C\text{-}E_F)_{bulk}$ and ν_n values according to Eq.(3.31) as it is shown in Fig.3.4 for T_0 values obtained from analytically calculated K-T dependencies.

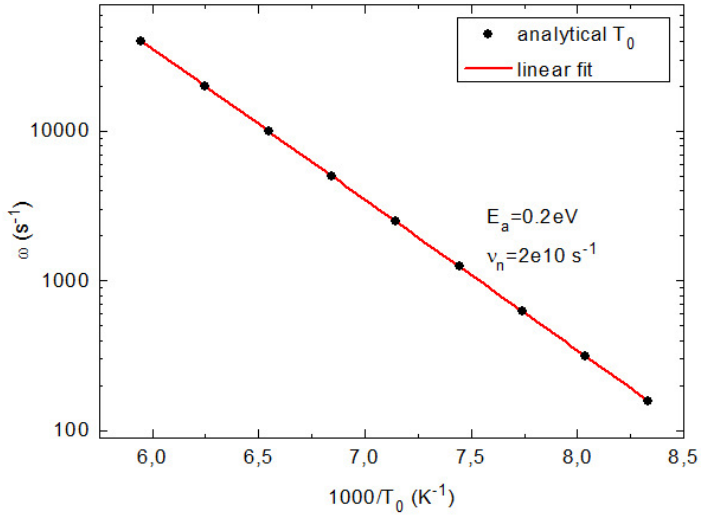

Fig.3.4. Arrhenius plot ω vs 1000/T_0 for T_0 values obtained from analytically calculated K-T dependencies. The derived activation energy and the attempt-to-escape frequency values are indicated.

Apart of this simple treatment presented above another approach introduced by Walter et al [3] is widely used. This model has been proposed to determine the defect distributions in the bandgap, and it is generally associated with copper indium diselenide (CIGS) material studies [4-6]. Walter et al. introduced a simplified spatial variation (linear or quadratic) of both the dc-and ac-electrostatic potentials. Their calculations were also developed in the framework of the abrupt cut-off model, and in the case of linear spatial variations of the electrostatic potentials, the following expression was obtained to perform the gap states spectroscopy:

$$N(E_\omega) = \frac{V_d}{qkTw}\frac{d\left(\frac{C}{A}\right)}{d(\ln(\omega))}, \tag{3.36}$$

where $N(E_\omega)$ stands for the gap states density at the limit level E_ω, which crosses the Fermi level at the cut-off abscissa x_ω, w is the space-charge width. This level is given by:

$$E_{C/V} - E_\omega = kT\ln\left(\frac{2\nu_{n/p}}{\omega}\right) \tag{3.37}$$

$E_{C/V}$ (or correspondingly $\nu_{n/p}$) stands either for E_C or E_V to indicate that the charge state of this level is changed with capture and emission processes of majority carriers coming predominantly either from the conduction or valence band edge respectively. If a particular level E_ω (such as a peak in the DOS distribution or the bulk Fermi level) can be

experimentally identified, then $v_{n/p}$ can be determined by plotting the data in the Arrhenius coordinates.

3.2 Modeling of a-Si:H Schottky diodes

Numerical modeling is a powerful tool to study semiconductor devices, namely solar cells. While the modeling of crystalline silicon wafers is well understood, the amorphous layer and especially the interface between the a-Si:H layer and the crystalline Si are by far more difficult to model. a-Si:H can be described as a semiconductor with a defect distribution consisting of band tail and dangling bond states in the band gap [7]. A demanding task concerns the various material parameters used as inputs in the simulation. Of crucial importance are the density, the distribution as well as the capture cross sections of the defects in the a-Si:H layer and at the interface.

All the material parameters mentioned above have in common that they are difficult to measure and that they can vary for a-Si:H of different doping levels, deposited under different conditions and possibly with different thicknesses. Thus, the simulation model has to be carefully calibrated with different measurement techniques such as *I-V* curves, external quantum efficiency (EQE), quasi-steady-state photo conductance (QSSPC) measurements, etc...

Numerical simulations were performed with AFORS-HET v3.0 software [8,9] and ATLAS device simulator from Silvaco International. The detailed description of the software tools and introduced parameters of the material can be found in Appendix B.1.

Numerical calculations of the capacitance as a function of temperature (*T*) and frequency (*f*) of a-Si:H Schottky diodes were carried out. The applied ac signal was set at 0.02 V. From the calculated *C–T–f* data, *K* was plotted against *T* and fitted to a linear function above turn-on temperature in order to derive T_0 and $N(E_F)$ values according to Eq.(3.35). The activation energy, $E_a=E_C-E_F$, and the attempt-to-escape frequency, v_n, were extracted as well by plotting ω against $1000/T_0$ according to Eq.(3.25). Here we focus on extracting $N(E_F)$, E_a and v_n in the conditions where we assume that the transport of charges is fast and does not affect the capture-release processes. In order to meet this condition the dielectric relaxation time τ_{dr} should be smaller than the characteristic release time τ defined by Eq.(3.25) and that is assigned here as $\tau_{c\text{-}r}$ (capture-release):

$$\tau_{c-r} / \tau_{dr} >> 1 \tag{3.38}$$

This way we assume that transport of electrons is fast enough and does not determine the global time constant of the considered processes. The dielectric relaxation time of electrons is defined as follows

$$\tau_{dr} = \frac{\varepsilon}{\sigma} = \frac{\varepsilon}{qn\mu_n} = \frac{\varepsilon}{qN_C \exp\left(-\frac{E_C - E_F}{kT}\right)\mu_n}, \tag{3.39}$$

where σ is the conductivity, q the electron charge, n the electron density, N_C the effective conduction band density of states and μ_n the electron mobility. Then condition from Eq.(3.38) can be written using Eq.(3.25) and Eq.(3.39)

$$\frac{\tau_{c-r}}{\tau_{dr}} = \frac{1 \Big/ 2v_{th}\sigma_n N_C \exp\left(-\frac{E_C - E_F}{kT}\right)}{\varepsilon \Big/ qN_C \exp\left(-\frac{E_C - E_F}{kT}\right)\mu_n} = \frac{q\mu_n}{2\varepsilon v_{th}\sigma_n} >> 1 \tag{3.40}$$

With typical values for amorphous silicon we obtain the limit for the capture cross-section $\sigma_n << 8\times10^{-14}$ cm^2. For all considered cases in Section 3.2.1 this condition is respected and the capture cross-section of electrons is kept equal to 1×10^{-17} cm^2. The possible influence of the capture cross-section and the charge mobility on the capacitance-temperature dependency is discussed in Section 3.2.2.

Capacitance-temperature dependencies calculated with AFORS-HET software for various frequencies are presented in Fig.3.5. The onset of the capacitance response is shifted to higher temperatures for larger frequencies according to Eq.(3.25).

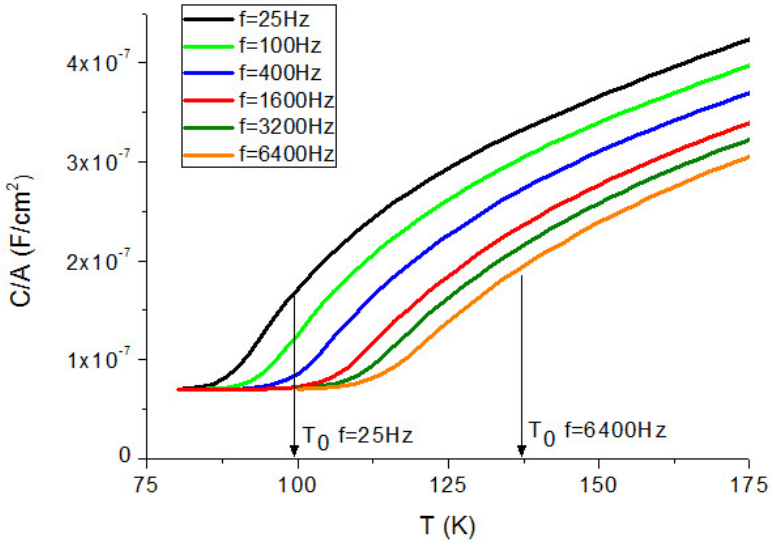

Fig.3.5. Capacitance-temperature curves of a-Si:H Schottky barrier for different frequencies using the parameters presented in Appendix B.1 for constant DOS $N(E)=1\times10^{19}cm^{-3}eV^{-1}$ *and* E_C-E_F=0.2 *eV. The indicated turn-on temperatures are obtained from the intercept of the linear fit with abscissa axis of the corresponding K-T dependencies.*

3.2.1 Determination of the DOS at the Fermi level, $N(E_F)$, the activation energy, E_a, and the attempt-to-escape frequency, ν_n

3.2.1.1 Constant DOS

At first the simplest case of constant density of states (DOS) is considered. Two cases, that represent *n*-type and undoped a-Si:H with the Fermi level at 0.2 and 0.7 eV from the conduction band edge respectively, are examined. The band gap of 1.75 eV was introduced. Capacitance-temperature dependencies are calculated for the temperature range T = 80-400 K and frequency range f = 100-1×10^{14} Hz. From the treatment *K-T* of *C-T* data for each frequency $L_D^{a\text{-}Si:H}$ and T_0 are derived. Then the activation energy and the attempt-to-escape frequency are obtained from the Arrhenius plot. Finally, the derived from the treatment procedure parameters $N(E_F)$, E_a and ν_n are compared to that introduced into simulations.

3.2.1.1.a n-type a-Si:H: E_C–E_F=0.2 eV, $N(E_F)$=1×10^{19}cm^{-3}eV^{-1}

Let us first consider the case with E_C–E_F = 0.2 eV. The position of the Fermi level was fixed at 0.2 eV at temperature close to theoretical value of T_0 for the considered case. Here E_C–E_F = 0.2 eV was fixed at T = 100 K. The work function of the metal was introduced at φ_M = 4.9 eV in order to have a band bending fixed at ($E_C^{x=0}$-E_C^{bulk}) = 0.85 eV. The constant DOS $N(E)$=$N(E_F)$=1×10^{19}cm^{-3}eV^{-1} was introduced into simulations. This high value of $N(E)$ is characteristic of *n*-type a-Si:H due to the presence of defects introduced by doping atoms. The

C–T curve calculated from the numerical simulation is compared to the one derived from the simplified analytical expression (Eq. (25)) in Fig.3.6(a). The low temperature capacitance in the analytical expression is zero since an infinite semi-conductor is assumed.

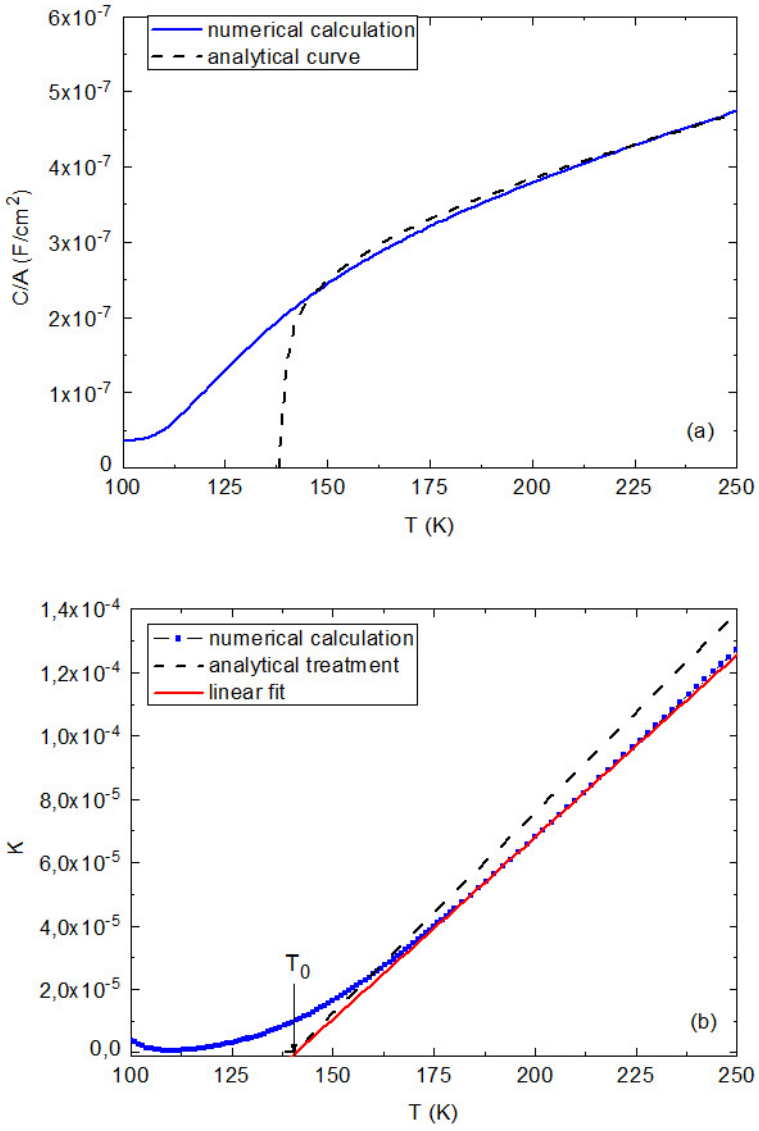

Fig.3.6. (a) Capacitance-temperature curves at f=400 Hz deduced from analytical and numerical calculation and (b) corresponding treatment curves. The introduced constant DOS is $N(E)=N(E_F)=1\times10^{19}cm^{-3}eV^{-1}$ *and the bulk Fermi level is fixed at* $E_C–E_F=0.2$ *eV at 100K.*

The main difference is that at low temperatures, numerically calculated capacitance increases more smoothly when compared to the analytically obtained *C–T* curve. However this does not affect the value of T_0 which is found to be equal to the theoretical one as it can be seen from the treatment of the capacitance data, *K-T* in Fig.3.6(b). It is noteworthy that the processed data shown in Fig.3.6b experience a well defined linear region that allows a good determination of the slope, which is close enough to the one obtained by the simplified

theoretical approach. Indeed, the DOS at the Fermi level derived from the linear fit of K vs. T according to Eq.(3.35) yields $N(E_F)$=8.2×10^{18} cm^{-3}eV^{-1}, which is quite close to the one that was introduced into the calculations.

As already shown in Fig.3.6b, the turn-on temperature deduced from the numerical calculations is the same as the one expected from the simplified analytical approach. The same behavior is observed for other frequencies, the turn-on temperature deduced from modeling being equal to that from the analytical prediction. These results are presented in the Arrhenius plot of ω vs $1000/T_0$ as it can be seen in Fig.3.7. The good reproduction of the turn-on temperatures for the whole frequency range allows one to determine precisely the attempt-to-escape frequency, as well as the activation energy E_C–E_F which is found equal to the one that was introduced in the model (0.2 eV).

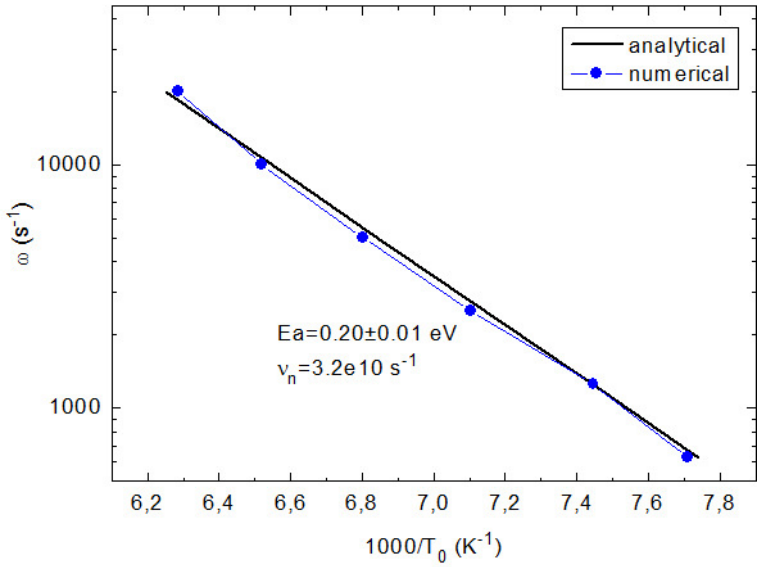

Fig.3.7. Analytically and numerically calculated Arrhenius plot ω vs $1000/T_0$ for E_C-E_F=0.2 eV and $N(E_F)$=1×10^{19}cm^{-3}eV^{-1}.

3.2.1.1.b n-type a-Si:H: E_C–E_F=0.2 eV, $N(E_F)$=1×10^{16}cm^{-3}eV^{-1}

Before studying the undoped a-Si:H Schottky diode with E_C–E_F=0.7 eV and typical DOS $N(E)$=1×10^{16} cm^{-3}eV^{-1} it is important to model the case, where only one parameter is changed, namely the DOS. In this paragraph we present the results of capacitance-temperature calculation performed on the n-type a-Si:H with E_C–E_F=0.2 eV fixed at 100 K, but with the DOS lowered to $N(E)$=1×10^{16} cm^{-3}eV^{-1}.

In Fig.3.8(a) and 3.8(b) the C–T and K–T curves are presented.

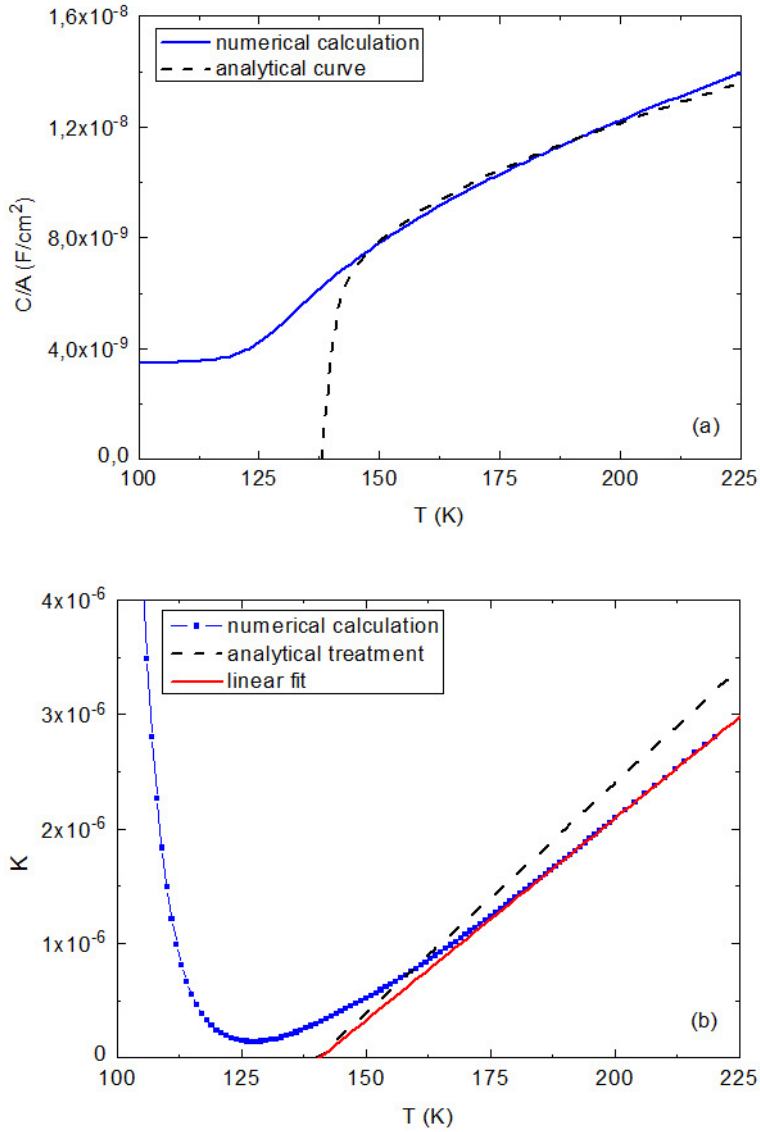

Fig.3.8. (a) Capacitance-temperature curves at f=400 Hz deduced from analytical and numerical calculation and (b) corresponding treatment curves. The introduced constant DOS is $N(E)=N(E_F)=1\times10^{16}cm^{-3}eV^{-1}$ *and the bulk Fermi level is fixed at* $E_C–E_F=0.2$ *eV at 100K.*

As it can be seen from Fig.3.8, numerical calculations show good reproduction of the theoretical *C-T* curve. The *K-T* treatment provides a T_0 value that is close to the analytical one, although $N(E_F)$ is slightly underestimated being equal to $7.7\times10^{15}cm^{-3}eV^{-1}$. The Arrhenius plot in ω vs $1000/T_0$ coordinates is presented in Fig.3.9.

One can see that at higher frequencies the deduced values of the turn-on temperature become lower than the analytical ones. This shift of T_0 leads to the slightly overestimated value of the activation energy that is found equal to 0.23 eV. The attempt-to-escape frequency is overestimated by one order of magnitude.

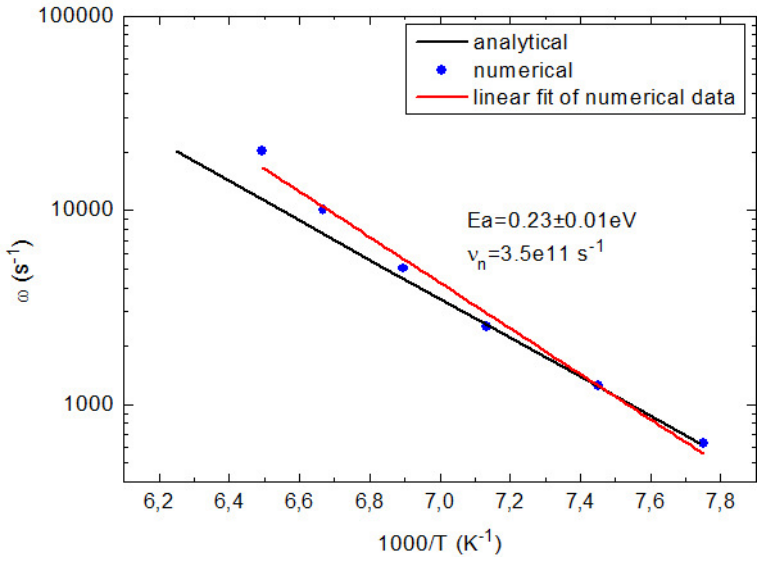

Fig.3.9. Analytically and numerically calculated Arrhenius plot ω vs 1000/T_0 for E_C-E_F=0.2 eV and $N(E_F)$=1×$10^{16}$$cm^{-3}eV^{-1}$.

The possible explanation of the shift of T_0 at higher frequencies is the temperature's influence on the considered system. At higher frequencies the chosen points for the linear fit of *K-T* data lie at considerably higher temperatures that the expected T_0. At these temperatures the studied system experiences some changes, namely the shift of the Fermi level which was fixed at 0.2 eV at 100 K. Another reason can be the ambiguity arising from the linear fit of the treatment curves. As one may notice the *K-T* curve at Fig.3.8b does not experience a sole linear region, therefore the accuracy of the derived parameters depends on the points chosen for the linear fit.

The main parameters obtained from the *K-T* treatment for the case of E_C-E_F=0.2 eV and two values of the density of states at the Fermi level are summarized in Table 3.1.

		$N(E_F)$ ($cm^{-3}eV^{-1}$)	E_C-E_F (eV)	ν_n (s^{-1})
n-type a-Si:H E_C-E_F=0.2 eV	introduced	1×10^{19}	0.20	2×10^{10}
	reconstructed	7.9-8.5×10^{18}	0.19-0.21	3.2-5.0×10^{10}
	introduced	1×10^{16}	0.20	2×10^{10}
	reconstructed	7.5-7.7×10^{15}	0.22-0.24	2-5×10^{11}

Table 3.1. Comparison of the parameters introduced in the numerical calculation with those derived from the simplified treatment of C–T–f curves for the position of the Fermi level in a-Si:H fixed at 0.2 eV from the conduction band egde and DOS values of either 10^{19} or 10^{16} $cm^{-3}eV^{-1}$.

It is shown that for the case of E_C-E_F=0.2 eV the treatment *K-T* works well yielding close values of the DOS at the Fermi level to the ones introduced into the calculations. The activation energy deduced from the Arrhenius plot is reproduced precisely as well. The considerable error is obtained for the attempt-to-escape frequency in the case of $N(E_F)$=1×10^{16}cm^{-3}eV^{-1} where the influence of the increasing temperature on the calculated results becomes significant.

One important parameter which influence on the capacitance signal was considered is the height of the Schottky barrier. As it was mentioned above the band bending was fixed at ($E_C^{x=0}$-E_C^{bulk})=0.85 eV that introduces a barrier of 1.05 eV. In order to compare the *C-T* curves for different heights of the barrier we introduced a smaller band bending ($E_C^{x=0}$-E_C^{bulk}) = 0.45 eV (barrier of 0.65 eV). Two numerically calculated capacitance curves are presented in Fig.3.10 as well as the analytical ones.

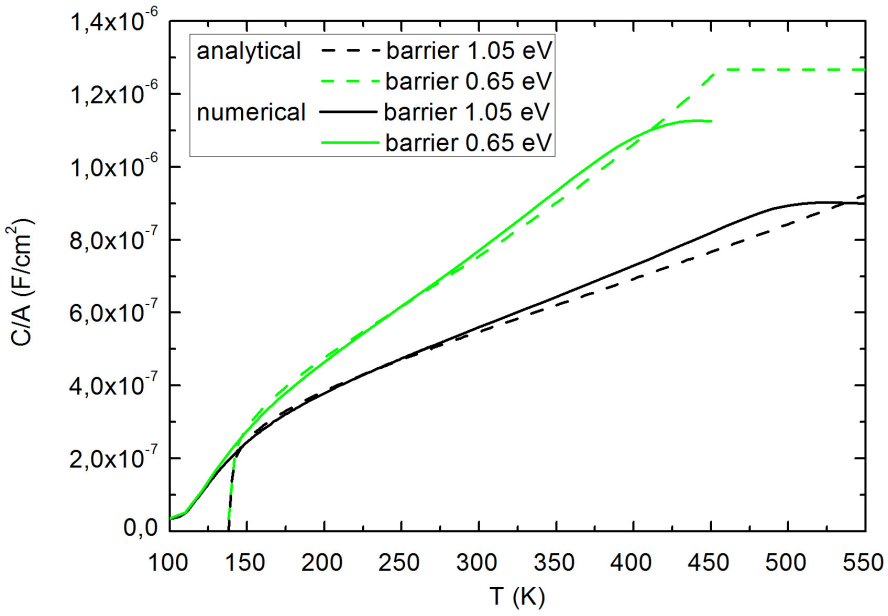

Fig.3.10. Capacitance-temperature curves at f=400 Hz deduced from analytical and numerical calculation for barrier heights 1.05 eV and 0.65 eV.

One can see that numerical calculations reproduce quite well the behavior predicted by theory. Indeed, at a given frequency ω the same defect level E_t crosses the Fermi level at different distance from the interface $x_{1\omega}$ and $x_{2\omega}$ for different values of the band bending respectively, as it is shown in Fig.3.11. Since $x_{2\omega}$< $x_{1\omega}$ the capacitance C_2 (green curve in Fig.3.10) calculated from Eq.(3.24) is larger than C_1 (black curve in Fig.3.10): C_1<C_2.

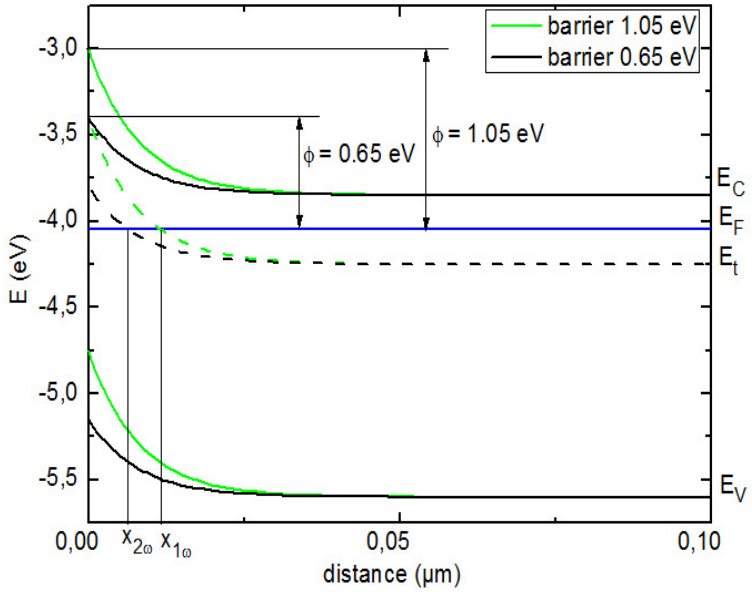

Fig.3.11. Band diagram of a Schottky barrier for n-type a-Si:H (E_C-E_F = 0.2 eV) for different values of the barreir height (ϕ) at the interface.

The saturation of the capacitance that can be observed in Fig.3.10 is predicted by theory as well. The maximum value of the capacitance is reached when x_ω becomes zero and the deepest level that can be probed is following the ac modulation. The saturation value of capacitance is thus: $C/A=\varepsilon/L_D^{a\text{-}Si:H}$. However, the saturation of the numerically calculated curves is reached at lower values of capacitance than those expected from analytical calculation. The possible explanation can be the intervention of holes and their recombination with free electrons close to the interface. In order to assess this supposition we modeled the same structures but with reducing capture cross section of the holes σ_p in the band gap to negligible values. In this way we suppress any capture-release exchange of holes. The results are shown in Fig.3.12.

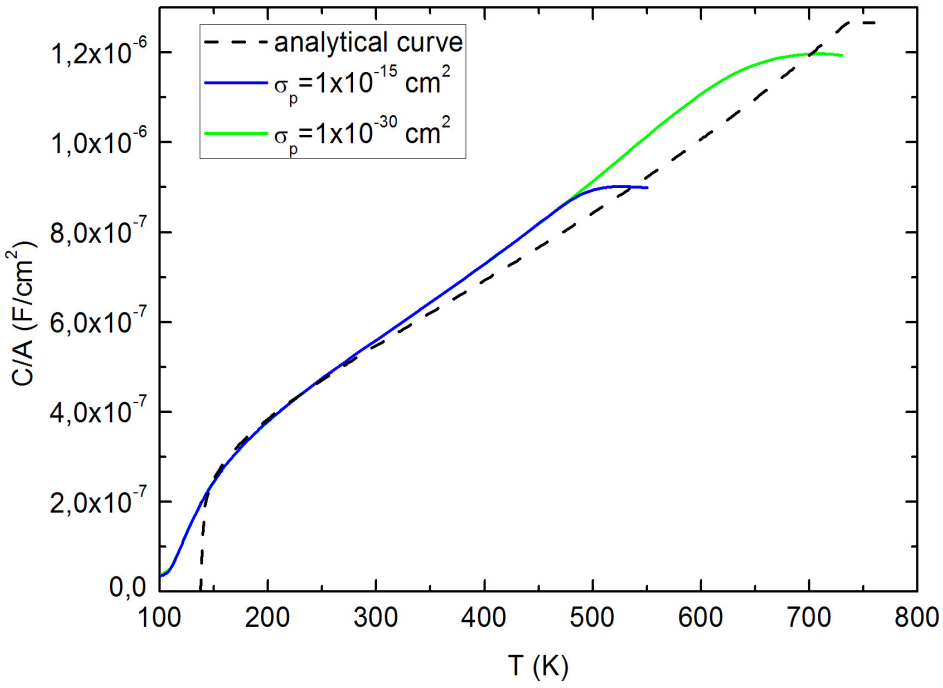

Fig.3.12. Capacitance-temperature curves at f=400 Hz obtained from analytical and numerical calculation for band bending value at ($E_C^{x=0}$-E_C^{bulk}) = 0.85 eV (ϕ = 1.05 eV) and different values of capture cross section of holes.

Reducing the hole capture cross section results in the significant increase of the capacitance saturation value that almost reaches the theoretical one. Indeed, the holes participate in the exchange with the valence band and can recombine with the electrons thus reducing their contribution to capture-release processes. This effect is more pronounced as the valence band approaches the Fermi level due to the band bending. The fewer electrons can follow the ac modulation the smaller capacitance is.

The deviation of the numerical *C-T* curves from the analytical ones at high temperature is explained by several factors. The Fermi level was fixed at 0.2 eV at 100 K close to the values of turn-on temperatures. However from 200 K the Fermi level is no longer kept at the introduced value, therefore the comparison with the theoretical curve at high *T* should be done with certain considerations keeping in mind that the Fermi level has increased. Another important reason is the validity of the assumptions introduced in the theoretical development section, namely the low-temperature approximation. The reliability of these assumptions is discussed further for the case of undoped a-Si:H with E_C–E_F=0.7 eV.

3.2.1.1.c Undoped a-Si:H: E_C–E_F=0.7 eV, $N(E_F)$=1×10^{16}cm^{-3}eV^{-1}

Let us now address the case where E_C–E_F=0.7 eV. Again, at first the simplest case of the constant DOS was considered with a value typical of device grade undoped a-Si:H,

$N(E)$=1×10^{16} cm^{-3}eV^{-1}. The metal work function was kept the same φ_M = 4.9 eV yielding the band bending fixed at ($E_C^{x=0}$-E_C^{bulk}) = 0.35 eV. In Fig.3.13(a) and 3.13(b) the *C–T* and *K–T* curves are shown. If we compare these results with those presented in Fig.3.6, we can see that the change of the position of the Fermi level and the density of states influences dramatically the results. The *C–T* dependence obtained from numerical modeling is characterized by a much lower turn-on temperature compared to the one derived from the analytical approach. One should note the appearance of the saturation of the capacitance signal at high temperatures for the numerically calculated curve. This saturation is due to the full response of all defect levels that can be probed by the technique, thus capacitance becomes constant and is equal to $\varepsilon / L_D^{a\text{-}Si:H}$.

The significant shift of the *C-T* curve to the lower temperatures leads to a determination of the attempt-to-escape frequency that is overestimated by about two orders of magnitude (see Fig.3.14). Furthermore the *K–T* curve yields a significantly underestimated value for the DOS at the Fermi level: $N(E_F)$=2.9×10^{15} cm^{-3}eV^{-1}, with a higher uncertainty due to the less well defined linear region.

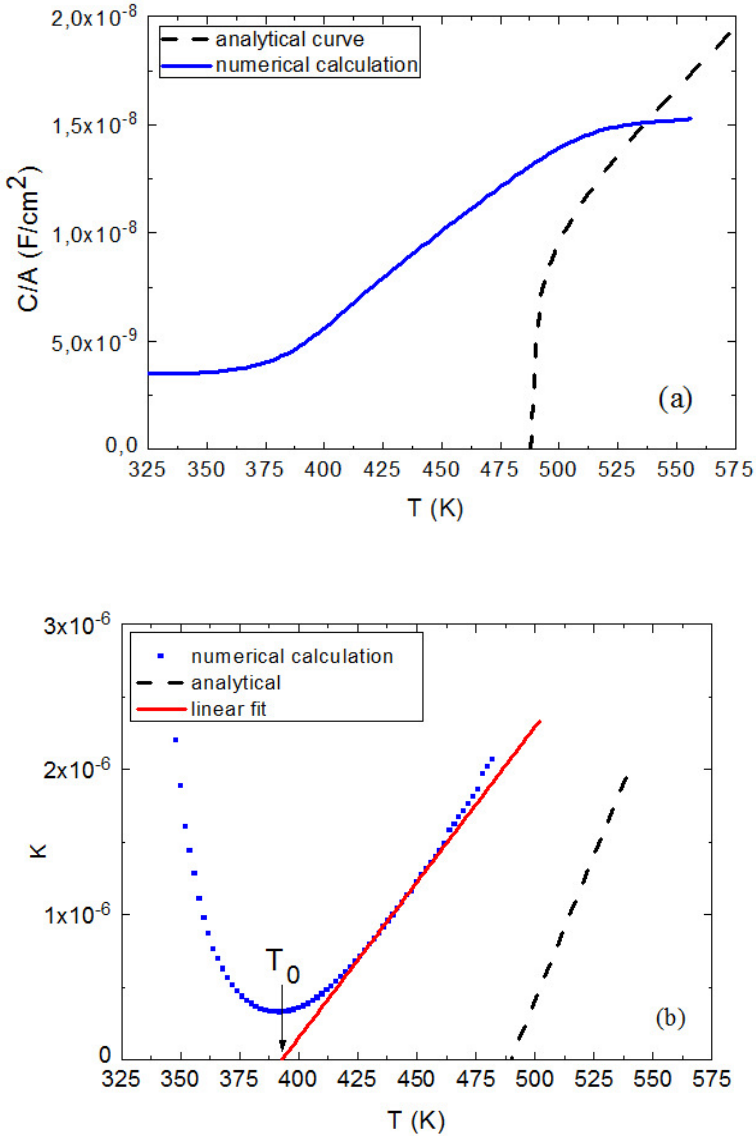

Fig.3.13. (a) Capacitance-temperature curves at f=400 Hz deduced from analytical and numerical calculation and (b) corresponding treatment curves. The introduced constant DOS is $N(E)=N(E_F)=1\times10^{16}cm^{-3}eV^{-1}$ *and the bulk Fermi level is fixed at* $E_C–E_F=0.7$ *eV.*

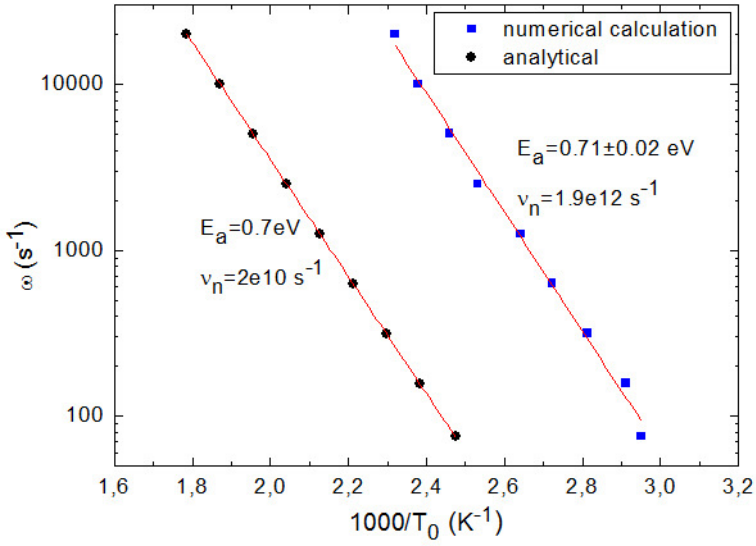

Fig.3.14. Analytically and numerically calculated Arrhenius plot ω vs 1000/T_0 for E_C-E_F=0.7 eV and $N(E_F)=1\times10^{16}cm^{-3}eV^{-1}$.

The determination of the activation energy from the Arrhenius plot in Fig.3.14 is very precise while again the attempt-to-escape frequency is greatly overestimated.

The same tendency is observed for the case E_C–E_F=0.7 eV with a higher DOS $N(E_F)$ = 1×10^{19} $cm^{-3}eV^{-1}$ as shown in Fig.3.15.

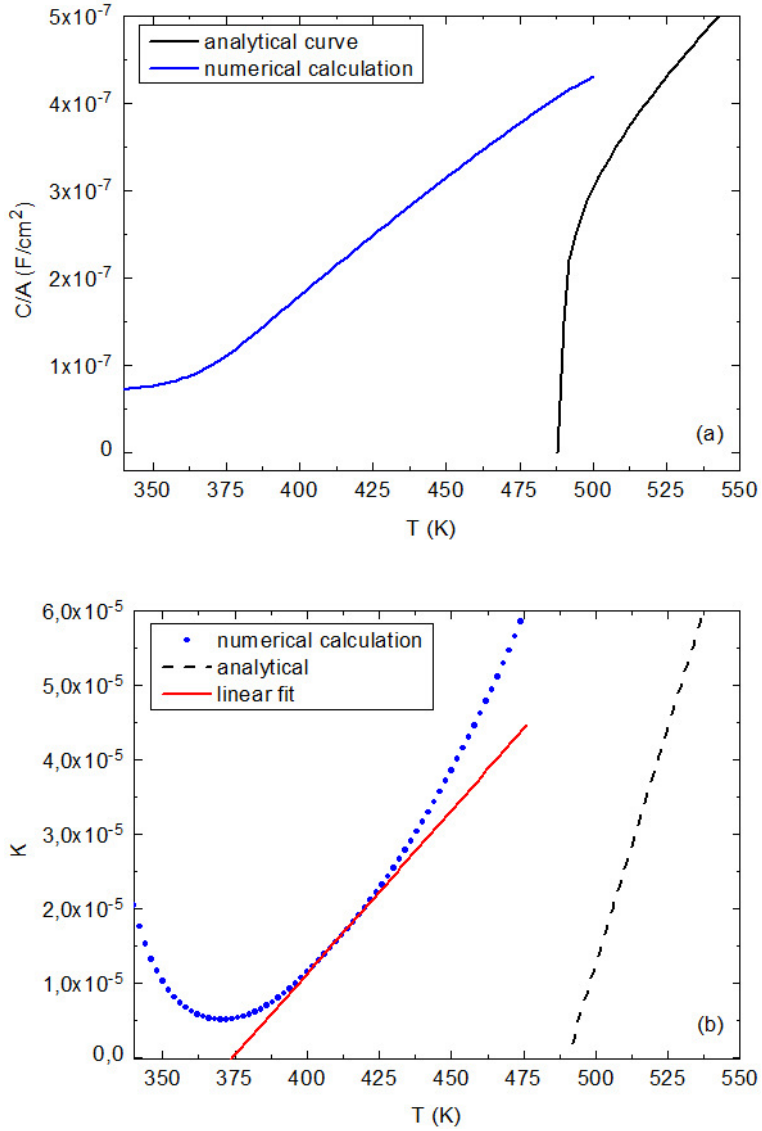

Fig.3.15. (a) Capacitance-temperature curves at f=400 Hz deduced from analytical and numerical calculation, (b) corresponding treatment curves. The introduced constant DOS is $N(E)=N(E_F)=1\times10^{19}cm^{-3}eV^{-1}$ *and the bulk Fermi level is fixed at* $E_C–E_F=0.7$ *eV.*

This case is characterized by difficulties with the linear approximation arising from the shape of the fitted *K-T* curve. As one can see in Fig.3.15(b) the *K(T)* curve does not experience a well-defined linear region. The calculated values of the DOS at the Fermi level are considerably underestimated by around one order of magnitude: $N(E_F)_{average}$ = $1.22\times10^{18}cm^{-3}eV^{-1}$. Again, the retrieved value of the attempt-to-escape frequency from the treatment of *K–T* curves was found largely overestimated (2.7×10^{12} s^{-1} instead of 2×10^{10} s^{-1}) while the obtained value of the activation energy is precise as it is shown in Fig.3.16. In addition, the error in the determination of $N(E_F)$ is much larger than in the low DOS case, the main source of errors in the determination of $N(E_F)$, as it was mentioned above, being the linear fit of *K–T* curves.

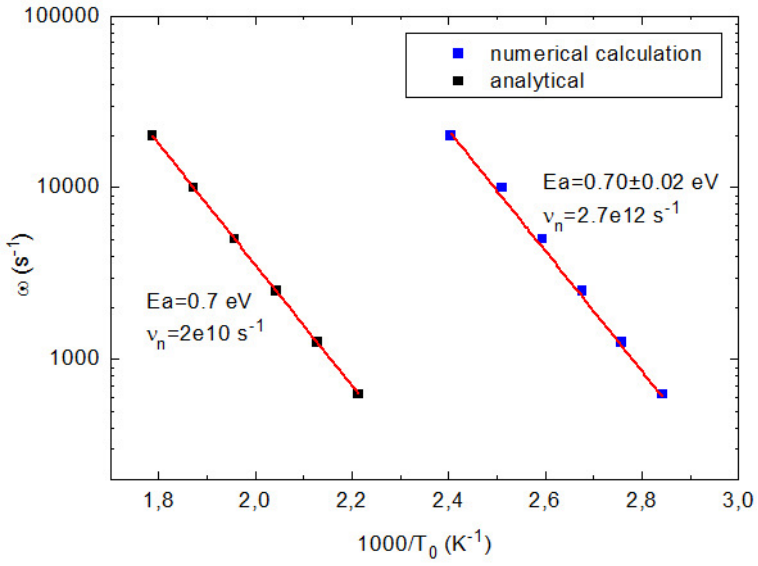

Fig.3.16. Analytically and numerically calculated Arrhenius plot ω vs 1000/T_0 for E_C-E_F=0.7 eV and $N(E_F)=1\times10^{19}cm^{-3}eV^{-1}$.

The comparison of the parameters introduced in the numerical modeling and those deduced from the treatment of *C-T-f* curves is given in Table 3.2.

		$N(E_F)$ ($cm^{-3}eV^{-1}$)	E_C-E_F (eV)	ν_n (s^{-1})
undoped a-Si:H E_C-E_F=0,7 eV	introduced	1×10^{16}	0.70	2×10^{10}
	reconstructed	$2.9\text{-}4.0\times10^{15}$	0.69-0.73	$1\text{-}4\times10^{12}$
	introduced	1×10^{19}	0.70	2×10^{10}
	reconstructed	$1\text{-}2\times10^{18}$	0.69-0.71	$2\text{-}4\times10^{12}$

Table 3.2. Comparison of the parameters introduced in the numerical calculation with those derived from the simplified treatment of C–T–f curves for the position of the Fermi level at 0.7 eV from E_C and DOS values of either 10^{19} or 10^{16} $cm^{-3}eV^{-1}$.

Up to this point we may conclude that changing the position of the Fermi level introduces significant error to the derivation of $N(E_F)$. It can be explained from the low-temperature limit approximation of gap states occupancy and the sharp cut-off approximation in the response to the ac modulation made to describe the changes in space charge density that were adopted when obtaining the equations presented in the theoretical development section. Indeed, the occupation function f_{oc} in the form of the Fermi function (Eq.3.4) is valid only in low temperature approximation. Therefore for the case of undoped a-Si:H with the analytically derived T_0 exceeding 400 K, the eligibility of the used approximation is questionable even for low frequencies. Numerical simulations showed that the onset of the response of the gap

states starts at far lower temperatures with more than 100 K difference from the analytical values. This can be interpreted as evidence that the T_0 approximation implied is no longer valid. As a consequence the treatment based on the preceding assumptions does not allow one to draw the correct value of $N(E_F)$. The inaccurate determination of T_0 leads to the erroneous determination of the attempt-to-escape frequency from the Arrhenius plot.

The sharp cut-off approximation implies that the states at E_F with an abscissa smaller than x_ω cannot follow the ac modulation, whereas those with an abscissa larger than x_ω will follow it instantly. We can evaluate this approximation by introducing two different constant defect distribution: one below the Fermi level (E_C–E_F=0.7 eV) and another above it so that the first distribution N_1 is defined by a constant DOS value equal to 1×10^{16} $cm^{-3}eV^{-1}$ between 0 and 1.55 eV from E_V, and the second one N_2 by the same constant DOS value between 1.55 and 1.75 eV from E_V. Apart from their energy repartition, these DOS distributions also differ from each other in the values of the capture cross section of defects in the gap. In order to suppress the response to the ac modulation of the state above the Fermi level we introduced negligible value of the capture cross-section of electrons $\sigma_n = 1\times10^{-30}$ cm^2 in the DOS N_2 and kept the previously used value $\sigma_n = 1\times10^{-17}$ cm^2 in N_1. The green *C-T* curve for this case is presented in Fig.3.17.

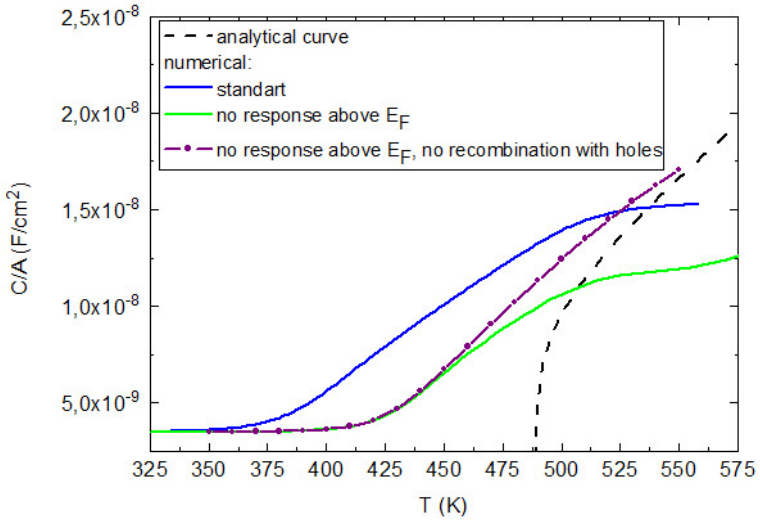

Fig.3.17. Capacitance-temperature curves at f=400 Hz deduced from analytical and numerical calculation. We introduced two constant DOS distributions: N_1 between 0 and 1.55 eV from E_V and N_2 between 1.55 and 1.75 eV from E_V, both DOS values being equal to 1×10^{16} $cm^{-3}eV^{-1}$. The bulk Fermi level was fixed at E_C–E_F=0.7 eV. Different capture cross-sections of the defects in the gap are considered (see text).

The suppression of the exchange of the states above the Fermi level influence significantly the *C-T* dependency. The turn-on temperature has shifted to higher temperatures.

Thus we may conclude that the previously deduced T_0 was due to response of the states above the Fermi level (or with an abscissa smaller than x_ω). It proves that the sharp cut-off approximation should be considered carefully and is no longer applicable at high temperatures. The purple curve in Fig.3.16 shows the case where the possible recombination of electron with holes is avoided by introducing very low value of the capture cross section of holes at $\sigma_p = 1\times10^{-30}$ cm^2 in N_1 distribution. As it was already shown in Section 3.2.1.1.b holes can reduce the amount of electrons capable of undergoing the capture-release processes and therefore decrease the capacitance. For the case of E_C–E_F=0.7 eV the influence of holes is even more significant since at the interface of the barrier the Fermi level is closer to the valence band than to the conduction band.

3.2.1.2 Non constant DOS distributions

In order to assess the reliability of the proposed treatment (Eq.(3.35)) for the case of more complicated gap states distributions, the cases of either exponential or Gaussian distributions were studied.

3.2.1.2.a Exponential conduction band tail DOS

The exponential conduction band tail (CbT) is defined by:

$$N(E)_{CbT} = N(E_C)\exp\left(-\frac{E_C - E}{k_B T_C}\right) \tag{3.41}$$

where T_C is the characteristic temperature that defines the slope of the tail, $N(E_C)$ is the density of states at the conduction band edge.

In order to study the influence of the shape of the exponential band tail on the *C-T* dependencies three different cases were considered. For all these structures the Fermi level was fixed at E_C-E_F = 0.2 eV (at T = 100 K) and the DOS at the Fermi level was kept equal to $N(E_F) = 1\times10^{19}$ cm^{-3}eV^{-1} by adjusting the value of $N(E_C)$. We varied the slope of the band tail by changing the characteristic temperature T_C. so that the parameter k_BT_C took the following values: 0.04, 0.09 and 0.13 eV. The *C-T* curves are shown in Fig.3.18.

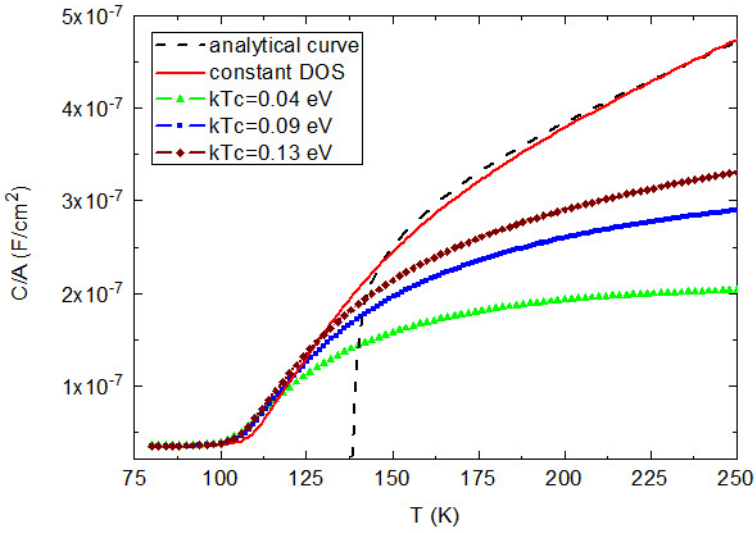

Fig.3.18. Capacitance-temperature curves at f=400 Hz deduced from analytical and numerical calculation, The introduced DOS is constant (red) or the exponential conduction band tail DOS (Eq.42) with fixed $N(E_F)=1\times10^{19}cm^{-3}eV^{-1}$ and different values of T_C. The bulk Fermi level is fixed at $E_C–E_F=0.2$ eV.

One can see that for all values of T_C the curves are shifted to the lower temperatures when compared to the analytically obtained one. But the more important feature is the significant difference in the slopes that affects the treatment curves and eventually the deduced parameters. Indeed, the obtained turn-on temperatures are around 20 K lower than that the ones predicted by theory and obtained for the constant DOS case.

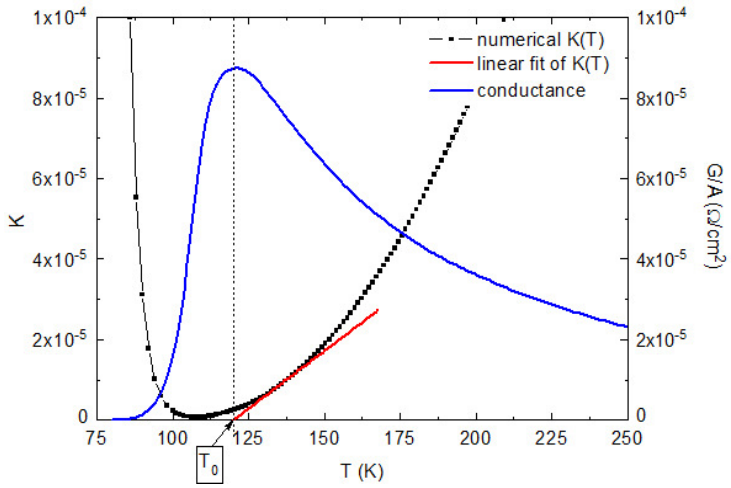

Fig.3.19. The linear fit of K(T) from T_0 derived from conductance-temperature curve. The exponential conduction band tail DOS with fixed $N(E_F)=1\times10^{19}cm^{-3}eV^{-1}$ and $k_BT_C=0.04$ eV. The bulk Fermi level is fixed at $E_C–E_F=0.2$ eV.

The linear fit of the *K-T* curves is troublesome since the dependencies are curved and do not experience a well-defined linear region. Therefore in order to define the region to be fitted the T_0 was first obtained from the maximum of the conductance-temperature (*G-T*) dependence. The *G-T* plot experiences a well defined pick at T_0 and the latter can be defined clearly. The part of the *K-T* curve for the linear fit was then chosen to obtain at the intersection with the abscissa axis the value of T_0 found from the *G-T* curve (see Fig.3.19).

The considerable shift of T_0 to lower temperatures can be explained the following way. As it was introduced in the theoretical development section, the turn-on temperature is a temperature at which the states at the Fermi level start to follow the ac modulation at a given frequency. It is assumed that no states above the Fermi level can respond to the signal. In the case of the conduction band tail, this sharp cut-off approach is no longer applicable. There always exist states above the Fermi level that contain electrons capable to undergo capture-release processes. These states start to follow the ac modulation at lower temperatures than the predicted T_0 that corresponds to the response of states at the Fermi level. However their contribution in the overall capacitance can be almost neglected for the case of constant DOS. On the contrary, with the exponential conduction band tail the states above the Fermi level are characterized by considerably higher density of states. Therefore their contribution becomes significant and should be taken into account.

The difference in the slopes can be explained by following the same reasoning. The higher is the temperature, the deeper lie gap states that can follow the ac signal with their DOS being considerably lower than that at the Fermi level. However for different T_C values the DOS of the states below the Fermi level is not the same. For k_BT_C = 0.04 eV the DOS of the states lying deep in the gap is negligible and few states below the Fermi level contribute to the capacitance signal. Thus the saturation of the capacitance takes place at low temperatures. The increase of the capacitance for the case of k_BT_C = 0.09 eV and 0.13 eV is more significant since the states below the Fermi level involved in the capture-release processes are characterized by larger density of states. The larger the value of k_BT_C is, the closer the *C-T* curve is to the case of the constant DOS.

The main parameters derived from the treatment procedure are presented in Table 3.3.

k_BT_C (eV)		T_0 at 400 Hz (K)	$N(E_F)$ ($cm^{-3}eV^{-1}$)	E_C-E_F (eV)	ν_n (s^{-1})
	analytical	140	1×10^{19}	0.20	2×10^{10}
0.04	introduced into a model	-	1×10^{19}	0.20	2×10^{10}
	reconstructed from *K-T* treatment	116	$1.5\text{-}1.7\times10^{18}$	0.20-0.22	$2\text{-}3\times10^{12}$
0.09	introduced into a model	-	1×10^{19}	0.20	2×10^{10}
	reconstructed from *K-T* treatment	120	$2.0\text{-}2.3\times10^{18}$	0.19-0.21	$2\text{-}3\times10^{12}$
0.13	introduced into a model	-	1×10^{19}	0.20	2×10^{10}
	reconstructed from *K-T* treatment	120	$2.5\text{-}2.9\times10^{18}$	0.19-0.21	$0.9\text{-}1\times10^{12}$

Table 3.3. Comparison of the parameters introduced in the numerical calculation with those derived from the simplified treatment of C–T–f curves for the exponential band tail DOS with different values of T_C. Analytically obtained T_0 value from Eq.(25) without any consideration of the DOS shape is presented as well.

Although the DOS at the Fermi level is underestimated for all values of k_BT_C, it is noteworthy that the results are dependent on the slope of the conduction band tail. The case of k_BT_C = 0.13 eV shows the closest values of $N(E_F)$ and ν_n to the introduced ones. Again, it can be explained from the slope of the band tail. The steeper the slope is, the less the DOS resembles the case of constant DOS, for which the treatment of *K-T* works the best as illustrated in Fig.3.20. Following this reasoning we find the best agreement with the introduced values for the case of k_BT_C = 0.13 eV.

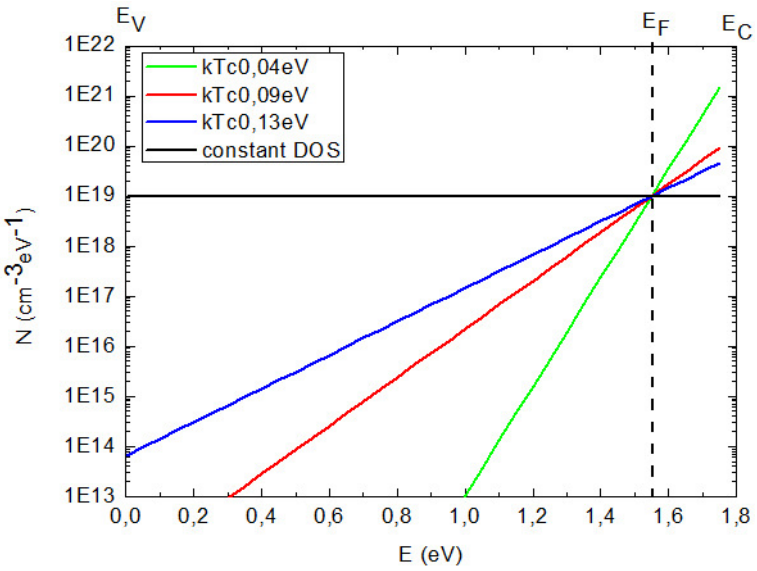

Fig.3.20. Comparison of exponential DOS for different values of the characteristic temperature T_C with the constant DOS.

3.2.1.2.b Gaussian DOS distribution

We have performed similar analysis as the one presented before for a Gaussian distribution is introduced for the DOS. Such a distribution can be expressed by:

$$N(E) = N_{0m} \exp\left(\frac{-(E - E_{mGauss})^2}{2w_{Gauss}^2}\right) \tag{3.42}$$

where N_{0m} is the maximum of the Gaussian distribution at the energy E_{mGauss} referred to the valence band edge, and w_{Gauss} is the width of the Gaussian distribution.

Here we would like to underline that Gaussian distribution is of particular interest since the deep states DOS are generally described by Gaussians as it was mentioned in Chapter 1. Since in a-Si:H typical deep defects are dangling bonds it was shown in Ref.[10] that they can be represented by two Gaussian distributions separated by a correlation energy.

Two cases were examined in order to compare the influence of the curvature of the Gaussians around the Fermi level, as shown in Fig.3.21.

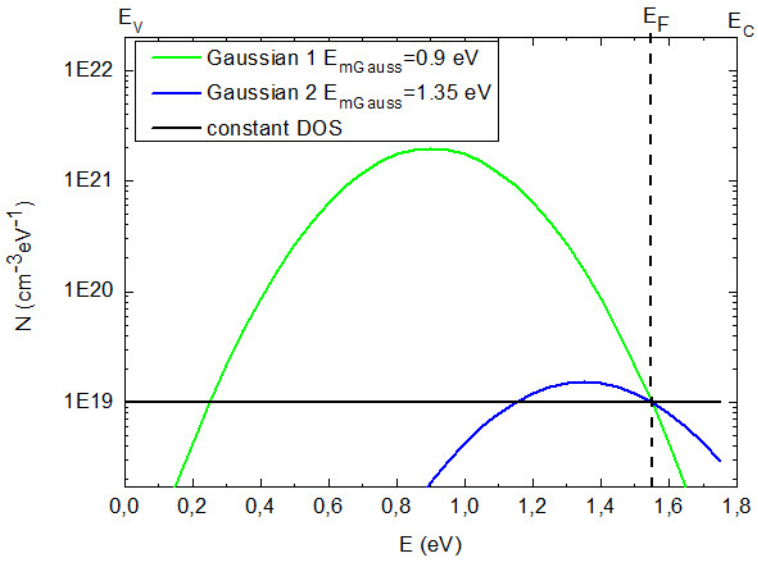

Fig.3.21. Comparison of the Gaussian DOS distributions introduced in simulations.

The *C-T* curves of the two studied Gaussian DOS distributions differ considerably, as it is shown in Fig.3.22. The capacitance corresponding to Gaussian 1, that is characterized by the important change of *N(E)* in the vicinity of the Fermi level, increases dramatically with the temperature with a slightly higher T_0 in comparison with the *C-T* curve corresponding to the other Gaussian distribution.

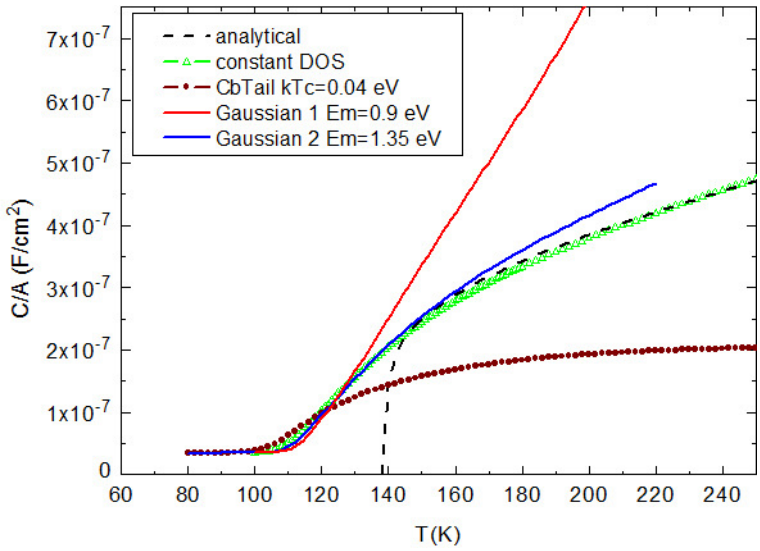

Fig.3.22. Capacitance-temperature curves at f=400 Hz deduced from analytical and numerical calculations for different shapes of the DOS. The DOS at the Fermi level is fixed at $N(E_F)=1\times10^{19}cm^{-3}eV^{-1}$, $E_C–E_F=0.2$ *eV (100 K).*

One should notice that the capacitance signal corresponding to both Gaussian DOS distributions starts to increase at the same temperatures as the one corresponding to the

constant DOS distributions. Consequently T_0 is expected to be close to the one predicted by analytical derivation.

The main derived parameters are listed in Table 3.4.

		T_0 at 400 Hz *(K)*	$N(E_F)$ ($cm^{-3}eV^{-1}$)	E_C-E_F (eV)	ν_n (s^{-1})
analytical		140	1×10^{19}	0.20	2×10^{10}
introduced into the model		-	1×10^{19}	0.20	2×10^{10}
reconstructed from *K(T)* treatment	Gaussian 1 E_{mGauss} = 0.9 eV	136	$5.9\text{-}6.3\times10^{18}$	0.21-0.22	$5.6\text{-}8.0\times10^{11}$
	Gaussian 2 E_{mGauss} = 1.35 eV	135	$5.0\text{-}5.5\times10^{18}$	0.21-0.22	$0.8\text{-}2.0\times10^{12}$

Table 3.4. Comparison of the parameters introduced in the numerical calculation with those derived from the simplified treatment of C–T–f curves for the two Gaussian DOS distributions. Analytically obtained T_0 value from Eq.(25) without any consideration of the DOS shape is presented as well.

The increase of T_0 in comparison with the exponential DOS distributions can be again explained within the sharp cut-off approximation. In the case of Gaussian distributions the DOS of the states above the Fermi level is significantly lower than that of the states lying deeper in the gap. And since considerable response to the ac modulation comes from the states with the higher *N(E)*, one can expect the onset of response from the states below the Fermi level at a higher T_0 than in the case of the exponential conduction band tail or constant DOS. This reasoning is confirmed by the values of the activation energy which are slightly higher than the introduced one. The treatment of *K-T* data is complicated by the non linear shape of the curves as well as in the case of the exponential band tail DOS. Again T_0 was first defined from the maximum of conductance-temperature curve as it is shown in Fig.3.23(a) and 3.23(b).

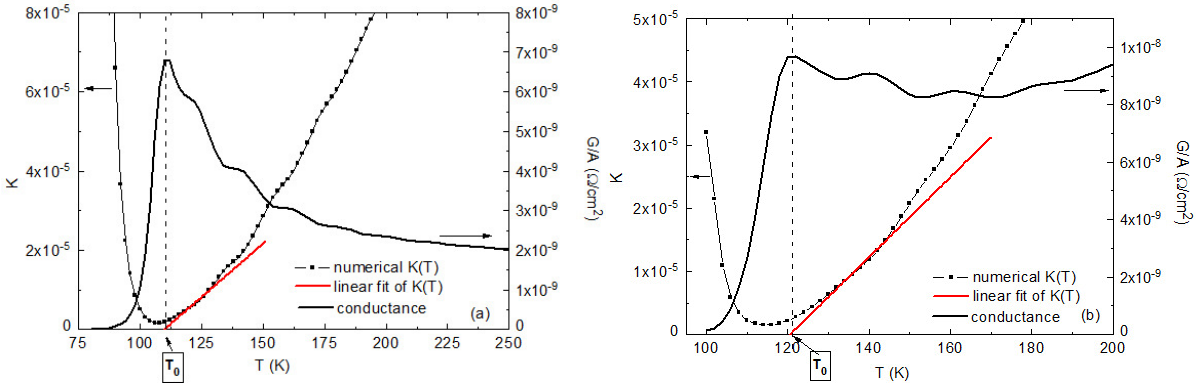

Fig.3.23. The linear fit of K(T) from T_0 derived from conductance-temperature curve at f=100 Hz. (a) Gaussian 1 DOS distribution E_{mGauss} =0.9 eV and (b) Gaussian 2 DOS distribution E_{mGauss} = 1.35 eV with fixed $N(E_F)=1\times10^{19}cm^{-3}eV^{-1}$. The bulk Fermi level is fixed at $E_C–E_F$= 0.2 eV.

The treatment yields again underestimated values for $N(E_F)$ and significantly overestimated attempt-to-escape frequency.

3.2.2 Capture cross section and mobility influence on capacitance-temperature dependencies

As it was mentioned at the beginning of Section 3.2 the capture-release processes are not restricted by the charge transport if the dielectric relaxation time is significantly smaller than the characteristic release time (Eq.3.38). In this section we address the validity of this condition and possible influence of capture cross-section and mobility on *C-T* and *K-T* dependencies.

Capture cross section's influence can be estimated from the definition of the attempt-to-escape frequency given in (Eq.3.20). For this purpose we introduced the structure already considered above. We fixed the Fermi level at 0.2 eV from the conduction band edge at 100 K and introduced the constant density of states with $N(E_F) = 1\times10^{19}cm^{-3}eV^{-1}$. Keeping the electron mobility constant at μ_n=10 $cm^2V^{-1}s^{-1}$ we varied the electron capture cross-section from $\sigma_n=8\times10^{-14}cm^2$ to $\sigma_n=1\times10^{-20}cm^2$.

The influence of this parameter on the numerically modeled *C-T* dependencies is presented in Fig.3.24.

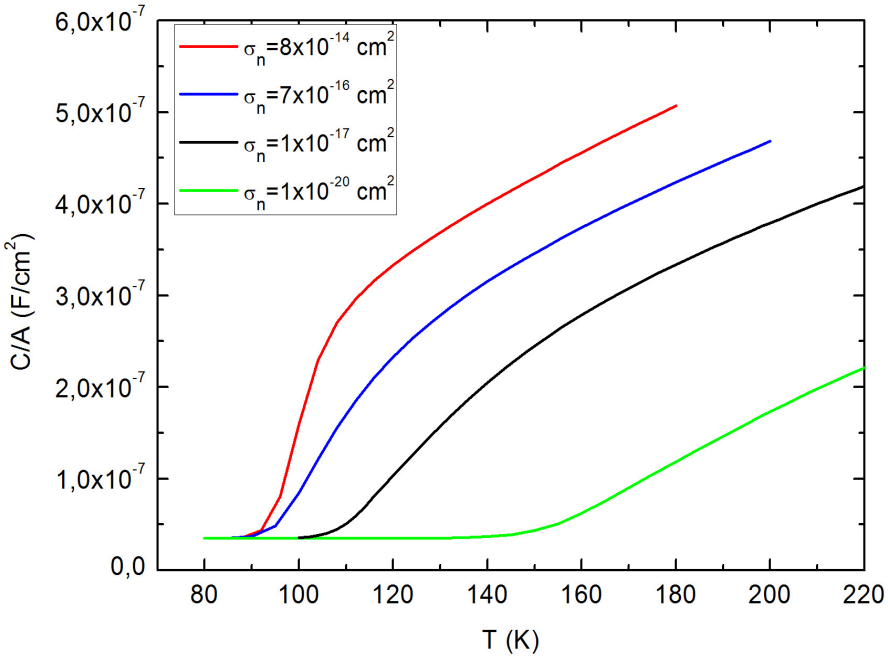

Fig.3.24. Capacitance-temperature curves at f=3200 Hz obtained from numerical calculation for different values of electron capture cross section σ_n. The constant DOS is introduced with $N(E_F)=1\times10^{19}cm^{-3}eV^{-1}$, $E_C–E_F=0.2$ eV.

According to the theoretical analysis the increase of capture cross section for electrons, σ_n, results in a consecutive shift of the turn-on temperature to lower temperatures. With increase of the capture cross section, more electrons are involved into capture-release processes at a given temperature and frequency. This tendency is also observed from numerical simulations. However, when reaching high values of σ_n the turn-on temperature varies less as it can be seen in Fig.3.25.

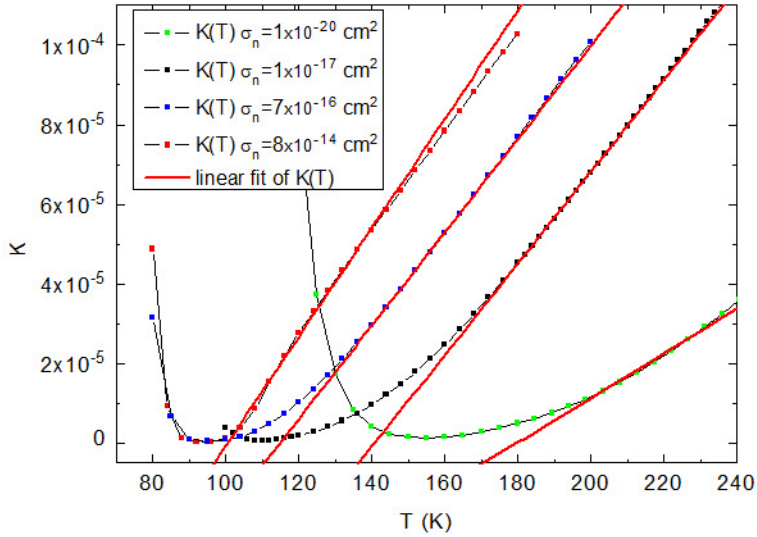

Fig.3.25. The linear fit of K-T data for different values of electron capture cross section σ_n. The constant DOS is introduced with $N(E_F)=1\times10^{19}cm^{-3}eV^{-1}$, $E_C–E_F=0.2$ eV.

In order to meet the condition $\tau_{c-r}/\tau_{dr} >> 1$, the electron capture cross section should be smaller than the limit value obtained as follows:

$$\sigma_n << \frac{q\mu_n}{2\varepsilon v_{th}} = \frac{1.6\times10^{-19}\cdot10}{2\cdot10^{-12}\cdot10^{7}} = 8\times10^{-14}\text{cm}^2 \tag{3.43}$$

For the highest values of σ_n the characteristic time of capture-release processes is comparable with that of transport of electrons. Therefore there are two competing processes with similar characteristic time that makes deduction of the turn-on temperature of response to ac signal no longer reliable. This is illustrated in Fig.3.24 and 3.25. One can see that the capacitance for the case of $\sigma_n = 8\times10^{-14}$ cm^2 increases sharply and deduced T_0 lies close to that of $\sigma_n = 7\times10^{-16}$ cm^2. Increasing the capture cross section to $\sigma_n = 8\times10^{-14}$ cm^2 leads to the pinning of T_0 and this calculated value is no longer equal to the theoretical one. The turn-on temperature does not follow the analytical prediction since the onset of the capacitance signal is now defined by the transport phenomena. The *C-T* and *K-T* curves for the case of the lowest value of $\sigma_n = 1\times10^{-20}$ cm^2 differ considerably from the other cases studied. The $N(E_F)$ value (the slope of the linear fit of *K-T* data) is significantly smaller than it was introduced into simulations. The obtained turn-on temperature is shifted to the lower temperatures in comparison with the theoretical value. The case of $\sigma_n = 1\times10^{-20}$ cm^2 reproduces the tendencies observed already for the case of undoped a-Si:H: shift of T_0 and underestimation of $N(E_F)$. Again it can be explained by the unreliability of the considered assumptions at higher temperatures. The calculated and analytical values of the turn-on temperature for different capture cross-sections are presented in Table 3.5.

σ_n (cm^2)	analytical T_0 (K)	numerical T_0 (K)
1×10^{-20}	240	174
1×10^{-17}	140	140
7×10^{-16}	111	113
8×10^{-14}	91	100

Table 3.5. Turn-on temperatures derived analytically and numerically from K-T dependencies for different values of the electron capture cross-section σ_n.

Another example of the influence of the transport phenomena on the capacitance-temperature curves is presented in Fig.3.26. Different values of the electron mobility are considered with a fixed capture cross section $\sigma_n = 7\times10^{-16}$ cm^2.

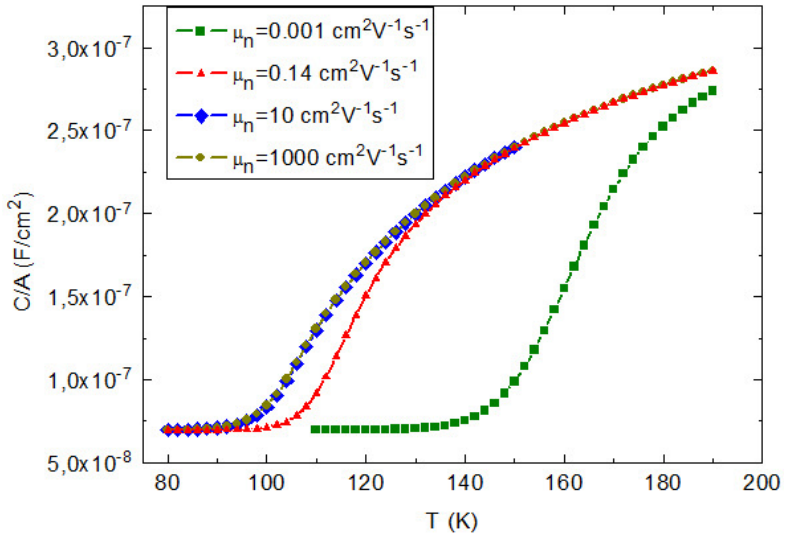

Fig.3.26. Capacitance-temperature curves at f=3200 Hz obtained from numerical calculation for different values of electron mobility μ_n. The constant DOS is introduced with $N(E_F)=1\times10^{19}cm^{-3}eV^{-1}$, $E_C–E_F=0.2$ eV.

One can see that for low values of the electron mobility, T_0 is significantly shifted towards high temperatures. This can be interpreted as follows: with the low mobility the transport of electrons is slower than the response of the states to the ac modulation and the turn-on temperature becomes linked to the onset of the transport. In order to prove this reasoning we calculate the turn-on temperature (T_{0dr}) related to transport (for f = 3200 Hz) according to the following expression providing that the time of capture-release is low enough:

$$\tau_{dr}\omega = 1 \tag{3.44}$$

$$\frac{\varepsilon}{qN_C \exp\left(-\frac{E_C - E_F}{k_B T_{0dr}}\right)\mu_n}\omega = 1 \tag{3.45}$$

The analytically obtained values of T_{0dr} are then compared with the numerically calculated ones. The numerical turn-on temperatures are derived from the maximum of conductance-temperature (*G-T*) dependencies. The results are presented in Table 3.6.

μ_n ($cm^2V^{-1}s^{-1}$)	numerical T_0 (K)	analytical T_{0rd} (K)
0.001	163	162
0.14	116	121
10	107	99
1000	107	83

Table 3.6. Turn-on temperatures derived analytically (Eq.(3.45)) and numerically from the maximum of G-T dependencies for different values of the electron mobility μ_n.

Indeed, high T_0 values for μ_n=0.001 $cm^2V^{-1}s^{-1}$ and μ_n=0.14 $cm^2V^{-1}s^{-1}$are related to the slow transport and this phenomenon defines the onset of the capacitance signal. For higher values of the mobility we find that T_0 is higher than the critical value of T_{0rd} and hence is limited by another process since the transport of charge is fast. Thus the *C-T* dependencies coincide for mobilities higher than 10 $cm^2V^{-1}s^{-1}$ (typical value of μ_n in a-Si:H).

From the results above we conclude that the onset of the capacitance signal is defined by the slowest process: transport of majority carriers or capture-release process. In order to derive the information of the DOS at the Fermi level from the capacitance data, it is necessary that the capture-release process defines the turn-on temperature.

Previous obsevations showed that attempt-to-escape frequency and consequently apparent capture cross section values derived from the treatment of numerically obtained *C-T* data are significantly overestimated if one compares with true values introduced into simulations: $\sigma_n^{app} > \sigma_n$. Considering this we rewrite Eq.(3.40) using the apparent capture cross section σ_n^{app} that is obtained from the treatment:

$$\frac{\tau_{c-r}{}^{app}}{\tau_{dr}} = \frac{1/2v_{th}\sigma_n{}^{app}N_C\exp\left(-\frac{E_C-E_F}{kT}\right)}{\varepsilon/qN_C\exp\left(-\frac{E_C-E_F}{kT}\right)\mu_n} = \frac{q\mu_n}{2\varepsilon v_{th}\sigma_n{}^{app}} >> 1 \qquad (3.46)$$

From Eq.(3.46) one can see that the apparent release time $\tau_{c\text{-}r}{}^{app}$ is underestimated thus giving the limit value of $\sigma_n{}^{app} = 8\times10^{-14}$ cm^2 that is reached at smaller values of the introduced into simulation true values of the capture cross section. This overestimation of the capture cross section results in the transport limitation at lower true values of σ_n. This is observed for the limit case of $\sigma_n = 8\times10^{-14}$ cm^2. For this introduced true value of the capture cross section $\sigma_n{}^{app}$ is larger and thus the condition of Eq.(3.46) is no longer satisfied. As the result the turn-on temperature is entirely defined by the transport phenomena.

In order to understand whether transport of charge influence the onset of capacitance signal simulations have to be performed in order to derive apparent capture cross section value and verify is the the condition of Eq.(3.46) is met. For typical values of the electron capture cross sectiona nd mobility parameters in a-Si:H (μ_n = 10 cm^{2}V^{-1}s^{-1}, σ_n =7×10^{-16} cm^2) that were introduced in simulation in Section 3.2.1 this condition is fulfilled for low turn-on temperatures. However, for the case of E_C-E_F = 0.7 eV where overestimation of ν_n is more drastic one should expect the contribution of transport to the onset of capacitance even at low introduced values of σ_n.

3.3 Experimental results. Comparison with modeling

One of the main objectives of the study presented in Section 3.2 is to assess the reliability of the treatment of *C-T* data in order to derive important information on a structure: $N(E_F)$, E_a, ν_n. In this Section we focus on the application of the *K-T* treatment on the experimentally obtained *C-T* dependencies.

3.3.1 The simplified *K-T* treatment of the experimental *C-T* data

The capacitance-temperature measurements at different frequencies were carried out on a set of a-Si:H Schottky diodes. The samples were fabricated by rf-PECVD deposition of 5μm thick a-Si:H layer on chromium covered glass substrate with platinum circular dots evaporated on the top. Furthermore, to investigate the transport and defect-related properties of the samples, two parallel aluminium electrodes (with 1 or 2 mm) gap have been deposited

on the part of the samples from the same set. Among the characterisation techniques that were performed on a-Si:H and hydrogenated polymorphous silicon (pm-Si:H) samples are dark conductivity, photoconductivity, steady-state photocarrier grating, modulated photocurrent (MPC) and constant photocurrent (CPM) measurements [11-15].

The capacitance temperature measurements were performed with an Agilent E4981A capacimeter that operates in small-signal mode at varied frequencies. The samples were placed in a nitrogen-filled vessel that is pumped to reach the vacuum of 10^{-5} mbar. The temperature was varied in the range 77 K-320 K. During the measurements samples were kept in the dark in order to avoid the photogeneration of the carriers. The obtained *C-T* dependencies are presented in Fig.3.27.

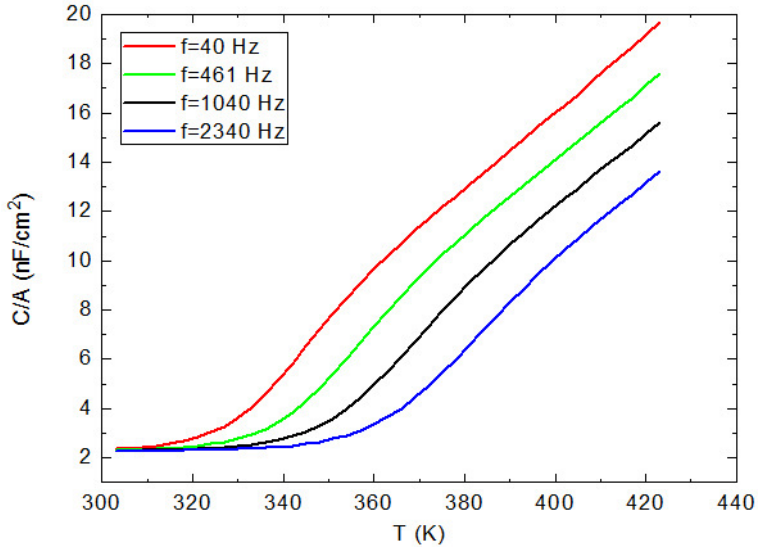

Fig.3.27. Experimentally obtained capacitance-temperature dependencies on a a-Si:H Schottky diode at different frequencies.

For all frequencies the *K-T* treatment was performed and $N(E_F)$, T_0 values were obtained. The *K-T* curves are shown in Fig.3.28.

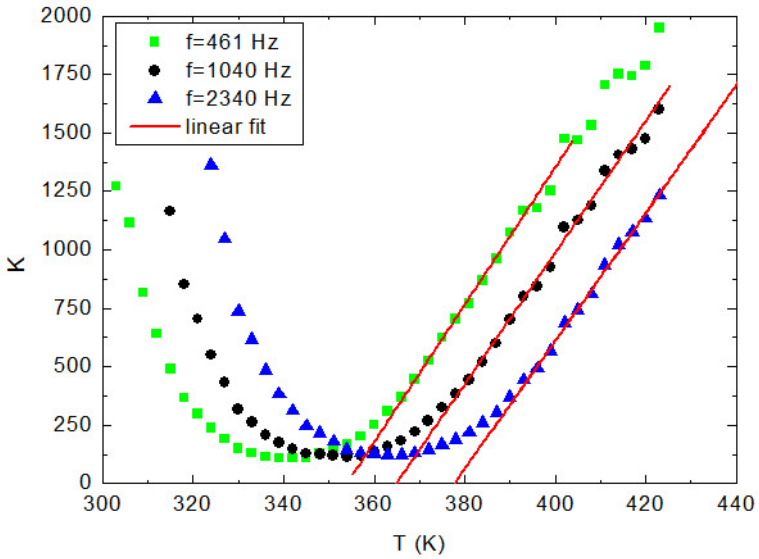

Fig.3.28. K-T curves obtained from the treatment of the experimental data shown in Fig.27.

The $N(E_F)$ was found to be equal to $5.4\times10^{15}cm^{-3}eV^{-1}$. The Arrhenius plot yielded the values of the activation energy at 0.77 eV and the attempt-to-escape frequency $\nu_n = 1.5\times10^{14}s^{-1}$.

Now we put the derived above parameters into numerical simulations in order to reproduce the experimental capacitance curves. Since we have no exact information on the shape of the DOS we introduced the simplest case of a constant distribution all over the band gap: $N(E) = N(E_F) = 5.4\times10^{15}cm^{-3}eV^{-1}$. The Fermi level was fixed at 0.77 eV from E_C at 300 K and the capture cross section of electrons calculated from the attempt-to-escape frequency was taken equal to $7.5\times10^{-14}cm^2$. The band gap was taken equal to 1.75 eV and the layer's thickness was 5 μm. All other parameters characterizing the material were kept the same as they had been introduced before in Section 3.2. This set of parameters we assigne as "simulation 1". The calculated and the experimental *C-T* curves at $f = 461$ Hz are presented in Fig.3.29.

It can be seen that the calculated capacitance curve is shifted to high temperatures in comparison with the experimental one and the curvature is not reproduced well enough. In our previous study we observed that in the case of undoped a-Si:H with $E_C–E_F = 0.7$ eV the DOS at the Fermi level derived from the treatment was underestimated and the attempt-to-escape frequency was largely overestimated. Slight error can arise in the determination of the activation energy as well. Also it was shown that for this range of turn-on temperatures the onset of capacitance signal can be limited by transpost of charge. In the case of the "simulation 1" we observe the transport limitation since the turn-on temperature is shifted to the higher temperatures, although it was observed previously that one may expect the shift of the numerical curves to the lower temperatures. The introduced into simulation value of the

attemp-to-escape frequency results in overestimation of the apparent capture cross section and the apparent release time from Eq.(3.46) is smaller than the dielectric reponse time.

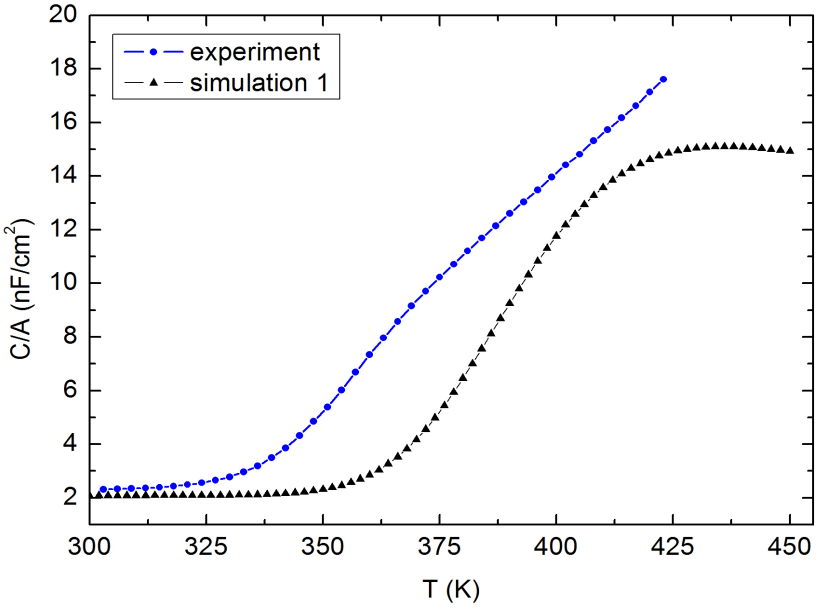

Fig.3.29. Capacitance-temperature curves at f = 461 Hz obtained experimentally and numerically with the parameters derived from the treatment of the experimental data.

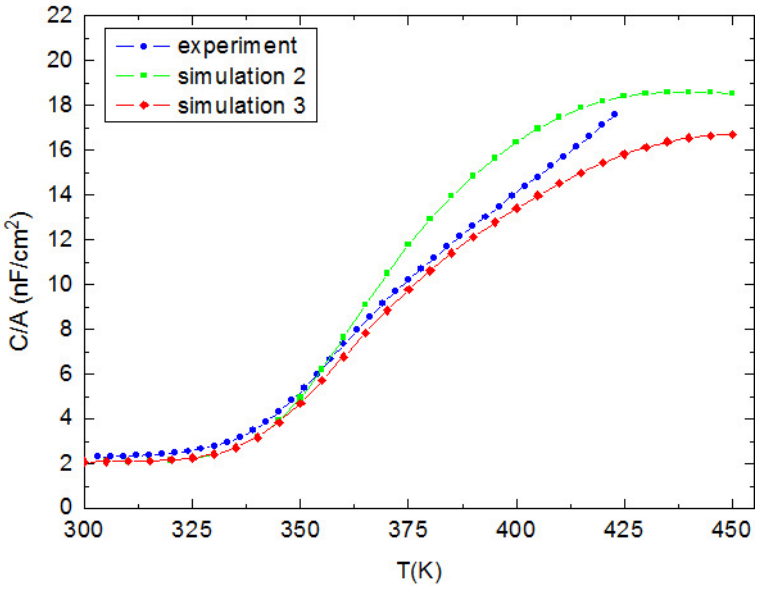

Fig.3.30. Capacitance-temperature curves at f = 461 Hz obtained experimentally and numerically. The parameters of "simulation 2" and "simulation 3" are given in Table 7.

Considering this, the next step was to diminish the activation energy in order to shift the *C-T* curve to lower temperatures and to diminish the overestimation of the apparent capture

cross section while keeping all parameters unchanged. The activation energy was introduced at 0.72 and the resulting *C-T* curve ("simulation 2") is shown in Fig.3.30.

As one can see a satisfactory shift of the capacitance curve is obtained when changing the activation energy to the value of 0.72 eV. In order to adjust the shape of the *C-T* curve we test a smaller value of the capture cross section of electrons knowing that the ν_n obtained from the treatment provides a strong overestimation of σ_n. In the set of parameters called "simulation 3" σ_n was taken equal to 1×10^{-14}cm^2, E_a was kept at 0.72 eV and other parameters remained the same. The corresponding *C-T* curve ("simulation 3") is shown in Fig. 3.30 as well. The last calculation provides a good initial approximation of the experimental data. However, for better reproduction we lack of the information about the studied sample, namely on the DOS distribution. Parameters introduced in simulations (1), (2) and (3) are summarized in Table 3.7.

Parameter	Simulation 1	Simulation 2	Simulation 3
E_a (eV)	0.77	0.72	0.72
$N(E_F)$ (cm^{-3}eV^{-1})	5.4×10^{15}	5.4×10^{15}	5.4×10^{15}
σ_n (cm^2)	7.5×10^{-14}	7.5×10^{-14}	1×10^{-14}

Table 3.7. Parameters of the constant DOS introduced in the simulations in order to reproduce the experimentally obtained C-T data.

3.3.2 Fitting of the experimental *C-T* data with the DOS distribution obtained from other techniques

In order to obtain more information on the sample one should address other characterization techniques. In Fig. 3.31 we show the density of states obtained from the combination of several techniques. The part of the DOS above the Fermi level was reconstructed from modulated photocurrent data (MPC) [11]. The sub-gap absorption which gives information on the valence band tail and deep defects below the Fermi level was deduced from either the constant photocurrent method (CPM) or the photothermal deflection spectroscopy, the data being calibrated with optical transmission measurements. The details of these measurements are given in the reference [16].

The DOS and the values of capture cross sections of deep states deduced from combination of the measurements and numerical modeling are presented in Fig. 3.31. The DOS was adjusted by the means of numerical modeling in order to obtain good reproduction of the experimental results of the MPC, CPM, SSPG (steady-state photocarrier grating) and

SSPC (steady-state-photoconductivity) techniques.

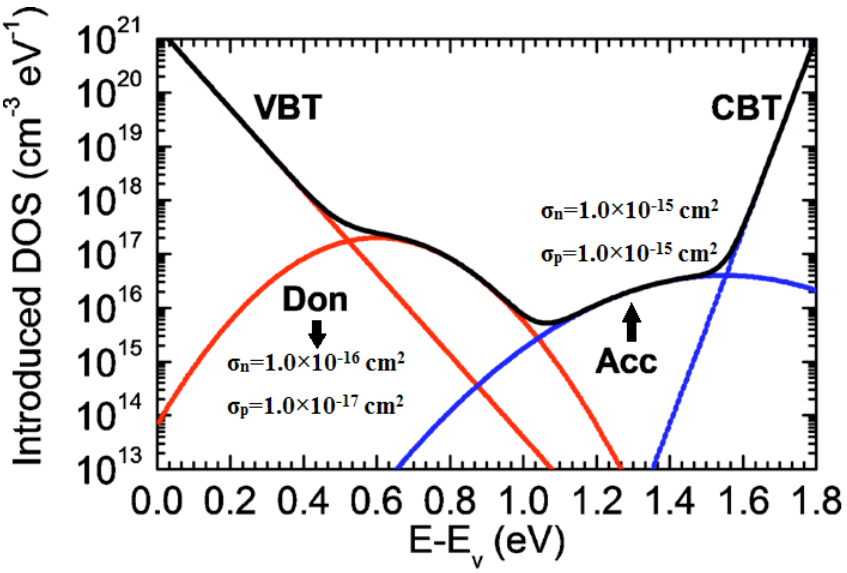

Fig.3.31. DOS deduced from photocurrent measurements (SSPC, MPC, CPM, SSPG) on an undoped device grade a-Si:H sample. The electron capture cross sections for the deep states are also indicated.

This DOS (that we shall call "initial DOS") and the corresponding parameters were then introduced for the numerical calculation of the capacitance. The resulting *C-T* dependency together with the experimental one is shown in Fig.3.32.

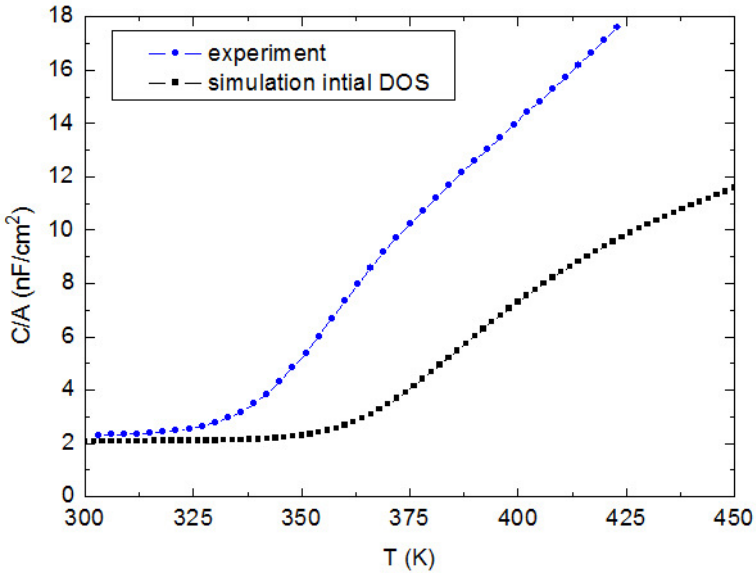

Fig.3.32. Capacitance-temperature curves at f = 461 Hz obtained experimentally and numerically with the DOS distribution obtained from MPC and other techniques shown in Fig.3.31.

As in the case of the constant DOS the calculated *C-T* curve is shifted to high temperatures due to the value of the activation energy that is fixed at 0.77 eV resulting from the introduced DOS and zero doping. Keeping the doping level at zero, we adjust the initial DOS in order to provide a good fit to the experimental *C-T* curves for all frequencies. A significant number of simulation runs have been performed, changing step by step the introduced DOS parameters until a good reproduction of the experimental capacitance data was obtained. The results of the best fit are shown in Fig.3.32.

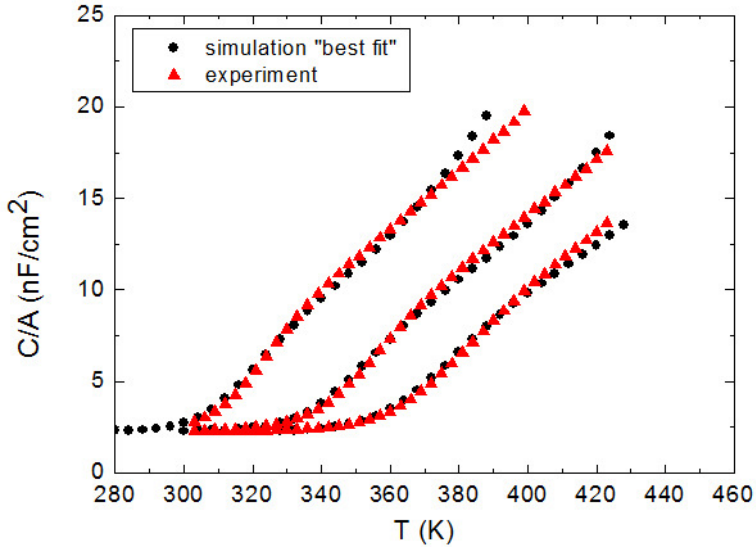

Fig.3.33. The capacitance-temperature curves obtained experimentally and numerically with the "best fit" DOS distribution described by the set of parameters given in Table 8 for three frequencies: f =40 Hz, 461 Hz and 2340 Hz.

The best reproduction of the experimental data was achieved by modifying parameters of the acceptor Gaussian distribution: a slightly reduced apmlitude (from 4.0×10^{16} to 2.0×10^{16} cm^{-3} eV^{-1}) and an increased value of the electron capture cross section (from 1.0×10^{-15} to 6.0×10^{-15} cm^2). The main parameters of the initial and "best fit" DOS distributions are summarized in Table 3.8.

	T_C (K)	T_V (K)	N_{0m} (cm^{-3} eV^{-1})	E_C-E_m (eV)	w (eV)	σ_n (cm^2)	σ_p (cm^2)
Both distributions							
CBT	280					1.0×10^{-15}	1.0×10^{-15}
VBT		660				2.5×10^{-16}	1.0×10^{-17}
Initial DOS E_g=1.8 eV, μ_n=10 cm^2s^{-1}, μ_p=1 cm^2s^{-1}							
Acc			4.0×10^{16}	0.25	0.22	1.0×10^{-15}	1.0×10^{-15}
Don			2.0×10^{17}	1.20	0.15	1.0×10^{-16}	1.0×10^{-17}
"Best fit" DOS E_g=1.75 eV, μ_n=10 cm^2s^{-1}, μ_p=1 cm^2s^{-1}							
Acc			2.0×10^{16}	0.25	0.22	6.0×10^{-15}	1.0×10^{-15}
Don			2.0×10^{17}	1.15	0.15	6.0×10^{-16}	1.0×10^{-17}

Table 3.8. Parameters of the DOS distributions: initial and "best fit" introduced in the simulations. The deep states Gaussian distributions are indicated by "Don" for donor-type states and "Acc" for acceptor-type states. The conduction and valence band-tails (CBT and VBT) are taken unchanged for both distributions.

When comparing the difference between initial and "best fit" DOS one should keep in mind that MPC measurements do not provide exact values of $N(E)$ or σ_n. Namely, MPC technique is sensitive to the term $\sigma_n N/\mu$. Therefore this term can be distributed in various ways according to the fitting procedure and the experimental curves that are to be reproduced. From the initial DOS adjusted to fit the MPC results we have $\sigma_n N/\mu$=4 cm^{-3} $eV^{-1}s^{-1}$. The "best fit" DOS gives $\sigma_n N/\mu$=12 cm^{-3} $eV^{-1}s^{-1}$. This value, although being larger than that obtained from the experiment, still lies within reasonable range.

Now since all parameters of the system are known, the interest is to compare the results of the *K-T* treatment with the values introduced into the simulations. The *K-T* curves of the experimental data and of numerically calculated *C-T* dependencies from the "best fit" DOS are shown in Fig.3.34. The analytical *K-T* data are very close to the experimental curves but slightly lower values of $N(E_F)$ are deduced. However this small variation is negligible if one considers the error of the linear approximation of the *K-T* data and the uncertainty arising from the choice of the region to be fitted. The introduced and reconstructed from the treatment parameters are presented in Table 3.9.

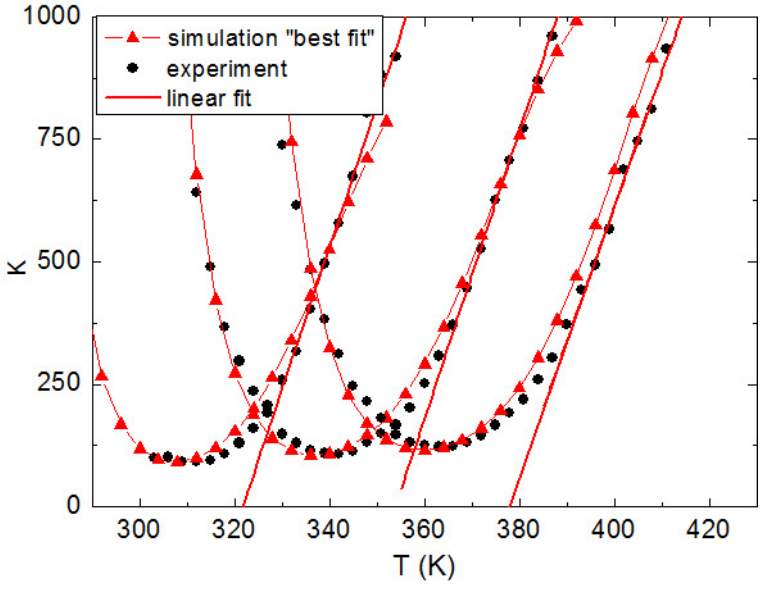

Fig.3.34. K-T treatment curves of C-T data from Fig.32 for three frequencies: f=40 Hz, 461 Hz and 2340 Hz.

		$N(E_F)$ ($cm^{-3}eV^{-1}$)	E_C-E_F (eV)	ν_n (s^{-1})
undoped a-Si:H	introduced "simulation 3" DOS	5.4×10^{15}	0.72	2×10^{13}
	introduced "best fit" DOS	5.3×10^{15}	0.72	1.2×10^{13}
	reconstructed experiment	$4.7\text{-}5.5\times10^{15}$	0.76-0.79	$1.0\text{-}4.0\times10^{14}$
	reconstructed "best fit" simulation	$3.0\text{-}4.6\times10^{15}$	0.72-0.74	$2.0\text{-}5.0\times10^{13}$

Table 3.9. Comparison of the parameters introduced in the numerical calculation from "best fit" and "simulation 3" DOS distributions with those derived from the simplified treatment of the experimental data and C-T results from calculation of "best fit" DOS.

The introduced DOS at the Fermi level is in good agreement with the one derived from the treatment of the experimental data. Overall the parameters introduced in simulations reproduce well the values obtained from the treatment of the experimental *C-T* data. Except for the attempt-to-escape frequency which value is again overestimated. This fact confirms the previous observations obtained by numerical calculations for the simple DOS cases.

It is noteworthy that the constant DOS with the parameters obtained from the treatment and then slightly modified provides for a good approximation of the real DOS in the vicinity of the Fermi level. Since the capacitance signal is related to the capture-release processes taking place at the Fermi level, we may conclude that the successful fit of experimental data depends on the introduced DOS at the Fermi level and E_a rather than on the shape of the DOS in the entire band gap. As it can be seen from Table 3.9, the set of parameters "simulation 3" (constant DOS in the band gap) reproduces the input characteristics of the "best fit" DOS very accurately regardless the shape of the DOS and provides for a satisfactory fit of the experimental data. Hence using only the information obtained from the *K-T* treatment it is possible to get a first credible glimpse on the properties in the band gap.

We may conclude that the DOS distribution defined with the help of numerical simulations from photocurrent techniques not only provides a good reproduction of the latter but also of capacitance measurements performed separately on a differently treated sample. The simple analytical treatment of experimental capacitance data allowed us to determine a value of $N(E_F)$ and E_C–E_F that are in good agreement with the values obtained from other

experimental techniques.

3.3.3 The comparison of pm-Si:H and a-Si:H by the *K(T)* treatment of the experimental capacitance data

In this Section we will address the possibility of reproducing the experimental *C-T* data of hydrogenated polymorphous silicon (pm-Si:H) and a-Si:H samples by introducing in simulations the parameters deduced from the *K-T* treatment.

Hydrogenated polymorphous silicon represents a kind of disordered silicon thin film material consisting in nanometric size ordered domains embedded in an amorphous matrix. The size and concentration of the domains are too low to give any signature in x-ray scattering experiments. However high resolution transmission electron microscopy and Raman spectroscopy have revealed the presence of the nanocrystallites [13,17]. The pm-Si:H films can be obtained in a radio-frequency glow discharge plasma-enhanced chemical vapour deposition (PECVD) system in a variety of deposition conditions. Previous studies have shown that hydrogenated polymorphous silicon has better transport properties and lower defect densities compared to standard hydrogenated amorphous silicon [12-15]. Our interest is to reveal the very low density of states at the Fermi level of pm-Si:H films and to reproduce the experimental data by introducing parameters deduced from *K-T* treatment into simulations.

Here we use data obtained on the previously studied samples of pm-Si:H and a-Si:H Schottky diodes. Details on the fabrication and the capacitance measurements can be found in Ref.10. From the *K-T* treatment $N(E_F)$, E_C–E_F and ν_n were deduced following the regular procedure of the linear approximation of *K-T* curves and plotting the derived values of the turn-on temperature in Arrhenius coordinates ω vs $1000/T_0$. The results are presented in Table 3.10.

	$N(E_F)$ ($cm^{-3}eV^{-1}$)	E_C-E_F (eV)	ν_n (s^{-1})
pm-Si:H	7.5×10^{14}	0.78	1.2×10^{14}
a-Si:H	5.5×10^{15}	0.78	3×10^{14}

Table 3.10. Parameters derived from the K-T treatment of the experimental capacitance data on pm-Si:H and a-Si:H Schottky diodes.

As we know from our previous study of the undoped a-Si:H Schottky diodes the treatment yields highly overestimated values of the attempt-to-escape frequency and

underestimated values of the DOS at the Fermi level. In order to adjust the input values for modeling as a primary set of parameters ("initial guess" DOS) we introduce constant DOS with $N(E_F)$ three times increased in comparison with the value from Table 3.10, σ_n derived from v_n was reduced of two orders of magnitude and the same E_a=0.78 eV was considered. The calculated *C-T* curves with this set of parameters are shifted to high temperatures in comparison with the experimental results. However, the slope of the curves is well reproduced. The *C-T* curves for pm-Si:H and a-Si:H obtained from numerical modeling with the "initial guess" DOS (see Table 3.11) are shown in Fig.3.35.

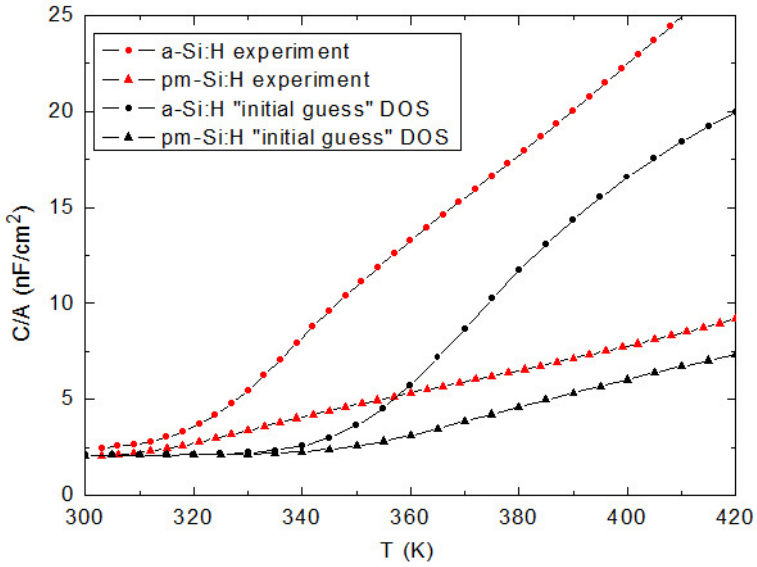

Fig.3.35. Capacitance-temperature curves of pm-Si:H and a-Si:H at f=91 Hz obtained experimentally and numerically with the "initial guess" DOS distribution.

As it can be seen from Fig.3.35 additional adjustment of the DOS parameters introduced into simulations is necessary in order to reproduce the experimental *C-T* curves. To shift the calculated *C-T* dependencies the activation energy was modified together with slight adjustment of the capture cross section and the DOS at the Fermi level. The best reproduction is achieved for the set of parameters noted as "best fit" DOS. The corresponding *C-T* curves are presented in Fig.3.36.

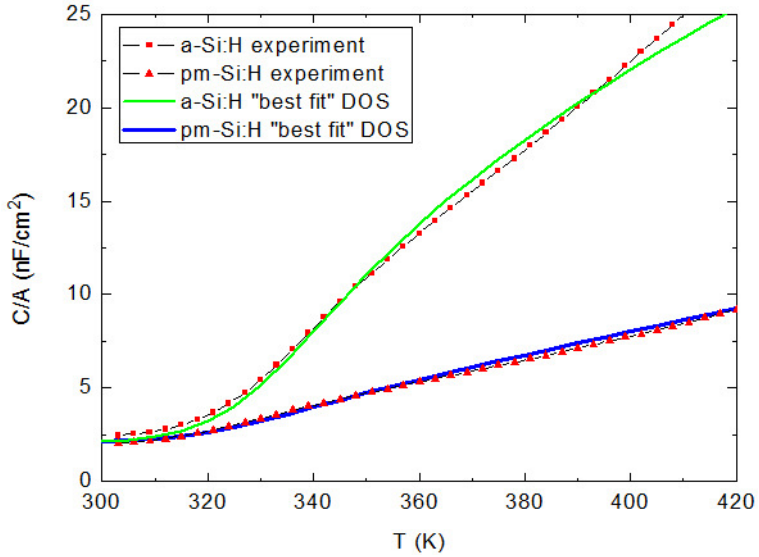

Fig.3.36. Capacitance-temperature curves of pm-Si:H and a-Si:H at f=91 Hz obtained experimentally and numerically with the "best fit" DOS distribution.

		$N(E_F)$ ($cm^{-3}eV^{-1}$)	E_C-E_F (eV)	ν_n (s^{-1})
pm-Si:H	reconstructed experiment	7.5×10^{14}	0.78	1.2×10^{14}
	introduced "Initial guess" DOS	2.25×10^{15}	0.78	1.2×10^{12}
	introduced "best fit" DOS	2.25×10^{15}	0.70	8×10^{11}
a-Si:H	reconstructed experiment	5.5×10^{15}	0.78	3×10^{14}
	introduced "Initial guess" DOS	1.65×10^{16}	0.78	3×10^{12}
	introduced "best fit" DOS	1.65×10^{16}	0.72	2×10^{12}

Table 3.11. Comparison of the parameters introduced in the numerical calculation from the "initial guess" and the "best fit" DOS distributions with those derived from the simplified treatment of the experimental data and C-T results from calculation of "best fit" DOS.

In conclusion, the *K-T* treatment of the capacitance data was used to derive the density of states at the Fermi level of pm-Si:H and a-Si:H films without any assumption on other physical parameters. To our knowledge, the derived values of $N(E_F)$ are underestimated and that of ν_n are highly overestimated. Adjusting the input values of these parameters following the tendencies observed in the theoretical study of the undoped a-Si:H in Section 3.2.1.1.c we obtained a good reproduction of the experimental data. The introduced values of the DOS at the Fermi level reveal the difference between two studied materials. $N(E_F) = 2.25\times10^{15}\text{cm}^{-3}\text{eV}^{-1}$ in pm-Si:H films and $N(E_F) = 1.65\times10^{16}\text{cm}^{-3}\text{eV}^{-1}$ in a-Si:H films prove that the defect density of disordered silicon thin films can be significantly reduced when going from amorphous to polymorphous material.

3.4 Conclusions

In this chapter we assessed the reliability and validity of the widely used simple *K-T* treatment of capacitance-temperature data suggested by Cohen and Lang. Several structures representing *n*-type and undoped hydrogenated amorphous silicon Schottky diodes were modeled and capacitance-temperature dependencies were obtained. Using the *K-T* treatment the density of states at the Fermi level, the activation energy and the attempt-to-escape frequency were derived and then compared to the introduced into simulations values.

It was shown that in the case of *n*-type a-Si:H with the position of the Fermi level E_C-E_F = 0.2 eV and an introduced constant DOS $N(E_F) = 1\times10^{19}\text{cm}^{-3}\text{eV}^{-1}$, the treatment *K-T* works well yielding close values of the DOS at the Fermi level and the attempt-to-escape frequency to that introduced into the calculations. The activation energy deduced from the Arrhenius plot was reproduced precisely as well. In the case of a lower DOS $N(E_F) = 1\times10^{16}\text{cm}^{-3}\text{eV}^{-1}$, an error of about two orders of magnitude was obtained for the attempt-to-escape frequency.

The accuracy and reliability of the extracted DOS parameters strongly depend on the position of the Fermi level and the DOS shape. The influence of the temperature on the results of the treatment is significant for the case of undoped a-Si:H with E_C-E_F = 0.7 eV. For this value of E_C-E_F with the introduced constant DOS the determination of $N(E_F)$ is erroneous and provided for underestimated values. Although $N(E_F)$ values are underestimated, the *K-T* treatment provided for a correct order of magnitude for $N(E_F)$, thus still allowing a rough estimation of this parameter. Exponential band tail and Gaussian distributions of DOS as well yielded underestimated values of $N(E_F)$.

The reliability of the studied treatment depends on the approximations used to obtain equations in the theoretical development section, namely the sharp cut-off approximation and the low-temperature limit. These approximations are no longer valid in the case of high

temperature onset of the capacitance signal (the case of $E_C–E_F$ = 0.7 eV) and significant variations of $N(E)$ in the vicinity of the Fermi level. The low-temperature limit defines the form of the occupation function of a defect level in the band gap and therefore determines the temperature range where the capture-release processes are described by the equations presented in the beginning of the chapter. In the case of non constant DOS it was shown that states above the Fermi level contributed to the final capacitance signal thus contradicting the sharp cut-off approximation. Another parameter derived from the treatment is the attempt-to-escape frequency ν_n. This parameter is considerably overestimated for almost all cases studied. This overestimation arises from the difficulties related to the linear fit of the *K-T* data and the erroneous values of the derived turn-on temperatures.

The influence of the capture cross section of electrons (σ_n) and the electron mobility (μ_n) was shown to bring considerable changes to the turn-on temperature. T_0 is defined by the characteristic time of the slowest process: capture-release of carriers from the gap states or charge transport. With the typical values of a-Si:H μ_n = 10 $cm^2V^{-1}s^{-1}$, $\sigma_n = 7\times10^{-16}$ cm^2 the turn-on temperature was determined by the capture-release process.

Finally numerical calculations were carried out to reproduce experimental capacitance data. A constant DOS was introduced into the simulation with the parameters ($N(E_F)$, $E_C–E_F$, ν_n) obtained from the *K-T* treatment of the experimental data without any additional information used. The calculated *C-T* curves although shifted to high temperatures showed reasonable behaviour and correct first approximation of the experimental data. After some adjustments performed on the parameters of the DOS a good reproduction of the experiment could be obtained. In order to approach the real DOS distribution data obtained from MPC and CPM techniques were introduced in modeling to calculate *C-T* dependencies. Again slight corrections of parameters describing the DOS distributions were performed within the precision of measurements and interpretation of the MPC data leading to a very good reproduction of experimental capacitance data. The simple analytical treatment of calculated capacitance data allowed us to determine a value of $N(E_F)$ and $E_C–E_F$ in good agreement with that obtained from experiment and the introduced values, while the attempt-to-escape frequency is again overestimated. We may conclude that the DOS distribution defined with the help of numerical simulations from photocurrent techniques not only provides good reproduction of the latter but also of capacitance measurements performed separately on a differently treated sample.

The possibilities of the *K-T* treatment was also analysed in the framework of comparison of the DOS at the Fermi level in pm-Si:H and a-Si:H. After adjusting the parameters ($N(E_F)$, $E_C–E_F$, ν_n) obtained from the *K-T* treatment of the experimental data considering the corrections observed for the studied case of undoped a-Si:H, a constant DOS was introduced into the simulation for both disordered materials. Again, a correct reproduction of the experimental data was achieved. The difference of introduced $N(E_F)$ values for both materials

confirms the previously observed lower defect density of the polymorphous material.

Thus the *K-T* treatment of the capacitance data together with numerical modeling provides for a valuable tool to assess some important parameters of a material without introducing any additional information on DOS of a studied structure.

3.5 References

[1] J.D. Cohen and D.V. Lang, “Calculation of the dynamic response of Schottky barriers with a continuous distribution of gap states”, *Physical Review B*, vol. 25, p. 5321, 1982.

[2] W. Schokley znd W. T. Read, *Physical Review B*, vol. 87, p. 835, 1952.

[3] T. Walter, R. Herberholz, C. Muller, H.W. Schock, “Determination of defect distributions from admittance measurements and application to Cu(In,Ga)Se_2 based heterojunctions”, *Journal of Applied Physics*, vol. 80, p. 441, 1996

[4] U. Rau, D. Braunger, R. Heberholz, H.W. Schock, J.F. Guille-moles, L. Kronik, D. Cahen, *Journal of Applied Physics,* vol. 86, p. 497, 1999.

[5] B. Canava, J. Vigneron, A. Etcheberry, D. Guimard, J.-F. Guillemoles, D. Lincot, S. Ould Saad Hamatly, Z. Djebbour, D. Mencaraglia, “XPS and electrical studies of buried interfaces in Cu(In,Ga)Se2 solar cells”, *Thin Solid Films*, vol. 403–404, p. 425, 2002.

[6] J. Serhan, Z. Djebbour, D. Mencaraglia, F. Couzinié-Devy, N. Barreau, J. Kessler, “Influence of Ga content on defects in $CuIn_xGa_{1-x}Se_2$ based solar cell absorbers investigated by sub gap modulated photocurrent and admittance spectroscopy”, *Thin Solid Films*, vol.519, p. 7312, 2011.

[7] C. Leendertz and R. Stangl: “Modeling an a-Si:H/c-Si Solar Cell with AFORS-HET”. In: Wilfried G.J.H.M. van Sark, Francesco Roca, Lars Korte (eds.) Physics and Technology of Amorphous-Crystalline Heterostructure Silicon Solar Cells, pp. 405-444, Springer-Verlag Berlin Heidelberg, 2012.

[8] R. Stangl, M. Kriegel, M. Schmidt, Proccedings. of the 4th World Conference on Photovoltaic Energy Conversion, Hawaii, USA, p.1350, 2006.

[9]http://www.helmholtz-berlin.de/forschung/enma/si-pv/projekte/asicsi/afors-het/index_en.html

[10] C. Longeaud and J. P. Kleider, “Trapping and recombination via dangling bonds in amorphous and glassy semiconductors under steady-state conditions: Application to the modulated photocurrent experiment”, *Physical Review B*, vol. 48, p. 8715, 1993.

[11] J. P. Kleider, C. Longeaud, M. Gauthier, M. Meaudre, R. Meaudre, R. Butté, S. Vignoli, and P. Roca i Cabarrocas, “Very low densities of localized states at the Fermi level in hydrogenated polymorphous silicon from capacitance and space-charge-limited current measurements”, *Applied Physics Letters*, vol. 75, p. 3351, 1999.

[12] M. Meaudre, R. Meaudre, R. Butté, S. Vignoli, C. Longeaud, J. P. Kleider, and P. Roca i Cabarrocas, “Midgap density of states in hydrogenated polymorphous silicon”, *Journal of Applied Physics*, vol. 86, p. 946, 1999.

[13] R. Butté, S. Vignoli, M. Meaudre, R. Meaudre, O. Marty, L. Saviot, and P.Roca i Cabarrocas, “Structural, optical and electronic properties of hydrogenated polymorphous

silicon films deposited at 150°C", *Journal of Non-Crystalline Solids*, vol. 266–269, p. 263, 2000.

[14] S. Vignoli, A. Fontcuberta i Morral, R. Butté, R. Meaudre, and M. Meaudre, « Hydrogen related bonding structure in hydrogenated polymorphous and microcrystalline silicon », *Journal of Non-Crystalline Solids*, vol. 299–302, p. 220, 2002.

[15] C. Longeaud and J. P. Kleider, *Physical Review B*, vol. 45, p. 11672, 1992.

[16] M.Y. Soro, M.E. Gueunier-Farret, J.P. Kleider, "Structural and electronic properties of hydrogenated polymorphous silicon films deposited at high rate", *Journal of Applied Physics,* vol. 109, p. 2371, 2011.

[17] P. Roca i Cabarrocas, S. Hamma, S. N. Sharma, G. Viera Bertan, and J. Costa, "Nanoparticle formation in low-pressure silane plasmas: bridging the gap between a-Si:H and μc-Si films", *Journal of Non-Crystalline Solids*, vol. 227–230, p. 871, 1998.

4 Capacitance spectroscopy of a-Si:H/c-Si heterojunctions

In this chapter the capacitance of a-Si:H/c-Si heterojunctions is considered. Firstly, we will recall the essential theory on a-Si:H/c-Si heterojunction. We will particularly focus on the band offsets and the existence of the interfacial inversion layer in c-Si. The possibilities of capacitance spectroscopy on a-Si:H/c-Si heterojunctions will be discussed. Next, frequency dependent and quasi-static modes of capacitance-temperature dependencies of a-Si:H/c-Si heterojunctions will be studied in details. The low-temperature steps on *C-T* curves will be considered and the influence of the parameters of a-Si:H will be studied by the means of numerical modeling.

The complete analytical calculation of the junction capacitance as a function of temperature and applied voltage will be presented and compared with traditional depletion approximation calculations. Finally, the comparison with the experimental results will be shown and discussed.

4.1 Theory on a-Si:H/c-Si heterojunctions

In this section the detailed description of (n) a-Si :H/(p) c-Si and (p) a-Si:H/(n) c-Si heterojunctions is provided. The capacitance measurements on these heterojunctions are discussed and some particular features due to the amorphous layer are shown. The derivation of band offsets from *C-V* measurements is discussed. We will also focus on the existence of an interfacial inversion layer and limitations to the *C-V* technique imposed by this phenomenon.

4.1.1 Band diagram and band offsets in a-Si:H/c-Si heterojunctions

A heterojunction is a junction formed between two different semiconductors. When two semiconductors have the same type of conductivity, the junction is called an isotype heterojunction. When the conductivity types differ, the junction is called an anisotype

heterojunction. In 1951, Shockley proposed the abrupt heterojunction to be used as an efficient emitter-base junction in a bipolar transistor [1]. Kroemer later analyzed a heterojunction as a wide-gap emitter [2]. Since then, heterojunctions have been extensively studied, and many important applications have been made, among them the room-temperature injection laser, light-emitting diode, photodetector, and solar cell.

Formation of a band diagram of a heterojunction creates certain difficulties, namely the problem of band lineup. This problem consists in the description of the equilibrium band diagram at the interface. If the system consisting of the two semiconductors in contact is in thermodynamic equilibrium, this implies that the Fermi level should be the same at any point. However, the condition of Fermi level alignment is not sufficient to properly describe how the bands are connected at the interface. The basic idea of most theories is to introduce a reference level in order to put the semiconductors on a common absolute energy scale, and then to align the reference levels in each semiconductor with each other for band lineup.

The energy-band model of an ideal abrupt heterojunction without interface traps proposed by Anderson [3] based on the previous work of Shockley introduces as a reference level the vacuum level E_{vac}. The two semiconductors are assumed to have different bandgaps E_g, different permittivities ε, different work functions Φ, and different electron affinities χ. Work function and electron affinity are defined as the energy required to remove an electron from the Fermi level E_F and from the bottom of the conduction band E_C, respectively, to a position just outside the material (vacuum level). The difference in energy of the conduction band edges in the two semiconductors is represented by ΔE_C and that in the valence-band edges by ΔE_V (band offsets).

When a junction is formed between two semiconductors, the energy band profile at equilibrium is as shown in Fig. 4.1(a) and 4.1(b) for the case of (p) a-Si :H/(c) c-Si and (n) a-Si:H/(p) c-Si heterojunctions, respectively. Since the Fermi level must coincide on both sides in equilibrium and the vacuum level is everywhere parallel to the band edges and continuous, the discontinuity in conduction-band edges (ΔE_C) and valence-band edges (ΔE_V) is invariant with doping in those cases where E_g and χ are not functions of doping (nondegenerate semiconductors). The total built-in (or diffusion) potential V_d is equal to the sum of the partial built-in voltage ($V_{d1} + V_{d2}$), where V_{d1} and V_{d2} are the electrostatic potential drops (so-called diffusion potentials) supported at equilibrium in a-Si:H and c-Si, respectively. The problem with Anderson's model is that neither ionization potential nor electron affinity are true bulk properties [4]. They depend on the structure of the surface, so are they affected by surface relaxation and surface reconstruction. Also, when the interface is formed, there may be charge transfer, microdiffusion of atoms across the interface, interface reconstruction or chemisorption. These phenomena lead to the formation of a dipole layer that is not taken into account in this simple theory. The dipole layer results in the additional potential drop at the interface within atomic distance that changes the apparent electron affinity or ionization

potential.

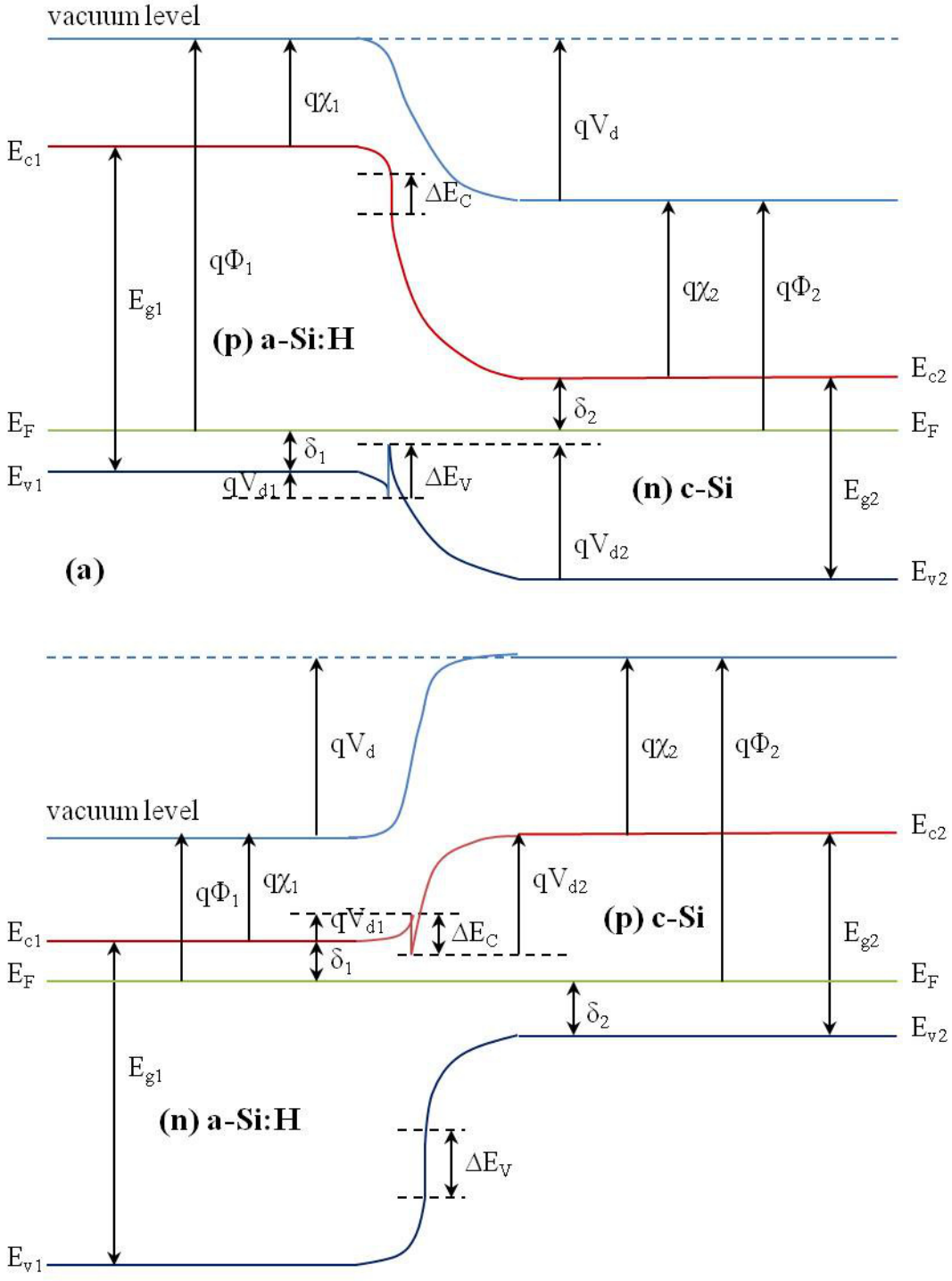

Fig.4.1. Band diagram at equilibrium of a (p) a-Si:H/(n) c-Si (a) and a (n) a-Si:H/(p) c-Si (b) heterojunctions .

The band offsets (ΔE_C and ΔE_V) are important parameters to be taken into account in

transport phenomena. Minority charge carriers in crystalline silicon face a barrier at the interface that leads to their accumulation and eventually under forward bias to their recombination with diffused majority carriers. On the other hand majority carriers also face the barrier that prevents them from reaching the amorphous layer and improves their collection at the front contact. Using the parameters of materials such as band gaps energies (E_g), electron affinities (χ), work functions (Φ) and the relations:

$$\Delta E_V + \Delta E_C = E_{g1} - E_{g2} \tag{4.1}$$

$$\Delta E_C = q(\chi_2 - \chi_1) \tag{4.2}$$

the band offsets can be related to the position of the Fermi level in both materials (referred to the majority carrier band, δ_1 or δ_2) and to the total diffusion potential V_d. For *n*-type c-Si:

$$\Delta E_V = qV_d + \delta_1 + \delta_2 - E_{g2}, \tag{4.3}$$

with

$$qV_d = q(\Phi_1 - \Phi_2), \tag{4.4}$$

and, for *p*-type c-Si:

$$\Delta E_C = qV_d + \delta_1 + \delta_2 - E_{g2}, \tag{4.5}$$

with

$$qV_d = q(\Phi_2 - \Phi_1). \tag{4.6}$$

If one wants to derive the band offsets values from parameters that are known or rather easily obtained, such as positions of the Fermi level in both materials (obtained from the doping concentrations) and the band gap in c-Si (that is well-known contrary to that one of a-Si:H) from Eqs (4.3) and (4.5) one can see that these parameters are related to ΔE_V or ΔE_C through the total diffusion potential V_d. For given values of the doping concentrations and thus δ_1 and δ_2 the total diffusion potential increases when ΔE_V rises for (p) a-Si:H/ (n) c-Si or when ΔE_C increases for (n) a-Si:H/ (p) c-Si.

Significant values of ΔE_V or ΔE_C can cause the appearance of a strong inversion layer in c-Si close to the interface. In the last years at LGEP a lot of work has been devoted to revealing the existence of this inversion layer at the interface and determining he band discontinuities for both types of crystalline substrate.

4.1.2 Inversion layer in c-Si at a-Si:H/c-Si interface

4.1.2.1 (p) a-Si:H/ (n) c-Si case

Here we provide more details on the study of the inversion layer in (p) a-Si:H/ (n) c-Si heterojunction that was done lately, namely in LGEP. The planar conductance measurement as a function of temperature is a powerful tool to study the interface and allows one to highlight the existence of the inversion layer [5,6].

It was shown that the planar conductance measured for (p) a-Si:H deposited on (n) c-Si wafer is several orders of magnitude higher than the one measured for samples deposited on glass substrates [5]. For the glass samples, the range of conductance is compatible with conductivities that are typical of (p) a-Si:H.

In Figure 4.2 a simplified equivalent electrical circuit for the current transport in the (p) a-Si:H/(n) c-Si structure is shown. One can see three possible paths for the carriers that contribute to the planar conductance. The first one is the path entirely in the amorphous layer. It can be neglected since measurements performed on the glass samples indicated a very low conductance compared to that of the c-Si samples. The contribution of the second path to the planar conductance is also negligible. This is because whatever the sign of the polarization, there is a reverse biased diode limiting the current flowing through this path between the two top coplanar electrodes. Thus the high conductance measured on the c-Si samples is due to the third path. This path does exist due to the presence of a hole inversion layer at the interface. An experimental proof for this path being dominant when a-Si:H is deposited on top of the c-Si is provided by the comparison of measurements on the c-Si sample before and after etching of the a-Si:H layer. From experimental data and results of numerical modeling a lower limit for ΔE_V could be found for the occurrence of the strong inversion layer: $\Delta E_V > 0.28$ eV [5].

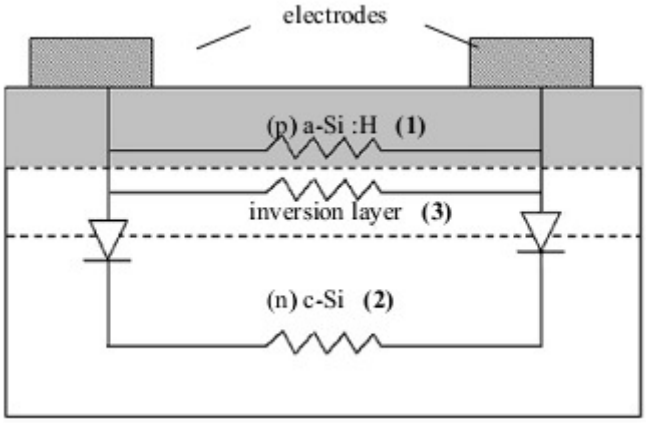

Fig.4.2. Simplified equivalent electrical circuit showing the contributions for the global conductance (from [5]).

During this thesis we proposed another approach to study the a-Si:H/c-Si interface namely by using the conducting probe atomic force microscopy (CP-AFM) technique [7]. Measurements were carried out using the setups at Ioffe Physical-technical Institute and at LGEP [8]. These setups allow one to apply a stable dc bias voltage to the device and to measure the resulting current flowing through the grounded tip as the sample surface is scanned in contact mode. Thereby, in both setups, simultaneous topographical and current (or resistance) mapping can be performed.

The idea of the suggested measurements is the following. If an inversion layer near the interface exists, then the local minority carrier density becomes considerable thus decreasing the resistivity. Since resistivity is directly related to resistance through the geometry of a sample it should be possible to spot the region of low resistance near the heterointerface by measuring the current (or resistance itself) along the sample. In order to perform such a measurement one needs to cleave the sample and scan along the cleaved section to access different regions of the heterojunction. The preparation of the samples has to be done very carefully since there are several constrains to CP-AFM technique arising from the quality of a measured surface and possible reconstruction of the surface. Modification of the band bending due to the surface defects and low sensitivity also can influence the revelation of the inversion layer by CP-AFM measurements. To minimize the possible presence of surface oxide layer cleaved samples should be dipped in a hydrofluoric acid (HF) solution and subsequently measured under nitrogen atmosphere.

Cleaved sections of ITO/(p)a-Si:H/(n)c-Si/ITO samples with different thickness of the a-Si:H layer (20, 100, and 300 nm) were studied. An example of simultaneous topography and current images is shown in Fig.4.3. The current image clearly reveals an interface layer that appears more conductive than both the c-Si substrate and the a-Si:H film. Such a conductive interface layer was detected on all samples, whatever the a-Si:H layer thickness.

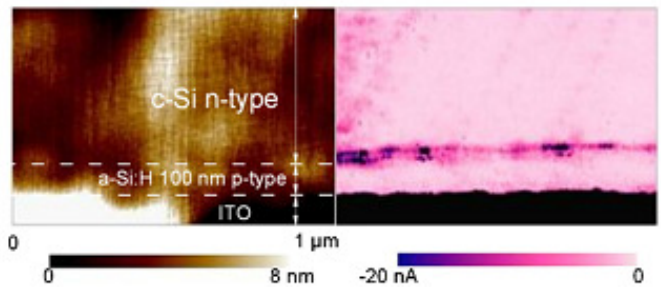

Fig.4.3. CP-AFM image showing a 0.5×1.5 µm² surface scan depicting (a) the topography and (b) the current map of a heterojunction based on (n) c-Si/(p) a-Si:H/ ITO from top to bottom. The bias applied to the sample was -2.5 V. In the current map darker regions correspond to higher negative current, i.e., more conductive regions.

4.1.2.2 (n) a-Si:H/ (p) c-Si case

The (n) a-Si:H/ (p) c-Si heterojunctions were studied as well in order to reveal the presence of the inversion layer in c-Si. Planar conductance measurements were carried out on (n) a-Si:H/(p) c-Si and (n) a-Si:H/glass samples. The latter showed conductance and its temperature dependence typical for (n) a-Si:H films, with an activation energy of 0.17 eV. The coplanar conductance of (n) a-Si:H/(p) c-Si samples was found several orders of magnitude higher, and the temperature dependence wass much weaker (with E_a=0.018 eV). The conduction of holes through the (p) c-Si substrate does not contribute to the current since it has to cross one reverse biased (n) a-Si:H/ (p) c-Si junction. Again, high conductivity is due to a high planar electron conductance at the c-Si surface. This was proved by the drastic decrease of conductance and increase of its activation energy observed after the a-Si:H layer had been removed by dry etching [9]. The temperature dependence of the sheet electron density allowed a precise determination of the conduction band offset between a-Si:H and c-Si: $\Delta E_C = 0.15 \pm 0.04$ eV [10].

CP-AFM measurements were carried out on cleaved sections of ITO/(n)a-Si:H/(p)c-Si/ITO samples. An example of topography and resistance image obtained in such conditions is illustrated in Fig.4.4 with, from top to bottom, the *n*-type a-Si:H layer and the *p*-type c-Si substrate. A conductive channel at the interface is again clearly observed. A careful look reveals that the channel lies on the c-Si part of the junction.

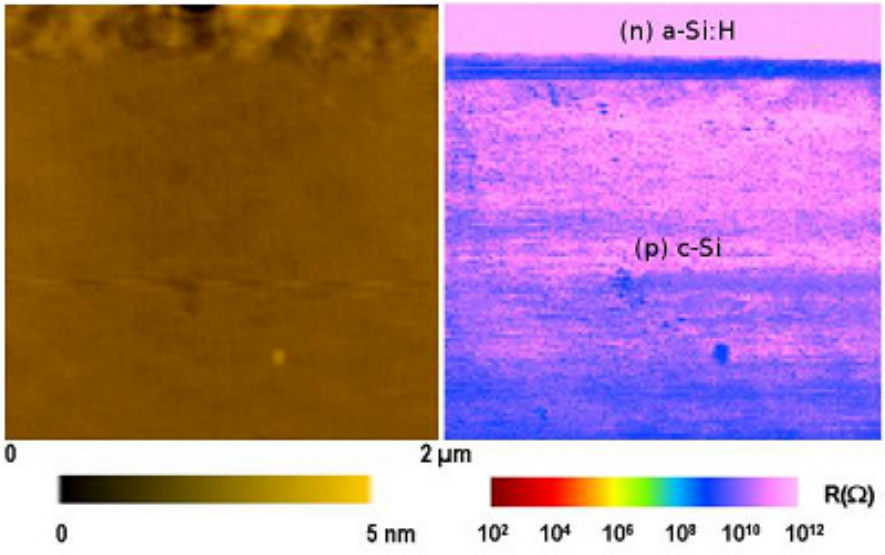

Fig.4.4. 2×2 µm² surface map illustrating the topography and the local resistance of (n) a-Si :H (300 nm)/ (p) c-Si heterointerface.

4.1.3 Capacitance measurements of a-Si:H/c-Si heterojunctions

Capacitance techniques have been widely used for band offset determination [11,12]. Similar to capacitance of a *p-n* junction considered in Chapter 2, the depletion widths and capacitance can be obtained by solving Poisson's equation for the step junction on either side of the interface within the depletion approximation. For a crystalline *p-n* anysotype heterojunction one can obtain for the depletion widths x_p and x_n in *p*- and *n*- sides, respectively:

$$x_p^2 = \frac{2}{q}\frac{N_D \varepsilon_p \varepsilon_n (V_d - V_a)}{N_A(\varepsilon_p N_A + \varepsilon_n N_D)} \tag{4.7}$$

$$x_n^2 = \frac{2}{q}\frac{N_A \varepsilon_p \varepsilon_n (V_d - V_a)}{N_D(\varepsilon_p N_A + \varepsilon_n N_D)} \tag{4.8}$$

where N_D and N_A are the donor and acceptor doping densities of the *n*- and *p*- side, respectively, ε_p and ε_n are the dielectric permittivities, and V_a the applied bias voltage The ac bias produces variations in the space charge density. These occur at the edges of the depletion region. The capacitance can thus be seen as the series of the capacitances associated to the depletion widths in each semiconductor and is then written per unit area *A*:

$$\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2} \tag{4.9}$$

$$\frac{C}{A} = \frac{\varepsilon_p \varepsilon_n}{(\varepsilon_n x_p + \varepsilon_p x_n)} = \sqrt{\frac{q}{2} \frac{(\varepsilon_p \varepsilon_n N_D N_A)}{(\varepsilon_p N_D + \varepsilon_n N_A)(V_d - V_a)}} \tag{4.10}$$

When the doping density of the *p*-side is stronger than that of the *n*-side, the depletion width x_p is smaller than x_n. Thus the measured capacitance is more sensitive to the side of the junction that has the larger space charge width [4]. For very high space charge density and very small space charge width on the *p*-side, the situation becomes similar to that of an equivalent Schottky barrier, considered in Chapter 2:

$$\frac{C}{A} = \sqrt{\frac{q}{2} \frac{\varepsilon_n N_D}{(V_d - V_a)}} \tag{4.11}$$

The square of the inverse capacitance varies linearly as a function of the applied voltage and the intercept of the extrapolated value to zero, V_{int}, is equal to the total diffusion potential. This is the basis of the *C-V* method [13]. From the knowledge of V_d, the valence band offset can be deduced from Eq.(4.3) on *n*-type c-Si.

Let us now apply the theoretical background described above to the case of a (p) a-Si:H / (n) c-Si heterojunction. The band diagram and the equivalent junction capacitance circuit are shown in Fig.4.5.

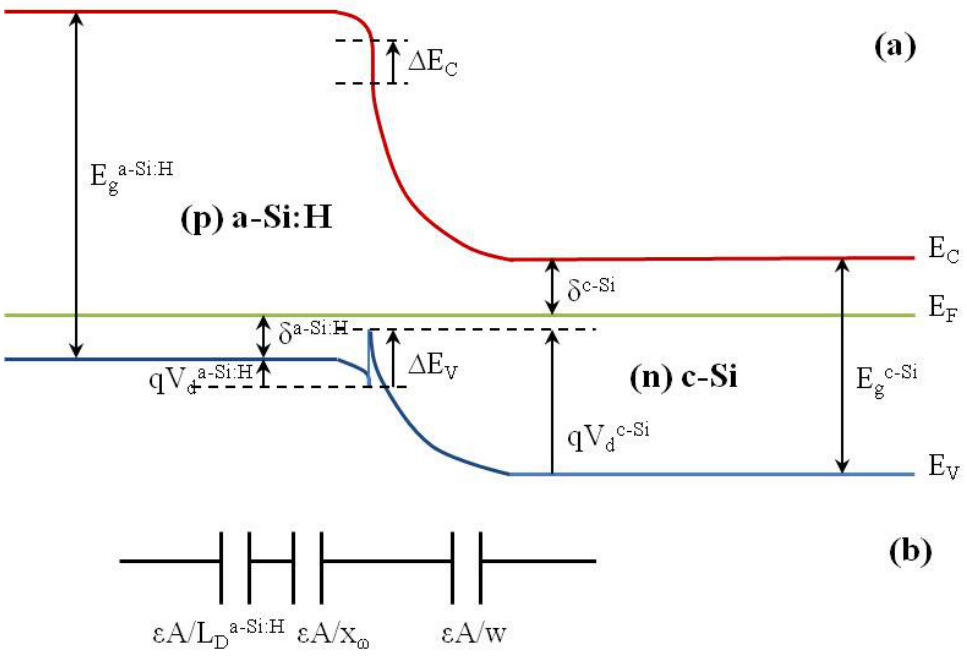

Fig.4.5. (a) Band diagram of (p) a-Si:H/(n) c-Si heterojunction. (b) Scheme of the equivalent capacitance. The capacitance of (p) a-Si:H layer is composed of two capacitances out in series: at the left of x_ω, the device behaves as a pure dielectric medium with the contribution of $\varepsilon A/x_\omega$, whereas at the right of this cut-off abscissa, the localized states contribution to the total capacitance is written as $\varepsilon A/L_D^{a\text{-}Si:H}$. The capacitance of (n) c-Si is defined as $\varepsilon A/w$, w being the depletion region width.

The a-Si:H/c-Si case is somewhat particular due to the properties of a-Si:H [4]. Two issues have to be considered. Firstly, since a-Si:H is not a crystalline semiconductor, it contains a huge quantity of bulk defects within the bandgap, and the space charge density is determined by the localized gap states around the bulk Fermi level rather than by the doping density. Therefore the simple depletion layer expressions are no longer valid. The second issue, also related to the bandgap states, concerns the dynamic response to an ac voltage. Indeed, in a-Si:H changes in the space charge density are linked to capture/emission of charges into/from defects around the Fermi level. This has been studied in details by several authors [14-16].

As it was discussed in details in Chapter 3 bulk gap states in an *n*-type amorphous silicon Schottky diode can exchange electrons with the conduction band. The onset of the response of gap states to the ac modulation results in a capacitance step when either the temperature is increased or the frequency is decreased [17]. While the position of the capacitance step depends on the capture cross section of the carrier being exchanged, the amplitude of the step is directly related to the quantity of defects regardless of the capture cross section.

Applying this observation for a-Si:H Schottky diodes to the case of a (p) a-Si:H / (n) c-Si

heterojunction two important issues are worth emphasizing. Firstly, one expects a step-like behavior in the capacitance versus temperature plot, just like for an a-Si:H Schottky diode. The same also applies to a (n) a-Si:H / (p) c-Si heterojunction. Such a capacitance step behavior has indeed been observed experimentally on silicon heterojunctions formed with undoped a-Si:H [18] as well as with doped a-Si:H. Secondly, due to the specific charge distribution related to defects in a-Si:H, one cannot use the simple Eqs. (4.7) and (4.8) to calculate the widths of the space charge regions. Therefore the simple bias dependence of the total capacitance expressed by Eq. (4.9) or (4.10) should not apply.

The possibility of obtaining the diffusion potential from the bias voltage dependence as well as the impact of frequency on the *C-V* curve was studied in Ref. [17]. Here we provide for a short overview of the main results of this study. In order to address frequency influence on capacitance numerical calculations using the AFORS-HET software for a (p) a-Si:H/(n) c-Si heterojunction were performed. The temperature dependence at zero dc bias is shown for two very different frequencies (100 Hz and 1 MHz) in Fig.4.6. In order to study the dc bias voltage dependence, the temperature $T = 250$ K was chosen, where the low frequency value of the capacitance is in the high plateau regime, while the high frequency value is in the low plateau regime. Thus, at this temperature the two selected frequencies exhibit the extreme behaviours of the a-Si:H gap states response.

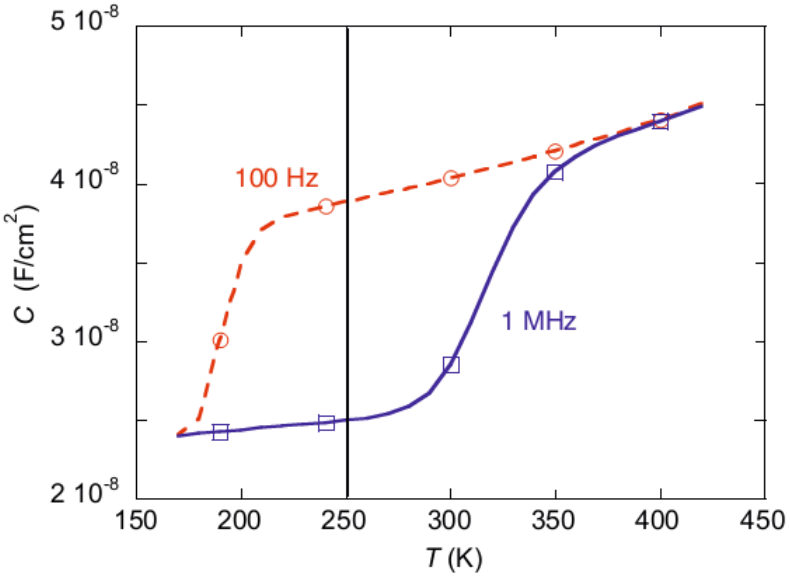

Fig.4.6. Capacitance versus temperature of a (p) a-Si:H / (n) c-Si heterojunction ($d^{a\text{-}Si:H}$ = 150 nm) calculated at two different frequencies (100 Hz and 1 MHz). At 250 K these frequencies show the extreme behaviours for the response in a-Si:H [from 4].

It was observed that the square of the inverse capacitance followed a linear dependence on the dc bias for both frequencies. However, the slope and the voltage intercept of the linear

fit were very different for the two frequencies. The exploitation of the capacitance data obtained at low frequency yields the correct value for the doping density introduced in the calculation for c-Si, while the value deduced from the high frequency regime capacitance data is erroneous by about 40%: N_D=1.1×10^{15} cm^{-3} was found using Eq.(4.11) instead of introduced value 1.5×10^{15} cm^{-3}. In the high frequency regime the a-Si:H layer behaves like an insulator and the corresponding capacitance is thus simply equal to the geometric dielectric capacitance $\varepsilon A/d^{a\text{-}Si:H}$. In the low frequency regime when the gap states in a-Si:H are able to follow the ac signal the corresponding a-Si:H capacitance is very large compared to the c-Si capacitance. This means that the space charge layer width in a-Si:H is very narrow compared to that in c-Si. From this point of view the system behaves like a *p*+-*n* one-sided junction and the potential drop in the amorphous layer can be neglected. In that case, despite the amorphous nature of the a-Si:H, the simplified expression of the capacitance given by Eq. (4.11) works for the determination of N_D.

Regarding the determination of the intercept voltage, V_{int}, one could expect that these data also yield the correct value of band offset since the low frequency data yielded the correct value of doping density in c-Si. However, it was shown, that the *C-V* intercept method applied to the (p) a-Si:H / (n) c-Si structure leads to a strongly undersestimated value for ΔE_V [4]. In the same way, the method applied to (n) a-Si:H / (p) c-Si structure leads to underestimated values for the conduction band offset [17]. By changing the conduction band offset value in the calculations (all other parameters being constant) it has been shown that there are two reasons that explain the underestimated values obtained for the band offset. First, increasing the band offset leads to an increase of the diffusion potential in the a-Si:H that becomes no longer negligible. Second, part of the potential drop in c-Si is not reflected in the simple depletion layer approximation because of the existence of a strong inversion layer in c-Si at the interface. In this layer the potential drop does not follow the quadratic dependence as in a depleted region but it has much steeper variations. The intercept voltage of the *C-V* method reflects the potential drop of the depleted region in the c-Si layer, and does not account for the two additional potential drops in a-Si:H and in the strong inversion layer in c-Si. This is why, when increasing the band offset the intercept voltage of the *C-V* method saturates at a value close to the potential drop in the depleted region of c-Si and does not increase linearly as does V_d [17] (see Fig. 4.7).

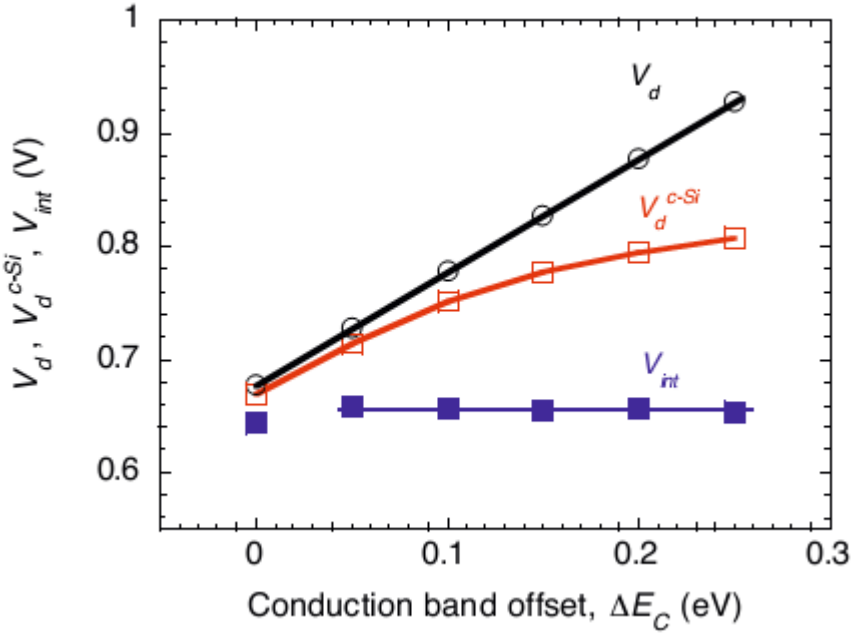

Fig.4.7. Calculated values of the total diffusion potential, V_d, the part of the diffusion potential in c-Si, $V_d^{c\text{-}Si}$, and the intercept voltage of the inverse square capacitance, V_{int}, in an (n) a-Si:H / (p) c-Si heterojunction, as a function of conduction band offset, ΔE_C [from 4].

Thus the flaw of the *C-V* method is that it disregards the potential drops in the a-Si:H layer as well as in the strong inversion layer in c-Si. The inversion layer issue was addressed for crystalline p^+-*n* homojunctions a long time ago in the work of Gummel and Scharfetter [19]. They showed on the example of p^+-*n* junction that the depletion approximation is not valid if one side of the junction is much more heavily doped than the other. They calculated the capacitance as the difference of stored electron charge associated with dc states due to the total voltage change, *dV*, divided by the voltage difference. In their theoretical development they considered that there was the spill-over charge, i.e. the charge resulting from carriers spilled over from the heavily doped side, by adding the term of the holes contribution to the charge in the *n*-side of the junction. They found that for asymmetrical junctions the intercept of a plot $1/C^2$ vs V_a with the voltage axis was nearly independent of the impurity concentration on the heavily doped side and was less than the built-in voltage. This is somewhat similar to the behavior observed in Fig.4.7 where V_{int} is independent of ΔE_C while Vd increases linearly.

A more detailed study of the influence of the surface inversion layer has been carried out during this thesis and will be proposed in the next sections.

4.2 Frequency dependent behavior of *C-T* dependencies: capacitance steps

In this section we focus on the study of the frequency dependent low temperature region of capacitance-temperature dependencies of (p) a-Si:H/(n) c-Si heterojunctions. As it was discussed in the previous section that *C-T* curves are expected to experience a low-temperature step which position is frequency dependent due to the capture-release processes in the amorphous layer. At higher temperatures *C-T* curves coincide and the capacitance increases smoothly. An example of capacitance-temperature dependency in a wide temperature range obtained by numerical modeling is presented in Fig.4.8. The parameters used to describe the structure shown in Fig.4.8 are presented in the following section.

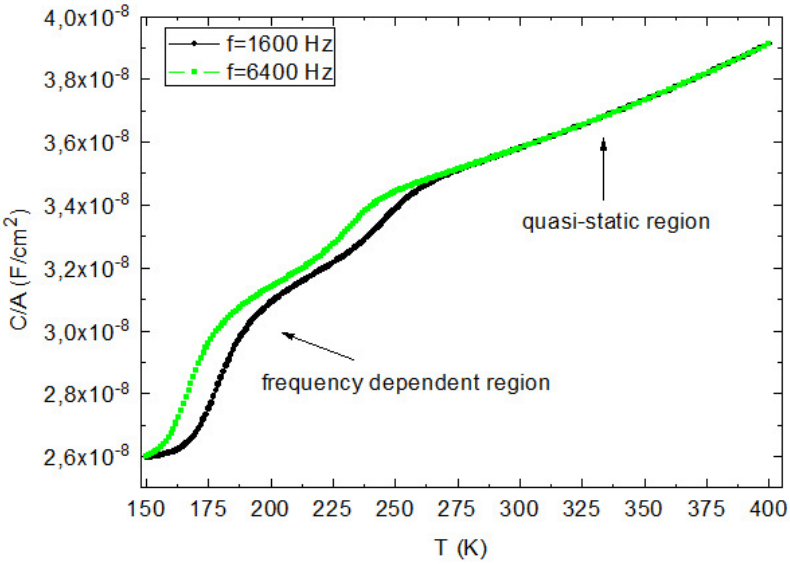

Fig.4.8. Calculated capacitance curves as a function of temperature for two frequencies (ΔE_V = 0.47 eV, μ_p = 1 $cm^2V^{-1}s^{-1}$ and $\sigma_p = 7\times10^{-16}$ cm^2). Frequency dependent steps and quasi-static region are indicated.

We clearly observe that the capacitance is independent of frequency in the high temperature region (T>250 K), that corresponds to the quasi-static response. At lower temperatures we have observed two capacitance steps. This is even a more peculiar feature compared to preceding works where only one step was mentioned (see Fig.4.6 and Ref.[4]). In the following we will discuss the origin of these two steps, and whether they may exist or not depending on a-Si:H/c-Si interface parameters.

4.2.1 Numerical modeling of *C-T* dependencies

Simulations were performed with AFORS-HET v3.0 software. The (p*)* a-Si:H/ (n) c-Si structure that was modeled is given Fig.4.9. For the *p*-type a-Si:H layer the density of states was taken independent of energy and equal to 10^{19} cm^{-3} eV^{-1} and the Fermi level position was fixed at 0.3 eV from the valence band edge at 300 K by introducing the corresponding concentration of acceptors $N_A = 1.44\times10^{19}$ cm^{-3}. The carrier mobilities were taken equal to μ_n = 10 $cm^2V^{-1}s^{-1}$ and μ_p = 1 $cm^2V^{-1}s^{-1}$. The electron and hole capture cross sections were introduced equal to $\sigma_n = \sigma_p = 7\times10^{-16}$ cm^2. A doping density $N_D = 1.2\times10^{16}cm^{-3}$ was introduced to set the Fermi level at 0.2 eV from the conduction band edge in (n) c-Si at 300 K. The carrier mobilities were taken equal to μ_n = 1040 $cm^2V^{-1}s^{-1}$ and μ_p = 412 $cm^2V^{-1}s^{-1}$. The valence band offset (ΔE_V) value was varied by changing the electron affinity of both materials, while keeping the band gaps constant, equal to 1.74 eV and 1.12 eV in a-Si:H and c-Si, respectively.

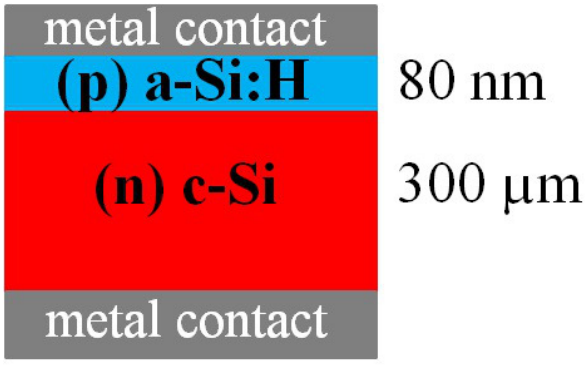

Fig.4.9. (p) a-Si:H/(n) c-Si heterojunction structure introduced in simulations.

It has been suggested that in the temperature dependence of the capacitance *C(T)* two steps may be observed that are shifted to higher temperatures when the measurement frequency is increased [20-22]. The first step, occurring in the low temperature range (100–200 K), was related to the transport and response of gap states in the a-Si:H layer, and the second step, occurring at higher temperatures (>200 K), was ascribed to the response of the interface states. In this study, we will not address the effect of interface states and we will concentrate on the low temperature step. The reason is that, for high quality silicon heterojunctions solar cells, the interface defect density is low enough and has influence on the *C-T* behavior. This was shown for both simulation and experiment on (n) a-Si:H/(p) c-Si heterojunction [10]. For (p) a-Si:H/(n) c-Si heterojunction, being the object of the present work, we performed the similar study of the influence of the interface defects on the capacitance-temperature dependencies. This analysis is presented on Section 4.4.2.

Considering this, in the simulations perfect interface without any interface states was introduced. Although the low temperature step is generally attributed to the response of the

gap states in the amorphous layer, the transport of carriers from the electrodes to the space charge region can also influence the capacitance value, especially in low mobility semiconductors like a-Si:H. These two processes may be competing as it was discussed in Chapter 3 for the case of a-Si:H Schottky diodes. Indeed, the characteristic times of the capture-release process and the transport of carriers can be comparable for certain values of the capture cross section and mobility of majority carriers, here those of holes, σ_p and μ_p. In addition, for the (p) a-Si:H/(n) c-Si heterojunction the presence of the free holes located in the inversion layer at the interface on c-Si side may also induce a capacitance response. All these processes would have different activation energies. Thus, the present interest is concentrated in deriving the activation energy of the capacitance step and its interpretation.

The calculated band diagram of the (p) a-Si:H/(n) c-Si heterojunction described above is shown in Fig.4.10.

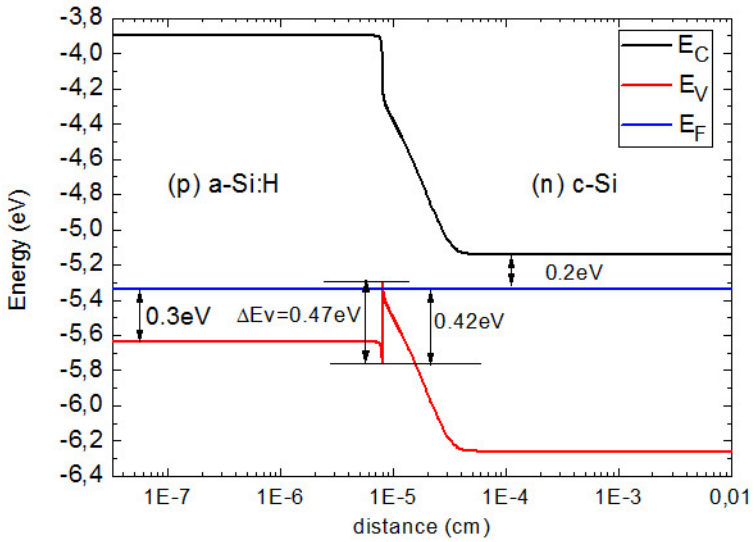

Fig.4.10. Calculated equilibrium band diagram of (p) a-Si:H/ (n) c-Si heterojunction at 300 K for a valence band offset value $\Delta E_V = 0.47$ eV and $N(E_F) = 1\times10^{19}$ cm^{-3}eV^{-1}.

Typical calculated capacitance curves are presented in Fig. 4.11. As in the case of a-Si:H Schottky barrier (see Chapter 3) the capacitance curves are shifted to higher temperatures for higher frequencies. Two capacitance steps are observed at characteristic temperatures $T_{0\ low}$ and $T_{0\ high}$. These two steps indicate that there are two processes being activated with the increasing temperature. The turn-on temperatures $T_{0\ low}$ and $T_{0\ high}$ of the capacitance steps were derived from the corresponding conductance-temperature (*G-T*) dependencies as the temperatures of the maximum on the *G-T* curves as it is shown in Fig.4.12.

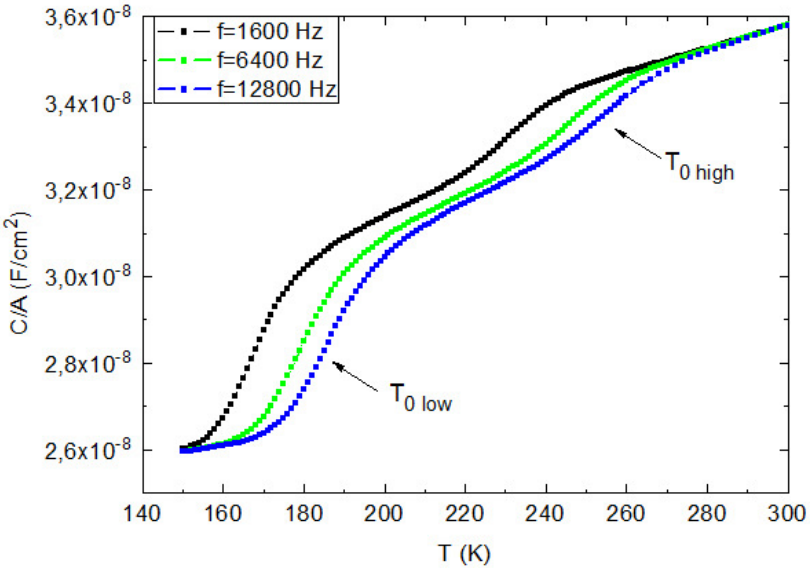

Fig.4.11. Calculated capacitance curves as a function of temperature for different frequencies (μ_p = 1 $cm^2V^{-1}s^{-1}$ and $\sigma_p = 7\times10^{-16}$ cm^2). Two characteristic temperatures $T_{0\ low}$ and $T_{0\ high}$ of two corresponding capacitance steps are indicated.

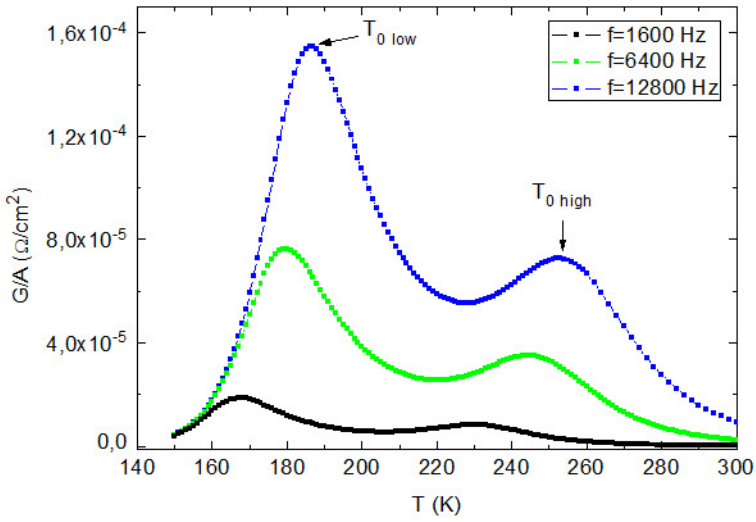

Fig.4.12. Calculated conductance curves as a function of temperature for different frequencies (μ_p = 1 $cm^2V^{-1}s^{-1}$ and $\sigma_p = 7\times10^{-16}$ cm^2). Two characteristic temperatures $T_{0\ low}$ and $T_{0\ high}$ of two corresponding capacitance steps are indicated.

The Arrhenius plot of ω vs $1000/T_0$ allows one to obtain the activation energy E_a of each capacitance step and thus the activation energy of the corresponding process. The activation energy can provide for information on which process can be linked with each step. For the curves shown in Fig.4.13 the two activation energies E_{a1} = 0.31 eV and E_{a2} = 0.45 eV were obtained for the low and the high temperature capacitance step, respectively.

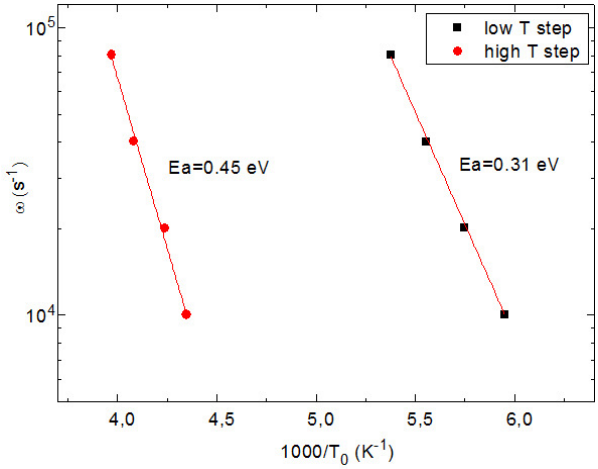

Fig.4.13. Arrhenius plot ω vs 1000/T_0 for $T_{0\,low}$ and $T_{0\,high}$ for the C-T curves presented in Fig.9 (μ_p = 1 $cm^2V^{-1}s^{-1}$ and $\sigma_p = 7\times10^{-16}$ cm^2).

In order to understand which processes are characterized by these activation energies we varied the position of the Fermi level $(E_F - E_V)^{a\text{-}Si:H}$, the valence band offset ΔE_V, hole mobility μ_p, in a-Si:H, and the hole capture cross-section of defect states in the a-Si:H band gap σ_p. The dependence of T_0 on the carrier mobility can indicate whether the capacitance steps are related to the transport in a-Si:H. In the same way, the dependence of T_0 on the capture cross-sections of defects in a-Si:H can indicate whether capture and emission processes are involved in the capacitance steps.

The influence of the capture cross section of holes on *C-T* curves for $(E_F\text{-}E_V)^{a\text{-}Si:H}$=0.3 eV, ΔE_V=0.47 eV and μ_p=1 $cm^2V^{-1}s^{-1}$ is shown in Fig.4.14.

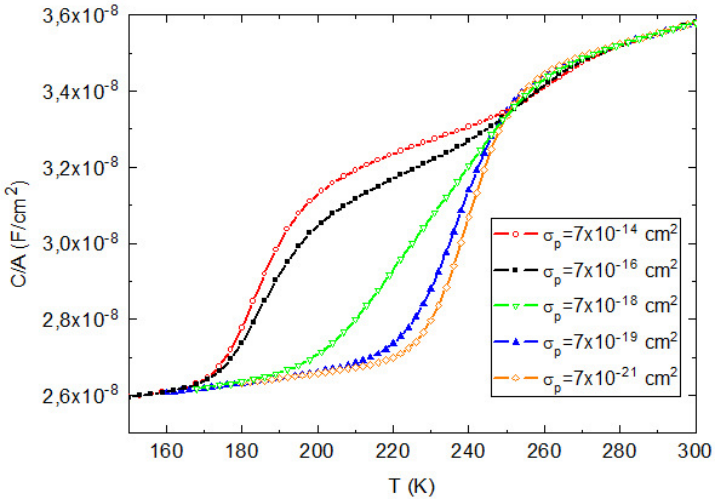

Fig.4.14. Calculated C-T curves for different values of capture cross section of holes in a-Si:H at f=12.8 kHz (μ_p=1 $cm^2V^{-1}s^{-1}$).

One can see that for $\sigma_p < 7\times10^{-18}$ cm^2 only one capacitance step is observed, while for $\sigma_p = 7\times10^{-14}$ cm^2 and $\sigma_p = 7\times10^{-16}$ cm^2 the two steps are more prominent. It is noteworthy that the high temperature step is almost unchanged for all considered values of σ_p. The absence of the low temperature step is confirmed by the conductance-temperature curve where only one maximum is observed (Fig.4.15). However, the only capacitance step for $\sigma_p = 7\times10^{-18}$ cm^2 is rather a superposition of two distinguished steps observed for higher values of the capture cross section than a "pure" high temperature step. The evolution of these steps can be seen on the *G-T* curves in Fig.4.15 for a range of capture cross section values from $\sigma_p = 7\times10^{-14}$ cm^2 to $\sigma_p = 7\times10^{-21}$ cm^2. One can see that the only step for $\sigma_p = 7\times10^{-18}$ cm^2 is characterized by wide peak in conductance curve that can be considered as a overlay of two peaks brought close to each other. However, for $\sigma_p < 7\times10^{-19}$ cm^2 the conductance peaks are well resolved and describe the high temperature step. The processes related to each step and the evolution of *C-T* curves with the change of σ_p will be discussed further, where the activation energies of each step are considered. Up to this point, we may conclude that the modulation of gap states occupancy through capture-release processes of holes in the space charge region on the a-Si:H side influences significantly the capacitance-temperature behavior, namely the position of the low temperature step.

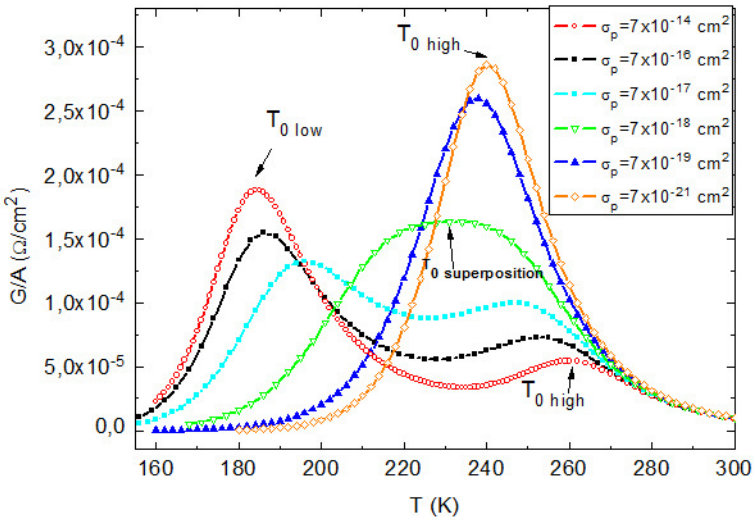

Fig.4.15. The conductance-temperature curves for different values of capture cross section of holes in a-Si:H at f=12.8 kHz (μ_p=1 cm^{2}V^{-1}s^{-1}).

The influence of the hole mobility in a-Si:H on C-T curves is presented in Fig.4.16. We observe the same trend as the one obtained when varying σ_p: one can observe that the capacitance-temperature curves exhibit only one distinguished step that occurs at lower temperatures for larger values of mobility.

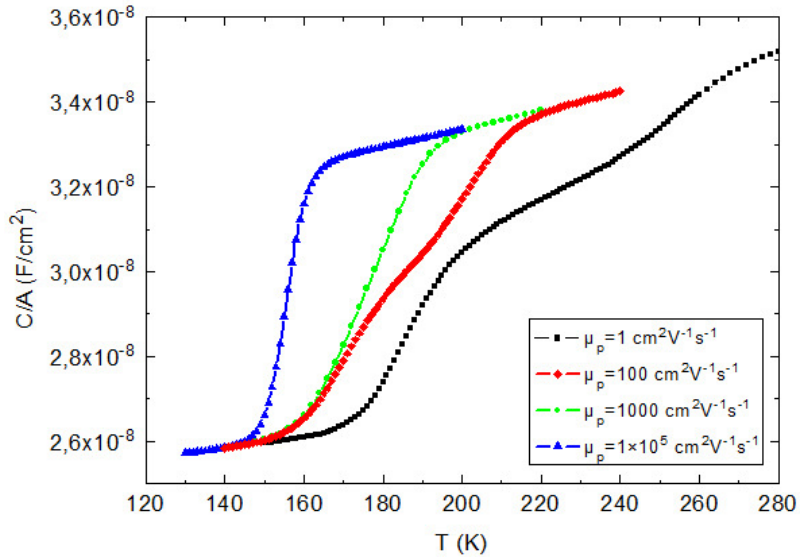

Fig.4.16. Calculated C-T curves for different values of mobility of holes in a-Si:H at f=25.6 kHz (σ_p=7×10^{-16} cm^2).

Again as in the case of changing t σ_p the only capacitance step at higher values of μ_p is the "pure" high temperature step shifted to the low temperatures, as it will be shown later from the derived activation energy values. From Fig.4.17 one can see that the temperature shift of the high temperature step is significant in comparison with that of the low temperature step. Thus the process related to the high temperature step is more sensitive to the change of the hole mobility.

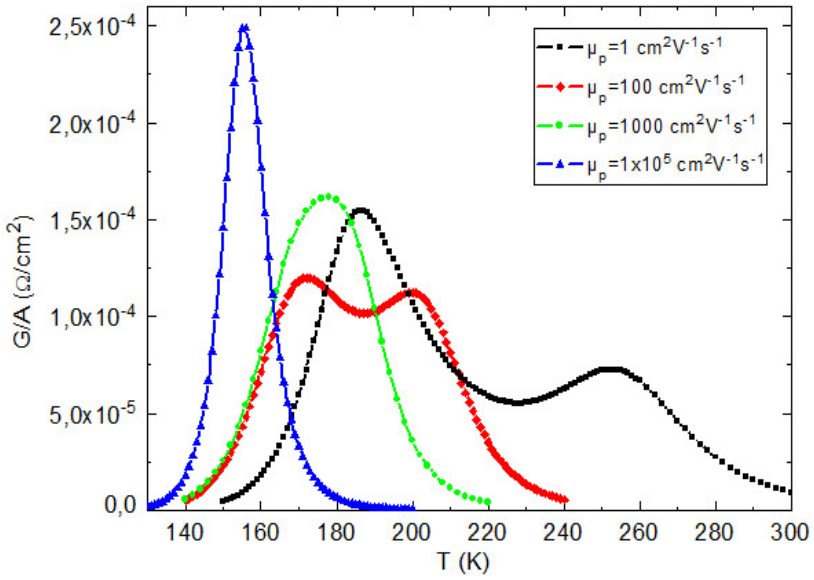

Fig.4.17. The conductance-temperature curves for different values of hole mobility in a-Si:H at f=12.8 kHz (σ_p=7×10^{-16} cm^2).

Let us now address the processes possibly involved into the observed capacitance steps. From the activation energies obtained for $\sigma_p = 7\times10^{-16}$ cm^2 and $\mu_p = 1$ cm^{2}V^{-1}s^{-1} we may conclude that the low temperature step is related to the capture-emission process in the bulk of the amorphous layer with $E_{a1} = 0.31$ eV that is close to the value $(E_F\text{-}E_V)^{a\text{-}Si:H\ bulk}$. The high temperature capacitance step with $E_{a2} = 0.45$ eV can be possibly related to the modulation of the hole's concentration in the inversion layer by the change of the ac signal since its activation energy is larger than that of $(E_F\text{-}E_V)^{a\text{-}Si:H\ bulk}$ and is very close to $(E_F\text{-}E_V)^{a\text{-}Si:H} = 0.42$ eV at the interface. Since the low temperature step is related to the capture-emission processes, the decreasing of the capture cross section of the holes at a given frequency ω_0 leads to the increase of $T_{0\ low}$ that agrees to the condition of the onset of the response of gap states at the bulk Fermi level:

$$2\sigma_p v_{th} N_V \exp\left(-\frac{(E_F - E_V)^{a-Si:Hbulk}}{k_B T_0}\right) = \omega_0, \tag{4.12}$$

where v_{th} is the thermal velocity and N_V is the effective DOS in the valence band. Since the high temperature step is not affected by the change of the capture cross section, the $T_{0\ high}$ value does not vary. As the results two steps are shifted closer to each other due to the increase of $T_{0\ low}$. For the value of the hole capture cross section $\sigma_p = 7\times10^{-18}$ cm^2 we can see the superposition of two responses to the ac modulation whose turn-on temperatures lie close to each other: in the bulk due to the capture-emission and at the interface due to modulation of concentration of the holes in the inversion layer. Further decreasing of the hole capture cross section results in the further shift of $T_{0\ low}$ to higher temperatures. As a results, $T_{0\ low}$ becomes higher than $T_{0\ high}$ and the temperature positions of the steps are inversed. From $\sigma_p = 7\times10^{-19}$ cm^2 we observe only the high temperature step. The activation energy of 0.42 eV was found for this capacitance step, that corresponds to $(E_F\text{-}E_V)^{a\text{-}Si:H}$ at the interface. The capture-emission processes that are limited by the low σ_p value should take place at $T > T_{0\ high}$. However, no step is observed at higher temperature that can be explained by the amplitude of the high temperature capacitance step. Indeed, the charge variation at the interface due to the high hole's concentration is more considerable that that one due to the capture-release processes. Once the modulation of the hole's concentration at the interface is activated the step related to the response of the gap states becomes negligible and therefore cannot be observed on *C-T* curves.

In order to confirm the attribution of the low temperature capacitance step to the capture-release processes the case of different thickness of a-Si:H layer was considered. The *C-T* curves for $\sigma_p = 7\times10^{-16}$ cm^2 and $\mu_p = 1$ cm^{2}V^{-1}s^{-1} are shown in Fig.4.18.

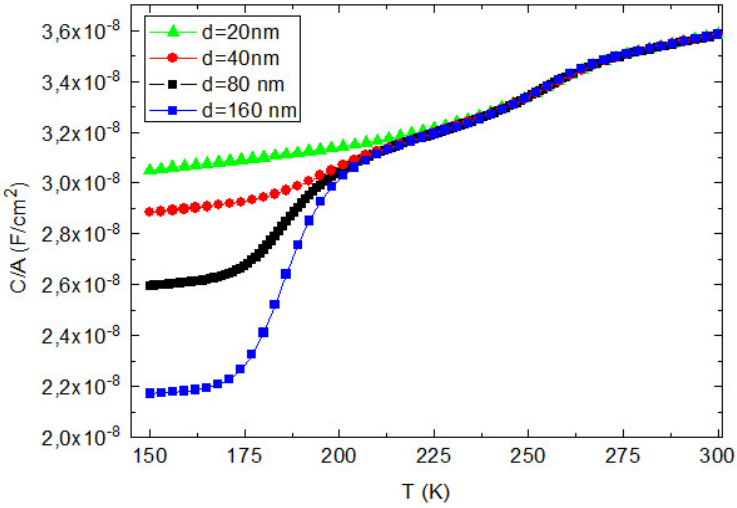

Fig.4.18. Calculated C-T curves for ΔE_V = 0.47 eV at f=12.8 kHz for different thicknesses of a-Si:H layer (μ_p = 1 $cm^2V^{-1}s^{-1}$ and $\sigma_p = 7\times10^{-16}$ cm^2).

As it was expected the change of the a-Si:H layer thickness influences considerably the low temperature step without bringing any change to the other step. The low temperature capacitance is equal to the two capacitances put in series: the geometrical capacitance of a-Si:H layer defined as $\varepsilon A/d^{a\text{-}Si:H}$ and the capacitance of c-Si. The low temperature step becomes less pronounced for very thin a-Si:H layer since the thickness is close to the Debye length in the material and small variation of capacitance can be perceived between two limit values in a-Si:H: $\varepsilon A/d^{a\text{-}Si:H}$ and $\varepsilon A/L_D{}^{a\text{-}Si:H}$. In order to study the influence of the Debye length on the low temperature step *C-T* curves were modeled for different values of $N(E_F)^{a\text{-}Si:H}$. The *C-T* curves are shown in Fig.4.19.

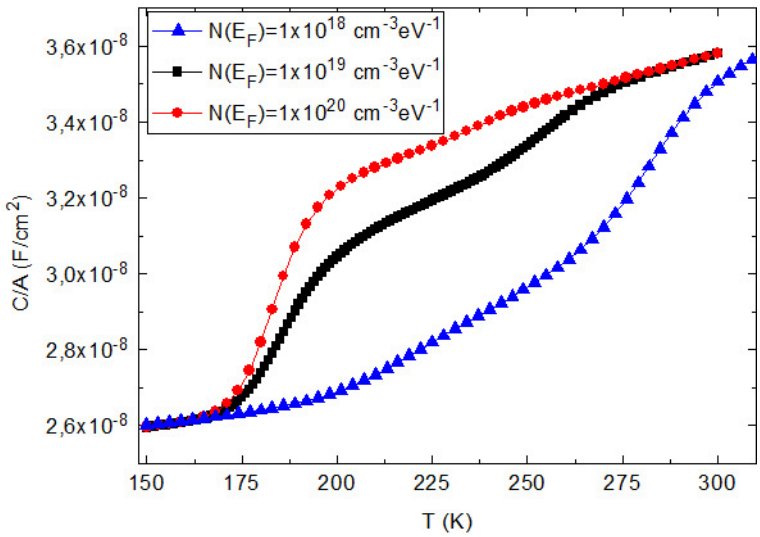

Fig.4.19. Calculated C-T curves for ΔE_V = 0.47 eV at f=12.8 kHz for different values of $N(E_F)^{a\text{-}Si:H}$ in the a-Si:H layer ($d^{a\text{-}Si:H}$ = 80 nm, μ_p = 1 $cm^2V^{-1}s^{-1}$ and $\sigma_p = 7\times10^{-16}$ cm^2).

The increase of the DOS at the Fermi level results in the lower value of the Debye length, $L_D^{a\text{-}Si:H}$, and thus the capacitance increases, that can be observed in Fig.4.19. The shift of the high temperature capacitance step for $N(E_F)^{a\text{-}Si:H} = 1\times10^{18}$ $cm^{-3}eV^{-1}$ is due to the change of the potential's distribution at the interface that will be discussed further.

The increase of the hole mobility influences dramatically the high temperature step. The activation energy of the step for the very high values of the hole mobility is around 0.44 eV, which corresponds to $(E_F\text{-}E_V)^{a\text{-}Si:H}$ at the interface. Since the change of the mobility influences considerably the *C-T* curves we may conclude that transport of carriers affects the capacitance signal. The presence of only one step at high values of μ_p and the vanishing of the low temperature step can be explained as follows. As it was shown in Chapter 3 for the simple case of an a-Si:H Schottky barrier there is a competition between two processes: transport of charge carriers and capture-release. The contribution of each process into the position of T_0 is defined by its characteristic time depending on the capture cross section for capture-emission processes and on the carrier mobility for transport. The slowest process would be determinant for the onset of the capacitance signal. Here one can see that the change of the mobility up to μ_p = 1000 $cm^2V^{-1}s^{-1}$ results in the limitation of the capture-response processes by the low capture cross section value. Therefore, the corresponding step takes places at the temperature superior to the T_0 of the step related to the modulation of the hole's concentration at the interface and cannot be perceived due to smaller charge variation, as it was discussed above. Indeed, for the higher values of $\sigma_p = 7\times10^{-14}$ cm^2 and $\mu_p = 1\times10^5$ $cm^2V^{-1}s^{-1}$ $T_{0\,low}$ is reduced due to the increase of σ_p and again two steps can be observed as it is shown in Fig.4.20.

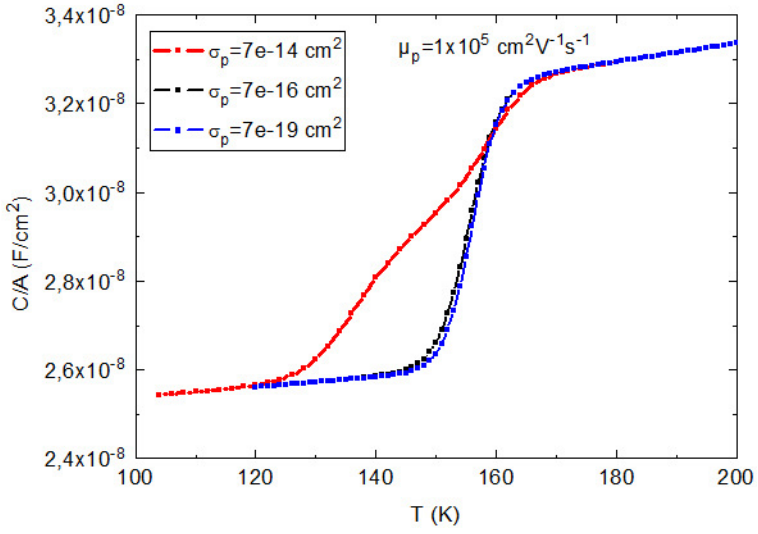

Fig.4.20. Calculated C-T curves for different values of capture cross section of holes in a-Si:H at f=12.8 kHz ($\mu_p=1\times10^5$ $cm^2V^{-1}s^{-1}$).

The activation of the response of the holes in the strong inversion layer is defined by the

term $(E_F\text{-}E_V)^{a\text{-}Si:H}$ at the interface, since holes have to overcome the barrier to be exchanged and evacuated by the a-Si:H layer. At high values of the hole mobility and for the values of capture cross section $\sigma_p = 7\times10^{-16}$ cm^2 and $\sigma_p = 7\times10^{-19}$ cm^2 the activation energy of the only step is $E_a = 0.46\pm0.04$ eV, which indeed corresponds to $(E_F\text{-}E_V)^{a\text{-}Si:H}$ at the interface. The increase of the hole mobility promotes the transport to the electrodes. In order to assign explicitly the obtained activation energy to $(E_F\text{-}E_V)^{a\text{-}Si:H}$ at the interface, the case of $N(E_F)^{a\text{-}Si:H} = 1\times10^{18}$ cm^{-3}eV^{-1} was considered with the band diagram shown in Fig.4.21.

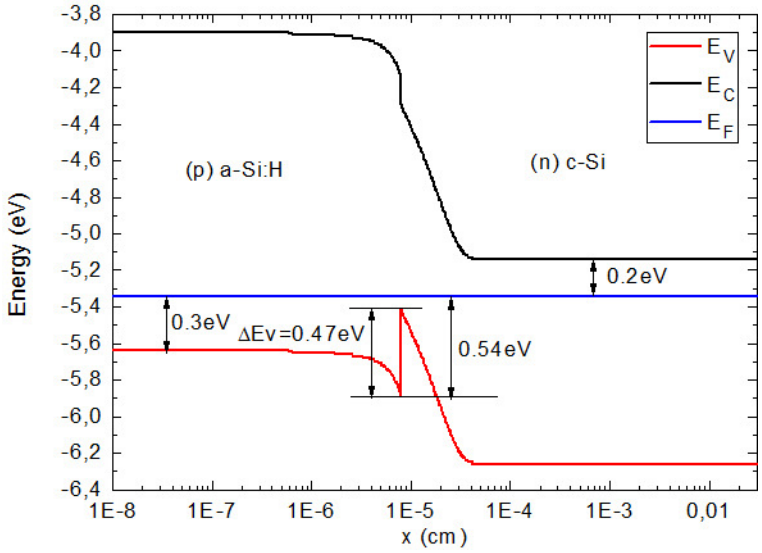

Fig.4.21. Calculated equilibrium band diagram of (p) a-Si:H/ (n) c-Si heterojunction at 300 K for a valence band offset value $\Delta E_V = 0.47$ eV and $N(E_F)^{a\text{-}Si:H} = 1\times10^{18}$ cm^{-3}eV^{-1}.

The decrease of the DOS at the Fermi level in a-Si:H changes the potential distribution between a-Si:H and c-Si layers. The potential drop in c-Si is reduced while $V_d^{a\text{-}Si:H}$ is increased. Due to this redistribution the strong inversion layer is less pronounced and the concentration of holes at the interface is reduced. In Fig.4.19 it is shown that $T_{0\ high}$ is shifted to higher temperatures and the activation energy for this high temperature step is equal 0.54 eV that corresponds exactly to $(E_F\text{-}E_V)^{a\text{-}Si:H}$ at the interface (see Fig.4.21).

All obtained activation energies for ΔE_V=0.47 eV are presented in Table 4.1.

$(E_F-E_V)^{a\text{-}Si:H}$ (eV)	μ_p ($cm^2V^{-1}s^{-1}$)	σ_p (cm^2)	E_{a1} (eV)	E_{a2}(eV)
0.2	1	7×10^{-16}	0.18	0.44
0.3	1	7×10^{-14}	0.28	0.46
	1	7×10^{-16}	0.31	0.45
	1	7×10^{-19}	0.42	
	100	7×10^{-16}	0.28	0.47
	1000	7×10^{-14}	0.29	0.50
	1000	7×10^{-16}	0.49	
	1000	7×10^{-19}	0.46	
	1×10^5	7×10^{-14}	0.28	0.48
	1×10^5	7×10^{-16}	0.44	
	1×10^5	7×10^{-19}	0.47	
0.35	1	7×10^{-16}	0.34	0.46

Table 4.1. Activation energis E_{a1} and E_{a2} of low and high temeperature capacitance steps (when applicable), respectively, extracted from C-T curves calculated for various input values of position of the Fermi level, hole mobility and defect capture cross sections in a-Si:H ($N(E_F)^{a\text{-}Si:H} = 1\times10^{19}\ cm^{-3}eV^{-1}$). The valence band offset was set at 0.47 eV.

As an illustrative example of the discussion presented above, a simplified equivalent scheme of a heterojunciton is shown in Fig.4.22. At low temperatures the total junction capacitance consists of two capacitances put in series: geometrical capacitance of a-Si:H, $\varepsilon A/d^{a\text{-}Si:H}$, and the capacitance of c-Si, $\varepsilon A/w$. With the increase of temperature the capture-release processes in a-Si:H are activated at a cutoff frequency ω_0 so that $(R_\mu^{a\text{-}Si:H} + R_d^{a\text{-}Si:H})\cdot C_d^{a\text{-}Si:H} = 1/\omega_0$, where $R_\mu^{a\text{-}Si:H}$ is the resistance related to transport, $R_d^{a\text{-}Si:H}$ to the time response of the gap states, and $C_d^{a\text{-}Si:H}$ is the capacitance associated to reponse of the defects, $\varepsilon A/L_D^{a\text{-}Si:H}$. Further increase of temperature results in the activation of the response of holes in the strong inversion layer with the activation energy $(E_F-E_V)^{a\text{-}Si:H}$ at the interface. This response provides for a low current path through R_{inv} and C_{inv}, resistance and capacitance associated to the time response of holes in the strong inversion layer, respectively. Thus, at high temperatures the total junction capacitance is defined by two capacitances put in series: C_{inv} and $\varepsilon A/w\text{-}x_{inv}$, where x_{inv} is the width of the strong inversion layer.

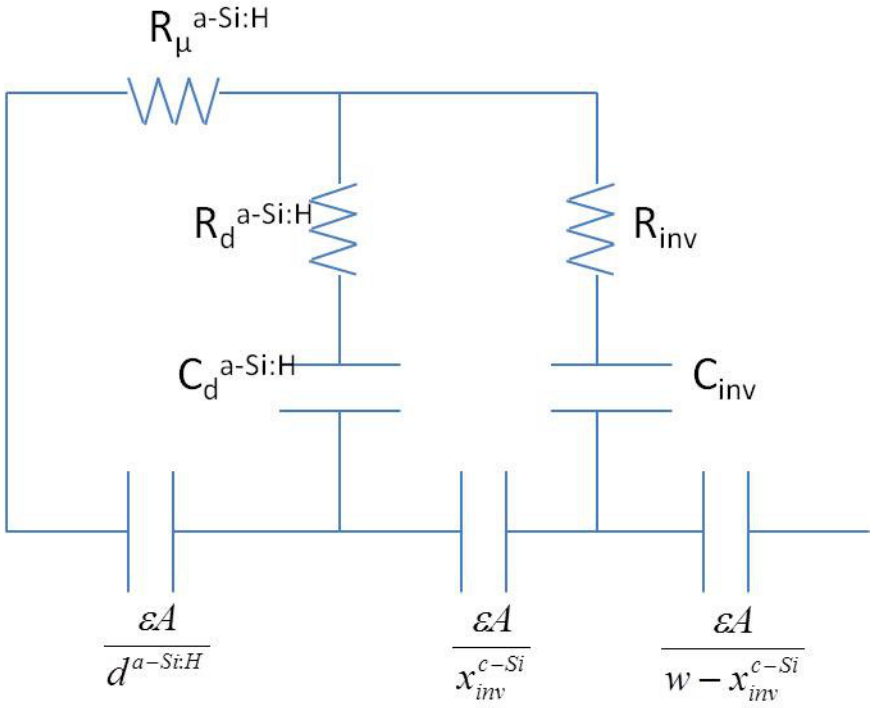

Fig.4.22. Simplified equivalent scheme of a (p) a-Si:H/(n) c-Si heterojunction. $R_\mu^{a\text{-}Si:H}$ is the resistance related to transport, $R_d^{a\text{-}Si:H}$ to the time response of the gap states, $C_d^{a\text{-}Si:H}$ is the capacitance associated to reponse of the defects, $\varepsilon A/L_D^{a\text{-}Si:H}$. R_{inv} and C_{inv} are the resistance and the capacitance associated to the time response of holes in the strong inversion layer of the width x_{inv}, respectively.

In order to study the influence of the inversion layer more carefully heterojunctions with different values of ΔE_V were modeled. Keeping the positions of the Fermi levels the same in both materials we tested a much lower value of ΔE_V, ΔE_V = 0.2 eV knowing that no strong inversion layer at the interface exists for this value of the valence band offset [5]. The comparison of the *C-T* curves for μ_p = 1 $cm^2V^{-1}s^{-1}$ and σ_p = 7×10^{-16} cm^2 is presented in Fig.4.23.

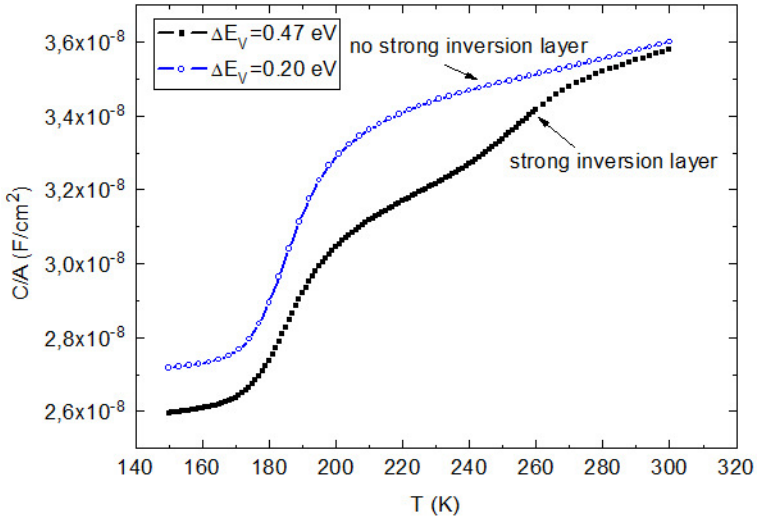

Fig.4.23. Calculated C-T curves for ΔE_V = 0.2 eV and ΔE_V = 0.47 eV at f=12.8 kHz (μ_p = 1 $cm^2V^{-1}s^{-1}$ and $\sigma_p = 7\times10^{-16}$ cm^2).

The main difference between the two curves in Fig.4.23 is the presence of only one capacitance step at low temperatures for ΔE_V = 0.2 eV that has an activation energy of 0.29 eV. Thus, by reducing the valence band offset we suppressed the strong inversion layer at the interface and no response of the holes in c-Si can be observed on the *C-T* curve. Only the expected capture-emission processes of holes in the bulk of the amorphous layer are seen with the activation energy corresponding to the bulk value of $(E_F\text{-}E_V)^{a\text{-}Si:H}$. We can also observe that the low temperature capacitance value differs as well for the two compared curves in Fig.4.23. This is due to the smaller depletion layer width in the crystalline silicon for ΔE_V = 0.2 eV that is the result of the reduced potential drop in c-Si.

We varied separately the hole mobility and the hole capture cross section as it was done for the case of ΔE_V = 0.47 eV. For all studied cases only one capacitance step was observed with the activation energy lying within the range 0.29-0.32 eV, i.e. equal within determination errors to the value $(E_F\text{-}E_V)^{a\text{-}Si:H}$ in the bulk. The results are presented in Table 4.2.

$(E_F\text{-}E_V)^{a\text{-}Si:H}$ (eV)	μ_p ($cm^2/V\cdot s$)	σ_p (cm^2)	E_a (eV)		
			ΔE_V=0.47 eV		ΔE_V=0.20 eV
0.3	1	7×10^{-16}	0.31	0.45	0.29
	1	7×10^{-19}	0.42		0.31
	100	7×10^{-14}	0.32		0.31
	100	7×10^{-16}	0.28	0.47	0.33

Table 4.2. Activation energy E_a of the capacitance step in C-T curves calculated for two input values of the valence band offset ΔE_V, hole mobility (μ_p) and hole capture cross section (σ_p) in a-Si:H. The Fermi level position in a-Si:H was set at 0.3 eV. In some cases, only one step could be observed on the C-T curves, leading to only one value of the activation energy.

Finally, for $\Delta E_V = 0.2$ eV we observed that changing of the mobility and the capture cross section both influences the position of the turn-on temperature. Thus, both transport of carriers and capture-release processes influence the capacitance-temperature dependencies and are involved in the determination of the position of the capacitance step.

4.2.2 Experimental results. Comparison with modeling

We present here some experimental results of capacitance measurements performed on (p) a-(Si:H/(n) c-Si heterojunctions. The samples were fabricated at Helmholtz-Zentrum Berlin für Materialien und Energie and at CEA-INES.

The typical structure is shown in Fig.4.24.

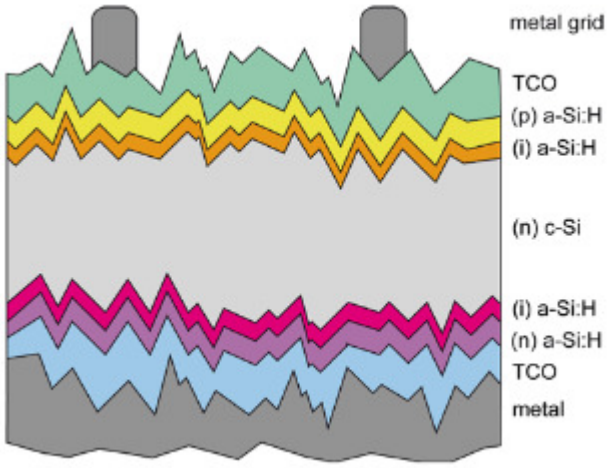

Fig.4.24. Basic structure of the investigated (p) a-Si:H/(n) c-Si heterojunction solar cell [from 29].

The HZB solar cells consist of float zone grown c-Si wafers (1–2 Ω cm, 200 µm thick, 〈1 0 0〉 oriented) treated by a sequence consisting of (1) standard RCA cleaning, (2) KOH/IPA pyramid etching, and (3) second RCA cleaning. Immediately before a-Si:H deposition, the wafers were etched in hydrofluoric acid (HF) (1% in H_2O, 1 min). This removes the oxide grown in the last cleaning step and passivates the surface by hydrogen. The

substrates were then introduced into the loadlock of the PECVD system and pumped down to a pressure P lower than 5×10^{-7} mbar. The *a*-Si:H layers were deposited in a conventional parallel plate RF-PECVD reactor at an excitation frequency of 13.56 MHz, using silane (SiH_4) as a precursor gas. Identical deposition conditions were maintained: base pressure lower than 5×10^{-7} mbar, RF power of 9 mW/cm^2. Doping of a-Si:H was achieved by mixing SiH_4 with H_2-diluted PH_3 for *n*-type and H_2-diluted B_2H_6 for *p*-type doping, respectively. The deposition temperature in both cases was adjustable between 60 °C and 300 °C. The p/n heterojunction was formed on the front side of the structure, and an a-Si:H layer with the same conductivity type as the c-Si wafer is deposited on the rear to obtain a Back Surface Field (BSF). Reactively sputtered ZnO:Al was used as a transparent conducting oxide, and aluminum is evaporated by electron beam (e-beam) to form the rear and front contact. The solar cells were finished by defining the front grid in a photolithographic lift-off process and the emitter area (1 cm^2) by mesa etching. More details on the fabrication can be found in Refs. [23,24].

The solar cell fabricated at CEA-INES were obtained as follows. The amorphous silicon layers deposition has been done on high quality FZ *n*-type monocrystalline 125 psq wafers (<100>; 200µm; 1-5Ω·cm) cleaned to remove the native oxide by a short 2% HF dip. The amorphous silicon layers were processed using a 13.56 MHz PECVD parallel-plate reactor at low substrate temperature (200°C). The deposition pressure, the inter-electrode distance, and the RF power were fixed. A gas mixture of SiH_4, H_2, B_2H_6, and CH_4 was used. Thin buffer layer was introduced just before deposition of the p-doped layer to enhance passivation. Total thickness of (i)+(p) a-Si:H stack was 12 nm. As BSF layer the stack (i)+(n) a-Si:H was used. The samples were then cleaned and textured. Finally, the front side is finished by ITO and a screen printed grid while the back side is a ZnO:B /Al stack. More details on the fabrication are presented in Refs. [25-29].

The capacitance measurements were carried out with an Agilent E4981A capacimeter that operates in small-signal mode (V_{ac} = 20 mV) at different frequencies. The samples were placed in a cryostat that is pumped to reach the vacuum of 10^{-5} mbar. The temperature was varied in the range 77 K - 320 K. During the measurements samples should be kept in the dark in order to avoid the photogeneration of the carriers. The *C-T* dependence obtained on one of HZB samples is presented in Fig. 4.25.

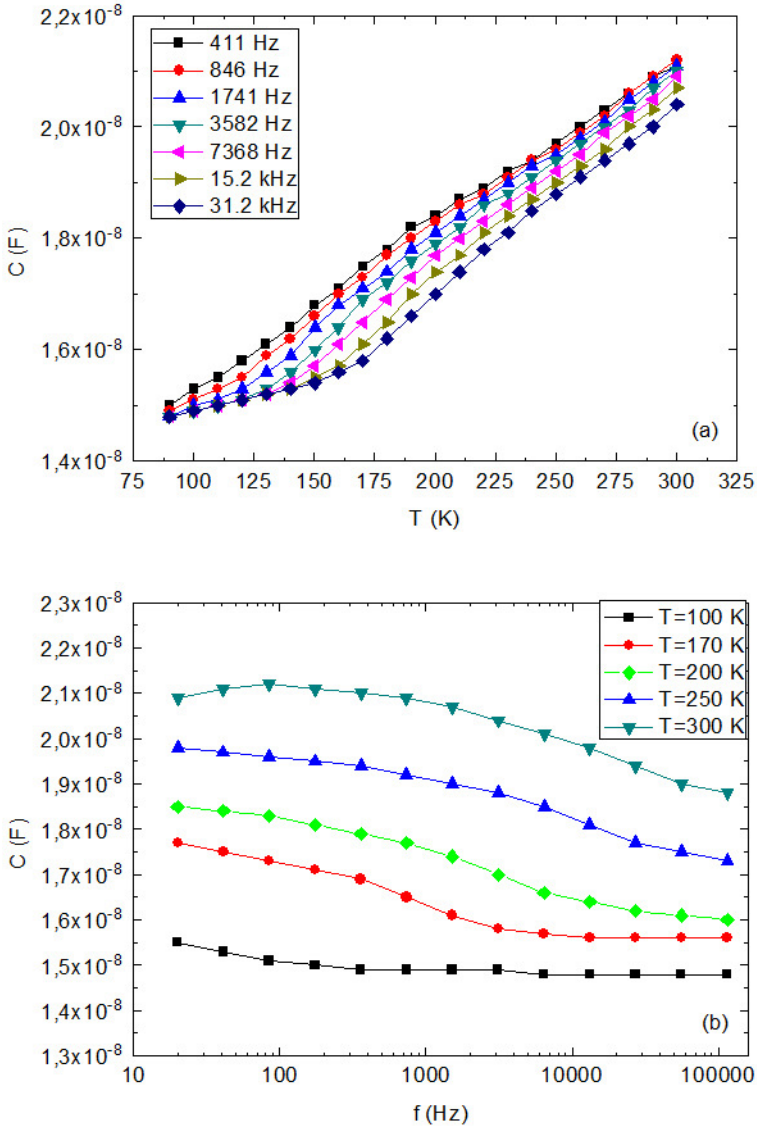

Fig.4.25. (a) Experimentally obtained C-T curves on HZB (p) a-Si:H/(n) c-Si sample; (b) capacitance-frequency curves at different temperatures of HZB (p) a-Si:H/(n) c-Si sample.

In Fig.4.25(a) one can see a step at low temperatures that shifts to higher temperatures with the increase of frequency. In Fig. 4.25(b) we present *C-f* curves for different temperatures. Again one can clearly observe a step on the *C-f* curves that shifts to higher frequencies as the temperature increases. The derived activation energy of this step is 0.29 eV. This value can be interpreted as the position of the Fermi level in the (p) amorphous layer. In the range 250-275 K another peculiarity can be observed on the curve that can be considered as a higher temperature step. However, the dispersion of *C-T* curves and overall increase of capacitance with temperature at any frequency (see the following) do not allow one to provide a reliable identification of this possible step.

The *C-T* curves obtained on one of the CEA samples are shown in Fig.4.26.

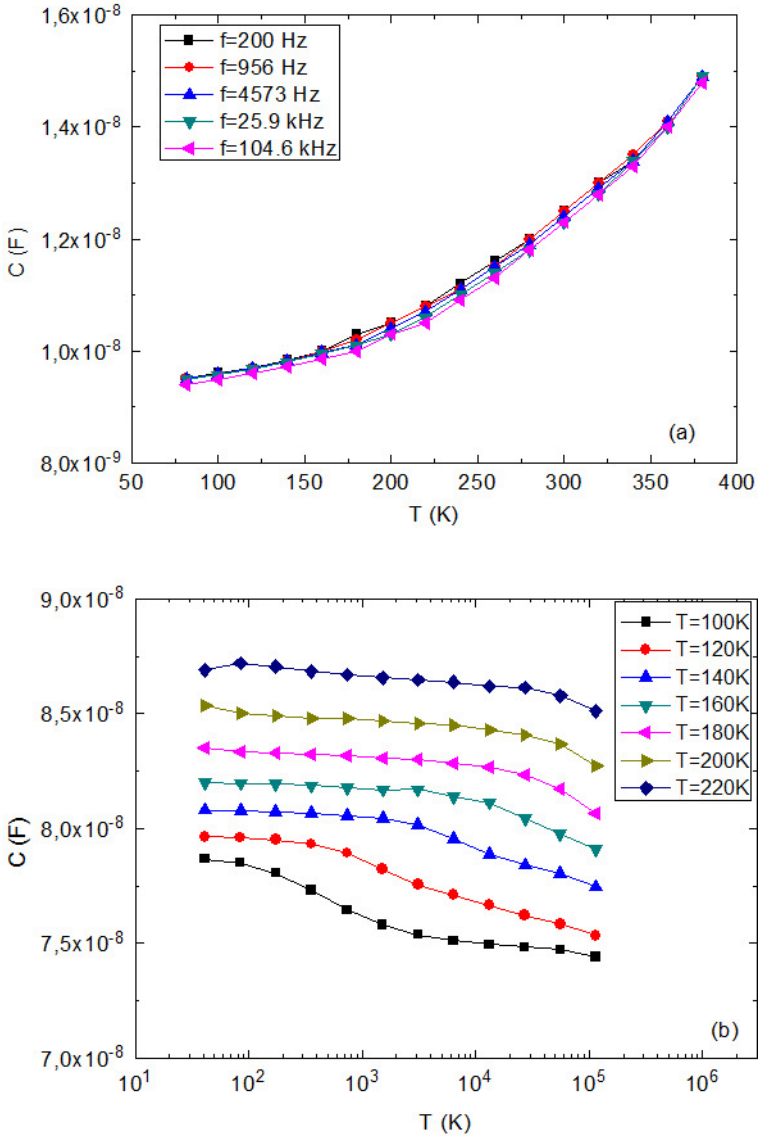

Fig.4.26. (a) Experimentally obtained C-T curves on CEA (p) a-Si:H/(n) c-Si sample; (b) capacitance-frequency curves at different temperatures.

A capacitance step can be observed on the *C-f* curves althought it is not clear if one considers only *C-T* data in Fig.4.26(a). The derived activation energy of this step is 0.08 eV. In order to interpret this value and assign the capacitance step to a concerned process we briefly recall the results of the numerical modeling. We observed two capacitance steps whose activation energies were assigned either to the position of the Fermi level referred to the top of the valence band of a-Si:H in the bulk or at the interface. The activation energy of 0.08 eV is too small to be comparable with either of these two values. The absence of the high temperature step characterized by rather large value of the activation energy can be explained by the absence of the strong inversion layer in which the response of the holes to the small

signal modulation was observed. However, this explanation does not hold true if one considers the overall increase of capacitance with temperature in the quasi-static mode. As it will be shown further, the *C-T* dependencies obtained on the CEA samples are reproduced by the calculation only if the minority carriers' contribution to the charge density in (n) c-Si is taken into account and this way the strong inversion layer is considered.

At this point we provide for an interpretation of the experimental results based on the transport phenomena in (p) a-Si:H. It was demonstrated that the variable range hopping is the dominant transport mechanism in amorphous silicon at low temperatures [30-33]. Between 250 K and room temperature the conduction is provided by charge carriers that are thermally activated across the band gap [31]. In this range amorphous silicon behaves quite like a crystalline semiconductor with a gap of forbidden states. At low temperatures thermal excitation does not take place into the bands anymore and hopping conductivity is observed. Hopping refers to tunneling transitions from occupied to unoccupied localized states near the Fermi level with the assistance of phonons. Indeed, as it is shown in Fig.4.27 at low temperatures the conductivity in (p) a-Si:H is larger by orders of magnitude than the conductivity expected in the case of only thermal excitation of carriers.

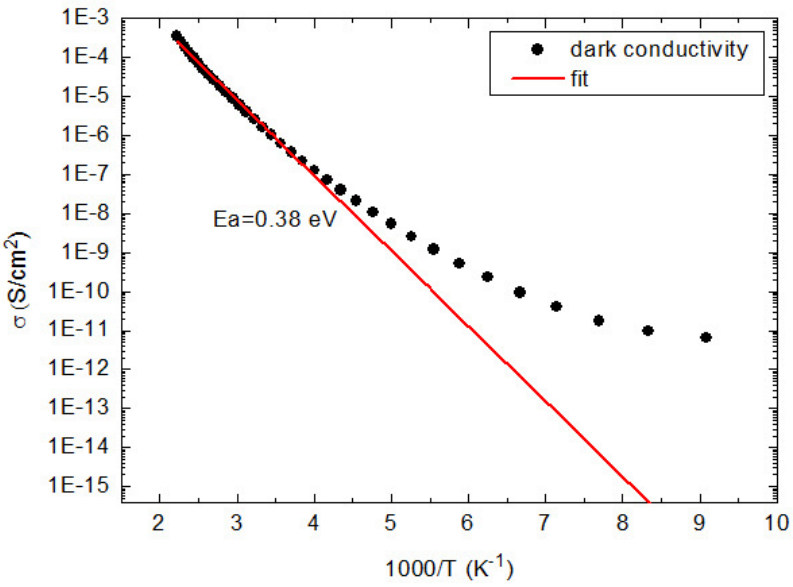

Fig.4.27. Arrhenius plot of the dark conductivity of (p) a-Si:H sample vs 1000/T. Exponential fit represents the expected behavior of the thermal conductivity if the high temperature mechanism remains unchanged.

Thus there should be no limitation due to the transport of charge since the mobility of carriers is high enough. We would like to emphasize that no hopping was considered in the numerical modeling carried out above and the conductivity followed the behavior shown by the exponential fit in Fig.4.27. Therefore, at low temperatures the transport was limited by the

low conductivity in the (p) a-Si:H layer. If hopping is the dominant process in a-Si:H at low temperatures, the filling (emptying) with holes of gap states does not proceed any more through capture (emission) processes from (to) the valence band. Therefore, no activation energy can be attributed to these processes and no capacitance step can be observed.

The high temperature capacitance step due to the modulation of the hole's concentration in the strong inversion layer, as it was shown above, mainly depends on the hole mobility and thus on the transport of holes. The numerically obtained activation energy, being equal to the position of the Fermi level in a-Si:H at the interface, is related to the barrier in the a-Si:H layer at the interface that holes should overpass in order to be collected at the electrodes. Yet holes from the strong inversion layer can tunnel to the band gap in a-Si:H instead of crossing the barrier by thermal activation. In the a-Si:H band gap, holes then flow from on gap state to another until a certain moment when the emission to the valence band becomes more preferable (i.e. the tunneling rate becomes smaller than the rate for hole release from the state tot he valence band). The corresponding activation energy is defined then as the difference between the gap state energy level from which a hole is emitted and the valence band. This energy difference is difficult to determine since there are many possible paths in the band gap for a hole to follow by hopping. The larger the DOS in a-Si:H is, the larger number of gap states are available. Thus, the activation energy of 0.08 eV can be attributed to the small energy difference between the gap level from which holes are emitted and the valence band in a-Si:H. This shematic illustration of these processes is presented in Fig.4.27.

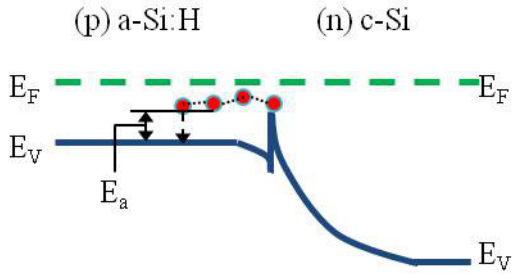

Fig.4.28. The schematic illustation of the holes tunneling from the strong inversion layer to the band gap of a-Si:H and their emission to the valence band with the activation energy E_a.

The multitunneling phenomenon was considered in the work of Matsuura *et al*. for the case of undoped a-Si:H/(p) c-Si heterojunction [34]. The authors suggested the multitunneling capture-emission mechanism as an explanation to the obtained current-voltage characteristics. As proposed by the authors, a hole in the valence band of (p) c-Si flows from one localized state to another in a-Si:H located within an energy range of k_BT by a multitunneling process and keeps flowing until a tunneling rate becomes smaller than the rate for hole release from the state to the valence band of a-Si:H or for recombination of the hole with an electron in the conduction band of a-Si:H. An ending point of tunneling might be close to the edge of the

depletion layer of a-Si:H, where the tunneling rate decreases due to a decrease of electric field. Our system can be regarded somewhat similar if we draw a parallel between the strong inversion layer in c-Si with the significant hole concentration and (p) c-Si layer described in the Ref.[34]. It allows us to expect the same behavior in the case of (p) a-Si:H/(n) c-Si heterojunction with the strong inversion layer in c-Si at the interface.

Considering tunneling and hopping mechanisms we propose a modified version of the equivalent scheme that was presented in Fig.4.22. As it can be senn in Fig.4.29 we introduced the tunneling low resistance R_t that shunts the response of the holes in the strong inversion layer with thelarge activation energy (R_{inv} and C_{inv}), therefore the corresponding capacitance step is not activated. Once holes tunnel to a-Si:H from the inversion layer they flow from one gap state to another by hopping that is represented by the resistance R_h. If hopping is the dominant transport mechanism the thermally activated capture-release processes between the Fermi level and the valence band (R_d^{a-}Si:H and $C_d^{a\text{-}Si:H}$) are not preferable and are shunted by low resistance R_h. As we already mentioned above, there may be an activation energy associated with hopping since at a certain moment a carrier is emitted to the valence band from a gap state. However, its determination is troublesome.

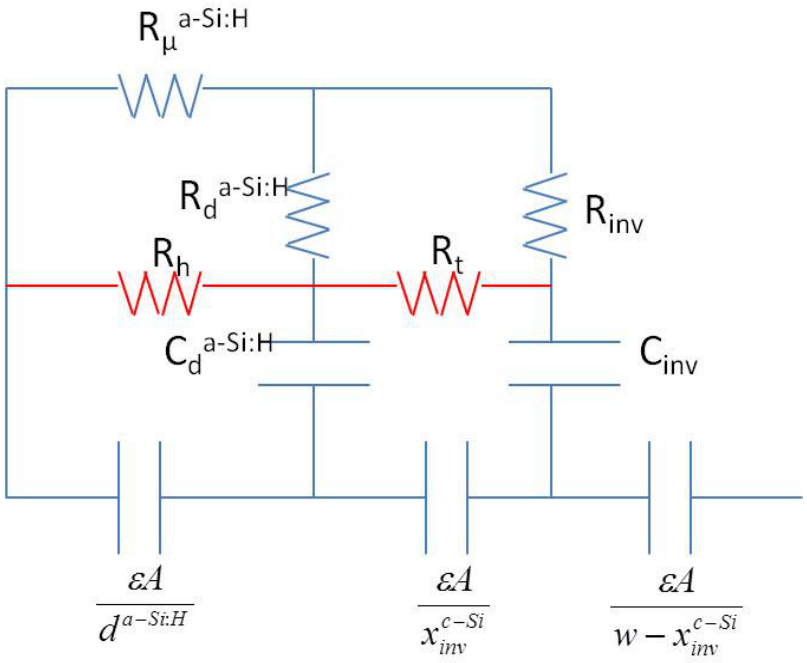

Fig.4.29. Simplified equivalent scheme of a (p) a-Si:H/(n) c-Si heterojunction with tunneling and hopping considered. $R_\mu^{a\text{-}Si:H}$ is the resistance related to transport, $R_d^{a\text{-}Si:H}$ to the time response of the gap states, $C_d^{a\text{-}Si:H}$ is the capacitance associated to reponse of the defects, $\varepsilon A/L_D^{a\text{-}Si:H}$. R_{inv} and C_{inv} are the resistance and the capacitance associated to the time response of holes in the strong inversion layer of the width x_{inv}, respectively. R_h and R_t are the resistances associated with tunneling and hopping, respectively.

Concluding this section we refer to the results obtained in National Renewable Energy Laboratory (NREL) on the capacitance study of the inversion layer in (p) a-Si:H/(n) c-Si heterojunction [35]. The authors observed that the capacitance-frequency dependence exhibits a step at a fixed temperature: the capacitance drops to a lower value above certain frequency f_{peak}. This step can be regarded as the equivalent of the step on a *C-T* curve obtained at a fixed frequency. Arrhenius plot — the logarithm of $2\pi f_{peak} /T^2$ plotted versus the inverse measurement temperature yielded an activation energy E_a = 161 meV at zero bias and E_a = 203 meV at -4V reverse bias. It was suggested by the authors that this activation energy was due to the carrier exchange between the holes in the inverted c-Si and the Fermi level at the a-Si/c-Si interface. This carrier exchange process is thermally activated with its activation energy being the difference between the Fermi level and the c-Si valence band edge at the interface.

This activation energy, although attributed to the same process in the inversion layer, is found to be different than in simulation performed in this thesis. We found the activation energy being equal to the position of the Fermi level in a-Si:H at the interface that is significantly larger that one obtained in the referred work from NREL. The possible explanation to the obtained E_a that is equal to the difference between the Fermi level and the c-Si valence band edge at the interface could be again tunneling of the holes through the barrier at the interface to the band gap of a-Si:H. Thus the energy is needed to activate the holes in the strong inversion layer in c-Si, which then tunnel to the amorphous layer and are collected at the contact. If we compare the results obtained in NREL with the experimental *C-T* curves obtained in this work, we can conclude that we do not observe a considerable activation energy that can be related to the difference between the Fermi level and the c-Si valence band edge at the interface due to the different band diagram at the interface. Indeed, from numerically calculated band diagram we saw that for large valence band offset values the valence band edge in c-Si lies very close or even crosses the Fermi level at the interface. High V_{oc} obtained on CEA samples and study of the quasi-static mode of the capacitance signal presented further allow us to estimate ΔE_V being larger than 0.4 eV, therefore negligible difference between the Fermi level and the valence band edge in c-Si is expected. Regarding this, in CEA samples no considerable energy is needed to modulate the holes in the inversion layer and to collect them on the contacts, if hopping mechanism takes place in a-Si:H.

4.2.3 Conclusions

The numerically obtained temperature and frequency dependencies of a-Si:H/c-Si heterojunction capacitance have been examined. Two capacitance steps have been observed on *C-T* dependencies for typical values of the hole mobility and hole capture cross section μ_p = 1 $cm^2V^{-1}s^{-1}$ and $\sigma_p = 7\times10^{-16}$ cm^2, respectively. The activation energies of the capacitance steps have been attributed to different processes. The low temperature step is characterized by the activation energy that corresponds to the position of the Fermi level in the bulk of

amorphous silicon referred to the top of the valence band. This is related to the transport and the capture-emission of holes by defects in a-Si:H, as detailed in the previous chapter for a-Si:H Schottky diodes. The high temperature step has the activation energy close to the position of the Fermi level in amorphous silicon at the interface referred to the top of the valence band, thus being related to the response of holes in the strong inversion layer at the interface. At low value of the valence band offset (ΔE_V=0.20 eV) the strong inversion layer disappears and only one capacitance step was observed with the activation energy equal to the position of the Fermi level in the bulk of amorphous silicon.

Change of the mobility and the capture cross section influences differently the position of the turn-on temperature of the steps. The low-temperature step depends considerably on the capture cross section while the second step is not affected by the change of the latter. At very low values of σ_p due to the shift of $T_{0\ low}$ to higher temperatures only high temperature step is observed since the capture-release processes are limited by the hole capture cross section and are activated at higher temperatures. However, no step is observed at higher temperature that can be explained by the amplitude of the high temperature capacitance step. Indeed, the charge variation at the interface due to the high hole's concentration is more considerable that that one due to the capture-release processes. Once the modulation of the hole's concentration at the interface is activated the step related to the response of the gap states becomes negligible and therefore cannot be observed on *C-T* curves.

The variation of the hole mobility influences drastically the high temperature step that results in the significant shift of $T_{0\ high}$ to low temperatures. The capture-release processes are influenced as well by the change of μ_p. For high hole mobility values the capture-release of holes is limited solely by the capture cross section value and the corresponding step cannot be observed on *C-T* curves since it is again absorbed by the strong change of capacitance within the high temperature step.

The *C-T* curves obtained experimentally on different samples showed different behavior in the low temperature range. At low temperature a capacitance step can be seen on the *C-T* curveson the HZB samples that can be attributed to the activation of response of gap states to the ac signal. The high capacitance step is not observed clearly, although, a peculiarity at around T = 225 K can be perceived but its further interpretation is complicated.

The *C-T* curves obtained on CEA samples experience a small capacitance step that can be observed more clearly on the *C-f* plot. The activation energy of this step is 0.08 eV. In order to interpret these results we assume hopping as the dominant transport mechanism in a-Si:H at low temperatures. Considering this, the filling (emptying) with holes of gap states does not proceed any more through capture (emission) processes from (to) the valence band, and therefore no activation energy can be attributed to these processes and no corresponding capacitance step can be observed. The absence of the high temperature step with large

activation energy, observed by numerical modeling and related to the response of holes in the strong inversion layer, is again explained by hopping processes. Holes from the strong inversion layer instead of crossing the barrier by thermal activation tunnel to the band gap in a-Si:H. In the band gap in a-Si:H holes then flow from on gap state to another until a certain moment when the emission to the valence band becomes more preferable (i.e. the tunneling rate becomes smaller than the rate for hole release from the state to the valence band). The corresponding activation energy is then defined as the difference between the gap state energy level from which a hole is emitted and the valence band. Thus, the activation energy of 0.08 eV we attributed to the small energy difference between the gap level from which holes are emitted and the valence band in a-Si:H.

4.3 Quasi-static behavior of *C-T* dependencies: band offsets and the inversion layer

In this section we concentrate on the temperature dependence of the low frequency capacitance in a wider temperature range, up to 400 K. As it was shown above at low frequencies from a certain temperature there is no limitation due to transport in a-Si:H and the charges in the a-Si:H space charge region and the inversion layer at the c-Si interface can follow the ac modulation and *C-T* dependencies become independent of the frequency. This behavior can be considered as quasi-static. Thus here we will focus on the quasi-static mode of *C-T* dependencies and will show that it is influenced by the presence of the strong inversion layer.

The classical depletion approximation for junction's capacitance will be recalled. The explicit analytical calculation of the junction capacitance taking into account the existence of a strongly inverted surface layer at the c-Si surface, as earlier evidenced from other experimental techniques, will be presented. Within this complete calculation we focus on two main features of interest: capacitance-temperature dependencies at zero bias and capacitance-voltage dependencies at different temperatures. The analytically obtained results will be compared with experimental data and the possibility of analyzing the band diagram and extracting the valence band offset will be discussed.

4.3.1 Calculation of the junction's capacitance: depletion approximation

In the quasi-static mode, for the case of (p) a-Si:H/(n) c-Si heterojunctions we consider that all gap states in a-Si:H respond to the ac modulation. The capacitance of the amorphous

layer is then $C^{a-Si:H} = \varepsilon A / L_D^{a-Si:H}$, $L_D^{\text{a-Si:H}} = \sqrt{\varepsilon / q^2 N(E_F)^{a-Si:H}}$ being the Debye length in a-Si:H associated to the density of states (DOS) at the Fermi level, $N(E_F)^{a\text{-}Si:H}$. In c-Si the classical depletion approximation neglects minority carriers and assumes total depletion of majority carriers in the space-charge region to a depth w in c-Si, and perfect charge neutrality beyond w. Then we have the well-known expression for the capacitance $C_{c\text{-}Si} = \varepsilon A/w$. Since the permittivity of a-Si:H can be considered equal to that of c-Si the total capacitance is then written as

$$\frac{C}{A} = \frac{\varepsilon}{L_D^{a-Si:H} + w}, \tag{4.13}$$

where w is defined through [36]

$$V_d^{c-Si} - \frac{k_B T}{q} = \frac{q N_D^{c-Si}}{2\varepsilon} w^2 \tag{4.14}$$

The correction factor k_BT/q instead of $2k_BT/q$ was introduced due to only one majority-carrier distribution tail at the edge of the depletion region in c-Si.

We here assume that that the Debye length in a-Si:H is smaller than the layer thickness, so that the a-Si:H layer can be considered as semi infinite [37]. In order to obtain capacitance-temperature dependencies it is necessary to find an explicit expression for $w=f(T)$. For this purpose we write the charge neutrality condition leaving out the interface charge that is negligible in good electronic quality devices like high efficiency solar cells:

$$Q^{c-Si} + Q^{a-Si:H} = 0, \tag{4.15}$$

where $Q^{c\text{-}Si}$ and $Q^{a\text{-}Si:H}$ are the charges per unit area in c-Si and a-Si:H, respectively, given by:

$$Q^{c-Si} = q N_D^{c-Si} w = q N_D^{c-Si} \sqrt{\frac{2\varepsilon}{q N_D^{c-Si}} \left(V_d^{c-Si} - \frac{k_B T}{q} \right)}, \tag{4.16}$$

and

$$Q^{a-Si:H} = \varepsilon \frac{V_d^{a-Si:H}}{L_D^{a-Si:H}}, \tag{4.17}$$

where $V_d^{c\text{-}Si} = V(w) - V(0)$ and $V_d^{a\text{-}Si:H} = V(-\infty) - V(0)$ are the potential drops in c-Si and a-Si:H, respectively. Knowing that $qV_d^{a\text{-}Si:H} + qV_d^{c\text{-}Si} = qV_d$ and using Eq.(4.15) we obtain the

expression for the potential drop in crystalline silicon:

$$V_d^{c-Si} = \frac{1}{2}\left[2V_d + V_1 - \sqrt{V_1(4V_d + V_1 - \frac{4k_BT}{q})} \right], \tag{4.18}$$

where

$$V_1 = \frac{2qN_D^{c-Si}L_D^{a-Si:H\,2}}{\varepsilon} \tag{4.19}$$

The depletion width then can be written according to Eq.(4.14), using the potential drop in c-Si defined in Eq.(4.18). Thus capacitance-temperature dependency can be expressed through the temperature dependency of the diffusion potential V_d and consequently of all the parameters entering in V_d from Eq.(4.3):

$$qV_d = E_g^{c-Si} + \Delta E_V - \delta^{c-Si} - \delta^{a-Si:H} \tag{4.20}$$

Capacitance-temperature dependencies were calculated for different values of the band offset (ΔE_V), density of states in a-Si:H, doping density in c-Si and a-Si:H. Our main objective was to fit the experimental results with the capacitance data obtained from the depletion approximation calculations. In our calculations we did not introduce the thin intrinsic layer of amorphous silicon that is present in the measured samples.

Introducing the (i) a-Si:H layer does not bring any change to *C-T* curves at high temperature (above 200 K) obtained by numerical modeling at low frequencies, as it will be shown in Section 4.4.1. Indeed since the thickness of the intrinsic layer is estimated to be in the range 1-5 nm, it does not modify significantly the band bending. Nor does it act as a pure dielectric layer, since at considered frequencies and temperatures the gap states can follow the ac modulation.

4.3.1.1 Failure of the depletion approximation to reproduce experimental *C-T* data

In Fig.4.30 we compare experimental *C-T* data to those calculated from the depletion approximation using the parameters listed in Table 4.3.

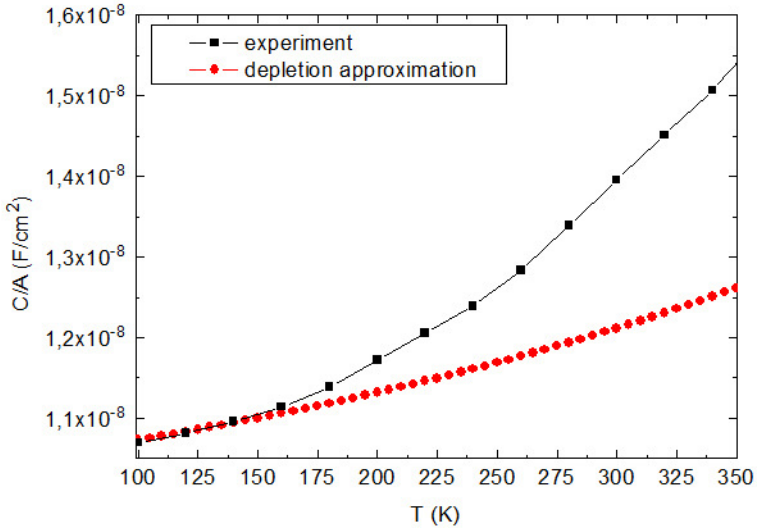

Fig.4.30. Comparison of experimental data with the C-T curve obtained from the depletion approximation calculation.

Parameter	Value
ΔE_V - $\delta^{a\text{-}Si:H}$ (eV)	0.1-0.5
$N(E_F)^{a\text{-}Si:H}$ ($eV^{-1}cm^{-3}$)	1×10^{19}
$\delta^{c\text{-}Si}$	$k_B T ln \frac{N_C^{c-Si}(T)}{N_D}$
$N_V^{c\text{-}Si}$ (cm^{-3})	$3\times10^{19}\cdot((T/300)^{1.85})$ [38]
$N_C^{c\text{-}Si}$ (cm^{-3})	$2.86\times10^{19}\cdot((T/300)^{1.58})$ [38]
$N_D^{c\text{-}Si}$ (cm^{-3})	1.5×10^{15} (measured independently by four-probe resistivity and quasi-steady-state photo conductance methods)
$E_g^{c\text{-}Si}$ (eV)	$1.1692-4.9\times10^{-4}\cdot T^2/(T+655)$ [39]

Table 4.3. Parameters used in depletion approximation calculations for the C-T data from Fig.27.

The calculation of the temperature dependency of the diffusion potential V_d implies knowing the variation with temperature of all parameters in Eq.(4.20):

$$qV_d(T) = E_g^{c-Si}(T) - \delta^{c-Si}(T) + \Delta E_V(T) - \delta^{a-Si:H}(T) \tag{4.21}$$

The variation with temperature of the band gap in crystalline silicon is well-known [39]. The temperature dependence of the position of the Fermi level in (n) c-Si is defined by:

$$\delta^{c-Si}(T) = k_B T ln \frac{N_C^{c-Si}(T)}{N_D} \quad , \tag{4.22}$$

where $N_C^{c\text{-}Si}(T)$ is known from Ref.[38].

The values and temperature dependencies of the two last terms in Eq.(4.21) are still subjects of discussion. To the first order, we can assume a linear temperature dependence:

$$\Delta E_V(T) = \Delta E_V(0) - \alpha_V T \quad , \tag{4.23}$$

$$\delta^{a-Si:H}(T) = \delta^{a-Si:H}(0) - \alpha_F T \quad , \tag{4.24}$$

so that

$$\Delta E_V(T) - \delta^{a-Si:H}(T) = \Delta E_V(0) - \delta^{a-Si:H}(0) - \alpha T \quad , \tag{4.25}$$

$$\alpha = \alpha_V + \alpha_F \quad , \tag{4.26}$$

where α_F and α_V are the temperature coefficients of the Fermi level position and the valence band offset, respectively, and $\Delta E_V(0)$ and $\delta^{a\text{-}Si:H}(0)$ are corresponding values at $T = 0$ K.

In Fig.4.31 we present capacitance-temperature dependencies calculted from the depletion approximation for different $\Delta E_V(0)$ - $\delta^{a\text{-}Si:H}(0)$ values with $\alpha = 0$.

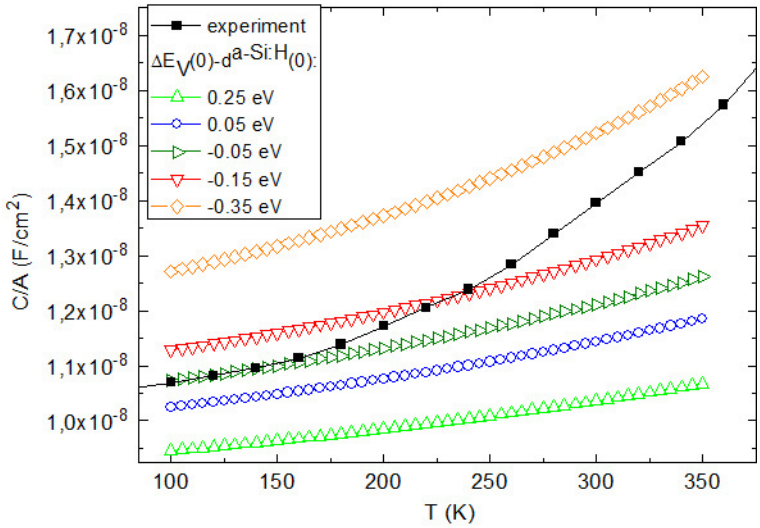

Fig.4.31. Comparison of experimental data with the C-T curves obtained from the depletion approximation calculation for different input values of $\Delta E_V(0) - \delta^{a\text{-}Si:H}(0)$ *with no temperature dependence considered.*

One can see that at low temperatures the best reproduction of the experimental data is achevied for $\Delta E_V(0) - \delta^{a\text{-}Si:H}(0) = -0.05$ eV. In Ref.[37] it was shown that the valence band offset value at 0 K is equal to 0.4 eV and its variation with temperature can be neglected, thus $\alpha_V = 0$. Using this value for $\Delta E_V(0)$ we obtain for the position of the Fermi level in (p) a-Si:H $\delta^{a\text{-}Si:H}(0) = 0.45$ eV.

Since no temperature variation of the valence band offset can be considered, only temperature dependence of the position of the Fermi level in (p) a-Si:H determines the term $\Delta E_V(T) - \delta^{a\text{-}Si:H}(T)$. This temperature dependence of the Fermi level is referred as statistical shift and it occurs because charge neutrality has to be maintained in the layer when the temperature varies [40]. The activation energy obtained from dark conductivity measurements in doped a-Si:H has to be corrected for the statistical shift if one wants to assess the $(E_F - E_V)$ term. The statistical shift of the Fermi level in *p*-type a-Si:H was studied in the work of Kazanskii and Kuznetsov [41]. It was shown that for heavily doped samples, E_F moves to the middle of the mobility gap in the low temperature region. On the contrary, for temperatures $T > 360$K the value of $E_F - E_V$, decreases when the temperature rises. The temperature coefficient of $(E_F - E_V)$ in high temperature range was found at – (2 to 3) $\times 10^{-4}$ eV/K. Considering this ambiguity in the temperature dependence of the Fermi level in *p*-type a-Si:H we decided to explore a range of values of the temperature coefficient: from -6×10^{-4} eV/K to 4×10^{-4} eV/K. Considering the values of $\Delta E_V(0)$ and $\delta^{a\text{-}Si:H}(0)$ that provided for the best reproduction of the experimental data in Fig.4.31, we calculated *C-T* dependencies introducing various temperature coefficients α. The corresponding curves are shown in Fig.4.32.

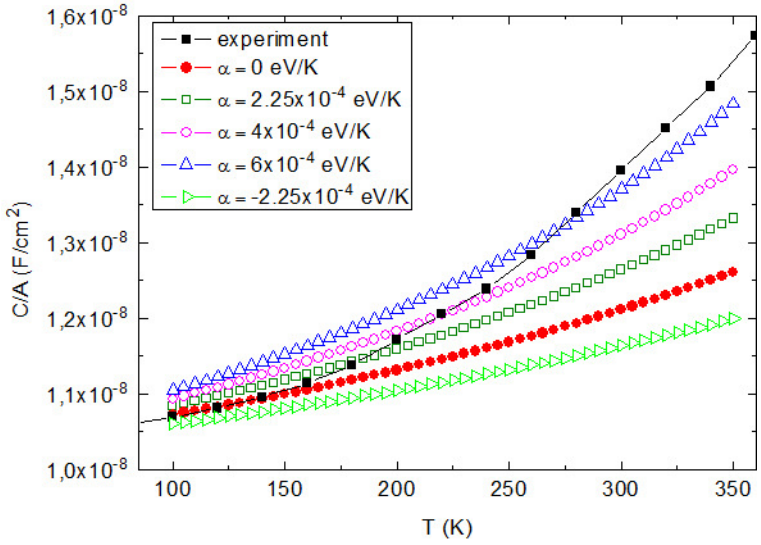

Fig.4.32. Comparison of experimental data with the C-T curves obtained from the depletion approximation calculation for different input values of temperature coefficient α for $\Delta E_V(0) - \delta^{a\text{-}Si:H}(0) = -0.05$ *eV.*

Changing the temperature dependence of the ΔE_V-$\delta^{a\text{-}Si:H}$ allows one to slightly change the behavior of capacitance-temperature curve as it can be seen in Fig.4.32. However, all values of the temperature coefficient α up to 1×10^{-3} eV/K do not provide for a satisfactory fit of the experimental capacitance data as shown in Fig.4.33. The value of $\alpha = 1\times10^{-3}$ eV/K implies too enhanced temperature dependence of $\delta^{a\text{-}Si:H}$. Furthermore, the value of $\delta^{a\text{-}Si:H}$ at T = 300 K is decreased in comparison with $\delta^{a\text{-}Si:H}$ (0) that contradicts the observations of Kazanskii. The absolute value of the temperature coefficient was estimated to lie in the range 3k-6k [33], which is much lower than $\alpha = 1\times10^{-3}$ eV/K. Therefore, none of the acceptable values of α is able to correctly reproduce the experimental capacitance increase with temperature that is always more pronounced than obtained within the depletion approximation calculation.

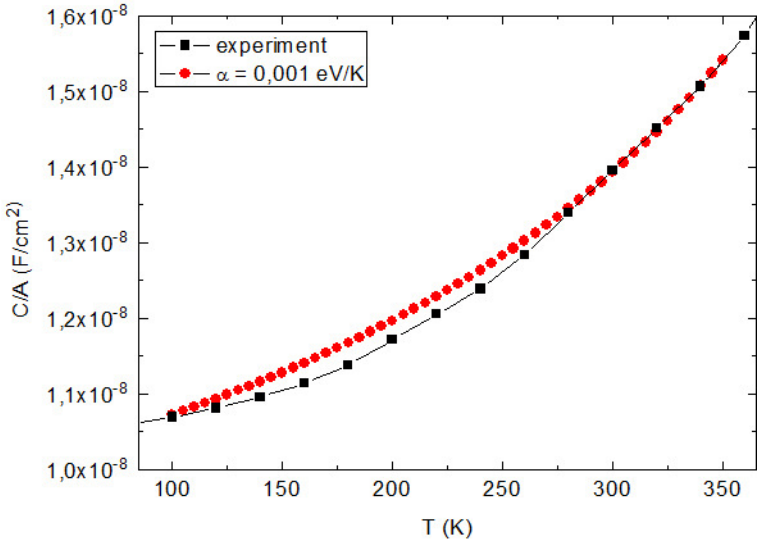

Fig.4.33. Comparison of experimental data with the C-T curve obtained from the depletion approximation calculation for temperature coefficient $\alpha = 1\times10^{-3}$ *eV/K* ($\Delta E_V(0) - \delta^{a\text{-}Si:H}(0) = 0.05$ *eV).*

4.3.2 Calculation of the junction capacitance: complete analytical calculation

As it was shown previously the depletion approximation does not allow one to reproduce closely the experimentally obtained *C-T* data. Therefore another approach should be developed without any approximations. Our objective is to provide the complete analytical calculation of the junction capacitance that takes into account the influence of the minority carriers and the potential drop in the c-Si without using the depletion approximation.

Here the detailed procedure of this calculation will be provided for the case of (p) a-Si:H/ (n) c-Si heterojunction. For the *n-p* case the procedure is the same with respect of the majority vs minority carriers.

We introduce the functions $u_e(x)$ and $u_h(x)$ to define the position of the electron and hole quasi Fermi levels in relation to the intrinsic level (close to the mid-gap):

$$u_e(x) = \frac{E_F^e - E_i(x)}{k_B T}, \tag{4.27}$$

and

$$u_h(x) = \frac{E_F^h - E_i(x)}{k_B T}, \tag{4.28}$$

where $E_i(x)$ is the intrinsic level in c-Si as a function of distance x from the junction (where $x = 0$). Here we assume that quasi Fermi levels $E_F{}^h$ and $E_F{}^e$ are independent of x in the space charge region. Using these functions we write the electron and hole concentrations (n and p, respectively) in n-type c-Si as follows:

$$n(x) = n_i \exp u_e(x), \tag{4.29}$$

$$p(x) = n_i \exp(-u_h(x)), \tag{4.30}$$

$$n(x)\,p(x) = n_i^2 \exp(u_e(x) - u_h(x)) = n_i^2 \exp\frac{E_F^e - E_F^h}{k_B T} = n_i^2 \exp\frac{qV_a}{k_B T} \tag{4.31}$$

In Eq.(4.31) we have used that the voltage drop across the junction is related to the splitting of the quasi Fermi levels. Thus, the concentration of holes can be expressed in terms of u_e and the applied voltage V_a:

$$p(x) = n_i \exp(-u_e(x)) \exp\frac{qV_a}{k_B T} \tag{4.32}$$

This minority-carrier term $p(x)$ adds a contribution $qp(x)$ to the space charge density in c-Si and by introducing it into the calculations one will be able to estimate whether its influence is negligible or not.

In order to solve the Poisson equation we obtain the expression for the charge density ρ:

$$\rho(x) = q\left[p(x) - n(x) + N_D^{c-Si}\right] = q\left[n_i \exp(-u_e(x)) \exp\frac{qV_a}{k_B T} - n_i \exp u_e(x) + n_i \exp u_e(\infty)\right], \tag{4.33}$$

and

$$\frac{d^2V(x)}{dx^2} = \frac{k_B T}{q}\frac{d^2 u_e(x)}{dx^2}. \tag{4.34}$$

Then the Poisson equation:

$$\frac{d^2V}{dx^2} + \frac{\rho}{\varepsilon} = 0 \tag{4.35}$$

is written as:

$$\frac{d^2u_e}{dx^2} + \frac{q^2 n_i}{\varepsilon k_B T}\left[\exp(-u_e(x) + \frac{qV_a}{k_B T}) - \exp u_e(x) + \exp u_e(\infty)\right] = 0 \tag{4.36}$$

After multiplication of both sides of Eq.(4.36) by the term $\frac{2du_e}{dx}$ and further integration we obtain the following expression:

$$\frac{du_e}{dx} = \frac{1}{L_D^{c-Si}}\sqrt{f(u_e(x), V_a),} \tag{4.37}$$

with

$$\begin{aligned} f(u_e(x), V_a) &= \exp u_e(x) + \exp(-u_e(x) + \frac{qV_a}{k_B T}) - \exp u_e(\infty) \\ &- \exp(-u_e(\infty) + \frac{qV_a}{k_B T}) + \exp u_e(\infty)\cdot\left(u_e(\infty) - u_e(x)\right), \end{aligned} \tag{4.38}$$

and $L_D^{c\text{-}Si}$ being the intrinsic Debye length:

$$L_D^{c-Si} = \sqrt{\frac{\varepsilon k_B T}{2q^2 n_i}}\,. \tag{4.39}$$

The positive sign has been chosen in Eq.(4.37) since the electric field is negative in the *n*-side of the *p*-*n* heterojunction.

Now we shall consider the total charge neutrality:

$$Q^{a-Si:H} + Q^{c-Si} + Q^{\text{int}erface} = 0 \tag{4.40}$$

The total charges in c-Si and a-Si:H are written in the following way:

$$Q^{c-Si} = \int_0^\infty \rho(x)dx = \varepsilon E(0^+) = \varepsilon \frac{dV}{dx}\Big|_{0^+} = \frac{\varepsilon k_B T}{q}\frac{du}{dx}\Big|_{0^+} = \frac{\varepsilon k_B T}{q}\frac{1}{L_D^{c-Si}}\sqrt{f(u_e(0),V_a)}\,, \tag{4.41}$$

$$Q^{a-Si:H} = \frac{\varepsilon}{L_D^{a-Si:H}}(V(-\infty)-V(0)) = -\frac{\varepsilon}{\sqrt{\frac{\varepsilon}{q^2 N(E_F)^{a-Si:H}}}}(V(0)-V(-\infty)) \tag{4.42}$$

Here we again neglect the interface charge as it has been done in the depletion approximation calculations. Rewriting the charge neutrality condition taking into account Eqs. (4.41) and (4.42) we obtain the following expression:

$$q(V(0)-V(-\infty)) = \sqrt{\frac{2k_B T n_i}{N(E_F)^{a-Si:H}}}\sqrt{f(u_e(0),V_a)} \tag{4.43}$$

The term on the left hand in Eq.(4.43) can be as well determined from the band diagram:

$$q(V(0)-V(-\infty)) = qV_d - qV_a - k_B T(u_e(\infty)-u_e(0))\,, \tag{4.44}$$

$$qV_d - qV_a - k_B T(u_e(\infty)-u_e(0)) = \sqrt{\frac{2k_B T n_i}{N(E_F)^{a-Si:H}}}\sqrt{f(u_e(0),V_a)}\,. \tag{4.45}$$

Eq.(4.45) is written with only one unknown variable – $u_e(0)$. Therefore a single-valued analytical solution can be obtained.

The analytical calculation of capacitance is based on the estimation of charge dQ that is extracted from one electrode with a change in terminal voltage dV_a

$$C = \frac{dQ}{dV_a}\,. \tag{4.46}$$

Since the number of extracted electrons on one side equals the number of extracted holes on the other side we can calculate only the charge of extracted electrons on the *n*-side:

$$Q_e = \int_0^{\infty} q(N_D^{c-Si} - n)dx \,. \tag{4.47}$$

Using Eq.(4.37) one can rewrite the expression for the charge and capacitance:

$$Q_e = \int_{u_e(0)}^{u_e(\infty)} \frac{q(N_D^{c-Si} - n)}{\frac{du_e}{dx}} du_e = qn_i L_D^{c-Si} I \,, \tag{4.48}$$

with

$$I = \int_{u_e(0)}^{u_e(\infty)} \frac{\exp u_e(\infty) - \exp u_e(0)}{\sqrt{f(u_e(0), V_a)}} du_e \,. \tag{4.49}$$

The capacitance is thus given by

$$C = qn_i L_D^{c-Si} \frac{dI}{dV_a} \,, \tag{4.50}$$

where dI/dV_a is written as follows:

$$\frac{dI}{dV_a} = -\frac{du_e(0)}{dV_a}\left[\frac{\exp u_e(\infty) - \exp u_e(0)}{\sqrt{f(u_e(0), V_a)}}\right] + \int_{u_e(0)}^{u_e(\infty)} \left(-\frac{1}{2}\right) \frac{\exp u_e(\infty) - \exp u_e}{\left[f(u_e, V_a)\right]^{3/2}} \cdot \frac{df(u_e, V_a)}{dV_a} du_e \,, \tag{4.51}$$

taking into account the result of differentiation of Eq.(4.38) with respect to V_a:

$$\frac{df(u_e, V_a)}{dV_a} = \frac{q}{k_B T}\left[\exp(-u_e(x) + \frac{qV_a}{k_B T}) - \exp(-u_e(\infty) + \frac{qV_a}{k_B T})\right] \tag{4.52}$$

With the help of MATLAB software the capacitance is calculated according to Eq.(4.50) as a function of temperature and applied voltage for different values of the band offset (ΔE_V), density of states in a-Si:H, doping density in c-Si and a-Si:H. It is worth emphasizing that based on the equations given above one can also calculate the capacitance without taking into account the holes and consequently neglecting the strong inversion layer in c-Si. If one

neglects holes' contribution to the charge density in Eq.(4.33) the function f is then reduced to f^* that is independent of V_a:

$$f^*(u_e(x)) = \exp u_e(x) - \exp u_e(\infty) + \exp u_e(\infty)\left(u_e(\infty) - u_e(x)\right). \qquad (4.53)$$

Then the capacitance is obtained from Eq.(4.50) by following the same procedure given above and substituting f by f^*. The step-by-step calculation is presented in Appendix C.

Now let us study in details the capacitance-temperature dependencies at zero polarization.

4.3.2.1 *C-T* dependencies at zero polarization

In Fig.4.34 one can compare the *C-T* dependencies obtained from the complete analytical calculation described above and the depletion approximation for ΔE_V = 0.4 eV, $N_D^{c\text{-}Si}$ = 1.5×10^{15} cm^{-3}, $N(E_F)^{a\text{-}Si:H}$ = 1×10^{19} cm^{-3}eV^{-1}, $\delta^{a\text{-}Si:H}$ = 0.45 eV.

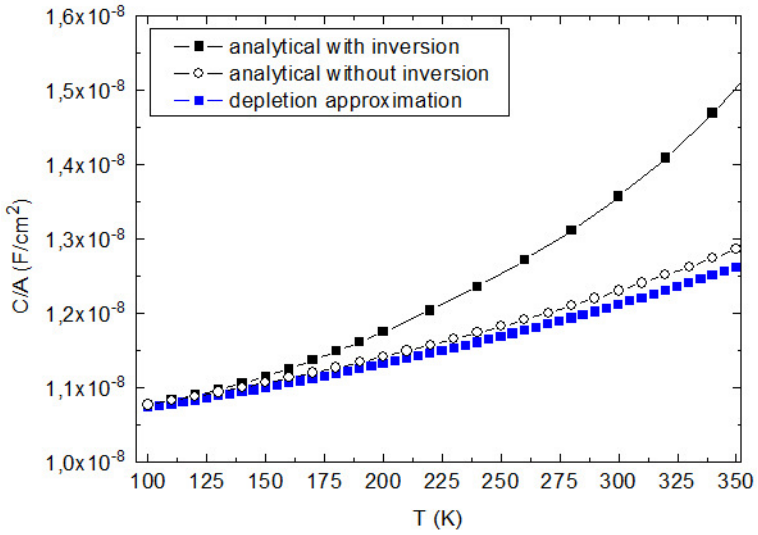

Fig.4.34. Analytical and depletion approximation C-T dependencies for ΔE_V =0.4 eV at zero bias. "With inversion" referrs to the calculation taking into account the contribution of holes in the space charge region; "without inversion" - to the calculation neglecting the contribution of holes in the space charge region

As it can be seen from Fig.4.34 the minority carriers in c-Si bring significant change to the capacitance behavior with temperature. The inversion layer reduces the potential drop in the c-Si layer resulting in the increase of the capacitance. The calculation carried out without taking into account the minority carriers' contribution provides almost the same *C-T* curve as the classical depletion approximation. It can be shown analytically (see Appendix C) that the

capacitance obtained using *f** function from Eq.(4.53) eventually reduces to the capacitance defined previously from the depletion approximation:

$$C = \frac{\varepsilon}{w + L_D^{a-Si:H}}, \tag{4.54}$$

with

$$w = \sqrt{\frac{2\varepsilon\left(V_d^{c-Si} - V_a - {k_B T}/{q}\right)}{qN_D^{c-Si}}}. \tag{4.55}$$

The influence of the inversion layer in c-Si is different for different values of the band offset. In Fig.4.35 *C-T* curves calculated for ΔE_V = 0.1 eV and ΔE_V = 0.3 eV are presented.

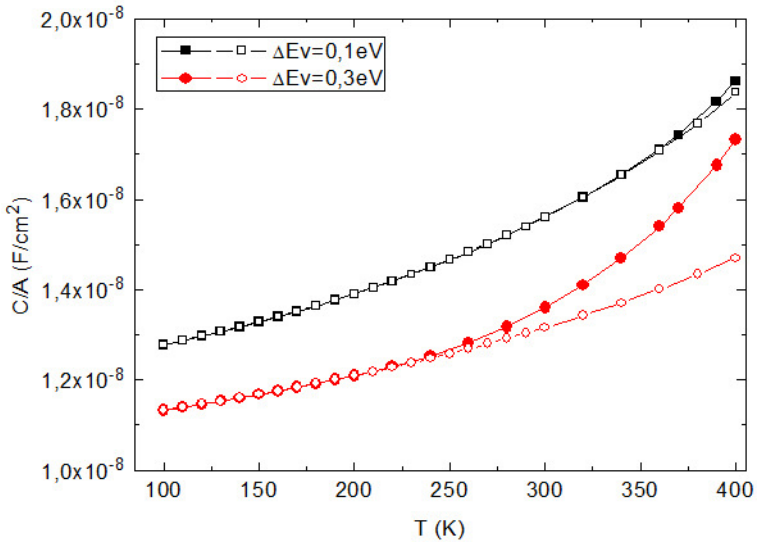

Fig.4.35. Analytical C-T dependencies for various ΔE_V at zero bias. Filled symbols show the calculation taking into account the contribution of holes in the space charge region; open symbols - the calculation neglecting the contribution of holes in the space charge region.

For ΔE_V = 0.1 eV no strong inversion exists at the interface up to high temperatures, therefore the contribution of the minority carriers is negligible. The case of ΔE_V = 0.3 eV is intermediate: the inversion layer becomes important above T = 250 K. For ΔE_V = 0.4 eV or larger (Fig.4.34) the presence of the inversion layer is observed even at low temperatures and its influence on the capacitance is important in the whole temperature range.

The comparison of the analytically obtained *C-T* curve for ΔE_V = 0.4 eV and the experimental one is presented in Fig.4.36.

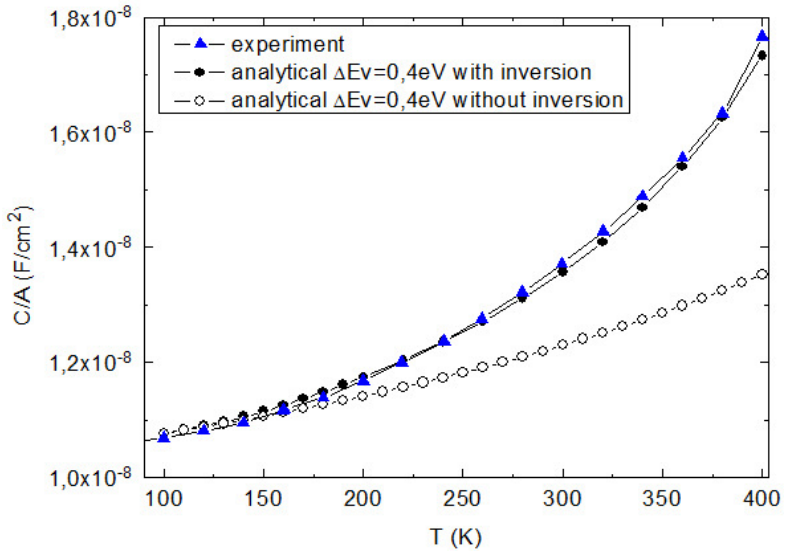

Fig.4.36. Experimental and analytically calculated C-T dependencies for ΔE_V = 0.4 eV.

As one can see the experimental curve is perfectly well reproduced by the analytically calculated *C-T* dependency if one takes into account the effect of the strong inversion layer. In a recent work based on planar conductance measurements the valence band offset value was evaluated: ΔE_V = 0.36±0.05 eV [42]. The fit of the experimental curve with ΔE_V = 0.4 eV shows good agreement with this value and provides a further confirmation of the existence of the strong inversion layer.

To estimate the contribution of the inversion layer in (n) c-Si a simplified estimation of the capacitance can be carried out by taking the potential drop in the depletion region in c-Si $qV_d^{c\text{-}Si}{}_{inlim}$ (inlim- inversion limited) that can written as follows:

$$qV_d^{c-Si}{}_{in\lim} = E_g^{c-Si} - 2\delta^{c-Si} \tag{4.56}$$

The term $qV_d^{c\text{-}Si}{}_{inlim}$ can be regarded as the effective potential drop in the depletion region in c-Si when the strong inversion layer exists. The part of the total potential drop in c-Si lies within the inversion layer thus the effective potential drop in the depletion region in c-Si that contributes to the capacitance, $qV_d^{c\text{-}Si}{}_{inlim}$, is smaller. This effect is shown in Fig.4.37.

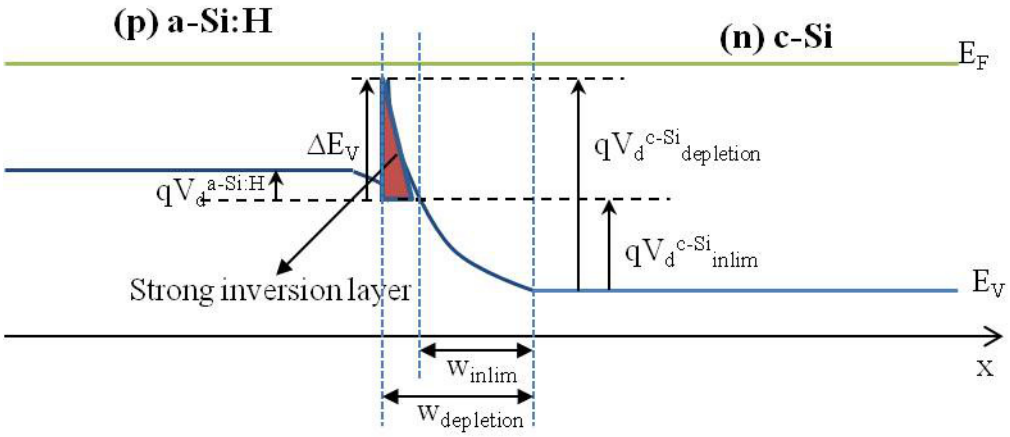

Fig.4.37. The influence of the strong inversion layer on the potential drop in the depletion region in c-Si. $V_d^{c\text{-}Si}{}_{inlim}$ defines the depletion width w_{inlim} that is the effective depletion width at the edge of which the charge is modulated and capacitance signal is obtained.

Indeed, the strong inversion layer does not contribute to the depletion region in c-Si, since it can supply for free carriers, i.e. holes. Therefore the depletion region in c-Si is defined now by the effective potential drop $qV_d^{c\text{-}Si}{}_{inlim}$ that equals to the difference between the total diffusion potential in c-Si and the potential drop in the inversion layer, as it can be seen in Fig.4.37. The corresponding depletion width w_{inlim} is smaller than the theoretical width, provided by the depletion approximation $w_{depletion}$. The capacitance C_{inlim} in this case is calculated in the same way as within the depletion approximation:

$$C_{in\lim} = \frac{\varepsilon A}{w_{in\lim}} = A\sqrt{\frac{\varepsilon q N_D^{c-Si}}{2(E_g^{c-Si} - 2\delta^{c-Si})}} \qquad (4.57)$$

This "inversion limited" capacitance was then compared with the complete analytical *C-T* data and depletion approximation calculation in Fig.4.38. The "inversion limited" capacitance defined by Eq.(4.57) does not depend on the junction properties and is derived only from the parameters that describe the crystalline layer. Since the effective potential drop in the depletion region in c-Si is fixed at the value defined by Eq.(4.56), it does not depend on temperature and the influence of the inversion layer is considered at the whole temperature range. Indeed, at low temperatures, where the influence of the strong inversion layer is weak or disappears, the "inversion limited" capacitance differs from both analytical and depletion approximation curves. From a given temperature, where the contribution of the strong inversion layer becomes considerable, the "inversion limited" curve reproduces well the *C-T* data obtained from complete calculation that takes into account the minority carriers in (n) c-Si, as it is shown in Fig.4.38. Thus we can conclude that if one considers the presence of the strong inversion layer at the interface in c-Si the depletion region in c-Si becomes thinner and is defined by the effective potential drop with the value close to $qV_d^{c\text{-}Si}{}_{inlim} = (E_g^{c\text{-}Si} - 2\delta^{c\text{-}Si})$.

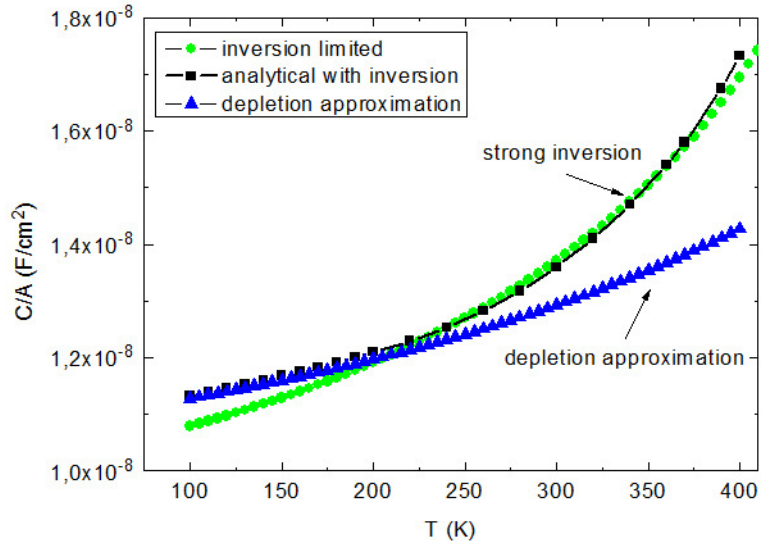

Fig.4.38. Analytical, depletion approximation and "inversion limited" C-T curves for ΔE_V*=0.3.*

4.3.3 Conclusions

In this section we studied the dependency of the junction capacitance on the temperature. It was shown that the classical depletion approximation does not provide for an acceptable reproduction of the experimental data obtained for (p) a-Si:H/(n) c-Si heterojunction. This is due to a strong inversion layer that exists at the interface of (p) a-Si:H/(n) c-Si junction. This layer absorbs part of the total potential drop across the junction and the effective potential drop in the depleted region in c-Si becomes close to the value $qV_d^{c\text{-}Si}{}_{inlim} = (E_g^{c\text{-}Si}\text{-}2\delta^{c\text{-}Si})$.

The complete analytical calculation of capacitance was developed that takes into account the minority carriers contribution to the charge density in (n) c-Si and therefore the inversion layer. Analytically calculated and obtained from the depletion approximation capacitance-temperature dependencies were compared in order to reveal the influence of the inversion layer in c-Si. It was shown that within complete analytical approach the inversion layer brings significant change to the capacitance for the values of the valence band offset larger than 0.3 eV. The influence of the inversion layer depends dramatically on the temperature. At low temperature for ΔE_V < 0.3 eV the strong inversion layer does not exist and brings no contribution into *C-T* dependencies. At higher temperatures the influence of this layer becomes considerable that results in the increase of the capacitance signal. For valence band offset values higher than 0.3 eV the strong inversion exists even at low temperatures. The experimentally obtained *C-T* curves showed a good agreement with the complete analytical calculation and the presence of the inversion layer in the studied samples was then fully confirmed.

The experimental *C-T* dependencies also allowed us to conclude that ΔE_V higher than 0.3 eV in the measured samples since the influence of the inversion layer was considerable even at low temperatures. *C-T* measurements performed on different samples showed the same behavior and the existence of the strong inversion layer was always revealed. A simplified "inversion limited" method of calculating the capacitance using the depletion approximation was proposed. It was demonstrated that the suggested value of the potential drop in the depletion region $qV_d^{c\text{-}Si}{}_{inlim} = (E_g^{c\text{-}Si} - 2\delta^{c\text{-}Si})$ represents well the change of this parameter due to the inversion layer and allowed one to reproduce the complete calculation *C-T* data. Thus using this approximation with a effective potential drop in the depletion region such as $qV_d^{c\text{-}Si}{}_{inlim} = (E_g^{c\text{-}Si} - 2\delta^{c\text{-}Si})$ allows one to well reproduce the *C-T* curve calculated without any approximation if a strongly inverted region exists.

4.3.3.1 *C-V* dependencies

In this section we will address the capacitance-voltage dependencies at different temperatures. Again the influence of the strong inversion layer will be studied as well as the possibility to extract of the band offset values from the *C-V* measurements.

It was shown previously that according to the depletion approximation the total diffusion potential V_d can be found from *C–V* measurements, and, more precisely, from the intercept of the linear extrapolation of $1/C^2$ versus the applied reverse voltage (V_a) with the voltage axis V_{int}. Knowing V_d and the positions of the Fermi level in a-Si:H ($\delta^{a\text{-}Si:H}$) and c-Si ($\delta^{c\text{-}Si}$) one could easily determine the band offset values from Eq.(4.3).

4.3.3.1.a Experimental $1/C^2$ vs V_a curves and intercept voltage V_{int}

The $1/C^2$ vs V_a data obtained from our complete analytical calculation is compared to experimental curves for two temperatures in Fig.4.39.

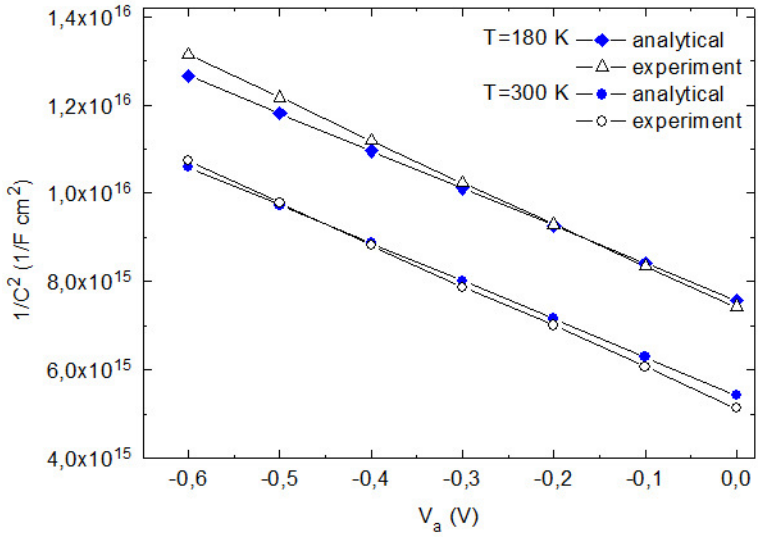

Fig.4.39. Experimental and analytically calculated $1/C^2$ vs V_a curves for T=180 K and T=300 K.

Experimental curves are very well reproduced by analytical approach with ΔE_V = 0.4 eV taking into account the strong inversion layer. However, the definition of the intercept value and the slope of experimental $1/C^2$ vs V_a curves is ambiguous due to the curvature of these curves. In Fig.4.40 experimental $1/C^2$ vs V_a curve at 300 K is shown together with two linear fits performed in different ranges of applied voltage.

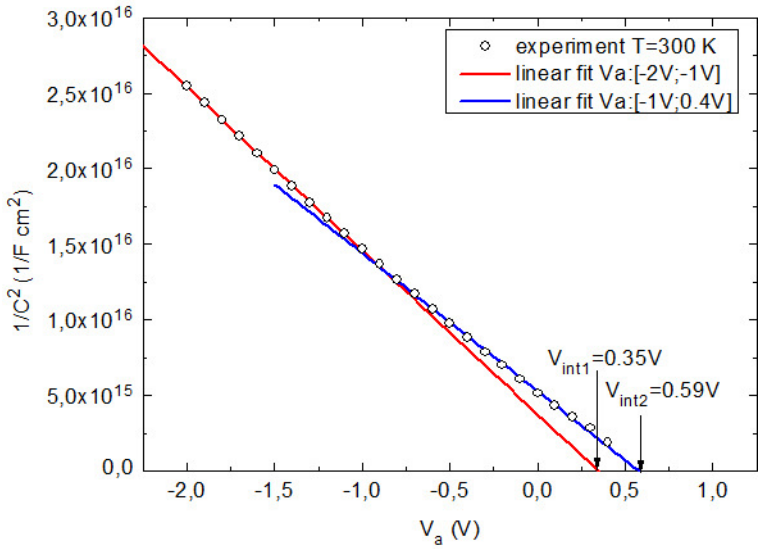

Fig.4.40. Experimental $1/C^2$ vs V_a curve at 300 K and two linear fits in different applied voltage ranges. The obtained intercept voltages V_{int1} and V_{int2} are indicated.

One can see that the choice of the fitted region significantly changes the derived intercept voltage value. We interpret the curvature of the $1/C^2$ vs V_a curve as a change of the effective

surface area at the edge of the space charge layer. Indeed, in the studied solar cell the junction surface is textured and the surface area of the device should be corrected by the area factor which represents the increase of surface area caused by texturing. This factor depends on the geometry of textured surface and *a priori* is unknown. Area factors between 1.1 and 1.7 were reported [43, 44]. The effective area considered in *C-V* measurements, however, depends on the applied voltages. Under small reverse bias voltages the area of the sample is close to the true area of the textured surface. When large reverse bias voltages are applied the surface enhancement caused by texturing tends to vanish and the effective area approaches that of a flat surface sample. This phenomenon was studied in the work of Schutze et al [45] on textured silicon solar cells. It was shown that if large reverse V_a can be applied to the sample, the doping density can simply be calculated from the slope of the $1/C^2$ vs V_a curve without knowledge of the surface enhancement. The reduction of the surface area under high applied voltages can be explained if one considers the width of the depletion region in c-Si. The larger the applied bias is the larger the depletion width is. Therefore the ac modulation of the depletion width takes place further from the junction textured surface than under small bias and if the depletion region's limit lies deeper in the bulk, the effective area is less influenced by the texture of the interface.

Considering the uncertainty in the determination of the effective area it becomes troublesome to determine the true intercept voltage value. For solar cells, the applicable reverse bias voltages are frequently limited by early junction breakdown due to, for example, high base doping, or special cell concepts. In this work we wanted to avoid breakdown of our high efficiency solar cells and therefore we limited the explored reverse bias range to -3V. Further in this work, we will consider the intercept voltages obtained from the linear fit of the small reverse voltages with the surface correction factor of 1.6, that is close to the value measured on similarly textured solar cells processed at INES. Nonetheless, our principal interest is to assess the temperature evolution of the derived V_{int} rather than interpretation of its absolute value so the choice of the surface correction factor is not of great importance.

In order to study the evolution with temperature of the intercept voltage and compare it with the total diffusion potential calculated from Eq.(4.3) and with the inversion limited potential drop in depleted region in c-Si we normalized the values of intercept voltage to that measured at T = 300 K. The normalized potentials are shown in Fig.4.41.

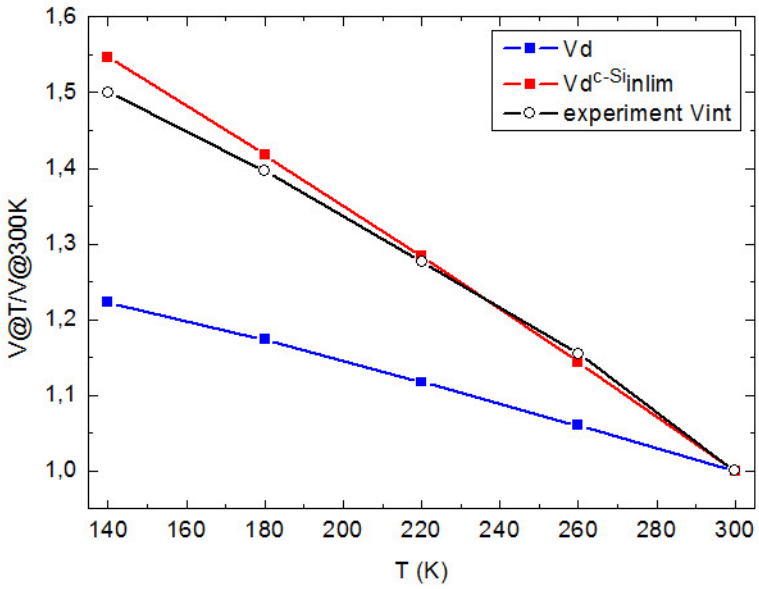

Fig.4.41. Evolution with temperature of the normalized values of the intercept voltage V_{int} derived from experiment, theoretical values of total diffusion potential V_d and inversion limited potential drop in the depleted region in c-Si $V_d^{c\text{-}Si}{}_{inlim}$ (ΔE_V = 0.4 eV).

One can see that the temperature dependence of the experimentally derived intercept voltages is very close to that of the potential drop in the depleted region in c-Si when the strong inversion layer is considered (defined by Eq.(4.56)). The evolution with temperature of the total diffusion potential is less pronounced. We can conclude that the intercept voltage derived from $1/C^2$ vs V_a plot does not represent the total diffusion potential as it is predicted by the depletion approximation and exhibits a more pronounced temperature dependence. In fact, if we suppose that V_{int} is close to the effective potential drop in c-Si, its temperature evolution is then related to the influence of the inversion layer that disappears at low temperatures. This reasoning explains the deviation from the temperature dependence of $V_d^{c\text{-}Si}{}_{inlim}$ at T=140 K. Since at this temperature, the inversion layer is less pronounced, the potential drop in the depletion region in c-Si becomes closer to the total diffusion potential. On the contrary, the term $V_d^{c\text{-}Si}{}_{inlim}$ is always affected by the presence of the strong inversion layer in the whole considered temperature range, as it was discussed previously. Another possible effect that influences the experimentally derived intercept voltage is the capacitance step that may exist at low temperatures. Thus it becomes problematic to measure the true quasi-static capacitance signal at very low temperatures.

4.3.3.1.b Intercept voltage derived from analytically calculated $1/C^2$ vs V_a curves

Now let us address the analytically calculated $1/C^2$ vs V_a curves and the derived V_{int} values. Again the evolution with temperature of V_{int} obtained from complete calculation with and without consideration of the strong inversion layer was studied as well as that one of V_d and $V_d^{c\text{-}Si}{}_{inlim}$. The obtained values of the intercept of the linear extrapolation V_{int}, V_d and $V_d^{c\text{-}}$

$^{Si}_{inlim}$ are plotted as function of temperature in Fig. 4.42.

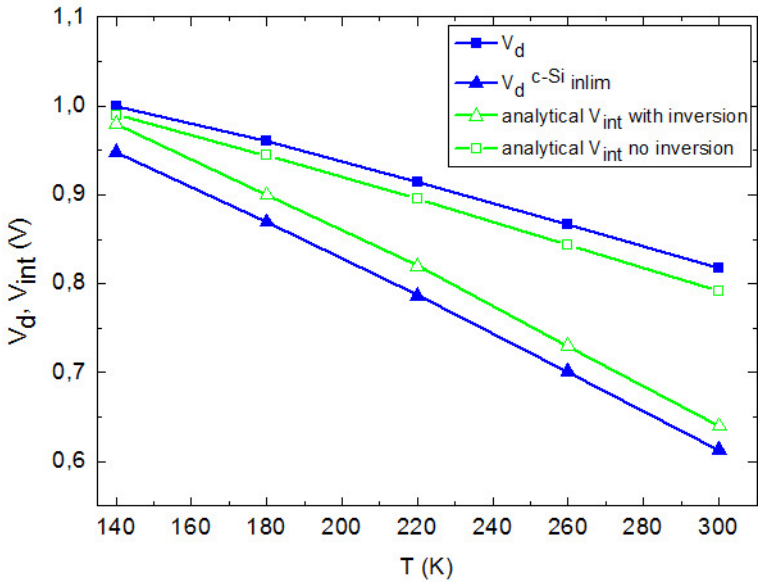

Fig.4.42. Evolution with temperature of V_{int} (with and without inversion) obtained from analytically calculated $1/C^2$ vs V_a curves at ΔE_V=0.4 eV and of theoretical values V_d and $V_d^{c-Si}{}_{inlim}$.

Analytical V_{int} values obtained from $1/C^2$ vs V_a curves are very different from the total diffusion potential if the strong inversion layer is considered. For low temperatures, where the inversion layer disappears, the difference is less pronounced. As it was done in the previous section, a reference value of the potential drop in depletion region in c-Si, $V_d^{c-Si}{}_{inlim}$ was considered. V_{int} is very close to this reference value. On the contrary, when no inversion is considered in the calculations, V_{int} is close to V_d. Thus, we may conclude that the presence of the strong inversion layer influences the derived intercept voltage that can no longer be considered as the total diffusion potential predicted by the depletion approximation. This term describes the potential drop in depletion region in c-Si which becomes close to V_d only at very low temperatures where the strong inversion layer is less pronounced. At higher temperatures, the influence of the inversion layer is important and the potential drop in the depletion region in c-Si has to be corrected by the part of the total diffusion potential that is absorbed by the inversion layer. Since the intercept voltage is not equal to the total diffusion potential, V_{int} cannot be used for the extraction of the band offset values.

Results from analytical calculations are given in Table 4.4 for 2 temperatures, 140 K and 300 K. To emphasize the contribution of the strong inversion layer to the capacitance and therefore to the determination of V_{int} value, the results are compared with the case of ΔE_V=0.1

eV, where no inversion exists in the considered temperature range.

	T = 140 K			T = 300 K		
	V_{int}, V	V_d, V	$V_d^{c\text{-}Si}{}_{inlim}$, V	V_{int}, V	V_d, V	$V_d^{c\text{-}Si}{}_{inlim}$, V
ΔE_V=0.4 eV with strong inversion layer	0.98	1.00	0.95	0.64	0.87	0.61
ΔE_V=0.4 eV without strong inversion layer	0.98			0.79		
ΔE_V=0.1 eV	0.68	0.69	0.95	0.49	0.52	0.61

Table 4.4. Intercept potential, V_{int}, total diffusion potential, V_d and inversion limited potential drop in the depletion region in c-Si, $V_d^{c\text{-}Si}{}_{inlim}$ for T = 140 K and T =300 K.

As it can be seen from Table 4.4 V_{int} values are very close to the total diffusion potential in the case of ΔE_V=0.1 eV, thus confirming that the absence of strong inversion allows one to obtain V_d from *C-V* measurements.

Although no area ambiguity exists for analytically calculated $1/C^2$ vs V_a curves, the dependence of the intercept voltage on the applied reverse bias can be shown. The previously discussed *C-V* and consequently $1/C^2$ vs V_a curves were calculated for the range of the reverse bias from -1 V to 0 V. Now we present the results obtained on the wide range of the applied reverse bias voltages.

Increase of the absolute values of the reverse bias voltages results in the increase of the derived intercept voltage that approaches the value of the total diffusion potential for such a configuration, V_d = 0.87 V. This evolution is presented in Table 4.5.

Range of reverse bias voltages for the linear fit (V)	Derived V_{int} (V)
[-17;-14]	0.72
[-10;-7]	0.69
[-7;-4]	0.68
[-1;-0]	0.64

Table 4.5. Intercept potential V_{int} as a function of the applied reverse bias voltage at T=300 K and ΔE_V=0.4 eV.

This dependence of the intercept voltage on the reverse bias voltage can be explained again by the influence of the strong inversion layer on the potential drop in the depleted region in c-Si. The increase of the reverse bias induces the increase of the potential across the junction while the part of the potential drop absorbed by the inversion layer remains the same. Therefore, for large values of total potential the influence of the inversion is less and less pronounced.

This phenomenon was studied in the work of Gummel and Scharfetter on *p*+-*n* step homojunctions [19]. It was shown that the derived intercept voltages depended dramatically on the doping ratio N_A/N_D of the layers and the applied reverse voltage. For heavily doped *p*-layers with the doping ratio higher than 10^3 V_{int} was found to be inferior to V_d under small reverse bias voltages. The authors explained this behavior by the increase of the junction capacitance when the holes' contribution in *n*-layer was considered in comparison with that predicted by the depletion approximation. The increase of the reverse bias resulted in the increase of V_{int} until it became equal to V_d. Therefore we may conclude that in (p) a-Si:H/(n) c-Si heterojunction we observe the similar situation where minority carriers bring significant change to the capacitance that results in the applied reverse voltage dependency of the *C-V* data.

4.3.4 Conclusions

In this section the detailed assessment of *C-V* dependencies at different temperatures was carried out. The analytically calculated $1/C^2$ vs V_a curves for (p) a-Si:H/(n) c-Si with ΔE_V=0.4 eV were compared with the experimental ones at various temperatures. It was shown that experimental data is well reproduced by complete analytical calculation that takes into account the minority carriers' contribution which is significant due to the existence of the strong inversion layer at the interface in c-Si. According to theoretical derivation based on the depletion approximation the total diffusion potential, V_d, is equal to the intercept of the linear extrapolation of $1/C^2$ versus applied reverse voltage (V_a) with the voltage axis, V_{int}. However, V_{int} values derived from both analytical and experimental $1/C^2$ vs V_a curves differ significantly from the total diffusion potential V_d predicted by theory. The problem of ambiguity of the V_{int} values derived from the experiment due to the area definition was discussed. The area for textured samples should be corrected by the area factor that depends on the geometry of the junction and is difficult to define. Considering this, the absolute intercept voltage values derived from experimental *C-V* curves have to be considered carefully.

The temperature dependencies of the intercept voltages obtained from experimental curves showed similar behavior to that of the potential drop in the depleted region in c-Si when the strong inversion layer is considered. We conclude that the intercept voltage derived from $1/C^2$ vs V_a plot does not represent the total diffusion potential as it is predicted by the depletion approximation and is close to the effective potential drop in the depletion region in c-Si. The temperature evolution of V_{int} was explained by the influence of the inversion layer at

the interface that limits the potential drop within the depleted region in (n) c-Si.

The intercept voltages derived from analytically calculated $1/C^2$ vs V_a curves for ΔE_V=0.4 eV were found to be close to the potential drop in the depleted region in c-Si when the strong inversion layer is considered. The temperature dependency of V_{int}, as in the case of the experimental results, was more pronounced than that of the total diffusion potential. This intercept voltage was found to be close to V_d only at low temperatures where the strong inversion layer does not exist. On the contrary, when no inversion is considered in calculations in the calculations V_{int} is close to V_d.

The dependency on the applied reverse bias voltage of V_{int} was demonstrated. Under large reverse voltages the derived intercept voltage approaches the total diffusion potential value. For large values of applied reverse voltage the influence of the inversion layer diminishes gradually until the part of the potential drop that lies within this layer becomes negligible in comparison with the total potential drop in the depletion region of c-Si under reverse bias.

The obtained results showed that the *C-V* measurements cannot be a reliable tool to determine V_d and consequently ΔE_V. For large band offset values, where the presence of the inversion layer at the interface should be considered, the obtained V_{int} values are highly underestimated in comparison with the predicted V_d.

4.4 Influence of the buffer (i) a-Si:H layer and interface defects on *C-T* dependencies

In this Section we will briefly address the possible influence of the intrinsic (i) a-Si:H layer and the interface defects on the capacitance-temperature behavior.

4.4.1 Buffer (i) a-Si:H layer and its influence on *C-T* curves

In high efficiency silicon solar cells it is essential to include additional, very thin (less than 10 nm thick) undoped – so called intrinsic – a-Si:H buffer layers between the wafer and the doped (emitter or BSF) a-Si:H layers. The reason is the reducing of the interface defect density at the a-Si:H/c-Si junction since the defect density in undoped a-Si:H is strongly decreased.

Although the experimentally studied (p) a-Si:H/(n) c-Si heterojunctions included (i) a-

Si:H buffer layer, in the numerical modeling performed in Section 4.2 and calculations in Section 4.3 we did not consider any additional layer between (p) a-Si:H and (n) c-Si. In order to justify this simplification here we present the numerically obtained *C-T* curves fn the structure defined at the beginning of Section 4.2.1 but with 5 nm (i) a-Si:H layer. The thickness of (p) a-Si:H layer was reduced to 75 nm in order to keep the geometric capacitance ($C/A = \varepsilon/(d^{(p)a\text{-}Si:H}+d^{(i)a\text{-}Si:H})$) at the same level as it was taken in the previous section for the (p) a-Si:H thickness equal to 80 nm. The constant DOS was introduced in the (i) a-Si:H layer with typical value for undoped a-Si:H of $N = 1\times10^{16}$ cm^{-3}eV^{-1}. No doping was introduced and the position of the Fermi level was found at 0.7 eV from the conduction band edge. The calculated *C-T* curve at $f = 12800$ Hz together with the one obtained without (i) a-Si:H layer is shown in Fig.4.43.

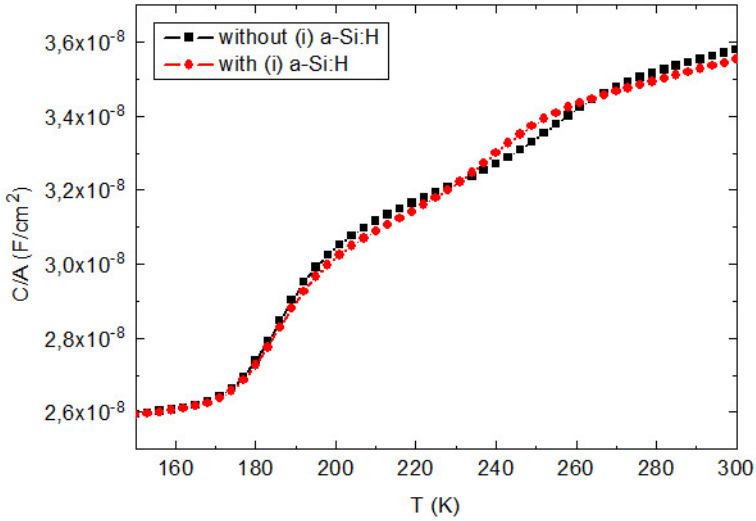

Fig.4.43. Calculated capacitance-temperature curves at $f = 12800$ Hz ($\mu_p = 1$ cm^{2}V^{-1}s^{-1} and $\sigma_p = 7\times10^{-16}$ cm^2) for the structures with and without (i) a-Si:H buffer layer at the interface.

As one can observe the (i) a-Si:H layer brings insignificant change to the low temperature capacitance step, therefore its influence on the capture-release processes in a-Si:H is negligible. The behavior of the high temperature step is more influenced by the introduction of the (i) a-Si:H layer. The slight shift of this step is due to the modifications of the potential distribution at the interface caused by the introduction of the (i) a-Si:H layer. Namely, the valence band offset values is reduced to the value ΔE_V=0.4 eV (previously, ΔE_V=0.47 eV). Although, the (i) a-Si:H layer contributes to the position of the high temperature step attributed to the response of the holes in the strong inversion layer, the activation energy of this step was found again to be close to the position of the Fermi level in a-Si:H at the interface. This value of the activation energy again confirms the origin of the step provided above. Thus the (i) a-Si:H layer does not modify significantly the characteristics of the *C-T* curves observed previously on the structures modeled without the buffer layer. We may conclude that the (i) a-Si:H layer, though bringing slight changes to the band diagram at the

interface of the heterojunction, can be omitted in the calculations of capacitance-temperature signal.

4.4.2 Influence of interface defects on capacitance-temperature behavior

As it was mentioned at the beginning of Section 4.2.1 low interface defect density, that characterizes high efficiency silicon heterojunction solar cells, had no influence on the capacitance of (n) a-Si:H/(p) c-Si heterojunctions. Here we present the numerically obtained *C-T* curve for the previously considered (p) a-Si:H/(n) c-Si heterojunction with the interface defects considered. The introduction of the interface defect was performed in the same way as described in Ref.[46]. The interface was described by introducing an interface layer with a thickness of 1 nm between c-Si and a-Si:H and E_g = 1.12 eV. The defect distribution in this interface layer was assumed to be Gaussian, with donor-like defects located at 0.56 eV above the valence band maximum. In the following D_{in} (in cm^{-2}) will denote the interface defect density, which is determined as the product $d_{int}*N_{it}$, where d_{int} is the thickness of the interface layer (1 nm) and N_{it} (in cm^{-3}) is the defect density in this layer, which is the integral over the band gap of the Gaussian interface DOS, g_{it} (in $cm^{-3}eV^{-1}$). Capture cross sections for both types of carriers were taken equal to 10^{-16} cm^2 for these interface states. For high quality silicon heterojunction solar cells it was shown that the interface defect density does not exceed 10^{12} cm^{-2} and lies within 1-4×10^{11} cm^{-2} range [47]. In our simulation we introduced D_{in} = 2.25×10^{11} cm^{-2}. The calculated C-T curves with and without interface defects are presented in Fig.4.44.

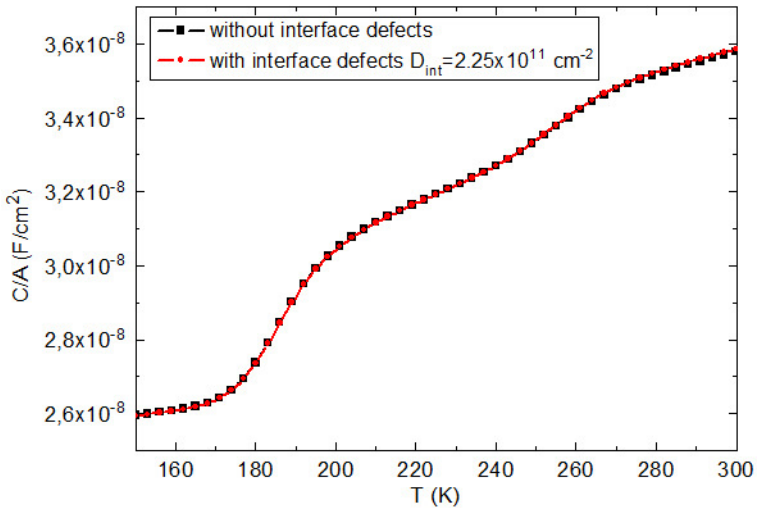

Fig.4.44. Calculated capacitance-temperature curves at f = 12800 Hz for the structures without and with interface defects with D_{it} = 2.25×10^{11} cm^{-2}.

One can see that introduction of the interface defect with D_{in} = 2.25×10^{11} cm^{-2} does not bring any change to the *C-T* curve. The interface defect density is low enough so that no possible exchange of holes between interface states can be perceived.

We conclude that interface defects with densities typical for high quality silicon heterojunction solar cells do not influence the capacitance-temperature behavior and thus they can be neglected in calculations.

4.5 References

[1] W. Shockley, U.S. Patent 2569, 347, (1951).

[2] H. Kroemer, "Theory of a Wide-Gap Emitter for Transistors", *Proceedings of the Institute of Radio Engineers*, vol. 45, p. 1535, 1957.

[3] R. L. Anderson, "Experiments on Ge-GaAs Heterojunctions", *Solid State Electronics*, vol. 5, p. 341, 1962.

[4] J.P. Kleider: Band Offsets from Electrical Measurements. In: Wilfried G.J.H.M. van Sark, Francesco Roca, Lars Korte (eds.) "*Physics and Technology of Amorphous-Crystalline Heterostructure Silicon Solar Cells*", pp. 405-444, Springer-Verlag Berlin Heidelberg, 2012.

[5] W. Favre, M. Labrune, F. Dadouche, A. S. Gudovskikh, P. Roca i Cabarrocas et J.-P. Kleider, " Study of the interfacial properties of amorphous silicon/n-type crystalline silicon heterojunction through static planar conductance measurements ", Physica Status Solidi C, vol. 7, p. 1037–1040, 2010.

[6] W. Favre, "*Silicium de type n pour cellules à hétérojonctions : caractérisation et modélisation"*. Thèse doctorat, Université Paris Sud XI, 2011.

[7] O. A. Maslova, J. Alvarez, E. V. Gushina, W. Favre, M. E. Gueunier-Farret, A. S. Gudovskikh, A. V. Ankudinov, E. I. Terukov et J.-P. Kleider, "Observation by conductive-probe atomic force microscopy of strongly inverted surface layers at the hydrogenated amorphous silicon/crystalline silicon heterojunctions", *Applied Physics Letters*, vol. 97, p. 252110, 2010.

[8] J. Alvarez, F. Houzé, J. P. Kleider, M. Y. Liao, and Y. Koide, *Superlattices Microstructures*, vol. 40, p.343, 2006.

[9] J. P. Kleider, M. Soro, R. Chouffot, A. S. Gudovskikh, P. Roca i Cabarrocas, J. Damon-Lacoste, D. Eon and P.-J. Ribeyron, "High interfacial conductivity at amorphous silicon/crystalline silicon heterojunctions", *Journal of Non-Crystalline Solids*, vol. 354, p. 2441, 2008.

[10] J. P. Kleider and A. S. Gudovskikh, "Characterization of amorphous/crystalline silicon interfaces from electrical measurements", *Materials Research Society Proceedings*, vol. 1066, 1066-A04-01, 2008.

[11] S. R. Forrest: Measurement of energy band offsets using capacitance and current measurement techniques. In: F. Capasso, G. Margaritondo (eds.) "*Heterojunction Band Discontinuities – Physics and Device Applications"*, pp. 311–375. North Holland, Amsterdam, 1987.

[12] D. V. Lang: "Measurement of energy band offsets by space charge spectroscopy". In: F. Capasso, G. Margaritondo (eds.) "*Heterojunction Band Discontinuities – Physics and Device Applications"*, pp. 377–396. North Holland, Amsterdam, 1987.

[13] B. M. Wilamowski, "Semiconductor Diode". In: *Industrial Electronics Handbook, vol. 1*

– *Fundamentals of Industrial Electronics,* 2nd Edition, pp. 8-1 to 8-15, CRC Press, 2011.

[14] D.V. Lang, J.D. Cohen, JP. Harbison, "Measurement of the density of gap states in hydrogenated amorphous silicon by space charge spectroscopy", *Physical Review B,* vol. 25, p. 5285, 1982.

[15] I. W. Archibald and R. A. Abram, "More theory of the admittance of an amorphous silicon Schottky barrier", *Philosophical Magazine B*, vol. 54, p. 421, 1986.

[16] J. P. Kleider, "Capacitance techniques for the evaluation of electronic properties and defects in disordered thin film semiconductors", *Thin Solid Films*, vol. 427, p. 127, 2003.

[17] A. S. Gudovskikh, S. Ibrahim, J. P. Kleider, J. Damon-Lacoste, P. Roca i Cabarrocas, Y. Veschetti, P.-J. Ribeyron, "Determination of band offsets in a-Si:H/c-Si heterojunctions from capacitance–voltage measurements: Capabilities and limits", *Thin Solid Films*, vol. 515, p. 7481, 2007.

[18] S. Gall, R. Hirschauer, D. Braünig, "Admittance measurements at a-Si:H/c-Si heterojunction devices", *Proceedings of the 13th European Photovoltaic Solar Energy Conference*, Nice, France, pp. 1264–1267, 1995.

[19] H. K. Gummel, D. L. Scharfetter, "Deplition-Layer Capacitance of p+n Step Junction", *Journal of Applied Physics*, vol. 38, p. 2148, 1967.

[20] T. Unold, M. Rösch, and G. H. Bauer, *Journal of Non-Crystalline Solids*, vol. 266–269, p. 1033, 2000.

[21]. A. S. Gudovskikh, J. P. Kleider, A. Froitzheim, et al., *Thin Solid Films*, vol. 451–452, p. 345, 2004.

[22] A. S. Gudovskikh, J. P. Kleider, R. Stangl, et al., *Proceedings of 19th European Photovoltaic Solar Energy Conference*, Paris, France, p. 697, 2004.

[23] H. Angermann, E. Conrad, L. Korte, J. Rappich, T.F. Schulze, M. Schmidt, "Passivation of textured substrates for *a*-Si:H/*c*-Si hetero-junction solar cells: Effect of wet-chemical smoothing and intrinsic *a*-Si:H interlayer", *Material Science and Engineering: B*, vol. 159–160, p. 219, 2009.

[24] T F. Schulze, L. Korte, B. Rech, " Impact of a-Si:H hydrogen depth profiles on passivation properties in a-Si:H/c-Si heterojunctions", *Thin Solid Films*, vol. 520, p. 4439, 2012.

[25] D. Muñoz, T. Desrues, A.-S. Ozanne, S. De Vecchi, S. Martin de Nicolàs, F. Jay, F. Souche, N. Nguyen, C. Denis, C. Arnal, G. d'Alonzo, J. Coignus, W. Favre, T. Blevin, A. Valla, F. Ozanne, T. Salvetat, P.J. Ribeyron, "Key Aspects on Development of High Efficiency Heterojunction and IBC-Heterojunction Solar Cells: Towards 22% Efficiency on Industrial Size", *Proceedings of 27th European Photovoltaic Solar Energy Conference*, Frankfurt, Germany, p. 576, 2012,.

[26] S. Martín de Nicolás, D. Muñoz, A.S. Ozanne, N. Nguyen, P.J. Ribeyron, "Optimisation of doped amorphous silicon layers applied to heterojunction solar cells », *Energy Procedia*, vol. 8, p. 226, 2011.

[27] A. Favier, D. Muñoz, S. Martín de Nicolás, P.-J. Ribeyron, « Boron-doped zinc oxide layers grown by metal-organic CVD for silicon heterojunction solar cells applications », *Solar Energy Materials and Solar Cells*, vol. 95, p. 1057, 2011.

[28] A. Danel, F. Jay, S. Harrison, C. Arnal, G. d'Alonzo, N. Nguyen, A.-S. Ozanne, P.E. Hickel, D. Muñoz, P.-J. Ribeyron, "Surface Passivation of c-Si Textured Wafers for a-Si:H/c-Si Heterojunction Solar Cells: Correlation Between Lifetime Tests and Cell Performance of a Pilot Line", *Proceedings of 26th European Photovoltaic Solar Energy Conference*, Hamburg, Germany, p. 2260, 2011.

[29] S. Martín de Nicolás, "*a-Si :H/c-Si heterojunction solar cells : back side assessment and improvement"*. Thèse doctorat, Université Paris Sud XI, 2012.

[30] N.F. Mott, *Philosophical Magazine,* vol. 19, p. 835, 1969.

[31] P. G. LeComber and W. E. Spear, *Physical Review Letters,* vol. 25, p. 509, 1970.

[32] C. Godet "Variable range hopping revisited: the case of an exponential distribution of localized states", *Journal of Non-Crystalline Solids*, vol. 299–302, p. 333, 2002.

[33] R. A. Street, *Hydrogenated amorphous silicon*. Cambridge Solid State Science Series, 1991.

[34] H. Matsuura, T. Okuno, H. Okuno, and K. Tanaka, "Electrical properties of n-amorphous/p-crystalline heterojunctions", *Journal of Applied Physics*, vol. 55, p. 1012, 1984.

[35] Jian V. Li, Richard S. Crandall, David L. Young, Matthew R. Page, Eugene Iwaniczko et al., "Capacitance study of inversion at the amorphous-crystalline interface of n-type silicon heterojunction solar cells", *Journal of Applied Physics*, vol. 110, p. 114502, 2011.

[36] S. M. Sze, *Physics of semiconductor devices*, 2nd edn. John Wiley & Sons, New York, 1981.

[37] R. Varache, "Development, characterization and modeling of interfaces for high efficiency silicon heterojunction solar cells*"*. Thèse doctorat, Université Paris Sud XI, 2012.

[38] M. A. Green, "Intrinsic concentration, effective densities of states, and effective mass in silicon", *Journal of Applied Physics*, vol. 67, p. 2944, 1990.

[39] V. Alex, S. Finkbeiner, J. Weber, "Temperature dependence of the indirect energy gap in crystalline silicon", *Journal of Applied Physics* , vol.79, p.6943, 1996.

[40] H. Overhof, P. Thomas, « Electronic transport in hydrogenated amorphous semiconductors", *Springer tracts in modern physics*, vol. 114, 1989.

[41] A. G. Kazanskii and S. V. Kuznetsov, "Statistical Shift of the Fermi-Level Position in p-Type Hydrogenated Amorphous Silicon", *Physica Statut Solidi (b)*, vol. 167, p. K39, 1991.

[42] R. Varache, W. Favre, L. Korte, J.P. Kleider, « Influence of the amorphous/crystalline silicon heterostructure properties on planar conductance measurements", *Journal of Non-Crystalline Solids*, vol. 358, p. 2236, 2012.

[43] F. Recart and A. Cuevas, "Application of junction capacitance mea-surements to the characterization of solar cells," *IEEE Transactions on Electron Devices*, vol. 53, p. 442, 2006.

[44] D. Hinken, A. Milsted, R. Bock, B. Fischer, K. Bothe, M. Schütze, J. Isenberg, A. Schulze, and M. Wagner, "Determination of the base-dopant concentration of large-area crystalline silicon solar cells," *IEEE Transactions on Electron Devices*, vol. 57, p. 2831, 2010.

[45] M. Schütze, D. Hinken, A. Milsted, M. B. Koentopp, and Karsten Bothe, "Extended Analysis of Capacitance–Voltage Curves for the Determination of Bulk Dopant Concentrations of Textured Silicon Solar Cells", *IEEE Transactions on Electron Devices*, vol. 58, p. 3759, 2011.

[46] D. Diouf, J.P. Kleider, T. Desrues, P.-J. Ribeyron, "Effects of the front surface field in n-type interdigitated back contact silicon heterojunctions solar cells", *Energy Procedia*, vol. 2, p. 59, 2010.

[47] C. Leendertz, N. Mingirulli, T. F. Schulze, J. P. Kleider, B. Rech, and L. Korte, "Discerning passivation mechanisms ata-Si: H /c-Si interfaces by means of photoconductance measurements", *Applied Physics Letters*, vol. 98, p. 202108, 2011.

5 Conclusions and perspectives

During last years the development of renewable energy sources and, namely, photovoltaics is increasing dramatically and the conversion results keep on improving. Solar cells based on a-Si:H/c-Si heterojunctions have reached the efficiency of 24.7% on large scale samples and benefit from low-cost technology due low temperature processing. However there are still a lot of uncertainties on their electronic properties, especially at the interface, that are crucial for understanding the functioning of the cell and promoting further improvement of their performance.

The objective of the present work was to study the possibilities and limitations of capacitance spectroscopy on hydrogenated amorphous silicon Schottky diodes and a-Si:H/c-Si heterojunctions.

In Chapter 1 we provided a description of hydrogenated amorphous silicon including its properties and PECVD growth technique. Our particular interest was addressed to the defects and the density of states in the band gap of the material. A brief review of the application of a-Si:H in photovoltaics was presented.

The capacitance technique is widely used for the characterization of *p-n* junctions and Schottky barriers. The principles of this technique were provided in Chapter 2. The depletion approximation was recalled since it plays a very important role in the description of a junction and may be a reason of erroneous interpretations of the capacitance measurements. The *C-V* technique is suggested to obtain the doping density and the barrier height of a junction. However, it was shown that there exists a lot of discussion on the accuracy of the derivation of these parameters.

The admittance spectroscopy and DLTS measurements were described considering their application for extracting the density of states in the band gap of a semiconductor. Our interest was concentrated on the simplified treatment suggested by Cohen and Lang that allows one to extract the density of states at the Fermi level in a-Si:H Schottky diodes from capacitance-temperature data obtained at different frequencies. Up to our knowledge no critical assessment of this treatment has been carried out. In Chapter 3 we focused on the study of the reliability and validity of this approach applied to a-Si:H Schottky barriers with different

magnitudes and shapes of the DOS. Several structures representing *n*-type and undoped hydrogenated amorphous silicon Schottky diodes were modeled with the help of numerical software (AFORS-HET and Silvaco Atlas) and capacitance-temperature dependencies were obtained. Using the simplified treatment the density of states at the Fermi level, $N(E_F)$, the activation energy, E_a, and the attempt-to-escape frequency, $\nu_{n,}$ were derived and then compared to values that were introduced into the calculations. It was demonstrated that the accuracy and reliability of the extracted DOS parameters strongly depend on the position of the Fermi level and DOS shape. It was shown that for the case of *n*-type a-Si:H with the position of the Fermi level rather close to the conduction band edege, E_C-E_F = 0.2 eV, and a constant DOS distribution the treatment works well yielding values of the DOS at the Fermi level and the attempt-to-escape frequency very close to that introduced into the calculations. For the case of undoped a-Si:H with E_C-E_F = 0.7 eV and constant DOS the determination of $N(E_F)$ is less accurate and provides underestimated values although yielding a correct order of magnitude. Exponential band tail and Gaussian distributions of DOS as well yielded less accurate values of $N(E_F)$. Another parameter derived from the treatment is the attempt-to-escape frequency. We have shown that this parameter was considerably overestimated for almost all cases studied. The reliability of the studied treatment is linked to the approximations used to obtain the explicit expression of the capacitance in amorphous semiconductors that is the basis of the proposed treatment, namely the sharp cut-off approximation and the low-temperature limit.

In the second part of Chapter 3 numerical calculations were carried out to reproduce experimental capacitance data. An attempt to fit the experimental results only with the information ($N(E_F)$, E_C-E_F , ν_n) extracted from the treatment and assuming a constant DOS distribution was addressed. The calculated *C-T* curves showed reasonable behaviour compared to the experimental oness but were mainly shifted to higher temperatures. After some adjustments performed on the parameters of the DOS a satisfactory reproduction of the experiment was obtained. In order to have a better insight into the DOS distribution data obtained from MPC and CPM techniques were introduced in modeling to calculate *C-T* dependencies. With only slight corrections of parameters describing the DOS distributions a very good reproduction of experimental capacitance data was obtained. It was thus shown that the DOS distribution deduced with the help of numerical simulations from photocurrent techniques (performed on samples with coplanar electrodes) not only provided good reproduction of the latter but were also able to reproduce Schottky barrier capacitance measurements performed separately on co-deposited samples. The possibilities of the simplified treatment was also analysed in the framework of a comparison of the DOS at the Fermi level in pm-Si:H and a-Si:H. After adjusting of the parameters ($N(E_F)$, E_C-E_F , ν_n) obtained from the treatment of the experimental data considering the corrections observed for the studied case of undoped a-Si:H a constant DOS was introduced into the simulation for both disordered materials. Again, a correct reproduction of the experimental data was achieved.

Thus the simplified treatment of the capacitance data together with numerical modeling provides a valuable tool to assess some important parameters of a material with some adjustments to be considered depending, namely, on the position of the Fermi level in a studied structure. However, the charge transport phenomenon can limit the response of the gap states making the treatment not applicable since the onset of the capacitance is defined by the onset of transport. This issue should be considered when treating the *C-T* data. We showed that for typical values of the electron capture cross section and the electron mobility the transport does not limit the capture-emission processes and the onset of the capacitance signal is related to the response of the defects in the band gap.

Chapter 4 was devoted to the study of capacitance spectroscopy when applied to a-Si:H/c-Si heterojunctions. This chapter was divided in two main parts. The first part was dedicated to the low-temperature step in *C-T* dependencies. Numerical modeling of (p) a-Si:H/(n) c-Si heterojunctions was performed with particular attention on the amorphous layer parameters. Two capacitance steps were observed on *C-T* dependencies for typical values of the hole mobility and hole capture cross section in a-Si:H. The two activation energies of the capacitance steps have been attributed to different processes. The low temperature step is characterized by an activation energy that corresponds to the difference between the Fermi level and the top of the valence band in the bulk of a-Si:H, and was attributed to transport and response of gap states in a-Si:H. The high temperature step has an activation energy corresponding to the difference between the Fermi level and the top of the valence band in a-Si:H at the interface. It was concluded that it is related to the response of free holes in the strong inversion layer of c-Si at the interface. At low values of the valence band offset, at which the inversion layer in c-Si is very weak or absent, the latter step disappears and only the former capacitance step remains, with an activation energy equal to the difference between the Fermi level and the top of the valence band in the bulk of a-Si:H. Experimental *C-T* curves obtained on two different solar cell samples (fabricated at two different institutes) were then presented. On one sample a low temperature capacitance step can be seen on the *C-T* curves. According to the previous modeling, the corresponding activation energy of 0.29 eV could be attributed to the difference between the Fermi level and the top of the valence band in the bulk of a-Si:H. On another sample, a very high efficiency solar cell (η>21%) fabricated at INES-CEA, the low temperature step in experimental *C-T* curves is less marked and has a much lower activation energy (of the order of 0.08 eV), which can hardly be attributed to the difference between the Fermi level and the top of the valence band either in the bulk of a-Si:H or at the interface. It is suggested that hopping and tunneling processes are involved in the transport in a-Si:H and at the interface, respectively, that result in much lower activation energies as obtained from the modeling where such processes are not taken into account. Apart from the capacitance step features that are anyway very weak in real solar cells owing to the very thin a-Si:H layer, we emphasized a well defined continuous increase of capacitance with temperature that is independent of frequency, thus traducing a quasi static behaviour.

In the second part of Chapter 4 we studied the quasi static temperature dependence of the junction capacitance. We developed the complete analytical calculation of the junction capacitance that takes into account the existence of a strongly inverted surface layer at the c-Si surface. This analytical calculation was compared with the depletion approximation and experimental results. We showed that the classical depletion approximation fails to provide acceptable reproduction of the experimental data obtained for (p) a-Si:H/(n) c-Si heterojunction solar cells. Due to the existence of the strong inversion layer the potential drop in the depleted region in crystalline silicon is smaller than assumed in the traditional depletion approximation. On the contrary, the experimental data can be very well reproduced by the complete analytical model taking account of the contribution of the strong inversion layer and with a valence band offset value of 0.4 eV that provides such a strong inversion layer in the whole explored temperature range.

Finally, the detailed assessment of the *C-V* technique for band offsets determination was carried out. The analytically calculated $1/C^2$ vs V curves for (p) a-Si:H/(n) c-Si with ΔE_V=0.4 eV were compared with the experimental ones at various temperatures. It was demonstrated that experimental data are very well reproduced by our complete analytical calculation. Both analytical and experimental data showed different behaviour from that predicted by the depletion approximation, according to which the total diffusion potential equals to the intercept of the linear extrapolation of $1/C^2$ with the voltage axis, V_{int}. The results were explained by the influence of the strong inversion layer at the interface that limits the potential drop in the depleted region of the space charge layer in (n) c-Si to a lower value than calculated in the depletion approximation. The obtained results proved that the *C-V* measurements should be considered carefully if one wants to determine the band offsets values. For large band offset values, where the influence of the strong inversion layer at the interface is important, the obtained V_{int} values are much smaller than V_d, thus yielding to underestimated valence band offset values.

In this work we showed the possibilities of capacitance measurements on a-Si:H Schottky diodes and a-Si:H/c-Si heterojunctions. The determination of the density of states in a-Si:H is crucial for characterization and improvement of solar cells. Further study could target the introduction dangling bonds defects into simulation as two monovalent defect distributions with certain correlation energy. The influence of this DOS distribution on the simplified treatment should be studied and, again, the assessment of the reliably should be addressed.

Application of capacitance spectroscopy of a-Si:H/c-Si heterojunctions can be extended in several directions. One of the subjects to be addressed is a metal/a-Si:H contact on the top of a cell. ITO, typically used to form a top contact, may form a Schottky barrier at the a-Si:H interface thus preventing the collection of photogenerated carriers. The behavior of this contact under small signal conditions can be studied by the means of capacitance

spectroscopy in order to provide knowledge on the charge carriers and transport mechanisms.

Important part of this work was dedicated to highlighting the existence of the inversion layer in c-Si near the interface. For the first time the presence of the inversion at certain values of the band offset was proved by the complete analytical calculation of the capacitance. Some improvements could be brought to this calculation in order to better reproduce a real solar cell. The influence of a finite a-Si:H layer thickness and the (i) a-Si:H layer could be studied with some modification introduced into the calculation.

In perspective one may consider the application of the analysis of the capacitance based on the complete analytical calculation to solar cells formed on CdS/CIGS heterojunctions. It was reported that a strong inversion layer that may exist at CdS/CIGS interface [1]. This heterojunction is characterized by a similar band diagram to that of a (n) a-Si:H/(p) c-Si heterojunction with a considerable conduction band offset which value is yet controversial [2]. Modifying the complete analytical calculation for the case of a n-p heterojunction and combining with experimental capacitance measurements one can obtain essential information on the influence of the inversion layer as well as determine a range of possible values of the conduction band offset.

References

[1] Dongxiang Liao and Angus Rockett, "Electronic and Chemical Phenomena at Cu(In, Ga)Se_2/CdS Heterojunctions and Their Implications for Photovoltaic Devices", *Proceedings of the Materials Research Society*, vol. 763, 2003.

[2] L. Kronik, L. Burstein, M. Leibovitch, Yoram Shapira, D. Gal, E. Moons, J. Beier, G. Hodes, David Cahen, D. Hariskos, R. Klenk, and H.-W. Schock, "Band diagram of the polycrystalline CdS/Cu(In,Ga)Se_2 heterojunction ", *Applied Physics Letters,* vol. 67, p. 1405, 1995.

Appendix A

Simulation software

A.1 AFORS-HET

The free software AFORS-HET (Automat FOR Simulation of HETero structures) is developed in Helmholtz-Zentrum Berlin für Materialien und Energie HZB. This software is conceived as a tool to model heterojunction structures in 1D [1], [2], particularly a-Si :H/c-Si heterojunctions.

A heterojunction is defined as a stack of different semiconductor layers; each of them is described by various parameters. The interface of AFORS-HET is intuitive and allows one to describe easily a desired structure for simulation as it is seen in Fig.A.1.

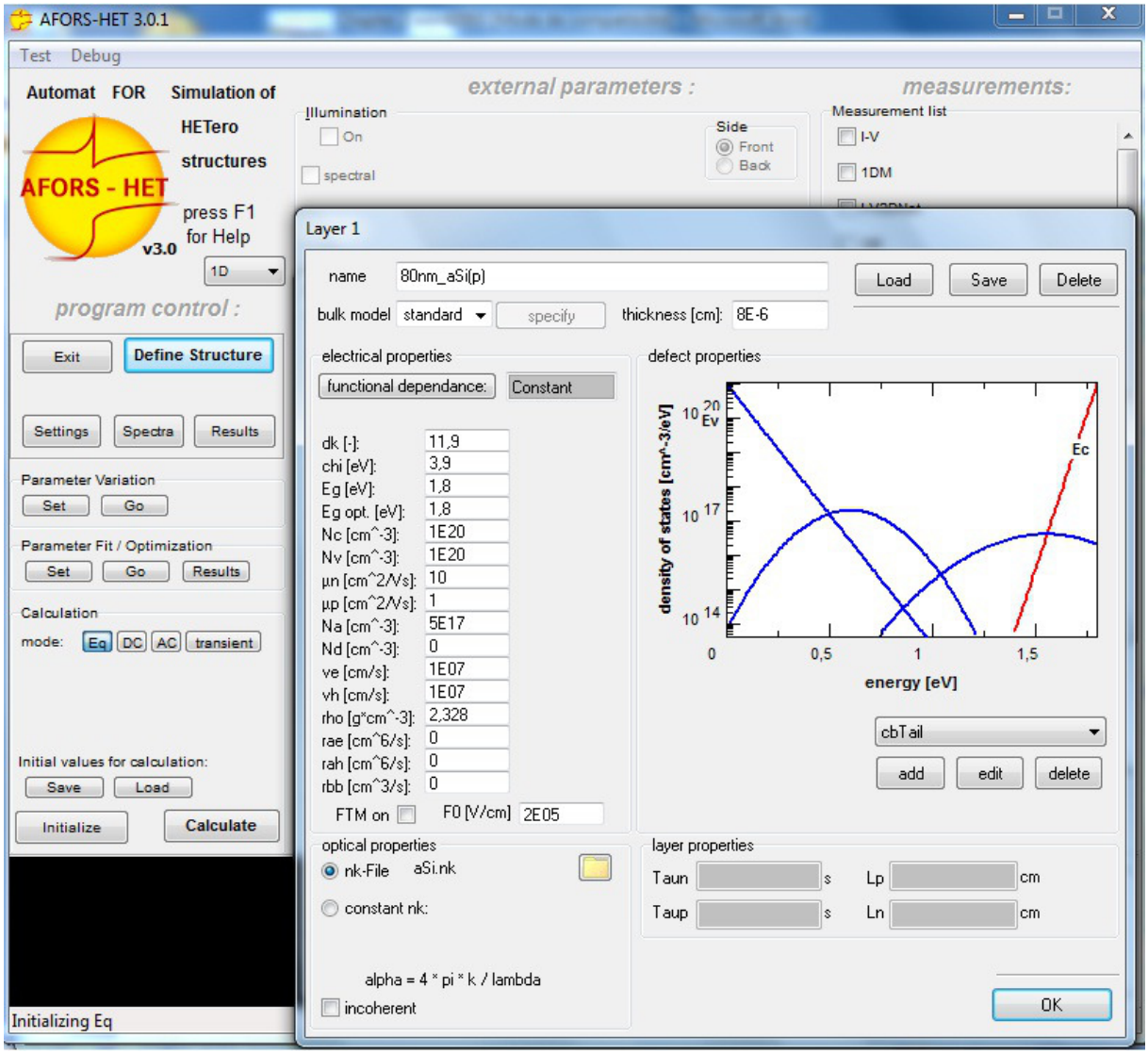

Fig.A.1. Interface of AFORS-HET software. Different parameters defining a material can be input (fields the left). The density of states in the band gap is also shown (on the right).

The electronic properties of a material can be defined for each layer (electron affinities, band gap, doping densities, mobilities, etc.), as well as the density of states in the band gap. The introduction of interfacial defects is also possible.

Once a desired structure is created the software solves the system of basic equations at thermodynamic equilibrium. Then it is possible to model the functioning of a structure under polarization (DC or AC) and/or illumination (monochromatic or polychromatic). Thus AFORS-HET offers a possibility to simulate various characterization techniques as function of temperature (current-voltage $I(V)$, capacitance-voltage $C(V)$, quantum efficiency, photoluminescence and electroluminescence, etc.).

1.2 ATLAS by Silvaco

ATLAS is a part of software package of the American company « Silvaco International ». This company provides for simulation software by finite elements.

ATLAS is a 2D and 3D simulator of semiconductor devices that allows one to obtain their electrical characteristics. A desired structure is created by a command file that contains commands describing a material. The environment of this software is somewhat less friendly and that of AFORS-HET and requires certain knowledge of the programming.

The main advantages of ATLAS software is the possibility to run simulations in 2D or 3D. Moreover, it is possible to introduce temperature dependencies of various parameters (doping, bandgap, etc.) that are fixed in AFORS-HET.

Detailed description of ATLAS software can be found in the thesis of Djicknoum Diouf, former PhD student of LGEP [3].

References

[1] R. Stangl, M. Kriegel et M. Schmidt Proceedings of the 4th World Conference on Photovoltaic Energy Conversion, p. 1350, 2006.

[2] http://www.helmholtz-berlin.de/forschung/enma/si-pv/projekte/asicsi/aforshet/index_en.html

[3] D. Diouf, Cellules photovoltaïques silicium à hétérojonctions et à structure interdigitée en face arrière. Thèse doctorat, Université Paris Sud XI, 2010.

Appendix B

Description of the main modeled structures

B.1 a-Si:H Schottky diode

Parameter	Value	Unit
Thickness	300	nm
Band gap	1.75	eV
Dielectric constant	11.8	
Electron affinity	3.85	eV
N_C	2×10^{20}	cm^{-3}
N_V	2×10^{20}	cm^{-3}
Electron mobility μ_n	10	$cm^2V^{-1}s^{-1}$
Hole mobility μ_p	1	$cm^2V^{-1}s^{-1}$

B.1.1 Constant DOS

B.1.1.a n-type a-Si:H: E_C–E_F=0.2 eV, $N(E_F)$=$1\times10^{19}cm^{-3}eV^{-1}$

(E_C-E_F) at 100 K	0.2	eV
Constant DOS		
Effective capture cross section		
Electrons σ_n	1×10^{-17}	cm^2

Holes σ_p	1×10^{-15}	cm^2
N(E) acceptor	1.14×10^{18}	$cm^{-3}eV^{-1}$
N(E) donor	8.86×10^{18}	$cm^{-3}eV^{-1}$

B.1.1.b n-type a-Si:H: $E_C–E_F$=0.2 eV, $N(E_F)$=$1\times10^{16}cm^{-3}eV^{-1}$

(E_C-E_F) at 100 K	0.2	eV
Constant DOS		
Effective capture cross section		
Electrons σ_n	1×10^{-17}	cm^2
Holes σ_p	1×10^{-15}	cm^2
N(E) acceptor	1.14×10^{15}	$cm^{-3}eV^{-1}$
N(E) donor	8.86×10^{15}	$cm^{-3}eV^{-1}$

B.1.1.c undoped a-Si:H: $E_C–E_F$=0.7 eV, $N(E_F)$=$1\times10^{16}cm^{-3}eV^{-1}$

(E_C-E_F) at 300 K	0.7	eV
Doping density N_D	$1{,}05\times10^{16}$	cm^{-3}
Constant DOS		
Effective capture cross section		
Electrons σ_n	1×10^{-17}	cm^2
Holes σ_p	1×10^{-15}	cm^2
N(E) acceptor	1×10^{16}	$cm^{-3}eV^{-1}$

B.1.1.d undoped a-Si:H: $E_C–E_F$=0.7 eV, $N(E_F)$=$1\times10^{19}cm^{-3}eV^{-1}$

(E_C-E_F) at 300 K	0.7	eV
Doping density N_D	$1{,}05\times10^{19}$	cm^{-3}
Constant DOS		
Effective capture cross section		
Electrons σ_n	1×10^{-17}	cm^2
Holes σ_p	1×10^{-15}	cm^2
N(E) acceptor	1×10^{19}	$cm^{-3}eV^{-1}$

B.1.2 Non constant DOS distributions

B.1.2.a Exponential conduction band tail DOS

(E_C-E_F) at 110 K	0.2	eV
Doping density N_D (k_BT_C=0.04)	4×10^{17}	cm^{-3}
Doping density N_D (k_BT_C=0.09)	9×10^{17}	cm^{-3}
Doping density N_D (k_BT_C=0.13)	1.35×10^{18}	cm^{-3}
Exponential conduction band tail		
Type	Acceptor	
Effective capture cross section		
Electrons σ_n	1×10^{-17}	cm^2
Holes σ_p	1×10^{-15}	cm^2
k_BT_C	0.04	eV
	0.09	eV
	0.13	eV
$N(E_C)$	4.66×10^{19}	$cm^{-3}eV^{-1}$

B.1.2.b Gaussian DOS distribution

(E_C-E_F) at 300 K	0.2	eV
Gaussian 1 deep defect		
Doping density N_D	9.85×10^{20}	cm^{-3}
Type	Acceptor	
Effective capture cross section		
Electrons σ_n	1×10^{-17}	cm^2
Holes σ_p	1×10^{-15}	cm^2
$E_{mGauss}-E_V$	0.9	eV
w_{Gauss}	0.2	eV
N_{0m}	2×10^{21}	eV
Gaussian 2 deep defect		
Doping density N_D	9.11×10^{15}	cm^{-3}
Type	Acceptor	
Effective capture cross section		
Electrons σ_n	1×10^{-17}	cm^2
Holes σ_p	1×10^{-15}	cm^2
$E_{mGauss}-E_V$	1.35	eV
w_{Gauss}	0.22	eV
N_{0m}	1.5×10^{19}	eV

B.2 (p) a-Si:H/ (n) c-Si heterojunction

B.2.1 Study of the capacitance steps

(n) c-Si substrate		
Thickness	300	µm
Band gap	1.12	eV
Doping density N_D	1.2×10^{16}	cm^{-3}
Activation energy	0.2	eV
Dielectric constant	11.9	
Electron affinity	4.05	eV
N_C	2.8×10^{19}	cm^{-3}
N_V	1.04×10^{19}	cm^{-3}
Electron mobility μ_n	1040	$cm^2V^{-1}s^{-1}$
Hole mobility μ_p	412	$cm^2V^{-1}s^{-1}$
(p) a-Si emitter		
Thickness	80	nm
Band gap	1.75	eV
Doping density N_A	1.44×10^{19}	cm^{-3}
(E_F-E_V) at 300 K	0.3	eV
Dielectric constant	11.9	
Electron affinity	3.9	eV
N_C	1×10^{20}	cm^{-3}
N_V	1×10^{20}	cm^{-3}
Electron mobility μ_n	5	$cm^2V^{-1}s^{-1}$
Hole mobility μ_p	1	$cm^2V^{-1}s^{-1}$
Constant DOS		
Effective capture cross section		
Electrons σ_n	1×10^{-17}	cm^2

Holes σ_p	1×10^{-15}	cm^2
N(E) acceptor	1×10^{19}	$cm^{-3}eV^{-1}$

Appendix C

Calculation of the capacitance without considering minority carriers' contribution

$$f^*(u_e(x)) = \exp u_e(x) - \exp u_e(\infty) + \exp u_e(\infty)\left(u_e(\infty) - u_e(x)\right) \tag{C.1}$$

$$qV_d - qV_a - k_B T(u_e(\infty) - u_e(0)) = \sqrt{\frac{2k_B Tn_i}{N(E_F)^{a-Si:H}}}\sqrt{f^*(u_e(0), V_a)} \tag{C.2}$$

After differentiating Eq.(C.2) with the respect to V_a one obtains:

$$-q + k_B T\frac{du_e(0)}{dV_a} = \sqrt{\frac{2k_B Tn_i}{N(E_F)^{a-Si:H}}}\frac{1}{2}(f^*(u_e(0)))^{-1/2}\frac{df^*(u_e(0))}{du_e(0)}\frac{du_e(0)}{dV_a}, \tag{C.3}$$

with

$$\frac{df^*(u_e(0))}{du_e(0)} = \exp u_e(0) - \exp u_e(\infty) \tag{C.4}$$

Thus Eq.(C.3) can be rewritten as follows:

$$\frac{du_e(0)}{dV_a}\left[k_B T - \frac{\exp u_e(0) - \exp u_e(\infty)}{2\sqrt{f^*(u_e(0))}}\sqrt{\frac{2k_B Tn_i}{N(E_F)^{a-Si:H}}}\right] = q \tag{C.5}$$

$$\frac{du_e(0)}{dV_a} = \frac{q}{k_B T} \frac{1}{1 - \frac{\exp u_e(0) - \exp u_e(\infty)}{2\sqrt{f^*(u_e(0))}} \sqrt{\frac{2n_i}{k_B T N(E_F)^{a-Si:H}}}} \tag{C.6}$$

Taking into account Eq.(C.6) one can obtain for the term dI/dV_a

$$\frac{dI}{dV_a} = \frac{q}{k_B T} \frac{\exp u_e(\infty) - \exp u_e(0)}{\sqrt{f^*(u_e(0))}} \frac{1}{1 - \frac{\exp u_e(0) - \exp u_e(\infty)}{2\sqrt{f^*(u_e(0))}} \sqrt{\frac{2n_i}{k_B T N(E_F)^{a-Si:H}}}} =$$

$$= \frac{q}{k_B T} \frac{\exp u_e(\infty) - \exp u_e(0)}{\sqrt{f^*(u_e(0))} - \frac{\exp u_e(0) - \exp u_e(\infty)}{2} \sqrt{\frac{2n_i}{k_B T N(E_F)^{a-Si:H}}}} \tag{C.7}$$

Capacitance is thus given by

$$C = q n_i L_D^{c-Si} \frac{dI}{dV_a} \tag{C.8}$$

$$C = \frac{q^2 n_i}{k_B T} L_D^{c-Si} \frac{\exp u_e(\infty) - \exp u_e(0)}{\sqrt{f^*(u_e(0))} - (\exp u_e(0) - \exp u_e(\infty)) \sqrt{\frac{n_i}{2k_B T N(E_F)^{a-Si:H}}}} =$$

$$= \frac{\varepsilon}{2L_D^{c-Si}} \frac{1}{\frac{\sqrt{f^*(u_e(0))}}{\exp u_e(\infty) - \exp u_e(0)} + \sqrt{\frac{n_i}{2k_B T N(E_F)^{a-Si:H}}}}, \tag{C.9}$$

where

$$L_D^{c-Si} = \sqrt{\frac{\varepsilon k_B T}{2q^2 n_i}} \tag{10}$$

Considering $u_e(0)-u_e(\infty) \approx q/k_BT(V_d{}^{c\text{-}Si}-V_a)$ and $\exp[u_e(0)-u_e(\infty)]$ converging to zero the Eq.(C.9) can be rewritten:

$$C = \sqrt{\frac{\varepsilon q^2 n_i}{2k_B T}} \frac{1}{\sqrt{\frac{\exp\left[u_e(0)-u_e(\infty)\right]-1+u_e(\infty)-u_e(0)}{\exp u_e(\infty)\left(1-\exp\left[u_e(0)-u_e(\infty)\right]\right)^2}} + \sqrt{\frac{n_i}{2k_B T N(E_F)}}} =$$

$$= \sqrt{\frac{\varepsilon q^2 n_i}{2k_B T}} \sqrt{\frac{k_B T}{q} \exp u_e(\infty)} \frac{1}{\sqrt{V_d^{c-Si} - V_a - k_B T/q} + \sqrt{\frac{k_B T}{q}} \sqrt{\frac{N_D^{c-Si}}{2k_B T N(E_F)}}} =$$

$$= \sqrt{\frac{\varepsilon q^2 N_D^{c-Si}}{2}} \frac{1}{\sqrt{V_d^{c-Si} - V_a - k_B T/q} + \sqrt{\frac{N_D^{c-Si}}{2qN(E_F)}}} = \frac{\varepsilon}{\sqrt{\frac{2\varepsilon\left(V_d^{c-Si} - V_a - k_B T/q\right)}{qN_D^{c-Si}}} + \sqrt{\frac{\varepsilon}{q^2 N(E_F)}}} =$$

$$= \frac{\varepsilon}{w + L_D^{a-Si:H}} \tag{C.11}$$

with

$$w = \sqrt{\frac{2\varepsilon\left(V_d^{c-Si} - V_a - k_B T/q\right)}{qN_D^{c-Si}}} \tag{C.12}$$

List of symbols and abbreviations

α	Temperature coefficient
α_F	Temperature coefficient of the Fermi level
α_F	Temperature coefficient of the valence band
β	Reverse thermal voltage
$\Delta E_{C,}\, \Delta E_V$	Conduction and valence band offset
ε	Dielectric permittivity
ε_s	Dielectric permittivity of a semiconductor
ε_0	Vacuum dielectric permittivity
η	Ideality factor
ν_n	Attempt-to-escape frequency of electrons
σ	Conductivity
σ_n, σ_p	Electron and hole capture cross section
τ	Release time from gap states
$\tau_{c\text{-}r}$	Characteristic capture-release time
τ_{dr}	Dielectric relaxation time
τ_{max}	Time constant corresponding to the maximum of DLTS signal
τ_n, τ_p	Mean electron and hole lifetimes
Φ	Work function
χ	Electron affinity
ω	Angular frequency
ω_0	Turn-on angular frequency
A	Area
c_n, c_p	Electron and hole capture coefficient
C	Capacitance
$C_d^{a\text{-}Si:H}$	Capacitance associated to reponse of the defects
C_{dif}	Diffusion capacitance
C_{inv}	Capacitance associated to the time response of holes in the strong inversion layer
d	Distance between the parallel plates of a capacitor

$d^{a\text{-}Si:H}$	a-Si:H layer thickness
D^0, D^+, D^-	Neutral, positively and negatively charged dangling bond
D_{in}	Density of interface defects
e_n, e_p	Electron and hole emission rate
E	Energy
E_a	Activation energy
E_{cor}	Correlation energy
E_C	Conduction band energy
E_{DB}	Dangling bond defect energy
E_g	Energy band gap
E_F	Fermi energy
$E_F^{\ e}$, $E_f^{\ h}$	Quasi Fermi levels of electrons and holes
E_{mGauss}	Energy position of maximum of a Gaussian distribution
E_t	Energy level of trap state
E_V	Valence band energy
E_{vac}	Vacuum energy level
f	Frequency
f_{oc}	Occupation probability function
$f_{oc}^{\ dc}$, $f_{oc}^{\ ac}$	Dc and ac parts of the occupation function
G	Conductance
G_n, G_p	Electron and hole generation rate
$\hbar$	Normalized Planck constant
I	Complex unit
I_d	Diode current
I_n, I_p	Electron and hole currents at a junction
J_{sc}	Short circuit current density
k	Momentum
k_B	Boltzmann's constant
K	treatment of capacitance C: $K = \quad C^2\left(\frac{dC}{dT}\right)^{-1}$
L_D	Debye length
$L_d^{\ a\text{-}Si:H}$	Debye length in a-Si:H
$L_d^{\ c\text{-}Si}$	Intrinsic Debye length in c-Si
m_e, m_h	Electron and hole effective mass

n	Electron density
n^{dc}, n^{ac}	Dc and ac parts of electron density
n_i	Intrinsic carrier density
n_t	Density of occupied trap states
n_0	Equilibrium electron concentration
N	Density of states distribution in band gap
N_s	Shallow-level traps concentration
N_t	Traps concentration
N_A, N_D	Acceptors and donors concentration
N_B	Acceptors (for $N_D >> N_A$) or donors (for $N_D << N_A$) concentration
N_C, N_V	Effective density of states in the conduction and valence band
N_{CbT}, N_{vbT}	Density of states in the conduction and valence band tail
N_{DD}	Deep defect density of states
$N(E_C)$, $N(E_V)$	Density of states at the conduction and valence band edge
N_{0m}	Density of states of maximum of a Gaussian distribution
p	Hole density
p^{dc}, p^{ac}	Dc and ac parts of hole density
p_t	Density of unoccupied trap states
p_0	Equilibrium hole concentration
r	Interatomic distance
r_e	Distance between two electrons
$R_\mu^{a\text{-}Si:H}$	Resistance associated to transport in a-Si:H
$R_d^{a\text{-}Si:H}$	Resistance associated to the time response of the gap states in a-Si:H
R_h	Resistance associated to hopping
R_{inv}	Resistance associated to the time response of holes in the strong inversion layer
R_n, R_p	Electron and hole recombination rate
R_t	Resistance associated to tunneling
q	Elementary charge
Q	Charge
Q_m, Q_s	Charge stored in metal and semiconductor of a Schottky junciton
Q_n, Q_p	Charge stored in *n*- and *p*-side of a junction
t	Time
T	Temperature
T_C, T_V	Characteristic temperature of the exponential conduction and valence band tail

T_0	Turn-on temperature
w	Depletion width
w_{Gauss}	Width of a Gaussian distribution
v	AC voltage
v_{th}	Thermal velocity of free carriers
V	Voltage
V_a	Applied voltage
V_d	Diffusion potential
V_{int}	Intercept voltage with V_a axis of $1/C^2$ vs V_a plot
V_{oc}	Open circuit voltage
V_T	Thermal potential
x_n, x_p	Depletion width in n- and p-side of a p-n junction
x_ω	Cut-off abscissa

ac	Alternating current
a-Si	Amorphous silicon
a-Si:H	Hydrogenated amorphous silicon
AFORS-HET	Automat for simulation of heterojunctions
Al	Aluminium
AS	Admittance spectroscopy
BSF	Back surface field
CIGS	Copper indium diselenide
CP-AFM	Conducting probe atomic force microscopy
CPM	Constant photocurrent method
CRN	Continuous random network
c-Si	Crystalline silicon
CVD	Chemical vapour deposition
CZ	Czochralski
DB	Dangling bond
dc	Direct current
DLTS	Deep level transient spectroscopy
DOS	Density of states
EQE	External quantum efficiency
FZ	Float zone
G-R	Generation-recombination
HF	Hydrofluoric acid
HIT	Heterojunction with intrinsic thin layer
HOMOCVD	Homogeneous chemical vapor deposition
HWCVD	Hot wire chemical vapour deposition

ITO	Indium tin oxide
LPCVD	Low-pressure chemical vapour deposition
µc-Si	Microcrystalline silicon
µc-Si:H	Hydrogenated microcrystalline silicon
MIS	Metal - insulator- semiconductor
MOS	Metal-oxide-semiconductor
MOSFET	Metal–oxide–semiconductor field-effect transistor
MPC	Modulated photocurrent
PECVD	Plasma-enhanced chemical vapour deposition
PERL	Passivated emitter rear locally diffused
PHOTOCVD	Photo-assisted chemical vapor deposition
QSSPC	Quasi-steady-state photo conductance
RF	Radio frequency
SHJ	Silicon heterojunction
Sn	Tin
SSPC	Steady-state-photoconductivity
SSPG	Steady-state photocarrier grating
TCO	Transparent conductive oxide

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