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Par Bernardo LEITE

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Design and modeling of mm-wave integrated transformers in CMOS and BiCMOS technologies

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Directeurs de recherche :

M. KERHERVÉ, Éric	Professeur	IPB Bordeaux	Directeur de thèse
M. BÉGUERET, Jean-Baptiste	Professeur	Université Bordeaux 1	Co-directeur de thèse

Soutenue le : 22 novembre 2011

Devant la commission d'examen formée de :

M. BÉGUERET, Jean-Baptiste	Professeur	Université Bordeaux 1	Co-directeur de thèse
M. DUÊME, Philippe	Ingénieur	Thales TSA, Élancourt	Examinateur
M. FERRARI, Philippe	Professeur	UJF, Grenoble	Rapporteur
M. GIANESELLO, Frederic	Ingénieur	STMicroelectronics, Crolles	Examinateur
M. KERHERVÉ, Éric	Professeur	IPB, Bordeaux	Directeur de thèse
M. RIUS, Éric	Professeur	UBO, Brest	Rapporteur
M. VERDEYME, Serge	Professeur	Université de Limoges	Examinateur

A Rachel

Design and modeling of mm-wave integrated transformers in CMOS and BiCMOS technologies

Abstract

Millimeter-wave wireless communication systems have considerably gained in importance in recent years. Important applications as 60-GHz WLANs and WPANs, 80- GHz automotive radar, and 94 GHz imaging have emerged, requiring significant effort on the design of transceiver's silicon-based integrated circuits. In this context, integrated transformers are of a particular interest. They may perform, among other functions, impedance matching, single to differential conversion, and power combination. The design and modeling of this type of transformers is the subject of this thesis. A comprehensive study on the topology of transformers is presented, regarding the layout of individual coils, their relative position, geometric dimensions, substrate shields, and the achievement of high transformation ratios. Their modeling through electromagnetic simulations and a lumped-element electric circuit is discussed as well. The model presents a 2-π topology and analytical equations depending on both technological and geometric characteristics to evaluate the totality of its components. A close agreement between model and measurement is shown for 65-nm CMOS and 130-nm BiCMOS transformers up to 110 GHz. Those transformers are then applied to the design of a 77-GHz BiCMOS mixer and a 60-GHz CMOS power amplifier.

Conception et modélisation de transformateurs intégrés millimétriques en technologies CMOS et BiCMOS

Résumé

Les systèmes de communication sans fil en fréquences millimétriques ont gagné considérablement en importance au cours des dernières années. Des applications comme les réseaux WLAN et WPAN à 60 GHz, le radar automobile autour de 80 GHz ou l'imagerie à 94 GHz sont apparues, demandant un effort conséquent pour la conception des circuits intégrés émetteurs et récepteurs sur silicium. Dans ce contexte, les transformateurs intégrés sont particulièrement intéressants. Ils peuvent réaliser des fonctions comme l'adaptation d'impédance, la conversion du mode asymétrique au différentiel et la combinaison de puissance. La conception et la modélisation de ce type de transformateur font le sujet de cette thèse. Une étude détaillée des topologies de transformateurs est présentée, concernant le dessin des inductances, leur position relative, leurs dimensions géométriques, le blindage du substrat et l'obtention de rapports importants de transformation. Leur modélisation par des simulations électromagnétiques et par un circuit électrique à éléments discrets est également discutée. Le modèle présente une topologie 2-π et une série d'équations analytiques dépendant de ses caractéristiques technologiques et géométriques pour évaluer tous ses composants. Un très bon accord entre les simulations et les mesures est observé pour des transformateurs en technologies CMOS 65 nm et BiCMOS 130 nm jusqu'à 110 GHz. Finalement, les transformateurs sont appliqués à la conception d'un mélangeur BiCMOS à 77 GHz et un amplificateur de puissance CMOS à 60 GHz.

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List of Abbreviations

AC	Alternative Current
ACC	Automatic Cruise Control
ASK	Amplitude Shift Keying
AV	Audio/Visual
BEOL	Back End Of Line
BiCMOS	Bipolar-CMOS
CAD	Computer-Aided Design
CG	Conversion Gain
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common Mode Rejection Ration
DAMI	Dual Alternate Mark Inversion
DC	Direct Current
DUT	Device Under Test
EIRP	Equivalent Isotropically Radiated Power
EM	Electromagnetic
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
FoM	Figure of Merit
GMD	Geometric Mean Distance

GMSK	Gaussian Minimum Shift Keying
GPS	Global Positioning System
GSG	Ground-Signal-Ground
GSM	Global System for Mobile Communications
HRP	High-Rate Physical Layer
IC	Integrated Circuit
IF	Intermediate Frequency
IR	Infrared
ISM	Industrial, Scientific and Medical
LNA	Low-Noise Amplifier
LO	Local Oscillator
LRP	Low-Rate Physical Layer
LRR	Long Range Radar
LTE	Long-Term Evolution
MIMO	Multiple-Input Multiple-Output
MRP	Medium-Rate Physical Layer
MSK	Minimum Shift Keying
NF	Noise Figure
NLOS	Non Line Of Sight
OFDM	Orthogonal Frequency-Division Multiplexing
OOK	On-Off Keying
PA	Power Amplifier
PAE	Power Added Efficiency
PCELL	Parametric Cell
PGS	Patterned Ground Shield

PPA	Pre-Power Amplifier
PSK	Phase Shift keying
QAM	Quadrature Amplitude Modulation
RF	Radiofrequency
SC	Single Carrier
SOI	Silicon On Insulator
SRR	Short Range Radar
SSB	Single-Sideband
UMTS	Universal Mobile Telecommunications System
UV	Ultraviolet
VCO	Voltage-Controlled Oscillator
WPAN	Wireless Personal Area Networks
WLAN	Wireless Local Area Networks

Introduction

The wireless communication industry underwent a remarkable growth in the past few decades. Applications including mobile phones and computer networks have become an integral part of an ever-increasing number of people's lives and company's activities. As a result, telecommunication systems have become more and more complex, as new standards and protocols have been regularly issued, exploiting operating frequencies in the order of a few gigahertz.

In order to address such mass markets, the implementation cost of integrated circuits designed for wireless communications becomes a critical factor. One path to minimize such costs is to integrate in silicon as many components of a transceiver as possible. This may include analog and radiofrequency circuits as well as their associated passive components.

It is in this context that integrated transformers appear. They can perform a number of essential functions within RF building blocks, including balanced-to-unbalanced conversion (balun) and impedance matching, while presenting a wideband behavior and occupying a reasonable amount of silicon area. Due to this interest, comprehensive studies have been issued regarding the use of RF transformers [GHA06-1, LON00].

As a reflection of the evolution on the frequency properties of silicon technologies, mm-wave systems have considerably gained in importance. There may however be significant differences to traditional radiofrequency design. Design techniques are not necessarily the same and the intensity of the physical phenomena to which components, especially passives, are subject may as well differ. Hence, it is essential that an in-depth investigation regarding both design and modeling of mm-wave integrated transformers be carried out so that they can be fully exploited in mm-wave IC design as well. This thesis aims at addressing those concerns.

Chapter 1 discusses the emerging wireless applications in the millimeter-wave band along with the use of transformers in integrated circuits. The first presented applications concern WPANs and WLANs at 60 GHz. International regulations for unlicensed use of this band are presented as well as the most relevant standards and specifications published so far. Thereafter, automotive radar operating near 80 GHz and imaging in frequencies such as 94 GHz are also detailed. Regarding the use of transformers, their fundamental operating principle is firstly described. Then, the technological families used for wireless communications are discussed. Finally, a significant set of examples on the use of integrated transformers within microwave and mm-wave ICs are presented, highlighting the main functions transformers may perform.

Chapter 2 focuses on the design of integrated transformers in mm-waves, as well as on their characterization. Firstly, the employed measurement setup and the most relevant measurement issues for on-chip transformers are discussed. Secondly, the physical phenomena leading to non-ideal operation are investigated, along with a description of the employed integration technologies. A comprehensive study on the topology of transformers is then carried out regarding the layout of individual coils, their relative position, geometric dimensions, and the interest of using substrate shields in order to enhance winding quality-factors. Finally, a topology allowing to obtain high transformation ratios is proposed and analyzed.

The modeling of mm-wave integrated transformers is treated in Chapter 3. Their representation by means of electromagnetic simulations is firstly discussed, highlighting the adopted setup which allows to provide accurate results while consuming a moderate amount of computational resources. Their behavior is then modeled through a lumped-element electric circuit. The model presents a 2-π topology and equations to evaluate the value of the totality of its components. These equations depend on both technological and geometric characteristics of the transformer. The model is validated through experimental data of a set of 2–port 65-nm CMOS and 130-nm BiCMOS transformers. A close agreement is shown for both S-parameter and inductance values up to 110 GHz. Moreover, good accuracy is obtained for the simulations of transformers in a 4-port configuration. Finally, as the model was validated, a parametric cell was implemented in Cadence Virtuoso associating the electric model to the automatically generated layout of the transformer.

Chapter 4 presents the application of integrated transformers to the design of two mm-wave building blocks. The first one is a 130-nm BiCMOS active mixer operating at 77 GHz and the second is a 60-GHz 65-nm CMOS power amplifier. The mixer features transformers performing single-to-differential conversion and as part of the input matching network. Sizing of the transformer is detailed along with its amplitude and phase balance performances. The design of the input matching circuit integrating the transformer is presented, providing a 12-GHz bandwidth. Measured noise figure, conversion gain and compression point of the mixer are displayed and compared to the state of the art. The PA includes several transformer-based baluns and an output transformer-based power combiner. Model-based analyses are presented demonstrating the advantages of the use of a current-and-voltage combining architecture and an optimized balun topology. Measurement results are presented including S-parameters and large signal measures, such as gain, saturated power and compression point. Both mixer and PA are rated among the best performances in the state of the art.

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1 Millimeter-wave Applications

1.1 Introduction

Electromagnetic waves offer a prolific support for a myriad of applications in the domain of telecommunications. Historically, the different regions of the electromagnetic spectrum have been exploited for very distinct uses. Audio broadcasting, for instance, had a notable development in the first decades of the 20th century employing the lower end of radiofrequencies (RF). It took advantage of long, medium, and short waves (between 150 kHz and 150 MHz), transmitting amplitude or frequency-modulated signals, as it is still currently done. With the later advent of television, the necessity of transmitting larger amounts of data to include image information drove this broadcasting system into more elevated frequencies attaining the microwave range.

In recent years, new applications of wireless communications in the region of microwave frequencies flourished. A meaningful example is constituted by mobile phone networks. Systems with increasingly higher complexity and data rates were engineered and widely adopted, symbolized by standards such as GSM, UMTS and LTE, for frequencies between 700 MHz and 2.6 GHz. Along with these advances, networks providing wireless data transmission for shorter distances have also been developed. This is distinctively the case of wireless local area networks (WLANs) and wireless personal area networks (WPANs). The most remarkable representative of WLANs is the series of IEEE 802.11 standards commonly labeled as Wi-Fi. In its most traditional forms (802.11b and 802.11g) it employs the ISM 2.4 GHz band allowing data rates as high as 54 Mbit/s, whereas the 802.11n variant, which exploits the 5 GHz band as well, enhances the attainable maximal bit rate to 600 Mbit/s. Microwave WPANs on the other hand are most distinctively represented by the Bluetooth standard [IEE05]. It also operates in the 2.4 GHz band and typically allows transfer rates of up to 3 Mbit/s. Finally, microwaves provide support to a number of radar applications as well as to the Global Positioning System (GPS).

Further in the frequency spectrum lie the visible light, infrared (IR) and ultraviolet (UV) radiation. Those components, whose boundaries are roughly considered between 3 THz and

30 PHz, are object to the study of the Optical sciences. Such frequencies are, by nature, suitable to a multitude of imaging uses, including but not limited to applications in astronomy, medicine and security. Moreover, infrared rays have also been used to establish short range data transmission as WPANs [IRD11].

Wavelengths immediately smaller than those of ultraviolet define the region of X-radiation. Among their possible applications, the use at medical and security-oriented imaging clearly stands out. In addition to the widespread use in radiography to the depiction of the skeleton and a number of internal tissues, X-rays have successfully been introduced into airport security devices. Such devices include luggage scanning as well as passenger screening with the recent advent of backscatter units [TSA11].

Comparatively to the aforementioned bands, the rise of terahertz and, most especially, mm-wave applications is a recent phenomenon. The mm-waves are defined as the portion of the electromagnetic spectrum comprising free-space wavelengths between 1 and 10 mm, which translates into frequencies in the interval between 30 and 300 GHz. Those frequencies have been object to a convergence of applications which had been traditionally restricted to different regions of the spectrum. In this study, three groups of applications are of a particular interest and will be discussed in more depth. They include WLANs and WPANs which are treated as a direct evolution to the wireless networks operating at microwaves, as well as automotive radar, which has risen as a new application, but inherits the principles of microwave radar. In addition, mm-wave imaging will be investigated as they are considered as a replacement or a complement to the possibilities offered by conventional optical and X-ray-based systems.

Figure 1-1 outlines the relevant portions of the electromagnetic spectrum and their associated frequencies and wavelengths. The boundaries illustrated in this figure are by no means rigid but rather indicative of their positions within the spectrum.

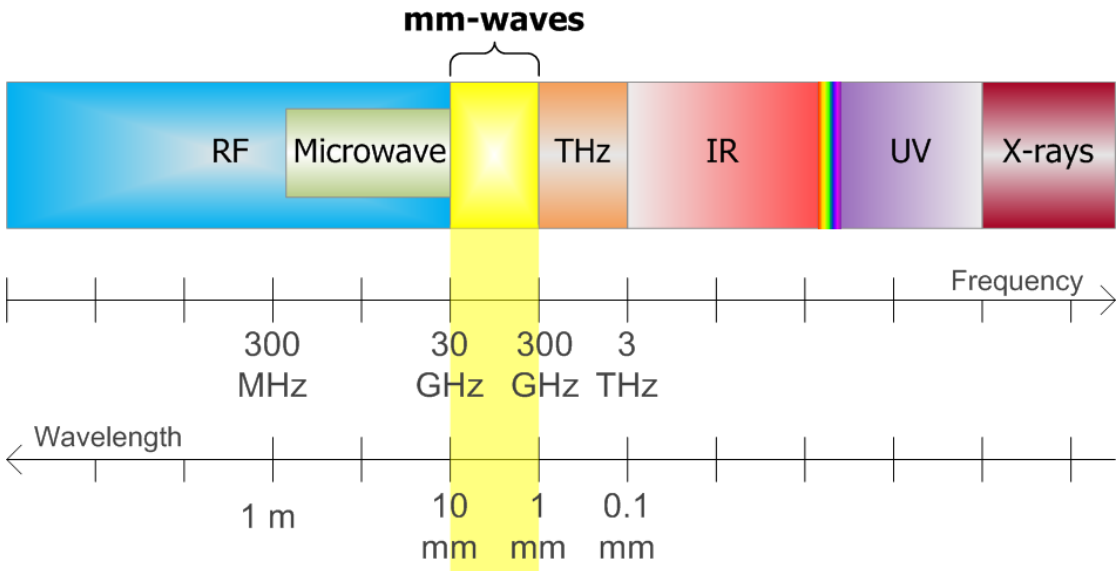


Figure 1-1 Representation of the electromagnetic spectrum.

1.2 WPAN / WLAN

As wireless network technologies evolve, an ever-increasing demand of higher data rates arises in order to support new applications. Three solutions are usually presented to address this demand: the use of more complex modulation schemes, the adoption of wider channel bands, and the development of new architectures of transceivers.

Especially in what concerns WPANs and WLANs, those three paths have been investigated. One noteworthy architectural innovation has been the use of multiple-input and multiple-output (MIMO) designs, which allow different data to be simultaneously transmitted through different antennas [ALO10-1]. Such techniques have been for instance successfully implemented in the IEEE 802.11n standard for microwave WLANs. As far as modulation is concerned, nevertheless, even though the use of very high order schemes could be feasible, it would require a substantial amount of additional transmit power to provide equivalent bit error ratios [SMU02].

In order to ensure data rates greater than 1 Gbit/s, the most suitable solution has been to operate in the mm-waves. In the vicinity of 60-GHz, in particular, a band of several gigahertz is defined for unlicensed use, which can be exploited for WPANs and WLANs. Furthermore, considerably high power levels are authorized, which favors the communication. Moreover, the 60-GHz band presents a number of characteristics which makes it especially suited for such short-range applications.

Unlike lower frequencies, where transmission loss can be mostly accounted to free space propagation, at mm-waves the absorption properties of gases present in the atmosphere play a major role [FCC97]. In particular for frequencies between 10 and 100 GHz, the behavior of water vapor and oxygen molecules predominate [ITU01]. Figure 1-2 depicts the average atmospheric absorption for mm-waves at sea-level. A number of peaks can be observed in the curve, corresponding to the resonances of those two gas molecules, including one at 60 GHz, which is due to oxygen absorption [OLV89].

Moreover, waves at 60 GHz are strongly attenuated by solid obstacles such as walls. For instance, a 15-cm concrete wall can cause an attenuation of up to 36 dB in a transmitted signal [SMU02]. Those characteristics have important consequences on the applications which can be addressed at this frequency. First of all, they will be limited to short range communications and, more specifically, to an indoor environment confined in a single room. Since interference is minor due to their attenuation properties, a high degree of frequency reuse is possible for 60-GHz systems, so that WLANs and WPANs can be successfully implemented at those frequencies.

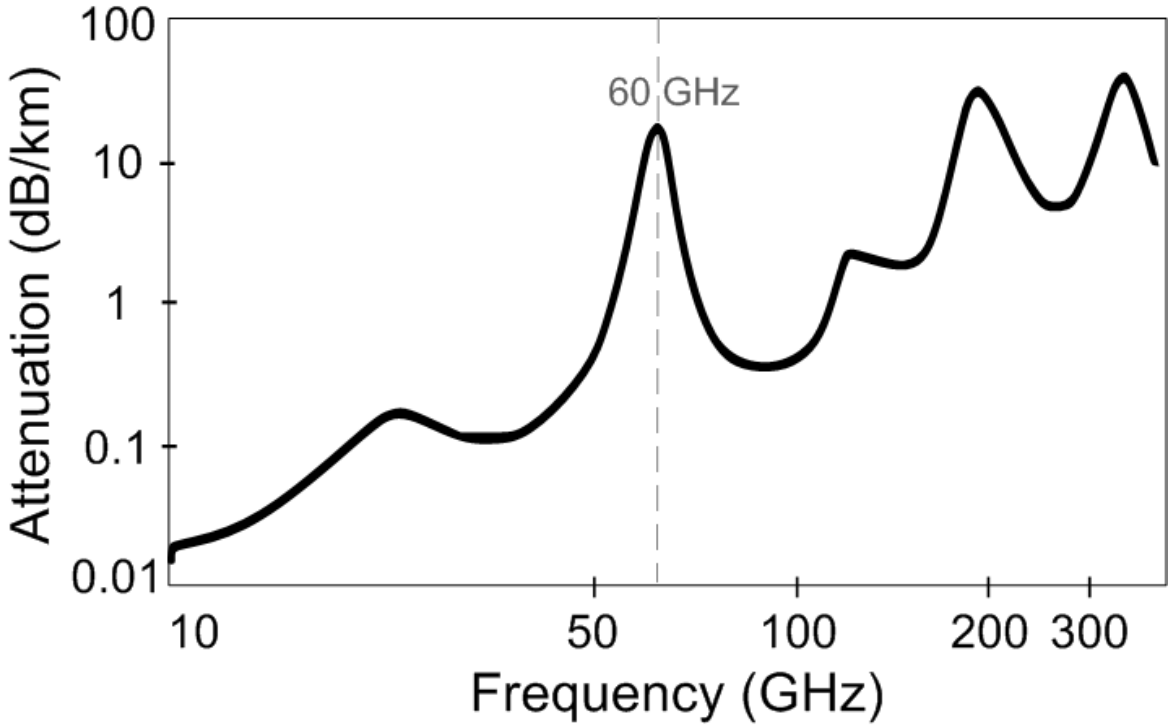


Figure 1-2 Average atmospheric absorption for mm-waves at sea-level.

1.2.1 60-GHz regulations

It has been mentioned that a considerably wide band is available for unlicensed use at 60 GHz. As a matter of fact, the limits of this band depend on the regulations adopted by each concerned country. Another important feature for such wireless applications is the authorized transmit power levels, usually expressed in terms of the equivalent isotropically radiated power (EIRP). As it is further detailed, the allowed EIRP is relatively high at this band which is another factor favoring the implementation of high data rate WLANs and WPANs at 60 GHz.

In 1995 the Federal Communications Commission (FCC) in the United States established the band comprised between 59 and 64 GHz as license-exempt for communication devices, and in 2000 extended this range to include 57 – 59 GHz [FCC02]. Current FCC regulations, specifically part 15.255 of their code, define uniform rules for this 7-GHz band [FCC09]. The authorized average EIRP level, measured during the transmit interval, is 40 dBm, whereas the maximum EIRP cannot exceed 43 dBm.

Following this development, other countries decided to implement regulations complying with FCC specifications. It is particularly the case of Canada, through their Spectrum Management and Telecommunications authority, and Brazil, through the National Telecommunications Agency (Anatel). Therefore, both countries have allocated the 57 – 64 GHz band for unlicensed use with respective maximum and average EIRPs of 43 and 40 dBm [ANA08, CAN10].

The European Union has adopted the standard EN 302 567 issued in 2009 by the European Telecommunications Standards Institute (ETSI) [ETS09-1]. It assigns the 57 – 66 GHz band as unlicensed for short-range devices. Unlike American regulations, the average EIRP level

is not specified. Instead, different maximum EIPR levels are defined depending on the applications: 40 dBm for indoor-only, and 25 dBm for a combined indoor and outdoor use.

Another country to discern indoor and outdoor applications in their rules was Australia. The Australian Communications and Media Authority compiled their Radiocommunications (Low Interference Potential Devices) Class Licence 2000 [AUS11] defining frequency range and maximum EIRP for data communications systems in the 60 GHz band. For outdoor use, the authorized band is limited to the 59 – 63 GHz range and the maximum EIRP is 52 dBm. For indoor use, on the other hand, which is mostly aimed for WLANs and WPANs, a wider band is allocated (57 – 66 GHz) but an inferior radiated power is permitted (43-dBm maximum EIRP).

In Asian countries the 60-GHz regulations differ as well. In Japan, the Ministry of Internal Affairs and Communications has allocated the 59 – 66 GHz for data transmission systems [MIC07], whereas, according to [YON11], the available bands in South Korea and China are respectively 57 – 66 GHz and 59 – 64 GHz. Moreover, [YON11] provides information on the maximum EIRP authorized in two of these countries; 57 dBm in Japan, and 27 dBm in South Korea.

The defined frequency bands and maximum specified EIRPs for indoor applications are summarized in Figure 1-3 and Figure 1-4. A common 5-GHz band is observed in all considered countries and a bandwidth of at least 7 GHz is specified for all but Chinese regulations. In terms of transmit power, excepting the South Korean, all of them permit EIRPs attaining 40 dBm. The combination of these two factors enabled the development of high data throughput communication standards.

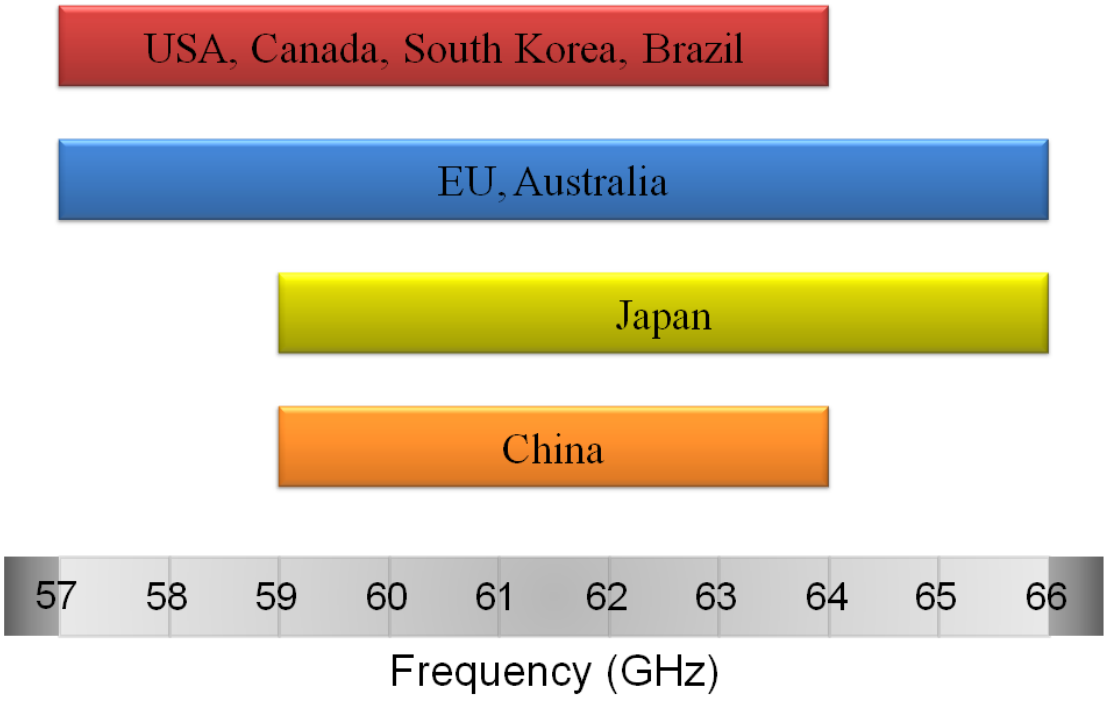


Figure 1-3 International unlicensed frequency allocation around 60 GHz.

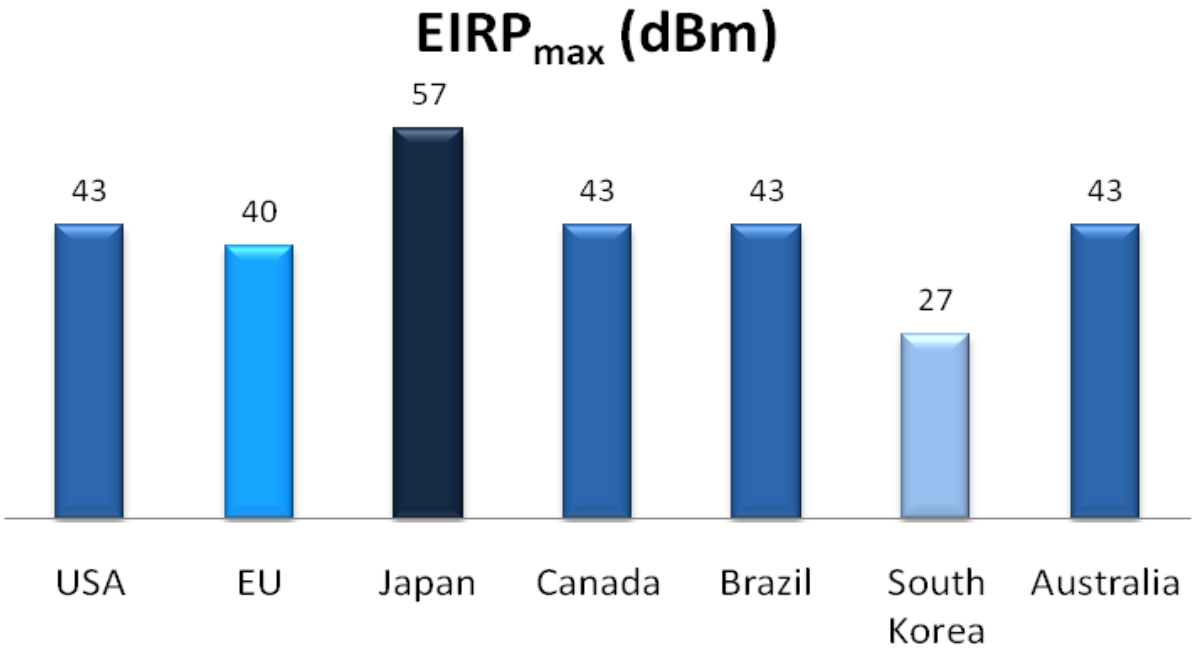


Figure 1-4 Internationally authorized maximum EIRP for indoor uses.

1.2.2 Standards

The combination of favorable properties of the 60-GHz band has stirred industry to support the development of a number of short-range wireless communication standards. The most relevant among these standards include ECMA 387/ ISO-IEC 13156, IEEE 802.15.3c, and WirelessHD for WPANs, and WiGig and IEEE 802.11ad for WLANs.

Even though some of the applications aimed at 60-GHz are situated near the boundaries between WLANs and WPANs, the distinction we adopt between these classes of networks is the same adopted by IEEE within their standardization groups. As it is stated in their 802.15.1 standard [IEE05]:

Wireless personal area networks (WPANs) are used to convey information over short distances among a private, intimate group of participant devices. Unlike a wireless local area network (WLAN), a connection made through a WPAN involves little or no infrastructure or direct connectivity to the world outside the link.

In other words, WLANs and WPANs are essentially distinguished by whether they are necessarily self-contained or they are able to operate as a bridge allowing connection to other networks in a higher level. This distinction becomes clear when traditional microwave standards are compared; while Wi-Fi is capable of enabling an Internet connection, Bluetooth uniquely concerns a small number of devices directly involved in the transfer link.

The most significant current 60-GHz standards for WPANs and WLANs are discussed hereafter. The modulation techniques and maximum data rates for the various operating modes of these standards are compiled in Appendix A.

1.2.2.1 ECMA 387/ ISO-IEC 13156

One of the firstly issued internationally recognized standards for short-range wireless communications was the ECMA 387 *High Rate 60 GHz PHY, MAC and PALs*. Their first edition was published in December 2009 [ECM08] and subsequently recognized as an ISO-IEC standard as well (ISO-IEC 13156). A second edition was issued in December 2010 [ECM10], which is, at the time of writing, under appreciation by ISO-IEC technical commissions.

The standard targets WPAN applications. Among the main identified usages, the streaming of high-definition uncompressed video, the implementation of wireless docking stations, as well as *Sync and Go* terminals may be cited.

The communication takes place within the 57 – 66 GHz range. More precisely, four unity channels are defined between 57.24 and 65.88 GHz. In order to increase the obtainable data rates, any adjacent channels can be bonded together, resulting in possible channel widths of 2.16, 4.32, 6.48, and 8.64 GHz. Those possibilities are illustrated in Figure 1-5.

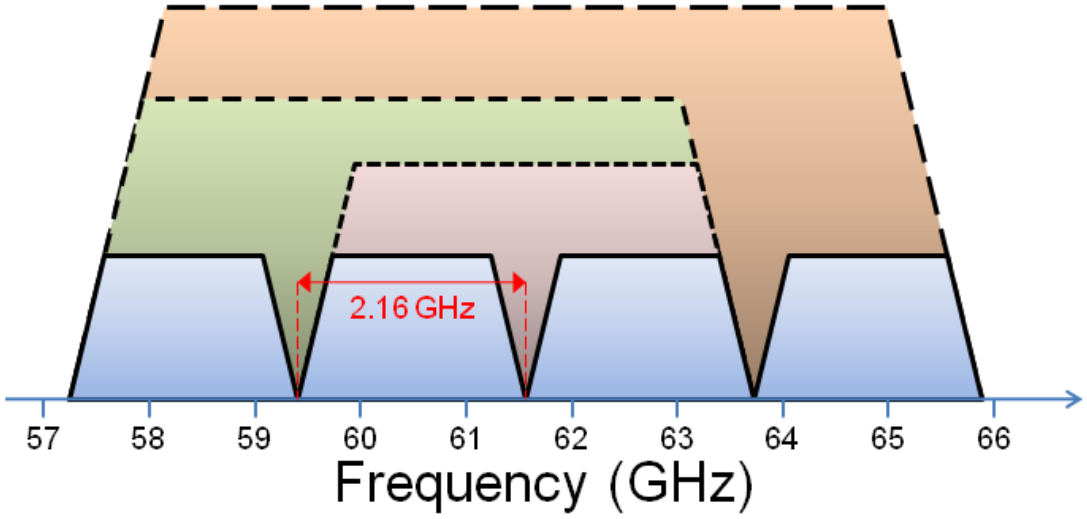


Figure 1-5 Channel allocation for 60-GHz standards. Channel bonding is authorized for ECMA 387.

According to their characteristics, different types of devices are defined. Type A devices provide the highest performances, attaining a 10-meter reach and integrating beamforming in order to allow non-line-of-sight (NLOS) communication. Type B devices are intended to provide a lower power consumption along with a simpler implementation, which comes at the expense of NLOS capabilities and communication range, which may be limited to 3 meters. Additionally, and exclusively for the first edition of the standard, Type C devices are defined as well. Those devices consume less and are less complex than Type B devices, and their operation is limited to ranges shorter than 1 meter.

Each defined device type can function under different operation modes, employing different modulation schemes. Such schemes include single carrier (SC) and orthogonal frequency-division multiplexing (OFDM), and, in the first edition, dual alternate mark inversion (DAMI) modulations. In terms of their constellations, different variations of PSK are employed, along with QAM implementations for type A and type B devices. Moreover, for type C devices,

amplitude shift keying schemes are used, namely OOK and 4ASK. The highest attainable data rates are then 25.402 Gbit/s for type A, 12.701 Gbit/s for type B, and 3.2 Gbit/s for type C devices.

1.2.2.2 IEEE 802.15.3c

In September 2009, the amendment 2 entitled Millimeter-wave-based Alternative Physical Layer Extension for the IEEE standard Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for High Rate Wireless Personal Area Networks (WPANs), known as IEEE 802.15.3c was released [IEE09].

As it targets WPANs as well, this standard presents a number of similarities with ECMA 387. The covered frequency band, for instance, is the same (between 57.24 and 65.88 GHz), and so are the 2.16-GHz wide unity communication channels. Channel bonding, nevertheless, is not specified for this standard.

Three operation modes are defined, in order to target different applications. The single carrier mode (SC) is mostly intended for kiosk file downloading, allowing systems to present a lower level of complexity and cost. The second mode is the high speed interface (HSI) which addresses the implementation of ad-hoc networks. The constraints for such applications are to provide bidirectional high speed links with a low latency. Finally, the audio/visual mode (AV) targets the streaming of audio and video. It is divided into two submodes, the low-rate (LRP) and the high rate (HRP), which provides the high data throughput required for high-definition uncompressed video.

All of these modes allow the use of beamforming techniques to allow NLOS communication. Unlike in the SC mode, OFDM is used for HSI and AV. The SC mode employs various modulation schemes (MSK, BPSK, QPSK, 8PSK, 16QAM, OOK, DAMI), and allows a maximum 5.28-Gbit/s throughput, whereas the HSI mode may present QPSK, 16QAM and 64QAM constellations, with a maximum data rate of 5.775 Gbit/s. For the AV, a BPSK modulation is used for the LRP, and QPSK and 16QAM are used for HRP. The maximum data rate attainable with this mode is 3.807 Gbit/s.

1.2.2.3 WirelessHD

A different WPAN specification was issued by a consortium of industry manufacturers in 2008. This specification was subsequently updated to the WirelessHD version 1.1 in 2010 [WHD10]. Even though it can be applied to various uses, it mostly targets uncompressed high-quality video streaming for a range of up to 10 m.

The WirelessHD specification adopts the same channel constitution of the previously described standards. It comprises 3 communication modes: the high rate (HRP), medium rate (MRP), and low rate (LRP). HRP and MRP modes are used to establish directional unicast links attaining throughputs as high as 7 Gbit/s for a single stream. Moreover, if spatial multiplexing is

employed, the date rate can rise to up to 28 Gbit/s. LRP, alternatively, also allows omni-directional and, hence, broadcast communication. All modes use OFDM modulation, with QPSK, 16QAM and 64QAM constellations for HRP and MRP, and BPSK for LRP.

1.2.2.4 WiGig / IEEE 802.11ad

Concerning WLANs, one relevant specification was published by the Wireless Gigabit (WiGig) Alliance in 2010 [WGI10]. This specification was then contributed to constitute the basis for a mm-wave amendment to the IEEE 802.11 standard, which is entitled *Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications* [IEE10]. This amendment is referred to as the IEEE 802.11ad and is expected to be published in 2012.

This specification is intended to allow full compatibility with Wi-Fi networks operating at 2.4 GHz and 5 GHz so that devices should be able to transparently switch among these networks. Hence, future systems are expected to adopt 60-GHz links for communication within a room, and 5-GHz when obstacles such as walls should be placed between terminals.

As for the described WPAN standards, four 2.16-GHz wide channels are defined in the range between 57 GHz and 66 GHz. Beamforming is once again supported and the targeted communications distances may exceed 10 meters.

Three modes are defined: one using OFDM and two using single carriers, including a mode which is optimized for low power consumption, targeting handheld devices. The low-power SC mode adopts BPSK and QPSK modulations, with a 2.5-Gbit/s maximum throughput, whereas the SC mode also uses 16QAM constellations allowing data rates as high as 4.6 Gbit/s. The OFDM mode employs QPSK, 16QAM, and 64QAM constellation, allowing to obtain data rates approaching 7 Gbit/s.

1.3 Automotive radar

Recent years have experienced significant technological advances in the automotive industry. Among these advances, a large part can be attributed to the incorporation of more and more electronic systems within vehicles. This evolution was driven toward improving the performance of the vehicles and the comfort of drivers and passengers but also, which has become their most important concern, toward ameliorating their safety.

It is in this context that the use of automotive radar has risen. It firstly appeared through the implementation of automatic cruise control (ACC) systems. Such systems scan the position of other vehicles in front of them in order to automatically maintain a safe cruising distance. More recently, a multitude of new applications emerged. One of them is obstacle detection and collision warning. In addition to warning the driver, such functions enable preemptive actions to be taken, including emergency braking, pre-tensioning seat belts or airbag arming. Other relevant applications comprehend parking aid and lane change assistance, which includes blind spot

detection to warn the driver or perform preemptive braking as well. The implementation of these functions requires a 360° coverage surrounding the vehicles, which is referred to as a *safety belt* (Figure 1-6).

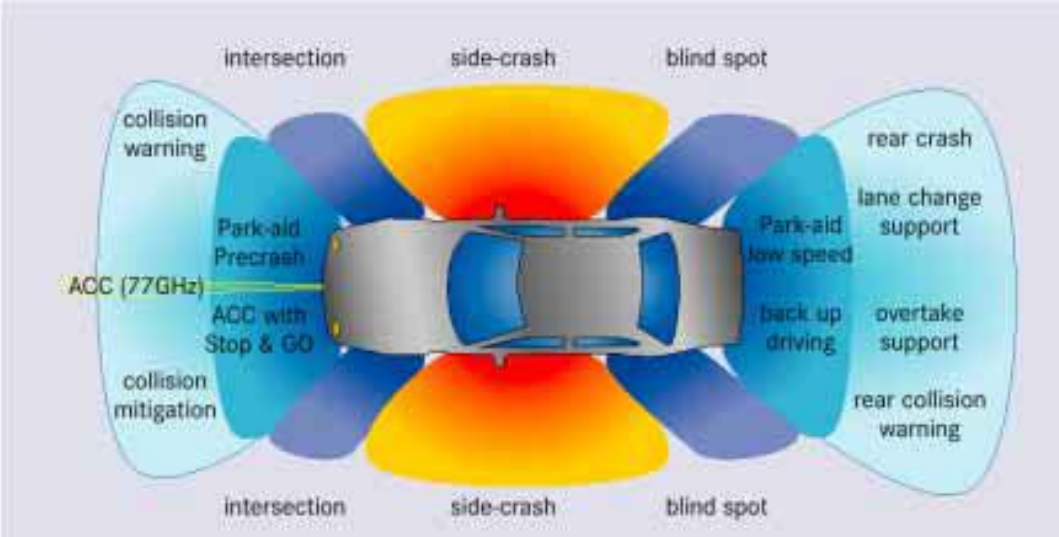


Figure 1-6 *Safety belt* for vehicles with SRR and LRR [ETS04].

1.3.1 Regulations

All the mentioned automotive radar applications are classified into two groups according to the communication range they are intended to address. Long range radar (LRR) comprehends ACC applications which present an operation distance of up to 150 m. Most of the other functions comprised in the *safety belt* require communications distances inferior to 30 m and hence fall into the short range radar (SRR) category [ETS04].

SRR functions rely on accurate measurements of the position and speed of objects surrounding the vehicles. In order to operate accordingly, some of these functions might require spatial resolutions as fine as 5 cm. For this reason, in contrast with LRR applications, SRR should require a considerably larger bandwidth.

Hence, according to the targeted application, different bands are allowed for automotive radar. For LRR, a 1-GHz bandwidth is appropriate and there is a certain international consensus regarding the 76 – 77 GHz band. It is namely the case for the United States and Canada which define this band *as restricted to vehicle-mounted field disturbance sensors used as vehicle radar systems* [CAN10, FCC09]. In the European Union, it is also defined that *the band 76-77 GHz shall be used for vehicular or infrastructure radar systems* [ECC02]. Analogously, Japan and Australia have set this band aside for vehicle radars [AUS11, MIC07].

Regarding SRR, for which a wider band is necessary, two regions in the spectrum are mostly considered; around 24 GHz and 79 GHz. In the United States, for instance, the FCC allocated the band comprised between 23.12 GHz and 29 GHz for this usage [FCC09]. Japan, as well, has defined regulations for 24 GHz and 26 GHz radar [SAR11]. The European Union, in contrast, has been more prominent on the regulation of mm-wave radar. Since a relevant part of

the spectrum around 24 GHz is reserved for radio astronomy applications, EU authorities defined the 77 – 81 GHz for wideband automobile radar [EU04]. Nevertheless, as the development of sensors for SRR applications operating at those frequencies is not yet sufficiently advanced to allow mass industrial production, the 24 GHz band has been temporarily authorized for this use. Hence, a calendar has been set for this band deployment, under the condition that vehicles using 24-GHz radar cannot exceed 7% of the fleet in any of the concerned states. Initially, and till 2013, the band between 21.65 GHz and 26.65 GHz is granted for automotive radar and then, between 2013 and 2018, new vehicles will only be authorized to employ the upper portion of this band, i.e., between 24.25 GHz and 26.65 GHz [EU05, EU11].

Following these definitions, Australian authorities have as well regulated the 79 GHz band, according to the European standards [AUS11]. It is expected that, as 79-GHz radar establishes itself in Europe, other regions decide for their adoption as well.

1.3.2 Standards

The European Telecommunications Standards Institute (ETSI) has published a series of communications standards complying with European regulations with regards to mm-wave automobile radar. Among these, the most relevant are ETSI EN 301 091 [ETS06], which adresses LRR, and ETSI EN 302 264 [ETS09-2], targeting SRR.

1.3.2.1 ETSI EN 301 091

Despite being entitled *Short Range Devices; Road Transport and Traffic Telematics (RTTT); Radar equipment operating in the 76 GHz to 77 GHz range*, the ETSI EN 301 091 standard is perfectly suited to what is here defined as long-range radar. Indeed, its main targeted application is identified as ACC.

The standard, whose version 1.3.3 was released in 2006, defines two classes of devices. Class 1 devices communicate using frequency-modulated continuous-wave techniques or FSK, and their average EIRP cannot exceed 50 dBm. Class 2, on the other hand, account for pulse modulation, whose maximum allowed average EIRP is 23.5 dBm. The maximum peak EIRP for both classes is specified at 55 dBm.

1.3.2.2 ETSI EN 302 264

In 2009, the ETSI EN 302 264 standard, entitled *Short Range Devices, Road Transport and Traffic Telematics (RTTT); Ultra Wide Band Radar Equipment Operating above 60 GHz*, was released in its version 1.1.1. This standard is intended for SRR applications in the 77 – 81 GHz band with a peak EIRP of 55 dBm.

Several modulation schemes are regarded. They include:

- Pseudo noise pulse position modulation ;

- Pulsed frequency hopping;
- Pseudo noise coded amplitude shift keying;
- Pseudo noise coded phase shift keying;
- Frequency modulated continuous wave.

1.4 Imaging

The first automatic imaging systems were developed in order to detect radiation in the visible part of the electromagnetic spectrum. Whereas this was the most natural approach, it was subsequently observed that a large amount of relevant information could be extracted if other portions of the spectrum were to be considered. Hence, infrared, ultraviolet and X-ray-based imagers were developed in order to address a various range of applications, including medical and security-related uses.

As mm-wave systems evolved, some of these applications found a favorable alternative to be exploited. The frequencies better adapted to this use are 35, 94, 140, and 220 GHz, which correspond to the atmospheric propagation windows, i.e., the minima observed in Figure 1-2. Moreover, as for many of current applications, 94-GHz systems are usually adopted [YUJ03].

Imaging systems may be classified into two fundamental categories: active and passive. Passive systems limit themselves to detect both the power emitted and reflected by the observed objects in order to generate an image by associating a color to each power level. Active imaging, on the other hand, includes as well the generation of a wireless signal which is directed onto the considered target. Whereas passive systems are simpler to implement and do not depend on power regulations, active imagers are usually able to detect lower power levels in the presence of different sources of noise [AGU07].

The security domain constitutes one of the major areas for mm-wave imaging systems. This is especially true for applications as concealed weapons detection, which have particularly gained importance in sensitive locations, such as airports. This mm-wave radiation is capable of penetrating clothing while being partially reflected by human skin. As the reflection pattern of metals, but also plastics, ceramics and liquids are readily detectable for radiation at these frequencies, mm-wave imagers have been considered as a superior alternative to traditional metal detectors [SHE96]. Figure 1-7 illustrates the generated images of mm-wave systems deployed in airports.

Another significant use of mm-wave imagers is for medical purposes. It supplies an interesting alternative to the use of X-rays with the advantage of presenting a non-ionizing nature. Furthermore, as the necessary circuitry can be integrated in silicon their use may be proven advantageous in terms of cost as well [ARB10].

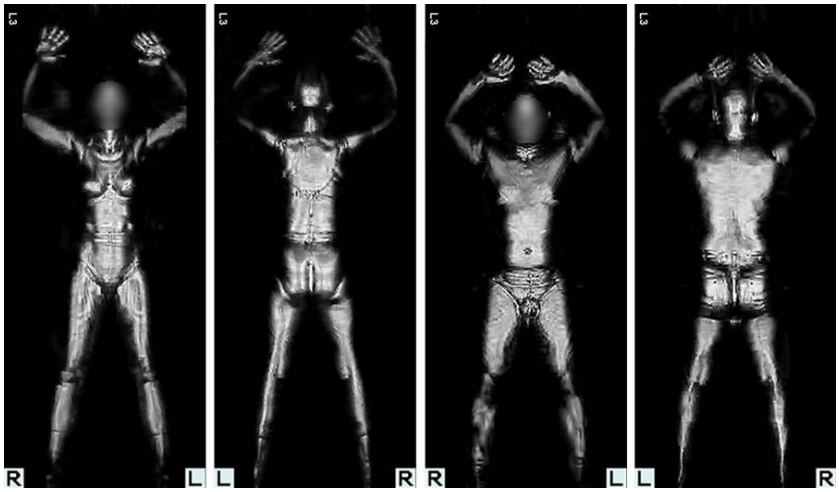


Figure 1-7 Millimeter-wave images used for concealed weapon detection [TSA11].

2 Transformers

2.1 Basics

A transformer is constituted by the combination of two magnetically coupled inductors, which are referred to as the primary and the secondary. Such coupling results from the fact that a portion of the magnetic flux generated by a time-varying primary current also crosses the secondary inductor. This coupling is expressed in terms of a mutual inductance.

Inductances are defined as the ratio between magnetic flux and electric current. Considering Figure 1-8 where primary and secondary are represented, if a current is applied to the primary, and the secondary terminals are left open, i.e. $i_S = 0$, then the primary voltage will not be affected by the secondary and will only depend on its self inductance L_P and the time-variation rate of the current di_P/dt, as in (1-1). Moreover, this primary current variation will induce a voltage in the secondary, which will be proportional to the mutual inductance M.

$$v_P = L_P \cdot \frac{d\,i_P}{d\,t} \tag{1-1}$$

$$v_S = M \cdot \frac{d\,i_P}{d\,t} \tag{1-2}$$

As the mutual inductance is symmetrical in both directions, the voltage–current relations in the general case, i.e., when currents are applied to both windings are expressed as follows:

$$v_P = L_P \cdot \frac{d\,i_P}{d\,t} + M \cdot \frac{d\,i_S}{d\,t} \tag{1-3}$$

$$v_S = L_S \cdot \frac{d\,i_S}{d\,t} + M \cdot \frac{d\,i_P}{d\,t} \tag{1-4}$$

Or, in complex notation for a sinusoidal excitation:

$$V_P = j\omega L_P \cdot I_P + j\omega M \cdot I_S \quad (1\text{-}5)$$

$$V_S = j\omega L_S \cdot I_S + j\omega M \cdot I_P \quad (1\text{-}6)$$

These relations, associated to the fact that primary and secondary electrical powers are identical for such lossless transformers, lead to a constant impedance ratio of the transformer, which is traditionally associated to the ratio of the number of turns constituting each coil. Thus:

$$N = \frac{V_P}{V_S} = \sqrt{\frac{L_P}{L_S}} \quad (1\text{-}7).$$

This means that any load placed in the secondary side is seen by the primary as multiplied by N^2. This property of impedance transformation is one of the most useful features in the use of transformers in electronic circuits.

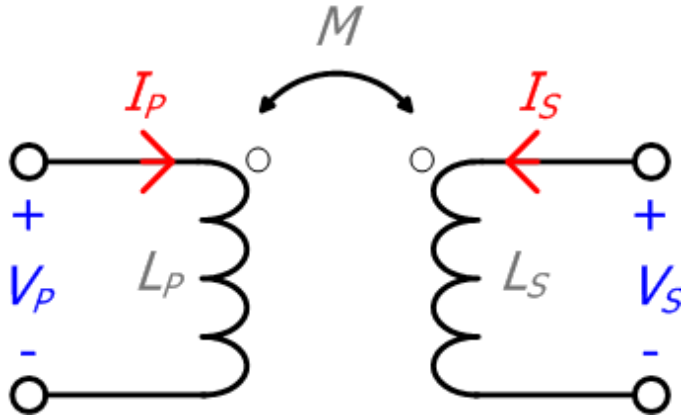


Figure 1-8 Fundamental circuit representation of a transformer.

These considerations assume an ideal purely inductive operation of the transformer. Actual implementations necessarily include additional resistive and capacitive components though. This is especially true for RF and mm-wave realizations, for which such components cannot be neglected. Their functionality remains nevertheless present and the use of RF and mm-wave transformers is shown to be advantageous in several aspects.

2.2 Integrated circuits context

Since recent telecommunications systems are implemented through the extensive use of integrated circuits (ICs), the evolution of the technologies which can be adopted for such applications is crucial. In this context, two technological families stand out: silicon-based and III-V compound technologies. Among the most relevant III-V technologies, GaAs, InP and the emerging GaN may be mentioned, whereas the silicon-based category includes not only pure Si CMOS processes, but also combinations with other group IV elements, such as SiGe, and SiGe:C.

Due to their high frequency performances, expressed most significantly in terms of the attainable transition frequency (f_t) and maximum oscillation frequency (f_{MAX}) of their transistors, III-V components have been traditionally preponderant in microwave and mm-wave applications. Silicon-based technologies, on the other hand, have been prominent in digital and lower frequency applications. For this reason, production volumes of Si circuits are largely superior, which yields lower costs and has attracted higher investments in research and infrastructure [ITR09-1]. These factors favored the development of new silicon technologies, which benefit from both vertical and horizontal scaling of devices, and are therefore able to successfully address microwave and mm-wave operation. Figure 1-9 illustrates the recent evolution of the transition frequency for silicon-based technologies.

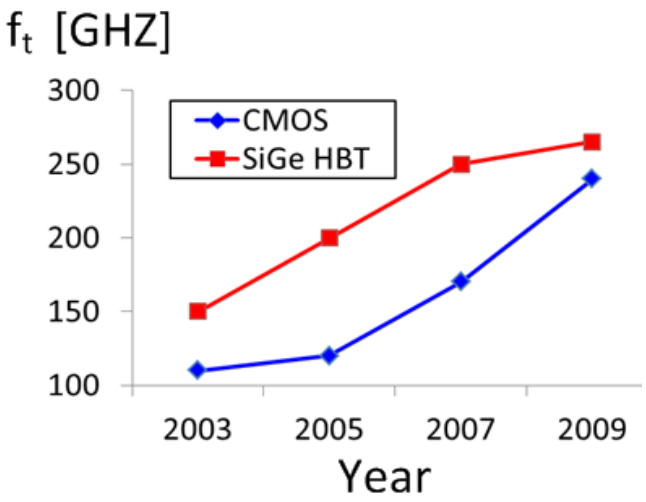


Figure 1-9 Transition frequency evolution of silicon-based transistors.

An important current trend on transceivers for telecommunication circuits is the System on Chip (SoC) concept. It aims to integrate in the same chip digital, analog, and radiofrequency circuits, including their associated passive components. This approach proves to be consistently cost-effective; nevertheless, a number of implementation issues arises. Indeed, in spite of the potential constraints concerning CMOS transistors, the integration of passives is considered to be particularly limiting to determine the overall performance of the circuits. This leads to two paths of optimization to ensure the integration of sufficiently high-quality passives. From one side, the technological process requires some modifications in comparison to standard digital technologies. These modifications may include the use of thicker metal levels or dielectric layers with a higher permittivity. Naturally, such improvements come at the expense of additional processing steps, and hence higher fabrication costs. Since globally, however, they are intended to reduce the costs in comparison to a realization with off-chip components, a substantial amount of effort needs to be made as well in what concerns passive design optimization.

2.3 Transformers in integrated circuits

Among the passive components employed within wireless communication circuits, integrated transformers are of a particular interest. They are capable of performing a number of important functions and they have been extensively used in ICs operating at microwaves. Figure

1-10 exemplifies such circuits [GHA06-2]. It consists in a power amplifier designed to operate at 5 GHz containing one transformer at the input and another at the output. Their main role in the PA is to act as baluns, i.e., to convert signals from a single-ended form to a differential or balanced one and vice versa. In addition to this function, especially at the input, they exploit their impedance transforming properties in order to take part in the PA's matching networks.

Analogously, [GAN06] includes transformers as baluns and part of the matching networks of both a PA and an LNA operating at 2.4 GHz (Figure 1-11). Furthermore, the design takes advantage of the DC decoupling property of the transformers to supply bias voltages through a center-tap in one of the windings.

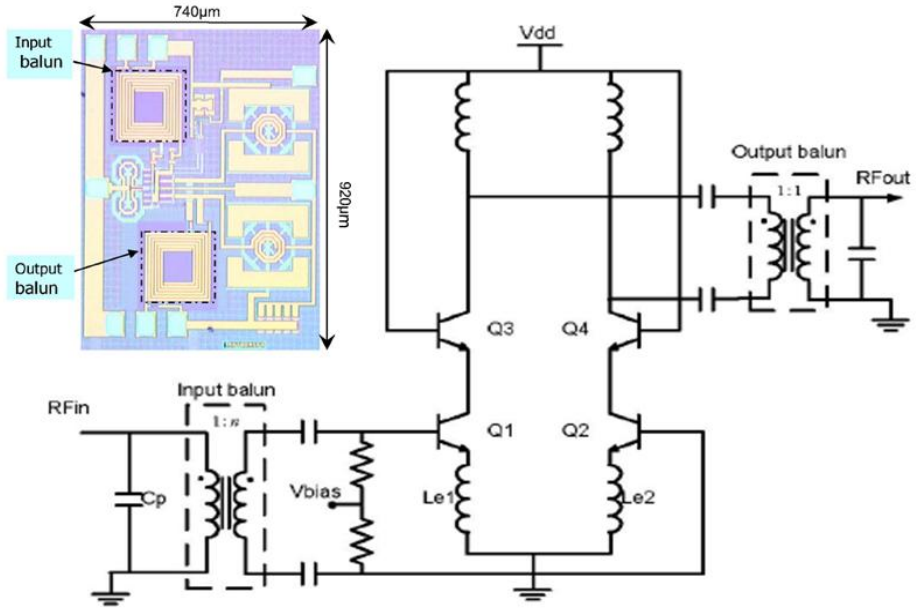


Figure 1-10 5-GHz LNA in [GHA06-2].

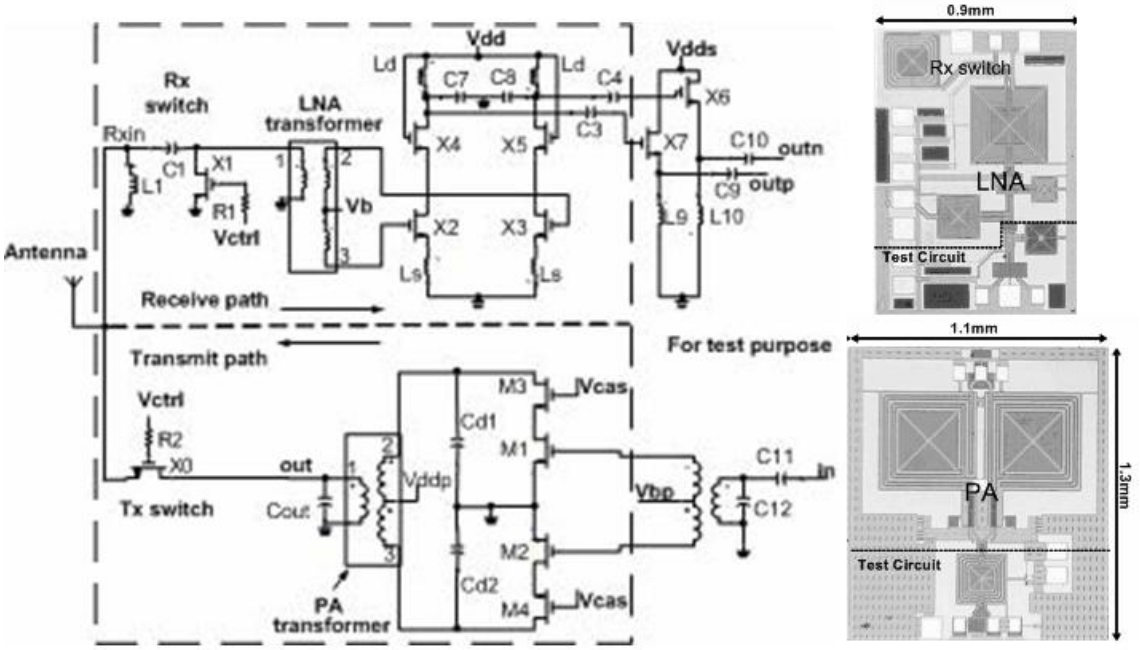


Figure 1-11 2.4-GHz LNA and PA [GAN06].

Another task which can be successfully performed by integrated transformers is power combining. This use can be illustrated by the 2.5-GHz PA of Figure 1-12 [KIM11], where, in addition to the transformer-based input balun, a transformer is introduced in the output in order to recombine power from a number of parallel amplifying cells. This kind of implementation favors good linearity measures while maintaining a high output power, especially as supply voltages scale.

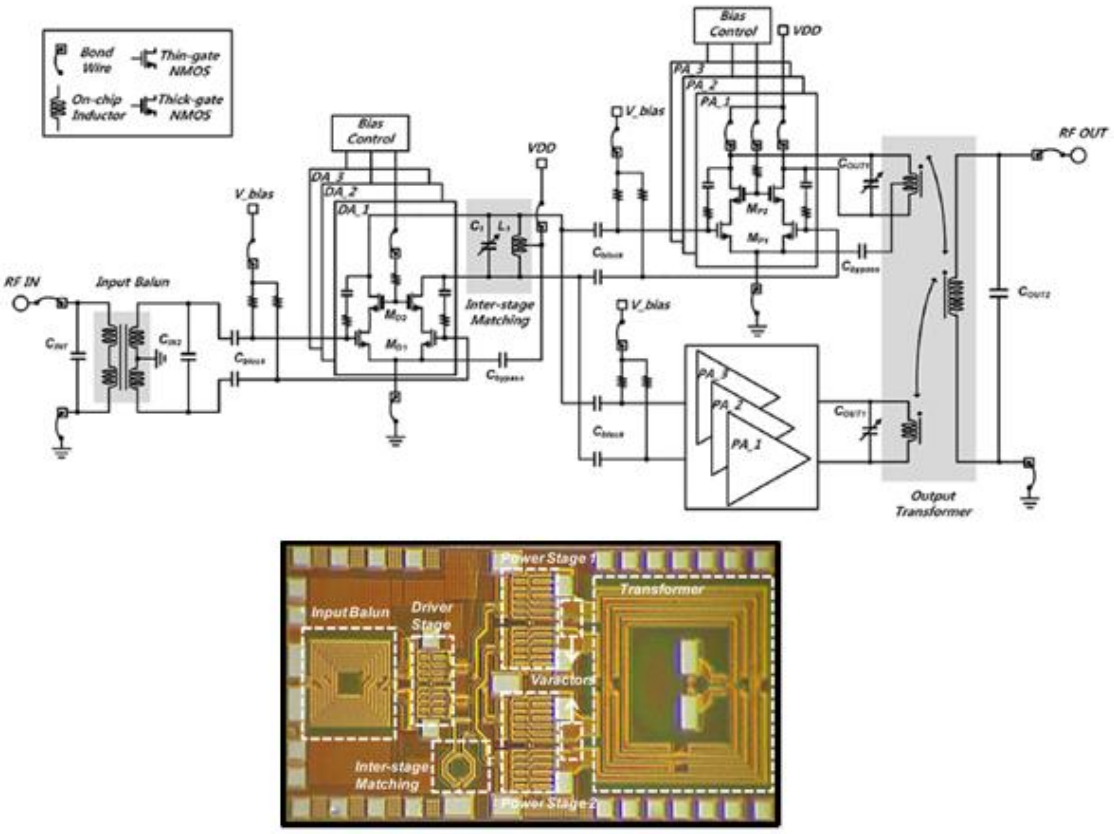


Figure 1-12 2.5-GHz PA in [KIM11].

Alternative uses of RF transformers have been reported in [KIH08] and [NG07]. In [KIH08] (Figure 1-13) a 4.7-GHz LNA combines the degeneration inductor with an internal inductor in its folded-cascode topology to constitute a transformer. The magnetic coupling between these elements introduces a feedback path within the circuit and allows a significant area gain in comparison to the case of two uncoupled inductors. In [NG07] a quadrature VCO operating at 17 GHz is presented. This circuit, depicted in Figure 1-14, contains two elementary VCOs, which are cross-connected through transformer coupling so that primaries at the drain of a VCO are coupled to secondaries at the source of the other VCO. Additionally, the primary of each transformer is used to resonate with the capacitance of the oscillators.

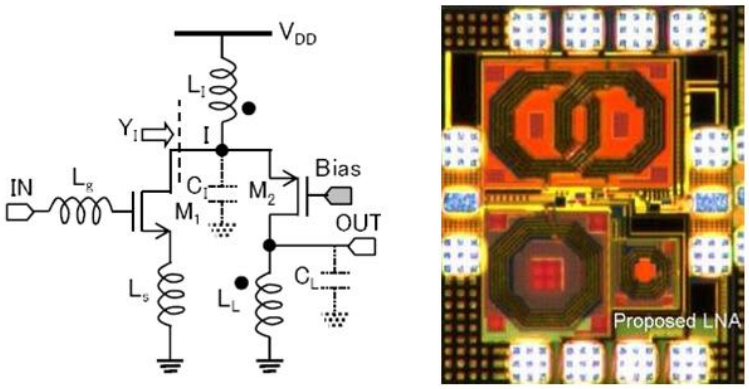


Figure 1-13 4.7-GHz LNA in [KIH08].

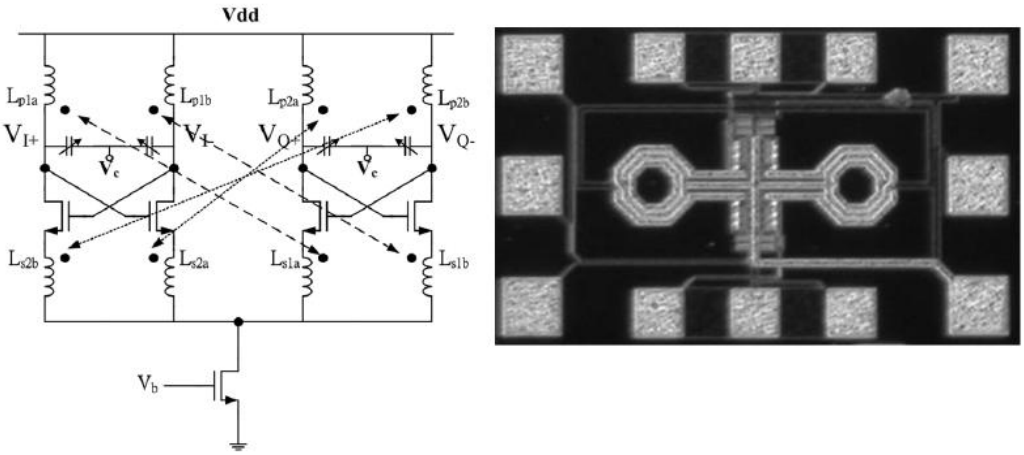


Figure 1-14 17-GHz VCO in [NG07].

Despite the different constraints that mm-wave design presents, transformers have also been shown to be very useful at these frequencies. If correctly designed, they allow an expressive area reduction comparing to purely transmission line-based circuits, while being able to provide broadband matching, and efficient power combining and balun conversion.

As in microwaves, mm-wave transformers are frequently integrated into power amplifiers. Figure 1-15 — Figure 1-18 exemplify such PAs. In [PFE05], for instance, a transformer is incorporated into the output matching network of the 60-GHz amplifier, whereas in [CHA10], four transformers are used within the different matching networks of the PA. Moreover, two of the transformers provide inter-stage coupling, and the transformers at the input and the output operate as baluns. Similarly, [CHE11] also uses transformers to perform power splitting and combining within the circuit along with their matching and balun functions. And in [DEM10], transformer-based baluns are employed as well, but targeting higher operating frequency, i.e., 79 GHz.

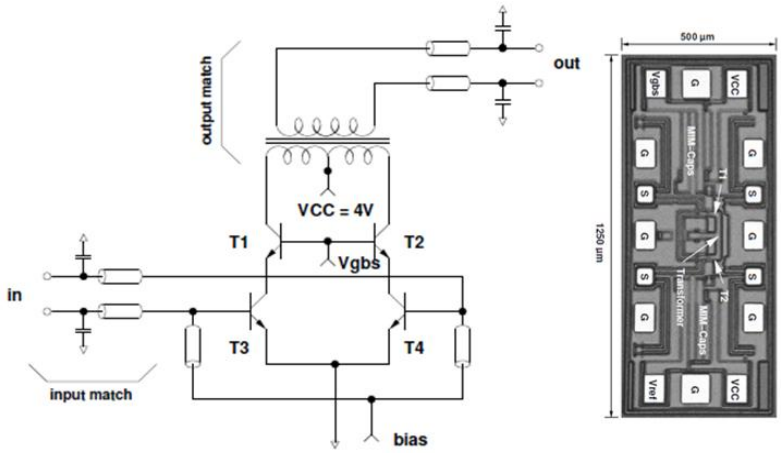


Figure 1-15 60-GHz PA in [PFE05].

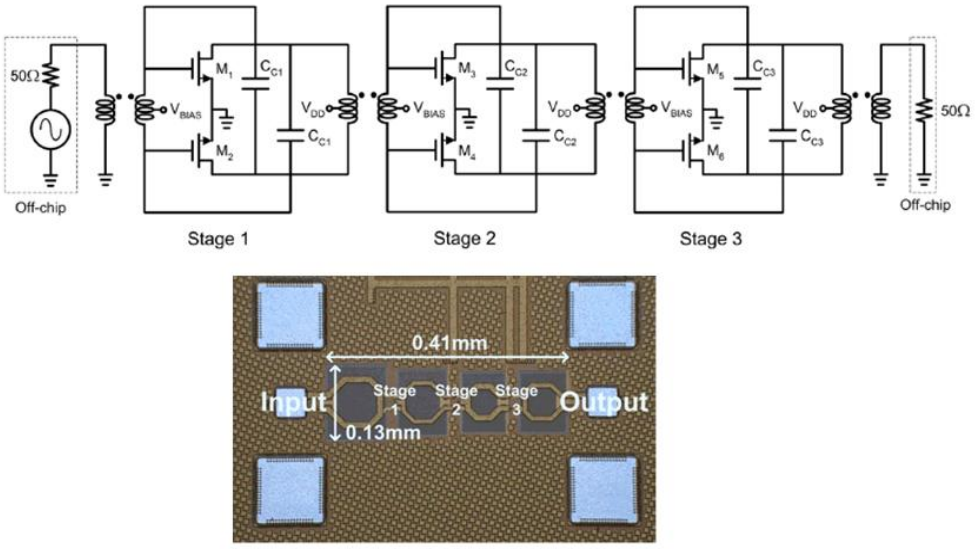


Figure 1-16 60-GHz PA in [CHA10].

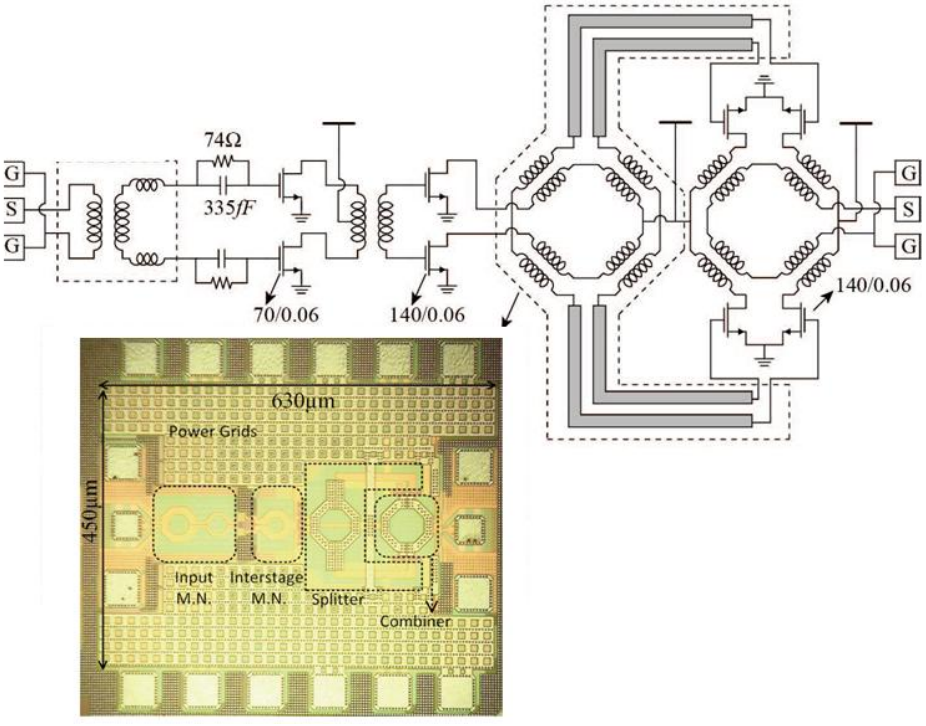


Figure 1-17 60-GHz PA in [CHE11].

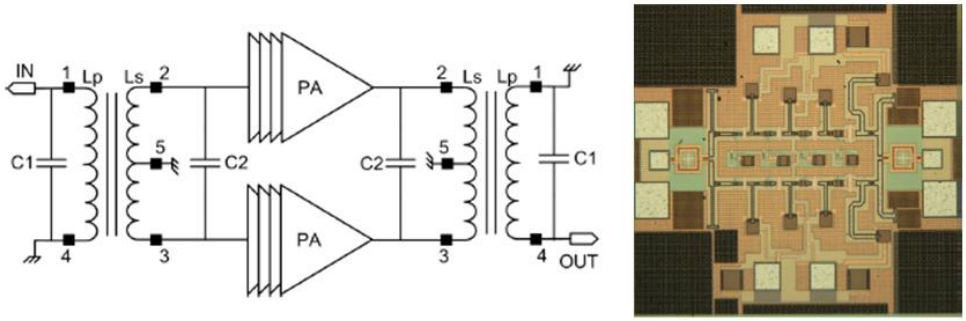


Figure 1-18 79-GHz PA in [DEM10].

In addition to their use in power amplifiers, mm-wave transformers have been largely reported within receivers as well as matching and balun elements. Two different designs are presented here to illustrate this use: a 60-GHz [ALL06] (Figure 1-19) and a 95-GHz receiver [LAS08] (Figure 1-20). Finally, different mm-wave blocks employing transformers in their structures have additionally been presented. It is namely the case of the frequency divider in [DIC06], which uses a balun operating up to 70 GHz (Figure 1-21) and the ASK modulator in [BRI10], which also employs transformers for matching (Figure 1-22).

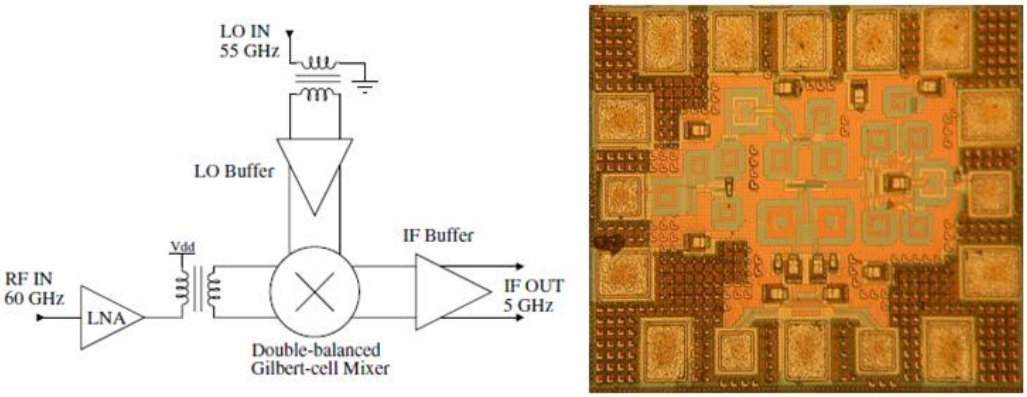


Figure 1-19 60-GHz receiver in [ALL06].

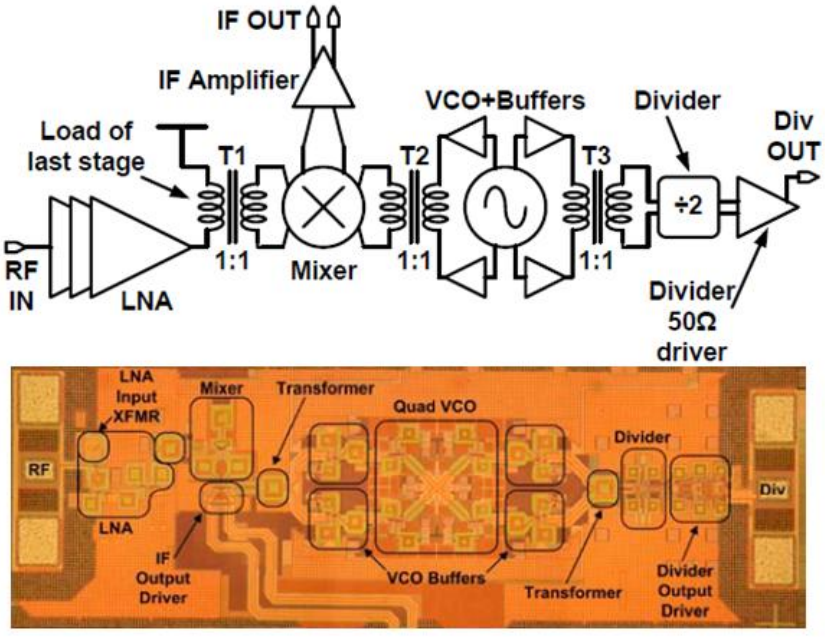


Figure 1-20 95-GHz receiver in [LAS08].

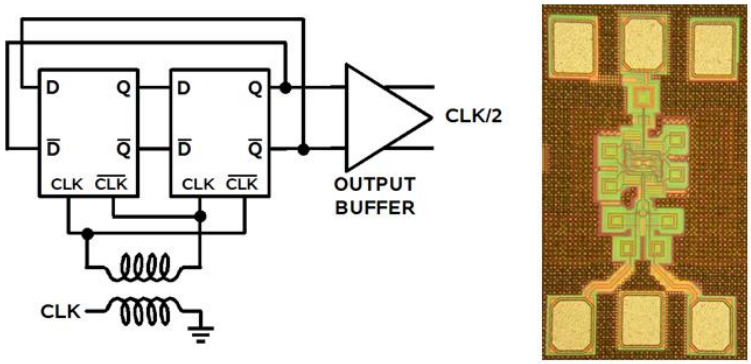


Figure 1-21 Millimeter-wave frequency-divider in [DIC06].

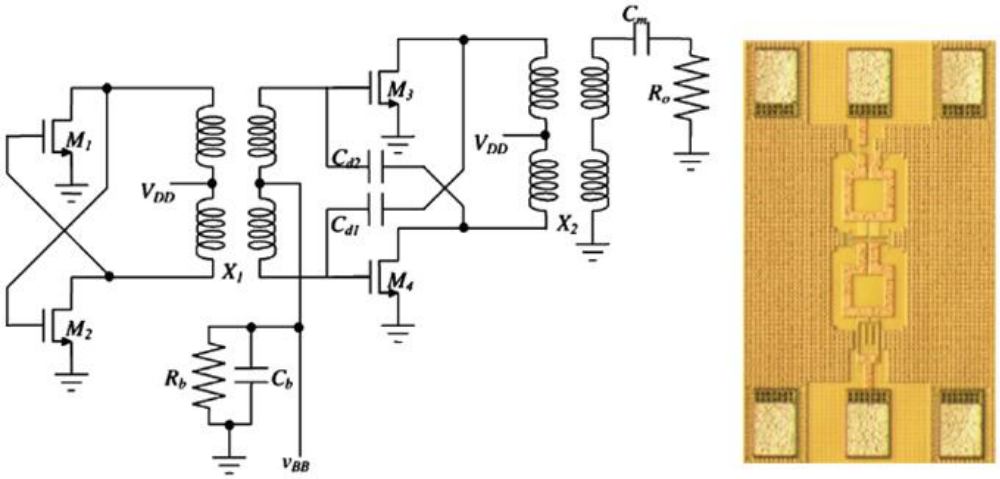


Figure 1-22 60-GHz ASK modulator in [BRI10].

2.4 Thesis contribution

In view of the presented background, this thesis proposes to carry out a comprehensive investigation regarding mm-wave integrated transformers. Due to the interest that the use of transformers in mm-wave ICs draws, it is crucial to examine the structures which are best adapted for the targeted operations. This thesis is therefore intended to provide an in-depth study on transformer design, handling the constraints of achieving sufficiently high operating frequencies while minimizing losses and procuring suitable transformation ratios.

Once the best performing topologies defined, the goal of this thesis is to establish an equivalent electric model for mm-wave transformers. Unlike most currently published models, which are frequently narrowband, limited to a single technology or a mere result of individual curve-fitting, the work in this thesis is intended to be predictive, providing reliable results over a wide frequency band. Additionally, the proposed model is intended to be scalable in terms of technologies as well as geometrical parameters of the transformers.

Finally, the ultimate goal of this thesis is to apply the performed investigations concerning transformer design and modeling to the development of complete mm-wave building blocks.

3 Conclusion

This chapter presented the motivation to the study of mm-wave integrated transformers. Two main themes were treated: the emerging mm-wave applications and the use of transformers within radiofrequency and mm-wave integrated circuits. Specifically, the relevant regulations, standards and applications for wireless communications in the range between 50 and 100 GHz were discussed.

One of the most important applications concerns the WLANs and WPANs operating around 60 GHz. They take advantage of an unlicensed band covering up to 9 GHz and allowing multi-gigabit data throughputs, which can be higher than 25 Gbit/s. The main related standards and specifications are ECMA 387, IEEE 802.15.3c, WirelessHD, WiGig, and IEEE 802.11ad. These standards focus on a mass market and, at the time of writing, some of them already present complying commercial products.

Another major mm-wave application is automotive radar. It focuses on improving driving security by the addition of short range and long range radar elements. While short range radar development has mostly taken place at frequencies immediately inferior to mm-waves (especially at 24 GHz), the tendency, leaded by Europe, is to shift those radars to 79 GHz in the following years. Long range radar systems, on the other hand, have been consistently implemented at 77 GHz.

The third presented field of application is related to mm-wave imaging. This use of mm-waves has been increasingly adopted, particularly for medical and security purposes, including concealed weapons detection. The most favored frequency for mm-wave imaging has been 94 GHz.

Concerning the integration of transformers, a review of the technological families used in radiofrequency circuits was presented. Especial attention is given to the evolution of silicon-based technologies, which currently allow the deployment of CMOS and BiCMOS for mm-wave ICs.

The last part of this chapter was devoted to a bibliographic review on the use of integrated transformers at RF and mm-wave ICs. Their most notable uses are to constitute matching networks, to operate as baluns or within power combiners, but they can also be employed as part of resonating and feedback circuits. Examples were introduced of transformers integrated within, among other blocks, PAs, LNAs, VCOs, and mixers.

The conjugation of these facts highlights the interest of an in-depth investigation on silicon integrated transformers for mm-wave integrated circuits.

Chapter 2 : Design and Characterization of mm-wave Transformers

1 TRANSFORMER CHARACTERIZATION 28
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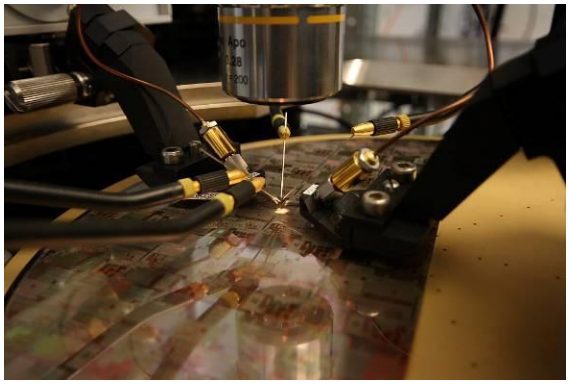
This chapter focuses on the design of integrated transformers in mm-waves, as well as on their characterization. Firstly, the employed measurement setup and the most relevant measurement issues for on-chip transformers are discussed. Secondly, the physical phenomena leading to non-ideal operation are investigated along with a description of the employed integration technologies. A comprehensive study on the topology of transformers is then carried out regarding the layout of individual coils, their relative position, geometric dimensions, and the interest of using substrate shields in order to enhance winding quality-factors. Finally, a topology allowing to obtain high transformation ratios is proposed and analyzed.

1 Transformer Characterization

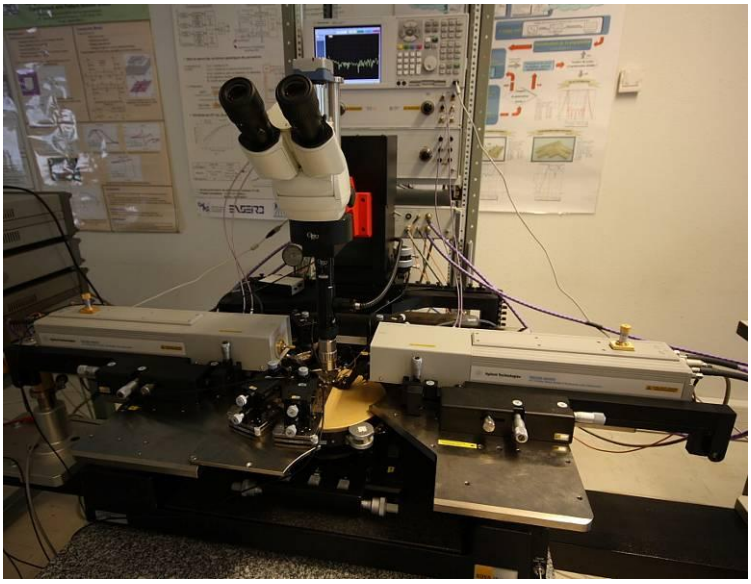
1.1 Characterization platform

The characterization of any integrated device must cope with a number of practical limitations. Especially as the frequencies of interest rise attaining the mm-wave band, the implementation of a comprehensive test bench becomes considerably complex and costly.

The IMS Laboratory disposes of the NANOCOM platform to perform RF and mm-wave measurements. In addition to hardware allowing source-pull, load-pull, multi-harmonics, spectral analysis and noise measurements, the platform contains a test bench especially set for S-parameter measurement up to 110 GHz. It is composed of an *Agilent E8361* vector network analyzer associated to mm-wave test heads and the corresponding Ground-Signal-Ground (GSG) testing probes (Figure 2-1). This configuration, nonetheless, is limited to the measurement of 2-port devices.



(a)



(b)

Figure 2-1 Millimeter-wave characterization platform.

1.2 De-embedding

It is not possible to perfectly reproduce in a test chip the structure of a silicon device as it will be inserted within a circuit. That is due to the need of testing pads and feed lines connecting them to the device under test (DUT). Especially at high frequencies such as mm-waves, as the dimensions of the devices tend to shrink, these parasitics exert a substantial influence on the global response. For this reason, it is vital that a correction method be applied.

Several techniques have been proposed to de-embed such parasitics from a measurement. They may be classified into two classes: those based in a lumped equivalent model and the cascade techniques [ISS07]. Cascade techniques consider the raw device as a series of cascaded two-port networks and do not make any assumption regarding the nature of the parasitics [CHE01, WEN95]. They present however a limitation in what concerns an eventual third port usually including parasitics from ground connections (Z_{S3} in Figure 2-2) and they often include relatively long transmission-lines, which can account on higher area occupation. De-embedding based on lumped-element equivalent models, on the other hand, presumes prior knowledge of parasitics distribution. The simplest technique consists in subtracting from the raw data the parallel admittance, which is mostly due to the probing pads capacitances, by using an *open* structure. As this method does not account for the series components of the parasitics, which become more relevant as feed lines are electrically longer and therefore more resistive and inductive, the *open-short* method, which includes an additional *short* dummy has been developed [KOO91]. De-embedding techniques employing a higher number of dummy structures have been reported as well. In [TIE05], for instance, a 3-step correction using 3 dummy structures is presented, while [CHO91], [KOL00], and [VAN01] use 4 de-embedding elements, and the technique proposed in [BIO07] employs a 5^{th} dummy structure.

While it is understood that the use of additional dummy structures, when properly selected and designed, will be reflected in an improved de-embedding accuracy, it will inexorably

impact the area occupation of the characterization dies. Hence, it is necessary that the choice of a de-embedding method be made so that the best trade-off between precision and silicon area can be attained. For this reason, the *open-short* method was adopted in the measurement of transformers in this work. It assumes the general parasitic distribution of Figure 2-2 and is calculated according to equations (2-1) – (2-3).

$$Y' = Y_{Raw} - Y_{Open} \tag{2-1}$$

$$Y'_{Short} = Y_{Short} - Y_{Open} \tag{2-2}$$

$$Z_{DUT} = Z' - Z_{Short} \tag{2-3}$$

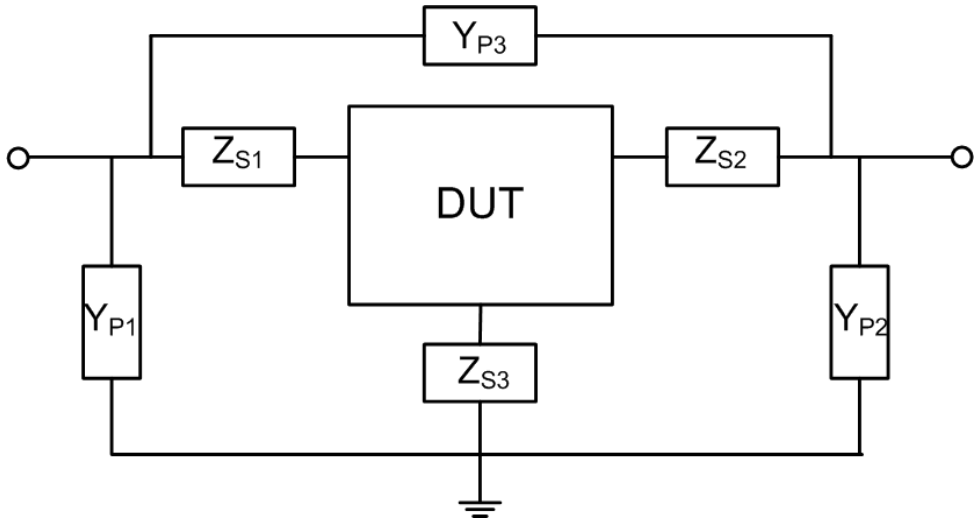
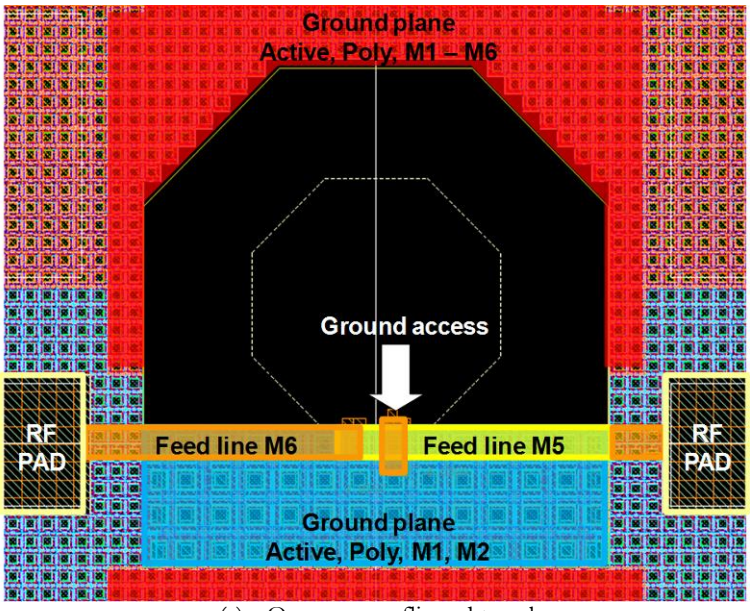


Figure 2-2 Parasitics distribution for open-short de-embedding.

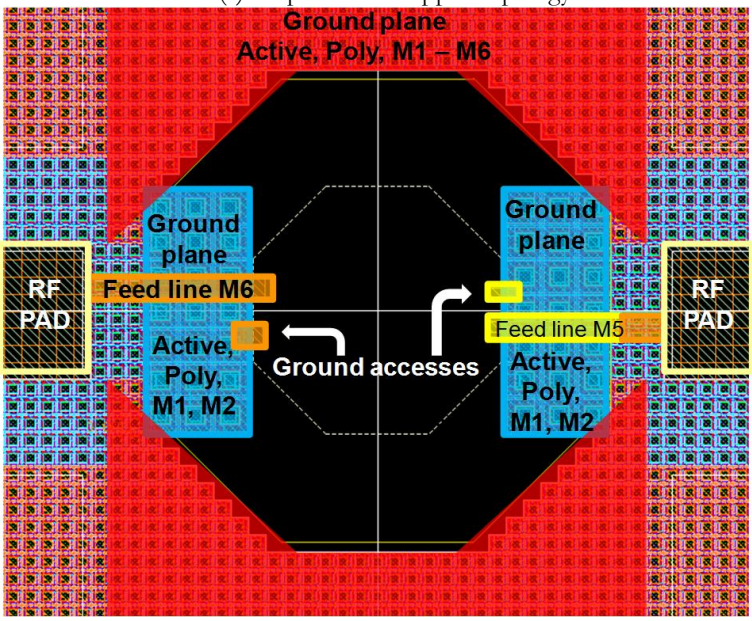
Once the de-embedding technique defined, the design of the test fixtures must be accomplished in a fashion which allows minimizing the number of sets of open-short dummies. Indeed, as test chips were designed, for each technology, only two pairs of dummy structures were necessary. They accounted for the different topologies regarding the relative position of feed lines, as discussed in subsection 4.3. Figure 2-3 illustrates the design of these dummy structures in a 130-nm BiCMOS technology.

1.3 Parameter extraction

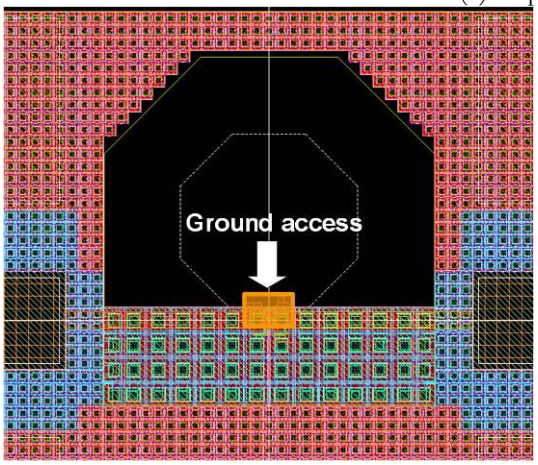
Measurement as well as electromagnetic simulation of integrated transformers supplies a matrix of scattering parameters swept over frequency as their output. These parameters provide useful information regarding reflection and transmission especially in the case of 50-Ω loads at both ends of the component. There are nonetheless, a number of other parameters which allow to gain deeper insight into the transformers operation.



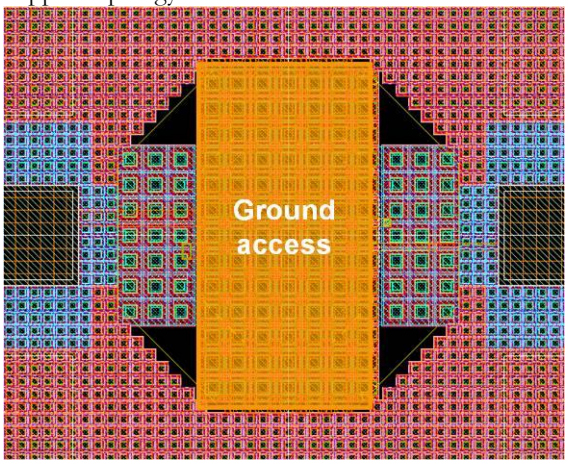
(a) Open – non-flipped topology.



(b) Open – flipped topology.



(c) Short – non-flipped topology.



(d) Short – flipped topology.

Figure 2-3 Dummy structures in a 130-nm BiCMOS test chip.

For transformers in a 2-port configuration (Figure 2-4), as it was the case in measurements, it is important to evaluate the equivalent primary and secondary inductances L_P and L_S. Those are extracted from the impedance parameters following equations (2-4) and (2-5), and the inductance ratio n_L is defined as in (2-6). Analogously, the mutual inductance between windings is obtained through (2-7). A typical form to represent the strength of the coupling is the coupling coefficient k. Comprised between 0 (null coupling) and 1 (perfect coupling), its value at low frequencies indicates the amount of the magnetic flux from one coil which is not captured by the other, and therefore is lost. It should be noted that these extracted values will not be constant over frequency. The complete equivalent electric model of the transformer contains a number of other components, especially capacitors, which are responsible for the resonating nature of the extracted self and mutual inductances. This model is thoroughly described in Chapter 3.

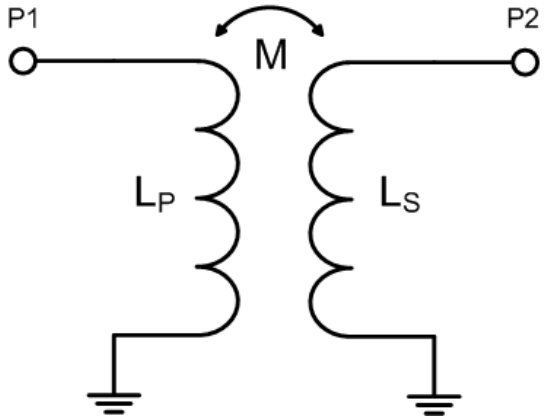


Figure 2-4 Transformer in 2-port configuration.

$$L_P = \frac{\mathrm{Im}(Z_{11})}{\omega} \tag{2-4}$$

$$L_S = \frac{\mathrm{Im}(Z_{22})}{\omega} \tag{2-5}$$

$$n_L = \frac{L_S}{L_P} \tag{2-6}$$

$$M = \frac{\mathrm{Im}(Z_{21})}{\omega} \tag{2-7}$$

$$k = \frac{M}{\sqrt{L_P \cdot L_S}} \tag{2-8}$$

There are a number of different definitions usually employed to evaluate the quality-factor of inductors. Its fundamental definition relates to the ratio between stored and dissipated energies by the passive component in an oscillation cycle. An integrated inductor stores magnetic energy by nature, but also presents parasitic capacitances which will be responsible for some electric energy storage. Therefore, since an inductive behavior is sought in an integrated transformer, the stored energy which is considered is the difference between the peak magnetic and electric energies, i.e. the net magnetic energy [YUE98]. It will therefore be computed as the

ratio between imaginary and real parts of the corresponding impedances, as equations (2-9) and (2-10) display.

$$Q_P = \frac{\mathrm{Im}(Z_{11})}{\mathrm{Re}(Z_{11})} \tag{2-9}$$

$$Q_S = \frac{\mathrm{Im}(Z_{22})}{\mathrm{Re}(Z_{22})} \tag{2-10}$$

The study on transformer design conducted in this chapter is not focused in a specific application, but is rather intended to be sufficiently general. Therefore, there is no prior information regarding the impedances that would be presented to the transformer terminals. Hence, in order to calculate the total losses that the device can introduce, the evaluation of the transmission loss for 50 Ω or any other arbitrary fixed load is not the most suitable metric. Instead, we opt for computing the minimum insertion loss IL_m of each device, i.e., the losses it introduces in the case where both ports are perfectly matched. Its value is calculated by (2-11) and (2-12).

$$\mathrm{IL_m} = \frac{1}{1 + 2 \cdot \left(x - \sqrt{x^2 + x}\right)} \tag{2-11}$$

$$x = \frac{\mathrm{Re}(Z_{11}) \cdot \mathrm{Re}(Z_{22}) - [\mathrm{Re}(Z_{12})]^2}{[\mathrm{Im}(Z_{12})]^2 + [\mathrm{Re}(Z_{12})]^2} \tag{2-12}$$

2 Loss Mechanisms

A transformer implemented within an integrated circuit environment suffers from a number of sources of loss, which make their behavior deviate from the ideal. In this section, some of the most significant loss mechanisms intervening for mm-wave transformers in a silicon-based technology are discussed.

The primary and secondary windings are realized by metallic conductors. As their intrinsic resistivity (ρ) is not null, they constitute a source of ohmic losses. In a low-frequency context, this resistance is assumed constant, depending only on the material constitution and the conductors dimensions. Nevertheless, as frequency rises, the ohmic losses are observed to rise as well. One phenomenon which largely contributes to this behavior is the *skin effect*. At those frequencies, field distribution acts in a fashion which concentrates most of current on the edges of the metal. This reduces the effective section area of the conductor and represents a significant increase of the corresponding resistance proportionally to the square root of the frequency. A useful metric for the skin effect is the associated skin depth δ. It represents the distance from the edge at which the current is reduced by a factor e^{-1} (nearly 37%), as shown in Figure 2-5. Evaluating (2-13), where μ represents the magnetic permeability of the material and ω the angular frequency, it is

observed that the skin depth of copper, for instance, is as low as 0.3 μm at 60 GHz, and 0.2 μm at 80 GHz.

$$\delta = \sqrt{\frac{2 \cdot \rho}{\mu \cdot \omega}} \tag{2-13}$$

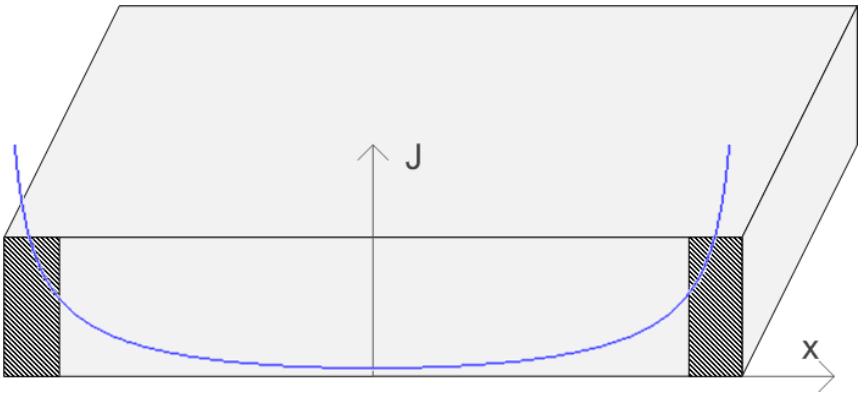


Figure 2-5 Skin effect on a rectangular conductor.

As aforementioned, imperfect coupling between coils is a source of loss as well. Due to the permeability of the dielectric between primary and secondary, a portion of the magnetic flux from the primary is leaked and might intercept neighboring conductors. Thus, this fraction of the flux does not contribute to the power transfer between windings. Moreover, the impact of the magnetic flux from adjacent conductor segments should be considered. Whereas orthogonal segments do not affect each other, mutual coupling is observed for parallel conductors. If the current on these segments flow in opposite directions, part of the magnetic flux will be cancelled in function of their proximity. Such coupling decreases the total inductance of the coil and should be taken into account when designing an integrated transformer.

Since on silicon-based technologies, unlike traditional III-V or SOI processes, substrate presents a considerably conductive nature, one of the major loss mechanisms for a transformer integrated on such technologies is substrate coupling. This coupling takes place through two main phenomena: electrically-induced and magnetically-induced losses. Electrically-induced loss stem from the capacitive coupling between conductors and the substrate. This originates displacement currents flowing through the lossy dielectrics and into the substrate. Magnetically-induced losses, on the other hand, are expressed in terms of eddy currents flowing in the substrate, arising due to the penetration of the magnetic field [GHA06-1]. Figure 2-6 illustrates those induced currents.

Additionally, for components whose dimensions are large in respect to the free-space wavelength of the signal, some of the power is lost through radiation. For most of the usual topologies adopted for integrated transformers, however, such losses may be neglected [NIK07].

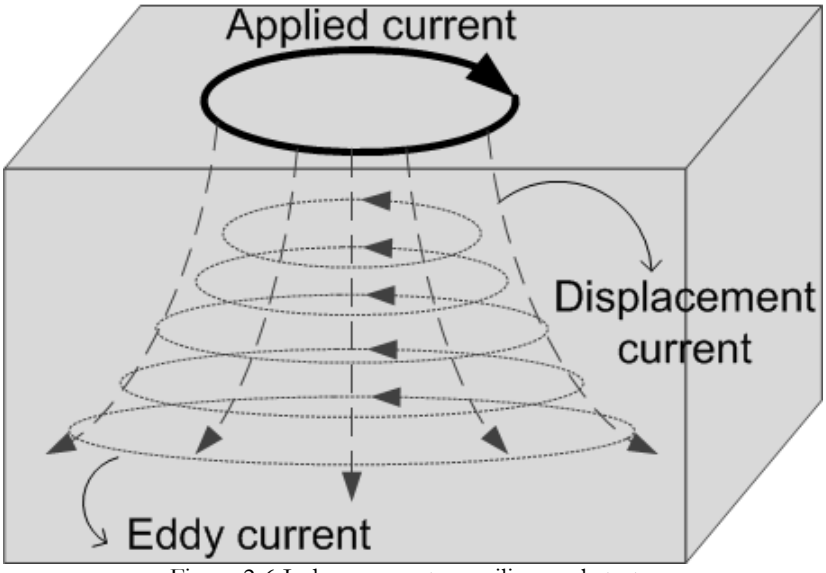
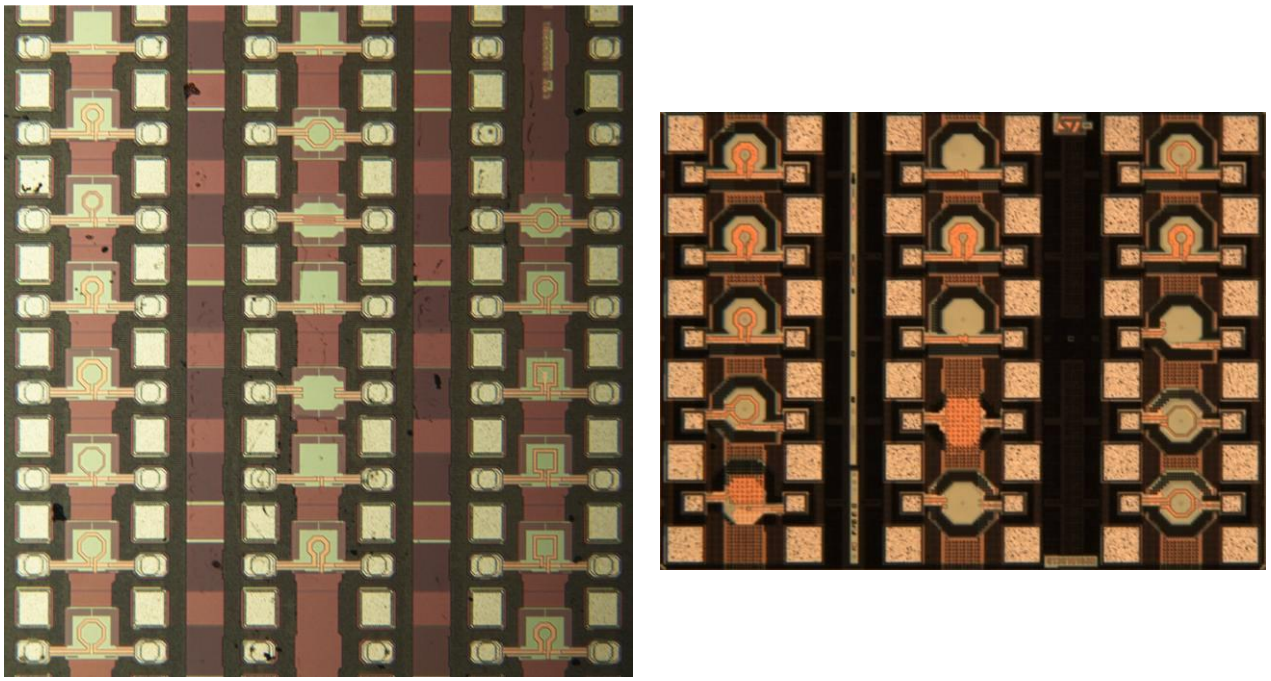


Figure 2-6 Induce currents on silicon substrate.

3 Technologies

This study on transformers design is intended to address a number of different applications. As a consequence, the conclusions to be drawn should be valid throughout different integration technologies. In the context of this project, two silicon processes were mainly targeted, both from STMicroelectronics: a 65-nm bulk CMOS and a 130-nm SiGe BiCMOS, which is optimized for mm-wave operation [AVE09]. Figure 2-7 depicts micrographs of test chips realized in these two technologies.



(a) (b)

Figure 2-7 Transformer test chips in (a) 65-nm CMOS, and (b) 130-nm BiCMOS technologies.

The properties of the silicon substrate for both technologies are quite similar. They present a moderate resistivity, lying in the region between 10 and 20 Ω.cm. The thickness of the substrate within a die is 250 μm for the CMOS technology, and 375 μm for the BiCMOS.

Concerning the back-end-of-line (BEOL), the constitution of the metal stack is of paramount importance in the design of integrated transformers. These metals are deposited through a damascene process within low-permittivity dielectrics. The 65-nm CMOS technology may present a number of different process options in regard to the metals. In this work, the option which was adopted counts a total of 7 copper layers, including two thicker metals on the top. The SiGe technology, on the other hand, presents 6 copper layers in its BEOL and also includes two thicker layers on the top of the stack. Despite presenting fewer metal levels, the metals in the BiCMOS technology are considerably thicker and more distant from the substrate than its CMOS counterparts. Such characteristics tend to be advantageous, as both resistive losses associated to the conductors and capacitive losses between them and the substrate should be minimized with this configuration. The vertical distance between the thick metals, however, is greater for the BiCMOS. This feature is expected to weaken the magnetic coupling between them. Figure 2-8 illustrates the profile of both back-ends. It should also be noted that both technologies contain an aluminum capping level above the highest copper level. These layers, however, are less suited to constitute transformer windings, due to aluminum's poorer resistivity and current handling capability [PAS09], [VEE08].

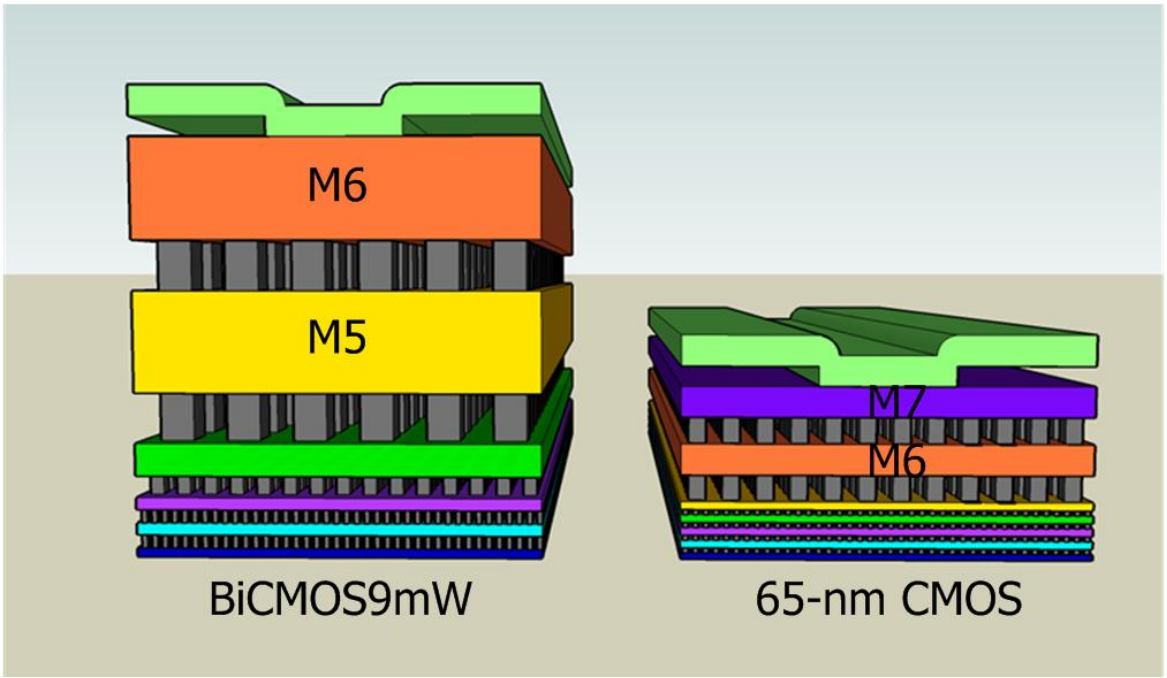


Figure 2-8 Back-end profiles of the 65-nm CMOS and BiCMOS9mW technologies.

Another important distinction regarding the targeted technologies concerns their design rules for the thick metals. Due to the stringent metal density rules adopted for the 65-nm design, only trace widths comprised between 4 and 12 μm are allowed in this process to constitute inductors or transformers. As those constraints are less severe for the 130-nm process, traces as wide as 30 μm can be implemented. The lower limit is unchanged and kept at 4 μm.

4 Transformer Topology

The layout of integrated transformers can be drawn in a multitude of manners. The individual design of the coils as well as the relative position allowing mutual coupling between them must be determined in order to ensure a proper operation at mm-waves.

Concerning the individual windings, symmetry has been favored in the layout. Such design, as exemplified in Figure 2-9, is symmetric regarding the two ports of the inductor, which enables an easily identifiable central point on the coil. The presence of such points, simultaneously representing an inductive, capacitive and resistive center, is of a particular interest especially when transformers are designed to operate as baluns.

In this section, we solely treat transformers with single-turn windings. This approach allows to obtain high operation frequencies and to minimize losses in the coils. It, nevertheless, limits the attainable inductances for a given surface. Transformers with more turns are discussed in Section 6.

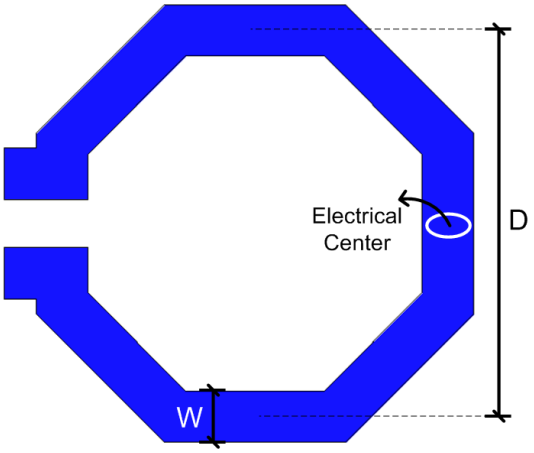


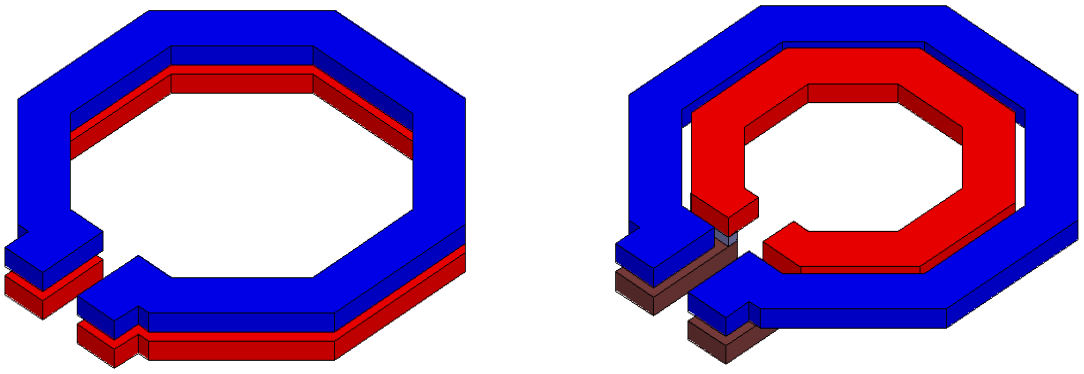
Figure 2-9 Symmetric layout of a winding with average diameter D and trace width W.

4.1 Coupling direction

In what concerns the direction at which magnetic coupling takes place between windings, two fundamental possibilities are presented: vertical and lateral coupling. Figure 2-10a illustrates a planar topology for which primary and secondary are implemented in the same metal level. The advantage of such construction would be for applications where symmetry in terms of parasitics is sought, as both windings are equally exposed to the substrate. Moreover, such topology might also be advantageous for technologies containing only one thick metal layer. Stacked transformers, on the other hand, realize each of the windings on a different metal (Figure 2-10b). This topology is expected to maximize the magnetic coupling while occupying a reduced area.

In order to compare those topologies, 3-D EM simulations were carried out. To perform this comparison, we considered the technology which would provide the most favorable case for the planar configuration in terms of mutual coupling. BiCMOS9mW presents considerably thicker metals, which maximizes the lateral area where primary faces are directly exposed to the

secondary. Additionally, this technology provides a greater distance between the two thickest metals, which is detrimental to vertical coupling.



(a) (b)

Figure 2-10 (a) Stacked, and (b) planar transformer topologies.

The stacked structure was designed so that the two single-turn windings present precisely the same geometric dimensions. It is nonetheless not possible to do the same with the planar configuration. The adopted criterion for the comparison was hence to design a planar transformer occupying the same total chip area as its stacked counterpart. This translates into the exact same primary for the transformers, represented by the top winding for the stacked or the outer winding for the planar. The secondary of the planar transformer was then designed with a smaller diameter, and lateral spacing between windings was set to the minimum authorized by the design rules.

The obtained results in terms of inductances are shown in Figure 2-11. A higher resonant frequency is observed for the planar topology. This is mostly due to the lower total inductance derived from the smaller secondary. The total capacitance of the structure, however, is estimated higher for the planar topology, as the incremented surface regarding the substrate is proportionally more substantial than the reduced distance between conductors and substrate.

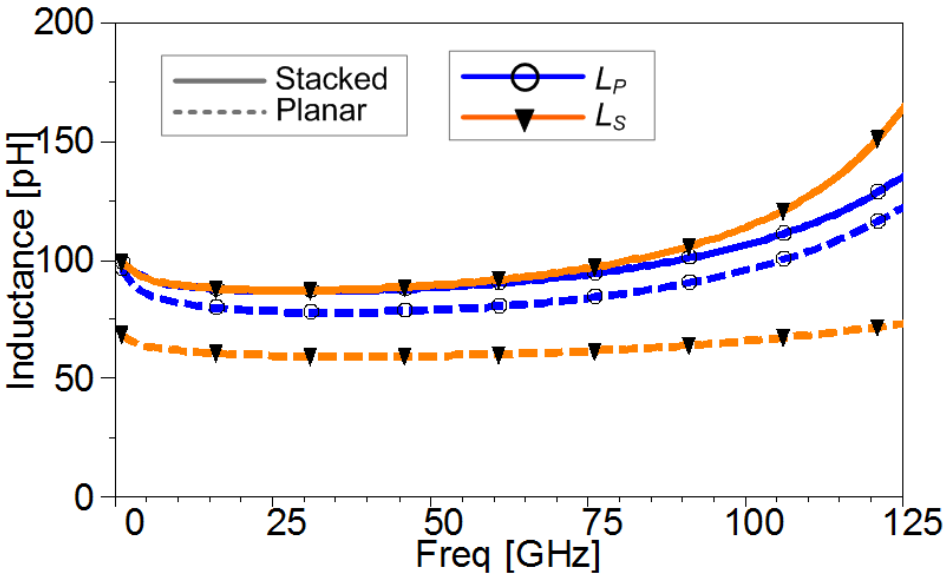


Figure 2-11 Simulated inductances of stacked and planar transformers.

It is observed as well that the stacked configuration provides a distinctively superior primary quality-factor, as depicted in Figure 2-12. As the winding layout is identical, the reason of such disparity is the secondary acting as a shield between primary and substrate and hence mitigating substrate losses in the stacked topology. The secondary quality-factor, on the other hand, is improved in the planar case, as the winding is implemented in a higher metal level, thus presenting a weaker substrate coupling.

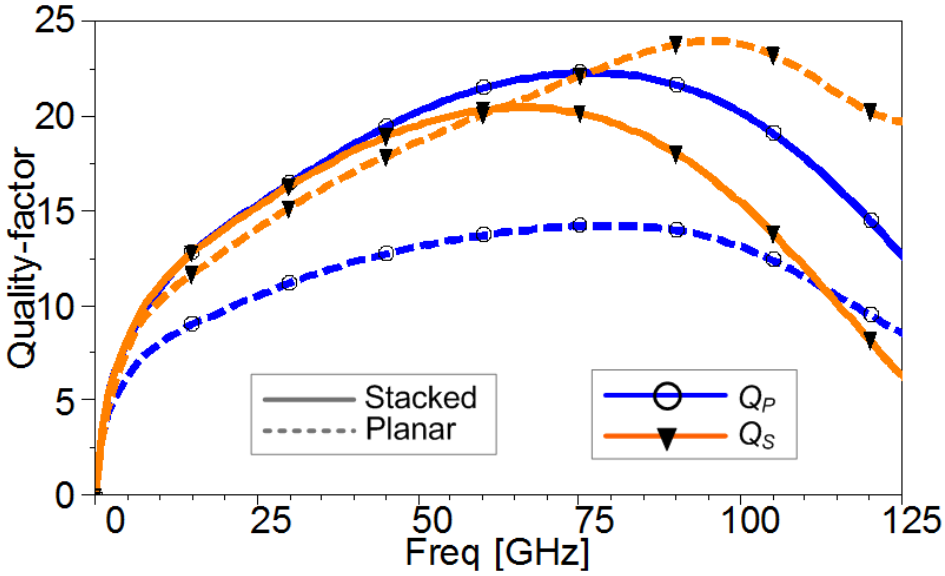


Figure 2-12 Simulated quality-factors of stacked and planar transformers.

Coupling coefficient and minimum insertion loss are presented in Figure 2-13. The magnetic coupling, as expected, yields a clear advantage for the stacked topology. Results show a 0.75 coupling coefficient for the stacked transformer while its value remains inferior to 0.6 for the planar configuration. Since in this particular case the distances separating primary and secondary were roughly the same, this highlights how magnetic coupling is closely related to the surfaces where the two conductors are in direct regard, as traces were 8-µm wide, and metals are 3-µm thick.

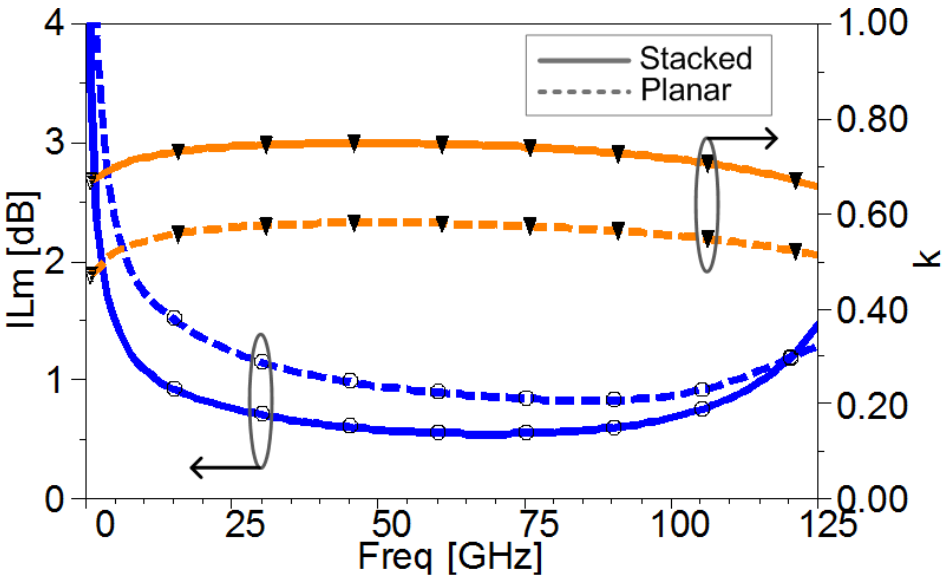
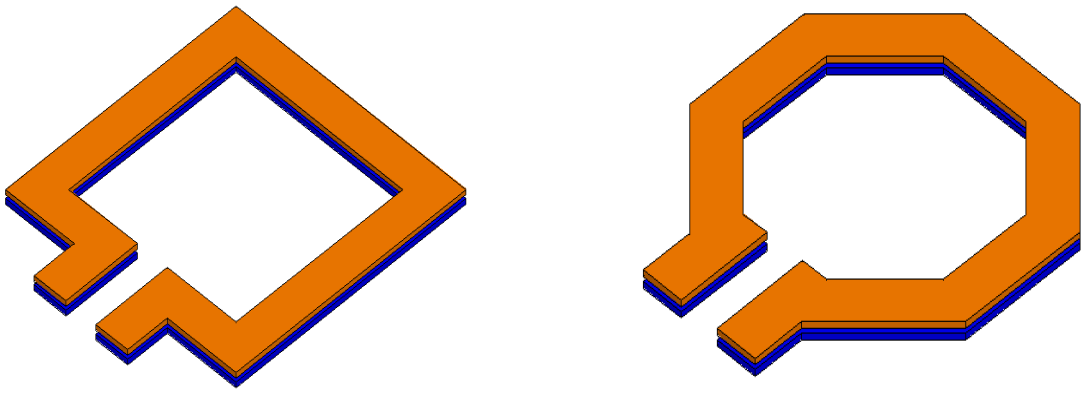


Figure 2-13 Simulated coupling coefficient and minimum insertion loss of stacked and planar transformers.

The minimum insertion loss takes simultaneously into account individual quality-factors and magnetic coupling considerations. As a consequence, the obtained results show a clearly superior performance for the stacked transformer over the entire considered frequency range. At 60 GHz, for instance, a 0.9 dB loss for the planar and a 0.55 dB loss for the stacked transformer are observed. It demonstrates how the attained improvement in the planar secondary quality-factor is outweighed by the degraded primary quality-factor and coupling coefficient. For this reason, the stacked topology is adopted hereafter in this work.

4.2 Winding shape

The shape of the windings is another important distinction regarding transformer topologies. Square, polygonal and circular spirals have already been reported to constitute inductors and transformers. Nevertheless, circular or polygonal topologies cannot always be employed. There are CAD and technological limitations which may restrain the angles which can be realized. For the processes adopted in this study, angles are limited to multiples of 45 degrees and comparison was hence restricted to a square (Figure 2-14a) and an octagonal transformer (Figure 2-14b).



(a) (b)

Figure 2-14 (a) Square and (b) octagonal topologies.

The measurement results for those two 65-nm CMOS transformers are shown in Figure 2-15 — Figure 2-17. The two components present the same diameter and same trace width. It is observed that for the same diameter, square coils present a higher inductance value. This difference is due to the greater total length the square device presents. We also note that octagonal transformers have slightly better quality-factors. This means that the reduction this topology brings to the resistance and capacitance of the windings is proportionally more substantial than the reduction on the inductance. As a result, since the coupling coefficient is the same for both structures, the minimum insertion loss is lower for octagonal transformers.

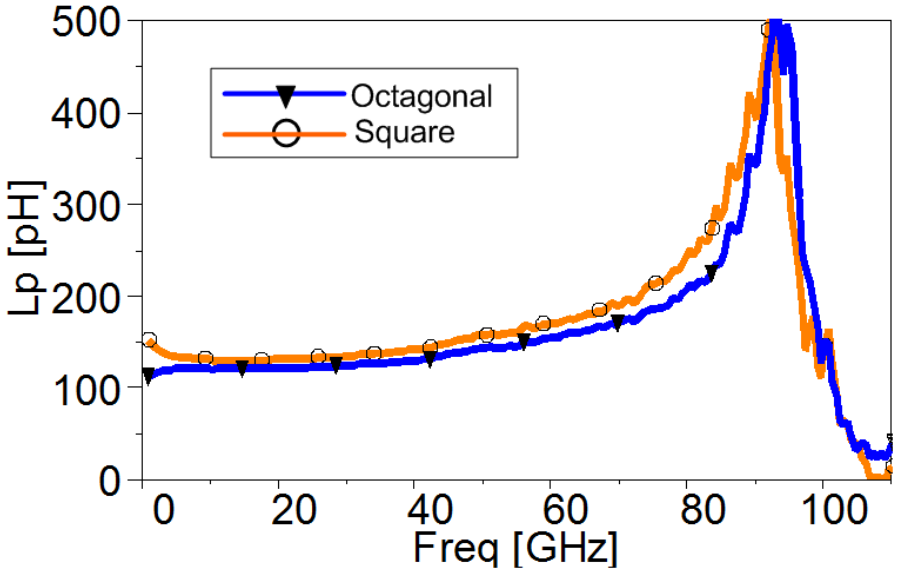


Figure 2-15 Measured inductances of square and octagonal transformers.

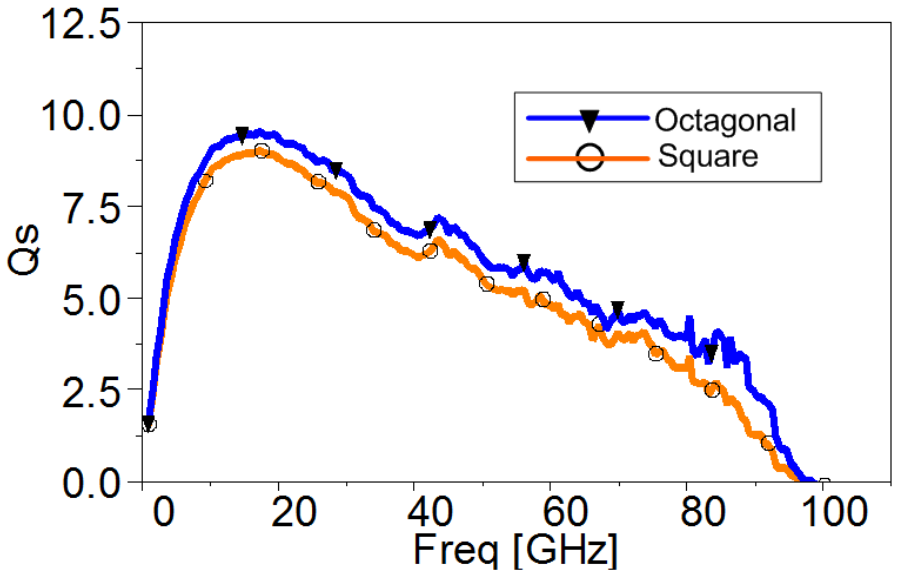


Figure 2-16 Measured quality-factors of square and octagonal transformers.

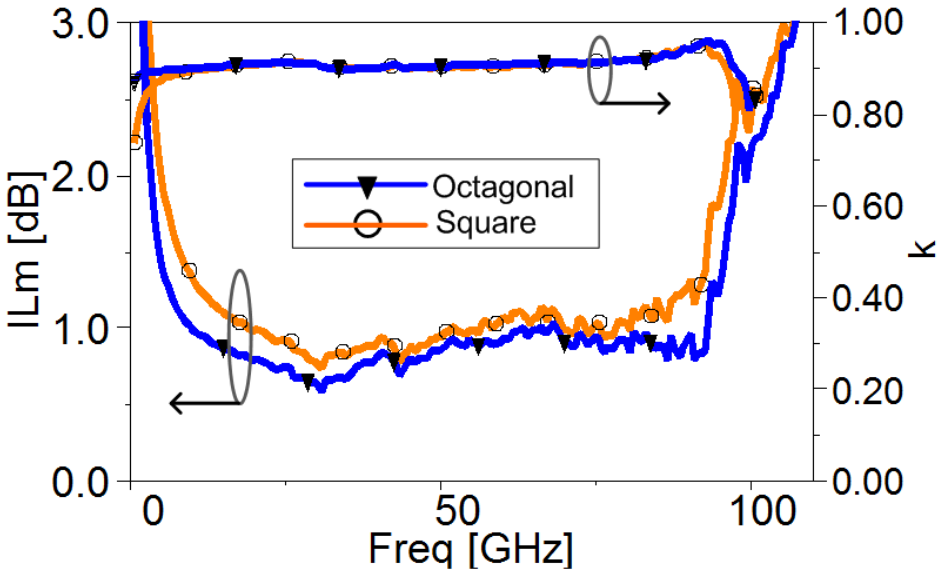
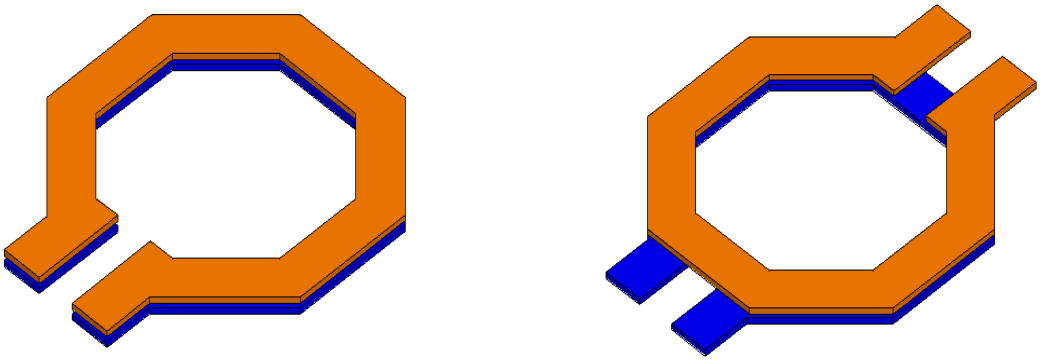


Figure 2-17 Measured coupling coefficient and minimum insertion loss of square and octagonal transformers.

4.3 Position of feed lines

As the stacked topology is adopted, the relative position between primary and secondary is further considered in terms of the location of their respective leads. One approach is to have the primary completely covering the secondary, so that their feed lines overlap (Figure 2-18a). Another possibility (flipped transformer) consists in a 180-degree rotation of one of the windings (Figure 2-18b). This configuration results in an uncovered zone of the coils, which tends to weaken their coupling. The choice between these structures should be made not only in function of their performance but also considering which one is better suited to the layout of a specific circuit.



(a) (b)

Figure 2-18 (a) Non-flipped and (b) flipped transformer topologies.

Figure 2-19 —Figure 2-21 present measurement results for transformers with those two topologies in the 65-nm CMOS technology. The obtained curves exhibit a significant reduction of the resonant frequency of the transformer when the flipped topology is adopted. Since low-frequency self-inductances remain unchanged and magnetic coupling is weakened, this reduction results mostly from the augmented oxide and substrate capacitance that this topology presents. Even though magnetic coupling is significantly lower, global coupling including capacitive effects presents similar results beyond 50 GHz. It is also observed that the flipped transformer shows a lower minimum insertion loss for frequencies greater than 50 GHz, whereas the non-flipped transformer presents a proper performance for a wider band.

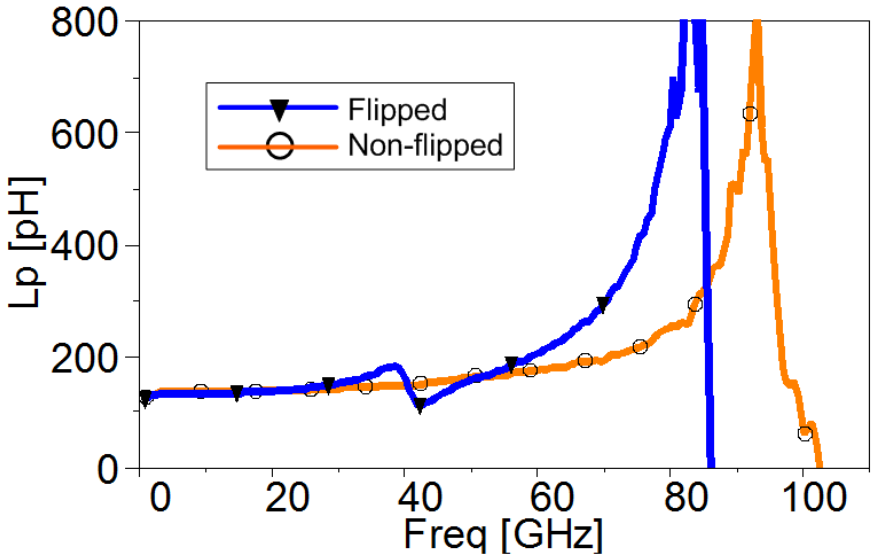


Figure 2-19 Measured inductances of flipped and non-flipped transformers.

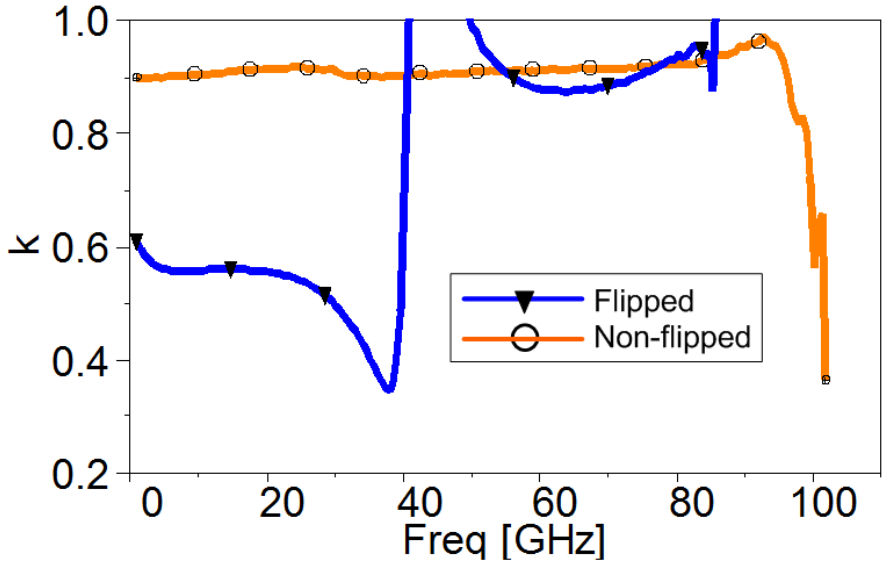


Figure 2-20 Measured coupling coefficients of flipped and non-flipped transformers.

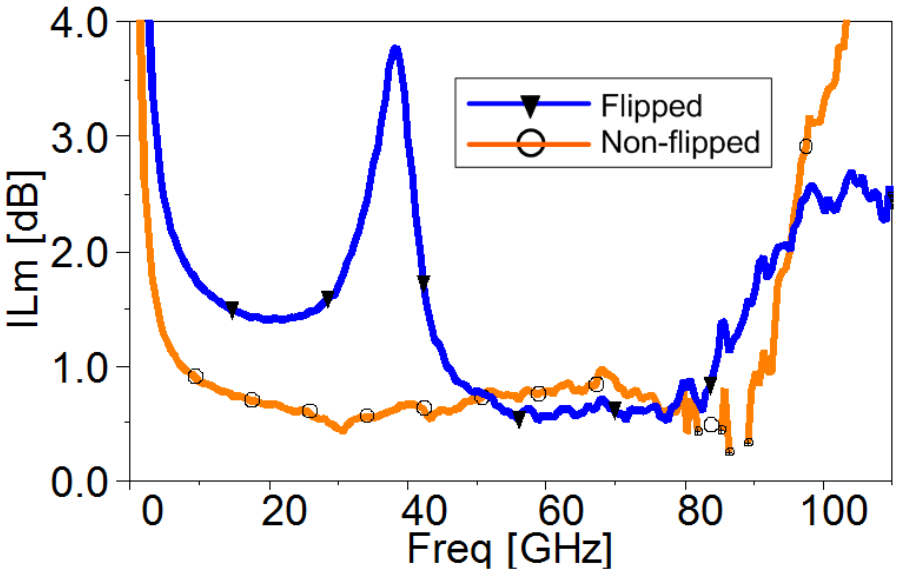


Figure 2-21 Measured minimum insertion loss of flipped and non-flipped transformers.

Nevertheless, the most notable phenomenon observed for the flipped transformer is its *partial resonance* around 40 GHz. This frequency corresponds to the resonant frequency of the primary when the secondary is shorted, as Figure 2-22 shows. Indeed, Q_{PY}, defined in (2-14) represents the quality-factor of the primary extracted from admittance parameters, i.e., when the secondary is shorted. A reflex of the weaker magnetic coupling, this frequency is seen to be inferior to the resonant frequency traditionally derived from the impedance parameters in the particular case of single-turn flipped transformers.

$$Q_{PY} = \frac{\mathrm{Im}\left(Y_{11}^{-1}\right)}{\mathrm{Re}\left(Y_{11}^{-1}\right)} \tag{2-14}$$

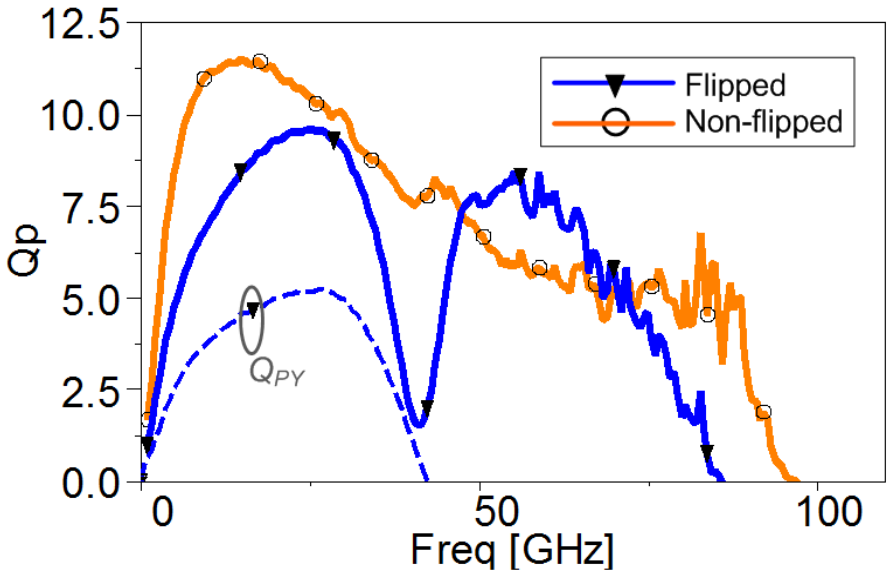


Figure 2-22 Measured quality-factors of flipped and non-flipped transformers.

4.4 Geometric dimensions

Once the general topology of a transformer is defined, it is important to examine the dimensioning of the component. Hence, the influence of the different geometric dimensions of the conductors on the transformer performances is studied in this section.

Firstly, the impact of the winding diameter is considered. Two 65-nm CMOS transformers presenting the exact same topology but different average diameters were compared. They were laid out in a flipped configuration with octagonal windings and 8-µm wide traces. The considered diameters are 50 µm and 60 µm.

Measurement results are presented in Figure 2-23 —Figure 2-26. As the increased diameter is directly reflected in an increased total electric length, the obtained results reinforce the direct dependency between length and the low-frequency inductance value. Also, magnetic coupling is observed to be stronger for the larger transformer, and, since the effective capacitance of the transformers is a function of their total area, the resonant frequency is distinctively lower for the greater diameter. Regarding the quality factors, we perceive that their maximum values remain unchanged before the partial resonance. Beyond this frequency, though, the Q-factor is superior for the smaller transformer. For this reason, the measured minimum insertion loss is equivalent for the two transformers in the vicinity of 60 GHz. Thus, we can conclude that for the same topology and conductor width, the choice of the transformers diameter for an integrated circuit should mostly rely on the desired inductance, resonant frequency and occupied surface.

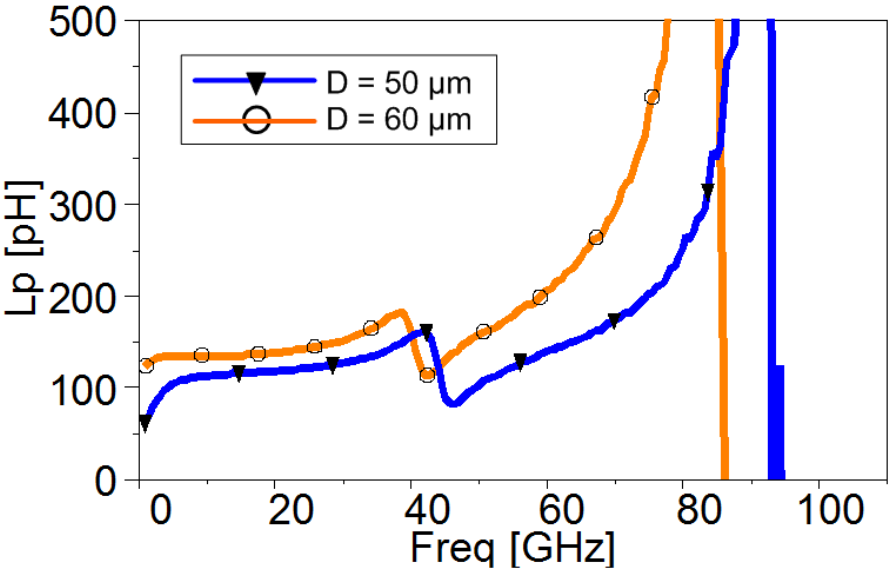


Figure 2-23 Measured inductances of transformers with different diameters.

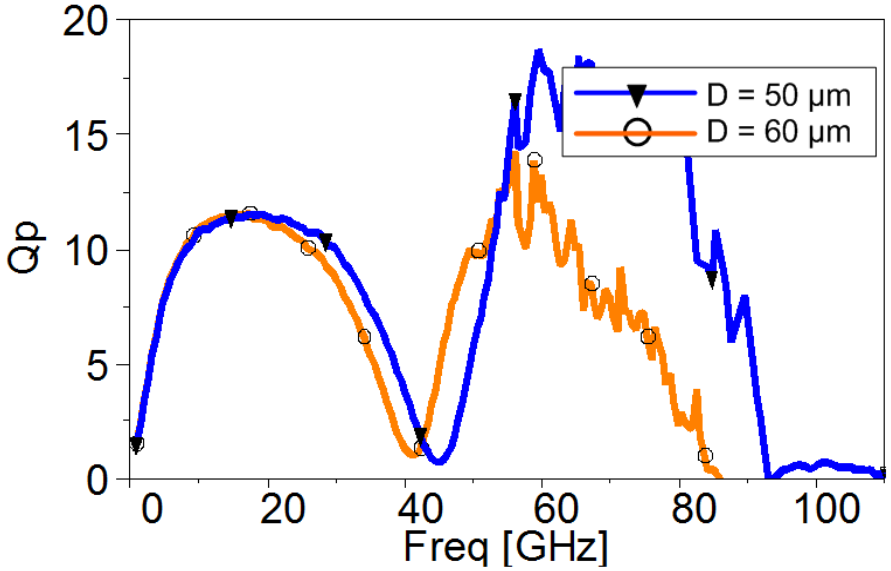


Figure 2-24 Measured quality-factors of transformers with different diameters.

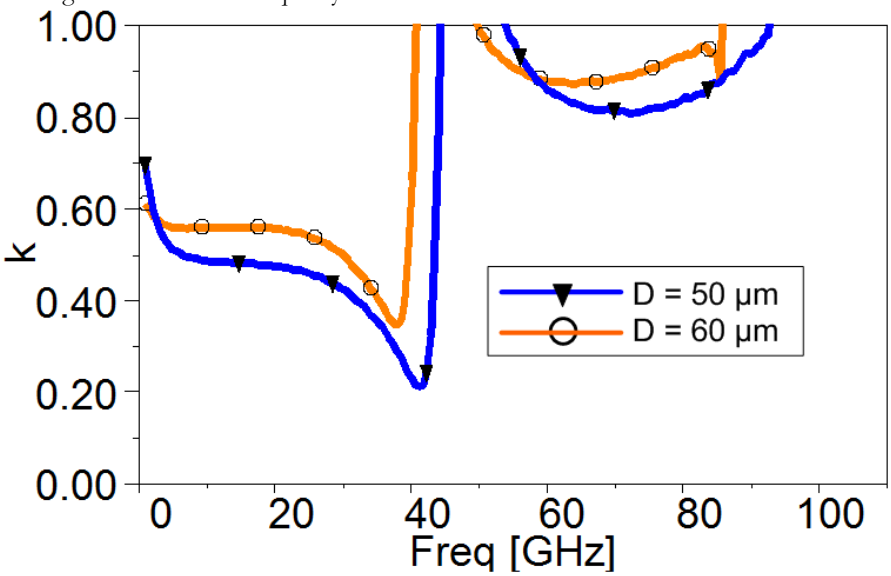


Figure 2-25 Measured coupling coefficients of transformers with different diameters.

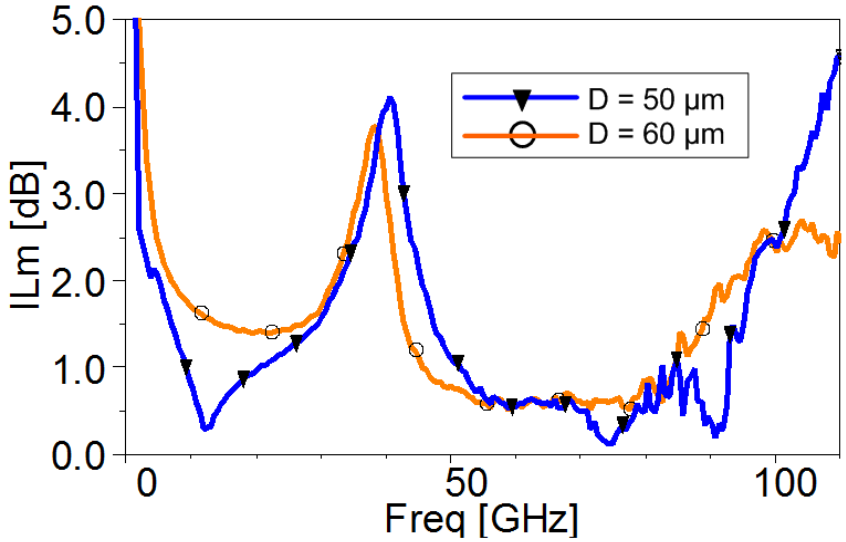


Figure 2-26 Measured minimum insertion loss of transformers with different diameters.

Afterwards, the trace width of conductors was analyzed. This study was based on measurements of three 65-nm CMOS transformers, with a non-flipped topology and the same average diameter (60 µm). Their respective widths were 4 µm, 8 µm, and 12 µm.

Obtained measurement results are depicted in Figure 2-27 — Figure 2-30. We remark a linear effect of the width on the inductance; the narrower the traces are, the higher the inductance is. The influence on the quality-factors, on the other hand, is not so straightforward. Results show that Q-factors vary as frequency increases, so that for lower frequencies the 12-µm wide transformer has a better Q, whereas the quality factor of the 4µm wide transformer is superior for higher frequencies. The resonant frequency of the transformer is not significantly affected, since the augmentation of the inductance for narrow traces is compensated by a reduction on the equivalent capacitance, which is related to the surface the transformer occupies. It is also observed that the coupling factor is improved for wider transformers. Finally, we observe that increasing the width from 4 µm to 8 µm produces an improvement on the minimum insertion loss. Nevertheless, if the trace width is further augmented to 12 µm, we verify an equivalent performance.

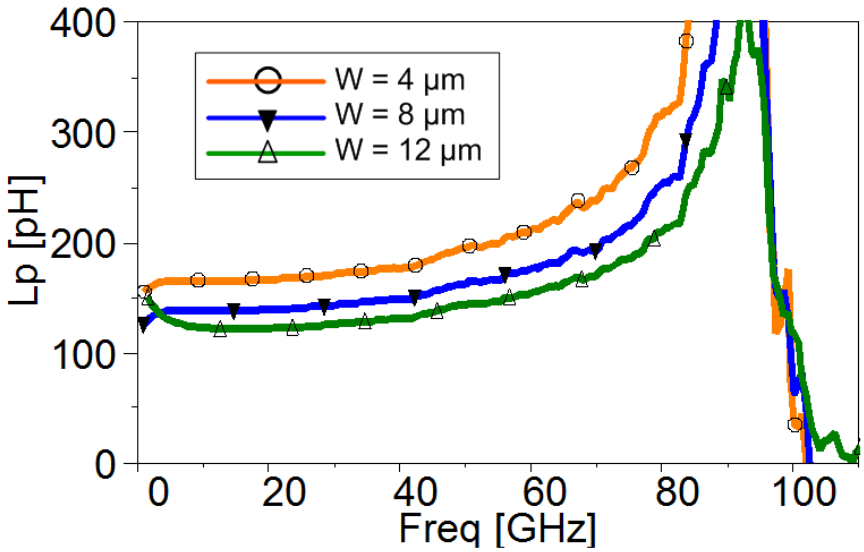


Figure 2-27 Measured inductances of transformers with different trace widths.

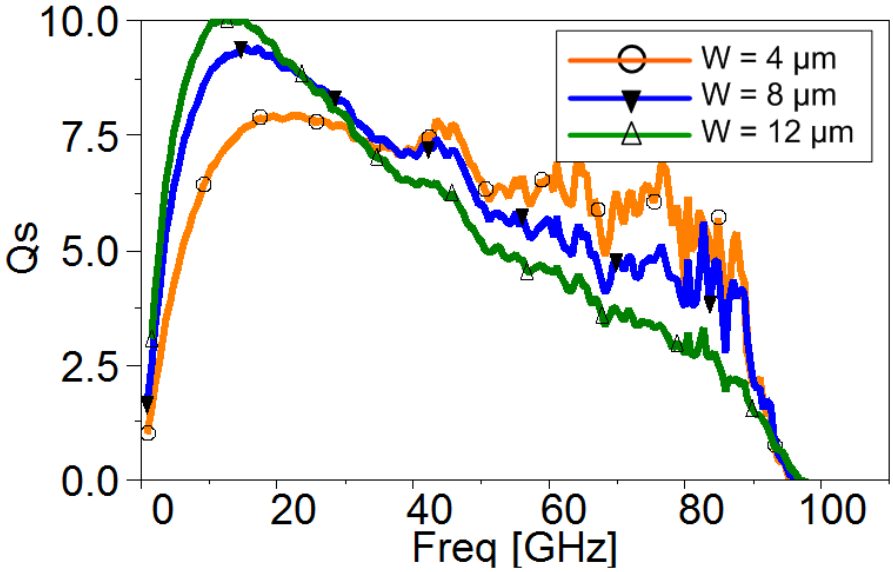


Figure 2-28 Measured quality-factors of transformers with different trace widths.

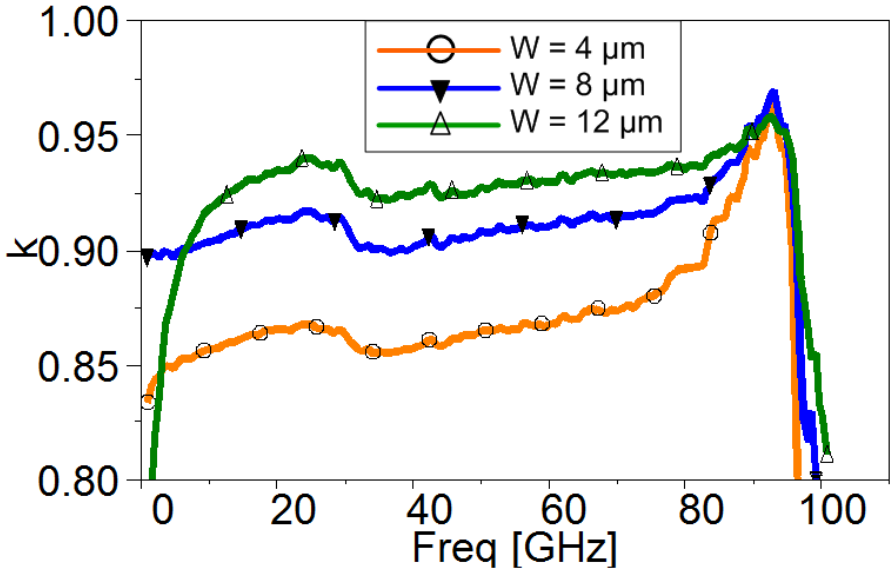


Figure 2-29 Measured coupling coefficients of transformers with different trace widths.

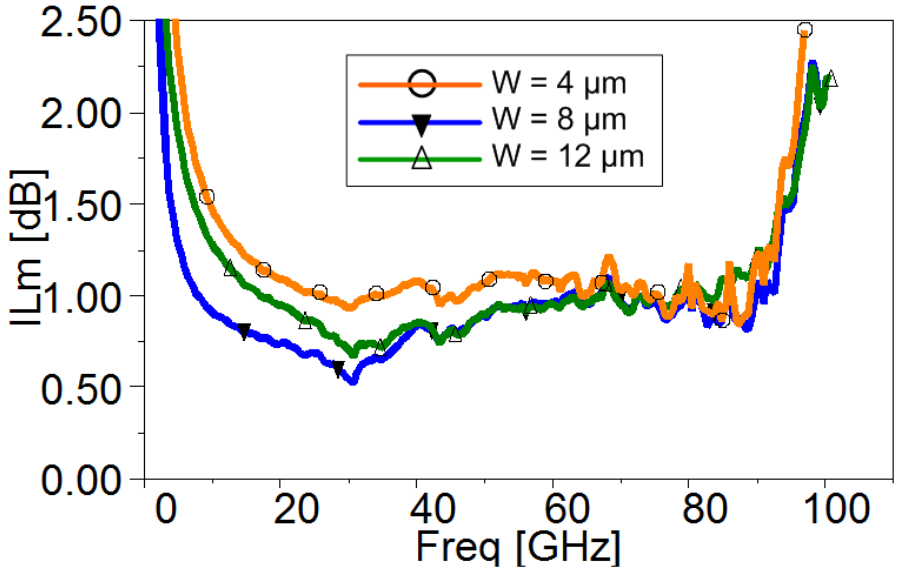


Figure 2-30 Measured minimum insertion loss of transformers with different trace widths.

Skin effect is patent for the considered conductors. Figure 2-31 shows the EM simulation of the current density on the bottom face of the primaries of the three transformers at 60 GHz. It is clearly noticed how, even for the 4-μm transformer, current is mostly concentrated on the edges of the conductors. This effect contributes to limiting the attainable insertion losses

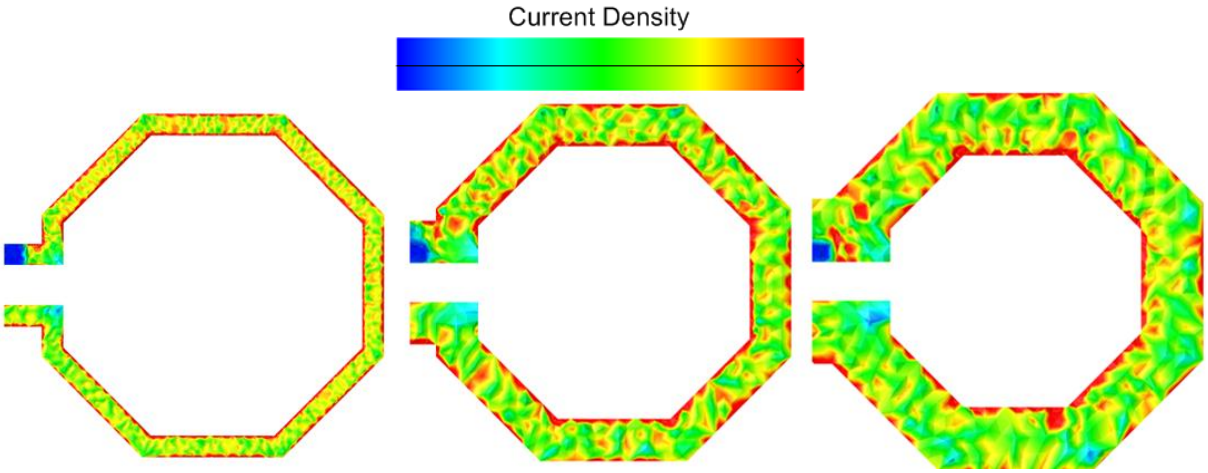


Figure 2-31 Simulated current density at 60 GHz for transformers with different trace widths.

Finally, the effect of metal thickness along with vertical spacing between coils and distance to the substrate was evaluated. As those characteristics are technology-dependant, this analysis concerned transformers with the same layout realized in the two different technologies considered in this work, i.e., 65-nm CMOS and BiCMOS9mW.

Figure 2-32 — Figure 2-34 depict the measurement results. A drastic reduction on the inductance is verified for the BiCMOS technology. This, analogously to the trace width observation, is due to the considerably thicker conductors. The resonant frequency, on the other hand, is substantially lower for the CMOS process. Such behavior is credited to the greater capacitance originated from the closer position between conductors and the substrate. Those two factors conjugated (thicker metals and higher back-end) provide a distinctively superior quality-factor in the case of the BiCMOS9mW transformer. Thus, in spite of the stronger magnetic coupling verified for the CMOS technology, minimum insertion loss is remarkably lower for BiCMOS9mW in the mm-wave range.

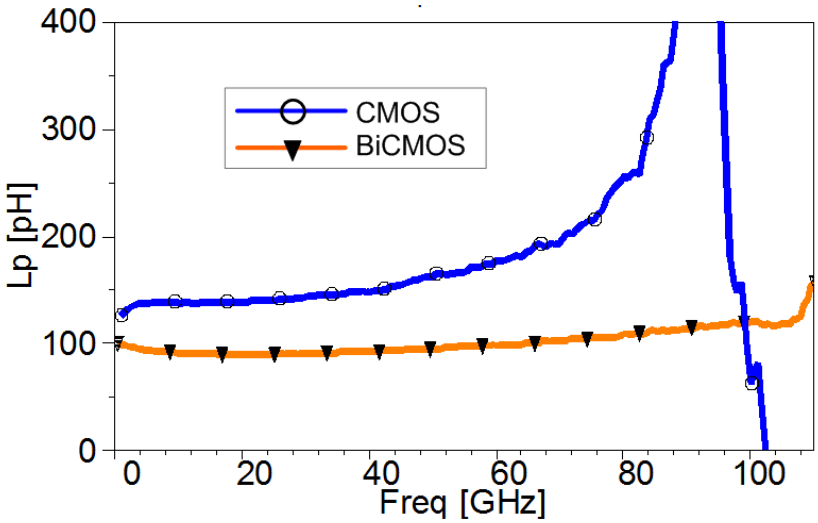


Figure 2-32 Measured inductances of transformers in different technologies.

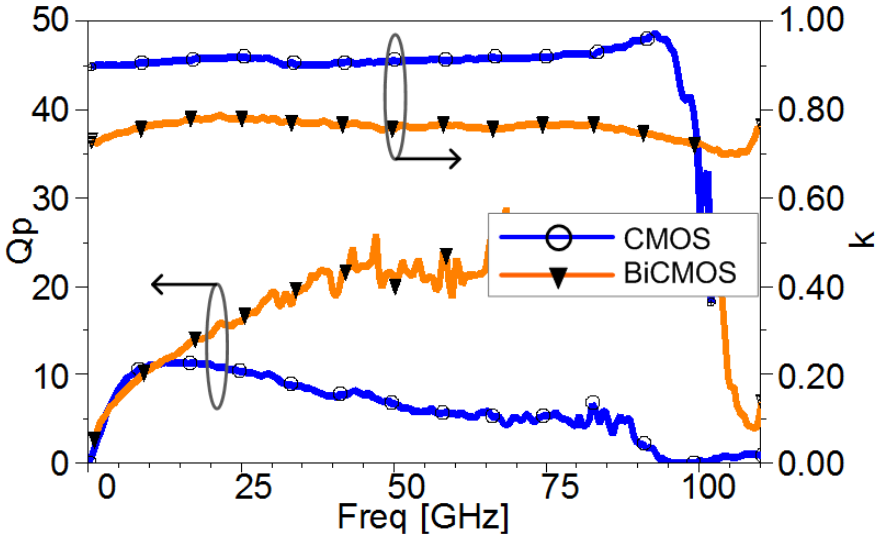


Figure 2-33 Measured quality-factors and coupling coefficients of transformers in different technologies.

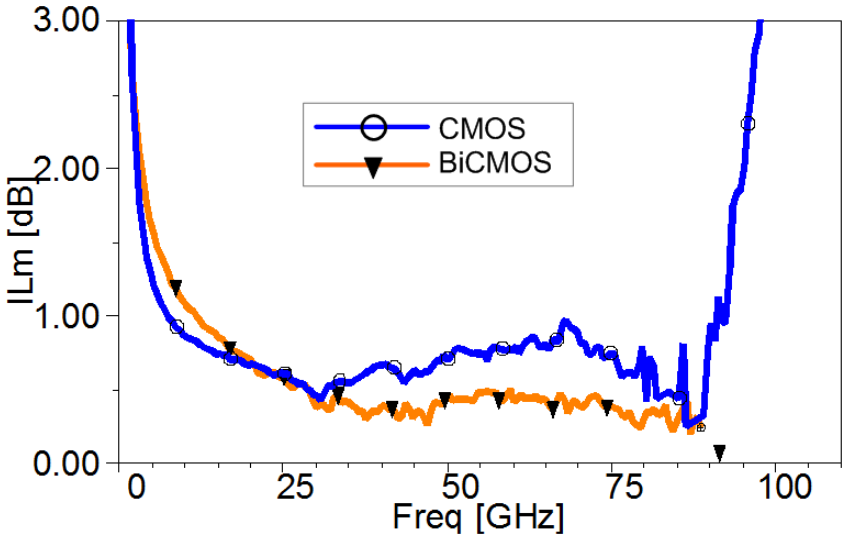


Figure 2-34 Measured minimum insertion loss of transformers in different technologies.

5 Substrate Shielding

The performance of integrated transformers and inductors are strongly influenced by substrate losses [CHE06-1]. For this reason, several methods have been proposed in order to reduce substrate losses and, hence, improve their quality-factors. In [NG02], the silicon substrate is physically removed and replaced by an insulating quartz substrate. This technique, however, presents an important drawback, since it requires additional fabrication steps. In order to reduce substrate losses using standard manufacturing processes and, therefore, not impacting the fabrication costs, patterned ground shields (PGS) are widely used [BIO06, GHA06-3, LIA06, NG02, YIM02, YUE98]. As an alternative to ground shields, [CHE06-1] proposed the use of a floating shield between the conductors and the substrate. Both structures have already been shown to mitigate substrate losses on inductors and transformers operating in frequencies inferior to 10 GHz. In this section, this study is carried out in the mm-wave range.

5.1 Patterned Ground Shield

The objective of employing ground shields is to reduce the penetration of the electric field originated from the coil into the substrate so that the effective resistance of the shield will approach zero. Consequently, it is supposed to reduce the overall substrate current, improving the quality-factors of the component.

Solid planes have been experimented [YUE98], but, regardless of the efficient electric shielding, they presented a significant amount of eddy current on the shield, which introduced additional losses and a substantial decrease of the effective inductance. Indeed, the idea of patterning the shield appeared, so that this current could be minimized.

Different configurations of PGSs have been proposed in the literature. In [BIO06], [LIA06], and [NG02] studies on various layout schemes are presented. Moreover, different materials have been reported to constitute the shields, such as lower metals, polysilicon, buried N+, P+ [LIA06], and N–well [YIM02] layers.

The layout of the patterned ground shield proposed in our realization is shown in Figure 2-35. It is very similar to the one used in [GHA06-3] and it is composed of polysilicon fingers and an *X* shape on the lowest available level of metal (M1). The purpose of M1 in this shield is to represent a low-impedance path connecting the four outer edges of the plane to a common ground potential. The polysilicon configuration is always orthogonal to the current flow on the conductor so as to avoid eddy currents. The polysilicon segments present a width of 4.5 μm, spaced by 1.7 μm.

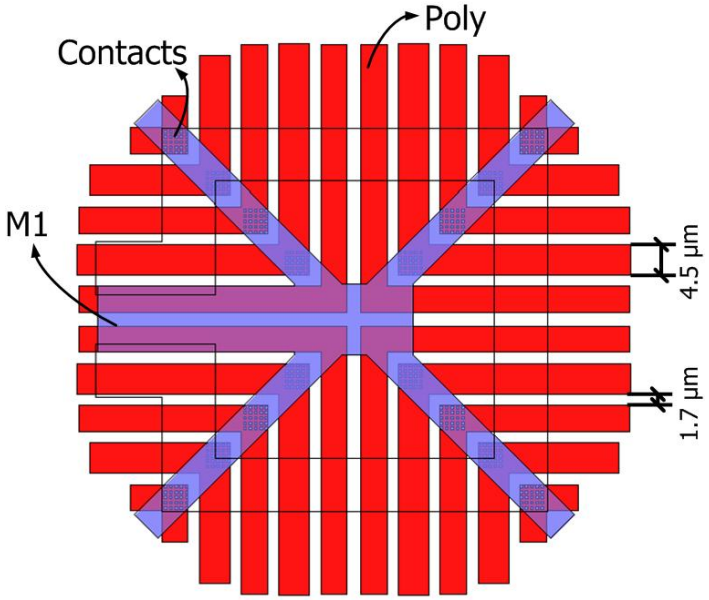


Figure 2-35 Layout of the patterned ground shield.

5.2 Floating Shield

Like for ground shields, the purpose of floating shields is to diminish the substrate current by preventing the electric field of the conductors from reaching the substrate (Figure 2-36). One drawback of ground shields is that they require a true 0 V reference, which is often difficult to obtain in an integrated circuit [CHE06-1]. Floating shields, though, by their nature, do not necessitate such references. Moreover, a floating shield improves the isolation among the devices on the circuit, since they are not connected together through their ground planes. Additionally, in order to satisfy the strict metal density requirements of advanced technologies, metal dummies are usually inserted in proximity of the component. Metal floating shields might replace these dummies with a positive impact on the quality-factors.

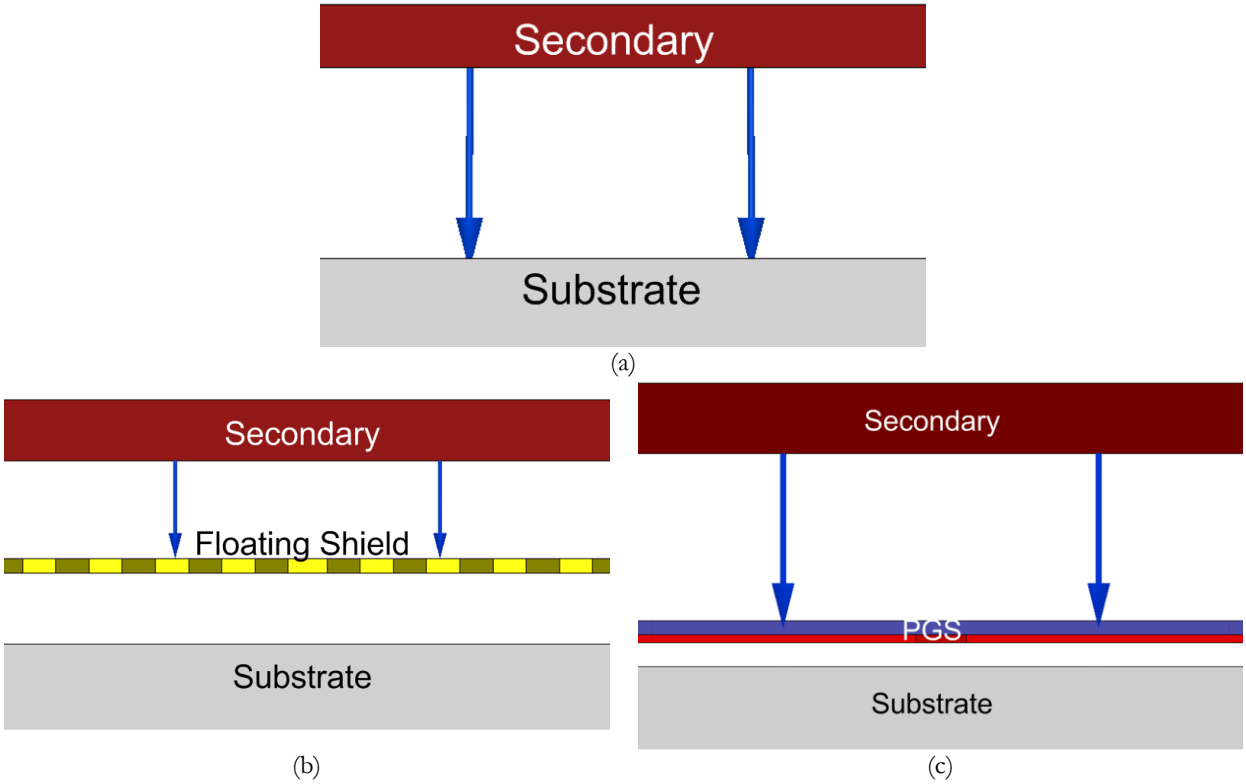


Figure 2-36 Electric field lines between conductors and substrate for integrated transformers with (a) no shield, (b) a floating shield, (c) a PGS.

Different designs of floating shields have been proposed in [CHE06-1] using the lower metal layers of the technology. In our study, the shield presents the topology exhibited in Figure 2-37. It consists of low metal strips (M1 and M2), which are placed beneath the conductors and not in the center of the spiral. The direction of the strips is always perpendicular to the current and they present a 0.5 μm width and a 0.5 μm distance between strips.

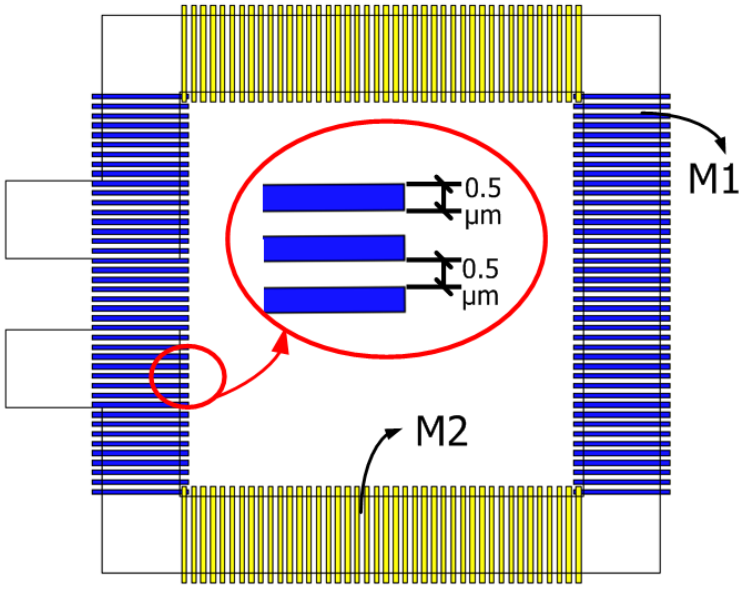


Figure 2-37 Layout of the floating shield.

5.3 Measurement results

A set of transformers exhibiting the same topology but different shielding structures was fabricated in a 65-nm CMOS technology in order to support this study. Extracted inductances are shown in Figure 2-38. We observe that the use of a shield does not affect their low-frequency values as they depend predominantly on the conductors' dimensions. Nevertheless, the resonant frequency of the windings is significantly reduced when a PGS is used, whereas it remains unchanged for a floating shield. This variation is due to the reduction of the distance between conductors and ground, which increases the corresponding capacitance. Such reduction is also observed for lower-frequency RF transformers, for which the use of patterned ground shields is customary. The use of floating shields, however, does not affect this capacitance.

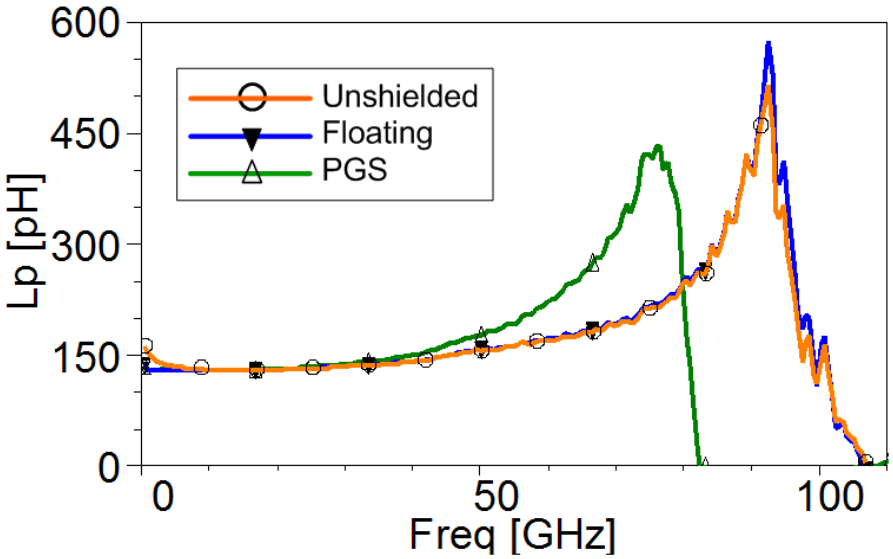


Figure 2-38 Measured inductances of transformers with a PGS, floating shield or without any substrate shielding.

Figure 2-39 depicts coupling coefficients. It is observed that substrate shielding does not impact mutual coupling considerably, despite the aforementioned influence on the resonance frequency. This result is due to the fact that transformer coupling is mostly concentrated in the region in between coils, and does not depend importantly on substrate currents.

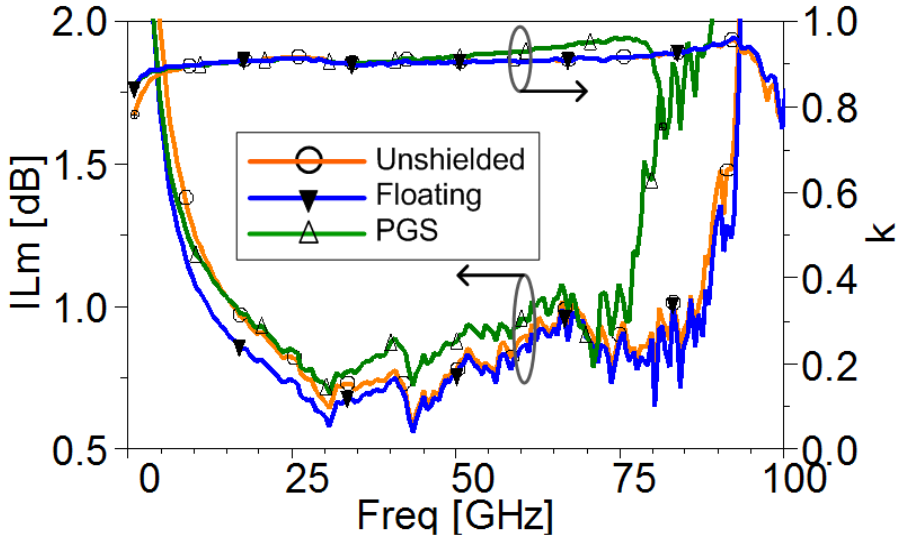


Figure 2-39 Measured coupling coefficient and minimum insertion loss of transformers with a PGS, floating shield or without any substrate shielding.

Since shielding does not present a strong effect on mutual coupling, the minimum insertion loss of the transformer is determined by the quality-factors. This corroborates the importance of this study on Q-factor enhancement of transformers. Measured quality-factors of primaries and secondaries are illustrated in Figure 2-40 and Figure 2-41. We notice that, in mm-waves, Q-factors diminish when a PGS is used. This result contradicts the observation made for RF transformers, for which such shields were shown to improve the performance of the component [GHA06-3]. For floating shields, on the other hand, the values of Q remain unchanged. As predicted, due to the results on coupling coefficients and quality-factors, the minimum insertion loss is increased for patterned ground shields and not significantly affected for floating shields (Figure 2-39).

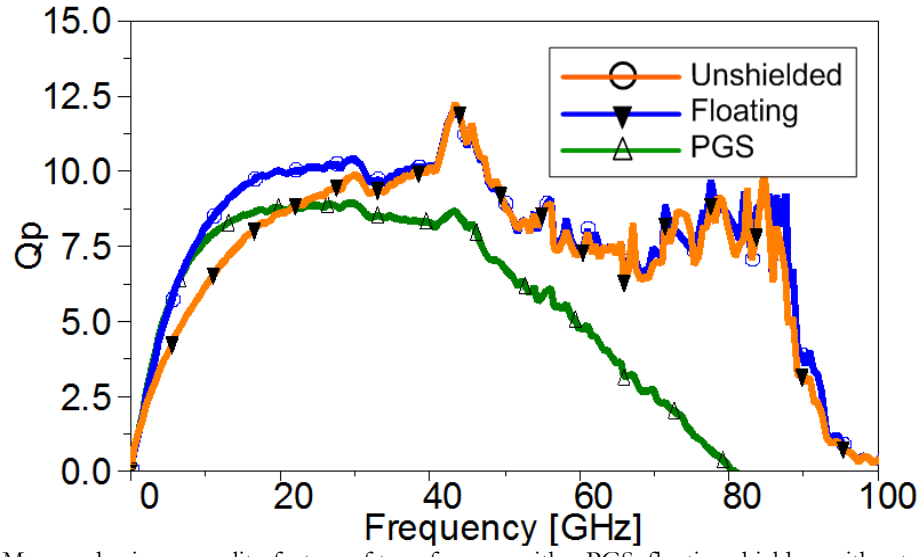


Figure 2-40 Measured primary quality-factors of transformers with a PGS, floating shield or without any substrate shielding.

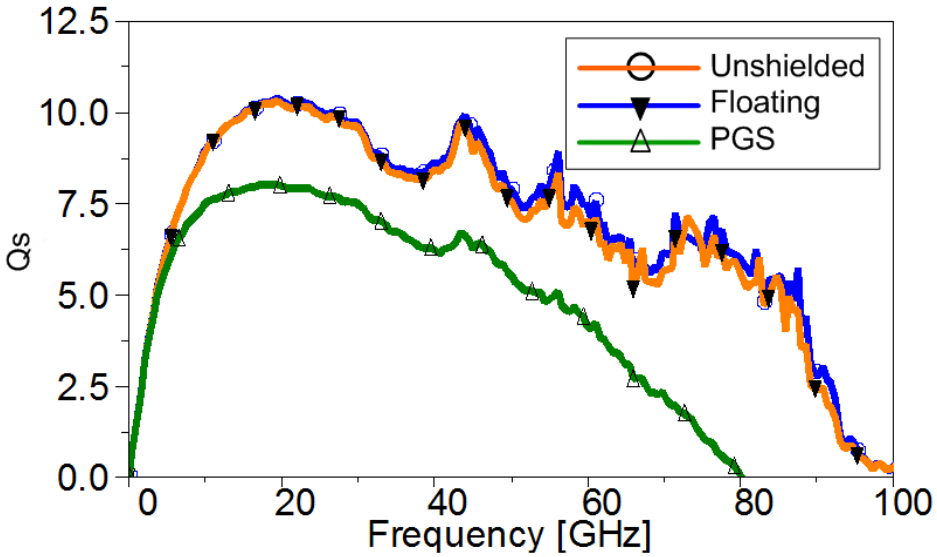


Figure 2-41 Measured secondary quality-factors with a PGS, floating shield or without any substrate shielding.

Electromagnetic simulations were carried out using Ansoft HFSS, in order to evaluate the influence of shielding, not only on the quality-factors, but on the respective substrate currents. The simulated substrate currents for the three studied transformers at 60 GHz are depicted in Figure 2-42. We observe that both types of shield reduce the substrate current and that this reduction is even more pronounced for the PGS.

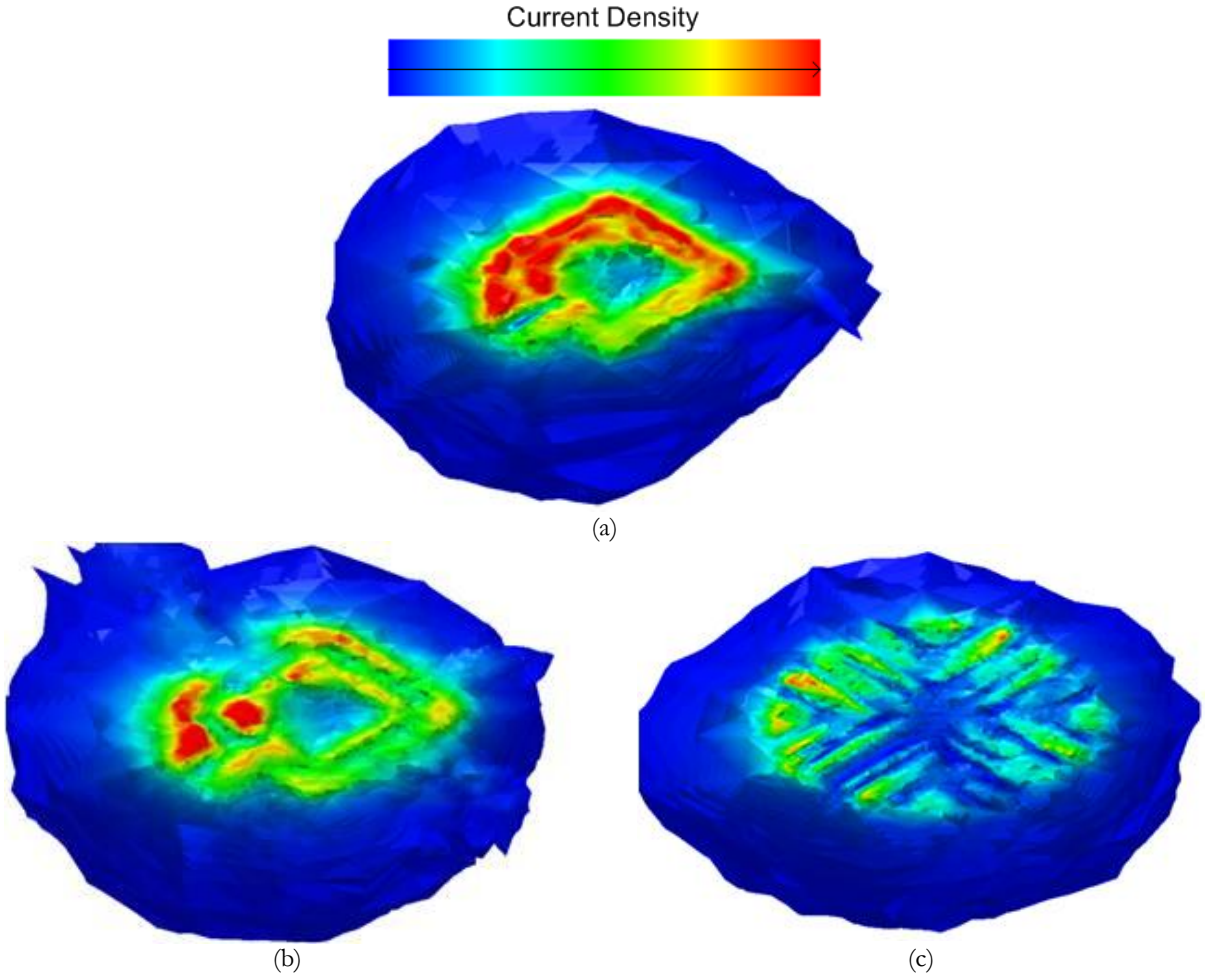


Figure 2-42 Simulated substrate current density for transformers with (a) no shield, (b) a floating shield, (c) a PGS.

In order to investigate the reason why the decrease on the substrate current is not reflected on a quality-factor improvement for the transformer with a PGS, the simplified transformer model of Figure 2-43 was considered. A comprehensive study of mm-wave transformer modeling, including the calculation of model components is provided in Chapter 3.

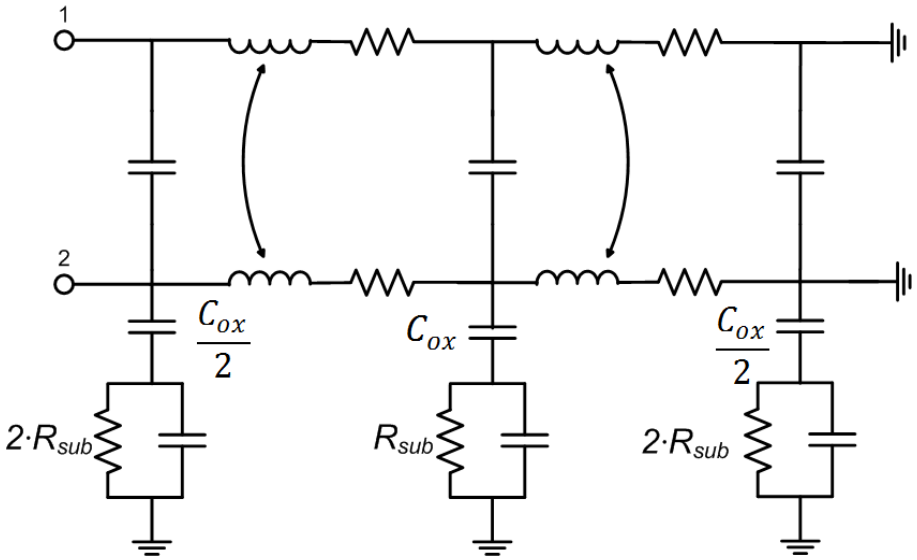


Figure 2-43 Simplified transformer model for shielding analysis.

It was considered that most of the effect of the PGS would be on the resistances whose values are R_{sub} or $2{\cdot}R_{sub}$ and the capacitances C_{ox} and $C_{ox}/2$. A typical unshielded mm-wave transformer was simulated, for which R_{sub} = 135 Ω and C_{ox} = 25 fF. Since the goal of using a PGS is to attain resistance values close to zero, two cases were further considered for lower values of R_{sub} (10 Ω and 0.1 Ω). Finally, in order to account for the influence of the PGS on the considered capacitance, another simulation was carried out considering C_{ox} = 30 fF. The obtained primary and secondary quality-factors are depicted in Figure 2-44 and Figure 2-45.

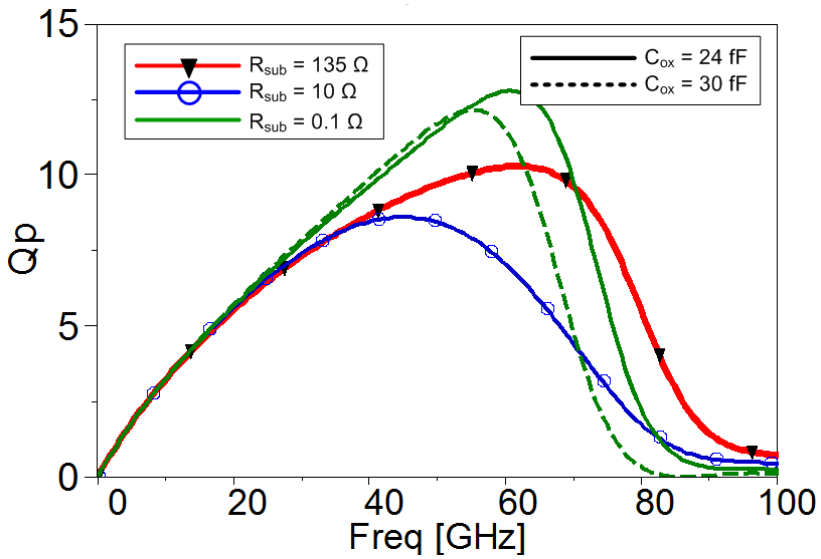
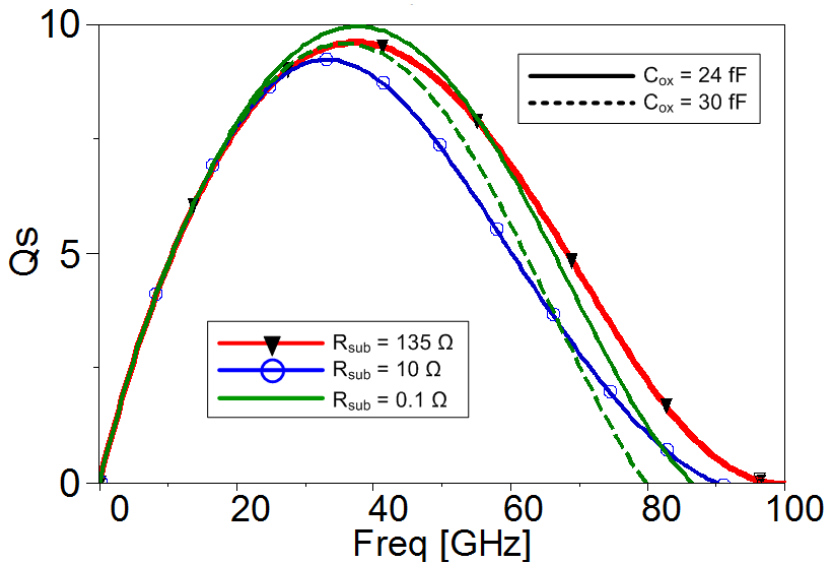


Figure 2-44 Simulated primary quality-factors obtained from model simulation for different values of R_{sub} and C_{ox}.



(b)

Figure 2-45 Simulated secondary quality-factors obtained from model simulation for different values of R_{sub} and C_{ox}.

It is observed from these simulations that, while keeping C_{ox} constant, reducing R_{sub} initially deteriorates the quality-factors, which is reversed only when these values become very low (in our simulations, for values inferior to 10 Ω and, especially at 0.1 Ω, when Q-factors are distinctly higher). Hence, it is clear that it is not sufficient to reduce substrate resistances by adding a shield to benefit from better quality-factors for the coils. Indeed, unless the constitution of transformer and shield allows considerably low resistance values, its addition will present the opposite effect, i.e., quality-factors will be degraded. Moreover, taking also into account the augmentation on C_{ox}, which is inevitable and reduces both resonant frequency and quality-factors, it is possible that even for a near-zero resistance, the Q-factor remain unimproved, as it is the case for the secondary in our simulation.

6 Transformation Ratio

Hitherto, transformers presenting the same geometry for primary and secondary have been examined in this study. It is known that the use of transformers to perform impedance matching may be very interesting in an integrated circuit. Thus, in order to accomplish this task as efficiently as possible, it is important that the component provide a suitable impedance transformation from its primary to secondary coil.

Previous works have reported techniques used to obtain the desired impedance ratios on integrated transformers. For RF transformers operating in lower frequencies, the adopted topology is usually based on multi-turn spirals. The transformation ratios are hence obtained through the choice of a convenient turn ratio between primary and secondary. In those cases, the number of turns of a particular winding is generally limited to 5 [GHA07, ROT06].

Nevertheless, even for those frequencies, different topologies have been proposed to achieve higher impedance ratios. In [GHA07], for instance, all turns of one of the windings are

connected in parallel in order to decrease its overall effective inductance. [LIM08] extrapolates this idea by connecting the different primary turns several times in parallel. Moreover, a multi-layer approach is used to further increase secondary inductances.

At mm-waves, on the other hand, we cannot design transformers with more than 2 turns in a winding. A superior number of turns would imply a considerably low resonant frequency, so that proper mm-wave operation would not be possible, and higher losses would appear. For this reason, most of the transformers currently used in mm-waves integrated circuits present stacked single-turn primaries and secondaries so that their inductance ratios are close to unity [CHA09, CHO09].

Some transformers which perform impedance transformation at mm-waves can be seen in [DIC05] and [LAR08]. Those transformers present a 1:2 turn ratio and a planar topology. Additionally, in all those cases, the trace width of primary conductors is the same as the secondary's. A different approach is presented in [CHE06-2]. For this transformer, the primary is placed within the secondary, i.e., the secondary completely encloses the primary both horizontally and vertically. In this case, the primary, which has 2 turns, presents narrower traces than the single-turn secondary.

In this work, we propose a novel topology based on a stacked configuration, for which primaries and secondaries present different trace widths and diameters in order to achieve higher transformation ratios at mm-waves [BEL10].

The proposed topology is based on two well-known principles of transmission lines and lumped inductances, which were verified in our previous measurements. First of all, the longer a line is, the higher its inductance will be. Considering the geometric parameters we adopt in our transformer design, it means that larger diameters will lead to higher inductances. Also, the wider a conductor trace is, the lower its respective inductance will be. Moreover, we also employ the number of turns as a parameter to obtain the desired impedance ratios. An inductor with two turns will present a higher inductance value not only for being electrically longer, but also due to the mutual inductance between turns.

Hence, we design a transformer presenting its primary and secondary with different conductor widths and different diameters. The dimensions should be comprised between the cases when inner diameters and when outer diameters of the windings coincide, so that vertical coupling can take place. The minimum and maximum trace widths, on the other hand, are determined by metal density rules, which are specific to each technological process.

Therefore, in order to achieve a transformation ratio as high as possible, the primary traces should be made as wide and the secondary traces as narrow as possible. Additionally, the primary must be single-turn and the secondary would present two turns. Finally, the outer diameters of the windings should coincide, as in Figure 2-46.

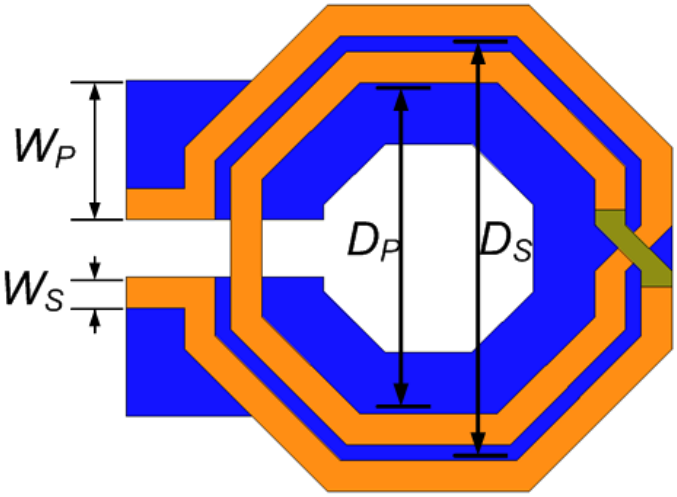
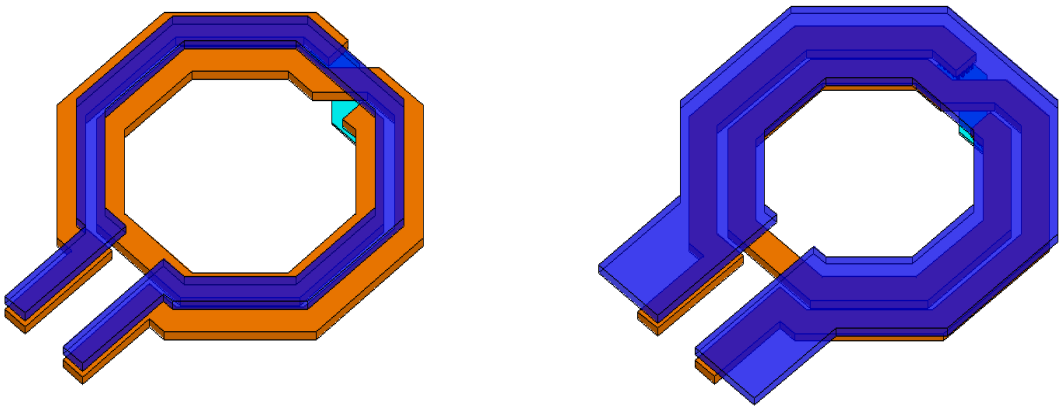


Figure 2-46 Layout of transformer with different primary and secondary diameters and trace widths.

6.1 Different trace widths

6.1.1 CMOS measurement

The first comparison we perform concerns the impact of presenting different trace widths for the primary and secondary. The structure of the considered CMOS transformers is shown in Figure 2-47. They present the same secondary geometry consisting on a 2-turn winding, with a 4-μm trace width, 1.5-μm spacing between turns, and a 42-μm average diameter. Primaries, on the other hand, present a 42-μm average diameter, so that they are centered above the secondaries. In the first case, as for a traditional design, the trace width is the same as for the secondary, i.e., 4 μm, and in the second case the primary is 12-μm wide, which corresponds to the maximum allowed width for this technology.



(a) (b)

Figure 2-47 3-D view of CMOS transformers with (a) W_P = 4 μm, (b) W_P = 12 μm.

The measurement results of these transformers are depicted in Figure 2-48 — Figure 2-51. It is observed that the proposed topology allows an increase from 3.1 to 4.2 on the inductance ratio at 60 GHz. On the other hand, the resonant frequency of the component is reduced, due to the augmentation of its effective capacitance. Moreover, the secondary quality factor is degraded, as well as the primary high frequency quality factor. Nevertheless, this is

compensated by the increased coupling factor the transformer with a 12-µm trace presents (0.86 against 0.81 for the traditional design), which allows a better minimum insertion loss. Indeed, using the proposed topology, the minimum insertion loss is reduced from 1.3 dB to 1 dB at 60 GHz. Thus, we observe that the use of a wider primary above the secondary not only allows a higher transformation ratio, but also a better performance at mm-waves.

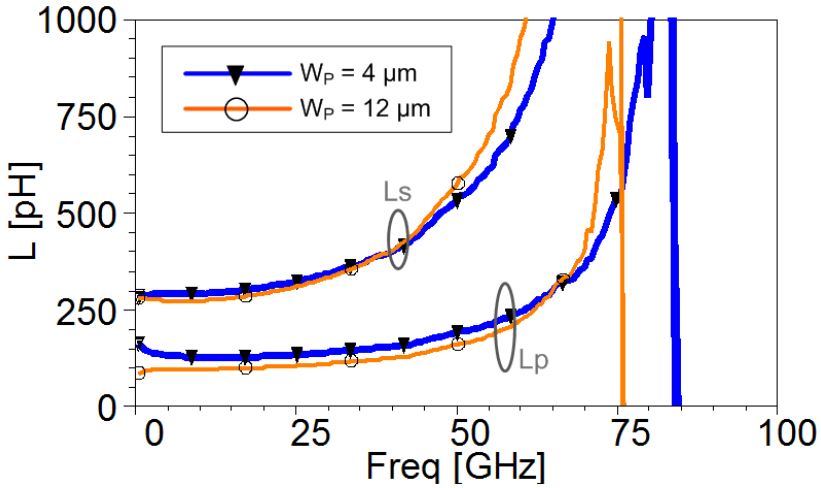


Figure 2-48 Measured inductances of CMOS transformers with different primary trace widths.

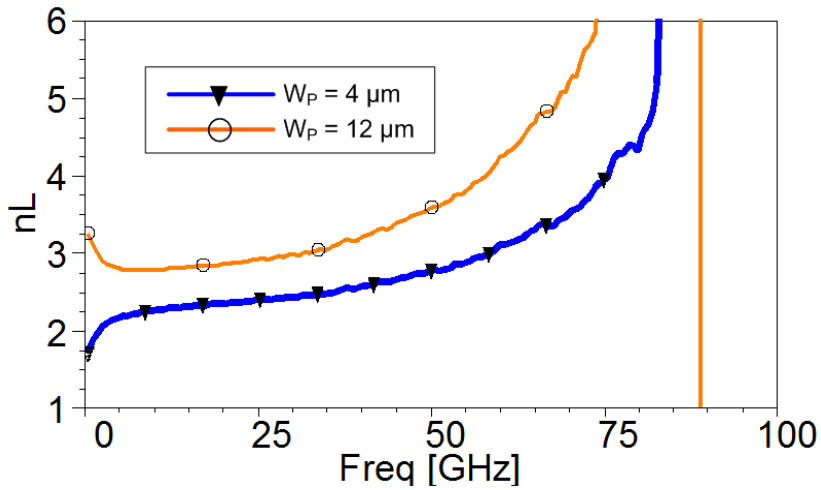


Figure 2-49 Measured inductance ratio of CMOS transformers with different primary trace widths.

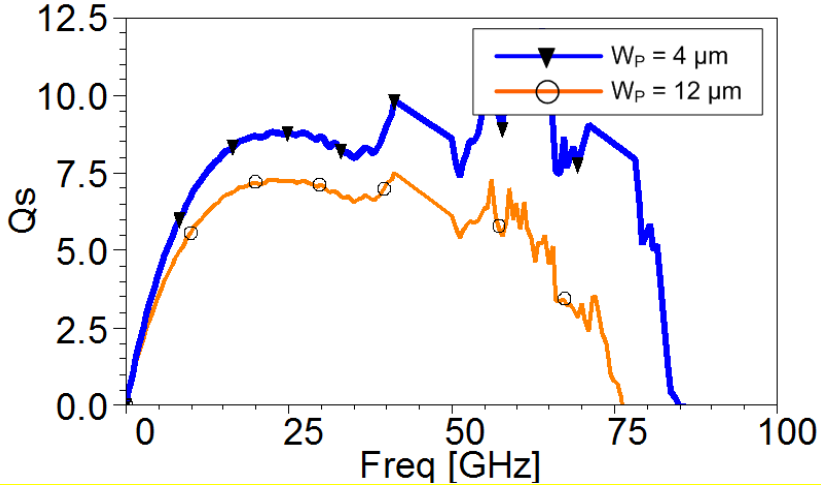


Figure 2-50 Measured quality-factors of CMOS transformers with different primary trace widths.

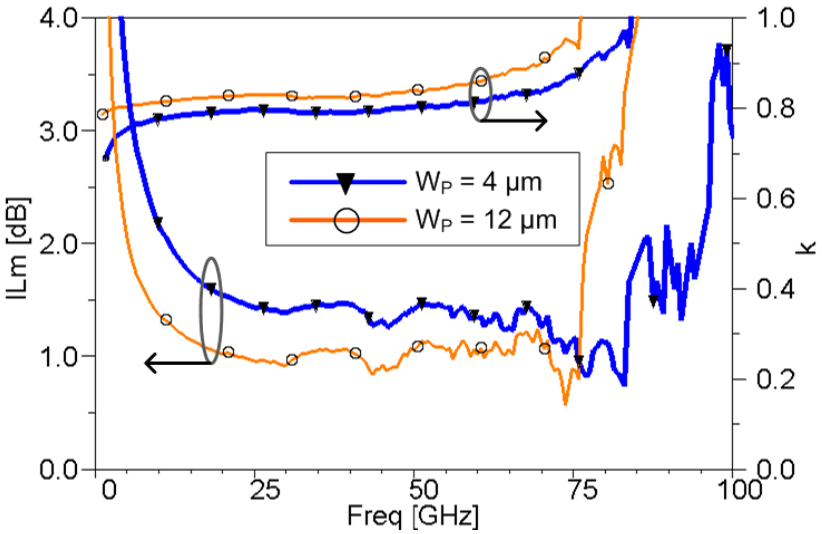
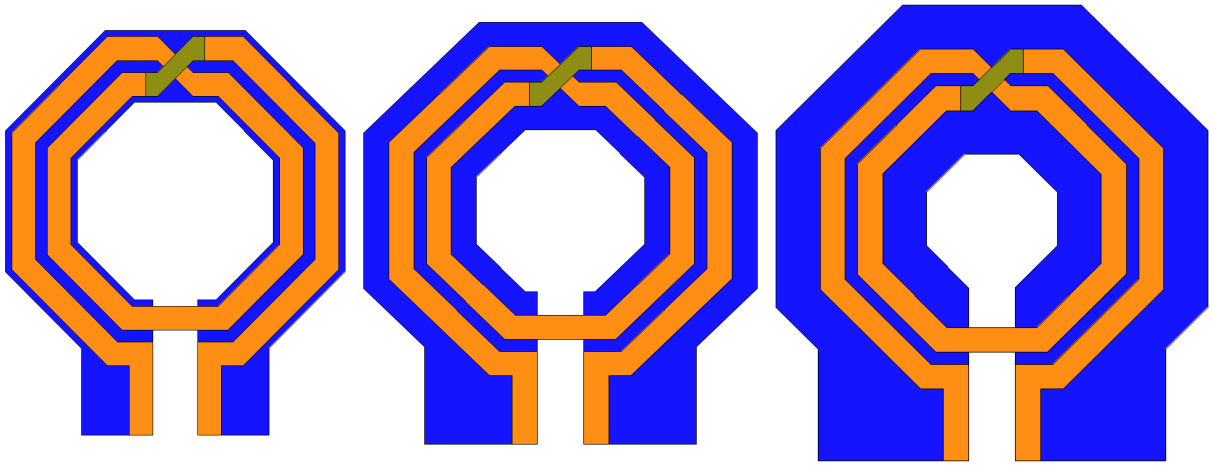


Figure 2-51 Measured coupling coefficient and minimum insertion loss of CMOS transformers with different primary trace widths.

6.1.2 BiCMOS measurement

In order to further evaluate this topology, 3 other transformers were designed in the SiGe technology, which allows metal widths up to 30 µm. The secondaries of these transformers present 2 turns, with a 45-µm diameter, 4-µm trace width, and a 2-µm inter-turn spacing. Their primary diameter is equal to 45 µm, while the metal widths are respectively 12 µm, 18 µm, and 24 µm (Figure 2-52).



(a) (b) (c)

Figure 2-52 Layout of BiCMOS transformers with (a) W_P = 12 µm, (b) W_P = 18 µm, (c) W_P = 24 µm.

The obtained results (Figure 2-53 — Figure 2-55) confirm how transformation ratios are increased as primaries are wider. Hence, the obtained ratios at 60 GHz are as high as 4.8, 5.5, and 6.1 for respective primary widths of 12 µm, 18 µm, and 24 µm. In these cases, resonant frequency is not strongly affected. Unlike the previous observation for CMOS transformers, widening primary traces leads to a weaker magnetic coupling. This is due to the fact that mutual inductance between coils depends directly on the overlapping area between primary and secondary, which in this observation becomes proportionally lower as primaries are enlarged. The results on the

quality-factor show a resembling performance for 12 and 18 µm and higher losses for the 24-µm transformer. As a consequence, minimum insertion losses are equivalent for both 12-µm and 18-µm primaries (IL_m about 0.8 dB), and higher for the 24-µm transformer (1.2 dB). These results show that there is a limit on improving the performance of the transformers as transformation ratios are increased using the trace widths of the windings.

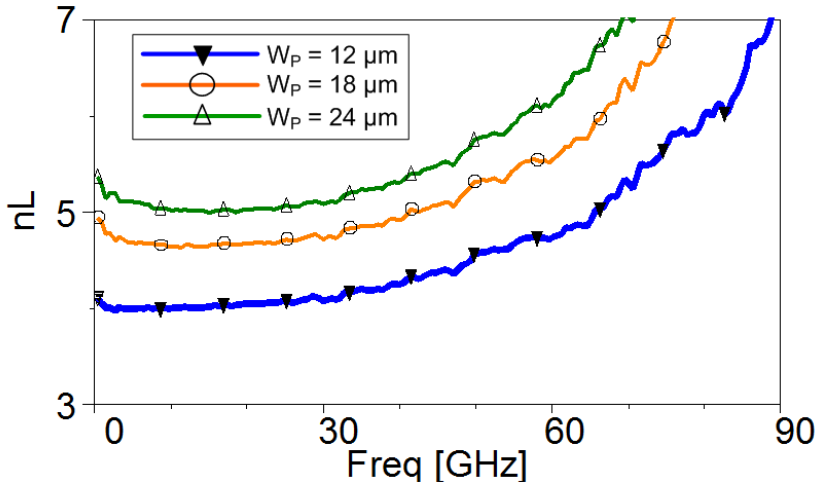


Figure 2-53 Measured inductance ratios of BiCMOS transformers with different primary trace widths.

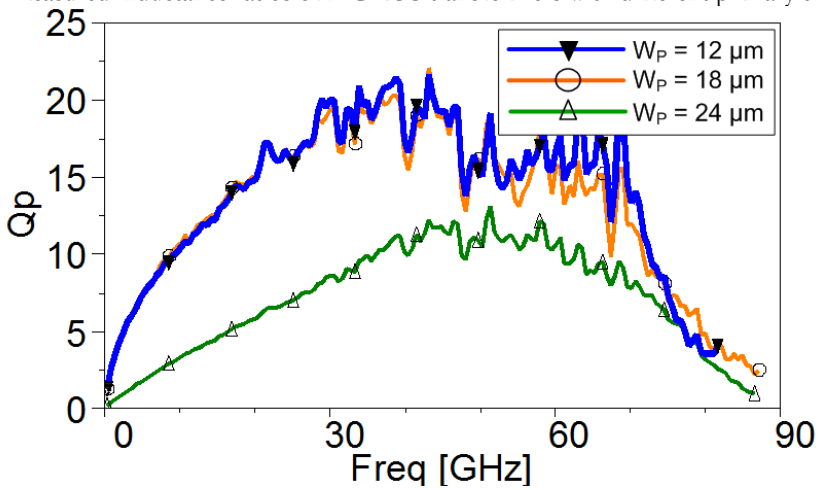


Figure 2-54 Measured quality-factors of BiCMOS transformers with different primary trace widths.

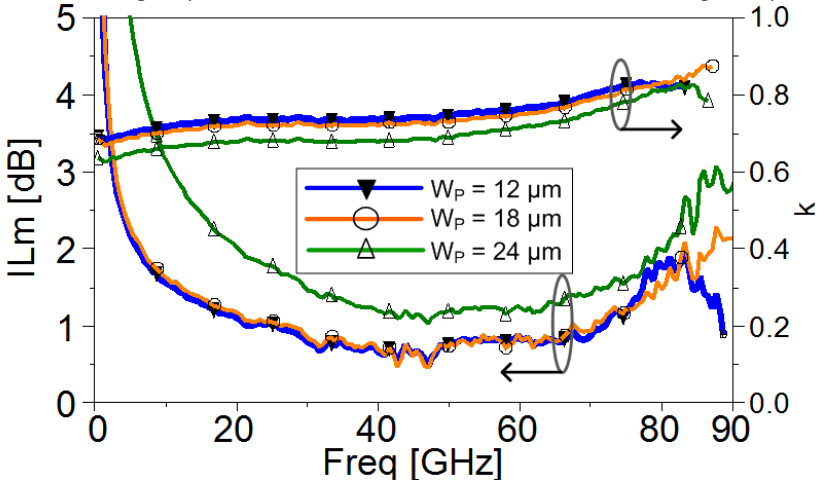
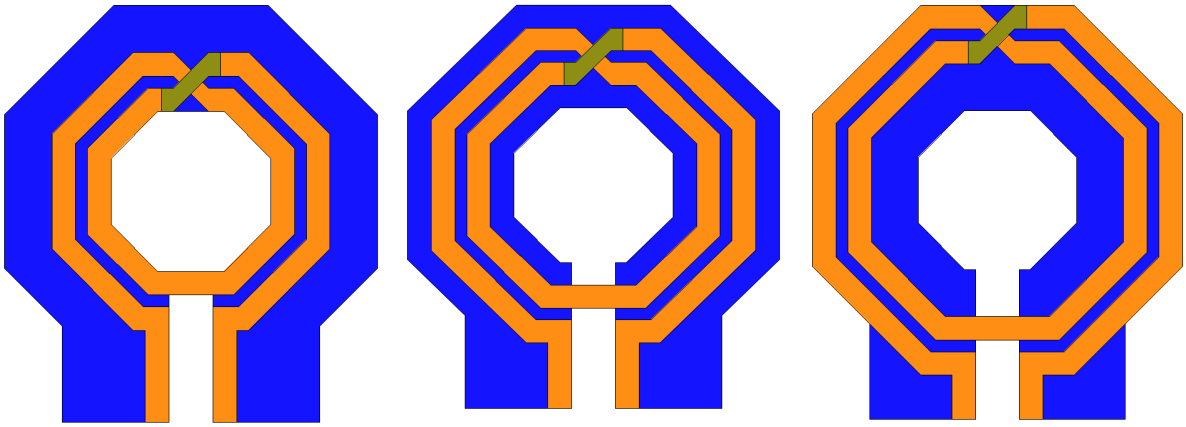


Figure 2-55 Measured coupling coefficient and minimum insertion loss of BiCMOS transformers with different primary trace widths.

6.2 Different diameters

6.2.1 BiCMOS measurement

The impact of designing transformers with different average diameters on the primary and secondary has also been investigated. Since the trace widths and number of turns of the two windings was not the same, the difference on the diameters meant a different relative position of the secondary below the primary. Layouts are presented in Figure 2-56. We have taken advantage of the greater widths allowed for this process, so that the primary traces of the designed transformers are 18-µm wide. The primary diameter D_P is 45 µm, secondary trace width is 4 µm and secondary inter-turn spacing is 2 µm. The first transformer presents both primary and secondary with the same inner diameter (D_S = 37 µm), for the second one the secondary is perfectly centered under the primary (D_S = 45 µm), and for the third one outer diameters coincide (D_S = 53 µm).



(a) (b) (c)

Figure 2-56 Layout of BiCMOS transformers with (a) D_S = 37 µm (D_{Sin} = D_{Pin}), (b) D_S =.45 µm (D_S = D_P), (c) D_S = 53 µm (D_{Sout} = D_{Pout}).

Measured results are shown in Figure 2-57 —Figure 2-59. As expected, it is observed that greater diameters provide higher secondary inductances and hence higher transformation ratios. At 60 GHz, the inductance ratio is equal to 4 for the coincident inner diameters, 5.5 for the average diameters, and 7 for outer diameters. As the influence of this variation is minor in quality-factors and coupling coefficient, we notice an equivalent minimum insertion loss in the three cases, when sufficiently distant from their resonant frequencies.

These results prove that, for the metal width range allowed for this BiCMOS technology, it is possible to achieve a substantial increment on the inductance ratio by defining the relative placement of the secondary under the primary, without impacting its losses.

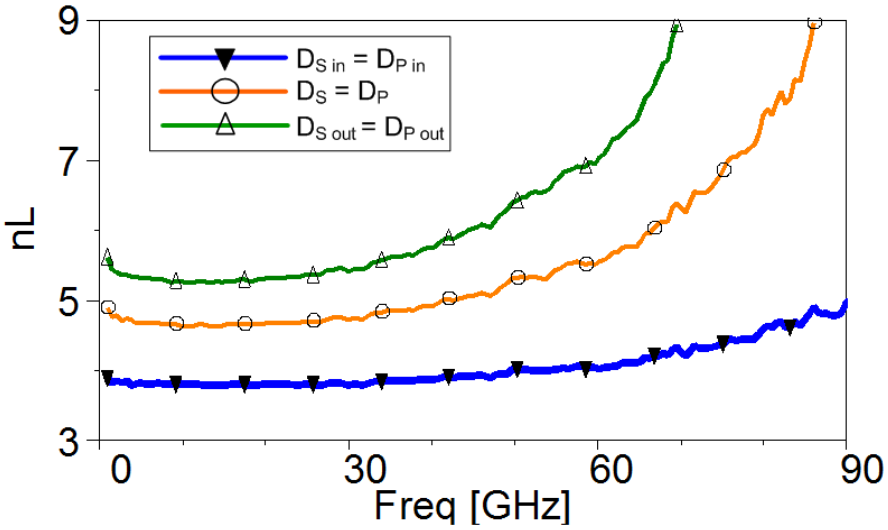


Figure 2-57 Measured inductance ratios of BiCMOS transformers with different secondary diameters.

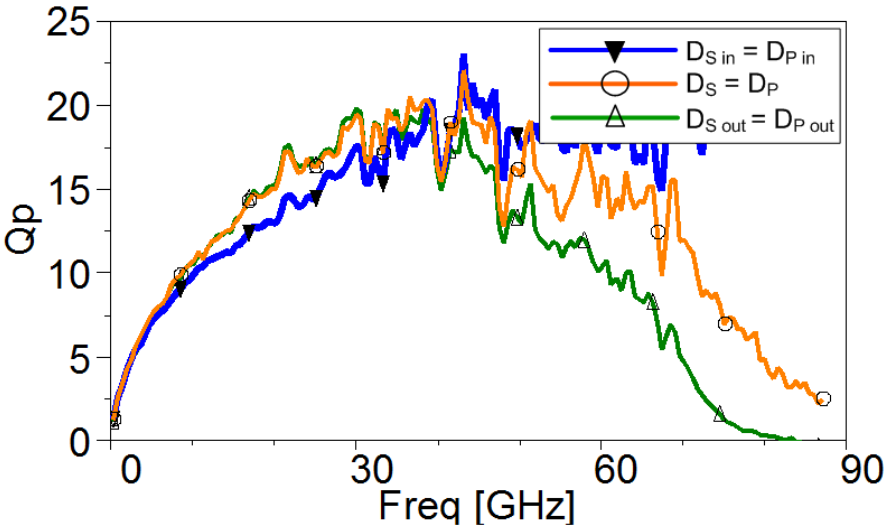


Figure 2-58 Measured quality-factors of BiCMOS transformers with different secondary diameters.

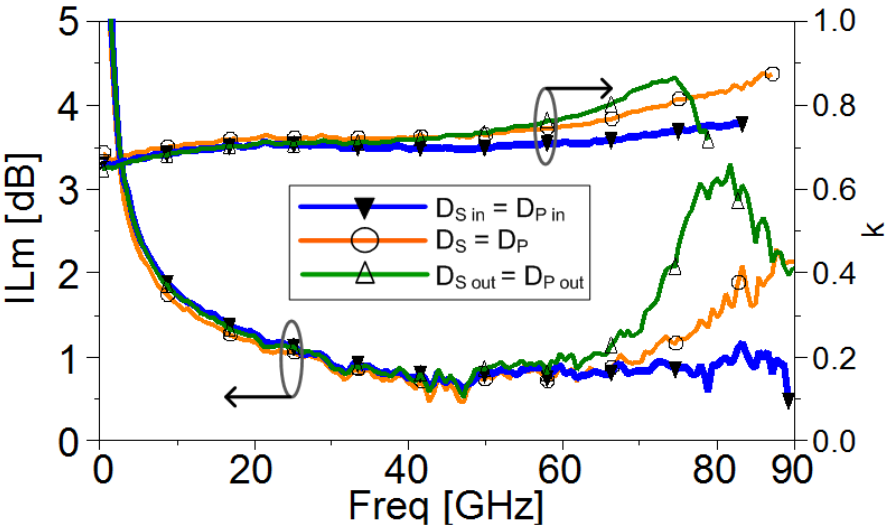


Figure 2-59 Measured coupling coefficient and minimum insertion loss of BiCMOS transformers with different secondary diameters.

7 Conclusion

This chapter focused in two main topics: the characterization and the design of mm-wave transformers. Regarding their characterization, the employed experimental sets were described. De-embedding of pads and leads was discussed, and the open-short technique was adopted for providing the best trade-off between accuracy and area occupation in test chips.

The loss mechanisms of integrated transformers were reviewed and substrate losses along with dissipation on the conductors were shown to be determinant to the performance of the devices. The silicon-based technologies employed in this work were then detailed. Both the 65-nm CMOS and the 130-nm BiCMOS considered processes present similar substrate characteristics but differ significantly in their metal stack. The metals used to construct the transformers on the BiCMOS technology are thicker, more distant from the substrate, and present a thicker dielectric layer between them.

The design of mm-wave transformers was approached in its different aspects. The first considered parameter was the direction in which coupling between windings takes place. It was shown that a vertical coupling is more advantageous, as it provides distinctively better coupling coefficients and minimum insertion loss. Concerning the shape of windings, octagonal transformers were shown to present higher quality-factors than their square counterparts. Moreover, the effect of the position of the feed lines of the two windings was investigated. It was shown that while flipped transformers can achieve lower losses, the non-flipped topology allows a stronger magnetic coupling and a more wideband behavior. It was then demonstrated that, in spite of the weaker coupling, the back-end of BiCMOS9mW provides a better performance for the transformers, thanks to the improved quality-factors.

Two structures which have been reported to mitigate substrate losses and improve the quality-factors of inductors and transformers were presented: patterned ground shields and floating shields. Measurements results indicated that using a PGS on mm-wave transformers is detrimental to their performance, unlike in radiofrequencies. It not only reduces the resonant frequency, but also deteriorates their quality-factors. Floating shields, on the other hand, did not present a considerable impact on the insertion losses. These structures may, however, be optimized so that significant progress is achieved, especially as the use of floating metals in the proximity of transformers is mandatory to comply with metal density rules.

A topology to design transformers with high transformation ratios and compatible with mm-wave constraints was presented as well. This topology consists on defining different trace widths and different diameters for the stacked primaries and secondaries of the transformers. The obtained results proved the proposed transformers effective at providing higher inductance ratios than traditional topologies while reducing insertion losses. Indeed, inductance transformation ratios as high as 7 at 60 GHz have been reported in our investigation.

The conclusions drawn in this study constitute an important base to allow the definition of the best-suited topologies for application in specific integrated circuits. Moreover, the results

obtained throughout this chapter were taken into account in order to guide the development of an electric model for mm-wave transformers.

Chapter 3 : Modeling of mm-wave transformers

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This chapter treats the modeling of mm-wave integrated transformers. Their representation by means of electromagnetic simulations is firstly discussed, highlighting the adopted setup which allows to provide accurate results while consuming a moderate amount of computational resources. Their behavior is then modeled through a lumped-element electric circuit. The model presents a 2-π topology and equations to evaluate the value of the totality of its components. These equations depend on both technological and geometric characteristics of the transformer. The model is validated through experimental data of a set of 2–port 65-nm CMOS and 130-nm BiCMOS transformers. A close agreement is shown for both S-parameter and inductance values up to 110 GHz. Moreover, good accuracy is obtained for the simulations of transformers in a 4-port configuration. Finally, as the model was validated, a parametric cell was implemented in Cadence Virtuoso associating the electric model to the automatically generated layout of the transformer.

1 Introduction

Transformers have emerged as very useful components in mm-wave IC design. Nevertheless, in order to allow a design flow as effective as possible, it is essential that accurate models be available to the IC designer. One approach usually adopted is the electromagnetic simulation of the transformer and use of its resulting scattering parameters within the circuit in which it is supposed to be included. The drawback of such strategy is that EM simulations can be reasonably time-consuming and demand a certain amount of knowledge about their setup in order to provide reliable results. Furthermore, in some cases, especially for transient simulations, circuit simulators may not be able to properly handle the S-parameters, causing simulations to diverge.

Hence, a more efficient approach consists in employing the EM simulations for verification rather than at early circuit design stages. In this context, an electric equivalent circuit should be developed in order to model the behavior of the transformers.

2 Electromagnetic Simulation

Electromagnetic simulators constitute a powerful tool to evaluate the behavior of mm-wave passive components. They are able to provide an accurate representation of devices for a multitude of forms and technological properties.

EM simulators differ on the field calculation methods which have an implication on how the tridimensional objects are taken into account. Two classes of simulators are prominent for the representation of integrated transformers: planar 3-D (frequently referred to as 2.5-D) and full 3-D. While planar 3-D simulators are reputed to provide satisfactory results while consuming less computational resources, the use of full 3-D tools may allow a more accurate representation

regarding vertical current distributions. For the modeling purposes of this work, a full 3-D representation was therefore preferred.

Among the available fully tridimensional commercial tools, *Ansoft HFSS* [ANS10] stands out as a precise and reliable EM simulator. Its operation is based on the finite element method. It divides the modeled objects into a number of tetrahedral forms and computes electromagnetic fields at each of their vertices. This meshing operation, performed at a specific frequency, is then refined, increasing density in regions where larger field errors are obtained, until convergence criteria are met. Once meshing of the structure is complete, fields are calculated for a number of frequency points and interpolated within the totality of the specified band. Scattering parameters are then obtained considering the amount of transmitted and reflected signals at those frequencies.

Depending on the size and complexity of the simulated structures, such calculations may nevertheless require a considerable amount of computational resources and simulation time. An efficient use of these tools must therefore include adequate simplifications of the 3-D simulation models.

Figure 3-1 illustrates the EM simulation model of an integrated transformer. Such model should include the silicon substrate, dielectric and metallic layers. Each material constituting

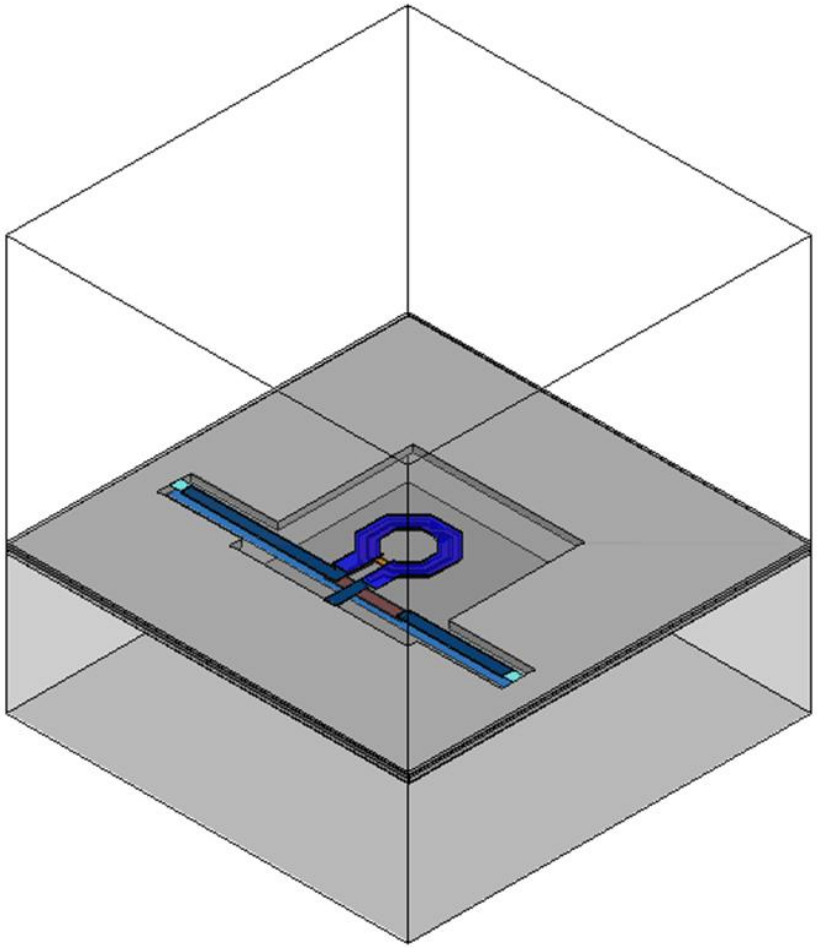


Figure 3-1 Tridimensional EM simulation model.

those objects is described in terms of properties such as dielectric permittivity and loss tangents, magnetic permeability and electrical resistivity. Physically, these characteristics are known to present a certain dependence on frequency, especially when mm-waves are concerned. In our study, nevertheless, these material properties are assumed constant over frequency.

One simplification which is arguably the most critical in this context concerns the dielectric stack. As copper deposition is implemented through a damascene process in the adopted technologies, the low-permittivity dielectric layers are intertwined with the respective barrier levels. These along with additional silicon nitride layers constitute a rather complex stack which accounts significantly for simulation time. It is thus clearly desirable to employ a simplified dielectric profile in EM simulations. On the other hand, if this simplification is not properly performed, they may yield a significant deviation from the correct results. The adopted approach consisted hence in considering two equivalent dielectric layers between the substrate and the top metal in the back-end, as illustrated in Figure 3-2. Considering the stacked topology adopted for the integrated transformers, one of the dielectric layers is defined to comprise the region between the two windings (i.e., the two top copper levels), which is where inductive and capacitive coupling between primary and secondary takes place and the other accounts mostly for coupling between secondary and substrate. The equivalent dielectric permittivities ε_{eq} of each two consecutive dielectrics are then computed using equation (3-1), where t represents the thickness of the corresponding layer [KRA77].

$$\varepsilon_{eq} = \left[\sqrt{\varepsilon_n} + \frac{t_{n-1}}{t_{n-1} + t_n} \cdot \left(\sqrt{\varepsilon_{n-1}} - \sqrt{\varepsilon_n} \right) \right]^2 \tag{3-1}$$

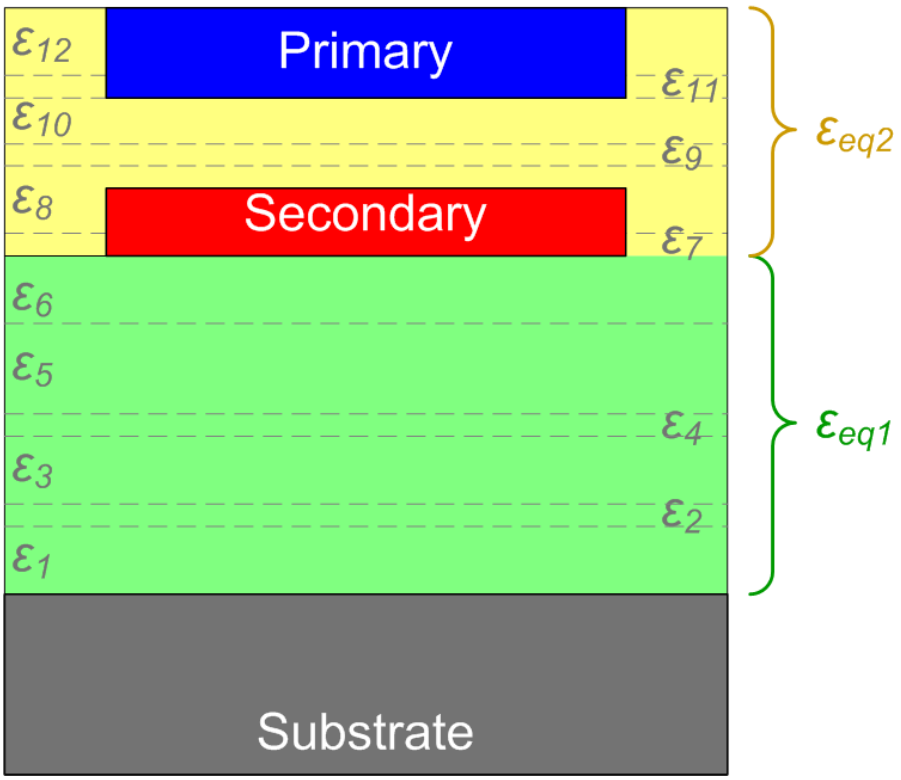
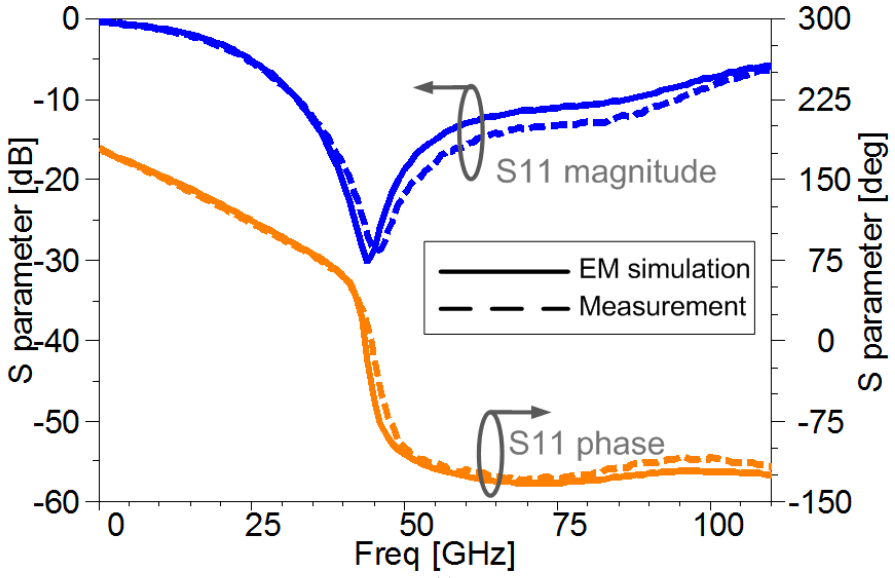


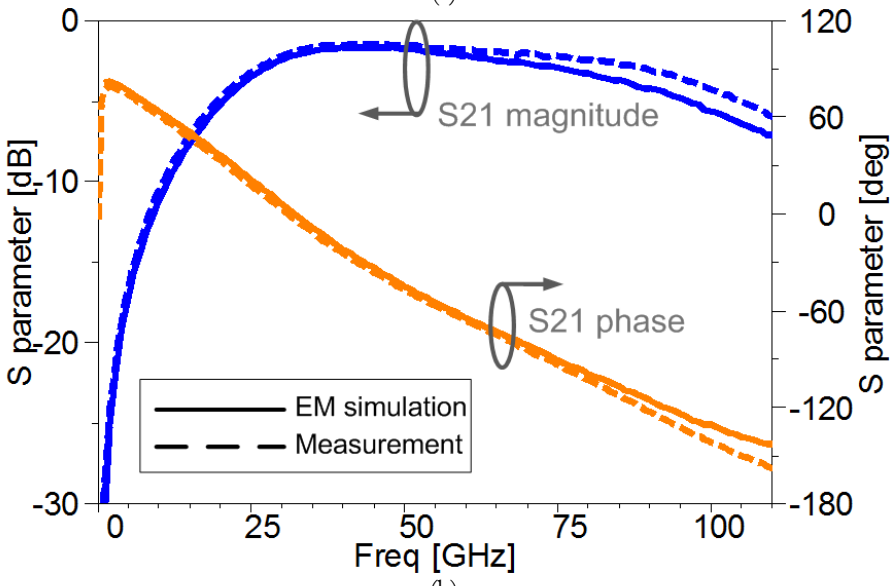
Figure 3-2 Physical and simplified dielectric stacks for a generic technology.

Another relevant approximation regards the constitution of ground planes surrounding the transformers. In the actual realization they are constituted by several different metal layers, which are interconnected through vias. Moreover, in order to comply with metal density requirements of the technologies, these planes are patterned. In the simulation model, though, all metals were merged into a single solid block

Figure 3-3 and Figure 3-4 compare EM simulation results to the measured S-parameters for one transformer in each of the employed technologies. In these simulations meshing was performed at 60 GHz and electromagnetic fields were calculated in the range between 1 and 110 GHz. A very close agreement is observed for both magnitude and phase results. The same degree of accuracy was verified for all of the measured transformers. Those results corroborate the reliability of the adopted model and simulation setups.



(a)



(b)

Figure 3-3 Comparison between measured and EM simulated S-parameters for a 65-nm CMOS transformer.

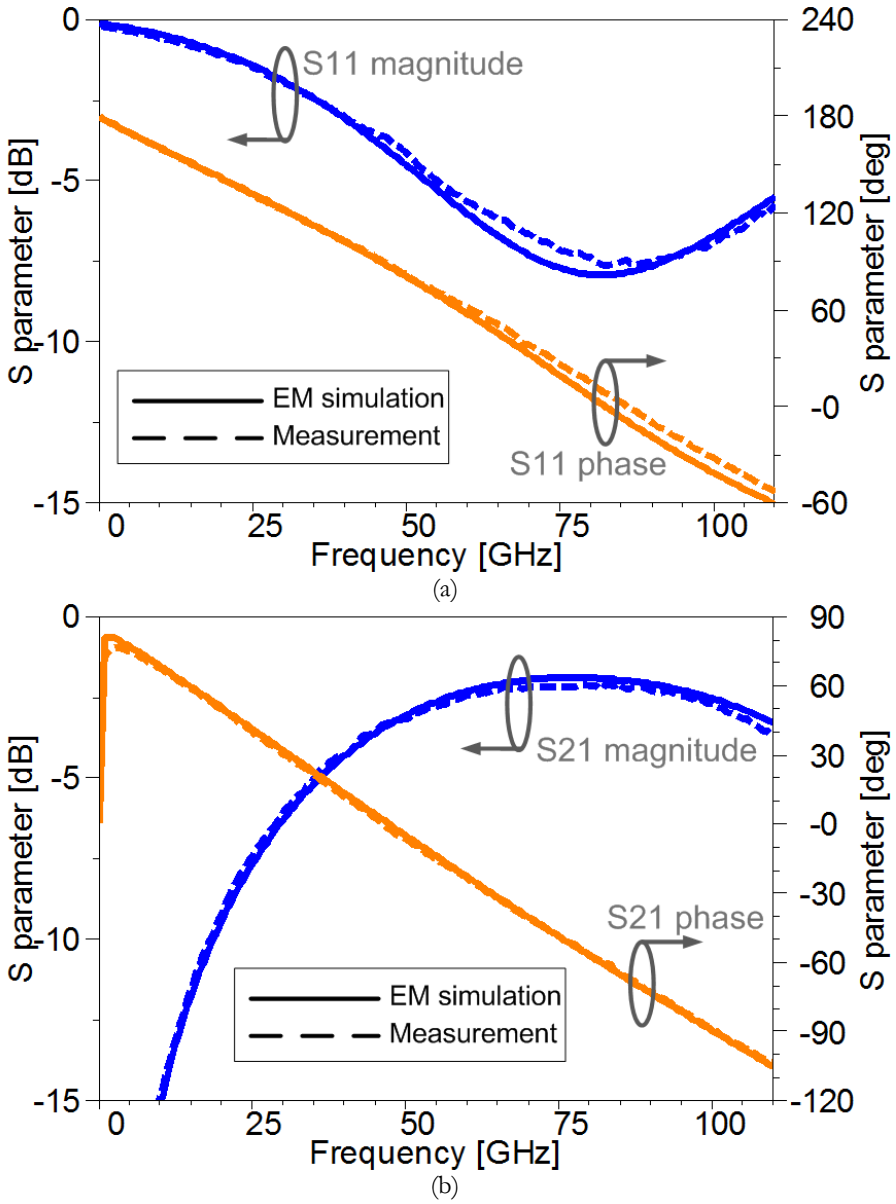


Figure 3-4 Comparison between measured and EM simulated S-parameters for a BiCMOS9mW transformer.

3 Electrical Model

For RF transformers, there is a number of models previously reported in the literature. [ROT06] presents an electrical model which takes into account the transformer and its parasitics, while [BIO06] and [WAN09] also include analytical expressions to compute some of its components. Likewise, [GHA07] presents an even more comprehensive model which contains equations to calculate each one of its elements. This model is shown to be scalable to geometric dimensions and different technologies.

In spite of their accuracy, these models are specific to their respective topologies and hence cannot be directly employed for mm-wave transformers. For instance, traditional RF transformers contain patterned ground shields between metal conductors and the silicon

substrate [YUE98, NG02], which were considered on the definition of their models. However, as presented in Chapter 2, such shields have been shown to be detrimental to the performances of mm-wave structures. Thus, it is crucial that models especially designed for mm-wave components be used. [BRI10] describes such a model, but it cannot predict the behavior of the transformers since it is solely based on the extraction of the elements' values from measured or simulated data. [CHO09] goes one step further on combining into their lumped-element model both analytical equations and fitting coefficients derived from simulation.

In this work we introduce a complete electrical model to represent mm-wave transformers. It presents a traditional 2-π topology and contains closed-form physics-related equations for all of its elements. This model is supposed to be predictive and supply an accurate and broadband representation of mm-wave transformers with equations relying uniquely on their different geometric and technologic parameters.

Technological parameters must be carefully considered in the development of the model, so that it can be valid for a number of different processes. A list of the technological parameters which are considered in the proposed model is presented in Table 3-1 and illustrated in Figure 3-5. The considered geometric parameters, which are derived from the dimensions in Figure 3-6, are summarized in Table 3-2.

Table 3-1 Transformer technological parameters

h_P	distance between the substrate and the primary lower face
h_S	distance between the substrate and the secondary lower face
t_P	primary thickness
t_S	secondary thickness
t_{Si}	substrate thickness
d_{PS}	distance between the primary lower face and the secondary upper face
ε_{oxP}	equivalent relative permittivity of the dielectric between substrate and primary
ε_{oxS}	equivalent relative permittivity of the dielectric between substrate and secondary
ε_{oxPS}	equivalent relative permittivity of the dielectric between primary and secondary
ε_{Si}	equivalent relative permittivity of the substrate
ρ_{MP}	primary metal resistivity
ρ_{MS}	secondary metal resistivity
ρ_{Si}	substrate resistivity

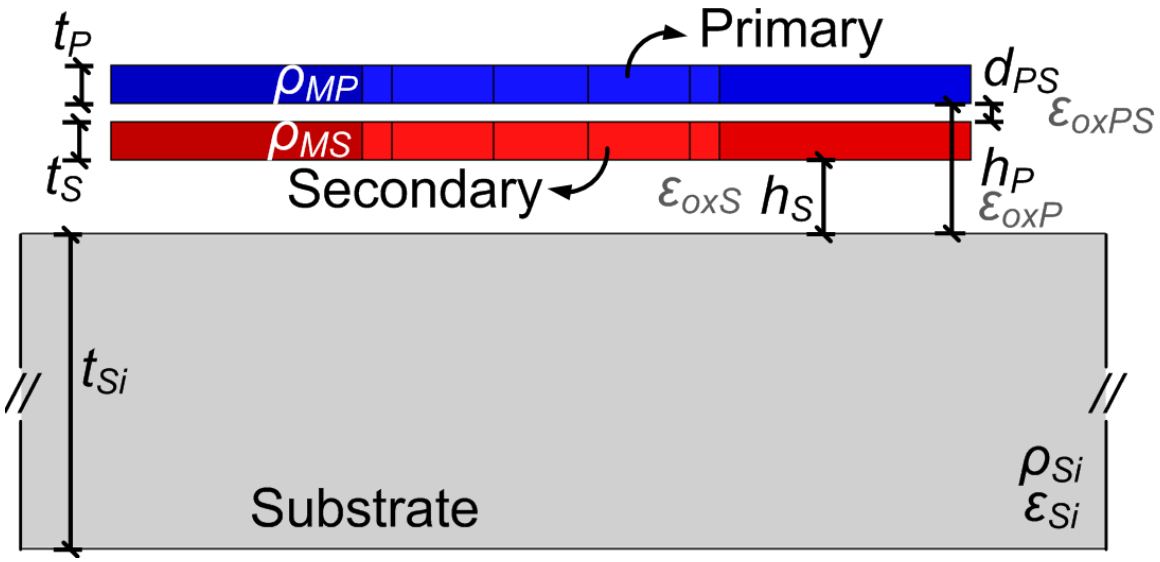


Figure 3-5 Technological parameters of the stacked transformer.

Table 3-2 Transformer geometric parameters

ℓ_P	primary length
ℓ_S	secondary length
W_P	primary trace width
W_S	secondary trace width
N_S	secondary number of turns
ℓ_{Sn1}	length of secondary outer turn
ℓ_{Sn2}	length of secondary inner turn
A_P	primary area
A_S	secondary area
A_{PS}	overlap area between primary and secondary

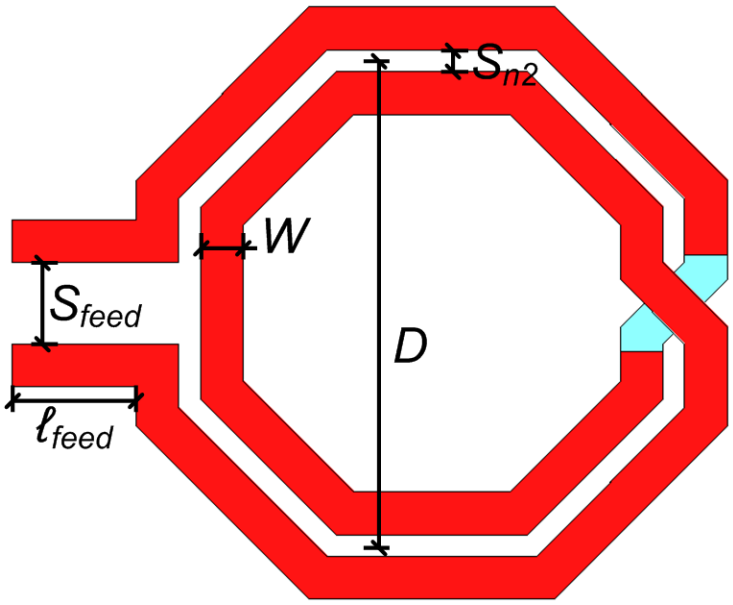


Figure 3-6 Geometric parameters of the windings.

3.1 Model topology

The architecture of the proposed model is depicted in Figure 3-7. It consists of a 4-port 2-π representation [KEH01] containing three groups of elements: the series branches, the substrate branches and the coupling elements. Each of the series branches includes a self inductance and a resistance, representing the inductive and resistive properties of the conductor constituting the winding. The substrate branches correspond to a capacitance C_{ox} in series with a parallel combination of a capacitance C_{sub} and a resistance R_{sub}. C_{ox} accounts for the electric coupling between the coil and the top of the substrate, whereas C_{sub} and R_{sub} represent the capacitance and resistance within the silicon substrate. Whereas series and substrate branches represent the behavior of the individual coils, the mutual coupling M and the capacitances C_{PS} represent the respective magnetic and electric interaction between them.

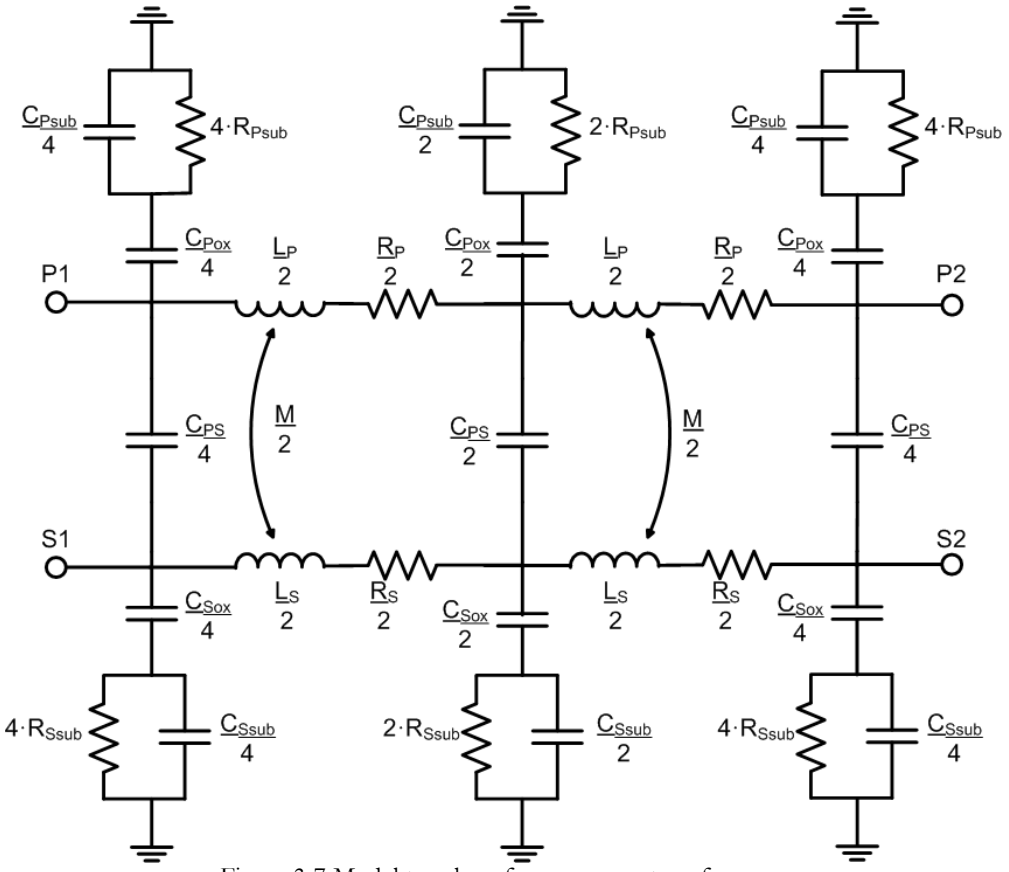


Figure 3-7 Model topology for mm-wave transformers.

3.2 Fundamental equations

The calculation of most of the model components values directly depends on basic expressions for capacitances, self inductances, and mutual inductances of simple conductors. Those are discussed hereafter.

3.2.1 Self inductance

The inductance of a circuit can be fundamentally defined as the ratio between its corresponding magnetic flux and flowing current. When particularized for single conductors, a number of different expressions have been proposed to address specific geometries.

The expression adopted in this work to compute self inductances of rectangular conductors is adapted from the one proposed in [GRO46]. The expression is derived from a formula to calculate the mutual inductance between filaments, for which the term representing the distance between them is replaced by the geometric mean distance (*GMD*) within the section of the conductor. Furthermore, it is considered that the conductor length ℓ is much greater than the other dimensions *W* and *t*. As the magnetic permeability of the metal conductors in our implementations is approximated to the permeability of free space μ_0, the equation is solely dependent on the physical dimensions of the conductor, as shown in (3-2) and (3-3).

$$Ind(\ell, W, t) = \frac{0.42 \cdot \mu_0}{\pi} \cdot \ell \cdot \left[\ln\left(\frac{2 \cdot \ell}{GMD(W,t)} \right) + \frac{GMD(W,t)}{\ell} - 1 \right] \tag{3-2}$$

$$GMD(W,t) = 0.2235 \cdot (W + t) \tag{3-3}$$

3.2.2 Mutual inductance

Mutual inductance arises when the magnetic flux generated by time-varying current in one conductor is intercepted by another conductor, inducing a current within the latter. This relation is reciprocal so that the same ratio between intercepted flux and induced current will be verified for both conductors.

In this model, the mutual inductance calculation is based on the method proposed by [ZHO03], which represents the mutual inductance between two conductors as a weighted sum of self inductances. It is dependent on the physical dimensions of the conductors as well as on their relative position. Hence, this formula can be applied regardless of whether the conductors are aligned on the same plane. In our calculations, nevertheless, the same equivalent length for the coupling is considered, as done in [UNT08].

The formulae for the mutual inductance between two conductors P and Q, whose cross-sections are shown in Figure 3-8, are presented in (3-4) – (3-6).

$$Mut(P,Q) = \frac{1}{4 \cdot W_1 \cdot t_1 \cdot W_2 \cdot t_2} \left[\sum_{i,j,k,l=0}^{1} (-1)^{i+j+k+l} \cdot A_{ijkl}^2 \cdot L_{ijkl} \right] \tag{3-4}$$

$$A_{ijkl}^2 = \left[x(Q_{kl}) - x(P_{ij}) \right]^2 \cdot \left[y(Q_{kl}) - y(P_{ij}) \right]^2 \tag{3-5}$$

$$L_{ijkl} = Ind\left(\ell, W = \left| x(Q_{kl}) - x(P_{ij}) \right|, t = \left| y(Q_{kl}) - y(P_{ij}) \right| \right) \tag{3-6}$$

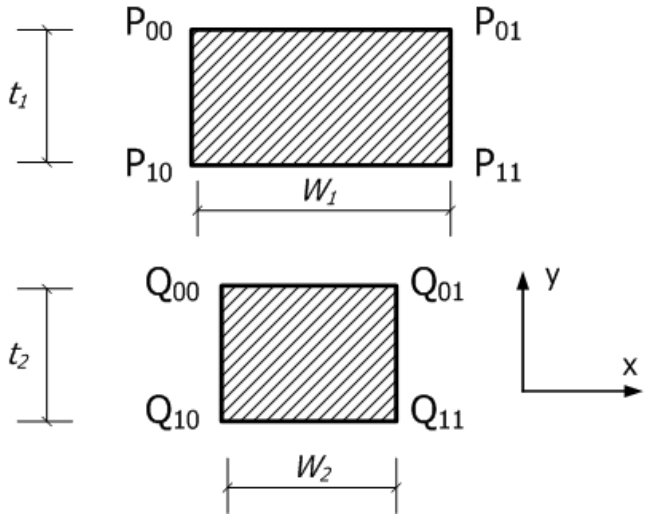


Figure 3-8 Conductors coordinates for mutual inductance calculation.

3.2.3 Capacitance

For the capacitance calculation, two expressions are considered, one for the parallel plate capacitance and another for the fringing capacitances. As illustrated in Figure 3-9, the parallel plate expression accounts only for the perpendicular electric field between two surfaces and hence does not consider the thickness of the objects. For this reason, fringing capacitances are also calculated, so that the electric field originated in the edges and lateral surfaces of the objects are also taken into account.

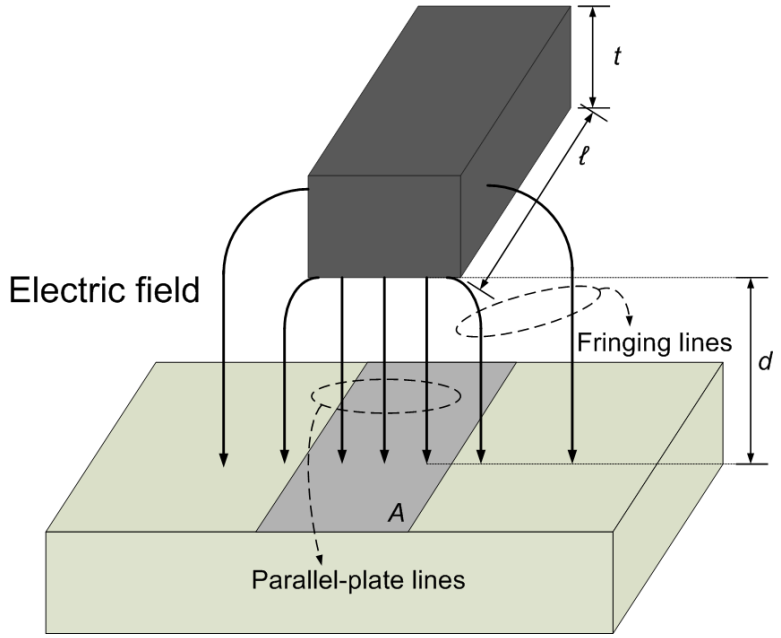


Figure 3-9 Electric coupling configuration: field lines for parallel-plate and fringing capacitances.

Equation (3-7) presents the classical expression for parallel plate capacitances, which is dependent on the permittivity of the dielectric between plates ε_{diel}, their area A and the distance between them d.

$$Cap_{par}(\varepsilon_{diel}, A, d) = \frac{\varepsilon_0 \cdot \varepsilon_{diel} \cdot A}{d} \tag{3-7}$$

The expression (3-8) calculates then the fringing capacitances in function of ε_{diel}, the distance d, and the dimensions ℓ and t, as proposed in [EO93].

$$Cap_{fr}(\varepsilon_{diel},\ell,t,d)=\frac{2\pi\cdot\varepsilon_0\cdot\varepsilon_{diel}\cdot\ell}{\ln\left[1+\frac{2d}{t}+\sqrt{\frac{2d}{t}\left(\frac{2d}{t}+2\right)}\right]}. \quad (3\text{-}8)$$

3.3 Component calculation

In our 2-π model, there is symmetry between both π portions. Hence the value of the components represented in the left and in the right portion of the model schematic will be the same, as shows Figure 3-7. The equations to evaluate the model components are presented hereafter. Additionally, the weighting coefficients present in some of these equations are summarized in Table 3-3.

Table 3-3 Model weighting factors

	k_{Rac}	k_{Cap}	k_M
Non-flipped topology	**175.10^3**	**$0.52\cdot(4\text{-}1.5\cdot N_S)$**	**0.9**
Flipped topology	**90.10^3**	**$1.2\cdot(4\text{-}1.5\cdot N_S)$**	**0.675**

3.3.1 Series branches

The series branches are composed by an inductance and a resistance each. The calculation of primary inductances is performed as indicated in (3-9). It considers the self inductance of the whole primary length and subtracts the mutual inductance of the opposite sides and feed lines of the winding as shown in Figure 3-10.

$$L_P = Ind(\ell_P) - Mut(feed_{\text{int}P}) - Mut(d_{\text{int}P}) \quad (3\text{-}9)$$

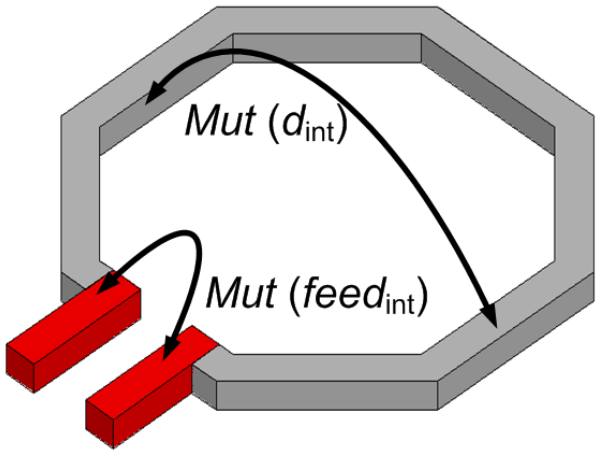


Figure 3-10 Negative mutual coupling between opposite sides (d_{int}) and feed lines ($feed_{int}$) in a winding.

For the secondary inductance, the procedure is the same if it is constituted by a single turn. In case it presents two turns, on the other hand, the self inductance of each turn (*N1* and *N2*) is calculated separately and then the mutual inductance between them is added, as depicted

in Figure 3-11. The negative coupling between opposite sides and feed lines is also considered. Thus:

for $N_S = 1$:

$$L_S = Ind(\ell_S) - Mut(feed_{intS}) - Mut(d_{intS}) \tag{3-10}$$

for $N_S = 2$:

$$L_S = Ind(N1) + Ind(N2) + Mut(N1, N2) - Mut(feed_{intS}) - Mut(d_{intS}). \tag{3-11}$$

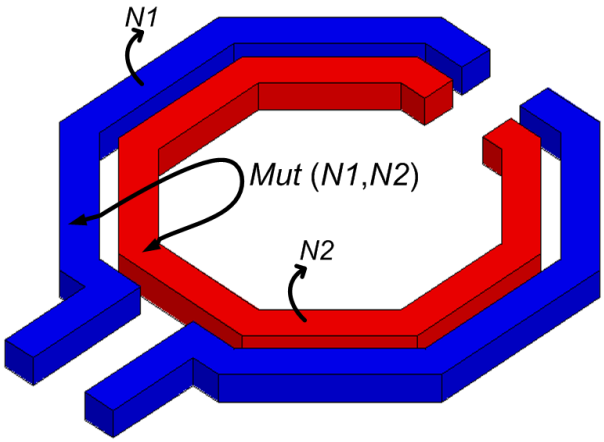


Figure 3-11 Illustration of the inductance calculation for 2-turn windings.

Concerning the series resistances, they are split into DC and AC components. The DC component is simply calculated in function of the conductor dimensions and resistivity. The AC component, on the other hand, is a function of frequency and takes into consideration the influence of skin effect, by including the metal skin depths δ into the calculation.

$$R_P = R_{Pdc} + R_{Pac} \tag{3-12}$$

$$R_S = R_{Sdc} + R_{Sac} \tag{3-13}$$

$$R_{Pdc} = \frac{\rho_{MP} \cdot \ell_P}{W_P \cdot t_P} \tag{3-14}$$

$$R_{Sdc} = \frac{\rho_{MS} \cdot \ell_S}{W_S \cdot t_S} \tag{3-15}$$

$$R_{Pac} = \frac{k_{Rac} \cdot \rho_{MP} \cdot \ell_P}{\left(1 + \frac{t_P}{W_P}\right) \cdot \delta_P \cdot \left[1 - \exp\left(\frac{-t_P}{\delta_P}\right)\right]} \tag{3-16}$$

$$R_{Sac} = \frac{k_{Rac} \cdot \rho_{MS} \cdot \ell_S}{\left(1 + \frac{t_S}{W_S}\right) \cdot \delta_S \cdot \left[1 - \exp\left(\frac{-t_S}{\delta_S}\right)\right]} \tag{3-17}$$

$$\delta_P = \sqrt{\frac{\rho_{MP}}{\pi \cdot \mu_0 \cdot \mu_{MP} \cdot f}} \tag{3-18}$$

$$\delta_S = \sqrt{\frac{\rho_{MS}}{\pi \cdot \mu_0 \cdot \mu_{MS} \cdot f}} \tag{3-19}$$

3.3.2 Substrate branches

Each substrate branch contains 3 elements, the capacitances C_{ox} and C_{sub}, and the resistance R_{sub}. The evaluation of C_{ox} includes a parallel-plate and a fringing capacitance between each winding and the top of the substrate. Since the secondary is placed beneath the primary, only the primary surface which does not overlap the secondary is considered for C_{Pox}. The resistance R_{sub} is determined as a function of the substrate resistivity and the dimensions of the conductors and the substrate [CAO03], whereas C_{sub} is calculated considering the relaxation time constant of the silicon substrate [DIC05].

$$C_{Pox} = k_{Cap} \cdot \left[Cap_{par}\left(\varepsilon_{oxP}, A = A_P - A_{PS}, d = h_P\right) + \frac{A_P - A_{PS}}{A_P} \cdot Cap_{fr}\left(\varepsilon_{oxP}, \ell_P, d = h_P, t_P\right) \right] \tag{3-20}$$

$$C_{Sox} = k_{Cap} \cdot \left[Cap_{par}\left(\varepsilon_{oxS}, A_S, d = h_S\right) + Cap_{fr}\left(\varepsilon_{oxS}, \ell_S, d = h_S, t_S\right) \right] \tag{3-21}$$

$$R_{Psub} = \frac{3 \cdot \rho_{Si} \cdot W_P}{\ell_P \cdot t_{Si}} \tag{3-22}$$

$$R_{Ssub} = \frac{3 \cdot \rho_{Si} \cdot W_S}{\ell_S \cdot t_{Si}} \tag{3-23}$$

$$C_{Psub} = \frac{\varepsilon_{Si} \cdot \varepsilon_0 \cdot \rho_{Si}}{R_{Psub}} \tag{3-24}$$

$$C_{Ssub} = \frac{\varepsilon_{Si} \cdot \varepsilon_0 \cdot \rho_{Si}}{R_{Ssub}} \tag{3-25}$$

3.3.3 Coupling elements

The magnetic and electric coupling between coils is modeled through a mutual inductance M and the capacitance C_{PS}. In the case of a 2-turn secondary, mutual coupling between each turn and the primary is evaluated independently and then added. For C_{PS}, due to the relatively small distance between windings, only the parallel-plate component of this capacitance is considered.

$$C_{PS} = k_{Cap} \cdot \left[Cap_{par}\left(\varepsilon_{oxPS}, A_{PS}, d_{PS}\right) \right] \tag{3-26}$$

for $N_S = 1$:

$$M = k_M \cdot Mut\left(Primary, Secondary\right) \tag{3-27}$$

for $N_S = 2$:

$$M = k_M \cdot \left[Mut(Primary, SecondaryN1) + Mut(Primary, SecondaryN2) \right] \quad (3\text{-}28).$$

3.4 Model validation

3.4.1 2-port measurements

The proposed model has been validated through the measurement of mm-wave transformers integrated in 65-nm CMOS and 130-nm BiCMOS technologies. Those transformers were implemented in a 2-port configuration, as discussed in Chapter 2. The comparison is effectuated through their S-parameters, as well as their inductances and coupling coefficients.

The first comparison between measurement results and the developed model is here presented in Figure 3-12 —Figure 3-14. It refers to a transformer with symmetric primary and secondary in 65-nm CMOS. Each winding presents a single turn, with a 60-µm average diameter and a 4-µm trace width.

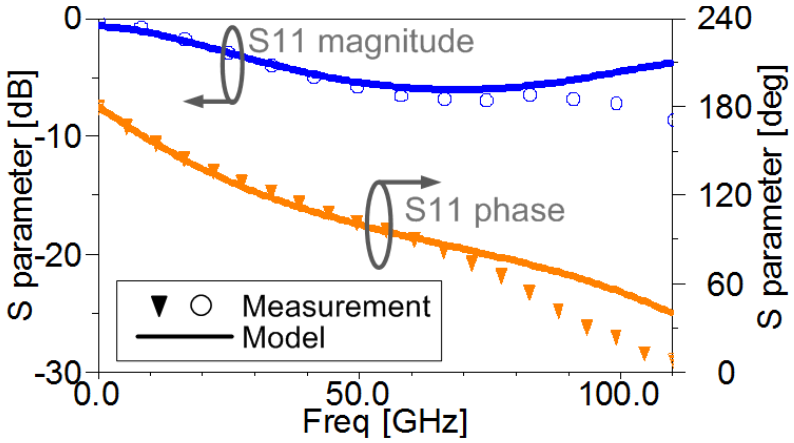


Figure 3-12 Measured and modeled magnitude and phase values of parameter S11 for a transformer with a 60-µm diameter and a 4-µm trace width in the 65-nm CMOS technology.

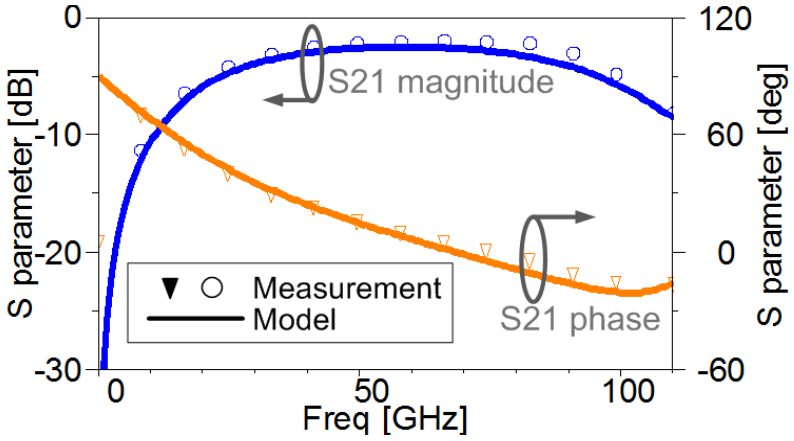


Figure 3-13 Measured and modeled magnitude and phase values of parameter S21 for a transformer with a 60-µm diameter and a 4-µm trace width in the 65-nm CMOS technology.

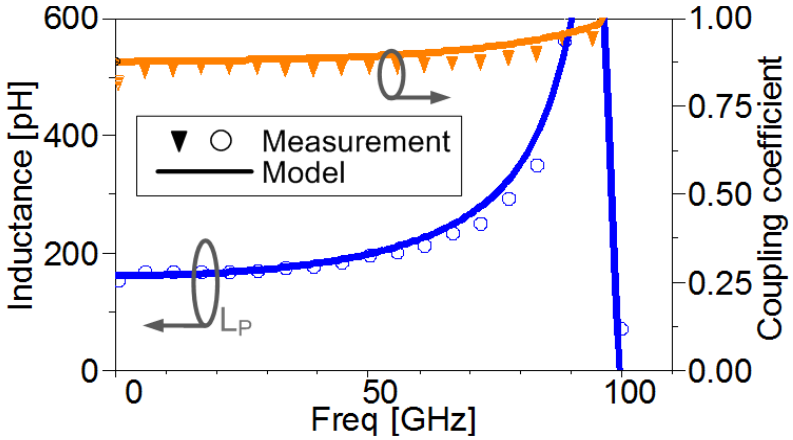


Figure 3-14 Measured and modeled values for the primary inductance and coupling coefficient of a transformer with a 60-µm diameter and a 4-µm trace width in the 65-nm CMOS technology.

While still considering a 1:1 transformer, we evaluate the scalability of the model in terms of geometric dimensions. Figure 3-15 — Figure 3-17 present therefore the measured and modeled S-parameters, inductances and coupling coefficient of a 65-nm CMOS transformer with a 60-µm diameter and a 12-µm trace width.

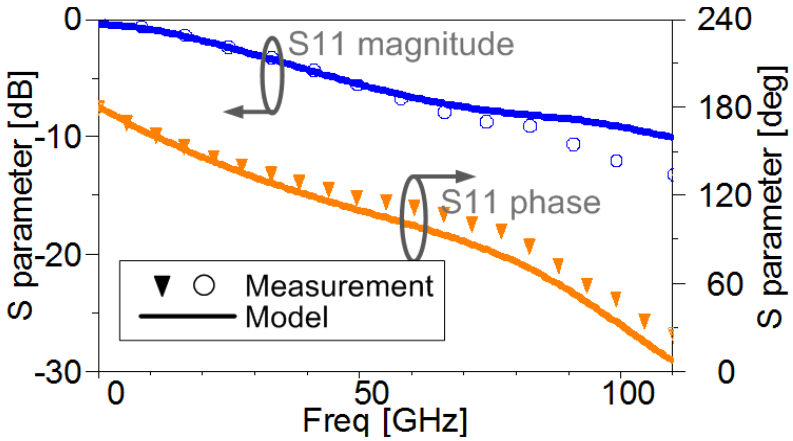


Figure 3-15 Measured and modeled magnitude and phase values of parameter S11 for a transformer with a 60-µm diameter and a 12-µm trace width in the 65-nm CMOS technology.

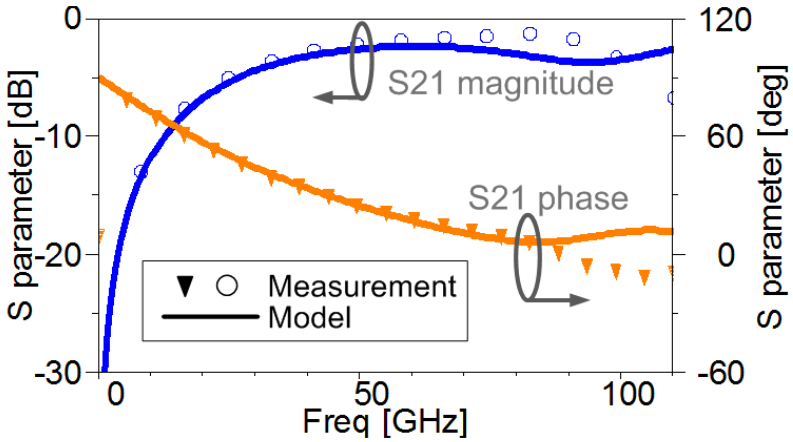


Figure 3-16 Measured and modeled magnitude and phase values of parameter S21 for a transformer with a 60-µm diameter and a 4-µm trace width in the 65-nm CMOS technology.

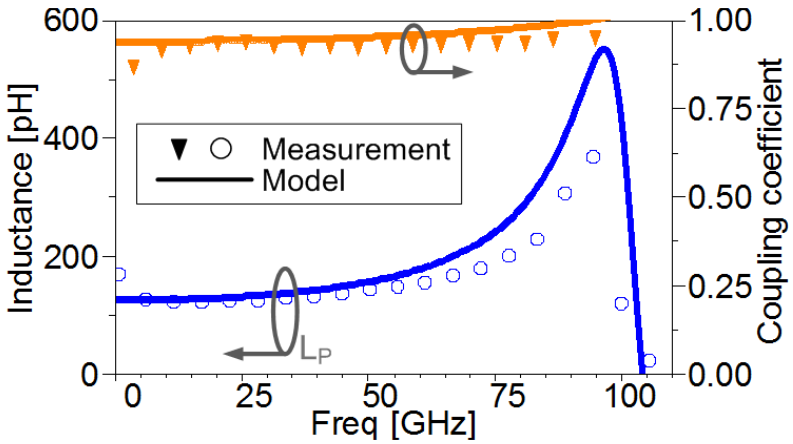


Figure 3-17 Measured and modeled values for the primary inductance and coupling coefficient of a transformer with a 60-µm diameter and a 12-µm trace width in the 65-nm CMOS technology.

In Figure 3-18 — Figure 3-20, the geometric scalability of the model is further verified. Additionally, to a different diameter (45 µm for both primary and secondary) we consider in this comparison, a different topology, with a 2-turn secondary. The trace widths are 12 µm for the primary and 4 µm for the secondary.

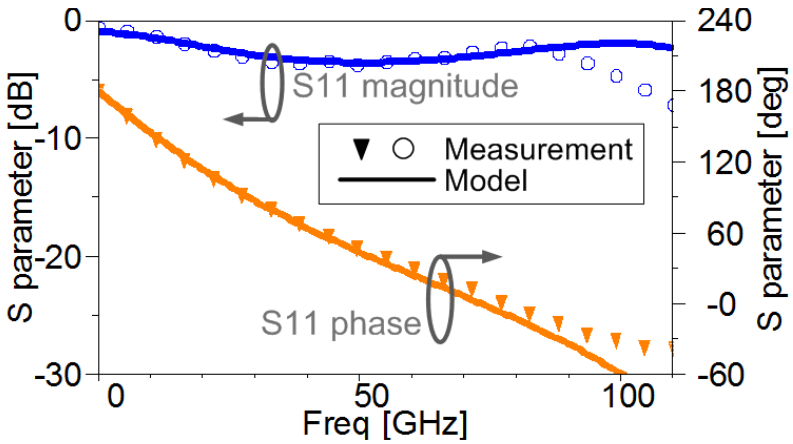


Figure 3-18 Measured and modeled magnitude and phase values of parameter S11 for a 65-nm CMOS transformer. The primary presents a 42-µm diameter and a 12-µm trace width, and the secondary presents 2 turns, a 42-µm diameter and a 4-µm trace width

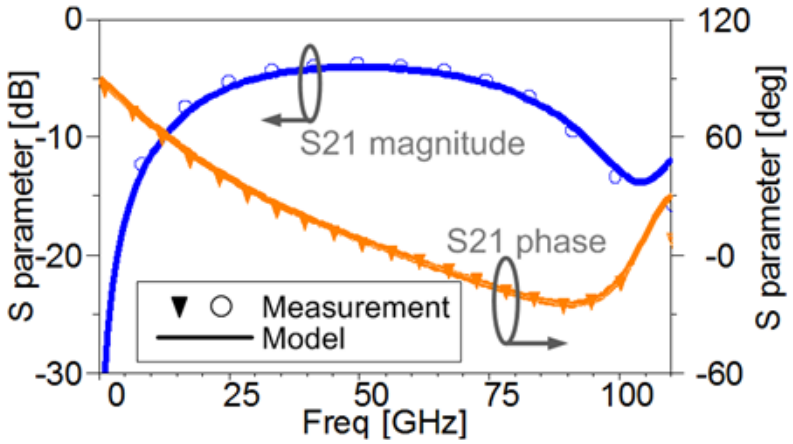


Figure 3-19 Measured and modeled magnitude and phase values of parameter S21 for a 65-nm CMOS transformer. The primary presents a 42-µm diameter and a 12-µm trace width, and the secondary presents 2 turns, a 42-µm diameter and a 4-µm trace width.

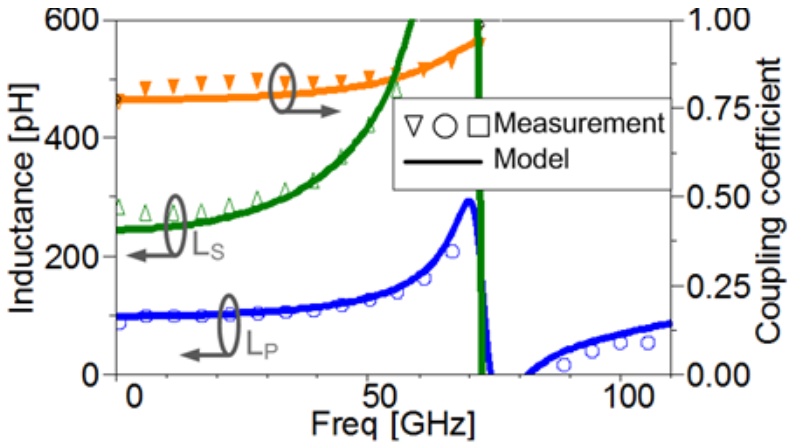


Figure 3-20 Measured and modeled inductances and coupling coefficient for a 65-nm CMOS transformer. The primary presents a 42-µm diameter and a 12-µm trace width, and the secondary presents 2 turns, a 42-µm diameter and a 4-µm trace width.

In addition to the geometric scalability, the technologic scalability is an important asset of the proposed model. Hence, the measured parameters of BiCMOS9mW transformers have been compared to model simulation as well. Figure 3-21 —Figure 3-23 present therefore the obtained results for a BiCMOS transformer presenting a single-turn primary with a 45-µm diameter and 18-µm trace width, and a 2-turn secondary with a 37-µm diameter and a 4-µm trace width.

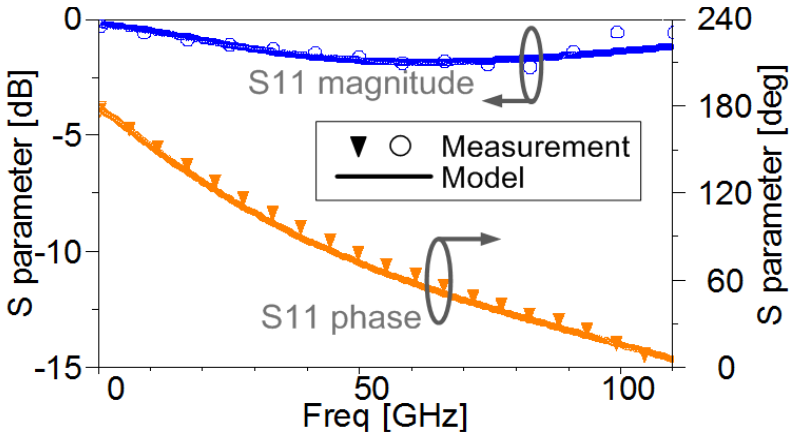


Figure 3-21 Measured and modeled magnitude and phase values of parameter S11 for a BiCMOS9mW transformer. The primary presents a 45-µm diameter and an 18-µm trace width, and the secondary presents 2 turns, a 37-µm diameter and a 4-µm trace width.

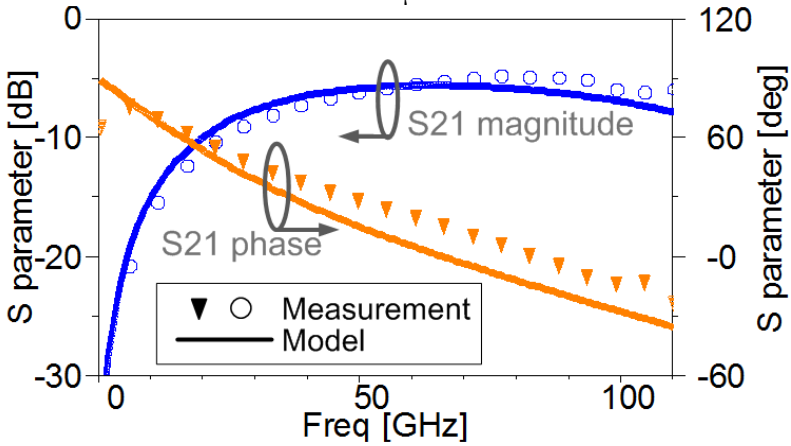


Figure 3-22 Measured and modeled magnitude and phase values of parameter S21 for a BiCMOS9mW transformer. The primary presents a 45-µm diameter and an 18-µm trace width, and the secondary presents 2 turns, a 37-µm diameter and a 4-µm trace width.

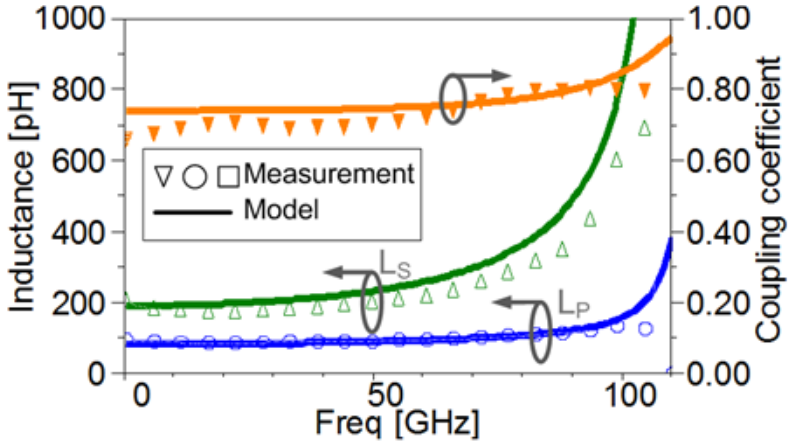


Figure 3-23 Measured and modeled inductances and coupling coefficient for a BiCMOS9mW transformer. The primary presents a 45-µm diameter and an 18-µm trace width, and the secondary presents 2 turns, a 37-µm diameter and a 4-µm trace width.

A final comparison between measured and modeled data is here presented in Figure 3-24 — Figure 3-26. Another BiCMOS transformer is presented, this time with a larger secondary diameter (53 µm). The primary presents once more a 45-µm diameter and an 18-µm trace width, whereas the secondary presents two turns with a 4-µm trace width.

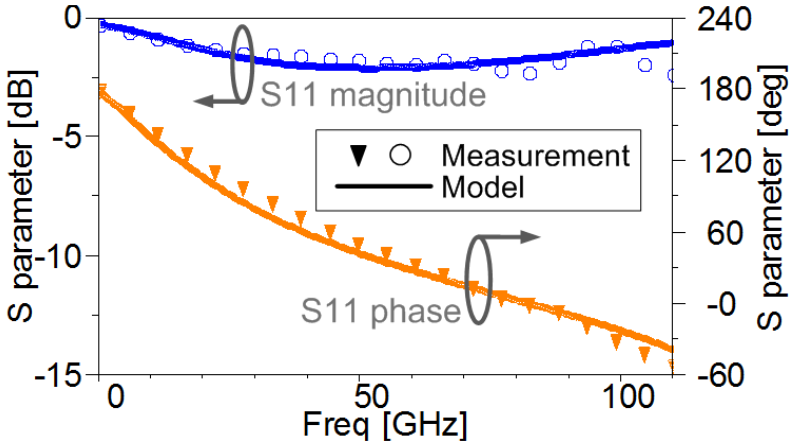


Figure 3-24 Measured and modeled magnitude and phase values of parameter S11 for a BiCMOS9mW transformer. The primary presents a 45-µm diameter and an 18-µm trace width, and the secondary presents 2 turns, a 53-µm diameter and a 4-µm trace width.

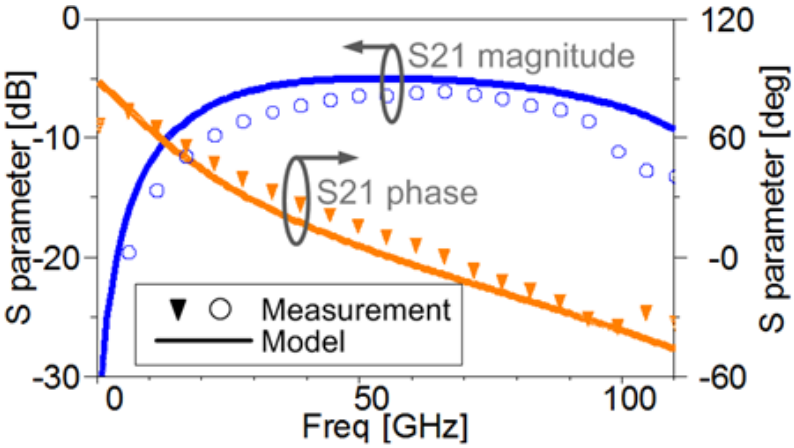


Figure 3-25 Measured and modeled magnitude and phase values of parameter S21 for a BiCMOS9mW transformer. The primary presents a 45-µm diameter and an 18-µm trace width, and the secondary presents 2 turns, a 53-µm diameter and a 4-µm trace width.

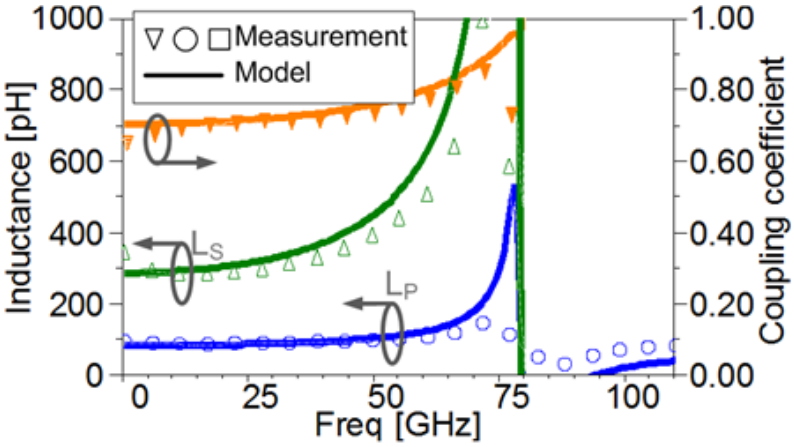


Figure 3-26 Measured and modeled inductances and coupling coefficient for a BiCMOS9mW transformer. The primary presents a 45-µm diameter and an 18-µm trace width, and the secondary presents 2 turns, a 53-µm diameter and a 4-µm trace width.

A close agreement is observed in these results. The model precisely captures the broadband behavior in terms of S-parameters magnitudes and phases, self and mutual inductances, and resonant frequencies, for transformers in two different technologies, transformers for which primaries and secondaries present the same geometry and transformers performing impedance transformation. The presented results include as well configurations with different numbers of secondary turns, different trace widths (ranging from 4 to 24 µm), and different primary and secondary average diameters (between 37 and 60 µm). It is additionally worth pointing out that the same analysis has been carried out for the totality of measured transformers, yielding analogous conclusions. The obtained results confirm the validity and scalability of the proposed architecture and expressions within the entire observed band.

3.4.2 4-port simulations

All of the presented results refer to transformers in a 2-port configuration. Nevertheless, transformers constitute essentially 4-port devices. Despite all the information which can be extracted from the employed 2-port characterization, it is not sufficient to completely capture the behavior of the transformers.

As aforementioned, the available test bench would only allow 2-port measurements in the mm-wave range. Hence, the 4-port behavior of transformers was evaluated through electromagnetic simulation. Figure 3-27 depicts the modeled and EM simulated mixed-mode S-parameter results for one transformer [BOC95] between 500 MHz and 100 GHz. Since mode conversion is minor for the considered transformers, only differential and common-mode parameters are presented.

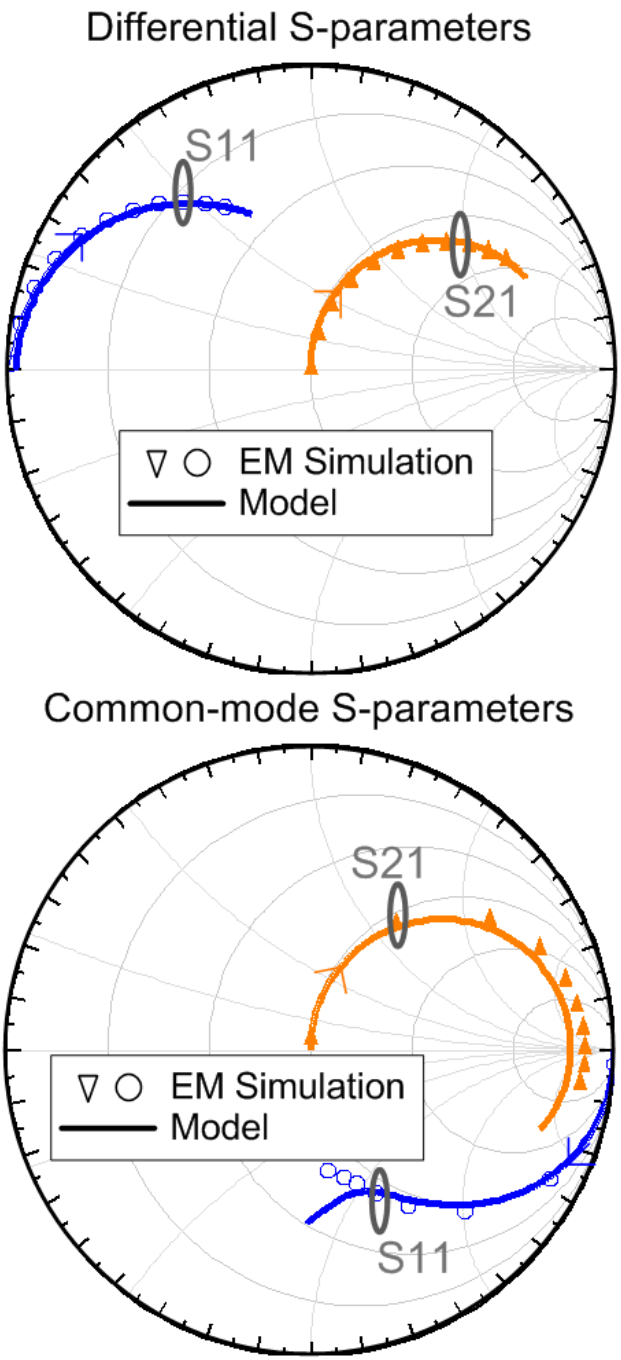


Figure 3-27 Comparison between EM simulated and modeled 4-port S-parameters for a 65-nm CMOS transformer.

Good agreement is verified for both differential and common-mode S-parameters in the entire considered band. As highlighted in Section 2, the employed simulation setup can be considered reliable enough to evaluate the actual behavior of the component. Thus, the proposed model is shown to accurately represent the transformer operation, regardless of having some of its terminals connected to ground.

4 Cadence PCELL

Cadence Virtuoso is one of the most widely adopted design environments for RF and mm-wave circuits, integrating schematic circuit simulation and layout drawing. Such IC design flow makes extensive use of components libraries which are usually supplied by the foundries and include the most commonly used active and passive elements. Integrated transformers, nevertheless, are not usually comprised in the standard provided libraries. For this reason, once the equivalent transformer model was established and validated, it was integrated into a parametric cell (PCELL) within Cadence framework.

PCELLs were implemented for both 65-nm CMOS and BiCMOS9mW technologies. Those cells receive the primary and secondary geometric dimensions as inputs (Figure 3-28) and automatically generate the corresponding electrical model and layout.

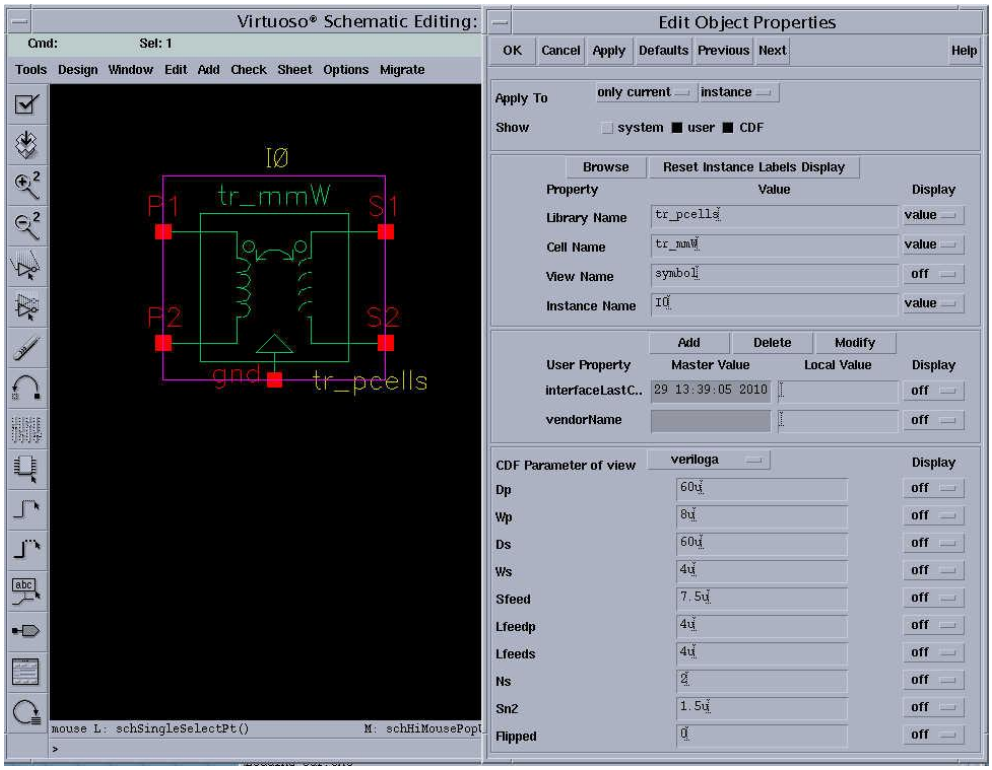


Figure 3-28 Symbol and input menu for the mm-wave transformer PCELL.

Programming for automatic layout was carried out using SKILL language whereas the electric model was described in Verilog-A. One specificity of Verilog-A modeling is that the behavior of components must be necessarily described as a function of time. Yet, as defined in equations (3-12)–(3-19), the series resistances in the transformer model present a frequency-dependent portion. In order to overcome this limitation, each of those resistances was replaced by the network depicted in Figure 3-29. The circuit contains three frequency-independent resistances and two inductances, whose values were obtained through polynomial regression of the analytic equations [CAS10]. Inductance values were dimensioned to be negligible in comparison to the series inductances of the windings. The results obtained for this sub-circuit and those obtained analytically are shown to be equivalent, as depicted in Figure 3-30

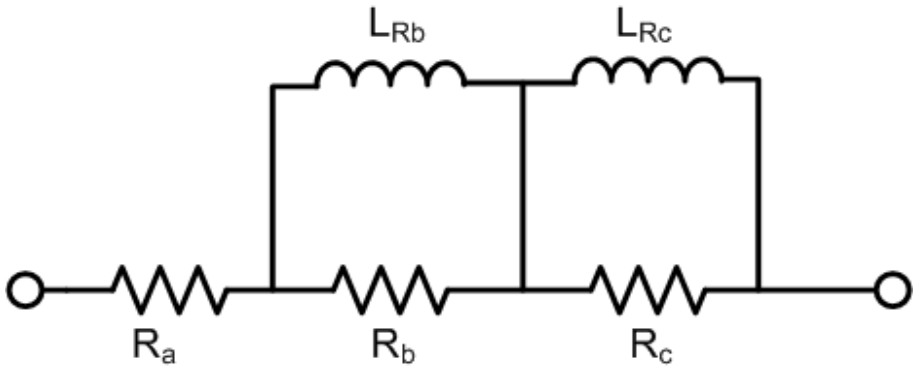


Figure 3-29 Equivalent circuit for the frequency-dependent series resistances.

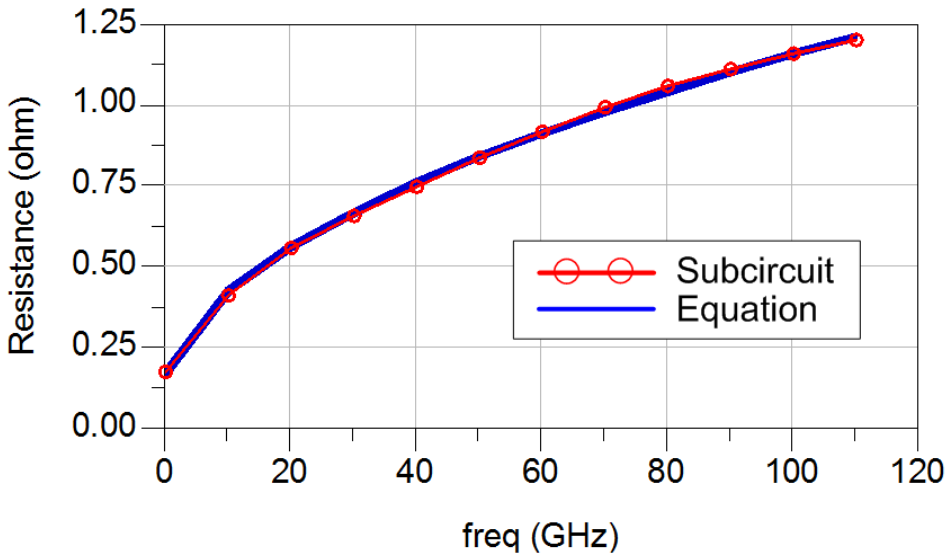
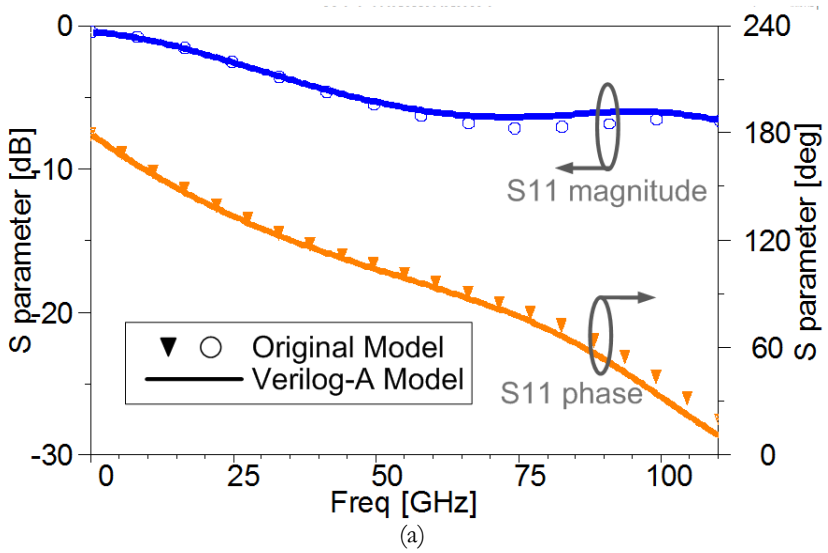
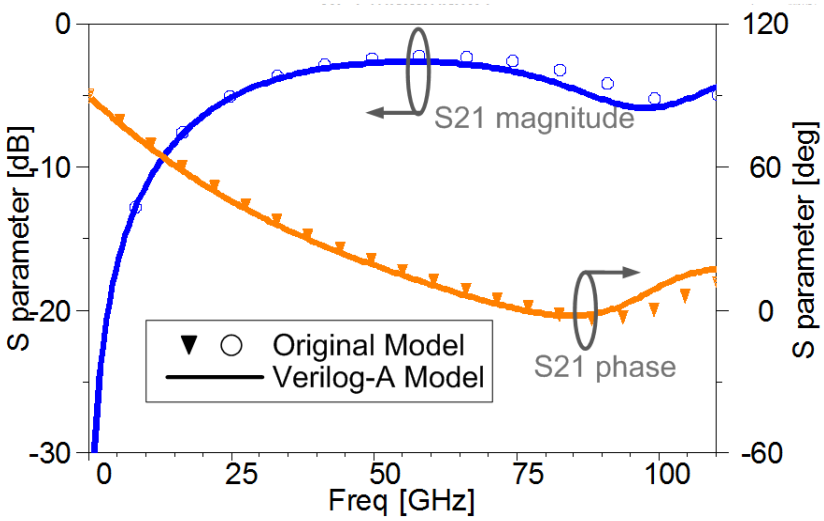


Figure 3-30 Equivalent resistance obtained through the analytical equation and proposed subcircuit.

Since the series resistances were adequately represented, PCELLs could be implemented. Figure 3-31 demonstrates how the original transformer model and the model implemented in Verilog-A supply equivalent results in terms of S-parameters. Moreover, an example of a generated layout is depicted in Figure 3-32. The developed cell was object to a technology transfer to STMicroelectronics.



(a)



(b)

Figure 3-31 Comparison of S-parameter simulation results for the original proposed model and implemented Verilog-A model for a mm-wave transformer.

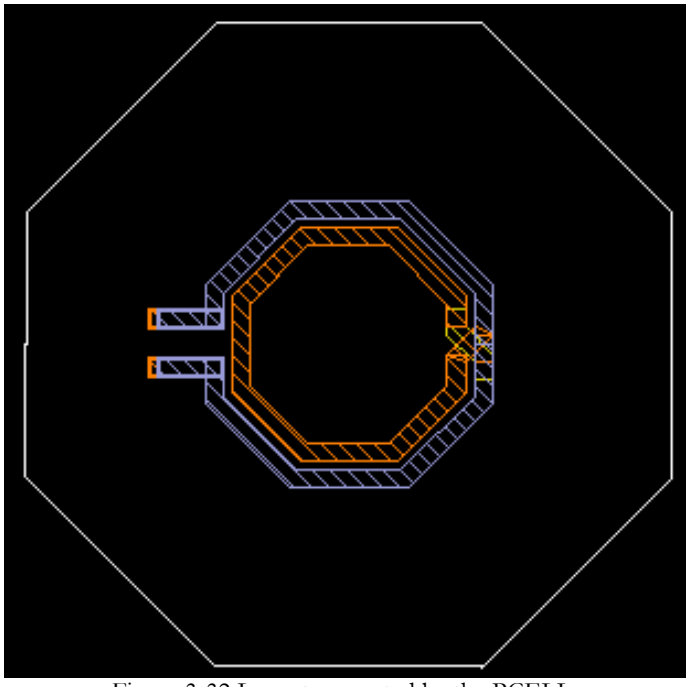


Figure 3-32 Layout generated by the PCELL.

5 Conclusion

This chapter discussed the most appropriate forms to model the behavior of mm-wave transformers: electromagnetic simulations and an equivalent electrical circuit. The advantage of EM simulations is that they can be applied for virtually any topology and technology, and yet supply very accurate results. Moreover, they offer the possibility of visualization of fields and currents within the simulate structure which may prove very useful in the analysis of the devices. The most notable downside of using EM simulators, however, is the considerably lengthy computation time. Besides, EM simulation tools typically require a reasonable amount of specific knowledge in order to properly configure their setup, which may prove impractical for a number of circuit designers.

In order to nevertheless take advantage of the possibilities offered by EM simulation, the operation of Ansoft HFSS was studied. A number of simplifications on the actual physical structure of the devices were carried out so that simulation time could be kept at reasonable levels without compromising the accuracy of the results. These simplifications were detailed and their validity was confirmed by measurements of integrated transformers in 65-nm CMOS and 130-nm BiCMOS technologies.

The most important focus of this chapter was the comprehensive description of an electrical model which is able to accurately predict the performance of transformers adapted to mm-wave operation. The model contains a 2-π lumped-element structure and analytic equations allowing to determine the value of each element. The proposed model was validated through experimental results of various transformers fabricated with different technologies, topologies and physical dimensions. Results have shown a good accuracy over a wide frequency band and scalability concerning technological and geometric parameters.

Even though it was not done in this work, it is possible to suppose that this model would succeed in representing other transformer structures, e.g., an interleaved topology, since mutual inductance and capacitance calculations take completely into account the relative position and surface occupation of conductors. The most important limitation however would be if new objects such as a substrate shield were to be introduced.

Chapter 4 : Application of integrated transformers to millimeter-wave building blocks

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This chapter presents the application of integrated transformers to the design of two mm-wave building blocks. The first one is a 130-nm BiCMOS active mixer operating at 77 GHz and the second is a 60-GHz 65-nm CMOS power amplifier. The mixer features transformers performing single-to-differential conversion and as part of the input matching network. Sizing of the transformer is detailed along with its amplitude and phase balance performances. The design of the input matching circuit integrating the transformer is presented, providing a 12-GHz bandwidth. Measured noise figure, conversion gain and compression point of the mixer are displayed and compared to the state of the art. The PA includes several transformer-based baluns and an output transformer-based power combiner. Model-based analyses are presented demonstrating the advantages of the use of a current-and-voltage combining architecture and an optimized balun topology. Measurement results are presented including S-parameters and large signal measures, as gain, saturated power and compression point. Both mixer and PA are rated among the best performances in the state of the art.

1 77-GHz BiCMOS Mixer

In order to put into practice the study on design and modeling described in the previous chapters, the design of mm-wave building blocks integrating transformers has been carried out. In the adopted approach, the characteristics of the transformers are taken into account since the early phases of circuit design. As a first example, a 130-nm BiCMOS double-balanced active mixer targeting 77-GHz automotive radar was designed. This work was done along with circuit designer A. Mariano.

The proposed mixer presents an active core with a differential architecture. Transformers are then used to convert the single-ended inputs RF_{in} and LO_{in} into a differential form, while taking part into the respective input matching networks, as depicted in Figure 4-1. The main contributions of this thesis to the proposed circuit, namely the design of the transformer-based baluns and the input matching network are detailed hereafter.

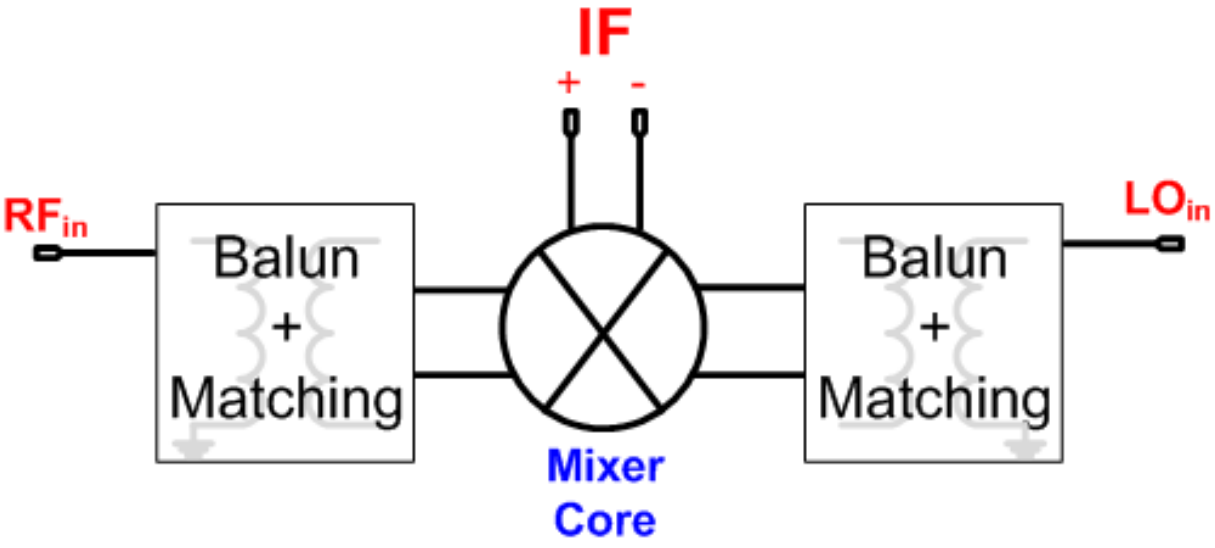


Figure 4-1 Block diagram of the proposed mixer.

1.1 Balun design

The use of balanced topologies in integrated circuits presents several advantages over their single-ended counterparts. The symmetry allows an increased immunity with respect to substrate coupling, digital circuitry, and power supply noise as well as a better tolerance to non-perfect 0-V grounds.

However, many integrated circuits are required to present their inputs or outputs in a single-ended form. In such cases, it is necessary that a mode conversion element be introduced. Hence, the benefits of balanced topologies will only be applicable if these elements do not introduce important insertion loss and signal distortion. For this reason, a correct design of balanced to unbalanced converters (baluns) is of foremost importance.

In radiofrequency domain, both active and passive baluns are commonly used. For mm-wave frequencies, nevertheless, the use of active structures becomes more troublesome as the delay introduced by the transistors yields a significant negative effect on the phase balance of the balun output [WAN06-1]. Among passive-based solutions, three categories stand out: the LC-based, the transmission-line based, and the transformer-based baluns. LC baluns rely on the resonance of inductive and capacitive components thus performing the balance at a single frequency. An alternative to enhance the bandwidth is the use of line-based baluns. Two main structures are prominent: the Marchand balun [LEE04], [LIU07], and the rat-race balun [DIN08]. Marchand baluns combine two pairs of coupled $\lambda/4$ lines, one of which is open-ended and the two others are shorted. Rat-race baluns, adapted from rat-race couplers, are set by 4 ports in a circular disposition with a total length of $3\lambda/2$. In the 60-100 GHz frequency band, the signal wavelength is in the millimeter range, making such solutions considerably cumbersome for silicon integration. Transformer-based baluns, on the other hand, present a compact implementation. Additionally, the broadband behavior of the coupling between primary and secondary windings makes them suitable for wideband operation.

The aim of this work is to design a transformer to operate as a balun. Three essential features must be considered to evaluate their performance: insertion loss, amplitude balance, and phase balance. Considering Port 1 represents the single-ended terminal, and Ports 2 and 3 represent the differential ports, the insertion loss will be obtained from the magnitude of the scattering parameters S_{21} or S_{31}. For a perfect balun, these parameters would be equal to 3 dB, which corresponds to the 2-way power splitting. Also, an ideal balun would have the same magnitude but opposite signs for these two ports, i.e., the phases of S_{21} and S_{31} would have a 180° difference. Hence, the measures of insertion loss, amplitude and phase imbalance are computed as in (4-1), (4-2) and (4-3).

$$\text{Insertion Loss} = \left| \frac{S_{31}}{2} \right| \tag{4-1}$$

$$\text{Amplitude Imbalance} = \left| \frac{S_{31}}{S_{21}} \right| \tag{4-2}$$

$$\text{Phase Imbalance} = \angle\left(-\frac{S_{31}}{S_{21}}\right) \tag{4-3}$$

The proposed balun presents a flipped and octagonal topology as shown in Figure 4-2. Moreover, it presents a center-tapped differential winding. This point, which is supposed to be AC-grounded, simultaneously represents the inductive, capacitive and resistive center of the corresponding winding. Such connection enables a short circuit for common-mode signals while not affecting the differential component.

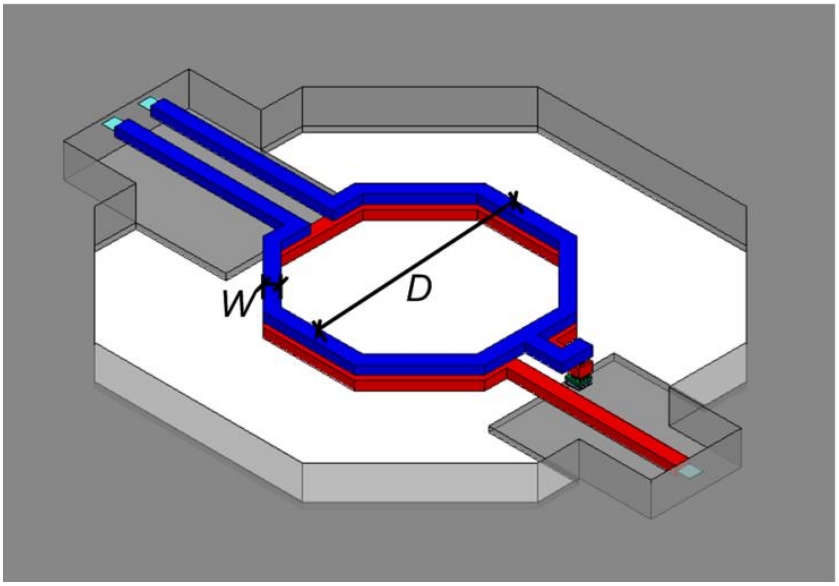


Figure 4-2 Topology of the designed transformer-based balun.

Figure 4-3 illustrates the need of this central ground connection. It compares HFSS EM simulations of the same transformer-based balun with and without a center tap. It demonstrates that the non-tapped structure provides balanced outputs up to 10 GHz whereas the tapped configuration achieves a low and flatter phase and amplitude imbalance up to 100 GHz.

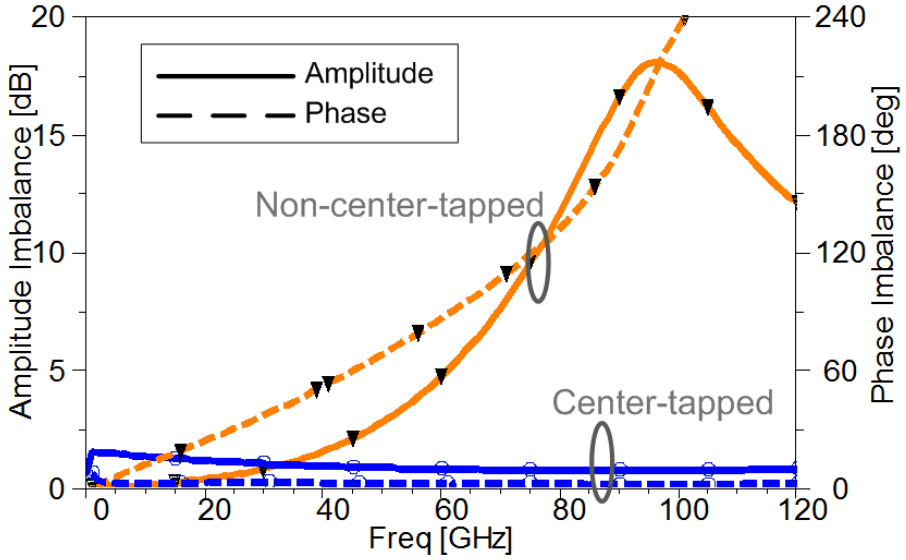
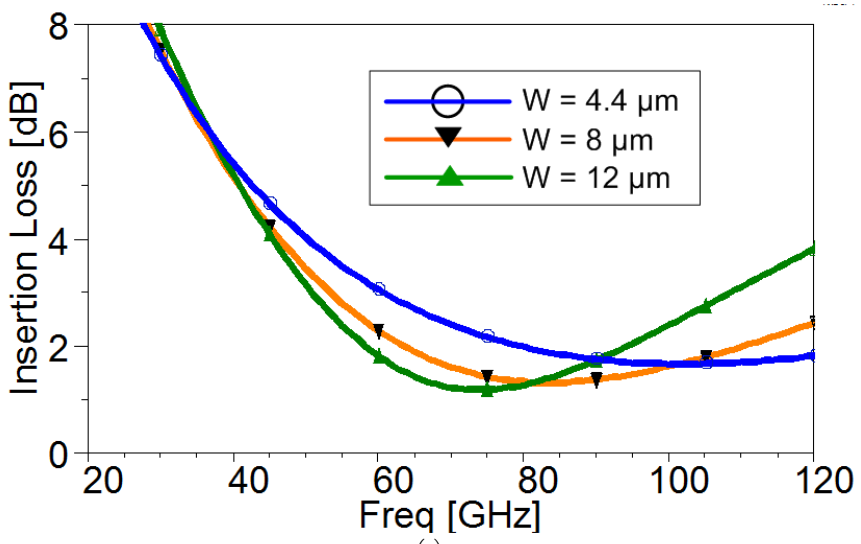
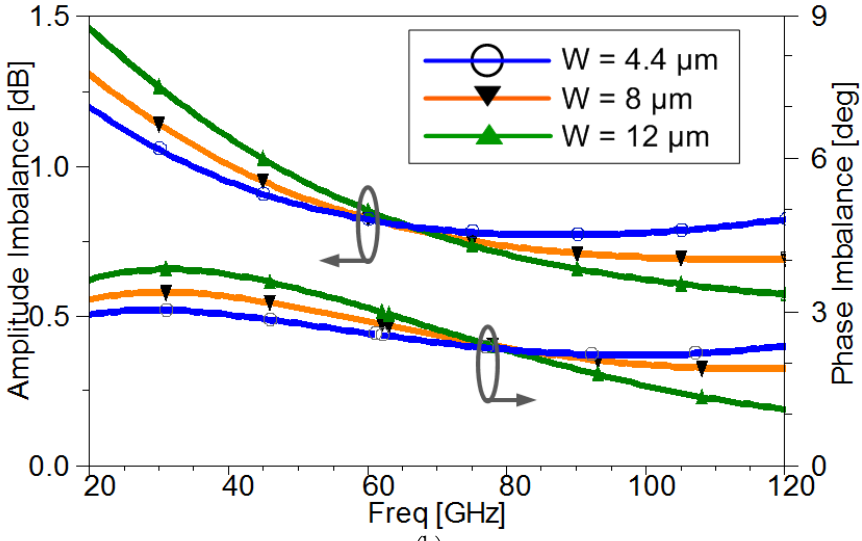


Figure 4-3 Simulated amplitude and phase imbalances for center-tapped and non center-tapped transformers.

Once the topology of the transformer is defined, its dimensions are optimized to ensure an effective balun operation. The impact of the trace width for a fixed diameter is firstly observed. Three values were studied: 4.4 µm, 8 µm and 12 µm. Figure 4-4 presents the EM simulation results of these three configurations. As traces are drawn narrower, the capacitive components of the transformer are reduced whereas the inductance and sheet resistance are increased. This leads to a decrease on the windings quality-factors, which is reflected in the insertion loss of the balun. On the other hand, it allows a clearly wider frequency behavior of the transformer S-parameters, expressed in terms of insertion loss and amplitude/phase imbalances. This is an important advantage as it considerably increases design robustness, palliating the influence of process variations or inaccurate modeling of interconnections. Finally, it is observed that the trace width has little influence over amplitude and phase balances, even though the results for narrow traces are shown to be flatter. Hence, the value of 4.4 µm was adopted for the trace width in our design.



(a)



(b)

Figure 4-4 Simulated (a) insertion loss, and (b) amplitude and phase imbalances for different conductor width values.

Having defined the conductor width, the design proceeded by dimensioning the transformer average diameter. In Figure 4-5, the simulated insertion loss, amplitude and phase balances are evaluated for three different diameters: 60 µm, 70 µm, and 80 µm. It is observed that, for the same trace width, the larger the transformer is, the lower its insertion losses are. A 70-µm diameter allows an insertion loss 0.5 dB higher than an 80-µm, while a 60-µm diameter provides an insertion loss as high as 2.9 dB. The 80-µm balun, however, presents the worst amplitude balance. The best tradeoff is hence the 70-µm diameter, which presents the best combination of amplitude and phase balances as well as the flattest balance response.

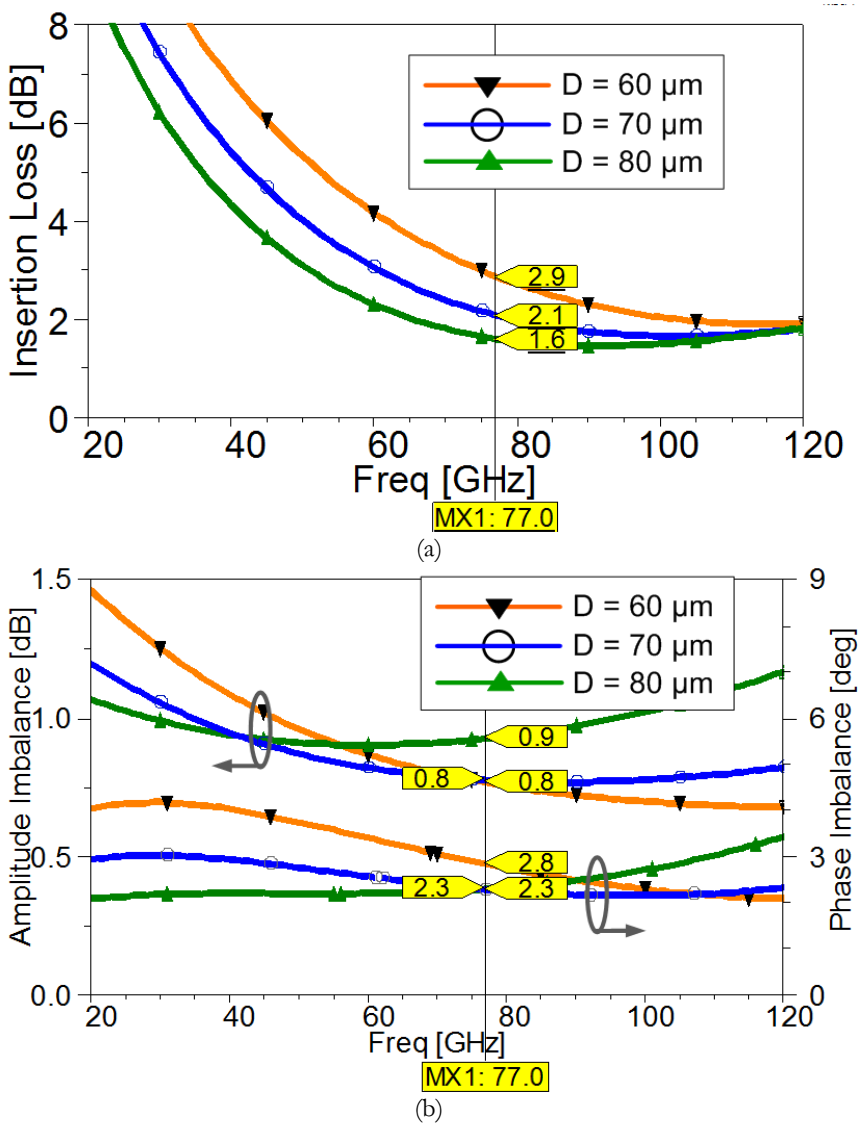


Figure 4-5 Simulated (a) insertion loss, and (b) amplitude and phase imbalances for different diameter values.

The designed balun presents a total inductance of 140 pH in each winding and a coupling coefficient of 0.67. Its dimensions, including feed lines and the specified distance between the conductors and the surrounding ground plane, is 190 × 150 µm². Table 4-1 compares the performance of this work to mm-wave baluns previously described in the literature. Our balun presents the broadest bandwidth and the best phase balance while occupying the smallest surface among the considered components.

Table 4-1 Summary of mm-wave balun performances.

Ref.	Topology	Technology	Frequency (GHz)	AI (dB)	PI	IL (dB)	Surface (mm^2)
[LEE04]	Marchand	GaAs	26 -55	< 1	< 5°	< 2	0.51
[LIU07]	Marchand	0.18 µm CMOS	25 - 65	<1.5	< 10°	< 7	0.55
[DIN08]	Marchand	0.13 µm BiCMOS	45 -75	< 0.5	< 6°	< 2.5	0.09
[DIN08]	Rat-race	0.13 µm BiCMOS	57 -71	< 0.6	< 10°	< 3.2	0.28
[HAM05]	Line-based	InGaP/ GaAs	15 -45	< 1	< 5.5°	< 7	0.04
[FEL07]	Transformer	0.13 µm CMOS	55 - 65	< 3	< 10°	3	0.05
This work (simulation)	Transformer	0.13 µm BiCMOS	60 - 120	< 1	< 3°	< 3	0.03

1.2 Mixer core design

The schematic of the proposed mixer core [MAR10-1] is depicted in Figure 4-6. It is based on a double-balanced active topology (Gilbert cell) consisting of a transconductance stage (T1, T2) which converts the input RF voltage into current and a switching stage (T3 – T6), that commutates the RF current between the two output IF nodes.

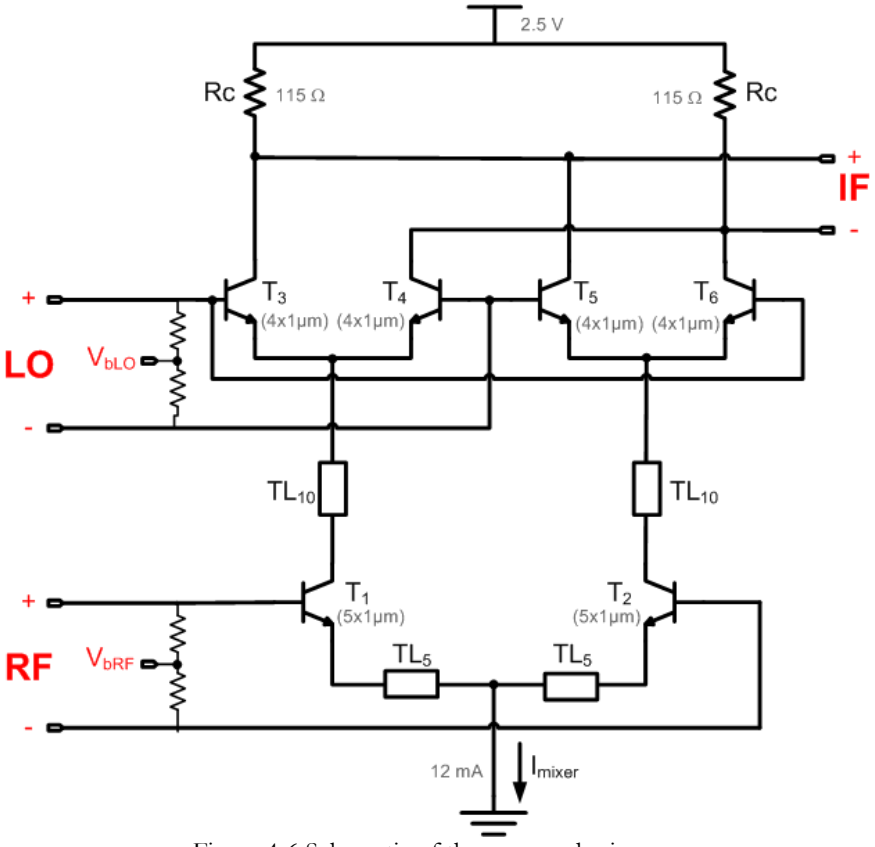


Figure 4-6 Schematic of the proposed mixer core.

1.3 Impedance matching

One main specification for the designed circuit is its wideband behavior. This specification is expressed as return losses better than 10 dB in the 76 - 81 GHz range. For robustness reasons and in order to fully exploit the possibilities offered by the adopted approach, this constraint was extended for a bandwidth between 74 and 86 GHz in our design.

As previously detailed, the RF input of the designed mixer presents a common emitter topology with an inductive degeneration. In order to perform the input matching, capacitors were introduced in series at the primary and secondary sides of the balun, and their connections with the circuit elements were performed using transmission lines. Figure 4-7 illustrates the obtained input matching circuit.

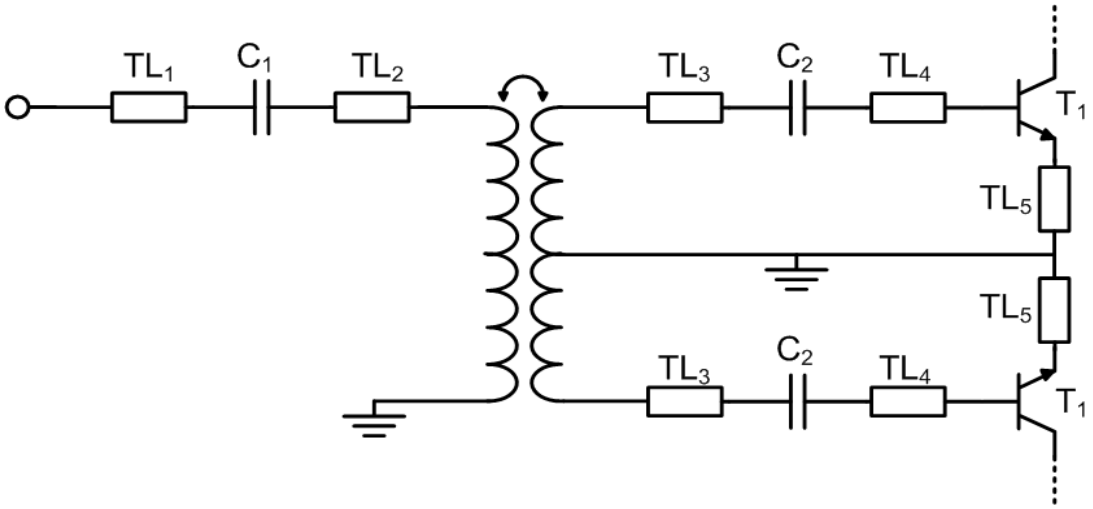


Figure 4-7 Input matching network of the designed mixer.

Simplified models were adopted to represent the different elements within this network. First of all, each transmission line was represented as a pure inductor. Moreover, as shown in Figure 4-8, the degenerated transistor was replaced in our analysis by a series combination of the degeneration inductance L_{TL}, the base-emitter capacitance C_{π}, and the equivalent input real impedance R_T obtained thanks to the transistor effect. The value of R_T is obtained by (4-4):

$$R_T = \frac{g_{m0}}{C_{\pi}} \cdot L_{TL} \tag{4-4}$$

Finally, the balun was represented by the simplified model of Figure 4-8(c). Each transformer winding is represented by a series frequency-independent resistance along with the magnetizing and leakage portions of the respective self inductances. Additionally, as the primary is located between the secondary and the silicon substrate, the capacitance to the substrate is only represented at the primary side. In this model, we refer all impedances to the secondary of the ideal transformer. Its transformation ratio T is calculated by (4-5):

$$T = k \cdot \sqrt{\frac{L_P}{L_S}} \tag{4-5}$$

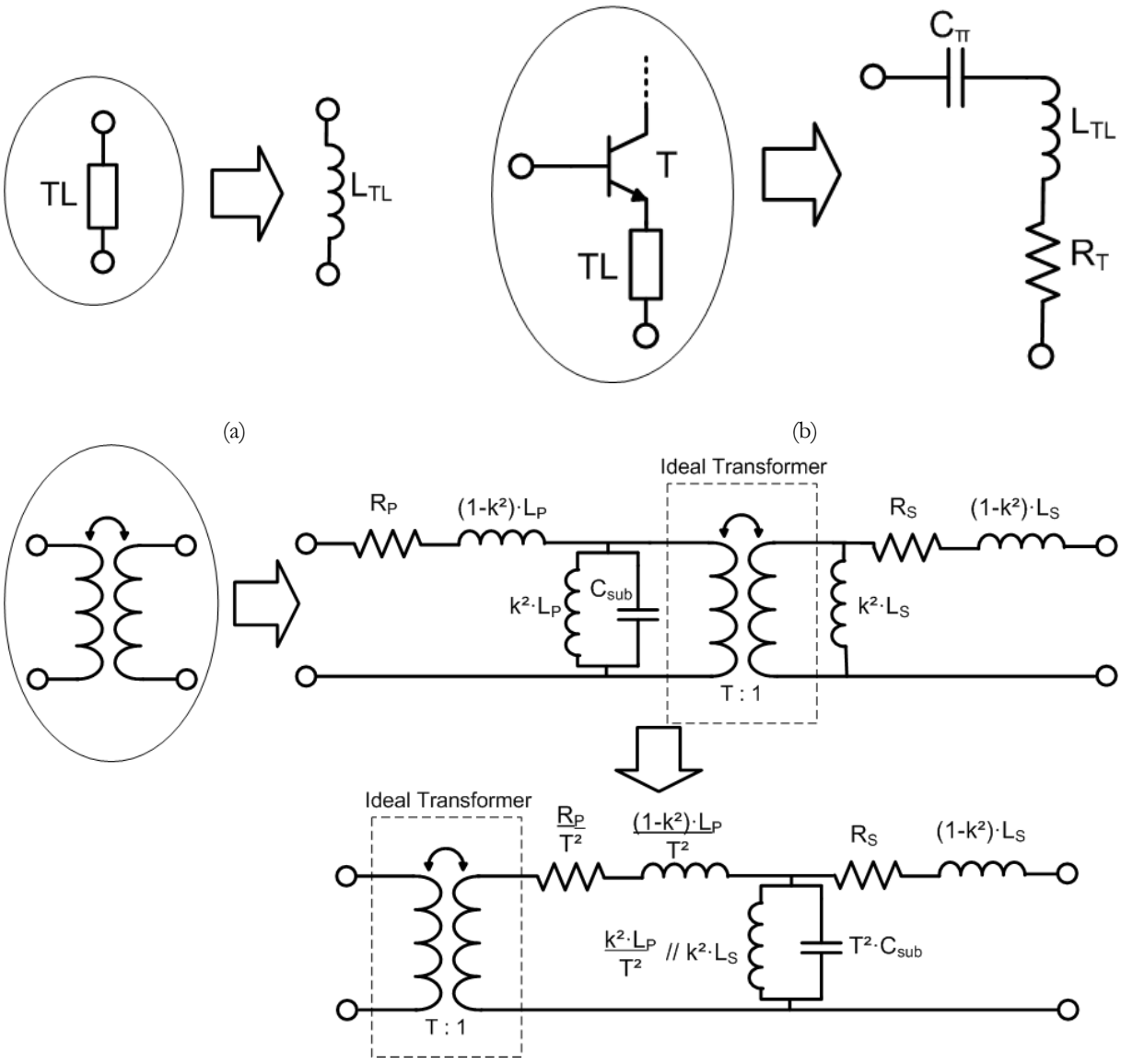


Figure 4-8 Simplified models for (a) transmission-lines, (b) degenerated transistor, and (c) transformer-based balun.

As the transistor, capacitors, and transmission lines models are combined with this transformer representation, we obtain the T-shaped 6th order bandpass filter network of Figure 4-9. Its elements are then computed as follows:

$$R_a = \frac{R_P}{2 \cdot T^2} \tag{4-6}$$

$$L_a = \frac{(1-k^2) \cdot L_P + L_{TL1} + L_{TL2}}{2 \cdot T^2} \tag{4-7}$$

$$C_a = 2T^2 \cdot C_1 \tag{4-8}$$

$$L_b = \frac{k^2 \cdot L_P}{2 \cdot T^2} // \frac{k^2 \cdot L_S}{2} \tag{4-9}$$

$$C_b = 2T^2 \cdot C_{sub} \tag{4-10}$$

$$L_c = \frac{(1-k^2)\cdot L_S}{2} + L_{TL3} + L_{TL4} + L_{TL5} \tag{4-11}$$

$$C_c = \frac{1}{\frac{1}{C_2} + \frac{1}{C_\pi}} \tag{4-12}$$

$$R_c = \frac{R_S}{2} + \frac{g_{m0}}{C_\pi}\cdot L_{TL5} \tag{4-13}$$

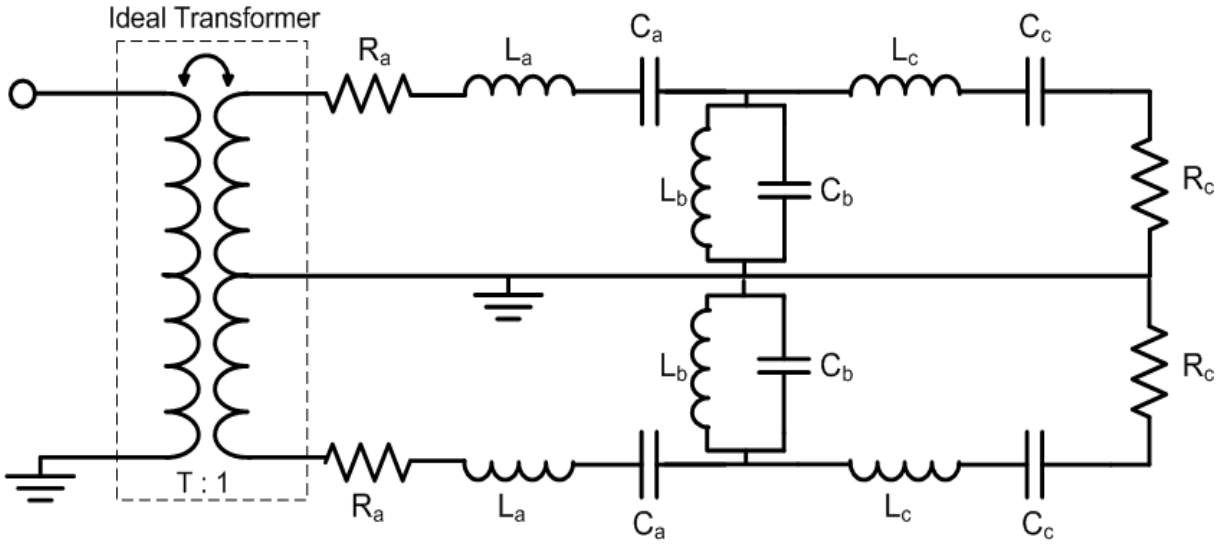


Figure 4-9 Simplified model of the input matching network.

The analytical calculation of the reflection coefficient S_{11} follows equation (4-14), where Z_{in} represents the input impedance of the network and R_{source} the source resistance for the measurements, which in our case equals 50 Ω.

$$S_{11} = \frac{Z_{in} - R_{source}}{Z_{in} + R_{source}} \tag{4-14}$$

If we define Z_a as the combination of R_a, L_a and C_a, Z_b as the combination of L_b and C_b, and Z_c as the combination of L_c and C_c, then:

$$S_{11} = \frac{Z_a + Z_b - \frac{Z_b^2}{Z_b + Z_c + R_c} - R_{source}}{Z_a + Z_b - \frac{Z_b^2}{Z_b + Z_c + R_c} + R_{source}} \tag{4-15}$$

The sizing of the components obeyed the following criteria. The transformer was first designed to provide the best tradeoff between balance and insertion loss, according to Section 1.1. This is especially important, since the simplified model here described assumes balanced differential ports. Then, the input transistors and their degeneration lines were dimensioned in order to address linearity and conversion gain concerns. Hence, the degrees of freedom in order to achieve the desired input matching were the capacitors C_1 and C_2, and the transmission line pairs TL_1-TL_2 and TL_3-TL_4. These values impact exclusively the impedances Z_a and Z_c in equation (4-15).

Figure 4-10 andFigure 4-11 show how the dimensions of these components affect the width and the lower limit f_{low} of the matched frequency band. The dimensions of TL_1 and TL_2, for instance, display a monotonic trend for which the lowest inductance values ensure the broadest band. Hence, these lines were designed in order to provide the smallest possible values within layout limitations, which led to a length of 32 µm and a 14-pH inductance. The remaining components were then conjointly set to allow a 12-GHz bandwidth between 74 and 86 GHz. The defined values are therefore 35 pH for the combined inductance of TL_3 and TL_4, 70 fF for C_1, and 60 fF for C_2. Table 4-2 summarizes the defined values of all elements in the circuit of Figure 4-9.

Table 4-2 Summary of the component values in the matching network.

L_a	102 pH	L_b	22 pH	L_c	113 pH
C_a	55 fF	C_b	202 fF	C_c	37 fF
R_a	12 Ω	T	0.67	R_c	80 Ω

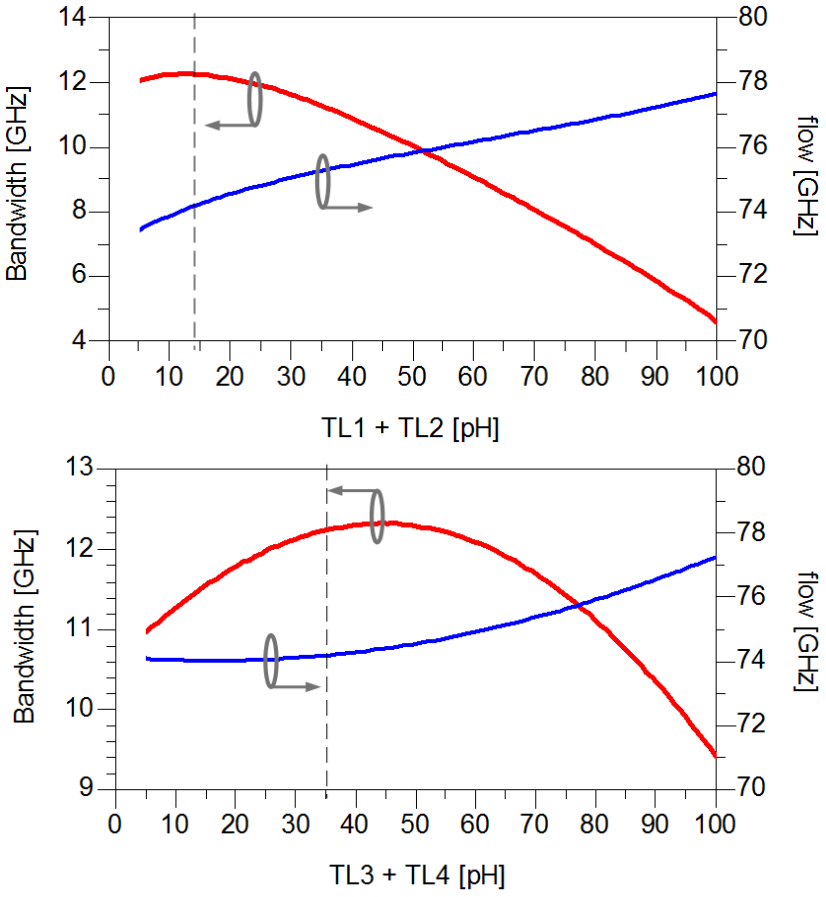


Figure 4-10 Bandwidth and lower limit frequency of the matching circuit in function of the transmission-line inductance values.

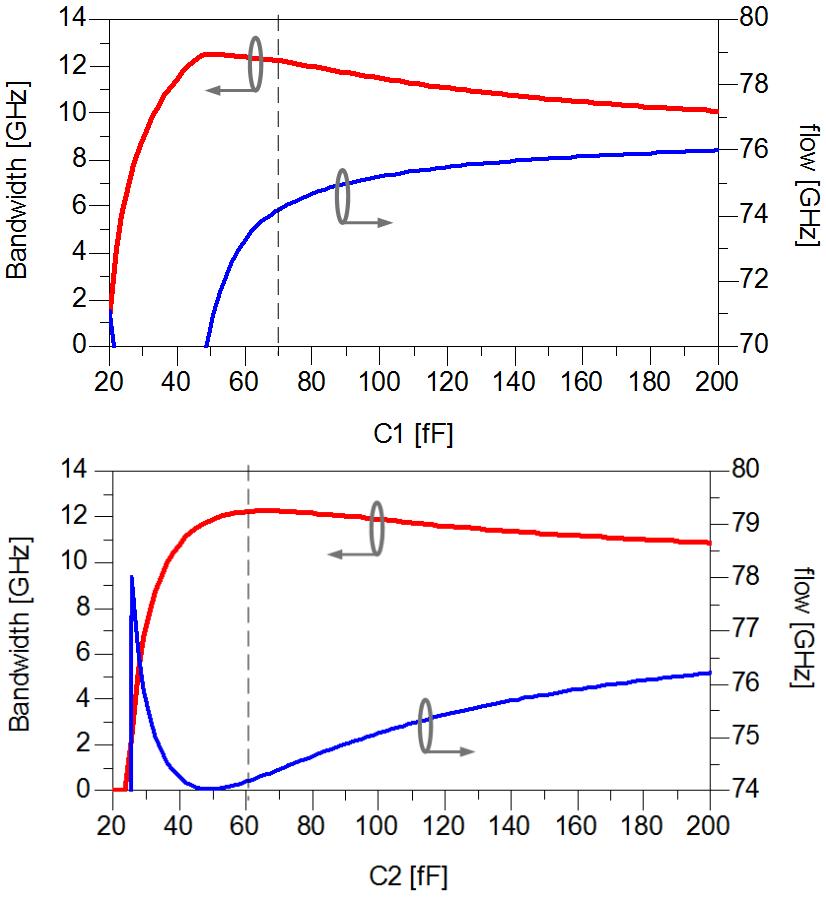


Figure 4-11 Bandwidth and lower limit frequency of the matching circuit in function of the capacitance values

1.4 Measurement results

Figure 4-12 depicts the micrograph of the designed mixer. The chip takes place within 0.57 mm^2 including pads. All measurements were done on wafer at 20°C with 110-GHz GSG probes. The RF (75 – 80 GHz) and LO (80 GHz) signals are provided by an Agilent PNA network analyzer E8361A and an Agilent PSG signal generator E8257D, respectively. The IF output is collected using an Agilent PSA spectrum analyzer E4440A via an external balun.

The proposed active mixer consumes 80 mW under 2.5 V. The measured conversion gain (CG) and single-sideband noise figure (NF_{SSB}) as a function of LO power (P_{LO}) are reported in Figure 4-13. Both characteristics improve with LO power and saturate for LO values exceeding +1 dBm. The maximum measured CG is 18.5 dB, achieved at 77 GHz. The lower value of NF_{SSB}, 13.8 dB, is obtained for these operating conditions. The mixer 1-dB compression point (ICP_1), calculated with a LO signal of 1 dBm at 80 GHz, corresponds to a –13-dBm RF input power.

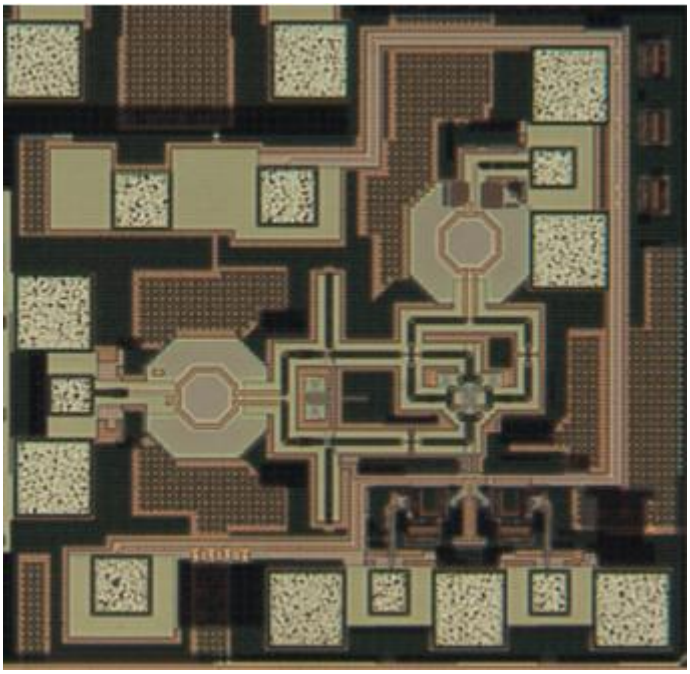


Figure 4-12 Micrograph of the mm-wave mixer.

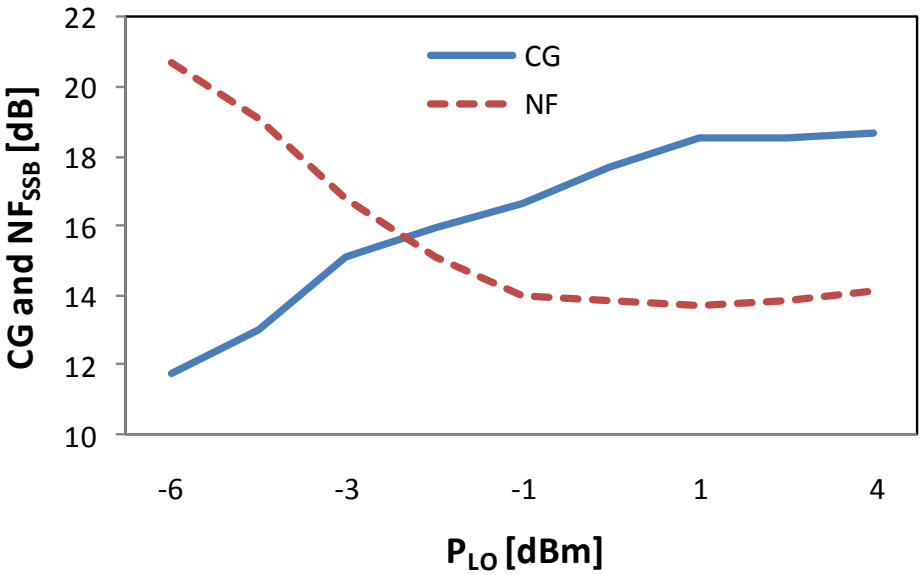


Figure 4-13 Measured CG and NF_{SSB} of the mixer as a function of LO power (f_{RF} = 77 GHz and f_{LO} = 80 GHz).

The measured return losses are depicted in Figure 4-14 and compared to the simulated results obtained from the circuit of Figure 4-9. This result highlights how, in spite of the several simplifications, the proposed approach manages to accurately capture the behavior of the circuit in terms of input matching. As predicted, the reflection coefficient is inferior to -10 dB for the whole range comprised between 74 and 86 GHz.

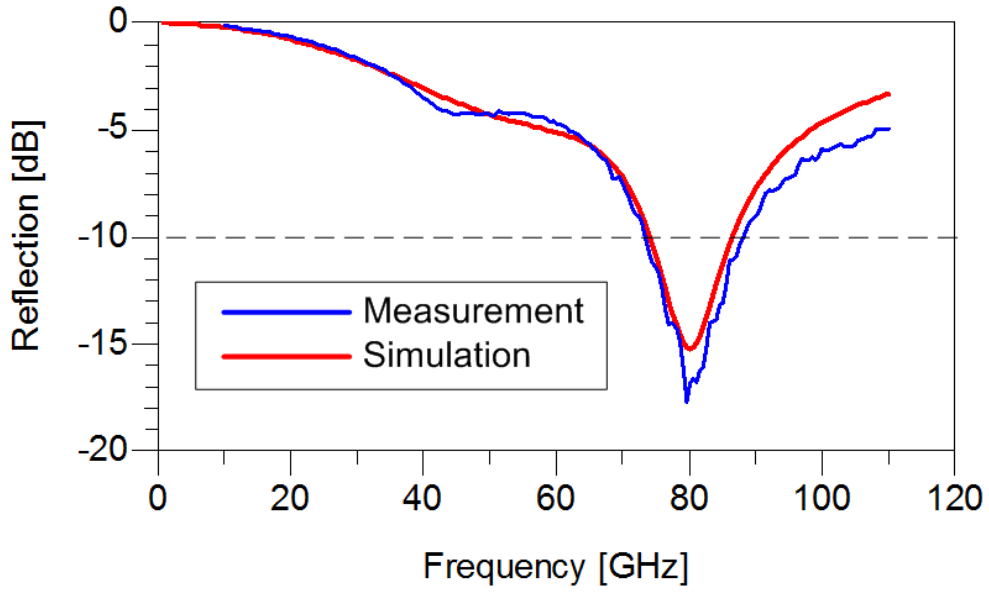


Figure 4-14 Measured and simulated reflection coefficient for the designed mixer input network.

Measurement results of the reported circuit, along with other SiGe 77-GHz mixers are listed in Table 4-3. A Figure of Merit (FoM) combining their most relevant metrics is defined in (4-16).

$$FoM_{mixer} = 10\log\left(\frac{10^{CG/20}.10^{ICP1/20}}{10^{NF_{SSB}/10}.P_{DC}.V_{cc}}\right) \quad (4\text{-}16)$$

The proposed mixer presents the lowest power consumption and a high conversion gain, resulting in the second best FoM among the considered circuits.

Table 4-3 Summary of 77-GHz SiGe Mixer performances.

Ref.	NF_{SSB} (dB)	CG (dB)	ICP_1 (dBm)	V_{cc} (V)	P_{DC} (mW)	FoM_{mixer} ($dB \cdot V^{-2} \cdot A^{-1}$)
[TRO07]	11.2	15	2.5	5.5	335	-33.85
[PER04]	14	24	-30	-5	300	-63.76
[DEH06]	16.5	11	0	5.5	413	-44.56
[WAN06-2]	18.4	13.4	-12	4.5	176	-52.69
[DIC05]	16	15.5	-3	5.5	187	-41.37
This work	13.8	18.5	-13	2.5	80	-40.56

2 60-GHz CMOS PA

In addition to the work done regarding the down-converter mixer, a mm-wave power amplifier was designed in order to apply the investigated transformers. The circuit was designed in 65-nm CMOS technology and it is intended to operate at the 60-GHz WPAN and WLAN band. This work was done along with circuit designers S. Aloui, N. Demirel, and Y. Luque.

The architecture of the proposed PA is depicted in Figure 4-15. Regarding actives, it contains a driver stage, also referred to as a Pre-Power Amplifier (PPA), and a power stage. The driver stage contains two pseudo-differential amplifying units (uPPA), while the power stage presents a parallel topology integrating 8 elementary amplifying cells (uPA). In order to combine the outputs from these cells, a transformer-based power combiner is employed. Moreover, transformer-based baluns are extensively used throughout the circuit (7 baluns in total).

The main contributions of this thesis to the proposed circuit, namely, the analysis and design of optimized transformer-based structures to perform balun operation, matching and power combination, are detailed hereafter.

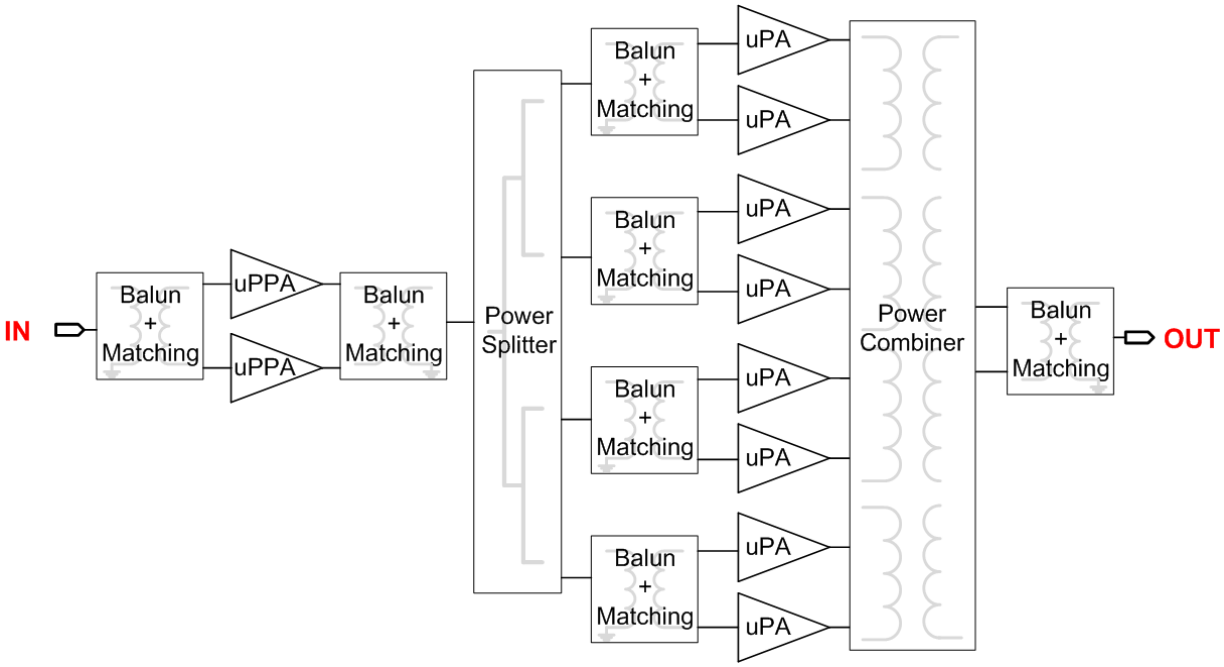


Figure 4-15 Architecture of the proposed PA.

2.1 Balun design

The traditional approach to apply transformers as baluns is to assign a single input to one of the primary ports and to ground the other, as it was done for the mixer. Nevertheless, the obtained behavior of the structure deviates from the ideal, as the observed signals at the differential ports do not present the exact same amplitude and a 180° phase difference. Despite the possible asymmetry in the substrate branches and series resistances, the reason for such imbalance is the electric coupling represented by the capacitors C_{PS}, in the model of Figure 4-16, which adds to the magnetic coupling in order to perform power transfer between primary and secondary. This is demonstrated in Figure 4-17 which compares amplitude and phase imbalances for the cases containing and not containing those capacitances. Perfect balance is achieved when the capacitors C_{PS} are not considered.

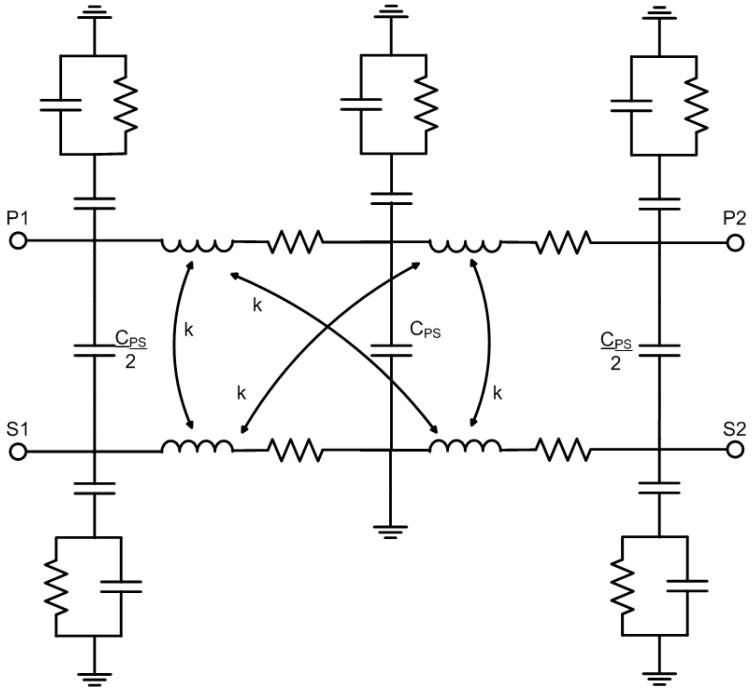
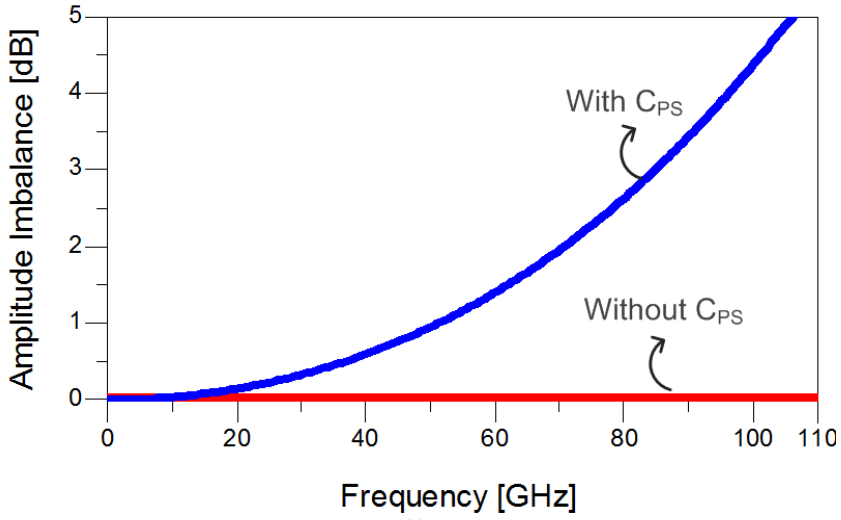
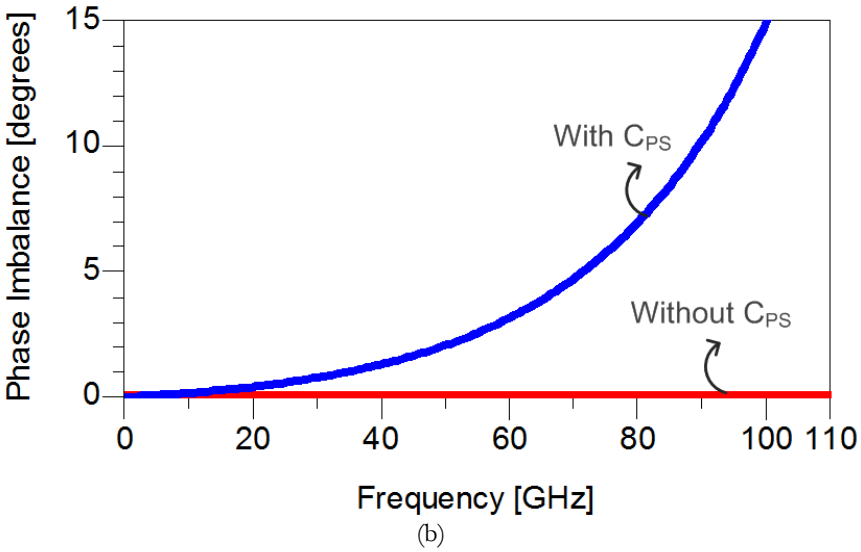


Figure 4-16 Transformer model with a grounded center-tap.



(a)



(b)

Figure 4-17 Impact of capacitive coupling on (a) amplitude and (b) phase imbalances.

In order to palliate the effect of these parasitic capacitances, the solution proposed in [ALO10-2] is to connect a capacitor C_{bal} to one of the primary ports, as in Figure 4-18. The simplified model of Figure 4-19 was considered in order to evaluate the effect of this modification. The model does not contain any components representing resistive losses or substrate coupling, but focuses instead on the elements responsible for the imbalance.

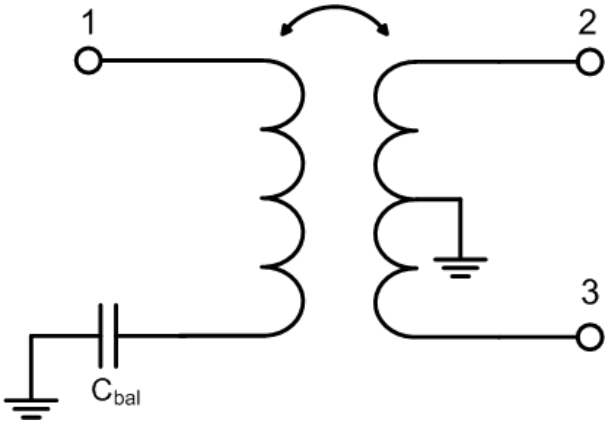


Figure 4-18 Optimized balun configuration.

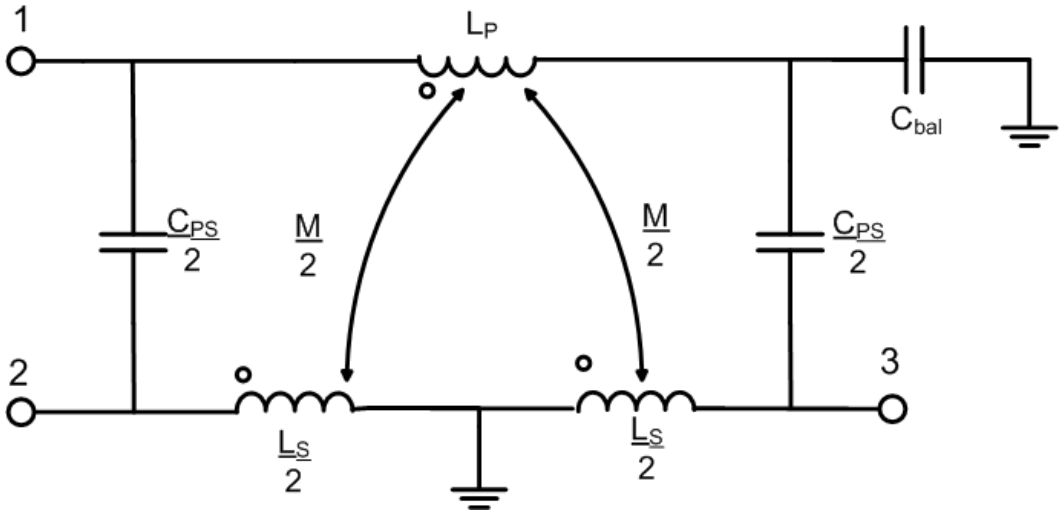


Figure 4-19 Simplified transformer model for balun analysis.

A useful metric to simultaneously evaluate amplitude and phase balance characteristics of a balun is the common mode rejection ration (CMRR). It is defined as the ratio between differential and common-mode gains, and its calculation in terms of the scattering parameters is given in (4-17) [BOC95].

$$CMRR = \left| \frac{S_{31} - S_{21}}{S_{31} + S_{21}} \right| \tag{4-17}$$

If we convert it into impedance parameters, the following expression is obtained, where Z_{Ref} represents the reference impedance presented at the balun ports.

$$CMRR = \left| \frac{Z_{31} \cdot \left(Z_{Ref} + Z_{22} + Z_{32}\right) - Z_{21} \cdot \left(Z_{Ref} + Z_{33} + Z_{32}\right)}{Z_{31} \cdot \left(Z_{Ref} + Z_{22} - Z_{32}\right) + Z_{21} \cdot \left(Z_{Ref} + Z_{33} - Z_{32}\right)} \right| \tag{4-18}$$

If the balun is sufficiently distant from its resonant frequency, then the value of Z_{32} will be proportionately small, while the values of Z_{22} and Z_{33} will be relatively close. In this case, CMRR approaches $CMRR_Z$ defined in (4-19).

$$CMRR_Z = \left| \frac{Z_{31} - Z_{21}}{Z_{31} + Z_{21}} \right| \tag{4-19}$$

Inspecting (4-19), it can be inferred that CMRR should reach its maximum value at the frequency point where $Z_{21} + Z_{31} = 0$. From the circuit of Figure 4-19, the values of these impedances are:

$$Z_{31} = \frac{j\omega \cdot \left\{ \frac{C_{PS}}{2} \cdot \left[\left(\frac{M}{2} \right)^2 - \frac{L_P}{2} \cdot \frac{M}{2} \right] \cdot \omega^2 + \frac{M}{2} \right\}}{\frac{C_{PS}}{2} \cdot \left(-M + \frac{L_P}{2} + L_S \right) \cdot \omega^2 - \left(1 + \frac{C_{PS}/2}{C_{bal}} \right)} \tag{4-20}$$

$$Z_{21} = \frac{j\omega \cdot \left\{ \frac{C_{PS}}{2} \cdot \left[-\left(\frac{M}{2} \right)^2 + L_P \cdot \frac{L_S}{2} \right] \cdot \omega^2 - \left(\frac{C_{PS}/2 \cdot L_P/2}{C_{bal}} + \frac{M}{2} \right) \right\}}{\frac{C_{PS}}{2} \cdot \left(-M + \frac{L_P}{2} + L_S \right) \cdot \omega^2 - \left(1 + \frac{C_{PS}/2}{C_{bal}} \right)} \tag{4-21}$$

The frequency ω_0, where $Z_{21} + Z_{31} = 0$, is then:

$$\omega_0 = \frac{1}{\sqrt{\left(L_s - \frac{M}{2} \right) \cdot C_{bal}}} \tag{4-22}$$

Hence, it is observed that if the primary port is directly connected to the ground, i.e. if $1/C_{bal}=0$, the only frequency where the condition $Z_{21} + Z_{31} = 0$ is satisfied is at DC. Using C_{bal}, on the other hand, CMRR can be maximized for a desired frequency through the choice of the capacitance value. Figure 4-20 compares the simulated CMRR with and without a capacitor dimensioned to provide maximum CMRR at 60 GHz. The obtained results corroborate the validity of the proposed topology. Therefore, optimized baluns presenting capacitors at the primary port have been used throughout the PA, providing additional impedance transformation and a low insertion loss.

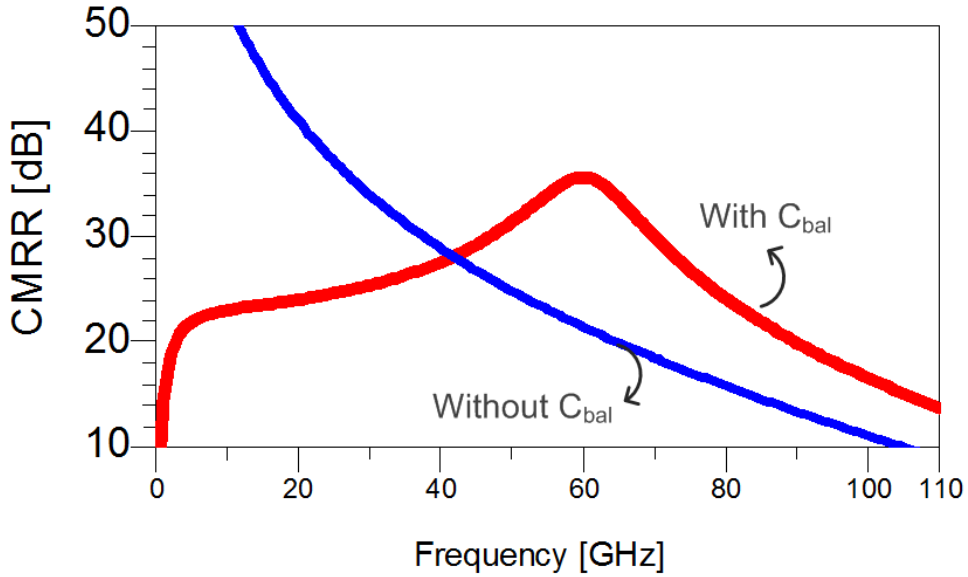


Figure 4-20 Impact of the capacitor C_{bal} on the simulated CMRR of the balun.

2.2 Power Combiner design

As CMOS technologies scale, it becomes more and more troublesome to conjugate high output power and a good linearity within a PA. One alternative to improve this compromise is the use of parallel architectures and power combiners.

For a 4-way combination, in particular, two architectures employing mm-wave transformers stand out: pure voltage combining and mixed current and voltage combining [LAI10]. For simplicity of analysis, the transformer model of Figure 4-21 was considered in this study. Whereas it neglects important aspects such as the inter-winding capacitances, it is sufficient to assess the main aspects in the operation of the considered topologies. The global schematics of the two power combining structures integrating this transformer model are presented in Figure 4-22 andFigure 4-23.

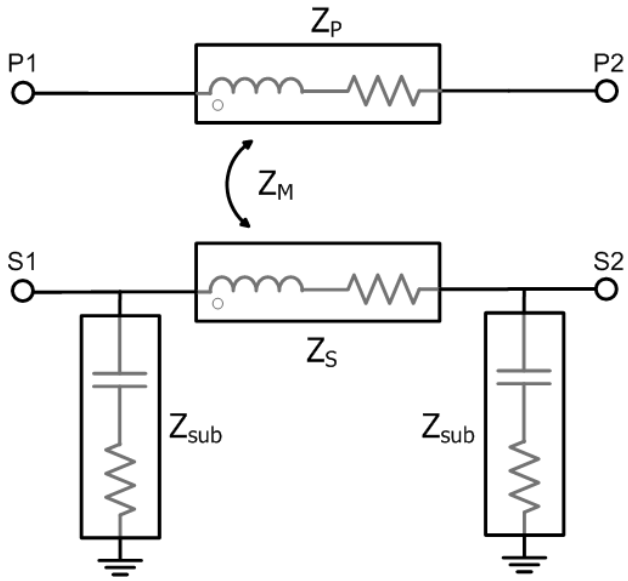


Figure 4-21 Simplified transformer model for combining analysis.

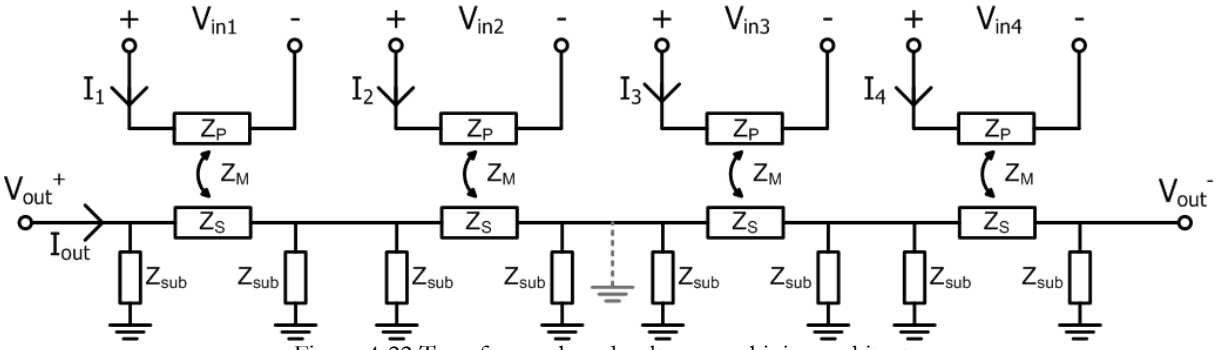


Figure 4-22 Transformer-based voltage combining architecture.

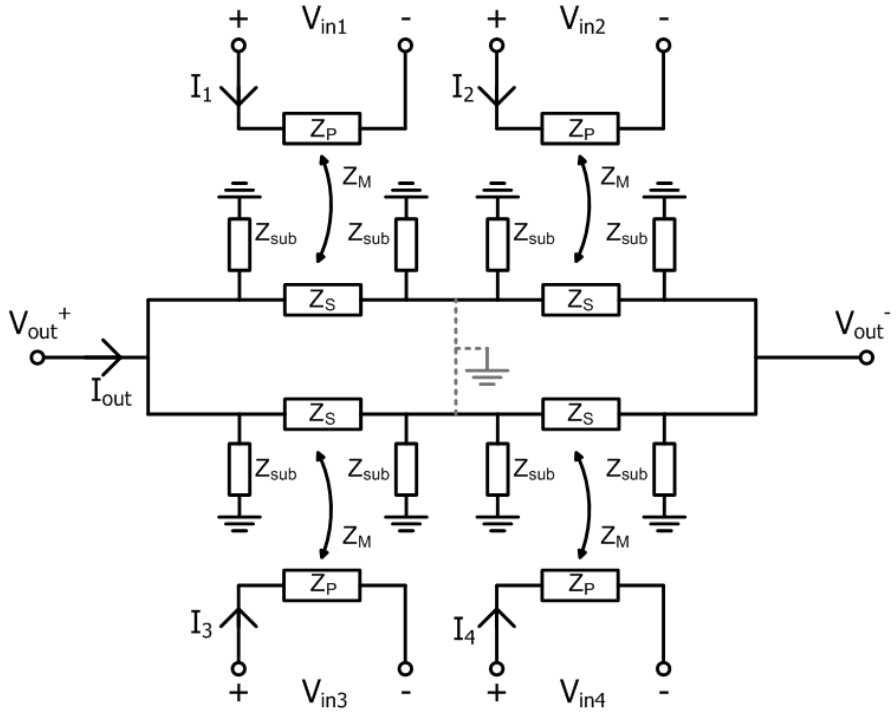
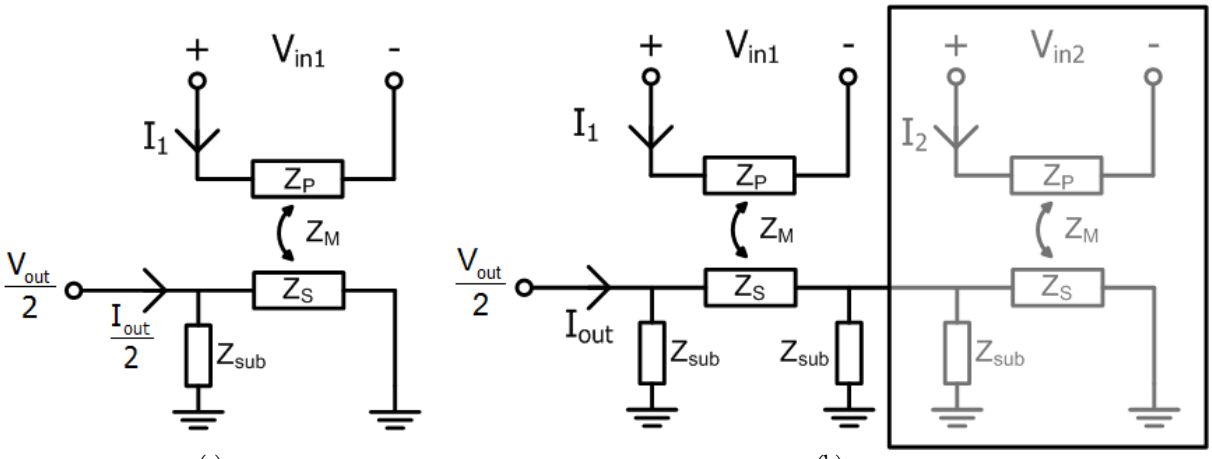


Figure 4-23 Transformer-based current-and-voltage combining architecture.

Due to the symmetry of their constructions, both circuits engender the introduction of virtual grounds among their secondaries. As a consequence, their global operations can be completely represented by the equivalent schematics of Figure 4-24.

By observing the constitution of their schematics, it can be inferred that the currents crossing all four primaries in the current-and-voltage combining structure are identical. For the pure voltage combining topology, nevertheless, inspection of the equivalent schematic suggests that I_1 and I_2 should have different values due to the unequal impedances at the terminals of each secondary, which is translated as well into different secondary currents and voltages. As a result of this observation, since the summation of complex quantities is maximum when they present the same phase, the current-and-voltage combining architecture is expected to provide a superior output power.



(a) (b)

Figure 4-24 Equivalent model of the (a) current-and-voltage combining, and the (b) voltage combining architectures.

In order to verify this assumption, we have calculated the output power provided by the power combiners. In this investigation, we considered that the applied load is matched to the output impedance of the circuits to provide maximum power transfer. Under such conditions, the output power calculation follows equation (4-23), where V_{eq} represents the equivalent open-circuit voltage in each circuit and R_{Load} the real part of their equivalent impedances.

$$P_{out} = \frac{\left|V_{eq}\right|^2}{R_{Load}} \tag{4-23}$$

The calculation of the Thevenin impedance and voltage Z_{IV} and V_{IV} of the current-and-voltage combining circuit was then performed according to (4-24) and (4-25).

$$Z_{IV} = Z_{sub} // \left(Z_S - \frac{Z_M^2}{Z_P} \right) \tag{4-24}$$

$$V_{IV} = 2V_{IN} \cdot \left(\frac{Z_S}{Z_M} + \frac{Z_M - \dfrac{Z_P Z_S}{Z_M}}{Z_P - \dfrac{Z_M^2}{Z_{sub} + Z_S}} \right) \tag{4-25}$$

Considering that the right-hand portion of the voltage combiner cell corresponds to a reproduction of the current-and-voltage combining equivalent cell, their equivalent impedance and voltage Z_V and V_V were computed as follows.

$$Z_V = 2 \cdot \left[Z_{sub} // \left(Z_S - \frac{Z_M^2}{Z_P} + Z_{sub} // Z_{IV} \right) \right] \tag{4-26}$$

$$V_V = \frac{V_{IV}}{1 - \dfrac{1}{2} \cdot \left(\dfrac{Z_P Z_{sub}}{Z_P Z_{sub} + Z_P Z_S - Z_M^2} \right)^2} \tag{4-27}$$

Therefore, the equivalent output power ratio comparing the two considered structures was obtained according to equation (4-28).

$$\frac{P_{IV}}{P_V} = \frac{|V_{IV}|^2 / R_{IV}}{|V_V|^2 / R_V} \tag{4-28}$$

In the performed analysis, the values of the components in the simplified transformer model were computed through the use of the analytical equations described in Chapter 3. The obtained results at 60 GHz, covering a wide range of physical dimensions, are depicted in Figure 4-25 and show an output power ratio superior to unity in the totality of the cases. Therefore, we conclude that the use of a current-and-voltage combining architecture is advantageous for the intended application.

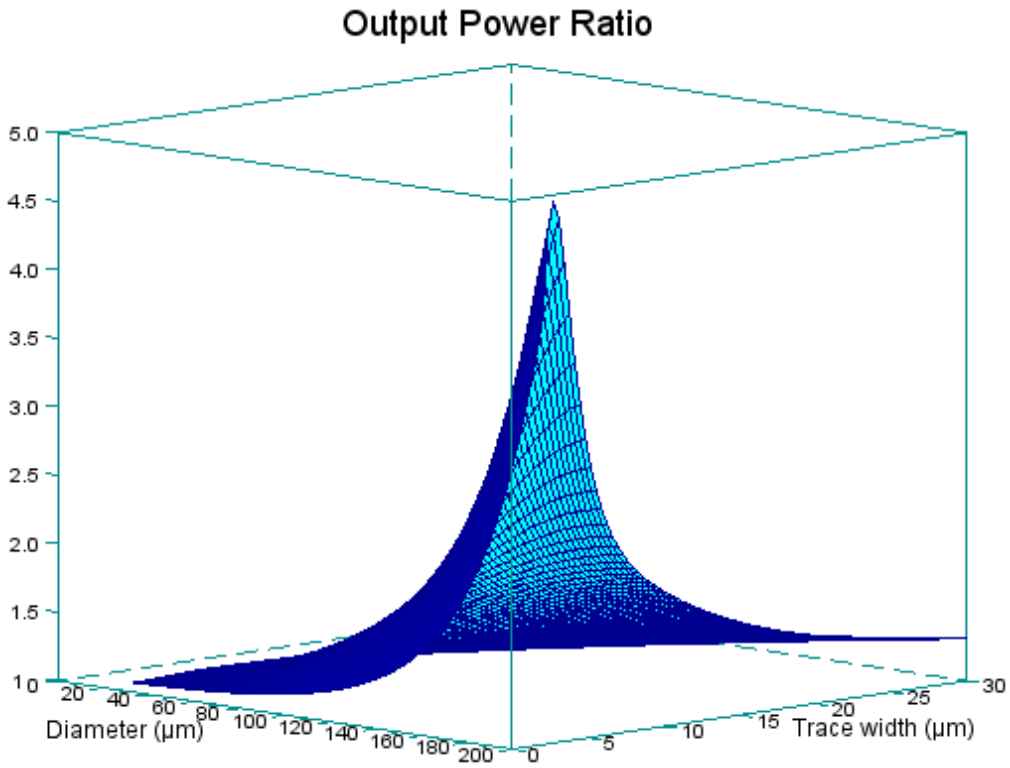


Figure 4-25 Output power ratio between current-and-voltage and pure voltage combining architectures.

Once the architecture of the transformer-based power combiner defined, its layout could be drawn. The 3-D view of the component is displayed in Figure 4-26. It can be noted how adjacent primaries are orthogonally placed in order to minimize negative coupling between segments.

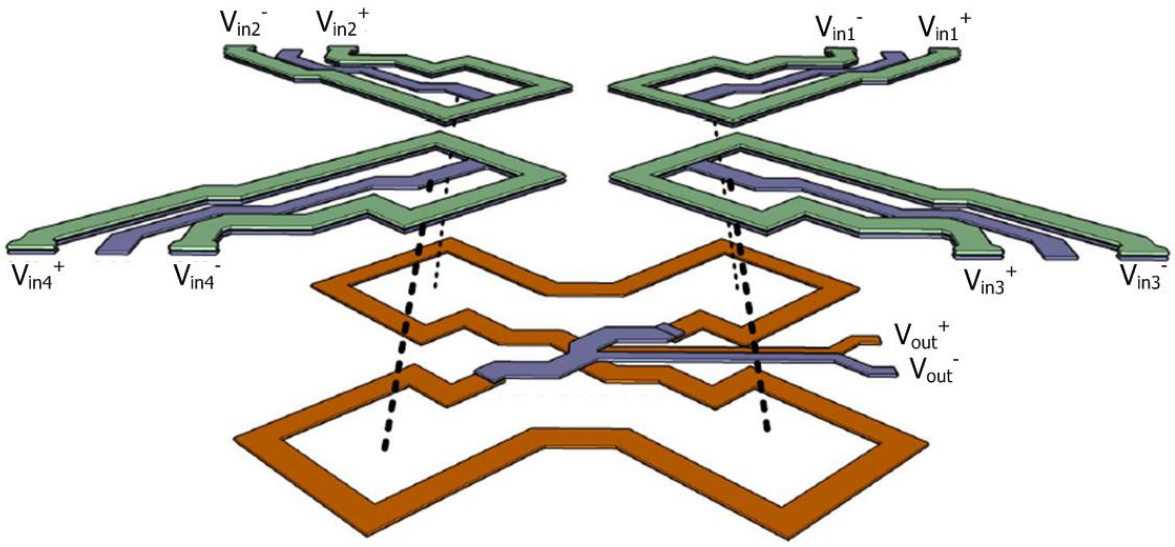


Figure 4-26 3-D view of the designed power combiner.

2.3 Power Splitter design

A 1:4 splitter was used to spread power between the output of the PPA and the parallel inputs of the unit amplifiers in the power stage. The power splitter was implemented through the use of transmission lines, including both coplanar waveguides and microstrips. As the isolation between adjacent output paths was insufficient, each output of the designed splitter was associated to a transformer-based balun, as it is displayed in the architecture description (Figure 4-15). Figure 4-27 shows how the isolation is improved by 16 dB through the use of these baluns. This improvement, however, comes at the expense of an increased insertion loss (Figure 4-28).

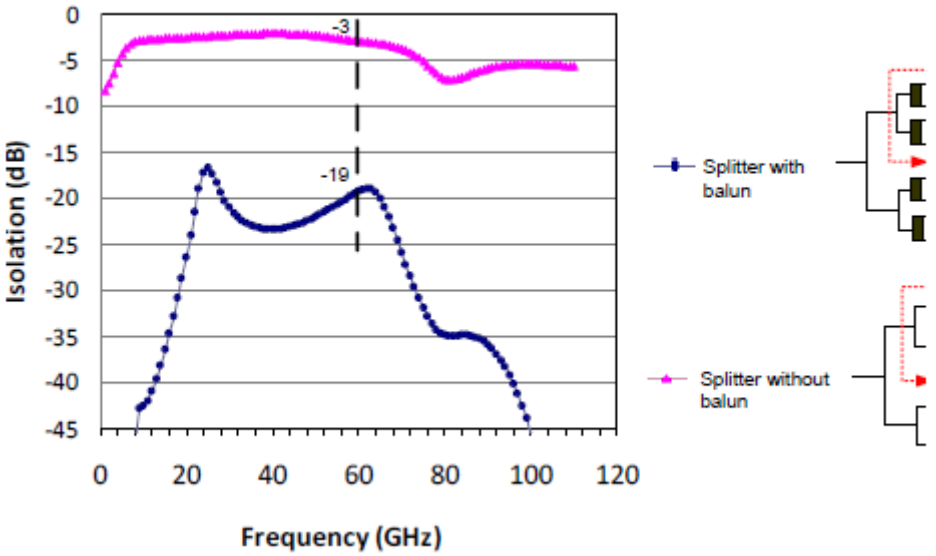


Figure 4-27 Simulated splitter's isolation coefficient with or without an associated balun.

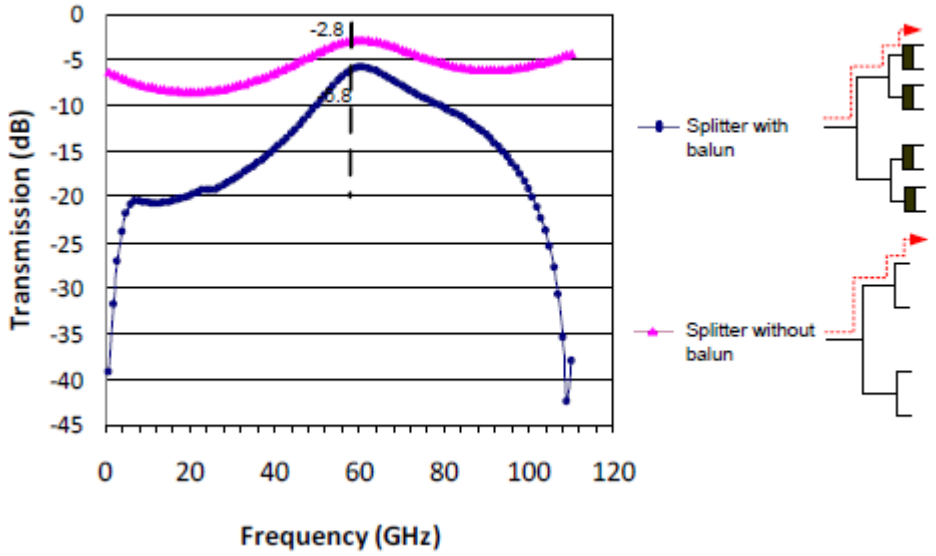


Figure 4-28 Simulated splitter's transmission coefficient with or without an associated balun

2.4 Unit PA design

The PA unit cells used in this circuit present a pseudo-differential architecture. A half-part of these cells is depicted in Figure 4-29, which consists in a two-stage common source topology. Class A operation is achieved thanks to a bias voltage V_{GS} equal to 0.95 V and a supply voltage V_{DD} of 1.2 V. The transistors M_1 and M_2 were respectively sized with 48 and 90 fingers. In both cases, the fingers are dimensioned 1-µm wide.

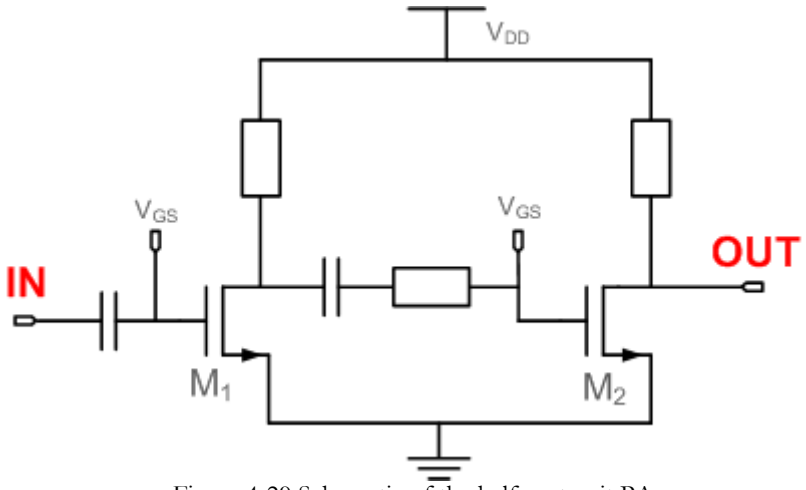


Figure 4-29 Schematic of the half-part unit PA.

2.5 Measurement results

The micrograph of the fabricated PA is depicted in Figure 4-30. The chip size is 2.25 mm² including pads. Scattering parameter measurements were carried out using an Agilent E83612 Vector Network Analyzer, whereas large signal measurements were made using a Focus load-pull system.

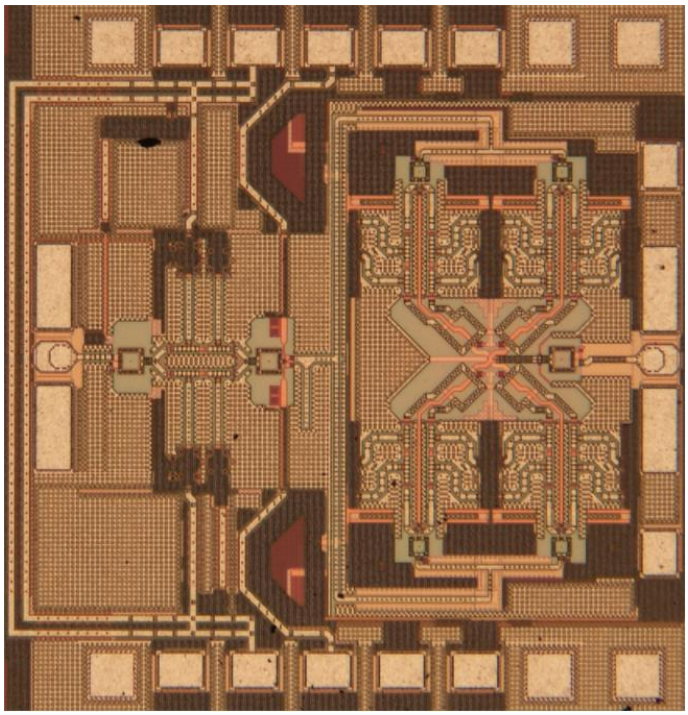


Figure 4-30 Micrograph of the mm-wave PA.

Measured and simulated S-parameters are displayed in Figure 4-31. Using a 1.2 V supply, a 20-dB maximum gain is achieved at 61 GHz. A 7-GHz 3-dB bandwidth is obtained, in the range between 57 GHz and 64 GHz. Moreover, isolation is found to be better than 47 dB over the whole considered band.

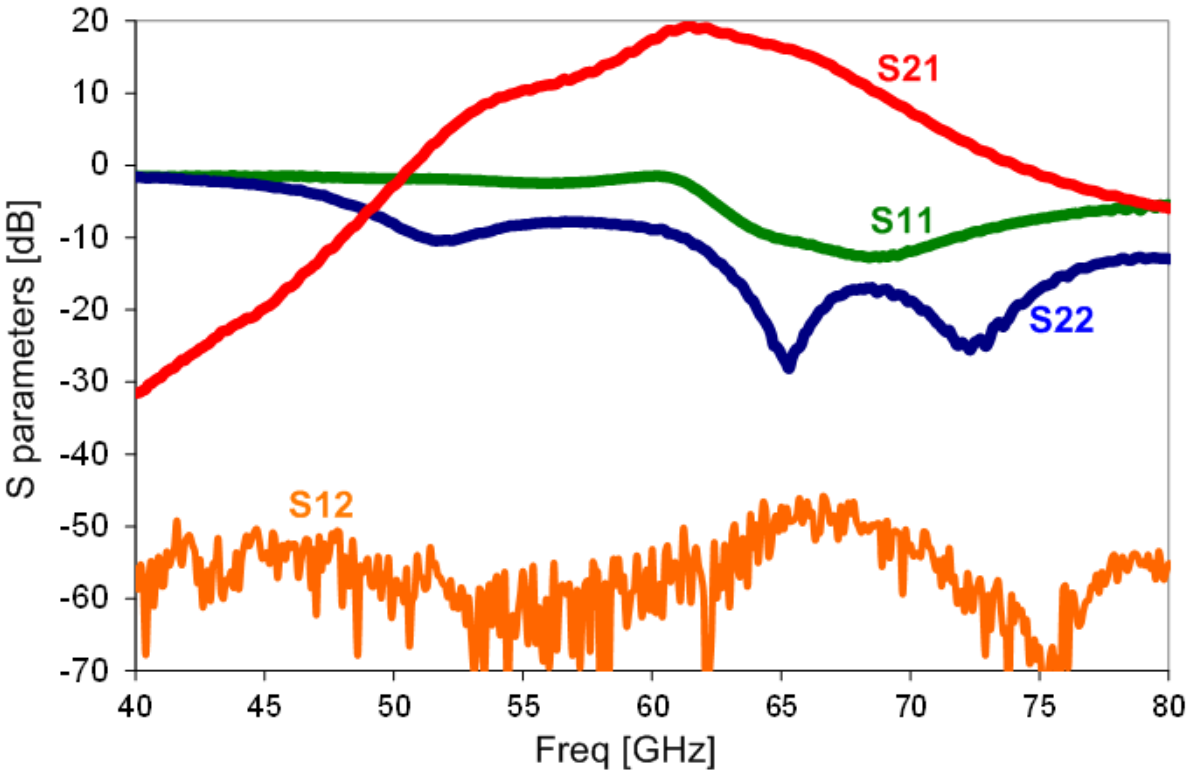


Figure 4-31 Simulated and measured S-parameters of the PA.

Large-signal parameters of the PA are displayed in Figure 4-32. Those results were obtained at 61 GHz for 50-Ω loads. The linearity of the circuit, which is directly dependent of common mode rejection, is evaluated by its output 1-dB compression point (OCP_1), which is shown to be as high as 13.5 dBm, whereas the saturated power (P_{Sat}) is 15.6 dBm for a 400-mA bias current consumption. Moreover, the maximum power added efficiency of the PA at 61 GHz is equal to 6.6%.

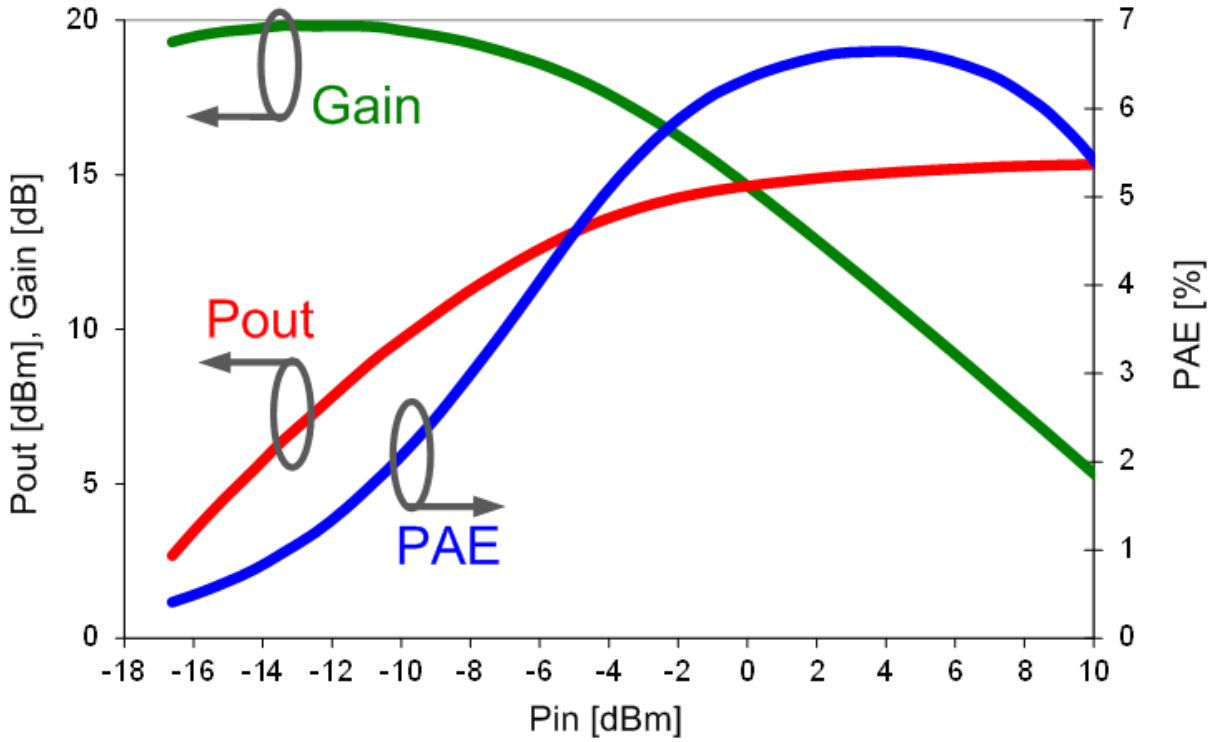


Figure 4-32 Simulated and measured large-signal parameters of the PA.

The measurement results of the presented PA are summarized in Table 4-4, along with other state-of-the-art 65-nm CMOS PAs. This table includes the ITRS FoM, which is defined in (4-29) [ITR09-2]. It takes into account the gain, output power and *PAE*, but not the linearity of the PA.

$$FoM_{PA} = f^2 \cdot Gain \cdot P_{Sat} \cdot PAE \tag{4-29}$$

From the displayed results it can be observed that the PA designed in this work has the third best FoM among the presented amplifiers, presenting noticeably the second highest gain, inferior only by 0.3 dB to the one achieved by [CHE11]. The linearity of the proposed circuit is highlighted by the third best OCP_1 among the considered PAs as well. The superior performance of [CHE11] and [LAI10] can be partly attributed to the fact that both designs employ general purpose (GP) transistors which provide a higher gain in comparison to the lower cost alternative represented by low power (LP) transistors used in our design. Moreover, in [LAI10], a more costly BEOL comprising 10 metal layers is used, which is beneficial for passive performance as well.

Table 4-4 Summary of 60-GHz 65-nm CMOS PA performances.

Ref.	Power combination	Gain (dB)	P_{Sat} (dBm)	OCP_1 (dBm)	PAE (%)	FoM_{PA} ($W.GHz^2$)
[CHA10]	no	16	11.5	5	15.2	308
[QUE10]	no	13.4	13.8	12.2	7.6	134
[LAI10]	yes	19.2	17.7	15.1	11.1	1957
[CHE11]	yes	20.3	18.6	15	15.1	4220
[HE10]	yes	10.2	14	10.8	7.2	64
[MAR10-2]	yes	14.3	16.6	11	4.9	221
[MAR10-2]	yes	15.5	18.1	11.5	3.6	302
This work	yes	20	15.6	13.5	6.6	892

3 Conclusion

This chapter presented the application of the investigations previously discussed within this thesis to the design of mm-wave integrated circuits. Two distinct building blocks were developed, targeting different bands and employing different technologies.

Firstly, a double balanced down-converter mixer was designed. It aims at both automotive short and long range radars. The adopted technology was 130-nm BiCMOS from STMicroelectronics. As the input ports of the active core of the mixer present a differential form, a transformer has been designed to operate as a balun. The simulated results of the balun display a very wideband behavior, presenting an amplitude imbalance better than 1 dB, a phase imbalance inferior to 3° and an insertion loss lower than 3 dB in the whole 60-120 GHz range. The developed balun was then incorporated into the mixer's input matching network. The design of this network was carried out using an alternative simplified transformer model, which was associated to transmission lines and capacitors. A 12-GHz bandwidth was then achieved, corresponding to a reflection coefficient lower than -10 dB in the 74-86 GHz range. Thanks to the low-loss, balanced performance of the transformers, the mixer obtained a 13.8-dB noise figure, an 18.5-dB conversion gain and a 1-dB compression point of -13 dBm, which resulted in the second best global performance among the reported state-of-the-art 77-GHz SiGe mixers, as well as the lowest power consumption.

Secondly, a power amplifier targeting 60-GHz WPANs and WLANs was designed using 65-nm CMOS technology. The PA presents a parallel architecture and makes comprehensive use of transformers. It includes 7 transformer-based baluns along with a transformer-based power combiner. The baluns employed in this PA have been optimized from the topology used within the mixer. A model-based analysis was carried out showing that the addition of a serial capacitor on the port which would traditionally be grounded in the single-ended winding leads to better common mode rejection. Moreover, this capacitor can be dimensioned to optimize balance at a given frequency of interest. The power combiner is used to gather the power from 8 parallel

amplifying cells. It adopts a mixed voltage and current combining topology. It is demonstrated through a model-based analysis that the use of this kind of topology allows obtaining a higher output power than pure voltage combiners. The use of such optimized topologies allowed the PA to present a 20-dB gain, a 15.6-dBm saturated power, a 6.6% PAE and a 1-dB compression point of 13.5 dBm. Those results place the designed PA as the third best performance among 65-nm CMOS state-of-the-art amplifiers at 60 GHz.

Conclusion

1 Summary

As new applications emerge in mm-waves, more and more interest has been drawn to the design of transceivers in this frequency range. Due to the recent evolution on the frequency capabilities of silicon-based technologies, they have become a suitable candidate to the implementation of building blocks of those transceivers. Transformers, in particular, can constitute a quite useful component in the design of such integrated circuits.

The most significant current applications for mm-wave wireless communications have been presented in this thesis. The WPAN and WLAN operating around 60 GHz, for instance, are of utmost importance. According to the geographic location, up to 9 GHz are available for unlicensed use at this frequency band, which stimulated the creation of standards such as ECMA 387, IEEE 802.15.3c, WirelessHD, WiGig, and IEEE 802.11ad. One major practical use for them is the short-range streaming of uncompressed video. Millimeter-wave automotive radar has been developed as well. Long range radar addressing automatic cruise control systems has been implemented at 76 – 77 GHz, whereas short range radar is being developed to supply a number of security features between 77 and 81 GHz. Moreover, mm-wave imaging, especially at 94 GHz, has been rising, aiming, among others, at medical and security applications, such as concealed weapon detection.

Important issues regarding transformer design have been discussed in this thesis as well. Investigations based both in measurement and electromagnetic simulation were made, using two technologies from STMicroelectronics: a 65-nm CMOS and a 130-nm BiCMOS optimized for mm-wave operation. Regarding the topology of transformers, a stacked configuration was shown to present better performances than a planar one, both in terms of magnetic coupling and insertion loss. Winding shape was analyzed, and octagonal layouts were shown to lead to better quality-factors. Square windings, nevertheless, might be an interesting alternative at certain cases, depending on the desired impedance values of the windings. Moreover, flipped and non-flipped topologies were compared. While non-flipped transformers present a flatter wideband behavior, the flipped topology may frequently provide a more convenient layout within a circuit. Two substrate shielding structures were then compared: patterned ground shields and floating shields. PGSs are frequently used to improve quality-factors of RF transformers, but their use at mm-waves leads to a degradation of the Q-factors and the global performance of the transformers. Floating shields, on the other hand, have only provided minor improvements to quality-factors in comparison to unshielded transformers. Finally, a design technique was proposed to allow

obtaining high transformation ratios in mm-waves. Since the number of turns of a winding is in practice limited to 2 at mm-waves, primary and secondary widths and diameters are separately set to provide additional impedance transformation. This technique has also the advantage of reducing the insertion loss of the transformer in a large number of cases.

A precise modeling is crucial for an effective use of transformers in mm-wave ICs. Electromagnetic simulations, if correctly configured, can accurately represent the behavior of passive structures employing a reasonable amount of computational resources. This thesis described the setup and the various simplifications associated to the designed mm-wave transformers, showing a very close agreement to measurement results. Such simulations, however, remain relatively time-consuming if compared to simple electric circuit simulations. For this reason, a lumped-element model has been proposed. It presents a 2-π topology, which provides a favorable trade-off between model simplicity and distributed modeling. All elements are calculated from analytical equations depending on the physical dimensions of the transformers and the material properties specific to the employed technology. These equations combine a physics-based form with a small number of simulation and measurement-based weighting factors. The scalability and accuracy of the model are verified by comparison to measurement of transformers presenting a diversity of topologies and dimensions for both 65-nm CMOS and 130-nm BiCMOS technologies over a wide band. This model was subsequently integrated into a parametric cell within circuit design environment.

Two mm-wave building blocks were developed integrating a number of integrated transformers designed in this thesis. The first of them was a 130-nm BiCMOS double balanced active mixer targeting automotive radar. As the circuit inputs were fed single-endedly, transformers were used to convert them to a balanced form at the active core of the circuit. The transformer was carefully sized to provide amplitude and phase imbalances respectively inferior to 1 dB and 3°. This transformer was then integrated within the input matching network of the mixer, which, thanks to the use of a transformer simplified model, allowed the desired matching in the band comprised between 74 and 86 GHz. The proposed circuit presented the lowest power consumption among state-of-the-art 77 GHz SiGe mixers (80 mW), as well as the second highest figure of merit. The design of integrated transformers to operate in a power amplifier was described as well. The PA was designed at 65-nm CMOS to operate at 60 GHz. This PA employed several transformer-based baluns and a transformer-based power combiner at its output. The balun structure was optimized, associating a capacitor to the integrated transformer, and the combiner used a mixed current-and-voltage combining architecture. Simplified transformer models were used to demonstrate the advantages of the adopted topologies over traditional baluns, as the one used in the mixer, and pure voltage combiners. The PA presented a high gain (20 dB) and a good linearity (13.5 dBm OCP_1), resulting in the third best global performance among 60-GHz state-of-the art 65-nm CMOS PAs.

2 Future research

Transformer experimental characterization in this work was carried out through small-signal 2-port measurements using fixed 50 Ω impedances at both transformer ends. A model was then derived demonstrating a close agreement to experimental results. A more comprehensive characterization would include 3 and 4-port measurements, in addition to the already performed EM simulations. Moreover, an investigation on the transformer behavior for different impedance values would constitute another valuable perspective. Source and load-pull measurements could be carried out and the model could be adapted accordingly to ensure scalability in terms of impedances as well.

The design of the mixer and the PA highlighted a significant limitation of the proposed model: it does not take into account a center-tap connection. Since the balun function is a major asset of integrated transformers, it is highly desirable that this element of their operation be modeled as well. Another relevant prospective work would consist therefore in revamping the proposed model, carefully separating the elements from each half-winding and then including the corresponding coupling elements between these halves.

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Appendix A : Data rates and modulation schemes for 60-GHz wireless standards

Table A-1 Data rates and modulation schemes for ECMA 387 operating modes.

Mode	Base data rate (Gbit/s) Number of bonded channels				Modulation	
	None	2	3	4		
A0	0.397	0.794	1.191	1.588	SC	BPSK
A1	0.794	1.588	2.381	3.175	SC	BPSK
A2	1.588	3.175	4.763	6.35	SC	BPSK
A3	1.588	3.175	4.763	6.35	SC	QPSK
A4	2.722	5.443	8.165	10.886	SC	QPSK
A5	3.175	6.35	9.256	12.701	SC	QPSK
A6	4.234	8.467	13.701	16.934	SC	8QAM
A7	4.763	9.256	14.288	19.051	SC	8QAM
A8	4.763	9.256	14.288	19.051	SC	16QAM
A9	6.35	12.701	19.051	25.402	SC	16QAM
A10	1.588	3.175	4.763	6.35	SC	QPSK
A11	4.234	8.467	12.701	16.934	SC	16QAM
A12	2.117	4.234	6.35	8.467	SC	QPSK
A13	4.234	8.467	12.701	16.934	SC	16QAM
A14	1.008	—	—	—	OFDM	QPSK
A15	2.016	—	—	—	OFDM	QPSK
A16	4.032	—	—	—	OFDM	16QAM
A17	2.016	—	—	—	OFDM	QPSK
A18	4.032	—	—	—	OFDM	16QAM
A19	2.016	—	—	—	OFDM	QPSK
A20	4.032	—	—	—	OFDM	16QAM
A21	2.016	—	—	—	OFDM	QPSK
B0	0.794	1.588	2.381	3.175	SC	BPSK
B1	1.588	3.175	4.763	6.35	SC	BPSK
B2	3.175	6.35	9.526	12.701	SC	QPSK
B3	3.175	6.35	9.526	12.701	SC	QPSK
B4*	3.175	6.35	9.526	12.701	SC	DAMI
C0*	0.8	—	—	—	SC	OOK
C1*	1.6	—	—	—	SC	OOK
C2*	3.2	—	—	—	SC	4ASK

* Only present in the first edition.

Table A-2 Data rates and modulation schemes for IEEE 802.15.3c operating modes.

Mode	Index	Base data rate (Gbit/s)	Modulation	
SC	0	0.026	SC	BPSK/(G)MSK
	1	0.412	SC	BPSK/(G)MSK
	2	0.825	SC	BPSK/(G)MSK
	3	1.650	SC	BPSK/(G)MSK
	4	1.320	SC	BPSK/(G)MSK
	5	0.440	SC	BPSK/(G)MSK
	6	0.880	SC	BPSK/(G)MSK
	7	1.760	SC	QPSK
	8	2.640	SC	QPSK
	9	3.080	SC	QPSK
	10	3.290	SC	QPSK
	11	3.300	SC	QPSK
	12	3.960	SC	8PSK
	13	5.280	SC	16QAM
	OOK	0.818	SC	OOK
	OOK	1.640	SC	OOK
	DAMI	3.270	SC	DAMI
HSI	0	0.032	OFDM	QPSK
	1	1.540	OFDM	QPSK
	2	2.310	OFDM	QPSK
	3	2.695	OFDM	QPSK
	4	3.080	OFDM	16QAM
	5	4.620	OFDM	16QAM
	6	5.390	OFDM	16QAM
	7	5.775	OFDM	64QAM
	8	1.925	OFDM	QPSK
	9	2.503	OFDM	QPSK
	10	3.850	OFDM	16QAM
	11	5.005	OFDM	16QAM
AV-HRP	0	0.952	OFDM	QPSK
	1	1.904	OFDM	QPSK
	2	3.807	OFDM	16QAM
	3	1.904	OFDM	QPSK
	4	3.807	OFDM	16QAM
	5	0.952	OFDM	QPSK
	6	1.904	OFDM	QPSK
AV-LRP	0	0.003	OFDM	BPSK
	1	0.004	OFDM	BPSK
	2	0.005	OFDM	BPSK
	3	0.010	OFDM	BPSK

Table A-3 Data rates and modulation schemes for WirelessHD operating modes.

Mode	Index	Base data rate (Gbit/s)	Modulation	
HRP	0	0.952	OFDM	QPSK
	1	1.904	OFDM	QPSK
	2	3.807	OFDM	16QAM
	3	1.904	OFDM	QPSK
	4	3.807	OFDM	16QAM
	5	0.952	OFDM	QPSK
	6	1.904	OFDM	QPSK
	7	1.428	OFDM	QPSK
	8	2.379	OFDM	QPSK
	9	2.855	OFDM	16QAM
	10	4.759	OFDM	16QAM
	11	5.711	OFDM	64QAM
	12	7.138	OFDM	64QAM
	13	1.428	OFDM	QPSK
	14	2.855	OFDM	16QAM
	15	5.711	OFDM	64QAM
MRP	0	0.476	OFDM	QPSK
	1	0.952	OFDM	QPSK
	2	1.904	OFDM	16QAM
	3	0.952	OFDM	QPSK
	4	1.904	OFDM	16QAM
	5	0.476	OFDM	QPSK
	6	0.952	OFDM	QPSK
	7	0.714	OFDM	QPSK
	8	1.190	OFDM	QPSK
	9	1.428	OFDM	16QAM
	10	0.714	OFDM	QPSK
	11	1.428	OFDM	16QAM
LRP	0	0.003	OFDM	BPSK
	1	0.004	OFDM	BPSK
	2	0.005	OFDM	BPSK
	3	0.010	OFDM	BPSK

Table A-4 Data rates and modulation schemes for IEEE 802.11ad and WiGig operating modes.

Mode	Index	Base data rate (Gbit/s)	Modulation	
SC	1	0.385	SC	BPSK
	2	0.770	SC	BPSK
	3	0.962	SC	BPSK
	4	1.155	SC	BPSK
	5	1.251	SC	BPSK
	6	1.540	SC	QPSK
	7	1.925	SC	QPSK
	8	2.310	SC	QPSK
	9	2.502	SC	QPSK
	10	3.080	SC	16QAM
	11	3.850	SC	16QAM
	12	4.620	SC	16QAM
OFDM	13	0.693	OFDM	QPSK
	14	0.866	OFDM	QPSK
	15	1.386	OFDM	QPSK
	16	1.732	OFDM	QPSK
	17	2.079	OFDM	QPSK
	18	2.772	OFDM	16QAM
	19	3.465	OFDM	16QAM
	20	4.158	OFDM	16QAM
	21	4.504	OFDM	16QAM
	22	5.197	OFDM	64QAM
	23	6.237	OFDM	64QAM
	24	6.757	OFDM	64QAM
Low-Power SC	25	0.626	SC	BPSK
	26	1.251	SC	BPSK
	27	2.502	SC	QPSK