# THÈSE

présentée à

## L'UNIVERSITÉ BORDEAUX 1

ÉCOLE DOCTORALE DE SCIENCES PHYSIQUES ET DE L'INGENIEUR

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POUR OBTENIR LE GRADE DE

## DOCTEUR

SPÉCIALITÉ : ELECTRONIQUE

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# Contribution to the Built-In Self-Test for RF VCOs

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Soutenue le: 26 Mars 2010

Après avis de:

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-2010-

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# INTRODUCTION

*A. The market of wireless microelectronics – explosion and related problems*

Starting from the mid-90's, the wireless telecommunication market has experienced an unstopped growth, powered by people's need to be connected, wherever they are, to the rest of the world.

While this connection was initially mainly restricted to voice transmission, other applications began to appear a few years later. We can now exchange data, images and videos thanks to the increased bandwidth reached by wireless transceivers.

This explosion pushed Integrated Circuits (IC) designers to focus their efforts on the study of new highly-performing Radio Frequency (RF) systems. The need for these new applications to be accessible to everyone created a demand for low-cost solutions.

High performance calls for complicated solutions, while low-cost calls for miniaturization and low-power consumption. This mixture of extremely complicated and miniaturized ICs kept growing and growing each year.

The RF designers, blinded by new possibilities never before imagined, forgot one major issue: the testability of their systems, unfortunately enhanced neither by complexity nor by miniaturization.

The point has now been reached where the test of RF circuits is becoming one of the less-trivial and most expensive steps in the development and characterization of commercially available transceivers.

*B. The motivation to implement Built-In Self-Test capabilities on RF ICs*

The first step in the realization of any commercial IC is the manufacturing; the result of this phase is a wafer, containing multiple instances of the IC. Before cutting the wafer to extract the IC and put it into a package, the circuit is tested on wafer.

This work focuses on lowering the cost of this step and on solving some major problems that arise when a RF circuit is the Circuit Under Test (CUT).

The production flow of an IC, together with the tests performed at each step, is shown in Figure 1.

During the design of the IC, the designer performs statistical simulations to guarantee that the circuit respects the specifications not only for nominal conditions but also for every corner case: fast and slow processes, high and low temperature, high and low supply voltage (PVT simulations).

Post-Layout Simulations are carried out to assure that the influence of parasitic elements does not degrade the performance of the IC, in terms of speed, output power, consumption, noise and operating frequency.

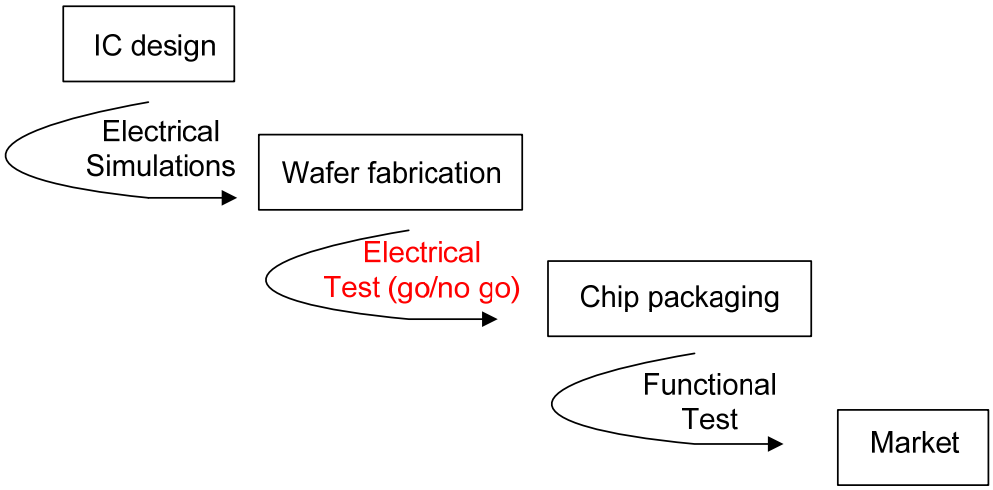


**Figure 1: IC flow - form the design to the market**

The description of the circuit is then sent to the foundry, where the wafer is fabricated. A wafer sort test is performed: it allows discriminating between good and faulty (malfunctioning) circuits. Faulty circuits are discarded and do not reach the packaging step. If a RFIC is the object of the test, many problems arise.

The three major issues are: the Automatic Test Equipment (ATE) needed to carry out a wafer test on RF circuits is very expensive; the risk of signal distortion and degradation when driving the signal off the die is high; the time needed to setup the wafer sort is very long.

All of the above problems cause a tremendous rise in the cost of the wafer test and a loss in accuracy of the test results. Sometimes, because of its complexity, the wafer sort is not performed on the RF section of the IC. Faulty circuits can then pass to the following step.

The ICs that pass the wafer test are encapsulated in a package. At this level also, the IC is tested, to be sure that it respects the specifications. Functional tests are performed, in which measurements such as the gain, noise figure and linearity of LNAs or frequency of oscillation, frequency range and phase noise of VCOs are carried out.

Because of the increased complexity of actual ICs, the packaging is becoming more and more expensive. Its cost may even exceed die manufacturing costs [Sri06]. This implies that the interest of the industry is that each encapsulated IC passes the functional tests; this could be guaranteed if the wafer sort were able to discard 100% of faulty circuits.

Finally, the IC is ready to be sold in the market. In order to sell it at a very competitive price, the cost of each step described above has to be reduced. This can be efficiently achieved lowering the cost and augmenting the performance of the wafer sort; this is probably the step that has the greatest weight in the IC process flow. As a matter of fact, projections say that the test cost can become as high as 40% of the manufacturing cost of complex ICs [Bat04].

The solution to all the problems of the wafer test is to perform directly inside the die a test able to discriminate between a good and a faulty circuit, giving at the output a binary signal (1/0) that can easily be read by a cheap digital multimeter.
The only additional cost is the increased silicon surface; the test could be performed very quickly; any distortion of the signal could be avoided.
The cost to detect a defect increases at each step of the assembly line; it is then convenient for the industry to find any problem at the wafer test step. It would be a loss of money not to perform it. Since the on-chip test would become much easier to carry out, there would be no need to skip any RF section of the IC.

This kind of test is called Built-In Self-Test (BIST).
It is nowadays common practice to design some means of BIST for digital circuits. Long digital words are sent to the chip and its response is recorded and compared with the expected response of the fault-free circuit (usually called “golden response”).
The BIST for RF circuits is still in its early phase.
The need for always better performance and lower cost RFICs causes the industries to be skeptical in the realization of BIST implementations that inevitably consumes extra surface and power, and could slow down the time-to-market.
In the following chapters it will be shown that realizations of BIST strategies that do not degrade the performance of the CUT and do not interfere with its functioning are possible.

*Chapter 1* presents a wide panoramic of BIST strategies applied to RF circuits and systems. After a short explanation of the main causes of generation of defects, some existing proposals for the detection of the faults are introduced.
The primal role of on-chip detectors is shown. Different structures of current, power, amplitude sensors and frequency-meters are presented.
The choice of the Voltage-Controlled-Oscillator (VCO) as the CUT for this work is done. Its principle of operation, its role inside a transceiver and some implementations are explained.

*Chapter 2* deals with the choice of the BIST architecture and the design of the analog blocks needed for the test. A catastrophic and parametric fault injection is performed to identify the quantity to monitor for the maximization of the fault coverage.

A temperature and supply-voltage independent CMOS voltage reference, a Low DropOut voltage regulator, the VCO, the detector and the comparator will be presented in detail, with post-layout simulations validating the operation of each block and the functioning of the system as a whole.
A methodology is also proposed for the on-line self-correction of the CUT, making use of the BIST circuit as a part of the corrective system.

*Chapter 3* presents the measurements for the BIST strategy implemented.
During this PhD work, we took advantage of only one run (S65C9_2).
First, the main building blocks of the BIST are measured as stand-alone circuits.
The measurements of the temperature and supply-voltage independent CMOS voltage reference and of the detector are presented.
Then, the complete BIST architecture is measured and verified.
A short-circuit in the output buffer prevented the RF measurement of the VCO output to be carried out.
Nevertheless, it was possible to verify the good behavior of the BIST system, showing that the detector, the comparator and the final digital stage are capable of providing a logic pass/fail output for the wafer sort.

*Chapter 4* concludes this work. An introductory study on the possibility to completely on-chip characterize the VCO is proposed. This built-in functional test aims at the replacement of the external tests nowadays performed after the packaging step shown in Figure 1. A complete chip validation and the eventual diagnosis of the problems is possible on-chip.
A study on the most suitable frequency-meter architecture for on-chip accurate measurement of high-frequency signals is carried out via VHDL-AMS simulations.
The road is then opened to the use of the same structure for on-chip jitter measurements.

*References*

**[Sri06]** G.Srinivasan, A.Chatterjee, F. Taenzler, "Alternate Loop-Back Diagnostic Tests for Wafer-Level Diagnosis of Modern Wireless Transceivers using Spectral Signatures", Proceedings of the 24th IEEE VLSI Test Symposium, 2006

**[Bat04]** S.Bhattacharya, A.Chatterjee, "A Built-In Loopback Test Methodology for RF Transceiver Circuits Using Embedded Sensor Circuits", Proceedings of the 13th Asian Test Symposium, 2004

# Contents

# I. STATE-OF-THE-ART

## *I.1. Definitions used in the test domain*

Before starting to examine the different strategies for implementing a Built-In Self-Test, it is useful to remind some definitions frequently encountered in the test domain.

### *I.1.1 Defining defect, fault and failure*

Confusion arises when talking about a fault, or a defect, or a failure.

Those concepts can be clarified with a "daily life" example.

"Consider an automobile with one tire that has a weak spot on its road surface. The *defect* could be a result of corrosion or due to improper manufacture and inspection. A hole in the tire is a *fault*. Low tire pressure due to the hole is an *error*. A tire that is unfit for use leads to a *malfunctioning*. Even if the automobile does not tolerate any malfunctioning, one can still drive an automobile having a flat tire, but the performance is seriously *degraded*. Finally, as a result of the above sequence of events, the entire automobile system can *fail*." [Par97].

Let's try now to apply the same concept to a VCO for a PLL.

Consider a VCO that has a weak spot on the metal path connecting a varactor to the LC tank. The *defect* could be a result of electromigration. An open circuit in the path is a *fault*. Unbalance in the output of the VCO is an *error*. If the VCO is unfit for use leads to a *malfunctioning*. Even if the PLL does not tolerate the malfunctioning of the VCO, one can still use the PLL, but the performance is seriously *degraded*. Finally, as a result of the above sequence of events, the entire PLL can *fail*.

### *I.1.2 Defining catastrophic and parametric faults*

Faults are grouped in two main categories: catastrophic (hard) and parametric (soft) faults.

- Catastrophic faults are faults that cause a topological change in the circuit; those are usually open circuits and short circuits.
- Parametric faults are faults that do not affect the connectivity of the circuit; those are, for the most, variations of the dimensions of transistors and passive components due to a not-well controlled technology process.

Moreover, parametric faults are further categorized as global or local [Mil98].

- Global parametric faults occur when all active and passive components on the die are affected (high lot-to-lot variation).

- Local parametric faults occur because of local defect mechanisms (high die-to-die variation).

### *I.1.3 Mechanisms of generation of a defect*

There are multiple mechanisms that can generate a defect. Pushing the technology to its limits, those mechanisms become more and more relevant. Oxide breakdown, hot electrons, Negative Bias Temperature Instability (NBTI), electromigration or bad process control are some of them.
The defect causes degradation and eventually the failure of the CUT.
Oxide breakdown affecting a Low Noise Amplifier (LNA), for example, can cause the decrease of its gain, the increase of its noise figure and the frequency shift of its operating frequency [Li01].

#### *I.1.3.1 Hot electrons*

Electrons move with a velocity determined by the vector sum of the thermal velocity and the drift velocity; the latter component is due to the electric field applied between source and drain. The drift velocity is linearly dependent on the electric field, and the constant of proportionality is the mobility of the electron.
When a low field is applied, the thermal velocity is the dominant component of the total velocity.
At high fields, the drift velocity becomes comparable with the thermal velocity, and the total energy of the electron increases significantly. As the kinetic energy is related to temperature, such electrons are called “hot electrons”.
Some of those high-energy electrons may enter the silicon-dioxide conduction band, where they may be trapped. This has for effect a positive shift of the threshold voltage and a degradation of the transconductance of the transistor.

#### *I.1.3.2 Negative Bias Temperature Instability (NBTI)*

The stress under constant negative voltage on the gate of MOSFETs causes the generation of interface traps between the gate oxide and the silicon substrate. This phenomenon is accelerated by high temperatures.
NBTI is more critical in pMOS than in nMOS transistors for two main reasons: the presence of holes in the inversion layer - which are known to interact with the oxide states – and the fact that a negative bias on the gate terminal is rarely applied on nMOS transistors.
NBTI is a real issue for sub-130nm CMOS devices because of its deleterious effect on threshold voltage and drive current.
Increasing oxide fields, thin gate oxide and the use of oxynitrides (to prevent Boron penetration and to reduce gate leakage) have exacerbated this pMOS-specific reliability issue.

### *I.1.3.3 Electromigration*

The miniaturization of devices and interconnections entails the increase of the current density. This phenomenon leads to the transfer of momentum from the electrons to the positive ions of the metal lines, which causes a mass transport in the metal.

Over time, this force knocks a significant number of metal atoms far from their original position. A break or gap (known as “void”) can then be generated in the conducting metal leading to an open-circuit.

Metal atoms can also pile up and drift towards a nearby conductor, leading to a short-circuit (hillock failure), as shown in Figure I-1.

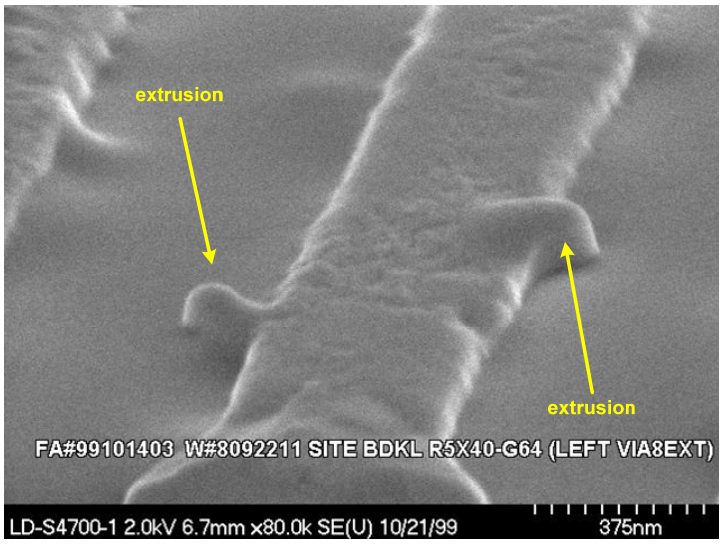


**Figure I-1: Extrusion caused by electromigration; this is a cause of short-circuit between metal paths.**

### *I.1.3.4 Oxide breakdown*

Oxide breakdown refers to the destruction of an oxide layer in a semiconductor device. Oxides become more vulnerable to the voltages applied to the device as they get thinner.

Oxide breakdown can be ESD induced; when a high voltage is applied across the oxide layer, a weak spot is created, allowing current to flow through the oxide.

Poor processing or uneven growth of the oxide is another cause of breakdown; presence of mobile sodium ions in the oxide, radiation damage and contamination are frequent causes of oxide breakdown.

Moreover, even very high quality oxides can suffer breakdown with time; this is called the Time-Dependent Dielectric Breakdown (TDDB).

The oxide breakdown, creating a path from gate to substrate, makes impossible the control of the current flowing from source to drain acting on the gate voltage.

### *I.1.4 Fault Coverage*

One of the most important metrics related to BIST applications is the fault coverage. It is defined as follows:

$$fault\ coverage = \frac{detected\ faults}{injected\ faults} \quad (1)$$

Ideally, a structural BIST should be able to detect every possible fault present inside the circuit, giving 100% fault coverage.

This concept is represented in Figure I-2. Some faulty circuits may pass the wafer sort; the fault coverage is maximized if their number is reduced to a minimum.

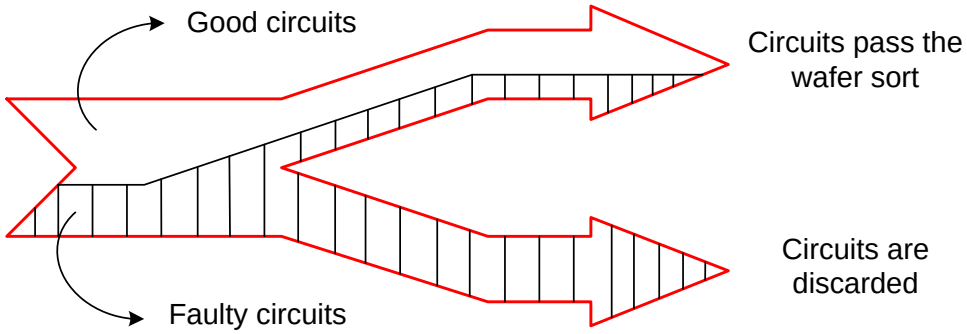


**Figure I-2: During the wafer sort, some faulty circuits can pass the test**

The designer injects faults in the circuit during simulations and determines if the BIST is able to detect every injected fault. The approach of injecting catastrophic and parametric faults into the circuit will be explained in the following chapter.

## *I.2. BIST strategies*

When talking about methodologies for BIST, two main strategies are possible: either a functional test or a structural test can be performed.

The main difference between the two is the goal of the test itself.

- A functional test targets the measurement of the specifications of a system. As an example, the gain, linearity and noise figure of an LNA or the frequency of oscillation, frequency range and phase noise of a PLL need to be directly measured on chip.
  If the result of the test is within the specifications given by the standard, the CUT passes the wafer test and it is not discarded.
- A structural test targets the detection of faults inside the CUT. As an example, open circuits and short circuits due to electromigration need to be detected. This is done through the monitoring of quantities such as DC or transient currents and voltages,

RMS power or frequency. It is assumed that, in the presence of a fault, those quantities deviate from their nominal value.

If this deviation can be measured on-chip, the structural test is able to screen out good circuits from faulty ones.

### *I.2.1 Functional Test (specification-based)*

As the name implies, this test aims at measuring the "function" which the CUT is devoted to.

During the wafer sort, the CUT on the wafer is tested to check if it respects the specifications. In the case of a RF circuit, expensive RF probes, RF coaxial cables and Vector Network Analyzers (VNA) are needed. Attention has to be paid not to degrade the signal or create perturbation of the circuit.

The goal of the functional test is to measure the specifications directly on-chip. The test outputs an analog signal giving the result of the measure, as shown in the right side of Figure I-3.

The measure is then read with simple and inexpensive multimeters and DC probes; the risk of perturbation or distortion of the signal is considerably lowered. Moreover, the presence of a human taking the pass/fail decision on the basis of the measurement is no more needed. A simple software can analyze the multimeter output and either reject or keep the CUT.

The most common techniques to carry out functional tests are now explained.

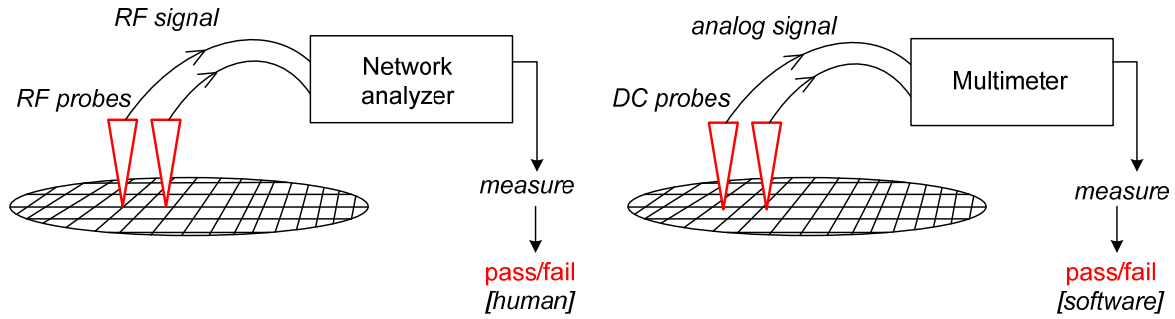


**Figure I-3: The functional test (right side) simplifies the classical measurement (left side) of the specifications of the CUT in the wafer.**

#### *I.2.1.1 Loopback Test*

This is a technique used to measure the specifications of complete transceivers.

Transceivers consist of the combination of a transmitter that up-converts the digital baseband information to RF and a receiver that down-converts the signal back to baseband.

As shown in Figure I-4, hooking the receiver to the transmitter results in a path with digital inputs and outputs sent and read from the DSP. The loop is usually closed using an attenuator, because the high power signal output from the Power Amplifier (PA) could not be sent directly to the LNA, which

does not have the appropriate dynamic range to directly handle the PA output. The digital baseband processor serves as the digital test patter generator and as the response analyzer.

This technique has the advantage of testing all of the blocks of the transceiver without affecting sensitive nodes and without introducing too much extra circuitry [Oze04].

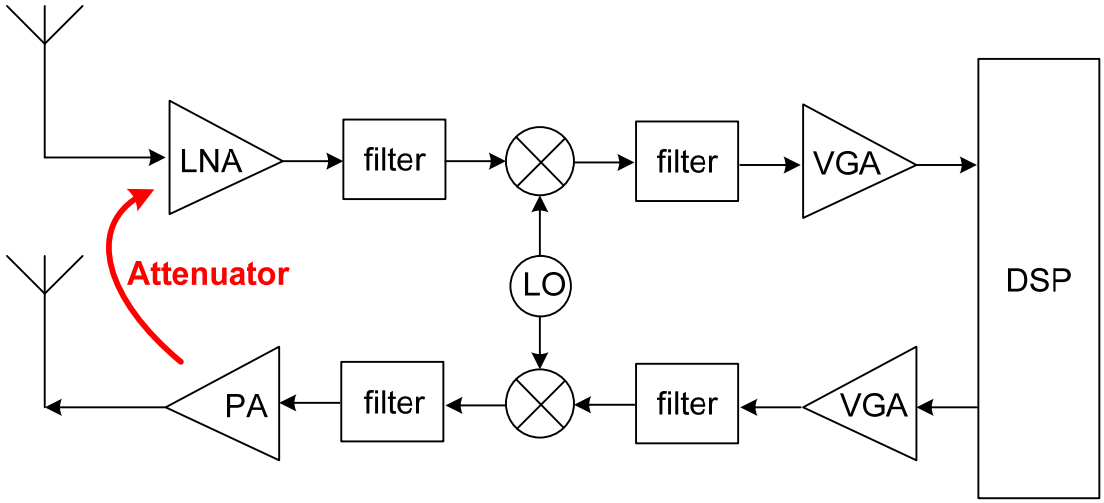


**Figure I-4: Simplified architecture of a transceiver; the ADC and the DAC are omitted.**

Depending on the architecture of the transceiver, multiple problems can arise that limit the use of the loopback technique.

1. Low-IF and wide-IF TDD transceivers share the same local oscillator (LO); this eliminates the possibility of true loopback simple signals. Even if switches were added to disconnect the LO either from TX or RX, this would cause the malfunctioning of the chain and alter the data.
2. Direct VCO modulation implies that the transmit signal is directly obtained from the LO output. A direct loopback would simply result in a DC-signal (self-mixing of the signal) at the output of the RX mixer. In the presence of DC-offset cancellation capacitors at the output of the mixer, the information is lost. Moreover, the DC-signal could saturate the stages following the mixer, altering the test data.

   The problem can be solved introducing a low-frequency ($f_{sw}$) switch between the PA and the LNA. Two additional tones at $f_{rf} \pm f_{sw}$ are then generated and the information contained in the $f_{sw}$ signal is sent to the baseband processor [Val06].
3. TX and RX not working at the same frequency. In the case of a Frequency Division Duplexing (FDD) transceiver, the LNA is not able to correctly amplify the signal sent from the PA.

   A mixer should be introduced to translate the PA signal to the operating frequency of the LNA. This increases the complexity and the cost of the loopback test.
4. Reduced observability of the signal path. Since the transceiver is tested as a whole, the malfunctioning of one block can be masked by the following or previous blocks.

Looking for example at the Friis formula:

$$NF_{Rx} = NF_{LNA} + \frac{NF_{MIXER} - 1}{G_{LNA}} + \frac{NF_{other} - 1}{G_{LNA} + G_{MIXER}} \quad (2)$$

it is possible to understand that the noise of elements of the chain following the mixer is masked by the noise of LNA and mixer.

The distortion of the TX can be masked by an excellent filter in the RX chain.

The weak gain of the LNA can be masked by the high gain of the mixer.

Better diagnosis capabilities can be achieved if detectors are connected at the input and output of critical blocks, giving specific information on the functionality and performance of that block [Neg06].

#### *I.2.1.2 Alternate Test*

One of the most popular methods for implementing a functional test is the Alternate Test.

The goal of this test is to indirectly measure the specifications of the CUT starting from the response of the CUT to external low-frequency stimuli. The response of the CUT to those stimuli is easier to measure compared to the direct measure of its gain, non-linearity, noise or frequency response.

The typical procedure that needs to be followed to carry out an Alternate Test is shown in Figure I-5.

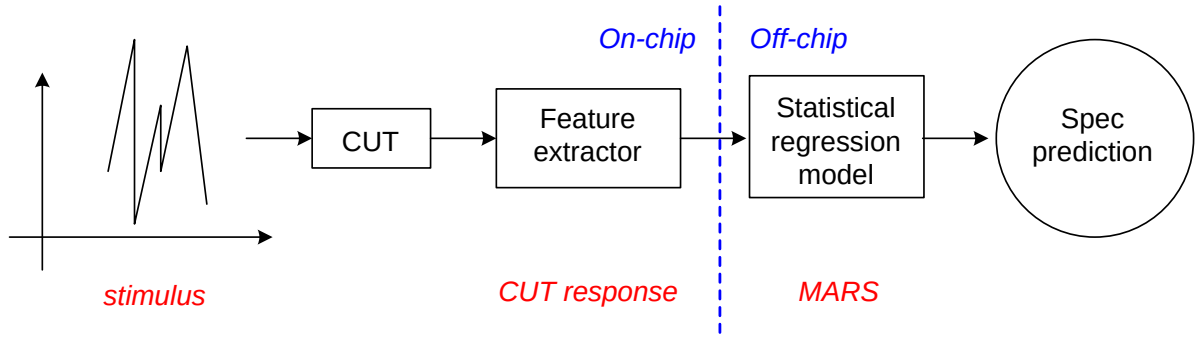


**Figure I-5: Characteristic flow for an Alternate Test.**

Here is the principle of this method: let's define *P* the circuit parameter space, *S* the circuit specification space, *M* the response measurement space. The variation of any process variable in *P* affects both *S* and *M*. Two different non-linear mappings define these relationships:

$f_{ps} : P \rightarrow S$

$f_{pm} : P \rightarrow M$

Nonlinear statistical multivariate regression analysis allows the construction of the function:

$f_{ms} : M \rightarrow S$

For a given set of measurements, the mapping can generate predictions of the specifications.

A test generation algorithm finds the low-frequency stimulus that grants the highest correlation between the specification and the measurements [Akb05].

The stimulus in then injected into the CUT; its response is measured on-chip and sent to the Multivariate Adaptive Regression Splines (MARS) algorithm. This algorithm, using the specifications from a training set of 100 instances of the CUT and the measurements obtained from the CUT, is able to generate the set of nonlinear mappings relating the measured response to the specifications.

The placement of the sensors used for the on-chip measurement is also very important. There is an optimal placement for the sensors to obtain the best prediction of the specifications starting from the sensor measurements. Thanks to the good placement of the sensor, the specifications of the CUT can be found with a high degree of accuracy [Bat04].

The alternate technique can be used in conjunction with the loopback test to measure the specifications of a complete transceiver. A single bit stream from the baseband can be used as stimulus and the response is captured at the RX-base band. The MARS algorithm can either find the specifications of the transceiver or of its single building blocks [Sri06].

While attractive for its results, the alternate test has two major problems: it requires a high computational effort, making a complete on-chip solution impossible; many instances of the CUT are needed to train the algorithm, slowing the time of the test and forcing the industry to use classical test methods in a first time.

#### *I.2.1.3 Hardware-based methodologies to perform a functional test*

Other methodologies focus on the use of embedded sensors to measure on-chip the figure of merit of single RF building blocks. The goal of these strategies is to output the final measure carrying out the analysis completely on-chip and without the need for external software.

(1) Using peak detectors

The input impedance, gain and noise figure of the CUT can be found implementing the scheme represented in Figure I-6.

Peak detectors (PD) are connected at the output of the CUT and of a test amplifier (TA). Switch 1 allows connecting or disconnecting the TA; switch 2 and switch 3 are used to connect the output of the CUT either to the 50Ω-RF output or to the peak detector.

Equations correlate the value of the output voltage of the peak detectors to the values of input matching, gain and noise figure of the CUT [Ryu06].

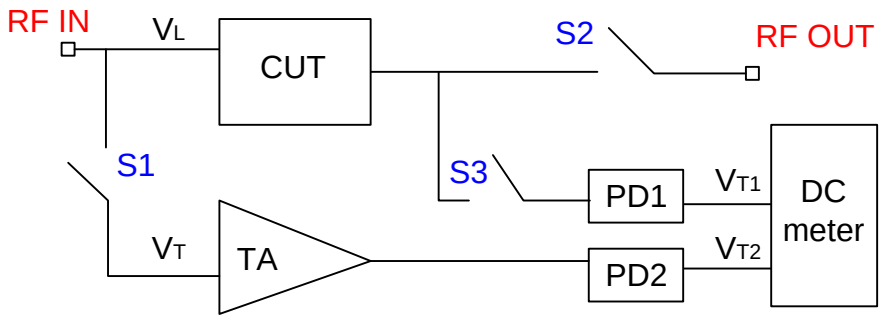


**Figure I-6: Block scheme allowing the measure of gain, input impedance and noise figure of the CUT.**

Let's define $V_{T2}$ the transient output of peak detector 2, $V_{T1}$ the transient output of the peak detector 1, $V_{02}$ the DC-output voltage of peak detector 2 and $V_{01}$ the DC output voltage of peak detector 1, $G_2$ the voltage gain of the test amplifier, $V_{in}$ the input voltage and $R_S$ the value of the source impedance.

The input impedance test is performed as follows: keeping S1 and S2 in the close position, the voltage gain $G_{02}$ is measured as:

$$G_{02} = \frac{V_{T2} - V_{02}}{V_{in}} \tag{3}$$

Defining $K_1 = G_{02}/G_2$, the following expression for the magnitude of the input impedance of the CUT is obtained:

$$|Z_{in}| = R_S \cdot \frac{K_1}{1 - 2K_1} \tag{4}$$

The gain test is carried out closing S3 and opening S1 and S2; the voltage gain $G_{01}$ is measured as:

$$G_{01} = \frac{V_{T1} - V_{01}}{V_{in}} \tag{5}$$

The voltage gain of the LNA can now be expressed as:

$$G_1 = \frac{R_S + |Z_{in}|}{|Z_{in}|} \cdot G_{01} \tag{6}$$

The noise figure can now be calculated, starting from the measurements carried out in the preceding steps. Defined the power gain as $G_0$ and the noise figure required by specifications as $NF_0$, we can write:

$$NF = 1 + \left(\frac{|Z_{in}|}{R_S + |Z_{in}|}\right)^2 \cdot \frac{G_0}{G_{01}^2} \cdot (NF_0 - 1) \tag{7}$$

The error of this embedded test compared to the measurements performed with external equipment is very low.

(2) Using mixing techniques

The frequency response of the CUT can be characterized on-chip using the system shown in Figure I-7. A mixer is connected at the input and output of the CUT; two switches allow deciding which signals are sent to the mixer.

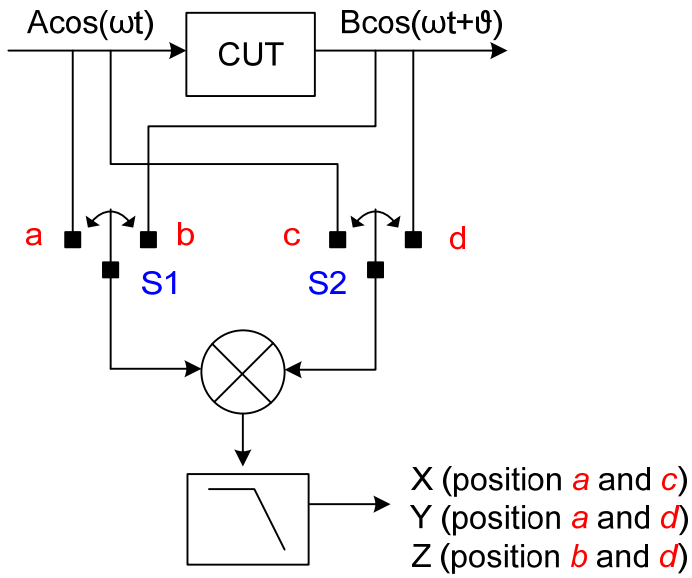


**Figure I-7: On-chip frequency response characterization system.**

Three signal multiplications are then performed, depending on the position of the two switches; a low-pass filter allows only the DC component to be sent out of the system.

The following outputs are obtained:

$$X = K \cdot \frac{A^2}{2}$$
$$Y = \frac{1}{2} \cdot K \cdot A \cdot B \cdot \cos\vartheta \quad (8)$$
$$Z = K \cdot \frac{B^2}{2}$$

where *A*, *B*, *K* are the amplitude of the input and output signal and the gain of the mixer, respectively.

An external ATE can then evaluate the phase and magnitude response of the CUT as follows:

$$|\vartheta| = \cos^{-1}\left(\frac{Y}{\sqrt{X \cdot Z}}\right)$$
$$\frac{B}{A} = \sqrt{\frac{Z}{X}} \quad (9)$$

The achieved resolution is of 1 degree for the phase measurements and of 1 dB for the magnitude measurements [Val06b]. The condition to use this strategy at RF is to have switches that do not degrade the signals and an accurate RF mixer.

(3) Using amplitude detectors

If the information on the phase is not needed, simple amplitude detectors can be connected at the input and output of the CUT, as shown in the left side of Figure I-8. The ratio of their DC output gives the gain of the CUT; if the input power is swept, the 1dB-compression point of the CUT can also be found.

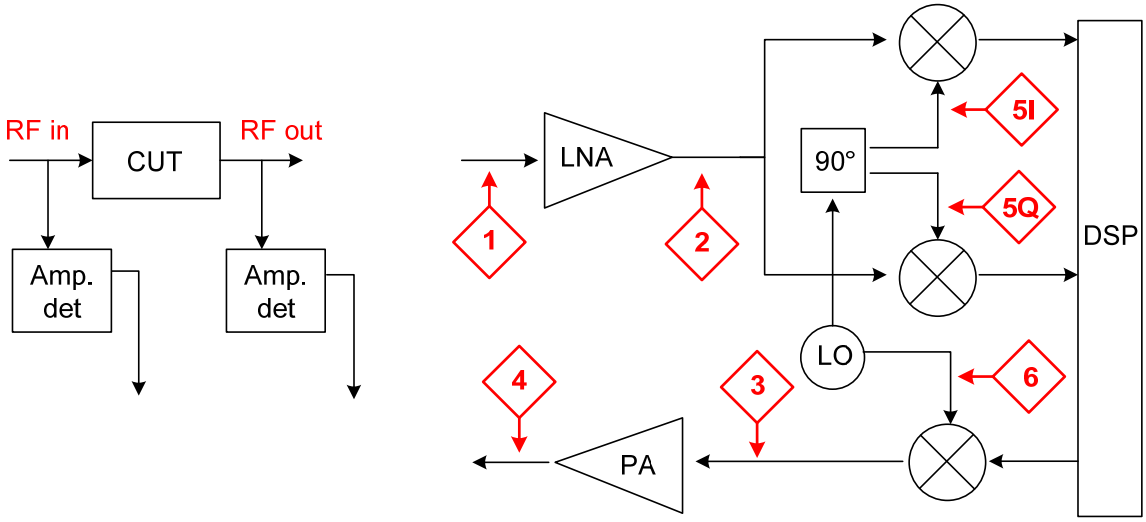


**Figure I-8: In the left portion amplitude detectors are used to characterize the single CUT; in the right portion the test strategy is applied to the whole transceiver.**

Connecting RMS amplitude detectors in strategically interesting points of the transceiver, as shown in the right side of Figure I-8, the following on-chip measurements can be realized [Val05]:

| Test Point | Measurement |
|---|---|
| 1 & 2 | LNA gain and 1dB-compression point |
| 3 & 4 | PA gain and 1dB-compression point |
| 3 | Up-converter output amplitude |
| 5I, 5Q, 6 | Local oscillator output power |

### *I.2.2 Conclusion on Functional Test*

Functional test can be very powerful because it allows measuring the performance of the CUT without any expensive equipment and without access problems. The risk of degradation of the RF signal is reduced to a minimum.

A great amount of external software post-processing is needed, though. Complete on-chip integration seems impossible.

Moreover, the extra circuitry needed (switches, mixers…) can very fast become too complicated. The risk is to spend more time in the debugging of the BIST than in the measure of the CUT.

In the case of a wafer sort, this is not acceptable.

### *I.2.3 Structural Test (defect-oriented)*

The structural test simplifies the wafer sort because the pass/fail decision is done without the need to measure the specifications of the CUT, as shown in Figure I-9.

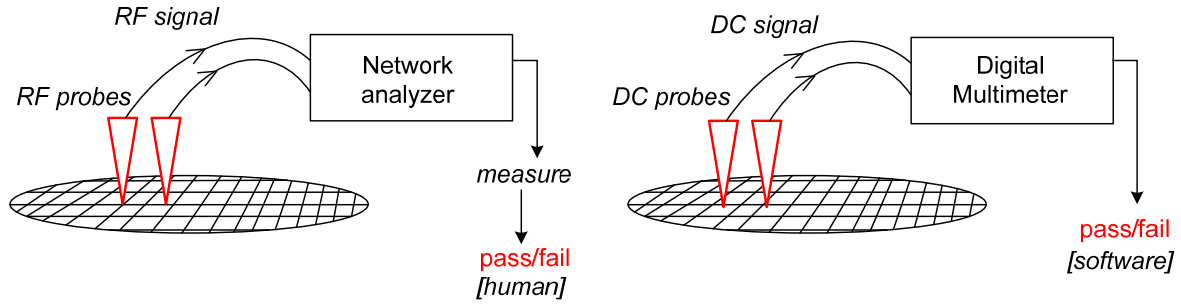


**Figure I-9: The structural test (right side) outputs the pass/fail decision without the need to measure the specifications of the CUT.**

The assumption is made that any defect in the circuit causes deviation of some electrical quantity (current, voltage, power etc.) of the CUT.

If the deviation is so important that the electrical quantity falls outside the boundaries fixed by the specifications, the CUT is considered faulty and discarded by the wafer sort. The conceptual flow of the structural test is presented in Figure I-10.

The sensor is integrated into the chip.

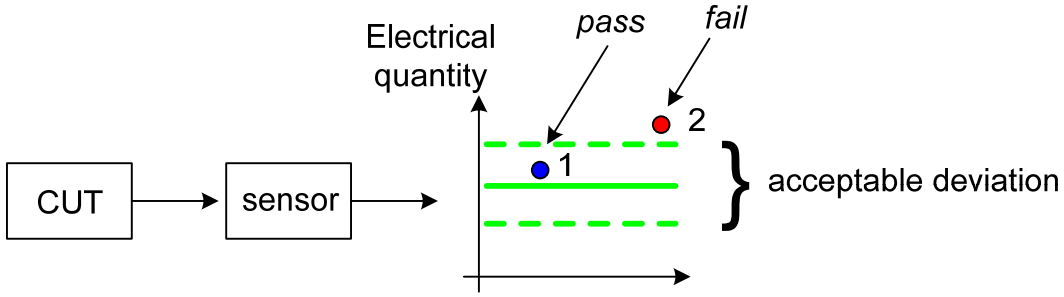


**Figure I-10: Conceptual flow of the structural test; point 2 is outside the boundaries, meaning that the CUT presents a defect.**

#### *I.2.3.1 Quiescent current sensing*

In the RF domain, the most common technique consists in selecting multiple power supply nodes and observing the corresponding quiescent current signature *Idd*. This technique, depicted in Figure I-11, is inherited from the digital domain.

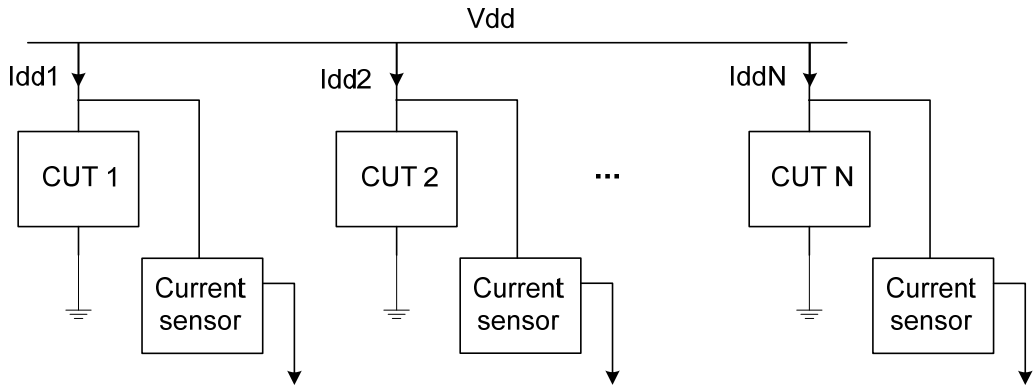


**Figure I-11: Structural test carried out measuring on-chip the supply current of the CUT**

Some faults may not cause an important deviation of the supply current. The risk is then to consider the circuit as "good" even if a defect is present inside its structure.
Techniques exist to alleviate this problem, trying to collect as much information as possible from the supply current, improving the chance of finding the faults.

#### *I.2.3.2 Sweep of the supply voltage*

A very effective one is to sweep the supply voltage *Vdd* and sense the supply current *Idd* for different values of *Vdd*.
Faults are more or less easily detectable depending on the operating region of the transistor.
Thanks to the sweep of the supply voltage, the MOS transistors will work at first in the sub-threshold region, then in the linear region and at the end in the saturation region, as shown in Figure I-12.

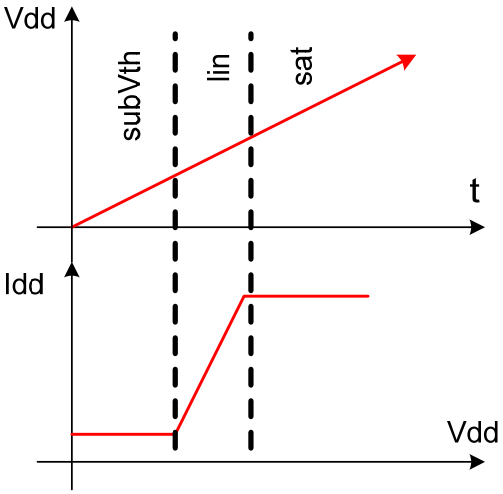


**Figure I-12: The supply voltage is swept in order for the transistors to enter each region of operation**

In Figure I-13, the supply voltage of a TX is swept from 0 Volts to 3.3V using uniformly incremented steps of 100mV of 5ms each. The best distinction from faulty and non-faulty TX is achieved observing the current signature when the supply voltage is swept from 2.1V to 2.3V [Sil05].

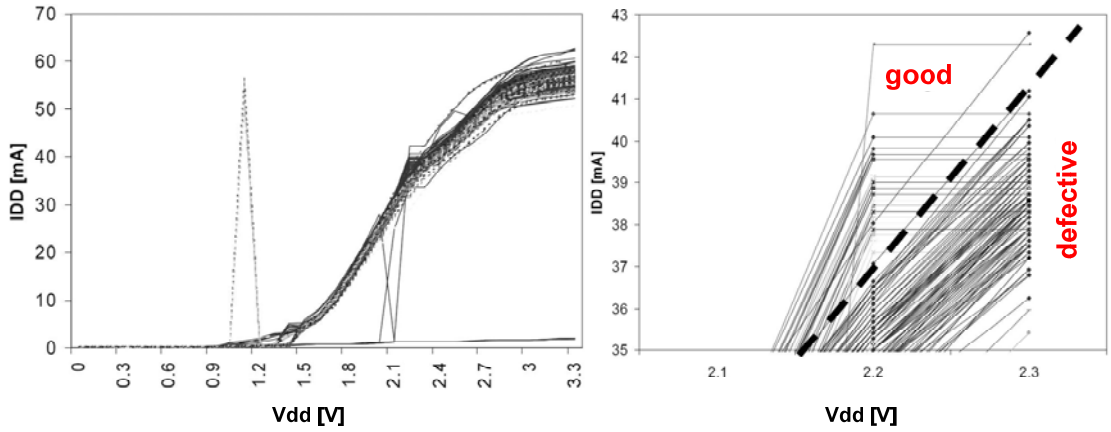


**Figure I-13: Current signature of TX for VDD ramp test in [Sil05]; the right side of the figure presents a zoom of the current signature when VDD is swept from 2.1V to 2.3V**

Even if this methodology is appealing, the continuous decrease of the supply voltage (1.2V for the CMOS 65nm technology) and of the allowed current consumption could cause this strategy to lose part of its interest. Moreover, the need to monitor the current at multiple VDD levels could complicate the on-chip current detector.

### *I.2.3.3 Transient current sensing*

In order to extract the highest amount of information from *Idd*, but without the need for a sweep of the supply voltage, the fluctuations of the supply current can be observed.

This grants to detect faults that would not have been detected by a simple monitoring of the DC current, because some faults do not affect the DC current but only its transient behavior.

This technique, called ΔIddq, consists in measuring on-chip the difference in supply current between maximum and minimum readings within a test period [Gop05].

The difference between the DC value of the supply current *Idd* and its variations is shown in Figure I-14.

The sensitivity of the sensor, if used for monitoring the ΔIddq of a RF circuit, has to be in the order of a few hundreds of nA.

Depending on the rate of change of the sensed value, the bandwidth of the sensor has to be more or less large.

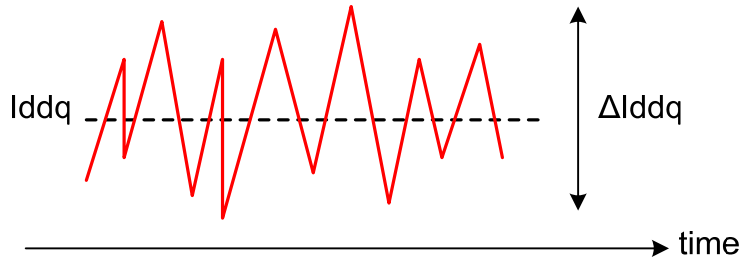


**Figure I-14: ΔIddq technique to enhance the information obtained from the current sensing.**

### *I.2.4 Conclusion on Structural Test*

The structural test is easier to carry out, compared to the functional test. The information extracted cannot be used for characterization of the CUT performance, but this is not the goal of the wafer test. If the right quantity is monitored, the structural test is very powerful in detecting and discarding a faulty circuit, without any post-processing. A complete on-chip solution is possible.

## *I.3. Detectors*

In both a functional and a structural test, detectors are connected to the circuit, in order to monitor some quantity on-chip. Depending on the BIST solution, a variety of detectors are needed.

The most employed are current detectors, voltage detectors, power detectors and frequency-meters.

The main specifications that any detector for BIST applications has to respect are:

- Low consumption (compared to the consumption of the CUT)
- Low surface (compared to the surface of the CUT)
- Simplicity
- Easy-to-use output information (DC output, binary output)

The first two requirements are dictated mostly by cost constraints; aiming at low cost ICs, the sensor should not impact on the cost of the complete system.

The third requirement guarantees that the probability of a faulty detector is much lower than the probability of a faulty CUT.

The last requirement allows having a completely integrated test solution, without the need of any software or DSP capability to get the final go/no go information for the wafer sort.

An overview of the most popular built-in detectors used for BIST applications is now proposed.

### *I.3.1 Built-In Current Sensors (BICS)*

The goal of any Built-In Current Sensor (BICS) is to sense the current flowing through the CUT.

#### *I.3.1.1 IDDQ*

If the detector does not have to discriminate between small variations of the DC current, there is no need for amplification of the monitored current. This methodology of test is called IDDQ (quiescent supply current).

One way to easily realize this detection is to use a current mirror, as shown in Figure I-15.

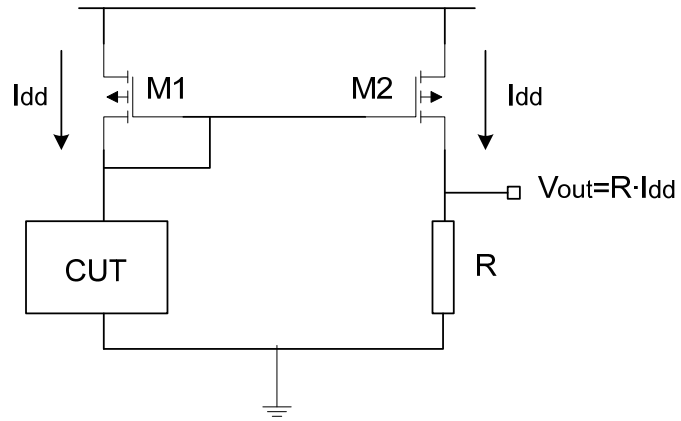


**Figure I-15: BICS based on current mirrors.**

Transistor M2 copies the supply current of the CUT; a resistor *R* is used to convert the current into voltage, allowing the sensor to output a voltage proportional to the sensed current (*U=RI*).

To lower the consumption of the BICS, M2 is *K* times smaller than M1, to divide by *K* the current flowing through the output branch of the sensor.

The main problem of this topology of sensors is the high voltage drop $V_{ds}$ across M1, which needs to work in the saturation region to guarantee the good functioning of the current mirror. The supply voltage for the CUT is then reduced; this causes the degradation of performance of the CUT.

Moreover, the simple current mirror presented in Figure I-15 suffers from bad current copy because of the different drain-source voltage of M1 and M2.

A way to solve those problems is to use the supply current of the CUT to unbalance a current mirror that can reach the equilibrium again only generating an output current equal to the supply current of the CUT. The CUT does not interfere in the structure of the current mirror, which can now be designed in a more efficient way than that of Figure I-15. Moreover, the decrease of the supply voltage for the CUT is eliminated [Cim06].

#### *I.3.1.2 ΔIDDQ*

If small variations of the DC current are to be sensed, amplification is needed; this sensing strategy is called ΔIDDQ.

In the presence of external factors (such as process parameters or temperature) the level of the quiescent current may vary. In this case, all IDDQ tests show the same increase, while ΔIDDQ measurements remain approximately the same. This is the main advantage of ΔIDDQ tests compared to IDDQ techniques.

The implementation of the sensor is straightforward.

A sensing element (usually a resistor or an inductor) is connected in series with the CUT. Its function is to convert the current information into a voltage.

The voltage is then amplified (in order to allow discrimination between currents having almost the same value) and sampled by an external sampler.

If a high rate of change of the current has to be observable, the system of amplification must guarantee a high bandwidth.

A processing unit is then able to collect the data and compare them to the expected value [Sol04].

In Figure I-16 the principle of operation of the ΔIDDQ sensing is shown.

While the concept is always the same, ΔIDDQ sensors differ mainly in the way the amplification is performed. The higher the bandwidth of the amplifier, the more performing the sensor will be.

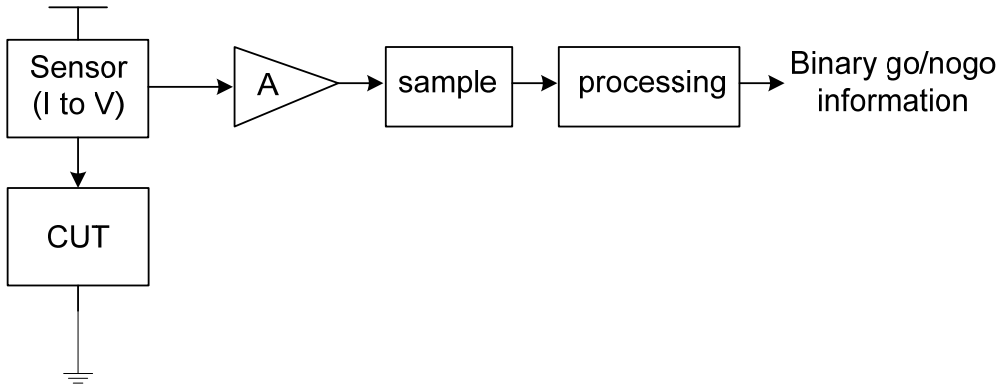


**Figure I-16: Principle of operation of the ΔIDDQ test.**

#### *I.3.1.3 Conclusion on current sensors*

IDDQ sensing is attractive for its simplicity. However, the DC current does not always grant the highest fault coverage for RF circuits. ΔIDDQ, even if potentially able to detect faults not detectable with a simple IDDQ test, needs a sampling unit and post-processing of the data, complicating the wafer test and making the complete on-chip integration very difficult.

Moreover, in both techniques, a sensing element needs to be connected between the CUT and the supply voltage. This series sensing element cannot be disconnected from the CUT; a degradation of performance is unavoidable.

### *I.3.2 Power sensors*

The power consumed by a resistor is defined as the product of the voltage across the resistor and the current flowing through it.

$$P = V \cdot I = \frac{V^2}{R} \tag{10}$$

Power is then directly proportional to the square of the voltage.

The goal of any power sensor is then to create an output which is proportional to the square of the input voltage.

The easiest way to implement a power sensor is then to use diode detectors with a square-law behavior; this method grants high working frequency and low costs, but suffers from a high temperature dependence and limited dynamic range. Moreover, Schottky diodes are often not available in many processes.

To overcome the limits of diode-based power detectors, it is necessary to create a circuit whose output is dependent on the square of the input signal.

Three possibilities arise:

- The use of bipolar transistors
- The use of MOSFET biased in the sub-threshold region
- The translinear loop

#### *I.3.2.1 Exponential current behavior*

The simplified behavior of the collector current in a bipolar transistor is the following:

$$I_C = I_S \cdot e^{V_{be}/V_T} \tag{11}$$

where $I_s$ is the saturation current, $V_{be}$ is the base-emitter voltage and $V_T$ is the thermal voltage.

The drain current in a MOSFET biased in the sub-threshold region is:

$$I_D = k_x \cdot \frac{W}{L} \cdot e^{(V_{gs}-V_{th})/nV_T} \tag{12}$$

where $K_x$ is a process parameter, $n$ is the fitting factor for MOSFET sub-threshold swing, $V_{th}$ is the threshold voltage, $W$ and $L$ are the width and length of the transistor, and $V_{gs}$ is the gate-source voltage.

Both equations show an exponential behavior of the current versus the biasing voltage.

If a sinusoidal input $A\cos\omega t$ is applied to the transistor, the equation can be approximated with a power series:

$$e^{\frac{A\cos\omega t+V_b}{V_T}} \approx e^{\frac{V_b}{V_T}}\left(1 + A\cos\omega_0 t + \frac{A^2 cos^2\omega_0 t}{2}\right) = e^{\frac{V_b}{V_T}}\left(1 + \frac{A^2}{2} + A\cos\omega_0 t - \frac{A^2 cos2\omega_0 t}{2}\right) \quad (13)$$

where $V_b$ represents the base-emitter voltage of a bipolar transistor or the gate-source voltage of a MOSFET.

The current contains a DC-term proportional to the square of the amplitude of the input sinusoid.

The current is converted to a voltage. It is then sufficient to filter out the higher order harmonics using a filter having a cutoff frequency lower than the frequency of the input signal.

The block scheme is presented in Figure I-17.

The final output is proportional to the square of the input signal [Hsi06].

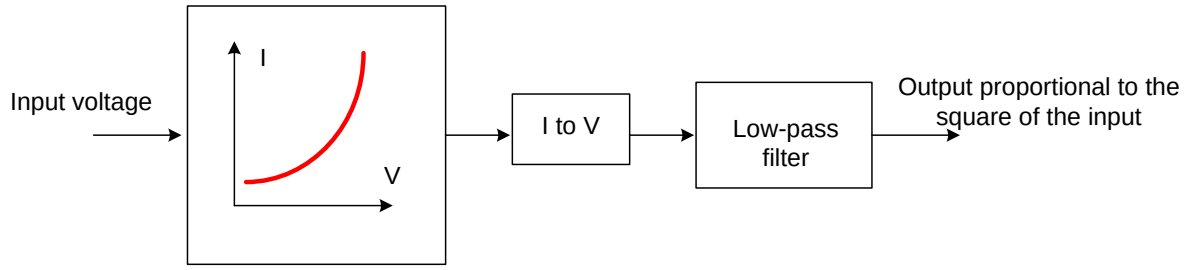


**Figure I-17: Concept of power detector implemented using transistors.**

#### *I.3.2.2 Translinear principle*

The translinear loop principle is another strategy useful when a transistor-based power sensor is needed.

Taking advantage of the exponential relation between current and voltage of bipolar and MOSFET transistors, we have:

$$g_m = \frac{\partial i}{\partial v} = A \cdot i \quad (14)$$

where A is a constant. The *trans*conductance is then *linear* with the current.

Looking at Figure I-18, the following simplified relations hold:

$$I_{out} = e^{V_{be}/V_T}$$
$$I_{in} - I_b = C \cdot \frac{dV_{be}}{dt} = C \cdot V_T \frac{1}{I_{out}} \cdot \frac{dI_{out}}{dt} \quad (15)$$

Solving the system we find:

$$I_{out} = \frac{I_{in}^2/I_b}{1 + sC\,V_T/I_b} \rightarrow low\ pass \rightarrow \langle \frac{I_{in}^2}{I_b} \rangle \quad (16)$$

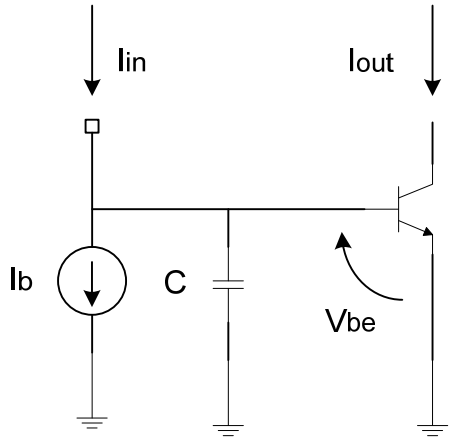


**Figure I-18: Circuit used to implement the translinear principle; $V_{be}$ is the input to our system.**

The output current is the mean square of the input current.

To use the translinear principle for power detection, it is then needed to convert the input voltage into a current, to send the generated current through the translinear circuit and convert back the current into a voltage [Yin05].

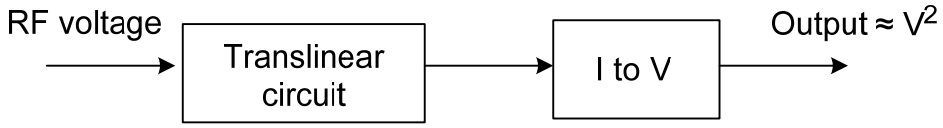


**Figure I-19: Use of the translinear principle to design a power detector.**

#### *I.3.2.3 Conclusion on power detectors*

The use of the exponential relationship between current and voltage is attractive for power detection, but a low-pass filter is needed. If the frequency of the input signal is not sufficiently high, the filter could take-up a non negligible Si surface.

The translinear principle solves this problem, but at the cost of increased complexity.

Moreover, it needs to be kept in mind that the output power of any CUT is dependent on the load connected to the CUT. The information on the square of the input amplitude is not exactly a measure of the power of the signal, but only an image of it.

### *I.3.3 Amplitude sensors*

Amplitude detection can be performed in many different ways.

If a detector has to work reliably and with good precision for any RF signal sent at its input, a common point for each signal has to be found.

The two main possibilities are to work with signals having either the same DC value (left side of Figure I-20) or the same negative peak value (right side of Figure I-20).

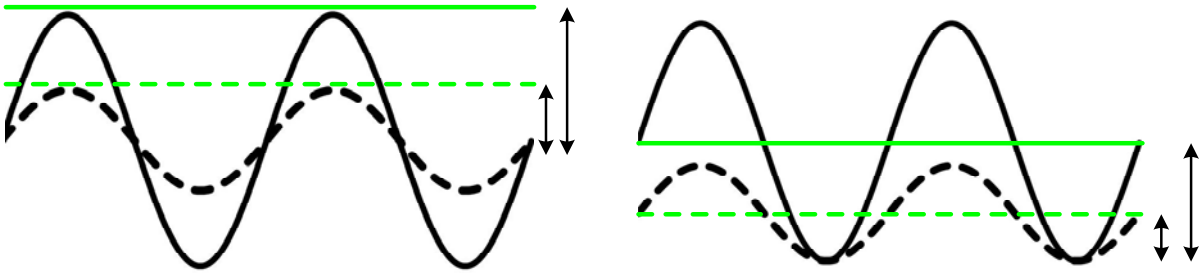

**Figure I-20: In the left side, the signals have the same DC value. In the right side, they have the same negative peak value.**

In the first case, the amplitude detector has to measure the peak value of the input signal, while in the second case the DC value of the input signal carries the information on the amplitude.

It is easier to grant the same DC-value than the same negative-peak value; a decoupling capacitor followed by a resistive divider can accomplish the task.

On the contrary, if high accuracy is needed, the peak value of the signal is harder to measure than the DC value of the sinusoid.

The principle of operation of a common peak detector is explained in Figure I-21: the RF voltage signal is converted into a current (optional), which is amplified, rectified and filtered before being converted to a voltage again [Val05]. The value of the output voltage is the value of the positive peak of the input RF signal.

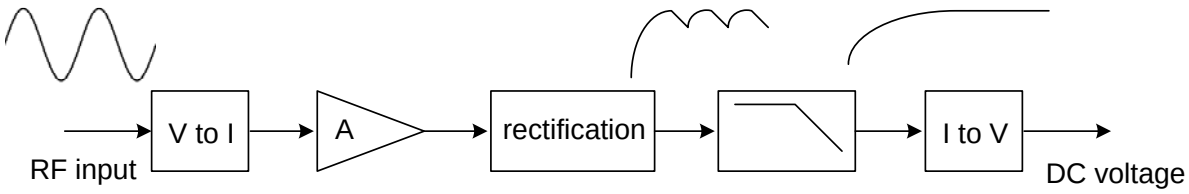


**Figure I-21: Principle of operation of an amplitude detector.**

### *I.3.4 Frequency-meters*

Those sensors are dedicated to measuring the frequency of oscillation of the monitored signal. Two main categories of frequency-meters exist: analog frequency-to-voltage converters (FVC) and digital time-to-digital converters (TDC). Both possibilities are now presented.

#### *I.3.4.1 Frequency-to-voltage converter (FVC)*

The goal of this detector is to create a voltage proportional to the period of the input signal. The schematic of a frequency-to-voltage converter (FVC) and its principle of operation are explained in Figure I-22.

The input signal is a periodic current; this current charges the capacitor *C* following the relation:

$$V_{out} = \frac{1}{C}\int_0^{T_d} i_{in}dt = \frac{1}{C}\cdot i_{in}\cdot\frac{T_d}{2} \qquad (17)$$

The switch *S1* discharges the capacitor to begin a new cycle.

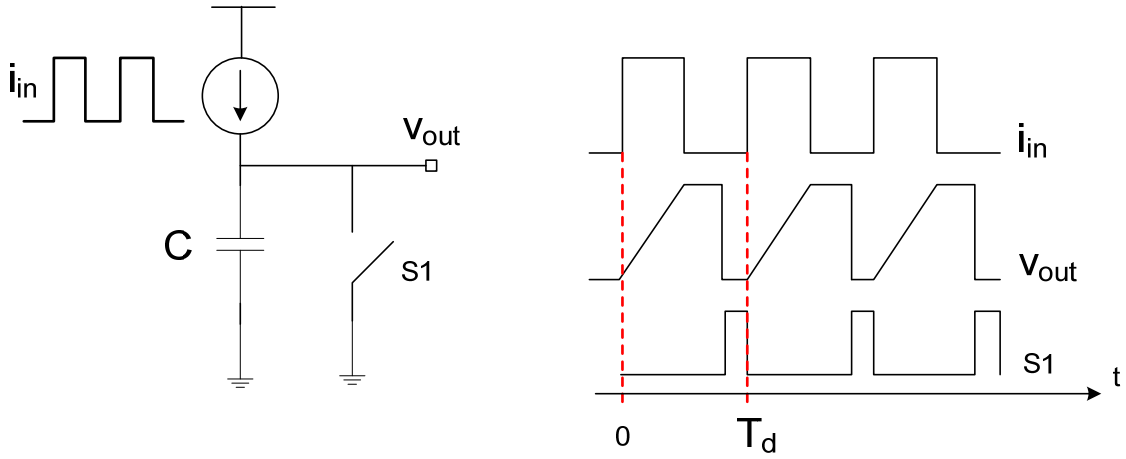


**Figure I-22: Principle of operation of the FVC.**

Two current signals with different frequency are presented in Figure I-23. For hypothesis, the integration takes place during 1/2 period of the signals and the capacitor is discharged just before the beginning of the following period. It is evident that the longer the duration of the period of the signal, the higher the charge stored in the capacitor will be, as demonstrated in equation 17.

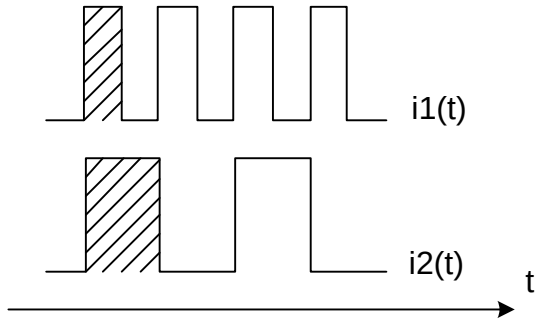


**Figure I-23: The longer the period of the input signal, the higher the charge stored in the capacitor.**

Frequency-to-voltage converters based on the charge and discharge of a capacitor to obtain the integration of the current are useful for low frequency applications.

Even if the detection of variations of the period of RF signals is possible, the output is not an exact measure of the frequency. The short time $T_d$ for the charge of the capacitor, and the finite rise and fall time of the charging current make the exact integration of the signal impossible.

As explained in Figure I-24, the integration of the signal will suffer from an error that causes loss of information. This is the main reason why, for high speed signals, the FVC output variation for a variation of the frequency of the input signal is very small [Bui05].

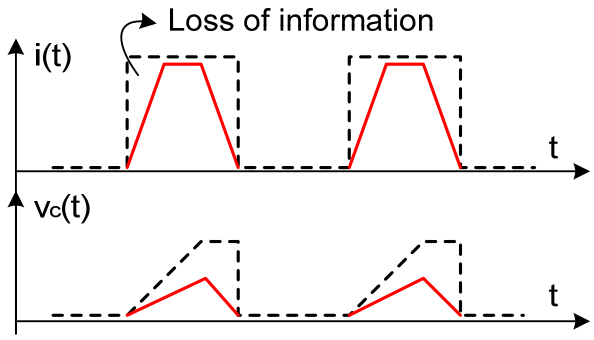


**Figure I-24: Ideal (dashed) and real behavior of current charging a capacitor and the voltage stored on the capacitor**

### *I.3.4.2 Time-to-digital converter (TDC)*

The problem of loss of information for high speed signals can be solved using time-to-digital (TDC) circuits.

The principle of operation of the TDC is represented in Figure I-25. During a clock period, the RF signal goes through an integer number *N* of periods. The last period of the RF signal does not completely fall inside the clock period. This is called the fractional part of the measurement.

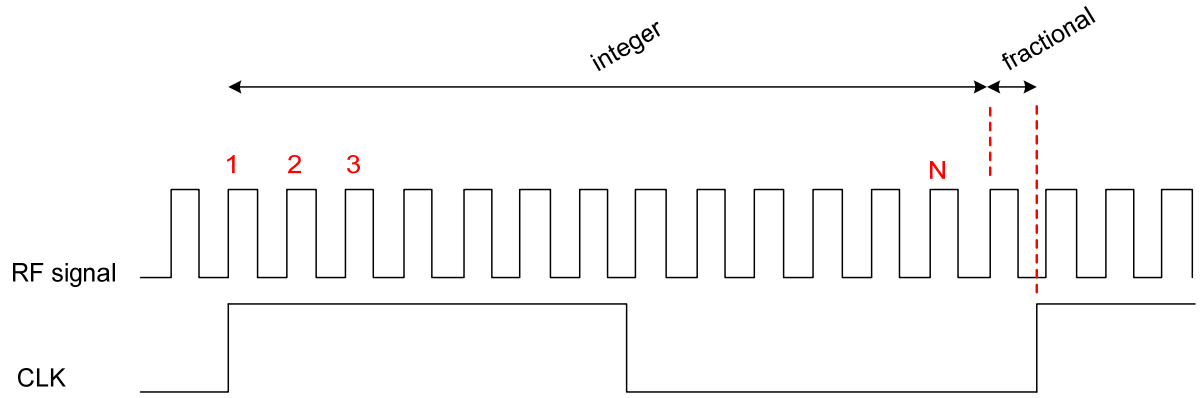


**Figure I-25: The measurement is composed of an integer portion (coarse) and a fractional part (fine).**

While the integer part of the measurement (*N*) can be found using a simple counter, the fractional part is less trivial to measure.

The strategy used to get the fractional part of the measure is explained in Figure I-26.

The RF signal passes through a chain of delay elements, whose delay Δ is known. As soon as the rising edge of the clock arrives, the RF signal and its delayed versions are sampled. A thermometer code (as for ADCs) is generated. The first '1' to '0' transition in the code quantifies the fractional part of the measurement in terms of number of delays Δ. If the transition occurs after *F* delays, the fractional measurement will be *F·Δ*.

The following relation holds:

$$T_{clk} = N \cdot T_{RF} + F \cdot \Delta \qquad (18)$$

where $T_{clk}$ and $T_{RF}$ are the periods of the clock and of the RF signal, respectively.

The only unknown in equation 18 is the period of the RF signal, which can rapidly be found.

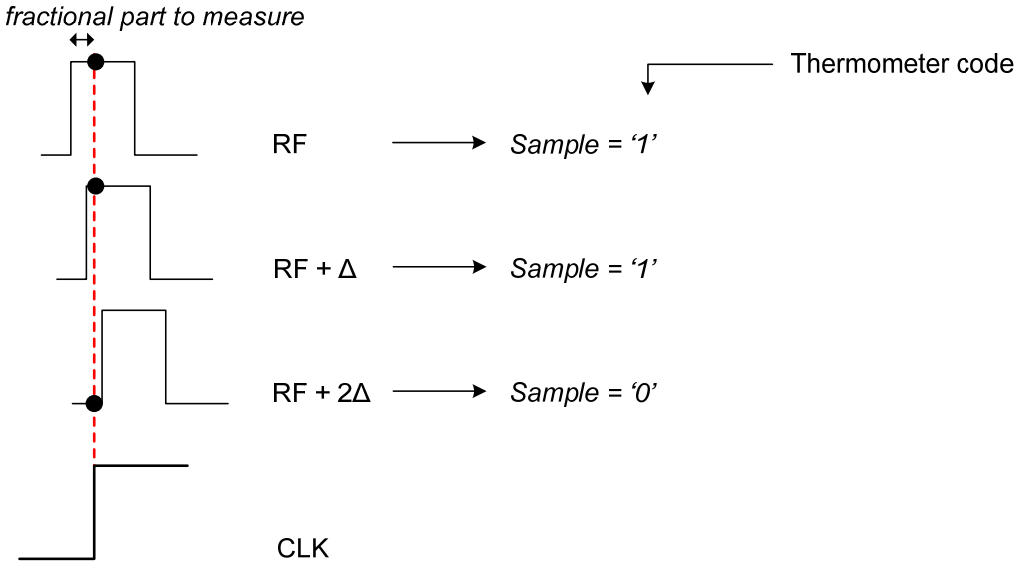


**Figure I-26: Principle of operation for the measurement of the fractional part.**

The main advantage of the TDC technique compared to the FVC is its all-digital nature. No capacitor has to be charged or discharged, so no upper boundary for the input frequency has to be fixed.
Moreover, the TDC is insensitive to the duty cycle of the input signal; this is not the case for the FVC, as inferred from Figure I-23.
The smaller the delay time, the higher the accuracy of the fractional measurement is. This means that fast rise and fall times are needed. The development of new technologies (45nm, 32nm) accounts for this need, allowing the TDC to reach a higher accuracy.

### *I.3.5 Comparative table for detectors*

In order to give an idea of the consumption, dynamic range and surface of on-chip detectors, a comparative table is here presented.

| Work | Type | Techno | Consumption | Area | Bandwidth | Dynamic Range |
|---|---|---|---|---|---|---|
| [Dra01] | ΔIDDQ | *IBM*0.25µm | 7.5mW | ////// | 3.9GHz | 11.5mA |
| [Cim06] | IDDQ | *STM*HCMOS9GP | /////// | 0.007mm$^2$ | /////// | 8mA |
| [Hsi06] | Power | CMOS0.18µm | 3.5mW | 0.06mm$^2$ | 5.2GHz | 25dBm |
| [Zha06] | Power | *IBM*7WLBiCMOS | 80µA | *0.39mm$^2$ | 20GHz | 20dB |
| [Yin05] | Power | *IBM*6HPBiCMOS | 340µW | *0.9mm$^2$ | 1.3GHz | 40dB |
| [Wan06] | Ampl. | CMOS0.18µm | 10µW | 0.0016mm$^2$ | 20GHz | 60dB |

* The area takes into account the pads also.

The fundamental criteria of low consumption and low surface are always fulfilled.

## *I.4. Choice of the Circuit Under Test*

The development of BIST strategies for RF blocks has focused essentially on LNAs. One of the main reasons for this choice is that a great number of data exist concerning the best quantity to sense on-chip to obtain the highest fault coverage for this block [Khe05].
BIST on Digital-to-Analog and Analog-to-Digital converters is also a known field; the test of those blocks benefits from the digital section of the CUT; the BIST inherits the test procedures of the digital domain (input and output test vectors).

The lack of information on BIST techniques for RF VCOs has oriented this work on the study of this essential RF building block.

### *I.4.1 Voltage-Controlled Oscillator*

The Voltage-Controlled Oscillator (VCO) is one of the fundamental blocks of any transceiver.
In the receiver chain, its role is to create the frequency that allows recovering the low frequency information contained in the modulation of the RF signal.

In the transmitter chain, its role is to create the carrier frequency that allows the propagation of the signal in the air.

We define an ideal VCO as a circuit that generates a periodic output whose frequency is a linear function of a control voltage.

$$y(t) = A \cdot cos\left(\omega_{RF} t + K_{VCO} \int_{-\infty}^{t} V_{ctrl} dt\right) \quad (19)$$

In the above expression, $\omega_{RF}$ is the free-running frequency of the VCO and $K_{VCO}$ is defined as the gain of the VCO.

In any frequency division duplexing (FDD) transceiver, a frequency band is allocated for the RX and a different frequency band is allocated for the TX. If the channelization chosen is the frequency division multiple access (FDMA), the bandwidth is partitioned in many channels, each of which assigned to a user. This situation is depicted in Figure I-27 for the standard GSM; the spacing between adjacent channels is 200 KHz.

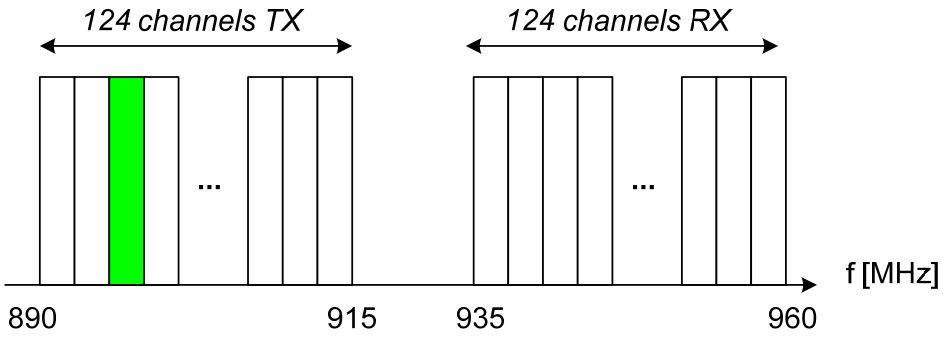


**Figure I-27: Allocation of the frequency spectrum for the standard GSM**

From this example, one of the most important constraints for frequency generation is evident: the channels have not to interfere with each others.

This means that the VCO must deliver a pure frequency signal (ideally a Dirac delta at the given frequency) and this frequency must not shift even in the presence of external perturbations (temperature, external noise etc.).

This is the reason why a VCO is rarely found stand-alone; it is usually used in a phase-locked loop (PLL).

### *I.4.2 PLL*

The structure of a PLL is shown in Figure I-28.

The RF signal of the VCO is divided by a programmable divider that generates the signal $V_{div}$.

The frequency and phase of $V_{div}$ are compared to the input signal $V_{ref}$ using a phase-frequency detector (PFD). This block outputs digital pulses whose widths are proportional to the phase error between the two input signals. If $V_{div}$ leads $V_{ref}$, then a down-signal is sent to the charge pump; if $V_{div}$ lags $V_{ref}$, then an up-signal is sent to the charge pump.

The charge pump charges or discharges a capacitor depending on its input signals, increasing or decreasing the voltage that is, after filtering, sent to the VCO.

The output voltage of the filter is the term $V_{ctrl}$ found in (19), needed to increase or decrease the frequency of oscillation on the VCO.

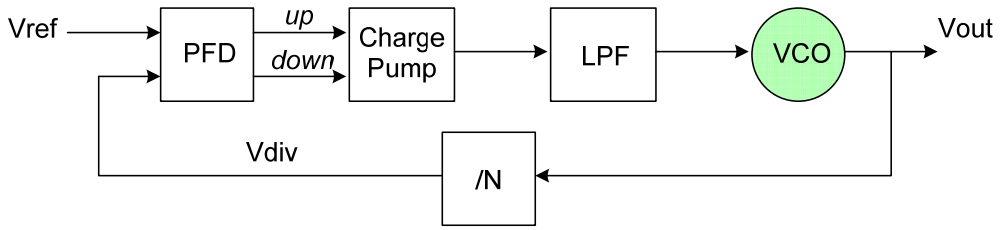


**Figure I-28: Block diagram representing the classical Phase Locked Loop.**

The basic operation of the PLL can be summarizes as:

$$if\ V_{ref} = V_{div} \Rightarrow f_{out} = Nf_{ref} \tag{20}$$

The PLL is then a feedback loop control and it entails all the benefits of every feedback system.

- In case of variation of a parameter in the transfer function of the direct path (between input and output), the relative error is much smaller in the case of a closed loop than in an open loop (in the frequency range in which the loop gain is sufficiently high).
- In case of noise injected in the direct path, the signal-to-noise ratio (SNR) of the closed-loop system is not lowered as much as the SNR of the open-loop system.

All the benefits of feedback systems are only true inside the bandwidth of the PLL.

The bandwidth cannot be greater than half of the input frequency (Shannon); in normal applications, the rule of thumb is to have:

$$BW \leq \frac{f_{ref}}{10} \tag{21}$$

This constraint allows the good suppression of the harmonics at frequencies $f_{RF} \pm f_{ref}$.

So, considering an input signal oscillating at the frequency of 200kHz (GSM standard), the bandwidth of the PLL will not exceed 2kHz.

Outside the bandwidth, the output signal of the PLL is the output of the VCO.

It is then important to design a VCO with good performances.

### *I.4.3 Phase noise*

Recalling Figure I-27, the frequency generated by the VCO should approach a Dirac delta.

Unfortunately, the smallest random excess phase creates deviations from the ideal behavior.

A normally periodic sinusoidal signal can be represented as:

$$y(t) = A \cdot cos[\omega_{RF} t + \Phi_n(t)] \quad (22)$$

where $\Phi_n(t)$ is a small random excess phase representing variations in the period of oscillation.

The function $\Phi_n(t)$ is called phase noise.

For $|\Phi_n(t)| \ll 1$, (22) can be written as:

$$y(t) = A \cdot cos\omega_{RF} t - A \cdot \Phi_n(t) sin\omega_{RF} t \quad (23)$$

showing that the spectrum of $\Phi_n(t)$ is translated to $\pm\omega_{RF}$.

The signal can then be visualized in the frequency domain as in Figure I-29; the spectrum assumes the shape of an impulse with skirts around the carrier frequency.

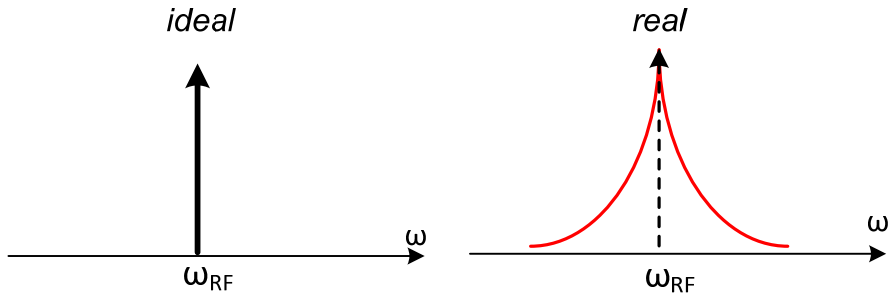


**Figure I-29: Spectra of an ideal and a real oscillator**

### *I.4.4 Condition for oscillation and possible implementations of the VCO*

In order to understand the different implementations for VCOs, it is mandatory to know the general condition assuring oscillation.

The oscillator must entail a self-sustaining mechanism that allows its own noise to grow and become a periodic signal.

To find the condition for self-sustained oscillation, the oscillator can be described using a “one-port” model or a “two-port” model, both shown in Figure I-30.

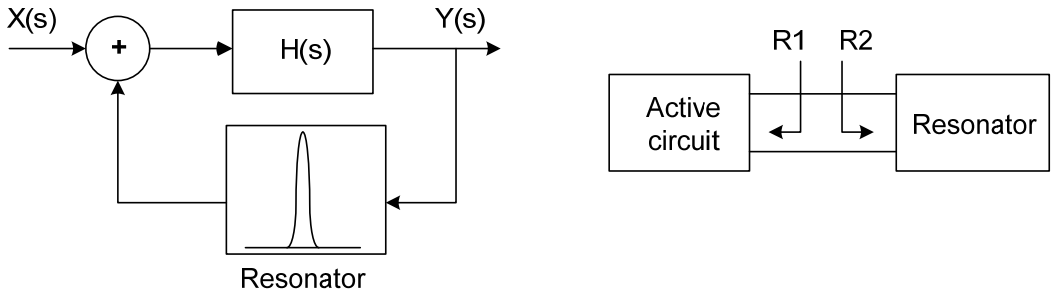


**Figure I-30: "Two-port" and "one-port" model describing the oscillator**

*I.4.4.1 Two-Port model*

Considering the "two-port" model, the following transfer function can be written:

$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1 - H(s)} \tag{24}$$

where the resonator in the feedback is not taken into account.

The Barkhausen's criteria (necessary but not sufficient) state that a self-sustained oscillation can take place at frequency $s_0$ if $H(s_0) = 1$ and its amplitude remains constant if $s_0$ is purely imaginary; so, for steady oscillation, the loop gain at $\omega_0$ must be equal to unity and the total phase shift around the loop must be equal to zero.

This model describes very well ring oscillators. If a cascade of 2N-1 inverters is placed in a feedback loop, the circuit creates an oscillation whose period is $2(2N-1)T_d$, where $T_d$ is the delay introduced by each inverter.

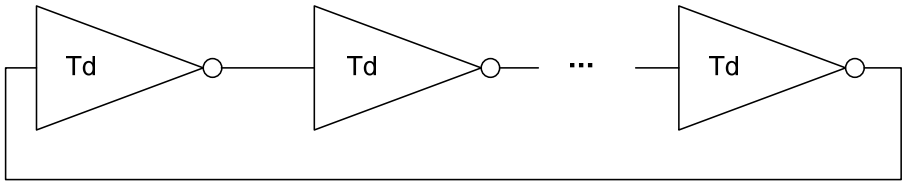


**Figure I-31: Ring oscillator composed of a chain of inverters**

Ring oscillators can be divided in two categories: non-saturated or saturated. In the first case, the MOS transistors of the inverter never switch off completely while in the second case they do.

The phase noise of non-saturated ring oscillators is higher than that of saturated ones, which also present a lower sensitivity to perturbations [Lag05].

The structure of ring oscillators is very suitable for integration, because no passive element is needed; this dramatically lowers the Si surface of the circuit.

Moreover, the frequency range of ring oscillators is very high; the delay time $T_d$ can be changed acting on the current flowing through the inverter.

Unfortunately its phase noise is much higher than that of other structures, which are examined next.

*I.4.4.2 One-Port model*

Let's now consider the "one-port" model. If the resonator is a simple LC tank, it can't oscillate indefinitely because of the energy dissipated through its parasitic resistance $R_P$. The idea is to create a negative resistance $-R_P$ to compensate for the losses of the resonator.

This model describes very well negative-$g_m$ oscillators.

In this type of oscillators, the negative resistance is created through the cross-coupling of active components, as shown in Figure I-32.

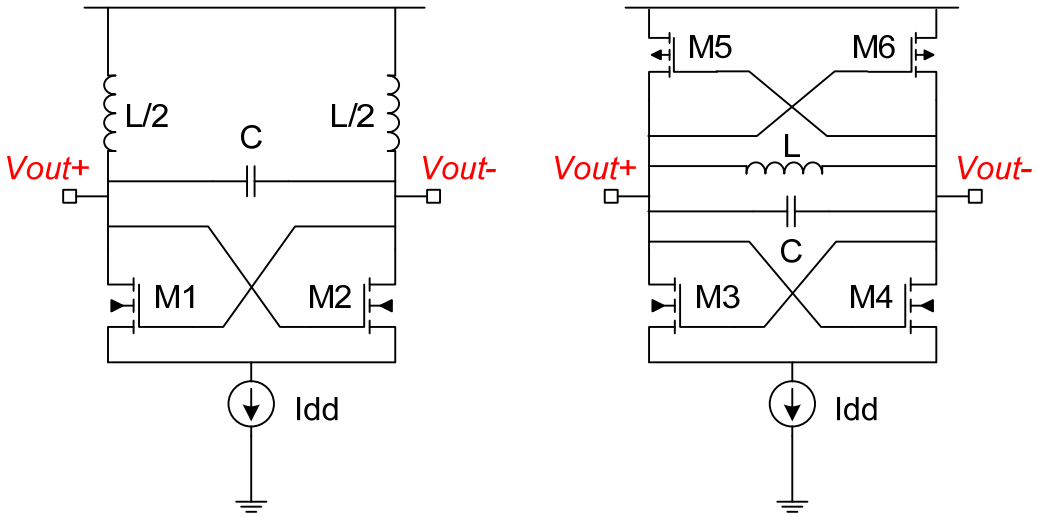


**Figure I-32: Negative-$g_m$ oscillators; cross-coupled nMOS VCO on the left side and cross-coupled complementary VCO on the right side.**

The complementary structure has a lower phase noise compared to the nMOS-only structure. This is due to two main factors.

For the same current consumption, the complementary-based VCO has higher transconductance which results in faster switching of the differential pair.

The rise and fall time have a better symmetry in the complementary-based VCO, which results in better $1/f^3$ noise corner [Haj99].

Another advantage of the complementary VCO is its higher power supply rejection ratio (PSRR). The low-frequency noise on the supply voltage is directly transferred to the output nodes of the VCO in the cross-coupled nMOS structure. In the complementary VCO, M5 and M6 help reducing the noise that can be transferred from the supply voltage to the output nodes of the VCO.

## *I.5. Conclusion*

The importance of implementing Built-In Self-Tests is highlighted by the interest of the scientific community on this issue.

A brief recall of the main test definitions and of the physical mechanisms generating a defect is given.

Then, the two main test strategies –functional and structural test – are discussed in great detail.

The most common techniques implementing specification-based tests are presented first: loopback, alternate test and hardware-based methods. Pros and cons of each solution are discussed.

While attractive for the great amount of data can be extracted from this kind of test, the high complexity of a functional test does not justify its use for wafer sort applications.

The techniques enabling defect-oriented tests are then introduced.

Emphasis is put on the detectors, which are the main blocks needed for any structural test. Detectors monitoring current, voltage amplitude, power and frequency are illustrated from a general point of view. This study was developed also with the idea to provide the reader with a “handbook” of detectors, which could help the designer in need of a particular on-chip monitoring scheme.

Finally, the decision to study the Voltage-Controlled Oscillator as the Circuit-Under-Test is made.

This main RF block is chosen because of the lack of information on its on-chip testability.

The goal of this work is to help filling this lack.

The role of the VCO in any RX/TX is presented, and its integration in a Phase-Locked Loop is introduced.

Finally, the two main schemes for the design of a RF VCO (ring oscillators and LC oscillators) are discussed.

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## Contents

# II CHOICE OF THE BIST STRATEGY AND OF THE SYSTEM ARCHITECTURE

## *II.1 Choice of a structural test for BIST of the RF VCO*

The first choice that needs to be made is the sort of test to perform. As seen in the previous chapter, there are two main scenarios: functional (specification-based) or structural (defect-oriented).

The main advantage of the functional test is that clear information on one figure of merit of the CUT is given. All ATE commonly used to measure that figure of merit can be eliminated.
The problem is the complexity of this kind of test.
The figure of merit on which almost all research on BIST for RF VCOs focuses, is the phase noise (jitter in the time domain). A great accuracy, in the order of the ps, is needed to be able to measure the phase noise close to the carrier. Large hardware overhead and long test time become fundamental bottlenecks of the test [Hua06].
The requirements for simplicity, low consumption and low Si surface of the BIST cannot be satisfied.
Moreover, no study confirms that the phase noise is the best indicator of the health of the VCO. The fault coverage could be far lower than 100%.

The advantage of the structural test is its simplicity. The wafer sort can discriminate between good and faulty circuits without the need to measure any figure of merit of the VCO.
Reliability is also enhanced. Some faults may not cause unacceptable degradation of the performance of the VCO (functional test says the circuit is good), but the matter of fact is that the fault is present somewhere in the VCO. This fault may cause a malfunctioning later on.
The structural test is able to detect the fault at the wafer sort level, discarding the CUT.

The decision of implementing a structural BIST for VCOs is then taken.

## *II.2 Catastrophic Fault Simulation*

If a fault appears somewhere in the structure of the VCO, all of the electrical quantities of the CUT undergo a deviation (more or less pronounced) from their nominal value.
In order to reach the highest fault coverage, the quantity experiencing the highest deviation for every possible fault (catastrophic and parametric) needs to be found.

This concept is illustrated in Figure II-1. Specifications define a nominal value for a quantity and an acceptable deviation (±Δ) that still guarantees that the required performances of the CUT will be reached.

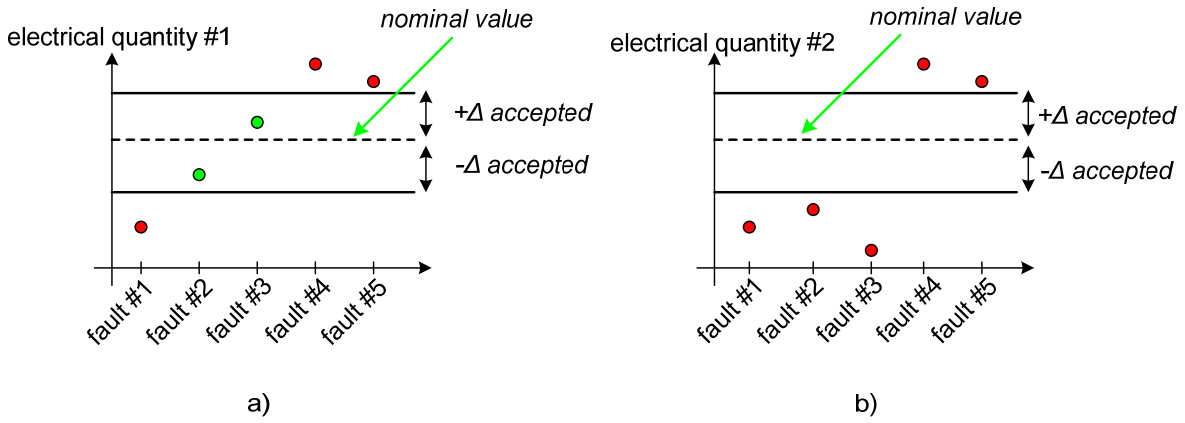


**Figure II-1: An electrical quantity that has small deviations for some faults (left side) and one that has greater deviation for every fault (right side).**

Five faults are injected one by the other in the circuit. In Figure II-1a, fault#2 and fault#3 cause only a small deviation from the nominal value of the electrical quantity #1; the value of the electrical quantity #1 is still inside the acceptance range.

On the contrary, the same faults have a different impact on the electrical quantity #2. In this case (Figure II-1b) every fault causes a deviation of the electrical quantity #2 that makes it exit the acceptance range.

The fault coverage of the case presented in the left side of Figure II-1 is *3/5=60%* while the fault coverage of the second case if *5/5=100%*.

This simple example shows the importance of the fault injection as the first step in the definition of every structural test. The goal of the fault injection is to find the electrical quantity experiencing the highest deviation for every injected fault.

Considering the transistor as a three-terminal device, the following short and open circuits (represented in Figure II-2) can be injected:

- Gate open
- Drain open
- Source open
- Gate-source short
- Gate-drain short

- Drain-source short

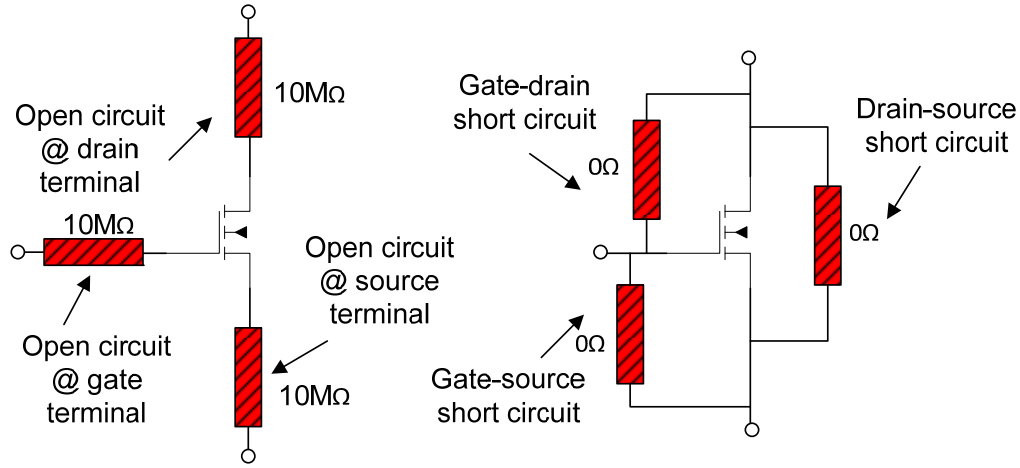


**Figure II-2: Open and short circuits affecting the three terminals of a transistor.**

Passive elements (resistors, capacitors and inductors) are considered as two-terminal devices; only two catastrophic faults can affect them, as shown in Figure II-3.

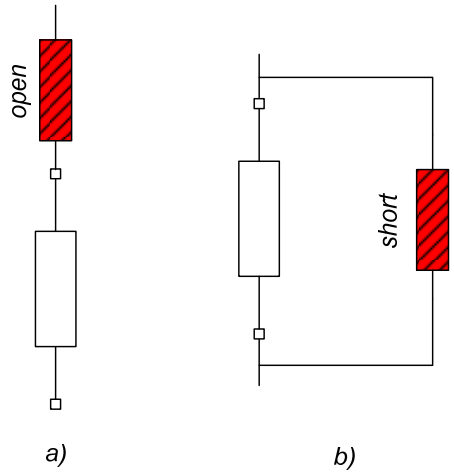


**Figure II-3: Open and short circuits affecting a two terminals passive element.**

In the domain of millimeter-waves, this way of simulating catastrophic faults can be questioned. At very high frequencies, an open-circuit in the line carrying the signal does not necessarily means that the signal will stop travelling through the line. Parasitic capacitances can play a role, as shown in Figure II-4a. A small fraction of the signal can pass the open.

A problem exists for short-circuits too; the coupling capacitance between two close lines may cause part of the high frequency signal to be injected from one line to the other even if no short circuit is physically present, as shown in Figure II-4b.

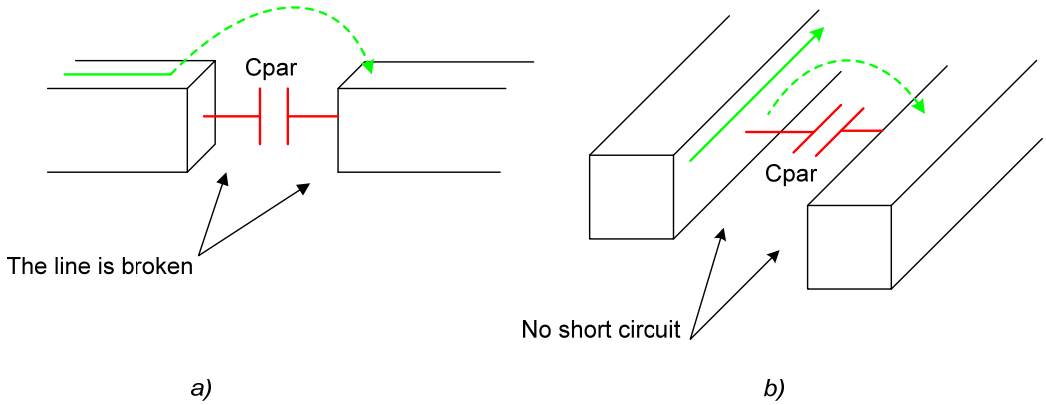


**Figure II-4: A parasitic capacitance may let a small fraction of the high frequency signal pass the open (left side of the figure). Another parasitic capacitance may act as a weak short circuit even if no metal physically connects the two lines (right side of the figure).**

In this work those effects can be neglected without any lack of accuracy.

### *II.3 Extensive fault coverage campaign on two VCOs*

The technology used for all the circuits designed in this work is the ST CMOS 65nm.

Among the different types of transistors available, only Low Power (LP) transistors are employed.

#### *II.3.1 The telecommunication standard addressed by the VCO*

The telecommunication standard addressed by the VCO is the WiMAX (Worldwide Interoperability for Microwave Access).This technology aims at providing business and consumer wireless broadband services on the scale of the Metropolitan Area Network (MAN).

The frequency spectrum allocated to this standard is represented in Figure II-5. Bands above the 5GHz are unlicensed bands not used for mobile applications. Bands between 2.5GHz and 2.7GHz have been allocated in the US, Mexico, Brazil and some Southern Asian countries. The band between 3.4GHz and 3.6GHz has been allocated for fixed wireless access in Europe and other countries [Abi06].

The VCO addresses this portion of the spectrum.

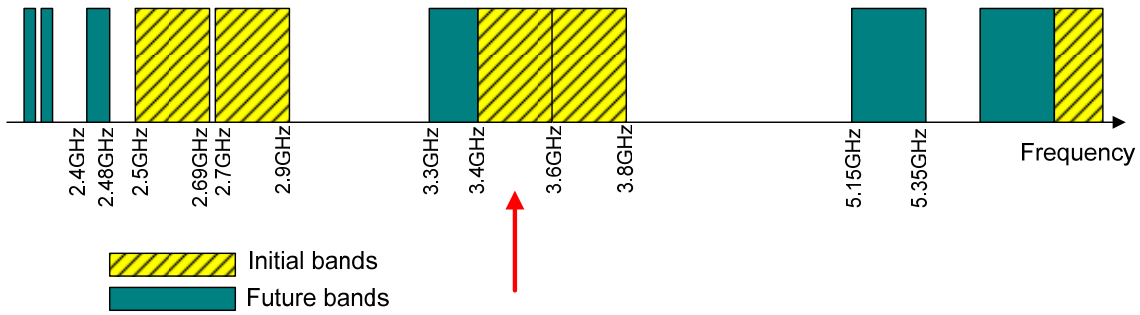


**Figure II-5: Frequency spectrum allocated to the WiMAX (IEEE 802.16) standard.**

### *II.3.2 The circuit under test*

The topology chosen for the realization of the VCO is the complementary cross-coupled structure. A detailed description of the design of the VCO used as a demonstrator will be given later in this chapter.

Here, the structure of the VCOs used for the fault coverage campaign is briefly introduced.

In Figure II-6, the changes made to the general VCO circuit presented in the previous chapter are presented. The main source of phase noise close to the carrier is the *1/f* noise of the transistor used for the current source *Idd*. The current source is then eliminated. A capacitor $C_F$ is connected from the source of M1 and M2 to ground to filter-out higher order harmonics. A resistor *R* is introduced to allow an easy control on the bias current and to allow a transient voltage on the source of M1 and M2 during the simulations.

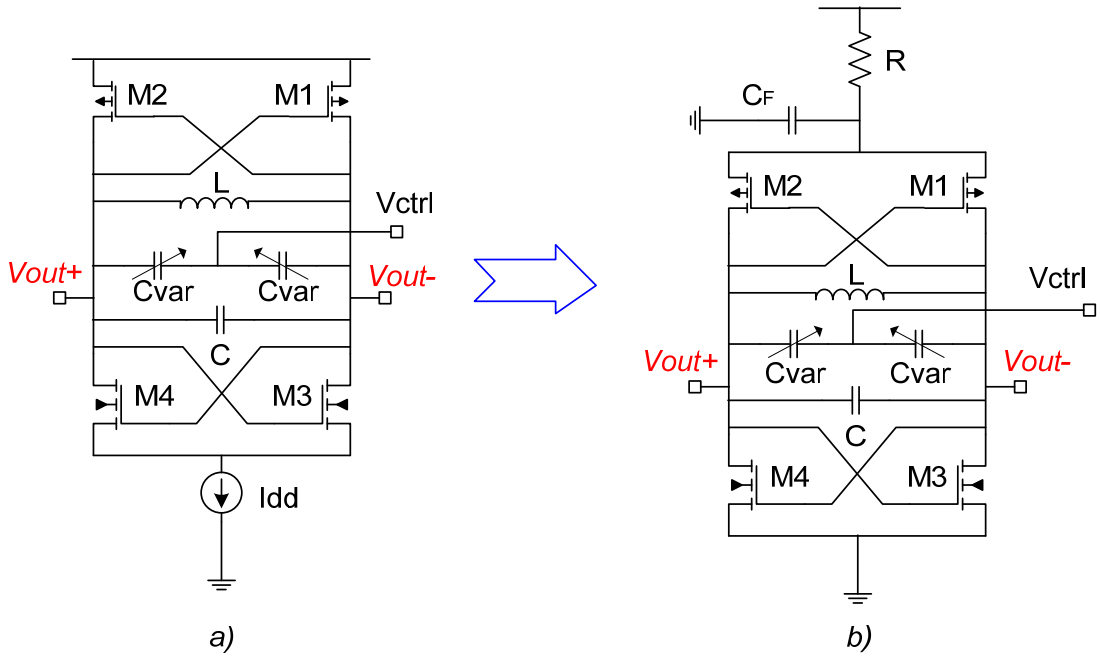


**Figure II-6: Changes made to the general VCO configuration (presented in chapter I)**

We decided to carry out the fault coverage analysis on two VCOs. They have the same LC architecture and almost the same frequency of oscillation, but different DC power and output voltage amplitude; this is achieved simply changing the value of the resistance *R* and the value of the supply voltage.

This decision was taken in order to understand if the fault coverage would have been more dependent on the structure of the CUT or on its consumed power.

The results that will be presented later on lead to the conclusion that the fault coverage is not dependent on the DC power of the CUT, at least at the first order.

This guarantees that the results of the fault analysis will be general for LC-tank VCOs.

The Figure Of Merit (FOM) classically used for VCOs is defined as [Fon03]:

$$FOM = L\{\Delta f\} - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P_{DC}}{1mW}\right) \quad (1)$$

where $L\{\Delta f\}$ represents the phase noise at a frequency offset $\Delta f$ from the carrier $f_0$ and $P_{DC}$ is the power consumption.

The FOM of the two VCOs is almost identical.

The following table summarizes the characteristics of the two VCOs under test.

| | **VCO #1** | **VCO #2** |
|---|---|---|
| **Vdd** | 900 mV | 950 mV |
| **Idd** | 3.4mA | 2.0mA |
| **nMOS** | W=30µm; L=0.1µm; m=2 | |
| **pMOS** | W=50µm; L=0.1µm; m=3 | |
| **L** | 0.88nH | |
| **C** | 1.7pF | |
| **Cvar** | 1.0pF | |
| **R** | 10 Ω | 85 Ω |
| **frequency** | 3.587 GHz | 3.616 GHz |
| **Phase Noise @ 1MHz** | -121.7 dBc/Hz | -118.8 dBc/Hz |
| **Peak-to-peak output voltage** | 760 mV | 480 mV |
| **FOM** | -187.9 dB | -187.2 dB |

**Table II-I: Characteristics of the two VCO used for the fault coverage analysis**

For the VCO#1, the choice was to have a Vdd=900mV in order to design a sub-1V VCO and the value of the resistor *R* was decided in order to have the smallest DC current needed for start-up.

For VCO#2, the choice was to design a CUT with a lower bias current compared to VCO#1. An increase of *R* would have granted a lower bias current, but the supply voltage was too low for the

correct start-up of the oscillation. For this reason, the supply voltage for VCO#2 was slightly increased. For a current consumption of 2.0mA, the value needed for the resistor was 85Ω.

### *II.3.3 Catastrophic Fault injection*

Three kind of catastrophic faults are injected in the VCO:

- Open-circuit emulated with a *10MΩ*-resistance
- Short-circuit emulated with a *0Ω*-resistance
- Short-circuit emulated with a *500Ω*-resistance

Intuitively, the higher the value of the resistance that creates the bridging short-circuit, the more difficult it is to detect. Data reported in [Rod92] show that only a small percentage of the bridges in a CMOS process have a resistance value above 500Ω.

For this reason, the decision was taken to use 500Ω as the maximal value of a short-circuit. If even those faults are detected, we can be confident that all realistic short circuits can be detected.

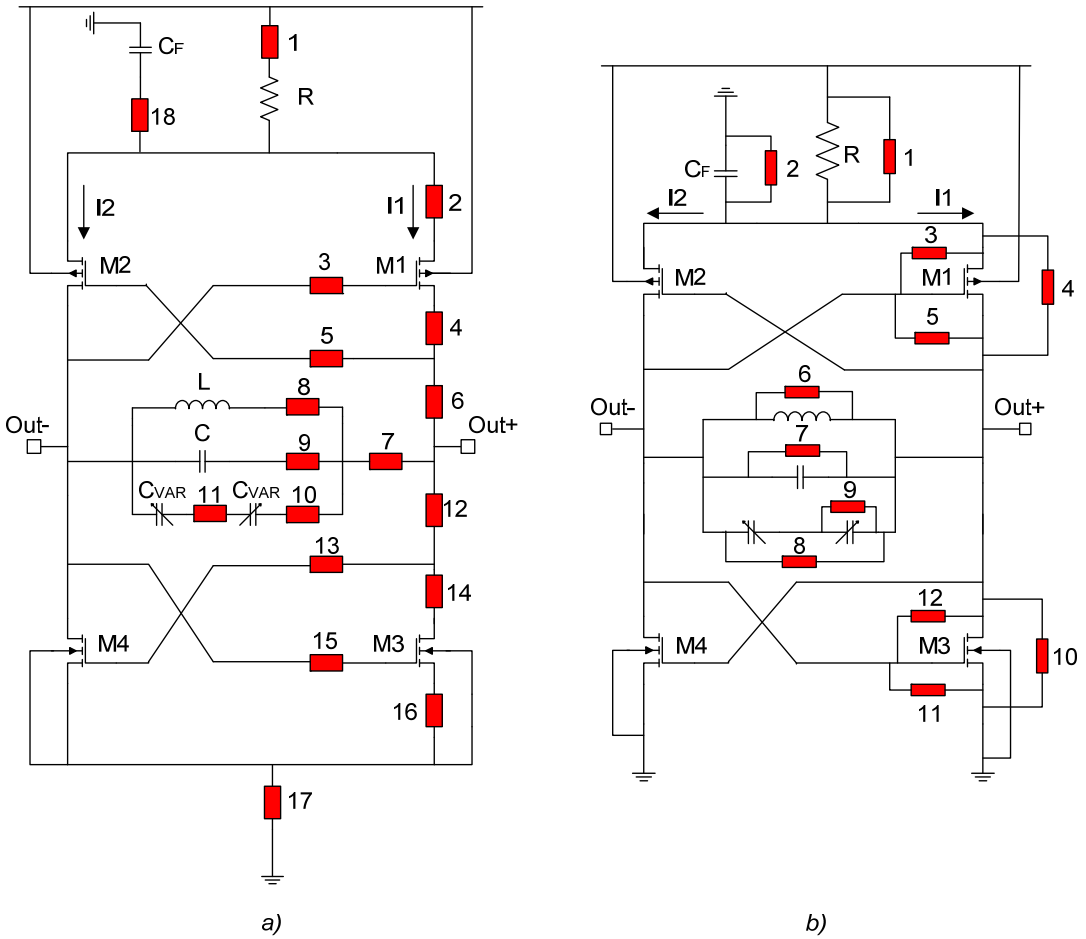


**Figure II-7: Catastrophic faults injected in the VCO. Open-circuits in the left side and short-circuits in the right side of the figure.**

The faults are singularly injected in the VCO, as shown in Figure II-7.

A total of 18 open-circuits and 12 short-circuits are introduced in the CUT. Thanks to the symmetry of the structure of the VCO, the information extracted injecting the 18 open-circuits on only one branch of the circuit can also be used to extrapolate data for the other half also. This gives a total of 28 open-circuits considered. Considering the 12 short-circuits injected, it can be noticed that shorts 5, 6, 7, 8 and 12 represent the same fault. The real number of short-circuits considered is then only 8.

Being the total number of faults quite important, an automatic procedure is created to inject one catastrophic fault at a time in a parametric simulation.

Each resistance is described by an expression rather than a fixed value; this expression contains a variable which is swept during the simulation.

The procedure is as follows: during the $x^{th}$ test for opens (shorts), every resistance is null (really high) except for the $x^{th}$ resistance.

The expression for the open-circuits follows:

$$\begin{cases} for\ x = 1, \dots, 18\ (parametric\ analysis) \\ R_i(x) = abs\left(10M\Omega \cdot \prod_{n=1, n\neq i}^{n=18} \frac{x-n}{n-i}\right) \quad 1 \leq i \leq 18 \end{cases} \tag{2}$$

The expression for the short-circuits is defined as:

$$\begin{cases} for\ x = 1, \dots, 12\ (parametric\ analysis) \\ R_i(x) = R_0 + abs[10M\Omega \cdot (x-i)] \quad 1 \leq i \leq 12 \end{cases} \tag{3}$$

In the expression for the short-circuits, the term $R_0$ represents the physical value of the short-circuit injected: either 0Ω or 500Ω. The term *10MΩ(x-i)* is needed for all other resistors shown in Figure II-7b to almost open-circuits.

### *II.3.4 Parametric Fault injection*

The injection of parametric faults consists in making variations in the dimensions of the geometries of the components of the VCO.

This represents errors and dispersions in the process of fabrication.

While parametric faults on transistors can be omitted, the influence of parametric faults on passive elements is higher. This is especially true for a VCO, whose frequency of oscillation is defined by the value of the passive elements composing the resonator. Moreover, the phase noise is a function of the quality factor of the tank.

The variations on the passive elements are performed as follows:

- L (1 ± 5%)
- C (1 ± 10%)

Those are realistic values for the ST CMOS 65nm process.

Having one fixed capacitor, two varactors and one inductor in the resonator, 8 simulations can be performed. Only one passive element at a time is affected by the fault injection.

### *II.3.5 Decision of the signals to take into account*

For every fault injected, a transient analysis is simulated.

The first step is to decide which signals need to be taken into account during the analysis. Keeping in mind that the on-chip realization of the detector has to be feasible, some quantities are rejected from the beginning. This is why the monitoring of the sum of the *average* of two currents is preferred to the monitoring of the *instantaneous* sum of the same currents, which would entail the design of a detector with very high bandwidth. For the same reasons, S-parameters are rejected also.

The choice of simple-to-detect signals lets the road open for BIST in the millimeter-wave field also.

The signals under study are then averages or peak values of currents and voltages. All those quantities can be detected on-chip with simple circuits, that won't need too much power or extra silicon area. The criteria for a simple detector and a low-cost BIST will then be fulfilled.

The list of the electrical quantities taken into account during the fault injection follows:

- Average (Vout+) & Average(Vout-)
- Average(Vout+) + Average(Vout-)
- Average(Vout+) - Average(Vout-)
- Max(Vout+) & Max(Vout-)
- Vpp(Vout+) & Vpp(Vout-)
- Vpp(Vout+) – Vpp(Vout-)
- Average(I1) & Average(I2)
- Average(I1) + Average(I2)
- Average(I1) – Average(I2)
- Average(Itot)
- Max(I1) & Max(I2)
- Ipp(I1) & Ipp(I2)

*Vout* represents the output voltage, *I1* and *I2* stand for the currents flowing in M1 and M2, *Max* is the function finding the maximum value of the quantity, *Vpp* is the peak-to-peak value of the output voltage, *Ipp* is the peak-to-peak value of the dynamic current.

Special care has been taken not to collect false data.

For example, when observing the waveforms of the currents *I1* and *I2* of the VCO, the Average operation is not carried out before the oscillation is stable.

The importance of this consideration can be understood looking at Figure II-8; before the start-up of the oscillation, the current flowing through the VCO is considerably lower than the current after onset of the self-sustained oscillation. If the simulator takes the initial transient into account for the calculation of the average, the value obtained is wrong.

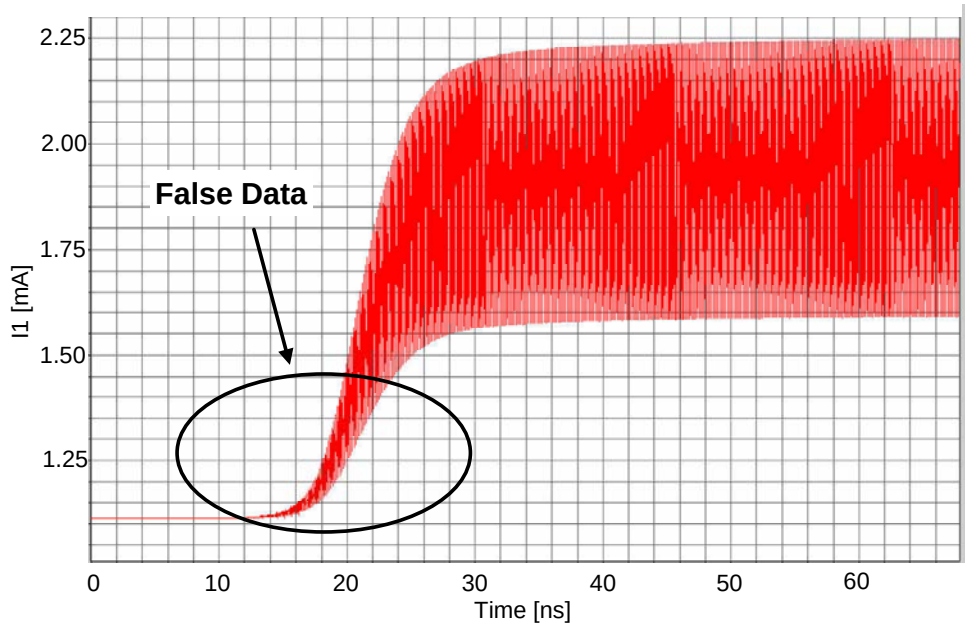


**Figure II-8: Start-up of the oscillation. The average operation on the current can be done only starting from t=50ns.**

### *II.3.6 Choice of the acceptance boundaries*

As explained in Figure II-1, an acceptance boundary is needed because any electrical quantity of the CUT is characterized by an average and a standard deviation.

Specifications should assign those boundaries. During this first study, no specifications were given. The decision was taken to establish the boundaries as follows:

$\Delta V = \pm 25$ mV

$\Delta I = \pm 500$ µA

Those values were chosen to take into account deviations of currents and voltages of the VCOs, caused by process variations and mismatch of the components. The current of VCOs is known to experience high deviations compared to the voltages. This is why, in percentage, the boundary chosen for the current is higher than the boundary for the voltages.

Once the boundary decision made, the transient simulation are run for each fault and for both VCOs. Two examples of the results are now given.

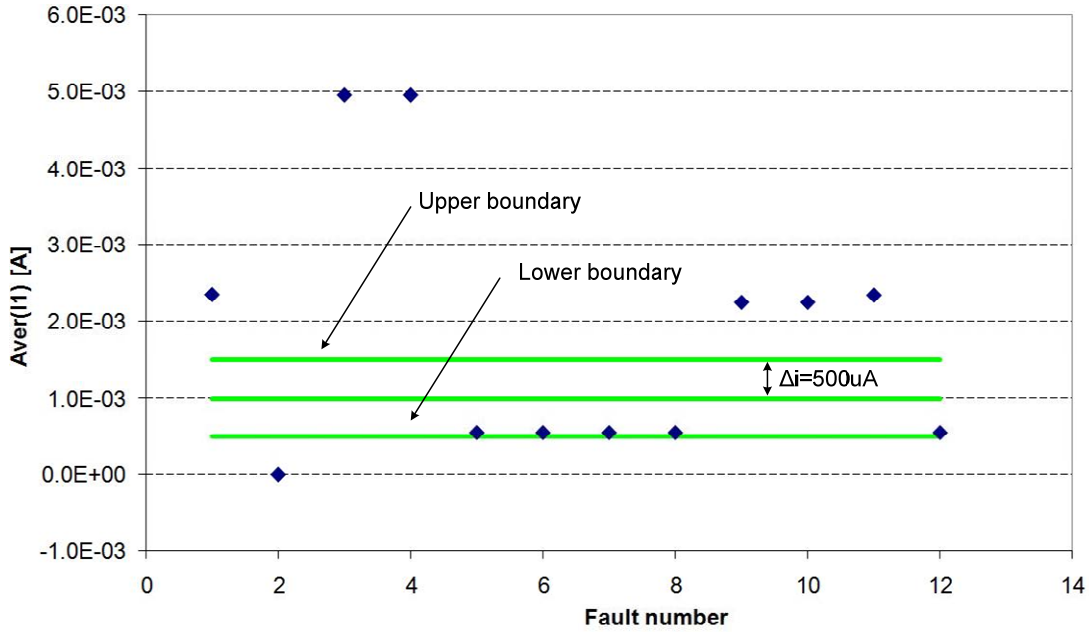


**Figure II-9: Values collected for *Average(I1)* in the case of the 0Ω short circuits injected; VCO#2.**

In Figure II-9 the 12 short circuits are singularly injected and the value of *Average(I1)* is collected. The results for faults 5, 6, 7, 8 and 12 (the faults shown in Figure II-7b) show the same value. Those faults are used a check on the simulation. In fact, being faults 5, 6, 7, 8 and 12 redundant, the fact of obtaining for them the same data validates the methodology used for the automatic fault generation.

A short-circuit between the output terminals of the VCO does not sufficiently change the average value of the current flowing in the branch of the circuit. This fault could not be detected using the DC current value as the sensing quantity.

In Figure II-10, the 12 short-circuits are singularly injected and the value of *Vpp(Vout+)* is collected. All faults create an important deviation from the nominal value; they are then all detectable.

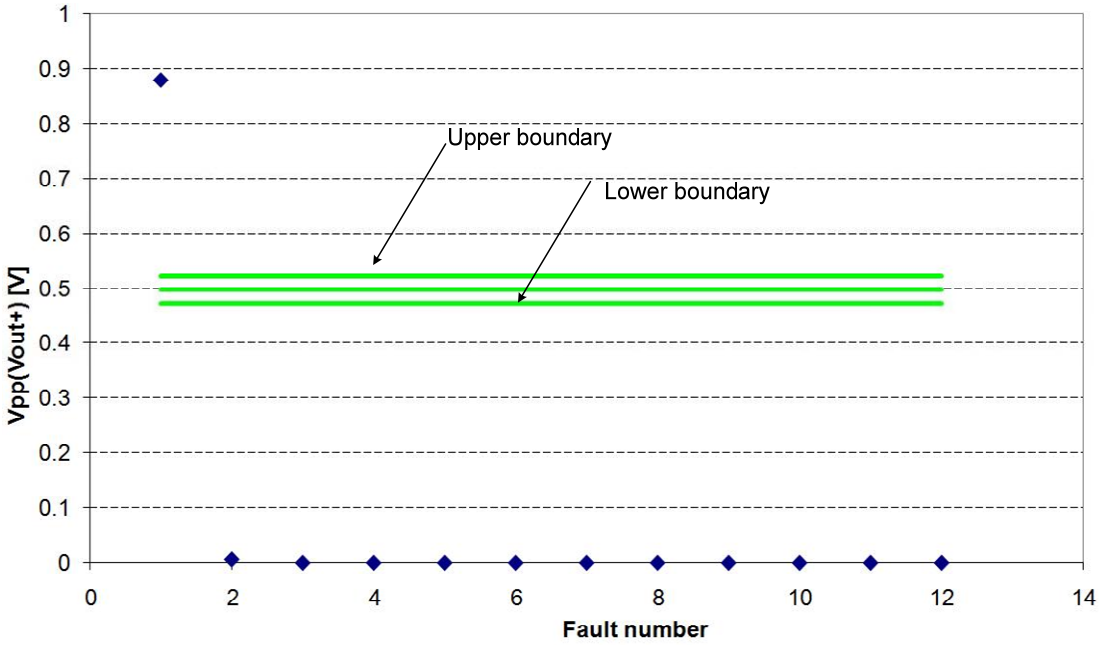


**Figure II-10: Values collected for *Vpp(Vout+)* in the case of the 0Ω short-circuits injected; VCO#2.**

### *II.3.7 Fault coverage for catastrophic faults – a first screening*

Graphs as those shown in Figure II-9 and Figure II-10 are created for every signal of the list given above.

The fault coverage is then calculated as the ratio between the number of detectable faults and the total number of injected faults.

The results of the injection of open-circuits and short-circuits (0Ω and 500Ω) are presented in Figure II-11.

There is only a slight difference in the fault coverage for the two VCOs. The following considerations are then valid for both of them and for LC-tank VCOs in general.

The signals that give the lowest fault coverage are those concerning the *difference* between symmetric quantities ("+" and "-" sides of the VCO). This is due to the fact that most injected faults equally affect the "+" and the "-" side of the VCOs. Their difference then does no show high deviations from the fault-free value.

The highest fault coverage is obtained monitoring either the peak-to-peak value of the current or the peak-to-peak value of the output voltage (97.7%). The peculiarity of those signals is that they give information on the "health" of the oscillation; signals based on average give information on the bias of the circuit. Being the CUT an oscillator, it is logic that peak-to-peak values give a better fault coverage.

From the catastrophic fault injection, *Ipp* and *Vpp* result the best candidates for the on-chip monitoring. The parametric fault injection will allow deciding between the two.

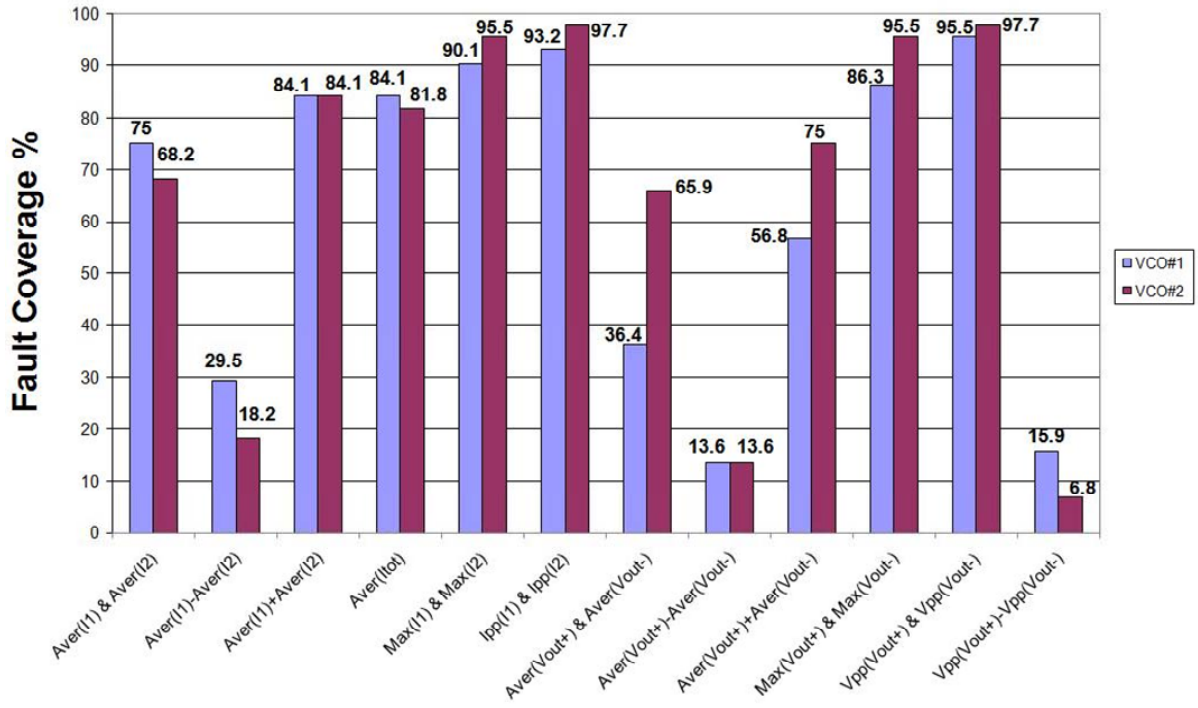


**Figure II-11: Fault coverage relative to catastrophic faults for VCO#1 and VCO#2.**

### *II.3.8 Fault coverage for parametric faults - decision of the signal to monitor*

Parametric faults are harder to detect than catastrophic faults.

Among all the signals monitored, only *Ipp(I1)*, *Ipp(I2)*, *Vpp(Vout+)*, *Vpp(Vout-)*, Max*(Vout+)* and *Max(Vout-)* show some deviation when the VCOs are affected by a parametric fault.

All other signals are almost unaffected.

In the following table, “Yes” means that the fault is detected, while “No” means that the fault is not detected.

| | VCO #1 | | VCO #2 | |
|---|---|---|---|---|
| | **Vpp** | **Ipp** | **Vpp** | **Ipp** |
| L·(1 - 5%) | Yes | No | Yes | No |
| L ·(1+ 5%) | No | No | Yes | No |
| C ·(1- 10%) | Yes | No | Yes | No |
| C ·(1+ 10%) | Yes | No | Yes | Yes |

**Table II-II: Results for the parametric faults coverage**

This final analysis clarifies the advantage of monitoring the peak-to-peak value of the output voltage, compared to the peak-to-peak value of the current.

*II.4 Choice and design of the system architecture*

A demonstrator needs to be designed in order to:

1. validate the BIST strategy and the choice of Vpp as the signal to monitor
2. show the transparency of the BIST

The architecture of the system is represented in Figure II-12.

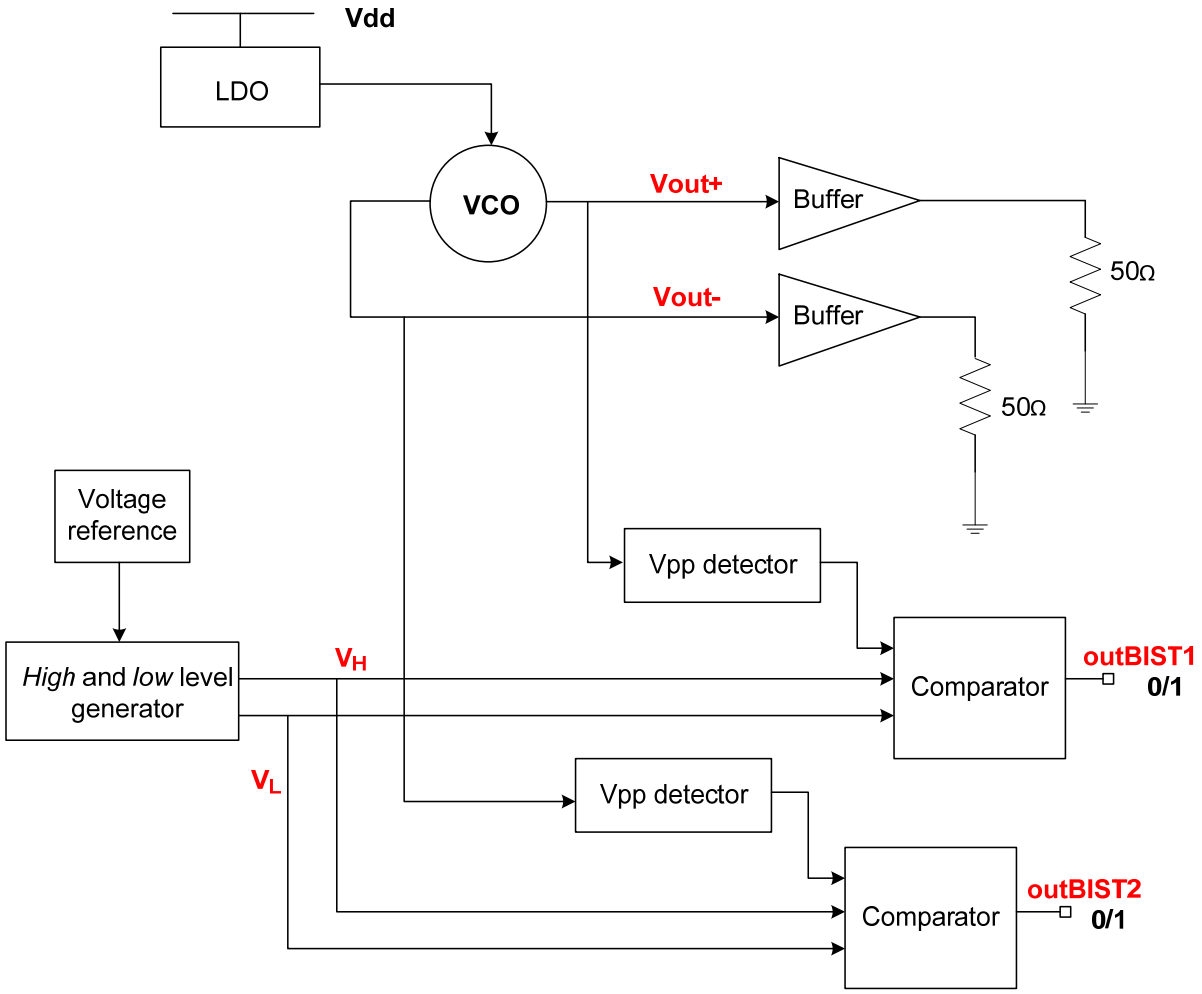


**Figure II-12: Block view of the architecture of the system**

A Low DropOut voltage regulator (LDO) supplies the VCO. The output of the VCO is connected to a buffer, needed to drive the 50Ω-load of the instrumentation.

The Vpp voltage detector is connected to the output of the VCO; this block outputs a DC-voltage that is an image of the peak-to-peak value of the output voltage of the CUT.

A voltage reference and a level generator are used to output the DC voltages used as the upper and lower boundaries of the acceptance range.

A comparator finally checks if the information of the VPP detector falls inside or outside the acceptance range. The binary output information (0-1) is used to decide if the CUT has to be discarded or if it passes the wafer sort test.

Every block will now be presented, together with results of simulations using Spectre in Cadence.

### *II.4.1 LDO – power management for the CUT*

The LDO is a voltage regulator that supplies the VCO with a well-specified and stable voltage.
This block has two main functionalities:

1. In the case of a battery-supplied system, the voltage of the battery decreases because of its aging; the LDO supplies the VCO always with a fixed voltage, even in the case of a low-battery situation.
2. It rejects the noise from the external power supply; this external noise is reported to be among the major contributors of the phase noise of the VCO.

The decision to power the VCO via an LDO has two main disadvantages:

1. The voltage available for the VCO is lowered, because of the voltage drop on the pass element shown in Figure II-13. This voltage drop can be reduced (hence the name LDO) increasing the size of the transistor playing the role of pass element.
2. The noise of the voltage reference (needed to drive the LDO) will be seen at the output of the LDO, and it will increase the phase noise of the VCO. This noise is still lower compared to the noise of the external supply voltage, and it can be evaluated (while the evaluation of the supply voltage noise is non-trivial).

The simplified synoptic of the LDO representation is given in Figure II-13.

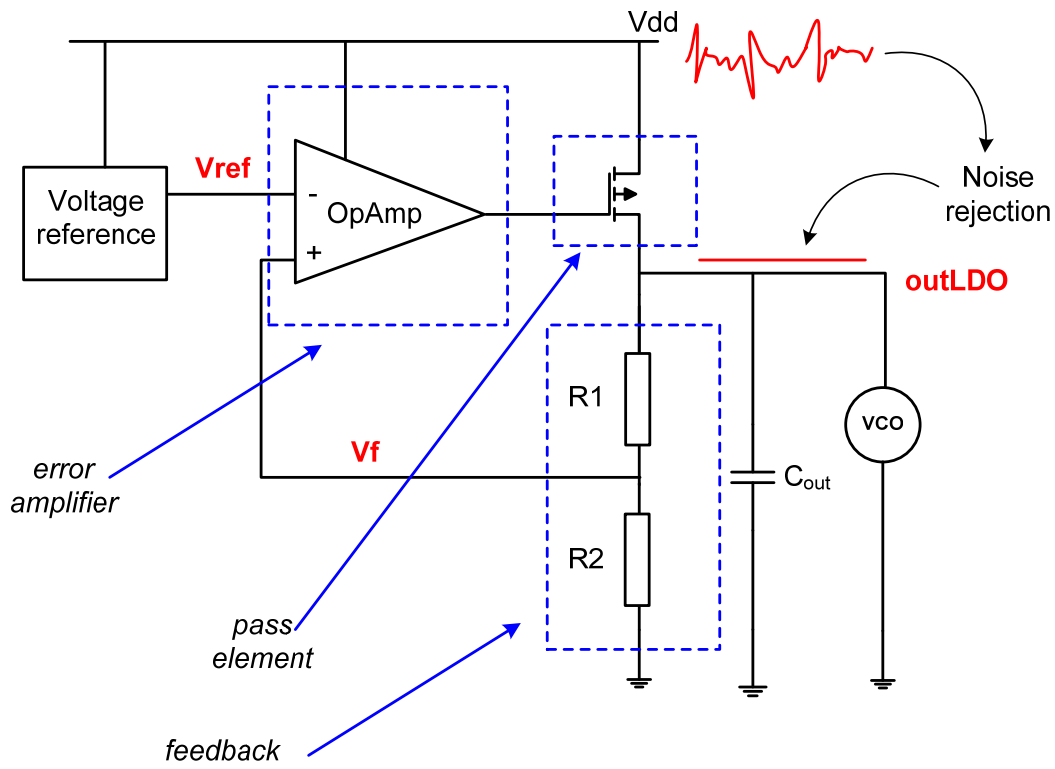


**Figure II-13: Simplified synoptic representation of the LDO**

The circuit is composed of a voltage reference, an error amplifier, a pass element and a feedback network. The operation of the circuit is based on feeding back an amplified error signal to control the current flowing through the pMOS pass element.

The voltage reference provides a stable DC-voltage with limited current driving capabilities.

The temperature coefficient of the LDO is defined by the temperature dependence of the voltage reference and by the input offset-voltage of the error amplifier [Rinc96].

Special care will be taken in the design of a temperature and supply-voltage independent voltage reference, which will be exhaustively presented in the following section.

The equations describing the behavior of the LDO (considering an OpAmp with infinite gain) follow:

$$outLDO = \frac{R_1 + R_2}{R_2} \cdot V_f \qquad (4)$$
$$V_f = V_{ref}$$

The voltage reference fixes the value of the voltage $V_{ref}$; the operational amplifier guarantees that the feedback voltage $V_f$ follows $V_{ref}$.

Since $V_{ref}$ is fixed, the value of the output voltage of the LDO is determined by the value of the two resistors $R_1$ and $R_2$.

Two criteria determine the value of the output voltage of the LDO:

1. The pMOS pass-element must work in the saturation region
2. The functionality of the VCO must be guaranteed

The first criterion implies a low output voltage, while the second calls for a high output voltage. Being the supply voltage 1.2V, the choice was made to fix *outLDO*=965mV.

The Power Supply Rejection Ratio (PSRR) is defined as the ratio between the magnitudes of the signal injected from the power supply and that of the signal at the output of the LDO.
If the open-loop gain is high, the PSRR is enhanced.
In order to have such a high open-loop gain, two operational amplifiers are cascaded.
Their design is shown in Figure II-14. An active load based on pMOS transistors is designed to allow a high gain limiting the voltage drop on the load.

Each operational amplifier is individually stable (phase margin >> 0°); the chain of the two operational amplifiers (OpAmp) however results in an unstable LDO. The Bode diagram of the open-loop system is shown in Figure II-15. The phase margin is negative. The response of the system to an impulse would be an oscillation.

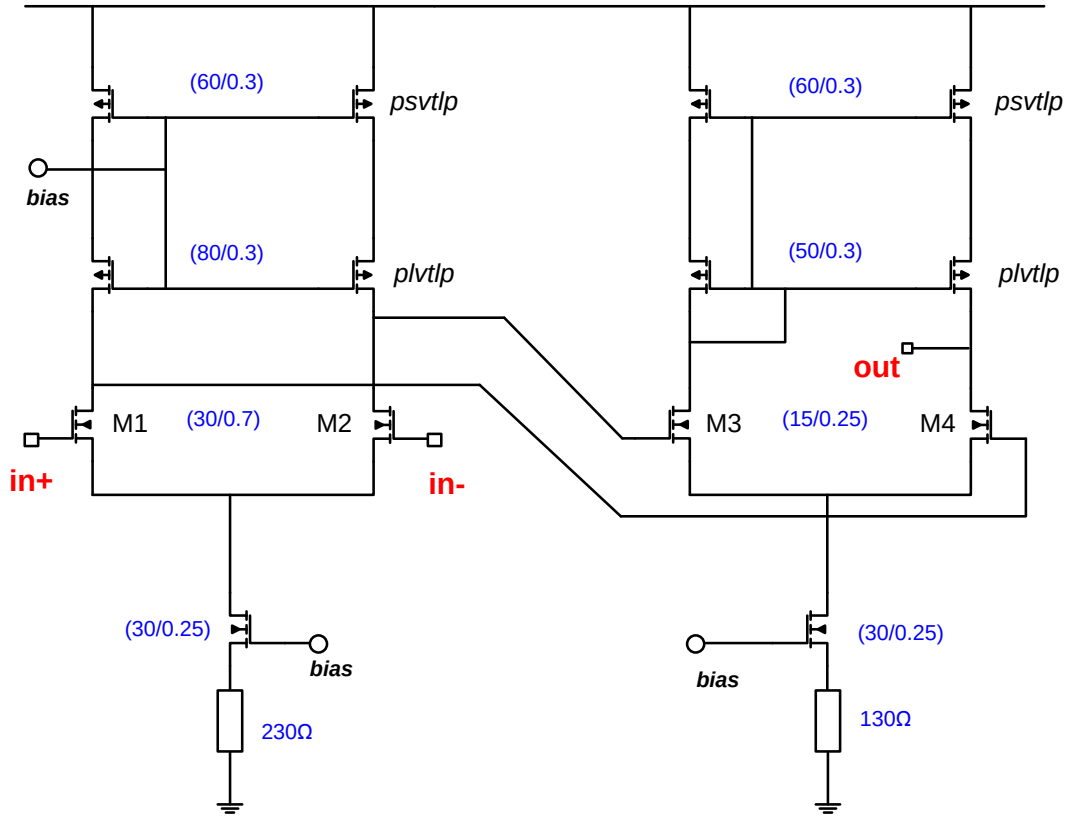


**Figure II-14: The two cascaded operational amplifiers are needed to have a high open-loop gain**

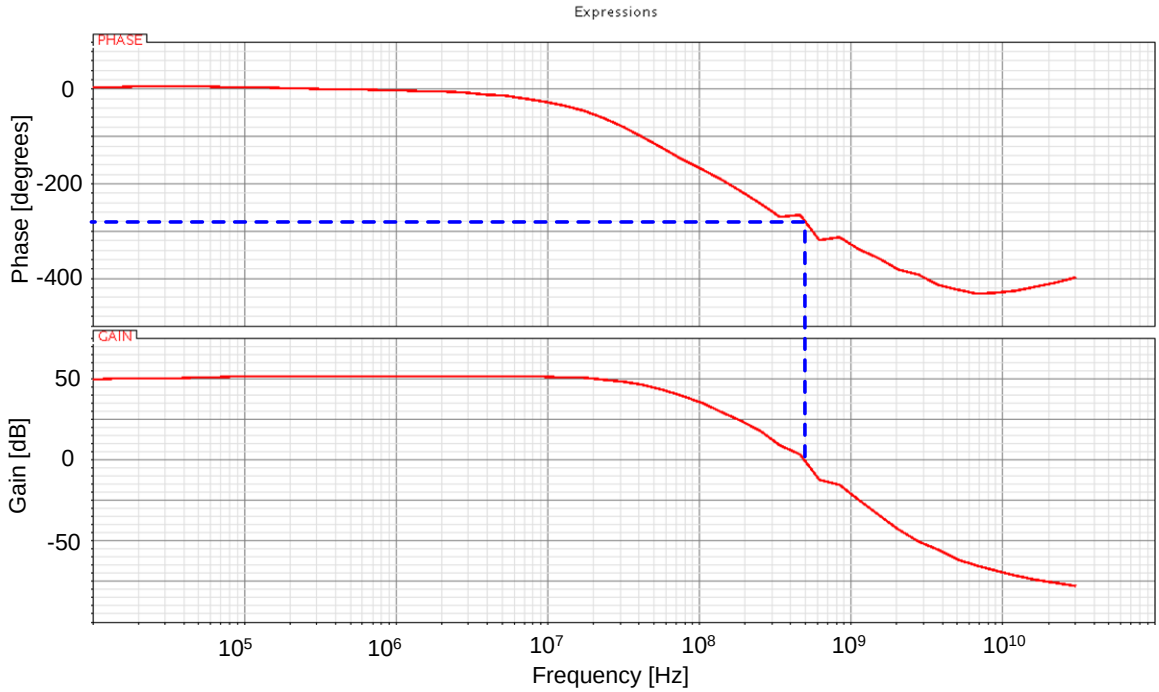


**Figure II-15: Bode diagram of the open-loop before compensation scheme; *phase margin = -100°***

To eliminate the instability and guarantee a good phase margin, three RC networks for compensation (nested Miller compensation technique) are introduced, as shown in Figure II-16.

The new Bode diagram of the open-loop system, represented in Figure II-17, shows a new phase margin of approximately 60°; the instability is removed.

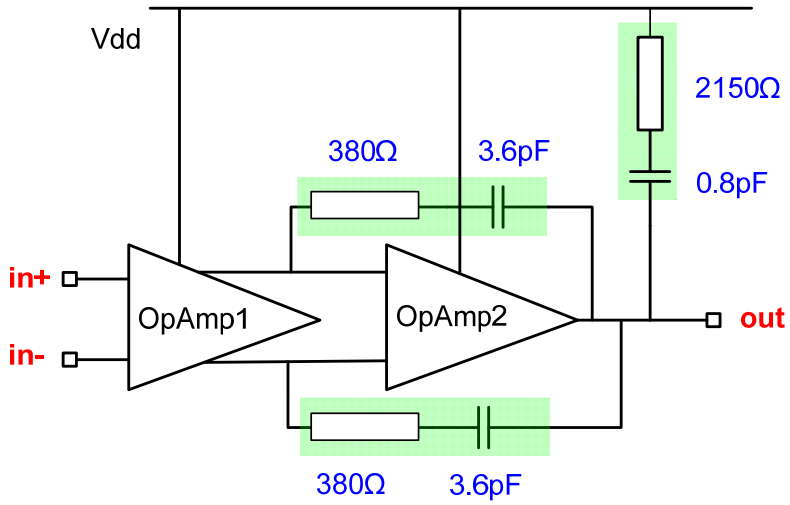


**Figure II-16: Nested Miller compensation network employed to eliminate the instability of the system**

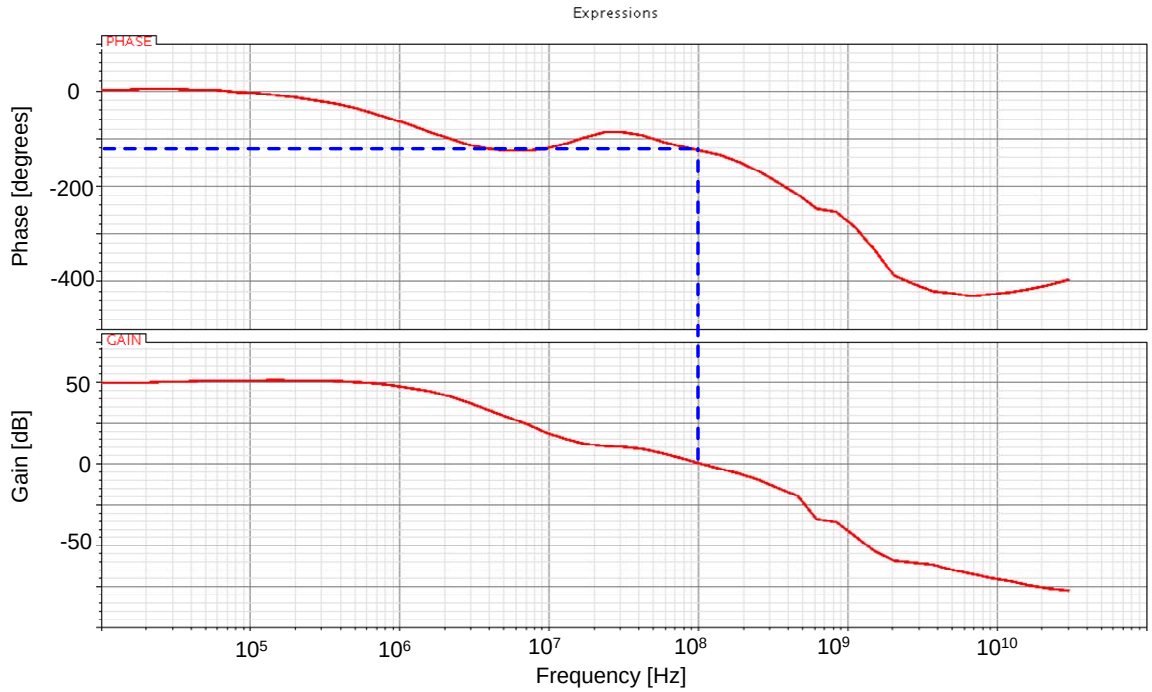


**Figure II-17: Bode diagram of the open-loop after compensation scheme; *phase margin = +60°***

A transient simulation can be used to confirm the stability of the system.

The response of the LDO to an output current pulse is observed in the lower portion of Figure II-18; the output voltage rapidly settles to its final voltage, without oscillations.

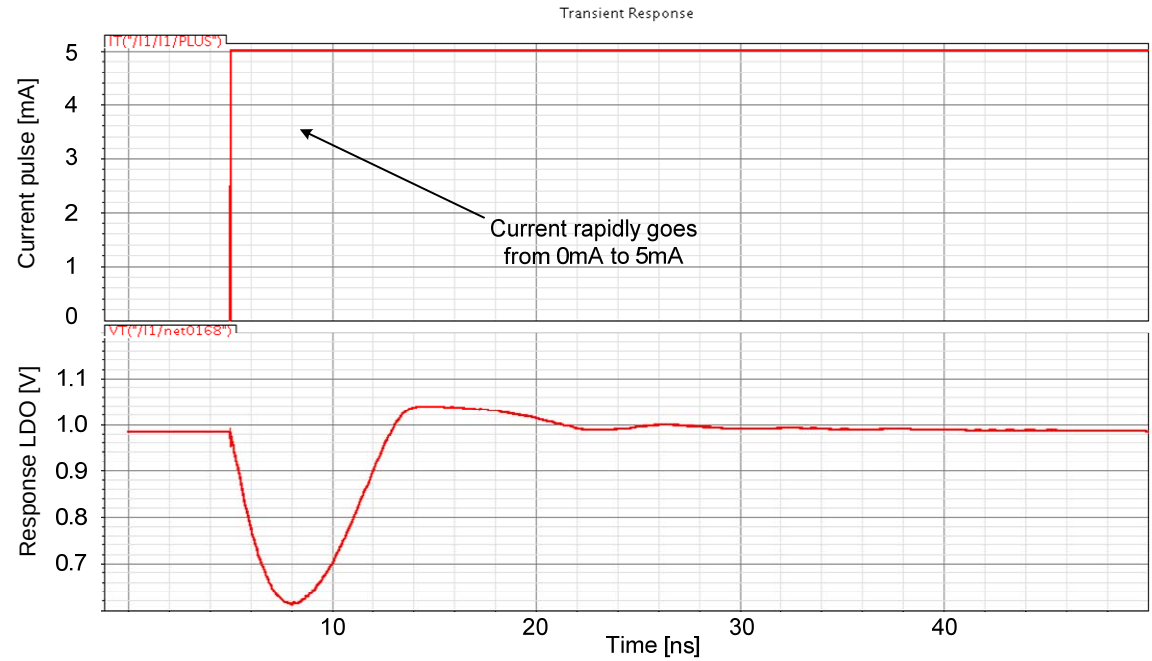


**Figure II-18: Current pulse on the upper portion of the figure; voltage response on the lower portion**

The common-mode of the two OpAmps needs to be controlled also. A change in the common-mode (due for example to a change in temperature), would cause the malfunctioning of the system.

The two input voltages $V_{ref}$ and $V_f$ of Figure II-13 would not be able to follow each other anymore.

This is why a common-mode feedback control is introduced, as shown in Figure II-19.

If the output common-mode voltage of the first OpAmp increases, the voltage at the source of M3 and M4 increases. The feedback allows the voltage at the gate of M7 to increase also. This increases the DC-current of the first OpAmp, allowing the output common-mode voltage to decrease.

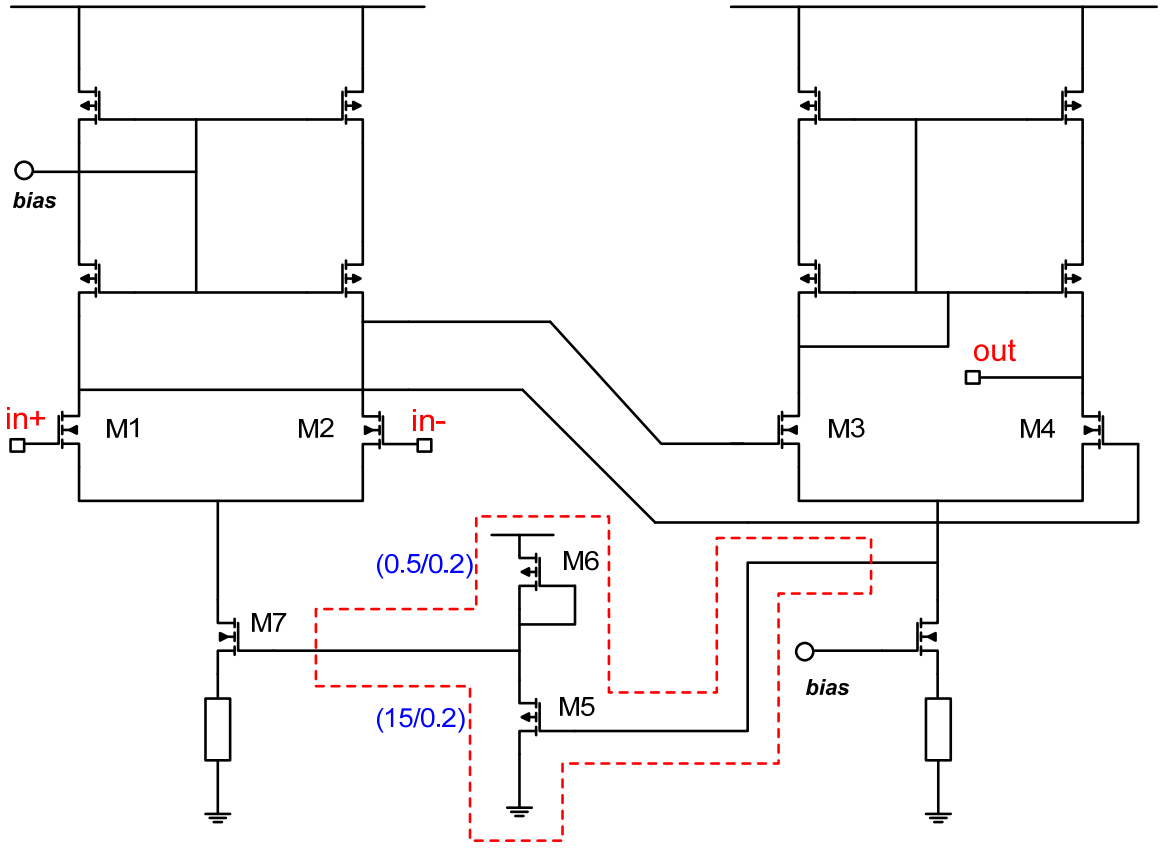


**Figure II-19: Common-mode control applied on the two OpAmps**

Finally, the PSRR of the LDO is simulated and presented in Figure II-20. Four main portions can be distinguished [Gup04]:

1. At low frequencies, the PSRR is closely related to the inverse of the open-loop gain of the system.
2. Beyond the bandwidth of the OpAmp, a zero in the transfer function of the PSRR appears and the PSRR starts deteriorating.
3. A pole appears at the Unity-Gain Frequency of the OpAmp; at this frequency the PSRR has its worst value, because the closed-loop output resistance is not decreased by the feedback

loop (because the open-loop gain is too small) and the output capacitor $C_{out}$ cannot shunt the output ripple to ground (because the frequency is not high enough).

4. At higher frequencies, the output capacitor $C_{out}$ starts shunting the output ripple to ground, improving the PSRR. If the equivalent series resistance of the capacitor $C_{out}$ were not negligible, a new zero would have appeared, deteriorating the PSRR again.

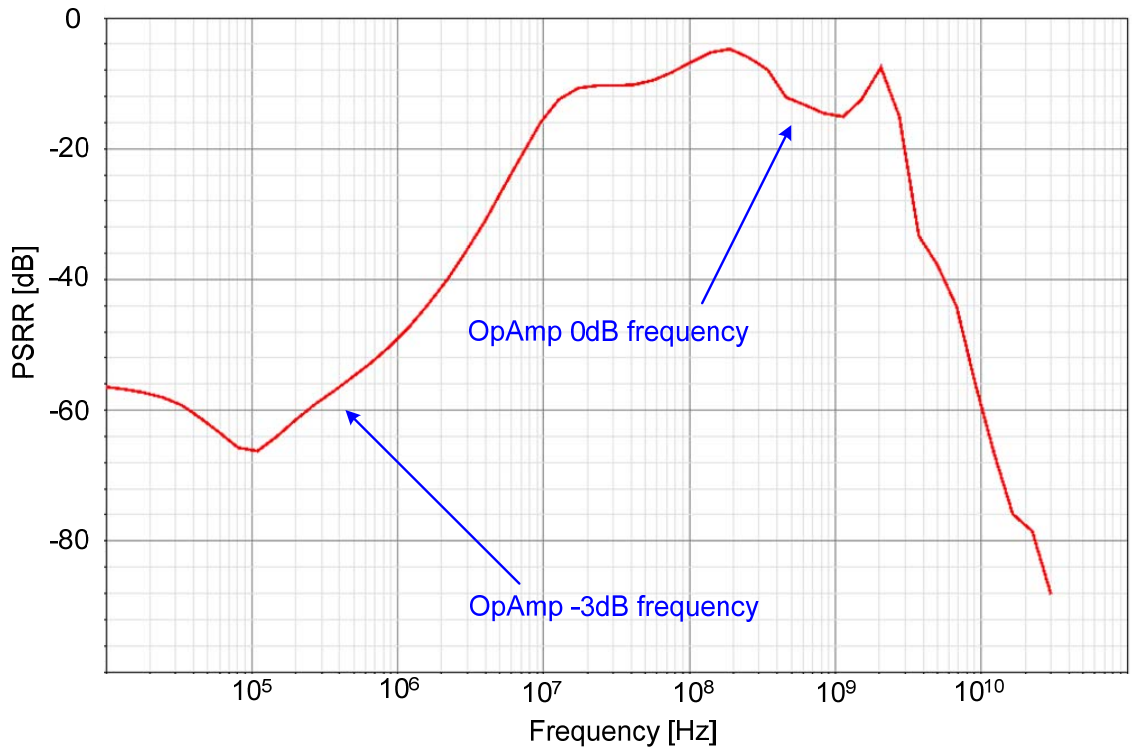


**Figure II-20: PSRR of the LDO**

The consumption of the LDO is almost entirely dictated by the consumption of the two OpAmps, because resistors R1 and R2 in Figure II-13 are chosen to sink a very small current.

Each OpAmp is powered with a 1.2V supply voltage and consumes approximately 230µA.

### *II.4.2 Voltage-Controlled Oscillator – the CUT*

As explained earlier in this chapter, the VCO is designed as a negative-gm oscillator.

The complementary cross-coupled transistors implement a negative resistance that counterbalances the energy loss in the LC resonator.

#### *II.4.2.1 Choice of the passives for the tank*

The values of the passive elements composing the resonator are primarily fixed by:

- Value of the center frequency of oscillation (3.5GHz)
- Value of the frequency range (200MHz)
- Dimensions of the inductor (need to be as small as possible in order to save Si area and grant a low-cost VCO)

Moreover, the rule of thumb that grants good performance of the VCO is:

$$L[H] \approx 1000 \cdot C[F] \quad (5)$$

The value of the inductor is approximately the value of the capacitor, multiplied by the factor 1000[H]/[F]. This allows maximizing the energy stored in the inductor.

The frequency of oscillation is a function of the values of the passive elements in the resonator; the relationship is:

$$\omega = \frac{1}{\sqrt{LC}} \quad (6)$$

where the value of *C* is the sum of every fixed, variable and parasitic capacitances connected at the tank.

The following values are then chosen:

| | |
|---|---|
| **L** | 0.88nH |
| **C** | 0.7pF |
| **$C_v$** | 0.95pF |

**Table II-III: Values chosen for the passive elements of the VCO**

Those values represent a good tradeoff that allows covering the frequency band 3.4GHz – 3.6GHz with a relatively small inductor and a value for the varactors that does not degrade too much the phase noise of the VCO, negatively affected by the connection of the varactors.

#### *II.4.2.2 Reminder of the negative-gm theory and first estimation of the value of gm*

The small-signal model of the cross-coupled pair is proposed in Figure II-21; a voltage generator is connected to find the input resistance of the structure:

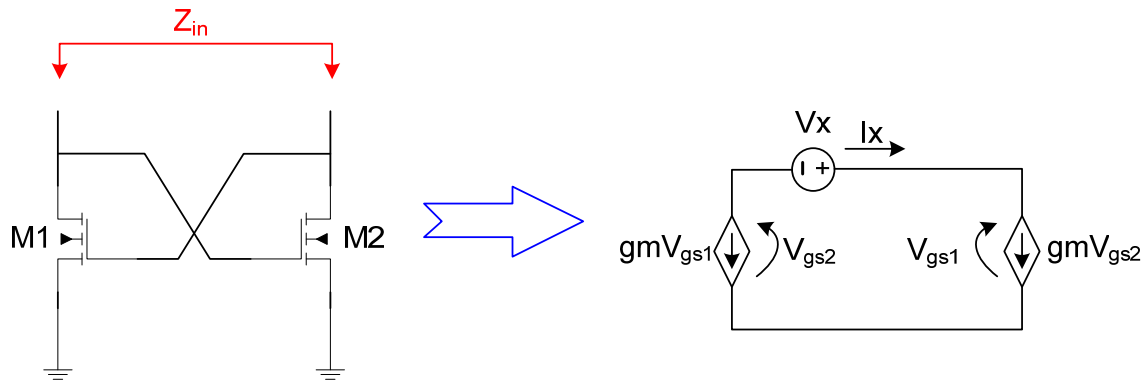


**Figure II-21: Small-signal model of the cross-coupled pair**

$$\begin{cases} g_m v_{gs1} = -g_m v_{gs2} \\ v_{gs2} = v_{gs1} - V_X \end{cases} \quad (7)$$

Then:

$$v_{gs1} = \frac{V_X}{2} \quad (8)$$

and finally:

$$I_X = -g_m \frac{V_X}{2} \quad (9)$$

The last equation proves that the input resistance is:

$$R_{in} \equiv \frac{V_X}{I_X} = -\frac{2}{g_m} \quad (10)$$

Even if this analysis is attractive for its simplicity, it has to be kept in mind that the small-signal model of the transistor is valid only for small variations from the bias point, which is not the case for a VCO. Anyhow, a first guess of the value of the transconductance needed for stable oscillation can be inferred.

The absolute value of $R_{in}$ needs to be (at least) as high as the equivalent parallel resistance of the resonator.

The element that limits the quality factor of the tank is the non-negligible series resistance of the inductor. To calculate the parallel resistance of the tank, it is then possible to take into account the only series resistance of the inductor and the quality factor of the inductor.

It is possible to demonstrate that:

$$R_p = Q^2 \cdot R_s \quad (11)$$

where $R_p$ represents the equivalent parallel resistance of the resonator, $R_s$ is the series parasitic resistance of the inductor and Q is the quality factor of the inductor, defined as:

$$Q = \frac{\omega L}{R_s} \tag{12}$$

A symmetric spiral inductor of approximately 1nH is used in the resonator. In the ST CMOS 65nm process, the value of the parasitic series resistance of this element is roughly $R_s$ = 2Ω.

At the frequency of 3.6GHz, this translates in a quality factor Q ≈ 10.

The value of the resistance that needs to be counterbalanced by the active circuit is then of about 200Ω.

This information gives a first lower limit to the transconductance. Making the hypothesis that pMOS and nMOS transistors have the same transconductance, and that the two cross-coupled pairs give rise to two negative resistances that are in parallel:

$$2R_{in} \geq -R_P \Longrightarrow 2 \cdot \left(-\frac{2}{g_m}\right) > -200\Omega \Rightarrow g_m > 0.02\ [S] \tag{13}$$

For the correct start-up of the oscillation, the gain needs to be slightly greater than 1 (Barkhausen's criterion). If the assumption is made that the load seen by the transistor is represented by the equivalent parallel resistance $R_p$ (which is true at the resonant frequency of the tank), then a new lower limit to the transconductance is found:

$$2 \cdot g_m \cdot R_p > 1 \Rightarrow g_m > 0.0025[S] \tag{14}$$

The transconductance is multiplied by a factor 2 because the structure is complementary.

Equation (40) proves also that the start-up of the oscillation in a complementary cross-coupled structure needs a lower current compared to the nMOS-only cross-coupled oscillator.

The most stringent criterion is the one dictated by the need to counterbalance the energy loss in the resonator. The current will primarily be established on this criterion.

#### *II.4.2.3 First estimation of the current*

The VCO is shown in Figure II-22. M1 and M2 are the nMOS cross-coupled pair; M3 and M4 are the pMOS cross-coupled pair. *L* is the inductor and *C* is the fixed capacitor. The two capacitors $C_v$ are the two varactors (variable capacitor) that give the possibility to change the value of the frequency of oscillation via the control voltage $V_{ctrl}$.

Making the assumption that the DC output voltage will be equal to half the output voltage of the LDO (fixed at 965mV), the value of the current granting the right value of transconductance can be found.

$$g_m = \frac{2I_d}{(V_{gs} - V_{TH})} \tag{15}$$

Then, considering a threshold voltage $V_{TH}$ = 250mV:

$$g_m > 0.02S \Rightarrow I_d \geq 2.3mA \quad (16)$$

Although inaccurate, this analysis allows having a first idea of the value of the current consumed by the VCO.

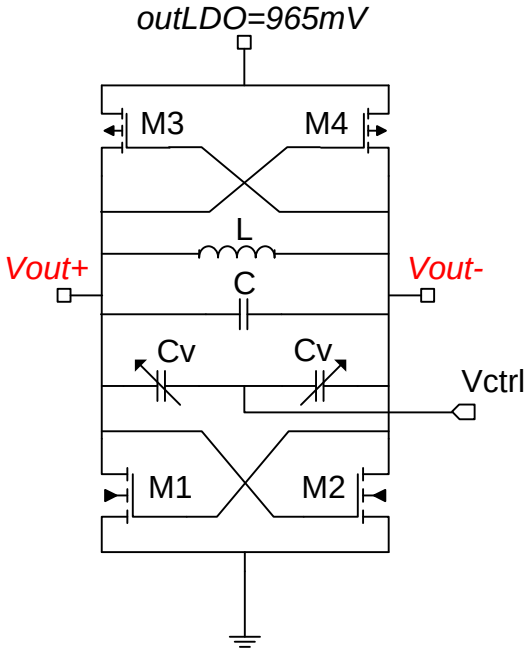


**Figure II-22: Schematic view of the VCO; its supply voltage is supplied by the LDO**

#### *II.4.2.4 Placement compared to the state-of-the-art*

The main goal of this work is not the design of a highly performing VCO, but to demonstrate the feasibility of a self-test for wafer sort, without degradation of the performance of the CUT.

Since no specifications were given, the decision was taken to design a VCO comparable (not necessarily better) with the state-of-the-art.

Follows a table listing recent works on LC-VCOs having oscillation frequency close to our needs.

| Work | Idd | Vdd | Techno | $f_0$ | PN@1MHz |
|---|---|---|---|---|---|
| [Nak06] | 4mA | 2.5V | 0.25µm Si-BiCMOS | 3.9GHz | -121 dBc/Hz |
| [Bro07] | 6mA | 1.8V | 130nm CMOS | 3.6GHz | -126.8 dBc/Hz |
| [Bui07] | 5.5mA | 1.8V | 0.18µm CMOS | 3.77GHz | -122.7 dBc/Hz |

**Table II-IV: Recent works on VCOs having a frequency of oscillation close to our target**

Being the supply voltage of our VCO (965mV) considerably lower than what used in the listed publications, the following specifications are fixed for the design:

- Idd < 6mA
- PN@1MHz ≈ -120dBc/Hz

The target for the phase noise is not as good as the phase noise presented in the publications listed in Table II-IV. Two reasons explain this choice:

1. The supply voltage available for our VCO is 965mV, which is half the supply voltage used in [Bro07] and [Bui07], and 2.6 times lower than the supply voltage in [Nak06], which makes use of bipolar transistors.
2. Our VCO is supplied by an LDO, and the LDO is driven by the voltage reference. Those two circuits generate noise, which will be up-converted close to the fundamental by the VCO, increasing its phase noise. The listed publications present stand-alone VCOs.

#### *II.4.2.5 Dimensioning of the active components and results of simulations*

Knowing that the VCO is supplied by 965mV, and that the current consumption should not exceed 6mA, the following values for the dimension of the pMOS and nMOS transistors are chosen:

| Dimension | nMOS | pMOS |
|---|---|---|
| **W [µm]** | 120 | 150 |
| **L [µm]** | 0.25 | 0.1 |

**Table II-V: Dimensions of the pMOS and nMOS transistors of the VCO**

It was decided not to use transistors with minimal length *L* in order to lower their *1/f* noise.
The pMOS transistors are known to have a lower 1/f noise compared to nMOS transistors [Klu00].
For this reason, in order to have nMOS and pMOS with approximately the same 1/f noise, the gate length of the nMOS is higher than that of pMOS transistors.

A pMOS buffer is used to drive the 50Ω-load of the instrumentation.

The results of the Post-Layout Simulations (case: typical) at the temperature of 45°C are presented in the following table.

| Vctrl | freq | power | PN@1MHz | Idd VCO | Vpp | FOM |
|---|---|---|---|---|---|---|
| 0 V | 3.617 GHz | 4.74 dBm | -118.8 dBc/Hz | 5.5 mA | 910 mV | -182.7 dB |
| 1 V | 3.376 GHz | 4.50 dBm | -119.7 dBc/Hz | 5.8 mA | 875 mV | -182.7 dB |

**Table II-VI: Results of the Post-Layout Simulations for the VCO**

The simulations take into account the parasitic capacitance, resistance and inductance of the micro-bonding needed to package the circuit.
The frequency range 3.4GHz-3.6GHz is covered with a variation of 1V on the control voltage $V_{ctrl}$ driving the varactors.

The spectrum of the single-ended output and the phase noise for an oscillation frequency of 3.38GHz are shown in Figure II-23 and Figure II-24, respectively. The characteristic slopes of -30dB/dec and -20dB/dec can be detected in the result of the phase noise simulation.

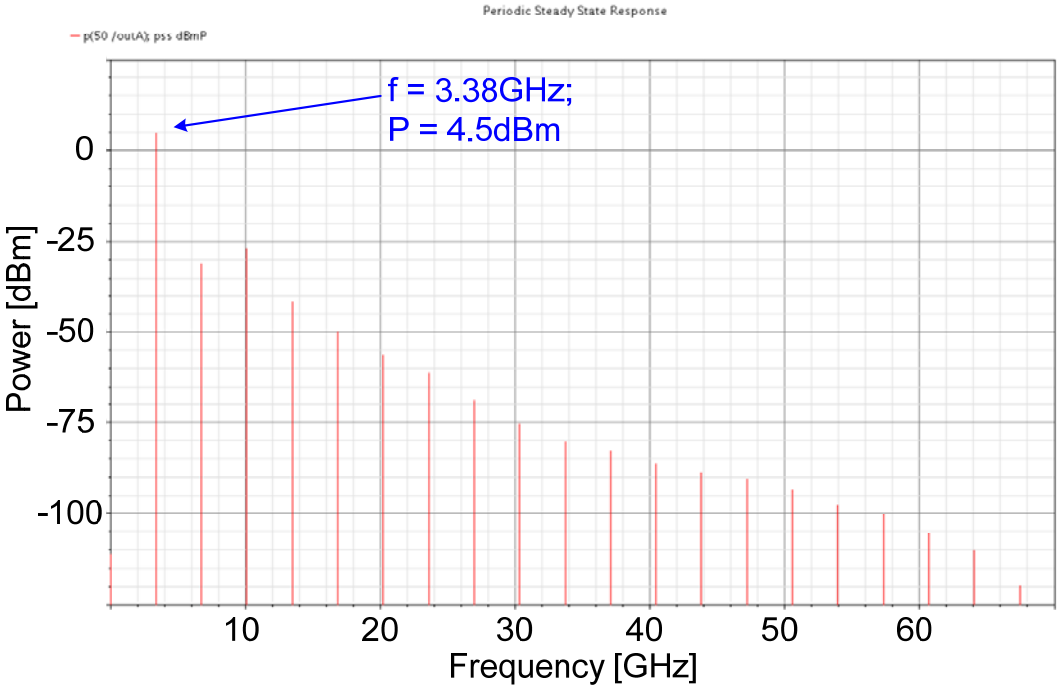


**Figure II-23: Spectrum of the single-ended output signal**

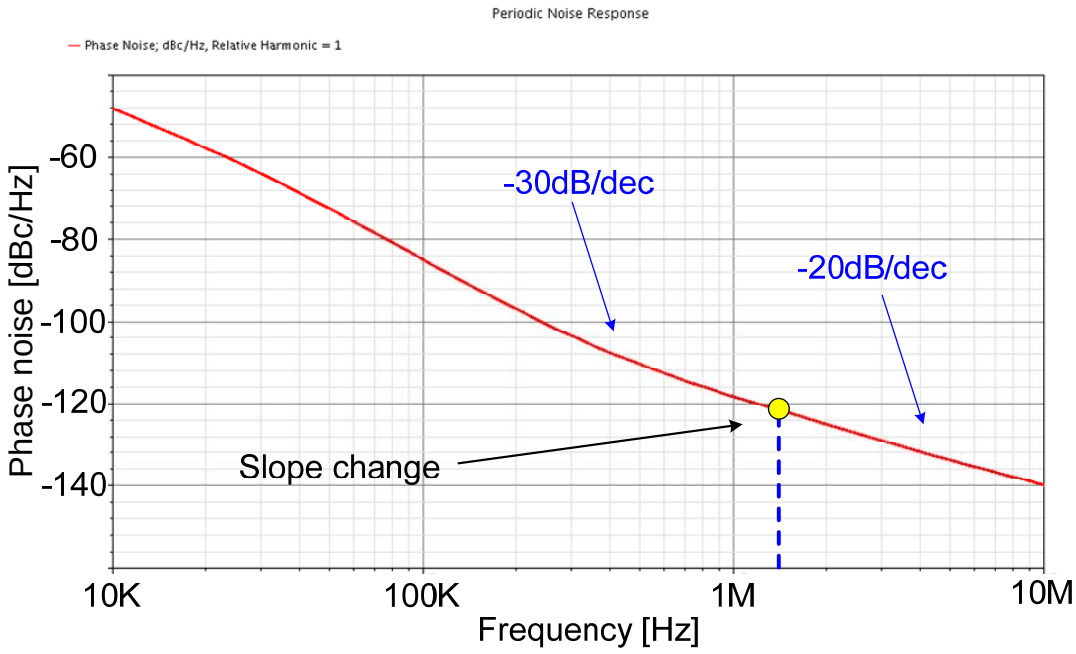


**Figure II-24: Phase noise of the VCO; the regions characterized by different slopes can be observed**

### *II.4.3 The BIST*

The main blocks needed for the BIST of the VCO are:

- The temperature and supply-voltage independent CMOS voltage reference
- The peak-to-peak voltage detector
- The comparators and the logic block to have a digital pass/fail information

Those blocks are now described in deep detail.

#### *II.4.3.1 Temperature and supply-voltage independent CMOS voltage reference*

A temperature and supply-voltage independent voltage reference is mandatory in two major parts of the system depicted in Figure II-12.

1. In order to have a LDO functioning for a large range of temperature. While the rejection of the supply noise can be guaranteed by a high open-loop gain of the OpAmps of the LDO, the output voltage of the LDO is dependent on the value of the output voltage of the voltage reference, as shown in equation 4. If this value changes with the temperature, then the output voltage of the LDO changes too.
2. In order to generate precise and stable high and low voltage limits, needed to settle the acceptance range for the structural test.

Those are the reasons why a great importance is attributed to this block.
The most common temperature-independent voltage reference is the bandgap reference. The principle of this circuit is to sum a quantity having positive temperature dependence with another having negative temperature dependence.
The quantities having this temperature behavior are:

- Base-emitter voltage of bipolar transistors (or more generally the forward voltage of a *pn*-junction diode): negative temperature coefficient
- Difference between base-emitter voltages of two transistors operating at unequal current densities: positive temperature coefficient

The most basic circuit allowing the sum of those voltages is depicted in Figure II-25. If $V_{out1}$ is forced to be equal to $V_{out2}$ via an OpAmp that can drive the current references, then [Raz01]:

$$\begin{aligned} RI &= V_{be1} - V_{be2} = V_T Ln(N) \\ V_{out2} &= V_T Ln(N) + V_{be2} \end{aligned} \quad (17)$$

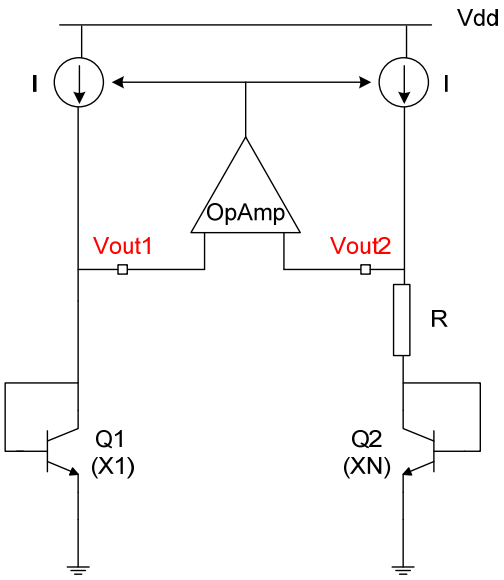


**Figure II-25: Basic bandgap-voltage-reference based on bipolar transistors**

In Equation 17, the term *N* is the ratio of the dimensions of Q2 and Q1.

Even if very efficient, this circuit cannot be designed in CMOS-only technology. Moreover, it is truly temperature independent in only a small temperature range.

It is then needed to find combination of electrical quantities of CMOS transistors exhibiting negative and positive dependence with temperature, in order to sum them.

Possible choices, together with their disadvantages, follow:

- Work function of pMOS and nMOS transistors [Wan02]

This solution requires knowing exactly the temperature behavior of the work function, controlled by the impurity concentration of gate electrodes. This data is hardly known by designers.

- Threshold voltage difference of pMOS and nMOS transistors [Leu01]

This circuit needs extra fabrication steps to implement multi-threshold voltage devices. Those steps are not always granted in every technology.

- Threshold voltage and thermal voltage [Mat05] [Ogu97]

The third solution seems to be the one that grants highest accuracy and portability towards other Si technologies.

The threshold voltage of MOS transistors has a negative temperature coefficient, while the thermal voltage has a positive temperature coefficient. The weighted sum of the two gives a temperature independent voltage in the form:

$$V_{out} = V_{TH} + \beta \cdot V_t \quad (18)$$

The term β is fixed by the relative temperature dependence of $V_{TH}$ and $V_t$.

Its value can be, for example, a function of the dimensions of the transistors in the circuit [Mat05]. The good dimensions need to be found in order for the output voltage to be temperature independent. This solution is not too attractive because it imposes constraints that are hard to respect, if the transistors have to work in a specific operation region (saturation, subthreshold…).

#### II.4.3.1.1 Temperature independence

The proposed solution to this problem is to make β a function of the ratio of the currents flowing into the circuit. This grants a higher portability of the circuit and removes the constraints on the dimensions of the transistors.

The voltage reference is depicted in Figure II-26.

The equations ruling its behavior follow.

Provided that M1 and M2 operate in the subthreshold region, M3 and M4 are in the linear region and M5 is in the saturation region (diode-connected):

$$I_1 = k_x \cdot S_1 \cdot exp\left[\left(V_{gs1} - V_{TH0}\right)/(nV_t)\right] \quad (19)$$

$$I_0 = k_x \cdot S_2 \cdot exp\left[\left(V_{gs2} - V_{TH0} - \Delta V_{TH0}\right)/(nV_t)\right] \quad (20)$$

$$I_2 = \frac{\mu_n C_{ox}}{2} \cdot S_4 \cdot \left[2(V_{out} - V_{TH0})V_{ds4} - V_{ds4}^2\right] \quad (21)$$

$$I_0 = \frac{\mu_n C_{ox}}{2} \cdot S_3 \cdot \left[2(V_{out} - V_{TH0})V_{ds3} - V_{ds3}^2\right] \quad (22)$$

$$I_2 = \frac{\mu_n C_{ox}}{2} \cdot S_5 \cdot \left(V_{gs5} - V_{TH0}\right)^2 \quad (23)$$

$C_{ox}$ is the gate capacitance per unit of area, $\mu_n$ is the electron mobility, $S_i=W_i/L_i$, $n$ is the fitting factor for MOSFET subthreshold swing, $k_x$ is a process parameter and $V_t$ the thermal voltage.

$V_{TH0}$ is the threshold voltage of a MOS transistor when source and bulk are short-circuited. In the case of a voltage difference between bulk and source (transistor M2), the model of the threshold is refined by adding the following corrective term to $V_{TH0}$:

$$\Delta V_{TH} = \gamma \cdot \left(\sqrt{2\Phi_F + V_{SB2}} - \sqrt{2\Phi_F}\right) \quad (24)$$

where γ is the body-effect parameter and $\Phi_F$ is the Fermi potential in the bulk.

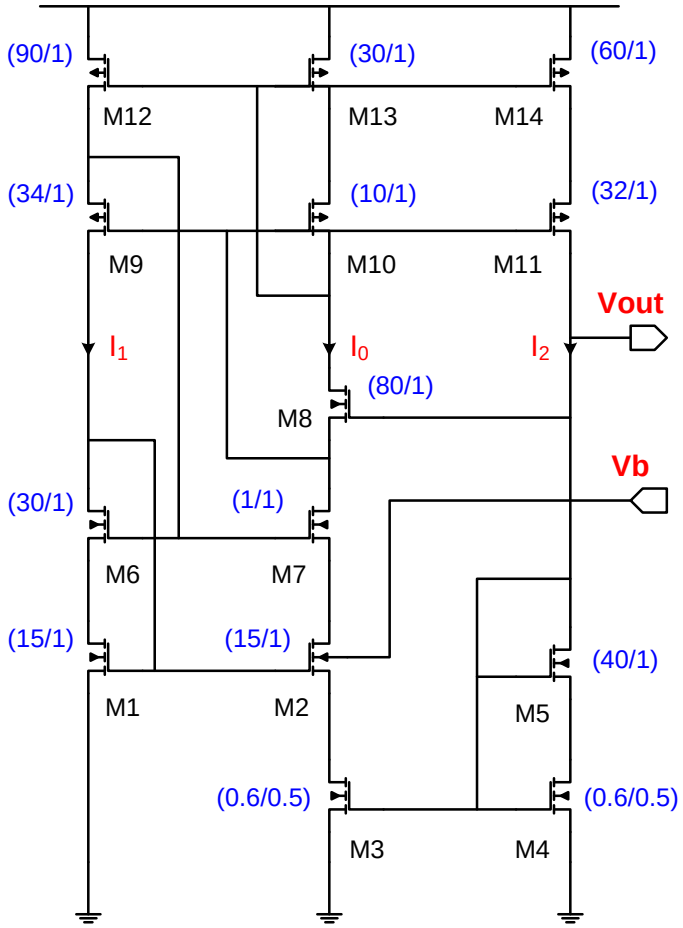


**Figure II-26: CMOS temperature and supply-voltage independent voltage reference; the bulk of M2 can be externally controlled to change the value of the output voltage**

Two voltage-loop equations have to be taken into account:

$$V_{gs1} = V_{gs2} + V_{ds3} \quad (25)$$

$$V_{sb2} = V_{ds3} - V_b \quad (26)$$

where $V_b$ is the voltage of the bulk of M2, which is externally controlled.

Transistors M9-M14 form a dual-output cascoded current mirror; its purpose is to fix the following temperature-independent current gains:

$$G_1 = \frac{I_1}{I_0} \quad (27)$$

$$G_2 = \frac{I_2}{I_0} \tag{28}$$

Studying Equations (21) and (23), and knowing that:

$$V_{out} - V_{ds4} = V_{gs5} \tag{29}$$

it is possible to write:

$$\frac{2}{\mu_n C_{ox}}\left(\frac{I_2}{S_4} + \frac{I_2}{S_5}\right) = (V_{out} - V_{TH0})^2 \tag{30}$$

This is equivalent to write:

$$I_2 = \frac{\mu_n C_{ox}}{2} \cdot S_{eq} \cdot (V_{out} - V_{TH0})^2 \tag{31}$$

where:

$$S_{eq} = \frac{1}{\frac{1}{S_4} + \frac{1}{S_5}} \tag{32}$$

Combining Equations (31), (22) and (28) it is possible to relate the output voltage to $V_{ds3}$:

$$V_{out} = V_{TH0} + C \cdot V_{ds3} \tag{33}$$

where the tuning parameter *C* is defined as:

$$C = \left(1 + \sqrt{1 - \frac{S_{eq}}{S_3} \cdot \frac{1}{G_2}}\right) \frac{S_3}{S_{eq}} \cdot G_2 \tag{34}$$

Equations (19), (20), (25) and (27) lead to the following expression for $V_{ds3}$:

$$V_{ds3} = A \cdot nV_t - \Delta V_{TH} \tag{35}$$

where the second tuning parameter *A* is defined as:

$$A = Ln\left(\frac{S_2}{S_1} \cdot G_1\right) \tag{36}$$

Substituting (26) into (24) and making the simplifying hypothesis:

$$|V_{ds3} - V_b| \ll 2\Phi_F \tag{37}$$

allows the determination of $V_{ds3}$:

$$V_{ds3} \approx \frac{A}{1+\alpha} nV_t + \frac{\alpha}{1+\alpha} V_b \tag{38}$$

where the parameter $\alpha$ has the following expression:

$$\alpha = \frac{\gamma}{\sqrt{2\Phi_F}} \tag{39}$$

Substituting (38) in (33) leads to the approximate expression for the output voltage:

$$V_{out} = V_{TH0} + \frac{A \cdot C}{1+\alpha} nV_t + \frac{\alpha}{1+\alpha} CV_b \tag{40}$$

It can be inferred from equation (40) that the output voltage is a function of the threshold voltage of MOSFET transistors and of the thermal voltage.

The voltage of the bulk of M2 appears also in the expression of the output voltage; this externally-controlled voltage allows having a controllable temperature-independent output voltage.

It is now possible to derivate the expression of the output voltage over the temperature. In order to simplify the analysis, only $V_{TH0}$ and $V_t$ are assumed to be temperature dependent.

$$\frac{\partial V_{out}}{\partial T} = \frac{\partial V_{TH0}}{\partial T} + \frac{A \cdot C}{1+\alpha}\frac{nk}{q} \tag{41}$$

where *k* is the Boltzmann constant and *q* is the charge of the electron.

Imposing the constraint of a temperature-independent output voltage (imposing its derivative over temperature equal to zero), the following condition is found:

$$A \cdot C = -\frac{\partial V_{TH0}}{\partial T}(1+\alpha)\frac{q}{nk} \tag{42}$$

The threshold voltage $V_{TH0}$ and the temperature T are related by the following decreasing affine law [Tsi87] [Uen07]:

$$\frac{\partial V_{TH0}}{\partial T} = \frac{V_{TH0} - [V_{TH0}]_{T=0K}}{T} \tag{43}$$

Combining equations (40), (42) and (43) allows the determination of the output voltage at thermal equilibrium:

$$[V_{out}]_{thermal\ eq} = [V_{TH0}]_{T=0K} + \frac{\alpha}{1+\alpha} C \cdot V_b \tag{44}$$

The feasibility to design an *adjustable* temperature-independent CMOS voltage reference is proven thanks to equation (44).

In the theory so far developed, the assumption was made that all transistors have the same threshold voltage; in reality, $V_{TH0}$ is also geometry and process dependent.

To come closer to our behavioral description, some constraints are imposed to the dimensions of the transistors: M1=M2 and M3=M4=M5.

In the light of this new constraint, parameters *A* and *C* simplify as follows:

$$A = Ln(G_1) \tag{45}$$

$$C = \left(1 + \sqrt{1 - \frac{1}{G_2}}\right) \cdot G_2 \tag{46}$$

The values of $G_1$ and $G_2$ used to obtain a temperature-independent output are:

- $G_1 = 3$
- $G_2 = 2$

The designer could proceed as follows:

1. Find a first set of values for the current gains $G_1$ and $G_2$ in order to reach the thermal equilibrium (this is easily done playing on the dimensions of the pMOS transistors composing the current mirror).
2. Vary the parameter $C$ (changing $G_2$) in order to find the needed value of output voltage (Equation 44).
3. Calibrate parameter $A$ (changing $G_1$) to reach the thermal equilibrium again (Equation 42).

The design of the circuit is now complete. The dimensions of each transistor are established and cannot be changed anymore.

At this point the importance of $V_b$ comes into play.
The designer has a new degree of freedom that can be used to dynamically change the value of the temperature independent output voltage.
From Equation 42 it can be inferred that the value of $V_b$ does not change the condition for thermal equilibrium (at the first order).

In order to precisely control the biasing of the bulk of M2, this transistor is designed making use of a triple-well process, available in the STMicroelectronics 65nm CMOS process.

The results of a simulation where the temperature is swept from -35°C to +125°C are shown in Figure II-27 for different values of $V_b$.
As stated in Equation (44), the output voltage changes in response to a change in $V_b$. Increasing $V_b$ slightly changes the values of $G_1$ and $G_2$; this causes the output voltage to become a little more temperature dependent, as observed in the curves for $V_b$=30mV, 40mV, 50mV represented in Figure II-27. Even in the worst case ($V_b$=50mV), the output voltage experiences a change lower than 20mV in a 160°C range, which may be acceptable for some applications.
Another interesting thing to notice is the linear change of the output voltage when different $V_b$ values are applied. For a $\Delta V_b$ of 10mV, the output changes by 14mV.

The following table summarizes the characteristics of the voltage reference, for the temperature range [-35°; +125°].

| Vb [mV] | Vout @ T=27°C [mV] | ΔVout max[mV] | ppm |
|---|---|---|---|
| 0 | 664 | 2.9 | 18 |
| 10 | 678 | 5.0 | 31 |
| 20 | 692 | 8.2 | 51 |
| 30 | 706 | 11.6 | 73 |
| 40 | 719 | 15.4 | 96 |
| 50 | 733 | 19.2 | 120 |

**Table II-VII: Characteristics of the voltage reference in the temperature range [-35°; +125°] for different values of Vb.**

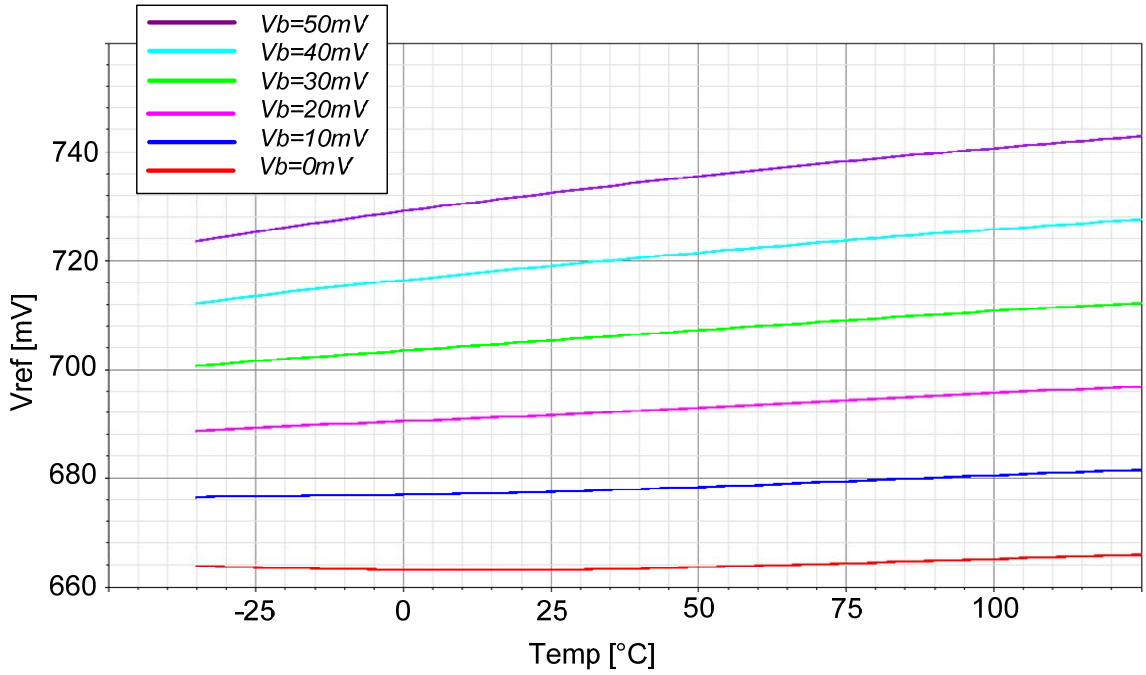


**Figure II-27: Output voltage of the voltage reference as a function of the temperature**

#### II.4.3.1.2 Supply-voltage independence

Two design strategies allow the output voltage to be supply-voltage independent:

- Both pMOS and nMOS current mirrors are designed using a bootstrap cascode structure
- A self-biasing technique for the two current mirrors has been adopted

The behavior of the output voltage as a function of the supply voltage is shown in Figure II-28, for different values of $V_b$. It can be noticed that, starting from approximately Vdd = 1.0V, changes in the supply voltage do not affect the value of the output voltage.

The PSRR of the voltage reference at 100Hz is -43dB.

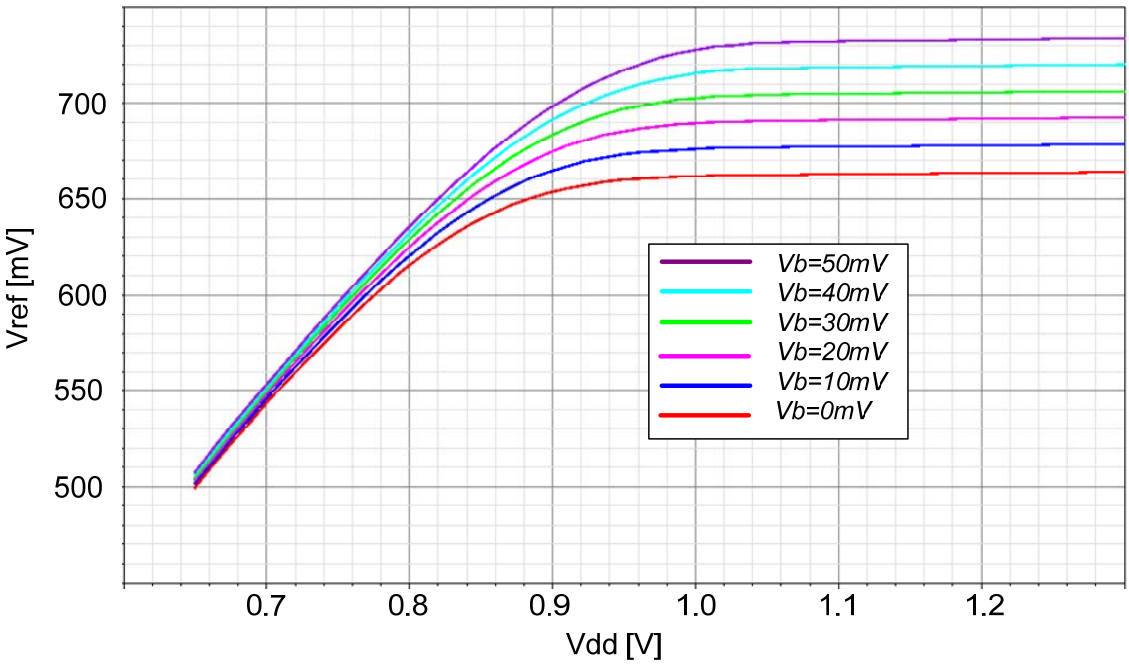


**Figure II-28: Output voltage of the voltage reference as a function of the supply voltage**

#### *II.4.3.2 Peak-to-peak voltage detector*

Earlier during this chapter the need to monitor the peak-to-peak value of the output voltage of the VCO was explained. A detector able to sense this information has to be designed.

The principle of operation of the implemented detector is the voltage follower.

If a signal is sent on the gate of a transistor, the voltage on its source follows the input. The output is then a copy of the input, as depicted in Figure II-29a for an nMOS transistor. The only difference between input and output signals is the DC-voltage value. For an nMOS voltage follower, the DC voltage drop is equivalent to a positive $V_{GS}$.

It can be shown that the expression of the voltage gain for the voltage follower is [Gra01]:

$$A_v = \frac{g_m r_0}{1 + (g_m + g_{mb}) r_0 + r_0 / R_L} \quad (47)$$

where $g_m$ represents the transconductance of the transistor, $g_{mb}$ is the body-effect transconductance, $r_0$ is the output resistance of the MOSFET and $R_L$ is the charge connected to the source, represented by the current source $I_{bias}$ in Figure II-29a.

Considering $R_L \to \infty$, it can be inferred from equation 47 that the voltage gain is almost unity.

If a capacitor is placed between the output node and ground, as shown in Figure II-29b, the behavior of the output voltage slightly changes.

When the input voltage increases, the output follows the input and charges the capacitor. When the input reaches its positive peak value *Vp*, the output reaches the value $Vp\text{-}V_{GS}$. When the input starts decreasing, the output does not change because the capacitor is charged.

The output voltage is then a clear image of the positive peak value of the input sinusoidal signal.

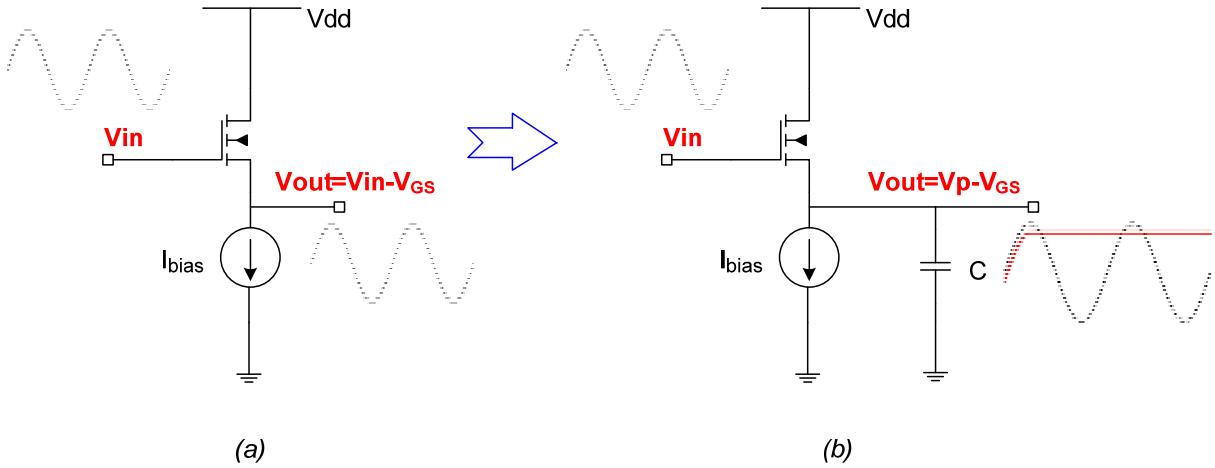


**Figure II-29: nMOS voltage follower configuration and its use as a peak detector**

If the same principle is applied for a pMOS transistor, the negative peak voltage ($+V_{GS}$) is detected.

The information on positive and negative peak values can now be combined to have an on-chip measure of the peak-to-peak voltage value.

The complete detector is shown in Figure II-30.

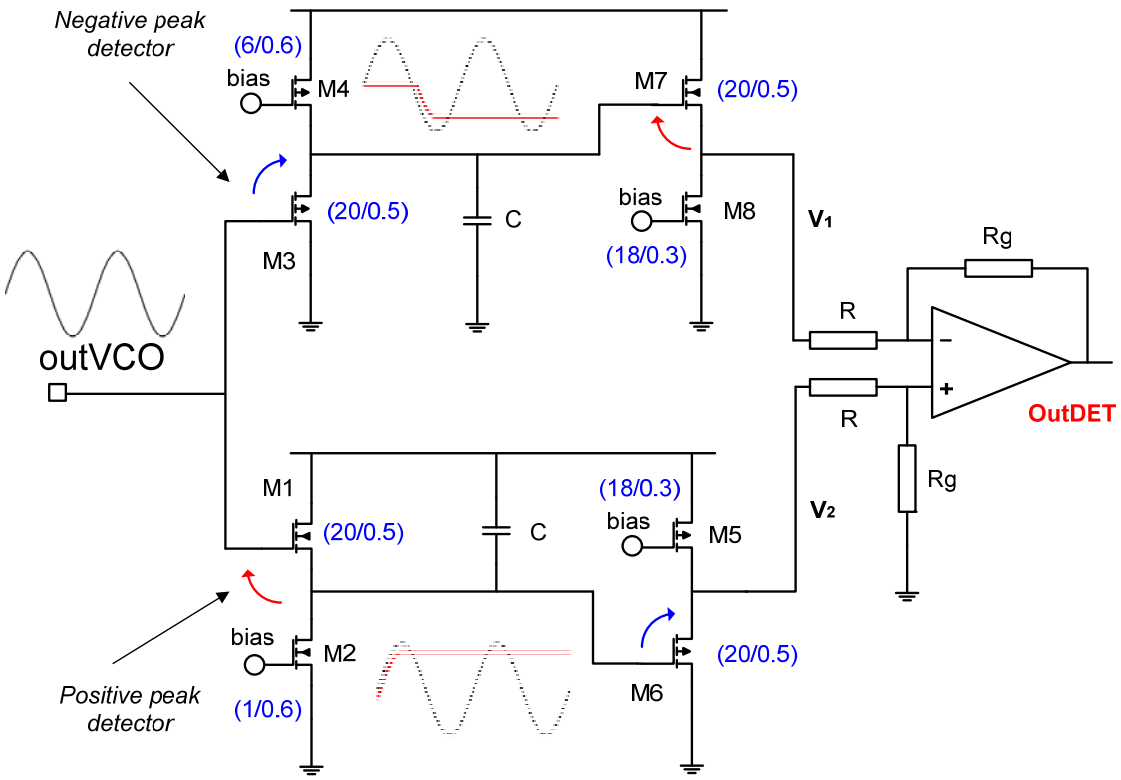


**Figure II-30: Peak-to-peak voltage detector**

Transistor M1 is the nMOS voltage follower used for positive peak detection; M3 is the pMOS voltage follower needed for negative peak detection. Transistors M2 and M4 act as current sources that bias the voltage followers, as $I_{bias}$ depicted in Figure II-29.

As explained, a $V_{GS}$ voltage from input to output is *lost* in M1 and *gained* in M3. This fact can create disequilibrium of the structure, harmful to the OpAmp that will subtract the two voltages created from the voltage followers.

This is why a second stage is introduced.

Transistor M7 allows to lose the $V_{GS}$ gained in M3; transistor M6 allows to gain the $V_{GS}$ lost in M1. Transistors M5 and M8 are used as current sources.

The two outputs $V_1$ and $V_2$ are now an image of the negative and positive peak values, respectively.

In Figure II-31 voltages $V_1$ and $V_2$ are shown in a transient simulation where the amplitude of the input signal is swept from 250mV to 550mV. Both the changes in positive and negative peaks are detected.

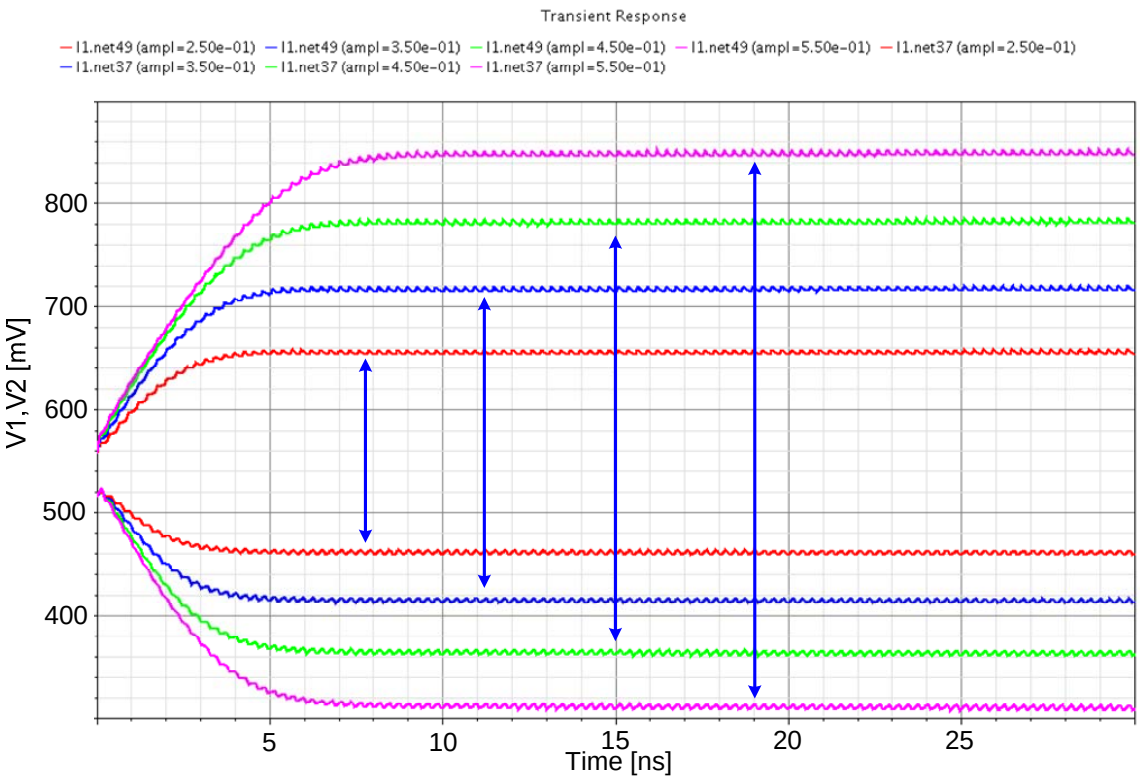


**Figure II-31: Transient simulation showing $V_1$ and $V_2$ for different values of input amplitudes**

It is now needed to subtract $V_1$ from $V_2$ in order to output a single voltage, image of the peak-to-peak value of the output voltage of the VCO.

In order to do so, a differential OpAmp is designed.

Referring to the schematic in Figure II-30, the output voltage of the detector is now:

$$outDet = \frac{R_g}{R} \cdot (V_2 - V_1) \approx \frac{R_g}{R} \cdot V_{pp} \qquad (48)$$

The output is dependent on the ratio of two resistors. In terms of process deviations and mismatch, this solution is more robust than the case in which the output is dependent on the value of a single resistor.

A Monte Carlo simulation with global process variations and mismatch is run on the detector.

1000 iterations give the result presented in Figure II-32.

The output voltage shows a 9mV standard deviation, which is considered acceptable for the application.

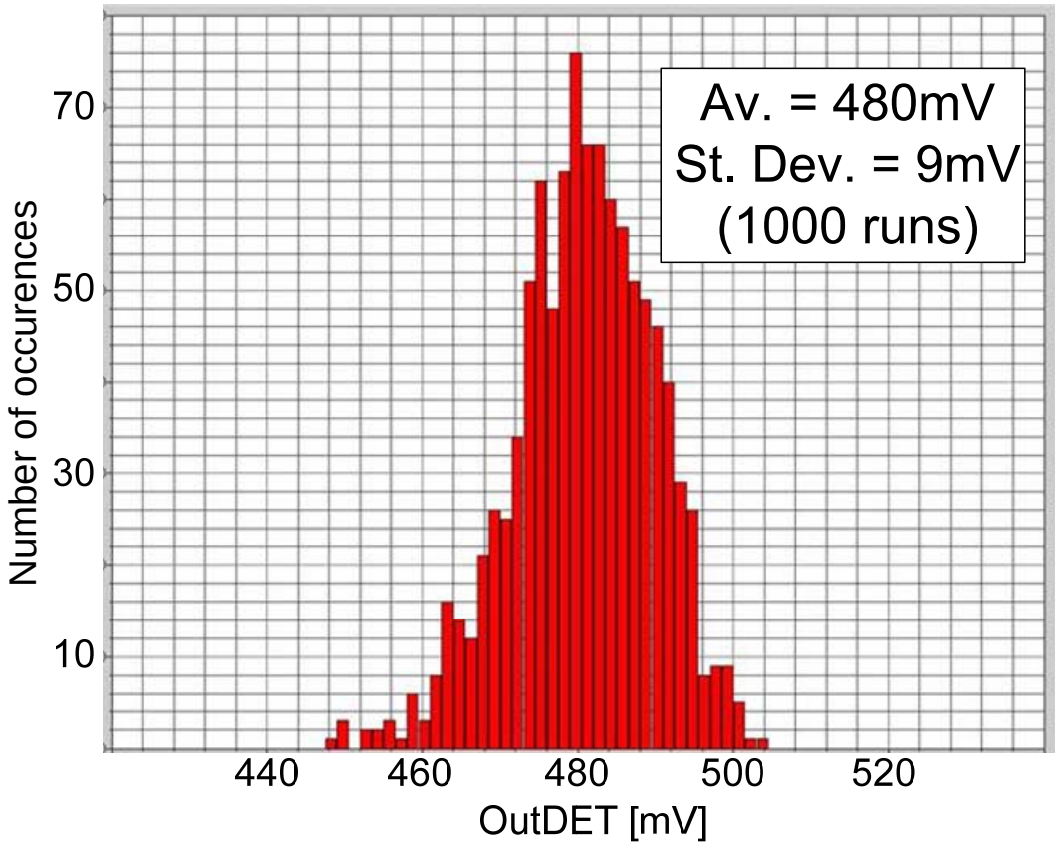


**Figure II-32: Monte Carlo simulations with process variations and mismatch on the proposed Vpp detector.**

The linearity of the proposed detector is shown in Figure II-33

The peak-to-peak value of the input voltage is swept from 500mV to 1.1V; the detector is powered with a 1.2V supply voltage. The simulation is run for three different temperatures: -40°C, +27°C, and +125°C.

The behavior of the detector is extremely linear in the whole input range.

While the slope of the input/output characteristic slightly changes in the temperature range, for each temperature the linearity is still guaranteed.

The behavior of the detector powered with a 1.0V supply voltage is the investigated.

In Figure II-34 the linearity of the detector is shown for the temperatures -40°C, +27°C, and +125°C when the supply voltage is lowered to the value of 1.0V.

It can be noticed that, for the temperature T=-40°C, the detector starts to lose its linearity for high input amplitudes.

The detector, without the OpAmp, consumes 350µA when the average value of the output voltage of the VCO is approximately 450mV.

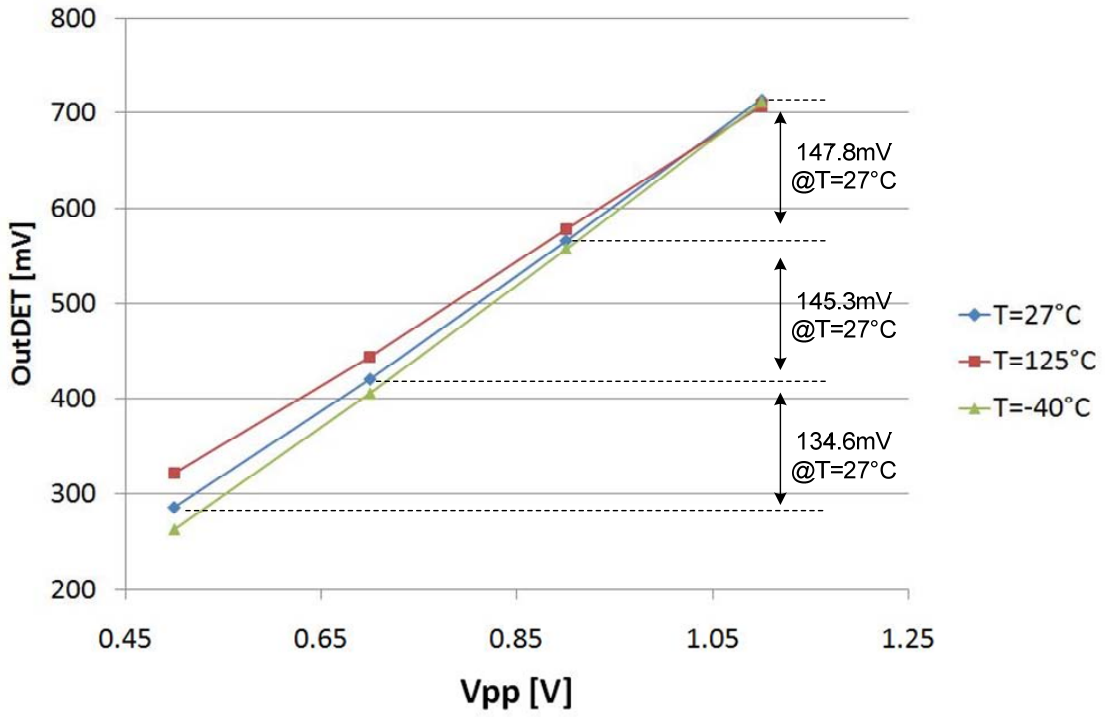


**Figure II-33: Linearity of the proposed Vpp-detector for three different temperatures (T=-40°, 27°, 125°) powered with a 1.2V supply-voltage.**

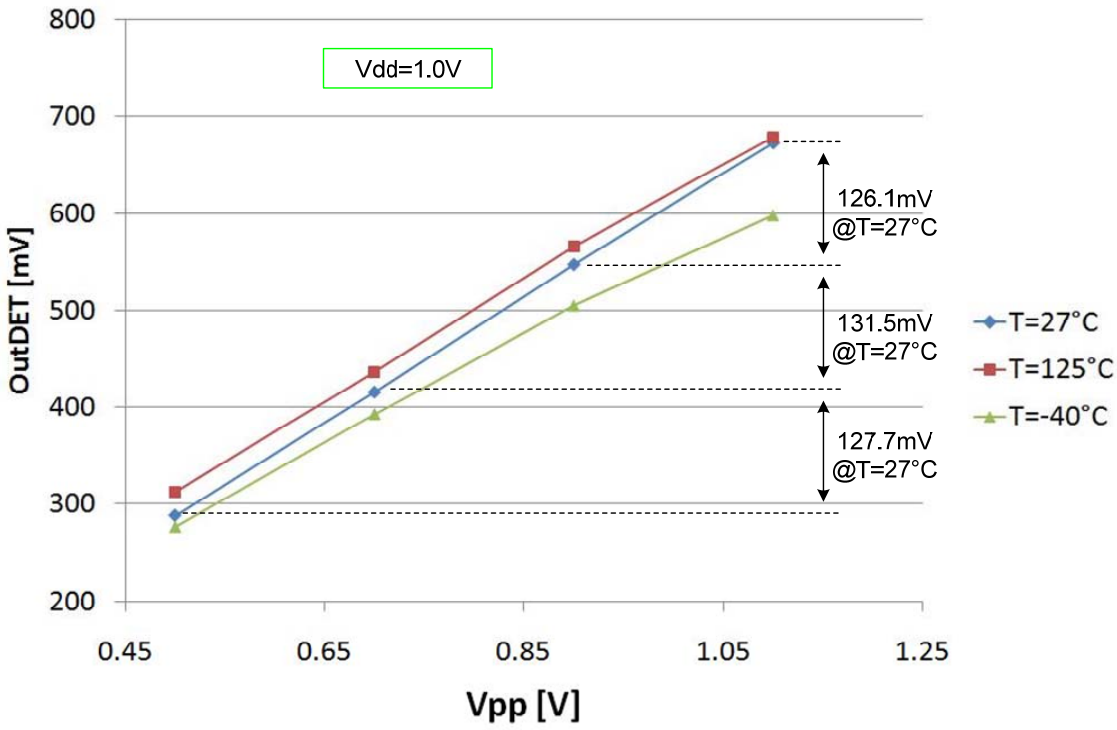


**Figure II-34: Linearity of the proposed Vpp-detector for three different temperatures (T=-40°, 27°, 125°) powered with a 1.0V supply-voltage.**

*II.4.3.3 Level generators and comparator*

The last two blocks that are needed for the BIST of the VCO are the voltage level generator and the comparator.

The level generator, starting from the output voltage of the temperature and supply-voltage independent voltage reference, creates two voltages, $V_H$ and $V_L$, which represent the acceptance range allowed for the peak-to-peak value of the output voltage of the VCO.

The generation of $V_H$ and $V_L$ is done via an OpAmp in a voltage follower configuration and a bank of resistors in series, as shown in Figure II-35a.

Each resistor is composed of many resistors in parallel, in order to minimize problems arising from process variations and mismatch.

One main advantage of this structure is that, if many more resistors are connected in series, many more voltage references can be created, as depicted in Figure II-35b.

The comparator then decides if the output of the on-chip detector is within the limits of acceptance $V_H$ and $V_L$. In this case, the VCO presents no fault and the BIST outputs the logic 0. The VCO passes the wafer sort.

The block scheme of the comparator is presented in Figure II-35.

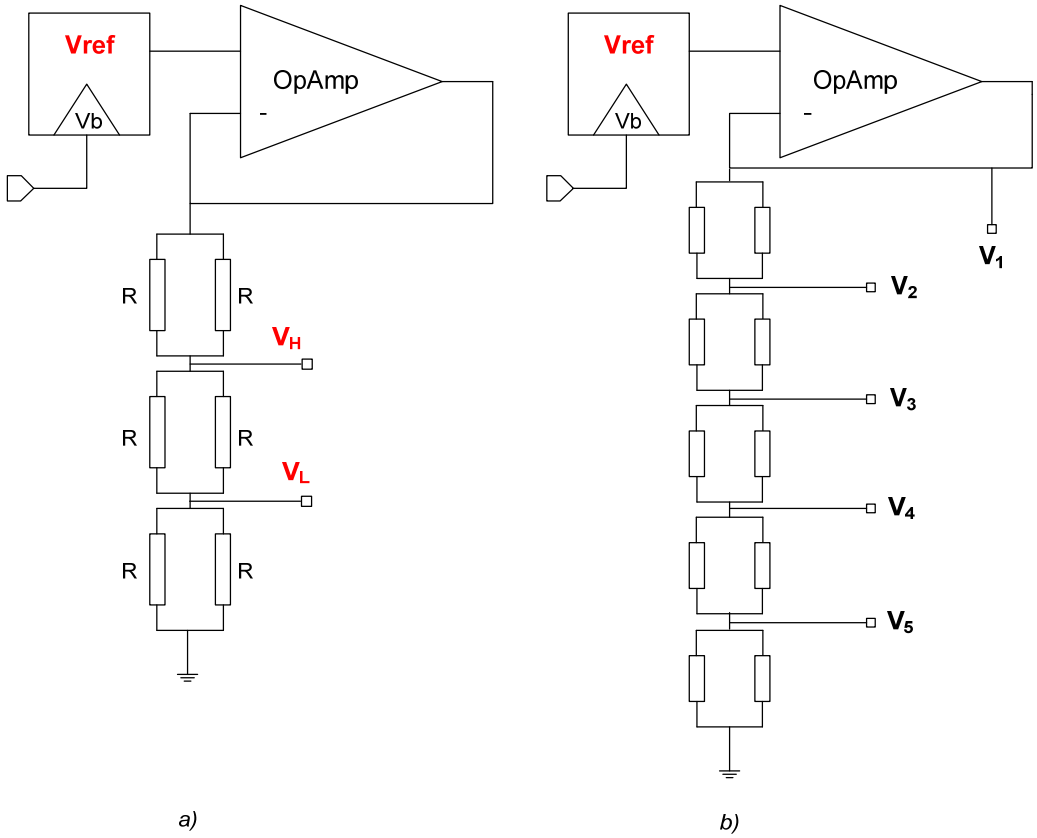


**Figure II-35: Circuit that generates $V_H$ and $V_L$ starting from the supply-voltage and temperature independent voltage reference. On the right side the possibility to have many more voltage references is shown.**

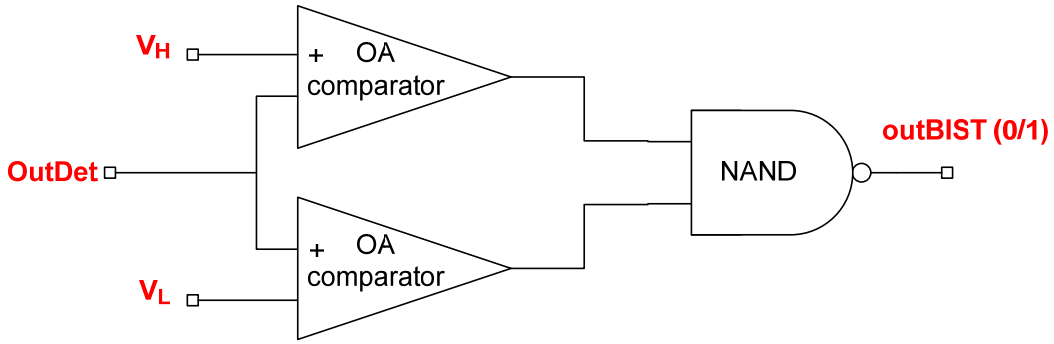


**Figure II-36: Comparator that decides if the output of the Vpp-detector is within the limits of acceptance**

*II.4.3.4 Simulation of the entire architecture*

The validation of the BIST architecture is done via a transient simulation. A fault is periodically injected and erased from the VCO and the behavior of the BIST is studied.

The results are shown in Figure II-37.

In the upper side of the figure, the output voltage of the detector (in blue) and the acceptance range (in green) are shown. In the lower side of the figure, the logic output of the BIST is presented.

The VCO starts oscillating. The detector detects the oscillation and outputs the value of Vpp. Without any fault, the output of the detector is within the limits of acceptance and the BIST outputs the logic 0. The CUT passes the wafer sort test.

At t=130ns a fault is injected in the VCO. This fault affects the value of the peak-to-peak output voltage of the CUT and the detector detects this change. The output of the detector falls out of the acceptance range and the logic 1 is immediately output by the BIST. The CUT does not pass the wafer sort test.

At t=280ns the fault is erased. The VCO finds back its proper functioning and its peak-to-peak output voltage settles to its good value. The detector now measures a Vpp-value that is again inside the acceptance range. The BIST outputs the logic 1 again.

This validates the architecture of the BIST and the proper functioning of each block also.

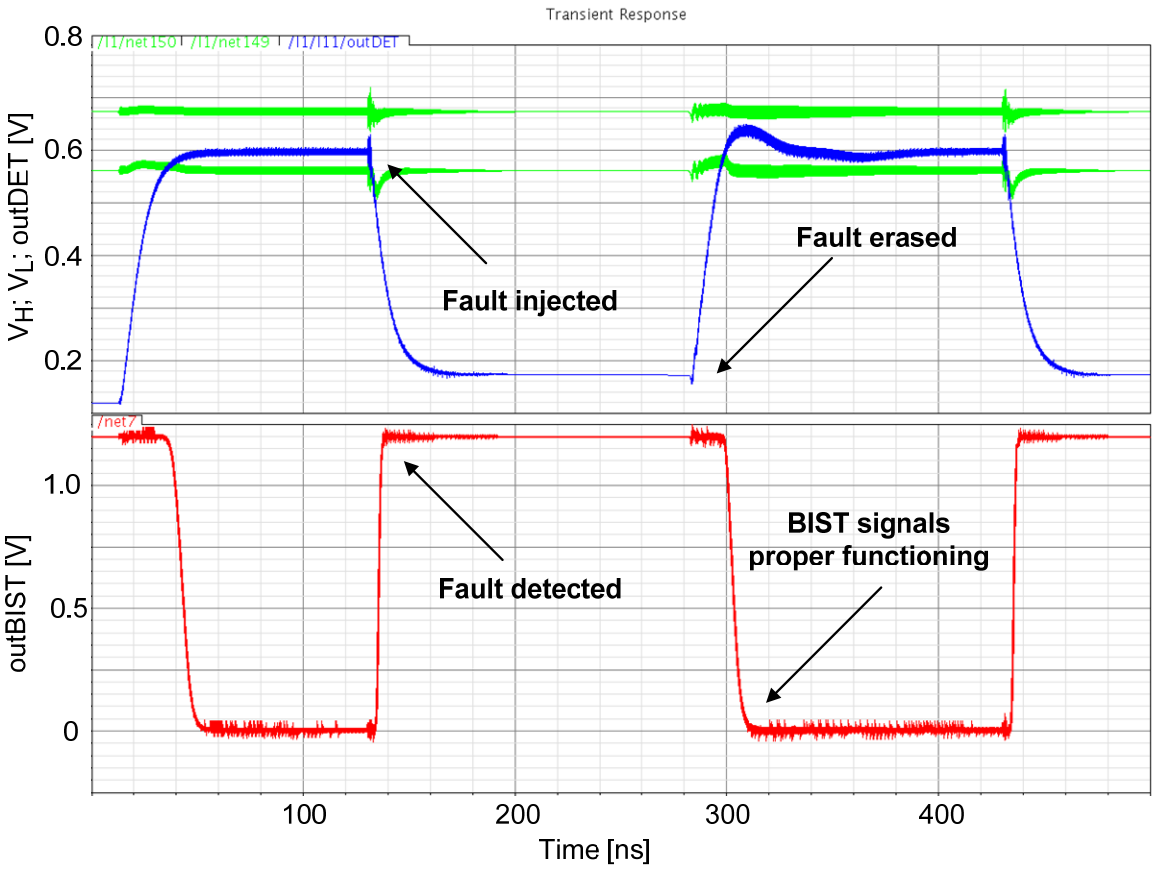


**Figure II-37: Transient simulation that validates the behavior of the BIST; a fault is injected at t=130ns and it is erased at t=280ns. The BIST architecture instantaneously responds with the logic 1 as soon as the fault is injected and returns to the logic 0 when the fault is erased.**

### *II.5 Transparency of the BIST*

The transparency of the BIST can be validated comparing the performance of the VCO with the BIST scheme connected to its outputs and the performance of the stand-alone VCO.

The following table reports the results (case: typical).

| Vctrl | freq | power | PN@1MHz | Idd | Vpp | FOM |
|---|---|---|---|---|---|---|
| **STAND-ALONE VCO** | | | | | | |
| 0 V | 3.638 GHz | 4.77 dBm | -118.9 dBc/Hz | 5.4 mA | 916 mV | -183.0 dB |
| 1 V | 3.394 GHz | 4.53 dBm | -119.9 dBc/Hz | 5.8 mA | 883 mV | -183.0 dB |
| **VCO + BIST** | | | | | | |
| 0 V | 3.617 GHz | 4.74 dBm | -118.8 dBc/Hz | 5.5+0.3 mA | 910 mV | -182.7 dB |
| 1 V | 3.376 GHz | 4.50 dBm | -119.7 dBc/Hz | 5.8+0.3 mA | 875 mV | -182.7 dB |

**Table II-VIII: Comparison of the characteristics of the stand-alone VCO and the same VCO with BIST**

It can be noticed that the major impact is the oscillation frequency that decreases by approximately 20MHz when the detector is connected. This is due to the input capacitance of the detector, which increases the capacitance presented at the resonator.

The two following equations show the impact of the connection of the detector.

$C_F$ is the fix capacitance of the tank, $C_{var}$ is the capacitance of the varactors, and $C_{par}$ is the parasitic capacitance due to the transistors in the VCO and to the layout interconnections. The frequency of oscillation of the stand-alone VCO is expressed by $f_1$.

When the BIST is connected, a new capacitance, $C_{bist}$, comes into play. As shown in the following equation, this capacitance lowers the frequency of oscillation of the VCO that is now described by $f_2$.

For an inductor of 0.95nH and with the sum of fix, variable and parasitic capacitance of approximately 2pF, a $C_{bist}$ of 25fF is enough to have a frequency shift of more than 20MHz.

$$f_1 = \frac{1}{\sqrt{L\left(C_F + C_{var} + C_{par}\right)}} \tag{49}$$

$$f_2 = \frac{1}{\sqrt{L\left(C_f + C_{var} + C_{par} + C_{bist}\right)}} \tag{50}$$

The amplitude of the output signal decreases by only a few mV.

The phase noise slightly increases by 0.2 dB, probably because of the small amplitude decrease.

It is possible to conclude that the BIST is almost completely transparent.

The other indicator of the quality of the BIST is its Si-surface compared to that of the CUT.

Here are the surfaces of VCO and BIST (detector + comparator):

- VCO = 0.032mm$^2$
- BIST=0.0058mm$^2$

The surface of the BIST is considerably lower than that of the VCO.

### *II.6 Corrective feedback*

The power consumption of the BIST can be eliminated if, after the wafer sort, the supply voltage is disconnected from the BIST.

However, the extra Si-surface would be wasted if, after the wafer test, the BIST architecture were switched off.

It is then decided to estimate the possibility to use the BIST even after the wafer sort, implementing an on-line testing that needs to continuously check the proper functioning of the CUT.

If a fault is found, the logic '1' output by the BIST needs to trigger a feedback able to correct - if possible – the VCO.

Recalling from Figure II-22, the VCO has no current source that can be driven by the feedback signal. The only degree of freedom comes from the LDO, and more specifically from the voltage reference used in the LDO, as shown in Figure II-38b.

The classical VCO design, shown in Figure II-38a, uses transistor $M_{cs}$ as a current source; if a feedback is implemented, the feedback signal is sent to the gate of this transistor, in order to change the current flowing in the VCO.

The output of the proposed voltage reference has the property to be controllable through the value of the bulk ($V_b$) of one of the transistors (transistor M2 in Figure II-26) composing its core.

This degree of freedom can play the same role as $M_{cs}$.

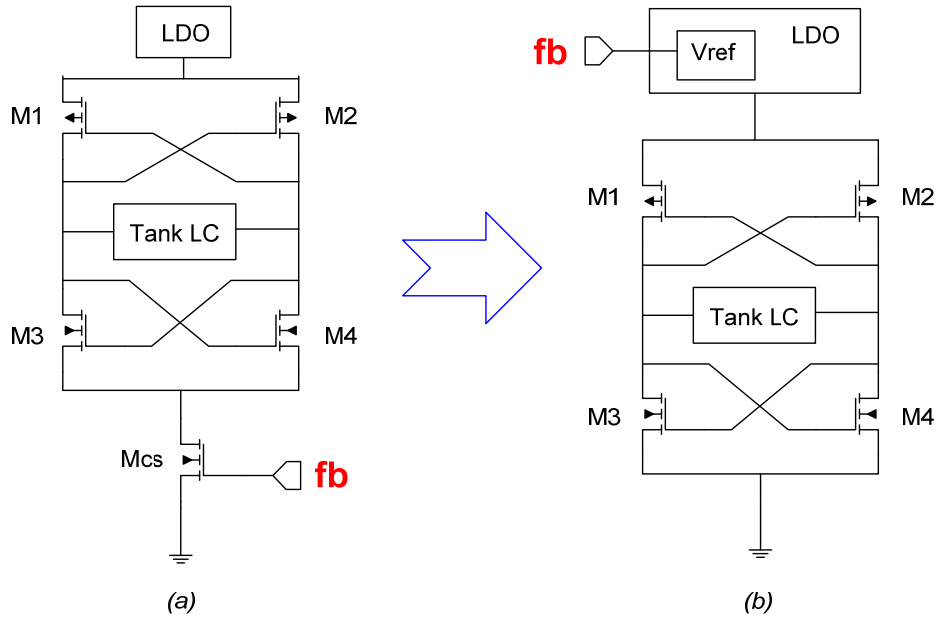


**Figure II-38: Classical feedback implementation (left) and proposed implementation (right)**

If $V_b$ is increased, the output of the voltage reference increases also.

This in turns causes an increase in the output voltage of the LDO (recall Equation 4).

Being the output voltage of the LDO the supply voltage of the VCO, the final consequence is an increase in the current flowing through the VCO.

### *II.6.1 Advantages and drawbacks of the proposed architecture for the feedback*

There are two main advantages in the proposed architecture for the feedback control on the VCO.
The first comes from the trend in industry to keep lowering the supply voltage of the systems; the second comes from the non trivial problem of having a low-noise feedback.

In any commercial system, the VCO is always supplied by an LDO. The lowering of the supply voltage will eventually make it impossible to allocate a voltage drop for the LDO, another for the VCO and a third voltage drop for $M_{cs}$ (Figure II-38a).
This problem is efficiently solved by the proposed feedback architecture (Figure II-38b), which saves one voltage drop.

The other big problem that needs to be faced when a feedback control is introduced on a VCO is the fact that the output noise of the detector (the first stage of every feedback control) increases the phase noise of the VCO.
Much effort is then spent by the designer to lower the noise of the detector.
In the proposed architecture, the detector does not drive directly the VCO, but the voltage reference instead. The low-pass behavior of the LDO can filter the noise of the detector, lowering its impact on the phase noise of the VCO.

The main drawback of this architecture resides in its lower response time.
Instead of acting directly on the current of the VCO, it is needed to pass through the voltage reference and the LDO, before being able to change the current of the CUT.

### *II.6.2 Proposed scenarios*

The feedback can correct the behavior of the CUT only in the case of “soft” faults. An open circuit cannot be fixed by the feedback.
Malfunctioning of the VCO caused by aging or hostile environment can be addressed by the feedback control.
Three scenarios are then emulated: temperature increase, space applications, deterioration of the passive elements in the tank.

To validate the principle of the feedback, after degradation of the circuit, $V_b$ is externally increased, without any feedback. This study is needed to validate the efficacy of $V_b$ as the means of current control.

#### *II.6.2.1 Temperature increase*

One of the most important stresses induced to a circuit comes from a rise of the temperature. Even when characterizing the reliability of a system, one of the most common ways to accelerate aging is to raise the temperature of the environment surrounding the CUT.

Many physical quantities that come into play in the description of the current flowing through a transistor are temperature dependent: the mobility of the carriers, the thermal voltage and the threshold voltage are only some of them.

The temperature of simulation is then raised to +150°C.

A first simulation is carried out keeping $V_b$ connected to the ground. Looking at Table II-IX, it is possible to understand that the main impacts are on Vpp (-104mV) and on the phase noise (+3.9dB).

Being the value of the peak-to-peak output voltage affected, the BIST is able to detect this malfunctioning.

The value of $V_b$ is then increased; it can be observed that both Vpp and the phase noise come closer to their nominal values, listed under the column “nominal” of Table II-IX.

| | **Vb = 0 mV** | **Vb = 30 mV** | **nominal** |
|---|---|---|---|
| Vpp [mV] | 774 | 863 | 878 |
| Freq [GHz] | 3.38 | 3.38 | 3.38 |
| PN [dBc/Hz] | -115.8 | -118.2 | -119.7 |
| OutLDO [mV] | 0.97 | 1.0 | 0.965 |
| Idd [mA] | 6.4 | 7.5 | 5.8 |

**Table II-IX: Data for increased temperature. The first column presents the performance of the VCO if $V_b$ is not controlled; the second column shows the improvement obtainable with a raise in $V_b$**

If a way to control $V_b$ is then implemented, the performance degradation caused by a sudden increase in the temperature can be recovered.

#### *II.6.2.2 Space applications*

One of the most hostile working environments for any IC is the space. RF systems for space applications that are designed using deep submicron technologies suffer from two effects: hot carriers and ionizing radiations. Both of them cause an increase in the threshold voltage of the transistors.

Hot carriers are high-energy electrons and holes in the pinched-off region of the channel near the drain that gain sufficient energy to enter the silicon-dioxide conduction band, where they may be trapped [Pul89]. The main consequence is a shift of the threshold voltage.

The radiations generally encountered in space are α-, β-, γ- and x-rays. The interaction between those high-energy incident ionizing radiations and MOSFETs has for major effect the generation of electron-hole pairs in the oxide layer. For high radiation doses, the threshold voltage of the MOSFET increases [Das03].

It is then decided to mimic the space environment increasing (by 100mV) the threshold voltage of the pMOS and nMOS transistors composing the VCO.

A first simulation is then run in those new conditions; the results are shown in Table II-X.

| | **Vb = 0 mV** | **Vb = 60 mV** | **nominal** |
|---|---|---|---|
| Vpp [V] | Oscillation never properly started! | 1.0 | 0.878 |
| Freq [GHz] | | 3.65 | 3.38 |
| PN [dBc/Hz] | | -112.4 | -119.7 |
| OutLDO [mV] | | 1.1 | 0.965 |
| Idd [mA] | | 5.8 | 5.8 |

**Table II-X: Data after threshold increase. The second column shows that a $V_b$-increase helps partially recovering the functioning of the VCO**

The degraded VCO is not able to start the oscillation.

The non-oscillation is easily detected by the peak-to-peak voltage detector, whose output could be used to trigger the feedback.

The control voltage $V_b$ is then externally increased to the value of 60mV.

The VCO is now able to oscillate; the performances of the CUT are not completely recovered (the phase noise is 7.3dB higher than in the nominal case), but the main function of the VCO is assured.

Once again, if a way to control $V_b$ is then implemented, the performance degradation caused by a harsh environment as space can be recovered.

#### *II.6.2.3 Deterioration of the inductance of the resonator*

The quality factor *Q* of the LC tank plays a major role in the functioning of the VCO. The consumption and phase noise of VCOs are highly dependent on it.

The most critical part of the tank is the inductor; its parasitic series resistance has a big impact on the degradation of the quality factor of the resonator.

To seriously degrade the VCO, a 2Ω-resistance is connected in series with each terminal of the inductor.

A simulation is carried out with a grounded $V_b$, and then its value is externally increased.

The results are shown in Table II-XI.

| | **Vb = 0 mV** | **Vb = 80 mV** | **nominal** |
|---|---|---|---|
| Vpp [mV] | Oscillation never properly started! | 780 | 878 |
| Freq [GHz] | | 3.25 | 3.38 |
| PN [dBc/Hz] | | -116.4 | -119.7 |
| OutLDO [mV] | | 1.1 | 0.965 |
| Idd [mA] | | 10.5 | 5.8 |

**Table II-XI: Data for inductor degradation. The second column shows that a $V_b$-increase helps partially correcting the CUT**

As in the previous case, the start-up of the oscillation is not possible. The increased value of $V_b$ allows the CUT to be fed with a higher current, and the oscillation can start.

The performances of the VCO are not entirely recovered, but the correction allows the VCO to oscillate, which is its main function.

This last scenario demonstrates, as the others, that a control via $V_b$ can be helpful in the self-correction of the VCO.

#### *II.6.2.4 Remarks*

A completely analog feedback would prove more efficient and would allow a better correction of the phase noise.

This study is only intended for evaluating the potential of a corrective feedback via $V_b$.

An analog feedback is beyond the scope of this work.

### *II.6.3 Implementation of a "discrete" feedback triggered by the logic output of the BIST*

To evaluate the response time of the proposed solution, a simple discrete feedback is designed.

If the BIST detects a problem, it outputs the logic '1'. This '1' triggers a feedback that changes the value of $V_b$ from 0mV to 75mV.

The schematic of this "discrete" feedback is represented in Figure II-39.

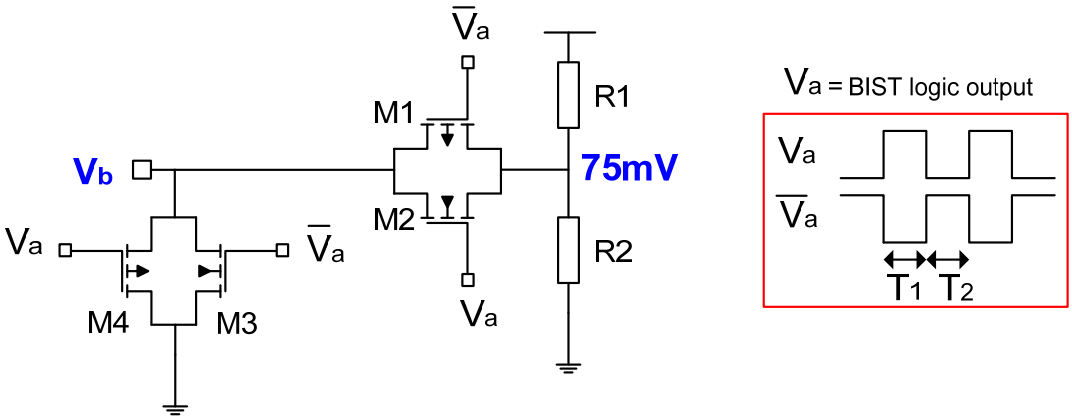


**Figure II-39: Transmission-gates connecting $V_b$ either to ground or to the value of 75mV depending on the output of the BIST**

The output of the BIST ($V_a$) and its complementary are used.

Two transmission-gates connect $V_b$ either to ground or to the value of 75mV.

The working principle of the feedback can be summarized as follows:

$$\begin{matrix} malfunctioning \Rightarrow V_a = 1 \; and \; \overline{V_a} = 0 \implies V_b = 75mV \\ good \; functioning \Rightarrow V_a = 0 \; and \; \overline{V_a} = 1 \Rightarrow V_b = 0mV \end{matrix} \quad (51)$$

A transient simulation is then run, in which the inductor of the LC resonator is degraded connecting in series to each one of its terminals a 2Ω-resistor.

The results of the transient response are shown in Figure II-40.

At t=150ns, the 2Ω-resistors are connected to the inductor. The VCO reacts stopping its oscillation. The peak-to-peak detector immediately detects this change, and triggers the corrective feedback. The value if $V_b$ is almost instantaneously increased to 75mV.

The voltage reference responds to this stimulus increasing its output voltage. This in turns increases the output voltage of the LDO, which supplies the VCO. The VCO is now feed with a higher current, which enables the oscillation again, as demonstrated in the lower portion of Figure II-40.

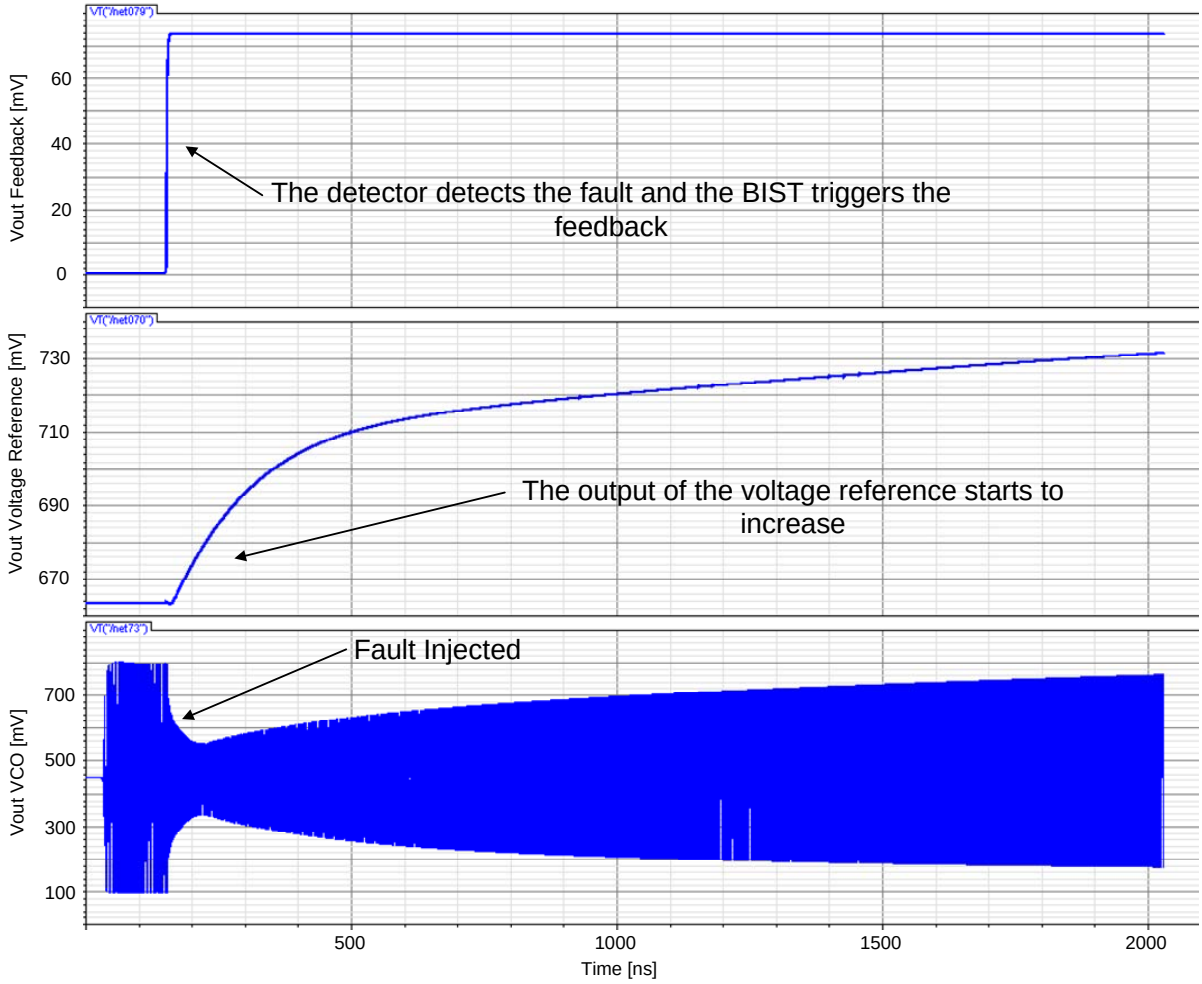


**Figure II-40: Transient response of the feedback system when a strong degradation of the inductor is introduced. The BIST efficiently detects the problem and triggers the corrective feedback that increases $V_b$.**

As already pointed-out, the correction of the CUT is slow. Almost 2µs are needed to recover the proper value of the output voltage amplitude. Depending on the application, this response time can be considered as acceptable or not.

The main bottleneck comes from the slow response of the voltage reference.

### *II.7 Conclusion*

The study starts with the decision of implementing a built-in structural test for wafer sort purposes.

Its simplicity compared to a functional test is the major reason for this choice, because it allows a low-cost solution hardly reachable if a functional test were implemented.

The methodology that needs to be followed to carry out any structural test is shown in detail.

Starting from the catastrophic and parametric automatic fault injection, it is demonstrated that, in the case of a RF VCO, the quantity that needs to be monitored on-chip is the value of the peak-to-peak output voltage of the VCO.

This quantity guarantees the highest fault coverage.

With this new information at hand, the architecture for the BIST is chosen and the main building blocks of the system are presented, through schematics and simulations.

The LDO, the VCO, the temperature and supply-voltage independent voltage reference, the detector and the comparator are implemented making use of the ST CMOS 65nm technology.

The BIST outputs the digital pass/fail information easy to handle by external software.

The behavior of the BIST is validated through transient simulations in which faults are injected and erased. The detector detects the faults and outputs the logic ‘1’ in the case of presence of a fault.

It is proven that the BIST is almost completely transparent; the performances of the VCO are not degraded.

Finally, the possibility to exploit the logic output of the BIST for self-correction is investigated.

The logic ‘1’ output by the BIST in case of a faulty circuit triggers a corrective feedback. This feedback exploits the characteristic of the voltage reference to be adjustable in order to change the consumption of the VCO.

It is shown that in different non-destructive scenarios, the system BIST + feedback is able to recover the functioning of the damaged VCO.

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## Contents

# III MEASUREMENTS OF THE BIST ARCHITECTURE FOR WAFER SORT

## *III.1 Measurement of the stand-alone building blocks for the BIST*

A first chip with stand-alone building-blocks has been sent to the ST foundries in March 2009.

The CMOS run is the S65C9_2.

This chip is depicted in Figure III-1. Its main purpose is to allow the individual characterization of every main block of the system (voltage reference, LDO, VCO, Vpp-detector).

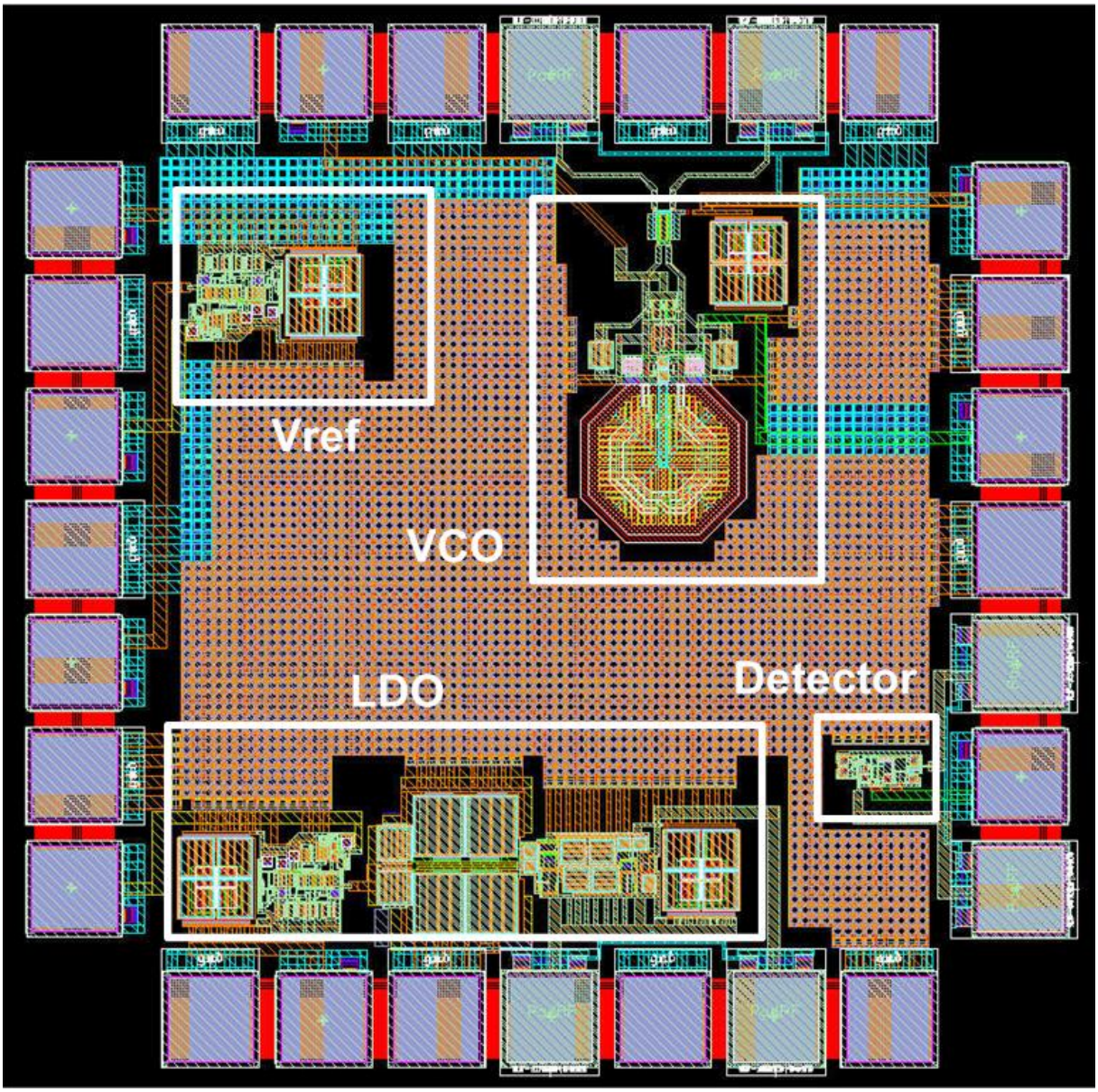


**Figure III-1: Chip with stand-alone building blocks for characterization**

### *III.1.1 Design of the Printed Circuit Board*

The chip was encapsulated in a SOIC28 package for measurement on a Printed Circuit Board (PCB). The board has been designed using ADS and the 50Ω-terminations were simulated with the software Momentum.

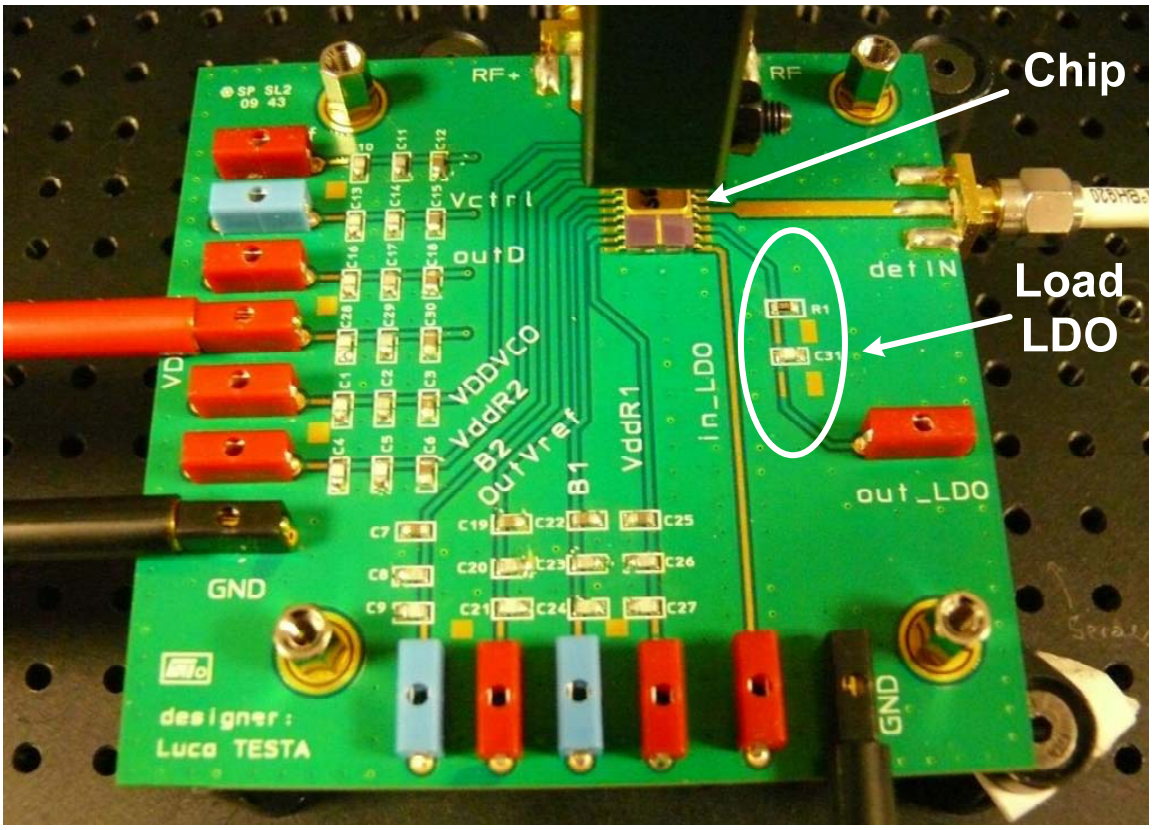


**Figure III-2: Photo of the PCB used for the measurement of the chip with stand-alone blocks**

In Figure III-2 the photo of the PCB is shown; the substrate is the low-cost FR4.

All the surface mounted passives are decoupling capacitors for noise reduction on the supply lines. Value of 10pF, 1nF and 100nF are used in order for the decoupling to be efficient on a large frequency range.

Only two passives are not used for decoupling; those are a resistor (200Ω) and a capacitor (20pF) in parallel, connected between the output of the LDO and GND. Those elements create a load for the LDO. In this way, the LDO drives the same amount of current as if the VCO was still connected to its output (thanks to the resistor) and it sees almost the same output impedance (thanks to the capacitor). This is not completely true because of the bonding between the die and the package, which has a large inductance associated with it (1nH/mm).

### *III.1.2 Measurement of the temperature and supply-voltage independent voltage reference*

Two measurements are performed on the voltage reference.

The first one, at room temperature, verifies the supply-voltage independence of the circuit and the control on the output voltage via the bulk voltage $V_b$ of the transistor in the triple-well.

The second measurement verifies the temperature independence of the circuit.

#### *III.1.2.1 Supply-voltage independence*

The supply voltage is swept from 0.5V to 1.2V and the output voltage of the voltage reference is measured, at room temperature.

This measurement was performed for different values of $V_b$, to verify the possibility to control the output voltage via this method.

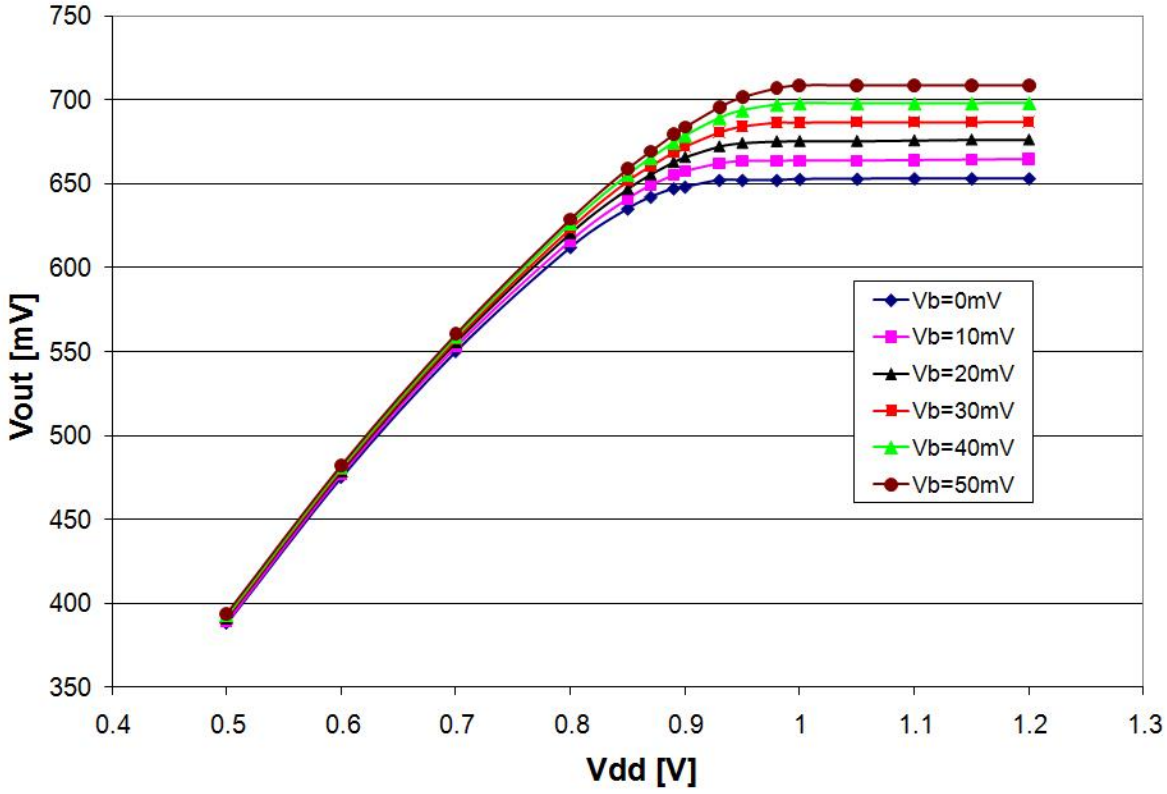


**Figure III-3: Output voltage of the voltage reference when the supply voltage is swept from 0.5V to 1.2V. The measurement has been carried out for 6 different value of $V_b$ to verify the control on the output voltage.**

In Figure III-3 the result of the measurements is presented. The multimeter 34401 by Agilent was used because this instrument has the option of really high input impedance (several GΩ), needed because the voltage reference cannot drive a high current.

The measurements reflect very well the simulations.

Starting from a supply voltage slightly lower than 1V, the output voltage stabilizes to its value, as expected. Starting from that point, the great flatness of the output voltage is a proof of the high power-supply rejection ratio of the circuit.

The control via $V_b$ works properly too. The output changes linearly with $V_b$. For a 10mV change in $V_b$, the output changes by approximately 12mV.

#### *III.1.2.2 Temperature independence*

The study of the behavior of the voltage reference in temperature is performed with the circuit inside a temperature-controlled oven.

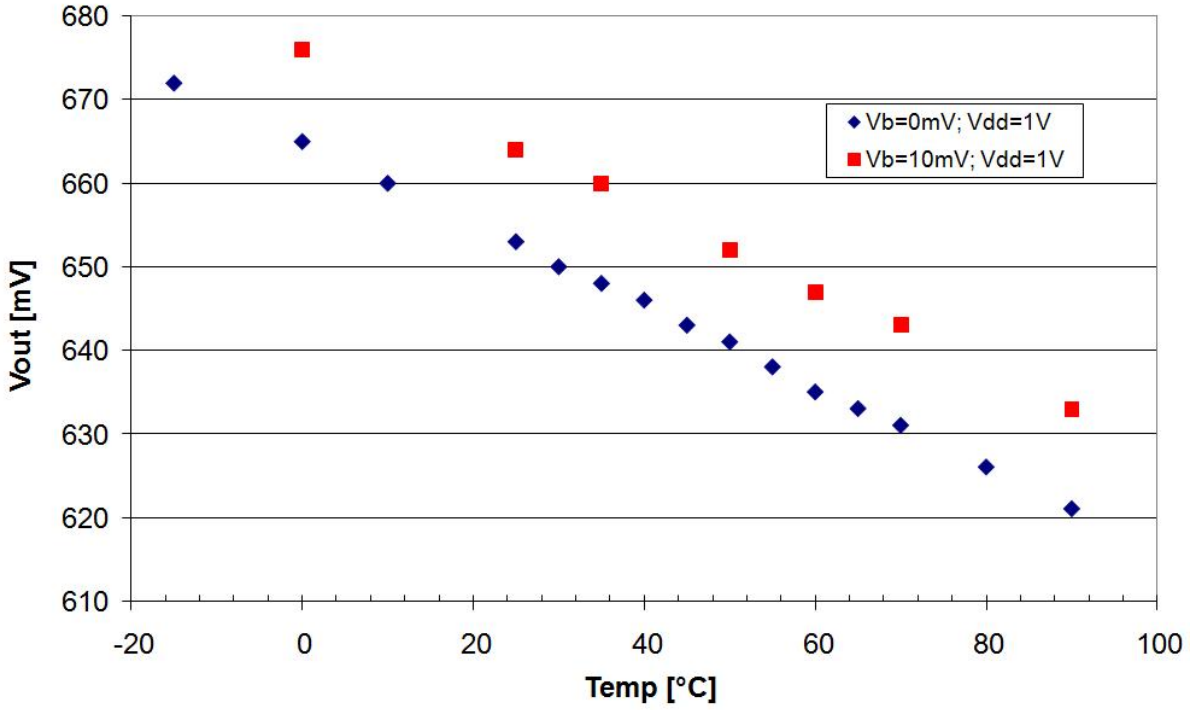


**Figure III-4: Output voltage of the voltage reference when the temperature is swept from -15°C to 95°C**

In Figure III-4 the measurement of the output voltage is presented for a temperature sweep (inside the oven) starting from -15°C to +95°C.

The measurements are performed with a supply voltage of 1.0V and for two different values of $V_b$.

Unfortunately the circuit does not result being temperature-independent. A 50mV change is measured for a 110°C sweep, resulting in 455ppm, unacceptable for a temperature independent voltage reference.

The same behavior is observed for different values of $V_b$.

Recalling from the previous chapter, the temperature independence of the output is reached through the right choice of two current gains, $G_1$ and $G_2$.

Those current gains are obtained with a pMOS current mirror in a cascode configuration.

If the current mirrors fail to give the right value for $G_1$ and $G_2$, then the temperature independence is lost. The copy of the currents is highly dependent on technology dispersions and mismatch.

In Figure III-5 the layout of the voltage reference is shown; in the upper portion of the layout, the pMOS current mirror is visible. The left side of the current mirror is in charge for $G_1$=3 while the right side should give $G_2$=2. The total Si area occupied by the circuit is approximately 0.0064 mm$^2$.

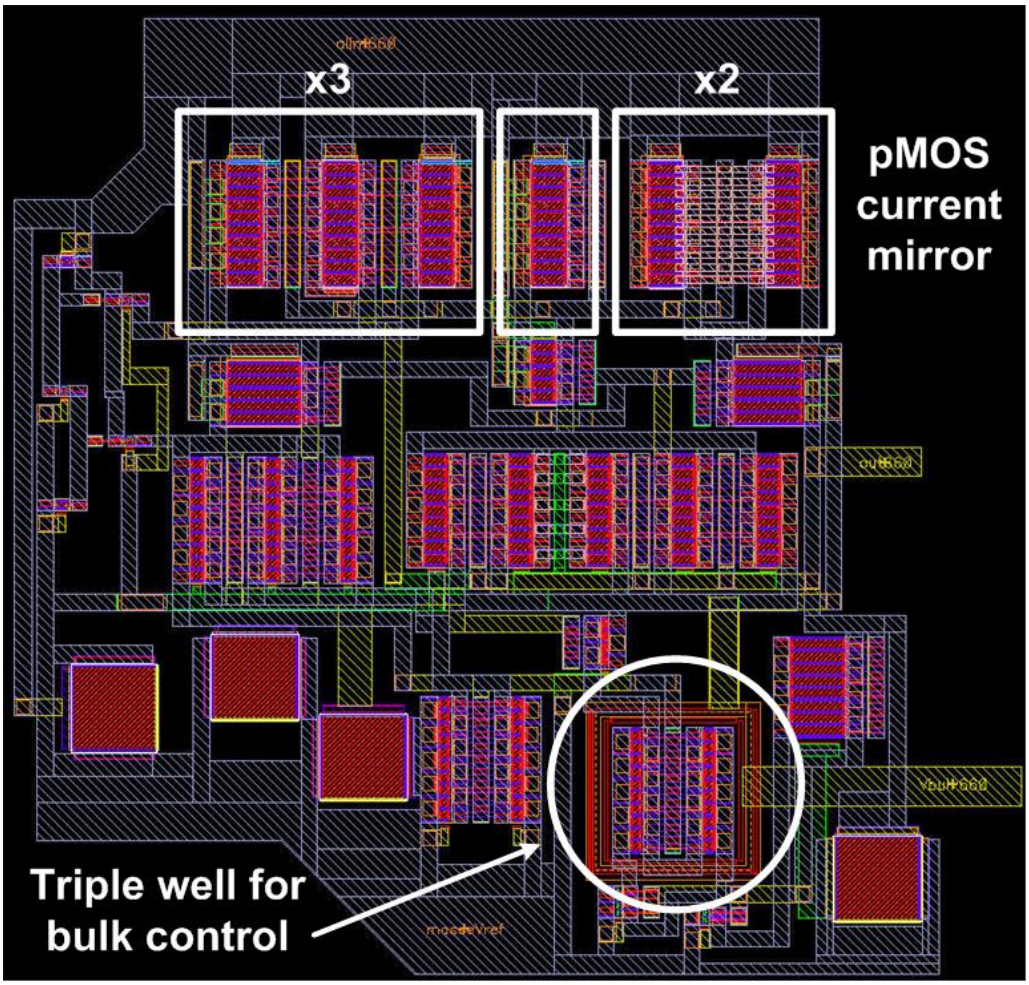


**Figure III-5: Layout of the temperature and supply-voltage independent voltage reference. The pMOS current mirror for generation of $G_1$ and $G_2$, and the triple-well for external control on the bulk are shown.**

Two are the main causes of the erroneous values for $G_1$ and $G_2$.

- There are no dummy-cells in the pMOS current mirror; the layout is poor. The errors caused by mismatch and technology dispersion are not minimized. The ratio of the widths of the transistors is not exactly the one that was expected.
- The low supply voltage and the high number of stacked transistors (6 between VDD and GND in the main branch) make it difficult to guarantee that the transistors in the current mirror will always work in the saturation region.

In a future version, some way of trimming the circuit can be introduced.

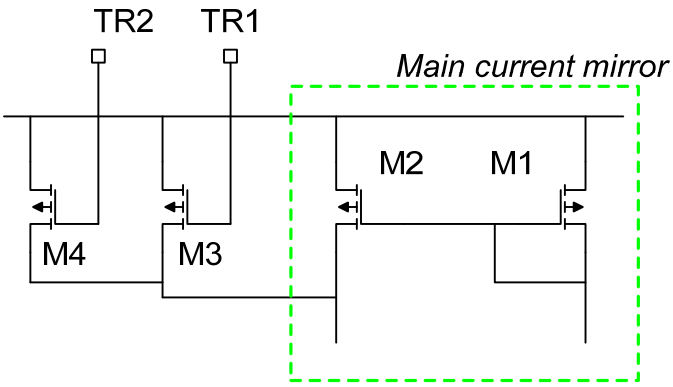


**Figure III-6: Digital trimming system for the current mirror**

A possible digital trimming system is depicted in Figure III-6; M1 and M2 build-up the main current mirror. In the case M2 results being too small after fabrication, giving rise to a too small current ratio ($I_{M2}/I_{M1}$), the small transistors M3 and M4 can be turned on sending a digital "1" to TR1 and TR2.
In this way, the total width of M2 slightly increases, allowing delivering the needed amount of current.

Another source of error comes from the model describing the temperature behavior of the transistor. If the technology is not mature, the model associated with it may be poor.
In particular, if the temperature behavior of the threshold voltage $V_{TH}$ is not well described, the two chosen gains $G_1$ and $G_2$ will be erroneous (Equation 42 in previous chapter).
The hypothesis of a decreasing affine law of $V_{TH}$ over temperature was made (Equation 43 in previous chapter).
Even if the value of $\partial V_{TH}/\partial T$ is not the expected one, from Figure III-4 it can be seen that the hypothesis of a decreasing affine law of $V_{TH}$ is correct.

### *III.1.3 Measurement of the peak-to-peak voltage detector*

The setup for the measurement of the peak-to-peak voltage detector is presented in Figure III-7.

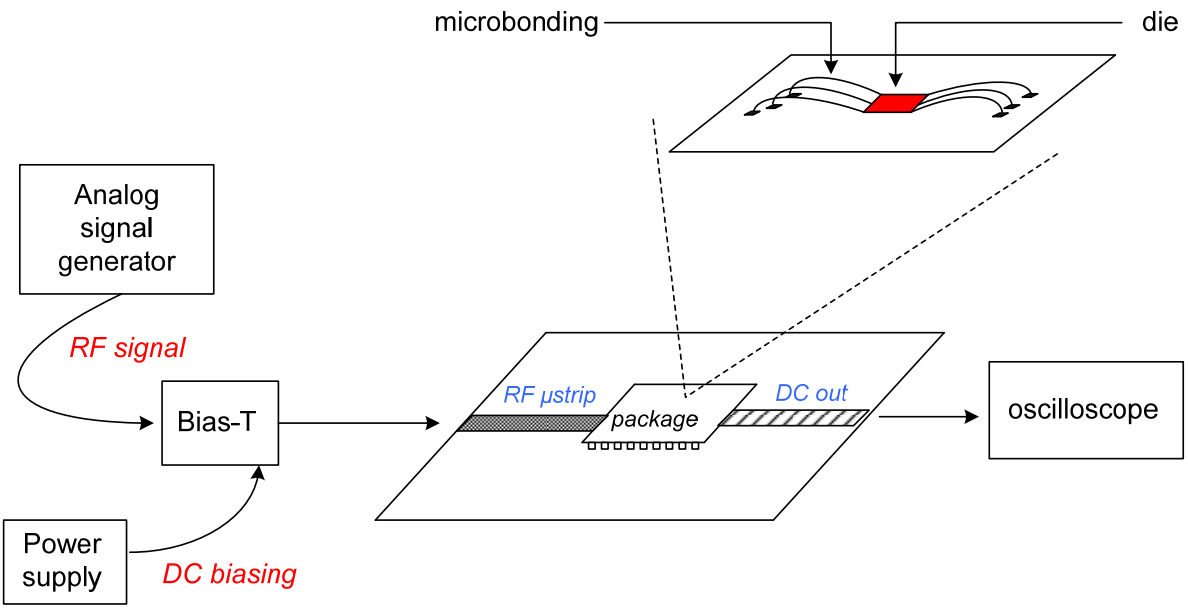


**Figure III-7: Setup for the measurement of the peak-to-peak voltage detector highlighting some de-embedding problems**

The analog signal generator Rohde&Schwarz SMIQ 06B was used to inject a RF 3.5GHz signal at the input of the detector. A bias-T was used to bias the input stage of the detector. The oscilloscope Tektronix TDS2014 was connected at the output of the detector to measure its DC-output voltage.

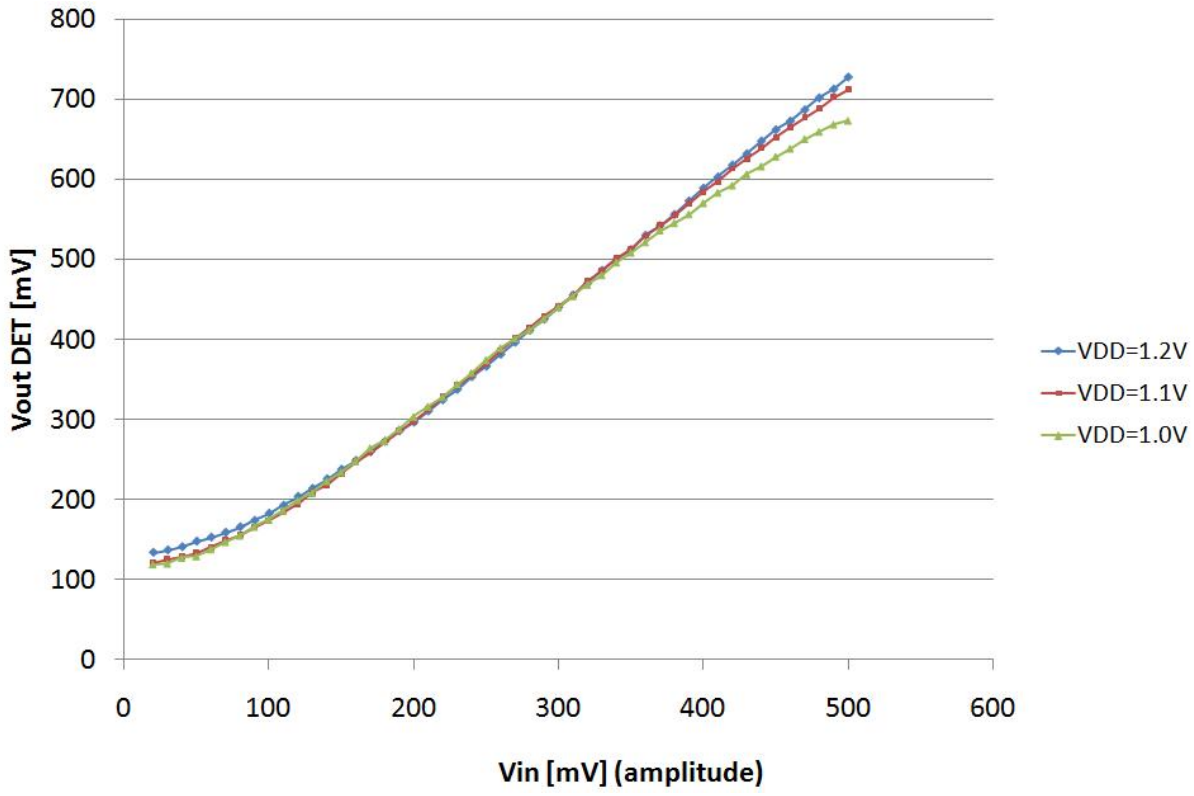


**Figure III-8: Input/output measured characteristic of the peak-to-peak voltage detector**

The measured input/output characteristic of the peak-to-peak voltage detector is shown in Figure III-8 for three different values of the supply voltage: 1.2V, 1.1V and 1.0V.

The detector shows a very linear behavior in a large input range and its ability to function properly even at low supply voltages is proved.

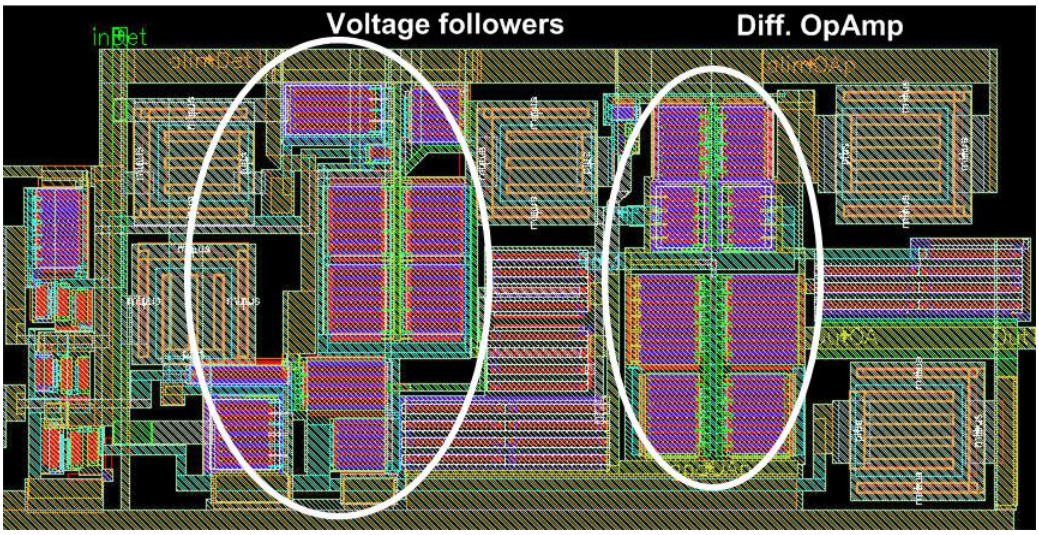


**Figure III-9: Layout of the peak-to-peak voltage detector**

In order to compare the measurements with the simulations, the de-embedding of the circuit has to be taken into account.

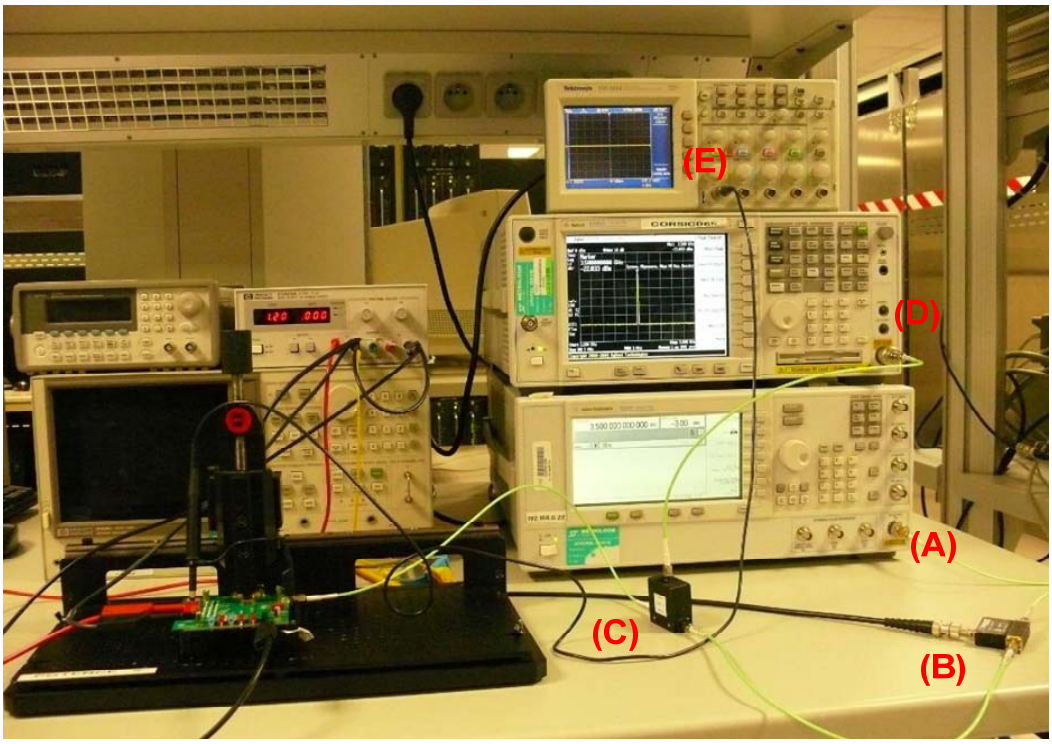


**Figure III-10: Photo of the measurement setup. *A* is the signal generator, *B* is the bias-T, *C* is the circulator, *D* is the spectrum analyzer and *E* is the oscilloscope**

As inferred from Figure III-7, before arriving at the on-chip input of the detector (shown in Figure III-9), the RF signal has to pass through some cables, the bias-T, the RF microstrip on the PCB and the micro-bonding from the package to the die.

The setup shown in Figure III-10 was used to measure the losses of the cables and of the bias-T. The circulator was used to measure the input reflected power, since the input of the detector does not present 50Ω-input impedance.

While the input reflected power can be neglected, the cables and the bias-T give rise to a total loss of approximately 3.2dB.

Once those losses taken into account, it is possible to compare the results of the measurements with the simulation of the input/output characteristic of the detector.

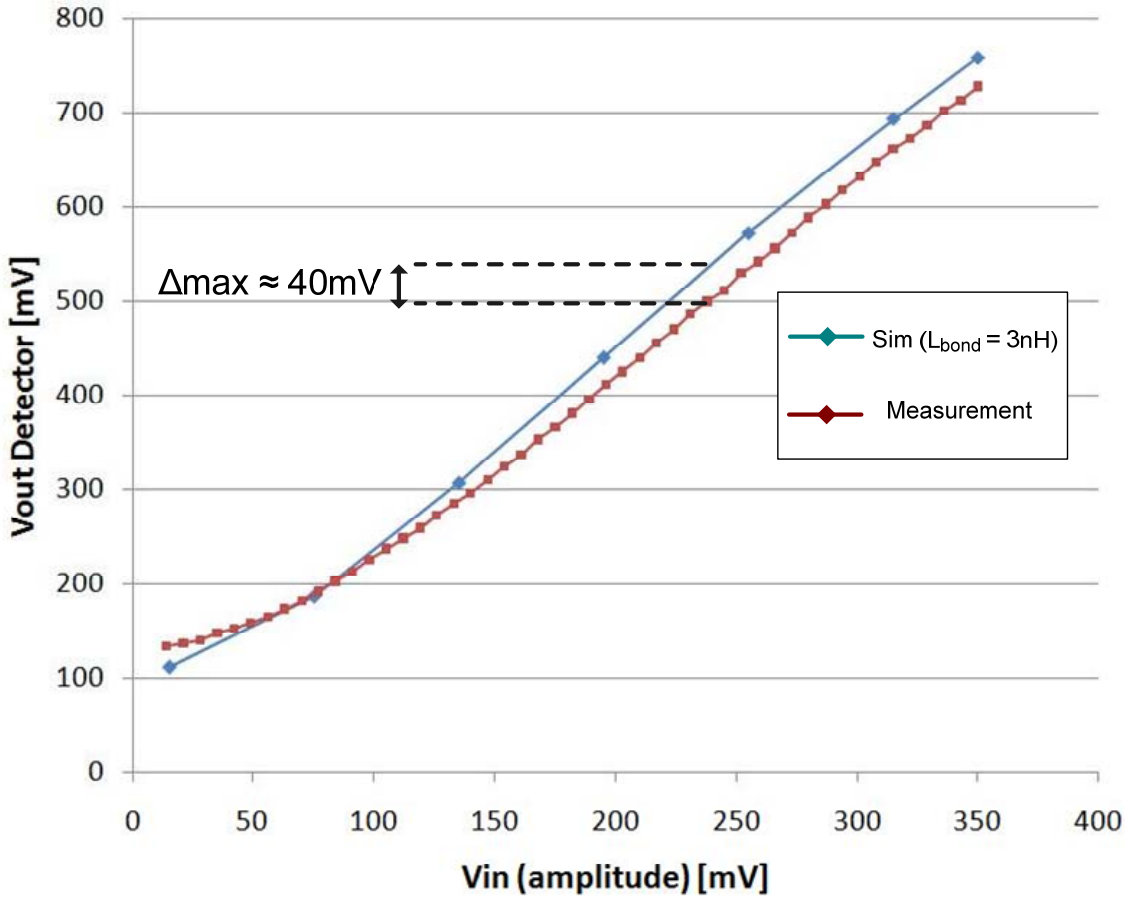


**Figure III-11 Comparison between simulation (blue) and measurement (red) of the detector**

The comparison between the measurements and the simulation of the detector is presented in Figure III-11. During the simulation, the micro-bonding between package and die is simulated with a 3nH-inductor.

The measurements reflect well the expected behavior of the detector. A maximal 40mV discrepancy is observed.

The losses of the cables and of the bias-T are de-embedded from the measurements; the losses due to the RF microstrip on the PCB are not taken into account. If added, those extra losses would shift the measured input/output characteristic of the detector to the left, making the measurements fit almost perfectly the simulations.

#### *III.1.4 Problems on the LDO and on the output buffer of the VCO*

It was impossible to measure either the LDO or the VCO.

The LDO is instable. Great care was taken during the layout phase in order to guarantee a phase margin higher than 60° for its open-loop frequency response. The stability study was carried out with the VCO connected to the LDO. The LDO had then a defined load and a known current passing through it. If the LDO is measured as a stand-alone block, its load changes; as a consequence, the location of poles and zeros of its transfer function change and instability issues may arise.
In order to avoid this possibility, a resistor and a capacitor in parallel were connected as external passives on the PCB at the output of the LDO, as shown in Figure III-2.
This precaution was not enough.
Probably, the micro-bonding between the die and the package and the long path on the PCB to connect the package to the external connectors added a non-negligible parasitic inductance that modified the load in such a way to produce instability.

The buffer connected at the output of the VCO presents a short-circuit between its supply voltage and ground. This problem, investigated in the next paragraph, causes any extraction of the RF signal impossible.

Those first measurements allowed the complete validation of the peak-to-peak voltage detector and the partial validation of the voltage reference.
Next, the entire system is presented.

### *III.2Measurements of the chip with BIST capabilities for the wafer sort*

The first prototype of the VCO with BIST capabilities for the wafer sort has been sent to the ST foundries in March 2009. The CMOS 65nm run is the S65C9_2.

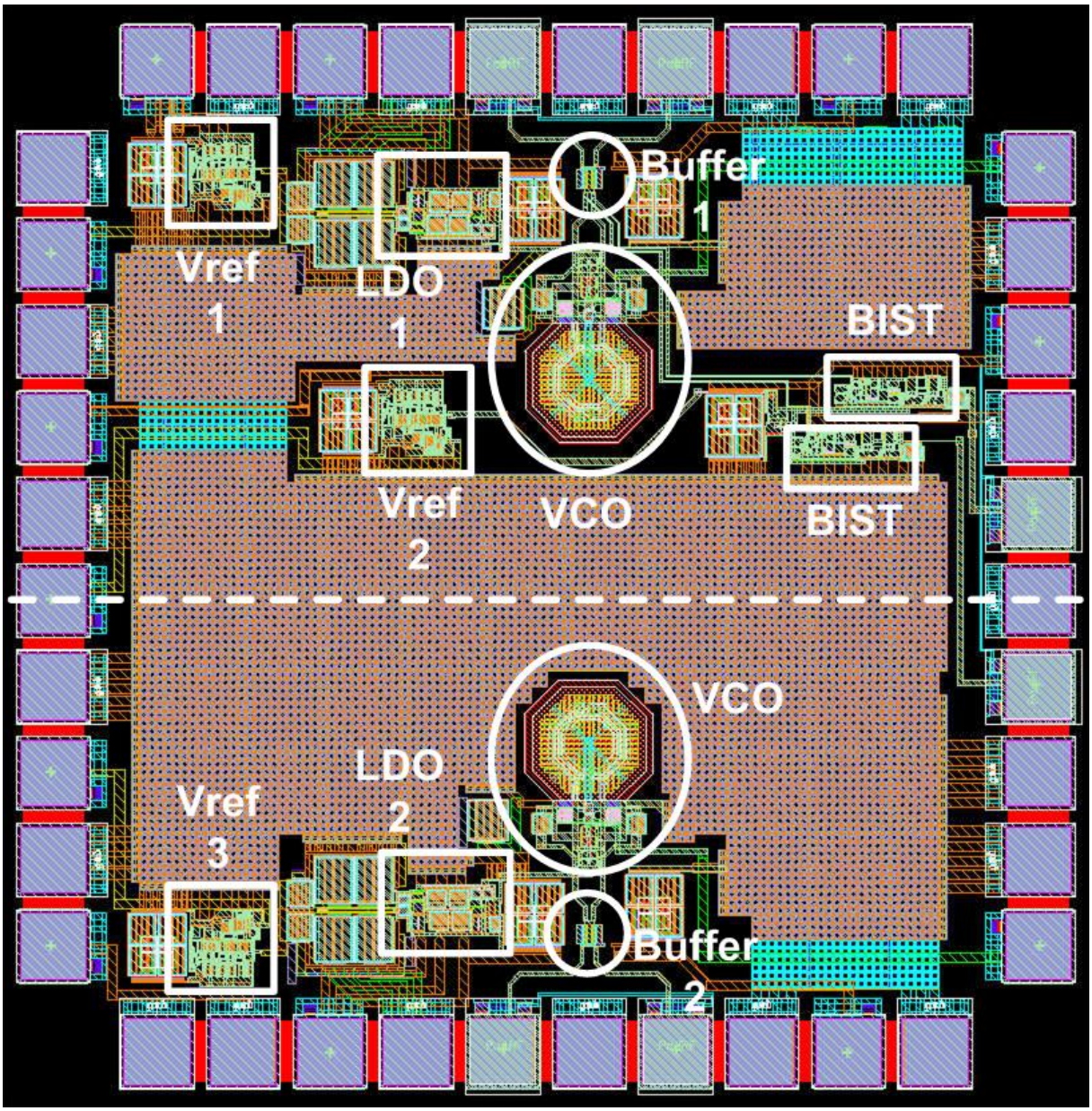


**Figure III-12: Layout of the first prototype. The upper portion of the chip contains the CUT and the BIST; the lower portion contains the stand-alone CUT.**

The layout of the prototype is presented in Figure III-12.

The upper portion of the chip contains:

- Voltage-reference Vref1 to drive the voltage regulator
- LDO1 to supply the VCO
- VCO
- Buffer1 to drive the 50Ω load
- Voltage-reference Vref2 to generate a stable voltage to obtain $V_H$ and $V_L$
- BIST ($V_H$ and $V_L$ generator, Vpp detector, comparator and final digital stage)

The lower portion of the chip contains:

- Voltage reference Vref3 to drive the voltage regulator
- LDO2 to supply the VCO
- VCO
- Buffer2 to drive the 50Ω-load

Each voltage reference has a separate supply voltage, with its own pad. The same is true for each LDO and each buffer. The BIST blocks are independently powered-up too.

The main reason for separate pads for the power supplies is that it will be possible, during the measurements, to have control on each block. The main drawback is that the layout becomes pad-limited. The total pad count is 40 for this chip.
The chip occupies a squared Si area of 1.7mm$^2$.

The blocks LDO, voltage reference, VCO and buffer are strictly identical in both the “stand-alone” and the “with BIST functionality” circuits.

### *III.2.1 Design of the Printed Circuit Board*

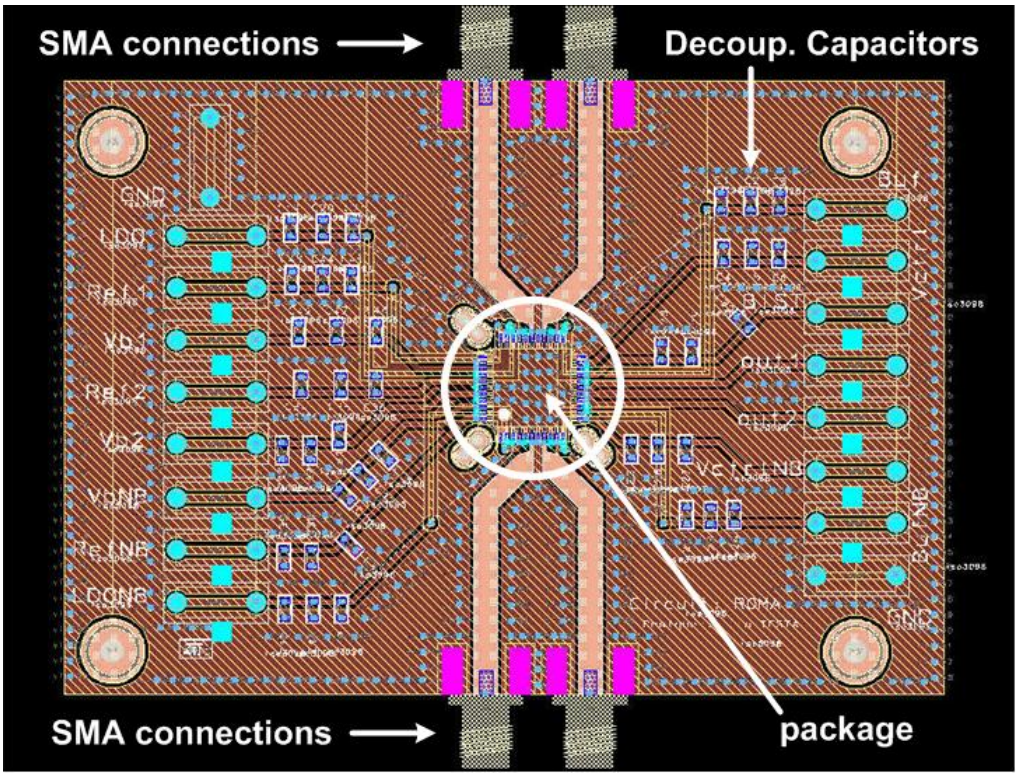


**Figure III-13: PCB designed with ADS. The RF microstrip lines connect the output of the buffers with the SMA connectors to reach the external instrumentation.**

The chip was encapsulated in the ceramic package CQFP44 for measurements on Printed Circuit Board (PCB).

The PCB was designed using ADS and the RF microstrip lines were simulated with the software Momentum to guarantee 50Ω-characteristic impedance.

In Figure III-13 the PCB is presented. The substrate is a low-cost FR4. Decoupling capacitors are added on the board, to reduce the noise on the power supply lines. Values of 10pF, 1nF and 100nF are used in order for the decoupling to be efficient on a large frequency range.

### *III.2.2 Layout of the CUT*

The common centroid technique is exploited for the layout of the VCO.

A pMOS couple and an nMOS couple are needed for the CUT; each transistor is composed of 2 transistors in parallel. This particular choice allows to layout the circuit as proposed in Figure III-14. This structure limits problems caused by cross-chip gradients and guarantees good matching performance. The main drawback resides in the fact that the layout of the interconnections becomes much more complicated.

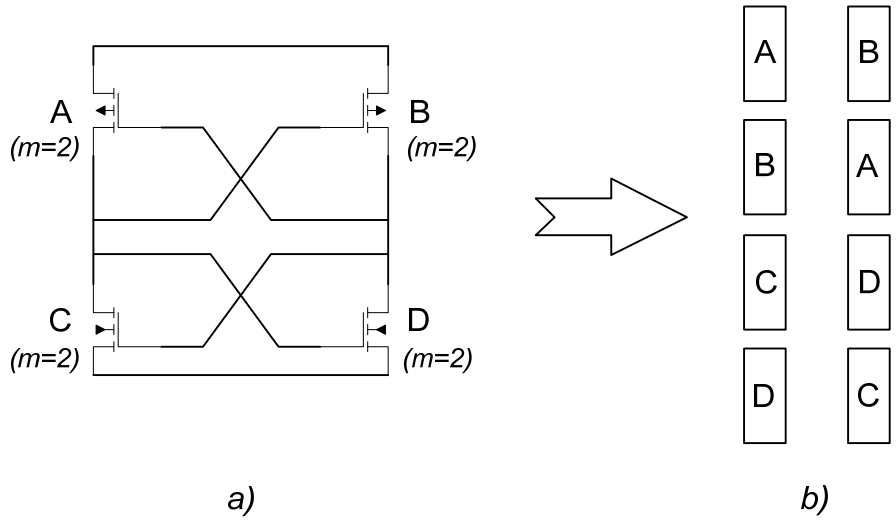


**Figure III-14: Common centroid layout for the active components composing the VCO**

The layout of the VCO is shown in Figure III-15. The capacitors and the varactors are placed as close as possible to the inductor, in order to minimize extra series resistances at the access of the inductor.

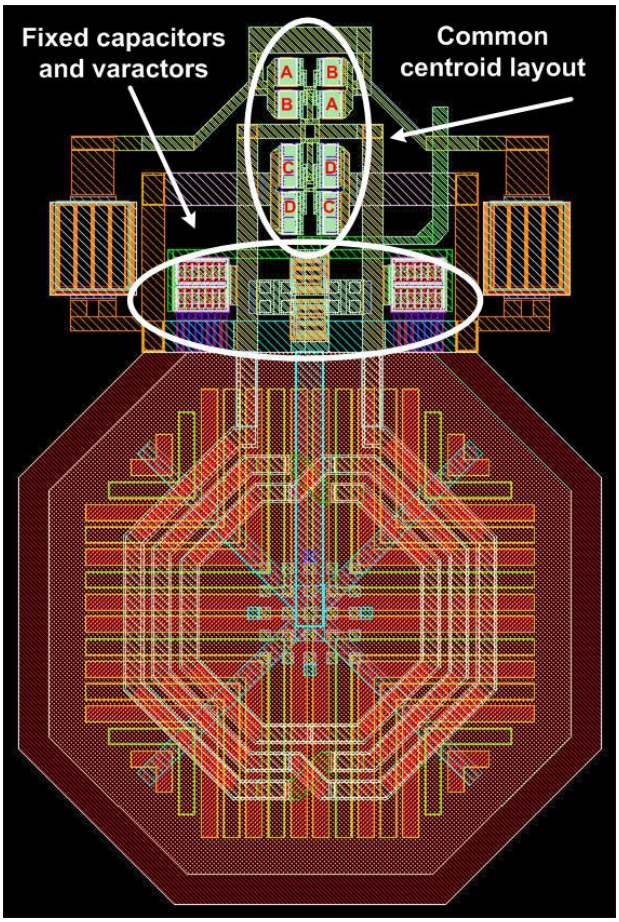


**Figure III-15: Layout of the VCO**

### *III.2.3 Layout of the buffer*

The choice for the buffer was a simple differential pMOS amplifying stage with open-drains. The drain terminals are terminated off-chip with a bias-T. The inductor of the bias-T provides the load needed for amplification at the frequency of oscillation of the VCO. Moreover, the inductor does not waste any DC-voltage drop.

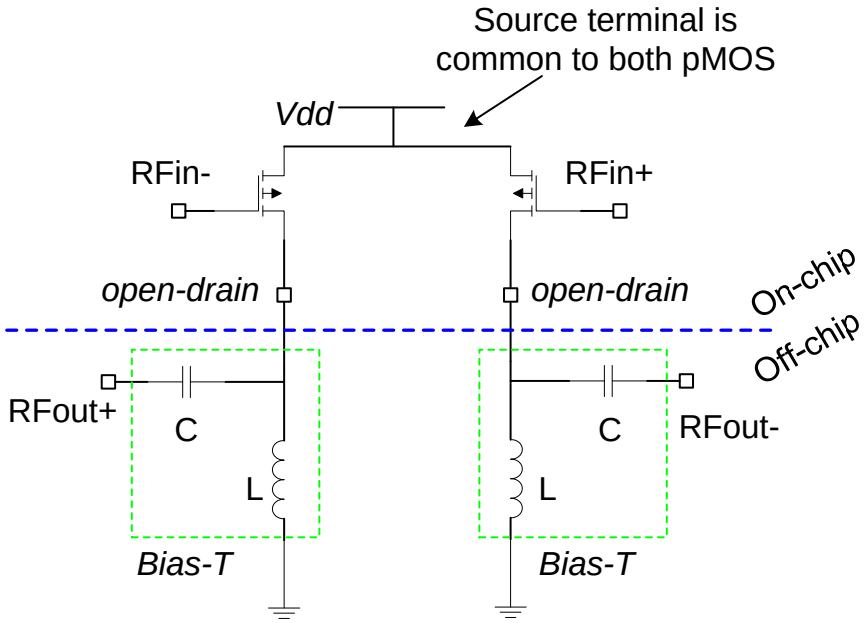


**Figure III-16: Schematic of the buffer; pMOS transistors with open-drain structure are used**

For the layout of the buffer, the fact that the two pMOS transistors share the same source terminal is exploited. Both a common centroid and an interdigitated technique are here used. The main advantages of the interdigitated technique are the save in area and the reduction of the complexity of the interconnections.

The layout is explained in Figure III-17. Each pMOS (called A and B in the figure) is composed of many transistors in parallel, whose disposition is depicted in Figure III-17a. Since A and B both share the source terminal, connected to the power supply, the fingers of source, gate and drain are arranged as shown in Figure III-17b. Letters *A* and *B* stand for the gate terminals of the two transistors, *Da* and *Db* are the drain terminals and *S* is the common source terminal.

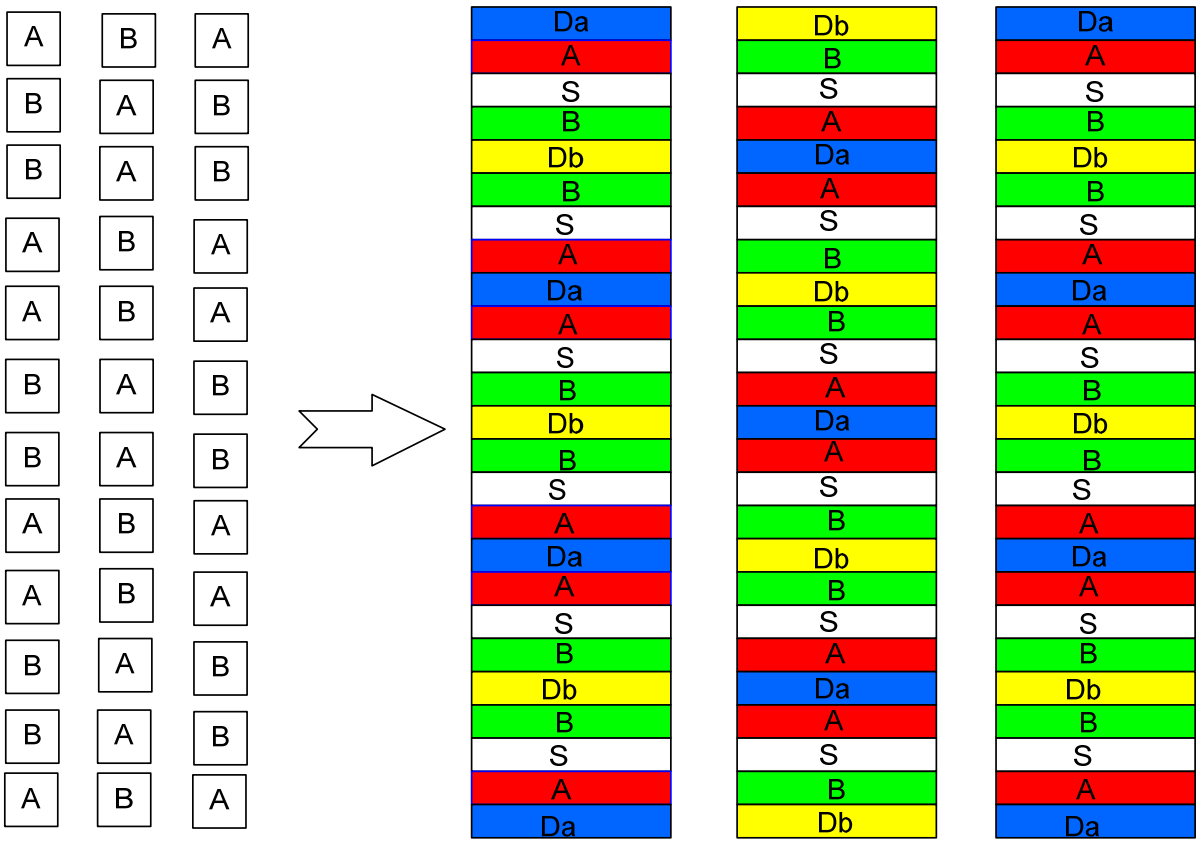


**Figure III-17: Representation of the disposition of the 2 pMOS used for the buffer. On the right side of the figure, the letter "S" stands for source (which is shared by both pMOS), "A" represents the gate of one pMOS, "B" is the gate of the other pMOS, "Da" is the drain terminal of one pMOS and "Db" is the drain of the other pMOS.**

The common centroid technique was used for the layout of both the VCO and the buffer in order to guarantee a good matching of the components. This, in turn, should guarantee the preservation of the differential structure of the circuits.

If the structures were not exactly differential, the negative impact on the phase noise would be important.

*III.2.4 Problems during the measurements*

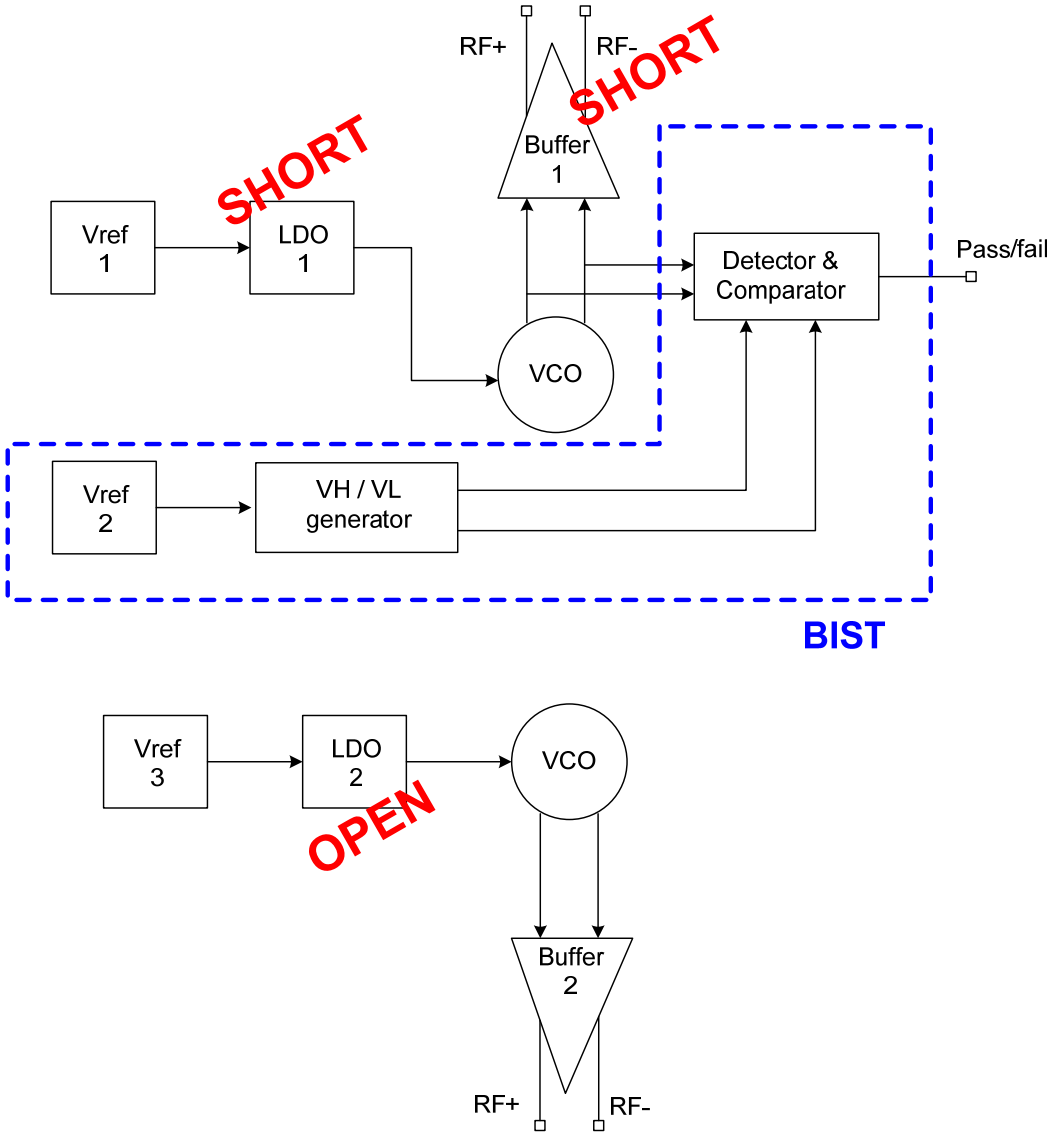


**Figure III-18: Floor-plan of the chip**

During the measurement phase, multiple problems have arisen.

In Figure III-18 the floor-plan corresponding to the layout of Figure III-12 is shown, to highlight the problems found together with their location.

The upper portion of the chip (version with BIST capabilities) presented two problems:

- Short-circuit between VDD and GND for the LDO
- Short-circuit between VDD and GND for the buffer

The lower portion of the chip (stand-alone CUT) presented the following problem:

- Open-circuit in the LDO

Those problems made the extraction of any RF signal from the chip impossible.

#### *III.2.4.1 Investigation of the problems*

Buffer1 and Buffer2 in Figure III-18 are identical, but the one in the upper portion of the chip is short-circuited while the other seems to have the right biasing.
Since LDO2 is open-circuited, it does not power-up the VCO. As a consequence, the DC output voltage of the VCO is not correct (closer to 0V than to 450mV as designed).
The buffer is a pMOS differential amplifying stage; since its DC-gate-voltage is lower than expected, the current consumption of Buffer2 should be higher than the designed case.
In fact, its current consumption is close to 40mA, the expected value if its DC-voltage input is 0V.

No conclusion can then be made on the cause of error in Buffer1, since the same structure used for Buffer2 does not seem to have any particular problems.

LDO1 is short-circuited while LDO2 (identical to LDO1) presents an open-circuit.
Once again, the two completely different behaviors for the same circuit make any conclusion on the cause of error impossible.

To investigate if the problem was caused by the package, some bare dice were measured on a probe station. As soon as the probes touched the pads, short-circuits of LDO1 and Buffer1 were detected. Neither the encapsulation of the die nor the package itself are the cause of either short-circuits or open-circuits on the chip.

One possible explanation may come from ESD (electro-static discharge) problems.
ESD is a sudden and momentary flow of current between two objects at different potentials. Among the main causes of ESD is the static electricity, generated through tribocharging (separation of electric charges that occur when two materials are brought into contact and then separated). The friction between two materials can result in tribocharging, creating a difference of electric potential that can lead to an ESD event.
The thin dielectric under the gate of the transistors can be highly damaged by ESD.
Prevention of ESD is usually based on the connection of diodes that can walk the sudden flow of current directly to ground without affecting the active or passive elements.

As shown in Figure III-19, diodes can be connected to the gate of every transistor in order to prevent damage of the thin gate oxide. Diode D1 conducts when the input voltage is higher than VDD, while diode D2 conducts when the input voltage is lower than GND.

The higher the surface of the diode, the higher is the protection. Those diodes should be connected to the gate via the lowest available metal in the back-end of the technology (e.g. metal1), in order for the gate to be connected to GND and VDD from the first steps of the fabrication.

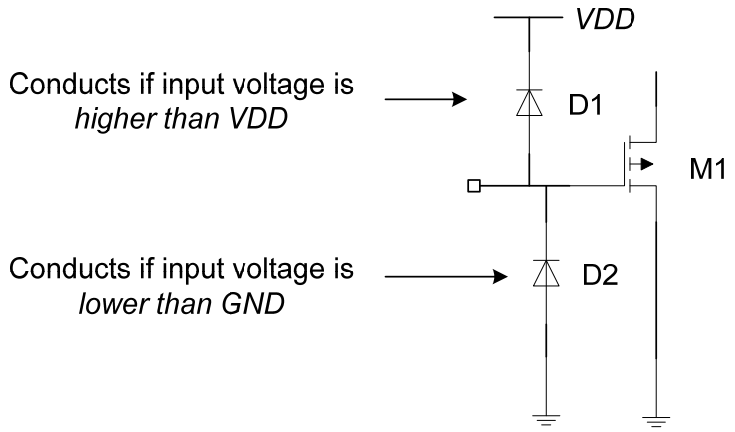


**Figure III-19: D1 and D2 have the function of ESD protection**

The same kind of protections should be applied to the VDD and GND pads also.

In the design of the chip, no protection diodes were used on the gates of the transistors.

Moreover, the protections on the pads were “light” compared to the industry standards.

Those two facts lead to the probable conclusion that the short and open circuits were induced by ESD problems.

### *III.2.5 Validation of the BIST*

The CUT is faulty; the measured BIST logic output is a “1”. The BIST portion of the chip, highlighted in Figure III-18, seems to be working correctly.

In order to validate the complete BIST capabilities of the chip, the main idea would have been to inject faults in the VCO through a sudden lowering of the supply voltage of the LDO. Unfortunately, the short-circuit of LDO1 prevents from this option.

Moreover, since the real state of the VCO is unknown, it is impossible to know either the DC input voltage of the Vpp detector or its DC-output.

The decision is then taken to play on the values of the limits $V_H$ and $V_L$.

Recalling from the previous chapter, those voltages are created via the voltage reference. If its output changes then the values of $V_H$ and $V_L$ change too.

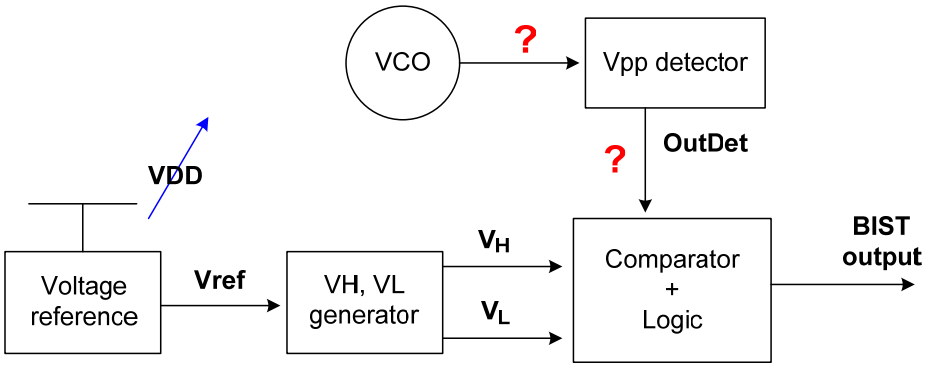


**Figure III-20: Measurement setup for the validation of the BIST**

In Figure III-20 the measurement setup for the validation of the BIST is shown.

The DC-outputs of the VCO and of the Vpp-detector are unfortunately unknown and cannot be changed. The output of the detector is compared to $V_H$ and $V_L$ and the logic "1" is output by the BIST in case *OutDet* is not within the range [$V_L$, $V_H$].

The output of the voltage reference *Vref* is changed via its supply voltage VDD. A lower supply voltage leads to a lower *Vref* and consequently to a lower value for $V_H$ and $V_L$.

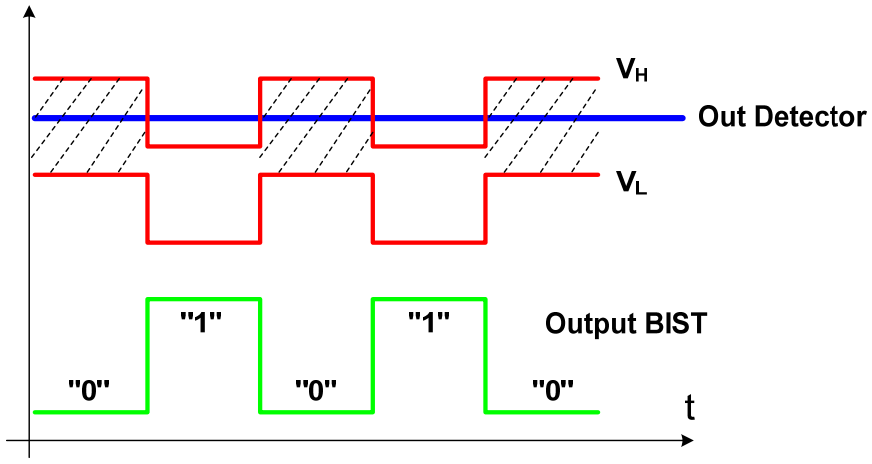


**Figure III-21: Behavior of the signals during the measurement for the validation of the BIST**

The signals that are to be created are shown in Figure III-21. $V_H$ and $V_L$ change in such a way that the output of the detector is periodically inside and outside the range of acceptance.

What is expected is then a periodic square wave at the output of the BIST.

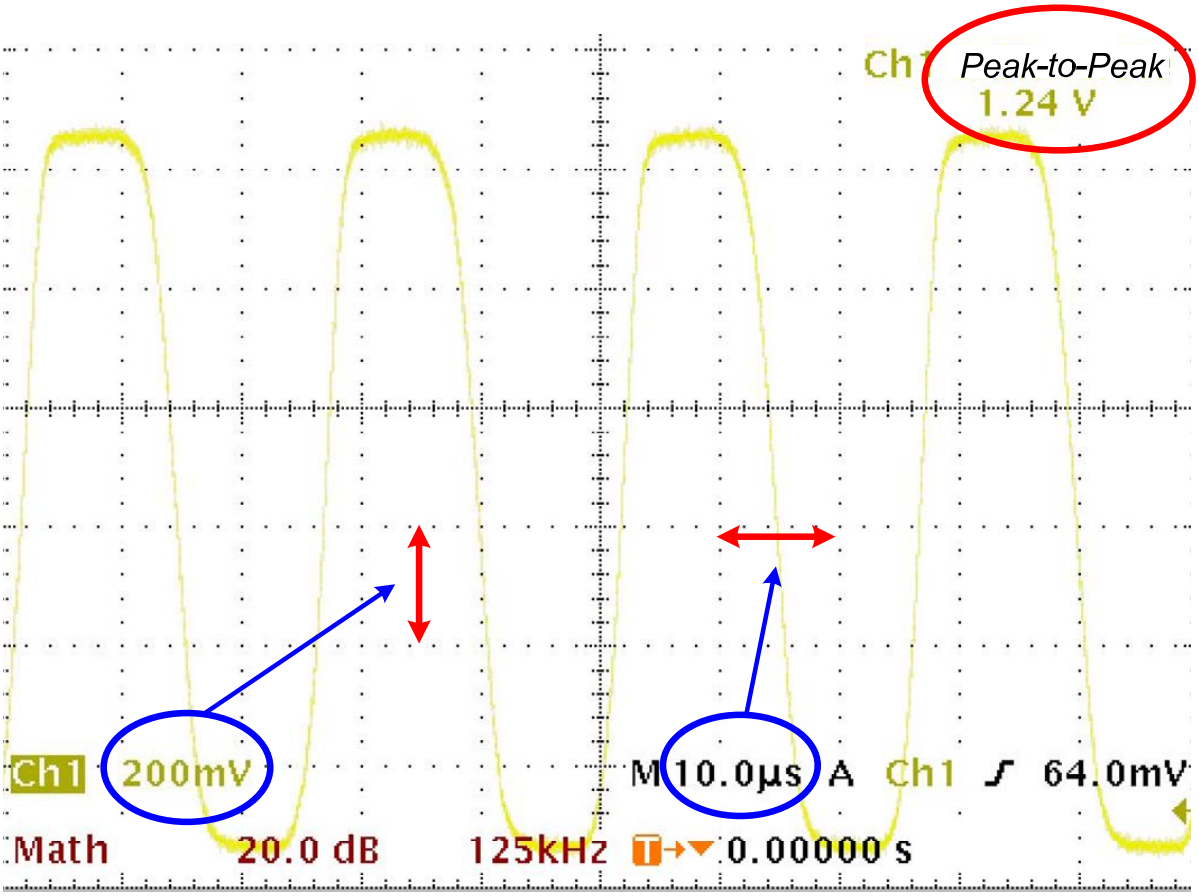


**Figure III-22: Screenshot of the oscilloscope connected to the output of the BIST**

The result of the measurement of the BIST output is presented in Figure III-22.

The supply voltage of the voltage reference is changed at a rate of 40 kHz via an AWG (arbitrary waveform generator), and consequently $V_H$ and $V_L$ change at the same rate. It can be seen that the output of the BIST switches from the logic level "1" to the logic level "0" with a period of 25 µs.

The good functioning of the comparator and of the final logic stage is demonstrated.

The high rise and fall times are caused by the method used to change $V_H$ and $V_L$. Changes in the VDD of the voltage reference do not reflect in a fast change in its output voltage.

Those measurements allowed the validation of all the blocks needed for the BIST system.

### *III.3 Conclusion*

The measurements of the main blocks needed for the BIST of the VCO are presented first.

All measurements are carried out on PCB, with the die encapsulated in a SOIC28 package.

The voltage reference shows the expected response to variations of the supply-voltage; its output voltage keeps extremely flat starting from a supply-voltage of approximately 1.0V.

The control via the bulk works as expected too. A linear relationship between output voltage and $V_b$ is measured.

The temperature independence of the voltage reference is not reached. The output experiences a 50mV excursion in the temperature range [-15°C ; +95°C]. This is probably due to a poor layout that did not guarantee the exact current copy performed by the current mirror, essential for the temperature independence. Another cause of error is the poor model of the threshold voltage behavior with temperature.

The measurements of the peak-to-peak detector fit the simulations. It's capability to work even at a 1.0V supply-voltage is proved.

The measurements of the overall architecture are then presented. All measurements are carried out on PCB, with the die encapsulated in a CQFP44 package.

A major problem is here encountered. The LDO driving the VCO and the buffer both present a short-circuit. The cause comes probably from the fact that the circuit was not protected against ESD.

The functionality of the VCO cannot then be proved.

Anyhow, the verification of the complete BIST architecture was still possible.

The high and low limits of the acceptance range are dynamically changed and measurements show that the BIST is able to output the digital pass/fail information needed for the wafer sort.

## Contents

# IV PERSPECTIVES: COMPLETE ON-CHIP CHARACTERIZATION

## *IV.1 Initial study for the complete on-chip characterization of the VCO*

The wafer sort results being the first very important test performed on the CUT. The possibility to completely integrate it leads to many economical advantages.

The wafer sort is not the only important test that has to be carried out; two main other tests need to be done: the characterization and the diagnosis of eventual problems.

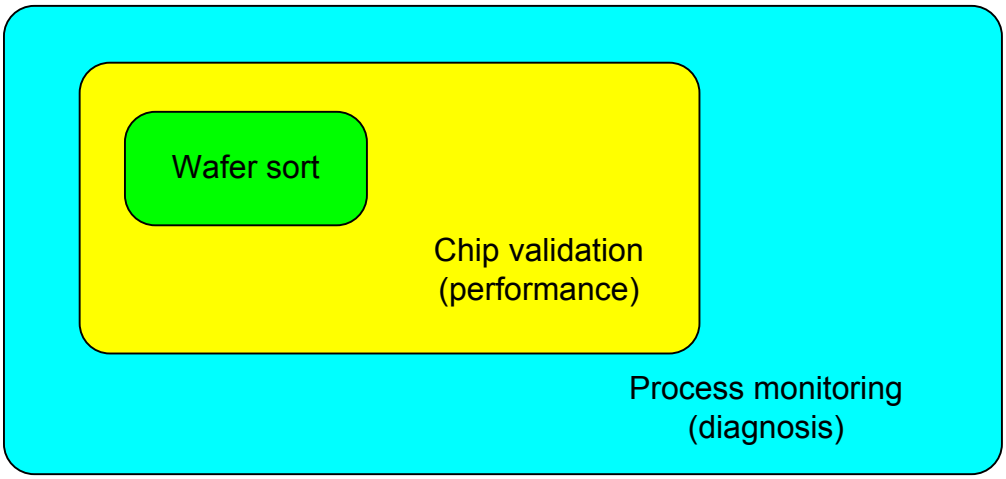


**Figure IV-1: The three main levels of test that are always performed on a CUT**

As shown in Figure IV-1, once the CUT passes the wafer sort, its performances need to be measured and compared to the required specifications. In the case the specifications are not met, a diagnosis process starts.

Both the chip validation and the diagnosis are carried out externally, with expensive equipments and slow procedures, causing loss of time and money.

Moreover, a lot of effort is spent in the debugging of the measurements.

If those tests could be performed on-chip, a money-saving and a better precision could be obtained, as in the case for an on-chip wafer test.

What has to be performed is now a functional test, which is, as explained in the first chapter, more complicated than a structural test. The circuits needed for this aim are more “area and power hungry” compared to those used for a structural test.

The main performances that need to be measured on a VCO are:

- Consumption

- Frequency of oscillation
- Conversion gain $K_{vco}$
- Phase noise

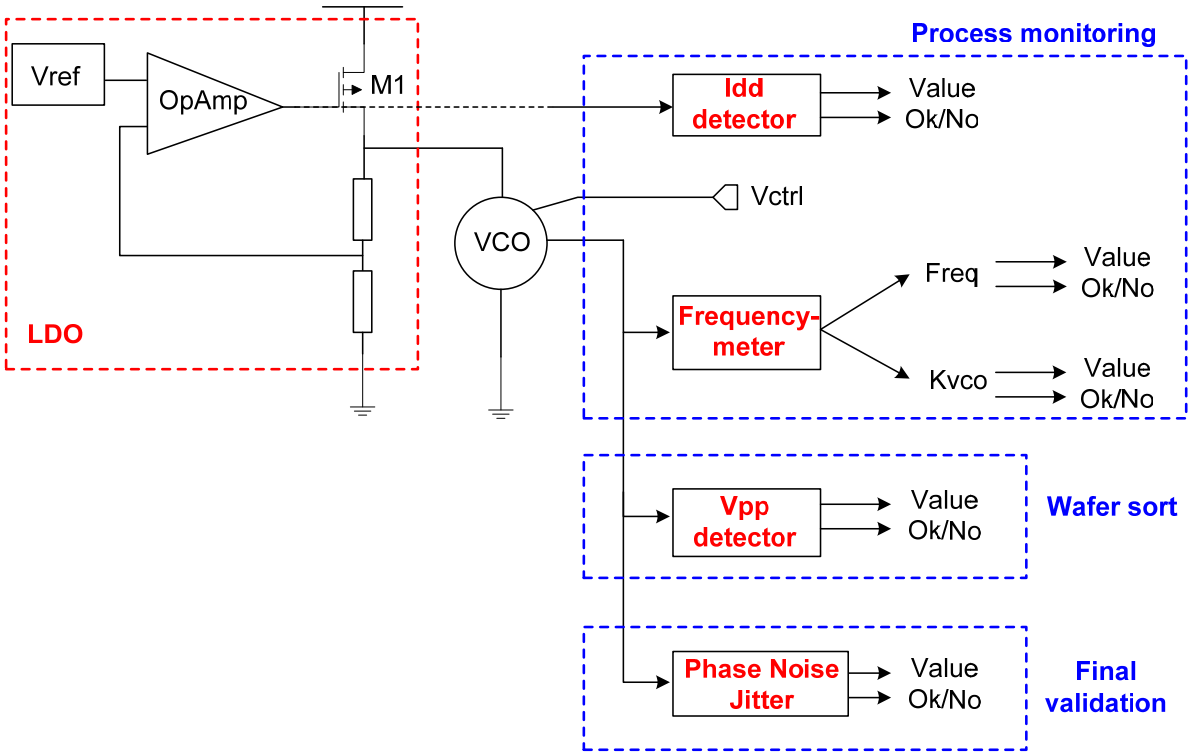


**Figure IV-2: Block scheme representing the complete on-chip characterization of the CUT**

The block scheme depicted in Figure IV-2 shows the implementation of the complete on-chip characterization and diagnosis of the VCO.

The VCO is still powered by an LDO. The current flowing through pMOS M1 can be copied with a current mirror or some different kind of current sensor. The current consumption of the VCO would then be known. The value could also be compared to the expected value in order to have a pass/fail information.

A frequency-meter can be connected to the VCO output in order to measure on-chip the frequency of oscillation of the CUT. The circuit needed for this aim is the subject of the next section.
If the frequency of oscillation is measured for different values of $V_{ctrl}$, the conversion gain $K_{vco}$ of the CUT can be determined.

The peak-to-peak detector is used for the wafer sort, as explained throughout this work.

Finally, a way to measure on-chip the phase noise (jitter) should be investigated.

With all of that information extracted from the VCO, in case of a malfunctioning, some diagnosis can be made.
The main idea to localize the eventual problem follows:

- If the *problem comes from the tank LC*, the main impact will be a shift of the oscillating frequency. The frequency-meter can measure the frequency of the output signal and compare it with a golden value. If the problem comes from the tank, an error signal can be output by the frequency-meter.
- If the *problem comes from the active part* of the VCO, the main impact will be a change in the transconductance of the transistors, and a consequent change in the current consumption of the CUT. The current detector can measure the current consumed by the VCO, compare it to a golden value and output an error signal in the case the measured value is not the expected one.

The next section will focus on the on-chip measurement of the frequency of oscillation of the VCO.
Two main strategies exist: Frequency-to-Voltage Converters (FVC) or Time-to-Digital Converters (TDC).
Both techniques, already introduced in Chapter 1, are now described in greater detail, trying to point out the pros and cons of each, in terms of complexity and capability to measure high-frequency signals with good precision.

The value of the oscillating frequency to be measured is chosen to be half of the oscillating frequency of the VCO presented in the previous chapter.
Two reasons lead to this choice:

- A divide-by-two frequency divider will surely be present in any PLL structure in which the VCO may be incorporated.
- The lower consumption of the frequency-meter.

### *IV.1.1 FVC for on-chip frequency measurement*

The frequency is converted to a voltage through the integration of the signal and the capacitors charge redistribution principle [Dje01].

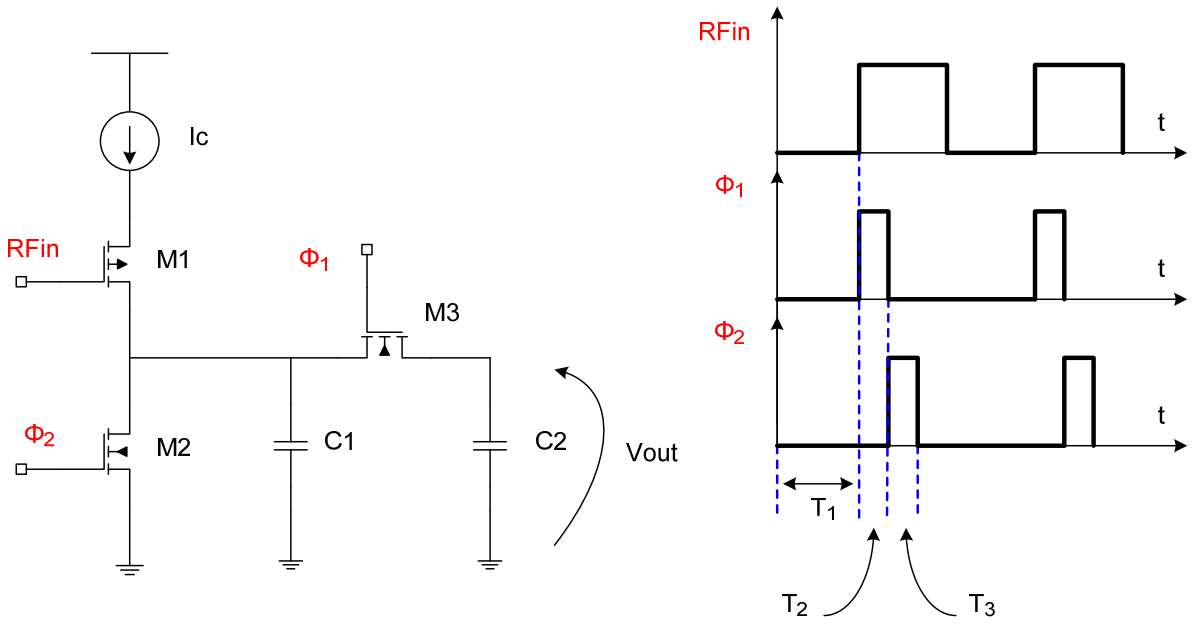


**Figure IV-3: Simplified scheme for the FVC and time diagram associated with it**

In Figure IV-3 the simplified circuit of a FVC is presented, together with the time diagram of the signals needed for its proper functioning.

During the time interval $T_1$, pMOS M1 is on and charges C1 with the current $I_C$. M2 and M3 are now off.

Capacitor C1 charges to the final value of:

$$V_{C1} = \frac{1}{C1}\int_0^{T_1} I_C(t)dt = \frac{I_C \cdot T_1}{C_1} = \frac{I_C}{C_1}\cdot\frac{T}{2} \qquad (1)$$

where T is the period of the input signal whose frequency has to be measured.

As soon as $RF_{in}$ goes high, signal $\Phi_1$ goes high. M1 and M2 are now off, while M3 is on. During the time interval $T_2$, charge redistribution between C1 and C2 takes place.

During the final step ($T_3$), only transistor M2 is on, discharging C1.

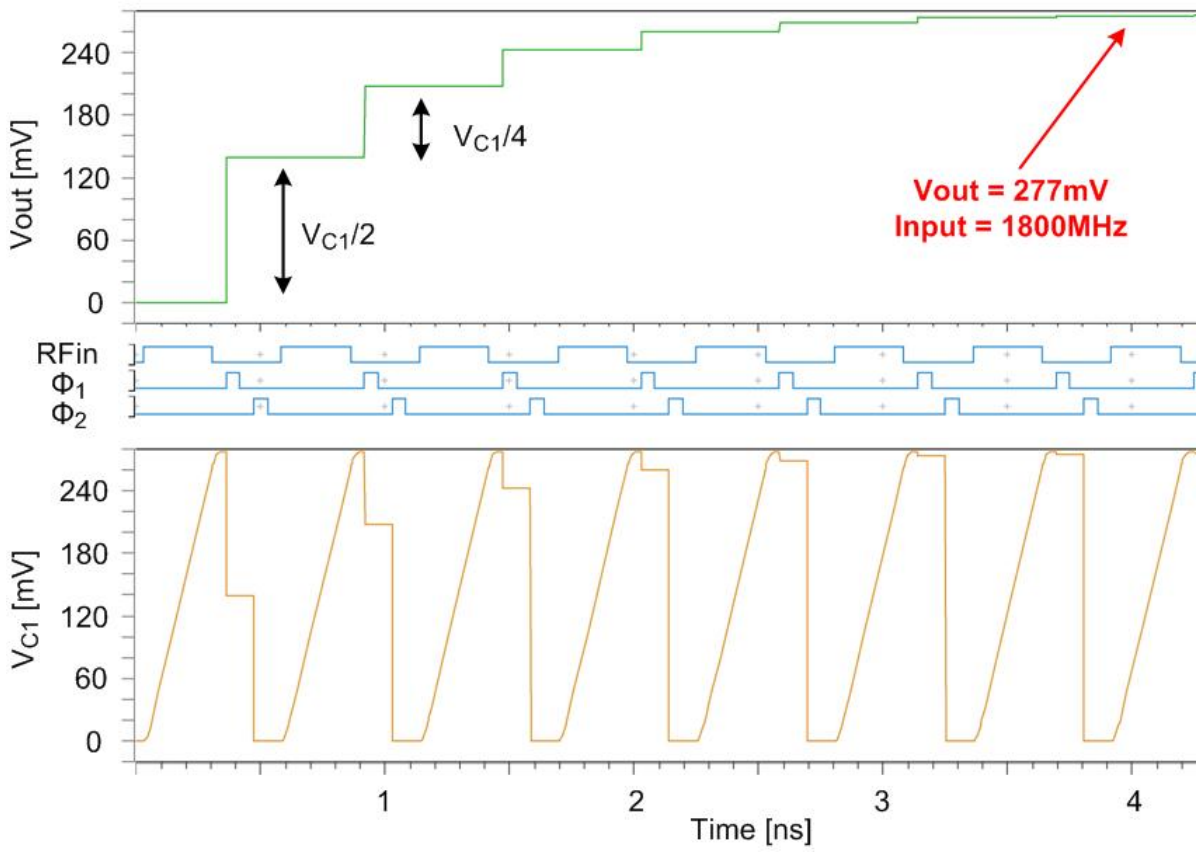


**Figure IV-4: VHDL-AMS simulation of the FVC with RF signal @ 1800MHz (duty cycle = 0.5)**

If capacitors C1 and C2 are equal, the output voltage Vout increases by the half of $V_{C1}$ after the first cycle, by the quarter of $V_{C1}$ after the second cycle, by the eight of $V_{C1}$ after the third cycle, and so on and so forth. It can be shown that after 8 cycles of the input signal, the error between Vout and $V_{C1}$ is approximately 0.4%.

The output voltage is then inversely proportional to the frequency of the input signal.

In Figure IV-4 the result of a VHDL-AMS simulation of the FVC is presented. The input signal (RFin) is a square wave oscillating at 1800MHz. The switches and the capacitors are ideal.

The values used for the simulation are: Ic = 1mA, C1=C2=1pF.

From Equation 1 the ideal final value for Vout should be 278mV. The value reached by Vout after 7 cycles is approximately 277mV.

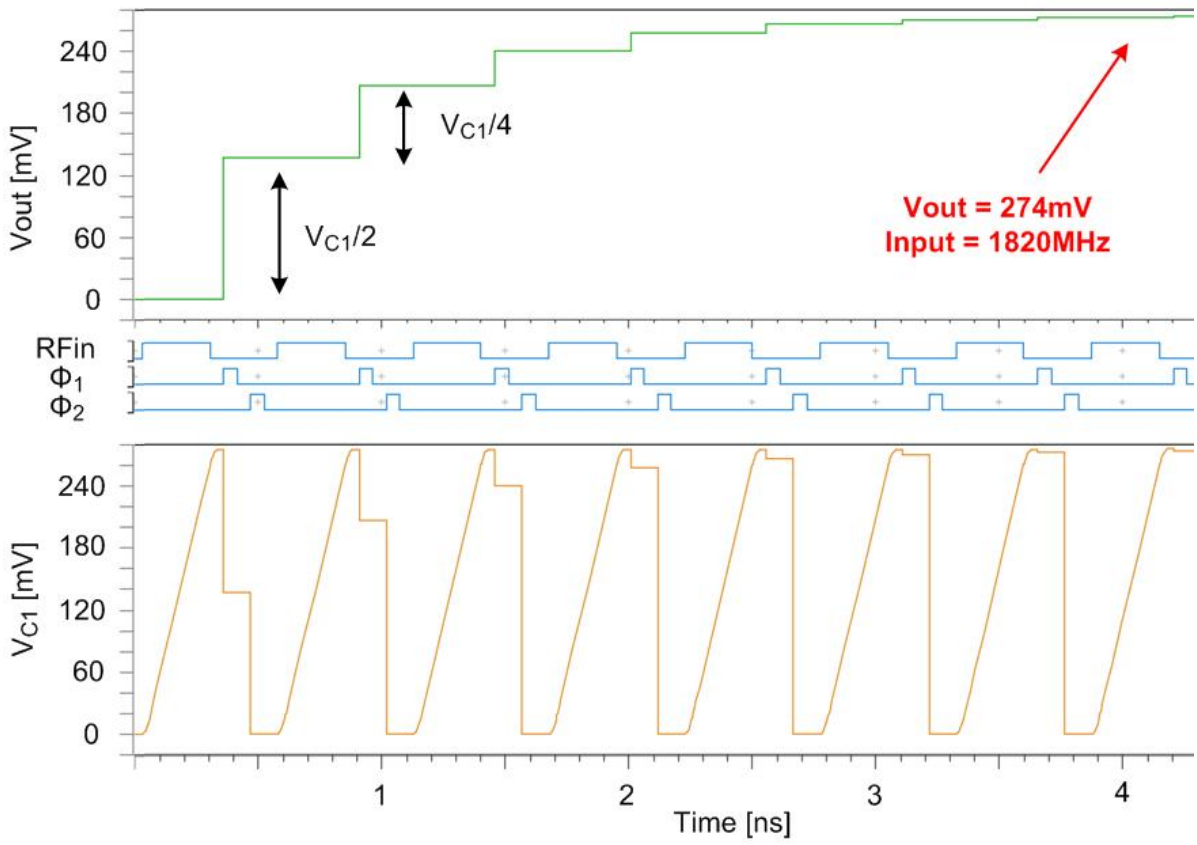


**Figure IV-5: VHDL-AMS simulation of the FVC with RF signal @ 1820MHz (duty cycle = 0.5)**

The same simulation is carried out with an input signal oscillating at 1820MHz.

The result is presented in Figure IV-5. As expected from Equation 1, the output voltage changes by only 3mV for a 20MHz frequency-shift.

This example highlights the first problem of FVCs: when the input signal oscillates at high frequency, a non-negligible frequency shift translates in a negligible change in the output voltage.

In order then to evaluate the FVC using non-ideal capacitors, a 25kΩ resistor is added in parallel to both C1 and C2 to introduce a leakage current of roughly 10µA.

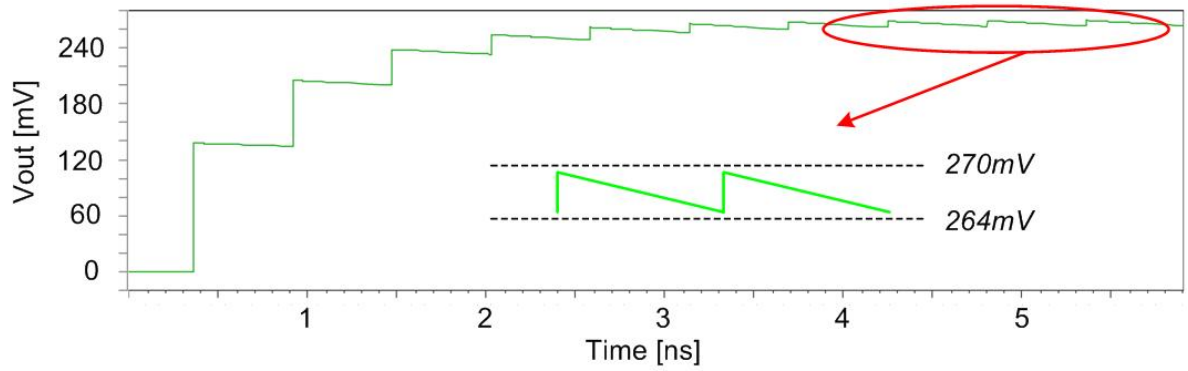


**Figure IV-6: VHDL-AMS simulation of the FVC with 10µA leakage current for each capacitor**

The result of the simulation, presented in Figure IV-6, shows that the output voltage cannot reach the expected 278mV; its value is more than 10mV lower than the ideal one.
To rely on the charge and discharge of capacitors for the measurement of the frequency does not grant a high precision.

In conclusion, the FVC solution is not suitable for the measurement of high-frequency signals because of two main reasons:

- A high-frequency shift does not affect enough the output voltage.
- Leakage current of the capacitors negatively impacts the accuracy of the output.
- The need for two narrow non-overlapping pulses ($\Phi_1$ and $\Phi_2$) that must occur within half a period of the input signal.

The first and second problems limit the accuracy of the final value of $V_{C1}$.
The third sets up an upper limit to the input frequency, because the generation of $\Phi_1$ and $\Phi_2$ is non-trivial. In fact, for an input at 3.6GHz, the non-overlapping signals $\Phi_1$ and $\Phi_2$ need to be generated in a time interval of approximately 139ps. This means that a rise and fall time in the order of 20ps would be too high and would negatively impact the final result.

The FVC can also be conceived to use only true single-phase clocking (TSPC), eliminating the problem of the generation of $\Phi_1$ and $\Phi_2$.
This solution [Bui08] combines the first two phases of the previous method.

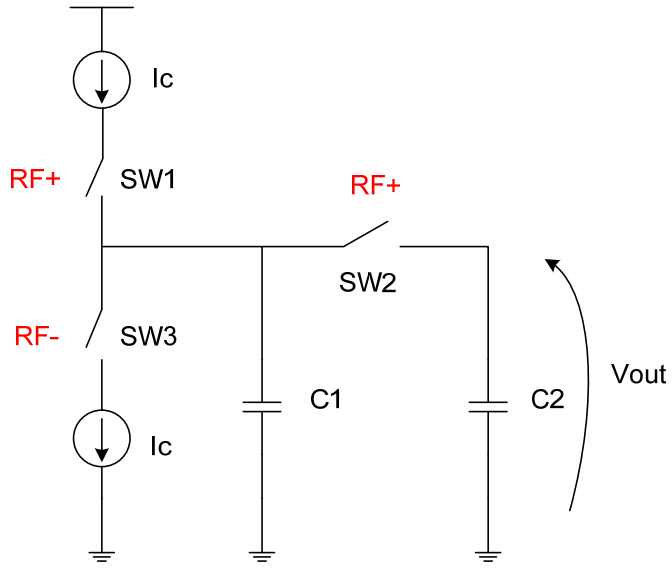


**Figure IV-7: FVC conceived to use a true single-phase clock**

The TSPC FVC is presented in Figure IV-7. During the first half of the input signal, switches SW1 and SW2 are on and capacitors C1 and C2 are charged simultaneously. During the second half of the input signal, only C1 is discharged. When the new cycle starts again, at the beginning of the new integration phase, the charge on C2 is redistributed between both capacitors.

Calling $C_{tot}$ the sum C1+C2 and T the period of the input signal, the output voltage after the first redistribution of charge becomes:

$$V_{out} = \frac{I_C \cdot T}{2C_{tot}} \cdot \frac{C_2}{C_{tot}} \qquad (2)$$

During charge sharing, the output voltage drops; this effect can be minimized by making C2 larger than C1.

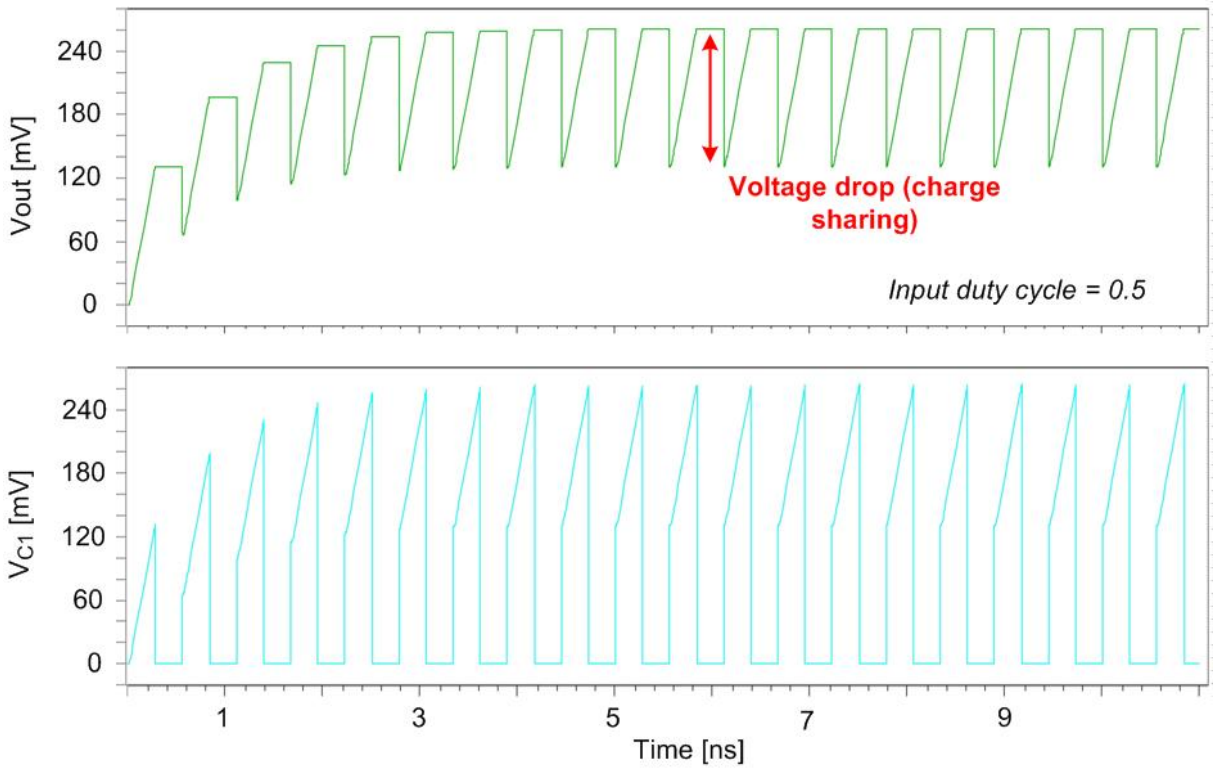


**Figure IV-8: VHDL-AMS simulation of the TSPC FVC with RF signal @ 1800MHz (duty cycle = 0.5)**

In Figure IV-8 the result of a VHDL-AMS simulation for the TSPC FVC is shown, for an input square wave oscillating at 1800MHz. The values used for the simulation are Ic=1mA, C1=C2=1pF.

As predicted, since the two capacitors are equal, the charge sharing causes a voltage drop equal to half of the final value of Vout.

A final problem is that the FVC is highly dependent on the duty-cycle of the input signal.

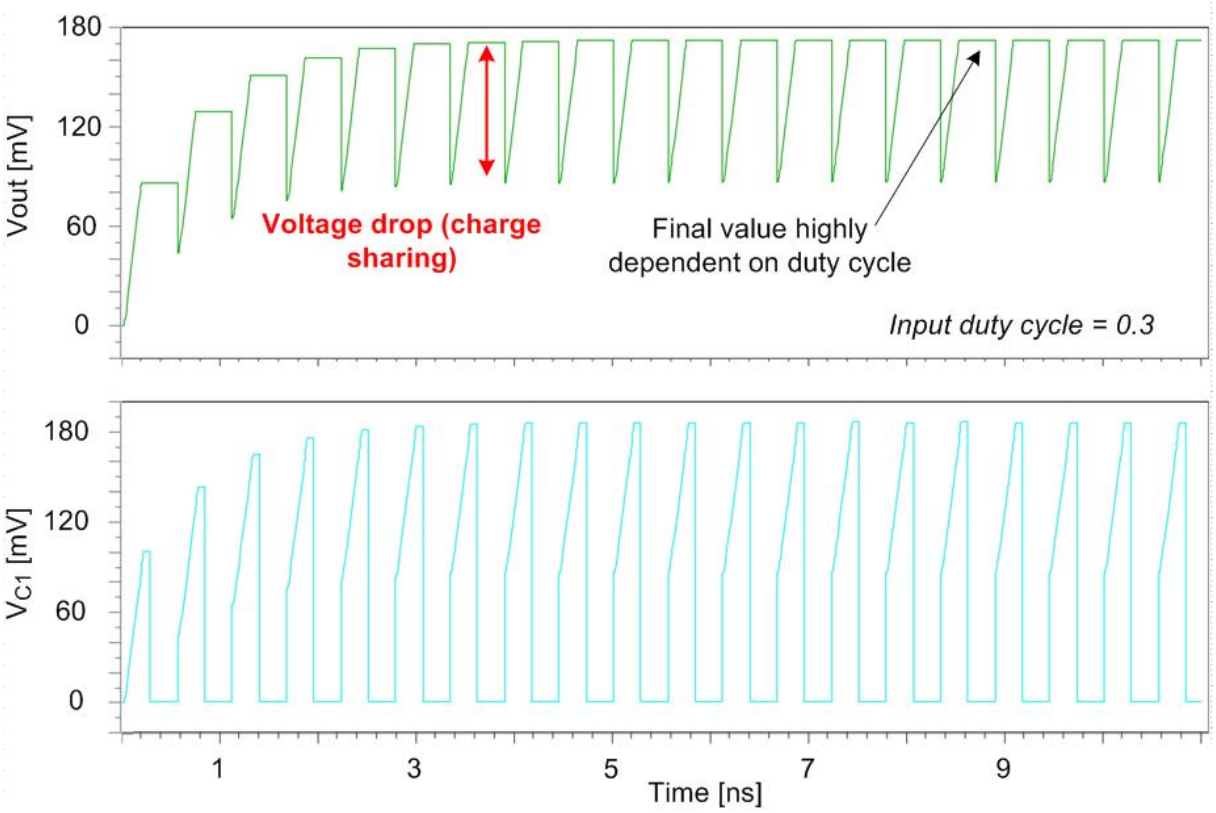


**Figure IV-9: VHDL-AMS simulation of the TSPC FVC with input frequency @ 1800MHz (duty cycle = 0.3)**

In Figure IV-9 the VHDL-AMS simulation of the same TSPC FVC shown in Figure IV-7 is presented, with the only difference that the input signal is now a square wave with a duty cycle = 0.3.

Comparing this simulation with the results obtained in Figure IV-8, it can be noticed that the final value of Vout has changed.

It can be also noticed that the ratio of the final values for Vout corresponds to the ratio of the duty cycles.

The FVC solution for the measurement of the oscillating frequency of RF signals is not appropriate. While appealing for its simplicity and its all-analog nature, the error in the measurement is too high.

### *IV.1.2 TDC for on-chip frequency measurement*

The main principle of operation of the TDC was introduced in Chapter 1 and is not repeated in greater detail.

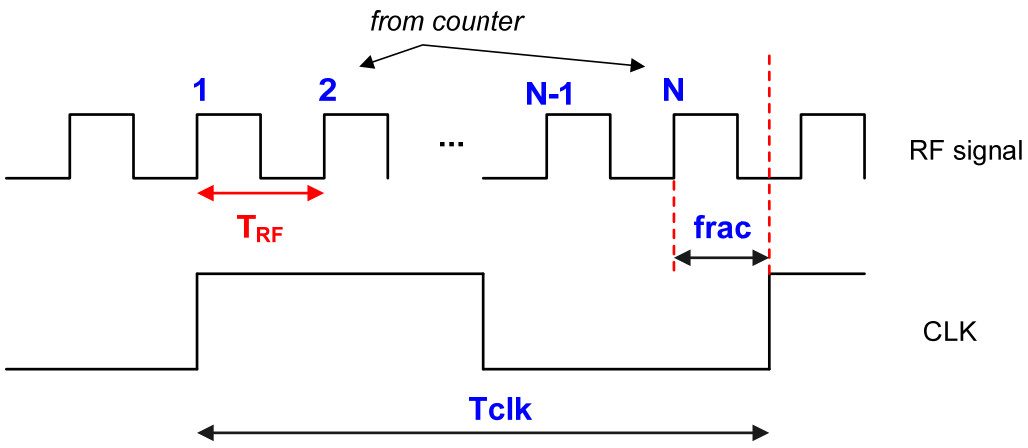


**Figure IV-10: Measurement of the period of the RF signal through the measurement of an integer and a fractional part in the case of a RF-signal synchronized with the clock**

In Figure IV-10, the timing diagrams of the RF-signal (whose frequency has to be measured) and of the low frequency clock are shown.

A counter counts the number of rising edges of the RF-signal that pass during one clock period (in Figure IV-10 the last rising edge is the $N^{th}$). This is called the *integer part*.

Since the frequency of the RF signal is not a multiple of the clock frequency, the $N^{th}$ period of the RF signal is not complete before the arrival of the new rising edge of the clock. This non-complete period (called "frac" in Figure IV-10) represents the *fractional part*.

While the measure of the integer part only needs a counter able to count at the frequency of the input RF signal (high frequency → high counter consumption), the measure of the fractional part is much less trivial.

The method for the measurement of the time "*frac*" of Figure IV-10 relies on the use of a delay chain and D Flip-Flops (DFFs) to sample the delayed versions of the RF signal.

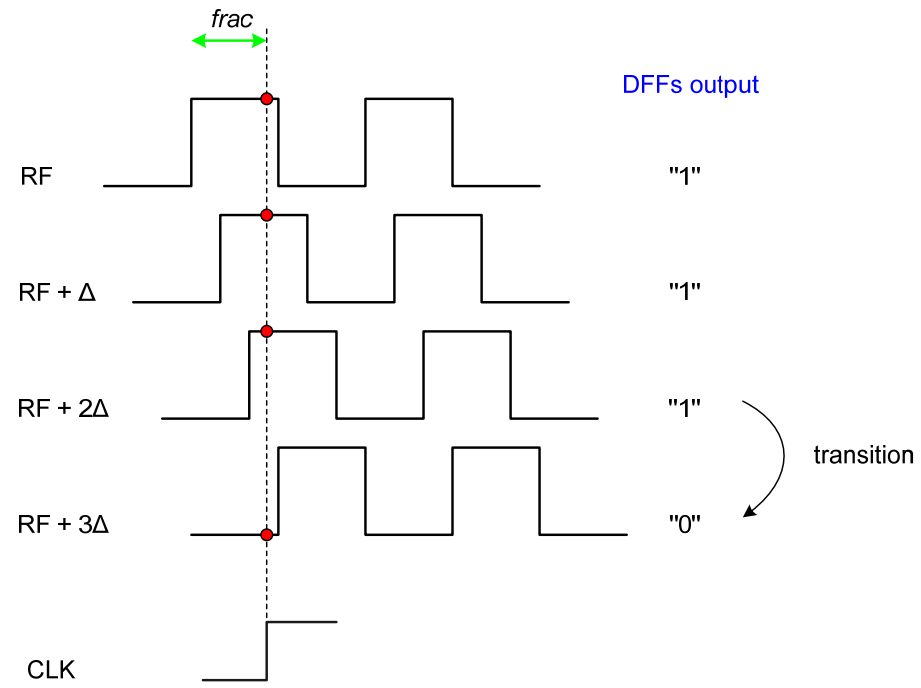


**Figure IV-11: Timing diagram explaining the measurement of the fractional part**

As shown in Figure IV-11, the RF-signal is delayed and when the clock goes high, the DFF samples its value. A thermometer code (as for ADCs) is generated and the first 1 → 0 transition identifies the value of "*frac*" as the number of the delay element at which the transition took place (number 3 in the figure) multiplied by the value of the delay Δ.

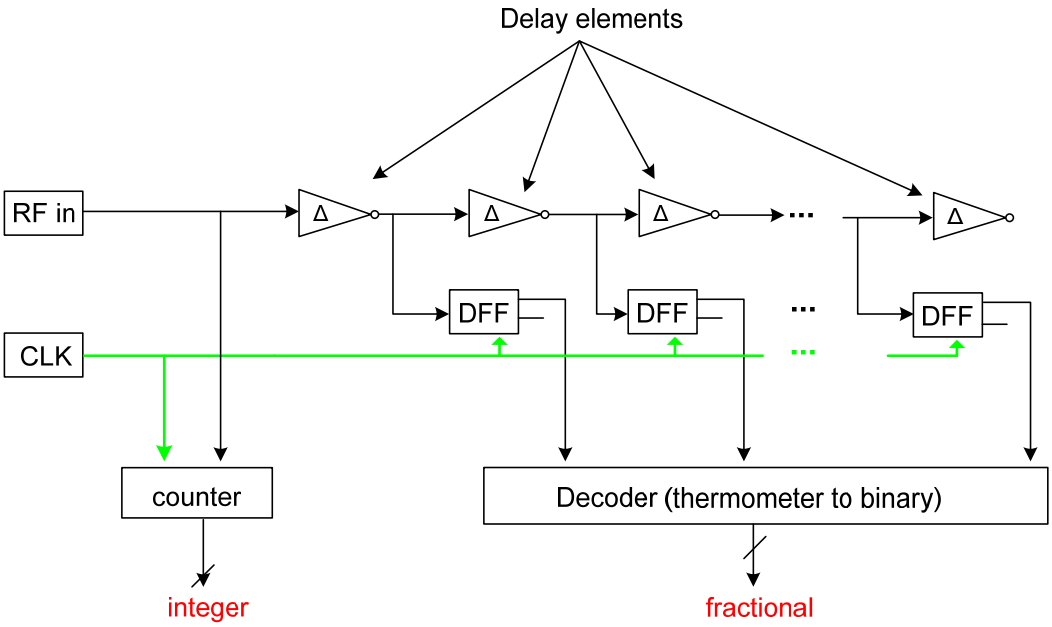


**Figure IV-12: Basic block scheme of the TDC, showing the methodology for the measure of the integer and fractional part of the RF input signal**

The block scheme of the basic TDC is shown in Figure IV-12; at each rising edge of the clock, an integer part and a fractional part are measured. The decoder finds the place in the delay chain at which the first 1 → 0 transition took place.

The lower the value of the delay element, the higher the accuracy in the measurement of the fractional part is.

Being the inverter propagation delay the finest logic-level regenerative timing method, inverters are used as delay elements [Sta06].

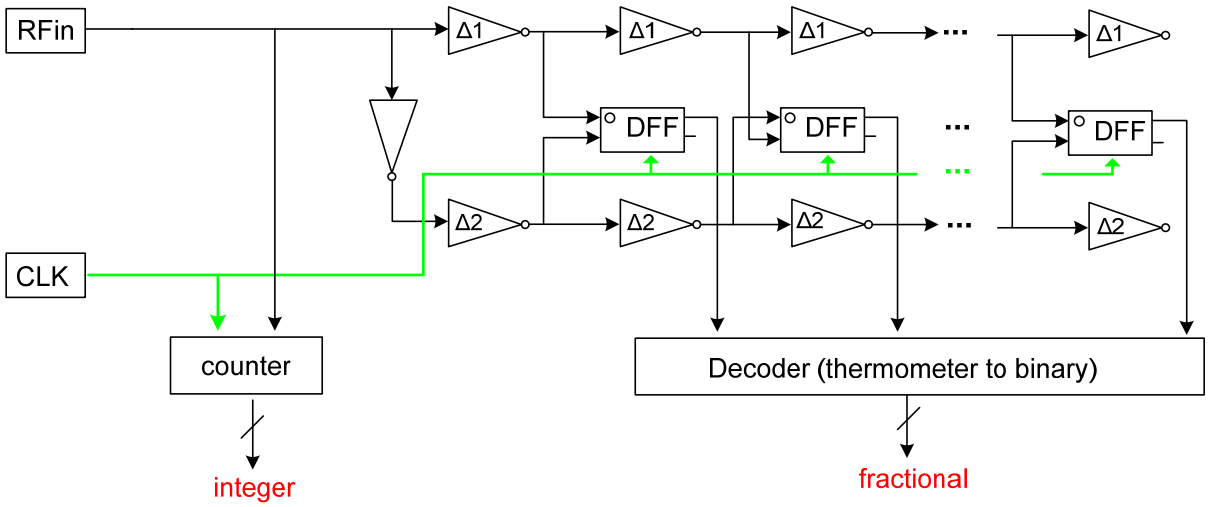


**Figure IV-13: TDC making use of two chains of delay elements to increase the accuracy of the fractional measurement [Sta06]**

The scheme depicted in Figure IV-13 is then used to exploit the fast propagation delay of the inverters. Each DFF is differential and the delay of the upper chain is identical to the delay of the lower chain.

Referring to the timing diagram in Figure IV-10, the expression giving the period of the RF-input signal can be found:

$$T_{RF} = \frac{T_{CLK} - frac}{N - 1} \tag{3}$$

Assuming that no error is made in the measurement of the integer part (N), if an error ε is made on the fractional part, we get:

$$\bar{T}_{RF} = \frac{T_{CLK} - (frac \pm \varepsilon)}{N - 1} = T_{RF} \pm \frac{\varepsilon}{N - 1} \tag{4}$$

From Equation 4 we infer that, if no constraints are given on the maximum time allowed for the measurement, it is possible to increase N (lower the clock frequency) to arbitrary decrease the error.

The equations slightly change in the case the RF-signal is not synchronized with the clock, as depicted in Figure IV-14.

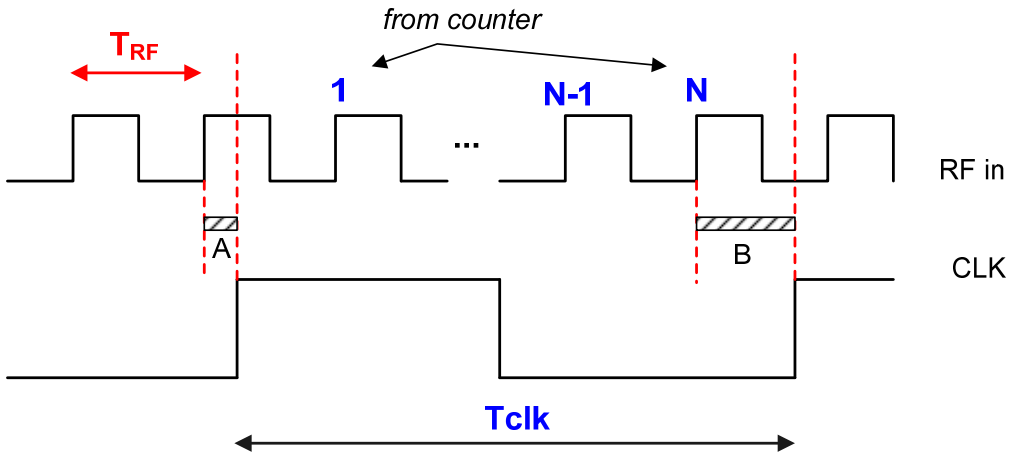


**Figure IV-14: Timing diagram in the case the RF signal and the clock are not synchronized (more realistic case)**

In this case the equation that holds is:

$$T_{RF} = \frac{T_{CLK} + A - B}{N} \quad (5)$$

Where *A* and *B* are two consecutive measurements of the fractional part.

If an error ε is now made on the fractional part, the error on the final measurement becomes:

$$\overline{T_{RF}} = T_{RF} \pm \frac{2\varepsilon}{N} \quad (6)$$

Considering that the maximal value of the error ε corresponds to one delay, a relationship can be established between precision and value of the single delay element.

The worst case happens for a small value of *N* (for the lowest measurable input frequency).

As an example, let's consider: $f_{RF}$=1600MHz, $f_{CLK}$=35MHz. The value of *N* is approximately 46.

If it is needed to discriminate between an input frequency of 1600MHz and another at 1602MHz, the error has to be smaller than 0.8ps (period difference).

This translates in ε < 18.4ps.

A high value for the delay implies:

- Lower consumption of the single delay element
- Lower number of delay cells and of DFFs → lower consumption and area of the TDC

Since no synchronization is present, the counter used for the measurement of the integer part never resets to zero when a new rising edge of clock arrives.

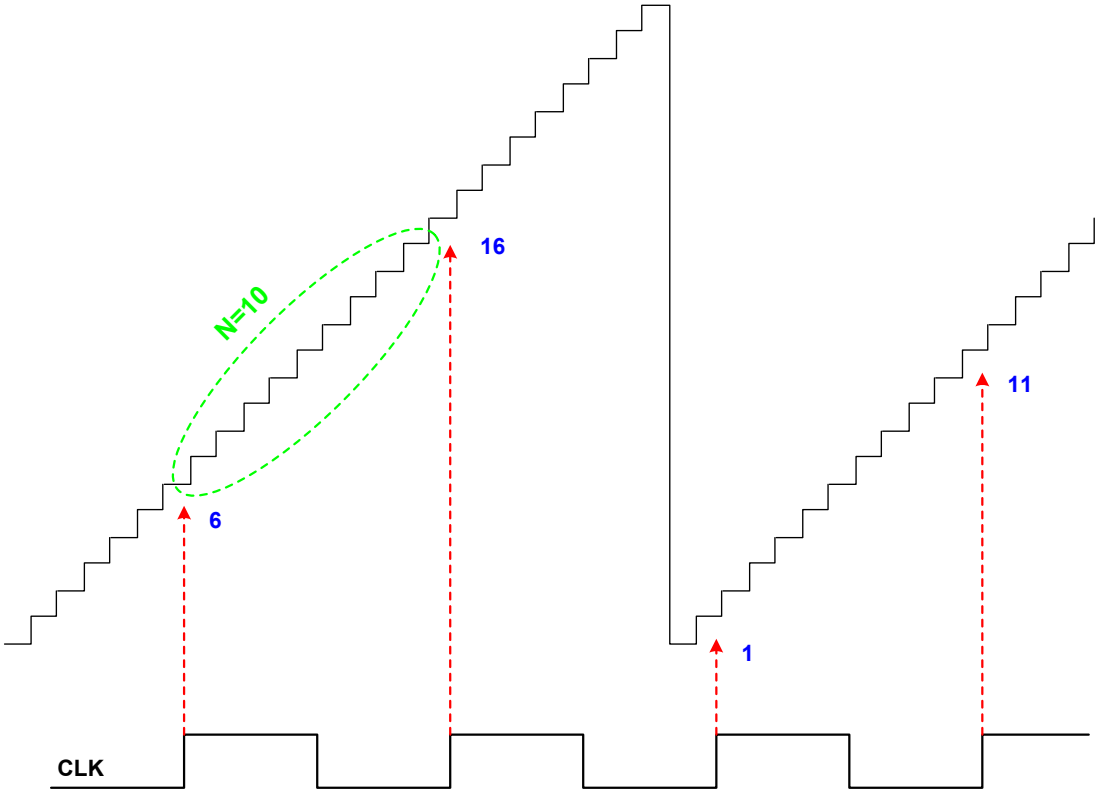


**Figure IV-15: Behavior of the counter that does not reset at each rising edge of the clock**

The behavior of the counter is presented in Figure IV-15. For each rising edge of the RF signal, the counter increases until it reaches its overflow and it starts all over again.

To have the information on the value of *N*, two consecutive values of the counter are needed (as it was the case for the fractional information).

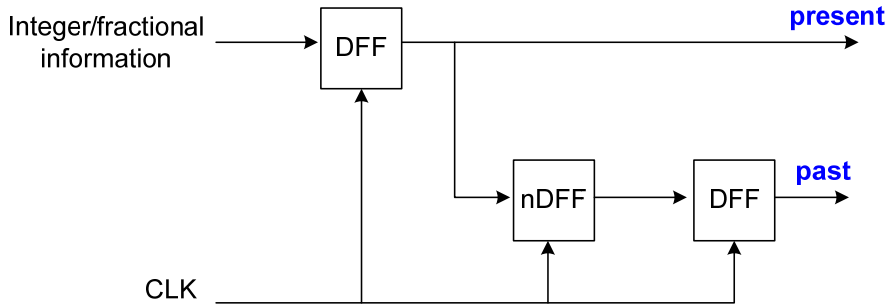


**Figure IV-16: Setup used to have both the past and present information on the fractional and integer parts**

The simple scheme depicted in Figure IV-16 is used to have both the past and present information on the values of the fractional and integer parts. Using a DFF active on the high level of the clock and a DFF active on the low level of the clock (nDFF), the information is delayed by one clock period.

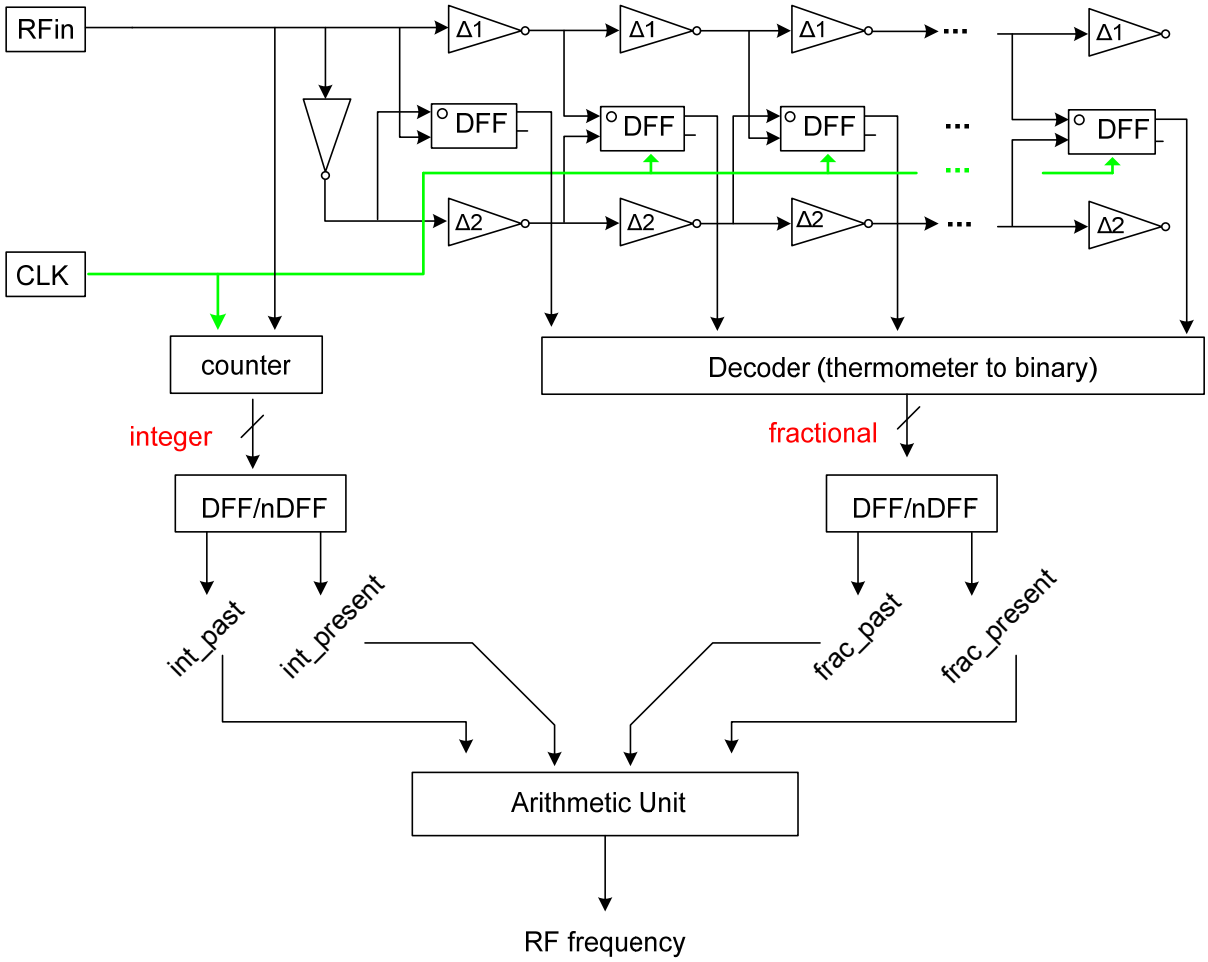


**Figure IV-17: The complete block scheme for the TDC**

The complete structure of the TDC is represented in Figure IV-17. The arithmetic unit performs Equation 5.

### *IV.1.3 TDC – validation of the structure*

The very high number of blocks makes the simulation of the TDC at the transistor level impossible. The time needed for a transient simulation would be too long.

For this reason the VHDL-AMS simulation is preferred.

Each block in Figure IV-17 is described at a behavioral level.

The first thing to do is to understand how small the delay element can be, using the CMOS 65nm technology.

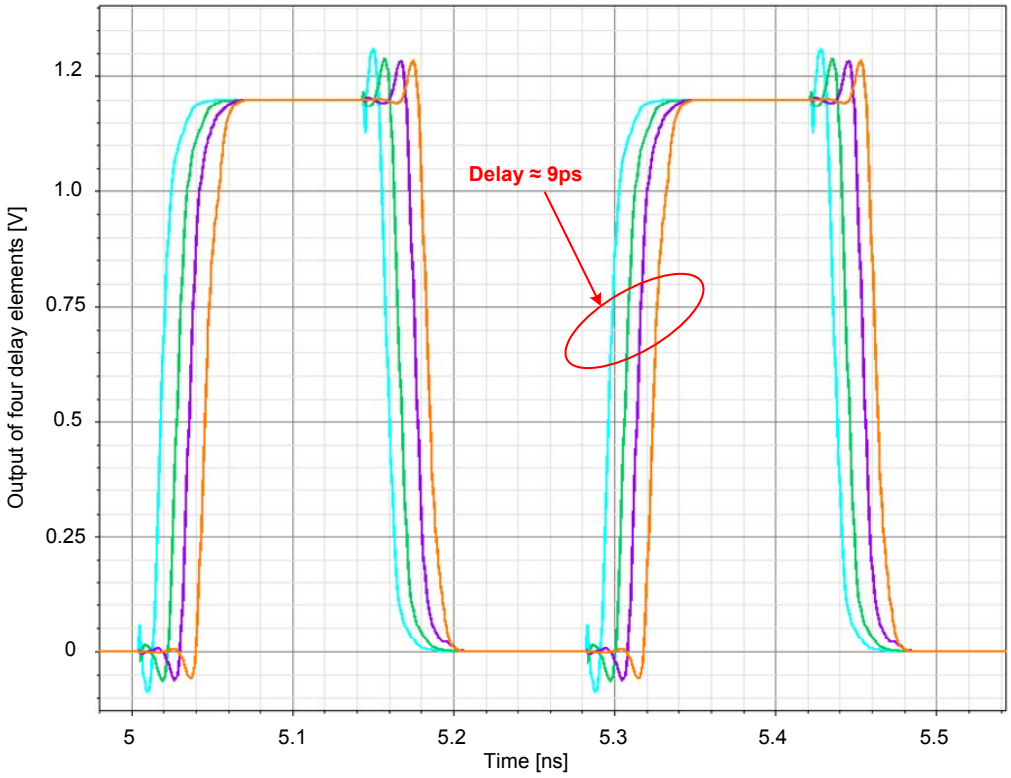


**Figure IV-18: Output of four consecutive delay elements**

If simple inverters are used, the delay can be as low as 9ps, as shown in Figure IV-18.

In order to have relaxed constraints, it is decided to fix the delay of each element at 12ps.

The complete delay chain must create a total delay equal to the period of the RF input signal.

The number of delay elements fixes then the *minimum* correctly measurable frequency.

Considering an input signal at 1600MHz, 52 delay elements are needed.

Then, the number of bits of the counter is chosen taking into account the *maximal* frequency that has to be correctly measured and the frequency of the clock.

The frequency of the clock is fixed at 35MHz.

If a maximal frequency of 2000MHz has to be measured, the maximal value that *N* (the integer part) can attain is 57. A 6-bit counter is needed.

In order to validate the principle and the structure, the system depicted in Figure IV-17 is simulated for different frequencies of the RF input signal.

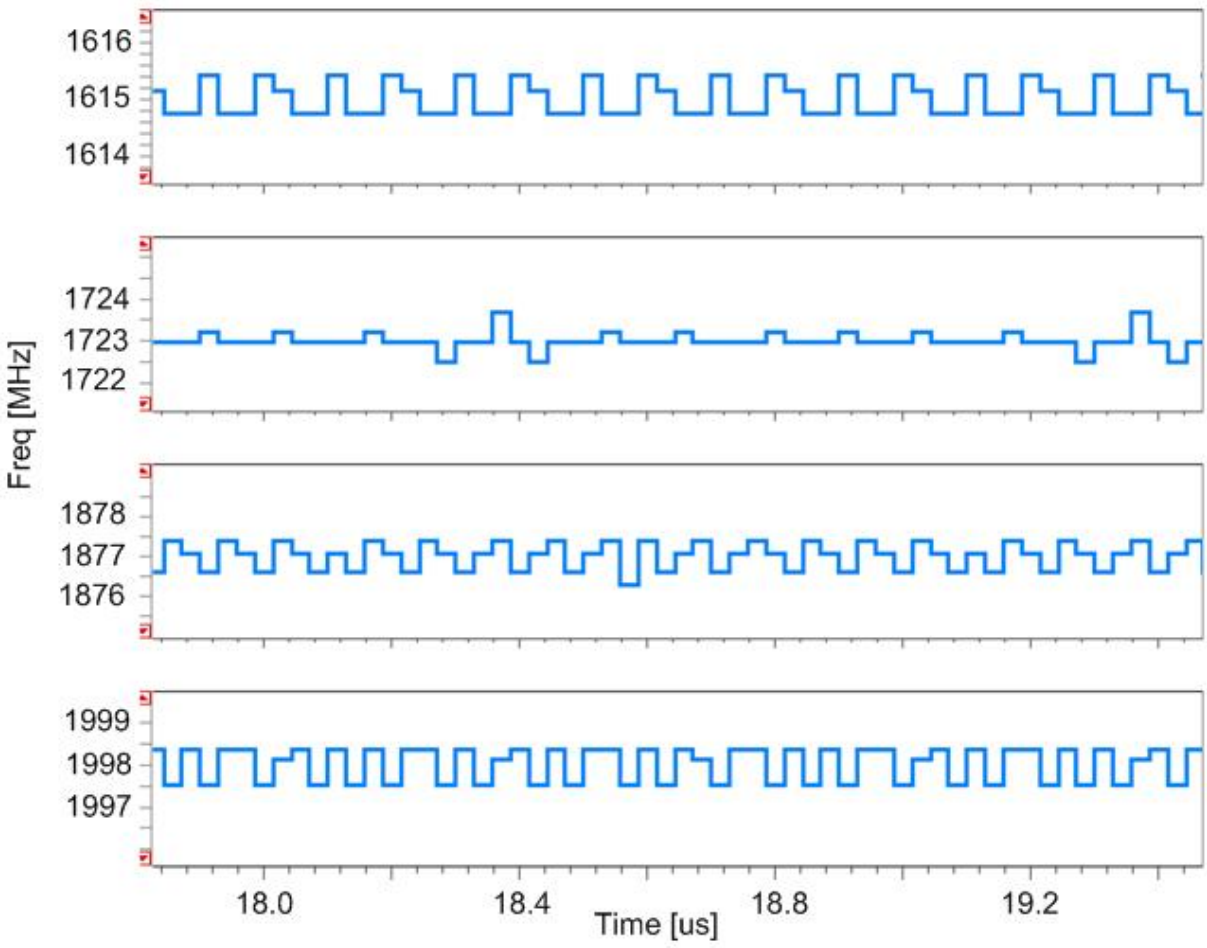


**Figure IV-19: Output of the TDC for different values of the frequency of the input signal**

In Figure IV-19 the output of the TDC is presented for different values of the input frequency: 1615MHz, 1723MHz, 1877MHz, and 1998MHz. The high precision (≈1MHz) of the system is demonstrated.

The TDC seems then a better candidate, compared to the FVC, to become the frequency-meter needed for the complete on-chip characterization of the VCO.

In order then to evaluate the robustness of the system, two scenarios are simulated:

- Non-null propagation time from the output of each inverter to the DFF
- Mismatch of the inverters

*IV.1.4 TDC – simulation of non idealities: propagation time*

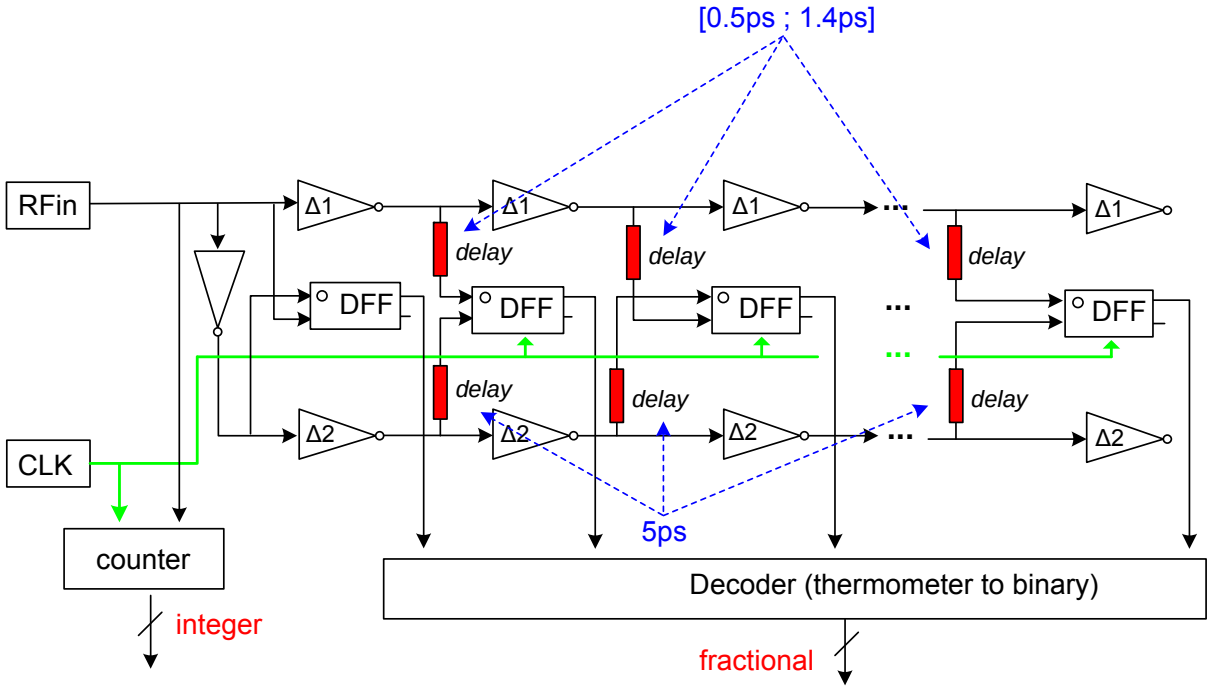


**Figure IV-20: Introduction of a non-null propagation time of the signal from the output of each inverter to the DFF**

In Figure IV-20 the core of the TDC is shown, with the introduction of small delays to take into account a non-null propagation delay from the output of each inverter to the input of each DFF.

The propagation delays after the "upper" inverter chain have increasing values starting from 0.5ps going to 1.4ps; the propagation delays after the "lower" chain have the constant value of 5ps.

This choice was made because equal delay times on both chains would have given no insight on eventual problems caused by those delays.

During this first analysis, no propagation delay is introduced before the first DFF, as can be seen from Figure IV-20.

Multiple simulations were performed, for different values of the input frequency. No noteworthy difference compared to the ideal case was found.

The impact of the propagation delay becomes visible when a delay is introduced before the first DFF.

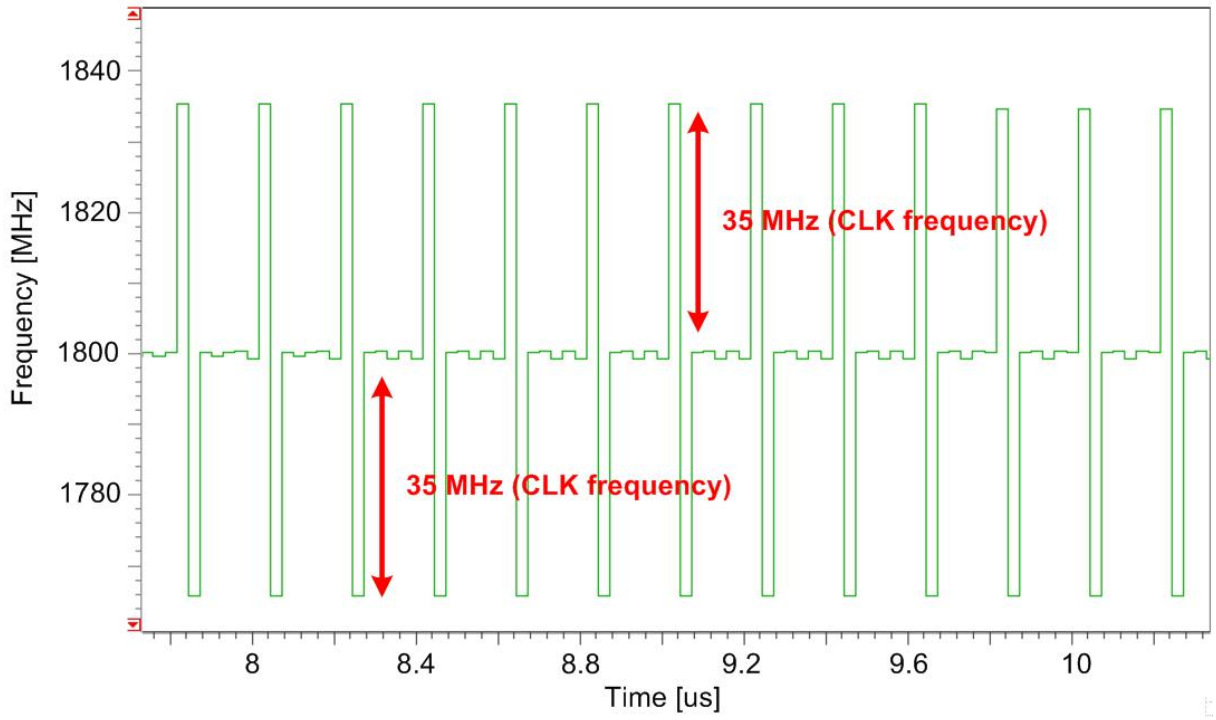


**Figure IV-21: Output of the TDC when the RF signal does not arrive at the first DFF and at the counter at the same time**

This phenomenon is shown in Figure IV-21. A propagation delay is introduced before the first DFF. The output presents a systematic error of exactly ±35MHz (the clock frequency).

This error is due to a different arrival time of the input RF signal at the counter and at the first DFF.

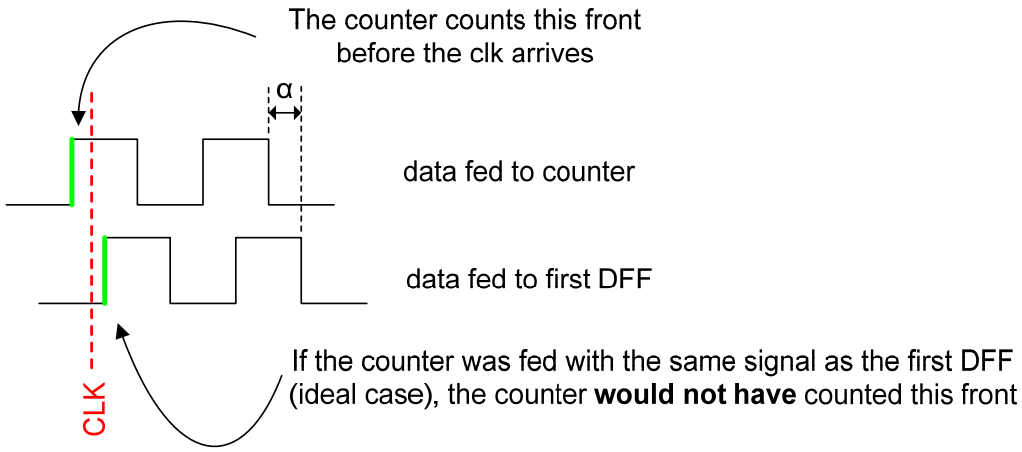


**Figure IV-22: Explanation of the ±35MHz error when a delay α is introduced before the first DFF**

The explanation of the error is given in Figure IV-22. Let's assume that the RF input signal arrives at the first DFF with a delay α compared to the arrival time to the counter. The rising edge of the clock arrives at the same time at the DFF and at the counter.

In the situation depicted in Figure IV-22, the counter has already counted an extra front of the RF-signal. This front would not have been counted if the signal fed to the counter was the same as the signal fed to the DFF. The value of *N* (the integer part) is *in excess* of one unit.

From Equation 5 we find:

$$f_{RF} = \frac{N}{T_{CLK} + A - B} \tag{7}$$

In the case an extra integer is counted, we have:

$$\overline{f_{RF}} = \frac{N+1}{T_{CLK} + A - B} = f_{RF} + \frac{1}{T_{CLK} + A - B} \approx f_{RF} + \frac{1}{T_{CLK}} = f_{RF} + f_{CLK} \tag{8}$$

Where the assumption that $T_{CLK}$ (≈28ns) is much greater than the term *(A-B)*, where A and B (the fractional part) can at most reach the value $T_{RF}$ (555ps for an 1800MHz input signal).

From Equation 8 it is possible to understand that an error on the integer count reflects at the output as an error whose value is the clock oscillating frequency.

#### *IV.1.4.1 Correction of the error introduced by the propagation delay*

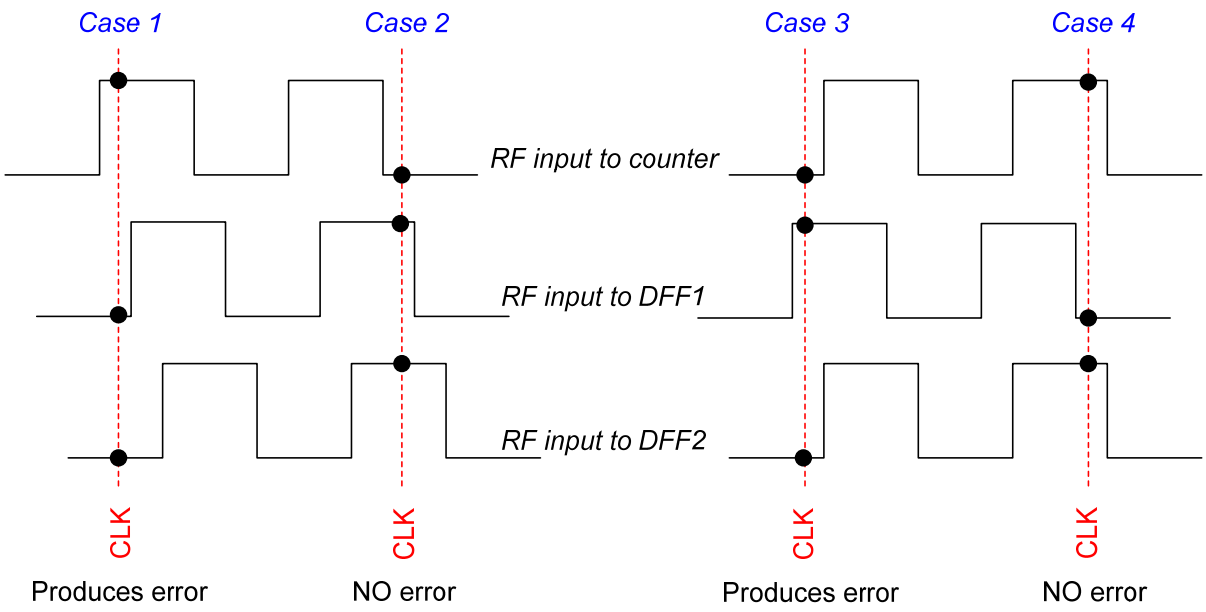


**Figure IV-23: Possible cases found when the RF input does not arrive at the same time at the counter and at the first DFF**

In Figure IV-23 four cases are depicted: in Case1 and Case2 the RF input arrives at the counter before arriving at the first DFF; in Case3 and Case4 the RF input arrives at the first DF before arriving at the counter.

Case2 and Case4 do not cause any error in the measurement of the input frequency, because they happen close to the *falling edge* of the RF signal (the counter counts the *rising edge* of the RF signal).

Case1 and Case3, on the other hand, produce an error in the measurement of the input frequency.
In Case1 the integer part is *in excess* of a unity, while in Case3 the integer part is *in deficit* of a unit.
In order to identify those four configurations, if only the signals fed to the counter and to the first DFF are monitored (this is done sampling the signals at the rising edge of the clock), no distinction could be made between Case1 and Case4, or between Case2 and Case3.
To be able to clearly identify the four cases, the signal fed to the second DFF has to be sampled and monitored too.

Let's call *int* the signal found sampling the RF input before the counter, *d1* the signal after sampling the RF input before the first DFF and *d2* the signal after sampling the RF input before the second DFF.
Let's call *check1* the identification of Case1 and *check2* the identification of Case3.
The algorithm needed to identify the problem becomes:

if (*int*=1 AND *d1*=0 AND *d2*=0)
    then *check1*=1 ; *check2*=0
elseif (*int*=0 AND *d1*=1 AND *d2*=0)
    then *check1*=0 ; *check2*=1
else
    *check1*=0 ; *check2*=0

Then the algorithm needed to correct the integer part is:

if (*check1*=1 AND *check2*=0)
then N=N-1
elseif (*check1*=0 AND *check2*=1)
then N=N+1

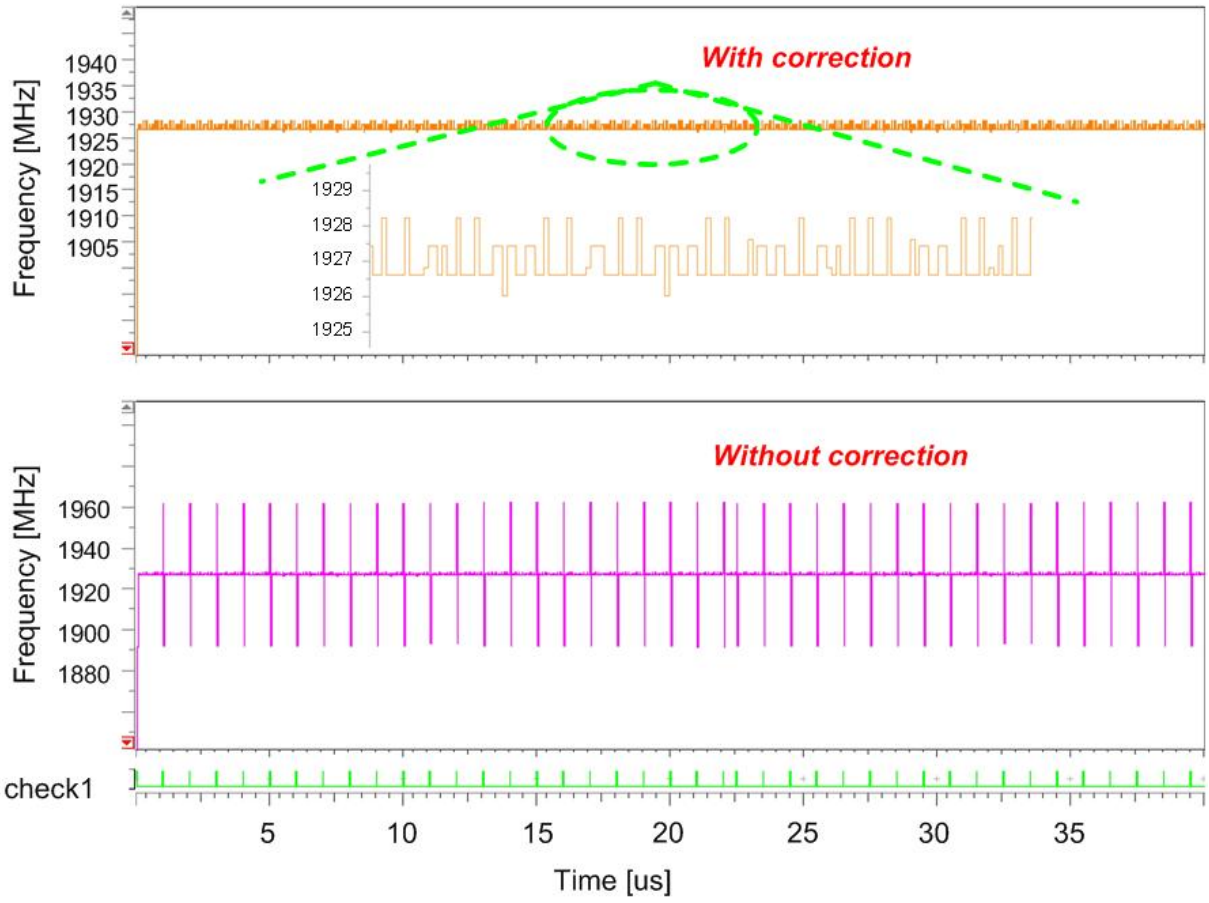


**Figure IV-24: Simulation showing that the errors are detected and corrected**

The effectiveness of the proposed algorithm to detect and correct the possible problems caused by the different arrival time of the RF input at the counter and at the first DFF is presented in Figure IV-24. The middle trace shows the measured frequency (input @ 1927MHz) and the ±35MHz errors made. The upper trace shows the measured frequency after the introduction of the corrective algorithm. The errors are eliminated.

### *IV.1.5 TDC – simulation of non idealities: mismatch of the inverters*

In order to simulate the effect of possible mismatch of the inverters, the upper inverter chain is described as shown in Figure IV-25. The delay introduced by the inverters increases from 10.8ps to 13.2ps (±10% of the ideal value). The choice to have increasing delay times respects the physical behavior of the circuit, affected by the complex routing of the blocks.

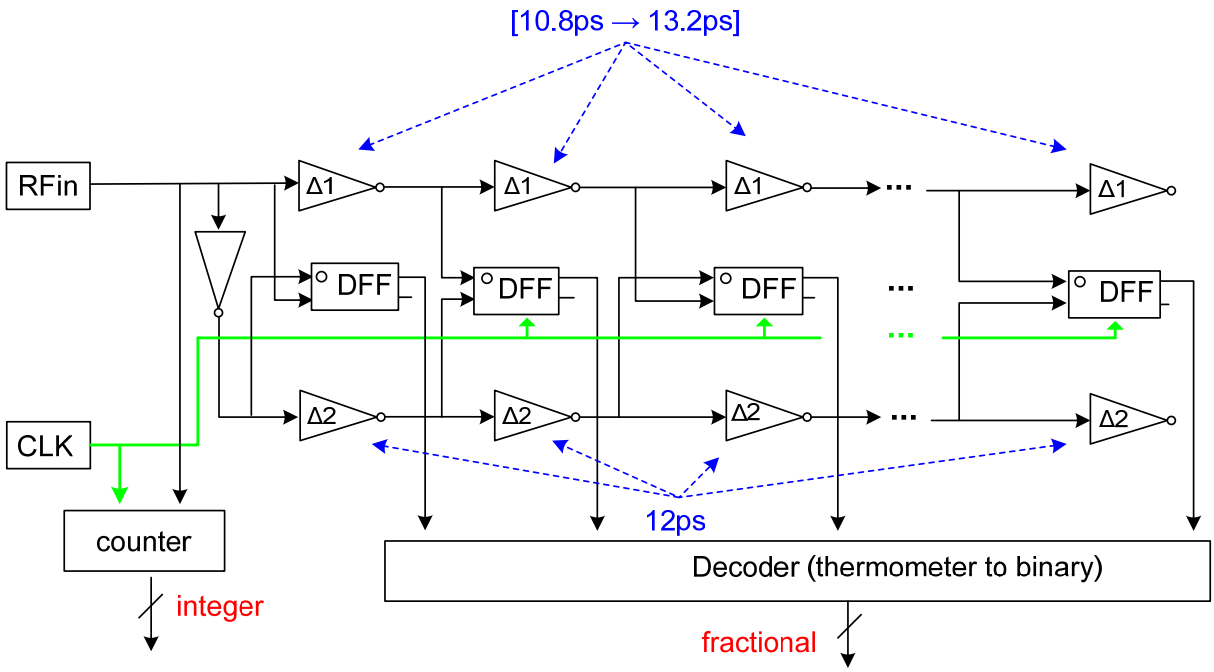


**Figure IV-25: Insertion of mismatch in the upper inverter chain**

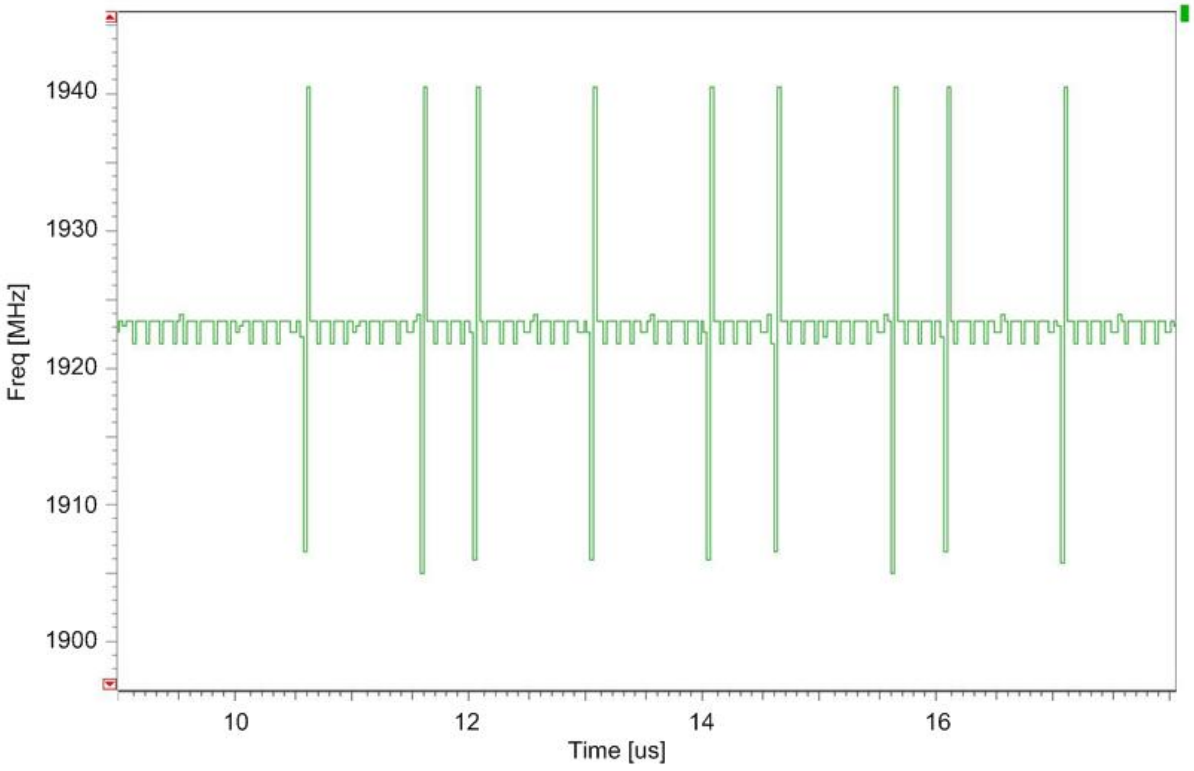


**Figure IV-26: Frequency measured when mismatch of the inverters is introduced (RFin = 1923MHz)**

As can be seen in Figure IV-26, mismatch of the inverters gives rise to errors on the measurement of the frequency of the input RF signal.

In this case, the fractional part is the one that is wrongly calculated.

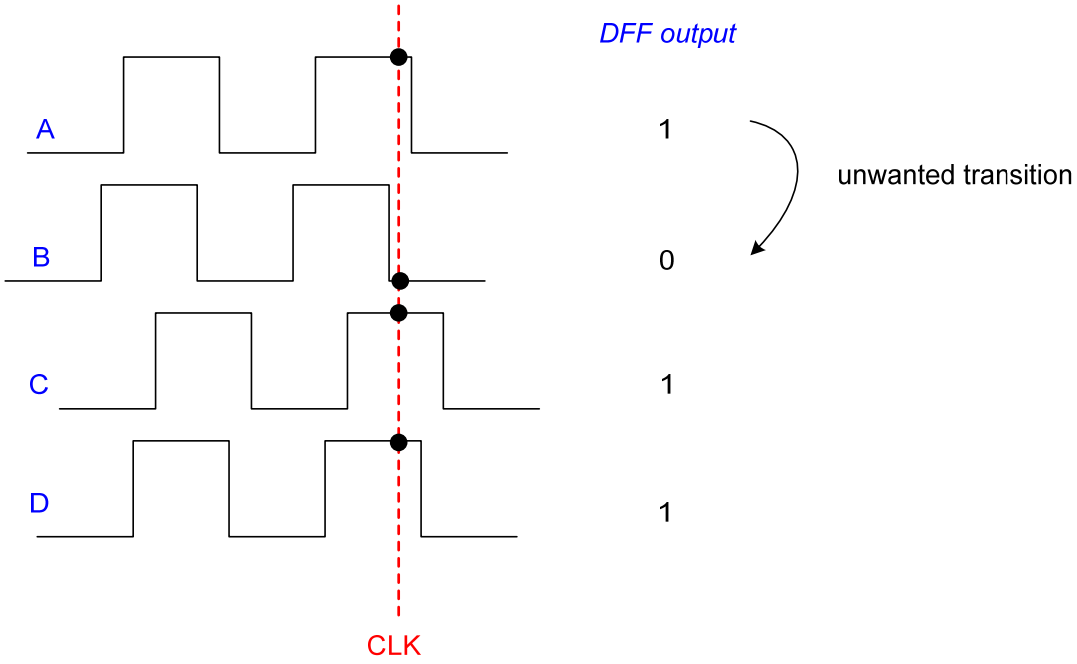


**Figure IV-27: The mismatch of the inverters causes a false 1 → 0 transition**

The fact of having two chains of delay elements can produce, when mismatch is introduced, the condition depicted in Figure IV-27.

Signal *B* should be the delayed version of signal *A*. Since the cumulated delay in one chain becomes different than that cumulated in the other, the delayed version of signal A arrives *before it*.

If the clock arrives near the falling edge of the RF input, an unwanted 1 → 0 transition may be seen at the output of the DFF chain.

The fractional part is then erroneously calculated.

Looking at Equation 5, the measured term B will be too small, giving at the output a measured frequency lower than the real one. The following clock cycle, the term A will be the wrong one, resulting in a too high measured frequency.

This effect can be seen in Figure IV-26. When an error is made, the measured frequency is too low and then, at the following clock rising edge, it is too high.

This problem can be solved if the decoder shown in Figure IV-25 is programmed to check the presence of a 1 → 0 → 1 transition. In this case, the transition is not taken into account.

### *IV.1.6 TDC for jitter measurement*

The last figure of merit of the VCO that needs to be measured is the phase noise.

The on-chip extraction of the phase noise curve is not trivial and not much work has been done by the scientific community in order to investigate this issue, especially at RF frequencies.

On the contrary, much more attention has been given to the on-chip measure of the jitter, the "time-equivalent" of the phase noise.

It has been shown that, even in the presence of non-idealities, the TDC is able to measure the period of the RF signal with high precision.

This is why it is here decided to investigate the use of the TDC for jitter measurement.

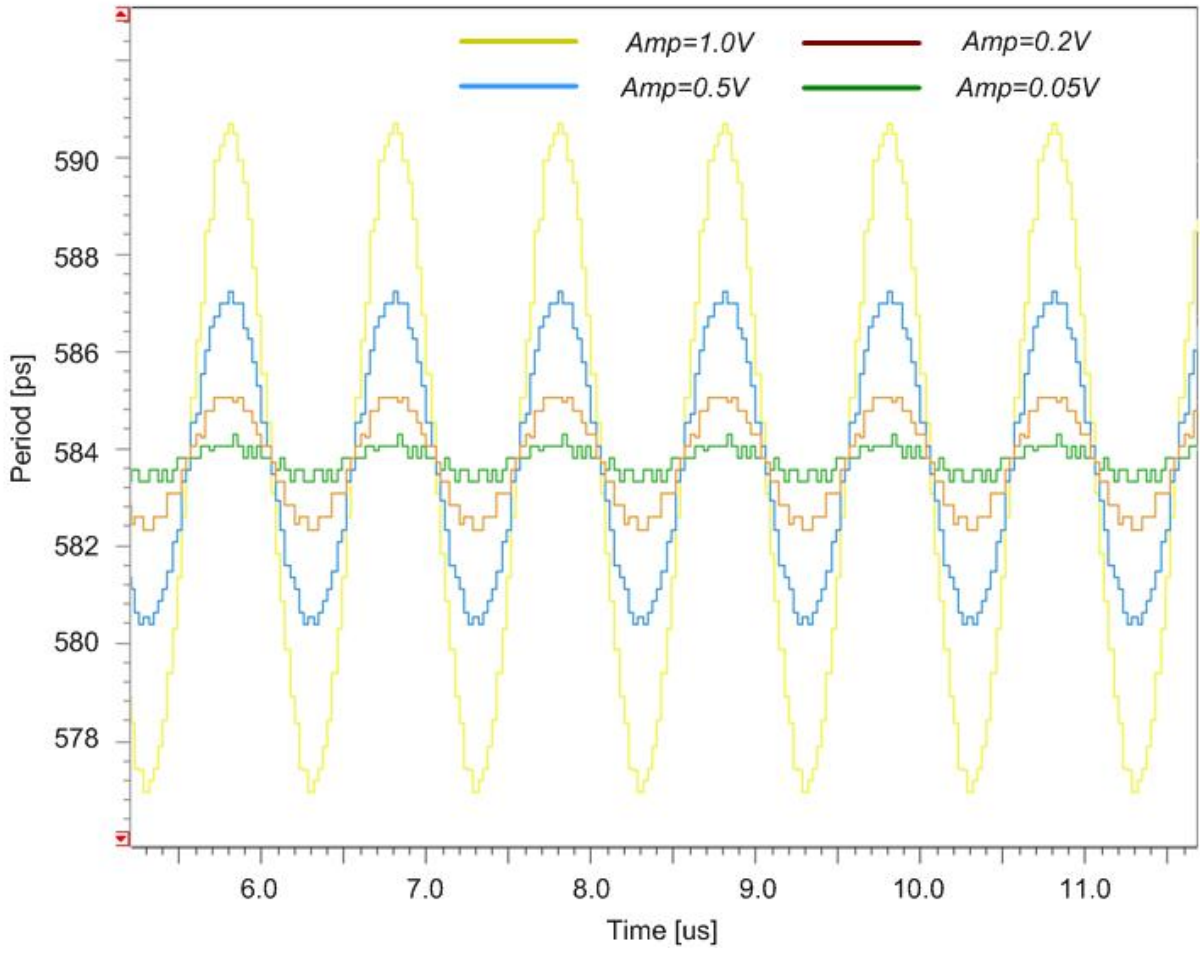


**Figure IV-28: Measure of the period of a frequency-modulated RF signal. An ideal VCO with $K_{VCO}$=20MHz/V is used, with a 1MHz sinusoidal control voltage. The simulation is repeated for different values of the amplitude of the control voltage.**

In order to investigate the accuracy of the TDC for jitter measurement purposes, the RF input signal is frequency-modulated. An ideal VCO with $K_{VCO}$=20MHz/V is used, with a 1MHz sinusoid applied to its control input. In Figure IV-28 the result of this analysis is shown, for different amplitudes of the control voltage.

It is shown that, even for a 50mV amplitude of the control signal (Δf=1MHz), the frequency modulation is detected.

Then, the jitter is modeled in VHDL-AMS as a random number with Gaussian distribution.

In order to create this distribution, a random number generator with uniform distribution is used, and its output is fed to a block performing the Muller-Box transformation [Box58].

Thanks to this transformation, the Gaussian distribution α is obtained.

$$\alpha = avr + std \cdot \left[\sqrt{\left(-2Log(u_1)\right)} \cdot \sin(2\pi u_2)\right] \quad (9)$$

α represents the Gaussian distribution, *avr* and *std* are its average value and its standard deviation respectively, $u_1$ and $u_2$ are the outputs of the random number generator with uniform distribution.

The period of the RF signal with jitter becomes:

$$\widetilde{T_{RF}} = T_{RF} \cdot \alpha \quad (10)$$

A simulation is run in order to validate the model for the jitter.

The jitter that is here measured is the *k*-cycle jitter or long-term jitter. It is the measure of the uncertainty in the length of *k* cycles of the input signal, as depicted in Figure IV-29.

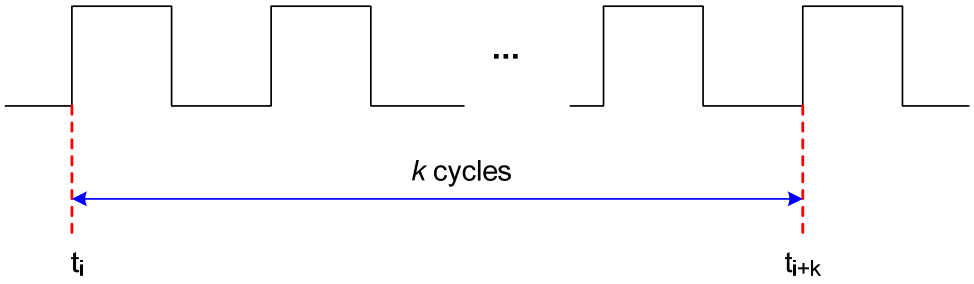


**Figure IV-29: k-cycle jitter (long-term jitter)**

Referring to Figure IV-29, the long-term jitter $J_k(i)$ can be defined as the standard deviation of $t_{i+k}$-$t_i$:

$$J_k(i) = \sqrt{var(t_{i+k} - t_i)} \quad (11)$$

The RF signal is set to 1700MHz, the average of the jitter to 1.0 and its standard deviation to 0.01.

The results are shown in Figure IV-30. At each rising edge of the clock, the period of the signal is measured.

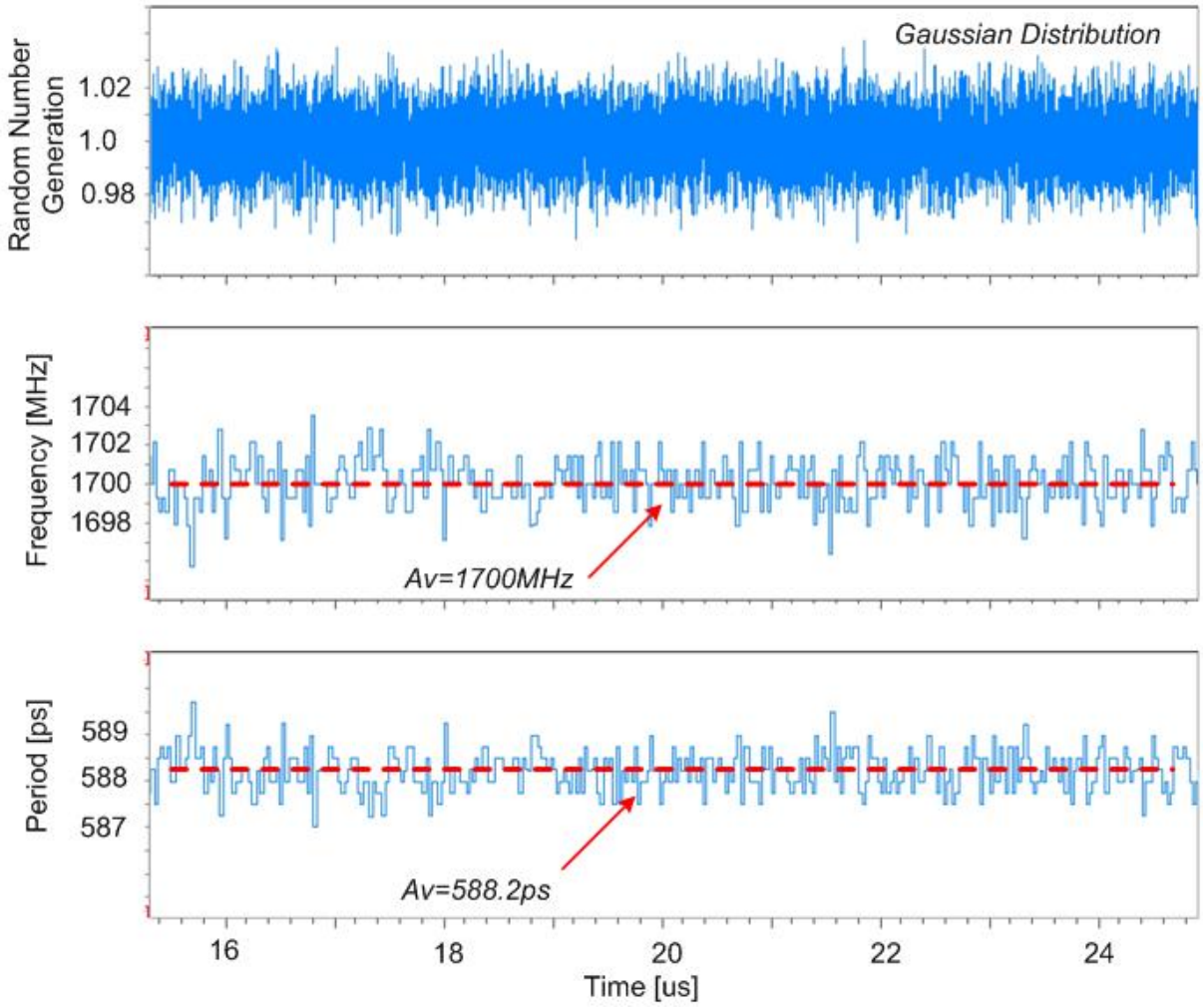


**Figure IV-30: Simulation of the TDC with jitter added to the RF input. The upper curve represents the random number α with Gaussian distribution. At each rising edge of the clock the frequency of the RF signal (middle trace) and its period (lower trace) are measured.**

As expected, since the average of the jitter is set to 1.0, the average measured frequency is 1700MHz and the average period is 588.2ps.

A new simulation is then performed, with the average of the jitter set to the value 1.001 and its standard deviation set to 0.01.

The expected result should be an average measured period of 588.8ps, corresponding to an average frequency of approximately 1698MHz.

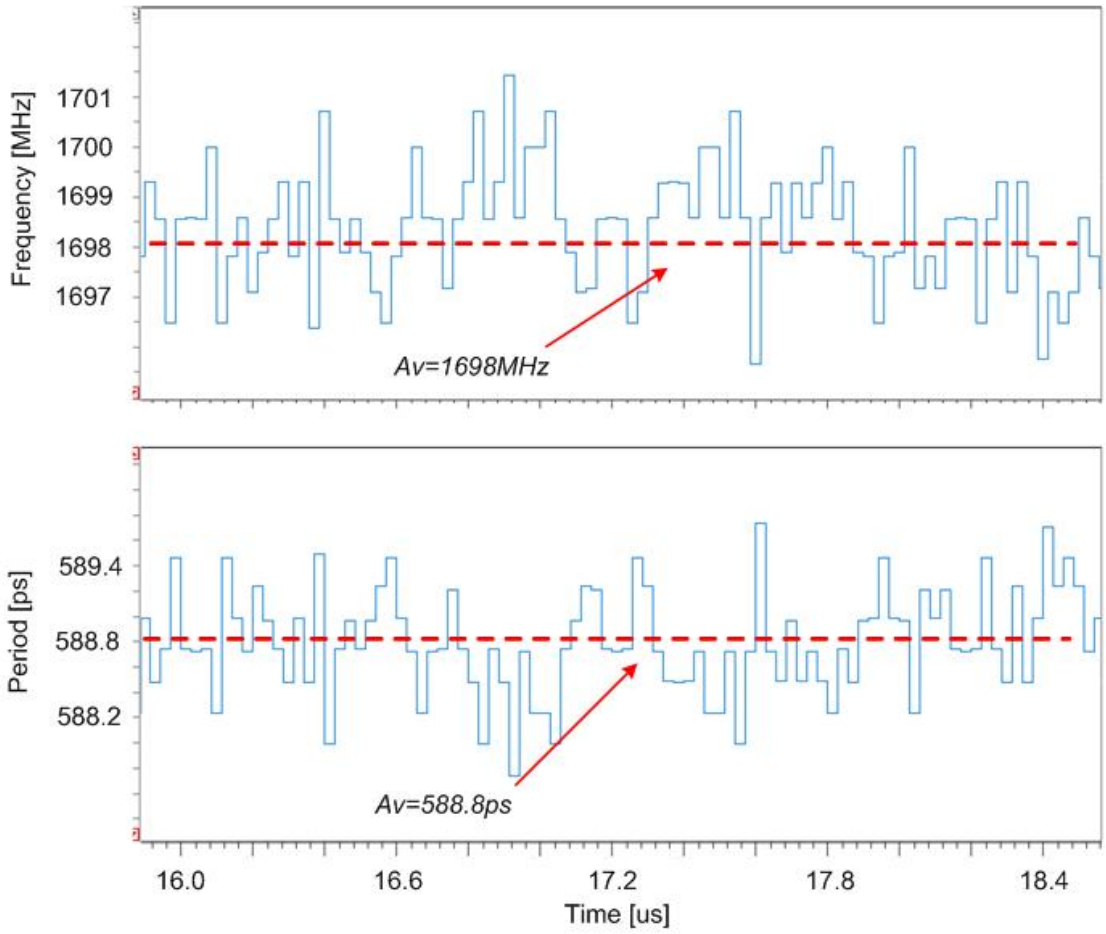


**Figure IV-31: Simulation of the TDC output when a jitter with average = 1.001 is introduced.**

The result, presented in Figure IV-31, confirms that the TDC is able to detect the long-term jitter introduced.

The results of those simulations show once more the suitability of the TDC for Built-In Self-Test purposes.

## *IV.2 Conclusion*

This chapter deals with an initial study on the complete on-chip characterization of the VCO for chip validation and process monitoring.

The validation process implies the verification of the current consumption of the CUT, of its output voltage amplitude, of its frequency of oscillation and conversion gain $K_{VCO}$, and of its phase noise (jitter).

Then in case of a malfunctioning, the process monitoring should be able to give information on the location of the problem. A frequency shift may result from problems in the LC tank, while an erroneous current consumption can be due to problems in the active part of the VCO.

The chapter focuses on the choice of the appropriate architecture of a RF frequency-meter.

Behavioral simulations using VHDL-AMS are carried out to decide the most suitable architecture for the on-chip accurate measurement of the frequency of oscillation of the VCO. The Time-to-Digital Converter (TDC) comes up as the best RF frequency-meter for on-chip test purposes.

Its behavior in case of non-idealities of the structure is also studied.

Finally, the possibility to have information on the long-term jitter using the same TDC is also investigated.

*IV.3 References*

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**[Sta06]** R.B.Staszewski, S. Vemulappi, P.Vallur, J.Wallberg, P.T.Balsara, "1.3 V 20 ps Time-to-Digital Converter for Frequency Synthesis in 90-nm CMOS", IEEE Transactions on Circuits and Systems – II: Express Briefs, Vol.53, n°3, March 2006

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# V GENERAL CONCLUSION

This work deals with the study and realization of Built-In Self-Test (BIST) strategies for RF VCOs.
Any commercial product goes through three main test steps:

- the wafer sort;
- the chip validation;
- the process monitoring and diagnosis.

The wafer sort aims at discriminating between good and faulty circuits at the wafer level.
Faulty circuits are discarded and don't reach the packaging phase.
Chip validation (die in package) implies the measurement of the CUT's performances. If the specifications are not met, the circuit can't be sold on the market.
If this test reveals problems, a diagnosis test phase starts, where engineers try to find the cause of the malfunctioning of the CUT.
Concerning RF blocks, those three test steps are nowadays carried out using external equipment (very expensive). The extraction of information at the wafer level, moreover, presents nontrivial problems due to the need to drive off-chip high-frequency signals without corrupting them.
In addition to this, a non negligible time is spent for the correct setup of those tests.

The goal of this work is to study the feasibility to carry out every test step directly on-chip, and propose a demonstrator for a built-in wafer sort test.

The first chapter presents a large panoramic of RF BIST solutions proposed in the literature.
The distinction is made between the two main BIST approaches to the wafer sort: functional test and structural test.
The first tries to measure on-chip the performance of the CUT. This methodology often relies on heavy, externally performed, software calculations. Moreover, the possibility to have information on the single RF building block is not always possible.
The second aims at finding catastrophic and parametric faults present in the circuit. This is done monitoring some electrical quantities and comparing them to their expected value. This technique is simpler compared to a functional test, and - despite its simplicity - is able to discriminate very well between a faulty and a good circuit (good fault coverage).

Emphasis is put on detectors, given their importance for a structural test. Current, amplitude, power and frequency sensors are presented from a general point of view.
Finally, the choice is done to focus our attention on the BIST of RF VCOs, because of their importance in any RX/TX chain and because of the lack of information on their on-chip testability.

In the second chapter the choice to implement a structural test is made.
The importance of the choice of the signal to monitor for the on-chip structural test is shown. Fault coverage is directly linked to this.
The best quantity to monitor is the one that presents the highest deviation from its nominal value for any catastrophic or parametric fault possibly present in the CUT.
This allows an easy discrimination between faulty and good circuits.
Catastrophic and parametric faults are automatically injected in the VCO and the deviation of multiple signals is studied; the result of this analysis shows that the peak-to-peak value of the output voltage is the quantity that needs to be monitored on-chip.
Starting from this assumption, the complete BIST architecture for wafer sort is implemented, using the ST CMOS 65nm process.
The VCO is powered by a LDO, which is driven by a temperature and supply-voltage independent controllable voltage reference. The BIST system counts a peak-to-peak voltage detector, a circuit for the generation of acceptance boundaries (the allowed deviation of the peak-to-peak value), a comparator and a final digital stage for the generation of the logic pass/fail information for the wafer sort.
It is proved, through Post-Layout simulations, that the BIST does not degrade the performance of the VCO. The silicon area occupied by the BIST is 5.5 smaller than the area occupied by the CUT.
Our solution can be considered transparent and low-cost.
Finally, it is shown that the BIST can be used as part of a corrective feedback able to recover, in certain scenarios, the functionality of the VCO. A new feedback system is proposed, that exploits the capability of the voltage reference to be controllable.

The measurements on PCB of the system are presented in the third chapter.
During this PhD work, we took advantage of only one run.
In the first part, the voltage reference and the detector are measured as stand-alone blocks. Those are the two main building blocks of the BIST architecture.
The voltage reference shows a very flat output characteristic for supply voltages higher than 1.0V, as expected. This is an indication of the good power supply rejection ratio of the circuit.

As demonstrated through equations and simulations, the voltage reference results being dynamically adjustable via the bulk voltage $V_b$. The output voltage changes linearly with $V_b$.

The output voltage is not temperature independent. A 50mV output voltage change is measured over 110°C. Two are the main causes of this problem: the poor layout that caused an erroneous functioning of the current mirror and the imprecise temperature model of the MOSFET.

The measurements of the peak-to-peak detector agree with the simulations. Its good linearity and its proper functioning at the low supply-voltage of 1.0V are proved.

Problems are encountered when trying to measure the overall system.

Nevertheless, it was possible to measure the overall BIST architecture. The good functioning of the circuit for the generation of the acceptance limits, the detector, the comparator and the final digital stage to have a logic pass/fail output is demonstrated.

Perspectives are presented in the fourth and last chapter.

After having given prove in the previous chapters of the feasibility of a BIST for wafer sort, the problem of the chip validation and diagnosis is addressed.

The main performances that should be measured are:

- current consumption;
- output voltage amplitude;
- oscillating frequency and conversion gain $K_{VCO}$ ;
- phase noise (jitter).

The main challenge is the accurate on-chip measure of the RF oscillating frequency.

Two main structures of frequency-meters are evaluated making use of VHDL-AMS behavioral simulations: Frequency-to-Voltage Converters (FVC) and Time-to-Digital Converters (TDC).

The study shows that the TDC is a better option for our purposes.

The same TDC architecture is used to extract information on the long-term jitter of the signal.

With information on oscillating frequency and current consumption in hand, some on-chip diagnosis in case of a problem can be performed.

If the current shows an important deviation from its expected value, the likely cause of error is a problem on the active part of the VCO. If, on the contrary, the oscillating frequency is the quantity showing the highest deviation, the problem will probably come from the LC tank.

In conclusion, this work shows the usefulness and the feasibility of BIST strategies for RF VCOs.

The performances of the CUT are not degraded, and the small Si area and consumption of the BIST guarantee a low-cost solution.

The road is now open to the substitution of traditional external test methodologies with more economical and still accurate built-in self-test solutions, even in the RF domain.