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Localized growth and characterization of silicon nanowires

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Abstract

This thesis deals with the epitaxial growth and characterization of silicon nanowires, because these nanostructures have recently been incorporated in functional devices with success, but a reproducible use requires a deeper understanding of their physical properties. As the growth proceeds through the incorporation of Si species into catalyst particles, we first investigated the formation of gold islands on Si (111)-(7×7) surfaces and demonstrated that a good control over the size and density of the particles can be obtained. Two growth techniques, the Molecular Beam Epitaxy (MBE) and the Chemical Vapour Deposition (CVD) were compared in order to get nanowires long enough and well oriented, so that the nanowires could be integrated into microstructures. With MBE and CVD at low silane partial pressure, <111>-oriented Si nanowire were grown, but the characterization of their structural properties by scanning and transmission electron microscopies as well as scanning tunneling microscopy revealed that the nanowires were tapered, their sidewalls were faceted and that the atomic structures of the facets were caused by the diffusion of gold from the catalyst particle. From the analysis of their morphology, we showed that the incorporation of Si directly onto the sidewalls strongly contribute to the shape of the nanowires and also suggested that the observation of alternating narrow and wide sidewalls is related to the atomic structure of the (111) interface between the gold droplet and the Si shaft.

We further analyzed the chemical composition of doped <111>-oriented Si nanowires by three-dimensional atom probe tomography (APT) and showed that boron impurities can be incorporated into the Si nanowires during the growth, by simply changing the ratio between the silane source and the diborane source. However the nanowire conductivity was unexpectedly too small to account for the concentration of boron impurities, probably due to the high amount of gold atoms that diffuse from the droplet and act as deep level centers. As a result, the growth of n-type and p-type doped Si nanowires at higher silane partial pressures were investigated and allowed to increase the nanowire conductivity.

Résumé

En raison de leur compatibilité avec la technologie conventionnelle du silicium, les nanofils de silicium semblent très prometteurs pour être utilisés comme briques de base de composants électroniques à l'échelle nanométrique. Ce travail de thèse se focalise sur la croissance épitaxiale et la caractérisation de tels nanofil. Les nanofils de silicium sont fabriqués par la méthode Vapeur-Liquide-Solide (VLS) à partir de catalyseurs d'or, en utilisant deux techniques: dépôt chimique en phase vapeur (CVD) et épitaxie par jets moléculaire (MBE). Dans la première partie de cette étude, les catalyseurs d'or sont déposés sur le substrat Si(111) en ultravide pour bénéficier d'une interface or-silicium de grande qualité. A partir de ces ilôts d'or, des nanofils orientés <111> sont obtenus par MBE et CVD, lorsque la pression partielle de silane est faible. En profitant de l'orientation contrôlée des fils qui favorise leur intégration dans les composants, plusieurs structures basées sur les nanofils ont donc été développées. Dans la deuxième partie de cette étude, les structures atomiques des surfaces facettées de nanofils orientés <111> ont été étudiées par microscopie à l'effet tunnel (STM) à basse température. En combinant ces observations avec des images de fils identiques en microscopie électronique, nous avons révélé la diffusion d'atomes d'or depuis le catalyseur le long des fils. Cette diffusion a plusieurs conséquences : elle conduit en partie à la forme conique des nanofils et est certainement à l'origine de l'alternance de la taille des parois des nanofils. Une troisième partie a porté sur le dopage des nanofils. Des gaz tels que la phosphine ou le diborane peuvent être utilisés pour incorporer des dopants de type n ou type p dans les nanofils pendant la croissance. La tomographie par sonde atomique (TAP) a été utilisée pour caractériser la distribution des impuretés dans le volume de nanofils de silicium dopés au bore et orientés <111>. Une distribution uniforme de bore a été observée au centre de nanofils et la concentration des impuretés mesurée correspond bien à la valeur estimée par le rapport entre le flux de silane et de diborane. Enfin, ces observations ont été comparés avec des mesures de conductivité dans des nanofils individuels.

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Chapter 1

Introduction

1.1 Nanotechnology and Nanostructures

Fifty years after that famous talk: " there is plenty of room at the bottom ", stated by Richard Feynman in the American Physical Society in 1959, nanotechnology presents nowadays an existing and rapidly expanding research area that spans the wide scope of interrelated fields from electronic, optoelectronic, and energy to healthcare. Much of the excitement in this area of research has arisen from recognition that new phenomena, multifunctionality, and unprecedented integration density are possible with nanometer-scale structures, in another word: nanostructures. Most of the results and much of the interest in nanotechnology today are focused on the study and applications of the nanostructures, because when at least one dimension of crystalline structures is reduced to the order of hundreds of atoms - the length scale of nanometers, the physical principles important to atoms, but normally negligible in bulk, begin to increase in importance [1], enabling unique applications. For instance, opaque substances become transparent (copper); stable materials turn combustible (aluminum); solids turn into liquids at room temperature (gold). A material such as gold, which is chemically inert at normal scales, can serve as a potent chemical catalyst at nanoscale.

The unique properties of nanostructures can be roughly separated into two primary categories: surface-related effects and quantum confinement effects. Surface effects arise because atoms at the surface of a crystalline solid experience a different chemical environment than other atoms, changing their behaviour. In bulk materials, the proportion of surface atoms to bulk atoms is entirely negligible, and processes that take place at the surface are usually of little consequence to the behaviour of the material as a whole. However, the surface-to-volume ratio of nanostructures is considerably higher - high enough that surface effects often cannot be ignored. The increased reactivity of the surface compared to the rest of the material reduced the inertness of materials with high surface area [2].

Quantum effects occur when the wavelength of an electron in a material is of the same order as a dimension of the material. This limits the motion of an electron in the material, which becomes quantized in that confining dimension. The density of states of the electrons is then determined by the dimensions in which electrons are quantified [3].

Classification of nanostructures

In describing nanostructures it is necessary to differentiate between the number of dimensions on the nanoscale. Nanostructures, more specifically, semiconductor nanostructures, can thus be generally classified into three types. Several examples are given in Fig.1.

- **Two-dimensional (2D) Superlattices:** Superlattices are artificial periodic structures composed of alternating layers (usually of several to tens nanometers thickness) of different materials grown generally by molecular beam epitaxy (MBE) on substrate. The electronic, optoelectronic, and thermal properties of superlattices can be turned to be desirable for specific applications by different material combinations and different layer thickness. For instance, Fig.1.1(a) shows a cross-section transmission electron microscopy image of the SiGeC/Si superlattice microcooler sample with an enlarged image on the right (10 nm $Si_{0.89}Ge_{0.10}C_{0.01}$/10 nm Si) [4].

- **One-dimensional (1D) nanotubes and nanowires:** One of the most well-known 1D nanostructure is carbon nanotubes. Since their discovery in 1991 [5], carbon nanotubes have been a subject of intense research because it provides a remakable 1D system. Single-wall carbon nanotubes (SWCNTs) could be one atom in thickness, a few tens of atoms on circumference, and many micron in length, which can be regarded as a single layer of a graphite crystal that is rolled up into a seamless cylinder. One example is given in Fig.1.1(b) where the surface of a SWCNT is imaged by scanning tunning microscope (STM) [6]. Carbon nanotubes can be either semiconducting or metallic depending on its diameter and chirality. Because of its controllable electronic properties and nanometer size, efforts such as using carbon nanotubes to make logic circuits with carbon nanotube transistors [7] and random access memory for molecular computing [8] have already been carried out.

- **Zero-dimensional (0D) quantum dots:** A quantum dot is a semiconductor whose excitons are confined in all three spatial dimensions. As a result, they have properties that are between those of bulk semiconductors and those of discrete molecules [9]. They can be thought of as tiny boxes with a dimension less than 100 nm, as it is shown in Fig.1.1(c) of a high resolution transmission electron microscopy image of a CdSe quantum dot. Quantum dots represents perhaps the ultimate in the miniaturization of electronic circuits. The number of free electrons contained in the boxes can be varied at between one and a few hundreds. Transport through such a quantum dot with only one electron can be used as a single electron device, a transistor of superior sensitivity [10].

How to create nanostructures ?

Since the properties and functions of nanostructures depend strongly on their structures, a controlled mean of fabricating such nanostructures are thus necessary.

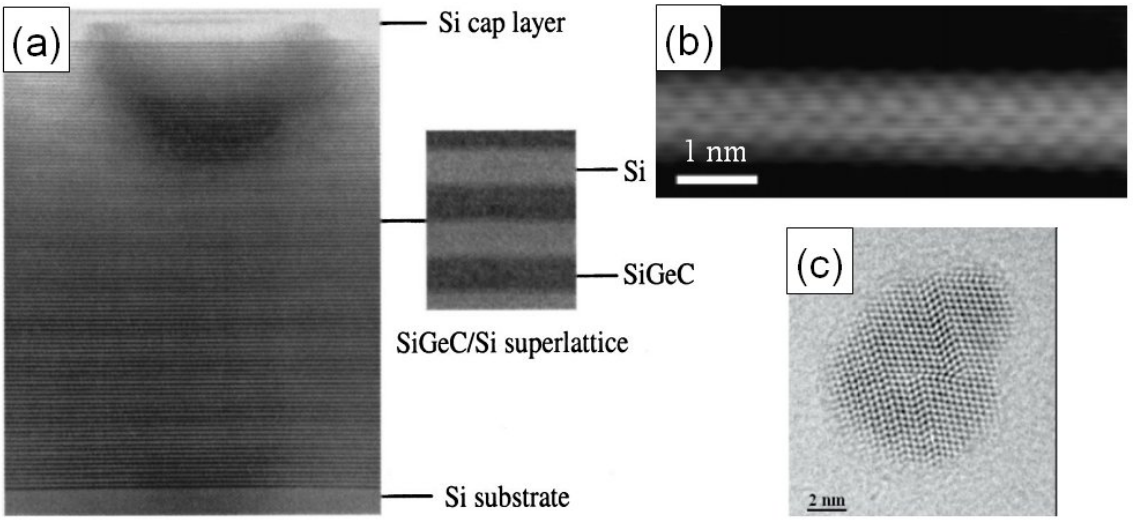

Figure 1.1: Classification of nanostructures. (a) Cross-section TEM image of the SiGeC/Si superlattice. The top is 100 nm Si cap layer; the middle is 2 μm superlattice of 100×(10 nm $Si_{0.89}Ge_{0.10}C_{0.01}$/10 nm Si); the bottom is the Si substrate. An enlarged superlattice image is shown on the right side [4]. (b) STM image of a single-walled carbon nanotube [6]. (c) HRTEM image of a CdSe quantum dot.

In general, there are two philosophically distinct approaches for creating nanostructures:

- **Top-down:** In this approach, small features are achieved in bulk materials by a combination of lithography, etching, and deposition to form functional devices and their integrated system. The top-down approach has been exceedingly successful in many venues, specially in microelectronics. While developments continue to push the resolution limits of this approach, the improvements in resolution are associated with a near-exponential increase in cost associated with each new level of manufacturing facility. Such economic limitation and other scientific challenges with the top-down approach, such as making nanostructures with near-atomic perfection and incorporating materials with distinct chemical and functional properties, have motivated efforts to search for new strategies to meet the demand for nanoscale structures today and in the future [11].

- **Bottom-up:** The bottom-up production methods, on the other hand, mimic nature's way of self-assembling atoms to form increasingly larger structures. Such techniques involve controlled crystallization of materials from vapor or liquid sources, typically yielding uniform and highly ordered nanoscale structures, and thus presenting a powerful alternative approach to conventional top-down methods. This approach has the potential to go far beyond the limits and functionality of top-down technology by defining key nanoscale metrics through synthesis and subsequent assembly - not by lithography. Moreover, it is likely that this approach will enable entirely new device concepts and functional systems and thereby create technologies that we have not yet imagined [12].

As it is described above, developing the bottom-up growth of nanostrucutures as building blocks in the fabrication of hybrid micro-nano-assembled system could be an intellectual path of nanotechnology in the future. Furthermore, understanding the physics of new nanostructures emerging from synthetic efforts is an important and fundamental part of the bottom-up approach, since such studies define properties that may ultimately be exploited for nanotechnology. An intimate integration between material growth and fundamental characterization could make it possible to define new device concepts unique to the nanoscale building blocks.

1.2 Nanowires

Nanowires can be defined as 1D structures that have a thickness or diameter constrained to tens of nanometers or less and an unconstrained length. Many different types of nanowires exist, including metallic (e.g. Ni, Pt, Au), semiconducting (e.g. Si, InP, GaN), and insulating (e.g. SiO_2,TiO_2). Among them, semiconductor nanowires represent one of best-defined and controlled classes of nanoscale building blocks at the forefront of nanotechnology. Comparing to another well-known 1D nanostructures: carbon nanotubes, whose electronic properties are largely determined by the chirality of the graphene layer, semiconductor nanowires offer several unique merits. First, a broad range of chemical compositions is achievable for nanowires versus simply carbon. Second, nanowire devices can be assembled in a rational and predictable manner because their size, surface properties and electronic properties can be precisely controlled during synthesis. Moreover, reliable methods exist for their parallel assembly. Such control has enabled a wide range of devices and integration strategies to be pursued in a rational manner. A brief overview of the current state of the nanowire synthesis, characterization, and integration into functional devices is given in the following.

1.2.1 Synthesis and Assembly

Among the numerous methods that have been explored, a strategy that has received increasing focus in the past several years involves exploiting a catalyst to confine growth in one dimension. Depending on the phases involved in the reaction, several growth concepts can thus be defined, such as vapor-liquid-solid (VLS) [13], solution-liquid-solid (SLS) [14] or vapor-solid (VS) [15], among which the VLS growth is the most utilized and adapt to a substantial productivity. In VLS growth, the catalyst is a metallic nanoparticle which defines the diameter of nanowire and serves as the site that preferentially directs the addition of reactant to the end of a growing nanowire. Fig.2 demonstrates some examples of VLS nanowire growth using different techniques and concerning different materials.

Fig.1.2(a) shows Si nanowires grown by Au nanoparticle-catalyzed chemical vapor deposition (CVD) [16], while Si nanowires can be also synthesized by molecular beam epitaxy (MBE) in ultra high vacuum (UHV) [17], as seen in Fig.1.2(b). In addition to the group IV materials, a wide range of III-V materials can also be involved in VLS growth, as it is shown in Fig.1.2(c) for InP nanowires grown by metal organic vapor phase epitaxy (MOVPE) [18].

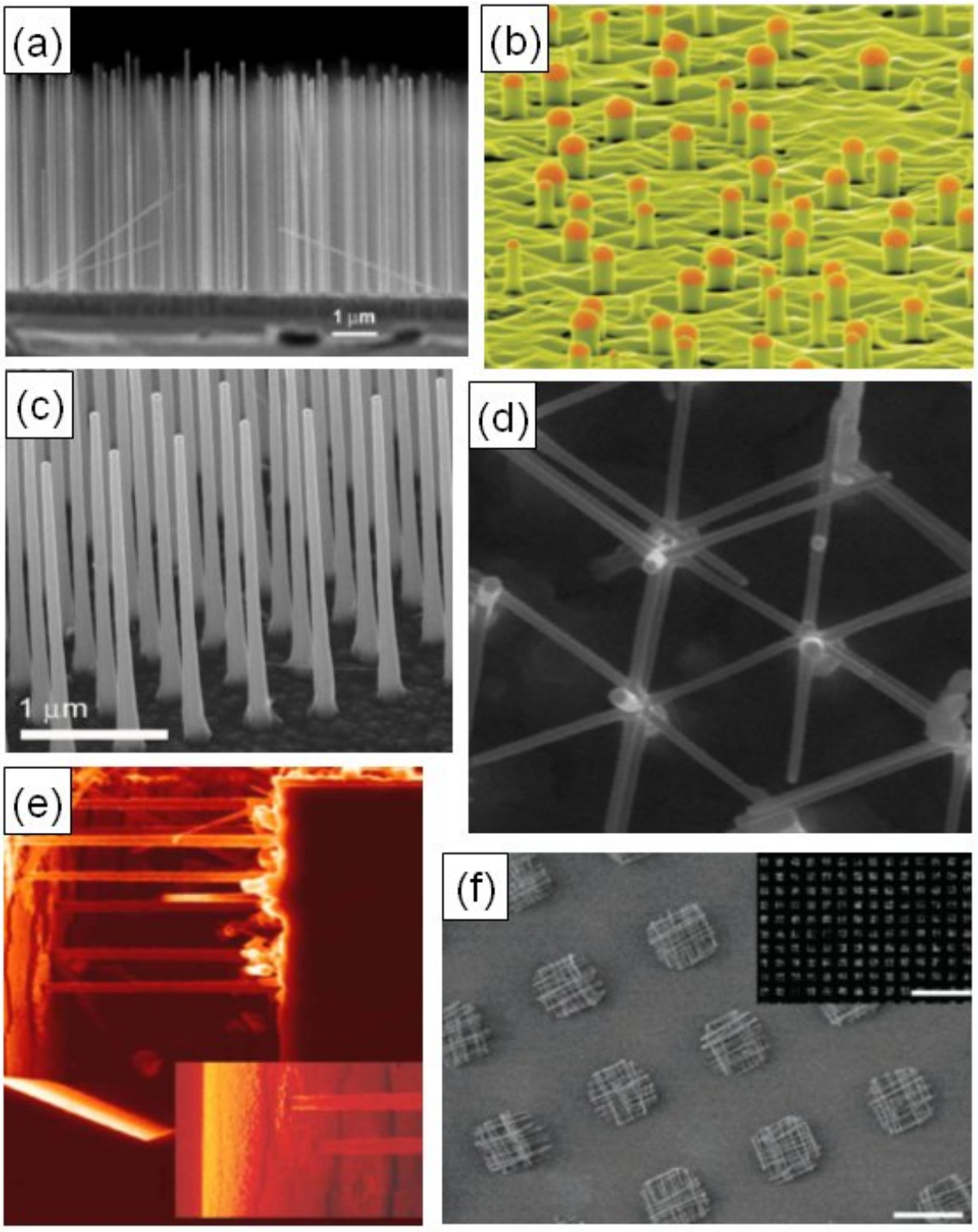

Figure 1.2: Synthesis and assembly of nanowires. (a) CVD growth of Si nanowires [16]. (b) MBE growth of Si nanowires [17]. (c) Array of InP nanowires grown from lithographically defined Au nanoparticles [18]. (d) Position-controlled InAs nanowire network [19]. (e) Lateral epitaxial Si nanowire growth across an 8 um wide trench, connecting to opposing sidewall [20]. (f) Large-scale hierarchical organization of nanowire arrays using the Langmuir-Blodgett technique [21].

The organization and directed assembly of nanowires into designed hierarchical structures is a key goal necessary for creating arrays of devices. In order to achieve the integration, the top-down approach is thus combined with the bottom-up synthesis. For instance, using lithographic positioning of metal seed particles, an array of nanowires can be grown, also shown in Fig.1.2(c) [18]. More complex nanostructured system such as nanotrees have been realized, as it is shown in Fig.1.2(d) of three-dimensional networks of InAs nanowires [19]. A position-controlled array of trunk nanowires is first produced using lithographically defined Au particles as seeds. With these wires positioned along the proper crystallographic directions with respect to each other, nanotree branches can grow toward neighboring trunks, connecting them together.

Fig.1.2(e) shows the growth of Si nanobridges between microtrenches prefabricated by microfabrication techniques [20], taking advantage of the controlled nanowire growth direction along the <111> direction. Another assembly strategy is the Langmuir-Blodgett (LB) technique, in which an ordered monolayer is formed on water and transferred to a substrate. Parallel and crossed nanowire structures have been assembled by single and sequential transfers over centimeter length scales, as it is shown in Fig.1.2(f) [21]. Through all these hierarchical assembles, it is possible to take advantage of the interesting properties and create novel applications.

1.2.2 Characterization

The emergence of nanotechnology is partly because of the availability of powerful observation and manipulation tools such as scanning electron microscope (SEM), transmission electron microscope (TEM), and scanning tunneling microscope (STM). These characterization tools allow the direct and precise analysis on the morphology, crystallography, surface structure and chemical composition of nanostructures, what make it possible to well understand their physical, electrical and chemical properties. Some recent imaging and analysis of nanowires are given in Fig.1.3, in order to give an idea on which level the characterization of nanostructures have already reached.

For example, the atomic scale imaging of the exterior surfaces of nanowires can be revealed by STM. Fig.1.3(a) shows a STM image of the surface of a small-diameter Si nanowire prepared by an oxide-assisted growth [22], while (b) is a STM image of a wurzite InAs nanowire [23], the inset shows the atomic As rows of top facet of this nanowire. On the other hand, a thorough characterization including the determination of the growth direction, cross-section, surface morphology, dislocations, and stacking faults can be achieved by using electron microscope techniques like TEM. Fig.1.3(c) is an *in situ* TEM analysis of a Si nanowire grown by UHV-CVD technique, showing the presence of sawtooth facets on the nanowire sidewall [24]. Fig.1.3(d) presents an high-resolution (HR) TEM image of the sidewall of a InAs nanowire, indicating two zinc blende (ZB) segments separated by two single twin planes [25].

More recently, it has been shown that atom probe tomography (APT) can be used to determine the composition of isolated nanowire with a single-atom sensitivity and also reveal its three dimensional reconstruction. An analysis of a reconstructed nanowire section ($14 \times 14 \times 23$ nm^3) including a Au catalyst/InAs nanowire het-

erophase interface is displayed in Fig.1.3(e). In, As and Au atoms are rendered as green, purple, and yellow dots respectively [26].

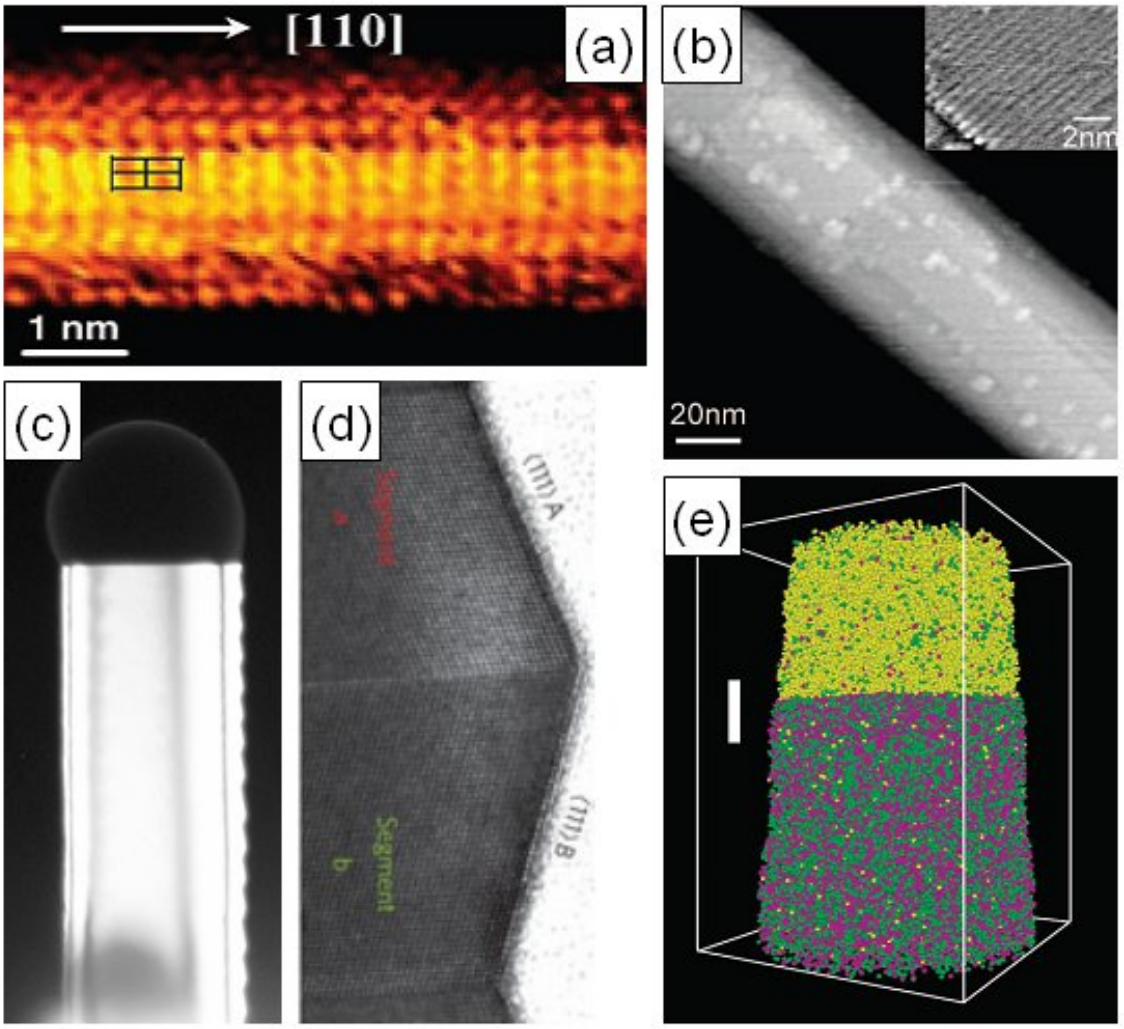

Figure 1.3: Characterizations of nanowires. (a) STM image of a Si nanowire [22]. (b) STM image of a InAs nanowire [23]. (c) TEM image of a Si nanowire with sawtooth facets [24]. (d) HRTEM image of a InAs nanowire sidewall [25]. (e) Three-dimensional reconstruction of an InAs nanowire with Au particle at the top. In, As and Au atoms are rendered as green, purple, and yellow dots respectively [26].

1.2.3 Application

The unique control of the microstructure of nanowire building blocks arises from the excellent understanding of their growth mechanisms and their properties. Such control has enabled a wide range of devices and integration strategies. Firstly, in the electronic applications, studies of Si or other nanowire materials have shown that the nanowire devices can behave as excellent field-effect transistors (FETs) and moreover, the carrier mobilities can be comparable to the best achievable in planar silicon. For example, VLS-grown doped Si nanowires have been integrated into vertical FETs [27] shown in Fig.1.4(a), and also horizontal FETs [28] shown in Fig.1.4(b).

The previous one demonstrates a hole mobility range from 7.5 to 102 $cm^2V^{-1}s^{-1}$ with an average mobility of 52 $cm^2V^{-1}s^{-1}$; while for the latter one, the device mobility has been found at 307 $cm^2V^{-1}s^{-1}$ for the P-type [29] and 260 $cm^2V^{-1}s^{-1}$ for the N-type structures [30]. In addition to the nanowire-based FETs fabricated with the help of lithography, the Langmuir-Blodgett assembled crossed nanowire array can be used as logic gate [31], as it is shown in Fig.1.4(c). These crossed nanowire p-n junctions and junction arrays are assembled in over 95% yield with controllable electrical characteristics. Nanowire junction arrays can be configured as key OR, AND and NOR logic gate structure with substantial gain.

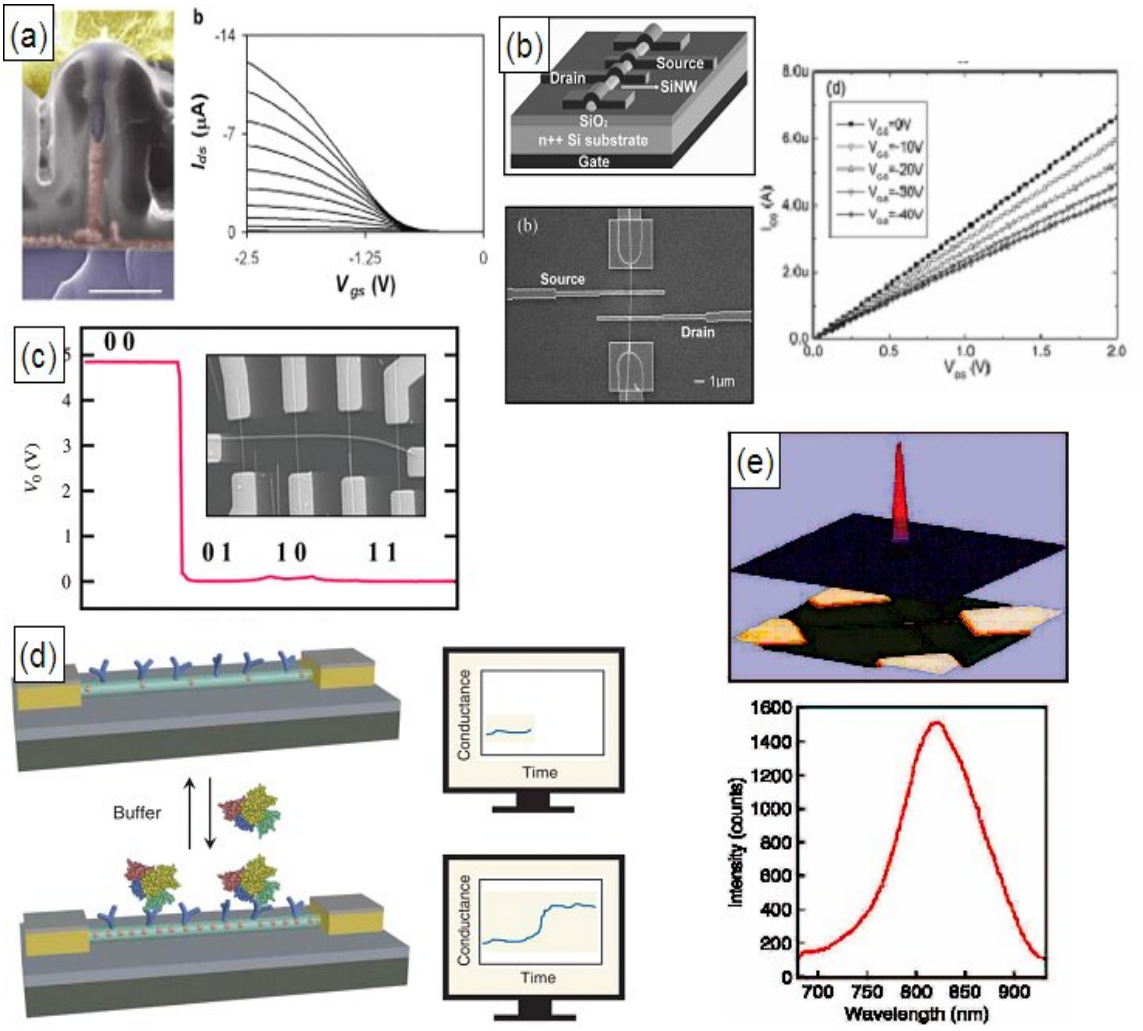

Figure 1.4: Applications of nanowires. (a) Cross-section SEM image of a vertical FET device with its characteristics on the right [27]. Blue corresponds to the Si source and nanowire, gray corresponds to SiO_2 dielectric, red corresponds to the gate material, and yellow corresponds to the drain metal. (b) Schematic representation and SEM image of a four-point back-gate n-type Si nanowire FET with its characteristics [28]. (c) Output from a crossed-nanowire NOR logic gate. The inset shows a SEM image of the logic gate structure: thin horizontal and vertical lines are nanowires [31]. (d) (left) Schematic illustration of a nanowire field-effect transistor configured as a sensor with antibody receptors (blue). (right) Binding of a protein with a net negative charge to a p-type nanowire yields an increase in conductance [32]. (e) Image of the structure and light emission (top) and plot (bottom) of the emission spectrum from a crossed-nanowire LED [33].

Another exciting venue resides at the interface between nanotechnology and biology. Many biological macromolecules, such as proteins and nucleic acids, are comparable in size to nanoscale building blocks. Nanowires can thus be served as sensors for the detection of chemical and biological species. The idea is that the conductance of nanowire-based FETs will change in response to the binding of chemical and biological species at the nanowire surface - that is, molecular or macromolecular species gate the nanowire-based FET and thereby change the conductance. The principle of nanowire-based biosensor is demonstrated in Fig.1.4(d) [32]. Finally, for the photonic applications, nanoscale light-emitting diodes (LED) has been fabricated, where the p/n junction of LED can be produced by sequential assembly of p-type and n-type nanowire in crossed-nanowire device. One example is given in Fig.1.4(e): multiple n-type direct-bandgap nanowires including GaN (ultraviolet), CdS (green), and InP (near-infrared) are assembled across single p-type Si nanowires to create nanoLEDs that can simultaneously produce ultraviolet, green, and red light [33].

1.3 Scope of work

Among all the semiconductor nanowires, Si nanowires show particular interests because silicon is the principal component of most semiconductor devices, most importantly integrated circuits. Si nanowires are therefore compatible with the conventional Si technology. Although an enormous studies have already been performed on the innovation of Si nanowire-based devices as it is described above, a more successful integration of Si nanowires in the future will depend ultimately on the degree of control that can be gained over their structural, physical and electrical properties, so a better understanding of their properties is still needed. For example, several questions concerning Si nanowires had not yet been well resolved at the time we started this work, such as how to control the growth direction of Si nanowires to achieve a direct integration of nanowires into devices? How to well incorporate dopants into Si nanowires during growth without changing their morphology and what is the real distribution of dopants and the doping level of Si nanowires? What is the role of nanowire surface on the thermal and electrical conduction of Si nanowires and can we get a good control of the properties of nanowire surface?

This thesis focuses on the epitaxial growth and characterization of Si nanowires. The aim of this work is to be able to resolve the questions mentioned above: in order to obtain a thorough understanding of particle-assisted Si nanowire growth, to develop a controlled fabrication technique that combines the bottom-up synthesis of nanowires with the top-down elaboration of microstructures, and finally to gain a deep comprehension of the properties of Si nanowires.

Chapter 2 introduces the experimental techniques used in this work, including the nanowire synthesis systems, the characterization tools and the microfabrication techniques. The main achievements are organized into three parts. Chapter 3 describes a strategy for the controlled Au catalyst deposition: Au islands are deposited on Si(111) substrates under UHV condition. The Au/Si(111) surface structures are studied by STM and the distribution of Au islands can be well controlled by regu-

lating the deposition parameters. Chapter 4 presents two approaches to synthesis Si nanowires, based on the VLS growth mechanism: Si nanowires are grown by Au island-catalyzed CVD and/or MBE techniques on Si(111) substrates in a controllable manner, which allows the further localized nanowire growth on certain microstructures. Chapter 5 focuses on various characterizations of the properties of Si nanowires, including their surface structure, chemical composition and electrical properties. Finally, some concluding remarks are given.

Chapter 2

Experimental techniques

This chapter presents the experimental techniques used in this work, which are generally classified into 3 parts:

- Nanowire synthesis systems: $\longrightarrow$ Bottom-up nanostructure growth.
- Characterization tools: $\longrightarrow$ Topographic, crystallographic, chemical and electrical analysis.
- Microfabrication techniques: $\longrightarrow$ Top-down microstructure fabrication.

All the techniques will be briefly introduced in the next sections and their functions will be integrated together in order to achieve the localized growth and characterization of Si nanowires.

2.1 Nanowire synthesis systems

Semiconductor nanowires are generally synthesized by employing metal nanoparticules as catalysts *via* vapor-liquid-solid (VLS) process [34]. Some gaseous reactants are used as the semiconductor source in the process. These gaseous reactants can be generated through decomposition of precursors in a chemical vapor deposition (CVD) process or through momentum and energy transfer methods such as pulsed laser ablation or molecular beam epitaxy (MBE) from solid targets. In this work, two growth systems have been used to perform the growth of Si nanowires: a low-pressure CVD reactor and a MBE UHV chamber.

2.1.1 LP-CVD reactor

Chemical Vapor Deposition (CVD) is a chemical process used to produce high-purity, high-performance solid materials. In a typical CVD process, the substrate is exposed to one or more volatile precursors, which react and decompose on the substrate surface to produce the desired deposit. Frequently, volatile by-product are also produced, which are removed by gas flow through the reaction chamber. A number of forms of CVD are in wide use, which differ in the means by which chemical reactions are initiated and process conditions:

- Low-pressure CVD (LP-CVD): CVD processes at subatmospheric pressures. Reduced pressures tend to reduce unwanted gas-phase reactions and improve film uniformity. The growth rate is thus relatively slow and the growth temperature is high.

- Plasma-enhanced CVD (PE-CVD): CVD processes that utilize a plasma to enhance chemical reaction rates of the precursors, which allows deposition at lower temperatures.

In this work, a high temperature LP-CVD reactor has been developed specially for the Si nanowire growth, as shown in Fig.2.1(a). Fig.2.1(b) presents the schematic of this CVD reactor, which consists of generally three parts:

- Gas distribution: Several gas are available in the reactor, such as N_2, H_2, Ar, SiH_4, B_2H_6 and PH_3. An Interlock security system is integrated in all the lines of the toxic gas.

- Furnace: A quartz tube (T_{max} 1150 °C) is used as the reaction place. 3 thermocouples control the heating condition in the different zones of the tube.

- Pumping system: An Alcatel dry pump is used to regulate the vacuum of the reactor which can be in the range of 10^{-3} to 500 mbar. A Boc Edwards scrubber system is added after the pump in order to remove the toxic particles or gases from the exhaust streams. The exhaust stream is diluted with N_2 in the scrubber before releasing into air.

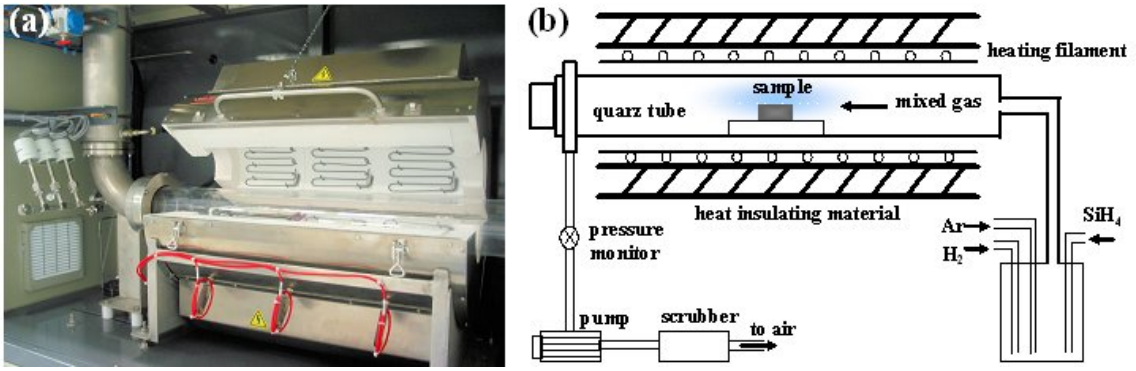

Figure 2.1: a) MPA LP-CVD reactor in IEMN; (b) Schematic of the CVD system

Si nanowires are synthesized in this reactor on the Si substrates with Au catalysts. SiH_4 is used as precursor gas following the reaction as:

$$SiH_4 \rightarrow Si + 2H_2 \tag{2.1}$$

While B_2H_6 and PH_3 are used as the doping gas, different temperatures and pressures conditions will be studied to grow nanowires with different structural properties, as it is presented in Chapter 4.

2.1.2 UHV-MBE chamber

Molecular Beam Epitaxy (MBE) is one of the several methods of depositing single crystals, which takes place in UHV environment. The most important aspect of MBE is the slow deposition rate (typically less than 1 μm per hour), which allows the films to grow epitaxially. In solid-source MBE, ultra-pure elements such as silicon are heated in separate quasi-knudsen effusion cells until they begin to slowly sublimate. The gaseous elements then condense on the substrate, where they may react with each other. The main advantage of MBE is that all the processes such as sample preparation, catalyst deposition and nanowire growth can be achieved in UHV condition. Before presenting the MBE growth environment, the UHV systems used in this work is introduced.

UHV systems

Ultra High Vacuum (UHV) is the vacuum regime characterized by pressures lower than about 10^{-9} mbar. UHV requires the use of particular pumping elements in creating and maintaining vacuum that can be reached through the bake out of the entire system to remove water and other gas trace adsorbed on the surfaces of the chamber. Based on this UHV environment, many surface analytic techniques can thus be integrated.

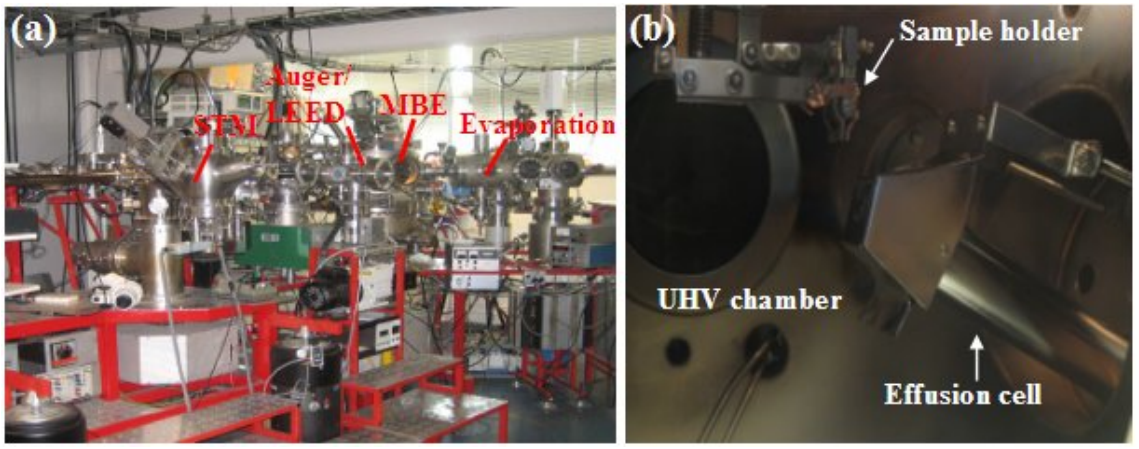

Figure 2.2: (a) RT-STM UHV system in IEMN; (b) MBE growth chamber in RT-STM.

Two UHV systems are used in this work and are named with respect to the type of scanning tunneling microscope (STM) that is hosted inside the system, one of which is the Room-Temperature (RT) STM system in IEMN shown in Fig.2.2(a), while the Low-Temperature (LT) STM system will be introduced in the next part. This system contains several chambers, one is equipped with an Omicron RT-STM, the other is a MBE growth chamber equipped with the analysis tools as low energy electron diffraction (LEED), and an evaporation chamber with a furnace in which metals like Au and Pt can be evaporated by Joule effect. The base pressure of the UHV system is typically below 10^{-10} mbar which is maintained by the ion getter pump and Titanium Sublimation Pump (TSP). All the UHV chambers are made

of stainless steel and contain several apertures in order to connect them to other chambers. Copper gaskets are used in order to avoid leaks.

Using this UHV system, samples can thus be transferred, prepared and analyzed all *in situ*: for example, Si substrate can be thermally cleaned and reconstructed in UHV environment, on which metal can be then evaporated to form metal-induced surface reconstruction or nanostrutures. These samples can be analyzed by LEED to determine the surface reconstruction or directly scanned by STM. Finally, Si nanowires can be grown in the MBE growth chamber.

MBE growth chamber

Based on the RT-STM UHV system, a MBE-Komponenten GmbH effusion cell with integrated cooling shroud and shutter is installed in the main UHV chamber, shown in Fig.2.2(b). Samples are transfered by manipulators. Sample holders are designed in the way that semiconductor samples can be heated by directly passing a current through the sample. The Effusion Cell is designed for elemental and compound evaporation or sublimation in the temperature range 200 °C to 1400 °C under the control of a thermocouple. The evaporant in the crucible is heated by tantalum or tungsten wire filaments and the heater is shielded by multiple layers of tantalum foil. A temperature stability of ± 0.1 °C and therefore very stable flux rates can be achieved with this cell. Standard crucible material is PBN (pyrolytic boron nitride), which is a very clean and stable ceramic material.

In our experiments, Si wafers are sublimated in the effusion cell by Joule effect and Si atoms will be then deposited with an angle of 60 ° on the Si sample with metal catalysts for the subsequent Si nanowire growth.

2.2 Characterization tools

In order to study the physical, chemical and electrical properties of Si nanowires, numerous characterization tools have been used which are introduced in the following.

2.2.1 Scanning Tunneling Microscopy and Spectroscopy

When in 1981 G.Binnig presented for the first time their idea of a scanning tunning microscope (STM) [35], they opened a door to a new and powerful tool for the analysis of surfaces. Shortly after, they demonstrated the capability of the STM to image surfaces with atomic resolution [36] and showed that this new tool is able to answer complex physical questions. Following these revolutionizing results, a rapid development started that led to a multitude of investigations using STM. Since then, several related methods have been developed, such as atomic force microscopy (AFM) [37] and electrostatic force microscopy (EFM) [38].

All of these techniques have in common that they use a probe to observe locally physical properties down to atomic lateral resolution. The data is thereby obtained by scanning a grid of points on the surface and combining the detected physical properties into an image using the data to code each point of the image. Because

of this scanning mechanism, all these techniques are summarized as scanning probe microscopes (SPM). The purpose of this part is to give a short introduction to STM, and its spectroscopic capabilities.

Tunnel effect

In 1924, De Broglie's idea of 'matter as wave' suggests that not only light but every piece of matter also has an undulatory nature. This theory had several important consequences, especially on the use of electron in microscopy: since their wavelength is much smaller than that of photons, they can thus be focused on small objects with a better resolution.

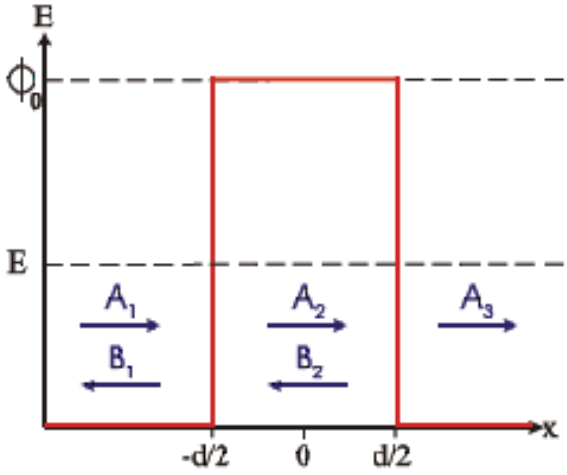

Figure 2.3: Schematic 1D tunnel barrier of width d and energy of Φ_0 in the x direction, the y and z directions are infinite.

Another phenomenon resulting from this wave-particle duality is that the particles of energy E can penetrate into a barrier of energy $\Phi_0 > E$, and even cross it if the barrier is thin enough, which is called the tunnel effect. A simplified demonstration is presented in Fig.2.3, where two metallic electrodes are separated by a square potential barrier in the one-dimensional case. The electron of energy $E < \Phi_0$ are described by their wave functions ψ_1, ψ_2 and ψ_3 that verify Schrödinger's equation in their respective region:

$$\begin{aligned} \frac{-\hbar^2}{2m}\frac{d^2\psi_1}{dx^2} &= E\psi_1 \\ \frac{-\hbar^2}{2m}\frac{d^2\psi_2}{dx^2} + \Phi_0\psi_2 &= E\psi_2 \\ \frac{-\hbar^2}{2m}\frac{d^2\psi_3}{dx^2} &= E\psi_3 \end{aligned} \tag{2.2}$$

The general solution in this case are:

$$\begin{aligned} \varphi_1(x) &= A_1 e^{ikx} + B_1 e^{-ikx} \\ \varphi_2(x) &= A_2 e^{\alpha x} + B_2 e^{-\alpha x} \\ \varphi_3(x) &= A_3 e^{ikx} \end{aligned} \tag{2.3}$$

where A_i and B_i are the incident and reflected part of each wave with i=1,2,3, while $k = \sqrt{\frac{2m}{\hbar^2}E}$ and $\alpha = \sqrt{\frac{2m}{\hbar^2}(\Phi_0 - E)}$.

The probability that an electron crosses the barrier (transmission coefficient) is given by:

$$T(E) = \left|\frac{A_3}{A_1}\right|^2 = \frac{1}{1 + \frac{\Phi_0^2}{4E(\Phi_0 - E)} sh^2(\alpha d)} \tag{2.4}$$

The fact that T(E) is not zero shows that electrons are able to cross a vacuum barrier thanks to their undulatory nature and the possibility of crossing the barrier depends on its thickness d. Moreover, with assuming electrodes made up of tungsten ($\Phi_0 = 4.5$ eV), at small energy, $\alpha = \sqrt{\frac{2m}{\hbar^2}(\Phi_0 - E)} \approx 1\mathring{A}^{-1}$. As a result, when the barrier d increase of $1\mathring{A}$, the transmission coefficient decreases by a factor of e^{-2}. The transmission coefficient can thus be simplified to:

$$T(E) \approx \frac{16E(\Phi_0 - E)}{\Phi_0^2} exp(-2d\sqrt{\frac{2m}{\hbar^2}(\Phi_0 - E)}) \tag{2.5}$$

This variation of the current versus distance was measured by G. Binnig and H. Rohrer when they demonstrated tunneling through a controllable vacuum gap in 1982 [35], as the origin of STM. The next part demonstrates the principles of such a tool.

Principles of STM

The STM uses the tunneling effect to obtain a current between a sharp tip and the sample by applying a voltage between both of them, before tip and sample come into contact. This tunneling current is held constant by processing it in an electrical feedback loop that compares it to a reference current and then varies the distance between tip and sample accordingly, moving the tip towards or away from the sample. When the tip is scanned over the surface, the tip height is determined by the local geometric and electronic structure of the surface and thus produces a surface map in the real space. The schematic representation of the tunnel junction in the real space is shown in Fig.2.4(a): an atomically sharp tip scans over a surface as the arrow shows. A tunneling current can thus be detected and only the last atom of the tip significantly contributes to the tunneling process.

Quantum mechanically, the system can be rationalized with the help of a one-dimensional simplification, demonstrated in Fig.2.4(b), where the sample as well as the tip are described by an ideal metal in which the electron states are filled up to the Fermi energy E_F. The two electrodes are separated by a small vacuum gap d.

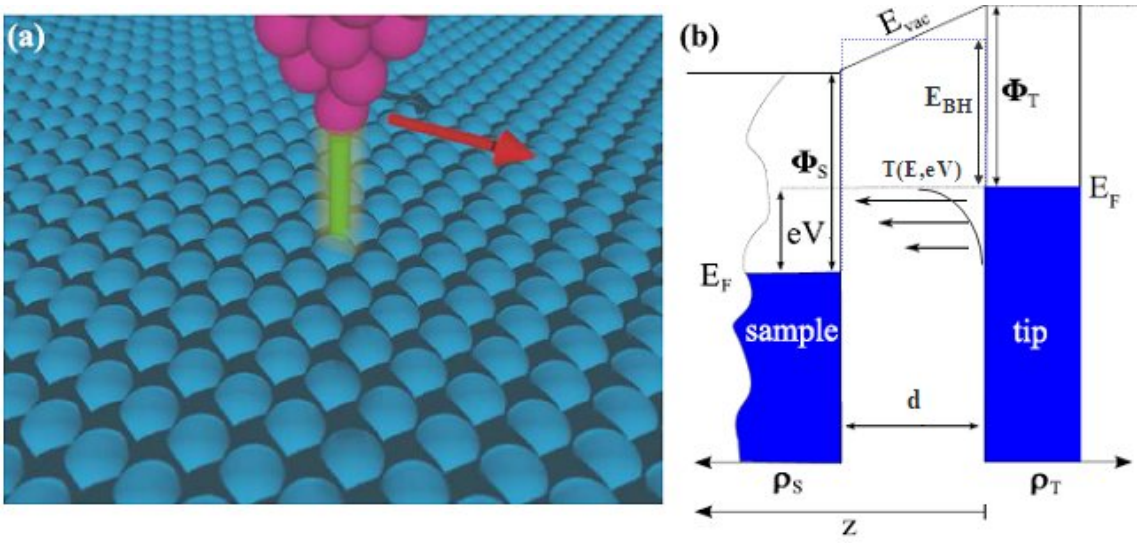

Figure 2.4: (a) Schematic representation of the tunnel junction. (b) Schematic diagram of the tunneling process between an ideal tip and a sample. ϕ_t and ϕ_s are the work functions of the tip and sample, eV is the bias, and if eV is small, the barrier can then be simplified as a square with a height E_{BH} (dash line) seen by the tip electron.

In order to measure the distance between both electrodes, a current is established by polarizing one electrode with respect to the other.

In order to calculate the current at a bias eV applied on the sample, we need to integrate the $T(E, eV)$ of the electrons across from $E_{FSample}$ to E_{FTip}=$E_{FSample+eV}$ at T=0K.

$$I = \int_0^{eV} T(E, eV)\rho_{tip}(E - eV)\rho_{sample}(E)\, dE \tag{2.6}$$

with ρ_{tip} and ρ_{sample} the local density of electronic states (LDOS) of respectively the tip and sample. Some approximations are usually taken to simplify the calculation and understanding:

1. The polarization of the electrodes is usually small compared to the height of the tunneling barrier. In such configuration, the trapezoidal barrier can be assimilated to a square barrier with the following characteristics:

$$E_{BH} = \frac{\Phi_t + \Phi_s}{2} - \frac{eV}{2} \tag{2.7}$$

2. The distance d between the tip and sample in STM is expected to be in the order of a few Angström. In this configuration, integrating E_{BH} into the Φ_0 of Eq.2.5, the expression of $T(E, eV)$ becomes:

$$T(E, eV) \approx \frac{16(E - eV)[E_{BH} - (E - eV)]}{E_{BH}^2} exp(-2d\sqrt{\frac{2m}{\hbar^2}([E_{BH} - (E - eV)])}) \tag{2.8}$$

When Eq.2.8 is injected into Eq.2.6, the tunneling current becomes:

$$I \approx \int_0^{eV} \frac{16(E-eV)(E_{BH}-E+eV)}{E_{BH}^2} exp(-2d\sqrt{\frac{2m}{\hbar^2}(E_{BH}-E+eV)})\rho_{tip}(E-eV)\rho_{sample}(E)\,dE \tag{2.9}$$

and for biases much lower than the average barrier height, it yields:

$$I \approx 16exp(-2d\sqrt{\frac{2m}{\hbar^2}E_{BH}}) \int_0^{eV} \frac{E-eV}{E_{BH}} \rho_{tip}(E-eV)\rho_{sample}(E)\,dE \tag{2.10}$$

The above equation demonstrates the exponential dependence of the current against distance. For example, tungsten electrodes, which have a work function of Φ = 4.5 eV, giving a decay constant of $\sqrt{\frac{2m}{\hbar^2}E_{BH}} \approx 1\ \mathring{A}^{-1}$. It means that an increase of 1 $\mathring{A}$ of the tip-sample distance leads to a change of the current by a factor $e^{-2} \approx 0.1$. Such exponential dependence of the current provides enough precision to detect atomic-scale variations.

Spectroscopy

One of the most fascinating potentials of STM is its capability to obtain spectroscopic data with its atomic resolution. Eq.2.10 shows that the tunnel current I depends on the bias V and the tip-sample distance d. In the topographic mode: V is fixed and the desired current I is regulated against d by the feedback loop at every point scanned by the tip. In spectroscopic mode, the tip is stopped at one specific place and one of the three values d, I, V is ramped while one other is kept constant and the last one is measured. In this study, we performed spectroscopic measurements of the elastic current versus bias $I(V)$.

This mode generally implies that the feedback loop is opened, a constant tip-sample distance. The tip is considered atomically sharp, with a s-like orbital for the apex atom. In these conditions, the density of states of the tip can be assumed constant, the expression of tunnel current becomes:

$$I \propto \rho_{tip} \int_0^{eV} T(E,eV)\rho_{sample}(E)dE \tag{2.11}$$

thus

$$\frac{\partial I}{\partial V} \propto e\rho_{tip}\rho_{sample}T(eV,eV) + e\rho_{tip}\int_0^{eV} \frac{d}{deV}[T(E,eV)]\rho_{sample}(E)dE \tag{2.12}$$

The above expression is dependent on the sample density of states. But the exponential increase of the signal against bias due to the influence of $T(E,eV)$ induces a larger contribution of the states lying at higher energy with respect to the states closer to the Fermi level when $V > 0$. This effect is significant for semiconductors, where higher bias are used in comparison to metals. Feenstra er al [39] have shown that the differential conductance can be normalized by the ratio I/V in order to cancel the exponential dependence because of $T(E,eV)$:

$$\frac{\frac{\partial I}{\partial V}}{\frac{I}{V}} \propto \frac{\rho_{sample}(eV) + \int_0^{eV} \frac{\partial}{\partial eV}[T(E,eV)]\frac{\rho_{sample}(E)}{T(eV,eV)}dE}{\frac{1}{eV}\int_0^{eV} \frac{T(E,eV)}{T(eV,eV)}\rho_{sample}(E)dE} \tag{2.13}$$

The second term of the equation is a slowly varying background term and as a result, the variations of $\frac{\partial I}{\partial V}$ as a function of V are mainly related to $\rho_{sample}(eV)$. Thus

$$\frac{\frac{\partial I}{\partial V}}{\frac{I}{V}} \propto \rho_{sample}(eV) \tag{2.14}$$

This relation provides a value that is proportional to the LDOS of the sample, independent of the tip-sample separation, from $I(V)$ curves. Moreover, in most tunneling spectroscopy experiments, the dI/dV signal is detected with the help of a Lock-In technique since the tunnel current is often too noisy to obtain reasonable data with this numerical method. The details of the Lock-In technique can be found in [40].

The Omicron LT-STM

As described before, two STM-UHV systems are used in this work: RT-STM with LEED, and LT-STM. The Low-Temperature Omicron GmbH STM shown in Fig.2.5(a), with which we can get a more stable condition and higher spectral resolution, is presented here.

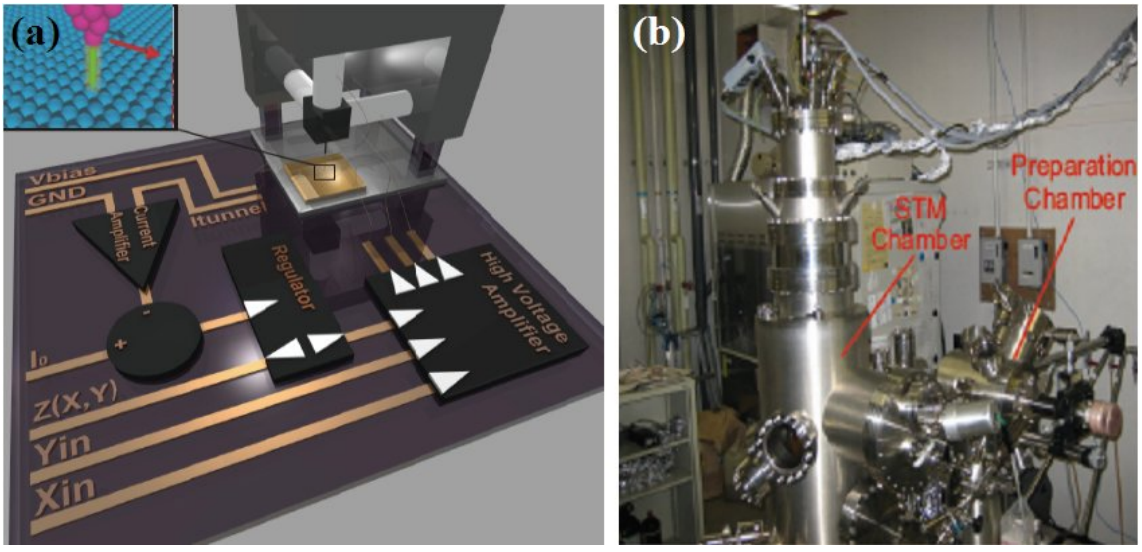

Figure 2.5: (a) Simplified schematics of a STM system, (b) LT-STM system.

A simplified schematics of a STM system is shown in Fig.2.5(a): on the top right side, the tip is mounted on a piezo tripod (three white cylinders, respectively X,Y and Z) over the sample. The polarization is done through the inputs V_{bias} and GND, respectively connected to the sample and to the tip. The tunnel current is collected on the tip side and amplified by a current amplifier. The output signal is

then compared to the reference current I_0 to produce the error signal I-I_0 that will drive the regulator. Topographic changes are given by the $\log(I - I_0)$. Modulations of the tip-sample distance can be regulated through the elongation or contraction of the Z piezo based on the proper choice of the gains in the feedback loop. In order to allow lateral movements of the tip, the two inputs X_{in} and Y_{in} drive the X and Y piezo motion. If zooming on the tunnel junction, the same configuration similar to Fig.2.4(a) can be observed, shown in the inset of Fig.2.5(a).

In the LT-STM, in addition to the pumping system which produces a base vacuum of 5×10^{-11} Torr, two cryostats are connected to the STM to cool down the system. One cryostat (outer) acts like a shield and is filled with Nitrogen only, whereas the other one (inner) can be refilled with Nitrogen or Helium depending on the temperature range to be used. The microscope can thus be operated over a broad range of temperatures, from 4K (liquid Helium temperature)to 77K (liquid Nitrogen temperature). In addition to perform low temperatures, the cryostats act as cryogenic traps for remaining contaminants in the chamber, lowering the pressure in the STM head. On some kinds of variable temperature heads, only the sample is cold, therefore the piezo motors and the tip are at room temperature. This has two inconvenients: lateral drift by the piezos and thermal broadening against the energy when doing spectroscopy. The main advantage of the LT-STM is that all active parts are thermalized: the tip, the sample and piezo motors are kept at the same temperature, so better results at a fixed temperature can be obtained.

In conclusion, the ability to image the sample surface in atomic resolution and detect the sample LDOS using spectroscopy, and specially, the stability brought by the cooling system makes the LT-STM an ideal tool for the analysis of nanoscale objects. In this work, the LT-STM was used to analyze the surface structure of Si nanowire at atomic scale and spectroscopy of either $\frac{dI}{dV}$ or $\frac{\frac{\partial I}{\partial V}}{\frac{I}{V}}$ was used to study the electronic structure of the nanowire sidewalls depending on their electronic characters.

2.2.2 Electron Microscope

Electron microscope is a type of microscope that uses electrons to illuminate a specimen and create an enlarged image. Electron microscopes have much greater resolving power and much higher magnifications than light microscopes, which is due to the wavelength of the electron, its de Broglie wavelength, being much smaller than that of a light photon. Two electron microscopes: SEM and TEM are used in this work. Before introducing these microscopes, the basic principle of electron microscopy: the electron-atom interaction is firstly explained.

Electron-Atom interaction

Electron-atom interaction is what makes electron microscope possible. The energetic electrons in the microscope strike the sample and various reactions can occur as shown in Fig.2.6(a). The reactions noted on the top side of the diagram are utilized when examining thick or bulk specimens (SEM), while the bottom side are

those examined in thin or foil specimens (TEM). The interaction volumes for various electron-atom interactions are illustrated in Fig.2.6(b). The formation and use of some important electron-atom reactions that were used in our experiments are described in more details in the following.

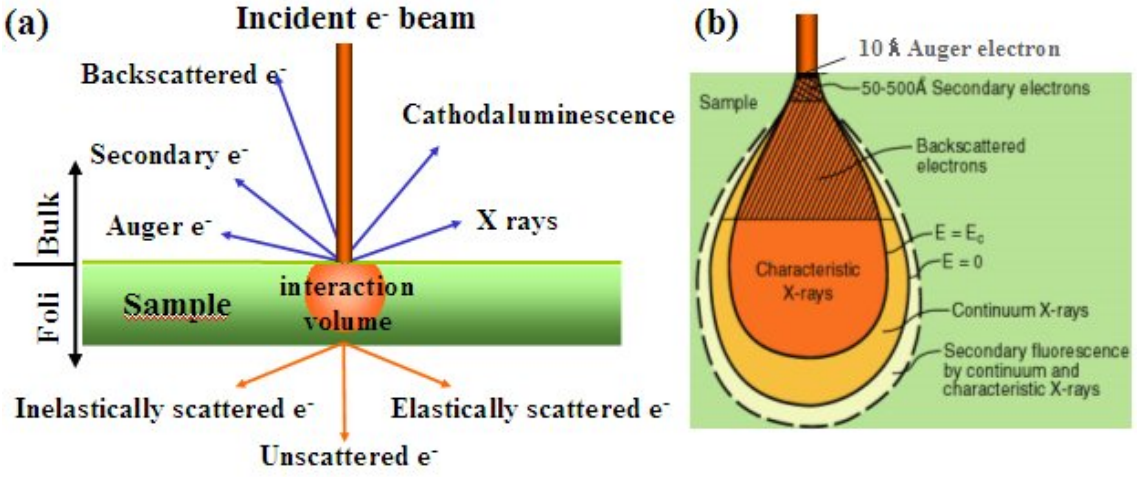

Figure 2.6: (a) Effects produced by electron bombardment of a material; (b) Illustration of interaction volume for the electron-atom interactions

- **Bulk Specimen Interaction**

  - Secondary electrons: When an incident electron passes near an atom in the specimen, it will impart some of its energy to a lower energy electron, causing the ionization of the electron in the specimen atom, which then leaves the atom with a very small kinetic energy (5 eV). Production of secondary electrons is very topography related. Due to their low energy, only secondaries that are very near the surface (< 50 nm) can exit the sample and be examined. Any changes in topography in the sample that are larger than this depth will change the yield of secondaries due to collection efficiencies.

  - Backscattered electrons: When an incident electron collides with an atom in the specimen, it will be then scattered 180 degrees. The production of these electrons varies directly with the specimen's atomic number.

  - X-rays: Caused by the de-energization of the specimen atom after a secondary electron is produced, X-rays emitted from the atom will have a characteristic energy which is unique to the element from which it originated.

- **Thin Specimen Interaction**

  - Unscattered electrons: Incident electrons which are transmitted through the thin specimen without any interaction. Areas of specimen that are thicker will have fewer electrons and so will appear darker, conversely the thinner areas will appear lighter.

  - Elastically scattered electrons: All these electrons are scattered according to Wavelength $= 2 \times$ Space between atoms in the specimen $\times$ sin(angle

of scattering). All incident electrons having the same energy (wavelength) will be scattered by the same atomic spacing, thus having the same scattered angle. These similar angle scattered electrons can be collected using magnetic lenses to form a pattern of spots which can then yield informations about the orientation and atomic arrangement.

- Inelastically scattered electrons: Incident electrons that interact with specimen atoms in an inelastic fashion, loosing energy during interaction. The inelastic loss of energy is characteristic of the elements that were interacted with, which is used in the electron energy loss spectroscopy (SSLS).

Scanning Electron Microscope

Scanning electron microscope (SEM) produces images by probing the sample with an electron beam with an energy ranging from a few hundred eV to 40 keV. The electron beam is provided by the electron gun with three main types: Tungsten hairpin, LaB_6 and Field emission gun (FEG), the latter one producing electron beam with a better brightness and smaller beam size. The electron beam is then focused by one or two condenser lenses to a spot about 0.4 to 5 nm in diameter. The beam passes through pairs of deflector plates in the electron column, which deflect the beam in the X and Y axes so that it scans in a raster fashion over a rectangular area of the sample surface. At each point of sample, the incident electron beam interacts with the sample, resulting in the reflection of backscattered electrons, emission of secondary electrons and emission of electromagnetic radiation, each of which can be detected by specialized detectors. Electronic amplifiers are used to amplify the signals which are displayed as variations in brightness on a cathode ray tube (CRT). The raster scanning of the CRT display is synchronized with that of the beam on the sample, and resulting image is therefore a distribution map of the intensity of the signal being emitted from the scanned area of the sample. A simplified schematic of SEM column is shown in Fig.2.7(a).

In this work, the SEM Zeiss Ultra 55 in IEMN is used. This SEM is equipped with a FEG and is maintained at a base pressure of 10^{-5} mbar. The acceleration voltage is 200 eV - 30 keV and the resolution is 1 nm at 15 keV. It is equipped with 2 types of detectors:

- Secondary electrons (SE): An Inlens detector is located inside the electron column and is arranged rotationally symmetric around the optical axis. Due to a sophisticated magnetic field at the pole piece, the secondary electrons are collected with high efficiency and images with high contrast can thus be obtained. The topography of the Si nanowires was observed by this mode.

- Backscatter electron (BSE): The backscatter coefficient (ratio of the number of BSEs to the number of electrons incident on the sample) shows a monotonic increase with atomic number (Z). Areas of the specimen composed of higher atomic number elements emit more backscatter signal and thus appear brighter in the image. This mode allows the identification of the Au catalysts on Si nanowires.

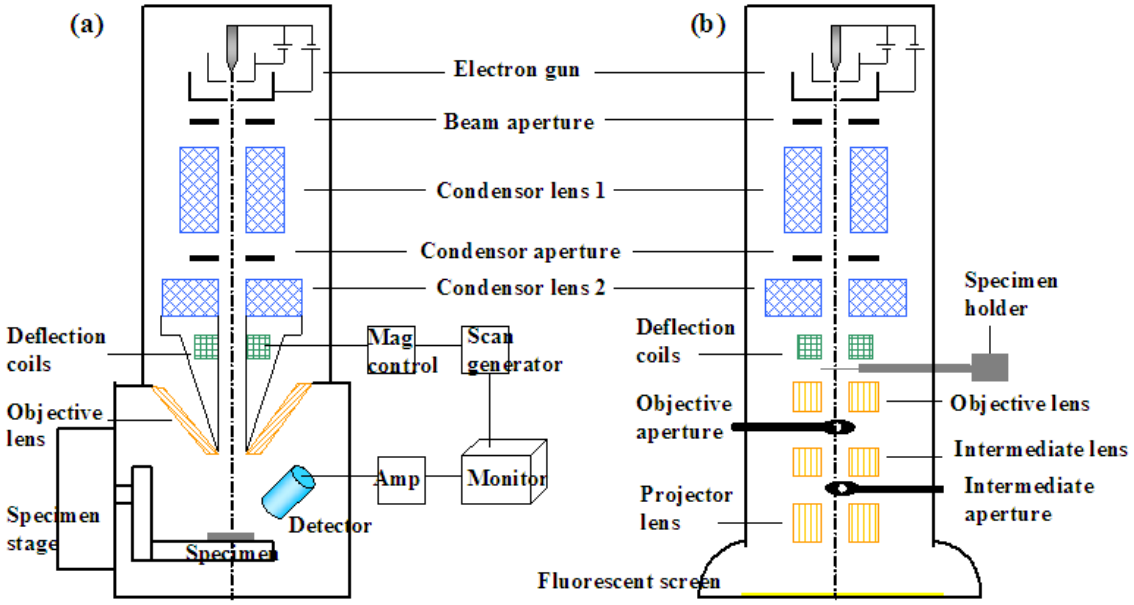

Figure 2.7: (a) Schematic of the SEM column; (b) Schematic of the TEM column.

Transmission Electron Microscope

Unlike the SEM, the transmission electron microscope (TEM) uses a relatively higher voltage (40 keV to 400 keV) electron beam to create an image. The electron beam with high energy is transmitted through the sample, where part of the electrons becomes scattered. When it emerges from the sample, the electron beam carries information about the sample structure that is magnified by the objective lens system. The spatial variation in this information is viewed by projecting the magnified electron image onto a fluorescent viewing screen coated with a phosphor or scintillator material such as zinc sulfide. The schematic of a TEM column is shown in Fig.2.7(b). Generally, two work modes are used: Scanning-TEM mode and diffraction mode. In the former, the electron beam is scanned over a defined area of the sample. At each point, the generated signal is simultaneously recorded by selected detectors, building up an image. More details are presented in the following:

- Bright field (BF): In this mode, as shown in Fig.2.8(a), an aperture is placed in the back focal plane of the objective lens which allows only the unscattered beam to pass. Therefore, mass thickness and diffraction contrast contribute to image information: thick area in which heavy atoms are enriched and crystalline areas appear with dark contrast. The BF detector is placed at the same site as the aperture and detects the intensity in the direct beam from a point on the specimen.

- Dark field (DF): In DF images, as shown in Fig.2.8(b), the direct beam is blocked by aperture while one or more diffracted beams are allowed to pass the objective aperture. Since diffracted beams have strongly interacted with the specimen, very useful informations about planar defects, stacking faults or particle size are presented. An annular dark field (ADF) is always used to collect more effectively the diffracted beams, which is a disk with a hole in the center where BF detector is installed.

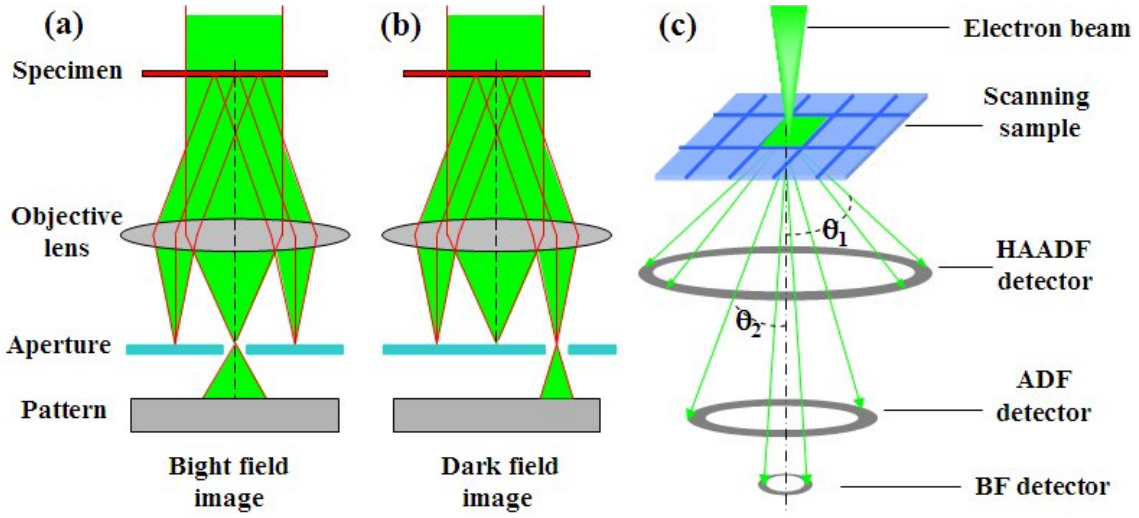

Figure 2.8: (a) Bight field mode; (b) Dark field mode; (c) Schematic of the STEM mode.

- High-angle annular dark field (HAADF-STEM): The strong Coulomb interaction of the incident electrons with the potential of an atom core, leads to high angles scattering (Rutherford scattering) or even to backscattering. The fact that the probability of such scattering events rises for heavier atoms (with a high atomic number Z), offers the possibility for obtaining chemical contrast. This means that areas or particles containing high Z elements scatter stronger and thus appear bright in images recorded with electrons scattered into high angles or even backwards. This effect is employed in HAADF STEM and in SEM using backscattered electrons (BSE). By the HAADF-STEM method, small clusters (or even single atoms) of heavy atoms (for example in catalysts) can be recognized in a matrix of light atoms since contrast is high (approximately proportional to Z^2). The HAADF detector is also a disk with a hole, but with a larger diameter and a closer position to the sample than the ADF detector, so the diffracted electrons with an angle $\theta_1 > \theta_2$ can thus be collected, as shown in Fig.2.8(c).

- High-resolution TEM (HRTEM): This mode refers to imaging in which lattice fringes are observed or atomic resolution is achieved. Unlike BF or DF TEM, HRTEM images are formed from a number of diffracted beams. This multi-beam approach is known as phase-contrast imaging, and is necessary to construct an image of the crystal lattice. HRTEM provides access to much information about the sample, such as analyzing crystalline defects and interfaces at the atomic scale, and observing nanoscrystals and nanostructures. The technique typically requires very thin TEM specimens free of preparation artifacts. Additionally, correct interpretation of HRTEM images may depend upon image simulation to overcome spherical aberration, a resolution up to 0.08 nm [41] has already been obtained.

In this work, the TEM analysis were carried out in two other laboratories: group LSPES, Université des Sciences et Technologies de Lille and group EMAT, University of Antwerp. More specifically, the HAADF-STEM are used to identify the presence of Au clusters on the nanowire surface, while the HRTEM is used to analyze the bulk structure of Si nanowires.

2.2.3 Low Energy Electron Diffraction

Low-energy electron diffraction (LEED) is a technique for the determination of the surface structure of crystalline material. If a crystal is cut along a certain plane, then the atoms near the surface may well be disturbed from their equilibrium positions in the bulk. This leads to changes in the relative positions of the near surface atoms (surface reconstruction). Such changes can be explored with LEED. Due to the short mean free path, low-energy electrons are diffracted only by a few atomic layers of the surface, what leads to Bragg rods perpendicular to the surface in the reciprocal space. As shown in Fig.2.9(a), the scattering vector $\mathbf{Q}$ and consequently the wave vector for the diffracted electrons $\mathbf{k}_f$ are selected by the intersection of the Bragg rods with the Ewald sphere, whose size varies as a function of the electron energy. Therefore, the surface crystallographic structure can be determined by bombarding the surface with a collimated beam of low energy electrons (10-150 eV) [42] and observing diffracted electrons as spots on a phosphorescent screen. The relative positions of the spots on the screen reveal the symmetry and dimensions of the surface unit cell. The average intensity and sharpness of the spots reveal the degree of ordering of the surface.

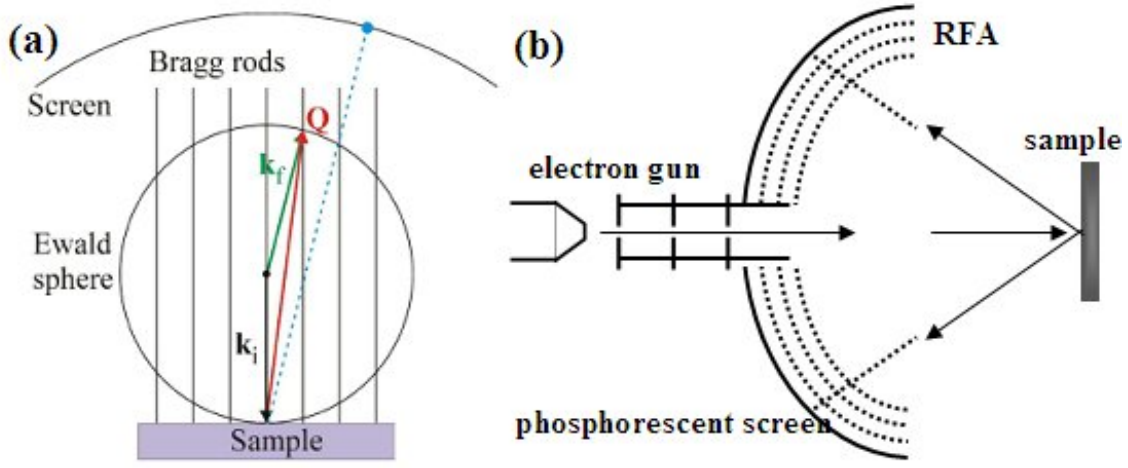

Figure 2.9: (a) Principle of LEED; (b) Schematic of a LEED set-up

Fig.2.9(b) presents a simplified schematic of a LEED setup. In order to keep the sample clean and free from unwanted adsorbates, LEED experiments are performed in the UHV environment. Monochromatic electrons are emitted by a cathode filament which is at a negative potential. The electrons are accelerated and focused into a beam by a series of electrodes serving as electron lenses. A retarding field analyzer (RFA) is used to block inelastically scattered electrons. Some of the electrons incident on the sample surface are backscattered elastically, and diffraction can be detected on the phosphorescent screen if a periodic atomic arrangement exists on the surface.

In this work, LEED is used to analyze the atomic reconstructions of Au/Si(111) surfaces.

2.2.4 Atom Probe Tomography

The atom probe tomography (APT) is a material analysis technique able to give a 3D virtual image of the analyzed atoms with a near-atomic spatial resolution in a volume smaller than 1 um^3 [43]. Such a capability could make the APT a key tool in the development of nano-electronics, more specifically, the distribution of the doping species in 3D and with a spatial resolution better than a nanometer.

In APT, the tip-shaped sample is ablated atom per atom by the effect of a high electric field at the surface submitted to a superposition of a standing high voltage (DC) and high voltage pulses (HV). This process is called field evaporation. The radius of curvature R of the tip has to be between 30 and 100 nm. The nature of the emitted ionized atoms is determined by Time of Flight Mass Spectrometry (TOF-MS). These atoms are received by a Position Sensitive Detector (PSD) The arrival positions of atoms are directly linked to their original positions at the surface, enabling the 3D reconstruction of the probed volumes after analysis. The principle of the tomography analysis is shown in Fig.2.10.

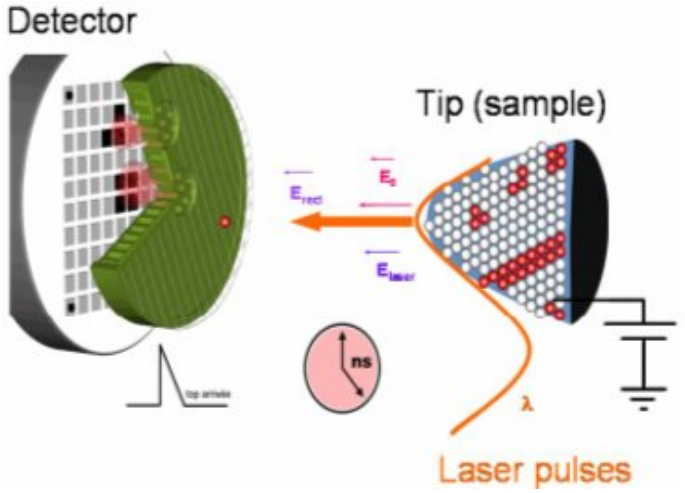

Figure 2.10: Illustration of tomography process

However, since HV pulses are used, samples have to be electrically good conducting material. Thus the APT is not really adapted to the analysis of semiconductors. In order to overcome this inconvenient, laser pulses are used in place of the HV pulse and make it possible to analyze the semiconductor materials. But the field evaporation in pulsed laser TAP is generated by the fast temperature rise due to a sub-nanosecond laser pulse used to ablate surface atoms. As a consequence, the temperature variation of the tip surface generates atom migration, degrading the spatial resolution of the PL-APT. More recently, the femtosecond lasers overcome this shortcoming [44]. The femtosecond duration of the laser pulses is shorter than the electron-phonon coupling time, usually of the order of a few tens of picosecond at the cryogenic temperature used in APT. By combining a standard APT to a femtosecond laser, it is possible to obtain excellent performance: the mass resolving power of the instrument can be increased by a factor 3.

In this work, the tomography analysis is used to study the chemical composition of Si nanowires, specially the dopant distribution in nanowires. The experiments

were carried out in Group GPM of University of Rouen using their femosecond laser assisted APT system (CAMECA).

2.2.5 Glove box with electrical measurement system

This glove box with electrical measurement system is used to electrically characterize samples in a dry, oxygen free environment. The system consists of three parts:

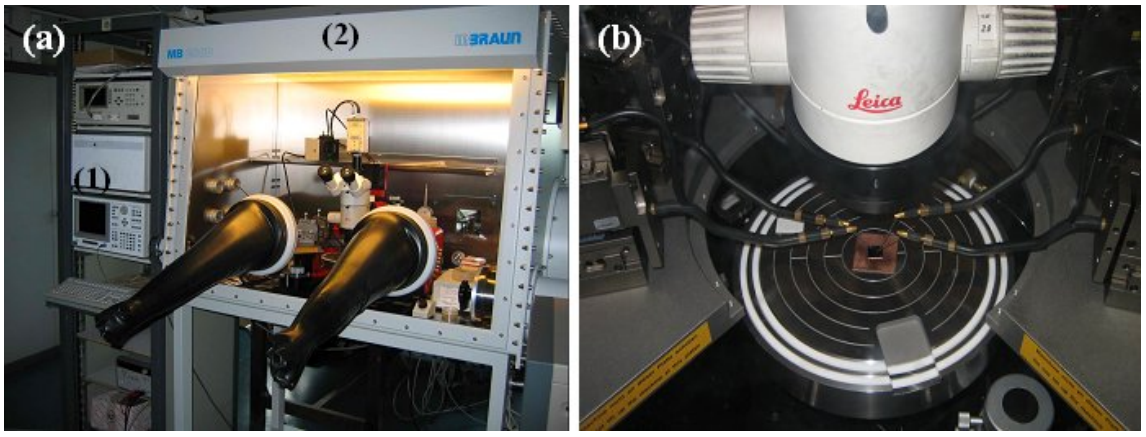

Figure 2.11: (a) Glove box with the electrical characterization system in IEMN; (b) Photography of the probe station.

- Hewlett-Packard 4155 C semiconductor parameter analyzer for the electrical characterization. The HP 4155 C contains four SMU (source units), each of which can be programmed to be a voltage source, a current source, or a ground. It reaches a current resolution of 1 fA and the accuracy of 20 fA. All measurements are displayed on the color CRT screen. This instrument is shown in Fig.2.11(a)-(1)

- Glove box: a glove box is a sealed container that allow one to manipulate objects while being in a different atmosphere from the objects. Build into the sides of the glove box are two gloves arranged in such a way that the user can place his hands into the gloves and perform tasks inside the box. In this work, a Braun glove box is integrated with the electrical measurement, shown in Fig.2.11(a)-(2)

- Probe station: four tungsten probes are used to connect the sample for the electrical measurement. The position of the probe is controlled by the manipulator, shown in Fig.2.11(b).

In this work, the electrical properties of Si nanowires are measured in this glove box.

2.3 Microfabrication techniques

Microfabrication is the term to describe processes of fabrication of miniature structures, of micrometer sizes or smaller. Historically the earliest microfabrication was used for semiconductor devices in integrated circuit fabrication. Practical advances in microelectromechanical systems (MEMS) and nanotechnology, where the technologies from IC fabrication are being re-used, adapted or extended, have led to the extension of the scope and techniques of microfabrication. In this work, microfabrication processes are used to fabricate some microstructures, on which the Si nanowires will then be localized. All these processes have to be achieved in a cleanroom, which is an environment having a low level of environmental pollutions such as dust, airborne microbes, aerosol particles and chemical vapors, typically used in manufacturing or scientific research. More accurately, a cleanroom has a controlled level of contamination that is specified by the number of particles per cubic meter at a specified particle size.

IEMN hosts a class 100 cleanroom of 1600 m^2, where numerous technological facilities exist. In this part of chapter, the main microfabrication processes such as lithography, etching and deposition are described.

2.3.1 Electron Beam Lithography

Electron beam lithography (EBL) is the process of scanning a beam of electrons in a patterned fashion across a surface covered with resist (exposing) where either exposed or non-exposed regions of the resist can be selectively removed (developing). The purpose is to create very small structures in the resist that can subsequently be transferred into another material. The primary advantage of EBL is its resolution. Indeed it surpasses the diffraction limit of light and make features in the nanometer regime, with resolution up to 5nm [45]. On the other hand, comparing to the conventional photolithography, the key limitation of EBL is its throughput: it takes a very long time to expose an entire silicon wafer. Moreover, several limitations such as proximity effect [46] also limit the resolution of EBL, specially for the sub-10 nm nanostructures. In this work, e-beam lithography has been chosen to pattern the microstructures such as micropillars and microtrenches in despite of its low throughput, because the form of our masks have to be changed a lot in the different experiments. If we use the photolithography, a new mask has to be made every time, which is even more time-consumed and costly.

The EBL system uses the same kind of electron source as the electron microscope system (see 2.2): electrons emitted from either thermionic source or field emission sources, are focused by the electrostatic and magnetic lenses into a fine electron beam. For very small beam deflections, electrostatic deflection lenses are used, larger deflections require stage movements. At IEMN, EBL is a core technology which has been developed since 1984 and there are presently two lithography systems: a VISTEC EBPG5000Plus and a VISTEC EBP5000PlusES. The latter consists of a high resolution Gaussian beam system, a FEG, a 50MHz pattern generator and an acceleration voltage of 20 kV, 50 kV or 100 kV. A ultimate resolution of sub-10 nm has been reached with this system for the top-down fabrications of nanowires [47].

2.3.2 Etching

Reactive Ion Etching

Reactive ion etching (RIE) is an etching technology that uses chemically reactive plasma to remove material deposited on wafers. The plasma is generated under low pressure by an electromagnetic field. High-energy ions from the plasma attack the wafer surface and react with it.

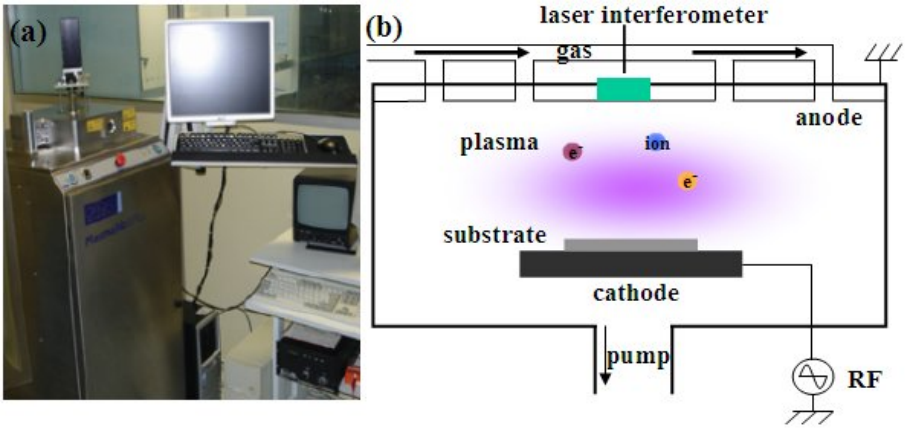

Figure 2.12: (a) Oxford plasmalab 80+ RIE system in IEMN; (b) Schematic of the RIE chamber

Fig.2.12(a) shows a photography of the Oxford plasmalab 80+ system used in this work, and (b) is the schematic of the RIE chamber. The typical RIE system consists of a cylindrical vacuum chamber, with a wafer platter located at the bottom. The wafer platter is electrically isolated from the rest of the chamber, which is grounded. Gas enters through small inlets into the top of the chamber and exits to the vacuum pump system through the bottom. Plasma is initiated in the system by applying a strong radio frequency (RF) electromagnetic field (13.56 MHz) to the wafer platter. The oscillating electric field ionizes the gas molecules by stripping them of electrons, creating a plasma. In each cycle of the field, the electrons are electrically accelerated up and down in the chamber, absorbing into the wafer platter and causing the platter to build up charge due to its DC isolation. This charge develops a large negative voltage on the platter, so the plasma, more specifically, the positive ions tend to drift toward the wafer platter and react with the sample. There are two types of etching processes between plasma and sample:

- Chemical etching: The ions react at the surface of the material being etched, forming another gaseous material which will be evacuated by the pumping system. The chemical etching is isotropic.

- Physical etching: If the ions have high enough energy, they can knock atoms out of the material without a chemical reaction. The physical etching is highly anisotropic.

It is possible to produce very anisotropic etch profiles by adjusting the balance between these two etching processes, since the chemical process depends on the pressure of the chamber, while the physical process depends on the polarization voltage. Moreover, an interferometer laser is used to control the etching, because the period of the signals detected will change when the material being etched changes.

Deep Reactive Ion Etching

Deep reactive ion etching (DRIE) is a highly anisotropic etch process used to create deep, steep-sided holes and trenches in wafers, with aspect ratios of 20:1 or more. There are two main technologies for high-rate DRIE: cryogenic and Bosch. The DRIE system used in this work is a STS ICP etching system with the Bosch process [48], so here, we will briefly introduce this process.

The Bosch process, also known as time-multiplex etching, alternates repeatedly between two modes to achieve nearly vertical structures:

- A standard, nearly isotropic plasma etch. The plasma contains some ions, which attack the wafer from a nearly vertical direction. (For Si, this often uses sulfur hexafluoride SF_6)

- Deposition of a chemically inert passivation layer. (For instance, C_4F_8 source gas yields a substance similar to Teflon)

Each phase lasts for several seconds. The passivation layer protects the entire substrate from further chemical attack and prevents further etching. However, during the etching phase, the directional ions that bombard the substrate attack the passivation layer at the bottom of the trench (but not along the sides). They collide with it and sputter it off, exposing the substrate to the chemical etchant. These etch/deposit steps are repeated many times over resulting in a large number of very small isotropic etch steps taking place only at the bottom of the etched pits. To etch through a 0.5 mm Si wafer, for example, 100-1000 etch/deposit steps are needed.

Anisotropic Wet Etching

In the microfabrication process, wet etching of silicon is used mainly for cleaning, shaping, polishing and characterizing structural and compositional features. Compared to dry etching, wet chemical etching provides a higher degree of selectivity, and is often faster. In anisotropic wet etching (typical etchants like KOH, TMOH), the etching rate is much faster in certain direction than in others, exposing the slowest etching crystal planes as etching time progresses, usually the (111) planes for silicon. Due to the etching rate dependence of orientation, anisotropic wet etching is often used to make V-grooves, silicon mesas and some free standing structures. SiO_2 can be used as mask for the wet etching as the selectivity of Si/SiO_2 is more than 500 [49]. Fig.2.13(a) shows the (111) planes can be formed with an angle of 54.7° to the Si (100) surface after etching, whereas the vertical (111) planes can be obtained after etching on the Si(110) substrate, as illustrated in Fig.2.13(b).

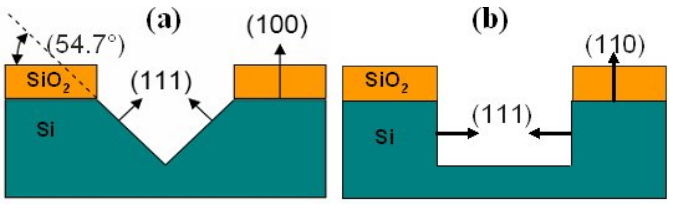

Figure 2.13: (a) Anisotropic wet etching on Si(100); (b) Anisotropic wet etching on Si(110); (c) Etch rate dependence on temperature

2.3.3 Metallic Deposition

In contrary to the CVD process at high temperature, the physical vapor deposition (PVD) process can be carried out at lower temperature and without corrosive gaseous products, so it is generally used for the metal deposition process.

Electron beam physical deposition (EBPVD) is a form of PVD in which a target anode is bombarded with an electron beam given off by a charged tungsten filament under high vacuum. The electron beam causes atoms from the target to transform into the gaseous phase. These atoms then precipitate into solid form, coating everything in the vacuum chamber with a thin layer of the anode material. Fig.2.14(a) shows a photography of the PLASSYS MEB 550S EBPVD machine in IEMN, and (b) illustrates the EBPVD system.

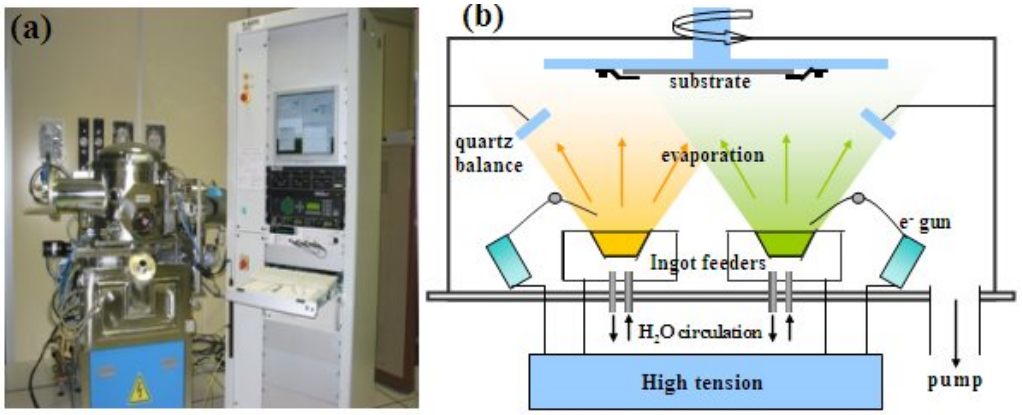

Figure 2.14: (a) PLASSYS MEB 550S EBPVD system in IEMN; (b) Schematic of the EBPVD system

In an EBPVD system, the deposition chamber is evacuated to a pressure of 10^{-4} mbar. The material to be evaporated is in the form of ingots. Electron beam can be generated by thermionic emission or field emission. The generated electron beam is accelerated to a high kinetic energy and focused towards the ingot. The kinetic energy of the electrons is mostly converted into thermal energy as the beam bombards the surface of the ingot, leading to the increase of the surface temperature of the ingot and resulting in the formation of a liquid melt. The liquid ingot material thus evaporates under vacuum and will deposit on the substrate on the top. A quartz crystal microbalance (QCB) is used to control the thickness of the film deposited. The frequency of oscillation of the quartz crystal is partially dependent on the thickness of the crystal. During the deposition, all the other influencing variables remain constant; thus a change in thickness correlates directly to a change in frequency, so the thickness of the deposition can be monitored. Moreover, the substrate can be rotated at a particular speed so that the film will be uniformly deposited. Numerous metals can be deposited using this technique, such as Au, Ti, Pt and Al. After the metallic deposition, a bi-layer resist process was used to obtain a cap profile of resist which would favor the lift off process in the next step.

In conclusion, using these microfabrication techniques, several kinds of microstructures such as Si micropillars and Si microtranches are fabricated, which will be used for the localized growth of nanowires, as it is described in Chapter 4.

2.4 Conclusion

In summary, all the techniques that were used in this thesis have been introduced. These techniques encompass various fabrication tools based on the bottom-up and top-down approaches to synthesize the Si nanowires and then allow their characterization and integration.

In order to understand the physical, chemical and electrical properties of Si nanowires, numerous characterization tools were then used. The bulk and surface structures of Si nanowires were observed by means of TEM and STM, the chemical composition, specially the dopant distribution of bore-doped Si nanowires was analyzed by TAP, while their electrical properties were studied by STS and the transport measurements. The outline of this work is shown in Fig.2.15.

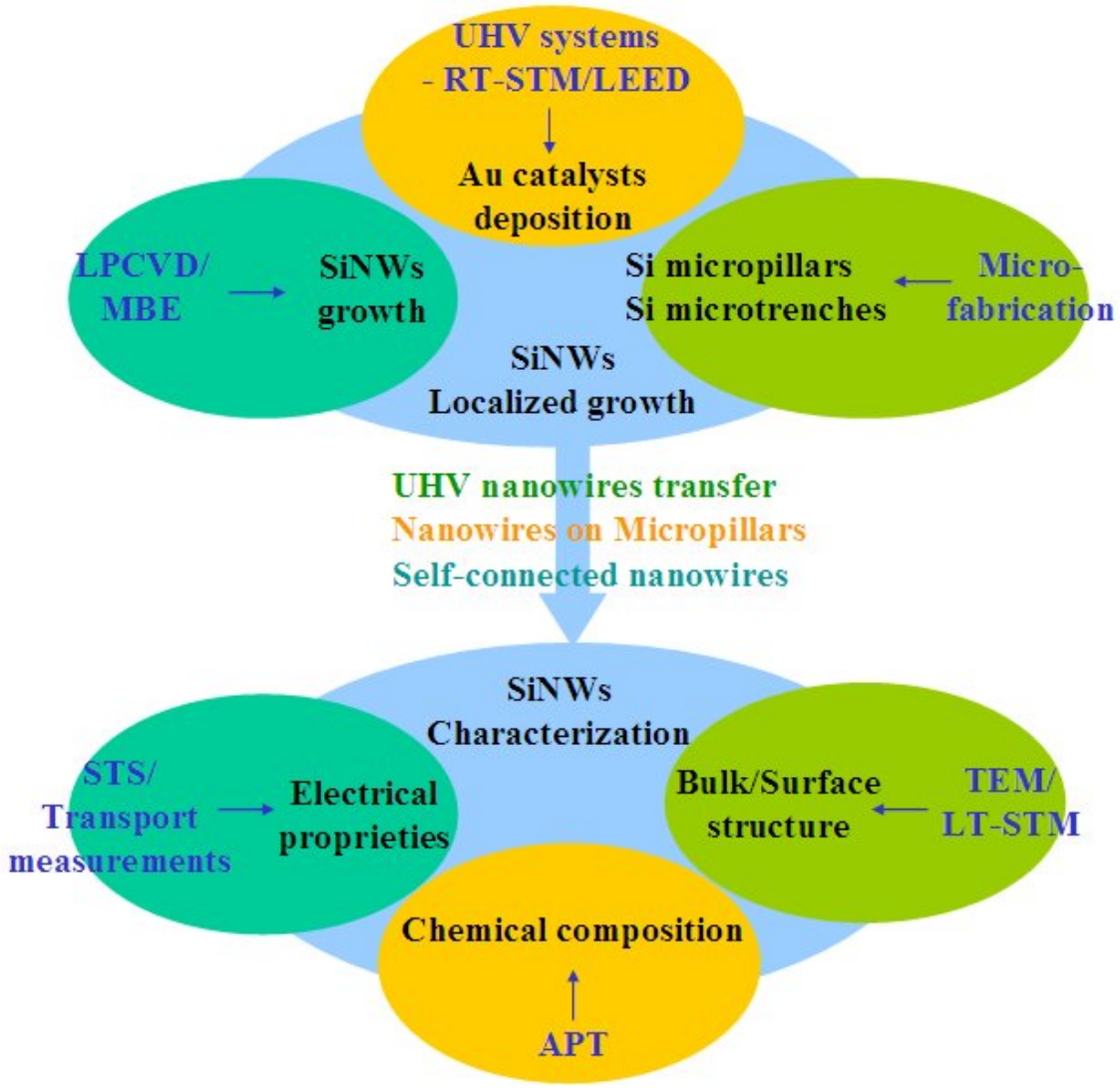

Figure 2.15: Outline of this work: localized growth and characterization of Si nanowires

Chapter 3

Au islands on Si (111)

Island growth on a flat surface plays an important part in surface growth since it forms the basis for all further growth [50]: for example, in the VLS nanowire growth, metallic nanoparticles, such as gold particles on silicon, behave as catalyst droplets in the presence of a silicon containing gas. They decompose the gas, so that the silicon atoms precipitate at the interface between the gold particle and the semiconductor surface, giving rise to a nanowire growth [51]. While seed particles can be obtained by using Au colloids [52] or dewetting a thin gold film [53], the growth of Au islands on the Si(111) 7×7 surface offers the unique advantage to control the interface between the Si surface and the Au droplet due to the ultra clean environment.

In this chapter, the formation of Au islands on Si(111) is investigated in the UHV condition ($\leq 10^{-10} mbar$) by low energy electron diffraction (LEED), scanning tunneling microscopy (STM) and also scanning electron microscopy (SEM). The mechanism and processes related to Au islands growth is understood, while the control of the distribution of Au islands is studied.

3.1 Epitaxial growth

Epitaxial growth refers to the method of depositing a monocrystalline film on a monocrystalline substrate. The deposited film is denoted as epitaxial film which may be grown from gaseous or liquid precursors. Because the substrate acts as a seed crystal, the deposited film takes on a lattice structure and orientation identical to those of the substrate. If a film is deposited on a substrate of the same composition, the process is called homoepitaxy, otherwise it is called heteroepitaxy. The growth method used here is the molecular beam epitaxy (MBE) in ultra high vacuum. Its essential advantage is the ability to control the growth process in the atomistic scale (below 10^{-7} meters). In the following, the growth modes and atomistic processes of the epitaxial growth using MBE technique is described.

3.1.1 Growth modes

Based on thermodynamics, the epitaxial growth was characterized into three growth modes by Bauer [54]. It relies on the concepts of free energy E_f and interface

energy λ. In short, on a clean surface in vacuum, the free energy is given as:

$$E_f = \gamma_i - \gamma_s + \gamma_o \tag{3.1}$$

where γ_s is the substrate-vacuum interface energy, γ_i overlayer-substrate interface energy, and γ_o overlayer-vacuum interface energy. As indicated in Fig.3.1, the three growth modes correspond to:

- **Frank-van der Merwe (FM)** growth: it describes a layer-by-layer growth for $E_f < 0 \Rightarrow \gamma_o + \gamma_i < \gamma_s$, as shown in Fig.3.1(b). Adatoms attach preferentially to surface sites resulting in atomically smooth, fully formed layers and the system gains a maximum energy. An experimental result for this growth behaviour is the deposition of a two-dimensional Ag film on Pt(111) [55].

- **Volmer-Weber (VW)** growth is observed for $E_f > 0 \Rightarrow \gamma_o + \gamma_i > \gamma_s$, see schematics in Fig.3.1(c). In this case, adatom-adatom interactions are stronger than those of the adatom with the surface, leading to the formation of three-dimensional adatom clusters or islands. Growth of these clusters, along with coarsening, will cause rough multi-layer films to grow on the substrate surface. For example, the growth of Pb islands on graphite was demonstrated in [56].

- **Stranski-Krastanov (SK)** growth is an intermediary process characterized by both 2D layer and 3D island growth, as illustrated in Fig.3.1(d). Transition from the layer-by-layer to island-based growth occurs at critical layer thickness where $\gamma_o + \gamma_i > \gamma_s$. Therefore, the SK mode is accompanied by the crystallographic change to the bulk lattice structure of the film at a critical thickness. This induces an abrupt increase in free energy at the interface between the two crystal structures and changes the energy balance to favor 3D growth. An experimental example for this mode is the growth of Ge on Si(100) [57].

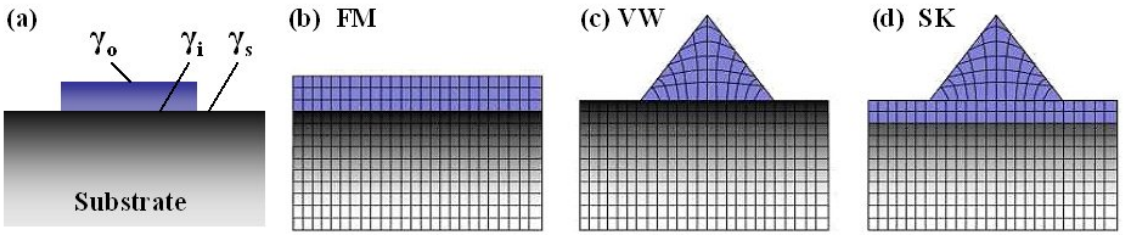

Figure 3.1: Growth modes. (a) Definition of surface energy, (b) Frank-van der Merwe growth, (c) Volmer-Weber growth, and (d) Stranski-Krastanov growth.

3.1.2 Atomistic processes

In the typical MBE epitaxial growth, there are several different types of atomistic processes on the crystalline surface. They are introduced in the following and schematically depicted in Fig.3.2.

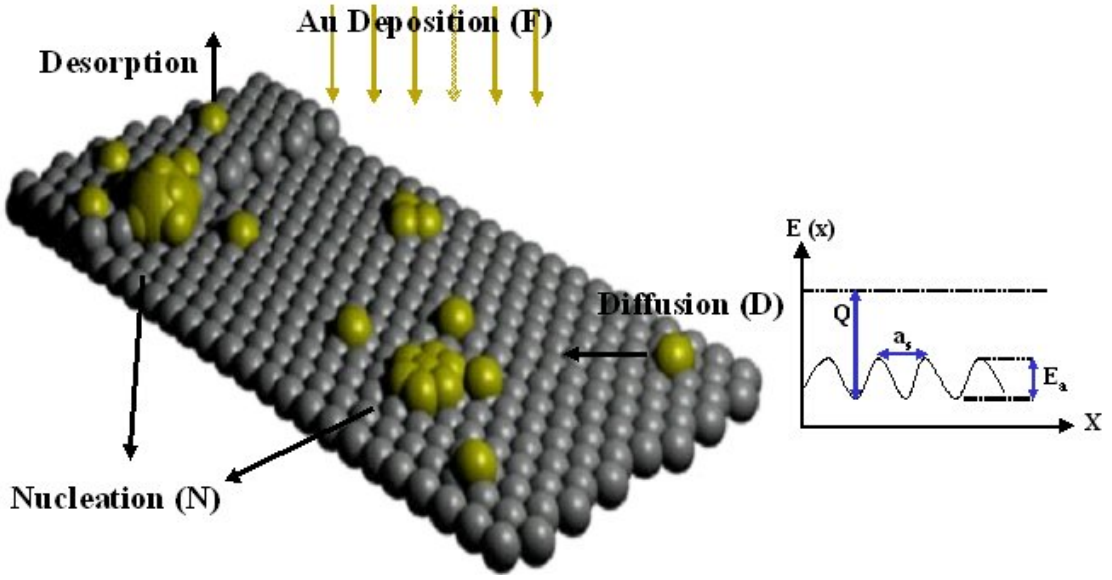

Figure 3.2: Schematic picture of the atomistic processes during MBE epitaxial growth; inset is the diagram of the energy landscape for diffusion in one dimension. x is displacement, E(x) is energy, Q is the heat of adsorption, a_s is the spacing between adjacent sites, and E_a is the barrier to diffusion (activation energy).

- **Deposition**: Atoms arrive at and adsorb to the growing surface at a rate F determined by the evaporation rate. Moreover, adatom desorption back to the gas phase can be ignored since typically growth during MBE occurs at rather low temperature.

- **Diffusion**: Surface diffusion kinetics can be thought of in terms of adatoms residing at adsorption sites on a 2D lattice, moving between adjacent adsorption sites by a jumping process, as shown in the inset of Fig.3.2.

  The jump rate is characterized by an attempt frequency and a thermodynamic factor which dictates the probability of an attempt resulting in a successful jump. The attempt frequency υ_0 is typically taken to be simply the vibrational frequency of the adatom, while the thermodynamic factor is a Boltzmann factor dependent on T, temperature and E_a, the potential energy barrier to diffusion (activation energy). The surface diffusion coefficient is related to the hopping rate of an adatom and can be described by an Arrhenius law, as given in Eq.3.2:

$$D = {a_s}^2 \upsilon_0 e \frac{-E_a}{k_B T} \tag{3.2}$$

  where the part of $\upsilon_0 e^{\frac{-E_a}{k_B T}}$ is the hopping rate. Importantly, this equation tells us how strongly the diffusion rate varies with temperature. The manner in which diffusion could take place is dependent on the relationship between E_a and $k_B T$.

- **Nucleation**: Adatoms will bond to their local neighbors and a large number

of separate islands can be formed. Nucleation of islands proceeds as long as adatoms form new islands instead of attaching to the existing ones.

In conclusion, the growth of surface structure using MBE involves deposition of atoms onto a surface, subsequent diffusion of those adatoms on the surface, and eventually nucleation of adatom clusters, commonly called islands. Atoms are deposited at random onto an initially flat substrate at a rate F (monolayers/sec), and then diffuse freely on the crystalline substrate until they encounter another atom, group of atoms, or a defect such as a step. Immediately upon application of the flux to a defect-free area of the substrate, the population of isolated adatoms begins to increase linearly with time until islands begin to nucleate. The number of islands can be predicted by the rate equations studies, which is introduced in the next part.

3.1.3 Rate equations

Insight into island growth or clustering process in general can be obtained from rate equations. There are a coupled set of deterministic differential equations describing the time evolution of n_s (density of s-atom islands). In this work, we consider the simplest rate equation description of growth [58], where adatoms are the only mobile surface species and the nucleation and growth of islands proceed by the irreversible attachment of adatoms (size of island can only increase). One obtains the rate equations for the size distributions:

$$\frac{dn_s}{dt} = Dn_1\sigma_{s-1}n_{s-1} - Dn_1\sigma_s n_s \tag{3.3}$$

where the first term on the right-hand side of equation is the creation rate of s-atom islands due to the capture of adatoms by (s - 1)-atom islands. The second term is the depletion rate of s-atom islands caused by their capture of adatoms to become (s + 1)-atom islands. For adatoms, one obtains:

$$\frac{dn_1}{dt} = F - 2D\sigma_1 {n_1}^2 - Dn_1 \sum_{i=2}^{\infty} \sigma_s n_s \tag{3.4}$$

where the first term is due to deposition of adatoms onto the surface, the second term describes the nucleation of a two-atom island by the irreversible attachment of two migrating adatoms, and the third term accounts for the depletion rate of adatoms due to their capture by islands. The quantity σ_i is the capture number, account for the diffusional flow of atoms into the islands. Eq.3.3 and 3.4 represent an infinite set of coupled ordinary differential equations. However, since the density of large (compared with the average size) islands decreases with their size, in practice the hierarchy in Eq.3.3 is truncated to obtain solutions for n_1 and the remaining n_s to any required accuracy. Notice that in writing Eq.3.3 it has omitted any direct interactions between islands. This restricts us to a regime where there is no appreciable coalescence of these islands.

To illustrate the calculus of rate equations, we consider a limited case where all of the capture numbers are set equal to unity. Then, by introducing the total island

density, N = $\sum_{s>1}$ n_s, using this definition in Eq.3.4 and summing the equations in Eq.3.3 over s, we obtain a closed set of two equations for n_1 and N:

$$\frac{dn_1}{d\theta} = 1 - 2Rn_1{}^2 - Rn_1N \tag{3.5}$$

$$\frac{dN}{d\theta} = Rn_1{}^2 \tag{3.6}$$

where R = $\frac{D}{F}$ and we have used the relation between the coverage and the flux in the absence of desorption, $\theta = Ft$. The Eq.3.5 and 3.6 are straightforward to integrate numerically and their solutions are shown in Fig.3.3(a) [58]. We will focus here on the initial and long time behaviour of the adatom and island densities, where analytic solutions to these two equations are easily obtained. At short times ($\theta << 1$),

$$n_1 \propto \theta, N \propto \theta^3 \tag{3.7}$$

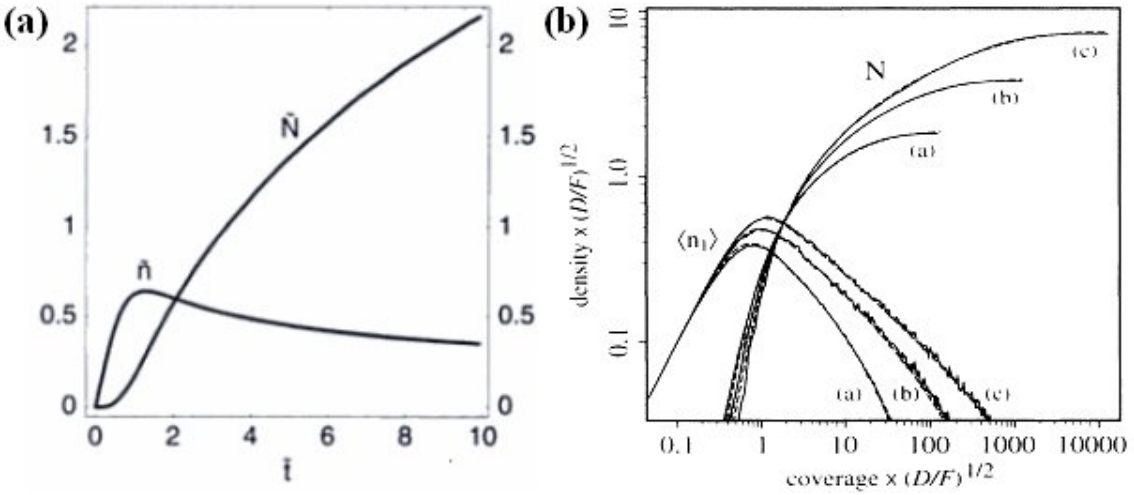

Figure 3.3: (a) The dimensionless adatom and island densities, denoted by $\widetilde{n}$ and $\widetilde{N}$, respectively, as a function of time, $\widetilde{t}$, obtained by integrating the rate equations: Eq.3.5 and 3.6 in the reference [58]; (b) The adatom and island densities, denoted by $\langle n_1 \rangle$ and N versus coverage at (a) $\frac{D}{F} = 10^5$, (b) $\frac{D}{F} = 10^7$, and (c) $\frac{D}{F} = 10^9$, obtained in the reference [59].

The density of adatoms initially shows a linear increase with coverage, which is due entirely to the deposition flux. The island growth is somewhat slower in the early development, showing a cubic time-dependence, because the adatom density is too low to lead to an appreciable island nucleation. Eq.3.6 shows that N continues to increase for all later times, but Eq.3.5 indicates that, although n_1 increases initially, it eventually begins to decrease, as shown in Fig.3.3(a). In this regime of island growth, we obtain *scaling laws* for the adatom and island densities:

$$n_1 \propto \theta^{\frac{-1}{3}} R^{\frac{-2}{3}}, N \propto \theta^{\frac{1}{3}} R^{\frac{-1}{3}} \tag{3.8}$$

This trend continues until we reach a regime of aggregation where n_1 << N and $\frac{dn_1}{d\theta} \approx 0$. In this case, the island density has saturated and the existing islands

capture all deposited atoms. However, the scaling of n_1 and N with θ is not correct in this regime. Indeed, the island density in Fig.3.3(a) does not exhibit saturation at all, which indicates that the approximation of constant capture numbers misses important aspects of island kinetics. The approximation was improved in the work of Bales et al [59], the spatial extent of islands in an average way was included by assuming that the local environment of each island is independent of its size and shape. Their results of the adatom and island densities were demonstrated in Fig.3.3(b) [59], where a saturation of island density was observed.

In conclusion, there are generally three regimes in the epitaxial island growth: nucleation, island growth and aggregation. Notice that in the island growth regime, the ratio D/F is the controlling parameter for quantities which characterize the surface morphology. In particular, Eq.3.8 indicates that increasing the temperature (increasing D) and/or decreasing the flux F causes the island density to decrease, resulting in fewer, but larger, islands. So in our experiments, we intend to choose this growth regime in order to precisely control the Au island distribution by regulating the growth parameters such as deposition rate and surface temperature.

3.2 Au/Si(111) surfaces

Surface experimental tools make possible the direct observation of surface structures and their phase transitions. By depositing submonolayer of Au on a Si(111) surface, various reconstructions have been found by reflection-high-energy electron diffraction (RHEED) and other techniques [60]. The formation of these reconstructions depends on the Au coverage and also delicate thermal treatments. In this work, before forming Au islands, we studied the Au/Si(111) submonolayer interfaces by using LEED and RT-STM *in situ* analysis to be able to calibrate the subsequent Au deposition on the Si(111) surface.

3.2.1 Surface phase diagram

Surface phase diagrams provide fundamental understanding of surface and interface phenomena, and can be used to predict the effects of changing parameters such as temperature or metal coverage on the atomic arrangement of surface structures. They also provide the starting point for understanding the kinetics of phase transitions at surface.

We present here an overview of the literature on Au/Si(111) which shows a great difference of the surface reconstructions as a function of temperature and Au coverage in the number of studies. Resolving the atomic structure for the two main surface phases of the Au/Si(111) system in the submonolayer regime, the (5×2) and ($\sqrt{3}\times\sqrt{3}$) Au/Si phases, in conjunction with results from numerous recent studies on this system allowed Plass [61] to propose a phase diagram, as shown in Fig.3.4. Their analysis was limited to the submonolayer region, although Fig.3.4 encompasses experimental observations from the literature up to 2 ML of Au coverage. The data points have errors of at least ± 0.04 ML on the Au coverage and ± 20 °C on temperature. The estimation is based on typical limitations of quartz monitors, Auger

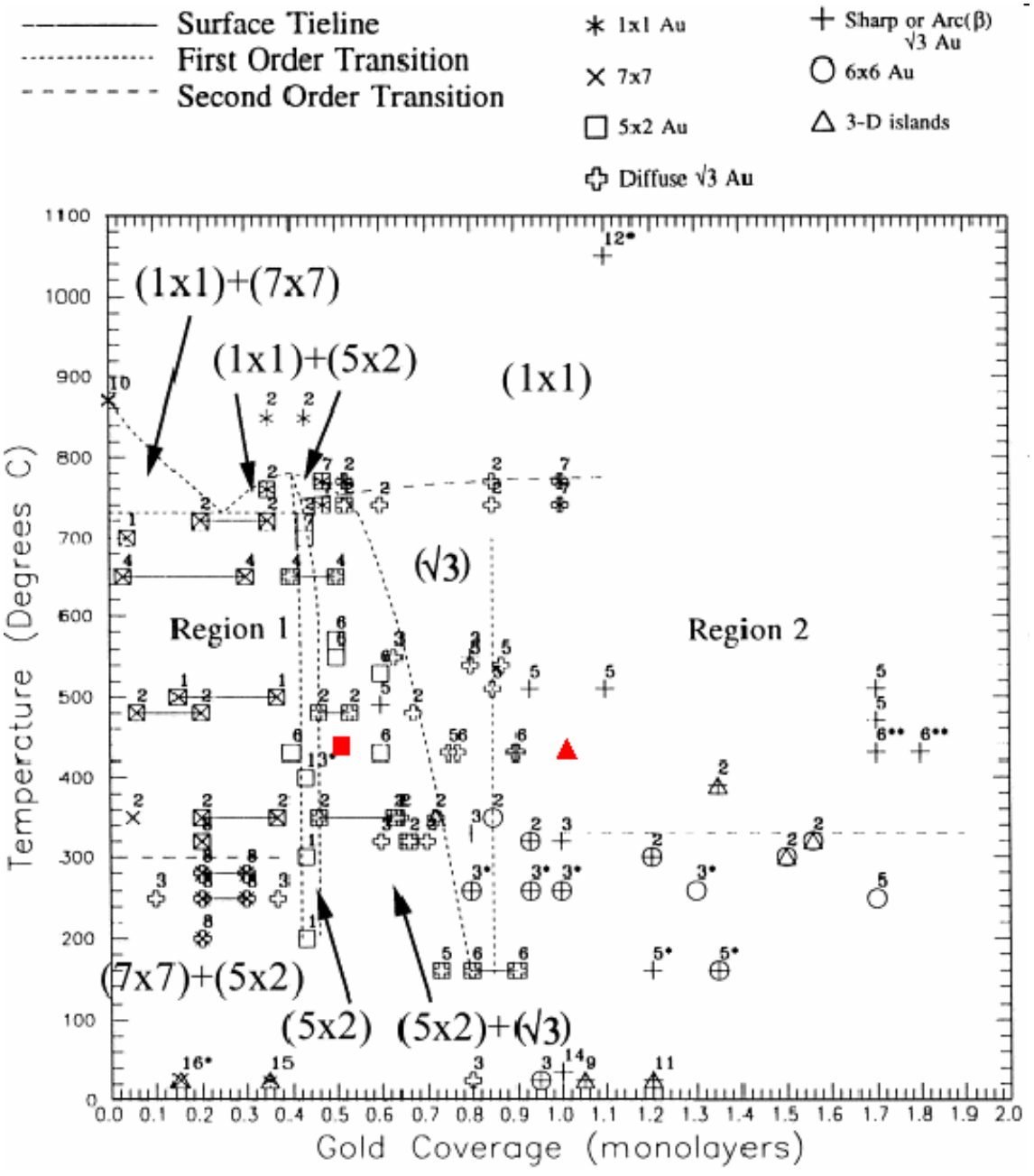

Figure 3.4: Surface phase diagram for the Au/Si(111) system proposed by Plass [61]. Region 1 (submonolayer coverage) with *in situ* experimental results. Region 2 (1-2 ML coverage) displays experimental data points. The number above a data point corresponds to its reference as follows: 1, Hasegawa et al. [62]; 2, Swiech et al. [63]; 3, Takahashi et al. [64]; 4, Tanishiro and Takayanagi. [65]; 5, Yuhara et al. [66]; 6, Yuhara et al [67]; 7, Daimon et al. [68]; 8, Shibata et al. [69]; 9, Fuchigami and Ichimiya. [70]; 10, Miki et al. [71]; 11, Ichimiya et al. [72]; 12, Kamino et al [73]; 13, Minoda et al. [74]; 14, Plass [61]; 15, Berman et al. [75]; 16, Meinel and Katzer. [76] The filled red square and triangle correspond to our Au coverage data of the 5×2 and β-$\sqrt{3}\times\sqrt{3}$ reconstructions.

electron spectroscopy (AES), Rutherford backscattering for coverage measurements, and pyrometers for temperature measurements.

3.2.2 LEED and STM characterizations

In our experiments, the Si(111) substrates were cleaved from n-doped wafers with a resistivity (0.03-0.05 Ω.cm). Before introducing the substrates into the UHV chamber, they were rinsed in ethanol and acetone repeatedly in an ultra-onic bath. The substrates were then outgassed at 550 °C for 10 hours and prepared by repeated flash annealing for a few seconds at 1100 °C by Joule heating in UHV to obtain the clean Si(111)-7×7 reconstruction, as described in the literature [77]. The temperature was measured with an optical pyrometer.

Before Au deposition, the (7×7) reconstructed surface of the Si(111) substrate was characterized by LEED and STM. Fig.3.5(a1) depicts its LEED pattern. The specular beam is covered by the electron gun in the middle. The 1×1 spots are marked by arrows and the extra spots in between are due to the 7×7 reconstruction. Fig.3.5(b1) shows the corresponding STM image where the 7×7 unit cell meshes of the reconstructed Si surface is clearly resolved. The unit cell consists of two triangular subunits. Each of them contains six protrusions, corresponding to the adatoms of the dimer-adatoms-stacking fault (DAS) model proposed by Takayanagi et al [78].

Au atoms were then deposited to the Si substrate from a tungsten (W) filament source by Joule heating. The deposition rate was calibrated from the phase transformation of 7×7, 5×2 and $\sqrt{3}\times\sqrt{3}$. The rate was set to 0.05 ML.s^{-1} in this experiment. Moreover, it is appropriate to consider the uncertainty in the Au coverage and an error on the order of 5-10 % is probably a realistic estimate. The surface temperature was kept at 430 °C. Evaporation of 0.5 ML Au results in a sharp 5×1 LEED pattern as shown in Fig.3.5(a2), while Fig.3.5(b2) is a STM image of the 5×2 surface. Atom rows with a lateral spacing 5 fold larger than the 1×1 unit cell of the unreconstructed Si (111) surface. On the edge of the rows, bright and dim features alternate and give a 2 fold symmetry that confers to this suface a 5×2 phase. The bright protrusions are Si adatoms [79]. Comparing to the previous results shown in Fig.3.4, our data (the red square, 5×2 at 0.5 ML), is in the range of the Au coverage (0.4 - 0.6 ML) to obtain the 5×2 structure.

Fig.3.5(a3) displays the β-$\sqrt{3}\times\sqrt{3}$ LEED pattern after depositing twice the Au coverage obtained for the 5×2 phase at 430 °C. The structure corresponds to a glass-like tilting ring structure sitting at ($\sqrt{3}\times\sqrt{3}$) lattice sites and giving a diffraction pattern with sharp spots surrounding by ring-like features. It is clearly different from the α-$\sqrt{3}\times\sqrt{3}$ structure which shows diffuse or cloudlike diffraction around $\sqrt{3}\times$ spots with a hexagonal shape and consisting of six small diffraction spots. Fig.3.5(b3) is the corresponding STM image. The $\sqrt{3}\times\sqrt{3}$ unit cell is demonstrated in the STM image, although the periodicity is hardly visible. In Fig.3.4, we have added our finding in the phase diagram and the occurrence of the β-$\sqrt{3}\times\sqrt{3}$ phase at an Au coverage of 1 ML, is consistent with the previous results. Moreover, It is known that with more than 0.9 ML coverage of Au, the β-$\sqrt{3}\times\sqrt{3}$ is formed by cooling the Si surface quickly, while the 6×6 is formed by slow cooling [60]. Since

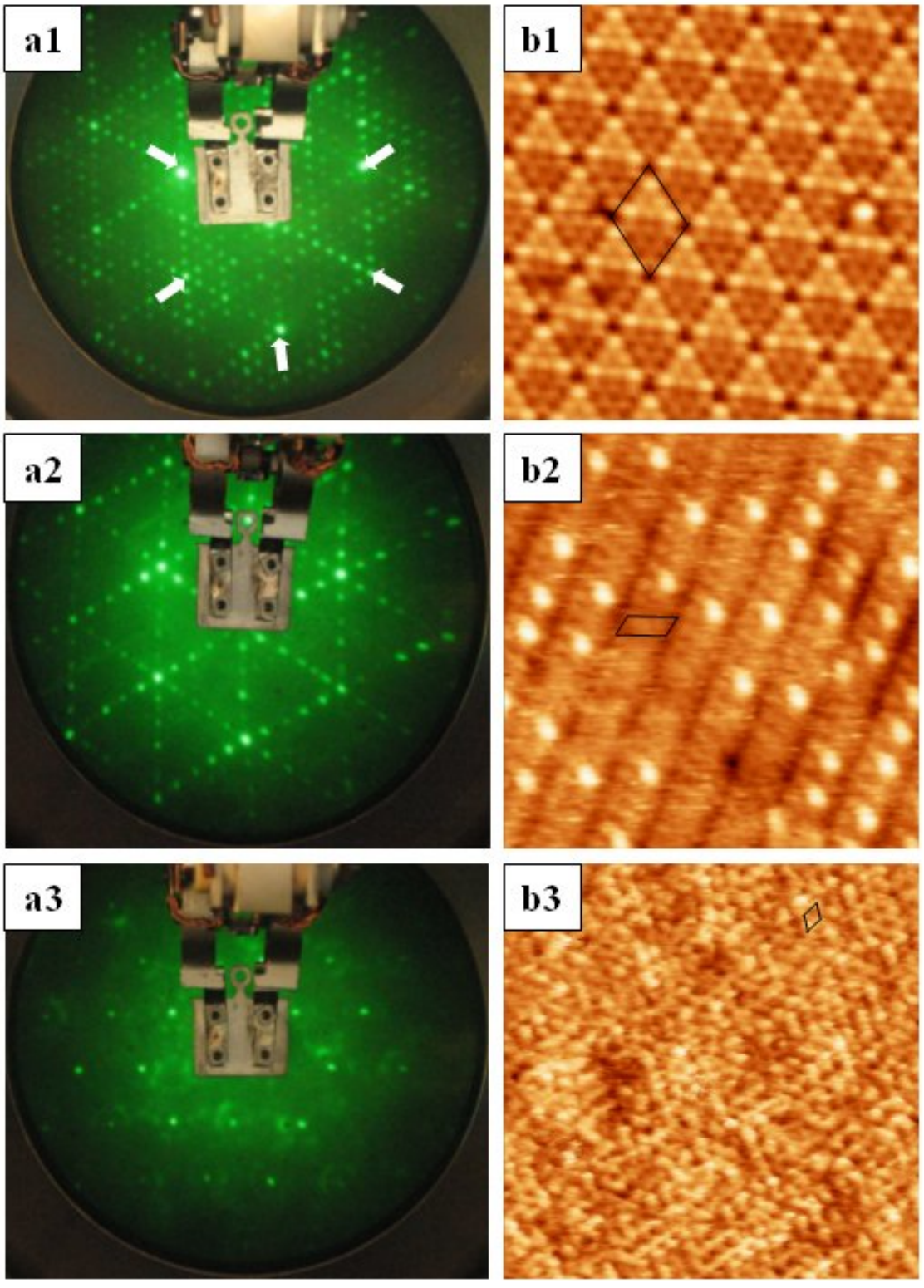

Figure 3.5: LEED and RT-STM results of the Au/Si(111) reconstructions as a function of Au coverage (θ), tip bias (V_{tip}), tunneling current (I). (a1),(b1): Si 7×7, θ=0 ML, V_{tip}=-3 V, I=30 pA; (a2),(b2): Au/Si 5×2, θ=0.5 ML, V_{tip}=-0.8 V, I=100 pA; (a3),(b3): Au/Si β-$\sqrt{3}\times\sqrt{3}$, θ=1 ML, V_{tip}=-0.4 V, I=500 pA. All the LEED patterns were recorded at 100 eV. All the STM images are empty-state STM images with the same scale (15×15 nm^2). The unit cell is indicated in each STM image.

the surface temperature was set immediately to 0 when the Au evaporation was stopped, the 6×6 was not observed in our experiments.

3.3 Au islands

The formation of the small 3D Au islands on the surface was clearly observed in Fig.3.6(a2) after depositing several ML Au at a surface temperature of 430 °C and the LEED result of Fig.3.6(a1) shows that the $\sqrt{3}\times\sqrt{3}$ reconstruction is always present on the surface, which can also be described as a wetting layer [80]. This formation of island after the completion of a wetting layer indicates that the growth follows the Stranski-Krastanov mode in our experiments. Moreover, The nucleation of Au islands is found to occur at step edges. In some previous works, the Si(111) vicinal surface [80] and the periodic lithographic patterns [81] were used as the template for the controlled positioning of the nanostructures. In our case, although Au was deposited on the flat Si(111)- 7×7 surface, the existence of the atomic steps favorite the nucleation of Au islands on them.

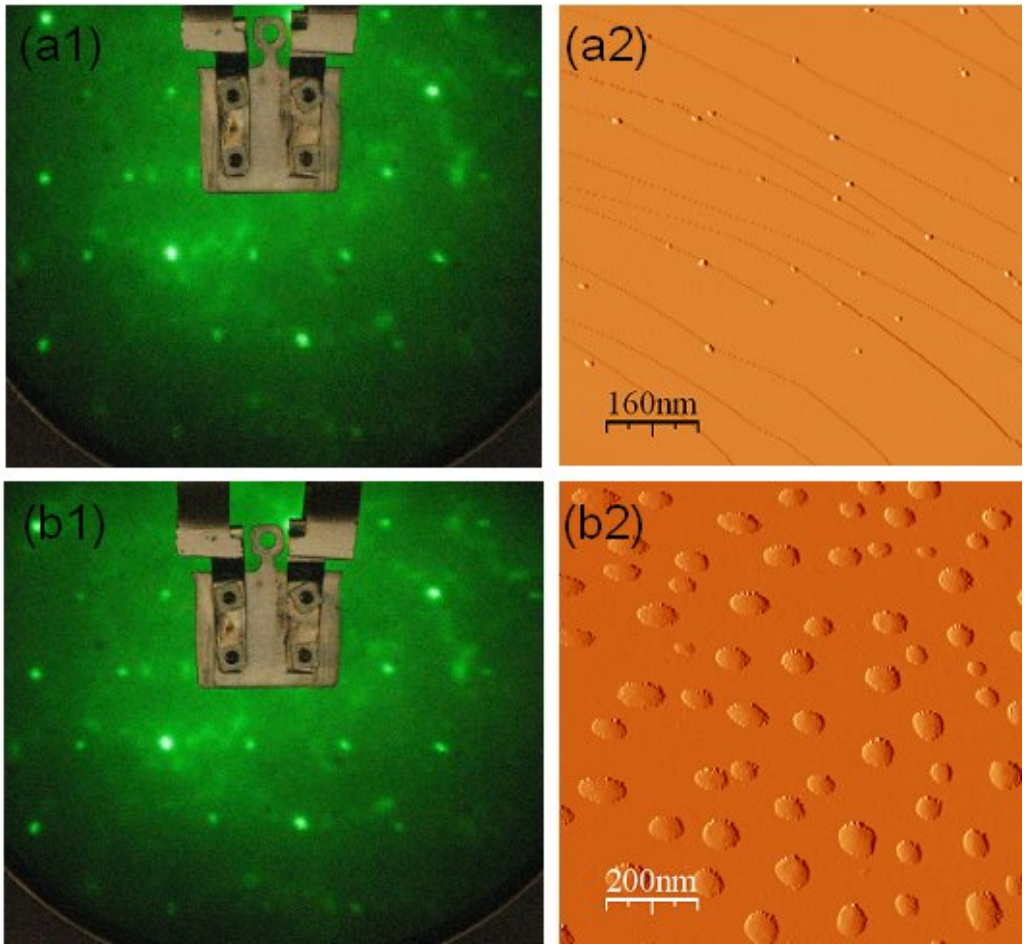

Figure 3.6: LEED and RT-STM results of Au islands on Si surface. Au coverage (θ), tip bias (V_{tip}), tunneling current (I). (a1),(a2): θ=several ML, V_{tip}=-2 V, I=20 pA, image size: 800×800 nm^2; (b1),(b2) θ=12 ML, V_{tip}=-2 V, I=20 pA, image size: 1000×1000 nm^2. All the LEED patterns were recorded at 100 eV.

The STM topography image of Fig.3.6(b2) shows that the density and size of the islands change when Au coverage increases to 12 ML. Meanwhile, the surface structure is still the $\sqrt{3}\times\sqrt{3}$ as shown in the LEED image of Fig.3.6(b1). In the initial stage of growth on a flat surface, if the deposition rate F is fixed, the value of the surface diffusion coefficient D (introduced in Eq.3.2) determines the average distance an adatom will have to travel before (a) finding and joining an existing island or (b) meeting another adatom to create the possibility of nucleating a new island. As nucleation continues, this distance decreases and eventually becomes constant. In this steady-state regime, newly deposited atoms will predominantly join existing islands and effectively prevent nucleation of new islands. In this work, the island formation has to be favored toward the island growth regime, in which the island density follows the scaling law described in Eq.3.8 and our goal is thus to control the island density and size distribution.

3.4 Control of Au islands distribution

Arrhenius equation

The Arrhenius equation is a simple, but remarkably accurate, formula for the temperature dependence of the rate constant, and therefore, a rate of a chemical reaction. It can be used to model the temperature-variance of diffusion coefficients, population of crystal vacancies and many other thermally-induce reactions. In short, the equation is given in the form:

$$k = Ae\frac{-E_a}{RT} \tag{3.9}$$

It can be also written equivalently as the Arrhenius plot:

$$ln(k) = ln(A) - \frac{E_a}{R}(\frac{1}{T}) \tag{3.10}$$

where k is rate constant, A: pre-exponential factor, E_a: activation energy, R: gas constant, and T: absolute temperature (K). When plotted in the manner described above, the value of 'y-intercept' will correspond to ln(A), and the gradient of the line will be equal to - $\frac{E_a}{R}$.

Experimental results

In this part of work, the influence of Au evaporation rate (F) and surface temperature (T) on the density and size distribution of Au islands was analyzed. In order to increase the accuracy on the counting of total quantities that may sightly vary due to fluctuations of step density on a simple, all the samples were observed by *ex situ* SEM in place of *in situ* STM. Six Si(111) 7×7 samples were then chosen. Two different Au evaporation rates: 0.05 ML.s^{-1} and 0.025 ML.s^{-1} were used, while the surface temperature varied from 360 °C to 460 °C and the growth time is 4 minutes. The SEM images are shown in Fig.3.7. Fig.3.7(a1,a2,a3) represent Si surface after Au depositions with an evaporation rate of 0.05 ML.s^{-1} at 380 °C, 400 °C and

430 °C; meanwhile Fig.3.7(b1,b2,b3) show Au depositions with an evaporation rate of 0.025 ML.s^{-1} at 380 °C, 400 °C and 430 °C.

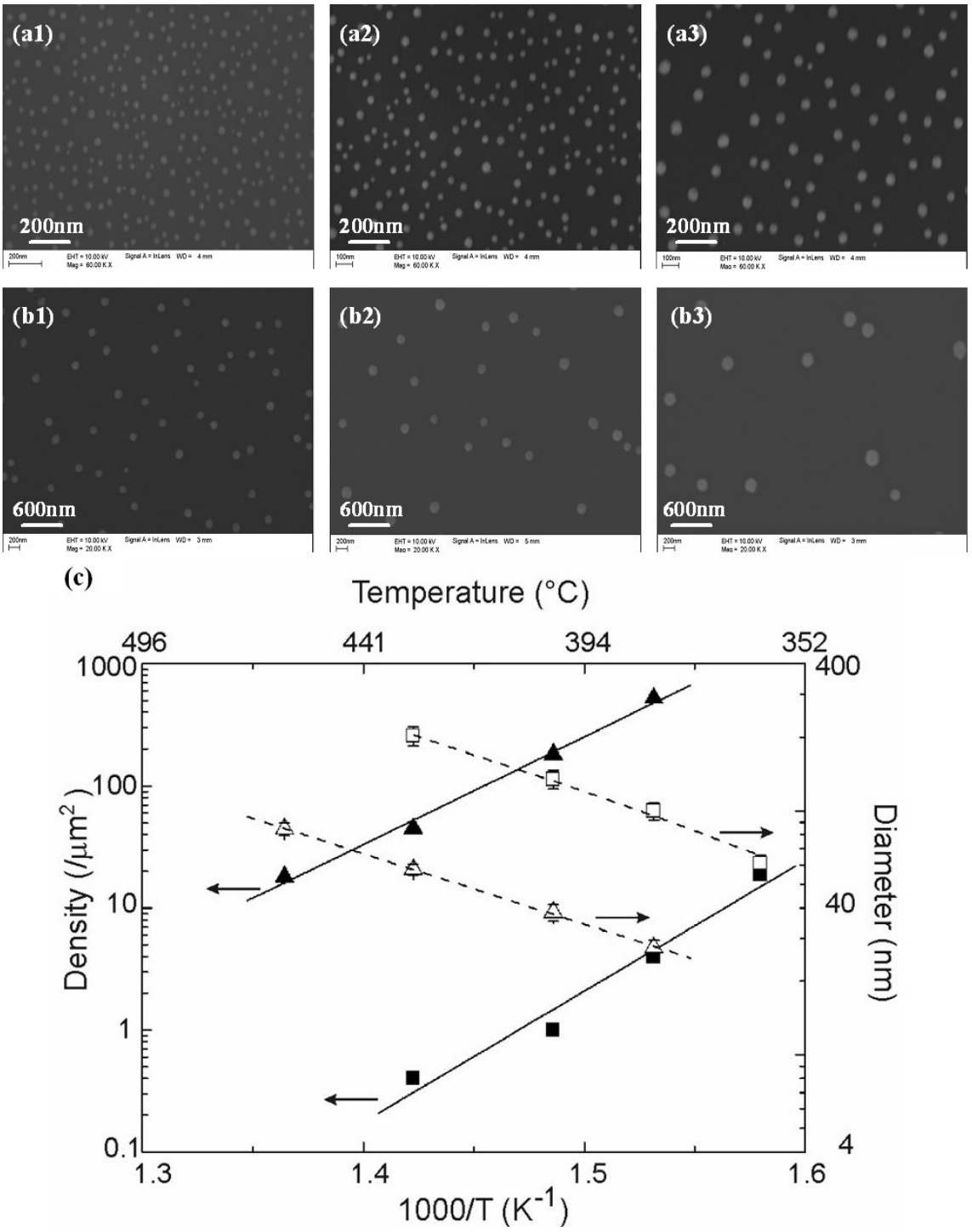

Figure 3.7: (a), (b): Top-view SEM images of Au islands. (a1,a2,a3) are the Au depositions with an evaporation rate of 0.05 ML/s at 380 °C,400 °C and 430 °C; (b1,b2,b3) are the results with an evaporation rate of 0.025 ML/s at 380 °C,400 °C and 430 °C; (c) Temperature dependence of Au islands densities (symbols: ▲, ■) and sizes (symbols:△, □) for evaporation rates of 0.05 and 0.025 ML/s, respectively. The deposition time was set to 4 min.

In these SEM images, the temperature and evaporation rate dependences of island densities and sizes are clearly observed. The island density is inversely proportional to the ratio D/F (surface temperature / evaporation rate), which corresponds to Eq.3.8. The island size is found to increase with the increase of surface temperature at a constant evaporation rate, since the Au adatoms are more likely to diffuse on the surface, meeting and joining the existing islands with a higher diffusion coefficient which is related to the surface temperature. All these SEM images indicate that the island deposition is in the island growth regime and not in the nucleation regime. In order to verify this observation, we can determine the ratio D/F by using the Arrhenius plot.

The statistic of the island distribution plotted in Fig.3.7(c) correspond respectively to data point obtained at an evaporation rate of of 0.05 ML/s and 0.025 ML/s. The graph shows that the island density exhibits an exponential decay behavior as a function of temperature. Fitting the plots to an Arrhenius form yields activation energies for diffusion E_a of 0.76 ± 0.02 and 0.92 ± 0.06 eV at F = 0.05 and 0.025 ML/s, respectively. Using the expression of the surface diffusion coefficient D of $D = {a_s}^2 \upsilon_0 e^{\frac{-E_a}{k_B T}}$, with ${a_s}^2$ the area of the unit cell for the β-$\sqrt{3}\times\sqrt{3}$ reconstruction being 38.3 $\mathring{A}^2$, we find that the ratio between the hopping rate $h = D/{a_s}^2$ and the evaporation rate F is always greater than 5.1×10^7, therefore favoring the propensity toward the island growth versus nucleation.

Moreover, in our experiments, we are interested in the formation of Au islands with appropriate distribution, more specifically, with a relatively low density and a size relatively important in order to obtain the controllable localized nanowire growth. Since we are in a growth regime where the majority of adatoms migrate into existing islands, the size of islands is expected to vary as the inverse of their density. Indeed, at a constant evaporation rate and deposition time (t), the product of the island size by their density yields the coverage (Ft) and this quantity is kept constant. The increase in the island diameter with the temperature can be seen in Fig.7(c), which is therefore consistent with the expected variation for the island size. So, by setting a relatively high surface temperature at 430 °C, and a low evaporation rate at 0.025 ML/s, the density of Au islands can thus be lower than an island per μm^2. Taking advantage over the control of Au island growth is a prerequisite to control the size and distribution of Si nanowires.

3.5 Conclusion

In this chapter, we have studied the epitaxial growth of Au islands on Si(111) under UHV condition using MBE technique. Combining STM and LEED characterizations, a phase transition of Si 7×7, Au/Si 5×2 and Au/Si β-$\sqrt{3}\times\sqrt{3}$ was observed in the submonolayer regime. After completing a Au/Si $\sqrt{3}\times\sqrt{3}$ wetting layer, 3D Au islands were then formed following the SK layer-plus-island growth mode. The size and density distributions of Au islands were analyzed by using *ex situ* SEM observations. By fitting the data related to the island size and density with Arrhenius plot, we have successfully found a range of surface temperatures, where the Au islands are prepared within the island growth regime. In this regime, we have

demonstrated the formation of Au islands that will be appropriate to further grow Si nanowires, as it is described in the next chapter.

Chapter 4

Si nanowire growth

One-dimensional semiconductor nanowires have been synthesized with controlled and tunable chemical composition, structure, size, morphology, and electrical properties [34]. Among these nanowires of various materials, silicon nanowires are of special interest, because silicon is the basic material in microelectronics. Many of the Si nanowires investigations regarding their synthesis have employed the Vapor-Liquid-Solid (VLS) process proposed by Wagner in 1960s during his studies of large single crystalline whisker growth [13]. This growth phenomenon demonstrated a unique attribute, namely a significantly accelerated growth rate in the vertical direction when compared to the lateral growth rate. In other words, the VLS reaction produces high aspect ratio structures as the vertical growth is favored while lateral growth is essentially suppressed. Several different techniques based on the VLS concept are widely used to synthesize Si nanowires, as Chemical Vapor Deposition (CVD) [82] and Molecular Beam Epitaxy (MBE) [17].

Furthermore, the integration of the Si nanowires into the conventional silicon systems have been intensively investigated: a number of nanowire-based devices have been fabricated, such as nanoscale field-effect transistors, solar cell, and biosensors [83, 84, 85]. However a good control of the nanowire growth and a deep understanding of their physical, chemical and electrical properties are still lacking. Several questions arise to achieve a controllable growth of Si nanowires, such as how to determine a specific orientation to facilitate the integration of nanowires, how to get a relatively rapid growth rate to yield a more efficient productivity, and also how to incorporate dopants into nanowires to improve their electrical properties?

In this chapter, with the objective to synthesize Si nanowires in a controllable way on the Si(111) substrate and also on more complex structures, we took advantage of our experience based on the controllable Au island growth to grow Si nanowires on Si(111) substrate by nanoscale Au-Si islands-catalyst-assisted CVD and MBE. The advantages of each technique were compared. The properties of nanowires such as growth direction, growth rate, structure and doping are discussed. From the control of Si nanowire growth on the Si(111) surface, a top-down fabrication followed by a bottom-up integration approach is then applied: Si nanowires are localized on some Si microstructures. These nanowire-based structures can then be used for further physical characterizations of the nanowires.

4.1 Growth mechanisms of Si nanowires

Several methods for the synthesis of Si nanowires have been established in the last years. These methods mainly differ with respect to the catalyst material used and with respect to the means by which the silicon is supplied. Concerning the silicon supply, the most popular method seems to be the chemical vapor deposition using a gaseous silicon precursor. Recently, another technique, molecular beam epitaxy under ultra-high vacuum conditions was also applied to synthesize Si nanowires. In this work, both techniques are used for the growth of Si nanowires. The growth systems: LP-CVD reactor and MBE-UHV chamber were already presented in chapter 2 and the growth mechanisms are introduced in this part.

4.1.1 Chemical Vapor Deposition

In the CVD case, the VLS mechanism requires the presence of a vapor phase and a liquid phase to realize a solid, one-dimensional nanostructure while temperature is a significant enabler of this reaction, governing the initiation and continuation of the reaction. The vapor phase precursor is the carrier of the desired nanowire material, where upon its thermal decomposition the desired nanowire material is available for the reaction. This reaction is different from a thin film deposition technique since in this case, metallic nanoparticles act as catalysts for the reaction by creating a preferred site for deposition. The decomposed vapor phase reactant is therefore preferentially deposited at these sites. Next, in order for the reactant to proceed, the metallic nanoparticles and the decomposed vapor phase reactant must form a liquid alloy at or above their eutectic temperature, as described by a binary phase diagram. The liquid alloy will continue to absorb the decomposed vapor phase reactants until the point of saturation is reached. Supersaturation will occur upon the additional deposition of the vapor phase reactant. Once supersaturation is reached, the alloy will precipitate excess decomposed vapor phase reactant in solid form, yielding a single crystalline structure, which is dimensionally constrained by the cross section of the liquid alloy. This process is often referred to as tip growth process, as the precipitated solid is always found below the liquid alloy. Consequently, as long as the vapor phase reactant and the corresponding thermal conditions are available, the supersaturation and precipitation process will continue. The VLS process is depicted schematically for silicon nanowires synthesis in Fig.4.1.

For Si nanowire synthesis, the vapor phase reactant must yield silicon upon its thermal decomposition and the metallic nanoparticle catalyst must form an eutectic with silicon. Silane (SiH_4), disilane (Si_2H_6) and silicon tetrachloride ($SiCl_4$) are commonly used as vapor phase sources. The selection of an appropriate metallic catalyst is required to ensure that the VLS reaction will take place. Silicon must be soluble in the specific metallic catalyst and the precipitation reaction must yield the desired nanowire material rather than another compound [86]. The eutectic temperature of the metal-silicon alloy is important in the catalyst selection as a lower temperature growth is more favorable in multi-step fabrication processes. A wide range of catalysts have been shown to effectively catalyze VLS based silicon nanowire synthesis, where a metal that forms an eutectic alloy with silicon is generally suit-

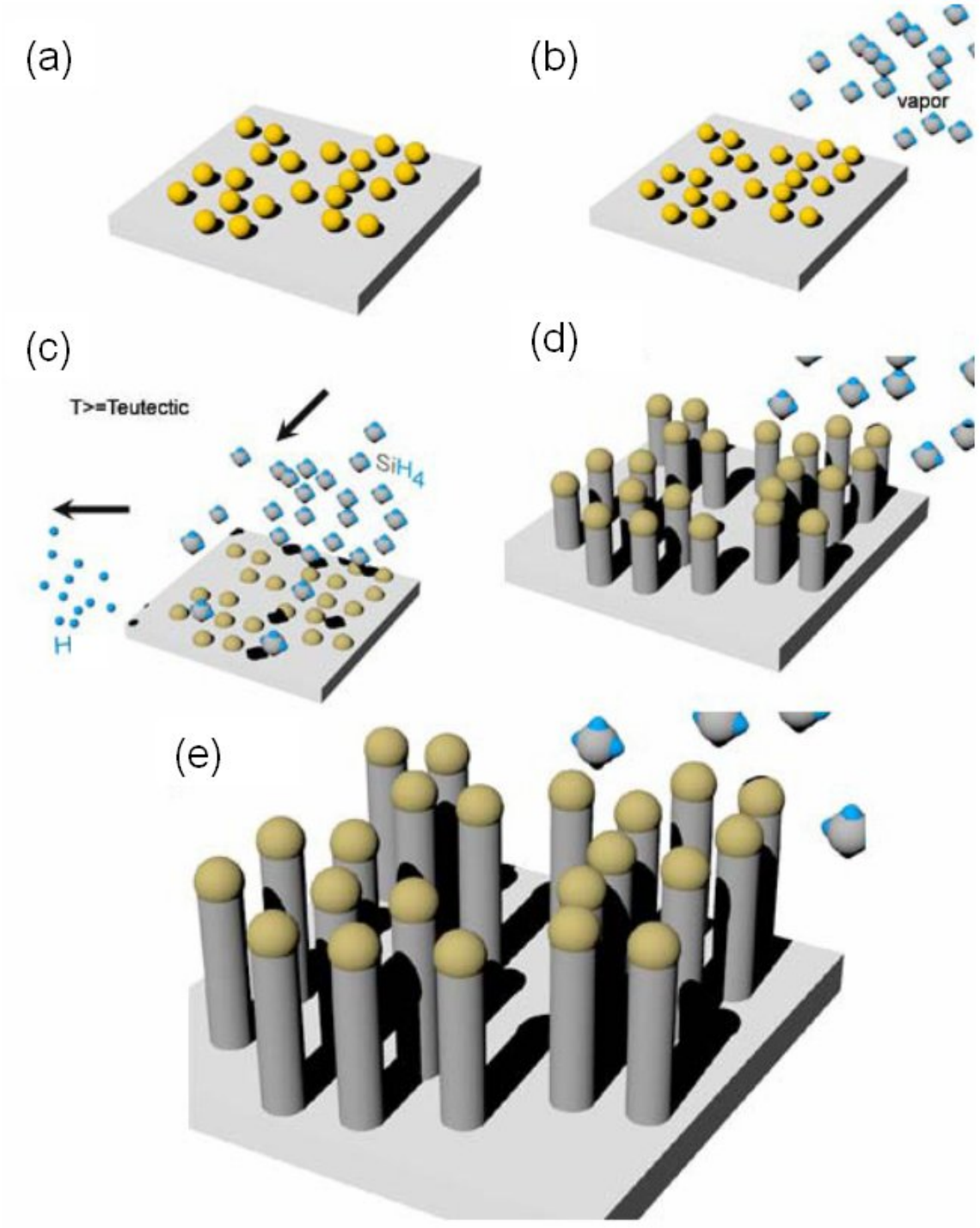

Figure 4.1: The VLS process for Si nanowire CVD synthesis. (a) Nanoscale metallic catalysts present on Si substrate. (b) Vapor phase (silane) reactant enters synthesis chamber. (c) Once the temperature requirement for the initiation of the VLS process is met, silane decomposes and preferentially deposits at catalyst location and a liquid alloy forms at the metal-silicon eutectic temperature. (d) Silicon continues to be absorbed by alloy until supersaturation is reached and silicon begins to precipitate from the alloy at the liquid solid interface, forming 1D nanowires. (e) Nanowire length is a function of growth time and growth conditions and reaction will continue as long as all elements are present.

able for this reaction, like gold, titanium, iron, nickel and aluminum [87, 88, 89, 90]. Tab.4.1 shows the eutectic temperature of alloys consisting of silicon and various metals which are used as catalyst. The various catalyst and vapor phase combinations yield a varying range of thermal requirements based on the catalyst-silicon alloy eutectic temperature, and the temperature required for the breakdown of the vapor phase.

Alloy	$T_{eutectic}$
Au-Si	363 °C
Ag-Si	837 °C
Fe-Si	> 1200 °C
Al-Si	577 °C
Pt-Si	980 °C

Table 4.1: The eutectic temperature of a few metal-silicon alloys

In conclusion, in the CVD case, the vapor-liquid-solid mechanism of Si nanowire growth basically consists of three steps:

- The adsorption and cracking of the gaseous silicon precursor, providing atomic silicon for the growth, followed by the incorporation of silicon atoms into the droplet.
- The diffusion of the silicon atoms through the droplet.
- The condensation of silicon onto the silicon nanowire at the liquid-solid interface.

Concerning the choice of the catalyst and gaseous precursor, the low eutectic temperature of gold-silicon (363 °C) and the low decomposition temperature of silane (350 °C) enable a rather low temperature synthesis and both of them are used in our experiments.

4.1.2 Molecular Beam Epitaxy

Comparing to the CVD technique, much less is known about the growth of Si nanowires by MBE. The MBE technique was applied for a number of III-V nanowires, such as GaAs [91]. Recently, Si nanowires were also synthesized by MBE [92]. The main advantage of this technique is to be compatible with the ultra high vacuum environment, so all the processes such as wafer preparation, catalyst deposition and nanowire growth can be performed *in situ*, what gives the possibility to better understand the VLS growth mechanism.

In the case of the MBE growth, the formation of nanowires is also initiated at the metal islands. However, there are some remarkable differences between nanowire growth by MBE and growth by CVD:

- **The substrate surface:** The nominal pressure in the MBE-UHV chamber lies in the region of 10^{-10} mbar, comparing to the pressure in the CVD reactor which is several mbar. Because of the reduced pressure, the substrate

can be additionally cleaned by a thermal treatment, and therefore be free of any oxide layer. For example, in our experiments on Si(111) surface, a 7×7 reconstruction can be formed before Au deposition.

- **Si deposition:** The flux of growing species in the MBE growth case, consists of single semiconductor atoms. The atoms, which have a specific kinetic energy, directly impinge on the clean Si surface for a specific time before their incorporation. These adatoms may diffuse on the clean Si surface for a specific time before their incorporation. These impingement and diffusion are considered as not significant in the CVD case, since the surface is covered with gas molecules.
- **Role of Au catalyst:** The Au droplet does not act as a catalyst for precursor gas, but result in a liquid Si/Au eutectic phase formation considerably reducing the nucleation barrier for nanowire growth. A supersaturation is supplied by the difference of the chemical potential of Si atoms located in the Si overlayer that is directly deposited on the surface, and on the top of the nanowire. It appears dues to relaxation of elastic energy stored in the overlayer caused by gold intrusions [93].

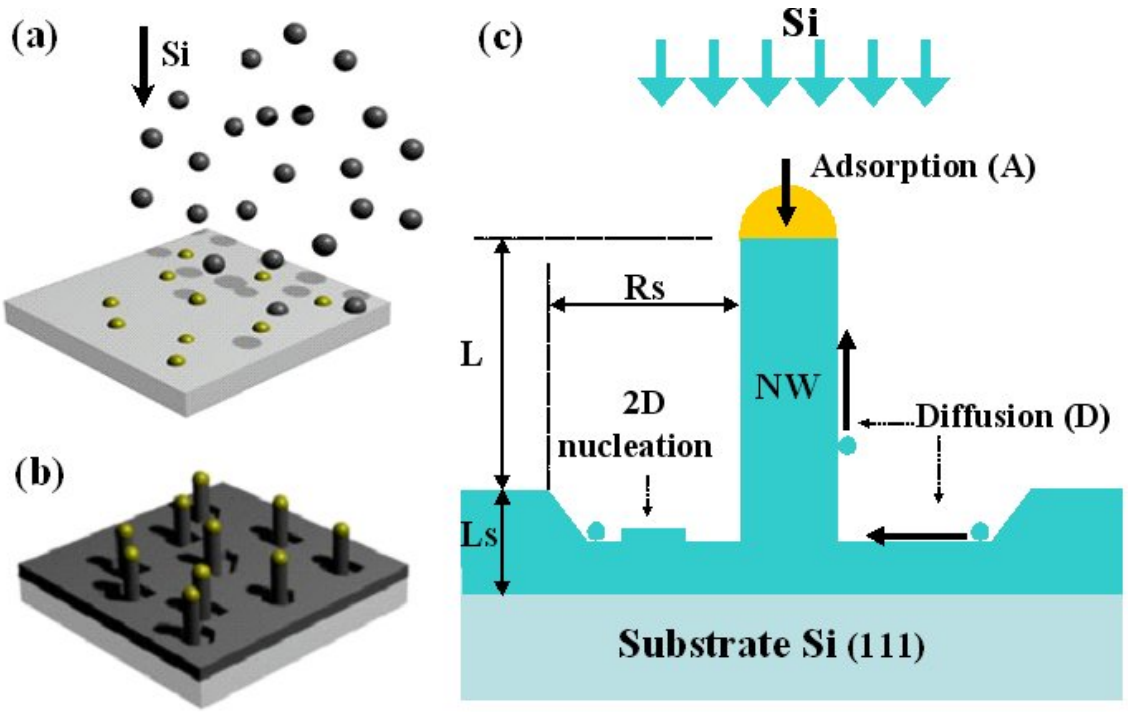

Figure 4.2: (a) Vapor source (Si) evaporates directly onto the Si substrate with gold catalysts. (b) Si atoms diffuse on the surface, leading to the growth of Si layer and specially the Si nanowires. (c) The model of a MBE nanowire growth and the basic kinetic processes at the surface

The process of MBE nanowire growth is described in Fig.4.2. Since the Si adatoms impinging on the surface are not desorbed, they diffuse on the surface and then nucleate and form the growing Si layer. In that case, two fluxes of Si adatoms can be distinguished as schematically shown in Fig.4.2(c). The flux Adsorption (A)

correspond to the Si atoms impinging directly at the metal droplet and a subsequent diffusion to reaction interface. It provides also the component of vertical elongation equal to the thickness of the overgrown Si layer L_s. However, if the nanowire and the Si layer grow with the same speed, no wire could be formed. The visible nanowire length L is detemined by flux Diffusion (D), which collects adsorbed Si adatoms from a region with a radius R_s around the nanowire. Si atoms diffuse upward to the Au catalyst and are incorporated into the (111) Si/Au interface. The growth process implies the presence of an adatom supersaturation which is caused by a gradient of the chemical potential $\Delta\mu > 0$ [94]:

$$\Delta\mu = \Delta\mu_0 - \frac{2\Omega\gamma}{R} \tag{4.1}$$

where $\Delta\mu_0 = \mu_s$ - μ_w results from the difference of the chemical potential between a Si atom on the substrate (μ_s) and a Si atom at the top of the nanowire (μ_w). The first term in Eq.4.1 is positive since $\mu_s > \mu_w$ because of the elastic energy relaxation in the nanowire [93]. In the second term, R denotes the nanowire's radius, Ω the atomic volume, and γ the surface energy. This term reduces the supersaturation $\Delta\mu$/kT (k: Boltzmann constant, and T: growth temperature) due to the increasing of surface energy and imposes limitations on the smallest nanowire radius. In conclusion, in the MBE case, the Si nanowire growth is determined by the surface diffusion of Si adatoms and associated with the difference in the chemical potential of Si atoms incorporated on the surface and on the top of nanowire.

4.2 Control of Si nanowires growth

With a basic understanding of the growth mechanism of Si nanowires, in the second part of this chapter, our objective is to well control several important parameters of nanowires. In order to integrate Si nanowires into devices, a specific growth direction should be first determined, then the growth rate of nanowires have to be controlled to get a rational length of nanowires, and finally the doping effect of nanowires should be understood. Two growth techniques: MBE and CVD are used in our experiments, as it is described in the following.

4.2.1 Control of the orientation of Si nanowires

In order to obtain the Si nanowires with controllable orientation, we have firstly used the MEB technique, since all the growth process can be carried out in UHV condition without any pollutions that may disturb the epitaxy during growth.

4.2.1.1 MBE approach

In our experiments, n-doped Si(111) wafers were prepared by standard procedures in a UHV chamber to yield surfaces with the 7×7 reconstruction [95]. Au was then evaporated to the Si surfaces being heated at temperatures higher than 360 °C to form the Au islands (see Chapter 3). For the subsequent growth of Si nanowires, the samples were transferred *in situ* to the MBE growth chamber, characterized by

a base pressure of about 10^{-10} mbar, where Si atoms can be directly evaporated onto the Si(111) surface from an effusion cell with integrated cooling shroud and shutter. The evaporation rate is determined by the heating temperature of the effusion cell which is generally above 1300 °C and calibrated by AFM measurements. For example, at 1350 °C, Si was evaporated on an Au sample, on which half of the surface was hided. The height profile of the deposited Si layer was then measured by AFM and the evaporation rate was thus calibrated, which is 0.05 nm/s. The substrate temperature was measured by an optical pyrometer. A set of samples were grown at 550 °C. Afterward, the samples were observed by SEM.

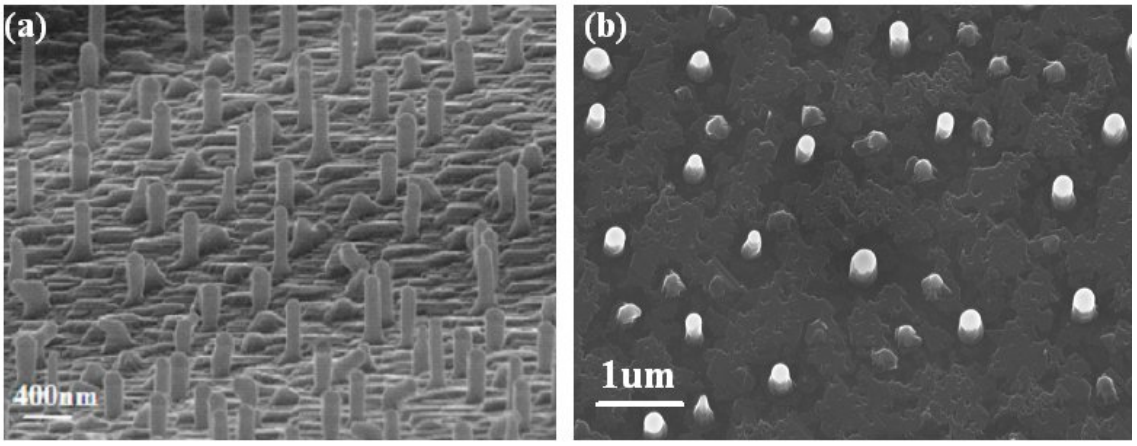

Figure 4.3: (a) Cross-section SEM image (with a tilted angle) of the MBE Si nanowires, (b) Top-view SEM image (with a tilted angle) of the MBE Si nanowires

An example of the MBE nanowires is shown in Fig.4.3, where the total growth time was set to 1h. The nanowires were found to stand in a pit visible as a darker ring around them, as shown in Fig.4.3(b). The existence of a pit around a nanowire can be explained by that Si adatoms are consumed by the nanowire and are included in the flux D, which confirms that in the MBE case, the nanowire growth is mainly dominated by the diffusion of Si adatoms. The growth direction of nanowires was found to be along [111] direction and they have a diameter in the range from 70 to 160 nm. The nanowires mostly have a cylindrical shape with a hemispherical Au cap. The presence of Au droplet on the top of wires is confirmed by SEM images of backscattered electrons (where contrast depends mostly on Z, the atomic number), as shown in Fig.4.3(b) where the brighter phase is Au.

Length/Diameter dependence

It has been found that in CVD growth by the VLS mechanism, nanowire length L normally increases with their diameter D: thicker nanowires thus grow faster than thinner ones. For thick nanowires, the growth rate is determined by the balance of adsorption and desorption processes on the planar surface of liquid alloy. Givargizov [96] suggested to attribute the observed increase of L(D) curves to the Gibbs-Thomson effect caused by the finite curvature of the nanowire surface. The Givargizov-Chernov theory [97] provides for the nanowire growth rate dL/dt the expression of form:

$$dL/dt = K(\Delta\mu_0 - \frac{4\Omega\gamma}{kTD})^2 \tag{4.2}$$

The coefficient $\Delta\mu_0$ is the difference of chemical potential between an atom in vapor phase and solid phase, T the growth temperature, Ω the atomic volume in the crystal, k Boltzmann constant and K coefficient of crystallization.

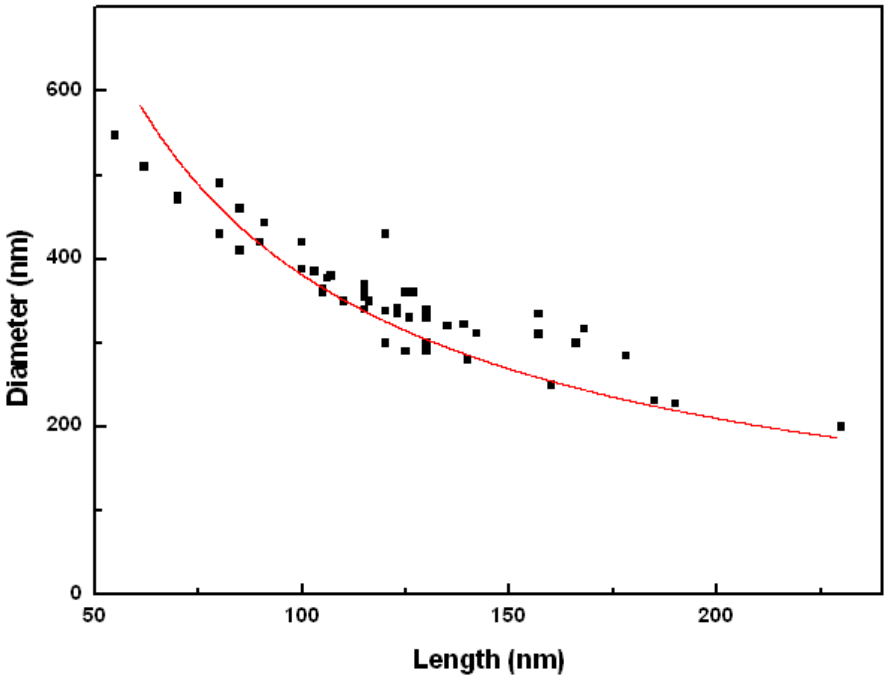

Figure 4.4: Correlation between the length L and diameter D of MBE Si nanowires.

In contrast, in our MBE experiments, the opposite L(D) curve was observed: thinner nanowires grow faster than thicker ones, as shown in Fig.4.4 (growth condition: Si flux rate: 0.05 nm s^{-1}, surface temperature: 550 °C, 1h). A simple fit based on a power-law L = C D^m leads to m = -0.9 (C is constant). This measured L(D) dependence is found to be similar to the work of Schubert et al [92], who has found that m ≈ -1. Such L(D) dependence is typical for the diffusion-induced (DI) growth of wirelike crystals that was investigated theoretically and experimentally by Neumann [98]. DI growth is controlled by the diffusion of adatoms towards the nanowire top along their side facets. When the surface is activated by the growth catalyst, the drop of a liquid alloy on the top of a nanowire may be quite an attractor for the adatoms and VLS growth may take many features of the DI mode. Our results support the assumption that the nanowire growth by MBE has a strong surface-related Si diffusion component, leading to a larger growth rate for nanowires with a smaller radius, which is in constrast to the CVD case.

Saturated growth

In order to analyze and use the nanowires for applications, they should be long enough, up to several micrometers for example, so nanowire growth with longer growth time has been tried. The statistic of the correlation between the length

of nanowires and growth time shows a saturation when the growth time becomes longer than 60 minutes, as shown in Fig.4.5. This saturation could be explained by the modification of the morphology of the Si overlayer: the substrate surface becomes rougher with the formation of pits around the nanowires, as illustrated in Fig.4.3(b). Therefore, the high potential differences for the diffusion of Si adatoms limit the atomic diffusion. The growth rate of nanowire decreases and becomes equal or even lower than the growth rate of the Si overlayer. Due to this limitation, the average length of the MBE Si nanowires is limited below 500 nm in our experiments.

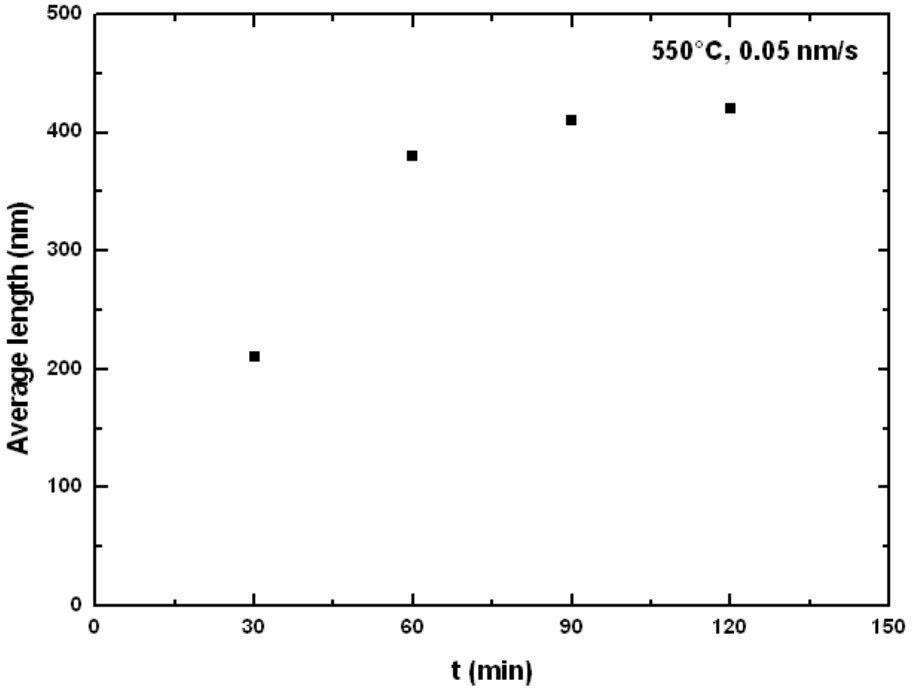

Figure 4.5: Saturated growth of MBE Si nanowires

Conclusion

Si nanowires were self assembled on Si(111) substrate under UHV condition using MBE technique. The growth direction was found to be [111]. In the formation of MBE Si nanowires, the nanowires are formed by two components of material flow. Beside the flux of adatoms collected by the droplet on the top, a significant amount of Si adatoms diffuse from the surrounding substrate surface to the Si/Au interface and thus form a nanowire. In contrast to the CVD growth process, in the MBE experiments described here, the nanowires with smaller diameters grow faster than the thicker ones. Moreover, a slow-down growth was observed with a long growth time, which limits the length of nanowires.

Although we can well control the growth orientation of Si nanowires in the [111] direction by MBE technique, their limited growth rate and the short length make the MBE Si nanowires very difficult to characterize, transfer and integrate into applications. In order to overcome this difficulty, the CVD technique was then used.

4.2.1.2 CVD approach

In this part of experiments, the same Si(111) substrates with Au catalysts were also prepared in UHV condition. For the subsequent growth of Si nanowires, the samples were then placed in the LP-CVD reactor in the clean room of IEMN. The process is similar to the CVD growth of thin film except that metal catalyst is present inside the reactor to promote nanowire growth. Several standard parameters determine the properties of the nanowires:

- Pressure of the reactor
- Temperature of the substrate
- Gas output: precursor gas SiH_4; carrier gas H_2 and doping gas B_2H_6 (5% diluted in Ar) and PH_3 (1% diluted in H_2).
- Growth time

Influence of surface oxide

Before the introduction of precursor gas source, samples with Au catalysts have to be desoxidized, because the surface oxide was found to induce defects during nanowire growth, which could disturb the epitaxial nanowire growth. For example, Tromp et al [99] have demonstrated that oxygen affects nanowire growth, leading to a preference for a different growth direction by introducing oxygen during the VLS nanowire growth even though the quantity of oxygen is very low. This effect was observed for both gas-phase and surface-bound oxygen. The sample cleanness has indeed an important influence to the growth direction, either an annealing at 700 °C under the H_2 flux during 10 minutes or an etching in 1% HF for 1 minute were used to improve the surface cleanness before nanowire growth.

Influence of the growth pressure

Three groups of growth parameters with different SiH_4 partial pressure were used to verify the influence of the growth pressure, shown in Tab.4.2:

Gas (sccm)	P (mbar)	T (°C)	P_{SiH_4} (mbar)	growth time (min)
SiH_4/H_2: 12/150	1.1	550	0.08	20
SiH_4/H_2: 55/150	1.1	550	0.3	20
SiH_4/H_2: 60/50	1.1	550	0.6	20

Table 4.2: CVD growth parameters

Fig.4.6 presents an example of nanowires grown at a low partial SiH_4 pressure of 0.08 mbar. The distribution of Au catalysts was observed before the nanowire growth (Fig.4.6(a)). After the growth, Si nanowires show a density similar to the density of the Au catalysts, as shown in Fig.4.6(b). Most of nanowires are found to grow in the <111> direction and the Au droplets are still visible at the top of the nanowires. Fig.4.7(a) shows a cross-section SEM image of this sample, and Fig.4.7(b) is its top-view SEM image. As almost every nanowire is naturally oriented perpendicular to one set of {111} planes indicated by the red arrows in Fig.4.7(b),

the projection on the substrate form a regular triangular network. The light spots in the top-view image are the nanowires grown perpendicular to the substrate, whereas the other three oblique directions form an angle of about 19.5° with respect to the substrate, as it is shown by the arrows in Fig.7(a). The growth rate is about 120 nm/min and the nanowires are slightly tapered.

Fig.4.8(a) shows the nanowires grown at a higher partial SiH_4 pressure of 0.3 mbar: no nanowire perpendicular to the substrate surface is visible and most of the nanowires form an angle of about 70° with respect to the substrate indicating a ⟨112⟩ direction. The growth rate is found to increase to about 500 nm/min. The shape of nanowire is rather straight. In the case of P_{SiH_4} set at 0.6 mbar, as it is seen in Fig.4.8(b), the growth direction seems to be dispersed to any specific direction. The growth rate is 2500 nm/min. Some nanowires become curved because of the long length.

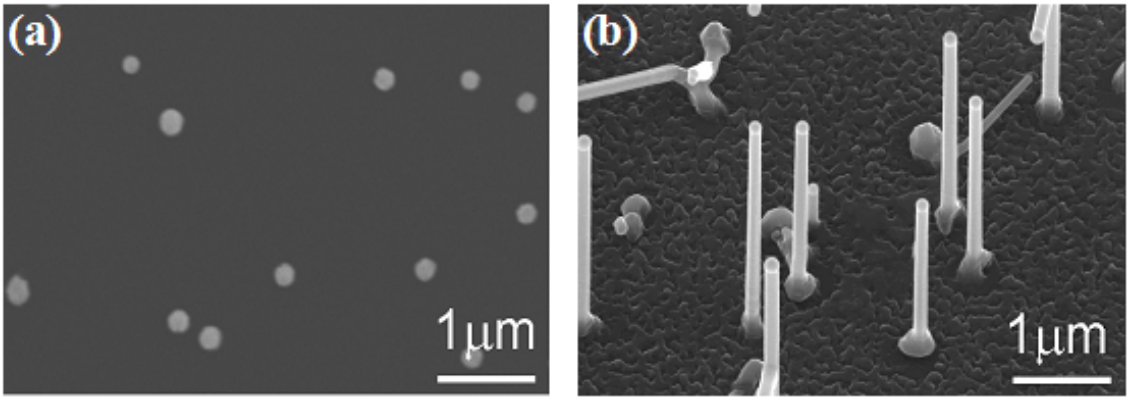

Figure 4.6: (a) SEM image of Au catalysts before CVD growth. (b) Tilted SEM image of predominantly ⟨111⟩ oriented Si nanowires grown from the surface shown in (a)

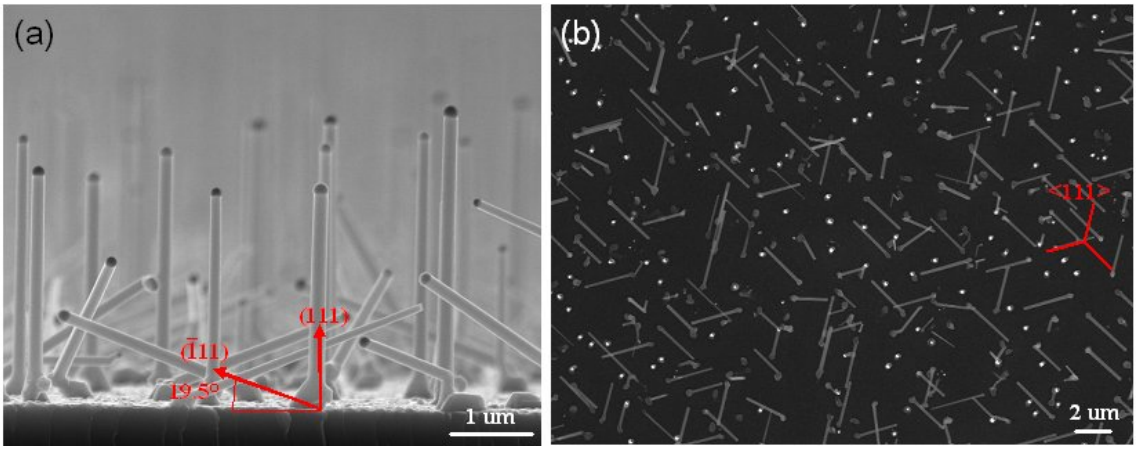

Figure 4.7: (a) Cross-section SEM image of Si nanowires grown at a low partial SiH_4 pressure (0.08 mbar) at 550 °C for 20 min. The red arrows indicate 2 ⟨111⟩ directions. (b) Top-view SEM image of Si nanowires grown at the same condition described in (a). The red arrows indicate the ⟨111⟩ directions.

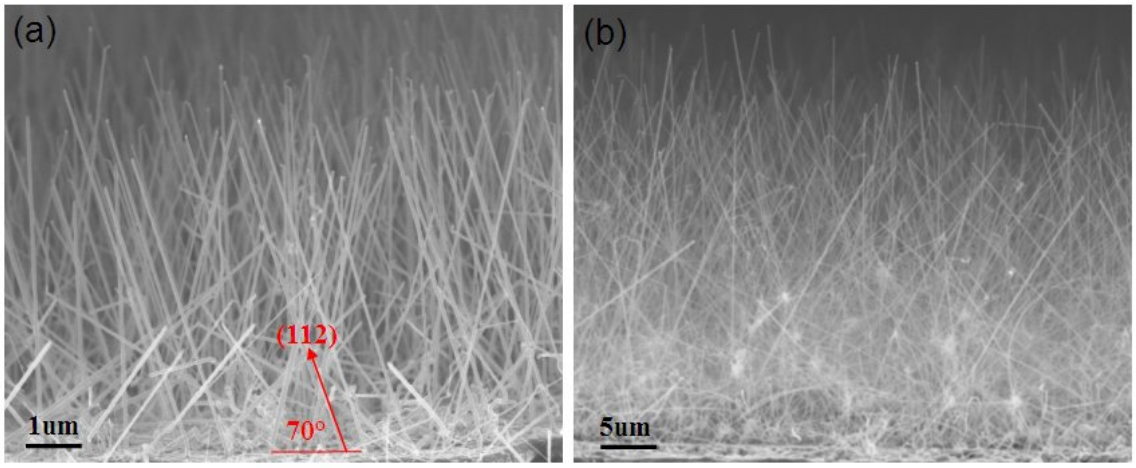

Figure 4.8: (a) Si nanowire growth at a partial SiH_4 pressure of 0.3 mbar. The red arrow indicates a ⟨112⟩ direction. (b) Si nanowire growth at a high partial SiH_4 pressure of 0.6 mbar.

In the earlier works of Si nanowires growth, it has been shown that Si nanowires grown by CVD with Au as catalyst and diameters greater than 100 nm prefer growing along the ⟨111⟩ direction [13]. The growth axis is believed to be determined by the formation of a single lowest-free-energy solid-liquid interface that is parallel to a single (111) plane [100]. However, more recent observations suggest that the crystallographic growth direction of Si nanowires grown with Au is diameter dependent [101, 102]. For large diameters, greater than about 40 nm, the nanowires tend to grow in a ⟨111⟩ direction. Conversely, for the diameters smaller than about 20 nm, the ⟨110⟩ and ⟨112⟩ growth direction are observed. The reason for this lies in the fact that a silicon atom precipitating upon the (111) surface during growth produces the largest decrease in Gibbs free energy, because (111) planes of silicon have the largest density of surface atoms when acting as an interface [103]. When the diameter is very small, the free energy of the side faces must be taken into consideration [104] and the other growth directions became more favorable.

In this experiment, the size of Au catalyst is in the range of 70-150 nm, which should favor the growth direction in the ⟨111⟩ direction, as we have observed at the low partial SiH_4 pressure. However the higher supersaturation of catalytic Au-Si alloy at the higher partial SiH_4 pressure may influence the nanowire nucleus structure [105] and change the nanowire growth direction.

Conclusion

Si nanowires were grown on Si (111) substrate using Au island-catalyzed CVD technique. The growth direction can be controlled by changing the partial SiH_4 pressure: nanowires grow along the ⟨111⟩ direction at low partial SiH_4 pressure, whereas the direction becomes less controllable at high partial SiH_4 pressure. In contrast to the MBE case, the length of CVD Si nanowires can easily reach several micrometers in a much shorter time, what makes it easier for the further localized nanowire growth and characterization. So we will continue using this technique, more specifically at low partial SiH_4 pressure to obtain <111>-oriented Si nanowires which can facilitate their integration with the conventional technologies.

4.2.2 Limited length for <111>-oriented Si nanowires

Influence of P_{SiH_4} and $P_{B_2H_6}$

At the first sight, the growth rate of Si nanowires was found to depend on the partial SiH_4 pressure, since the higher SiH_4 pressure results in a larger supply of the Si source. In the CVD case, the growth rate is limited by the supply of the Si source, so the larger supply of Si results in a higher growth rate, as it is shown in Fig.4.9. At 550°C and a total pressure of 1.1 mbar, the growth rate increased more than 100 times when the SiH_4 partial pressure increased from 0.03 mbar to 1 mbar. In addition to this dependence of P_{SiH_4}, the nanowire growth rate was found to be related to the use of doping gas. At the growth condition of 550°C, P_{tot}:1.1 mbar and P_{SiH_4}:0.08 mbar, when B_2H_6 was added during growth with a ratio B:Si of 8×10^{-3}, the growth rate was found to be doubled. B_2H_6 is known to be used as a p-type dopant source for epitaxial and microcrystalline Si films [106]. A growth-rate enhancement is observed frequently when B_2H_6 is used as a dopant in Si thin-film chemical vapor deposition [107]. The influence of dopants is discussed in more details in the next section.

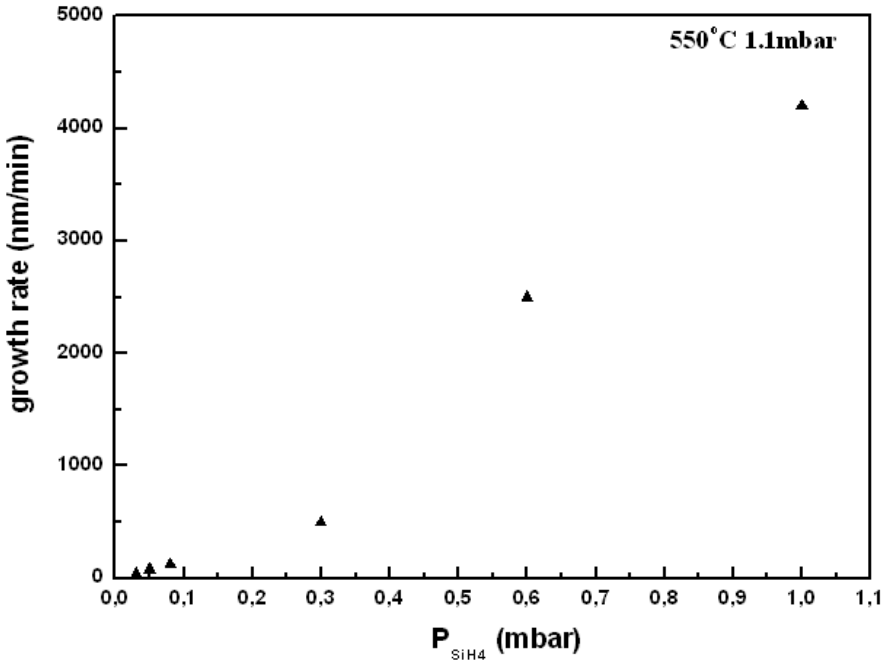

Figure 4.9: Growth rate dependence on P_{SiH_4}

Influence of Au diffusion

Generally, it is believed that the diameter of nanowires depends on the diameter of their catalysts, however the lateral growth (direct Si deposition) can occur on the nanowire sidewall and Au could diffuse along the nanowire sidewall during growth in certain growth conditions, giving the nanowires a taper shape. In our experiments, working at a low partial SiH_4 pressure (0.08 mbar) and a temperature relatively high (550°C), the taper shape becomes clear when the growth time is long (1h), as it is shown in Fig.4.10(a). Moreover, in this figure, Au droplets have completely disappeared on the shortest nanowires and for these nanowires, the sidewalls become

very rough (see Fig.4.10(c)). For the nanowires that still have an Au droplet on the top, their lower parts show the same roughness, but the higher parts near the Au droplet are relatively smooth (see (b)).

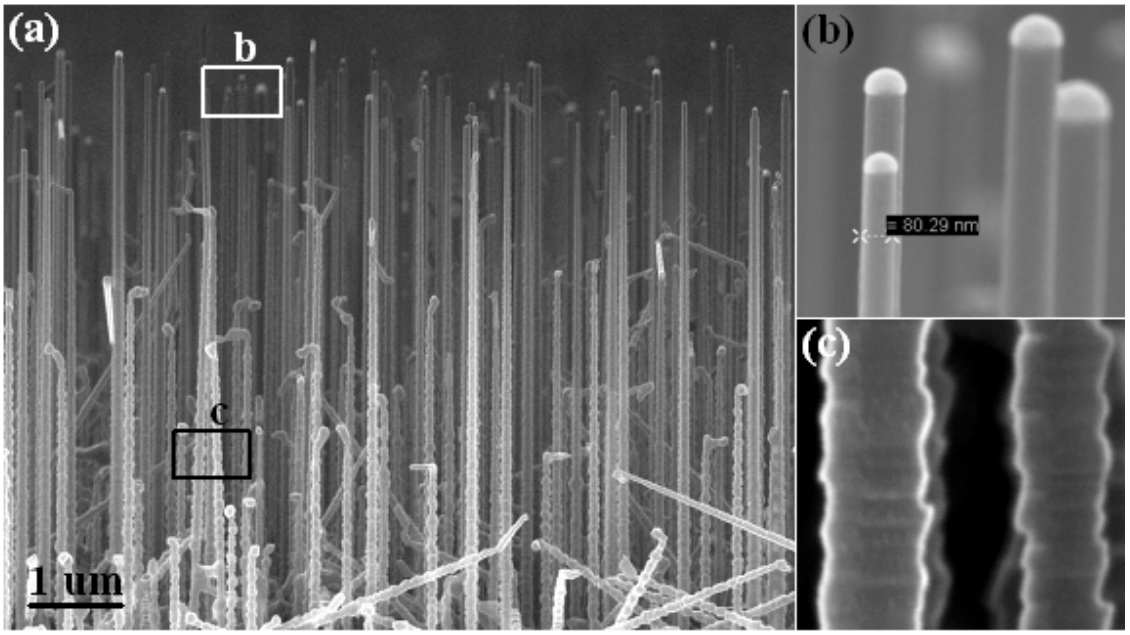

Figure 4.10: (a) Influence of the Au diffusion on the length of Si nanowires. (b) Zoom on the nanowires with Au catalysts after growth. (c) Zoom on the nanowires that do not have Au catalysts after growth.

These observations were also obtained by Hannon et al [108]. They showed that Au from the catalyst droplets diffuses and wets the nanowire sidewalls. Once the droplets are consumed, nanowire growth terminates, while direct CVD growth of Si on the sidewalls continues, dramatically altering the sidewall morphology. When the Au droplets are still present, the growth rate of nanowires is fast comparing to the rate of direct Si deposition, leaving the nanowire sidewalls relatively smooth. Furthermore, if Au from the catalyst droplet is transfered to the sidewall, the droplet will be completely consumed. Consodering that the Au catalyst droplet is hemispherical while the shape of nanowire is cone (in the case of 1D nanowire, the generatrix can be considered to be equal to the height of cone), the maximal nanowire length L_{max} is thus :

$$\frac{1}{2} \times \frac{4}{3}\pi r^3 = a\theta\pi r L_{max} \rightarrow L_{max} = \frac{2r^2}{3a\theta} \tag{4.3}$$

Where r is the radius of the nanowire at base, θ is the average coverage of Au on the sidewall, and a^3 is the atomic volume of Au (a≈0.26nm). The value of θ could be estimated as 1 monolayer. The correlation of length/radius of nanowires using this equation are shown in Tab.4.3.

This analysis implies that at the low partial SiH_4 pressure growth condition, the length of nanowires depends on the initial size of Au droplets. When the growth time is long, some of the longest nanowires have no catalyst, presumably because their

r (nm)	10	40	50	68
L_{max} (μm)	0.27	4	8	12

Table 4.3: Length/Radius correlation of Si nanowires

droplets were consumed just before growth ended. This property of the length/radius dependence can be used to estimate the length of nanowire by controlling the size of the Au islands, which is very useful for the localized nanowire growth. Moreover, as the adsorption of metals at the surface of semiconductors causes a modification of the atomic reconstruction and electronic properties [109], the diffusion of Au atoms on the Si nanowires sidewalls are expected to have an important influence on the surface structure of nanowires, as it is discussed in Chapter 5.

4.2.3 Doping of Si nanowires

Although pure elements such as silicon play an important role in many semiconductor devices, it is most often utilized by adding very small but controlled amount of impurities in order to alter its properties. The pure silicon is an intrinsic semiconductor with the Fermi level placed in the middle of the bandgap, between the conduction band and the valence band. Doping can produce two types of semiconductors depending upon the element added. If the semiconductor is doped with an element having at least one less electron than the host material, then a P-type semiconductor is created. If element used for doping has at least one more valence electron than the host semiconductor, then a N-type semiconductor is created. All these doping types are illustrated in Fig.4.11.

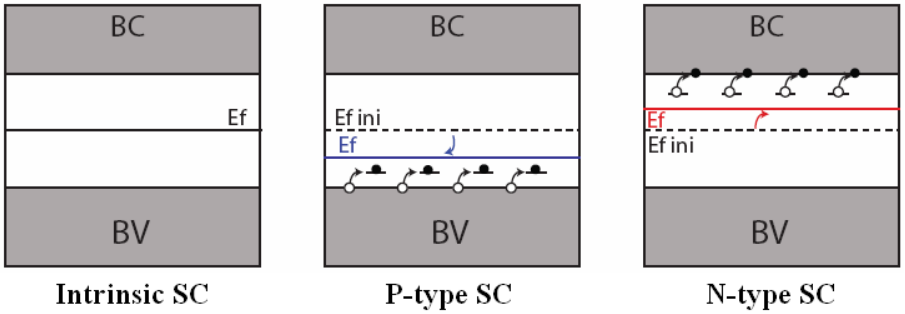

Figure 4.11: Intrinsic, P-type and N-type semiconductor

As practically all semiconductor devices rely on a controlled doping of the semiconductor material, a both quantitatively and spatially controlled doping of the Si nanowire is desirable. For the bulk and thin film doping of silicon as well as other semiconductors, the standard process like ion implantation techniques as well as the introduction of dopants into the flow stream are mainly used methods. For the Si nanowire doping, in principle, the more advanced alternative doping method is to add a small amount of a gaseous dopant precursor for the *in situ* doping: P-type doping of Si nanowires was demonstrated by adding either the traditionally utilized diborane (B_2H_6) [110] or the organometal precursor trimethylboron (TMB)

[111] to the flow stream, while N-type nanowire doping is obtained by using a phosphine (PH_3) source [110]. This method offers the possibility of varying the doping of nanowires during growth by changing the partial pressure of the corresponding dopant gas. Another *ex situ* doping technique is used in certain works [112]: after nanowire growth, a predeterminated amount of boron is introduced into the near surface region of nanowire by holding the boron source in close proximity to the nanowires. The dopant concentration is thus controlled by the predeposition temperature and time, with 800 and 950 °C and 5 - 10 min used in their work.

In our experiments, both N or P-type Si nanowires were fabricated by adding phosphine or diborane during growth. The growth parameters are shown in Tab.4.4 and the respective SEM images after growth are shown in Fig.4.12:

P_{SiH_4} (mbar)	P_{tot} (mbar)	T (°C)	B:Si	P:Si	growth time (min)
0.08	1.1	550	8×10^{-3}		20
0.08	1.1	550		8×10^{-4}	20
1	1.1	430	8×10^{-3}		20
1	1.1	430		8×10^{-4}	20

Table 4.4: CVD doping growth parameters

Two types of growth parameters were used: in the case of low P_{SiH_4} at 0.08 mbar and 550°C, when B_2H_6 was added, the morphology of nanowires was not changed (in <111> direction and slightly tapered) and the growth rate was significantly increased. However the nanowires doped by PH_3 was found to be very kinked and the growth rate was decreased. In the case of high P_{SiH_4} at 1 mbar and 430°C, the doping effect is rather different: there was not significant changes of the nanowire morphology when PH_3 was added,: the nanowires were rather straight with growth direction less controllable and no enhancement of growth rate was observed. For the P-type using B_2H_6, the morphology was completely changed. The wires became very tapered and kinked.

In order to understand such differences of nanowire growth with dopants, we considered the previous study of the Si film deposition by LP-CVD. In that case, it was observed that the addition of a dopant gas to silane induces some variations of the growth rate of Si [107]. These variations, under particular conditions, might cause non-uniformity problems in the growth and doping of the deposited layer. For example, Briand et al [113] showed that at 550°C, the phosphorus-doped silicon layers present a lower growth rate than the undoped silicon layer, while the boron-doped silicon layers grow faster. The reduction of growth rate with phosphorus is generally attributed to the fact that phosphine is preferentially adsorbed on growth site [114]. Once adsorbed, the phosphine is stable under silane flow and thus effectively passivates the silicon surface with respect to the heterogeneous silane chemical reactions and is responsible for the decrease in the growth rate. To explain the increase of growth rate with boron, it has been proposed elsewhere that this enhancement would result from the catalysing effect of diborane on the gas-phase reaction [115]. The above observations of the rate changes agree well with our results of doped nanowire growth which was performed at 550°C and P_{SiH_4} at 0.08 mbar. Meanwhile, the kinked morphology of phosphorus-doped nanowires can be

explained by the passivation effect that is induced by phosphine, and leads defects during growth.

Furthermore, the crystallinity and the dopant incorporation in any deposited film are strongly related to the deposition temperature and the deposition rate (P_{SiH_4}) [116]. That could explain why the doping effects on the nanowire grown in the different conditions are completely different. However, more knowledges and experiments of the influence of dopant on nanowire growth are still needed.

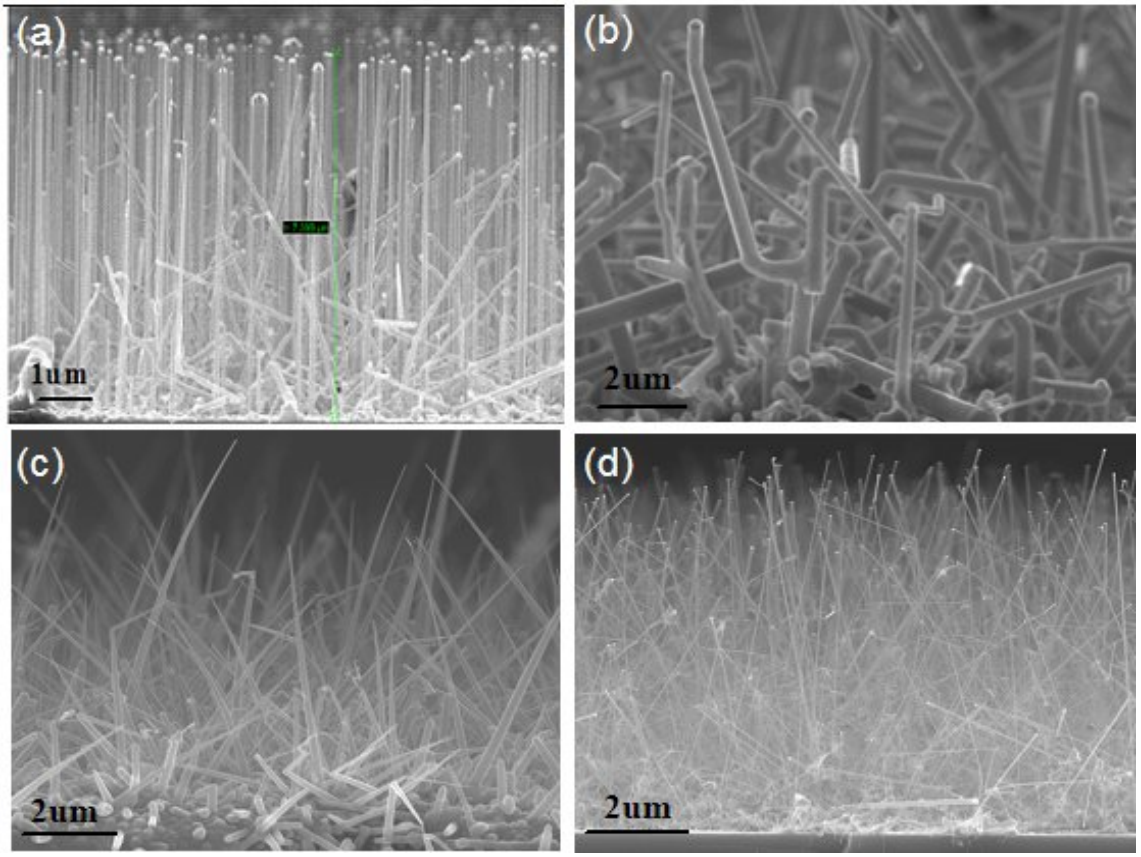

Figure 4.12: Cross section SEM image of doped Si nanowires. (a,b) Growth condition : 0.08 mbar P_{SiH_4} , 550°C, 1.1 mbar P_{tot} with (a) B:Si : 8×10^{-3} and (b) P:Si : 8×10^{-4}. (c,d) Growth condition : 1 mbar P_{SiH_4} , 430°C, 1.1 mbar P_{tot} with (a) B:Si : 8×10^{-3} and (b) P:Si : 8×10^{-4}.

Conclusion:

Using the CVD technique, dopants can be incorporated during Si nanowire growth. More specifically, the incorporation of boron in Si nanowires can be well controlled at low partial SiH_4 pressure (0.08 mbar) and 550°C. The growth rate of nanowire is relatively rapid comparing the MBE nanowire growth and is found to be related to the SiH_4 flux and also the dopant flux. For the nanowires grown at low partial SiH_4 pressure, a tapered shape is observed which is caused by the Au diffusion on the nanowire sidewall. Due to this Au diffusion, the length of this type of nanowires is limited by the initial size of Au islands. Using the controlled $\langle 111 \rangle$ growth direction and the nanowire length/Au size dependence, the boron-doped Si nanowires grown at low partial SiH_4 pressure can thus be localized on some more complex microstructures, as it is discussed in the next section.

4.3 Localized synthesis of Si nanowires

For practical applications of Si nanowires, different strategies have been explored to fabricate nanowire-based devices. The pick-and-place approach [117] has succeeded in making individual devices such as field-effect transistors, isolated thermal bridges, and chemical sensors, but it is time-consuming and unsuitable for large-scale manufacturing. The Langmuir-Blodgett technique has been utilized as a powerful and low-cost approach to align nanowires and make large-scale arrays of devices [118]. However, in some circumstances, instead of following the 'bottom-up synthesis first, assembly and top-down fabrication next' approach, it is desirable to grow nanowires precisely in predeterminated device architectures [119]. Direct integration of growth into fabrication will markedly simplify procedures and avoid deterioration of nanowires in some processes. In this part of work, we have combined the bottom-up and top-down techniques to finely control the extent of Si nanowire growth by enabling the VLS reaction to take place only at a selected region in defined some microstructures, such as Si micropillars and microtrenches.

4.3.1 Growth of Si nanowires on Micropillars

In this part of work, we investigated the growth of Si nanowires on Si micropillars. Since the size of Au islands depends on surface temperature and deposition rate, we were able to form Au islands with appropriate sizes to grow Si nanowires with a length of several micrometers. In addition, we took advantage of the ability to control the density of Au islands, to grow a very limited number of Si nanowires on Si micropillars, in a similar manner to the seminal work of Givarzigov [120] but with smaller diameter Si nanowires. This configuration allows the manipulation of a single Si nanowire for the analysis of its chemical composition using atom probe tomography (APT) technique [121].

4.3.1.1 Fabrication processes

The concept of nanowire-on-pillar structures is based on the epitaxial growth of Si nanowires along the $\langle 111 \rangle$ direction. Si micropillars with (111) faces are fabricated using the microfabrication techniques in the clean room of IEMN before the subsequent growth of nanowires on these micropillars by CVD. The fabrication processes are shown in Fig.4.13:

(a) Oxidation of the Si substrate
(b) Pattern design: spin-coating and lithography
(c) Formation of SiO_2 mask: RIE etching
(d) Formation of Si micropillars: DRIE etching and removal of the oxide
(e) Au catalysts evaporation
(f) Si nanowires synthesis: CVD growth

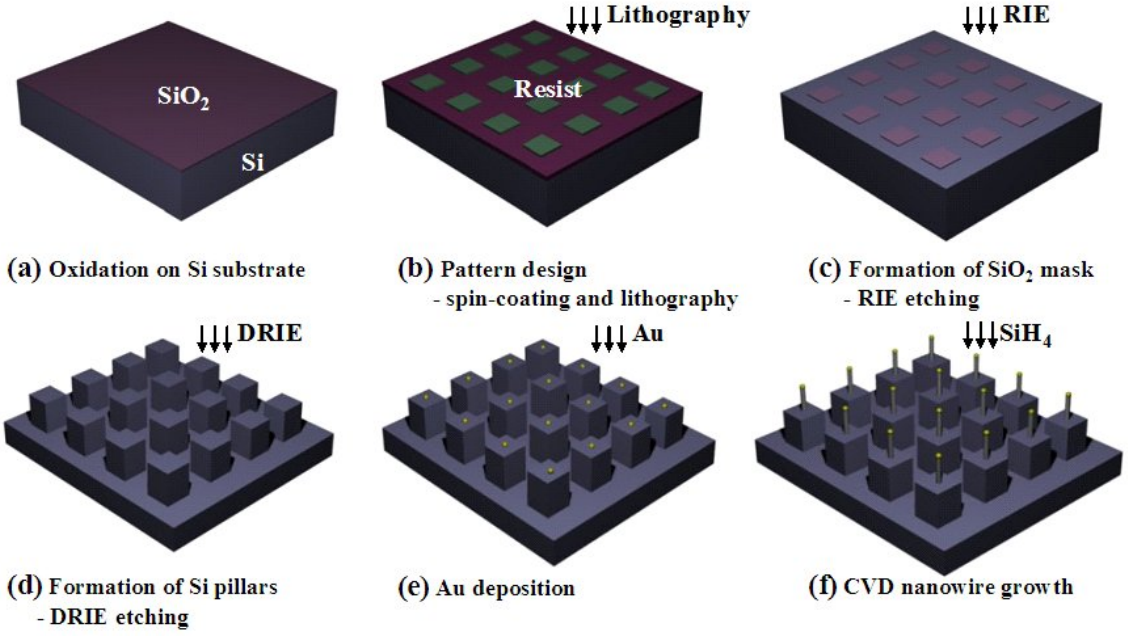

Figure 4.13: Schematic illustration of the nanowire-on-pillar structure fabrication

4.3.1.2 Experimental results

Wafer clean

N-doped Si(111) wafer with a resistivity (0.03-0.05 Ω.cm) was used as substrate in this experiment. The wafer was firstly cleaned as followed:

- Ultrasonic in an acetone bath for 10 minutes, followed by a rinse in an isopropyl alcohol (IPA) bath, and a rinse in DI water. This step is used to remove all the particles on the wafer surface.

- Rinse in piranha (Sulfuric acid/hydrogen peroxide:1/1) for 1 minute to remove organic contaminations on the wafer surface.

- Dip in Hydrofluoric acid (HF) for 1 minute to remove the native oxide on the Si surface.

Pattern design

In order to fabricate the micropillars with several tens of micrometers as height, SiO_2 was used as the mask since the selectivity Si:SiO_2 can be more than 1:150 using the dry etching technique [122]. A thermal SiO_2 film of 500 nm in thickness was thus grown on the clean Si(111) surface in H_2O vapor at 1050 °C by LP-CVD.

A negative electronic resist SAL601 was then used to define the patterns for micropillars with the different diameters and positions. Before depositing the resist, a layer of HMDS (Hexamethyldisilazane) was deposited to improve the adhesion of SAL601. The protocol used here is:

- Dehydration of sample at 110 °C on hot plate for 5 minutes.
- Spin coating resist HMDS:
  - Speed: 3000 tr/min; - Acceleration : 1000 tr/min; - Time: 20s
  Thickness measured: 60 nm

- Spin coating resist SAL 601:
  - Speed: 1000 tr/min; - Acceleration : 1000 tr/min; - Time: 15s
  Thickness measured: 1000 nm
- Annealing at 110 °C on hot plate for 3 minutes.
- E-beam lithography:
- Develop:
  - Annealing at 110 °C on hot plate for 3 minutes.
  - Soak in MF322 solution for 10 minutes.
  - Rinse in DI water

Formation of SiO_2 mask

Reactive ion etching (RIE, see Chapter 2) was then used to etch and form the SiO_2 mask. A mixture gas of CHF_3 and CF_4 was used to etch relatively quickly the oxide. The parameters of etching are shown in Tab.4.5. After etching, the residual resist was removed by acetone in ultrasonic.

CHF_3 (sccm)	CF_4 (sccm)	Pressure (mTorr)	Power (W)	Time (s)
20	20	50	180	1080

Table 4.5: RIE parameters

Formation of Si micropillars

In this part, another anisotropic dry etching Deep Reactive Ion Etching (DRIE, see Chapter 2) was used to fabricate the micropillars with height of 50 μm. The etch cycle worked with a mixture of SF_6 and O_2, whereas the passivation cycle was obtained by cracking a C_4F_8 gas. The etch parameters are shown in Tab.4.6. The Si micropillars, with height of 54 μm and width of 6 μm, were finally obtained, as shown in Fig.4.14(a) and (b).

C_4F_8 (sccm)	SF_6 (sccm)	O_2 (sccm)
100	450	50
Etch Power (W)	Passivation Power (W)	Time (s)
2500	1000	720

Table 4.6: DRIE parameters

Au deposition

Since the controlled growth of Au islands on the Si(111) surface is simply based on the proper choice of the Au evaporation rate and the surface temperature, this method allows the formation of Au seed particles on the Si(111) surface or more complex structures, such as ⟨111⟩ oriented Si micropillars. In our experiment, the sample of Si micropillars was introduced in the UHV RT-STM system and prepared by standard procedures in the UHV system [95]. For the Au islands growth, the Au evaporation rate was kept constant of 0.025 ML/s, with which the density of Au islands could be lower than an island per μm^2 at a relatively high surface temperature (see Chapter 3). Meanwhile, a nanowire with a length of several micrometers

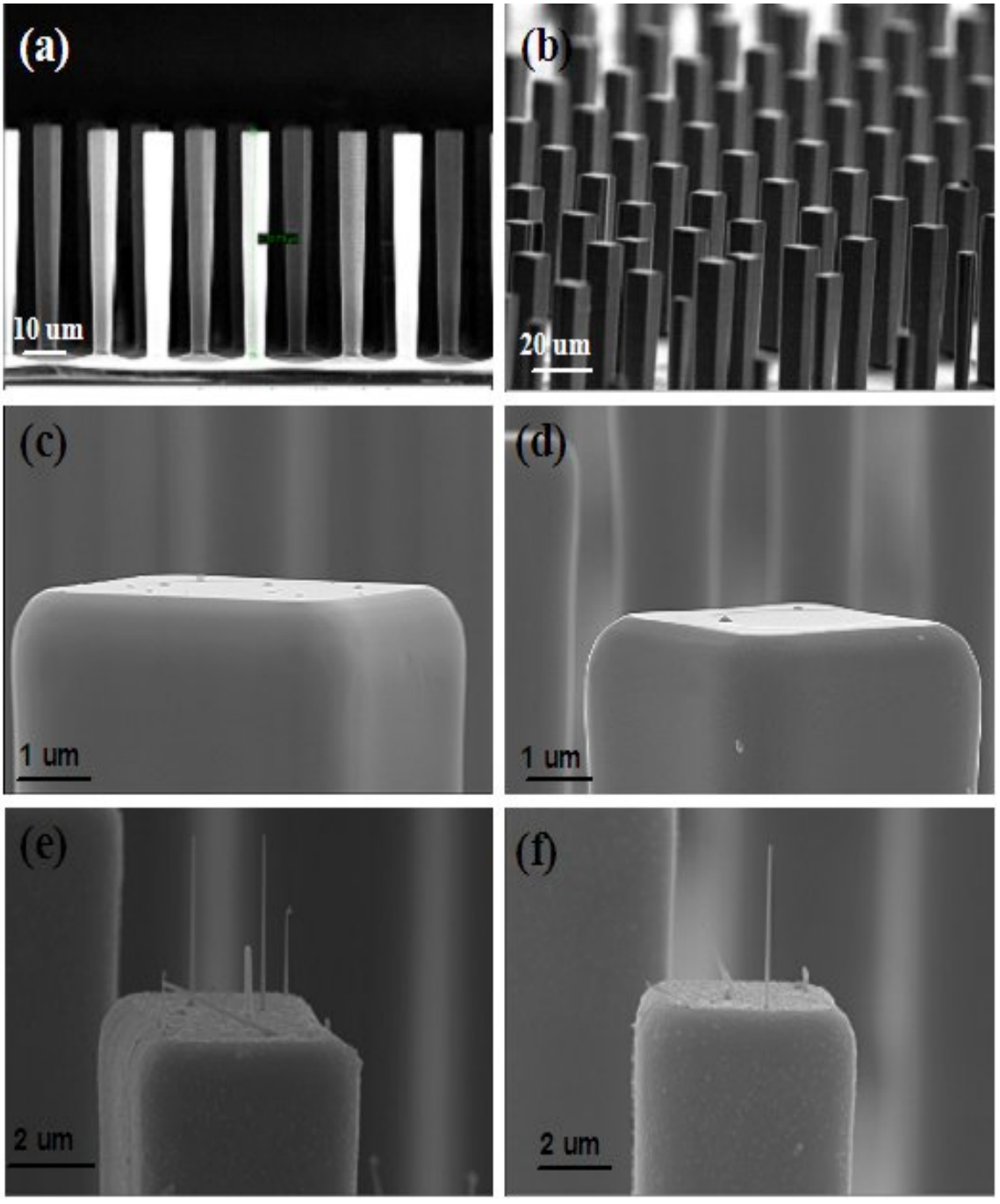

Figure 4.14: Growth of Si nanowires on Si micropillars. (a),(b) cross-section SEM images of Si micropillars with height of 54 μm and width of 6 μm. (c) Au deposition with a surface temperature of 430 °C. (d) Au deposition with a surface temperature of 470 °C. (e),(f) Growth of Si nanowires on micropillars with different density.

requires islands with a diameter bigger than 100 nm, since the seed particle is consumed during the nanowire growth [108]. Different surface temperatures were thus used to control the density and size of Au islands deposited on the micropillars. Fig.4.14(c) and (d) show several Au islands deposited on a micropillar with a surface temperature of 430 °C and 470 °C, respectively. The island distribution is in agreement with the results obtained in chapter 3: only two Au islands are self assembled at the highest temperature.

Si nanowire growth

For the subsequent growth of Si nanowires, the samples were then placed in the LP-CVD chamber and annealed at 700 °C for 10 minutes to improve the surface cleanness. A relatively low partial SiH_4 pressure was used in order to get the controlled $\langle 111 \rangle$ growth direction. The source gas, SiH_4, with a flow rate of 12 sccm, was diluted in H_2 (flow rate of 150 sccm) to set the pressure in the chamber to 1.1 mbar, the growth temperature was 550 °C and the growth time was 30 min. Si nanowires with length about 4 μm were thus synthesized on the micropillars, shown in Fig.4.14 (e) and (f). The density of nanowires depends on the density of Au islands and the small density of islands per micropillar allows the subsequant growth of a few nanowires on top of the micropillars down to a single nanowire. Since the top of the micropillar consists of a (111) face, the nanowires show a predominant vertical orientation, as it was observed for planar Si(111) surfaces. Moreover, dopants flux like B_2H_6 could be added during the nanowires growth for the incorporation of Boron in the Si nanowires on the micropillars.

Using the atom probe tomography technique, such structures are indeed appropriate to create a high electrical field at the nanowire apex that allows the field ion evaporation of atoms from the nanowire. By time of flight mass spectrometry, it is possible to reveal the three-dimensional distribution of the chemical composition in a single nanowire, as it is discussed in next chapter.

4.3.2 Growth of Si nanowire bridges in Microtrenches

In this part of the work, Si nanowires were synthesized laterally in microtrenches which were prefabricated on silicon-on-insulator (SOI) substrate, demonstrating that nanowire growth and device fabrication can be achieved simultaneously. Lateral bridging growth was first investigated for GaAs nanowires [123], carbon nanotubes [124], and recently for Si nanowires [125]. However, the distribution of the nanobridge fabricated in the previous work was not yet well controlled. Using our experiences of the controlled growth of Au islands on Si surface, we demonstrate here epitaxial growth of bridging Si nanowires and effective control of their distribution.

4.3.2.1 Fabrication processes

The nanowire-in-trench structure is also based on epitaxial growth of Si nanowires since Si nanowires grow preferentially along $\langle 111 \rangle$ direction at low partial SiH_4 pressure [105]. Some works have shown that if vertical $\{111\}$ planes can be obtained by etching a Si substrate, the nanowires should grow laterally. (110)-oriented Si wafers

contain vertical {111} planes and anisotropic wet chemical etching of a masked (110)-oriented Si wafer in KOH can etch a trench into Si, leaving {111} planes as the sidewalls of the trench. In this way, nanowires should grow laterally from one sidewall toward the opposite sidewall of the trench. If the two vertical surfaces are closely spaced, the laterally growing nanowires should impinge on the opposit vertical surface, forming the nanowire bridges. All the processes are shown in Fig.4.15:

(a) Oxidation of the SOI substrate
(b) Pattern design: spin-coating and lithography
(c) Formation of SiO_2 mask: RIE etching
(d) Formation of Si microtrenches: KOH wet etching and removal of oxide
(e) Catalyst deposition: Au angle evaporation
(f) Si nanowires synthesis: CVD growth

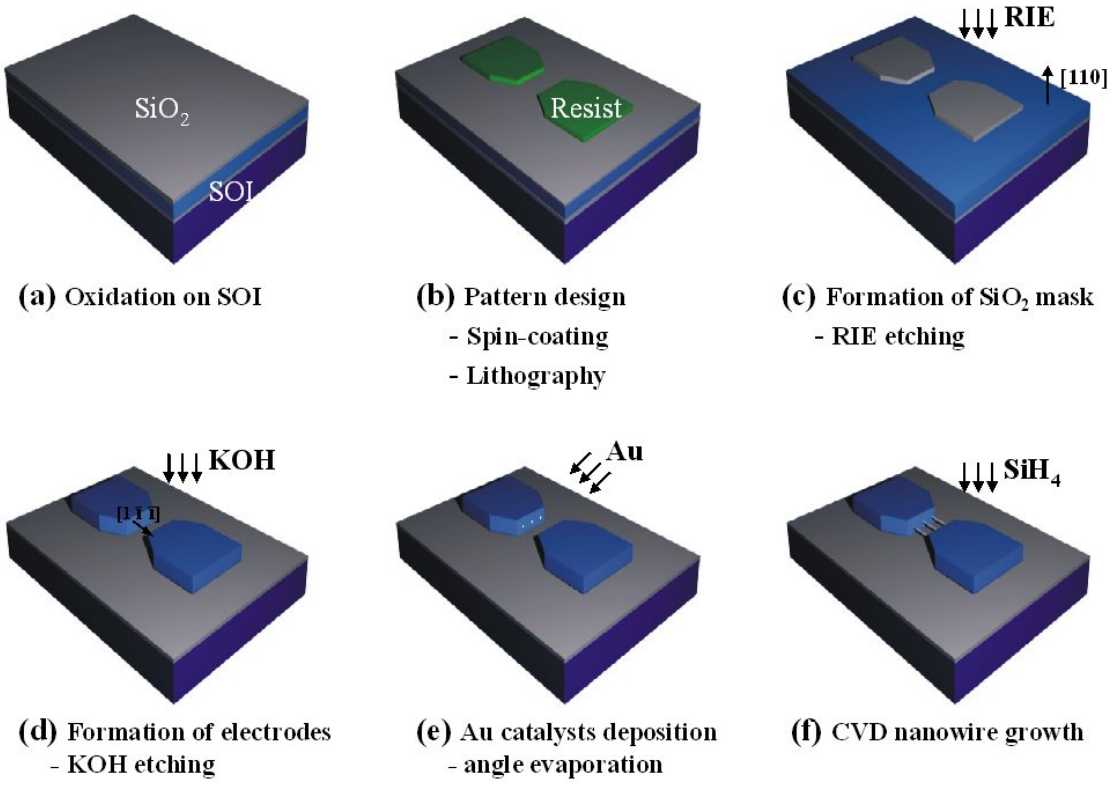

Figure 4.15: Schematic illustration of the fabrication of the nanowire-in-trench structure

4.3.2.2 Experimental results

SOI substrate

Silicon on insulator (SOI) technology refers to the use of a layered silicon-insulator-silicon substrate in place of conventional silicon substrates in semiconductor manufacturing, especially microelectronics, in order to reduce parasitic device capacitance and thereby improve performance [126]. SOI-based devices differ from conventional silicon-built devices in that the silicon junction is above an electrical

insulator, typically silicon dioxide or (less commonly) sapphire. The choice of insulator depends largely on intended application, with sapphire being used for radiation-sensitive applications and silicon dioxide preferred for improved performance and diminished short channel effects in microelectronics devices. SiO_2-based SOI wafers can be produced by several methods:

- SIMOX - Separation by implantation of Oxygen - uses an oxygen ion beam implantation process followed by high temperature annealing to create a buried SiO_2 layer.
- Smart Cut^{tm} - the insulating layer is formed by directly bonding oxidized silicon with a second substrate. The majority of the second substrate is subsequently removed, the remnants forming the topmost Si layer. The Smart Cut^{tm} process is illustrated in Fig.4.16:

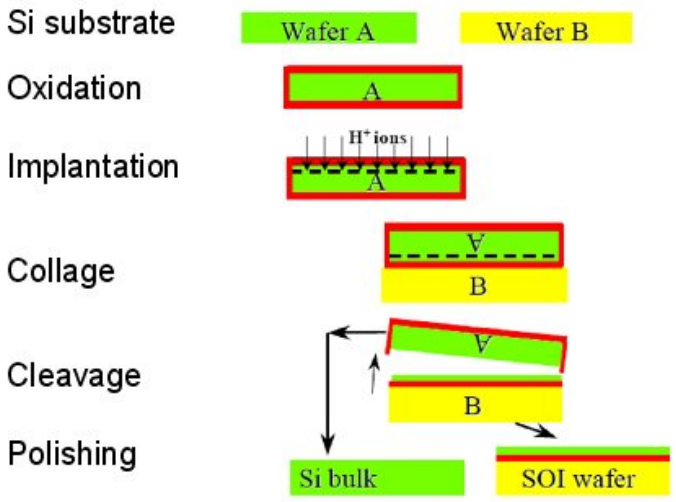

Figure 4.16: Schematic illustration of the SOI fabrication by Smart Cut^{tm} process

Two types of SOI, which are fabricated by the Smart Cut^{tm} process, from the company ULTRASIL were used in our experiments. The parameters of these substrates are shown in Tab.4.7. Si(110) is chosen as the device layer in order to obtain the vertical Si(111) faces by the anisotropic wet etching and achieve the lateral nanowire growth.

	Device layer Si(110)	Thermal oxide SiO_2	Handle wafer Si(111)	Doping of Si(110)
Type P	5 μm	500 nm	500 μm	0.07-0.14 ohm.cm
Type N	5 μm	500 nm	300 μm	6-9 ohm.cm

Table 4.7: SOI parameters

Pattern design

The SOI wafers were cleaned using the same processes as we described in the previous section. A thermal oxide layer of 100 nm as thickness was first grown on the

SOI substrate, which is patterned to serve as the mask for the subsequent Si etch. Similar resists (HMDS/SAL601) were used to define the patterns of microtrenches. The mask edges were carefully aligned along the intersections of vertical {111} planes with the top surface so that the subsequently etched trench is surrounded by two (111) surface. It is known that with an angle of 54.7° with respect to the (100) plane, the {111} planes could be obtained after the anisotropic wet etching. The pattern design process is described as followed:

- Dehydration of sample at 110 °C on hot plate for 5 minutes.
- Spin resist HMDS:
  - Speed: 3000 tr/min; - Acceleration : 1000 tr/min; - Time: 20s
  Thickness measured: 60 nm
- Spin resist SAL 601:
  - Speed: 2000 tr/min; - Acceleration : 1000 tr/min; - Time: 15s
  Thickness measured: 600 nm
- Annealing at 110 °C on hot plate for 3 minutes.
- E-beam lithography:
- Develop:
  - Annealing at 110 °C on hot plate for 3 minutes.
  - Soak in MF322 solution for 8 minutes.
  - Rinse in DI water

Formation of SiO_2 mask

The oxide was then etched using RIE with a mixture gas of CHF_3 and CF_4. The parameters of etching are shown in Tab.4.8. After the etching, the residual resist was removed by acetone in ultrasonic.

CHF_3 (sccm)	CF_4 (sccm)	Pressure (mTorr)	Power (W)	Time (s)
20	20	50	180	270

Table 4.8: RIE parameters

Formation of Si microtrenches

An anisotropic wet etching was then used to fabricate the Si microtrenches with the vertical (111) planes (see Chapter 2). In this experiments, 25% KOH diluted in H_2O was used as etchant. The etch rate was found to increase according to the solution temperature, shown in Tab.4.9. At 70 °C, the etch rate is 1 μm/min, so it takes 5 minutes to etch completely 5 μm Si(110) on the SOI wafer. Fig.4.17(a) shows a SEM image of a pair of microtrenches with the vertical {111} planes ($[1\bar{1}\bar{1}]$,$[\bar{1}1\bar{1}]$,$[\bar{1}\bar{1}1]$).

25% KOH/H_2O	50 °C	60 °C	70 °C
Etch rate (μm/min)	0.2	0.6	1

Table 4.9: KOH etch rate

Au deposition

After forming the microtrenches and cleaning the samples, the nucleating Au catalyst was deposited onto the vertical (111) surfaces of the etched grooves in our

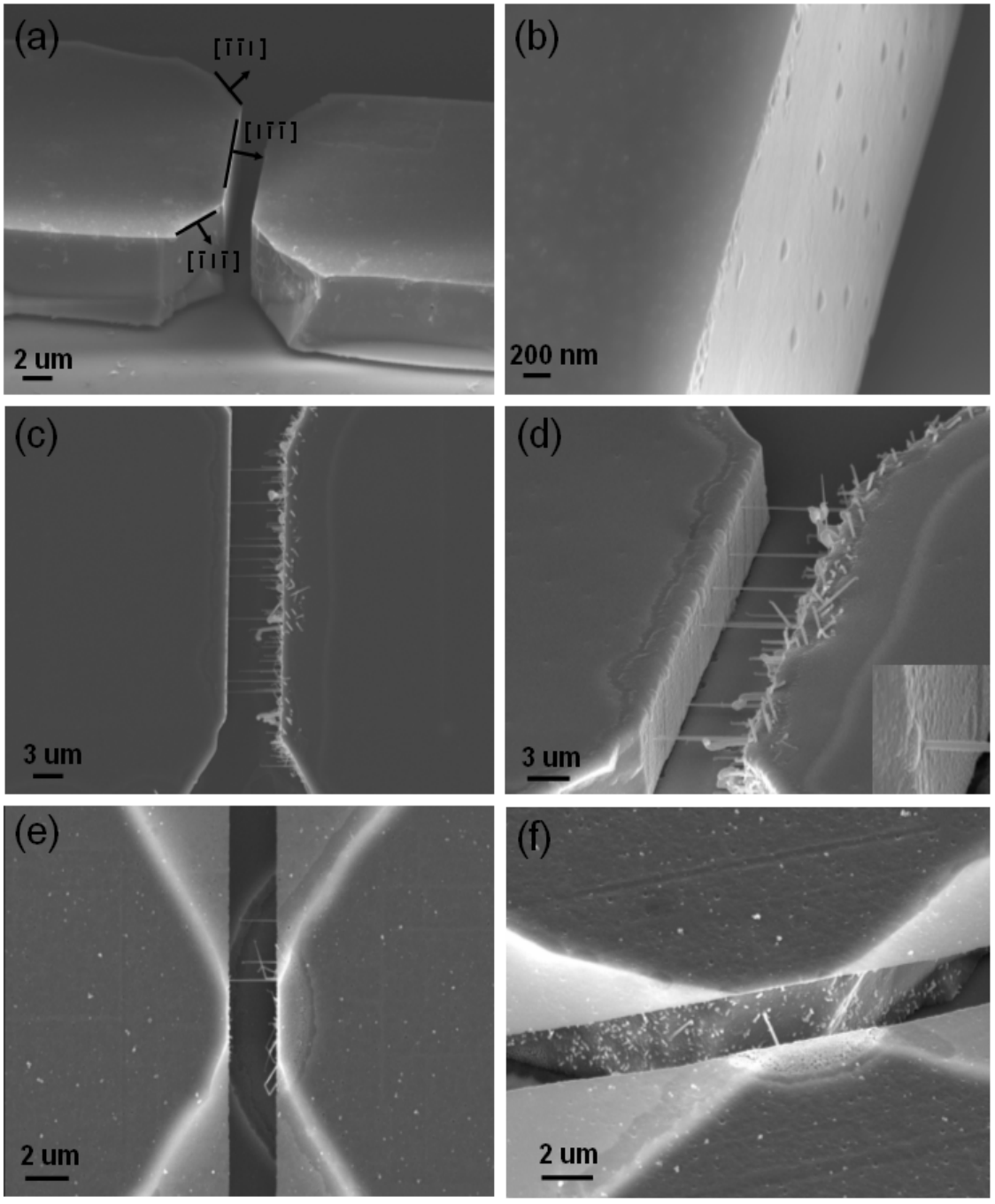

Figure 4.17: Growth of Si nanowires in microtrenches. (a) Cross-section SEM image of a pair of microtrenches surrounded with the vertical (111) planes; (b) Deposition of Au islands on one sidewall of microtrenches; (c),(d) top-view and cross-section SEM images of nanowire bridges grown in the microtrenches with a 6 μm gap; (e),(f) top-view and cross-section SEM images of an unique nanowire bridge grown in the microtrenches with a 2 μm gap. The thin layer with a bright contrast corresponds to the remmaining SiO_2 mask.

UHV chamber. The samples were held at an angle of 45 ° from the normal to deposit the catalyst on only one sidewall. This one-sided growth is not critical for the bridged structure, but allowed the nucleating and impinging ends of nanowires to be studied separately. Fig.4.17(b) shows the Au islands deposition on one sidewall of microtrench. Different densities and diameters of the Au islands could be obtained by controlling the Au evaporation rate and sample temperature, as described in chapter-Au. Moreover, no catalysts were found to be deposited on the masking oxide and the bottoms of trenches which are oxide of SOI. Indeed, the sample temperature was normally above 400 °C during evaporation and Au atoms re-evaporate on these oxide surfaces. The masking oxide could be removed after Au deposition or CVD nanowire growth by HF etching.

Si nanowire growth

The sample was then transferred through air to the CVD reactor and annealed at 700 °C for 10 minutes to improve the surface cleanness. The temperature was set at 550 °C for the nanowire growth, and a mixture of SiH_4 and B_2H_6 was introduced into the hydrogen ambient to grow the nanowires. The total pressure was controlled at 1.1 mbar, with 150 sccm of H_2, 12 sccm of SiH_4 and 1 sccm of 5 % B_2H_6. Fig.4.17(c) and (d) illustrate the top-view and cross-section SEM images of boron-doped Si nanowires growing laterally between the microtrenches with 6 μm wide gap after 30 minutes growth (growth rate estimated around 230 nm/min). Most nanowires grow along the (111) direction. The mean diameter of the base of nanowires which corresponds to the diameter of the initial Au islands has to be more than 100 nm to support the 6 μm growth.

The connection between the Si sidewall and the impinging nanowire is critical to the use of the bridging structure. One of the connections is shown in the inset of Fig.4.17(d). Islam et al have demonstrated that the lateral nanowires formed a mechanically strong connection [127]. Since the nanowire carries a molten droplet of Au-Si alloy on the top, when the nanowire impinges on the opposing sidewall, the axial growth stops and the molten alloy spreads radially, contributing a secondary nucleation. The robustness of the connection was also verified in our experiments: after some microfabrication processes like spin-coating, lithography and metalization, most connections were still remained.

More subtle control has been applied to get only one connection between the microtrenches. The width of the microtrenches was defined to be smaller and the density of Au islands was reduced by increasing the sample temperature or decreasing the Au evaporation rate during the catalyst deposition, in order to obtain a few Au islands on the sidewall of microtrench. Fig.4.17(e) and (f) illustrate the top-view and cross section SEM image of an unique connection between the small microtrenches with a 2 μm gap. The brighter contrast in the images refers to the masking oxide, which could be used to avoid the Au deposition on the tilted {111} planes of the microtrench and will be removed by HF after the growth.

The nanowire-in-microtrench structures constructed in our work provide the building blocks needed to enable the electrical measurements of the doped Si nanowires; moreover their lateral geometry is applicable to sensors where fluid should have access to the entire nanowire sensor.

4.4 Conclusion

In this chapter, we have investigated the growth of Si nanowires on Si(111) substrate using two techniques: CVD and MBE. In the CVD case, a Si containing gas is cracked at the metal droplets acting as a seed for the nanowire growth. Si atoms are dissolved in the liquid metal. Due to a supersaturation within this droplet, Si precipitates at the liquid-solid interface and form a nanowire. In the MBE case, Si nanowires are fabricated with UHV condition. The formation of nanowires is also initiated at the metal droplets, but the growth is mainly controlled by the adatoms diffusion on the surface. The objective of this work is to obtain the Si nanowires with controllable orientation, length and doping properties. After comparing these two growth techniques performed at different growth conditions, as shown in Tab.4.10, we have chosen the CVD technique, more specifically, the CVD growth at low partial SiH_4 pressure, to obtain Si nanowires with the $\langle 111 \rangle$ orientation. The growth rate of CVD Si nanowires is relatively rapid and their length is found to depend on the initial size of the Au catalysts. Moreover, dopants such as boron can be incorporated into nanowires during growth, without changing the morphology of nanowires at this growth condition.

	CVD	MBE
Growth condition	SiH_4: 0.03 - 1 mbar 550 °C	Si: 10^{-9} mbar 550 °C
Growth direction	$\langle 111 \rangle$ at low P_{SiH_4} $\langle 112 \rangle$ or incontrollable at high P_{SiH_4}	$\langle 111 \rangle$
Diameter	50-200 nm	50-200 nm
Growth rate	rapid, length > 10 μm	slow, length < 500 nm
Doping	P-type with boron at low P_{SiH_4}	

Table 4.10: Comparison Si nanowire CVD/MBE

After controlling Si nanowire growth on a simple Si(111) substrate, combining our experiences of the controlled growth of Au islands on the Si substrate, we have succeeded to localize the Si nanowires in a controllable manner (limited density, controlled position) onto some microstructures which were prefabricated by microfabrication processes. Since we can control the orientation of nanowires in the $\langle 111 \rangle$ direction, they can be thus localized vertically or horizontally on the Si micropillars with (111) top faces or between the Si microtrenches with (111) vertical faces.

For the further characterization, the atomic structure of the Si nanowires grown at low partial SiH_4 pressure will be studied by microscopic techniques in order to better understand Au diffusion during nanowire growth. The nanowire-on-micropillar structures will be used for the compositional analysis by the APT technique to reveal the 3D distribution of impurities in a Si nanowire. The nanowire-in-microtrench structures can be used as biosensor application or channels of field-effect transistors.

Chapter 5

Si nanowire characterization

Si nanowires have been synthesized in the previous chapter using Au-catalyzed VLS process in a rather controllable manner: the growth direction of nanowires can be controlled by regulating growth conditions such as silane partial pressure, while dopants can be incorporated into nanowires by using appropriate gas such as diborane. In the next step, in order to be able to use Si nanowires in the future applications, a good degree of control should be gained over their structural, physical and electrical properties. Nowadays, the development of powerful characterization tools allow the direct and precise analysis of nanowires with techniques introduced in Chapter 2, and plenty of results have already been obtained. However, several questions are still not well resolved, such as what is the atomic structure of the nanowire surface? What is the real distribution of dopants in the nanowires? Why the electrical characteristics of doped Si nanowires generally deviate slightly from those expected for an ideal nanowire?

In this chapter, a comprehensive characterization of Si nanowires is performed in order to get an overall understanding of their properties and to be able to answer the questions mentioned above. The work is generally classified into three parts:

- **Surface analysis:** The atomic structures of Si nanowire sidewalls, more specifically, the <111>-oriented Si nanowires grown at low silane partial pressure, are studied by using electron microscopies and scanning tunneling microscopy (STM).
- **Volume analysis:** The chemical composition of boron-doped Si nanowires, more specifically, the distribution of doping impurities in the volume of Si nanowires is analyzed by atom probe tomography (APT) to understand the real doping efficiency during nanowire growth.
- **Electrical analysis:** The conductivity of nanowire surface is studied using scanning tunneling spectroscopy (STS), while the volume conductivity of the doped Si nanowire is measured using single nanowire-based field effect transistor devices. Modifications of the growth conditions will be necessary to improve the electrical properties of the nanowires.

5.1 Surface analysis of Si nanowire

The surface structure and morphology, down to the atomic scale of Si nanowires is central in determining important electrical, optical, and chemical properties of the wires as well as influencing the growth [128]. As a result, detailed informations of the nanowire surface is highly relevant in designing nanowires for applications. For example, structures such as wraparound gate transistors [129] or core-shell heteostructures [130] require good control of the wire surface, both to achieve good electrical contact and to minimize carrier scattering at rough surface. Therefore we concentrate, in the first part of this chapter, in the analysis of Si nanowire surface structure by means of electron microscopy and scanning tunning microscopy (STM) in order to gain a deeper insight into the physical properties of the nanowire surface.

5.1.1 General form of <111>-oriented Si nanowire

Si nanowires were synthesized on a Si(111) substrate by the VLS mechanism using the Au-catalyzed CVD technique. More specifically, the Si nanowires studied here were grown at a low SiH_4 partial pressure and a relatively high temperature (growth condition: P_{tot}: 1.1 mbar, P_{SiH_4}: 0.08 mbar and T: 550 °C), which favor the growth along the <111> direction. This controlled direction is compatible with the self-assembly of nanowires between microtrenches or on micropillars for the integration of nanowires into devices, as it is described in chapter 4.

The general form of a typical <111>-oriented nanowire was observed by SEM as shown in Fig.5.1. The Au-Si eutectic droplet is clearly visible at the top of the nanowire, while the cross-section of the nanowire is a hexagonal with three long (L) and three short (S) sidewalls. Tilting observation of nanowire reveals the presence of sawtooth facets on the left sidewall of nanowire, which is in agreement with the previous work of Ross et al [131]. In their work, Si nanowires were grown in an UHV-CVD system at an even lower SiH_4 partial pressure (10^{-6} Torr) and at 600 °C. The growth direction was also <111>, and the same hexagonal cross-section form with alternating wider and narrower sidewalls as well as the sawtooth facets on the nanowire sidewall were observed in their experiments. They have also proposed some thermodynamic arguments to explain this phenomenon of sawtooth facet. In the simple case of growth in two dimensions (see Fig.5.1(c)). The allowed facets correspond to a wire that is widening or narrowing as it grows. When the wire grows wider, the Au-Si droplet is stretched thinner and meets the Si at a steeper angle. This generates an inward force favoring introduction of the other facet (the narrowing one). Conversely, in the case of see Fig.5.1(d), the narrowing of wire eventually leads to the droplet applying an increasing outward force on the wire, favoring introduction of the widening facet of Fig.5.1(c). While this explanation accounts for the existence of facets on the sidewall, no reason was given to explain alternating narrow and wide sidewalls. In addition, only the left sidewall shows clear facets not the right one.

A deep insight into the nanowire morphology shows that at the top of nanowire near the Au droplet, six additional faces appear which truncate the edges of the hexagonal prism and make the cross-section of nanowire become dodecagonal. The

presence of the new faces which are also faceted with tilted facets is somewhat visible in Fig.5.1(b), although the resolution of image is limited. A single nanowire was then observed with four angles in order to better understand this structure, as it is shown in Fig.5.2. At 0° and 90°, the narrow sides of the hexagonal cross-section of nanowire with the new downward tilted faces were clearly observed; while at 180° and 270°, the wide sides of the nanowire were present. The sawtooth facets are clearly visible on the three narrow sidewalls and are also visible on the wide ones, but with a much smaller amplitude and period. Moreover, these major sidewalls are separated by additional sidewalls at the top of the shaft, and their width is seen to shrink further away from the droplet until a height where the major sidewalls merge.

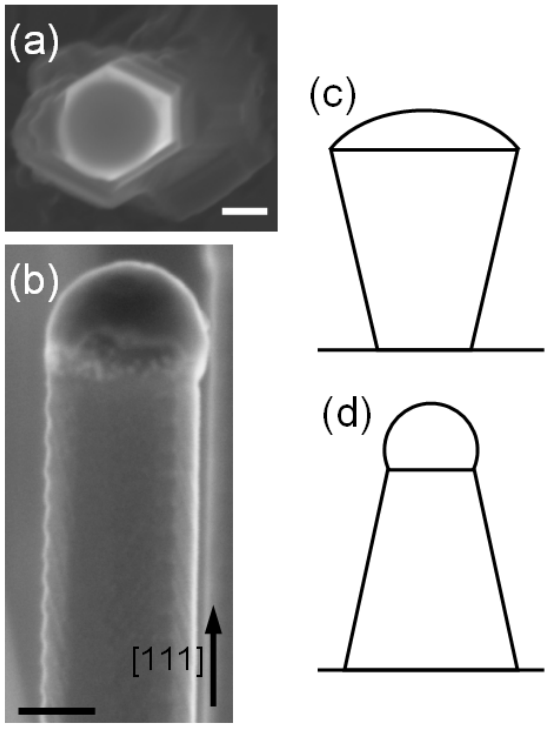

Figure 5.1: (a) Top-view SEM image of Si nanowire grown in <111> direction. Scale bar: 50 nm. (b) Lateral SEM image of the same nanowire with the visible sawtooth-facets on its left side. Scale bar: 100 nm. (c),(d) Schematic 2D thermodynamic arguments of the occurrence of sawtooth facets described in [131].

This nanowire was then zoomed in its different parts, as shown in Fig.5.3. Fig.5.3(a) is an overall SEM image of a single nanowire, while Fig.5.3(b)-(g) are enlarged views of this nanowire from its top to base. The existence of the new faces and their tilted facets can be clearly observed in Fig.5.3(b) to (d), while their size is wider at the top. The new faces become almost non-existent at the bottom (Fig.5.3(f) and (g)). The transition of the dodecagonal section to the normal hexagonal section is shown in Fig.5.3(e). All these observations are in agreement with the work of David et al [132], in which the <111>-oriented Si nanowires were analyzed by X-ray experiments. In their work, the directions of the six major sidewalls were determined as $[\bar{1}\bar{1}2]$,$[\bar{1}2\bar{1}]$,$[2\bar{1}\bar{1}]$,$[11\bar{2}]$, $[1\bar{2}1]$ and $[\bar{2}11]$, while the directions of the edges between two faces and the additional sidewalls are $[1\bar{1}0]$ and the five other

equivalent directions. These additional sidewalls were also observed but only on the large-diameter nanowires (diameter lager than 200 nm), however these new faces were always observed in our experiments whatever the diameter of the nanowires.

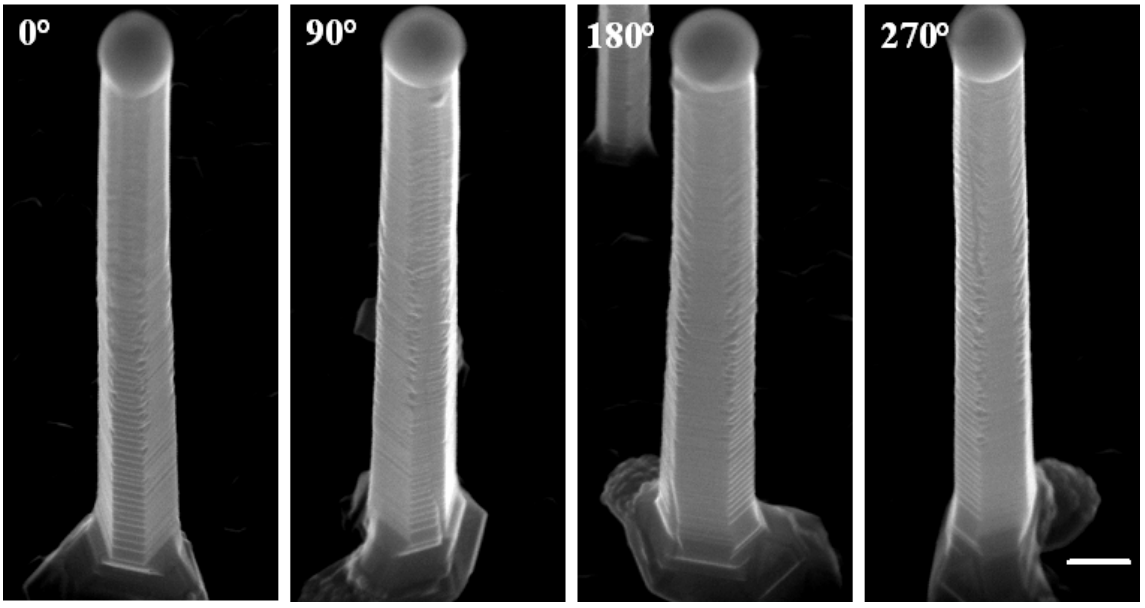

Figure 5.2: SEM images of a single nanowire with four angles of observation. Scale bar: 100 nm.

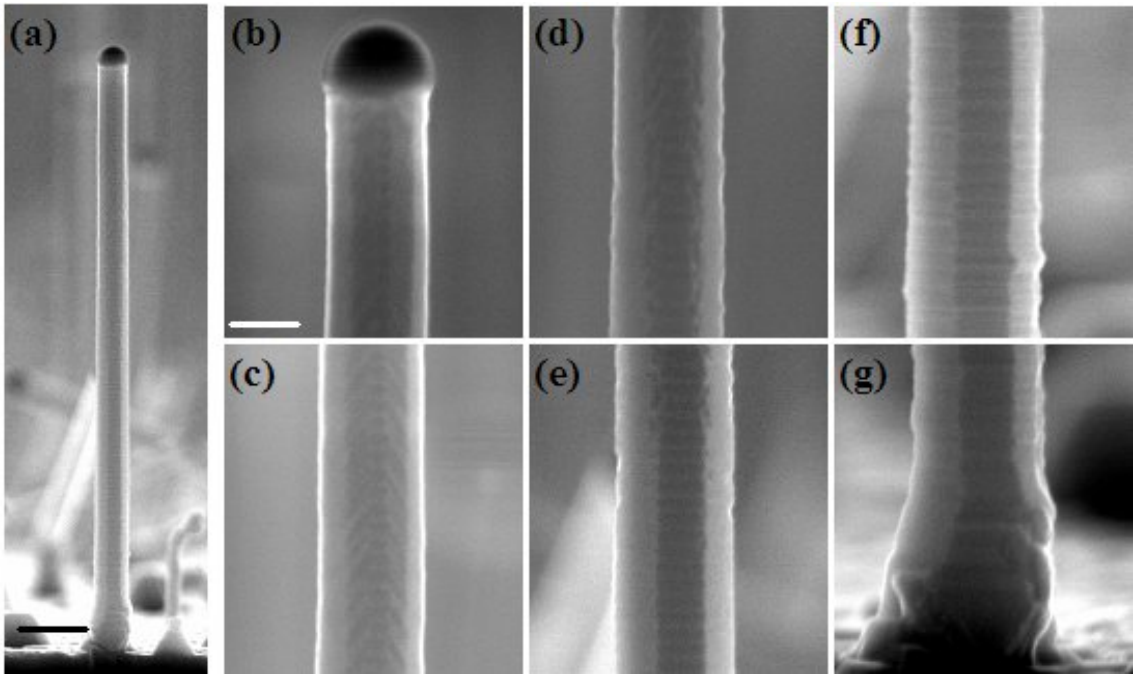

Figure 5.3: (a) Overall SEM image of a single nanowire. Scale bar: 300 nm. (b)-(g) Zoom of this nanowire from its top to underside.

5.1.2 Orientation of facets

The previous SEM analysis allows an effective observation on the nanowire sidewalls, however the resolution of SEM is always limited and the sidewalls of nanowire are so narrow that it is difficult to analyze directly and precisely. So, in this part, the TEM and STM analysis are performed in order to get more information on the crystallographic struture of the nanowire sidewalls.

5.1.2.1 TEM analysis

For TEM observations, Si nanowires were transfered by sonication of sample in isopropyl alcohol (IPA) and then deposited on holy carbon grids. The analysis of the facet periodicity along the sidewall shows that the nanowires with the larger diameter (> 200 nm) appear to have sawtooth-faceted sidewalls with a regular periodicity, as it is shown in Fig.5.4(a), in accordance to the results described in [132]. From the knowledge of the growth direction along the [111] axis, the sidewalls are found to consist of alternating downward {111} and upward {113} planes. Conversely, Fig.5.4(b) shows that when the diameter of nanowires is smaller, the sidewall is smoother. The upward and downward facets are still visible, but the regular periodicity is lost.

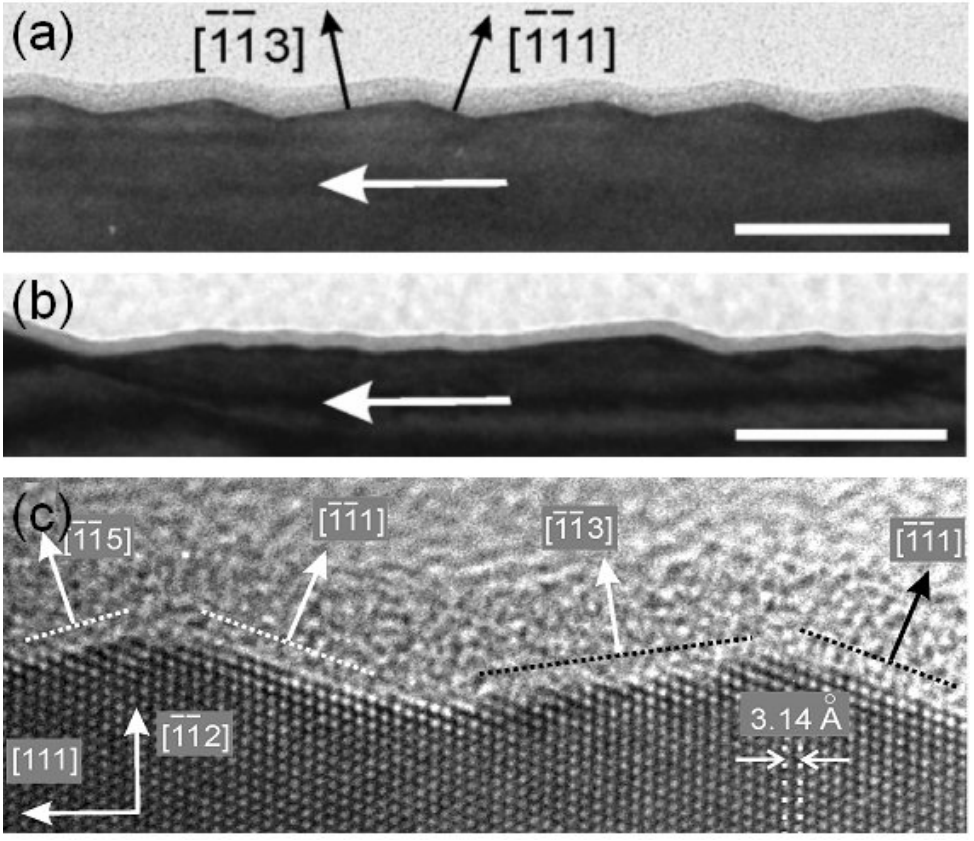

Figure 5.4: (a) TEM image of a 300 nm diameter nanowire with periodic sawtooth-faceted sidewalls. The facet orientations are indicated. (b) TEM image of a 68 nm diameter nanowire with irregular sawtooth-faceted sidewalls. The thin light gray layer in the TEM images corresponds to the oxyde layer. The scale bars correspond to 50 nm. (c) HRTEM image of the sidewall of a small nanowire.

In order to determine the facet orientations of the nanowires with a smaller diameter, HRTEM measurement along [-110] axis was acquired on a S side of nanowire, as shown in Fig.5.4(c). Based on the observation of the (111) atomic planes perpendicular to the nanowire axis, the direction perpendicular to this S side is found to be along the $[\overline{1}\overline{1}2]$ direction. Due to the hexagonal cross-section of nanowires, the directions of the other S sides are the $[\overline{1}2\overline{1}]$ and $[2\overline{1}\overline{1}]$ directions, whereas for the L sides, we obtain the $[11\overline{2}]$, $[1\overline{2}1]$ and $[\overline{2}11]$ directions. In Fig.5.4(c), the downward facets are found to be in the $[\overline{1}\overline{1}1]$ directions with an angle of 70.6° with respect to the [111] direction. For the upward facets, it is more complex: two upward facets alternate with the {111} facets. The larger one corresponds to a {113} plane, whereas the small one is measured to be about 38.9° off a {111} plane, indicating that it is a {115} plane. By performing such analysis of the facet orientations on nanowires with different diameters between 50 to 200 nm, we find that the downward facets are all oriented in a <111> direction, whereas the orientation of the upward facets might deviated from a <113> direction.

5.1.2.2 STM analysis

The SEM and TEM analysis allow the observations of the morphology and crystallography of Si nanowires, however the surface atomic structure of the nanowires is still lacking. One method which in principle can contribute to such knowledge on both the surface and electronic properties of the nanowires is STM. Indeed, for many types of nanostructures such as carbon nanotubes and quantum dots, some results have already been obtained using STM [133, 134]. However, few STM studies have been reported for nanowires and only one work presenting atomically images of surfaces of free-standing Si nanowires has been published: Lee et al succeeded to observe by STM small diameter (1 to 7 nm) H-terminated Si nanowires which were grown by the oxide-assisted growth method [135].

The difficulties presented to study the atomic structure of the nanowire faceted sidewalls by STM are that:

- The typical diameter of VLS Si nanowire used in our experiments is between 50 to 200 nm, which is much larger than the ones grown by the oxide-assisted method. The larger height can make more damage to the STM tip during observation and a much slower scanning rate is thus required.

- In order to perform the STM analysis, specially at low temperatures, Si nanowires should be transferred in the UHV condition to avoid any pollutions which could disturb the image resolution. So the classic suspension transfer method (nanowires sonicated in IPA) can not be applied.

- As shown in Fig.5.4, the TEM images reveal that the Si nanowire surface are always covered by a thin layer of oxide (with a gray contrast) due to the exposure of wires in the air after growth. This oxide layer prevents the detection of the tunneling current during STM observation and should be removed.

In our experiments, an *in situ* dry contact deposition method has been developed to overcome these difficulties. Si nanowires were transferred and deoxided in UHV, while the atomic structure of the facets on nanowire sidewalls are studied by STM at low temperature.

- UHV dry contact deposition of Si nanowires

Sample with nanowires grown at the same condition of the ones observed in the previous TEM analysis was introduced into an UHV chamber of the LT-STM system. The length of nanowires is around 11 μm and most wires grow along the <111> direction, as it is shown in Fig.5.5(a), while Fig.5.5(b) shows a single nanowire with faceted sidewalls, seen in the sample.

In order to remove the native SiO_2 on the nanowire surface, the most effective method is the chemical etching by HF, which is not possible to be performed *in situ* in UHV. Another thermal method has been reported [136]: a rapid thermal annealing (RTA) at 800°C was used to remove the surface oxide. Under this condition, theoretically, surface SiO_2 reacts with underlying Si to form SiO which vaporizes and leaves an oxide-free surface. So our sample with nanowires was briefly heated by directly passing a current through the sample in UHV at 800°C during 10 minutes to remove the thin oxide layer.

Before the transfer, a fresh Si (111) 7×7 sample was prepared by standard procedures which would be used as the plate of deposition. Using two manipulators (as seen in the photo of Fig.5.5(c)), the sample with nanowires was then manipulated into direct contact with the fresh Si substrate, nanowires were thus cleaved and transferred onto the Si surface. The result of transfer was observed *ex situ* by SEM as it is shown in Fig.5.5(d): a number of nanowires was deposited on the surface with a sufficient density, which makes it possible to find them in STM. Moreover, the SEM observations confirmed that the overall morphology of nanowires was not affected by the annealing at high temperature, as visible by the comparison of the nanowires shown in Fig.5.5(b) and (e): the facets were always presented on the nanowire surface. Meanwhile the irregular hexagonal shape of the nanowire shaft with three L sides and three S sides is better seen when the nanowires are cleaved, as shown in the inset of Fig.5.5(e).

- Determination of the facet orientation

After transfer, STM experiments at 77 K were performed on the nanowires with diameters ranging between 50 and 180 nm. Nanowires with bigger diameters are generally difficult to image because of the limited extension of the piezoelectric ceramic supporting the tip at low temperature. At a first sight, it seems to be rather difficult to scan a nanowire with such a large diameter by STM. However, due to the hexagonal shape of the nanowire shaft, we expect the wire to rest rather on a sidewall than on one of their edges. If one of their six sides is in contact with the flat Si(111) surface, the opposite side can be then almost parallel to the scanning plane and such configuration allows a good observation of the facets. The acquisition of data for a single nanowire is a time-consuming work which requires hours to days

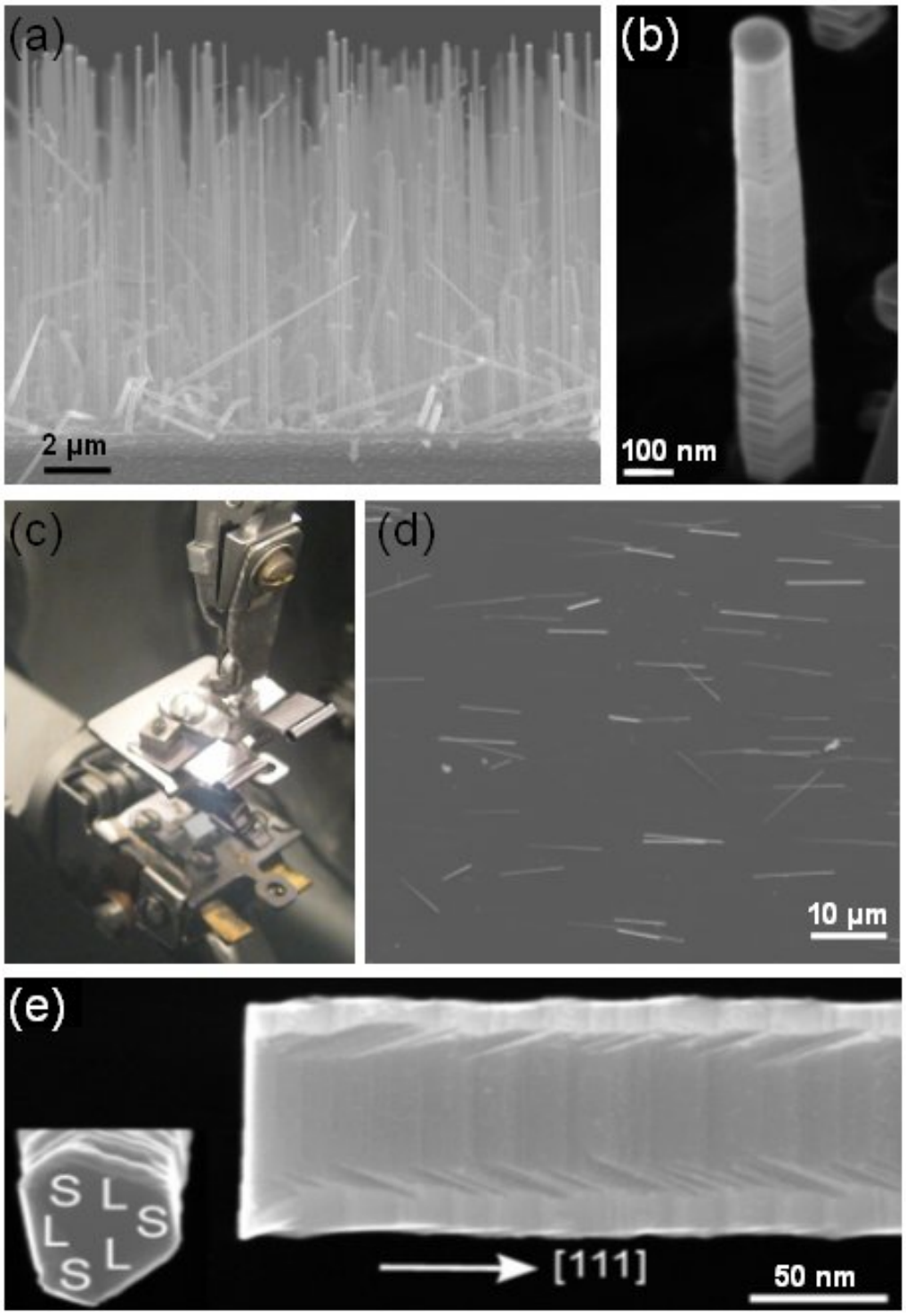

Figure 5.5: (a) Sample of vertical Si nanowires with an average length of 11 μm; (b) Zoom of a single nanowires with faceted sidewalls before transfer; (c) Photo of the manipulators used for the dry contact deposition of nanowires: the upside manipulator with the sample of nanowires approaches and scrubs onto the downside one with a fresh Si sample, nanowires can thus be cleaved and deposited on the fresh Si surface for the subsequent STM observations. (d) *ex situ* SEM image of the deposition of Si nanowires. (e) Zoom of the surface of a nanowire lying on the Si surface after transfer. Inset: Cross-section showing the nanowire base with an irregular hexagonal shape.

to locate the wires and to get a stable observation, even an important quantity of nanowires has been deposited on the surface. The sample voltage, tunneling current and temperature used in this experiment were +2.0 V, 100 pA and 77 K.

Fig.5.6(a) shows a large scale three-dimensional STM image of a nanowire with an average diameter of 170 nm, lying on the Si(111) 7×7 surface. The sawtooth facets are clearly visible on the top sidewall of the nanowire. The examination of the height profile across the nanowire width reveals that the bottom part of the profile consists of short steep line segments on each side of the nanowire, as it is shown in the inset of Fig.5.6(a). Such small line segments are attributed to the contour followed by the tip along S sides. Having a L side in contact with the Si surface certainly favors the most stable configuration and a similar positioning was successfully imaged on another nanowire shown in the under inset of Fig.5.6(c). Due to this configuration, the nanowire sidewall that are studied always correspond to a narrow sidewall.

Although in some cases the gold seed particle is not observed at the end of the broken nanowires, the growth direction of the nanowires is always obtained from measuring height profiles along the main axis: due to the tapering of the nanowires, the nanowire diameter continuously decreases toward the [111] direction. Knowing the [111] direction then allows the identification of the upward and downward facets, as it is shown in the height profile of Fig.5.6(c) which is measured along the dash line of the topographic image(b).

- For the downward facets, the angle between the normal vector of the facet and the [111] direction was measured as 71° which is very close to the value of the tilt angle between [111] and $[\overline{1}11]$ (70.6°). So the orientation of downward facets can thus be determined to be <111> direction, which is in agreement with our previous HRTEM analysis.

- For the upward facets, it is more complex since it has been found in the HRTEM observations that these facets might slightly deviate from the <113> direction when the diameter of nanowire is less than 200 nm. In the STM analysis, after identifying the orientation of the downward facets which is always $[\overline{1}11]$, the orientation of the upward facets can be determined from the angle θ between the normal vector of the facet and the $[\overline{1}11]$ direction with an uncertainty of ±1°. The facet with the smallest angle corresponds to a {115}-oriented plane with an angle of around 39° tilted off the $[\overline{1}11]$ direction, as shown in the height profile of Fig.6(c). Two other facets in the figure are also observed and are found to be more tilted off. A statistical analysis of the facet orientations reveals the existence of four different types of planes: the {115}, {117}, {119}, and {1111} planes. The values of angles between these facets and the $[\overline{1}11]$ direction are shown in the top inset of Fig.6(c). Therefore the STM observations confirm the previous TEM analysis.

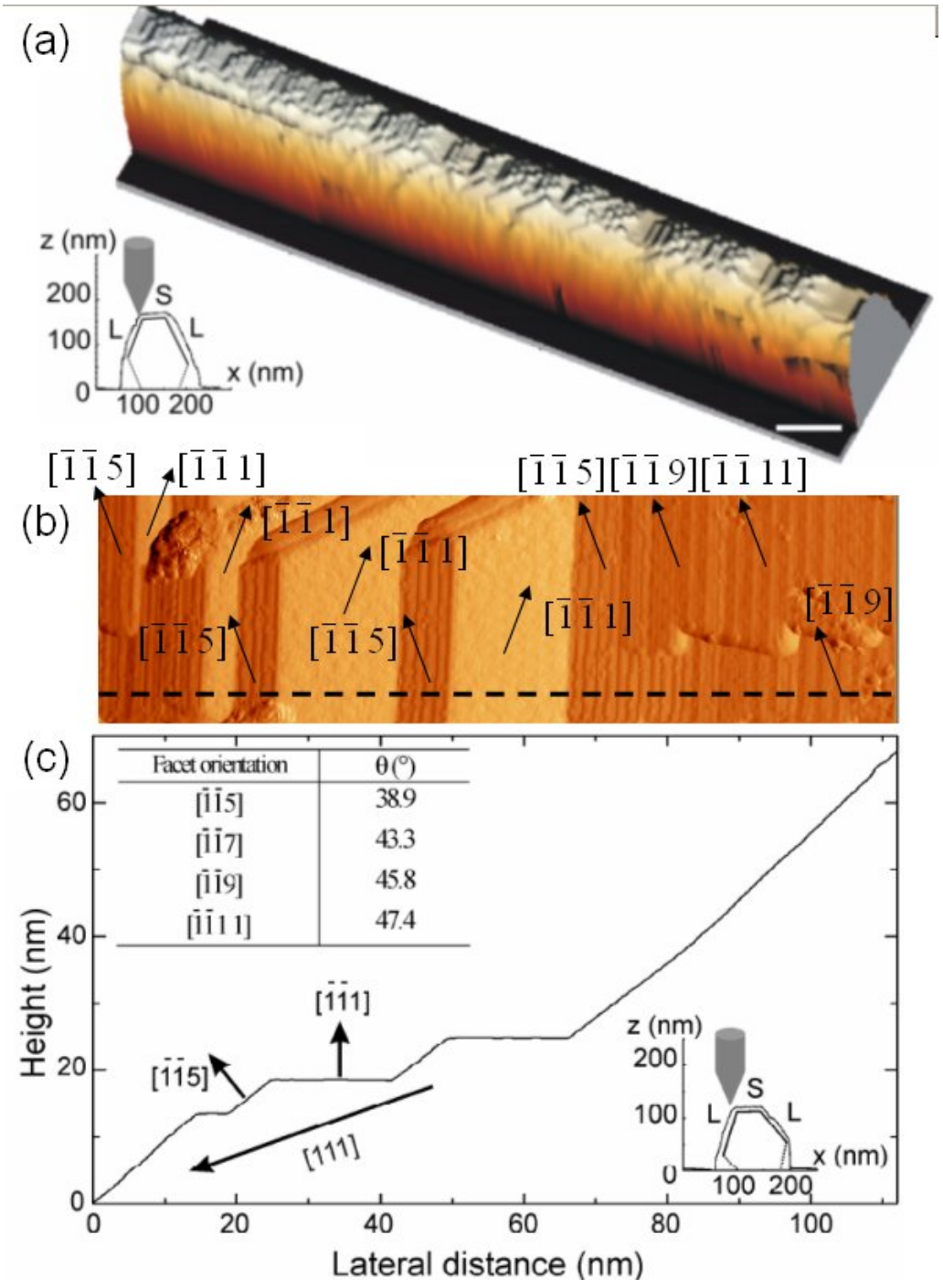

Figure 5.6: (a) Large scale three-dimensional STM image of a Si nanowire grown along the [111] direction. The average diameter of the wire is 170 nm. The nanowire is deposited on a Si(111) 7×7 surface. Scale bar: 100 nm. Inset: Topographic height profile above a schematic transverse section of the nanowire. (b) STM image of a nanowire sidewall, where the facet orientation is indicated. The average diameter of the nanowire is 120 nm. (c) Height profile measured along the dash line of the topographic image(b). Up inset: Table giving the tilt angle θ between the $[\bar{1}\bar{1}1]$ direction and the direction of the other facets. Lower inset: Topographic height profile above a schematic transverse section of the nanowire shown in (b). The STM images were obtained at a sample voltage, tunneling current and temperature of +2.0 V, 100 pA and 77 K.

5.1.3 Au on Si nanowire sidewalls

It is known that Au can diffuse very rapidly into Si and make deep centers that increase p-n junction leakage and decrease dielectric strength [137], which has to be avoided in electronic applications. Therefore, understanding the role of Au in Si nanowires during VLS growth is crucial for application of Si nanowires in electronic devices. In the last chapter, we have demonstrated that Si nanowires grown at low silane partial pressure are tapered and their length is limited. This taper shape indicates that the Au catalyst particle loses an amount of Au and Au could diffuse on the nanowire surface. However, an accurate and direct measurement is still needed, HAADF-STEM and STM analysis were thus performed to verify the presence of Au on nanowire sidewalls.

5.1.3.1 Presence of Au clusters on Si nanowire surface

From the previous SEM experiments, the width of the six sidewalls of nanowires ranges into S and L types. The S side facets are found to have larger heights and lengths than the facets with L sides. Indeed, a S side is always facing a L side. Thus by looking in a direction normal to one of the nanowire edges, which are parallel to the main nanowire axis, a cross-section of a S side with its opposite L side is obtained in the HAADF-STEM image of Fig.5.7(a). The top sidewall (S side) appears with a stronger corrugation and longer facets than the bottom sidewall (L side), where the amplitude of the sawtooth facets is much smaller.

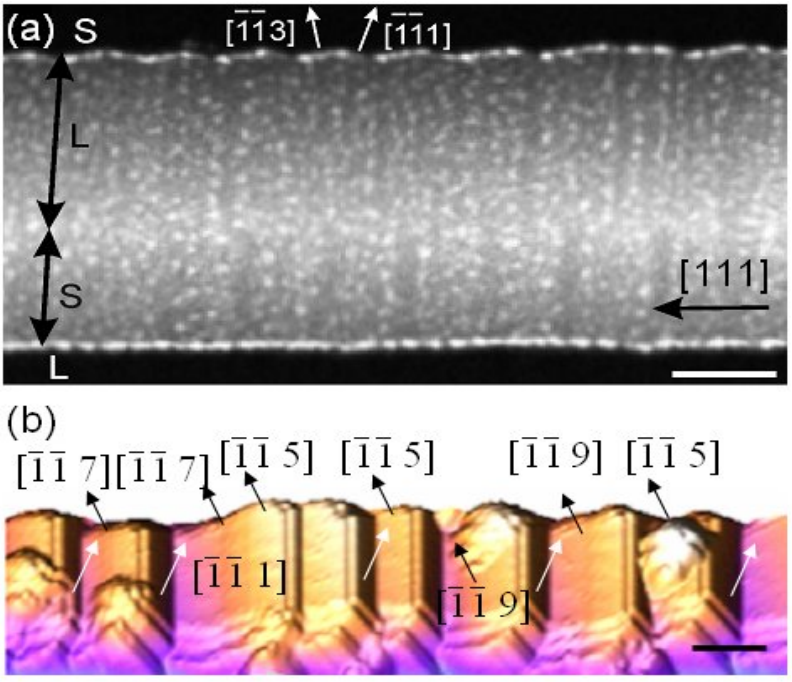

Figure 5.7: (a) HAADF-STEM image of a 65 nm diameter Si nanowire, where Au-rich clusters appear as bright protrusions decorating the nanowire sidewalls, the horizontal arrow points towards the [111] growth direction; (b) Three dimensional view of a Si nanowire sidewall, where Au clusters are seen on the high index planes only. The STM image was obtained at a sample voltage, tunneling current and temperature of -1.6 V, 100 pA and 77 K. Scale bar: 20 nm

Moreover, the HAADF-STEM image indicates that the nanowires are covered with numerous bright protrusions. The HAADF, or so-called Z-contrast, imaging shows a strong sensitivity to the atomic number (Z) (see Chapter 2). This means that the heaviest atoms are imaged as brighter dots whereas the contrast from very light atoms is negligible. Since the contrast is roughly proportional to the mean square Z, even small changes in atomic structure and chemical composition can be detected. Therefore, we attribute these protrusions to Au-rich clusters. Interestingly, these Au-rich clusters preferentially form on the high index planes, as it is visible on the sawtooth facets of the top S sidewall although the resolution is limited. In addition to this top and bottom sidewalls, Fig.5.7(a) also shows two other sidewalls, the upper one having a large width (L), whereas the lower has a small width (S). On these sidewalls, alternating bright and dark fringes appear and are better resolved on S side, where the periodicity is known to be higher. Based on the distribution of the Au-rich clusters along the top S sidewall, such fringes also reveal that the Au-rich clusters preferentially form on the high index planes. The STM image confirms the HAADF observation, as it is shown in the 3D topographic STM image of Fig.5.7(b): four Au clusters are found on the high index planes and not on the {111} planes which appear black in this STM image. In conclusion, HAADF-STEM and STM analysis of the nanowire sidewalls allow the identification of Au-rich clusters on the nanowire sidewalls, giving evidence for the diffusion of Au during growth. However, one question arise is that why the Au clusters preferentially locate on the high index plane instead of on the {111} planes? To answer this question, it is thus necessary to know the atomic structures of all these faceted sidewalls of nanowires, as it is shown in the next section.

5.1.3.2 Au-induced atomic structures of Si nanowire faceted sidewalls

Si surfaces show a variety of different surface reconstructions depending on temperature and the crystallographic orientation. Driving force for the formation of the surface reconstruction is the minimization of surface free energy, which is very often identical with a reduction of the number of dangling bonds. Adsorption of foreign elements reduces the surface free energy and it strongly modifies the electronic structure of the surface [138].

It has been shown in Chapter 3, that Au can induce Au/Si 5×2 and $\sqrt{3}\times\sqrt{3}$ reconstructions on the Si(111) surface, similar atomic rearrangement are expected to occur on the nanowire sidewalls. Such modifications are related to the lowering of the surface free energy by the metal adsorbates. A flat surface can thus be turned into 'hill and valley' structure or vice versa, depending on the orientation of the surface and the concentration of the adsorbates. In the previous HAADF and STM analysis, the Au migration on the nanowire surface during growth has been confirmed. Such observations suggest that the atomic structure of the facets could be related to the presence of Au. In order to verify this assumption, atomically resolved STM observations on the nanowire surface are performed.

- {111} facets: Filled and empty state STM images of such facets are shown in Fig.5.8(a) and (b). Their atomic structures clearly differ from the well-known 7×7 reconstruction usually observed for a bare Si(111) surface. Although

the surface is not well ordered, some patterns are reproducibly observed and arrange in an hexagonal lattice with a six fold periodicity with respect to the Si(111) substrate. Such structure is similar to the one visible in [139, 140], and corresponds to the 6×6 phase of the Au/Si(111) surface. Foe example, Fig.5.9(a) and (b) show the Au/Si(111) 6×6 structure on the bare Si(111) substrate, where the black line outlines a single 6×6 unit cell [139].

- High index facets: All the high index facets: the {115}, {117}, {119} and {1111} consist of stripes along the <110> direction, as it is shown in Fig.5.8(c) to (h). A row structure was always observed. Indeed, the stripes are well resolved for the {115} facet (see Fig.5.8(d)) and correspond to atomic rows yielding a 4×2 structure. In contrast, the stripes of the {117}, {119} and {1111}-oriented facets are more complicated to interpret although periodic structures are visible. It is difficult to accurately determine the reconstruction of these facets due to a high density of defects and their limited size (see Fig.5.8(e) to (h)).

  The atomic structures of bare Si (115), (117), (119) and (1111) surfaces have been studied by Baski et al [141], as it is shown in Fig.5.9(c) to (f). The almost perfectly periodic array of row structures oriented along the $[\bar{1}10]$ direction were always obtained. So a comparison of the facet structures of nanowires with these STM observations of a large variety of Si planes with orientations ranging from the [111] to the [001] clearly shows that the high index facet structures differ from the bare Si surface with the same orientation. Combining the observations in the last section which show the presence of Au clusters on the high index planes of nanowire facets, with the observations of atomic arrangements obtained here that do not exist on bare Si surfaces with similar orientations, we conclude that the high index facet reconstructions are also caused by Au.

Since the 6×6 phase on the Au/Si(111) surface occurs for Au coverage higher than 0.96 monolayer (ML) [142], the {111} facets roughly correspond to a Au coverage of 1 ML (equivalent to 7.84×10^{14} Au atoms/cm^2). For the high index planes, assuming that the formation of Au clusters follows the SK (island-layer) growth mode, the Au coverage should be more than 1 ML. For a more accurate measurement of the Au quantity along nanowire, Bailly et al [143] showed that the Au presenting on the nanowire sidewall is distributed homogeneously, corresponding to 1.8 ML from quantitative energy-filtered X-ray photoelectron emission microscopy (XPEEM).

After understanding the atomic structure of nanowire sidewalls, it is thus possible to explain why the Au clusters preferentially nucleate on the high index facets rather than on the (111) facets, which is observed in the previous HAADF and STM topographic images.

It has been shown that Au-islands preferentially formed on the facet areas in the case of Au adsorption on vicinal Si(100) surfaces [144] or at the top of step bunches on vicinal Si(111) surfaces rather than in the middle of flat terraces [145]. The atomic reconstruction of Si surfaces is dictated by the reduction of the energy trough the minimization of the number of dangling bonds. In addition to dimers,

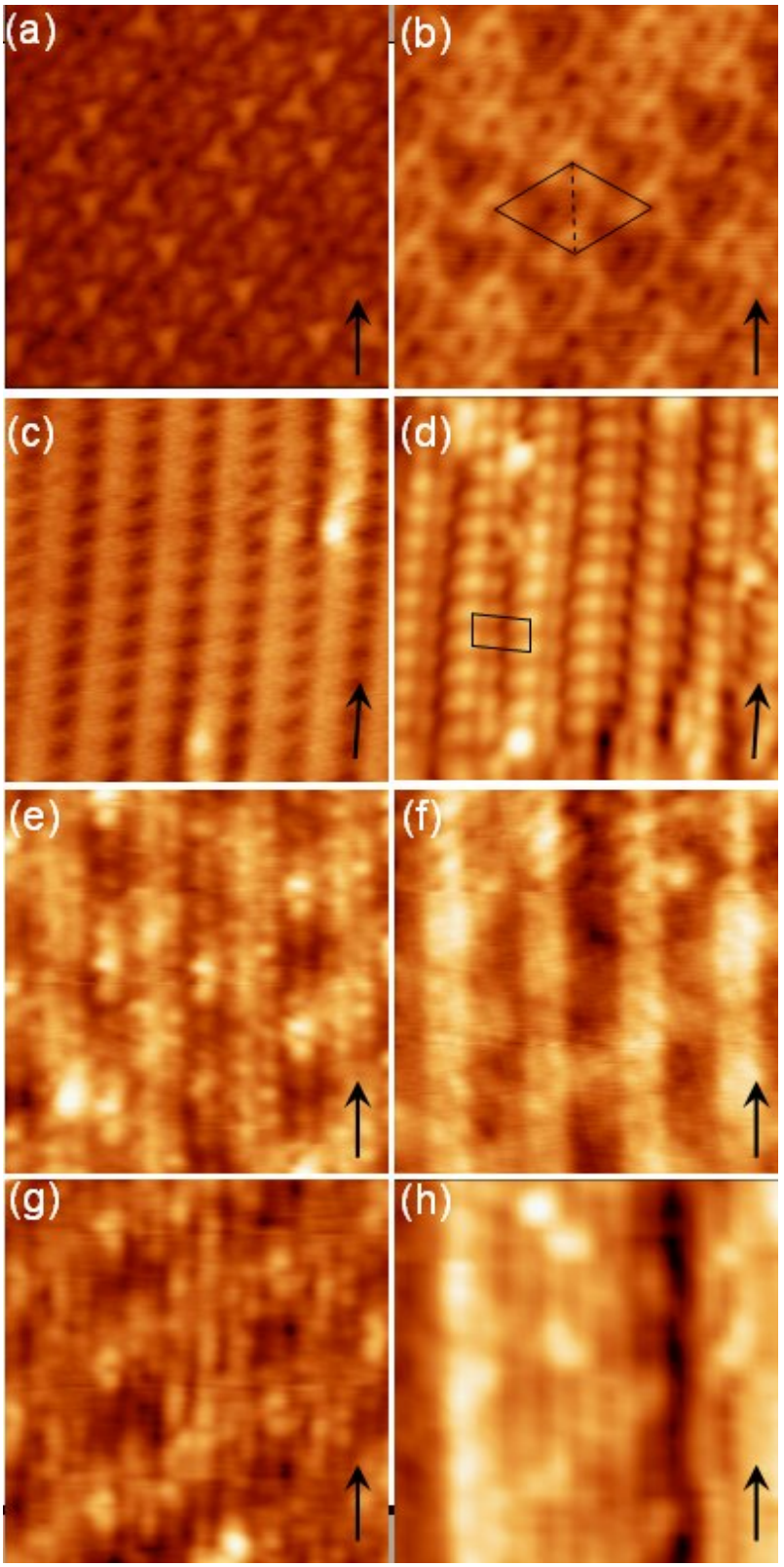

Figure 5.8: Filled and empty state STM images for the (a),(b): Si{111}, (c),(d): Si{115}, (e),(f): Si{119} facets. STM images for the (g) Si{117} and (h) Si{1111} facets. The images (a)-(b) and (e)-(f) were acquired simultaneously. The feedback parameters (sample voltage, tunneling current) were (a) -1.3 V, 100 pA; (b) 1.3 V, 100 pA; (c) -2 V, 100 pA; (d) 2 V, 500 pA; (e) -2 V, 500 pA; (f) 2 V, 500 pA; (g) -1.3 V, 100 pA; (h) 2 V, 100 pA. The sample temperature was 77 K. The vertical arrow indicates a <110> direction. The unit cells are indicated for the (a,b) 6×6 and (c,d) 4×2 reconstructions. All image sizes are 10 nm × 10 nm.

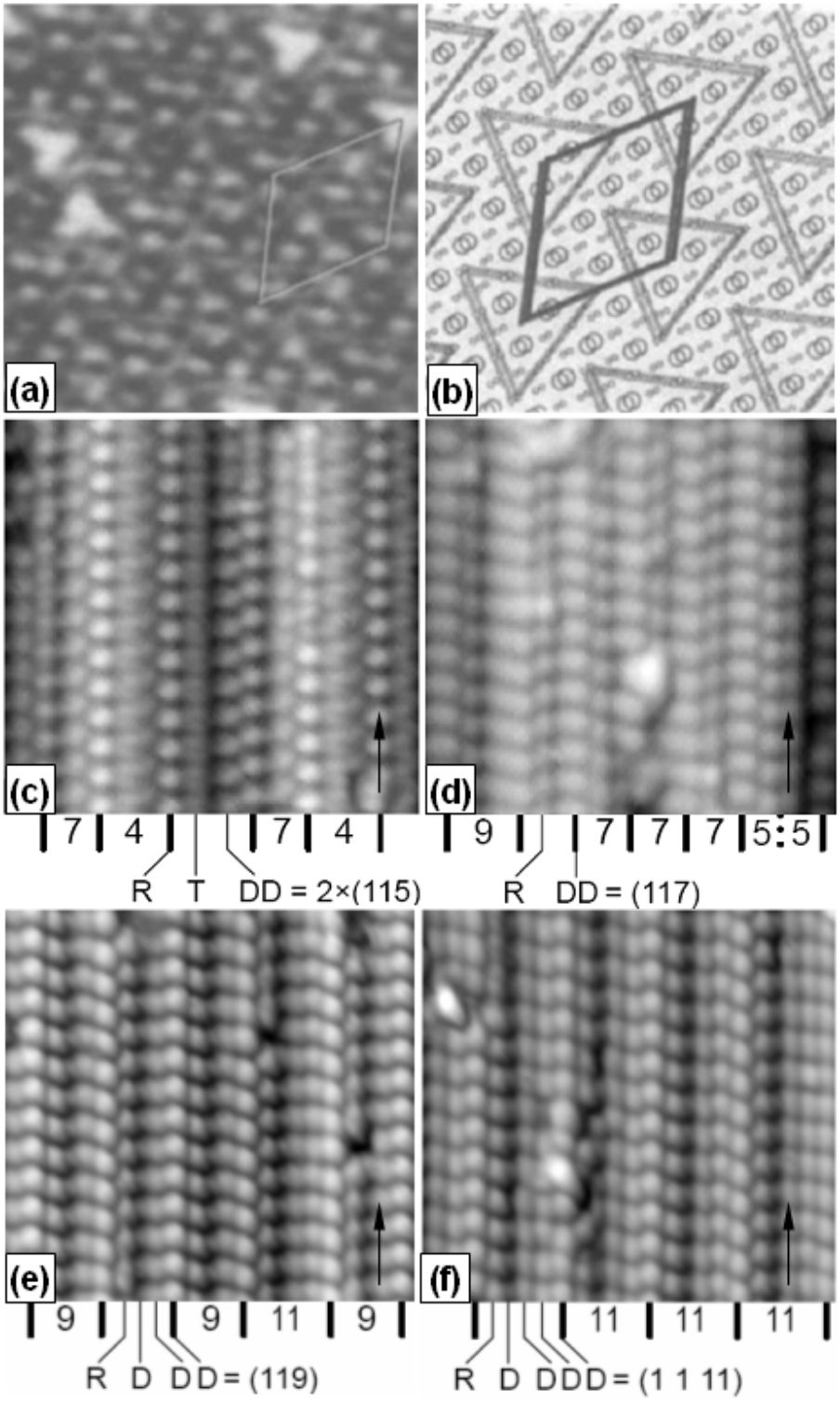

Figure 5.9: (a)-(b) STM images of Au/Si(111) 6×6 obtained in [139]. (a) An image of the Au/Si(111) 6×6 structure with V_T=0.8 V. One unit cell is outlined. (b) A domain-wall model of the 6×6 structure. Small circles indicate a 1×1 lattice, and larger circles show the positions of maxima in the image. Shaded lines show the domain walls, and the black line outlines a single 6×6 unit cell. (c)-(h) STM images of bare Si (115), (117), (119) and (1111) surfaces obtained in [141]. (c): Si(115), (d): Si(117), (e): Si(119) and (f) Si(1111). All image sizes are 10 nm × 10 nm.

high index Si surfaces generally consist of rebonded steps, non rebonded steps and π-bonded chains [141]. Because, the clusters contain not only gold, but also silicon, the incorporation of the Si atoms is easier from steps and should preferentially occur on high index facets, where numerous atomic rows are seen in comparison with the {111} planes. Indeed, the atom chains of one-dimensional surface structure on silicon, as those observed in Fig.5.8(c)-(h), are known to originate from Si atoms with broken bonds [146], and it requires less energy to detach such weakly bonded atoms than Si atoms residing in a {111} plane. In addition, rebonded steps introduce tensile surface stress. Similarly, the periodic linear atomic rows observed on the high index planes of nanowire sidewalls, as shown in Fig.5.8(c)-(h), are likely to induce a stress perpendicular to the <110> direction, which can modify the interfacial area between the cluster and the facet. Assuming a constant contact angle whatever the orientation of the facets, then a decrease of the interface energy would favor the nucleation of the islands on high index facets of nanowire sidewall rather than a {111} plane.

5.1.3.3 Control of Au diffusion on Si nanowires

After confirming the presence of Au on Si nanowire sidewalls, it is thus important to be able to control this Au diffusion during nanowire growth because of the enormous impact that even the slightest concentrations of Au dopant atoms will have on the electronic properties of Si nanowires. With this objective, Si nanowires were grown at higher silane partial pressures and lower temperatures to compare with the nanowires that we have studied in the previous sections.

Fig.5.10(a) shows a nanowire grown at a silane partial pressure of 1 mbar and a temperature of 430°C. In the region far from the Au droplet (left part of the TEM image), the contrast on the nanowire surface is homogeneous and the nanowire sidewalls are straight and parallel to the growth direction (inset of Fig.5.10(a)). Therefore, the Au diffusion can be controlled at these growth conditions. An increase of the silane partial pressure favors the adsorption of silane molecules on the nanowire sidewalls, while a lowering of the temperature reduces the rate of silane dissociation and also the mobility of Au, as it was suggested in [147]. The saturation of Si dangling bonds by silane molecules or products of the silane decomposition prevents Au from diffusing along the nanowire surface. The observation of straight sidewalls implies that the diffusion of Au is crucial for the formation of faceted sidewalls. However, the shaft appears speckled over a length of 120 nm in the region below the Au droplet located at the top of the nanowire (right part of the TEM image). The dark features with sizes of a few nanometers correspond to Au-rich clusters, as it was demonstrated in [147]. Such transitional region and the presence of Au clusters even when Si supply was sufficient, can be attributed to the different response time of pressure and temperature in the CVD reactor. When the nanowire growth was stopped, gas flow was immediately stopped and the substrate heating lamp was switched off. But the temperature response is relatively slow and it takes several minutes to fall below 300°C. During the slow decrease in temperature, the further growth of nanowires from residual silane gas and also the subsequent Au diffusion is still possible.

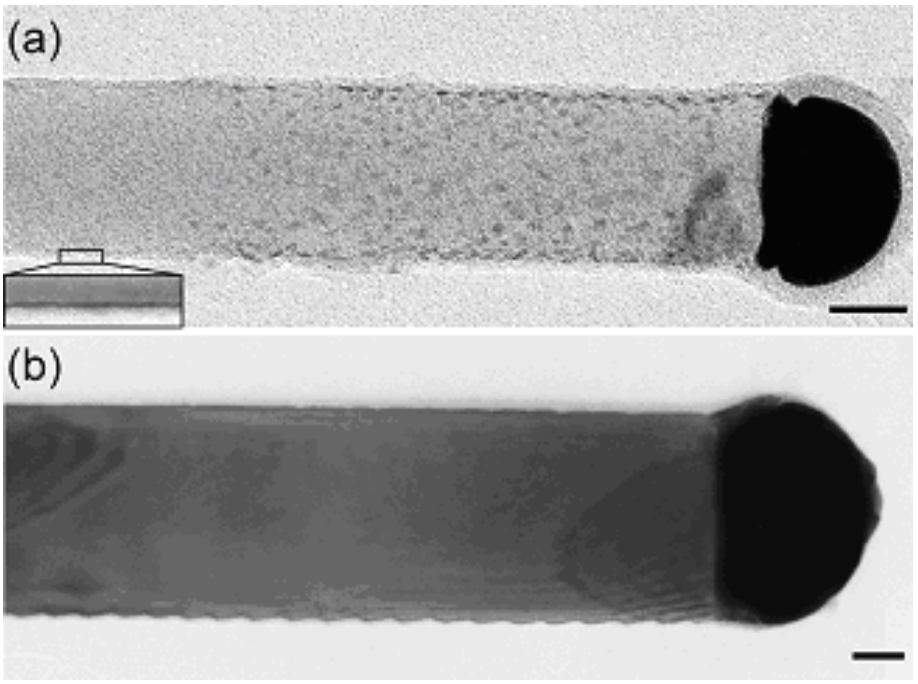

Figure 5.10: (a) TEM image of a Si nanowire with a silane partial pressure of 1 mbar at a temperature of 430°C. Dark protrusions visible on the shaft below the seed particle correspond to Au-rich clusters. Inset: zoom on the nanowire edge to show the straight sidewall. (b) TEM image of a Si nanowire grown with a silane partial pressure of 0.08 mbar at a temperature of 550°C. The nanowire sidewalls are faceted. Scale bar: 20 nm.

Fig.5.10(b) shows a Si nanowire grown at a smaller silane partial pressure of 0.08 mbar and 550°C, where both L and S types of faceted sidewalls are clearly resolved. The growth was stopped based on the same interruption procedure for the gas flow as the one used for nanowire grown at high silane pressure. Due to the high temperature inertia of the growth reactor, growth is also expected from the residual silane pressure albeit at a lower growth rate. Comparison of the catalyst-nanowire interface between both nanowires (Fig.5.10(a) versus (b)) reveals the absence of facets in the transitional region of the nanowire grown at 430°C, whereas facets are always visible just below the droplet for the nanowire grown at 550°C. Such result indicates that the formation of faceted sidewalls is favored at high temperature, corresponding to a higher mobility for the Au atoms.

In conclusion, we showed that the Au diffusion on nanowire surface can be controlled with a high silane partial pressure and a low temperature. This control can not only inhibit Au migration and also allow thin nanowire growth (thin nanowires can not grow very long if they constantly lose catalyst). Furthermore, since the presence of Au on the nanowire surface or even in the volume can make deep centers that increase p-n junction leakage and decrease dielectric strength, this control can be thus very important to improve the transport properties of Si nanowires.

5.1.4 Lateral overgrowth

The previous SEM observations have demonstrated that the nanowires grown at a low partial silane pressure and a high temperature have an irregular hexagonal cross section at the base, whereas an irregular dodecagonal cross-section is present at the top just below the catalyst particle. This modification can not be related to the interruption of growth when the pressure and temperature decrease, because it usually extends over several hundreds nanometers along the growth direction. In order to understand this change of morphology during nanowire growth, a deeper analysis was performed. Fig.5.11 shows an example of a <111>-oriented Si nanowire which was imaged with different view angles: (a1) 26°, (a2) 10°, and (b1-2) top-view observations on transferred lying nanowires. The truncated sidewalls are visible on a height of 1.9 μm in addition to the six main sidewalls. The six truncated sidewalls connect the <112>-oriented sidewalls and are assigned to be <110>-oriented. These sidewalls also consist of facets and the width of the facets is seen to shrink as they are located further away from the top of the Au particle (Fig.5.11(b1)). This decrease results in an alignment of the facets for two adjacent S and L sidewalls, which become really effective, when the truncated sidewalls have disappeared, as it is shown in Fig.5.11(b2).

Because for short growth times, the irregular hexagonal cross section is hardly visible at the base of nanowires, these observations indicate that lateral growth can occur in addition to the VLS mechanism. Therefore, the tapering of Si nanowires grown at low silane partial pressure is partly related to the reduction of the Au particle size due to the diffusion of Au during growth, and partly to the incorporation of Si species impinging directly onto the sidewalls. The base of Si nanowires undergoes the longest exposure time to the Si species, so it has the largest diameter. This latter observation is consistent with the sidewall growth obtained for III-V nanowires which is enhanced at elevated temperatures [148, 149, 150], and also for Si nanowires grown by CVD under plasma excitation [151]. Considering the surface tension γ of bare Si (111), (112) and (110) faces, it was theoretically shown that $\gamma_{111} < \gamma_{112} < \gamma_{110}$ [152]. Although the surface tensions differ when the surface contains Au adsorbates, such trend suggests why the <110>-oriented sidewalls disappear to the benefit of less costly <112>-oriented sidewalls, when lateral growth proceeds.

To confirm the existence of the lateral growth, the width of the S and L sidewalls were measured at the end of the transitional region and at the base of the nanowires, in the region where nanowires have an irregular hexagonal cross section. This region extends over a height H. By plotting the ratio between the width at the end of the transitional region and the width at the base (W_1/W_2) as a function of the Au particle diameter (D), no direct relationship appears in Fig.5.12(a). Conversely, in Fig.5.12(b), the ratio, always lower than one, is found to decrease linearly as a function of the height H. Since the flow of silane is constant during growth, this result shows that the width of the facets is directly related to the duration of growth: the facets becomes wider and wider as more and more Si species are directly incorporated on the sidewalls.

Another argument to verify the presence of lateral overgrowth during nanowire growth is to compare the measured and estimated values of the diameter at the

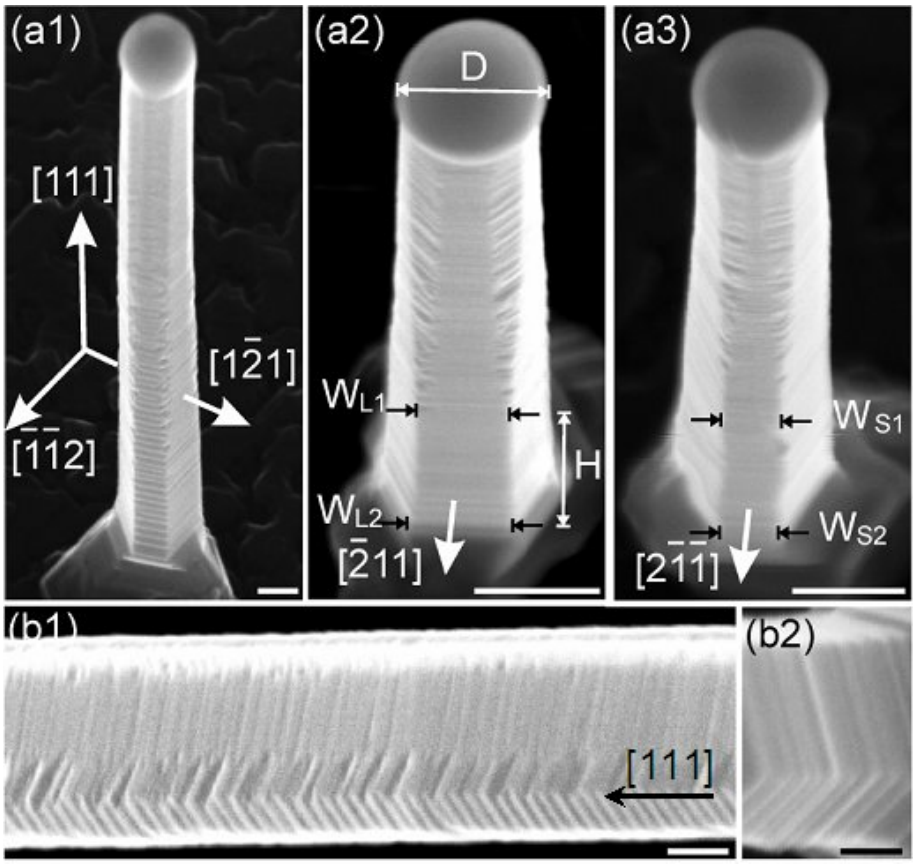

Figure 5.11: (a) SEM images of a <111>-oriented Si nanowire viewed from different directions with the sample stage either rotated at (a1) 26° or (a2-3) 10°. The orientations of the most visible sidewalls are indicated. The diameter of the Au particle, the width of the L and S sidewalls at the end of the transional region and at the nanowire base, and the height between the transional region and the nanowire base are labeled D, W_{L1}, W_{L2}, W_{S1}, W_{S2} and H respectively. (b) Top-view SEM images of the (b1) base and (b2) top of a <111>-oriented Si nanowire transferred onto a Si(111) surface. Scale bar: 50 nm

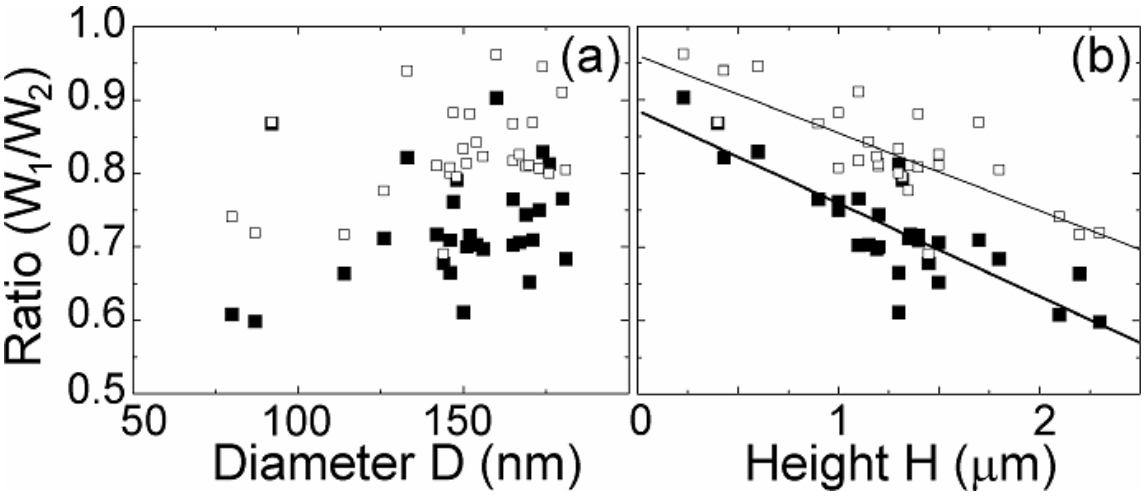

Figure 5.12: Variation of the sidewall width as a function of (a) Au particle diameter D, and (b) the height H. D and H are defined in Fig.11. The ratios between the width at the end of the transitional region and the width at the base are plotted in filled and open squares for the L and S sidewalls respectively.

base of nanowire. Because Au is known to diffuse from the catalyst particle, leading to a reduction of particle size as the growth proceeds, the diameter of the initial particle D_{bAu} can be estimated from the particle size D and the total height h of the nanowire measured by SEM after growth. Considering that the nanowire has a simplified hexagonal symmetry, as seen in Fig.5.13(b), taking into account of the small Au-rich clusters adsorbed on the sidewalls to fix the Au coverage, and assuming that the decreased volume of the Au particle is uniformly distributed on the hexagonal nanowire surface, D_{bAu} can thus be verified in the following equation:

$$\frac{\pi}{18}({D_{bAu}}^3 - D^3) = a\theta(D_{bAu} + D)\sqrt{\frac{3}{16}(D_{bAu} - D)^2 + h^2} \tag{5.1}$$

where a^3 is the atomic volume of Au (a = 0.26 nm) and θ is the Au coverage on the nanowire sidewall. Based on the synchrotron measurements of Si nanowires with similar growth conditions [143], θ was set to 1.8 monolayer. Fig.5.13(a) clearly shows that the measured cross section D_{bm} at the base of nanowire is constantly larger than D_{bAu}. Such result confirms the overgrowth process, due to the direct incorporation of Si species onto the nanowire sidewalls.

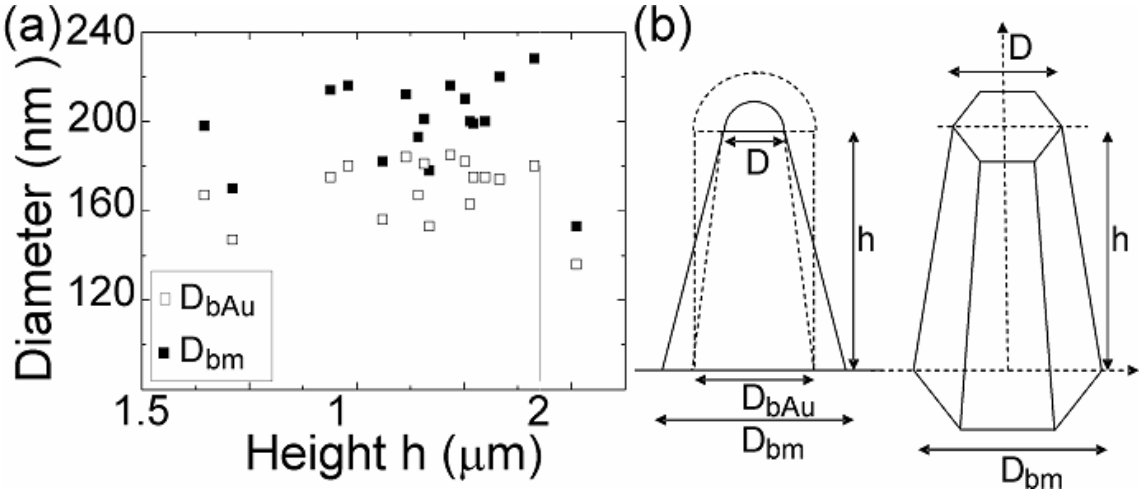

Figure 5.13: (a) Comparison of the measured D_{bm} and estimated diameter D_{bAu} at the base of the nanowires, knowing their diameter D and total height h at the end of the growth. D_{bAu} corresponds to the diameter of the catalyst particle before the growth in case where there is no lateral growth and the reduction of the particle size is only caused by Au diffusion. (b) Simplified geometry of the nanowire to determine the variation of the diameter due to Au diffusion.

5.1.5 Discussion

From the combined TEM and STM analysis, Au clusters have been found to be present on the nanowire surface, while the surface structures on the nanowire sidewalls are induced by Au. In addition to the Au diffusion, the overgrowth from the direct incorporation of species onto the nanowire sidewalls has also been found to contribute to the tapering of nanowires. However, several phenomenons are not yet clearly understood: how to explain the irregular cross-section of nanowires? Why some of the high index planes tilt from the {113} plane on the faceted sidewalls of

smaller nanowires, whereas the {113} plane is not observed by STM? Therefore, in this part, we try to study the physical mechanisms at the origin of the nanowire morphology.

Why the nanowire cross-section has alternating long and short sides?

It has been shown in Fig.5.12(b) that the overgrowth process has a faster incorporation rate along the L sidewalls in comparison with the S sidewalls. It is known that deposition of Si on a vicinal Si(111) surface by molecular beem epitaxy leads to a step-flow growth pointing towards the $[11\overline{2}]$ direction with the formation of zigzag arrays of steps perpendicular to the $[2\overline{11}]$ or equivalent direction [153]. Therefore, the incorporation of Si on the nanowire sidewalls seems to follow a similar behaviour in opposite directions. Focusing now on the top part of nanowire, where the cross-section form is dodecagonal, Fig.5.11(a3) shows that the S sidewalls are quite narrow in comparison with the L sidewalls. Such significant difference between the widths of the S and L sidewalls just below the catalyst particle indicates that the energy to form a sidewall perpendicular to the $[11\overline{2}]$ direction is not equivalent to the energy required to obtain a $[\overline{11}2]$-oriented sidewall. This result closely resembles that of Si islands grown on the Si(111) surface for temperatures between 500 and 900 K, where triangular islands are obtained rather than hexagonal islands [154] and is also in agreement with the shape of very large triangular Au-rich islands built on the Si(111) surface and observed at temperatures higher than the eutectic temperature [155, 156].

The occurrence of preferred growth orientations has been attributed to the influence of the surface reconstruction that is responsible for the existence of different nucleation barriers depending on the orientation of the step edges. Indeed, the Si(111)-7×7 dimer-adatom stacking fault surface is divided into two triangle subunits, a faulted half cell (F) and an unfaulted half cell (U). Because the growth on a faulted half cell requires rearrangement of the surface atoms, the transformation of the reconstructed surface layer towards the bulk structure is associated with a larger barrier energy. Therefore, during the homoepitaxial growth of atomic terraces on the Si(111) surfaces, the destruction of the faulted half cells is the rate-determining process for step-flow, whereas the epitaxial growth on the unfaulted half cells at the lower step edge is rapid, leading to wide and narrow steps perpendicular to the $[\overline{11}2]$ and $[11\overline{2}]$ directions respectively [157], as it is shown in Fig.5.14. As a result, we attribute the observation of narrow S and wide L sidewalls below the catalyst particle and the Si nanowire to the existence of an unit cell with two inequivalent subunits. Such assumption would explain why the lateral growth rate is higher on the wide sidewalls of nanowires, implying the formation of wide steps surrounded by half unit cell with high energy barriers. The same physical effect is expected to account for the growth of the L sidewalls at a higher growth rate than the S sidewalls below the transitional region. Considering the phase diagram of the Au/Si(111) surface [158] and the reconstruction of the {111} facets observed on the nanowire sidewall by STM, the 6×6 phase is likely to be the phase at the origin of the trigonal symmetry of nanowire, as this phase exists at high temperature [159]. The structure of the Au/Si(111)-6×6 was determined by Grozea et al [160] using direct methods

and surface X-ray diffraction data, as it is shown in Fig.5.14(c), where the primitive unit cell is indicated by solid lines and the notation Au-p for the partially occupied sites. A sight difference of the two parts of unit cell can be observed, as indicated by the two red circles, where the positions of the second layer silicon atoms are quite different. In our experiments, the STM image obtained on the downward {111} facets of the nanowire reveals that the unit cell consists of two parts with different contrast as shown in Fig.5.14(d). Combining the literature and our observations, we conclude that the growth kinetics of nanowire can be affected by the existence of an interfacial atomic structure with two inequivalent parts in the unit cell, giving an irregular cross-section of the nanowire.

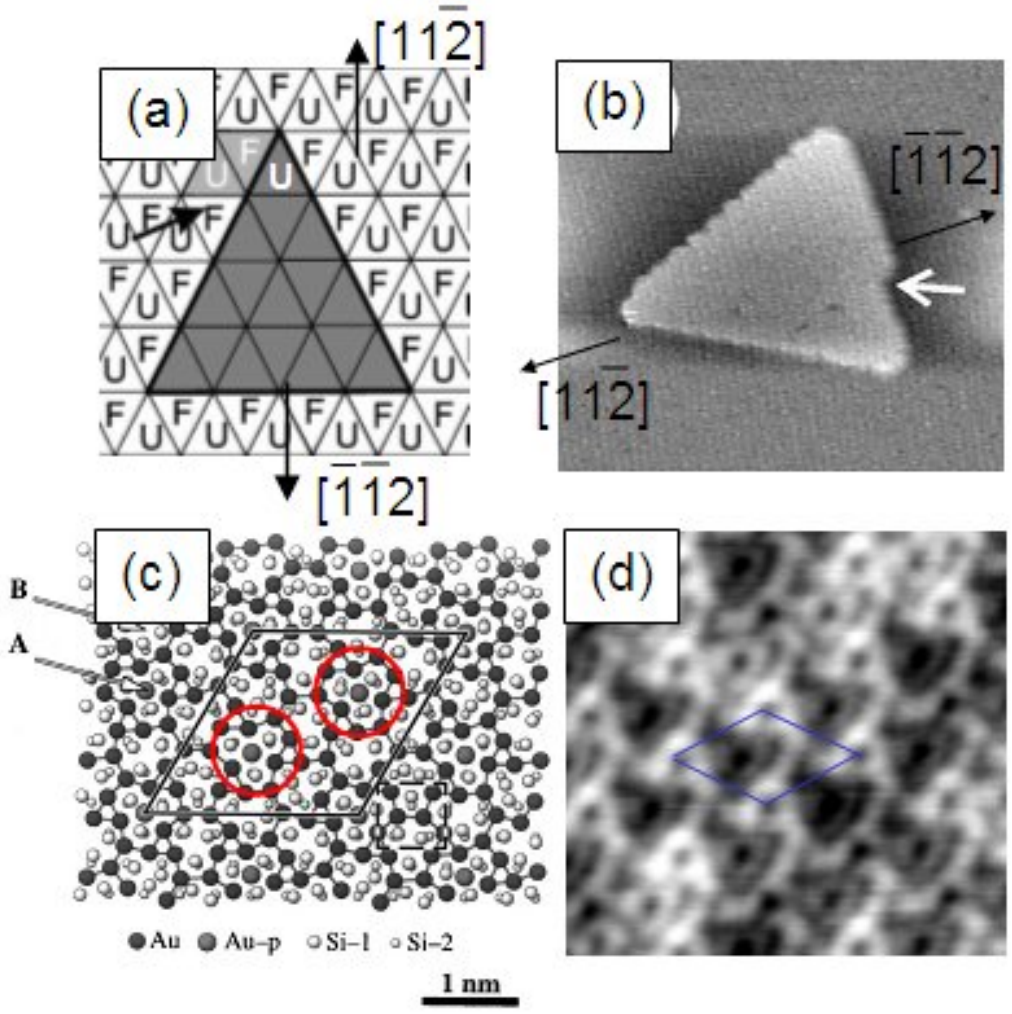

Figure 5.14: (a) Principle arrangement of the U and F parts of the (7×7) unit cells on the substrate. The higher growth speed along the [11$\bar{2}$] direction can be explained by a high energy barrier for the initial nucleation of the growth on a faulted triangle (F) in the case of the slow growing [$\bar{1}\bar{1}$2] facet, and a low barrier for the nucleation at an unfaulted triangle (U) for growth rate at the fast growing [11$\bar{2}$] facet [154]. (b) STM image of a triangle Si island grown on Si(111) substrate [154]. (c) Diagram of the Au/Si(111)-6×6 structure [160]. (d) STM image for the {111} facet of the nanowire at a sample voltage, tunneling current and temperature of 1.3 V, 100 pA and 77 K. The unit cell is indicated for the 6×6 reconstraction. The image size is 10 nm × 10 nm.

Why the facet orientations on the thinner nanowire are varied?

In addition to variations in the sidewall widths, the orientation of the upward facets are found to change along the S sidewalls on the thinner nanowires (diameter: 50 - 200 nm) while the sawtooth facets are periodic on the larger nanowires (diameter > 200 nm). It has recently been shown that the adsorption of Au on a Si(112) surface triggers a transformation of the surface [161]. Above a critical coverage, stable facets are obtained and their orientation alternates between (111) and (113) planes. From the TEM and STM analysis, it appears that some facets are more tilted than the <113> direction. Faceting of vicinal Si(100) surfaces by Au leads to the formation of stable (119) planes, but more inclined facets with respect to the [100] direction can be obtained by decreasing the temperature or increasing the Au coverage [144]. As it has been demonstrated above, silicon species are incorporated on the sidewalls during the growth. An increase of the silicon concentration on the sidewalls might thus favor the transformation of (113) planes into higher index planes. However, at the same time, Au is expected to continuously diffuse from the catalyst particle and numerous Au-rich clusters are observed on high index facets with different orientations. Therefore, it is difficult to believe that fluctuations of the Au coverage only lock the facet orientation in the case of the nanowire sidewalls.

The nanowire growth takes place at the interface between the catalyst particle and the Si shaft, and facets are already visible just below the interface, as seen in Fig.5.15(b) for example. From SEM images such as the one shown in Fig.5.15(a), it is clear that the contact angle increases as the diameter of the catalyst particle decreases. In addition, SEM top- view of the catalyst particle has a noncircular cross section (Fig.5.15(c)). The particle base accommodates to the dodecagonal cross section of the nanowire with an expansion and a contraction of the particle when it is respectively in contact with <112> (L and S) and <110> (T: truncated)-oriented sidewalls. As the contact angle increases with smaller diameters, the deformation of the particle becomes more complex. Therefore, for nanowire with small diameters, the accommodation process to wet the entire top of the shaft at the three phase boundary may induce small variations of the contact angle and thus of the facet tilt.

Taking α as the facet angle between the nanowire growth direction and the direction parallel to the facet, the contact angle θ relates to α by the Young's equation:

$$cos\alpha = \frac{\gamma_s}{\gamma_l} sin\alpha - \frac{\gamma_{sl}}{\gamma_l} - \frac{2\tau}{\gamma_l}.\frac{1}{D} \tag{5.2}$$

where γ_s, γ_{sl}, γ_l and τ are the solid (silicon), solid-liquid (interfacial), liquid (droplet) and the line tensions. By measuring the contact angles of different nanowires for the S and L sidewalls, it appears that the cosinus of both contact angles θ_S and θ_L follows the same behaviour: the angles increase as the nanowire gets thinner; θ being always smaller at the interface between a S sidewall and the particle in comparison with the opposite sidewall (see the inset of Fig.5.15(b)). From the results obtained above, α increases when the nanowire diameter becomes smaller. Since the TEM and STM analysis show the existence of higher index facets than the {113} plane on the S sidewalls of those nanowires, sinα should also increase and if the contribution of the tilted facet is high in the Young's equation, then cosα is

expected to increase. But the measurements of the contact angles indicate that the cosinus function of the contact angle decreases for smaller and smaller diameters. Therefore, the contribution of the facet inclination to the contact angle is small and due to the limited resolution of SEM, it is difficult to get enough accuracy to determine the interplay between the contact angle and the facet angle. Conversely, the line tension seems to govern the behaviour of the contact angle with respect to the nanowire diameter. Indeed, the graph shown in Fig.5.15(b) indicates that $\cos\theta$ varies as the inverse of the nanowire diameter whatever the type of the sidewall. From the fit of both types of data, the line tension can be measured and yields a positive value of $2.0 \pm 0.1 \times 10^{-8}$ J.m^{-1}, taking the particle surface tension as γ_l = 0.85 J.m^{-2} [162]. Such value is in the range of line tensions commonly measured for other systems [163].

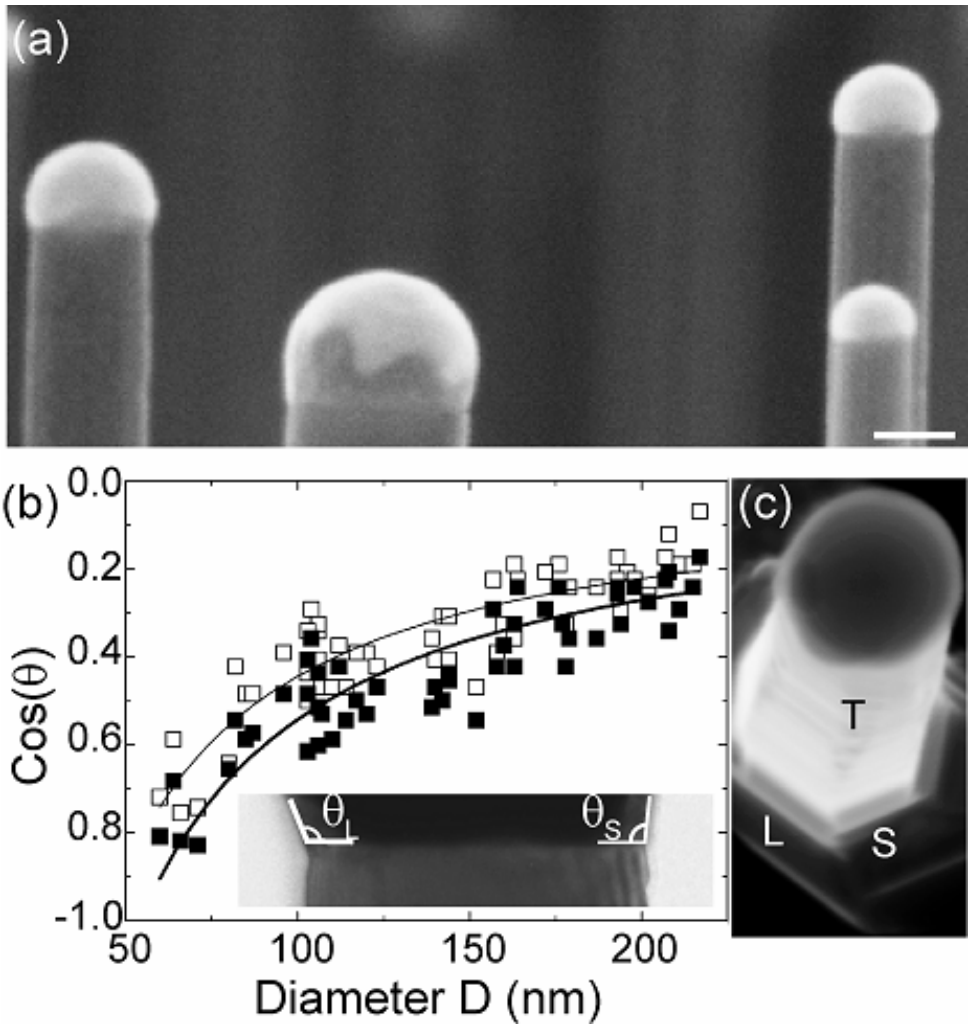

Figure 5.15: (a) SEM image of Au catalyst particles located at the top of <111>-oriented Si nanowires. Scale bar: 80 nm. (b) Variation of the contact angle as a function of the catalyst particle for the L and S sidewalls. Inset is a zoom of θ_S and θ_L on the S and L sidewalls respectively. (c) Tilted SEM images of a <111>-oriented Si nanowire, where the deformation of the particle to wet the different types of sidewalls is visible. The long, short and truncated sidewalls are labeled L, S and T respectively.

Why the STM does not reveal the {113} facets on nanowire sidewalls?

Finally, it is surprising that the {113} facets that are clearly observed by TEM are not found in the STM analysis. While we can not attribute the change of facet orientation to the annealing in UHV at high temperature, since {113} facets are found for annealed nanowires that are observed with TEM, the disappearance of the {113} facets seems to be related to the removal of the oxide layer. The existence of Au/Si(113) planes was demonstrated by adsorbing Au on high-index Si(5512) surfaces at a temperature between 600 and 800°C [164]. Surprisingly, in this case, the (113) planes did not show any ordered reconstruction in contrast to all other high index planes. Due to the small size of the nanowire sidewalls and the high probability to encounter Au clusters on the high index planes, that certainly modify the strain in the layer, the formation of {113} facets may be energetically precluded, when the oxide layer is removed.

Conclusion

In summary, by combining TEM, SEM and STM observations of Si nanowires grown on a Si(111) surface at low silane partial pressure, we can draw the following conclusions. First, the atomic structures of the facets observed on the S sidewalls have been found to be induced by Au. Then, in addition to the tapering effect attributed to a reduction of the catalyst particle size during growth because of Au diffusion, lateral growth has been demonstrated, turning the irregular dodecagonal cross-section of the nanowire below the catalyst particle into an irregular hexagonal cross-section at its base. Finally, the shape of the <111>-oriented nanowire cross section is dependent on the surface reconstruction that is induced by Au and requires a unit cell with two inequivalent parts. The STM topographic images point towards the 6×6 phase to account for the formation of nanowires with a trigonal symmetry.

5.2 Volume analysis of Si nanowires

Si nanowires of controlled doping shows great promise as multifunctional components in a number of emerging device technologies. The continued advancement of these nanometer-scale devices will depend critically on the knowledge of their atomic-scale structure [165] because compositional fluctuations as small as a single dopant atom can affect device performance. The incorporation of intentional impurities into nanowires, or doping, is usually accomplished by introducing dopant precursor gases during synthesis, as it is described in chapter 4, but the concentration and distribution of dopants has not been determined. It is therefore highly desirable to determine the composition of individual nanowires with the upmost precision. The spatial resolution of secondary ion mass spectroscopy (SIMS) has been pushed below 100 nm [166], but for nanowires, their scales of interest are much smaller. TEM is capable of imaging single dopant atom under specific conditions [167], however it can not be considered a general tool for the volumetric mapping of low-concentration elements in nanowires. Recently, atom probe tomography (APT) technique has been showed to be able to determine the composition of semiconductor nanowires at atomic scale [168].

In this part of work, we use this APT technique to demonstrate the three-dimensional composition mapping of a boron-doped Si nanowire and, more specifically, to study the dopant distribution in an individual nanowire.

5.2.1 Preparation of nanowires for APT analysis

APT is an analytical characterization technique that enables the spatial and chemical identification of atoms in a small needle-shaped specimen with sub-nanometer resolution [169]. In short, voltage pulses are used to field evaporate ions from the specimen tip and time-of-fight mass spectroscopy is used to determine the identity of the ion. A position sensitive detector is used to relate the ion trajectory to its original location on the surface of specimen (see Chapter 2). Moreover, for APT analysis of semiconductors, a pulsed laser is used in place of voltage pulse to facilitate ion evaporation. In general, the use of laser pulses instead of voltage leads to a reduced standing voltage, reduced sample fracture, better resolved mass spectra, and more facile optimization of evaporation conditions to achieve stoichiometric evaporation [170].

In order to analyze nanowires by APT, several requirements on the sample geometry have to be complied.

- The maximum radius of the specimen tip should be 50-100 nm to produce a sufficient high local electric field.
- Nanowire should be vertical on the sample tip and the number of nanowires has to be limited in order to avoid the shielding of the nanowire field by other wires.
- Nanowires should be grown on the structures such as post with a height of several tens of μm on the planar substrate to facilitate the post-growth mounting of nanowires.

Given the sample requirements described above, we decided to use the nanowire-on-micropillar structure that we have described in chapter 4 to comply with sample geometry imposed by APT technique. The schematic of the nanowire sample to be analyzed by APT is illustrated in Fig.5.16. In brief, since the controlled growth of Au islands on the Si(111) surface is based on the proper choice of the Au evaporation rate and the surface temperature, this method allows the formation of Au seed particles on the Si(111) surface of more complex structures: such as Si micropillars. A proof of concept is shown in Fig.5.17(a). In the inset of this figure, two Au islands, grown at a temperature of 470°C using a Au deposition rate of 0.025 MLs^{-1}, are seen on top of a <111>-oriented Si micropillar fabricated by DRIE process. Such a small density of islands per micropillar allows the subsequent growth of a very limited nanowires on the top of the micropillars, down to a single nanowire. Since the top of the micropillars consists of a (111) face, using a growth condition of P_{SiH4}: 0.08 mbar and T: 550 °C which favors the nanowire growth along the <111> direction, the nanowires show a predominant vertical orientation on the micropillar. Doping gas such as diborane was added during nanowire growth for the incorporation of boron into the nanowire. The ratio of B/Si used in this experiment is 2×10^{-3}.

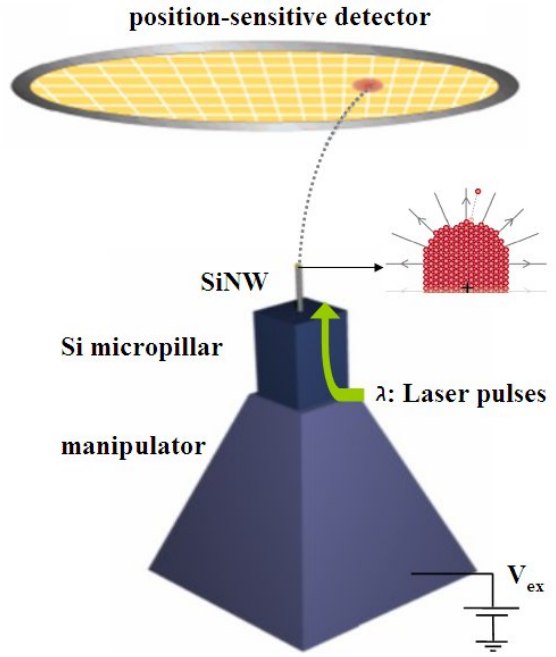

Figure 5.16: Schematic of APT analysis on a Si nanowire. An individual nanowire is grown on a Si micropillar, which is then welded on a tungsten (W) tip. Laser pulses superimposed on the DC voltage produce field evaporation of atoms from the nanowire tip. The positively charged ions travel toward the detector, where the position and time-of-flight is recorded. The inset demonstrates that a large positive voltage creates an electrical field at the nanowire tip sufficient to induce field evaporation of atoms. Enhanced field evaporation at surface asperities leads to the development of an approximately hemispherical tip shape.

The average diameter of nanowires is around 100 nm, while the height and width of micropillars are 50 μm and 6 μm. Moreover, nanowires have to protrude far enough from the planar substrate to facilitate the field evaporation of atoms from the surface of nanowire. The surface electric field (E) of the nanowire depends on the

ratio between the length of the nanowire and the width of the micropillar. Therefore, the length of nanowire should be higher than 3 μm which gives a ratio higher than 0.5 yielding a field factor smaller than 6 for nanowire diameters of the order of 100 nm. The field factor is thus small enough to evaporate ions with standard DC voltage usually lower than 15 KV [171].

Prior to the APT analysis, as shown in Fig.5.17(b)-(c), the micropillar with nanowires on the top was separated from the substrate by a focused ion beam (FIB) process and then glued to a truncated tungsten tip using *in situ* FIB. An *ex situ* additional weld by silver epoxy increases the mechanical property of the assembly. For micropillars supporting more than one nanowire, the additional nanowires were removed with FIB. The final sample to be analyzed by APT is shown in Fig.5.17(d).

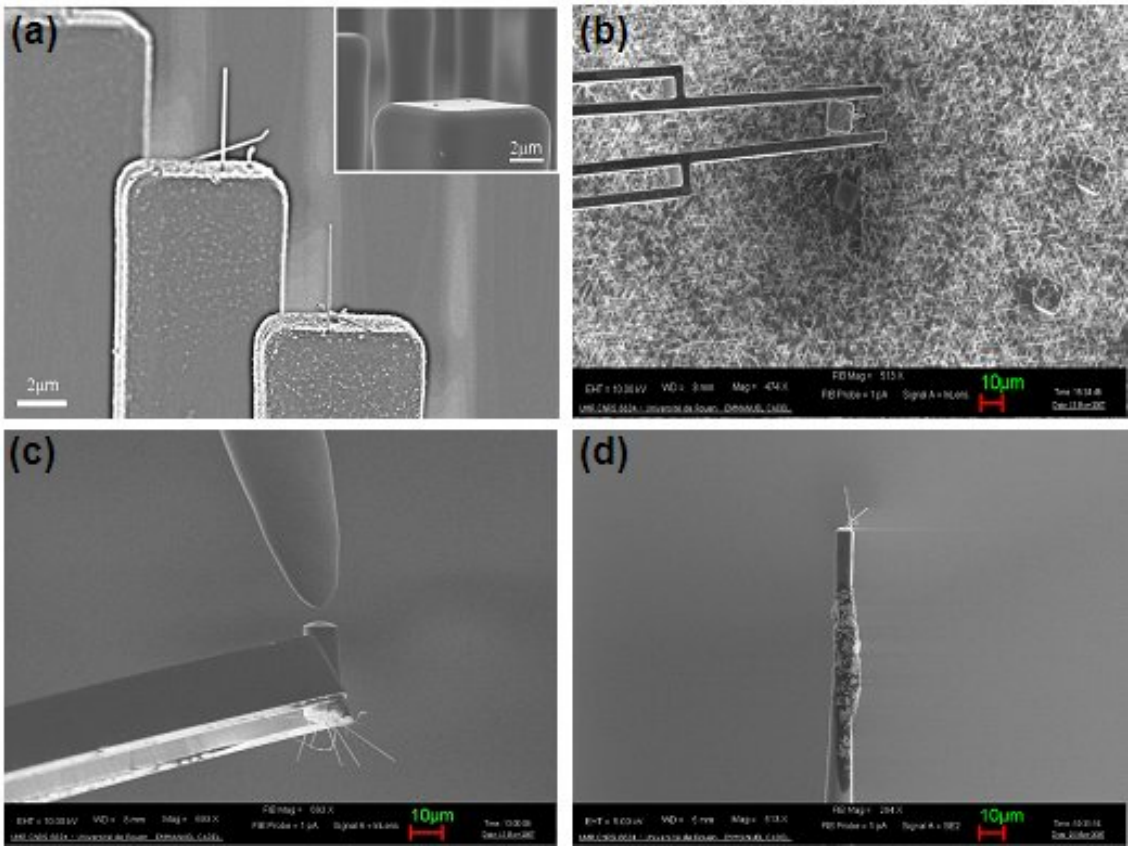

Figure 5.17: Preparation of the nanowire sample for APT analysis. (a) SEM image of micropillars with Si nanowires grown on top. Inset: SEM image of a micropillar with two Au islands on the top Si(111) surface. (b) A micropillar with nanowires on top is separated from the substrate by a FIB process. (c) The micropillar is glued to a W tip. (d) Final nanowire sample to be analyzed by APT.

5.2.2 Dopant distribution of the boron-doped Si nanowires

Nanowire surface atoms are field-evaporated by mean of high-frequency (2 kHz) laser pulses (100 nJ/350 fs) superimposed on the DC voltage. Only ions which are field-evaporated from a 20 nm wide area located in the center of the NW, held at

80 K, are analyzed by mass spectrometry, as described in Fig.5.18(a). The three-dimensional APT analysis was obtained at a collection rate of 0.4 million atom/h. During the evaporation process, the DC applied voltage remains constant due to the cylinder shape of the nanowire. Fig.5.18(b) and (c) respectively show a typical mass spectrum, and the 3D atom maps for Si and B species. The major limitations that may affect the detection of very low concentrations with atom probe are the background noise in the mass spectrum, the sampling errors and the finite number of ions taken into account. The background noise, decreasing as $\sqrt{n/M}$ (with M in amu. and n the charge state), is higher for the lightest species. The presence of a large peak can also limit the detectability threshold, in particular when the laser pulses induce thermal effect (thermal tail seen in Fig.5.18(b) for high mass to charge ratio). In the mass spectrum, the most prominent peaks are associated with double ionized silicon (mass of 28 amu) and also the silicon isotopes of 29 and 30 amu. The boron isotopes produce visible peaks, with intensity well above the noise level (established here at $\approx 5 \times 10^{18}$ at/cm^3 per atom mass unit). The presence of boron in the nanowire can thus be confirmed.

Atomically resolved three-dimensitonal reconstruction of a B-doped Si nanowire was obtained, as it is shown in Fig.5.18(c). An uniform doping distribution is observed and the doping concentration ranges between 2600 and 3000 parts per million, taking or not into account the thermal tail of the Si peak. Even though the analyzed volume ($16 \times 16 \times 58$ nm^3) is much smaller than the nanowire itself, such concentration corresponds to an impurity concentration of $1.3 \pm 0.3 \times 10^{20}$ B.cm^{-3}. It thus agrees well with the ratio of the flow rate between B_2H_6 and SiH_4 (B/Si: 2×10^{-3}) which gives a concentration at 1.02×10^{20} B.cm^{-3} for stoichiometric incorporation. Therefore, the APT analysis demonstrates that the doping level of Si nanowires can be well controlled by regulating the precursor gases.

In summary, boron-doped Si nanowires were grown on Si micropillars with a limited density and dimensions that are appropriate for a compositional analysis by APT technique. As a first result, the boron distribution was found to be uniform in the center of nanowire and the concentration was measured as $1.3 \pm 0.3 \times 10^{20}$ B.cm^{-3}. However, further detailed studies should be made to confirm the efficient incorporation of boron impurities throughout the whole volume of nanowire. It is also interesting to verify the presence of Au atoms in the volume of nanowire, since Au is known to be a deep trap and can act as a recombination center. Moreover, the doping level measured here indicates that the nanowires are highly doped. Question is then raised to know about whether these dopants are all active? So electrical measurements of the doped nanowires need to be carried out to answer this question.

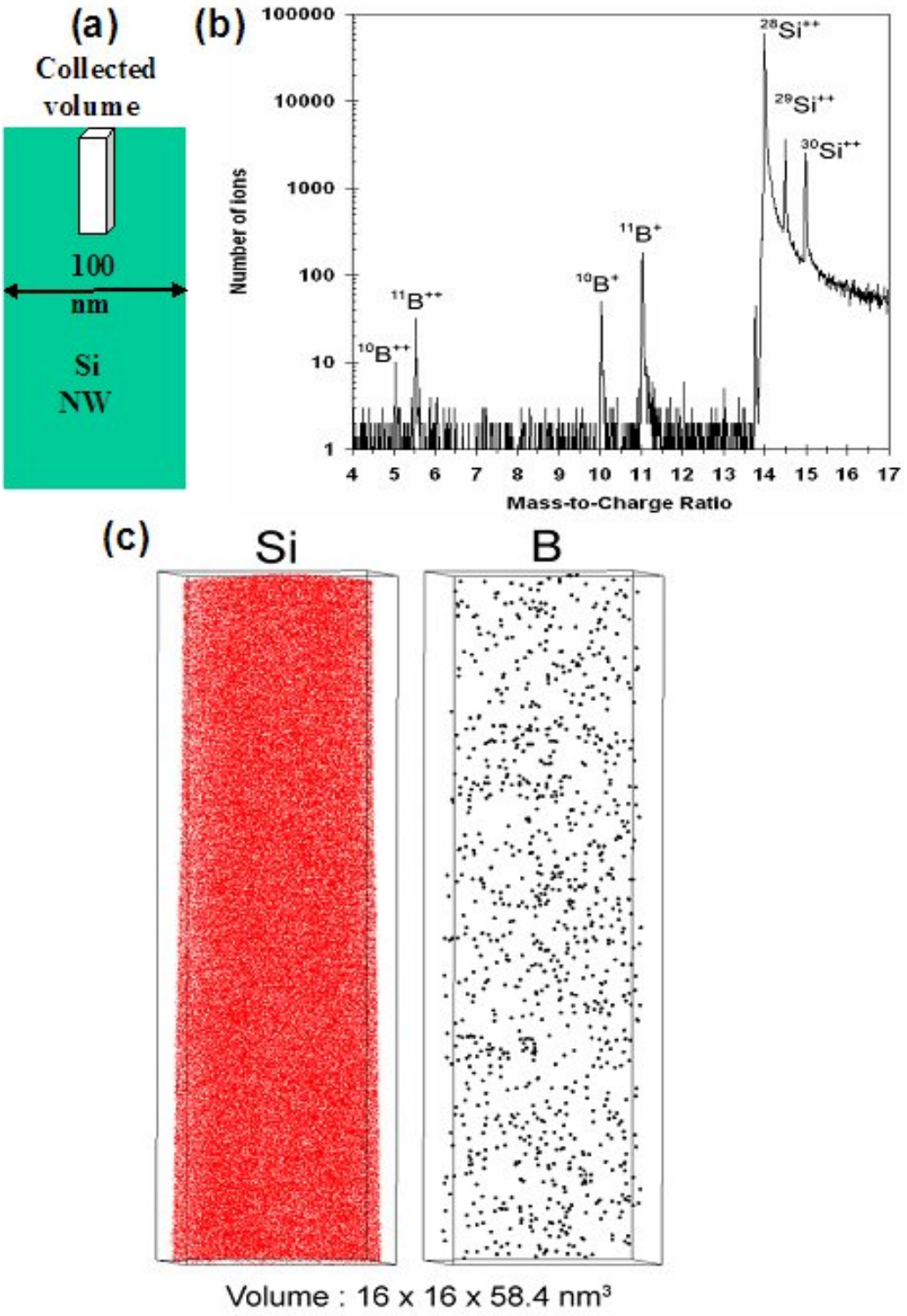

Figure 5.18: (a) Schematic diagram of the analysed volume in the Si nanowire. (b) Mass spectrum of a B-doped Si nanowire. (c) Three-dimensional of the Si nanowire for both Si and B species. The growth axis runs from the bottom to the top.

5.3 Electrical analysis of Si nanowires

In this section, scanning tunneling spectroscopy (STS) analysis are performed on the nanowire faceted sidewall in UHV at low temperature to study their surface conductance, while single doped nanowire-based FET is fabricated by Top-down approach and two/four-point probe measurements are performed in order to understand the electrical properties of nanowires and to verify their doping level.

5.3.1 STS measurements on the Au-induced Si nanowire faceted sidewalls

While the adsorption of metals on the semiconductor surface is known to create a large variety of low-dimensional surface structures, the increased interactions and subsequent correlations that the surface electrons experience can lead to surfaces with different conducting properties [146]. For the <111>-oriented Si nanowires, the presence of Au on the nanowire sidewalls is expected to have an important influence on the conducting properties of nanowire surface. As a result, STS measurements have been performed on the facets that are found with the highest occurrence, the {111} and {115} facets.

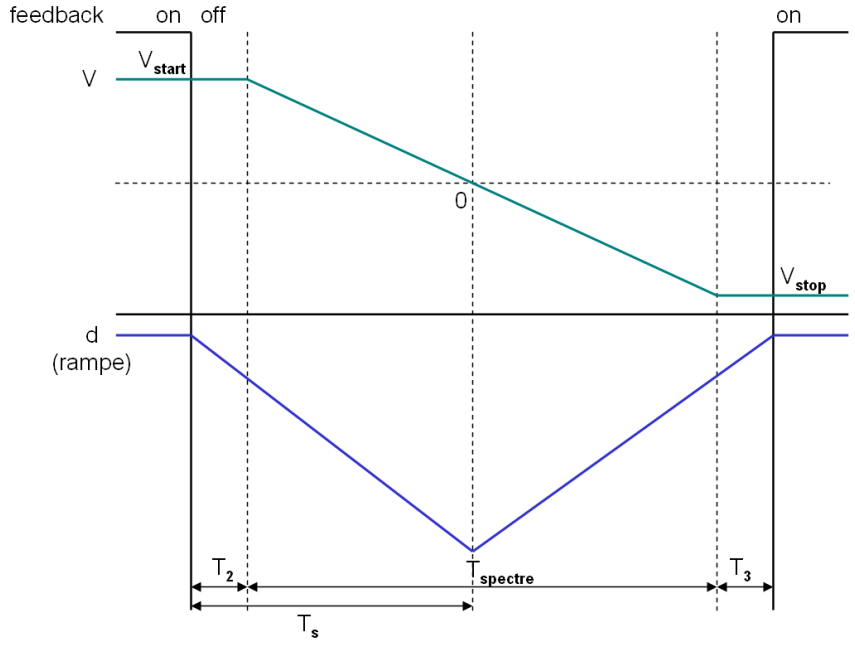

Figure 5.19: Principle of the tip-sample variable distance method.

It has been written in Chapter 2 that in the tunneling spectroscopic mode when the feedback loop is opened, the tip-sample distance is constant. The local density of electronic states (LDOS) of the sample is proportional to $\frac{\frac{\partial I}{\partial V}}{\frac{I}{V}}$. In the following experiments, a tip-sample variable distance method is used to acquire the spectra data. The principle of this method is shown in Fig.5.19: when the feedback loop is opened, a ramp is used to approach the tip to the sample, therefore spectroscopy results can be obtained with a better sensibility. The frequency of the ramp should

be fixed at $f = \frac{1}{2T_s} = \frac{1}{T_2+1/2T_{spectre}}$ to perform the spectroscopy when the tip is close mostly to sample, while T_s should be $\leq (T_{spectre} + T_2 + T_3)/2$ to synchronize the ramp with the feedback loop. T_2 and T_3 is the stabilization time to open and close the tunneling current.

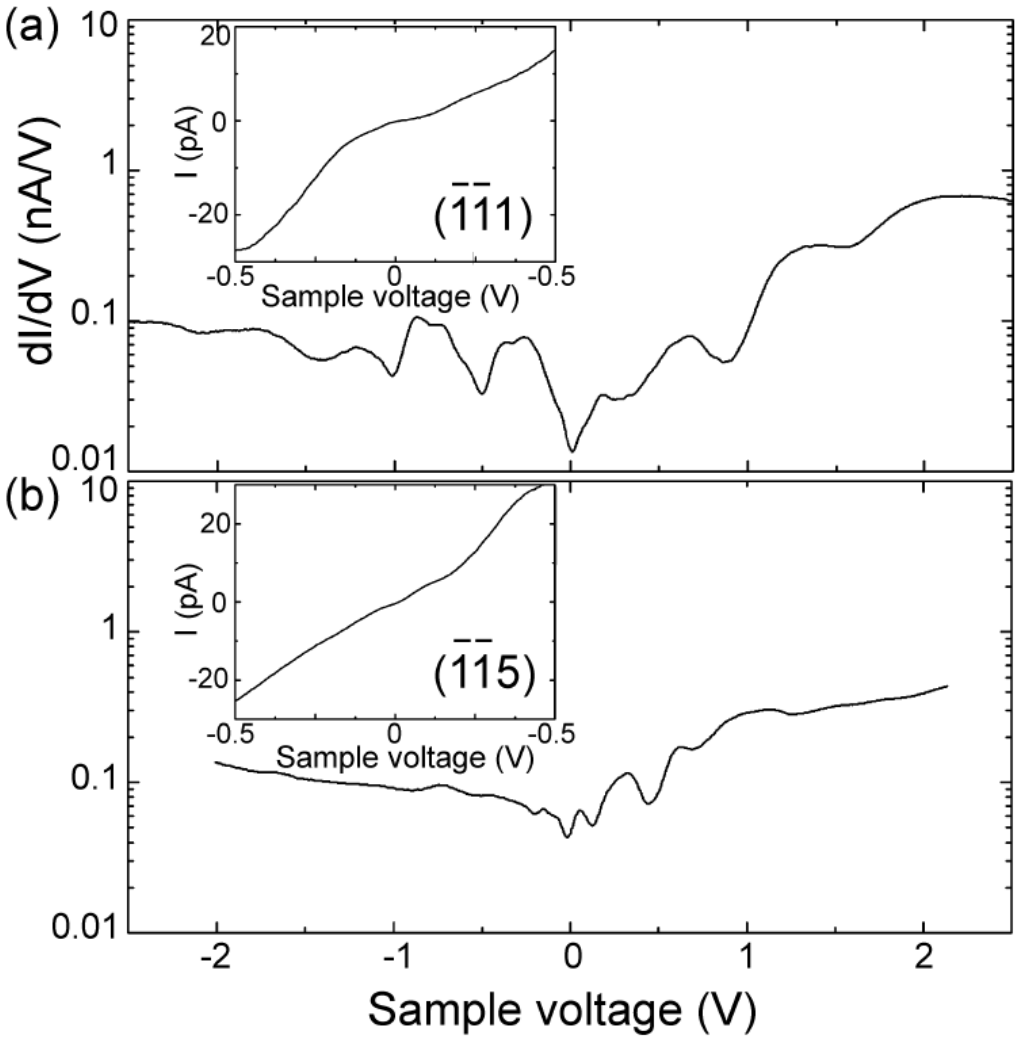

Figure 5.20: Differential conductivity spectra measured on (a) Si{111} and (b) Si{115} facets. The insets show the tunneling current spectra on a smaller voltage range. The feedback parameters (sample voltage, tunneling current) were (a) -2.5 V, 100 pA, and (b) -2 V, 100 pA at a temperature of 77 K. Both spectra were acquired with a tip-sample variable distance method where the tip was approached linearly towards the surface at a rate of 0.80 and 0.67 $\mathring{A}$/V respectively.

In Fig.5.20, the spectra measured on the Au/Si{111}-(6×6) and Au/Si{115}-(4×2) facets reveal a metallic nature of the electronic states from the I(V) characteristic. The tip was approached linearly towards the surface at a rate of 0.80 and 0.67 $\mathring{A}$/V respectively. Measurements of the differential conductance clearly show the existence of several bands of electronic states in the energy region around 0 V and extending up to 1 eV, which corresponds to the band gap of Si. For states lying below the Fermi level (0 V), such results is consistent with the formation of several bands of filled surface states that were probed by angle-resolved photoelectron spectroscopy for the bulk Au/Si(111)-(6×6) [172] and yielded, in the case of

the highest band, a metallic character when the order of this phase was not perfect [173]. In the case of Au/Si{115}-(4×2) facets, the stripes clearly correspond to atomic chains. Ideal atomic chains are known to exhibit Peierls instability with the opening of an energy gap at low temperature. However, as the electronic wave functions decay exponentially away from the atomic chains, the electronic coupling between the chain or with the substrate can be strong enough to give a residual two-dimensional character, leaving the surface metallic, as recently found for other similar systems at low temperatures [174, 175, 176].

In summery, both facets of nanowire are found to be metallic, in contrast to the expected semiconductor nature of the nanowire core. While UHV conditions preserve the metallicity of the facets, the facet reconstructions are very much likely to be disrupted in air, when an oxide layer forms. Rather than improving the nanowire conduction, Au atoms could then act as trapping centers for free carriers and disturb the electrical properties of nanowires.

5.3.2 Transport measurements of boron-doped <111>-oriented Si nanowires

In this part of work, we fabricated Si nanowire-based field-effect transistor (FET) in order to study the electrical properties of Si nanowires, more specifically the boron-doped <111>-oriented Si nanowires grown at low silane partial pressure and high temperature.

5.3.2.1 Connection of a single Si nanowire

Si nanowires were grown in the presence of silane and diborane gases with a ratio of B/Si: 8.3×10^{-3} until they reached a desired length, for example 10 μm. Next, the nanowire-based FETs were fabricated in the cleanroom of IEMN. The fabrication processes are shown in Fig.5.21 and the experimental details are briefly described in the following:

(a) Oxidation on Si substrate

A heavily doped p+ (0.01 Ohm.cm) Si substrate was used to act as global back gate and 300 nm thick dry oxide was then grown on the Si surface using LPCVD as the gate dielectric.

(b) Formation of the connecting electrodes and alignment marks

Prior to transfer the nanowires onto the surface, the alignment marks (Ti/Au: 5/20 nm, which will be used to locate the position of the deposited nanowire), and the connecting electrodes (Ti/Au: 20/200 nm, which will used to put the tungsten tips for the electrical measurement) were defined using a standard photolithography, metal deposition and lift-off procedure.

(c) Si nanowire deposition and localization

The boron-doped Si nanowires were suspended into isopropyl alcohol (IPA) by sonication from the nanowire growth substrate. A few drops of the suspension were

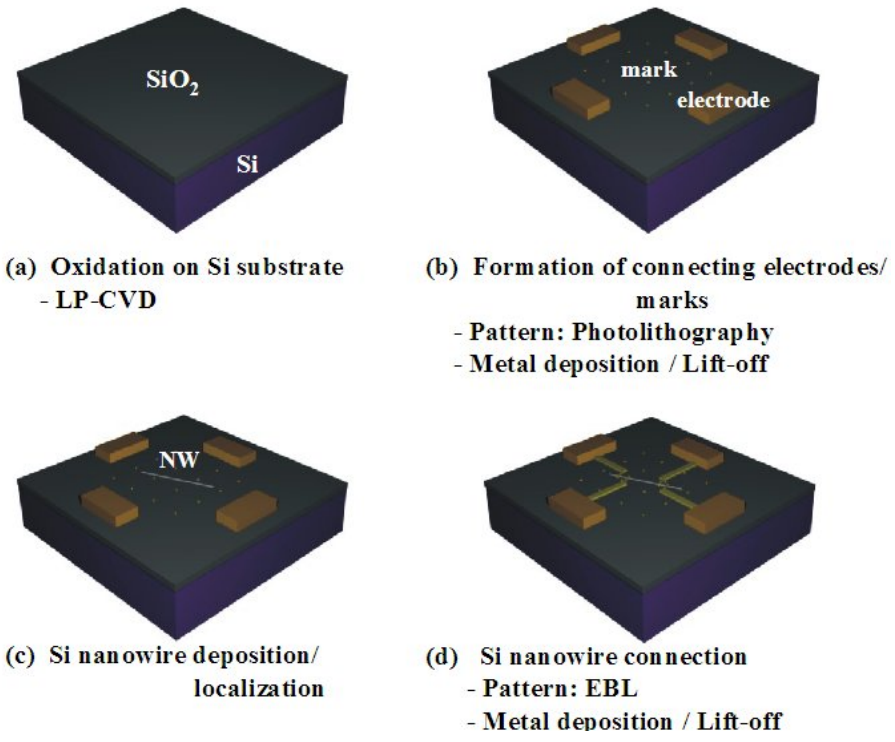

Figure 5.21: Principle of the connection of a Si nanowire

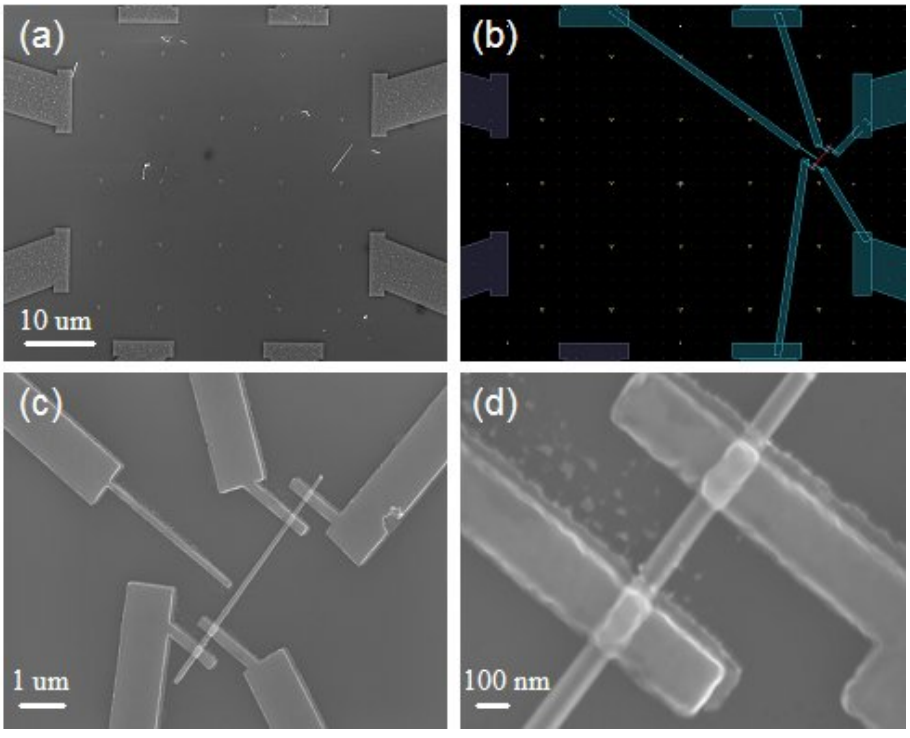

Figure 5.22: Connection of a Si nanowire: (a) Deposition of a nanowire; (b) Pattern design; (c) Connection of a nanowire; (d) Zoom of the metal/nanowire connection.

spun onto the Si substrate with the electrodes and marks, then the nanowires were dispersing on the surface using spin coater in order to get the nanowires into the marked area. For example, Fig.5.22(a) shows a nanowire deposited on the substrate in the marked area. The nanowire of interest was then located with respect to the alignment marks under the SEM. Next, the location information was used to define an electrode pattern (set of four electrodes and a lateral gate in this experiment) on the nanowire using electron beam lithography (EBL). The designed pattern is shown in Fig.5.22(b).

(d) Si nanowire connection

- Bi-layer resist deposition:

  A bi-layer resist process was used to obtain a cap profile of resist which would favor the lift-off process in the next step. Two positive resists: COPO 13% and PMMA (polymethyl methacrylate) 495k were spin coated on the oxide surface having nanowires on it. The protocol used in our experiments is:

  - Resist spin-coating of COPO 13%:

    - Speed: 2900 tr/min, - Acceleration : 1000 tr/min, - Time: 12s

    Thickness measured: 600 nm

  - Resist spin-coating of PMMA 495k:

    - Speed: 3400 tr/min, - Acceleration : 1000 tr/min, - Time: 12s

    Thickness measured: 60 nm

  - Annealing on hot plate at 80 °C for 1 minute

  - Baking at 170 °C for 30 minutes

- EBL exposure:

  The sample with the bi-layer resist was then exposed by the electron beam following the pattern designed in Fig.5.22(b).

- Develop:

  - Developing in MIBK/IPA (1:2) for 2 minutes

  - Soaking in IPA for 30s

- Desoxidation:

  Immediately before the metal deposition, the surface native oxide on the exposed segments of the nanowires was removed in a BHF solution (comprises a 6:1 volume ratio of 40% NH_4F in water to 49% HF in water) for 5s, leaving the nanowire surface hydrogen terminated prior to metal deposition.

- Metal deposition:

  Metal of Ti/Au (100 nm/200 nm) were deposited in the electron-beam evaporation system as the connecting electrodes, because Ti was found to have the lowest contact resistance compared to Cr, Al and Au.

- Lift off:

  Soaking in acetone for 30 minutes.

The connection of a Si nanowire is shown in Fig.5.22(c) with four electrodes and a lateral gate. The larger metal pads are used for probing the charge transport in the nanowires on a standard probe station. Fig.5.22(d) shows a zoom of the metal/nanowire connection, confirming the good contact of nanowire and the connecting electrodes.

5.3.2.2 I-V measurements

Two-point or four-point current-voltage measurements were carried out in the glove box under a nitrogen gas ambient atmosphere (see chapter 2) to minimize the deleterious effects of adsorbed moisture on the nanowire surface. Measurement were taken with a Cascade Microchamber probe station and HP semiconductor analyzer 4156B at room temperature. From the apparent 2-point measurement, the measured resistance is the sum of contact and nanowire resistances. Therefore, the identification of the resistance of wire itself requires 4-point measurement. We used an electrometer with > 100 TΩ input impedance to measure the voltage drop across the inner electrodes 2 and 3 (V_{23}). Current flowing through the outer electrodes 1 to 4 (I_{14}) is measured by a picoammeter. Since negligible current flows through the electrometer, V_{23} is thus the correct potential drop in the nanowire. The resistance of nanowire can be calculated by $R_{nw} = V_{23}/I_{14}$.

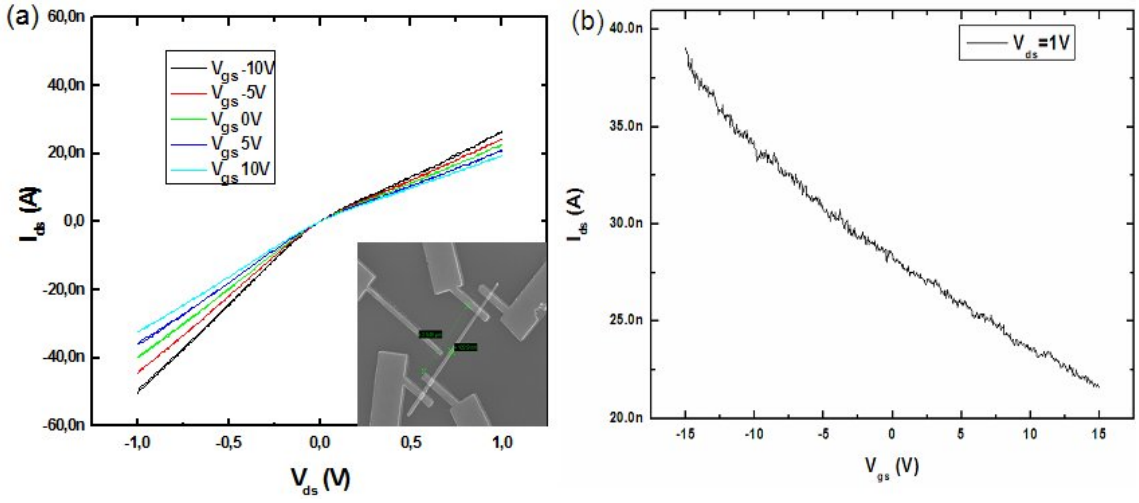

Figure 5.23: (a) SEM image of a connected boron-doped Si nanowire. (b) Four-point I-V measurement of this nanowire. (c) I_{ds} vs V_{ds} curves recorded at different gate voltage (V_{gs}). (d) I_{ds} vs V_{gs} curves recorded at $V_{ds} = 1$ V.

Fig.5.23 shows the I-V measurements on a boron-doped <111>-oriented Si nanowire with a doping level equivalent to the ratio of gas flow of B/Si: 8×10^{-3}. The inset of Fig.5.23(a) is the SEM image of a connected nanowire with a distance of the inner electrodes L = 2.5 μm and a nanowire diameter D = 100 nm, while the four-point measurement of this nanowire gives the resistance of nanowire $R_{nw} = 60$ MΩ. The resistivity of the nanowire can thus be deduced: $\rho_{nw} = \frac{R_{nw}\pi(D/2)^2}{L} = 18.85$ Ω.cm.

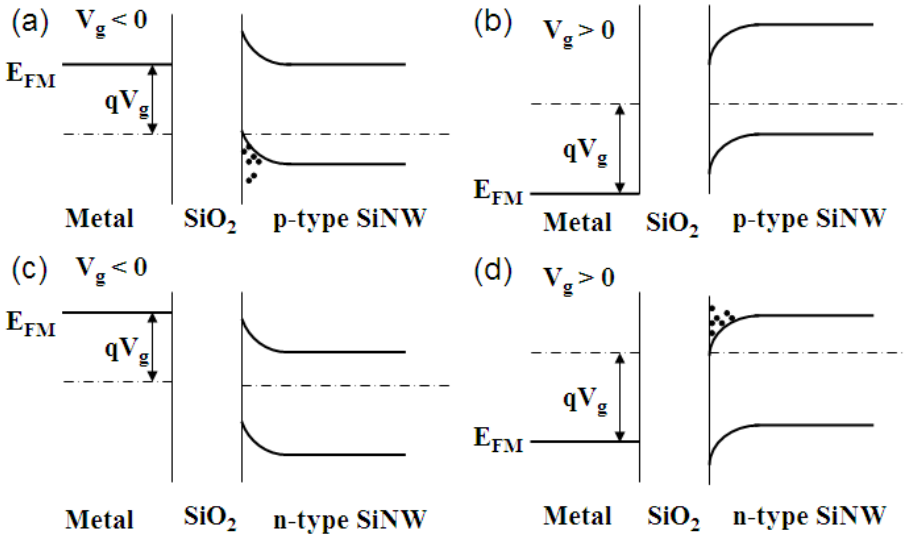

Figure 5.24: Energy band diagrams for (a) n-type Si nanowire (b) p-type Si nanowire devices. The diagrams show schematically the effect of V_{gs} on the electrostatic potential for both types of nanowires.

Output characteristics (I_{ds} - V_{ds} vs V_{gs}) of nanowire are plotted in Fig.5.23(a). The gate-dependent conductance measured using the back-gated test structure is dominated primarily by the modulation of the Schottky barrier formed between the S/D contacts and the Si nanowire, which is strongly dependent on the carrier type (p- or n-type) and the doping level of Si nanowire. The observed gate dependence can be understood by referring to the schematics shown in Fig.5.24, which show the effect of the electrostatic potential on the Si nanowire band. In these diagrams, a p-type nanowire (a,b) and a n-type nanowire (c,d) are contacted at both ends to metal electrodes. The modulations are performed through the back gate. The Si nanowire bands bend (up for $V_{gs} < 0$; down for $V_{gs} > 0$) to bring the nanowire Fermi level in line with that of the gate contact. When $V_{gs} > 0$, the bands are lowered, which depletes the holes in p-type Si nanowires and suppresses conductivity, but leads to an accumulation of electrons in n-type Si nanowires and enhances the conductivity. Conversely, $V_{gs} < 0$ will raise the bands and increase the conductivity of p-type Si nanowires and decrease that of the n-type. Indeed, Fig.5.23(b) shows clearly a decrease of I_{ds} when V_{gs} is increased, indicating that the doping type of this Si nanowire is p-type.

In addition, it is possible to estimate the mobility of carriers from the transconductance [177], $dI_{ds}/dV_{gs} = \mu\ (C/L^2)V_{ds}$, where μ is the carrier mobility, C is the capacitance, and L is the measured length of the Si nanowire. The nanowire capacitance is given by $C \approx 2\pi\epsilon\epsilon_0 L/\ln(4h/D)$, where ϵ is the dielectric constant, h is the thickness of the SiO_2 layer, and D is the diameter of nanowire. Therefore, the slope of dI_{ds}/dV_{gs} (4.8×10^{-10}) yields the mobility of the boron-doped Si nanowire of 0.16 $cm^2/V.s$.

In the previous APT analysis, it has been revealed that the concentration of boron dopants in the nanowire is more than 10^{20} B/cm^3, whereas the measured transport values of these nanowires are largely lower than that we have estimated.

Two explanations can be given: Firstly, the presence of Au on the nanowire sidewalls or even in the volume of nanowire, can make deep centers that trap the carriers. Secondly, it is possible that the boron impurities incorporated in the nanowires during growth are not all active. Therefore, in the next part, we tried to overcome these difficulties to improve the electrical properties of Si nanowires.

5.3.3 Improvements of the electrical properties of Si nanowires

It has been shown in the previous TEM analysis that the Au diffusion during nanowire growth can be controlled by using relatively high silane partial pressures and low temperatures. Furthermore, the growth temperature has been found to have an important influence on the doping effect, as it is shown in chapter 4: at 550°C, boron can be well incorporated during growth, while the addition of PH_3 does not change the nanowire morphology at 430°C. As a result, we decided to use a higher silane partial pressure to avoid Au diffusion and a temperature at 500°C to well incorporate both n- and p- types dopants. The growth parameters are shown in Tab.5.1:

P_{SiH_4} (mbar)	P_{tot} (mbar)	T (°C)	B:Si	P:Si	growth time (min)
0.65	10	500	5.10^{-4}		20
0.65	10	500		$2.5\ 10^{-4}$	20

Table 5.1: Improved CVD doping growth parameters

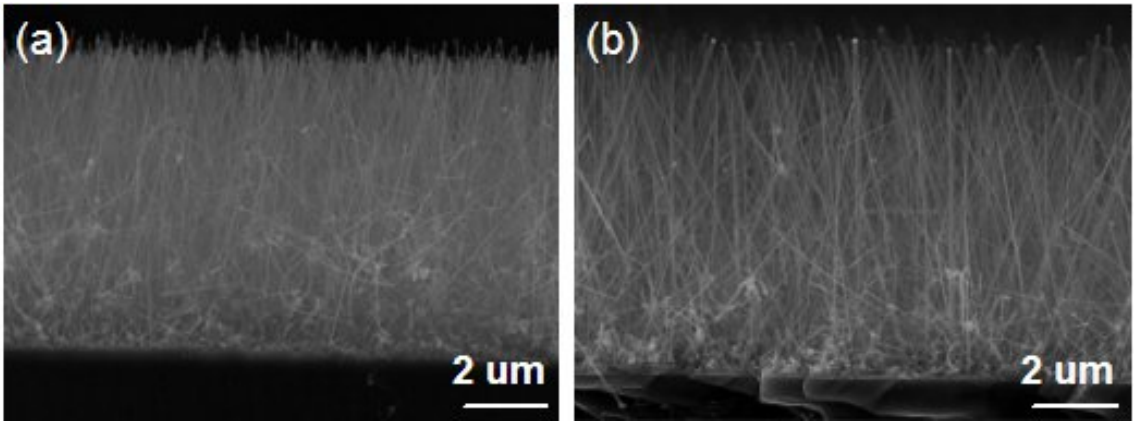

Figure 5.25: (a) N-type Si nanowires; (b) P-type Si nanowires.

Fig.5.25(a) shows the n-type Si nanowire growth using the above parameters, while Fig.5.25(b) shows the p-type Si nanowires. The addition of dopants is found to have no influence on the nanowire morphology: the shape of nanowires is straight and no facets were observed on their sidewalls, even though the control of the <111> growth direction was lost because of the high silane partial pressure. These nanowires were then transferred and connected using the technique developed in the last section, and their electrical properties were measured, as it is shown in Fig.5.26 and 5.27.

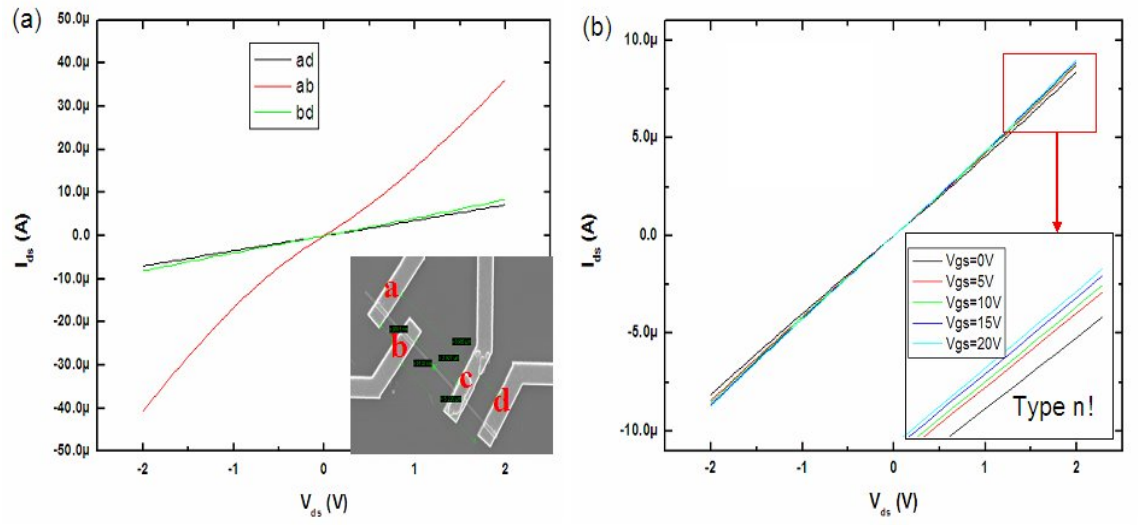

Figure 5.26: (a) SEM image of a connected phosphor-doped Si nanowire. (b) Two-point I-V measurements of the different parts of this nanowire. (c) I_{ds} vs V_{ds} curves recorded at different gate voltage (V_{gs}). (d) I_{ds} vs V_{gs} curves recorded at V_{ds} = 1 V.

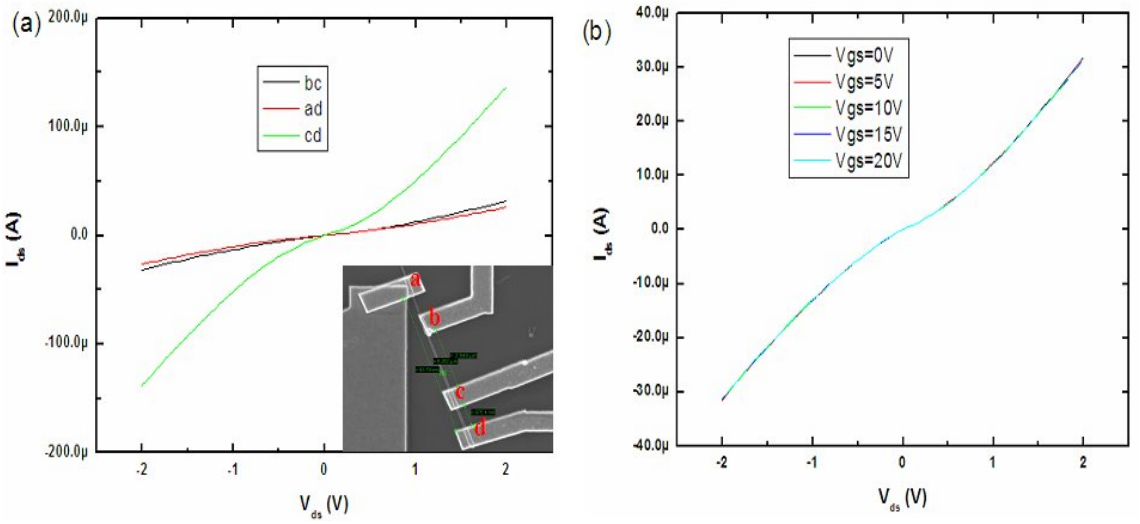

Figure 5.27: (a) SEM image of a connected boron-doped Si nanowire. (b) Two-point I-V measurements of the different parts of this nanowire. (c) I_{ds} vs V_{ds} curves recorded at different gate voltage (V_{gs}). (d) I_{ds} vs V_{gs} curves recorded at V_{ds} = 1 V.

- N-type Si nanowires: An example of a connected nanowire is shown in the inset SEM image of Fig.5.26(a). 2-point measurements were performed on the different parts of the nanowire to calculate the contact resistance R_c and the resistivity of nanowire ρ_{nw}. The total resistances of the segments ab and ad can be calculated from the I(V) curves in Fig.5.26(a), giving R_{ab} = 52 kΩ and R_{ad} and 280 kΩ, respectively, while the lengths of measured wire are L_{ab}: 0.94 μm and L_{ab}: 0.94 μm. Using these measured values and the following equations, R_c and ρ_{nw} are obtained as 8.3 kΩ and 0.024 Ω.cm, respectively.

$$\begin{aligned} 2R_c + R_{abnw} &= R_{ab} \\ 2R_c + R_{adnw} &= R_{ad} \\ \frac{R_{abnw}}{R_{adnw}} &= \frac{L_{ab}}{L_{ad}} \end{aligned} \tag{5.3}$$

  The gate dependent I_{ds}-V_{ds} curves are shown in Fig.5.26(b), in which no significant dependence is observed, indicating that nanowire is heavily doped. A deeper insight into this graph shows that I_{ds} slightly increases with the increase of V_{gs} yielding a n-type nanowire. The mobility of the carriers is then calculated from dI_{ds}/dV_{gs}, giving an electron mobility μ_n: 6.72 cm^2/V.s.

- P-type Si nanowire: Similar measurements were performed on a p-type Si nanowire, as it is shown in Fig.5.27. The measured and calculated results are shown in Tab.5.2. The nanowire is found to be also heavily doped and the resistivity is 0.008 Ω.cm, while the mobility is much lower than the n-type which is reasonable for the holes comparing to the electrons.

	Diameter	Length	R_c	ρ_{nw}	μ
n type	90 nm	L_{ab}:0.94 μm,L_{ad}:7 μm	8.3 KΩ	0.024 Ω.cm	6.76 cm^2/V.s
p type	94 nm	L_{cd}:0.98 μm,L_{ad}:6.4 μm	1.6 KΩ	0.008 Ω.cm	0.72 cm^2/V.s

Table 5.2: Parameters of doped Si nanowires.

	doping level	ρ	μ
n type	3.85 10^{19} cm^{-3}	0.001 Ω.cm	86.6 cm^2/V.s
p type	1.08 10^{21} cm^{-3}	0.0001 Ω.cm	45.8 cm^2/V.s

Table 5.3: Parameters of doped Si bulk.

As a result, after controlling the Au diffusion during nanowire growth, the conductivity of nanowire is found to increase significantly comparing to the <111>-oriented nanowire. For example, for the both p-type, the resistivity of nanowire with controlled Au diffusion is 2300 times lower than that of the <111>-oriented nanowire, although the number of impurities incorporated into this nanowire is expected to be 10 times lower. This improvement confirms the influence of Au on the

transport properties of Si nanowires and shows the necessity to control Au diffusion during growth.

In order to calculate the concentration of free carriers and the subsequent concentration of active dopants in the nanowires, we can use the equations as following for the approximate estimation even they maybe not very suitable in the highly doped case:

$$n = \frac{1}{e\mu_n\rho_{nw}}, p = \frac{1}{e\mu_p\rho_{nw}} \tag{5.4}$$

Using the values in Tab.5.2, the concentrations of dopants in the n- and p- types nanowires are given as 3.85×10^{19} and 1.08×10^{21} cm^{-3}. However, comparing to the bulk values for Si materials with the same doping concentrations shown in Tab.5.3, the resistivity and mobility measured in the nanowires are still much smaller. To explain this poor performance, firstly more statistics have to be obtained to confirm the electrical properties of nanowires; then there might be much more impurities incorporated into nanowires than what we have estimated, yielding to a very low mobility. It is also possible that they are not all active, so an annealing should be performed to verify this assumption.

5.4 Conclusion

In summary, a comprehensive characterization has been performed in this chapter on the Si nanowires in order to get an overall understanding of their structural, physical and electrical properties.

In the first part, we report the study of the morphology and facet structures of Si nanowires with a <111> orientation, synthesized by VLS process with low silane partial pressure reactant and Au as the catalyst by means of electron microscopy and STM. While a modification of the number of sidewalls is observed during nanowire growth, with the occurrence of alternating wide and narrow sidewalls, all the sidewalls consist of facets that are covered with Au-rich clusters. Due to the preferential adsorption of cleaved nanowires with one of their wide sidewalls in contact with a surface, the structural properties of the facets belonging to the short sidewalls are revealed with STM and confirm the formation of Au-induced facets. From these observations, the tapering of nanowires is found to be related to two contributions: the reduction of the catalyst particle size during growth and lateral growth from the direct incorporation of Si species onto the nanowire sidewalls. Because the rearrangement of atoms at surfaces and interfaces might affect the growth kinetics, the trigonal symmetry as well as the higher lateral growth rate on the wide sidewalls are explained from the existence of an interfacial atomic structure with two inequivalent parts in the unit cell.

In the second part, a limited number of vertically oriented Si nanowires are grown on top of (111)-oriented Si micropillar by controlling the density of the Au seed particles and their size. Such nanowire-on-micropillar structures allow the analysis of the chemical composition of Si nanowires at atomic scale by the femtosecond laser assisted APT. Three-dimensional images of the atom distribution in the boron-doped <111>-oriented Si nanowire, in particular, the distribution of boron impurities, are

obtained and compared to the intended impurity concentration. The presence of boron in the nanowires is thus confirmed, while it has been shown that the doping level of nanowires can be controlled by regulating the appropriate gas (such as diborane) during growth.

In the third part, the transport properties of Si nanowires are measured. Firstly, scanning tunneling spectroscopic measurements are performed on the major facets of the <111>-oriented Si nanowire sidewalls and the results reveal a metallic behaviour of nanowire surface at 77 K in UHV, which is lost when the nanowires are released in air. Then, the boron-doped <111>-oriented Si nanowires were electrically connected by using EBL technique. The gate-dependent measurements confirm that electrically active boron impurities are incorporated into nanowires. However four-point measurement reveals a resistivity of nanowires much higher than that the one expected from the APT analysis. This poor performance can be explained by the presence of Au which acts as the recombination traps, so nanowires are then grown at different conditions that can prevent the Au diffusion. The I-V measurements reveal a significant improvement of the transport properties of nanowires, even though it is not yet competitive comparing to the Si bulk.

General conclusion

The objective of this thesis was to synthesize Si nanowires using Au island-assisted VLS growth and to obtain a comprehensive understanding of their properties. After giving an overview of the one-dimensional nanostructures in Chapter 1, more specifically nanowires, from their synthesis to applications; and introducing all the experimental techniques that we have used in Chapter 2: the nanowire synthesis system, characterization tools and microfabrication techniques; three key-points of this work: Au catalyst, VLS Si nanowire localized growth, and characterizations of Si nanowires have been then intensively studied and detailed in the following.

In Chapter 3, we have studied the epitaxial growth of Au islands on Si(111) under UHV condition using MBE technique. The phase transition of Si 7×7, Au/Si 5×2 and Au/Si β-$\sqrt{3}\times\sqrt{3}$ was observed in the submonolayer regime by means of STM and LEED. Three-dimensional Au islands were then formed after the completion of a Au/Si $\sqrt{3}\times\sqrt{3}$ wetting layer following the Stranski-Krastanov layer-plus-island growth mode. The number of islands can be predicted by the rate equations studies and the island density was found to be inversely proportional to the ratio D/F (surface temperature / evaporation rate). By fitting the data related to the island size and density with Arrhenius plot, we have successfully found a range of surface temperatures, where the Au islands are prepared within the island growth regime. In this region, a very limited number of Au islands can be obtained by regulating the growth parameters. Taking advantage over the growth of Au islands is a prerequisite to control the size and distribution of Si nanowires.

In Chapter 4, we have investigated the Au-catalyzed VLS Si nanowire growth using CVD and MBE techniques. The principle goal is to obtain Si nanowires with rational properties to be able to integrate them into the devices. Because of the low output and limited length of MBE Si nanowires, we have decided to use the CVD technique. It has been found that the growth direction of nanowires depends on the partial SiH_4 pressure, more specifically, the $\langle 111 \rangle$ orientation can be obtained at low partial SiH_4 pressure. The growth rate of CVD Si nanowires is relatively rapid and their length was found to depend on the initial size of the Au catalysts. Furthermore, dopants can be incorporated into nanowires during growth, while the doping effect was found to be related to the growth parameters such as the deposition temperature and the partial SiH_4 pressure.

After controlling Si nanowire growth on a simple Si(111) substrate, combining our experiences of the controlled growth of Au islands on the Si substrate, we have succeeded to localize the Si nanowires in a controllable manner (limited density,

controlled position) onto some microstructures which were prefabricated by microfabrication processes. Since we can control the orientation of nanowires in the ⟨111⟩ direction, they can thus be localized vertically or horizontally on the Si micropillars with (111) top faces or between the Si microtrenches with (111) vertical faces.

In Chapter 5, an overall characterization was performed on the Si nanowires in order to get a deep insight of their structural, physical and electrical properties. Three kinds of analysis were performed:

- Surface analysis: By combining SEM, TEM and STM observations of the <111>-oriented Si nanowires grown at low partial SiH_4 pressure, we have found that the nanowire surface is covered by Au clusters due to the Au diffusion during nanowire growth and the atomic structures of the facets on the nanowire sidewalls are also induced by Au. Then, in addition to the tapering effect attributed to the reduction of the Au particle size during growth because of Au diffusion, lateral overgrowth has been demonstrated. Finally, we have demonstrated that the shape of the nanowire cross-section is dependent on the surface reconstruction that is induced by Au and requires an unit cell with two inequivalent parts.

- Volume analysis: The chemical composition of boron-doped <111>-oriented Si nanowires at atomic scale was revealed by APT. The presence of boron in the nanowires has been confirmed by mass spectrum, while the atomically resolved three-dimensional reconstruction of the nanowire indicated an uniform distribution of boron impurities and the impurity concentration agreed well with the ratio of the flow rate between B_2H_6 and SiH_4.

- Electrical analysis: A metallic behaviour of the nanowire surface has been revealed at 77 K in UHV by using STS measurements. Then, the boron-doped <111>-oriented Si nanowires were electrically connected by using EBL technique. The gate-dependent measurements confirm that electrically active boron impurities are incorporated into nanowires. However the presence of Au on the surface or even in the volume of nanowires can lead to a very poor electrical performance of this kind of nanowires. As a result, the growth parameters have then been changed to avoid the Au diffusion along the nanowires. Their electrical characterization have revealed a significant improvement of their transport properties.

As it is described above, a rather comprehensive understanding of Si nanowire growth and their properties has been obtained during this thesis, the next step will be to move beyond fundamental science, towards applications of nanowires in functional devices. A variety of prototypical components have been demonstrated, as shown in Chapter 1. However, extensive processing and development will be required to make such applications profitable. This leaves much to be done from a material science perspective and more efforts are still needed: for example, even the controlled <111> orientation of Si nanowires favors their integration into devices, it has been shown in this work that Au can diffuse on the nanowire sidewalls, leading

to a poor electrical performance of nanoiwres. In order to overcome this problem and also try to maintain the <111> orientation of nanowires, specific gas such as HCl can be used since this gas can play an etching role during growth. Another possibility is to find another particle material to replace Au so that no foreign atoms diffuse in the particle, or the growth rate is enhanced without the creation of defects. Moreover, after controlling the Au diffusion during nanowire growth and improving their transport properties, it is very interesting to study the surface structure of this type of Si nanowires, and also the physical origin of their morphology, like that we have done with the <111>-oriented Si nanowires. Anyway, a more consistent and predictive work on the Si nanowires is still needed and will allow a more efficient realization of device requirements in the future.

List of publications

- Growth of Si nanowires on micropillars for the study of their dopant distribution by atom probe tomography
  T. Xu, J. P. Nys, B. Grandidier, D. Stiévenard, Y. Coffinier, R. Boukherroub, R. Larde,E. Cadel, P. Pareige
  J. Vac. Sci. Technol. B, 26(6), (2008)

- Gibbs-Thomson and diffusion-induced contributions to the growth rate of Si, InP, and GaAs nanowires
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- Faceted sidewalls of silicon nanowires: Au-induced structural reconstructions and electronic properties
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- Study of the effect of gas pressure and catalyst droplets number density on silicon nanowire growth
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Communications

- Localized growth and characterization of Si nanowires
  T. Xu, J. P. Nys, B. Grandidier, D. Stiévenard
  Poster session in Summer school on semiconductor nanowires (3SN08), 15-20 June 2008, Roscoff, France

- Localized growth and characterization of Si nanowires
  T. Xu, J. P. Nys, B. Grandidier, D. Stiévenard
  Oral presentation in 9th International Workshop on Beam Injection Assessment of Microstructures in Semiconductors (BIAMS), 29 June - 3 July 2008, Toledo, Spain.

- Elaboration de nanofils de silicium pour caractérisation en sonde atomique et microscopie champ proche
  T. Xu, J. P. Nys, B. Grandidier, D. Stiévenard, R. Larde, E. Cadel, P. Pareige
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- Atomic scale structure of Si nanowire
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- Atomic scale structure of <111>-oriented Si nanowire
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