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par

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Potentialités de la technologie CMOS 65nm SOI pour des applications sans fils en bande millimétrique

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Introduction

According to the *Figure 1*, the millimeter wave band is defined as the frequency band covering 30 to 300 GHz which means a wavelength between 1 and 10 mm. There are many advantages associated with increasing the operating frequency for already developed applications. They include the potential for increased available bandwidth and the directivity which can be obtained for a given antenna aperture. This implies smaller size systems offering increased transmission capacity in the case of communication systems or improved resolution for radar or imaging systems. In the latter case, millimeter wave systems are used to achieve useful resolution for image recognition, or identify explosive materials by their spectroscopic signatures [1].

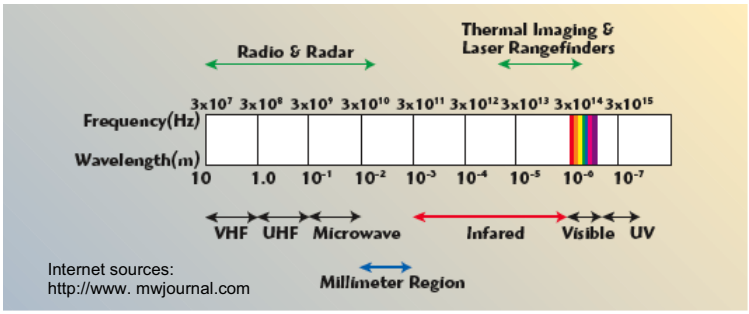
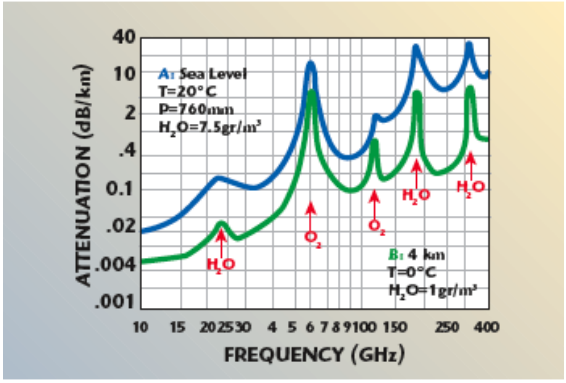


Figure 1. *Millimeter-wave region of the electromagnetic spectrum [2]*

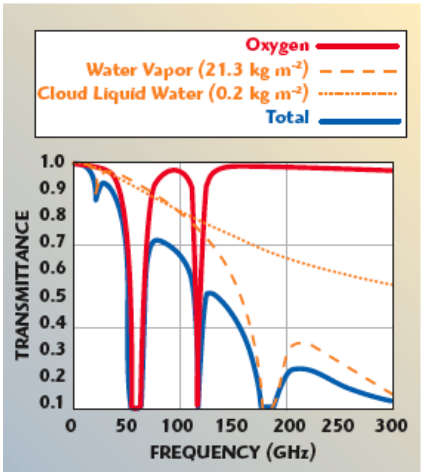
Additionally, there are unique features associated with the transmission properties of the atmosphere in the millimeter spectrum region. *Figure 2* shows the effective zenith atmospheric transmission in dB/km for typical conditions at sea level and at an altitude of 4 km. The impact of the 60 and 120GHz O_2 lines and multiple resonances of the H_2O molecule can be seen. The high attenuation of the 60GHz O_2 allows high density unlicensed communication and covert systems.



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Figure 2. *Atmospheric attenuation within the millimeter-wave spectrum*

The window frequencies are better illustrated in *Figure 3*, which shows linear transmission at zenith with the contributions due to atmospheric gases and liquid water for a mid-latitude location.



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Figure 3. Atmospheric transmission in the 30 to 300 GHz region.

The 50 to 60 GHz band may be used at shorter ranges for high data rate communications (0.5 to 5… 10Gb/s) such as wireless uncompressed HD-video streaming (W-HDMI) and ultra fast file transfers (USB2.0, …). The available unlicensed band extends from 57GHz to 66GHz depending on the geographic region (*Figure 4*). Four organizations drive the 60-GHz radios standardization. Among them, there are the IEEE standard body [1], [3] and the WiMedia alliance which is an industrial association [4]. The IEEE 802.15.3 Task Group 3c (IEEE 802.15.3c) is developing a millimeter wave based alternative physical layer (PHY) for the existing 802.15.3 WPAN Standard IEEE-Std-802.15.3-2003. With merging of former multi-band OFDM alliance (MBOA), the WiMedia alliance is pushing a 60GHz WPAN industrial standard, likely based on orthogonal frequency division multiplexing (OFDM) technology. The shooting data rate is 2 Gb/s or higher. Among a large number of proposals, the majority of them can be categorized to either multi-carrier (meaning OFDM) or single-carrier types, where the former one is expected to support extremely high data rates (10 Gb/s).

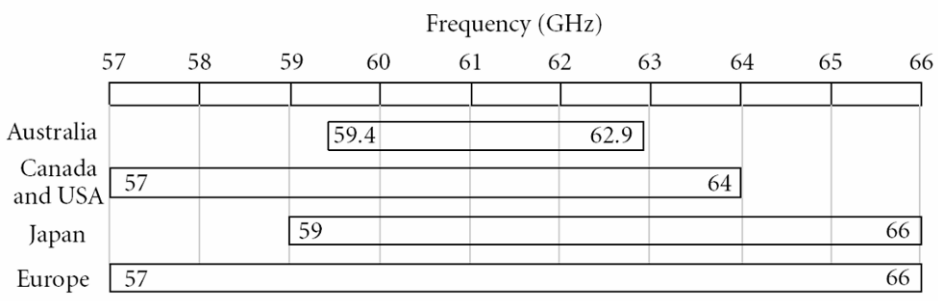


Figure 4. Unlicensed band going from 57 to 66GHz

The second targeted application is automotive. Adaptive cruise control systems using 24GHz and 77GHz frequency bands sensors are now a reality. Initially based on Gunn diode technologies, it is becoming one of the main application areas for GaAs MMICs and a potential market for lower cost (Bi)CMOS/SOI[1] CMOS. These sensors are marketed as autonomous cruise control (ACC) radars. The last potential applications are the mm-wave imaging systems for medical and security applications. These topics have been the subject of intensive recent developments, responding to the security needs of airports and other establishments. In the middle 80s companies such as *Millitech* or *TRW* (now *NGST10*) had been prototyping millimeter wave cameras. Today, the targeted frequency bands for such applications are at 94GHz and above 100GHz.

The present thesis evaluates the 65nm CMOS SOI for millimeter wave design, in order to address the above applications. This work is built on four chapters which are decomposed as follows:

Chapter I reviews the SOI technology. After presenting the major industrial groups working on SOI, it highlights the major benefits of the SOI-MOSFETs in comparison with bulk transistors. Partially Depleted and Fully Depleted SOI transistors are also discussed.

Chapters II and *III* treat about the active and passives elements in CMOS SOI. Several figures of merit are introduced. The characterization and modeling methodologies developed in this thesis work are presented and discussed. The performances of the CMOS SOI and bulk 65nm technology are compared with the state of the art.

Chapter IV introduces and develops CMOS integrated millimeter wave receiver requirements. Special focus is put on LNAs and Mixers in 65nm CMOS node on bulk and SOI substrate. A robust industrial millimeter wave CMOS design methodology developed during this thesis is presented. Finally, LNA and mixer simulations and measurements for millimeter wave systems (77GHz and 60GHz) are presented and a comparison between CMOS bulk and SOI for these target frequencies is examined.

The *conclusion* summarizes the major contributions of this thesis and suggests topics which merit further work.

[1] SOI: Silicon On Insulator

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[1] A. Cathelin, et al., "Design for Millimeter-wave Applications in Silicon Technologies", *ESSCIRC2007*, Munich, Sept. 2007.

[2] http://www.mwjournal.com

[3] IEEE 802.15 Working Group for WPAN, http://www.ieee802.org/15/.

[4] WiMedia alliance, http://www.wimedia.org/.

Chapter I

The CMOS Silicon On Insulator Technology

In this chapter, we present the Silicon on insulator technology (SOI) which refers to the use of a layered silicon-insulator-silicon substrate in place of conventional silicon substrates in semiconductor manufacturing. The SOI technology is already in use in the industry, for example in *AMD's* 130 nm, 90 nm and 65 nm single, dual and quad core processors since 2001. *Freescale* has also adopted SOI in its PowerPC 7455 CPU in late 2001; currently Freescale is shipping SOI products in their 180nm, 130nm, 90nm and 65nm lines. *IBM* began to use SOI in *PowerPC G4 7455* chips since late 2000. The 90 nm PowerPC-based processors used in the *Xbox 360*, *PlayStation 3* and *Wii* use SOI technology as well. On the foundry side, *Chartered Semiconductor* devoted a whole fab to SOI.



Figure I.1. SOI users with new factories or high production based on SOI 300 mm wafers

Recently, a group of companies have launched a silicon-on-insulator (SOI) consortium that is aimed at accelerating the technology in the marketplace [1].

The SOI Industry Consortium will also promote the benefits of SOI technology in the market. The founding membership in the group includes the following: *AMD*, *ARM*, *Cadence*

Design Systems, CEA-Leti, Chartered Semiconductor Manufacturing, Freescale Semiconductor, IBM, Innovative Silicon, KLA-Tencor, Lam Research, NXP, Samsung, Semico, Soitec, SEH Europe, STMicroelectronics, Synopsys, TSMC and UMC.

I.1. The SOI Substrate

SOI-based devices differ from conventional silicon-built devices in that the silicon junction is above an electrical insulator, typically silicon dioxide. The choice of the insulator depends largely on intended application, with sapphire being used for radiation-sensitive applications and silicon oxide preferred for improved performance and diminished short channel effects in microelectronics devices. From a manufacturing perspective, SOI substrates are compatible with most of the conventional fab processes. In general, an SOI-based process may be implemented without special equipment or significant retooling of an existing process. The primary barrier to SOI implementation is the increase in substrate cost, which contributes an estimated 10 - 15% increase to total manufacturing costs.

Many techniques have been developed for producing a film of single-crystal silicon on top of the insulator. Some of them are based on the epitaxial growth of silicon on either a silicon wafer covered with an insulator (homo-epitaxial techniques) or on a crystalline insulator (hetroepitaxial techniques). Other techniques are based on recrystallization of thin silicon layer from the melt (laser recrystallization, e-beam recrystallization and zone-melting recrystallization). Silicon-on-insulator can also be produced from a bulk silicon wafer by isolating a thin silicon layer from the substrate through the formation and oxidation of porous silicon (FIPOS) or through the ion beam synthesis of a buried insulator layer (SIMOX[1], SIMNI and SIMON). Finally, SOI material can be obtained by thinning a silicon wafer bonded to an insulator and mechanical substrate (wafer bonding BESOI). Every approach has its advantages and its drawbacks, and the type of application to which the SOI materials is destined dictates the material to be used in each particular case. SIMOX and UNIBOND[2] seem to be the ideal candidates for VLSI CMOS application, while wafer bonding is more adapted to bipolar and power applications.

In the last decade, the dominant SOI technology was SIMOX, which is synthesized by internal oxidation during the deep implantation of oxygen ions into a silicon wafer. Annealing at high temperature restores the crystalline quality of the film. SIMOX wafers

[1] Silicon Implanted Oxide
[2] Trade name for SOI wafers using Smart Cut process

have good thickness uniformity, low defect density, sharp Si–SiO_2 interface, robust BOX[3], and high carrier mobility.

Wafer bonding and etch back is another mature SOI technology. An oxidized silicon wafer is bonded to a second silicon wafer. When two flat, hydrophilic surfaces such as oxidized surfaces are placed against one another, bonding naturally occurs, even at room temperature, which forms the hydrogen bonds across the gap between two surfaces. After bonding, upper wafer is thinned down from 600µm to few microns to reach the target thickness of the silicon film. The thinning is usually done grinding followed by chemical polishing followed by etch-back process.

Unlike the wafer bonding method, in UNIBOND, the etch-back process is avoided. The Smart-Cut mechanism uses the deep implantation of hydrogen (*Figure I.2*) to generate microcavities [2]. After bonding and annealing, the wafers separate naturally at a depth defined by the location of hydrogen microcavities. The UNIBOND wafer is finished by CMP[4]. The smart-cut approach has several advantages:

- No etch-back step, with much better uniformity of surface (0.15nm).
- The prime-quality wafer is fully recyclable and UNIBOND reduces to a single wafer process, only conventional equipment is needed for mass production.
- Unlimited combinations of BOX and film thicknesses can be achieved in order to match most device configurations (ultra-thin CMOS or thick-film power transistors and sensors).

The following figure presents the Smart Cut process [2]:

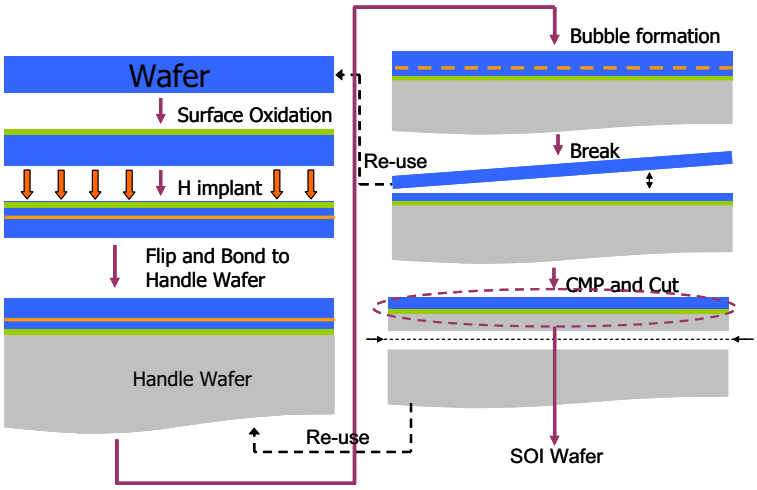


Figure I.2. Smart Cut process

UNIBOND wafers using Smart Cut process are currently used for the CMOS SOI 65nm process.

[3] BOX : Buried Oxide
[4] Chemical Mechanical Polishing

I.2. MOSFET transistor on bulk and SOI

The implementation of SOI technology is one of several manufacturing strategies employed to allow the continued miniaturization of microelectronic devices, commonly referred to the Moore's Law.

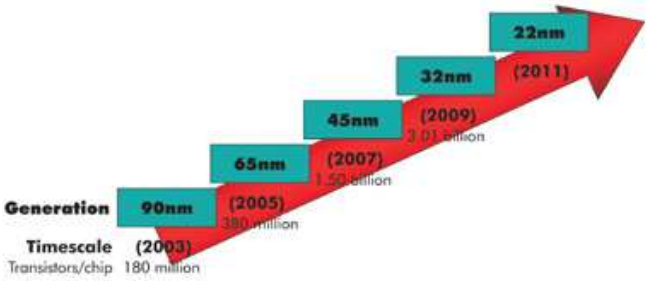


Figure I.3. MOS transistors ITRS roadmap

As CMOS devices scale down a lot of issues appear:

- As L is reduced, drain-to-channel capacitance increases.
- Therefore, gate-to-channel capacitance must also be raised, that is oxide must be thinner.
- Also V_{TH} needs to be reduced along with V_{DD}.

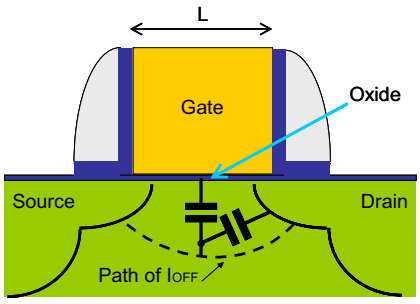


Figure I.4. Schematic cross section of a MOS transistor

Those issues imply new challenges:

- SiO_2 is too leaky bellow 1.2nm
- A thin oxide cannot control a current path far from the gate

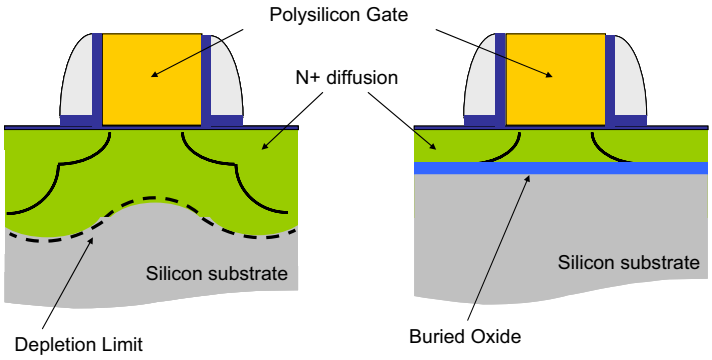
The performances of bulk devices and circuits will not be able to follow the Moore's Law owing to the complexity of problems to be solved. But, as it has been shown, the use of SOI can help to increase the performances in term of figure of merit (f_T and f_{max}) [3], [20], [22], [23] and [24]. SOI technology has been demonstrated to be an alternative technology to

mainstream bulk silicon for the realization of high-speed, low-power digital [4] and analog CMOS circuits [5], as well as niche applications such as antenna switches [19], [30], [31], extreme high temperature [6] or radiation conditions.

I.2.1. Comparison between bulk and SOI MOSFET

The main differences between bulk and SOI transistors are:

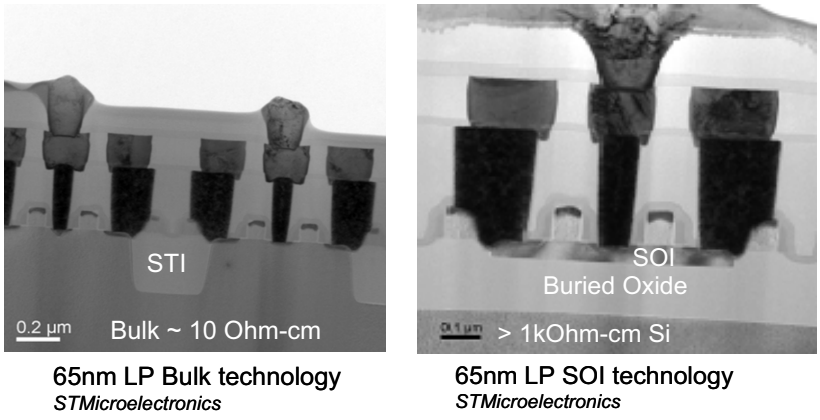
- Bulk MOSFETs are built at the top of the surface of a monocristalline silicon wafer (*Figure I.5 – a*)
- In SOI, the top active silicon region is separated from the under-laying mechanical substrate by a thick insulator layer called buried oxide (*Figure I.5 - b*)
- The SOI mechanical substrate may as well be high resistivity or low resistivity.



a) *b)*

Figure I.5. Cross section of bulk (a) and SOI MOSFET (b)

The following cross section structure illustrates how in SOI technology the buried oxide insulates the active silicon area with respect to the substrate:



a) *b)*

Figure I.6. Cross section photograph of bulk (a) and SOI MOSFET (b) of the 65nm LP technology

I.2.1.a. Benefits of the SOI technology

Concerning the active devices, reported benefits of SOI technology relative to conventional silicon (bulk CMOS) processes include lower parasitic capacitances, no latch-up in small devices, a short channel effects reduction, a better inverse subthreshold slope and a better density integration.

I.2.1.a.i Lower parasitic capacitances

Due to isolation from the bulk silicon, smaller parasitic capacitances are observed in SOI, in this way the power consumption is improved for a given performance. In bulk devices, doping level in submicron technologies increases the parasitic source and drain to substrate capacitances. In SOI, capacitance between junctions is fixed by the thickness of the BOX. Since the relative permittivity of the oxide (~4.5) is smaller than the silicon one (~11.7) the junction capacitance in SOI is always smaller than in bulk.

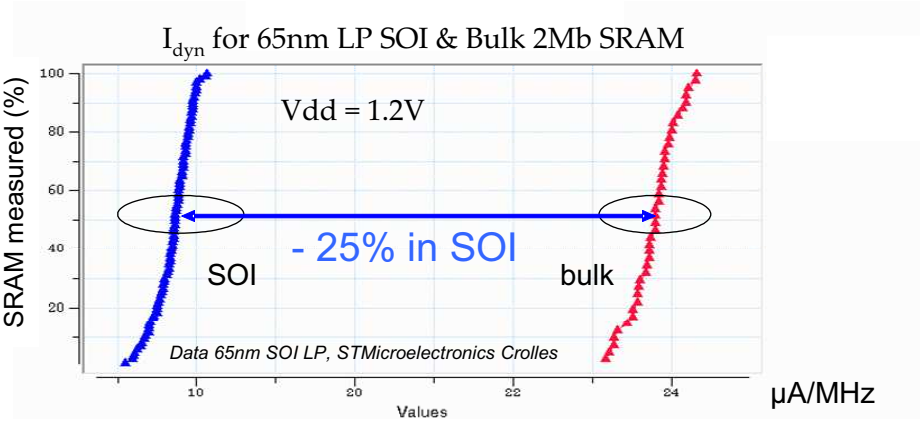


Figure I.7. Dynamic power consumption in CMOS 65nm SOI and bulk at same frequency

For digital devices, thanks to parasitic capacitances reduction, SOI offers 25% less dynamic power than bulk for the same operating frequency (cf. Figure I.7) and 40% higher maximum speed with respect to a bulk implementation, at constant power consumption [10].

I.2.1.a.ii No latch-up effect

Another benefit reported in SOI is the resistance to latch-up due to complete isolation of the N- and P- well structures. This parasitic effect consists in the activation of the PNPN structure formed by two parasitic bipolar transistors (NPN and PNP) which are in the bulk structure. In a CMOS inverter this effect can short circuit V_{dd} and GND. This can result in a self-destruction or a malfunction of a circuit. The *Figure I.8* illustrates the parasitic bipolar transistors formed between N and P MOS transistors [12].

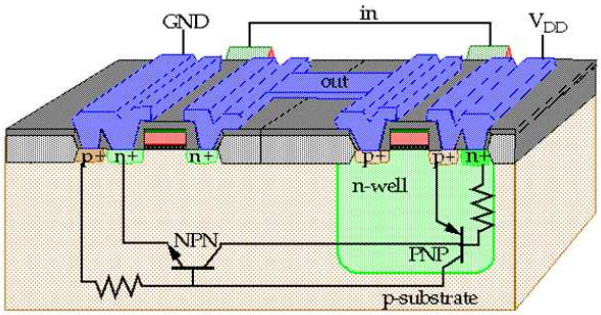


Figure I.8. Parasitic bipolar transistors formed between n and p MOS transistors

I.2.1.a.iii Short channel effect reduction

A MOSFET device is considered to be short when the channel length is in the same order of magnitude as the depletion-layer widths of the source and drain junction. As the channel length is reduced to increase both the operation speed and the number of components per chip, the short-channel effects arise. The short channel effects are associated to the loss of control of the channel by the gate. In the case of Fully Depleted[5] SOI MOSFET, the space charge in the thin silicon film is well controlled by the gate. Thus, the short channel effects are reduced in comparison with bulk MOSFET.

I.2.1.a.iv Inverse subthreshold slope

In FD SOI MOSFET the I_d-V_G characteristics exhibit a small subthreshold swing close to the ideal value of 60mV/decade [13]. This is because, thanks to the thin SOI layer and the thick buried oxide, the depletion capacitance in the channel region is too small to affect the surface potential. This allows the threshold voltage to be reduced without any increase in the leakage current, thereby making operation at ultra low voltage possible.

I.2.1.a.v Integration density and power consumption

Since SOI MOSFET do not have a well or a fourth body terminal[6], as bulk devices do, the isolation for n- and p- MOSFETs is smaller and the layout occupies about 30% less area than that of bulk devices. The small layout area implies a small output load capacitance, which helps to maintain the current drivability at ultra low supply voltages. This means that the threshold voltage does not have to be reduced excessively, which helps suppress the leakage current. The density integration is also improved in RF design, especially for inductor (*Chapter III.I.4.a*). Inductors made with HR[7] SOI occupy 40 % lower area for a given Q factor in comparison with bulk ones [32].

[5] FD in literature
[6] Except for body contacted SOI MOSFET
[7] High Resistivity substrate

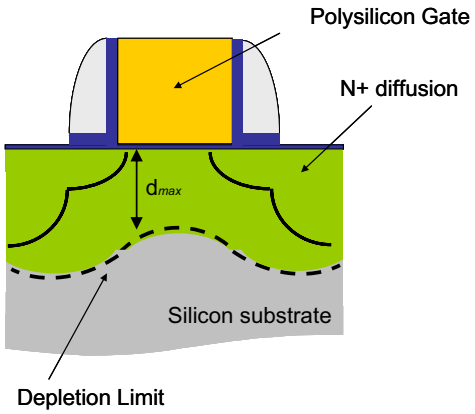
I.2.1.a.vi High resistivity substrate compatibility

Classical bulk CMOS wafer substrate resistivity has typically spanned from 5 mohm-cm on heavily doped epi substrates to 30 ohm-cm on polished wafers. Heavily doped substrates are necessary to prevent against latch-up. SOI technology offers a natural protection against latch-up (*I.2.1.a.ii*), thus it becomes possible to use high resistivity substrates. This type of substrate offers new possibilities for wireless technologies:

- Reduced substrate coupling [27]
    - Digital & Analog/RF on the same die (suppress digital noise coming from substrate)
    - Multi-standards: RF diversity
- High quality factor inductances (more than 50% increasing have been observed) [7], [32]
- Higher density metal to metal capacitors by using all metal layers with reduced substrate losses [10]
- Low attenuation constant transmission lines at RF and millimeter frequencies [18], [34] and [33].

I.3. Properties and Behavior of SOI MOSFET

In a MOSFET transistor channel (*Figure I.9*), the maximum depth of the depletion zone can be expressed by the following equation [3]:



$$d_{\max} = \sqrt{\frac{4\varepsilon_{si}\phi_F}{qN_a}} \qquad (1.1)$$

Figure I.9. Cross section of a MOSFET

Where ϕ_F and ε_{si} are the Fermi potential and the permittivity of the silicon, q is the charge of the electron, and N_a is the density of acceptor atoms.

I.3.1. Comparison and properties of Fully and Partially Depleted SOI MOSFET

When the depletion limit extends over the entire thickness of the active film of silicon, the MOSFET is said to be fully depleted (FD). If a part of the silicon film is not depleted, the MOSFET is called partially depleted (PD). The following figure illustrates these two different structures:

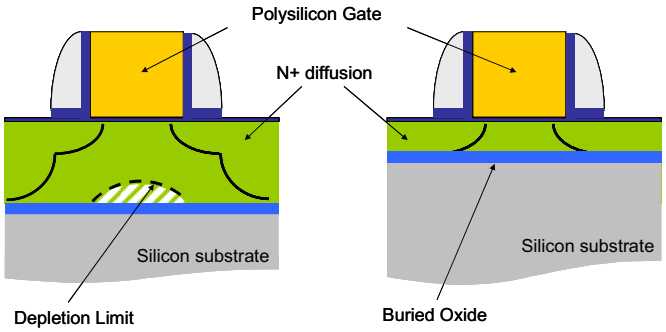
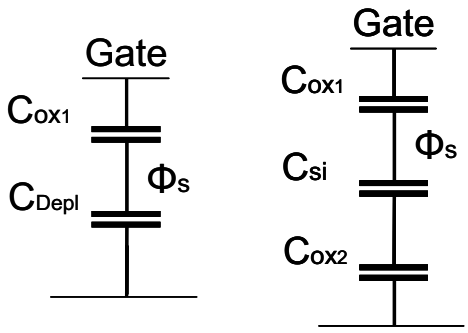


Figure I.10. Partially (left) and Fully (right) Depleted MOSFET

To facilitate the distinction between PD and FD MOSFET, an 'α' coefficient is introduced [14]. This coefficient is a function of the total gate capacitance C_{ox1}, the capacitance of the silicon film and the buried oxide capacitance. The values of 'α' are given by the following equations for FD and PD MOSFET:



$$\alpha_{FD} = \frac{C_{OX2} C_{si}}{C_{OX1}\left(C_{OX2} + C_{si}\right)} \tag{1. 2}$$

$$\alpha_{PD} \approx \frac{C_{depl}}{C_{OX1}} \tag{1. 3}$$

Where C_{OX1} and C_{OX2} are the gate and buried oxide capacitance, C_{depl} and C_{si} are the capacitances related to the depletion zone of the PD and the thin film silicon. The 'α' coefficient measures the efficiency of the coupling between the gate potential and the MOSFET channel potential (Φ_s) at the Si-SiO_2 interface. The best coupling is achieved for a small alpha. Typically, for FD MOSFET alpha is close to zero and around 0.3-0.5 for PD and bulk MOSFET. Nevertheless, the value of alpha is increased for small devices, exhibiting the loss of gate control for the channel potential (Φ_s).

Using the classical space charge assumption, it is possible to develop the expression for the saturation current of the long channel SOI MOSFET:

$$I_D = \frac{W}{L} \cdot \frac{\mu C_{OX1}}{2\left(1+\alpha\right)} \cdot \left(V_{gs} - V_{th}\right)^2 \tag{1. 4}$$

With W and L the width and the length of the transistor, μ is the mobility, V_{gs} is the gate to source voltage, and V_{th} is the threshold voltage. From *(1. 4)* the transconductance is:

$$gm = \frac{\partial I_D}{\partial V_{gs}} = \frac{W}{L} \cdot \frac{\mu C_{OX1}}{\left(1+\alpha\right)} \cdot \left(V_{gs} - V_{th}\right) = \sqrt{2 \cdot I_D \cdot \frac{W}{L} \cdot \frac{\mu C_{OX1}}{1+\alpha}} \tag{1. 5}$$

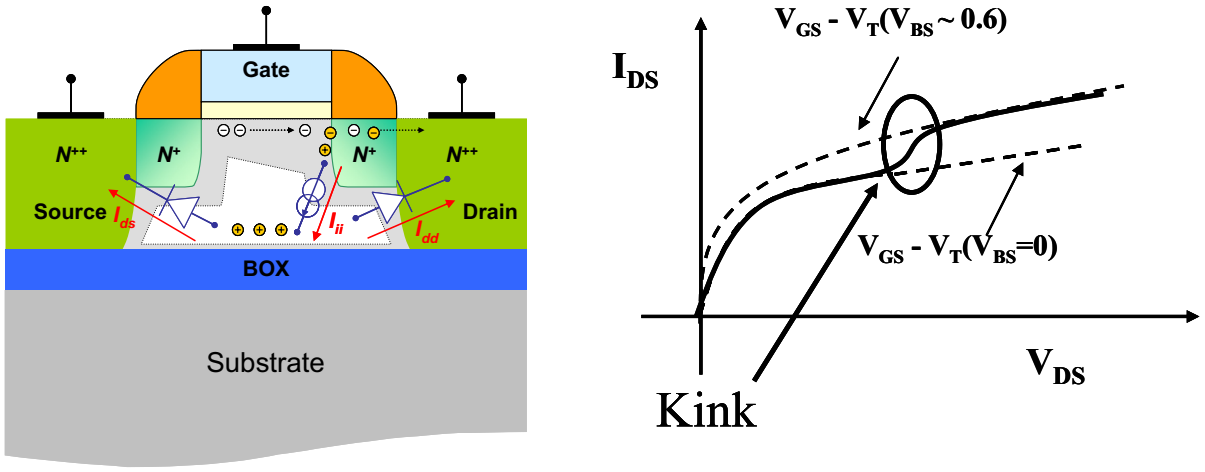
From these ideal equations and the equations *(1. 2)(1. 3)*, it can be deduced that for a technology node, the FD MOSFET has a better transconductance and current drive than the PD or bulk MOSFET. This, because the alpha coefficient is smaller in the case of FD SOI. Nevertheless, the very fine silicon film thickness required in FD MOSFET is hard to process.

I.3.2. Floating Body effects

In Partially Depleted MOSFET, silicon film thickness is larger than the depletion depth *(1. 1)*. So there exists a piece of neutral silicon beneath the front depletion region. If this neutral piece of silicon, called "body", is connected to ground by a "body contact"[8], the characteristics of the device is exactly same as the bulk device. But if this body is left electrically floating, the device will basically behave as a bulk device, but with the notable exception of two parasitic effects, the first one is kink effect or floating body effect, and second on is the presence of parasitic open based NPN bipolar transistor between source and drain.

I.3.2.a. The kink effect

The kink effect is illustrated in the following figure:



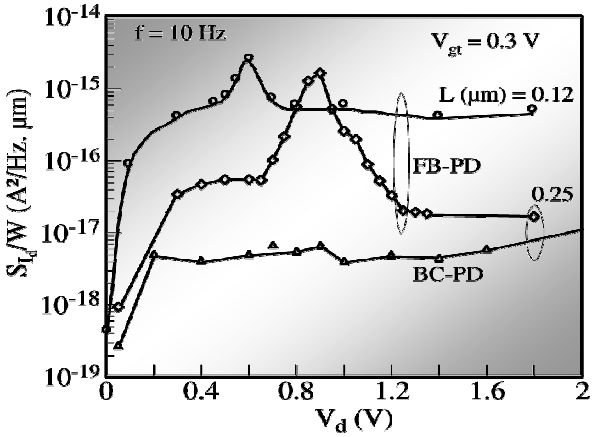
a) *b)*

Figure I.11. kink mechanism illustration (a), I_{DS}-V_{DS} output characteristic of a PD MOSFET (b)

The kink effect mechanism can be explained as follows. For a NMOS transistor, when the drain potential is raised, the channel electrons can acquire sufficient energy in the high electric field zone near the drain to create electron-hole pairs. The generated electrons move into the channel while the holes migrate to the lowest potential, which is the floating body. When the current is reached (i.e. the level of holes is high enough), the diode between the floating body and the source becomes forward biased. The body potential increases. The effective threshold voltage of the MOSFET is reduced, as the potential of the body increases, inducing a higher current and conductance.

[8] Body Contacted MOSFET : BC in the literature

Kink effect also impacts the low frequency noise (*1/f*) [7]. The following figures illustrate this behaviour:



Data from STMicroelectronics CMOS SOI LP 0.13µm & 0.25µm

Figure I.12. Low frequency noise measurements of a PD MOSFET

I.3.2.b. Parasitic open based NPN bipolar effect in FD SOI MOSFET

This effect occurs when the source, body, and drain of MOSFETs act as the emitter, base, and collector of parasitic transistor in which the base current consists of majority carriers produced by ionization [17]. The following figure illustrates this effect:

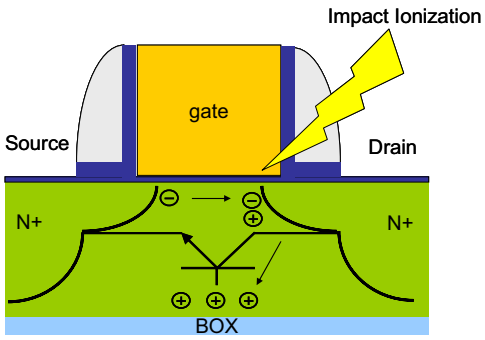


Figure I.13. Illustration of the bipolar effect

Since the body region is more depleted in FD than in PD SOI devices, the emitter injection efficiency for the parasitic bipolar transistor is higher, which makes these effects more likely to occur. When they do occur, they have a number of consequences, such as a reduction in the breakdown voltage between the source and the drain, abnormally steep subthreshold characteristics beyond the theoretical limit, a larger off current, and a smaller threshold voltage.

I.3.3. Which SOI Device for which design?

In order to take advantages of the SOI devices in circuit performances, SOI MOSFET must be chosen taking into account some design considerations. First of all, let's have a look at the advantages and drawbacks of PD and FD MOSFET for a circuit design point of view:

Partially Depleted (PD) MOSFET (silicon thickness under the gate t_{Si} : >60nm):

Benefits	*Drawbacks*

• Reduced parasitic capacitances
• Possibility to leave transistor's body floating
• Direct & easy derivability from CMOS bulk process flow
• Availability of a body terminal to avoid FB[9]:
  ○ Fixed body potential
  ○ Body driven design
	• Self-Heating compared to bulk
	• History effect [9], [8]

Table I.1. Benefits and Drawbacks of the PD SOI MOSFET

Fully Depleted (FD) MOSFET (silicon thickness under the gate t_{Si} < 50nm):

Benefits	*Drawbacks*

• Higher gm for undoped Si layer
• Lower short channel effects
• Quasi ideal sub-threshold slope (60 mV/dec.)
	• Higher self-heating compared to PD
	• Challenges:
	  ○ Very fine film thickness control
	  ○ Limit series resistance increasing
	  ○ Metallic gates required for undoped Si layer
	  ○ Passgate leakage

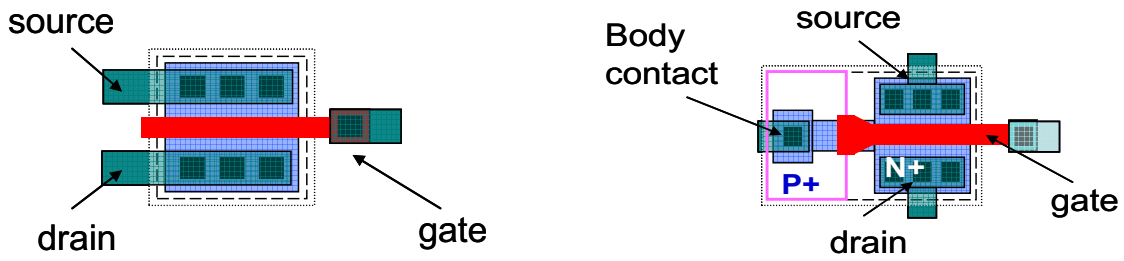
Table I.2. Benefits and Drawbacks of the FD SOI MOSFET

[9] FB : Floating Body in the literature

Despite the attractive benefits of the FD transistor, from the industry point of view, it appears that PD SOI MOSFET is the best trade-off and ready to use SOI MOSFET in comparison with bulk. However, *Intel* exhibits some results of a 50nm FD SOI transistor demonstrating the benefit of using FD SOI transistor [16]. But, in the same time *STMicroelectronics* and *IBM* which are working on PD technologies, argue that FD transistors do not allow the use of multiple threshold voltages [10], [11]. Actually, higher threshold voltages are obtained by increasing the doping level of the channel (N*a*). The value of the maximum depletion depth (d_{max}) is reduced *(1. 1)*. It is then more difficult to keep the transistor Fully Depleted. Also, PD transistors, unlike FD transistors, allow using the technological solutions already developed for bulk transistors from the same technology node.

I.4. FB and BC MOSFET from the CMOS SOI 65nm technology

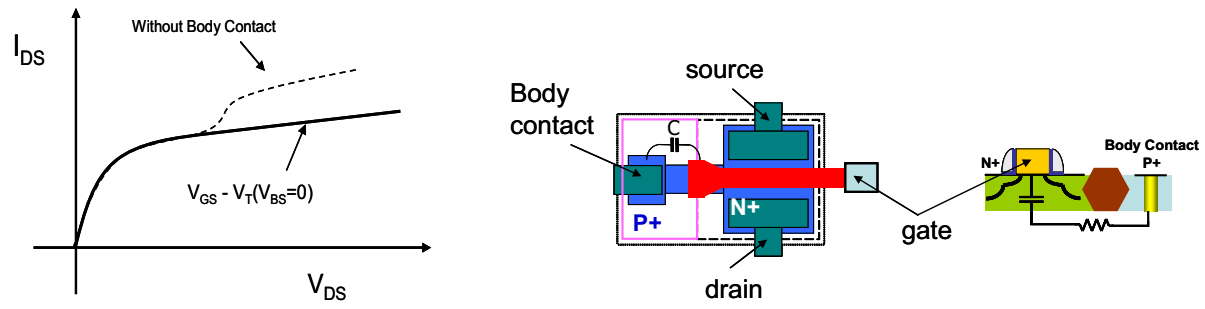
The CMOS SOI 65nm LP technology from *STMicroelectronics* has two SOI MOSFET topologies available. The body contacted and the floating body MOSFET.



a) *b)*

Figure I.14. Floating Body a) and Body Contacted MOSFET

The *Figure I.14* illustrates the layout of the FB and BC device. By using a body contact the BC MOSFET does not suffer from the kink effect. Thus the DC characteristics of the device is exactly the same as the bulk device *Figure I.15 - a)*. Nevertheless, the body contact added to the device has an impact on the size of the component which is not negligible for high integration circuit. Another drawback of the body contact is the additional capacitance created by the contact *Figure I.15 – b)*. This capacitance increases, the drain-source coupling to the gate [19] and thus impacts the high frequency performances [10].



a) *b)*

Figure I.15. a) I_{DS}-V_{DS} BC MOSFET Characteristic ; b) illustration of the additional capacitance in the BC MOSFET

I.4.1. Which PD SOI MOSFET for which design?

As for PD versus FD, the question is open for BC and FB MOSFETs. First of all, it is necessary to estimate which MOSFET figure of merit is targeted in each design. For analog design, the DC gain and the matching between devices (i.e. current variation between two identical devices) are two critical points. Thus, BC MOSFET are preferable since they do not suffer from kink effect and have a higher intrinsic gain [10]. For RF design the choice is more complex:

- If the design needs high gain, low drain-source coupling, low high frequency noise (LNA, MIXER, and SWITCH) the FB MOSFET is preferable [10], [18] and [19].
- If the design is sensitive to low frequency noise, typically a VCO, the BC MOSFET is preferable [7]. In case of high breakdown voltage (PA for instance), BC is also preferable.

I.5. Summary

We have shown that the SOI technology is already used in the industry. The recent SOI consortium creation demonstrates the wish of numerous companies to develop the SOI technology for the mass market.

Several processes to fabricate SOI wafers were discussed in this chapter and finally both SIMOX and UNIBOND techniques are viewed as industrially scaled process.

We have seen the advantages of SOI-MOSFETs in comparison with bulk are important not only for the digital world but also for analog/RF design. Today, for RF applications, the SOI technology allows lowering the total power consumption in both RF and Digital circuits (key for mobile). SOI permits also an easier co-integration of analog/RF and Digital circuits (lower cost by reduced area).

We have exposed that the comparison between Fully Depleted and Partially Depleted SOI shows that despite the attractive benefits of the FD transistor, the currently manufacturable technology is the PD SOI MOSFET. We have also illustrated that for the cases in which floating-body effects must be completely eliminated, it is possible to form an electrical body contact in PD SOI, but not in FD. There are compelling reasons why the PD device design is preferable; these are summarized in *Table I.1* and *Table I.2*.

In the near future, SOI is one of the most promising solutions for applications at high frequencies (60 GHz WLAN…etc). As we have seen, wireless technologies require high-performance transistors and low-loss passive devices (inductors and capacitors). SOI allows the use of high-resistivity substrate (>3KΩ-cm), which can result in high *Q* for the passive elements. High device performance is manifested in SOI MOSFETs having unity current and power gain cut-off frequencies, f_T and f_{MAX}, of more than 150 GHz (for the 65nm generation).

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Chapter II

Actives elements in SOI CMOS 65nm

In comparison to other technologies, CMOS is the most cost-effective solution to date for large scale digital applications and it enables ultra high level system-on-a-chip integration. Driven by high performance digital applications, high frequency performances in silicon technology have considerably increased with geometry scaling. Non digital figure of merits, such as f_T, f_{max} or NF_{min} show that silicon transistors become competitive with III-V transistors [1].

This chapter is built as follows. First, transistor RF figures of merit are discussed, then high frequency small signal model of the MOSFET transistor is presented. Next, the noise sources and their modeling in MOSFET transistors are developed. After that, SOI MOSFET characterization is presented and performances of the CMOS SOI and bulk 65nm technologies are compared with the state of the art. Finally, BSIM MOSFET model are detailed.

II.1. Transistor RF figures of merit

The two most important features of transistor are its ability to amplify (important for analog and RF) and its ability to act as a switch (important for digital electronics and mixers). These two characteristics are evaluated using the gain definition for analog RF and the I_{on}/I_{off} performances for digital electronics. Today CMOS technologies have to deal with these two important figures of merits. Unilateral gain is used to evaluate the figure of merit f_{max}. The maximum oscillation frequency is the frequency at which the unilateral power gain is equal to 1. The current gain is used to evaluate the figure of merit f_T. The device f_T is the frequency at which the short circuit current gain falls to unity (0dB). In this work, transistors are evaluated using the maximum stable gain (MSG), the maximum available gain (MAG), the unilateral power gain or Mason gain (U), the current gain (H_{21}) and the associated gain (G_{ass}) All these gain definitions are given in appendix.

II.2. High Frequency small signal model of the SOI MOSFET transistor

One of the advantages of SOI transistors compared to bulk devices is that at millimeter wave frequencies, the substrate does not impact significantly the behaviour of transistors. Thanks to the thickness of the buried oxide, the body effect can be neglected at high frequency [2]. Thus, it is not necessary to develop a four terminal model for the SOI floating body transistor used at RF and millimeter wave frequencies.

In the next two sections, a general small signal equivalent circuit of floating body SOI MOSFETs is presented, taking into account its intrinsic behavior and its physical structure. The model extraction methodology is not discussed here. The complete description of this methodology is given in [3] and [4]. An example of extracted small signal circuit elements is given in appendix.

II.2.1. Quasi static model

Small signal or linear models are used to evaluate the stability, gain, noise and bandwidth of designed circuits. A small-signal model is generated by taking derivatives of the current-voltage curves at biasing point. As long as the signal is small relative to the nonlinearity of the device, the derivatives do not vary significantly, and can be treated as standard linear circuit elements. A big advantage of small signal models is they can be solved directly, while large signal nonlinear models are generally solved iteratively, with possible numeric convergence or stability issues.

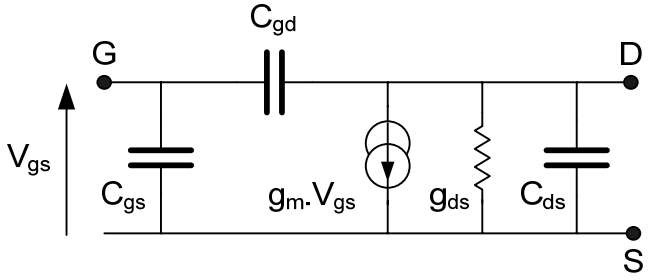


Figure II.1 Intrinsic quasi static small signal model of a (SOI) MOSFET

To get an understanding of the high-frequency properties of a MOSFET and to analyze them, the equivalent circuit should be simplified a lot. Quasi-static behavior of the channel charge is assumed under the hypothesis that the electron channel transit time is negligibly small. The transcapacitances are also neglected. *Figure II.1* described the intrinsic quasi static

model of the MOSFET. The bulk or substrate node has been neglected as explain previously (not necessary in SOI) as well as the g_{mbs}, C_{gb} and R_B components. The transistor geometry affects each device terminals by capacitive coupling and can be modeled by capacitances added in the equivalent circuit as shown in *Figure II.1*. All these components are bias dependent and are related to variations of charges or currents when a small signal is applied around equilibrium on a terminal. The capacitances between the source, drain and gate are defined as follows:

$$C_{gd} = -\left.\frac{\partial q_g}{\partial v_d}\right|_{v_s=v_g=0}$$
$$C_{gs} = -\left.\frac{\partial q_g}{\partial v_s}\right|_{v_d=v_g=0} \quad (2.\ 1)$$
$$C_{ds} = -\left.\frac{\partial q_d}{\partial v_s}\right|_{v_d=v_g=0}$$

These relations can be used only in quasi-static operation. The applied small signal is varying slowly enough such as the charges respond instantaneously to the applied signal. The capacitances are the representations of the influence on the charges of a voltage applied on a terminal, with regards to the MOSFET physic. They are called intrinsic capacitances. Moreover, MOSFETs are imperfect current sources, thus an output conductance must be added in the model. It is defined by:

$$g_{ds} = \left.\frac{\partial i_{ds}}{\partial v_{ds}}\right|_{v_s=v_g=0} \quad (2.\ 2)$$

II.2.2. Non quasi static model

In the previous section, a MOSFET equivalent circuit has been presented, considering that charges respond without delay to the applied signal. But when the frequency increases, the charges are not able to follow the signal instantaneously. According to Tsividis, the frequency upper limit of the quasi-static model is proportional to $1/L^2$, where L is the channel length of the transistor [5]. To model the non-quasi-static effects, the MOSFET channel can be divided into several small transistors connected together. Then, quasi-static models are used for all sub-transistors. This solution can be used when the values of the intrinsic elements are obtained using formulae from the physical model. If they have to be extracted from measurements, this method cannot be used, because the number of

unknowns becomes too high. Instead of dividing the MOSFET into several small transistors, the non-quasi-static effects can be modeled by introducing new elements in the equivalent circuit (R_i, R_{gd} and a time delay (τ) affecting the transconductance) [5]. These elements are represented in *Figure II.2*. The command of the voltage controlled current source is still the potential "V_{gsi}"applied to the intrinsic capacitance C_{gs}.

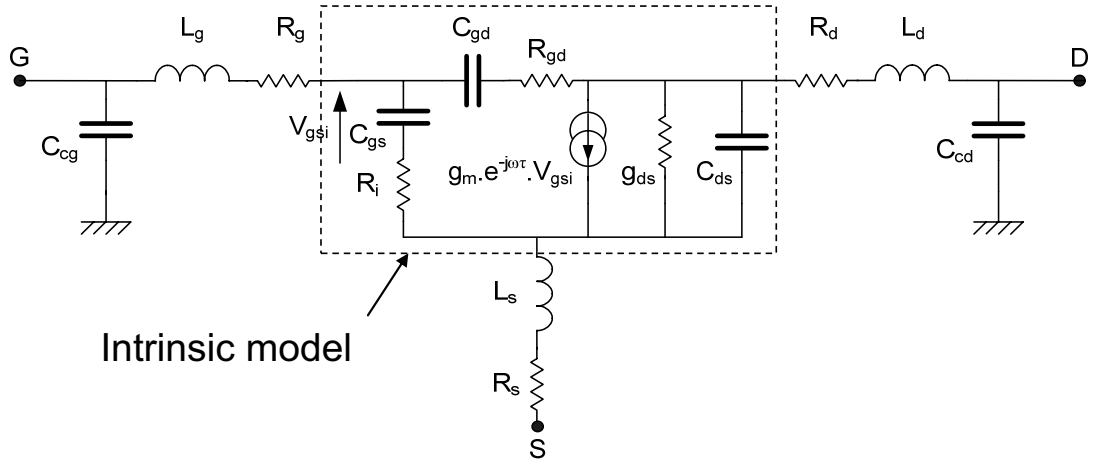


Figure II.2 Non quasi static RF small signal model of the MOSFET including extrinsic parasitic elements.

The extrinsic gate to source (C_{gse}), gate to drain (C_{gde}) and drain to source (C_{dse}) capacitances (not shown in schematic) are included into C_{gs}, C_{gd} and C_{ds}. They come from two different causes:

- C_{gse} and C_{gde} include overlap capacitances, located between the gate oxide and the source and drain diffusion under the gate. They also include the fringing capacitances from the gate sides to the source and drain implants.
- The capacitance C_{dse} is completely different from the two other extrinsic capacitances. It is the expression of the coupling between source and drain through the film of silicon, the buried oxide and the substrate.

II.2.2.a. Extrinsic parasitic access models

The intrinsic gate, source and drain are connected to the Metal one of the BEOL[1] by the gate, source and drain finger contacts (also called CO). These fingers and contacts have a given resistivity. They are distributed elements but since the transistor is generally small compared to the wave length they are modeled by using lumped resistances called R_g , R_s and R_d connected to the gate, the source, and the drain respectively (*Figure II.2*). The resistances R_d and R_s include the metallic losses and the contact resistances between the metal and the source and drain implants. They are proportional to the inverse of the transistor width. The resistance R_g includes the resistance of the gate fingers, which is proportional to the transistor width, and the resistance of the contacts and metallic lines. In

[1] Back End Of Line

most of the cases, the resistance of the gate finger is much higher than the others. An equation of R_g taking into account all these parasitic can be obtain by combining [6] and [17] :

$$R_g = \frac{R_{\square} \cdot W_f}{g_a^2 L \cdot 3N_f^{\,2}} + \frac{R_{\square}.XGW}{g_a^2 L \cdot 3N_f^{\,2}} + \frac{R_{cont}}{N_{cont}.N_f.g_a} \tag{2. 3}$$

With is $R_{\square}$ is the material sheet resistance, N_f is the number of fingers, g_a is the number of gate accesses (1 or 2), XGW the distance between the gate contacts and the active part of the transistor, L and W_f the length and the width of a unit finger and R_{cont} and N_{cont} the contact resistance and the number of contacts respectively.

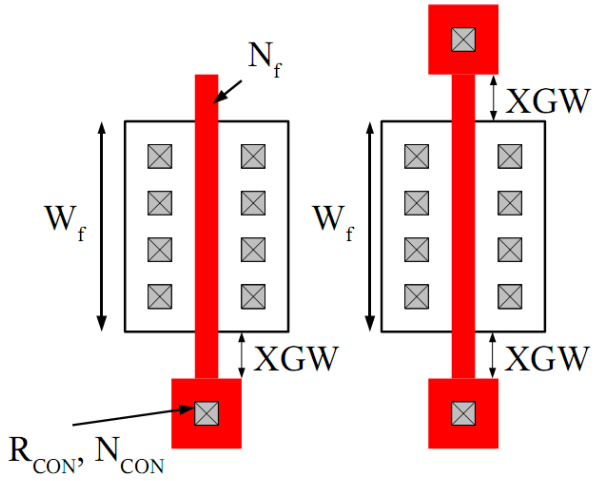


Figure II.3 Geometrical aspect of the gate resistance with one (left) and two (right) gate accesses

Using the same methodology, parasitic inductances can be defined. They are called L_g, L_d and L_s in *Figure II.2*. For sub-micron MOSFETs, these inductances are usually a few pico Henry (up to metal one) and are nearly negligible within the frequency band of operation.

Finally the capacitances C_{cg} and C_{cd} represent the contact metallic interconnection capacitances from the gate and the drain.

II.2.2.b. f_T, f_{max} figures of merit from small signal model

f_T, f_{max} figures of merit described in section *II.1* can be derived from the elements of the small signal model described in the previous section (*Figure II.2*). A first approximation for f_T is given by:

$$f_T \approx \frac{g_m}{C_{gs}\sqrt{1+2\cdot\frac{C_{gd}}{C_{gs}}}} \tag{2. 4}$$

A more complete expression of f_T is then given in [25]:

$$f_T \approx \frac{f_c}{1+\frac{C_{gd}}{C_{gs}}\left(1+\left(R_s+R_d\right)\left(g_m+g_{ds}\right)\right)+\left(R_s+R_d\right)\cdot g_{ds}} \quad \text{with} \quad f_c=\frac{g_m}{2\pi C_{gs}} \tag{2. 5}$$

The f_{max} figure of merit is given by:

$$f_{\max} \approx \frac{g_m}{2\pi\cdot C_{gs}\cdot 2\sqrt{\left(R_g+R_s+R_i\right)\cdot\left(g_{ds}+g_m\frac{C_{gd}}{C_{gs}}\right)}} \tag{2. 6}$$

A more complete expression of f_{max} has been also defined in [26]:

$$f_{\max} \approx \frac{f_c}{\left(1+\frac{C_{gd}}{C_{gs}}\right)\cdot\sqrt{4g_{ds}\left(R_g+R_s+R_i\right)+2\cdot\frac{C_{gd}}{C_{gs}}\cdot\left(g_m\left(R_s+R_i\right)+\frac{C_{gd}}{C_{gs}}\right)}} \tag{2. 7}$$

Thanks to these expressions, the limiting factors of the MOSFET gain performances can be easily estimated [7].

II.3. Noise analysis of the MOSFET transistor

Noise is a natural phenomenon that affects every electronic systems. Because noise may mask the desired signal, it is important to understand and minimize its effects on the performance of RF devices. In the following section the noise contribution in MOSFET transistor is investigated. To understand the noise mechanisms, a single MOSFET can be seen as a small circuit as depicted in *Figure II.4*. Thus different noise sources exist in a MOS transistor as shown in *Figure II.4*. They include access resistance thermal noise at the gate $\overline{i_G^2}$, access resistance thermal noise at the drain $\overline{i_D^2}$, access resistance thermal noise at the source $\overline{i_S^2}$, thermal noise and the flicker noise in the channel $\overline{i_d^2}$ [11], [12], induced gate noise $\overline{i_g^2}$ [9] and for CMOS bulk transistor, the substrate resistance thermal noise $\overline{i_{SB}{}^2}, \overline{i_{DB}{}^2}, \overline{i_{DSB}{}^2}$ [11]. In CMOS SOI body contacted transistors another noise source comes from the resistance of the body contact [13] (not depicted here).

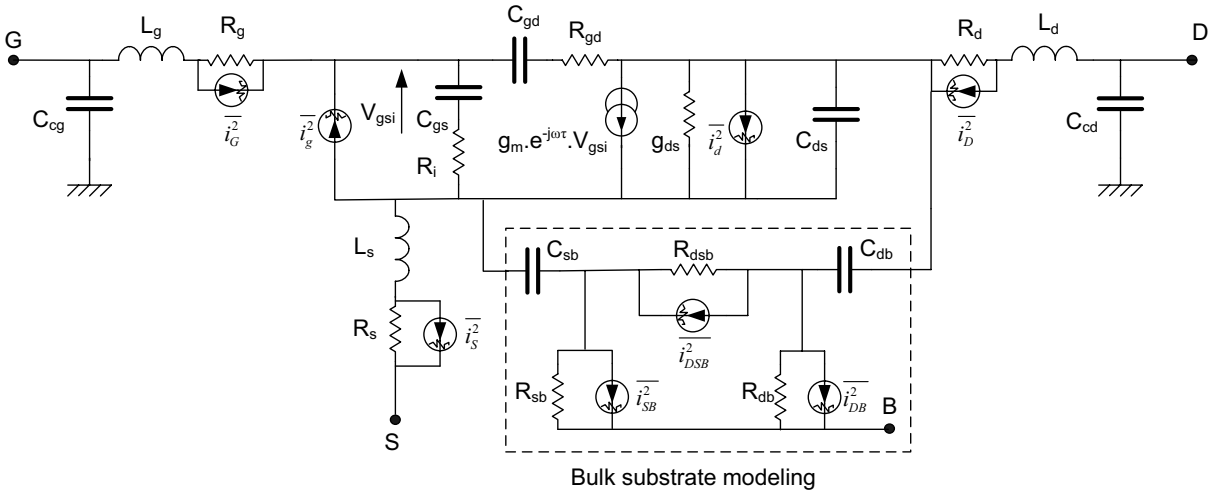


Figure II.4 The different noise sources in a MOSFET transistor (bulk and SOI FB).

Channel resistance and all terminal resistances contribute to the thermal noise at high frequency, but typically channel resistance dominates in the contributions of the thermal noise from the resistances in the device. Induced gate noise is generated by the capacitive coupling of local noise sources within the channel to the gate, and usually it plays a more important role as the operation frequency goes much higher than the frequency at which channel thermal noise dominates.

II.3.1. Flicker Noise

In principle, flicker noise also called 1/f noise is a low frequency noise and it mainly affects the low frequency performance of the device, so it can be ignored at very high frequency. However, the contribution of flicker noise should be considered in designing some RF and millimeter wave circuits such as mixers, oscillators, or frequency dividers that up-convert the low-frequency noise to higher frequency. It is the dominant source for phase noise in silicon MOSFET circuits and it sets a lower limit on the level of signal detection. It is one of the factors limiting the achievable dynamic range of CMOS ICs (cf. *Chapter IV*). In this section this noise modeling is not developed but a modeling approach can be found in [5].

II.3.2. Thermal noise

The thermal noise of the MOSFET imposes a fundamental limitation on CMOS LNAs [14]. Based on the fact that the MOSFET is a modulated resistor capacitively coupled to the gate (*Figure II.5*), Van Der Ziel has proposed a thermal noise model for MOSFETs, which consists of drain current noise, induced gate current noise, and their cross-correlation coefficient [9]. This model has been improved by Pucel [15] and Cappy [15] and is called "PRC". The P, R, C coefficients are defined in the following equations:

$$\overline{i_g^2} = 4 \cdot k \cdot T_A \cdot R \cdot \frac{\omega^2 C_{gsi}^2}{g_{mi}} \Delta f \tag{2. 8}$$

$$\overline{i_d^2} = 4 \cdot k \cdot T_A \cdot P \cdot g_{mi} \Delta f \tag{2. 9}$$

$$\frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2}\,\overline{i_d^2}}} \approx j \frac{\Im\left(\overline{i_g i_d^*}\right)}{\sqrt{\overline{i_g^2}\,\overline{i_d^2}}} = jC \tag{2. 10}$$

With T_A is the ambient temperature, k is the Boltzmann constant and P, R and C are dimensionless coefficients.

Using this model the intrinsic minimum noise factor may be defined as:

$$F_{\min} = 1 + 2\frac{f}{f_c}\sqrt{R.P.\left(1 - C^2\right)} \quad with \quad f_c = \frac{g_{mi}}{2\pi C_{gsi}} \tag{2. 11}$$

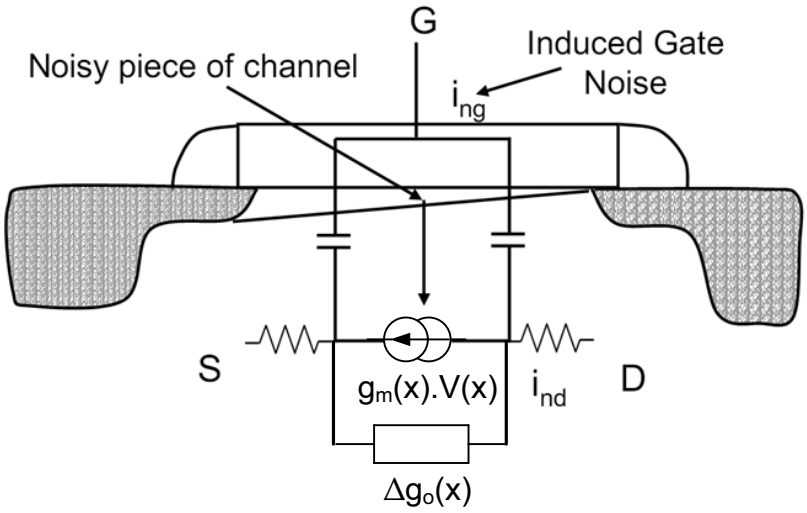


Figure II.5 Induced gate noise effects in MOSFET devices.

II.3.3. Thermal noise from access resistances

In order to fully evaluate the minimum noise factor of a MOSFET, thermal noise coming from the different terminal accesses of the device must be taken into account (Figure II.4). Contrary to the thermal noise and the induced gate noise, these noises are not depending on the applied voltage. Among these sources the poly gate resistance R_G is the main noise contributor.

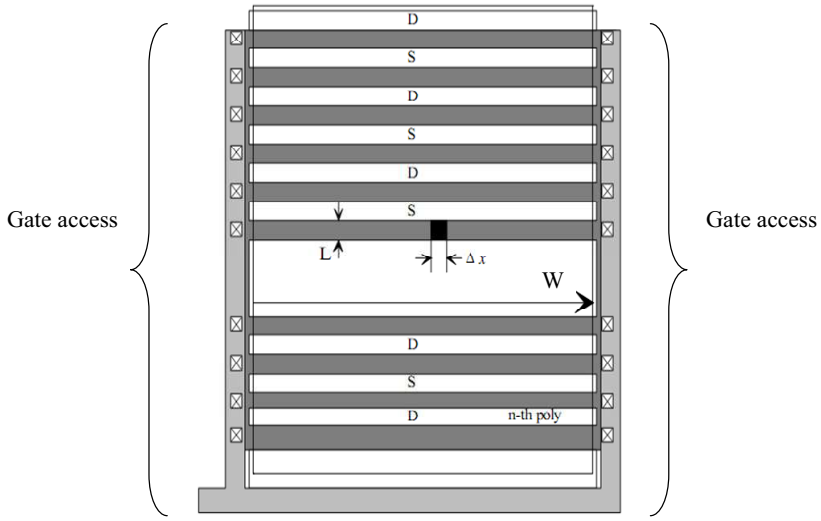


Figure II.6 The finger structure of a MOS transistor.

Taking into account the distributed aspect of this resistance (*Figure II.6*) the equivalent lumped resistance can be express using (2. 3). There is an optimum finger size that minimizes the NF_{min} (*Chapter IV*). At first order, the smallest finger would be the best since the R_G value is reduced. But for small finger size (<1µm in the CMOS 65nm technology) the fringing capacitance coming from the contacts become preponderant over the other capacitances reducing f_T and f_{max} and the minimum noise is not improved [19].

An expression taking into account the access resistances R_G and R_D and the extrinsic capacitances C_{gse} (gate-source capacitance) and C_{gde} (drain-source capacitance) has been given by Danneville [20]:

$$F_{\min} \approx 1 + 2\frac{f}{f_c}\left(\frac{C_{gd}}{C_{gs}}\right)\sqrt{PR + P\left(R_G + R_S\right)g_m} \qquad (2.\ 12)$$

II.4. Noise temperatures

In [21], Pospieszalski proposed an alternative high frequency noise model. This model dissociates the noise on the gate from the noise on the drain. In this way, the noisy equivalent circuit includes an input voltage noise source e_g and an output current source i'_d as shown *Figure II.7*:

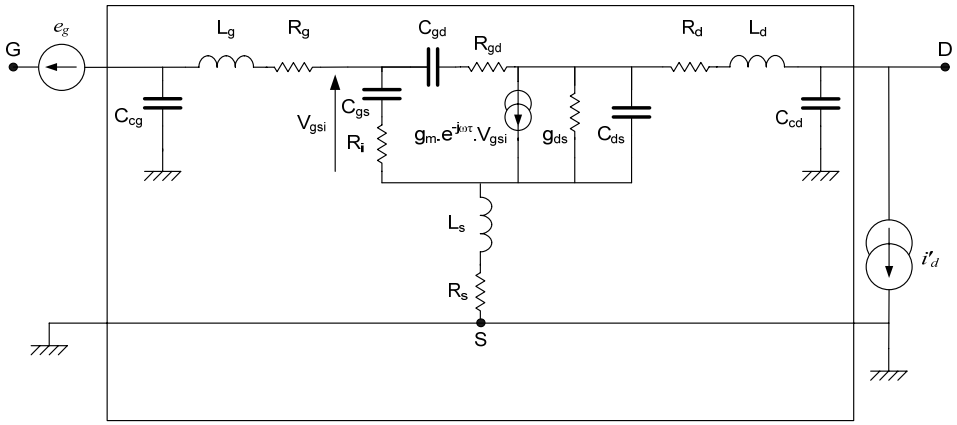


Figure II.7 RF MOSFET small signal model including two uncorrelated noise sources.

The correlation between e_g and i'_d, $\overline{e_g i_d^{'*}}$ is assumed to be equal to zero. From these two noise sources Pospieszalski defined two equivalent noise temperatures T_g and T_d as:

$$T_g = \frac{\overline{e_g^2}}{4k\Re\left(\left[H_{11}\right]\right)\Delta f} \tag{2. 13}$$

$$T_d = \frac{\overline{i_d^2}}{4k\Re\left(\left[H_{22}\right]\right)\Delta f} \tag{2. 14}$$

With [H] the H extrinsic matrix of the quadripole. Even if this model has been developed for MESFET it is well suited for MOSFET devices because the high frequency noise mechanisms are similar [22].

II.4.1. High Frequency noise measurements and associated models

In this work, the noise measurement technique called NF50 (FET Noise characterization under 50Ω impedance) has been used. An illustration of this technique is given in *Figure II.8*.

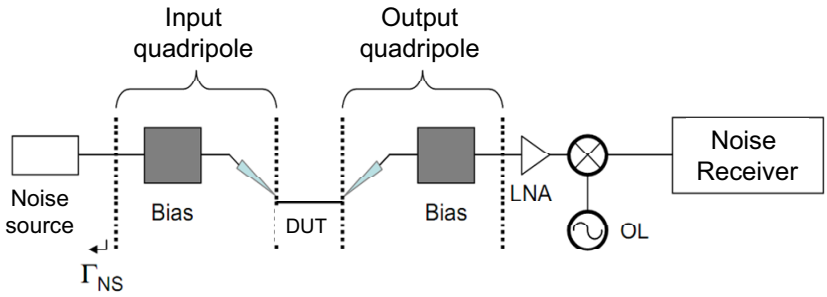


Figure II.8 NF50 noise measurement bench

The four noise parameters are obtained from noise figure with a single 50Ω generator impedance measured versus frequency and the two uncorrelated noise parameters model described in *Figure II.7*. This measurement technique is described by Dambrine in [22]. By

adding two-uncorrelated noise sources, all the MOSFET's noise parameters $\left(NF_{\min}, R_n, \left|\Gamma_{opt}\right| \text{ and } \arg\left(\Gamma_{opt}\right)\right)$ can be deduced.

II.5. SOI MOSFET characterization

In this section, SOI CMOS n-MOSFET characterization results are presented. These transistors are floating body and body contacted (cf. *Chapter I*). The transistors are processed in STMicroelectronics manufacturing process SOI CMOS065 LP with a MOSFET physical gate length of 60nm. They were measured on wafer and all measurements were performed at a source and load impedance of 50Ω. S-parameters were measured using a 0-110GHz vectorial network analyzer. The noise figure test bench uses the NF50 method described previously and consists of a noise figure meter, a test set extension and a mixer allowing accurate measurement from 0 to 40GHz.

Ref device	Lpoly (um)	Wfing um)	Nfing	Ngc	Ncell	Wtot (um)
ZTM12 FB	**0.06**	**2**	**4**	**2**	**8**	**64**
ZTM13 FB	**0.06**	**1**	**8**	**2**	**8**	**64**
ZTS12 BC	**0.06**	**2**	**4**	**2**	**8**	**64**
ZTS13 BC	**0.06**	**1**	**8**	**2**	**8**	**64**

Table II.1. Summary of the characterized devices

The *Table II.1* summarizes the measured devices which are NMOS Low Vt, Low Power (GO1), Floating Body (FB) and Body Contacted (BC) transistors. All transistors have a total width of 64µm and 0,06µm length with double gate access (Ngc=2). The unit finger size are 1 and 2µm for both floating body and body contacted transistors.

II.5.1. DC performances

The measured DC performances are summed up in the *Table II.2.* These results show that the floating body transistors offer a better transconductance g_m. However the DC gain is ~7% better for the Body Contacted transistor. The threshold voltage is the same for all transistors regardless of the geometry. These results illustrate that the DC gain is at first order not a function of the finger size contrary to the RF performances.

Ref device	V_{th} (V)	Gm_{max} @ V_{gs}=0.8V	I_{ds} @ V_{gs}=0.8V	Intrinsic @V_{gs}=0.8V		
				g_m	g_{ds}	g_m/g_{ds}
ZTM12 FB	0.48	50.24 (mS)	21 (mA)	58 (mS)	11 (mS)	5.27
		785 (mS/mm)	328 (mA/mm)	906 (mS/mm)	172 (mS/mm)	
ZTM13 FB	0.48	52.42 (mS)	19.8 (mA)	60 (mS)	11 (mS)	5.45
		819 (mS/mm)	310 (mA/mm)	937 (mS/mm)	172 (S/mm)	
ZTS12 BC	0.48	36.74 (mS)	13.8 (mA)	61 (mS)	11 (mS)	5.55
		574 (mS/mm)	215 (mA/mm)	953 (mS/mm)	172 (mS/mm)	
ZTS13 BC	0.48	38.91 (mS)	14 (mA)	65 (mS)	11 (mS)	5.91
		608 (mS/mm)	218 (mA/mm)	1016 (mS/mm)	172 (mS/mm)	

Table II.2. DC performances of the measured devices

II.5.2. RF performances

The following figures summarize the RF performances of FB and BC transistors. The *Figure II.9* shows performances of the FB and BC transistors of 64x1x0,06 µm². The f_T and f_{max} of the two transistors are 155/200 GHz and 108/126 GHz respectively. The NF_{min} and the associated gain analysis shows that for millimeter wave low noise applications the floating body transistor is the more appropriate. It offers 3.5dB minimum noise figure at 80GHz with 5dB associated gain while body contacted transistor does not offer more than 2dB gain with 8.5dB noise figure.

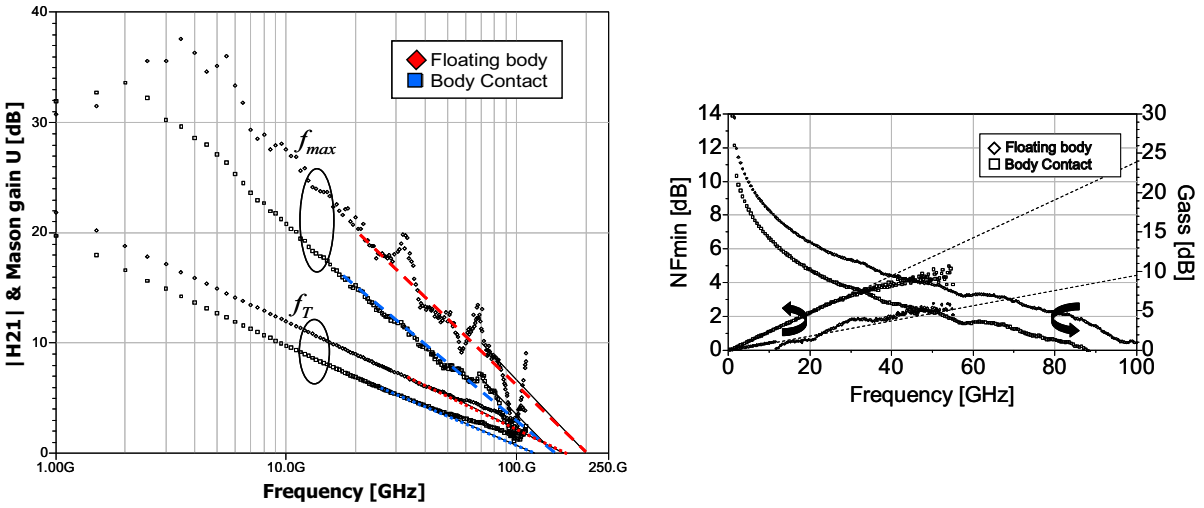


Figure II.9 f_T, f_{max}, NF_{min} and G_{ass} for a Floating body and a body contacted transistor; n-MOSFET ref ZTM13 & ZTS13 (cf.Table II.1), Vd=1.2V, Id=300mA/mm for (f_T/f_{max}) and Id=100mA/mm for NF_{min}/G_{ass}

These performances differences come from the parasitic capacitance added by the body contact. Nevertheless, the optimum finger width is different between the floating body and the body contacted devices. When the finger width is over reduced, proportion of added parasitic capacitance is increased decreasing performances [8]. The following figure illustrates this effect:

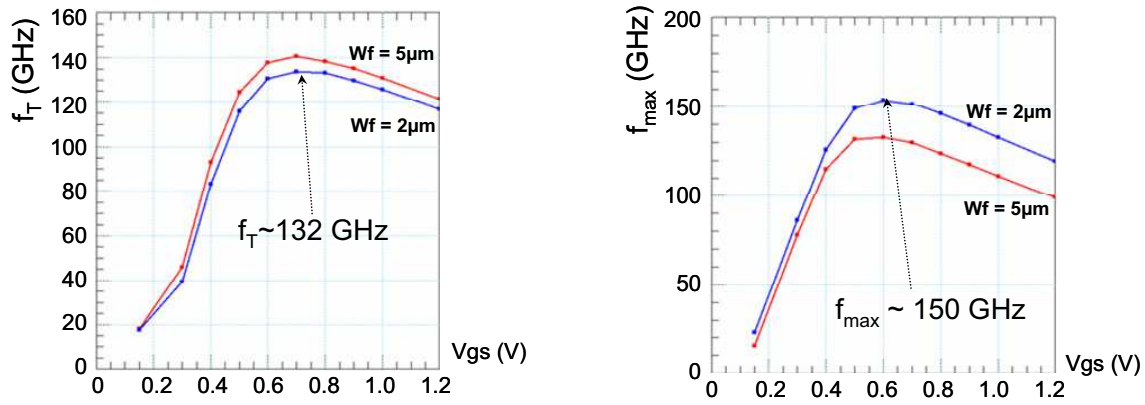


Figure II.10 f_T, f_{max} of two body contacted transistors ;n-MOSFET L=0,063µm, Vd=1.2V [8]

These results show that even if the floating body device is preferred to avoid the parasitic capacitance added by the body contact, high f_{max} is also possible with body contacted devices by using an optimized layout.

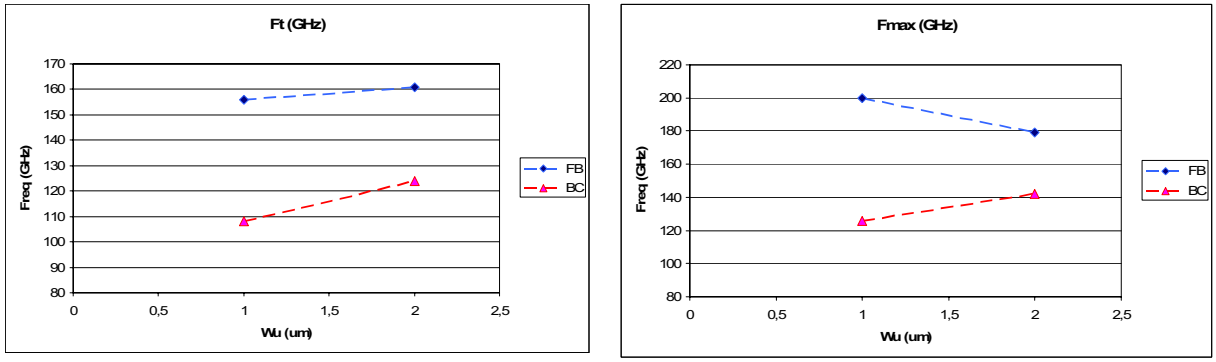


Figure II.11 f_T and f_{max} trend for measured transistor versus unit finger size (Wu)

The *Figure II.11* shows the trend for f_T and f_{max} with respect to the unit finger size. This trend is in line with the previous observation. The *Figure II.12* summarizes the NF_{min} and associated gain performances for the measured transistors. The best performance is achieved for the floating body transistor using unit finger size of 1µm and double gate access. This figure shows also that the optimum current density for noise performances is independent of the size and the type of transistor (BC or FB). The optimum biasing is always achieved for a drain current density of 150mA/mm.

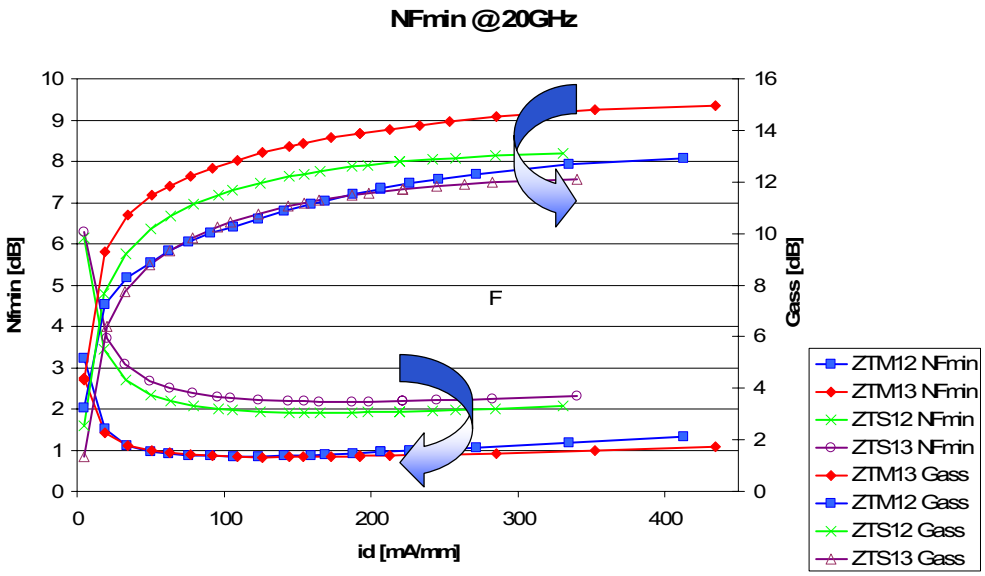


Figure II.12 NF_{min} and G_{ass} at 20GHz summary for the measured devices

II.6. CMOS Transistors State of the Art

As CMOS technology continues to scale down allowing operation millimeter wave region, it provides the opportunity for low-cost integration of RF/digital/analog functions on the same chip. Today, CMOS performances (f_T/f_{max}) are high enough to design circuits from analog to millimeter wave frequencies as shown in *Figure II.13*:

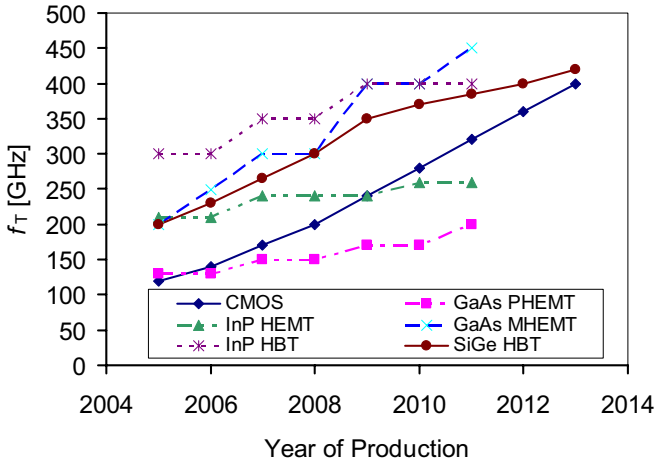


Figure II.13 Roadmap of the f_T according to the year of production for Silicon and III-V devices (from the 2006 ITRS[1]).

The following two figures give an overview of f_T and f_{max} performances according to physical gate length for different NMOS devices (LP and GP):

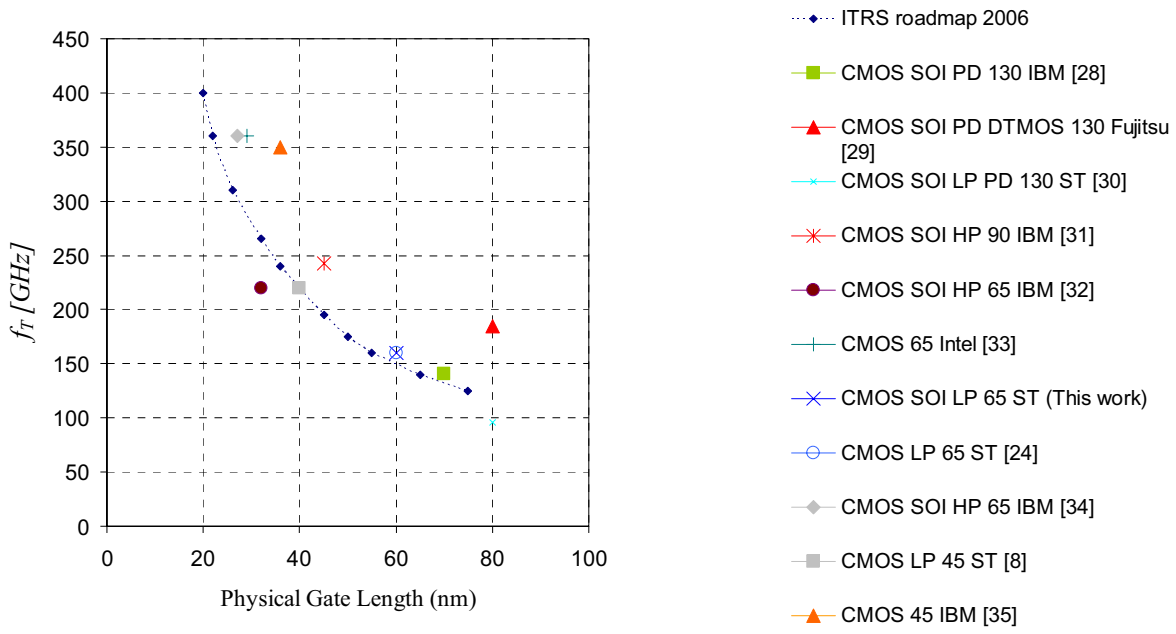


Figure II.14 f_T ITRS road-map and several foundries' performances

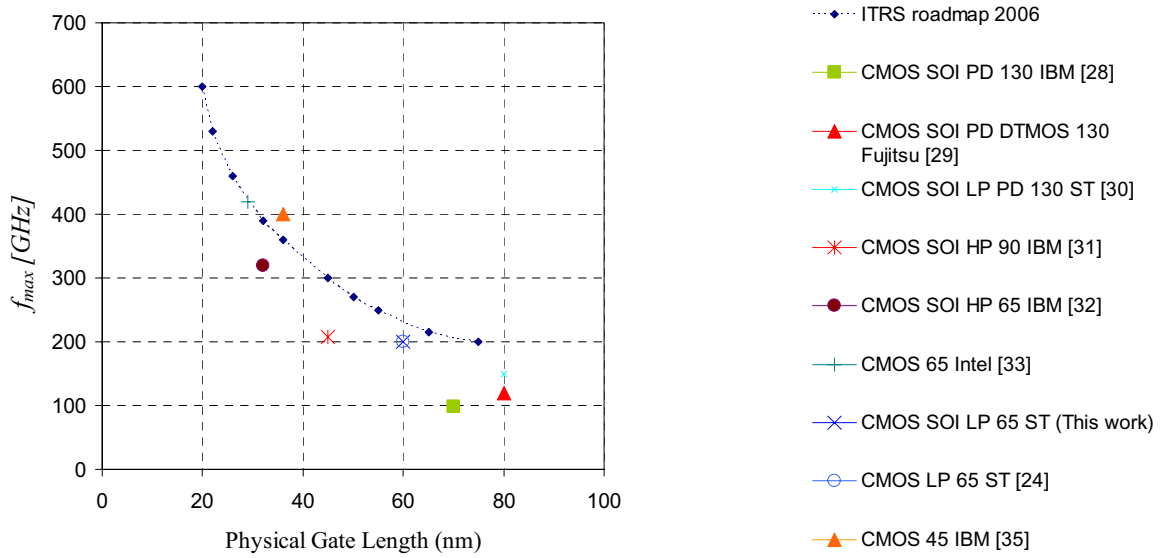
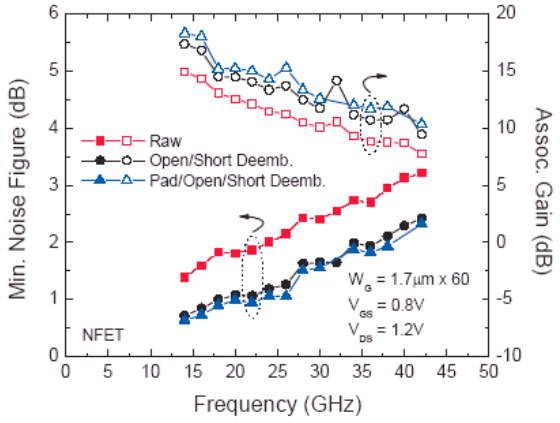
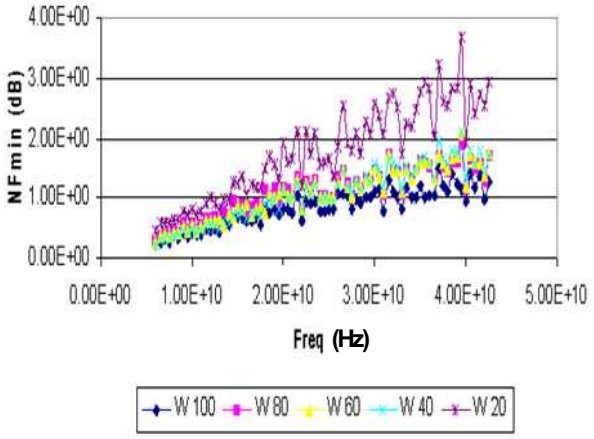


Figure II.15 f_{max} ITRS road-map and several foundries' performances

From the above figure it appears that to improve NF_{min} as f_T and f_{max} the solution would be to reduce the gate length. But the gate length reduction does not always guarantee lower NF_{min}. If by scaling down the gate length the gate or source/drain resistance is not reduced, NF_{min} does not decrease as expected [8]. The following figure illustrates this phenomenon. The two devices from *IBM* and *STMicroelectronics* have the same NF_{min} at 24GHz but a gate length of 35nm and 60nm respectively.



IBM [27]
NMOS Bulk 45nm, Lg = 35nm
2 gate access, Wf = 1.7µm, Nf=60
Vgs =0.8V, Vds = 1.2V
NF_{min} ~ 1dB @ 24GHz



STMicroelectronics [24]
NMOS Bulk & SOI floating 65nm LP,
Lg = 60nm , 2 gate access, Wf =1µm
Ids = 150µA/µm, Vds = 1.2V
NF_{min} ~ 1 dB @ 24GHz

Figure II.16 NF_{min} comparison for different gates length and technology[8]

The *Table II.3* gives the summary of CMOS SOI and bulk performances of several foundries:

References	Technology Nodes	Foundries	L_{poly} (nm)	f_T (GHz)	f_{max} (GHz)	NFmin @ 10GHz
[28]	CMOS SOI PD 130	IBM	70	141	98	<1.5
[29]	CMOS SOI PD DTMOS 130	Fujitsu	80	185	120	0.8
[30]	CMOS SOI LP PD 130	ST	80	96	150	1.3
[31]	CMOS SOI HP 90	IBM	45	243	208	-
[32]	CMOS SOI HP 65	IBM	32	220	320	1.4
[33]	CMOS 65	Intel	29	360	420	-
This work	CMOS SOI LP 65	ST	60	160	200	0.5
[24]	CMOS LP 65	ST	60	160	200	0.5
[34]	CMOS SOI HP 65	IBM	27	360	-	1
[8]	CMOS LP 45	ST	40	220	-	-
[35]	CMOS 45	IBM	36	350	400	1

Table II.3. SOI and Bulk NMOS performances of several foundries

The technology studied in this work has shown the best noise performance reported for CMOS devices. In comparison with III-V or bipolar technologies, CMOS performances (f_T/f_{max}) become quite similar and are high enough to design analog circuits from RF to millimeter wave frequencies.

II.7. MOSFET Transistor Models

In this work, two types of models have been used. In order to evaluate stability, gain, noise and matching the small signal model described in *II.2.2* has been extracted from measurements (cf. appendix B.). For linearity simulations and more complex design using various MOSFET geometries and biasing, the BSIM model from Berkeley University has been used.

II.7.1.a. BSIM3 SOI Model

A derivative of the BSIM3 MOSFET model is the SOI version: BSIM3SOI [36]. The BSIM3 model is made more complex, in order to account for the different SOI effects. These include the floating body effect, which has been made dynamically depending on the device geometry and operating voltages. This model can dynamically and continuously describe the transitions from FD to PD behavior affecting both the current and active charge models. The I_d/V_d model is modified from BSIM3v3.1 and the charge model represents a lot of new formulations. Basically, the active charge model is related to the Yang, Epler and Chatterjee model, but more charge components in the substrate have been taken into account. The description of depletion charge is different to BSIM3. As in BSIM3, the charge model has a separate effective channel dimension. The zero-bias and fringe capacitances from the gate are similar to the basic BSIM3 model. However, the buried oxide requires additional fringe capacitances (C_{essw} and C_{edsw} in Figure II.17). The physical sources of SOI MOSFET parasitic capacitances are shown in *Figure II.17* and the resulting equivalent circuit in *Figure II.18*.

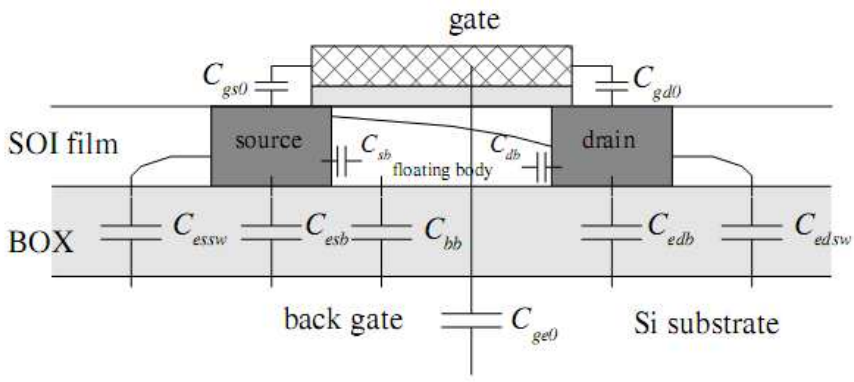


Figure II.17 Sources of SOI MOS parasitic capacitances.

There are notable capacitances formed between the source and the back-gate, as well as between the drain and the back-gate. These are the fringing side-wall components Cessw and Cedsw, as well as the extrinsic bottom area capacitances Cesb and Cedb, which are

voltage dependent. The capacitance between the floating body and back-gate has also been taken into account.

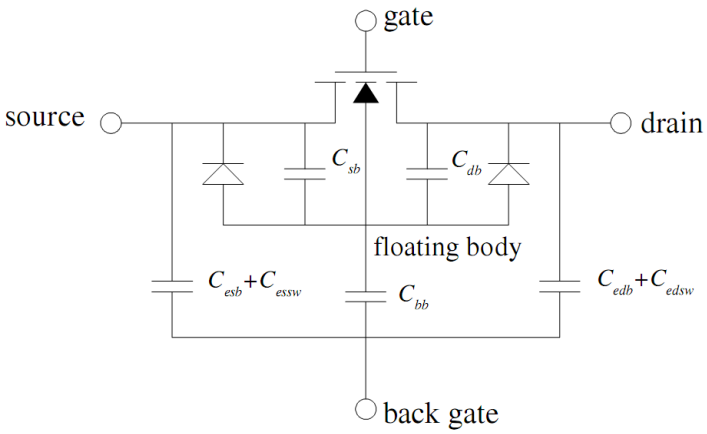


Figure II.18 BSIM3SOI components between the floating body, source, drain and back gate.

Because of the over 200 parameters, the BSIM3SOI is a heavy model to simulate. This complexity makes BSIM3SOI a slow model in circuit simulation, being more than 10 times slower than the regular BSIM3 model. This may lead to vendors using simpler models like BSIM3 for SOI purposes, trading off accuracy for speed [37]. In this work, in order to take advantage of the already done extraction of the CMOS 65nm bulk, BSIM4 model instead of BSIM3SOI has been used for modeling the SOI floating body NMOS. This model offers a better accuracy for sub 100nm transistors and millimeter wave frequencies but does not take into account the kink effect in DC simulation (cf. *Chapter I*).

II.7.2. BSIM4 model

The BSIM4 is based on BSIM3 but has a lot of improvements and modifications. The number of model parameters according to BSIM4 documentation [38] is over 300. Thus almost 700 parameters are needed to be defined for a scalable BSIM4 model. Many efforts have to be put on parameter characterization which is a slow process. The intention of the model is to reach accurately to even smaller dimension than BSIM3: the sub 100 nm channel length regime. Most notable improvements from the RF perspective are the gate resistance model options as well as the substrate resistance network as shown in *Figure II.19*. R_G resistance previously taken into account by an extrinsic models, for instance in BSIM3, has been absorbed into the core model description. An intrinsic input resistance, Rii, intended to better account for the NQS[2] effects is included. Also the Elmore resistor approach of BSIM3 is used along with a new transient charge-deficit NQS-model. The substrate resistance network is quite complex and the resistance values are scalable with the geometry. The parasitic source and drain series resistances can be described as extrinsic with a constant part and a

[2] Non Quasi Static in the literature

bias dependent part as in *Figure II.19*. The constant part is due to diffusion resistance. In general many features previously modeled by the extrinsic vendor models have been absorbed into the core model. In addition to the RF equivalent circuit improvements also a lot of efforts have been put to develop multifinger device geometry dependences.

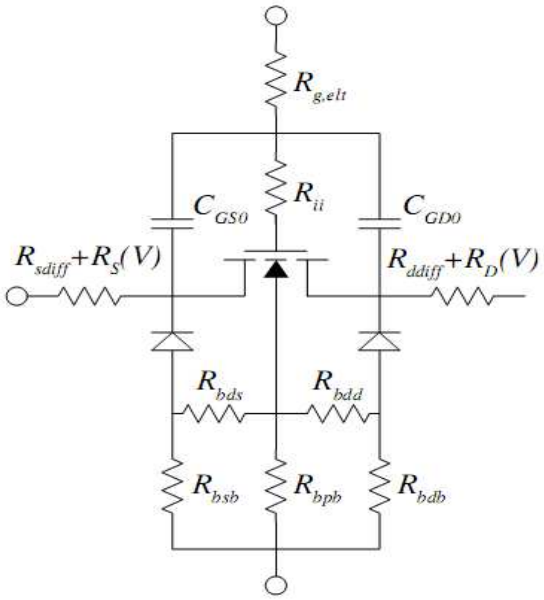


Figure II.19 Parasitic of the equivalent circuit of BSIM4

The drain conductance model is quite similar to BSIM3 but has some modifications to account for even smaller geometry effects. Also tunnelling from gate to other nodes is considered for oxide thicknesses below 3 nm where the effect is notable. The active charge model is similar to BSIM3v3. Also the zero-bias and fringe capacitance model is similar to the BSIM3v3 model except for the possible use of inner intrinsic gate resistance R_{ii} in *Figure II.19*. The zero-bias capacitances from gate to source and drain are connected from the outer side of R_{ii} instead of being in parallel with the intrinsic capacitances.

II.8. Summary

We have shown that at RF and millimeter wave frequencies, transistors are evaluated using the figure of merit f_T, f_{max} and NF_{min}. These figures are the expression of the ability to combine gain and low noise, two essential qualities to design analog millimeter wave circuits.

The MOSFET small signal model has been presented. The condition of validity of the model has been also discussed. From this model, noise sources of the MOSFET have been shown. These include thermal noise from parasitic resistances and induced gate noise. The noise temperature model has been studied. We have expressed the figure of merit f_T, f_{max} and NF_{min} from the non quasi static RF small signal model (*Figure II.2*)

We have exposed the millimeter wave performances of the SOI 65nm CMOS technology. The maximum f_T and f_{max} for the floating body and body contacted NMOS transistors are 155/200 GHz and 132/150 GHz respectively. The NF_{min} performance of the FB NMOS transistor is 3.5dB at 80GHz. In comparison with CMOS state of the art (*Table II.3*), the technology studied in this work has shown the best noise performance reported for CMOS devices. These results demonstrate clearly the potentiality of the CMOS technology for full-CMOS chips in applications from analog, RF, millimeter wave to digital.

This chapter has exhibited two modeling approaches with small signal and BSIM model. In this work both have been explored. In order to evaluate stability, gain, noise and matching the small signal model described in *II.2.2* has been used. For more complex design using various MOSFET geometries and biasing, the BSIM model from Berkeley University has been preferred.

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II.10. Appendixes:

A. RF gain definition

The general definition of the power gain is given by:

$$G = \frac{P_{out}}{P_{in}} \tag{2. 15}$$

The other gain definitions are given as follow:

The maximum stable gain:

Given a 2 x 2 scattering matrix, this measurement returns the maximum stable gain between the input and the measurement ports:

$$MSG = \left|\frac{S_{21}}{S_{12}}\right| = \left(\left|\frac{Y_{21}}{Y_{12}}\right| = \left|\frac{Z_{21}}{Z_{12}}\right|\right) \tag{2. 16}$$

Maximum available gain:

Given a 2 x 2 scattering matrix, this measurement returns the maximum available gain between the input and the measurement ports. This equation should be used in a stable system, i.e. when the stability factor (k) is greater than 1:

$$MAG = \left|\frac{S_{21}}{S_{12}}\right|\left(k - \sqrt{k^2 - 1}\right)$$

With (2. 17)

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}||S_{21}|} = \frac{2 \cdot \Re(Z_{11}) \cdot \Re(Z_{22}) - \Re(Z_{12}Z_{21})}{|Z_{12}Z_{21}|}$$

Unilateral power gain U :

The unilateral power gain is defined as the power gain of a two-port having no output-to-input feedback, with input and output conjugately impedance matched to signal source and load, respectively:

$$U = \frac{\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{2 \cdot \left(k \left|\frac{S_{21}}{S_{12}}\right| - \Re\left(\frac{S_{21}}{S_{12}}\right)\right)} \qquad (2.\ 18)$$

$$or \quad U = \frac{\left|Z_{21} - Z_{12}\right|^2}{2 \cdot \left(4 \cdot \Re(Z_{11}) \cdot \Re(Z_{22}) - \Re(Z_{12}) \cdot \Re(Z_{21})\right)}$$

The unilateral gain is used to define the figure of merit f_{max}. The maximum oscillation frequency is the frequency at which the unilateral power gain is equal to 1. When f_{max} can not be measured, it is extrapolated from the theoretical evolution of U (-20dB/dec).

Note:

Frequently f_{max} is not extrapolated from measured U, but from measured MAG or MSG. The U measurement is not always easy to exploit because of measurement noise. In this case, some authors use MAG or MSG. But when MSG is close to the frequency where k=1 the f_{max} can be overestimated [26].

Forward current gain H_{21}:

The forward current gain is defined as follow:

$$\left|H_{21}\right|^2 = \left|\frac{-2 \cdot S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}\right|^2 \qquad (2.\ 19)$$

The current gain is used to define the figure of merit f_T. The device f_T is the frequency at which the short circuit current gain falls to unity (0dB).

Associated Gain G_{ass}:

The associated gain G_{ass} is defined as the available gain under noise matching conditions.

$$G_{ass} = \frac{1 - \left|\Gamma_{opt}\right|^2}{\left|1 - \Gamma_{opt} \cdot S_{11}\right|^2} \cdot \left|S_{21}\right|^2 \cdot \frac{1 - \left|\Gamma_L\right|^2}{\left|1 - \Gamma_L \cdot \Gamma_{out}\right|^2} \qquad (2.\ 20)$$

$$with \quad S'_{22} = S_{22} + \frac{S_{12}S_{21}\Gamma_{opt}}{1 - S_{11}\Gamma_{opt}}$$

Generally G_{ass} is associated with the NF_{min} figure of merit in order to evaluate the low noise amplification ability of the transistor

B. Small signal model extraction and comparison with measurements

The following table gives an example of extracted elements for the device ZTM13 FB (n-MOSFET FB, 64x1x0.06µm².).

Ref device	V_{gs} (V)	Extrinsic								Intrinsic				T	
		R_g (Ω)	R_d (Ω)	R_s (Ω)	C_{cg} (fF)	C_{cd} (fF)	L_g (pH)	L_d (pH)	L_s (pH)	g_m (mS)	g_{ds} (mS)	C_{gs} (fF)	C_{gd} (fF)	T_{in} (K)	T_{out} (K)
ZTM13 FB	0.8	6.2	0.8	0.2	1.8	6	16	16	8	60	11	37	20	296	1338

Table II.4. Example of extracted elements of the small signal equivalent circuit

From these elements the equivalent circuit gives in *Figure II.2* can be used as RF model. The following figures give several comparisons between the extracted model and measurements:

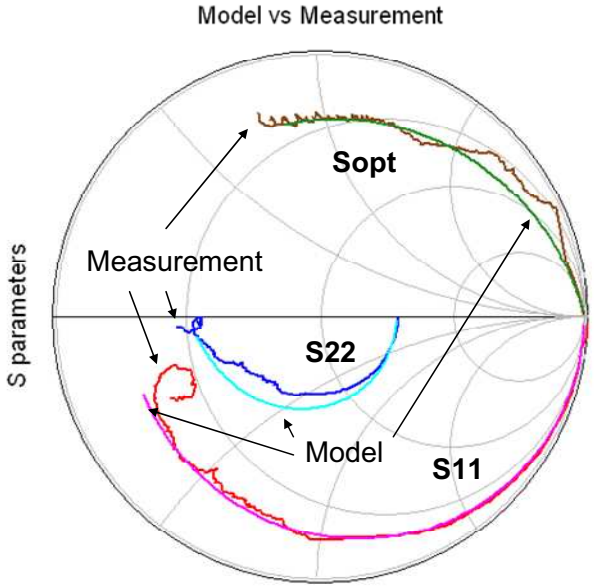


Figure II.20 Model versus measurement for input, Output S-parameters (0.5-110GHz) and Γ_{opt} (0.5-55GHz) ; Ids=350mA/mm, n-MOSFET FB, 64x1x0.06µm².

The model fits well the measurement over a wide bandwidth as shown in *Figure II.20*, *Figure II.21* and *Figure II.22*.

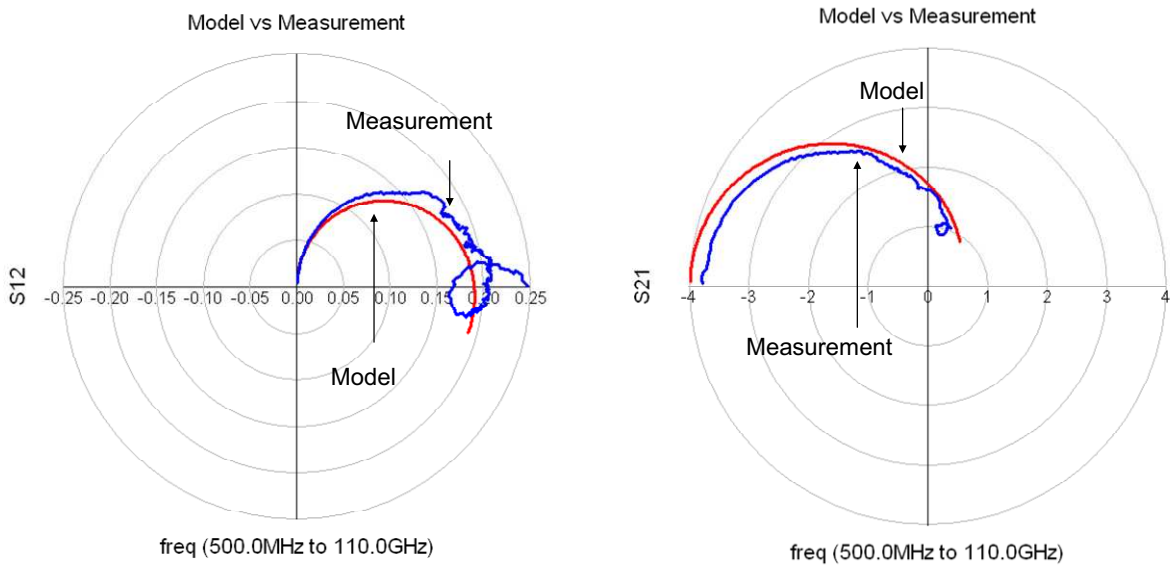


Figure II.21 Model versus measurement for S_{12} and S_{21}; Ids=350mA/mm; n-MOSFET FB, 64x1x0.06µm².

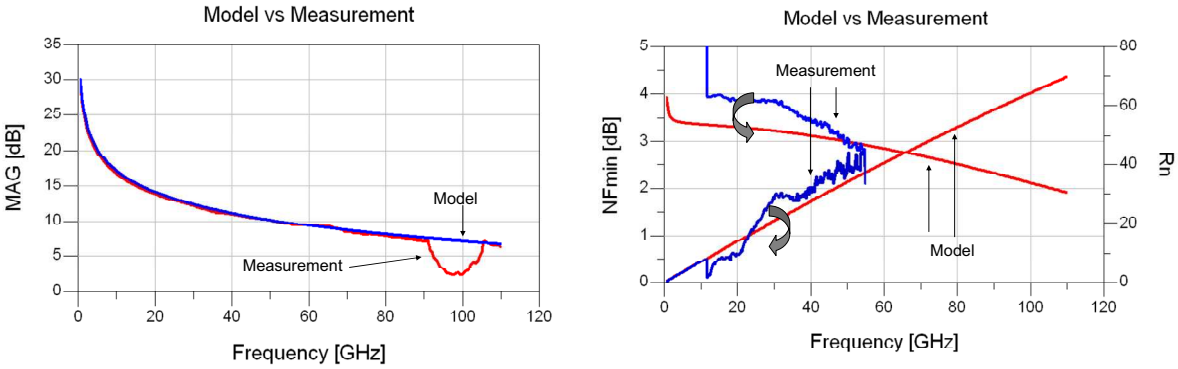


Figure II.22 Model versus measurement for MAG, NF_{min} and R_n; Ids=350mA/mm; n-MOSFET FB, 64x1x0.06µm².

This extracted model as been used in this work in order to evaluate stability, gain, noise and matching.

Chapter III

Passive elements in SOI CMOS 65nm

In this chapter, we review passive elements performances in SOI CMOS 65nm technology and see how they are modeled. Section III.1 discusses commonly used passive elements in RF and millimeter wave design. HR SOI substrate performances versus *bulk* are also highlighted. Section III.2 examines the characterization techniques used to evaluate passives elements. Section III.3 describes the common approach used to model on-chip spiral inductors and coplanar transmission lines. Analytical and measurement based model are presented.

III.1. Passive elements for RF and Millimeter wave frequencies

Passives elements in RF and millimeter wave frequencies are decisive design factors. Good active devices performances are nothing if passives elements have low figure of merit. In order to compare with other existing technology, we present passive elements for RF and millimeter wave design compliant with manufacturing rules.

III.1.1. States-of-the art passives elements in industrial silicon technology

Transmission lines[1] are key elements for millimeter wave design. Recent works have demonstrated the feasibility of such lines in digital BEOL[2] ([2], [12], [13] and [24]). The *Figure III.1* shows an evaluation of T-lines performances and *Table III.1 :* gives the 50Ω T-Lines description.

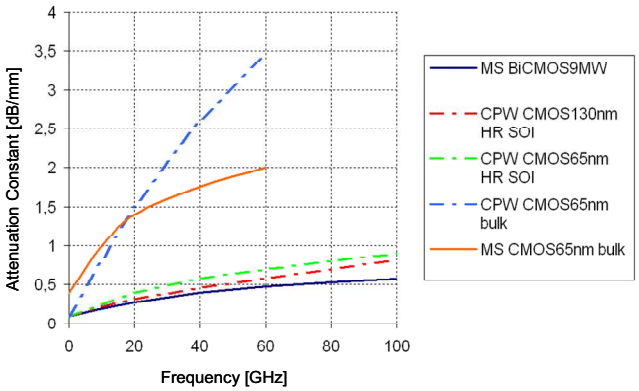


Figure III.1 Measured attenuation constants for 50Ω transmissions lines in different technologies (all lines are compliant with manufacturing design rules)

Reference lines	MS BiCMOS9MW	CPW CMOS130nm HR SOI	CPW CMOS65nm HR SOI	CPW CMOS65nm	MS CMOS65nm
Technology	BiCMOS (Millimeter wave dedicated): - 6 metal levels - 3 thick	SOI CMOS 130nm (Pure digital): - 6 metal levels - 1 thick	SOI CMOS 65nm (Pure digital): - 6 metal levels - 1 thick	CMOS 65nm (Pure digital): - 6 metal levels - 1 thick	CMOS 65nm (Pure digital): - 6 metal levels - 1 thick
Substrate	Low Resistivity	High Resistivity	High Resistivity	Low Resistivity	Low Resistivity
Line type	Microstrip	Coplanar	Coplanar	Coplanar	Microstrip
Size	Conductor width: 5µm (M6+Alu) Distance to ground (M1+M2), h=8.4µm	Conductor width: 26µm (M1 to Alu) Space to ground (M1 to Alu) s=22µm	Conductor width: 12µm (M1 + Alu) Space to ground (M1 to Alu) s=5µm	Conductor width: 12µm (M6 + Alu) Space to ground (M1 to Alu) s=6µm	Conductor width:5µm (M6) Distance to ground (M2) h=1.78µm

Table III.1 : 50Ω T-Lines characteristics

[1] T-Line in literature
[2] Back End Of Line in the literature

When moving from one CMOS node to the next, there is a vertical shrink of the BEOL together with a decreasing of the metal and dielectric thickness and of the metal pitch in order to increase integration density. Thus, coplanar wave guide designed in CMOS 65nm suffer from substrate proximity (*Figure III.1*).

It is difficult to benchmarked performances of passives lumped elements because the result is both influenced by the technology and the geometry. Nevertheless, latest results in CMOS technology [25] show 2-4 nH inductors with quality factor of ~10 for CMOS and ~15 for SOI HR CMOS. Small value (Bi)CMOS inductors (50-250pH), suitable for millimeter wave design, have been measured with quality factor of 10 to 25 [8].

Density results for RF capacitors using standard metal layers of the BEOL CMOS 65nm and SOI CMOS 65nm core process show 1.84fF/µm² and 2.27fF/µm² respectively [10].

III.1.2. Interconnects in 65nm SOI CMOS technology

The SOI CMOS 65nm technology is derived from 65nm node. Like the other SOI technologies, this one is distinguished by the presence of a buried oxide[3] allowing use of the high resistivity substrate (HR substrate). The back end of line is composed of 6 or 7 copper metal layers (depending on the option) and a last encapsulated aluminum layer[4]. In this work, all results come from the 6 metal levels option. The *Figure III.2* describes this structure.

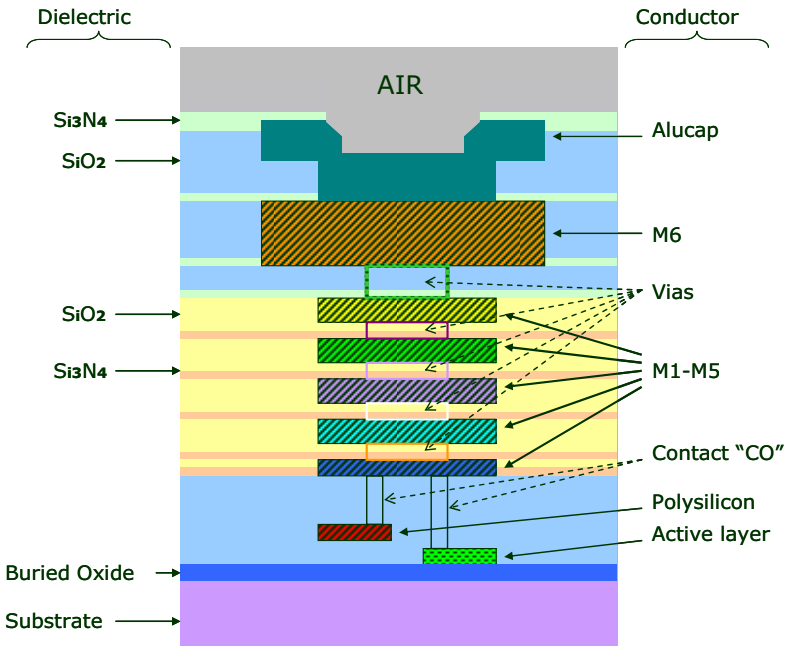


Figure III.2 Structure of the SOI CMOS SOI 65nm

[3] BOX in the literature
[4] ALUCAP or AP in the literature

The structure is made up of 5 thin copper levels (M1 to M5), a thick copper level (M6) and a last aluminum level (ALUCAP). The method of copper deposition is the damascene one, which is based on the principle of trenches which are filled by metal. Once the operation carried out, the CMP[5] allows leveling each metal level. Each (inter-metal) layer is made up of silicon dioxide (SiO_2) and of silicon nitride (Si_3N_4) being used to limit the diffusion of copper in the oxide. In this technology the substrate has a resistivity larger than $3K\Omega.cm$.

III.1.2.a. Multi-layer constraints of integration

As we have just seen it, the operation of CMP polishes the metal levels in order to avoid any risk of short-circuits or open-circuits [1]. However this operation of flattening is only possible if the densities of metal are homogeneous. This implies that the full metal drawing or the absence of metal on a large surface is not possible. Thus, the levels of metallization must be perforated if their size is too important and some small tiles of dummy metal must be placed to preserve the homogeneity of density. It should be noticed that these rules of densities follow the projection of the technologies in the future [2]. These constraints will be moreover more severe (smaller control windows).

The *Figure III.3* illustrates some of the rules of design on one metal level.

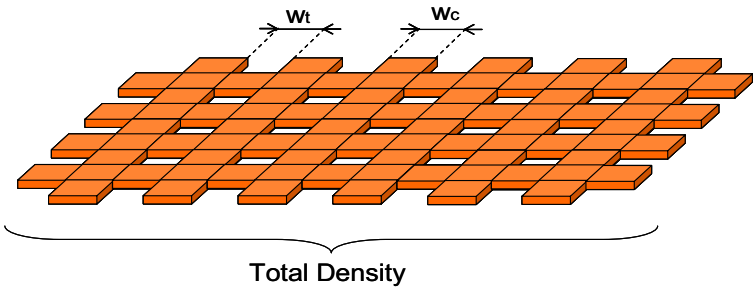


Figure III.3 Example of a metal layer design rules

Among the rules to be respected on one metal level, let us quote *inter alia*:

- The minimum and maximum density (in general between 20 and 80%)
- The minimum size of a hole in metal (W_T, *Figure III.3*)
- The minimum and maximum width of a metal stripe (W_C, *Figure III.3*)

III.1.3. Lumped or distributed circuit elements ?

One of the key elements for the design of circuits in high frequency is the choice of the passive elements which will be used for various impedance matching. To perform this operation, two choices are possible: lumped components (capacitor, inductor, etc) or

[5] Chemical Mechanical Polishing

distributed components such as waveguide lines (microstrip, coplanar, etc). This choice answers several criteria:

- Working frequency
- The self resonant frequency of the component[6]
- The current density to drive

All these criteria depend on the geometry of the component and are interdependent. For all of then, a major criterion is the occupied chip area.

III.1.3.a. Working Frequency

A component in a circuit is known as lumped when electrical signal path time from one point to another in the component can be neglected. In this case, the voltage and the current are not dependent on time and in position. In order to determine if a component can be looked as lumped one it is suitable to compare the size of the component with the wavelength. Usually the following rules of thumb are used:

If: $\frac{d.\sqrt{\varepsilon_r}.freq}{c} < 0{,}01$ then the element can be seen as definitely lumped.

If: $\frac{d.\sqrt{\varepsilon_r}.freq}{c} > 0{,}1$ then the element can be seen as definitely distributed.

With d the largest dimension of the component, ε_r the permittivity of the dielectric where the component is implemented and c the light celerity. The following graph illustrates the rules stated before for $\varepsilon_r = 4$:

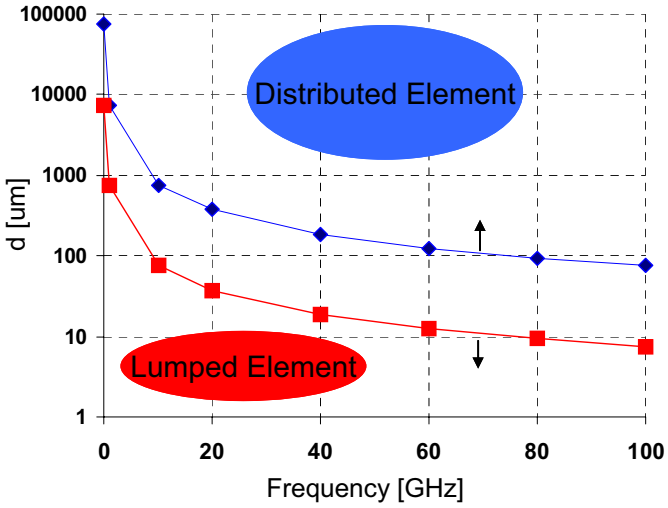


Figure III.4 Simulation behavior of an element according to its dimension and the frequency

[6] SRF in the literature

The *Figure III.4* shows that a circuit element could not be used as lumped element if its behavior is that of a distributed element.

III.1.3.b. Self Resonant Frequency

Passive components cannot be considered as strictly capacitive, inductive or resistive at millimeter wave frequencies. Indeed, each one of these components is associated to a RLC network. From this network it is possible to calculate the self resonant frequency of a component (f_0):

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \quad \text{(Hz)} \tag{3. 1}$$

Below this frequency, the component has a given behavior (capacitive, inductive, resistive…) but beyond the component cannot be used any more like that. As an example, the following figures show the behavior of a capacitance and an inductance versus the frequency:

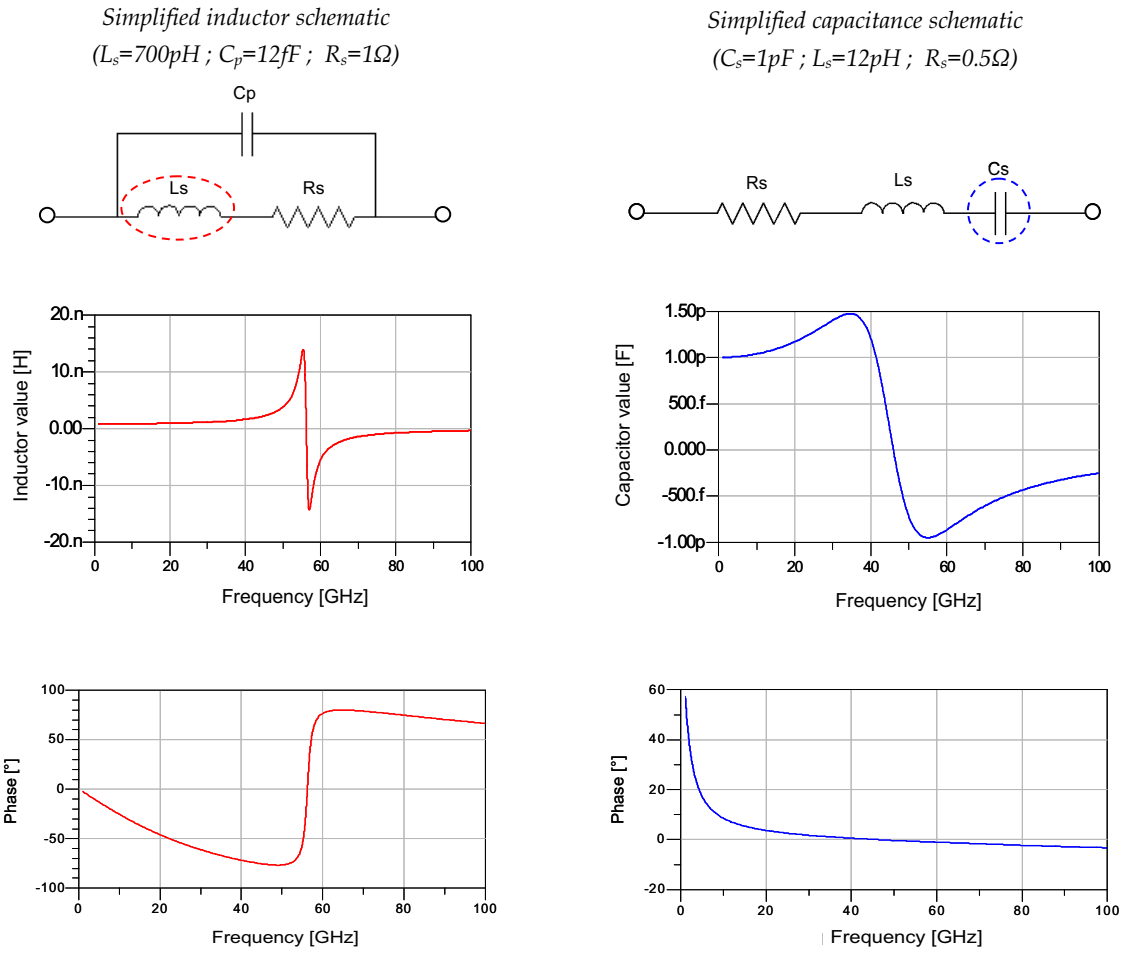


Figure III.5 Frequency dependant behavior of a capacitance and an inductance

The low self resonant frequency of a circuit element may force the designer to use a distributed element solution, and this trend is reinforced in the millimeter wave frequency band.

III.1.3.c. Current Density

To respect the current density rules it is not always possible to optimize the dimensions of passive circuit elements to respect lumped condition as explained in the above paragraph. Indeed we saw that the behavior of a circuit element (distributed/lumped) is determined by its geometrical dimensions and the working frequency. To illustrate the geometrical dependence of a metallic line with respect to the current, the following graph shows the evolution of the DC and RMS maximum current density in a metal level (M1 to M5) for the given temperature of 80°C.

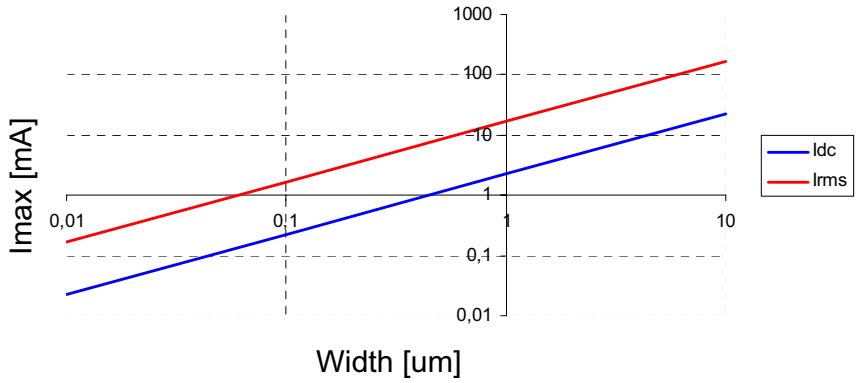


Figure III.6 Maximum current density according to the conductor width at 80°C

As shown in the graph, the current density necessary for a given circuit application often constrains the design. This is particularly true for applications such as power amplifiers.

III.1.4. Inductors in SOI CMOS technology

There are various topologies of inductances presented in the literature [3]. In this chapter we are interested in inductances called on- chip spiral[7] inductors. They are composed of one or more metal layers connected together, drawing a spiral above the substrate. These inductances are most largely used in the industry of microelectronics, particularly in RF[8] applications. As detailed at the beginning of this chapter, in SOI, the substrate is composed of a buried oxide on the top of a high resistivity silicon layer.

[7] Here spiral term is used for squares, hexagonal, octagonal and circular inductors.
[8] Radio Frequency lower than 10 GHz in the literature

III.1.4.a. SOI Inductors for RF applications

In order to understand the high frequency electromagnetic mechanisms, the following figure represents a simple square inductance and its electrical lumped model[9].

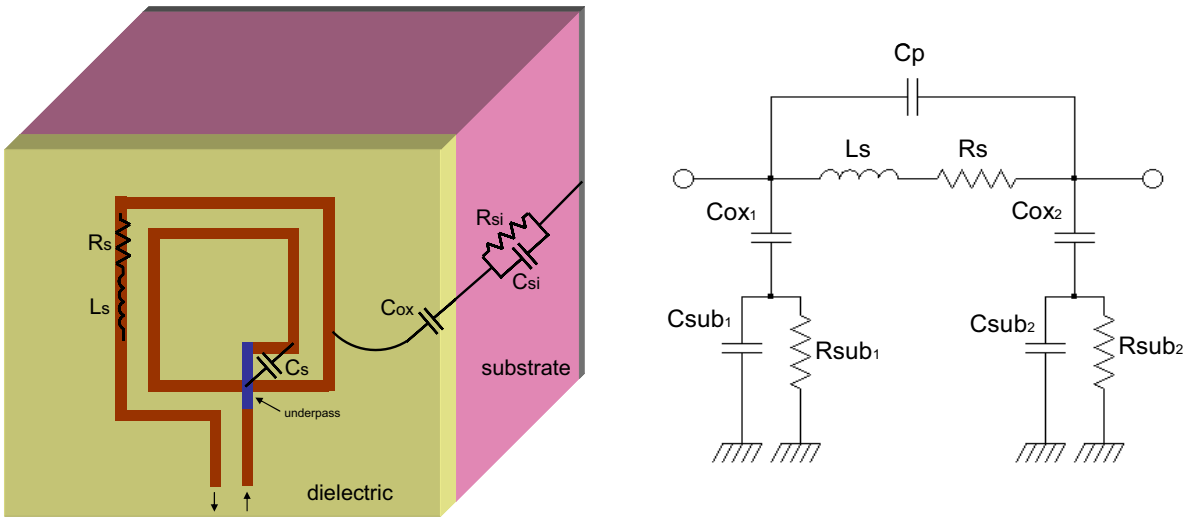
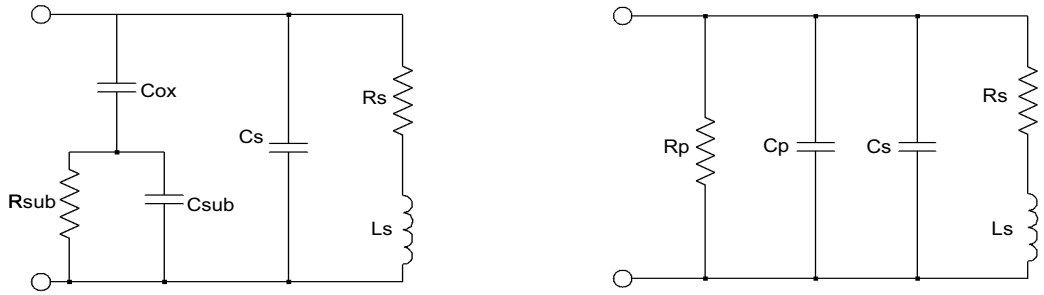


Figure III.7 Inductor representation and schematic model

It is possible to express the quality factor of this type of inductor according to the elements of its 2 ports equivalent circuit [4]. When one port is connected to the ground (*Figure III.8*), the energetic equivalent circuit is the following:



a) *b)*

Figure III.8 a) Simple equivalent circuit of an inductor with one port connected to the ground – b) equivalent energy model

The definition of the quality factor of an inductive element is given by:

$$Q = 2\pi \frac{Peak\ magnetic\ energy - Peak\ electric\ energy}{Energy\ loss\ in\ one\ oscillation\ cycle} \quad (3.\ 2)$$

From the energy equivalent model of the inductor, the values of the energy stored and lost in the inductor are:

[9] Generic model for spiral inductors

$$E_{E\max} = \frac{V_0^{\,2} C_0}{2} \tag{3. 3}$$

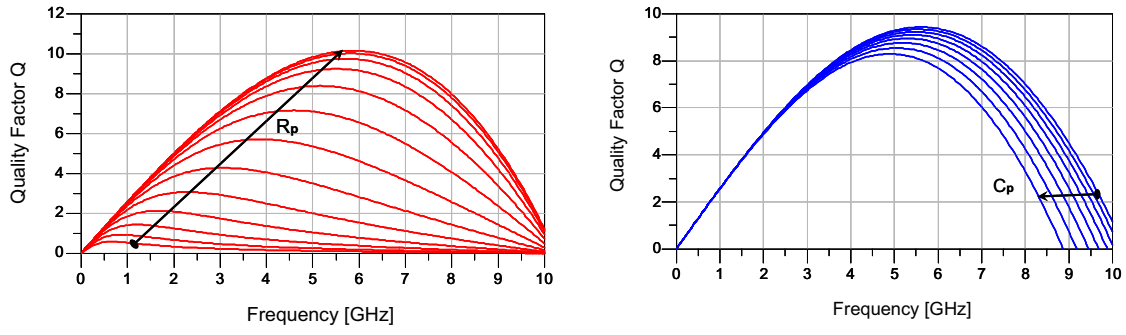
$$E_{M\max} = \frac{V_0^{\,2} L_s}{2 \cdot \left((\omega . L_s)^2 + R_s^{\,2} \right)} \tag{3. 4}$$

$$E_{loss} = \frac{2\pi}{\omega} \frac{V_0^{\,2}}{2} \cdot \left[\frac{1}{R_p} + \frac{R_s}{(\omega L_s)^2 + R_s^{\,2}} \right] \quad with \quad C_0 = C_p + C_s \tag{3. 5}$$

$E_{E\ max}$, $E_{M\ max}$ and E_{loss} are the peak electric energy, the peak magnetic energy, and the energy losses respectively. From the previous equation, the quality factor can be express as:

$$Q = \frac{\omega L_s}{R_s} \times \frac{R_p}{R_p + \left(\left(\frac{\omega L_s}{R_s} \right)^2 + 1 \right) R_s} \times \left(1 - \frac{R_s^2 C_0}{L_s} - \omega^2 L_s C_0 \right) \tag{3. 6}$$

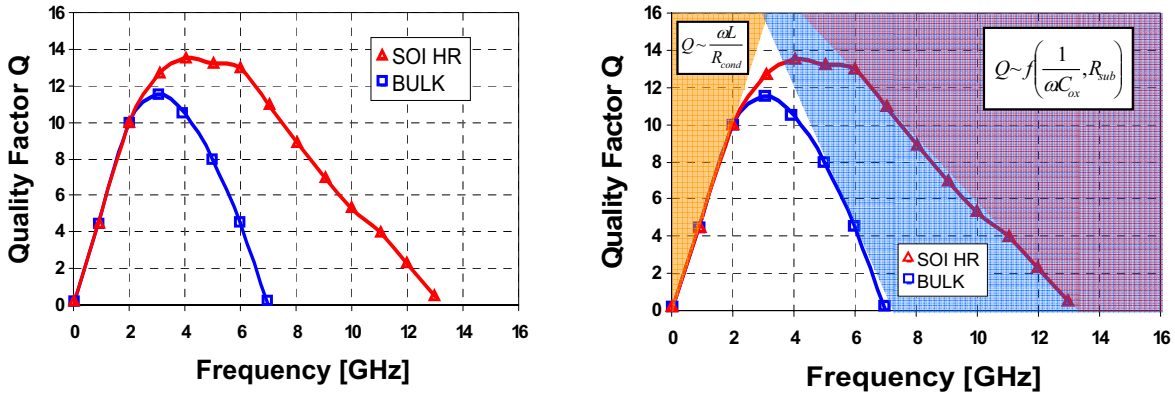
Where $\omega L_s / R_s$ is the stored magnetic energy, the second term represents the losses in the substrate, and the third is the self resonance frequency which describes the reduction of Q when the frequency is close to the resonant frequency. For inductances made on SOI substrate, the profit obtained on the quality factor Q is linked to the second term since the other elements of the expression are related to the shape ratio of the inductance metallization. Note that the values L_s and R_s are common to bulk and SOI technologies, but the SOI technology is distinguished with the value of R_p, definitely higher and a smaller value of C_p. Indeed R_p represents the resistivity of the substrate and C_p is influenced by the buried oxide and the high resistivity of the substrate, contributing thus to the reduction of its value. The following figures show the evolution of the Q according to the variations of the values of R_p (from 10Ω to 10KΩ) and C_p (from 10 to 50fF) for an inductance of 2nH:



a) *b)*

Figure III.9 Simulated evolution of the quality factor according to the frequency for a variation of the R_p value (from 10Ω to 10KΩ) (a) and C_p values (from 10 to 50fF) (b)

Some measurements performed on two inductances made on SOI and bulk and optimized for a frequency of 2.4 GHz illustrate the above demonstration [5], [9] :



a) *b)*

Figure III.10 *(a) Quality factor of a 2.4nH inductance on SOI HR and bulk, (b) illustration of the behavior of the Q factor*

As predicted in the above paragraph, the Q factor increases in SOI (+20%) thanks to a higher value of R_p. The self resonant frequency is also pushed away (+80%) due to the decreasing of C_p [6].

An additional benefit from HR SOI is the area reduction. High resistivity substrate allows using all metal levels (including metals close to the substrate) because at fist order there are no substrate losses. Therefore, there is 40 % lower area with HR SOI, for a given Q factor inductor [7]. The following figure illustrates the possible area reduction by using HR SOI.

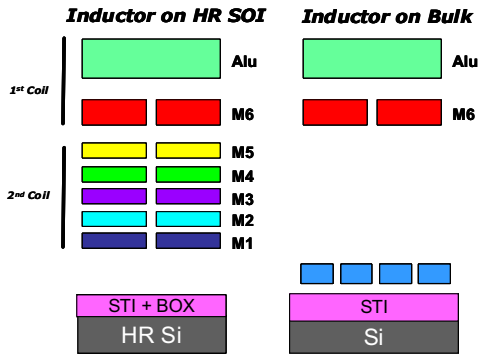


Figure III.11 *BEOL used for inductance in bulk and SOI*

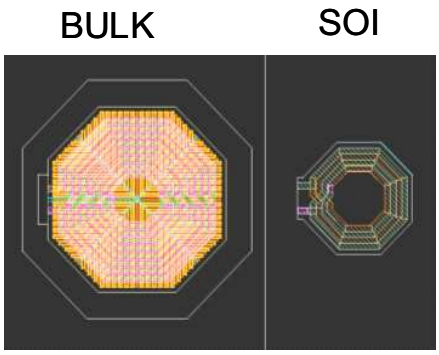


Figure III.12 *layout of same value inductors with a given Q in bulk and SOI*

III.1.4.a.i Inductance with patterned ground shield (PGS)

For an inductance made above a patterned ground shield[10] the losses in the substrate are strongly attenuated since the ground shield masks the substrate. On the other hand the presence of the conducting plane increases artificially the value of the oxide capacity. Indeed, this one is proportional to the ratio of the inductance area over the oxide thickness between the ground shield and the inductance.

Even if the PGS enables the improvement of the quality factor, it does not allow carrying out inductances as good as on SOI substrate. In fact, increasing C_{OX} capacitance impact the term C_0 (3. 5) contributing to the reduction of the Q factor.

III.1.4.b. Millimeter Wave Inductance

Inductance quality factor made on silicon is determining by the losses in the substrate and the resistance of the conductor (R_{cond}) [7]. As explained previously, the high resistivity substrate in SOI enhances reduction of the losses in the silicon substrate but in millimeter wave frequency, HR substrate presents a second advantage.

In order to reduce the losses related to the metal resistivity, the logic in RF design consists in using the widest possible conductor and several stacked metals. Although this method is effective to reduce serial resistance, it increases the oxide and substrate parasitic capacitances (C_{ox} and C_{sub}) which are proportional to the area of the inductance. In addition to increasing the losses, these capacitances decrease the value of the self resonant frequency (SRF). Since inductances are generally used around the maximum value of the Q factor, which is at frequencies much lower than the SRF, this method cannot be used at the millimeter wave frequencies. For a use at such frequencies, one solution consists in reducing the width of the conductor to decrease the capacities [7]. However this solution has two problems: serial resistance strongly increases *(3. 7)* and the maximum current density decreases.

$$r_{cond} = \sqrt{{r_{DC}}^2 + {r_{HF}}^2} \quad [\Omega.m^{-1}] \tag{3. 7}$$

with $r_{DC} = \dfrac{l}{w.t.\sigma}$ [Ω.m^{-1}] and $r_{HF} = \sqrt{\dfrac{2\pi.freq.\mu_0}{2.\sigma}}\dfrac{l}{2.w+2.t}$ [Ω.m^{-1}]

$l = length$
$w = width$
$t = thickness$
$\sigma = conductivity$
$\mu_0 = 4.\pi.10^{-7}$

[10] PGS in the literature

The substrate equivalent capacitance is strongly reduced by using SOI HR substrates. As in RF design, this property allows increasing the Q factor but it also helps to have inductances of wider area for the same resonance frequency or enables using all the metal layers available. As explained in the first part, this is an advantage for the applications which require large current densities (LNA[11], PA[12]).

Here, as previously, SOI substrate provides great benefit. The following figures show inductances for millimeter wave frequencies simulated on a BULK and SOI substrate.

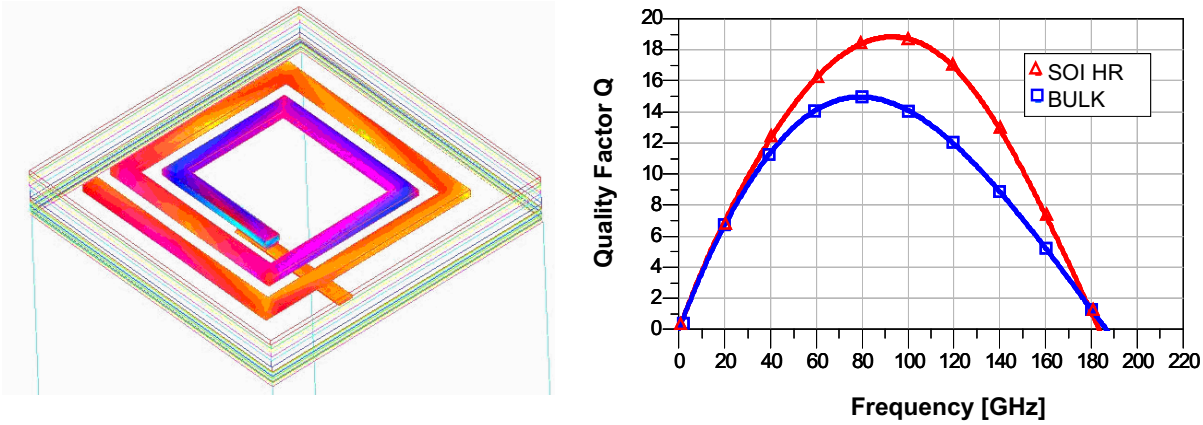


Figure III.13 MOMENTUM[13] simulation of a 200pH (w=2µm)inductor on BULK and HR SOI substrate

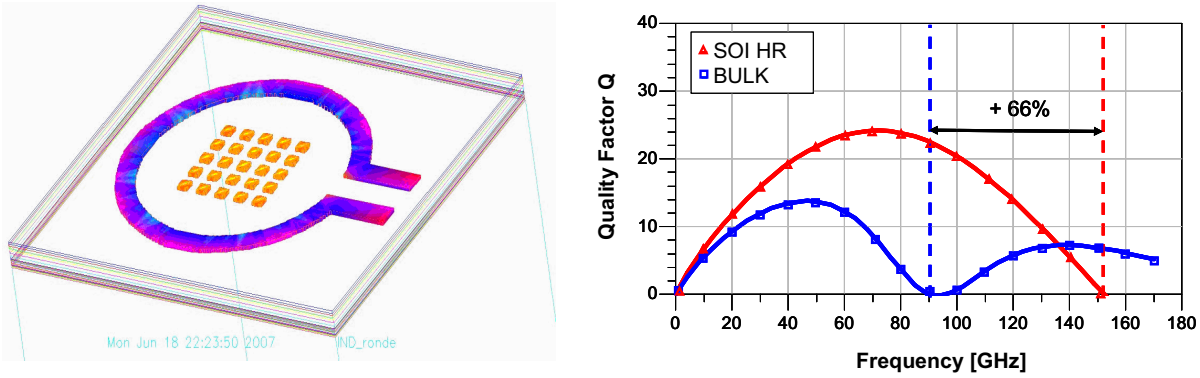


Figure III.14 MOMENTUM simulation of a 136pH (w=6µm) inductor on BULK and HR SOI substrate

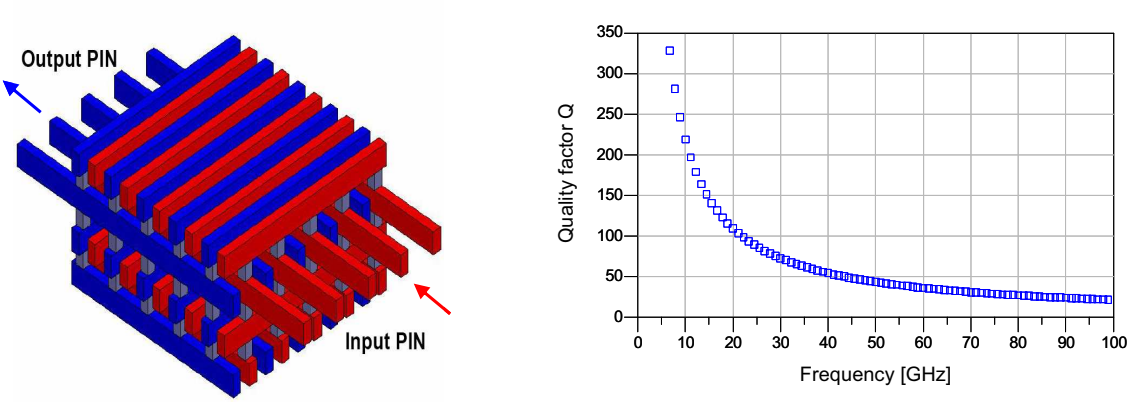
These two simulations illustrate the gain which is possible to obtain thanks to the HR SOI for inductances at millimeter wave frequencies.

[11] Low Noise Amplifier
[12] Power Amplifier
[13] MOMENTUM: Electromagnetic simulator software from Agilent (*cf. III.2.2*)

III.1.5. MOM Capacitor in SOI CMOS technology

MOM capacitors are "free" capacitance building by using standard metal layers of the BEOL in core process. High performance capacitors are required to implement RF and millimeter wave circuits. The main requirements are capacitance density, symmetry and high quality factor. By using HR SOI two of above requirements can be emphasized. The increase in substrate resistivity results in higher Q for capacitors [9]. In addition, in HR SOI the pattern ground shield is not required thus the density structure is increased (+23% in compare with bulk, 2.27fF/µm² [10]).

In order to increase the SRF (cf. *III.1.3.b*) a specific layout is used called woven structure. This MOM is described in *Figure III.15* :



a) *b)*

Figure III.15 RF MOM capacitor from STMicroelectronics (a) , Simulated quality factor of a 1pF RF MOM (b)

The woven structure allows very high SRF while having good density (2.27fF/µm²). As shown in *Figure III.15 b)* the quality factor ($Q = Imag(Y_{11})/Real(Y_{11})$) of such capacitors is steel high at millimeter wave frequencies.

III.1.6. Waveguide components on silicon substrate

III.1.6.a. Transmission Lines

The transmission line equivalent circuit represents the transmission line as an infinite series of two-port elementary lumped components, each representing an infinitesimally short segment of the transmission line (*Figure III.16*)

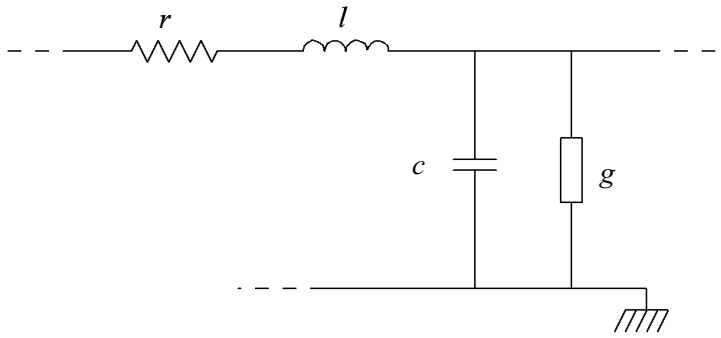


Figure III.16 Equivalent circuit of a TEM line

The distributed resistance *r* of the conductors is represented by a series resistor, the distributed inductance *l* is represented by a series inductor, the capacitance between the two conductors is represented by a shunt capacitor *c* and the conductance of the dielectric material separating the two conductors is represented by a conductance *g* shunted between the signal wire and the return wire.

The model consists of an infinite series of elements shown in the *Figure III.16* , and each component is specified per unit length. If *r* and *g* are not neglected, the characteristic impedance is:

$$Z_c = \sqrt{\frac{R + jL\omega}{G + jC\omega}} \quad [\Omega] \tag{3. 8}$$

The propagation constant for lines with losses, taking into account the resistance along the line as well as the resistive path between the conductors is:

$$\gamma = \sqrt{(R + jL\omega)(G + jC\omega)} \tag{3. 9}$$

$$\gamma = \alpha + j\beta$$

The complex part of the complex propagation constant is the phase constant β:

$$\beta = \frac{2\pi}{\lambda_d} \quad [\text{rad.m}^{-1}] \quad \text{with} \tag{3. 10}$$

$$\lambda_d = \frac{\lambda_0}{\sqrt{\varepsilon_r}} \; ; \; \lambda_0 = \frac{c}{freq} \; [\text{m}] \quad \text{and} \quad c = \sqrt{\mu_0.\varepsilon_0} \approx 2.998.10^8 \; [\text{m.s}^{-1}]$$

The phase velocity is:

$$V_\varphi = \frac{\omega}{\beta} \quad [\text{m.s}^{-1}] \tag{3. 11}$$

In silicon technology, the attenuation constant can be split into three components, one representing metal losses, one representing dielectric losses due to loss tangent and the last one the losses due to substrate conductivity (stray radiation is neglected):

$$\alpha = \alpha_c + \alpha_d + \alpha_g \tag{3. 12}$$

The metal losses vary in most cases at $\sqrt{freq}$. This frequency dependency is due to finite conductivity of metals, and skin effect. Losses due to metal conductivity (α_c) are:

$$\alpha_c = 8.686 \cdot 10^{-3} . \frac{\sqrt{r_{DC}^2 + r_{HF}^2}}{2.Z_0} \quad [\text{dB.mm}^{-1}] \tag{3. 13}$$

with r_{DC} et r_{HF} coming from (3. 7)

Attenuation due to the dielectric loss tangent is proportional to frequency as given in (3. 14).

$$\alpha_d = 27{,}3 \cdot 10^{-3} \cdot \frac{\varepsilon_r}{\sqrt{\varepsilon_{reff}}} \frac{\varepsilon_{reff} - 1}{\varepsilon_r - 1} \frac{\tan\delta}{\lambda_0} \quad [\text{dB.mm}^{-1}] \tag{3. 14}$$

$$\tan\delta = \frac{\sigma}{\omega\varepsilon} = \frac{\varepsilon''}{\varepsilon'} \quad \text{and} \quad \varepsilon = \varepsilon_0 \varepsilon_r = \varepsilon' + j\varepsilon'' \tag{3. 15}$$

Attenuation due to substrate conductivity (α_g) is not a function of frequency. A generic equation for this loss mechanism is:

$$\alpha_g = 8.686 \cdot 10^{-3} . \frac{G.Z_0}{2} \quad [\text{dB.mm}^{-1}] \tag{3. 16}$$

Taking into account the substrate conductivity of a multilayered technology, the electrical model of a transmission line given in *Figure III.16* becomes:

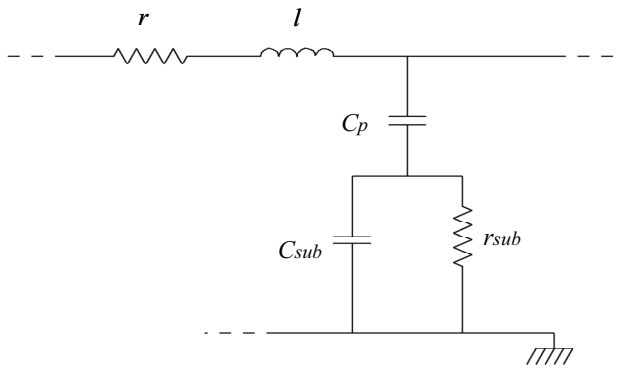


Figure III.17 Lumped physical model of transmission line on silicon

In this model the c, g network is replaced by a capacitance C_p in series with a parallel RC network modeling the substrate.

III.1.6.b. Thin Film Microstrip Line

The microstrip line is represented in *Figure III.18 ;* it is made up of a conducting strip on a dielectric in parallel to a ground plane. In silicon technology, the conducting strip is separated from the ground plane by one or several inter-metal dielectric[14]. The electric and magnetic fields are orthogonal in the transverse plane (*Figure III.19).*

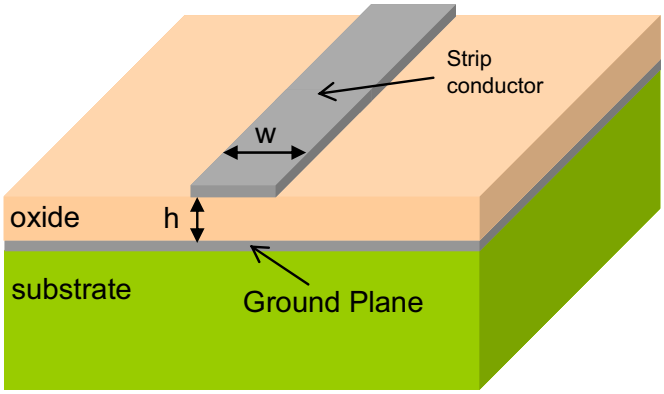


Figure III.18 Silicon thin film microstrip line

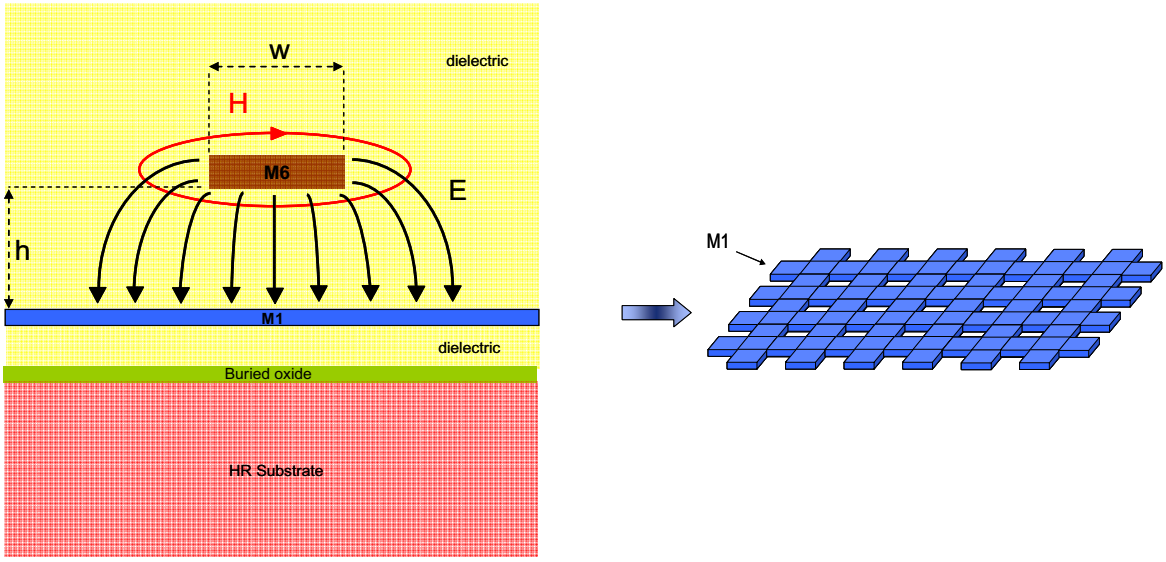
The characteristic impedance of a microstrip line depends on its dimensions and the type of dielectric which surrounds it. In the case of 65nm CMOS technology the only degree of freedom to vary the characteristic impedance are the width of the line and the choice of the metallization (M1 to M6) layers. However, to make microstrip lines in CMOS technology, the choices of width and height are also constrained by the technology design rules (cf. III.1.2.a.). Figure III.19 illustrates the realization of a microstrip line using as conducting strip the top metal level (M6) and the bottom metal level (M1) as ground plane. As explain on III.1.2.a a full plane cannot be carried out. Taking into account density rules, the ground plane is made as a wired mesh. The behavior of this plane is nearly identical to a full plane since the "holes" carried out in metal are smaller than the signal wavelength for frequencies lower than 100GHz *(Figure III.4).*

In a microstrip line made on silicon technology, the propagation of the electromagnetic field is either done in the substrate or in the air; the structure is thus none homogeneous. The mode of propagation cannot thus be TEM[15]. However as the longitudinal fields magnitudes

[14] Generally made of silicon dioxide (SiO_2) and a small layer of silicon nitride (Si_3N_4)

[15] TEM: Transverse Electromagnetic Mode. Non-dispersive mode without cut-off frequency where the magnetic fields and electric do not have longitudinal components (E_Z=H_Z=0).

are negligible, the approximation quasi-TEM can be made. Because the line features only two metal conductors, only one mode of propagation is possible.



a) *b)*

Figure III.19 *a) microstrip line – b) ground plane zoom*

The *Figure III.20* summarizes the performances which it is possible to reach with the described microstrip line (*Figure III.19*). The range of characteristic impedances extends from 25Ω to 100Ω with losses of 3dB/mm for a 50Ω characteristic impedance line at 80GHz.

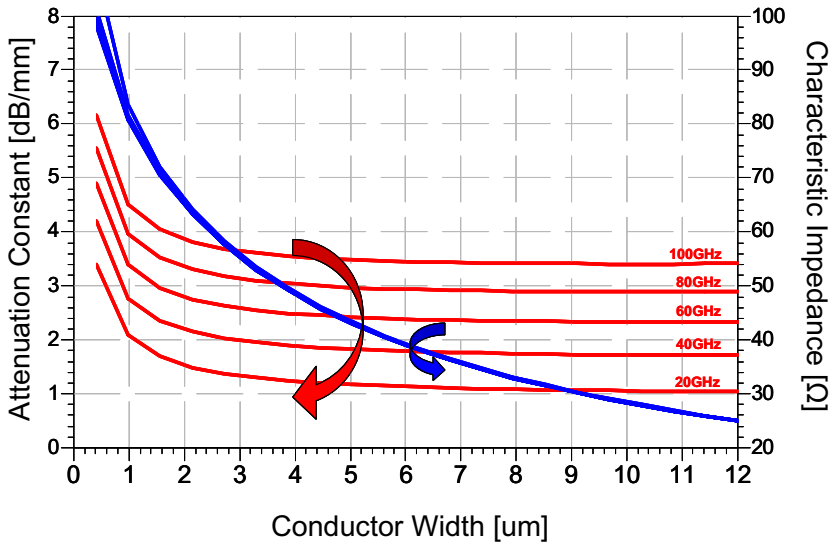


Figure III.20 *MOMENTUM simulation of a microstrip line made with top metal level(M6)*

As explained in *III.1.6.a*, the attenuation constant of a transmission line in silicon is the sum of the losses due to metal and substrate conductivity. For a microstrip line the losses due to substrate do not exist since the ground plane masks this one preventing the

penetration of electro-magnetic field. In order to reduce the losses, the only degree of freedom thus remains on metallization thickness (if the skin depth[16] is higher than the conductor thickness) and the width of the microstrip conductor. However taking into account the design rules (cf. *III.1.2.a*), in order to keep a wide range of characteristic impedances, the only option thus consists in using the last thick metal level (M6) to reduce the series resistance. *Table III.2 :* summarizes the performances of the microstrip line in SOI CMOS 65nm:

Metallization	**Z_c min (Ω)**	**Z_c max (Ω)**	**$\alpha_{30\Omega}$ @ 80 GHz (dB.mm^{-1})**	**$\alpha_{50\Omega}$ @ 80 GHz (dB.mm^{-1})**	**$\alpha_{70\Omega}$ @ 80 GHz (dB.mm^{-1})**
Metal 6	25	100	3	3	3.5

Table III.2 : Performances of the SOI CMOS 65nm microstrip line.

To conclude, the microstrip line covers a broad range of characteristic impedances with losses about 3dB/mm at 80GHz. Taking into account the presence of the ground plane, these performances do not depend on the type of the substrate (HR or not) and are thus identical in standard CMOS technology.

III.1.6.c. Coplanar Waveguide

The coplanar wave guide[17] shown on *Figure III.21* is formed by a conductor surrounded by a pair of ground planes, all on the same plane, at top of a dielectric medium (silicon and silicon dioxide). In the ideal case, the thickness of the dielectric is infinite. A variant of coplanar waveguide is formed when a ground plane is provided on the opposite side of the dielectric, which is called grounded coplanar waveguide (CPWG). In CMOS 65nm technology CPWG are difficult to use since they offer a capacitive behavior (small oxide thickness).

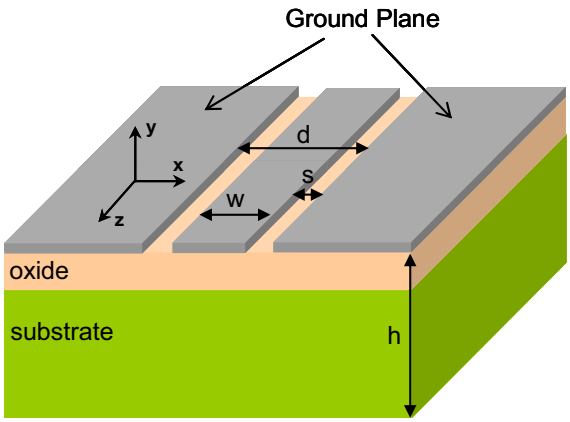


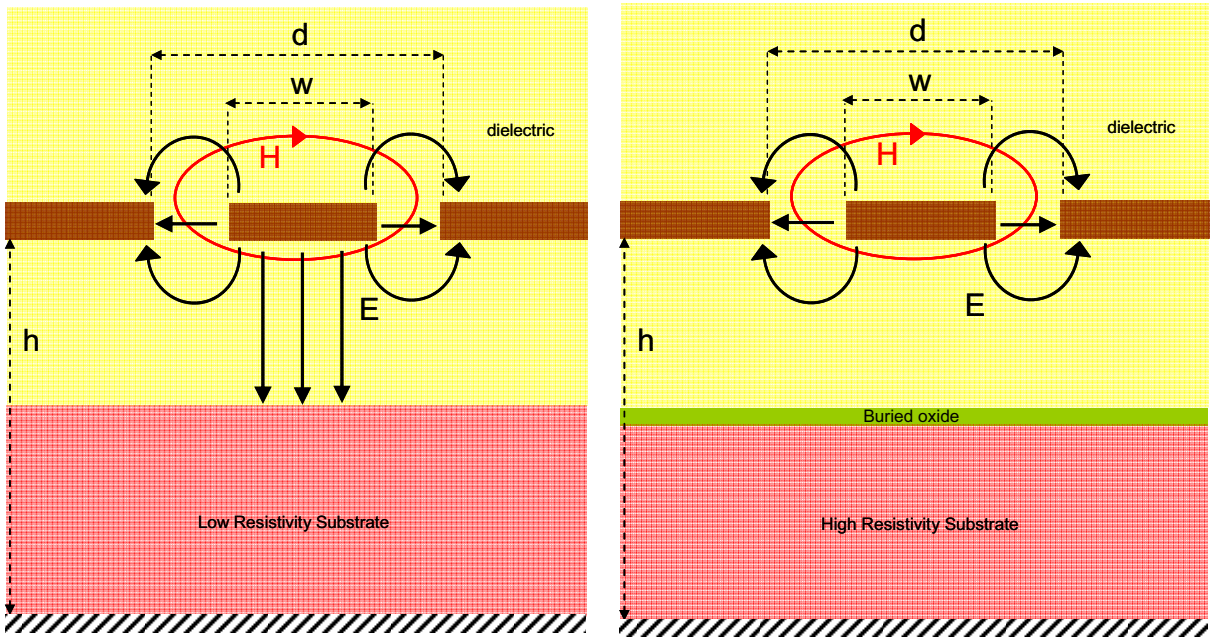
Figure III.21 silicon coplanar wave guide

[16] When a conductor carries current at high frequency, the electric field penetrates the outer surface only about one skin depth so that current travels near the surface of the conductor.
[17] CPW in the literature

The electric and magnetic fields are orthogonal in the transverse plane (*Figure III.22 .a*). The CPW can support the even mode of propagation Quasi-TE and odd mode quasi-TEM called coplanar mode. In the even mode, the electric field is propagated between the two ground planes. It occurs in particular in the presence of a discontinuity (junction, corner…). To avoid this phenomenon, it is necessary to place some underpasses to bring back ground plane sides to the same electrical potential and it is also advisable to observe the following conditions [22]:

$h < 0.12\lambda_d$, with λ_d wave length in substrate (cf. (3. *10)*) , h the total dielectric height and d the inter-ground distance (*Figure III.21*) (3. 17)

$d << w_g$; $d << h$ and $d < \frac{\lambda_d}{10}$, with w_g the width of the ground plane (3. 18)



a) *b)*

Figure III.22 Electrical end magnetic fields behavior on bulk substrate (a) and SOI HR (b)

Unlike the microstrip lines which are formed only on top of the chip, the performances of coplanar lines depend on the substrate used. Indeed the conductivity of this one directly influences the losses and the characteristic impedance as predicted in the equations *(3. 16)* and *(3. 8)*. *Figure III.22* illustrates the behavior of the electric field for BULK and SOI HR substrate.

By combining (3. 14) and (3. 16), losses in substrate can be estimated as:

$$\alpha_d = \frac{139.8725 \cdot \left(\sigma + 1.171 \cdot 10^{-12} \cdot freq\right) \cdot \left(\varepsilon_{reff} - 1\right) \cdot \varepsilon_r}{\sqrt{\varepsilon_{reff}} \cdot \left(\varepsilon_r - 1\right)} \text{ with } \varepsilon_{reff} \approx \frac{\varepsilon_r - 1}{2} \tag{3. 19}$$

Taking $\varepsilon_r = 11.7$ for silicon substrate, *Figure III.23* shows substrate attenuation constant versus silicon conductivity at 60 GHz.

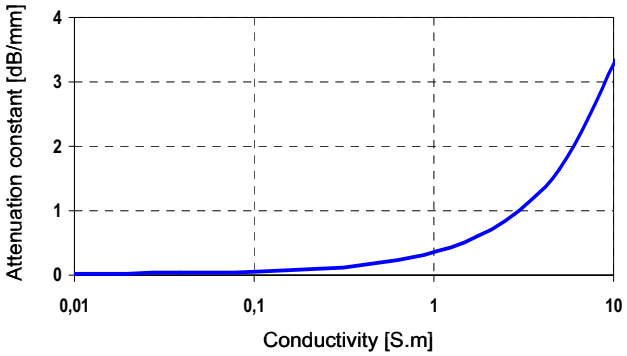
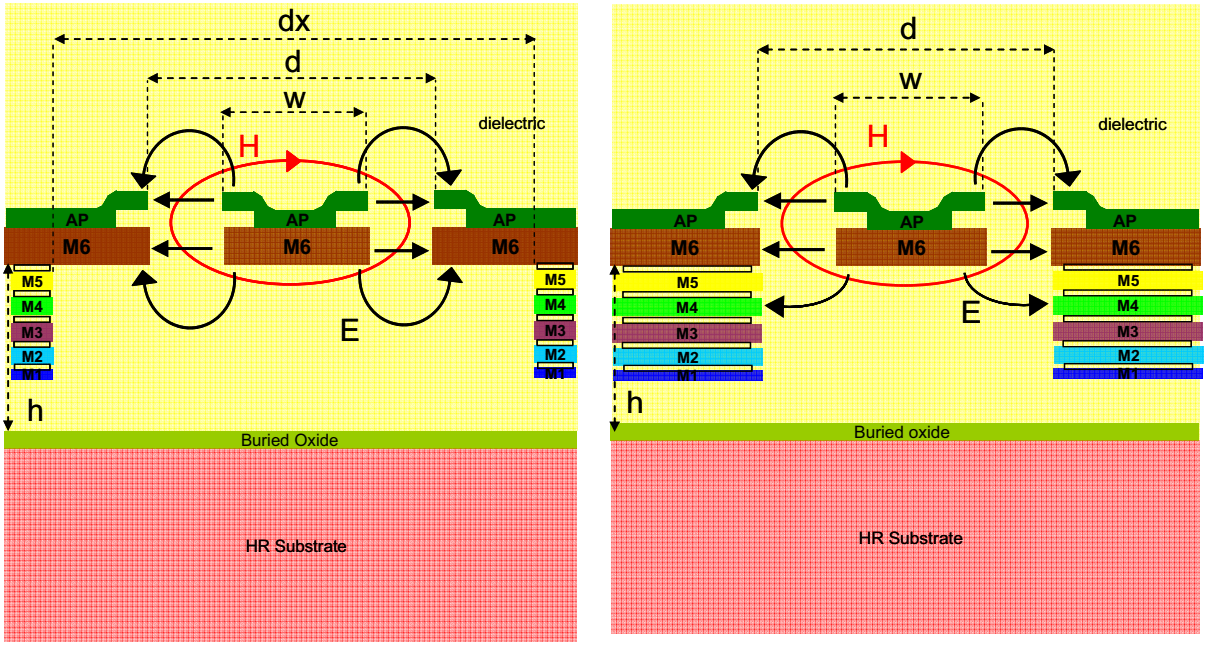


Figure III.23 Attenuation constant versus silicon substrate conductivity at 60GHz

III.1.6.c.i Vertical ground plane coplanar waveguide

Taking into account the CMOS technology design rules, it is not possible to carry out a coplanar line using only the last thick metal level (Metal 6). Thus it is necessary to find a trade off between the respect of the minimum metallization densities and the quasi-TEM propagation condition. This compromise is showed in *Figure III.24* .



a) *b)*

Figure III.24 vertical ground plane transmission line

This solution called vertical ground plane coplanar line[18] offers a similar behavior to coplanar line made all on the same plane. Moreover, it offers a better immunity to coupling between two lines [12]. *Figure III.25* summarizes the performances of this kind of line. The range of characteristic impedances extends from 34Ω to 75Ω with losses about 0.7dB/mm for a characteristic impedance of 50Ω at 80GHz.

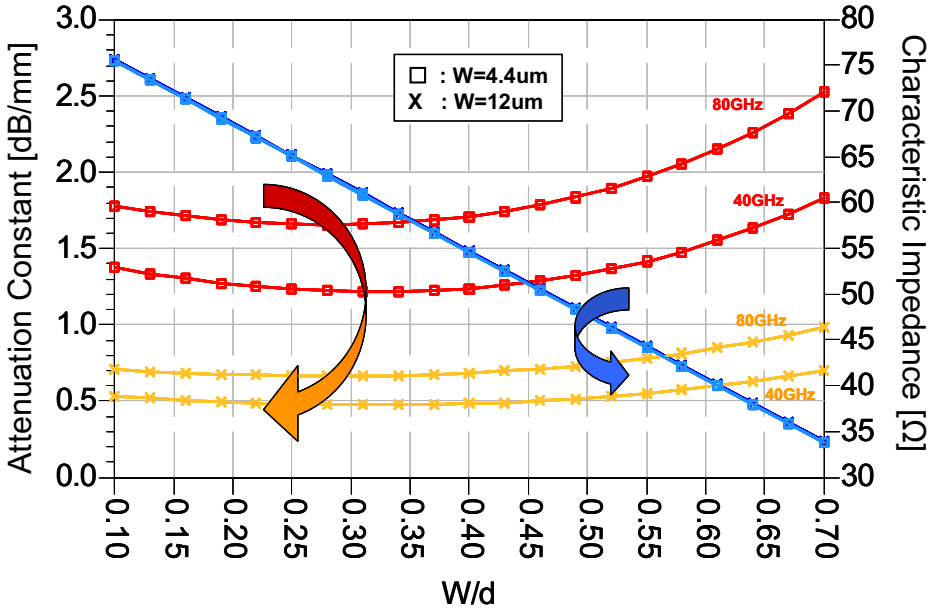


Figure III.25 Vertical ground plane transmission line MOMENTUM simulation

By using HR substrate, the coplanar line presents extremely weak losses comparable with the state of the art [13]. The corresponding losses can be approximated as being only due to metallization.

The following table summarizes the performances of the vertical ground plane coplanar line in CMOS SOI 65nm:

Metallization	**Z_c min (Ω)**	**Z_c max (Ω)**	**$\alpha_{30\Omega}$ @ 80 GHz (dB.mm^{-1})**	**$\alpha_{50\Omega}$ @ 80 GHz (dB.mm^{-1})**	**$\alpha_{70\Omega}$ @ 80 GHz (dB.mm^{-1})**
Metal 6+AP	34	75	1	0.7	0.7

Table III.3 : Performances of the SOI CMOS 65nm VGCPW line.

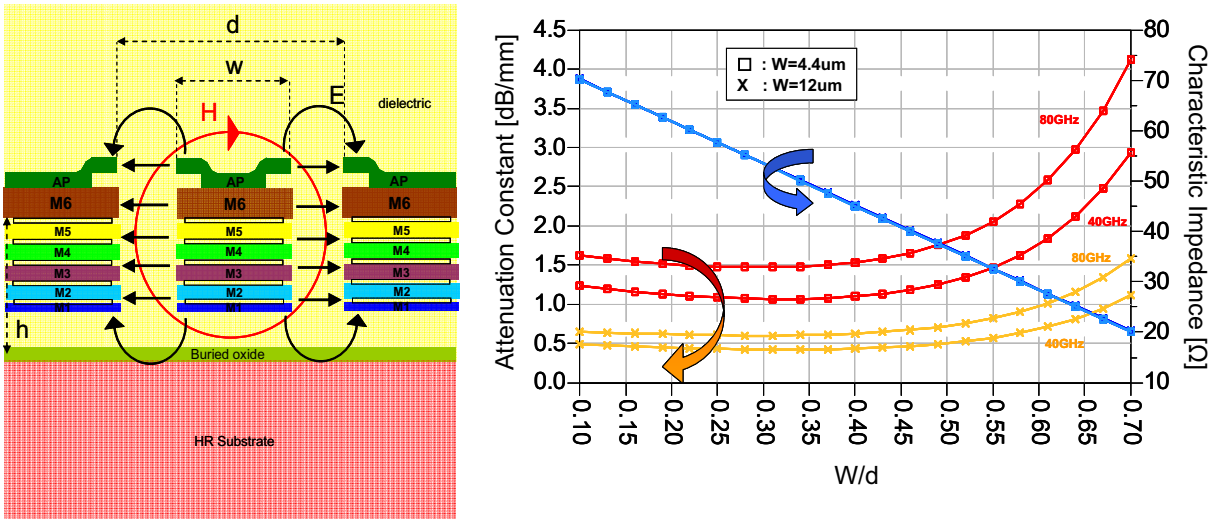
The VGCPW line does not cover a range of characteristic impedances as broad as the microstrip line. However the losses are definitely better (0.7 dB/mm @ 80 GHz). It should be noticed that without SOI HR, for the same structure, the losses would have been of about 4dB/mm at 80 GHz [14].

[18] VGCPW in the literature

III.1.6.c.ii Metal Stacked Coplanar Line

Performances of coplanar lines depend on the substrate used and metal resistivity *(3. 13)(3. 16)*. A good solution to decrease serial metallization resistance is to stack all metal layers, but by doing that the electromagnetic fields are closer to the substrate. Therefore, this solution is less efficient in bulk technology.

The following figure shows the cross section of this type of coplanar line *(a)* and the performance summary for varying characteristic impedances *(b)*.



a) *b)*

Figure III.26 Metal Stacked Coplanar Line cross section a) performance summary b)

The metal stacked coplanar line[19] range of characteristic impedances extends from 20Ω to 70Ω with losses of about 0.6dB/mm at 80GHz. This line allows a smaller value of characteristic impedance in comparison with the VGCPW, because of a higher capacitance ($Z_c \approx \sqrt{L/C}$).An interesting characteristic comes out for small values of conductor width. Because of the important thickness of the conductor line, it is possible to reduce the total line width with good performances in contrast with VGCPW. The next table summarizes the performances of the metal stacked coplanar line in CMOS SOI 65nm:

Metallization	Z_c min (Ω)	Z_c max (Ω)	$\alpha_{30\Omega}$ @ 80 GHz (dB.mm^{-1})	$\alpha_{50\Omega}$ @ 80 GHz (dB.mm^{-1})	$\alpha_{70\Omega}$ @ 80 GHz (dB.mm^{-1})
All	20	70	0.8	0.6	0.6

Table III.4 : Performances of the SOI CMOS 65nm MSCPW line.

[19] MSCPW

The MSCPW line offers a complementary solution for CPW in CMOS. In addition the losses are very good (0.6 dB/mm @ 80 GHz). It should be noticed that without SOI HR, this solution is not conceivable.

III.2. Passive elements characterization

Accurate simulation and modeling of on-chip passive devices (transmission lines, spiral inductors…) is critical for design success. To develop accurate models, measured S-parameters must be de-embedded because high frequency measurements are always influenced by parasitic components (chip influences, pads, test fixture…). Thus, an accurate de-embedding methodology is essential. However, for the last ten years, electromagnetic simulations offer additional tools to develop model and design.

III.2.1. De-embedding methodology

There are different methodologies to de-embed active and passive devices [2], [23]. However a simple and low silicon area consuming technique is hardly compatible. In this section, "open-short" techniques are discussed and a modified open-short de-embedding is proposed.

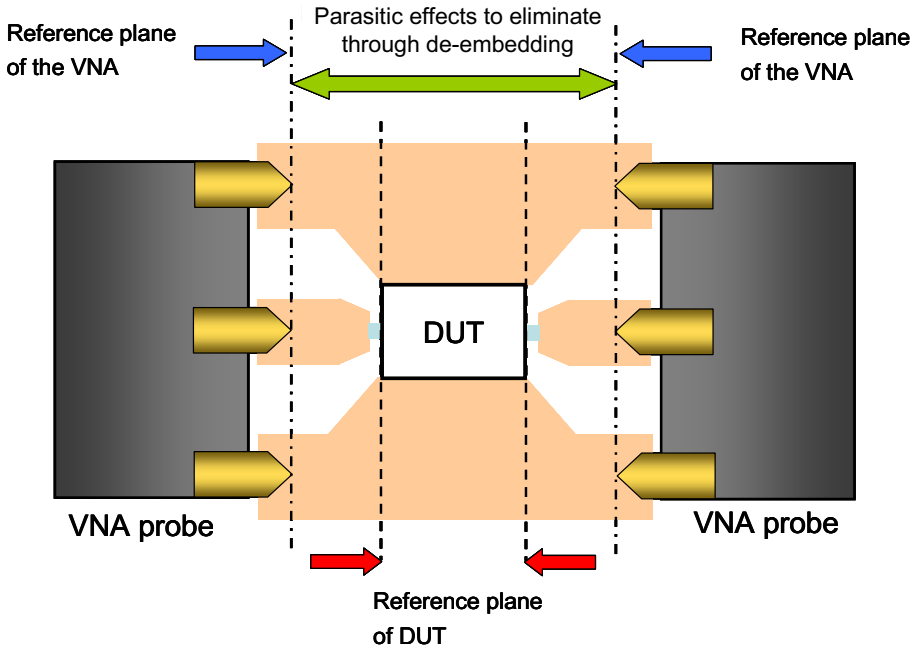
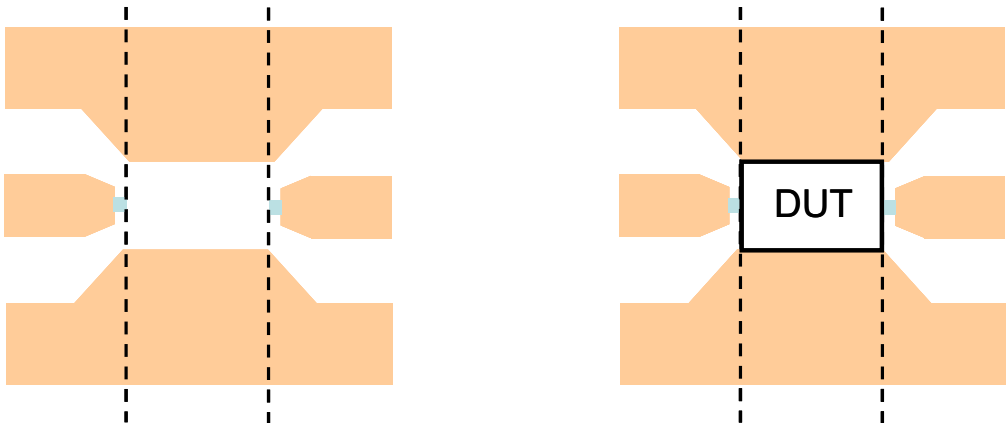


Figure III.27 Measurement configuration

The *Figure III.27* shows the measurement configuration. The calibration of the VNA is located at the end of the probe tips. The influence of the parasitic elements must be eliminated through de-embedding.

III.2.1.a. Open Circuit de-embedding

Open circuit (CO) de-embedding is the simplest method. It is based on the *Figure III.28* . The prerequisite for this de-embedding is an "OPEN" dummy test pad.



a) *b)*

Figure III.28 Open Circuit method illustration, open dummy a), DUT + parasitic elements b)

This method is based on the assumption that parasitic elements consist only of parallel elements. Thus, the calculation of DUT Y-parameters is:

$$[Y_{DUT}] = [Y_{MEAS}] - [Y_{OPEN}] \quad (3.\ 20)$$

Because only parallel elements are taken into account this method is limited. Generally, this technique is used for frequency under 10 GHz.

III.2.1.b. Open-Short Circuit De-embedding

"Open Short Circuit" (CC) de-embedding use an extra structure called "SHORT" to correct the errors from "OPEN" de-embedding. Therefore, serial parasitic elements are also taken into account:

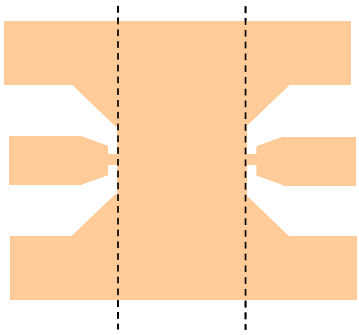


Figure III.29 Short dummy test Pad

The new calculation of DUT Y-parameters is:

$$[Y_{DUT}] = \left(\left([Y_{MEAS}] - [Y_{OPEN}] \right)^{-1} - \left([Y_{SHORT}] - [Y_{OPEN}] \right)^{-1} \right)^{-1} \quad (3.\ 21)$$

In this approach, it is assumed that all parallel parasitics were located in the signal pads and all series parasitics in the interconnect lines. A second de-embedding technique based on the same "OPEN" and "SHORT" as been developed has also been developed by *Tiemeijer* [15]. This technique is referred as “short-open” de-embedding. In this approach, the order of the series impedance and parallel admittance is switched in comparison with *(3. 21)*.

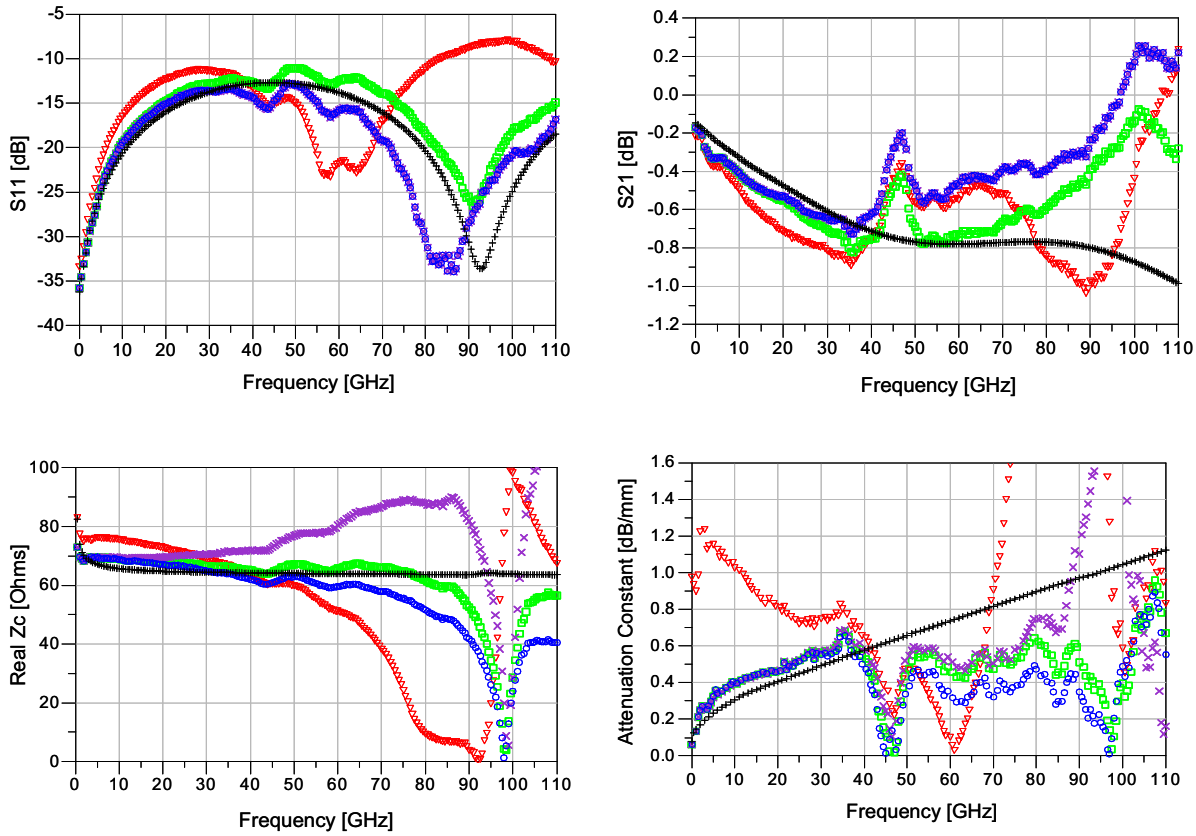
$$[Y_{DUT}] = \left([Z_{MEAS}] - [Z_{SHORT}] \right)^{-1} - \left([Z_{OPEN}] - [Z_{SHORT}] \right)^{-1} \quad (3.\ 22)$$

By combining the two previous equations, a new calculation is proposed. It can be used when the relative distribution of the inductances and capacitances is unknown:

$$[Y_{DUT}] = \frac{\left(\left([Y_{MEAS}] - [Y_{OPEN}] \right)^{-1} - \left([Y_{SHORT}] - [Y_{OPEN}] \right)^{-1} \right)^{-1}}{2} + \frac{\left([Z_{MEAS}] - [Z_{SHORT}] \right)^{-1} - \left([Z_{OPEN}] - [Z_{SHORT}] \right)^{-1}}{2} \quad (3.\ 23)$$

III.2.1.c. De-Embedding Comparison

These de-embedding techniques have been compared to electromagnetic simulations using a coplanar transmission line as DUT. The next figure shows the results:



Red triangle : "OPEN" method (3. 20) ; Purple X : "OPEN-SHORT" (3. 22) ; Blue circle : "OPEN-SHORT" (3. 21)
Green square : "OPEN-SHORT" (3. 23) ; Black cross : Momentum Simulation

Figure III.30 CPW line de-embedding comparison

From these results, it appears that the "OPEN" technique is not good for transmission line de-embedding; also the proposed method *(3. 23)* is the most accurate in this type of measurement. In addition, this method uses only two test pad dummies in comparison to TRL or through de-embedding.

III.2.2. Electromagnetic Simulation

Today, electromagnetic simulations offer additional tools to develop model and design. In this work, Agilent Momentum [16] has been used for all electromagnetic simulations. The simulator setup follows this methodology:

- Substrate definition is the same as describe in *III.1.2.*, vias are define as only 2D distributed (vertical currents only), thus it possible to simplify via matrix into an equivalent geometric shape.
- Ports are set to single for edge stimulation or as point for intra-metallic input/output.

- Most of the time mesh control is set to maximum simulation frequency and uses a mesh density of 20 cells/wavelength

Electromagnetic simulation allows accurate results for most of passives elements. *Figure III.31* shows a comparison between Momentum simulator and measurement[20] of a VGCPW (Width=12um, Gap=5um, Length=800um):

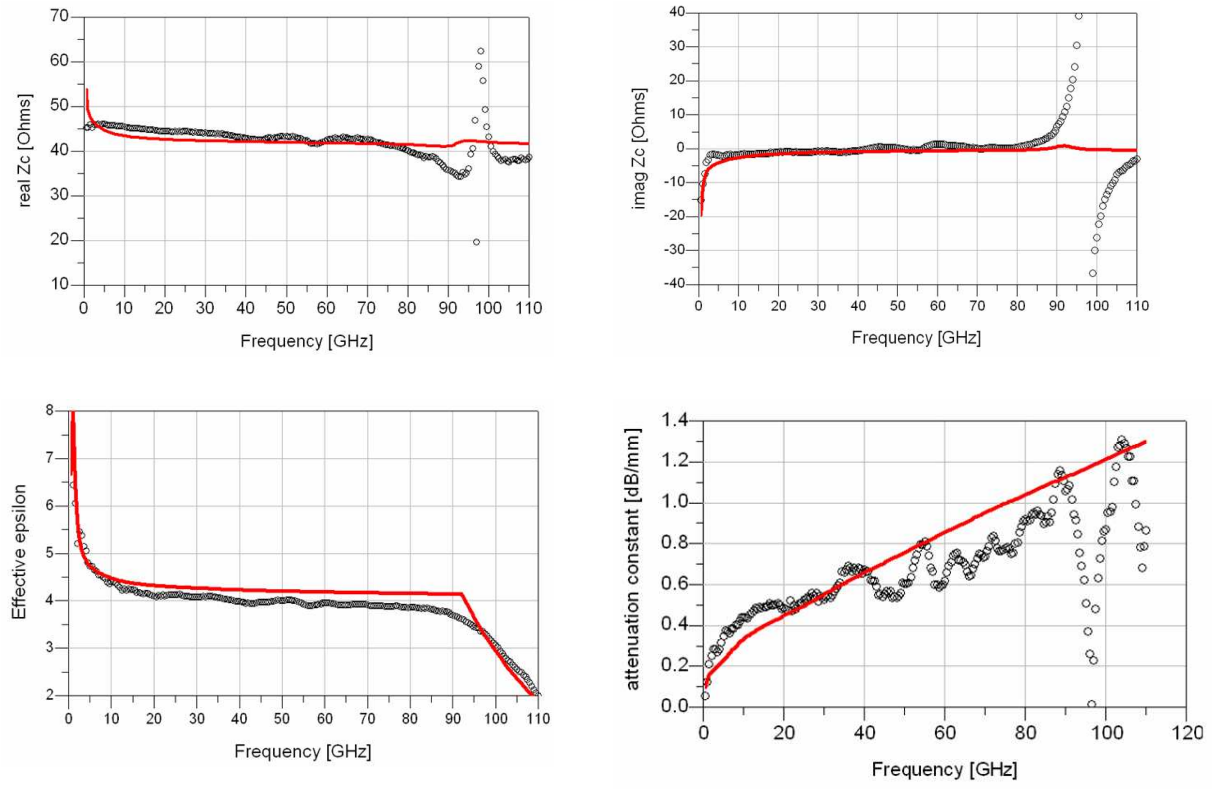


Figure III.31 Momentum (red line) versus measurement for a CPW line

These results show how thanks to EM simulator it becomes possible to save silicon area by using only few measured structure to calibrate simulator. It becomes also possible to investigate new structures.

[20] De-embedding use here is the *(3. 23)*

III.3. Modeling of passive elements

In the following section, analytical and empirical model are described. Methodology extraction of lumped elements of each model is also given. Capacitance and micro-strip lines model are not studied here. In *III.3.2.a* a new analytic model for silicon coplanar line is presented. As for discontinuities modeling, it is described in appendixes.

III.3.1. Inductance

The modeling of on-chip spiral inductors described here uses compact, scalable lumped circuit [3], [17]. Segmented circuit models are not discussed here. As highlighted in section III.1.4, inductance studied here used HR SOI substrate which presents very low substrate losses. Therefore inductance model presented does not take into account substrate magnetic coupling.

III.3.1.a. Analytical

The equivalent circuit of the inductor is shown in *Figure III.7* and the layout in *Figure III.32*

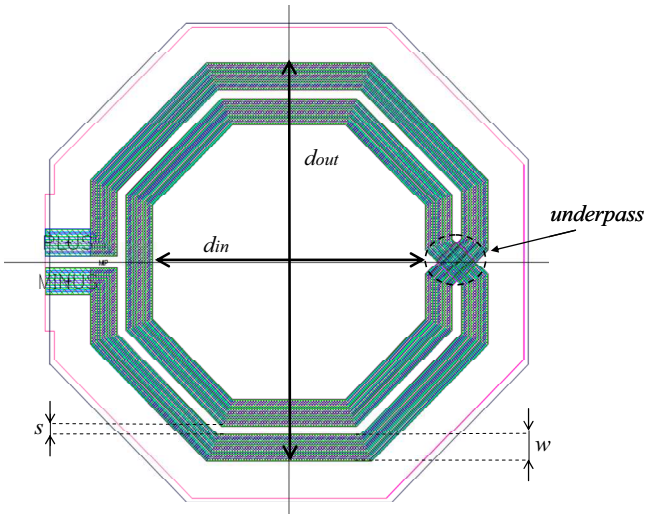


Figure III.32 On-chip inductor layout

The lumped elements of this equivalent circuit are obtained from the following lateral parameters of a spiral:

- Number of turns, *n*

- Number of sides, N
- Metal width, w
- Edge-to-edge spacing between adjacent turns, s
- The outer diameter d_{out} and the inner diameter d_{in}

The average diameter is calculated as follow:

$$d_{avg} = \frac{1}{2} \cdot \left(d_{out} + d_{in} \right) \quad \text{[m]} \tag{3. 24}$$

The fill ration ρ is defined as:

$$\rho = \frac{1}{d_{avg}} \cdot \left(n\left(w+s\right) - s \right) \text{ with } s \text{ edge-to-edge spacing between conductors} \tag{3. 25}$$

From above values, the length l of the spiral is well approximated by:

$$l = \frac{1}{T} \cdot \left(\left(4n+1\right) \cdot d_{in} + \left(4 \cdot \left[n\right] + 1\right) \cdot \left[n\right] \cdot \left(w+s\right) \right) \quad \text{[m]} \quad \text{with } [n] \text{the integer part of } n \text{ and } 1/T \text{ the shape ratio of the inductor (T=1 for square and T=1.21 for octagonal inductor)} \tag{3. 26}$$

The lumped model of the spiral is then:

$$R_s \approx l.r_{cond} \quad [\Omega] \quad \text{with } r_{\text{cond}} \text{ defined in (3. 7)} \tag{3. 27}$$

The oxide capacitance, C_{ox} is:

$$C_{ox} \approx \frac{1}{2} \frac{\varepsilon_0 \varepsilon_{ox}}{t_{ox}} l.w \quad \text{[F]} \tag{3. 28}$$

The substrate capacitance is:

$$C_{sub} \approx \frac{1}{2} .C_{si} .l.w \quad \text{[F]} \tag{3. 29}$$

with C_{si} substrate capacitance per unit area (C_{si}* ≈ 3.48e-6 F/m² in CMOS 65nm)

The substrate resistance is:

$$R_{sub} \approx \frac{2}{G_{sub} .l.w} \quad [\Omega] \tag{3. 30}$$

with G_{sub} substrate conductance per unit area (G_{sub}* ≈ 805230 S/m² in CMOS 65nm bulk and G_{sub}≈ 8052 S/m² in SOI)

*extrapolated from measurement

The capacitance between the spiral and the metal underpass is modeled by:

If $\frac{w}{t_c} > 3$, then $C_s \approx n \cdot w^2 \left[\frac{\varepsilon_0 \varepsilon_{ox}}{t_{ox,M1-M2}} \right]$ [F] with t_c conductor thickness. Else the fringing capacitance must be take into account [19] :

$$C_s \approx \varepsilon_0 \varepsilon_{ox} \cdot n \cdot w \left[\frac{w}{t_{ox,M1-M2}} + \frac{1}{2} \cdot \left[0.77 + 1.06 \left[\left(\frac{w}{t_{ox,M1-M2}} \right)^{0.25} + \left(\frac{t_c}{t_{ox,M1-M2}} \right)^{0.5} \right] \right] \right] \text{ [F]} \quad (3.31)$$

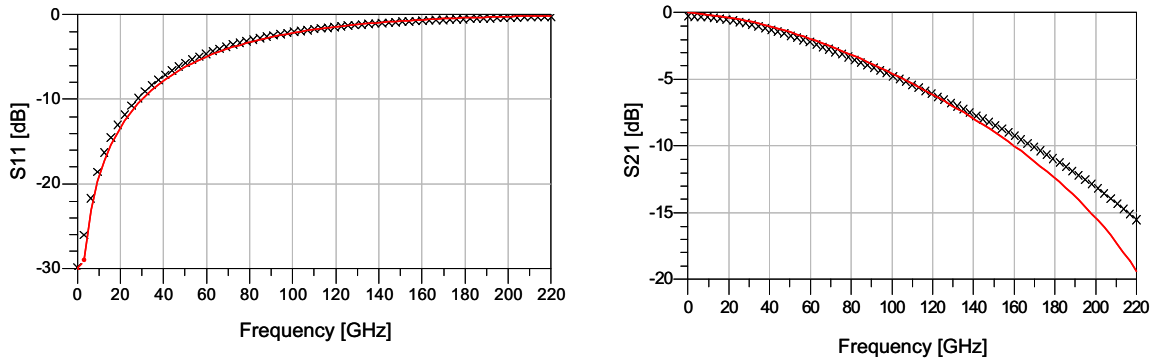
From *Wheeler* formula and [3], the expression for the inductance L_s of planar spiral integrated inductors is:

$$L_s = K_1 . \mu_0 . \frac{n^2 d_{avg}}{1 + K_2 \rho} \text{ [H]} \quad (3.32)$$

Layout	K_1	K_2
Square	2.34	2.75
Hexagonal	2.33	3.82
octagonal	2.25	3.55

Table III.5 : K_1 and K_2 coefficients for L_s calculation

The next figure shows a comparison between the above analytic model and a Momentum simulation of the inductance on *Figure III.13*



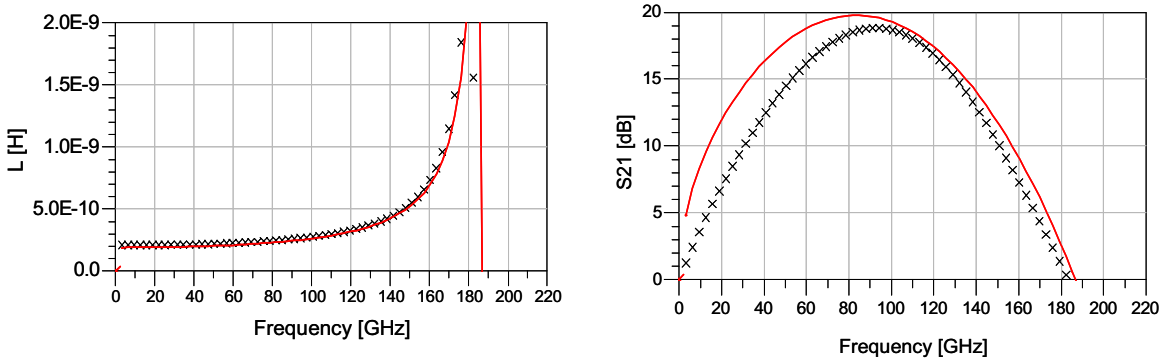


Figure III.33 Comparison between analytical inductor model (dashed lines) and EM simulation (continuous lines) for a 200pH inductor

This analytical model shows a good accuracy for small inductance beyond millimeter wave frequency. For large inductances the distributed aspect must be taking into account.

III.3.1.b. Model extraction from measurement

The elements of the equivalent circuit (*Figure III.7*) are straightforwardly obtained from the Y-parameters of a simulated or measured inductor as follows:

$$L_s = \frac{Im\left\{-y_{12}^{-1}\right\}}{2.\pi.freq} \quad [\mathrm{H}] \tag{3. 33}$$

$$R_{DC} = Re\left\{-y_{12}^{-1}\right\} \quad [\Omega] \quad \text{at very low frequency} \tag{3. 34}$$

$$R_{HF} = k.\sqrt{freq} \quad [\Omega]\ ; \qquad k = \sqrt{\frac{-\left(R_{DC}^2 - \mathrm{Re}\left\{-y_{12}^{-1}\right\}_{f_0}^2\right)}{f_0}} \tag{3. 35}$$

f_0 is a frequency point in the linear region of $Re\left\{-y_{12}^{-1}\right\}$ plotted as a function of frequency (Figure III.34)

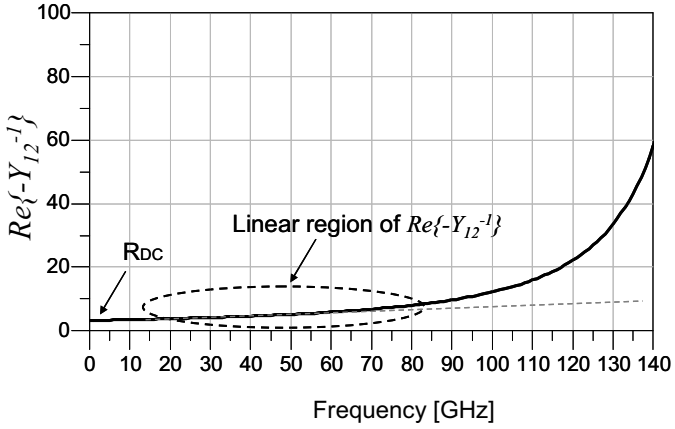


Figure III.34 $Re\left\{-y_{12}^{-1}\right\}$ *plotted as a function of frequency*

$$R_s = \sqrt{R_{DC}^2 + R_{HF}^2} \ [\Omega] \tag{3. 36}$$

$$C_{ox1} = \frac{\left[Im\left\{\frac{1}{y_{11}+y_{12}}\right\}\right]^{-1}}{2.\pi.freq} \quad C_{ox2} = \frac{\left[Im\left\{\frac{1}{y_{22}+y_{21}}\right\}\right]^{-1}}{2.\pi.freq} \ [F] \tag{3. 37}$$

$$R_{sub1} = Re\left\{\frac{1}{y_{11}+y_{12}}\right\} \quad R_{sub2} = Re\left\{\frac{1}{y_{22}+y_{21}}\right\} \ [\Omega] \tag{3. 38}$$

$$C_{sub1} = \frac{\varepsilon_0 \varepsilon_r \rho_{si}}{R_{sub1}} \quad C_{sub2} = \frac{\varepsilon_0 \varepsilon_r \rho_{si}}{R_{sub2}} \ [F] \quad \text{with } \rho_{si} \text{ the resistivity of the substrate} \tag{3. 39}$$

This model is not a physical equivalent circuit since all elements are variable according to the frequency. Anyway, this type of model is very accurate. However this model is valid only for the extracted device and is not scalable.

III.3.2. Coplanar Lines

Coplanar lines models had been widely discussed [20], [26], [26] and [27]. However, those studies do not take into account the multilayered and lossy silicon aspect. In this section we developed a new analytical model adapted to multilayered silicon technology. Models extracted from high frequency measurement are also presented in the second part.

III.3.2.a. Analytical model

To totally describe the actual behavior of the coplanar line on CMOS technology we updated the electrical model previously shown in *III.1.6.a* as follows:

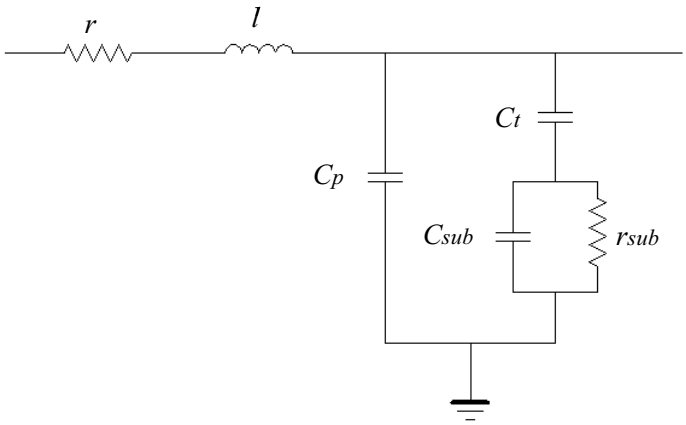


Figure III.35 CMOS coplanar electrical model

Here, the total capacitances are decomposed into three main capacitances. The next figure shows parallel elements of the electrical model describes in *Figure III.35*

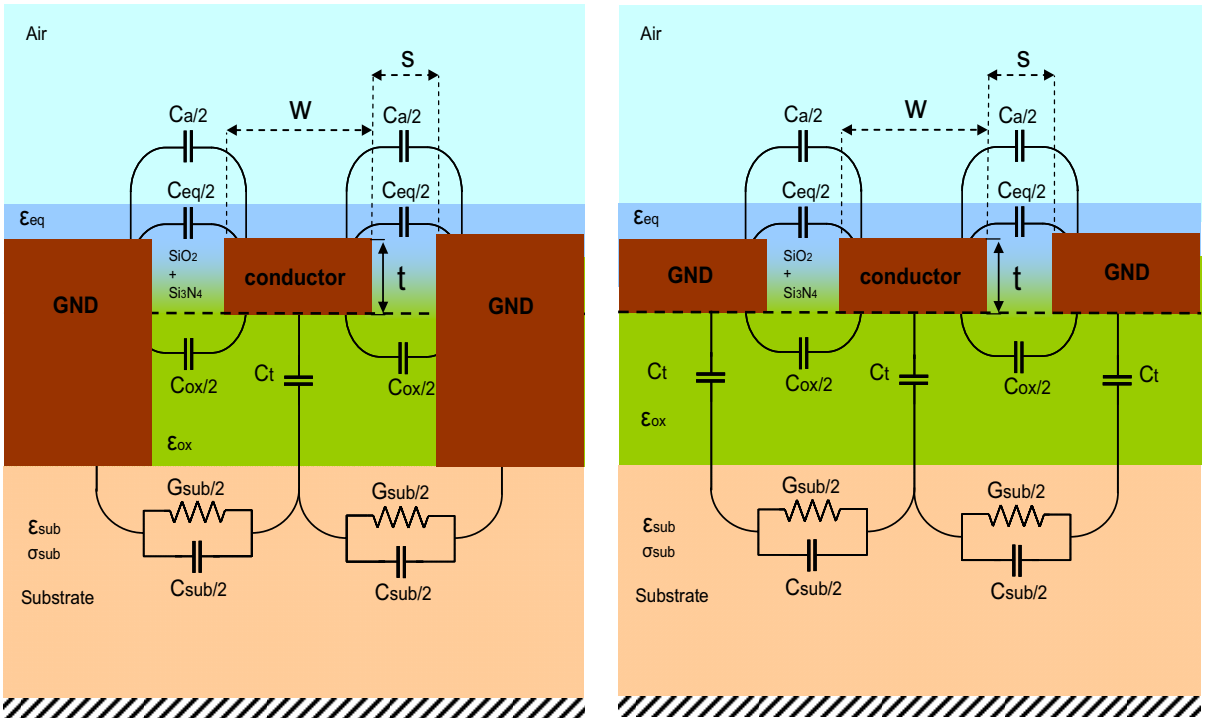
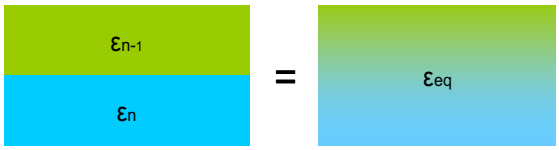


Figure III.36 parallel electrical elements of VGCPW (a), and CPW (b)

The total capacitance is decomposed in 5 elements depending on the different dielectric materials surrounding the line. Here, we distinguish 4 dielectric materials with the following permittivity: ε_0 (air), ε_{eq} (oxide and passivation layer), ε_{ox} (oxide under conductor line) and ε_{sub} (silicon substrate). The equivalent dielectric is calculated using the *Kraszewski* formula [18]:



$$\varepsilon_{eq} = \left(\sqrt{\varepsilon_n} + \frac{h_{n-1}}{h_{n-1} + h_n} \left(\sqrt{\varepsilon_{n-1}} - \sqrt{\varepsilon_n} \right) \right)^2 \qquad (3.\ 40)$$

III.3.2.a.i Elements extraction with conformal mapping

Using conformal mapping from *Schwartz-Christoffel* transformation, the transmission line can be split up into the above elements. The next picture shows these splitting steps:

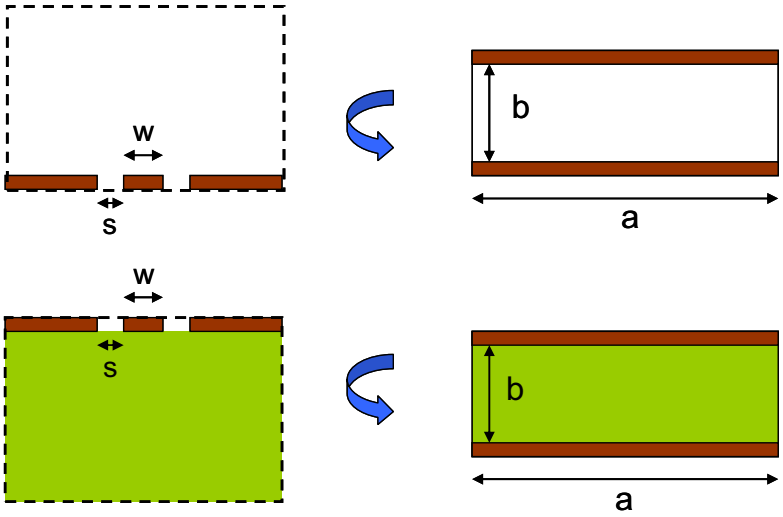


Figure III.37 Conformal mapping representation

The equivalent fringe capacitance of the coplanar line is transform on pure parallel plate capacitances with specific dielectric. The transformed area is obtained by scaling each linear dimension of the original area by a factor of *a* and rotating the original element by an angle φ. This transformation is obtained by using the complete elliptic integral of the first kind, K(k) which is given in appendixes. Thus, capacitances C_a, C_{eq}, C_{ox} and C_{sub} are defined as follow:

$$C_a = 2.\varepsilon_0 \left(\frac{K(k_e)}{K(k_e')} - \frac{K(k_{ie})}{K(k_{ie}')} \right) \quad [\mathrm{F}] \tag{3. 41}$$

$$C_{eq} = 2.\varepsilon_0.\varepsilon_{eq} \left(\frac{K(k_{ie})}{K(k_{ie}')} \right) \quad [\mathrm{F}] \tag{3. 42}$$

$$C_{ox} = 2.\varepsilon_0.\varepsilon_{ox} \left(\frac{K(k_i)}{K(k_i')} \right) \quad [\mathrm{F}] \tag{3. 43}$$

$$C_{sub} = 2.\varepsilon_0.\varepsilon_{sub} \cdot \left(\frac{K(k)}{K(k')} \right) \quad [\mathrm{F}] \tag{3. 44}$$

The parallel plate capacitance under the conductor is given by the following equation:

$$C_t = \varepsilon_0.\varepsilon_{ox} \cdot \frac{w}{h_{ox}} \quad [\mathrm{F}] \tag{3. 45}$$

Thus, the total line capacitance is:

$$C_{tot} = C_a + C_{eq} + C_{ox} + \frac{C_{sub}.C_t}{q.(C_{sub} + C_t)} \quad [\mathrm{F}] \tag{3. 46}$$

q depending of the thickness of ground planes, for VGCPW line $q \approx 3$, for CPW $q \approx 2$

The conformal mapping is used also to find the conductance *G* and the inductance *L* of the line:

$$G_{sub} = \sigma . \left(\frac{K(k)}{K(k')} \right) \quad [\mathrm{S}] \tag{3. 47}$$

$$L = \frac{\mu_0}{4} . \frac{K(k_e')}{K(k_e)} \quad [\mathrm{H}] \tag{3. 48}$$

Finally, T-line resistance is given by:

$$R = \sqrt{R_{DC}{}^2 + R_{HF}{}^2} \quad [\Omega] \tag{3. 49}$$

with $R_{DC} = \frac{1}{w.t.\sigma}$ [Ω] and $R_{HF} = \sqrt{\frac{2\pi . freq . \mu_0}{2.\sigma}} \frac{1}{w+t}$ [Ω]

$w = width$
$t = thickness$
$\sigma = conductivity$
$\mu_0 = 4.\pi.10^{-7}$

From those equations, *r,l,c* and *g* lineic parameters of the electrical model are:

$$\begin{aligned} l &= L \cdot length \quad [\mathrm{H.m^{-1}}] \\ r &= R \cdot length \quad [\Omega.\mathrm{m^{-1}}] \\ c &= C_{tot} \cdot length \quad [\mathrm{F.m^{-1}}] \\ g &= G_{sub} \cdot length \quad [\mathrm{S.m^{-1}}] \end{aligned} \tag{3. 50}$$

Note that we do not use multilayered technique describes in [20] because the assumption for the equivalent capacitance in silicon technology is false because $\varepsilon_{ox} - \varepsilon_{sub}$ is negative.

III.3.2.a.ii Analytical model comparison with measured and EM data

The analytical model has been implemented into ADS[21] simulator and compared to measurement and EM simulations. The first comparison is for a measured VGCPW (*III.1.6.c.i*) with the following dimension:

- Width: 5 µm
- Gap: 8.5 µm
- Length: 800 µm

[21] ADS: Advanced Design System software from Agilent

The de-embedding methodology used is the modified open-short method explains in *(III.2.1.b)*.

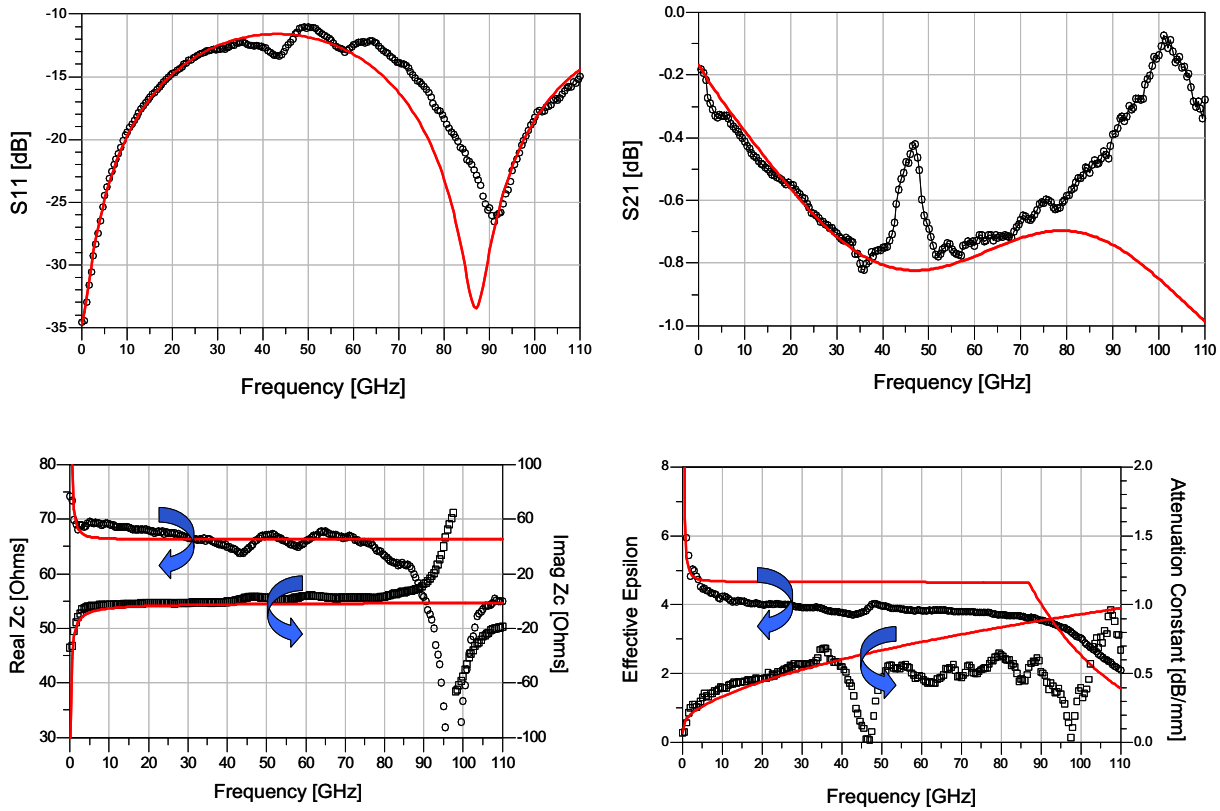


Figure III.38 Measurement versus analytical model for a VGCPW line

As discussed previously, measurement results are very sensitive to de-embedding method. Nevertheless, the analytical model shows good results in a wide frequency range.

The second comparison is for a simulated CPW line describes in (III.1.6.c.ii) with the following dimension:

- With: 12 µm
- Gap: 11 µm
- Length: 800 µm

The EM simulator setup is the same as explain in *(III.2.2)*

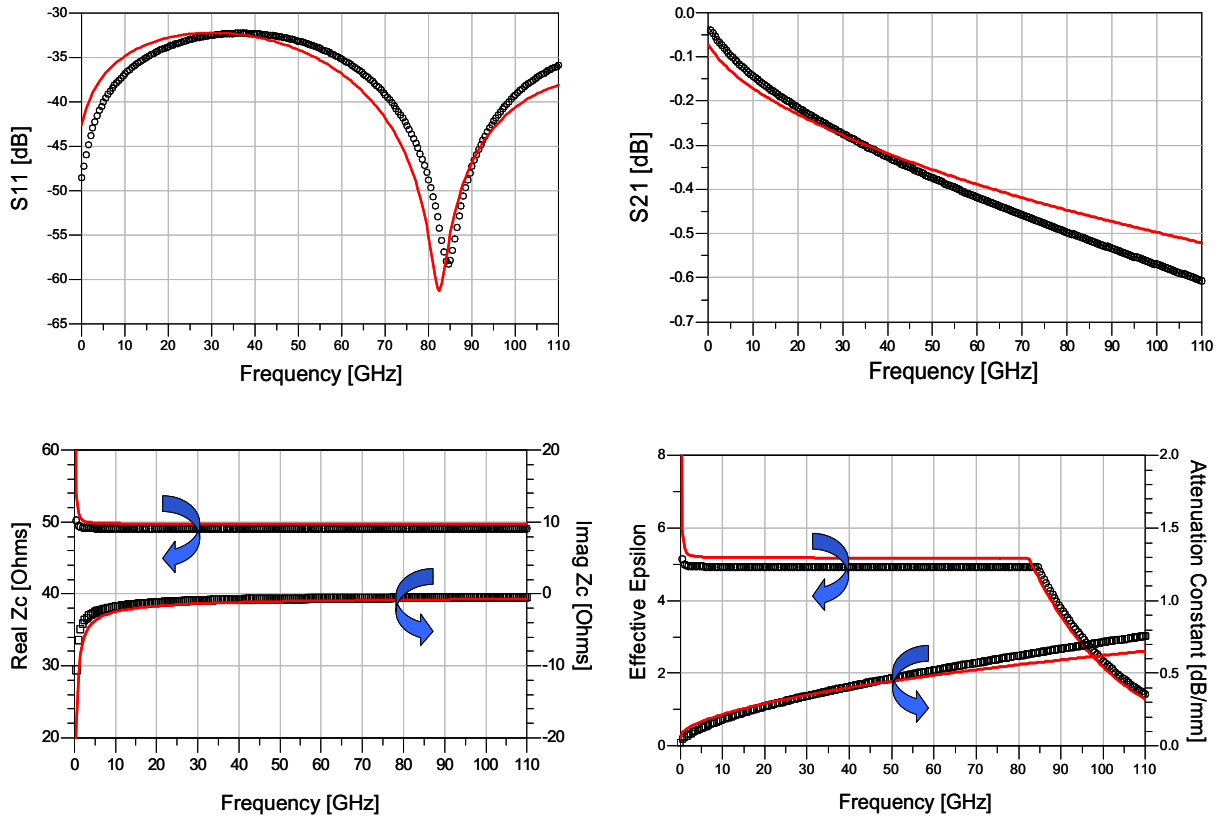


Figure III.39 EM simulation versus analytical model for a CPW line

These two comparisons show that this quasi-TEM model yields sufficient accuracy up to millimeter wave frequencies. By taking into account all layers (metals and dielectrics) this model can also be used to find the best CPW size to minimize losses. It can be noticed that it can be used for both HR SOI and bulk substrates.

III.3.2.b. Model extraction from measurement

Distributed *r*, *l*, *c* and *g* elements specified per unit length (*Figure III.16* used to modeling a line could be extracted directly from S parameters using the following methodology.

The characteristic impedance is:

$$Z_c = Z_0 \cdot \sqrt{\frac{(1+S_{11})(1+S_{22})-S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}} \quad [\Omega] \tag{3. 51}$$

The propagation constant is:

$$\gamma = \frac{1}{l} \cdot \cosh^{-1}\left(\frac{(1-S_{11})(1+S_{22})-S_{12}S_{21}}{S_{12}+S_{21}}\right) \tag{3. 52}$$

From Z_c and γ distributed elements can be directly extracted:

$$r = Real\left\{\frac{\gamma}{Z_c}\right\} \quad [\Omega/\mathrm{m}] \tag{3. 53}$$

$$l = \frac{Imag\{Z_c \cdot \gamma\}}{2\pi . freq} \quad [\mathrm{L/m}] \tag{3. 54}$$

$$g = Real\left\{\frac{\gamma}{Z_c}\right\} \quad [\mathrm{S/m}] \tag{3. 55}$$

$$c = \frac{1}{2\pi . freq} \cdot Imag\left\{\frac{\gamma}{Z_c}\right\} \quad [\mathrm{F/m}] \tag{3. 56}$$

As for inductors, this type of model is very accurate. However this model is valid only for the extracted device and it is only scalable in length.

III.4. Summary

In this chapter, we have reviewed passive element performances in SOI CMOS 65nm technology and see how they are modeled. We have shown the commonly used lumped and distributed passive elements in RF and millimeter wave design.

The CMOS SOI technology for coplanar wave guides design has been compared with the silicon transmission lines state of the art. Except for millimeter wave dedicated technology (BiCMOS9 MW from *STMicroelectronics*), CMOS SOI 130nm and 65nm processes present the best attenuation constant performance (*Table III.1 :*).

The High Resistivity substrate potentiality and interest for millimeter wave passive components have been demonstrated. Characterization and electromagnetic simulations have highlighted the increase performances by using SOI instead of bulk.

Spiral inductors and coplanar transmission lines model have been presented. Analytical and measurement based models have been developed and discussed. The condition of validity of the different models has been also studied.

III.5. Bibliography

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III.6. Appendixes:

A. Z_c, α and ε_{reff} calculation from S parameters measurement

The characteristic impedance of a transmission line is given by:

$$Z_c = Z_0 \frac{(1+S_{11})(1+S_{22}) - S_{12}S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}} \quad [\Omega] \tag{3. 57}$$

The propagation constant is calculated as follow:

$$\gamma = \operatorname{acosh}\left(\frac{(1+S_{11})(1-S_{22}) + S_{12}S_{21}}{S_{12}+S_{21}}\right) \tag{3. 58}$$

Then the attenuation constant and the phase constant are defined as:

$$\alpha = \Re\{\gamma\} \quad [\text{Np.m}^{-1}] \quad \text{and} \quad \alpha_{dB} = 8.686e^{-3} \cdot \Re\{\gamma\} \quad [\text{dB/mm}]$$
$$\beta = \Im\{\gamma\} \quad [\text{rad.m}^{-1}] \tag{3. 59}$$

Finally, the effective permittivity is:

$$\varepsilon_{reff} = \frac{\beta^2 c^2}{4 \cdot freq^2 \pi^2} \tag{3. 60}$$

B. Conformal mapping

As discuss in *III.3.2.a.i*, conformal mapping is used to extract the elements of the *Figure III.36* . The conformal mapping transformation is obtained by using the complete elliptic integral of the first kind, *K(k)* which can be defined as follow:

$$\frac{K(k)}{K(k')} = \begin{Bmatrix} \dfrac{\pi}{\ln\left(2.\dfrac{1+\sqrt{k'}}{1-\sqrt{k'}}\right)} \\ \dfrac{1}{\pi}\ln\left(2.\dfrac{1+\sqrt{k}}{1-\sqrt{k}}\right) \end{Bmatrix} \quad \text{with} \quad \begin{Bmatrix} 0 \le k \le 0.707 \\ 0.707 \le k \le 1 \end{Bmatrix} \tag{3. 61}$$

$$\frac{K(k)}{K(k')} = \left[\frac{K(k')}{K(k)}\right]^{-1}$$

$K'(k) = K(k')$, the variables k and k' are geometrically dependent, and are given as:

$$k = \frac{w}{w + 2.s} \qquad \text{and} \qquad k' = \sqrt{1-k^2} \tag{3. 62}$$

The above expression is given for a sheet conductor with no thickness. To take into account the conductor thickness it is necessary to use the corrective parameters Δ:

$$\Delta = \left(1.25\frac{t}{\pi}\right)\left[1 + \ln\left(4\pi\frac{w}{t}\right)\right] \tag{3. 63}$$

The equivalent values for *w* and *s* are:

$$\begin{aligned} s_e &= s - \Delta \\ w_e &= w + \Delta \end{aligned} \tag{3. 64}$$

And the variables k and k' become:

$$k_e = \frac{w_e}{w_e + 2.s_e} \qquad \text{and} \qquad k_e' = \sqrt{1-k_e^2} \tag{3. 65}$$

Since it is not possible to consider each layer as infinitively thick new values for *s, w, k* and *k'* are defined as follow:

$$w_i = 2.\sinh\left(\frac{\pi.w}{4.h_i}\right) \qquad s_i = \sinh\left(\frac{\pi\left(s + \dfrac{w}{2}\right)}{2.h_i}\right) - \frac{w_i}{2} \tag{3. 66}$$

$$k_i = \frac{w_i}{w_i + 2.s_i} \qquad k_i' = \sqrt{1-k_i^2} \tag{3. 67}$$

Using Δ to take into account conductor thickness and the dielectric thickness *s*, *w*, *k* and *k*' are written as:

$$w_{ie} = 2.\sinh\left(\frac{\pi.w_e}{4.h_i}\right) \qquad s_{ie} = \sinh\left(\frac{\pi\left(s_e + \frac{w_e}{2}\right)}{2.h_i}\right) - \frac{w_{ie}}{2} \tag{3. 68}$$

$$k_{ie} = \frac{w_{ie}}{w_{ie} + 2.s_{ie}} \qquad k_{ie}' = \sqrt{1 - k_{ie}^2} \tag{3. 69}$$

As for T-line capacitance, to calculate the line inductance it is necessary to take into account the thickness of the metal conductor. Again, a Δ' corrective parameter is introduced:

$$\Delta' = \left(1.25\frac{t}{2.\pi}\right)\left[1 + \ln\left(8.\pi\frac{w}{t}\right)\right] \tag{3. 70}$$

The equivalent values for *w* and *s* become:

$$\begin{aligned} s_L &= s - \Delta' \\ w_L &= w + \Delta' \end{aligned} \tag{3. 71}$$

And the variables k and k' become:

$$k_L = \frac{w_L}{w_L + 2.s_L} \quad \text{and} \quad k_L' = \sqrt{1 - k_L^2} \tag{3. 72}$$

C.Discontinuities modeling

Underpass

Underpasses are used to bring back ground plane sides to the same electrical potential as explain in *III.1.6.c.*

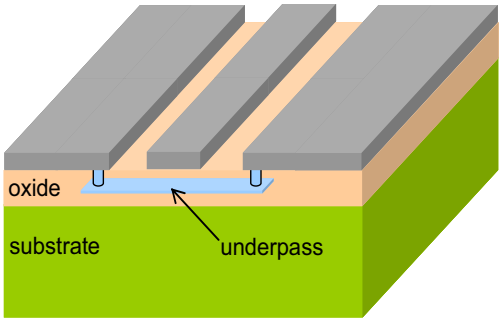


Figure III.40 Underpass representation

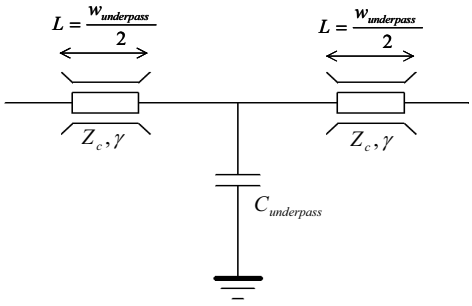


Figure III.41 Underpass model

The $C_{underpass}$ capacitance is composed of the parallel plate capacitance and also the fringing capacitance:

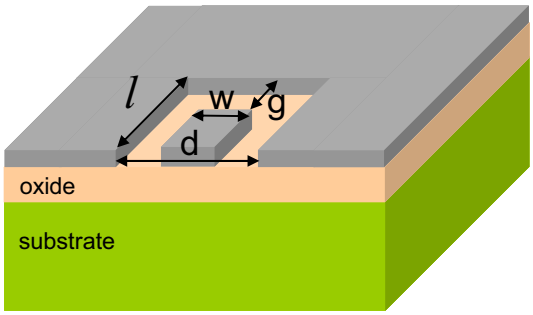
$$C_{fringe} \approx \varepsilon_0 \varepsilon_{ox} \cdot w_{CPW} \left[\frac{w_{underpass}}{t_{ox}} + \left(0.77 + 1.06 \left(\left(\frac{w_{underpass}}{t_{ox}} \right)^{0.25} + \left(\frac{t_{CPW}}{t_{ox}} \right)^{0.5} \right) \right) \right] \quad (3.\ 73)$$

t_{ox} distance between coplanar line and the underpass ; t_{CPW} thickness of the coplanar line

Coplanar Stub CO[22] and CC[23]

It has been demonstrated that a coplanar stub can be modeled by an equivalent coplanar line with a given length in addition with an extended line value (l_{ext}) [21].

For an open circuit stub (CO) the equivalent model is the following:



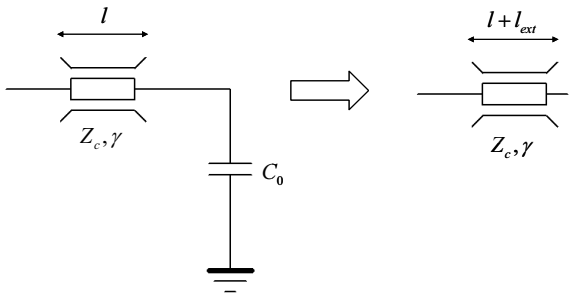


Figure III.42 Stub CO representation and the corresponding model

[22] CO : open circuit
[23] CC : short circuit

$$l_{ext} = C_0 / C \approx d/4 \quad C: lineic\ capacitance\ of\ the\ line$$
$$If: g > d; 0.2 < W/d < 0.8; t < 5\ \mu m \tag{3. 74}$$

The same methodology is used for the short circuit stub (CC):

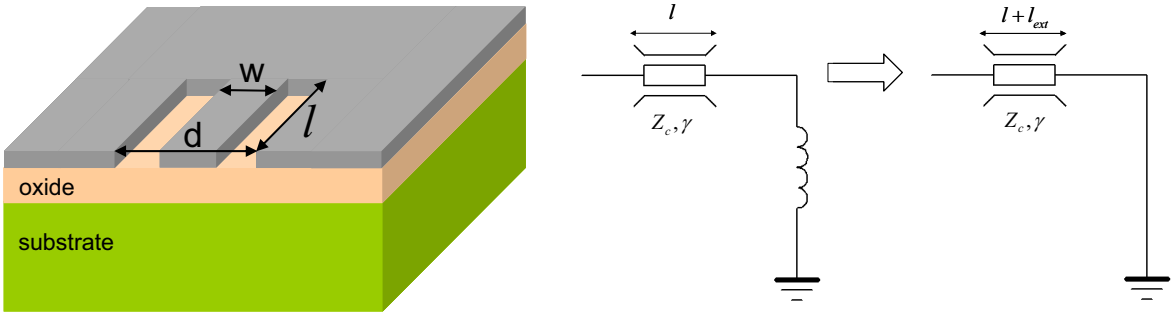


Figure III.43 Stub CC representation and the corresponding model

$$l_{ext} = L_0 / L \approx d/8 \quad L: lineic\ inductance\ of\ the\ line$$
$$If: \frac{d - w}{2} > t \tag{3. 75}$$

The *T* junction

The T junction is modeled by three homogenous coplanar lines which length references are taken as showed in *Figure III.44* .

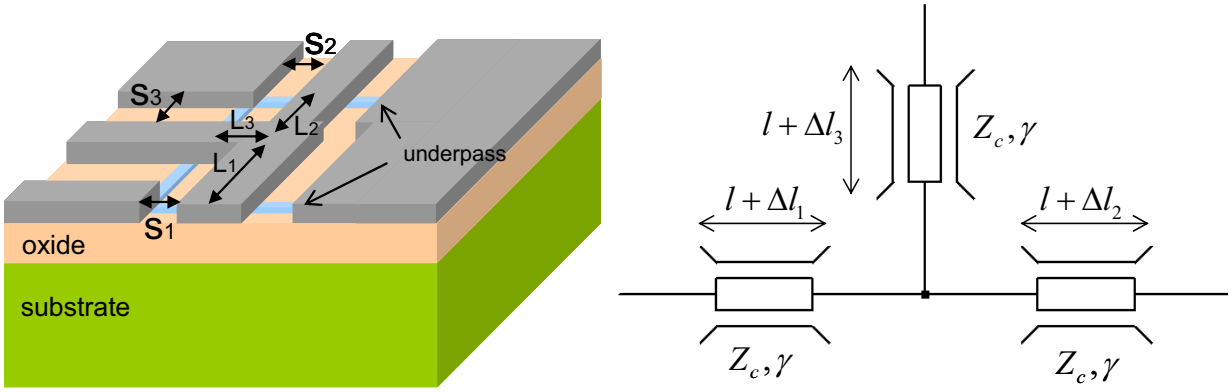


Figure III.44 T junction representation and the corresponding model

Extended Δl values are calculated as follow:

$$\Delta l_3 = \frac{s_1 + s_2}{2} \quad ; \quad \Delta l_1 = \Delta l_2 = \frac{2.s_3 + w_3}{2} \tag{3. 76}$$

The cross junction

The cross junction follows the same methodology as the T junction. Four homogenous coplanar lines which length references are taken as showed in *Figure III.45* setup the equivalent model.

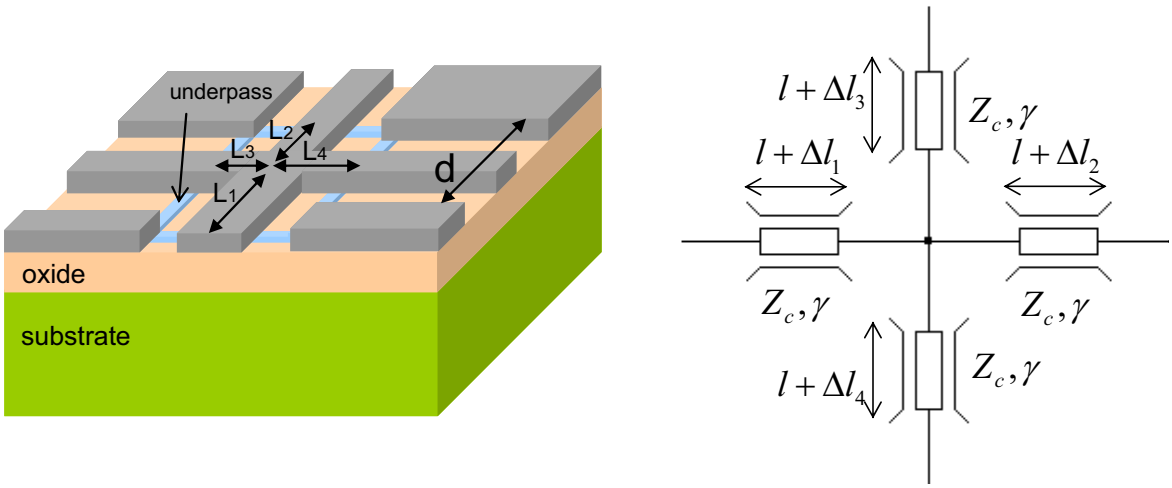


Figure III.45 Cross junction representation and the corresponding model

The equivalent length for the four coplanar lines is defined by:

$$\Delta l_1 = \Delta l_2 = \Delta l_3 = \Delta l_3 = \frac{d}{2} \tag{3. 77}$$

Chapter IV

Design of millimeter wave receiver building blocks

The feasibility of mm-wave low noise amplifiers and mixers in SiGe technologies has already been demonstrated in the scientific literature [6], [7]. In the meantime, 65nm node CMOS transistors have also shown performances compliant with millimeter wave applications (cf. *Chapter II*). In this Chapter, we explain first the dynamic range specification for a receiver. Then millimeter wave LNA and Mixer state of the art in industrial silicon technologies is presented. As a third part, millimeter wave LNA Design considerations are discussed. Finally, LNA and mixer simulations and measurements for millimeter wave systems (77GHz and 60GHz) are presented and a comparison between CMOS bulk and SOI for these target frequencies is examined.

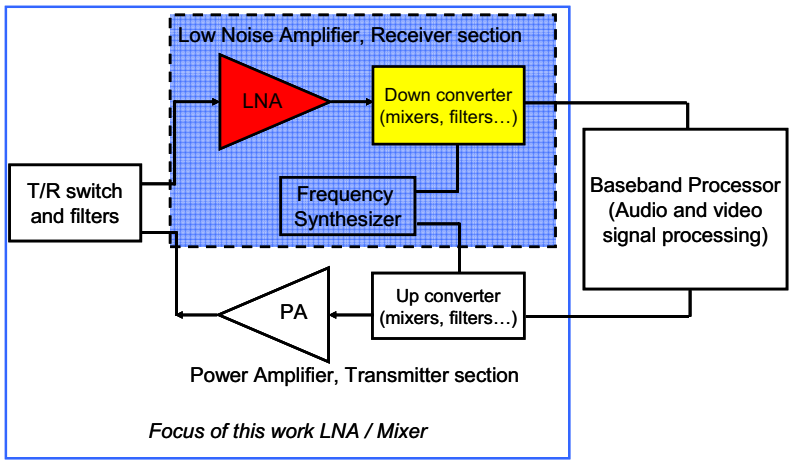


Figure IV.1. Low Noise Amplifier and down conversion Mixer illustration in a transceiver

IV.1. Dynamic range specification for a receiver

A RF receiver should match the dynamic range of the desired signal at the receiver input to the dynamic range of the signal processor. The dynamic range is defined as the range of desirable signal power levels over which the hardware will operate successfully. It is limited by noise, signal compression, interfering signals and their power levels.

IV.1.1. Noise Figure

In RF designs, the Noise Figure (NF) is the most widely used figure of merit to characterize a building block with respect to noise behavior. In receiver architecture, the Friis approach is generally used. This NF procedure analyze is based on the definition of the available signal power[1]. The *Friis* expression used for a cascade of n stages (each having an available power gain G_n and a noise factor F_n) is given by:

$$F_{total} = F_0 + \frac{F_{0+1} - 1}{G_0} + \frac{F_{0+2} - 1}{G_0 \cdot G_{0+1}} + \ldots \tag{4. 1}$$

With *G* and *F* in linear form, not in dB. The noise figure is defined as follow:

$$NF_{dB} = 10\log_{10}(F) \tag{4. 2}$$

From *(4. 1)*, it appears that the minimum overall noise requires minimizing individual noise power (especially F_1) and maximizing individual *G*'s (especially G_1). The bottom end dynamic range is limited by thermal noise at the input, and by the gain distribution and addition of noise as the signal progresses through the receiver. Once a signal is below the minimum detectable signal[2] level, it will be lost entirely (except for specialized spread spectrum receivers). The driving requirement is determined by the signal clarity needed at the signal processor. For analog systems, the signal starts to get noisy at about 10 dB above the noise floor. For digital systems, the allowable bit error rate determines the acceptable margin above the noise floor. Thus the signal with margin sets the minimum threshold

[1] The available signal power is the power of the signal delivered to the input of a two port network under a matched condition (when the input impedance of the network Z_{in} is matched to the source impedance Z_s the maximum signal power $\frac{V_s^2}{8 \cdot \Re(Z_s)}$ is delivered to the network)

[2] MDS in the literature

desirable signal level. The noise power at the input of the receiver will be amplified and attenuated like any other signal. Each component in the receiver chain will also add noise. Passive devices as well contribute a small amount of internally generated thermal noise. Thus the actual noise figure of a two ports passive network is the attenuation of that component. For instance, passive mixers generally have a noise figure equal or greater than the conversion loss. Active devices can exhibit loss or gain, and signal and noise power at the input will experience the same effect when transferred to the output.

IV.1.2. Linearity

The nonlinearity is defined as the difference between the expected output level, given by the low level gain, and the actual output level for a given input signal level. Intermodulation linearity is mostly characterized by third-order intermodulation product (IM_3). The input compression point (ICP_1) is used to estimate the overall linearity. It is defined as the power gain where the nonlinearities of the transistor reduce the power gain by 1dB over the small-signal linear power gain. As defined:

$$ICP_1 \equiv \left(RFout\left[dBm\right] - RFin\left[dBm\right]\right) - linear\ gain\left[dB\right] = -1\left[dB\right] \quad (4.3)$$

When two or more frequencies are applied to a nonlinear receiver, the output contains additional frequency components. The mix tones due to the nonlinear elements in the receiver or receiver component generate products that can be used to characterize the extent of the nonlinearity. This relationship dictates a 3:1 slope for the IM_3 products, as shown in *Figure IV.2*:

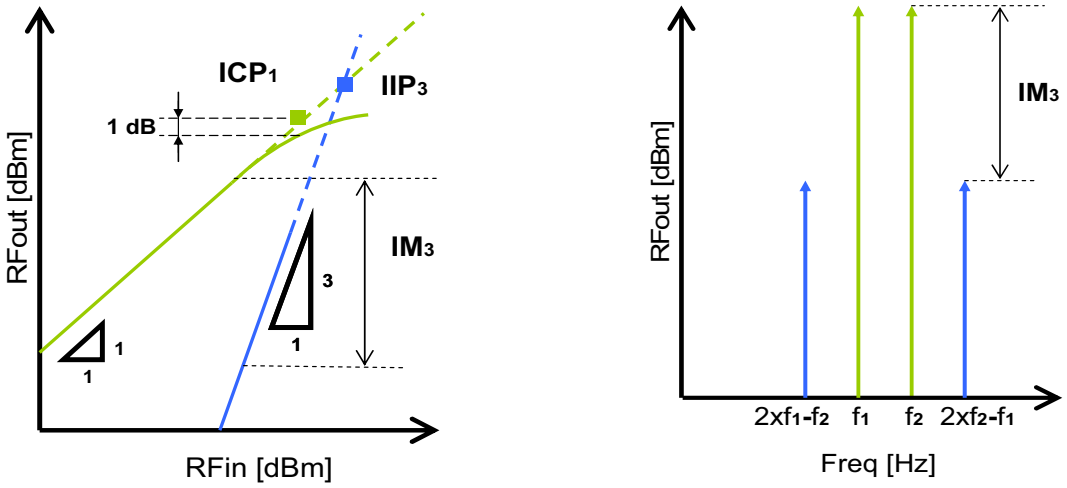


Figure IV.2. a) RFout vs. RFin showing third and second order intercepts point; b) Two tone spectrum response.

For low order nonlinearity (i.e., n<5), the ratio of IIP_3 and ICP_1 is a constant of ~10dB and IM_3 (cf. *Figure IV.2 – b*) can be defined as:

$$\left.\begin{array}{l} Linear\ response \Leftrightarrow RF_{out} = G_0 \times RFin \\ Third\ order\ response \Leftrightarrow RF_{out_3} = \frac{3}{4} \cdot G_3 \times RFin^3 \end{array}\right\} IM_3 = \frac{3 \cdot G_3 \cdot RFin^2}{4 \cdot G_0} \qquad (4.\ 4)$$

Thus it can be demonstrated that the third order intercept point, IIP_3 is linked to the input signal with respect to the following equation:

$$IIP_3 = RFin[dBm] + \frac{IM_3[dB]}{2} \qquad (4.\ 5)$$

In general, the n^{th} order intercept point is linked to the input power and is given by:

$$IIP_n = RFin[dBm] + \frac{\Delta IM_n[dB]}{n-1} \qquad (4.\ 6)$$

For a link budget analysis, the overall ICP_1, as the third order IIP_3 for a cascade of n stage (each having gain G_n and non linearity ICP_{1_n} or IIP_{3_n}) is:

$$ICP_{1total} = \left[\frac{1}{ICP_{1_n}} + \frac{1}{G_n \cdot ICP_{1_n-1}} + \frac{1}{G_n \cdot G_{n-1} \cdot ICP_{1_n-2}} + \ldots \right]^{-1} \qquad (4.\ 7)$$

$$IIP_{3total} = \left[\frac{1}{IIP_{3_0}} + \frac{G_0}{IIP_{3_1}} + \frac{G_0 \cdot G_1}{\cdot IIP_{3_2}} + \ldots + \frac{G_0 \cdot G_1 .. G_{n-1}}{\cdot IIP_{3_n}} \right]^{-1}$$

With G, ICP_{1_n} and IIP_{3_n} in linear form, not in dB. Therefore, for an n-stage circuit, there is an optimum for linearity as for noise *(4. 1)*. Maximum overall IIP_3 requires maximizing individual IIP_3's (especially IIP_{3_n}) and minimizing individual G's (especially G_1).

IV.1.3. Reception sensitivity and dynamic range

Sensitivity is the minimum level of input signal that the receiver must successfully detect and demodulate in the presence of noise. For instance, in Bluetooth system, the receiver must detect signal as small as -70dBm, with a BER[3] better than 0.1%.

The signal-to-noise ratio (SNR) and bit error rate (BER) are the key parameters that define the performance of the receiver. As shown in (4. 8), the signal-to-noise ratio is a simple measure describing the difference (in dB) between the signal power and the noise floor. This measure is sometimes modified to include the interference and described as the signal-to-noise and interference ratio S/(N+I). Signal-to-noise ratio is used to define energy-to noise (Eb/No) parameter needed to predict the BER performance of a receiver. The relationship between SNR and Eb/No is dependent on the modulation scheme of the received signal.

$$SNR = \frac{signal}{noise}$$

$$SNR\left[dB\right] = signal\left[dBm\right] - noise\left[dBm\right] \tag{4. 8}$$

The minimum signal power of a signal needed for demodulation must break through the noise floor. This input signal quantity is called Minimum Detectable Signal (MDS):

$$MDS\left[dBm\right] = SNR + 10\log\left(k \times T \times BW\left[Hz\right]\right)$$
$$+ \textit{additional Noise Power in N Hz Bandwith} \tag{4. 9}$$

With T the temperature in Kelvin, k the Boltzmann constant and BW the band width.

The MDS is linked to the two tone dynamic range of a receiver (DR) as follow [2]:

$$DR\left[dB\right] = \frac{2}{3}\left(IIP_3\left[dBm\right] - MDS\left[dBm\right]\right) \tag{4. 10}$$

An example of MDS calculation is given in appendix.

[3] Bit Error Rate (BER) in the literature. BER is the average number of erroneous bits in the received data.

IV.2. Millimeter wave LNA and Mixer state of the art in industrial silicon technologies

This section gives an overview of recent published CMOS LNA and Mixer for millimeter-wave applications.

Millimeter wave CMOS Low Noise Amplifiers

Table IV.1 presents some state of the art LNA implementations in both SOI CMOS and CMOS technologies. The LNA are either common source ([3], [11], [13]) or cascode designs ([4], [5], [8], [9], [10], [12], [14]) and most of the solutions employ T-Line.

CMOS node	f_T/f_{max} (GHz)	**Frequency (GHz)**	**Gain (dB)**	**S_{11}/S_{22} (dB)**	**Power (mW)**	**Noise Figure (dB)**	**Pin_{-1dB} (dBm)**	**IIP_3 (dBm)**	**Area (mm^2)**	**Ref.**
130nm	140/135	57	12.0	-15/-15	54 @1.5V	8.8	-10.0	-0.36***	-	[8]
130nm	108/91	55	24.7	-8/-5	79 @2.4V	8.0	-22.7	-12	0.48	[9]
SOI 90nm	149/147	40	9.5	-6/-8	40.8 @2.4V	4	-7.9	1.74***	-	[5]
90nm	107/180	61.3	17.9	-	21.6 @1.5V	5.2	-	-6.5***	0.86	[4]
90nm	140/170	58	14.5	-6/-6	24 @1.5V	4.5*	-24.5	-6.8	0.14	[10]
90nm	100/200	62	12.2	-12/-30	10.5 @1.5V	6.0*	-8.2	1.44***	0.48	[11]
90nm	107/180	52	25	-20/-17	110 @1.5V	5	-20 @48GHz	-10***	1.13	[12]
90nm	-	64	15.5	-25/-15	86 @1.65V	6.5	-11.7	-2.06***	0.52	[14]
SOI 65nm	160/200	80	7.2	-14/-10	70 @1V	5.7	-3.75*	5.89***	0.98	This work
65nm	-	60	11.5	-9/-7	104 @1.2V	5.6	-10	-0.36***	0.6	[13]
65nm	160/190	55	15	-18/-11	30 @1.2V	9.0**	-27	-17	0.74	This work
65nm	160/190	55	22.5	-22/-11	50 @1.2V	8.0**	-29	-20.5	0.74	This Work

* Simulated

** Simulated based on one frequency point measurement (cf.IV.5.1)

*** Estimated from the following relation: $ICP_1[dBm] = IIP_3[dBm] - 9.64[dBm]$

Table IV.1. State of the art mmW LNA solutions.

From the *Table IV.1*, at first order, it appears that the best performance is achieved with a 90nm CMOS node. But those results must be considered with care. First of all, a technology node does not predict the active and passive devices performance. For a given node the transistor can be low power (LP) or general purpose (GP), the gate oxide thickness can change (regarding of the supply voltage). Taking into account these considerations, the f_T *and* f_{max} figures of merit are more relevant. For an amplifier, f_{max} must be considered for gain evaluation. It uses conjugate matching of input and output transistor ports. The f_T figure of merit can be used to estimate the device noise performance (cf. *Chapter II*). The second thing to consider is the BEOL thickness of each node. The trend when moving from one CMOS node to the next is the vertical shrink of the BEOL together with the decrease of the metal and dielectric thicknesses and of the metal pitch in order to increase integration density [1]. Hence, metal resistance and parasitic losses from substrate increase. The availability of High Resistivity (HR) SOI substrates alleviate these issues, by reducing all parasitic losses towards the substrate (*Chapter III*, [3] and [5]). Therefore, in *Table IV.1* 90nm and 65nm node can be considered as equal performance (for mm-wave LNA design). Another important parameter to consider when circuits are compared is the power consumption and the supply voltage. The circuit manufacturability is dictated by the respect of electromigration design rules. Small spiral inductors like those used in [10] offer a good ratio between performances and occupied area. But having good quality factor and characteristic impedance high enough require small width conductors not compliant with design for manufacturing. In the same way, using a supply voltage over the nominal value required for the device is not compliant with design rules [14]. Finally, in order to benchmark different LNA, a last point must be examined: the trade off between the input insertion losses and the noise matching. Except for co-design between antenna and LNA, the input characteristic of a LNA must be set as close as possible to 50Ω. This condition is considered to be reached if S_{11}<-10dB. This is not the case in [5], [9], [10] and [13].

Millimeter wave CMOS Mixers

There are two different kinds of mixer topologies that have been published in CMOS. The first one is the active mixers obtained with Gilbert cells or with simple Gm-cells, implemented with single ended or balanced RF and LO inputs. The second one consists of passive resistive mixers, made with a single NMOS transistor LO-pumped either on the gate or on the source, while the RF is applied on the drain, the gate or combined together with the LO on the gate terminal.

Table IV.2 presents state of the art mixer implementations in CMOS:

CMOS node	Frequency (GHz)	Conversion gain (dB)	Noise Figure (dB)	LO power (dBm)	LO to RF isolation (dB)	ICP_1 (dBm)	IIP_3 (dBm)	Topology	Power (mW)	Ref.
180nm	24	13	-	-	-	-	-	Active single to balanced	6	[15]
130nm	60	-2	11.5**	0	-12	-3.5	-	Active single ended	2.4	[16]
90nm	60	-11.6	12.6*	4	-	6	16.5	Resistive single ended	~0	[17]
90nm	31	-11	-	9.7	-27	-	3	Resistive Source pumped	~0	[18]
SOI 90nm	27	-10.3	11.3*	0	-24	-	12.7	Resistive Gate pumped	~0	[19]
65nm	60	-12.5	13.5*	8.7	-35	5	-	Resistive single to balanced	~0	[20]
65nm	60	-14.8	20*	0	-20	-4**	6*	Resistive gate pumped	~0	This Work
SOI 65nm	60	-7.7**	9*	-5	-20**	-10**	0**	Resistive drain pumped	~0	This work

* Estimated (cf. *IV.1.1*)
** Simulated

Table IV.2. State of the art mm-wave down-conversion CMOS mixers.

The Table IV.2 analysis shows that active mixer offers better conversion gain, less LO power and generally a good noise figure. This, to the detriment of the power consumption and the linearity. The resistive mixers present almost zero DC power consumption and a very linear behavior [17], [18], [19] and [20]. Their main drawbacks consist of high conversion losses and the need of a higher LO power with respect to that for the active mixers. For mm-wave mixers, the SOI CMOS seems to be the best compromise. Since this technology gives the possibility to use HR substrate (cf. *Chapter III*), it becomes possible to obtain less losses, low noise resistive mixer [19] while keeping the advantages of the resistive mixer topology.

IV.3. Millimeter wave LNA Design considerations

In this section, millimeter wave LNA design considerations are examined. Mixer design is not processed here but for more information the reader can refer to [21].

IV.3.1. LNA stability

The primary concern in the design of a high-frequency amplifier is to ensure that the active device does not oscillate at any frequency and especially at the frequency of operation. The Figure IV.3 represents a two port active device:

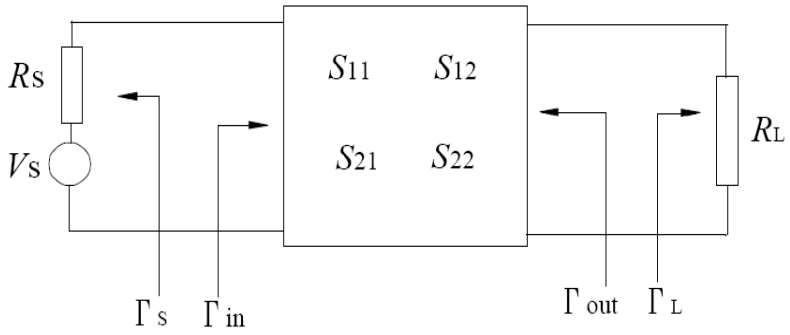


Figure IV.3. Stability conditions of a two-port active device

A two-port active device is unconditionally stable if both its input and output impedances have positive real part for any passive source and load terminations. In S-parameter terminology, it is defined as follow:

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \qquad with \qquad Z_{in} = \frac{\Gamma_{in} - 1}{\Gamma_{in} + 1}$$

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \qquad with \qquad Z_{out} = \frac{\Gamma_{out} - 1}{\Gamma_{out} + 1} \tag{4. 11}$$

$$|\Gamma_{in}| < 1 \quad \text{and} \quad |\Gamma_{out}| < 1 \quad \text{for any passive } \Gamma_L, \Gamma_S$$

The necessary and sufficient conditions for unconditionally stable operation are:

- $|S_{11}| < 1$ and $|S_{22}| < 1$
- $1 - |S_{11}|^2 > |S_{12}S_{21}|$ and $1 - |S_{22}|^2 > |S_{12}S_{21}|$

- The stability factor *K*, also known as *Rollet* stability factor, is greater than unity and the modulus of Δ is less than 1

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}||S_{21}|} \tag{4. 12}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

Considering that the *K* factor *(4. 12)* of an NMOS transistor is lower than one up to mm-wave frequencies (*Figure IV.4*), the design must take into account any potential instability problems.

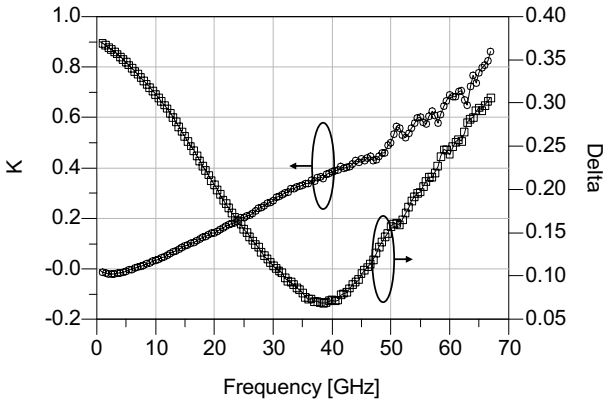


Figure IV.4. Measured K and |Δ| factors; Ids=350mA/mm; n-MOSFET, 48x1.33x0.06μm².

IV.3.1.a. Techniques to achieve stability

In the case of potentially unstable devices, there is no maximum gain design because maximum gain implies a gain of infinity, in other words, oscillation. A potentially unstable device is a device which has input and output reflection coefficients greater than unity for particuliar source and load terminations. In order to achieve stability, there are some stabilization techniques as shown on *Figure IV.5*:

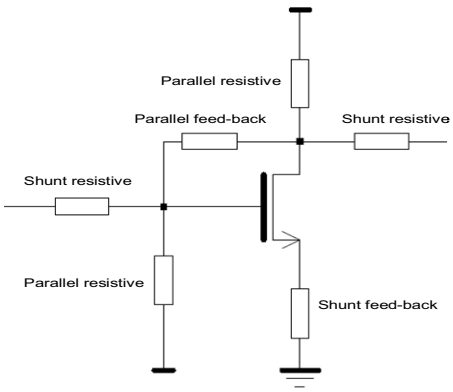


Figure IV.5. Illustration of stabilization techniques

There are several ways to stabilize a transistor (*Figure IV.5*) but for a LNA some of them have to be proscribed. Shunt resistive stabilization is too noisy, parallel feed-back are not advisable if the available gain is low. From those considerations, the two common used solutions for low noise amplifiers are series feedback (if the gain is enough at the operating frequency) and parallel resistive stabilization. The series feedback is achieved by using an inductor in order to simultaneous match noise and gain as described in section IV.3.2.c.

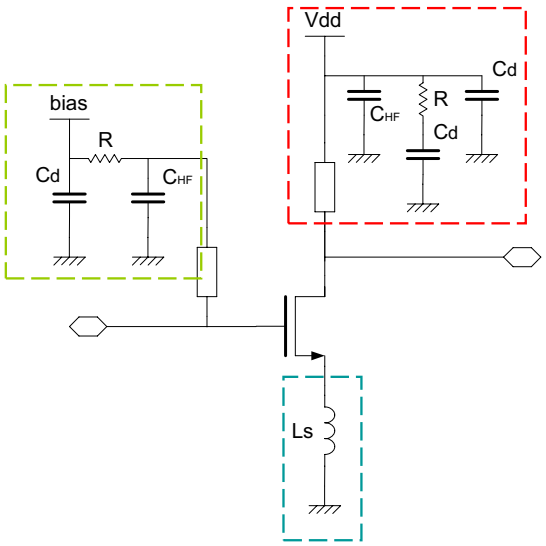


Figure IV.6. Two stabilization techniques: parallel resistive and shunt feed-back

The Figure IV.6 illustrates two high frequency stabilization techniques. C_d are decoupling capacitors, typical values for a mm-wave design are in the range of 10 to 20pF. C_{HF} capacitors are used to shunt the two parallel stubs at the operating frequency, the value varies from 50 to 500fF. The R resistance is used to reduce the quality factor of the resonant RLC network formed with the interconnect inductors. The R value is from 2 to 50Ω. Figure IV.7 illustrates the effect of a parallel resistive stabilization on the K factor and the MSG/MAG:

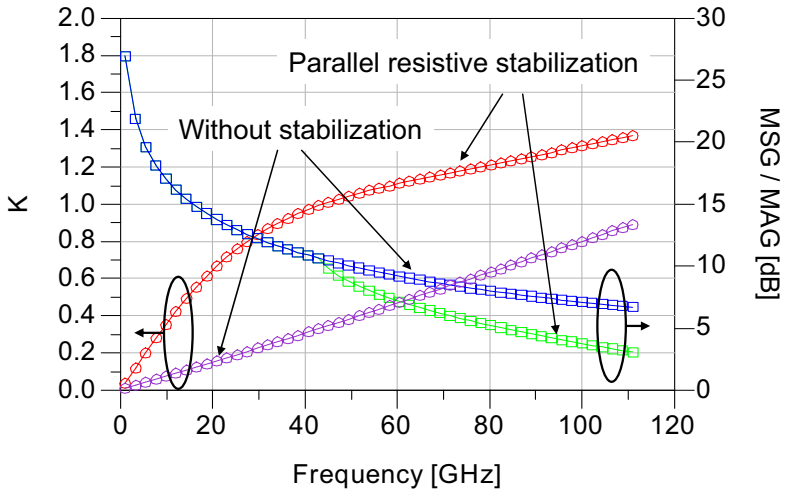


Figure IV.7. Simulated K factor and MSG/MAG with and without parallel resistive stabilization; Ids=300mA/mm; n-MOSFET, 64x1.33x0.06µm²

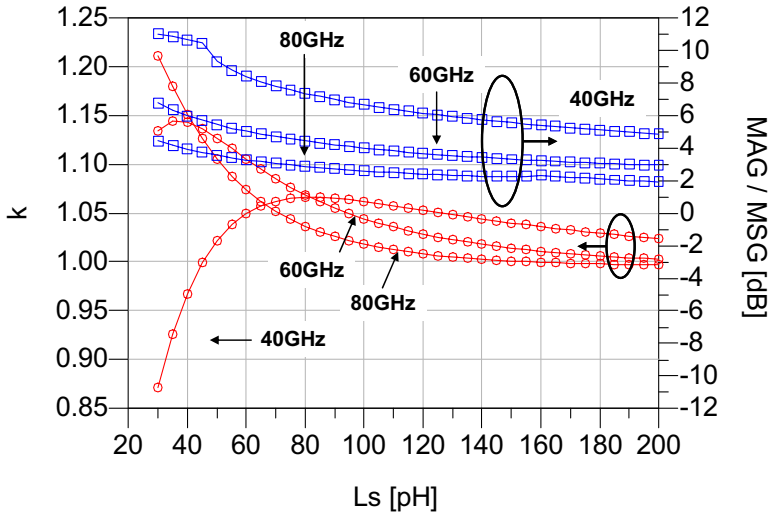


Figure IV.8. Simulated K factor and MSG/MAG with a shunt feed-back inductors (Ls) stabilization technique at 40, 60 and 80GHz ; Ids=300mA/mm; n-MOSFET, 64x1.33x0.06µm²

The *Figure IV.8* illustrates the series feedback technique for different values of L_s. It should be noticed that this technique is lowering the gain at high frequency. The low frequency stabilization is naturally achieved by the input and output matching network as illustrated in the following example:

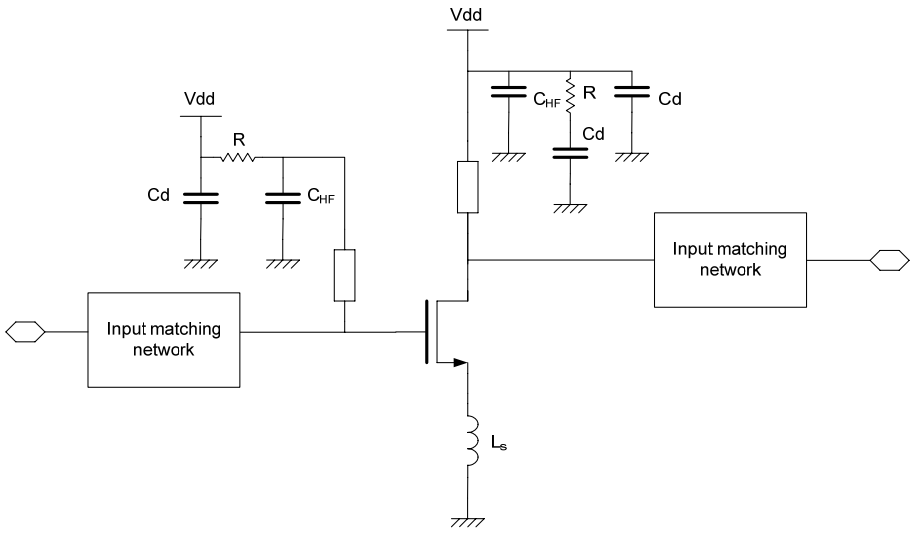


Figure IV.9. stabilized amplifier with input and output matching

The Figure IV.10 shows the simulated S-parameters and the k factor of a 60GHz common source amplifier using the same topology as shown on *Figure IV.9*. The in-band stability is achieved with both parallel resistive and series feedback inductor. The out of band instability rejection is obtained thanks to the input and output matching.

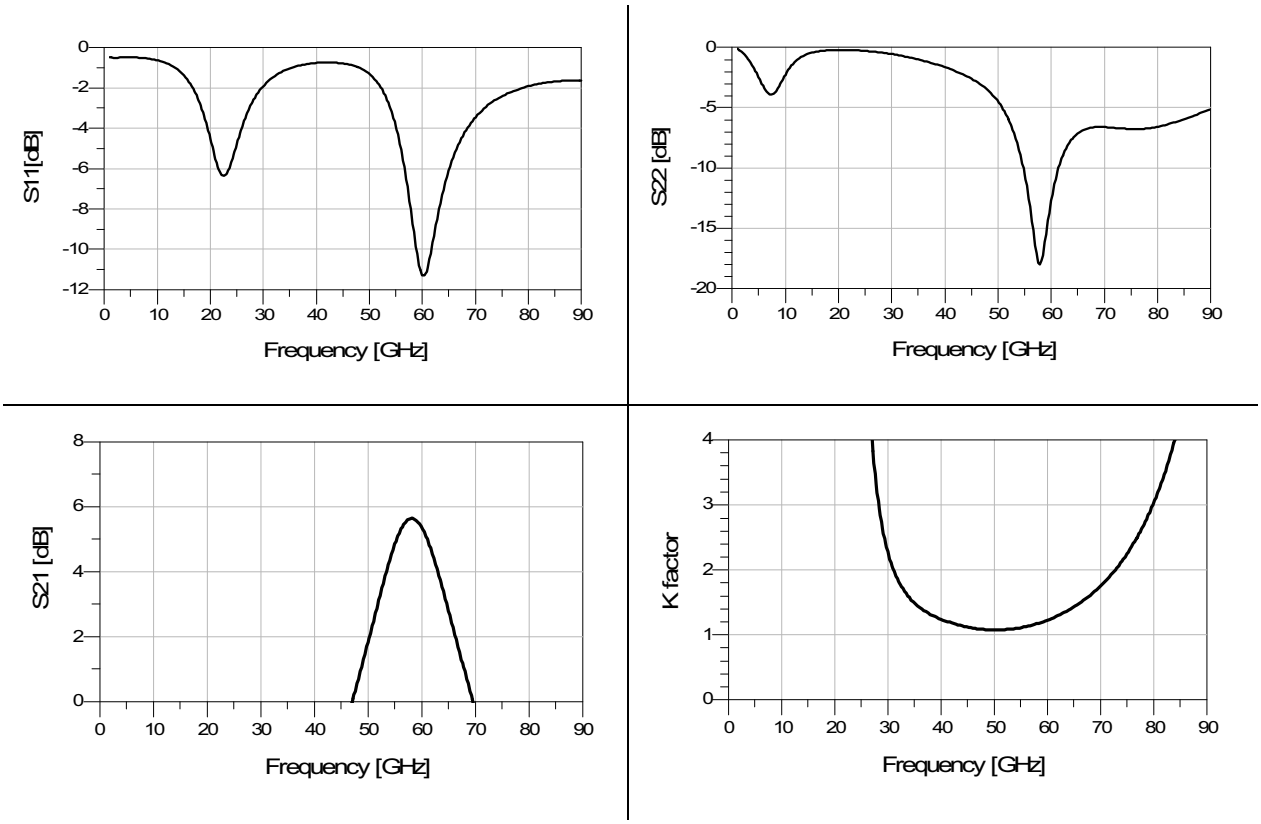


Figure IV.10. Simulated S-parameters and the k factor of a 60GHz common source amplifier

IV.3.1.b. Stability in multi-stages amplifiers

When two separate amplifiers are combined into a *multi-stage* amplifier (*Figure IV.11*), it is necessary to be very careful to ensure that the resulting amplifier is stable. Provided that both stages are unconditionally stable over the entire frequency range, the multi-stage amplifier will be stable as well. If one or more of the stages is not unconditionally stable, care must be taken when designing the interstage matching.

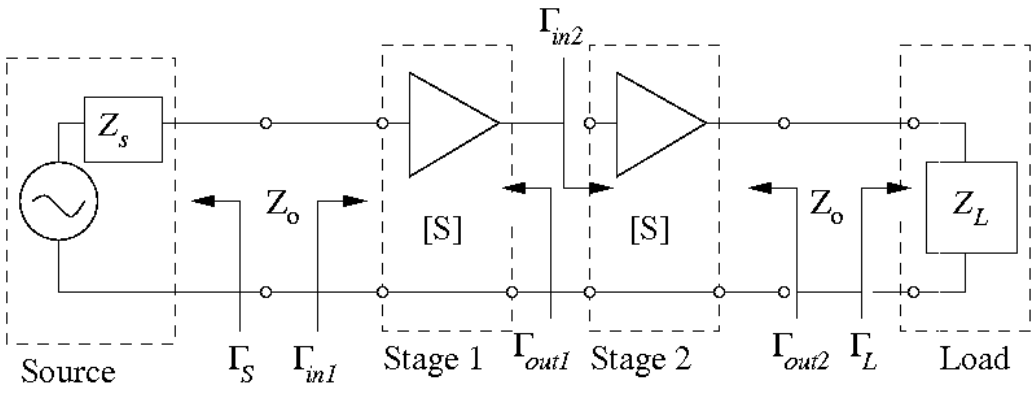


Figure IV.11. Multi-stages amplifier illustration

One approach is to design Γ_{out1} and Γ_{in2} to be at the same time matched at the system impedance (usually 50 Ω), and ensure that both are stable for that impedance. Another

option is to allow Γ_{out1} and Γ_{in2} to take on any values such that $\Gamma_{out1} = \Gamma_{in2}^{*}$, resulting in optimum power match. This requires that Γ_{out1} should be in the stable region for the source stability circle[4] of stage 2, and that Γ_{in2} be in the stable region of the load stability circle for stage 1. In this case the amplifier is defined as potentially stable. One method of simulating oscillation between stages is presented in [22].

IV.3.2. LNA design

The first stage of a multistage amplifier or a single-stage amplifier is normally designed for a minimum noise figure, maximum power gain, and a minimum input and output insertion losses. In a multistage amplifier the output insertion losses of the first stage is usually not a critical parameter. When the constraint on the output insertion losses is relaxed, there is a better degree of freedom to achieve the other design requirements.

IV.3.2.a. Noise Figure for two ports network amplifier

The noise parameters of a two ports amplifier are analyzed in order to study the minimum noise conditions :

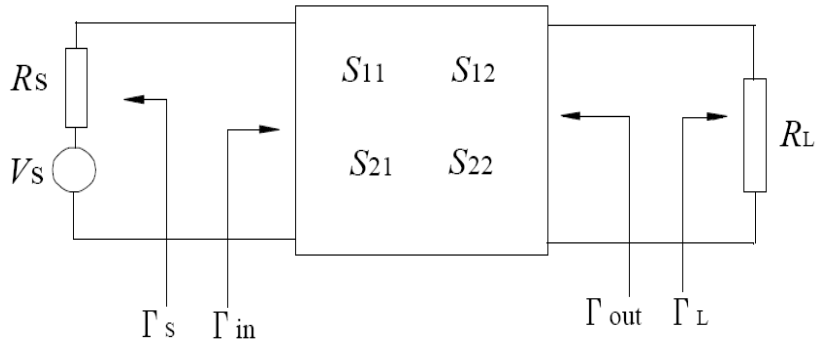


Figure IV.12. Two ports network amplifier

Looking at a two ports network amplifier (*Figure IV.12*), the noise figure is given by:

$$F = F_{\min} + \frac{R_n \left| Y_s - Y_{opt} \right|^2}{\Re\left(Y_S\right)} \qquad (4.13)$$

Where:

- F_{min} is the minimum noise factor with respect to Y_s
- R_n is the equivalent noise resistance of the device

[4] A graphical method can be used to determine which of the terminations Γ_S and Γ_L could produce instability [23].

- Y_{opt} is the optimum admittance at which $F=F_{min}$

Y_{opt} is defined as follow:

$$Y_{opt} = G_{opt} + jB_{opt} \tag{4. 14}$$

With:

$$Y_S = \frac{1-\Gamma_S}{1+\Gamma_S}, \qquad Y_{opt} = \frac{1-\Gamma_{opt}}{1+\Gamma_{opt}} \tag{4. 15}$$

It results then:

$$F = F_{\min} + \frac{4 \cdot R_n \left|\Gamma_s - \Gamma_{opt}\right|^2}{\left(1-\left|\Gamma_s\right|^2\right)\left|1+\Gamma_{opt}\right|^2} \tag{4. 16}$$

It can be noticed that R_n indicates the dependence of F_{min} on Y_{opt} or Γ_{opt}. A low value of R_n is desirable to insure a noise figure insensitivity on input impedance source.

IV.3.2.b. Transistor impedance matching

The first step in a LNA design consists in choosing the right MOSFET length, width, number of fingers and number of gate accesses. These considerations are driven by different parameters for low noise amplification:

- The minimum Noise Figure of the device
- The ability to obtain simultaneously noise and gain matching
- The maximum gain
- The device stability
- The power consumption

Some of these parameters are antagonist, therefore a trade-off is necessary.

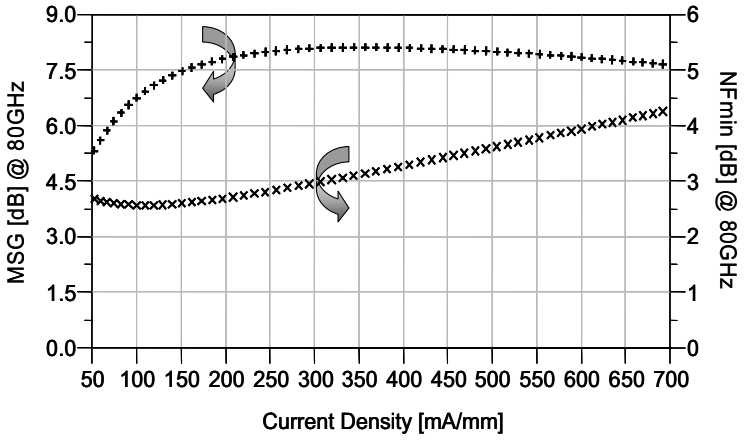


Figure IV.13. Simulated Maximum Stable Gain and NFmin versus current density ; Vds=1.2V ; Freq=80GHz ; n-MOSFET Floating Body, 48x1.33x0.06µm²

The Figure IV.13 shows that for CMOS MOSFET transistors there is an optimal current density for minimum noise and maximum gain. Usually the minimum noise figure is achieved for a density of 0.15mA/µm and the maximum gain is obtained for 0.3mA/µm. In multi-stage amplifiers the first stage is usually biased at 0.15mA/µm in order to minimize the overall noise *(4. 1)*. For a single stage, a trade-off must be dealt between noise and gain. Once the optimum bias is found the width of the transistor is determined in order to minimize R_n *(4. 16)* and with respect to the power consumption budget. The *Figure IV.14* shows that for a given finger size, the width of a NMOS transistor does not act on the minimum noise figure but it does impact the noise parameter R_n.

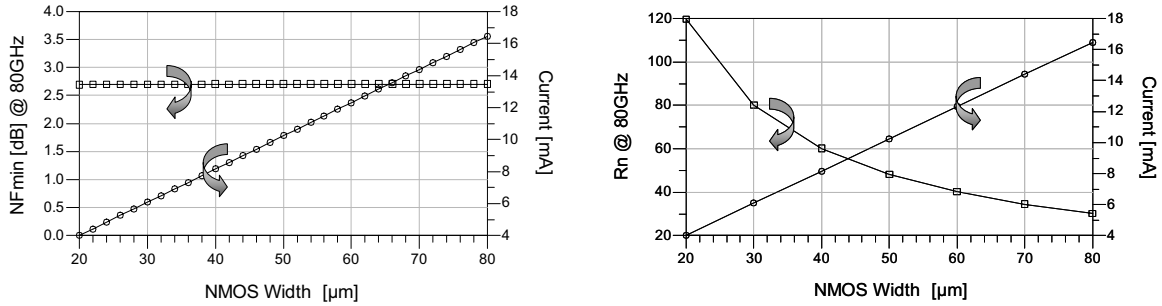


Figure IV.14. Simulated NFmin, Rn and Current consumption versus NMOS width ; Vds=1.2V ; Ids=200mA/mm; Freq=80GHz ; n-MOSFET Floating Body; Finger size=1µm; L=0.06µm

Two other geometrical parameters can be used to improve transistor's performance: the unit finger size and the number of gate accesses. Therefore, the second step consists in finding an optimal finger width to maximize the gain and minimize the NF_{min}. *Figure IV.15* illustrates the impact of these two parameters on the maximum stable gain (MSG) and on the minimum noise figure (NF_{min}):

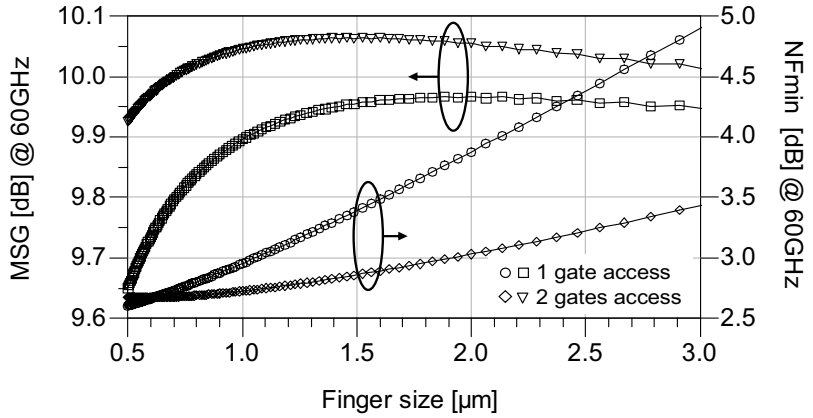


Figure IV.15. Simulated Maximum Stable Gain and NFmin versus finger size for single and double gates access layout ; Vds=1.2V ; Ids=350mA/mm ; Freq=60GHz ; n-MOSFET, 48x1.33x0.06µm²

As shown in *Figure IV.15* there is an optimum finger size that maximizes the gain. At first order, the smallest finger would be the best since the gate resistance value is reduced (cf. f_T / f_{max} formulas in *Chapter II*). But for small finger size (<1µm) the fringing capacitances coming from the contacts become preponderant over the other capacitances reducing f_T and

f_{max}. This effect does not appear for the NF_{min} because it is above all sensitive to the gate resistance (except for very small finger value <0.5µm where the decreasing of f_T balance the gate resistance reduction).

IV.3.2.b.iNMOS layout optimization for millimeter wave design

The Figure IV.16 shows the measured performances of an n-MOSFET transistor including the intrinsic device and all accesses up to metal 1 (such as it is presented in a layout p-cell in a design kit). The measured f_T and f_{max} are 160 and 190GHz respectively. When taking into account the metal access from the last metal (M6) towards the intrinsic transistor (i.e. the extrinsic device) the f_T and f_{max} become 140GHz and 170GHz respectively.

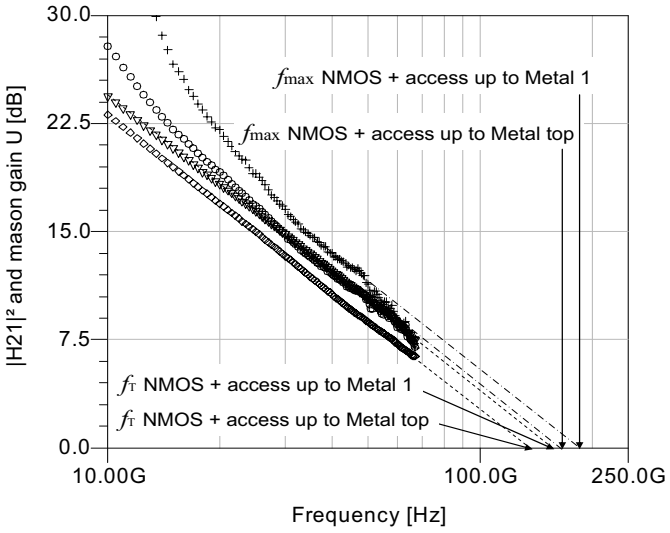


Figure IV.16. Measured |H21|² & Mason gain U versus frequency; Vds=1.2V; Ids=350mA/mm; n-MOSFET, 48x1.33x0.06µm².

These results demonstrate how the high frequency performance is sensitive to layout parasitic [1], [3]. Considering the metal access parasitic R_{ga}, C_{gsa} and C_{gda}, the expression of f_{max} and f_T become:

$$f_{\max} \approx \frac{g_m}{2\pi \cdot \left(C_{gs}+C_{gsa}\right) \cdot 2\sqrt{\left(R_g+R_{ga}+R_s+R_i\right) \cdot \left(g_d + g_m \frac{C_{gd}+C_{gda}}{C_{gs}+C_{gsa}}\right)}} \tag{4. 17}$$

$$f_T \approx \frac{g_m}{2\pi \cdot \left(C_{gs}+C_{gsa}\right)\sqrt{1+2 \cdot \frac{C_{gd}+C_{gda}}{C_{gs}+C_{gsa}}}} \tag{4. 18}$$

It appears that f_T is sensitive to parasitic capacitances and f_{max} is above all sensitive to the gate resistance. In this work, taking into account these considerations an optimum layout structure has been generated [3]. Several transistor layout topologies are used in order to

minimize the extrinsic parasitic elements added to the intrinsic transistor core [3][11]. In comparison, the classical in-line approach is showed in *Figure IV.17*:

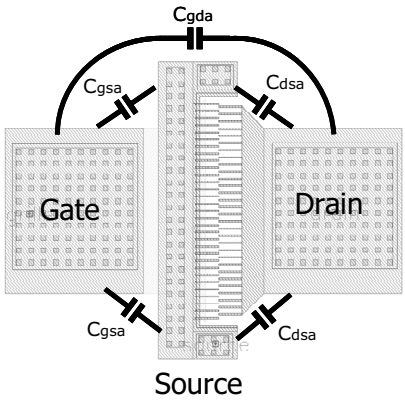


Figure IV.17. In-line layout of n-MOS transistors

The transistor layout structure proposed in this work (also presented in [3]) is depicted in *Figure IV.18* . In this case the transistor is divided into two equal parts with a double contacted gate. This allows minimizing the parasitic capacitances and the gate resistance while using coplanar accesses [25]. Source contacts are located on the transistor periphery making easier the contact to the coplanar ground plane. Finally, this structure allows an impedance matched access towards and from the active device to the rest of the circuit.

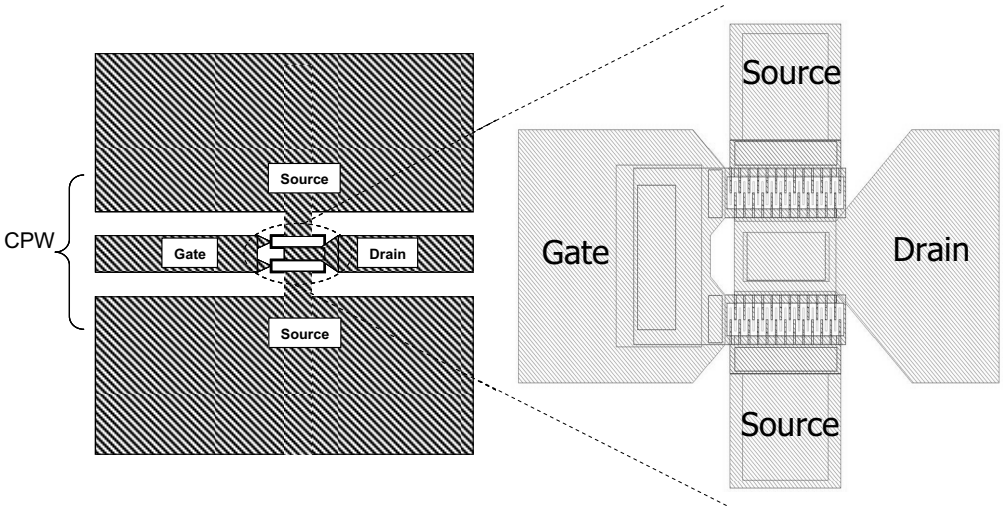


Figure IV.18. Layout of n-MOS transistors to maximize mm-wave performances and to limit discontinuity [3]

IV.3.2.c. LNA topologies

Numerous solutions to design mm-wave LNAs are already available in the scientific literature (cf. *Table IV.1*). First of all, it appears that at millimeter wave frequency, the CMOS transistor gain is not sufficient to provide a single stage LNA solution. Each stage of a multi-stage LNA can use a specific topology to improve noise, gain or linearity (cf. *IV.1.2*).

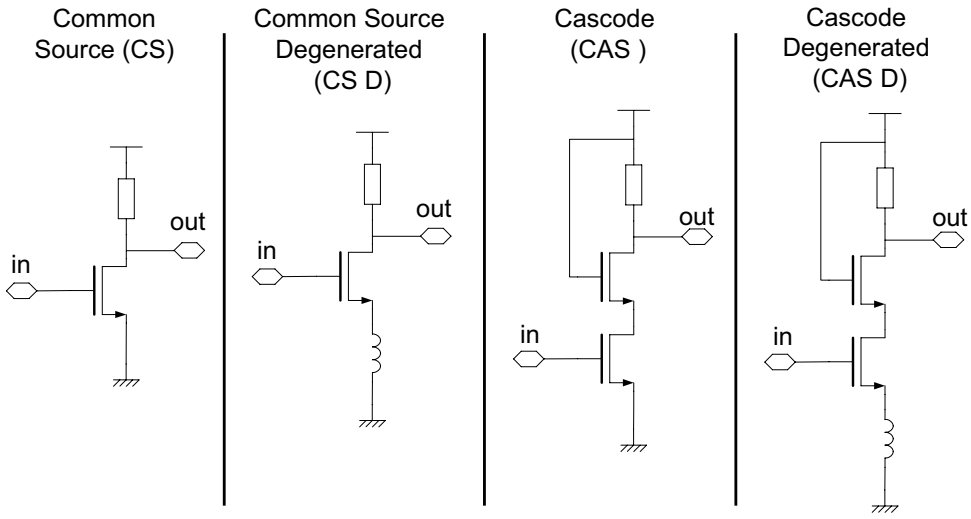


Figure IV.19. Classical LNA topologies (bias not shown)

The *Figure IV.19* shows 4 classical LNA topologies found in the literature [3]. *Figure IV.20* gives a simulated comparison between these four architectures.

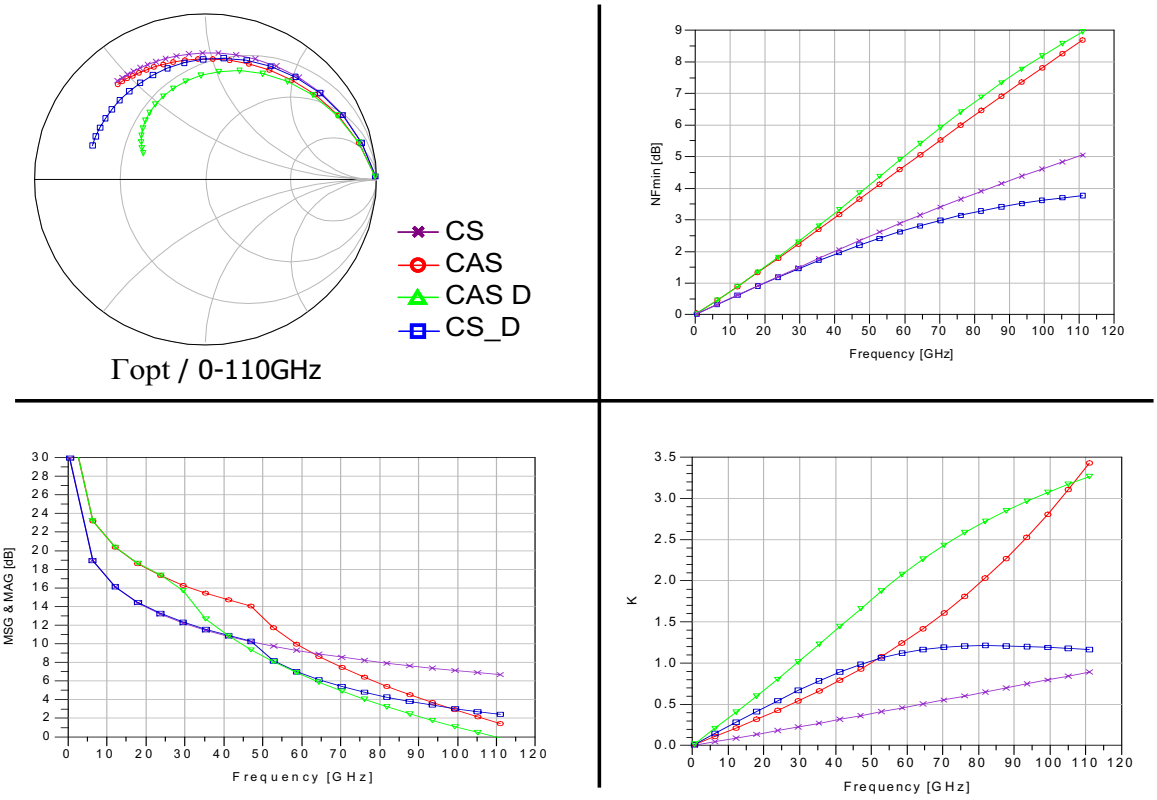


Figure IV.20. Simulated Γopt, NFmin, MSG/MAG and K; Ids=350mA/mm; n-MOSFET, 48x1.33x0.06µm².

Looking at the Γ_{opt} simulation, it appears that degenerated architectures allow a better simultaneous gain/noise matching because Γ_{opt} is closer to the 50Ω impedance. This effect is provided by the shunt-feed back brought by the degenerated inductance which impacts on the imaginary part of Y_{opt} *(4. 14)*. Concerning the MSG/MAG and the K factor it stands out that the common source is not a stable topology, as expressed in *IV.3.1,* implying that at high

frequency the MSG /MAG is higher for this topology. The cascode topology provides better gain for design unders 90GHz but suffers of poor noise figure. In a cascode architecture, at high frequency the parasitic capacitance at the drain node of the first transistor (common source) significantly reduces the overall impedance to ground and thus increases the noise contribution from the second transistor (common gate) to the cascode structure [3], [24]. The common source degenerated structure offers the better noise and a good stability but shows about 30% less gain in comparison with cascode at 60GHz.

Taking into account the best ratio between noise and gain it stands out that cascode topology is well adapted for frequencies below 60GHz. Beyond this frequency a simple common source offers the best trade but requires stabilization.

IV.3.2.d. Millimeter wave matching network

In this section, matching networks using transmission lines are presented. The same methodology can be used with lumped components such as inductors and capacitors [24].

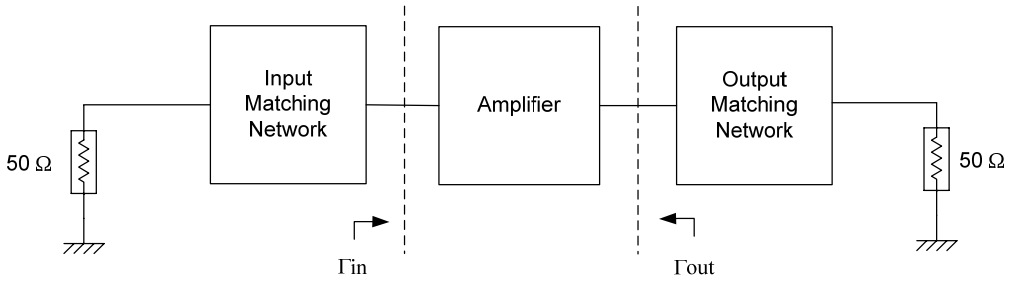


Figure IV.21. RF amplifier circuit

IV.3.2.d.iMillimeter wave input matching network

In amplifier design, a complex load impedance is required for the output and complex source impedance for the input, even though the final input and output connections are two 50Ω lines. In a typical amplifier circuit as shown in *Figure IV.21*, the function of the input matching networks is to transform the 50Ω terminal impedances to the required complex source (Γ_{in}* for gain matching or Γ_{opt} for noise matching) and load impedance Γ_{out}*. *Figure IV.22* shows Γ_{opt} and Γ_{in} of a NMOS transistor from 40GHz to 100GHz.

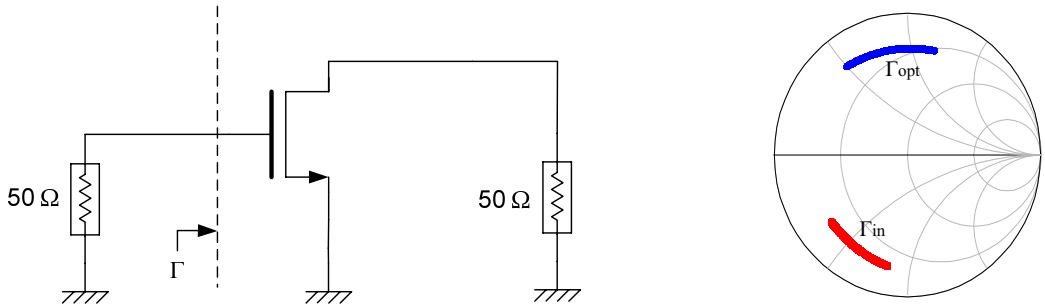


Figure IV.22. Simulated Γ_{in} and Γ_{opt} from 40GHz to 100GHz (bias not shown); Ids=150mA/mm; n-MOSFET, 48x1.33x0.06µm².

As shown in the Smith chart, Γ_{opt} and Γ_{in} are far from the center 50Ω. As a first step, a parallel stub is added in order to bring Γ_{opt} and Γ_{in} close to 50Ω. Using a parallel stub enables to combine input matching and biasing of the MOS transistor. The *Figure IV.23* shows the effects of a parallel stub on Γ_{opt} and Γ_{in}.

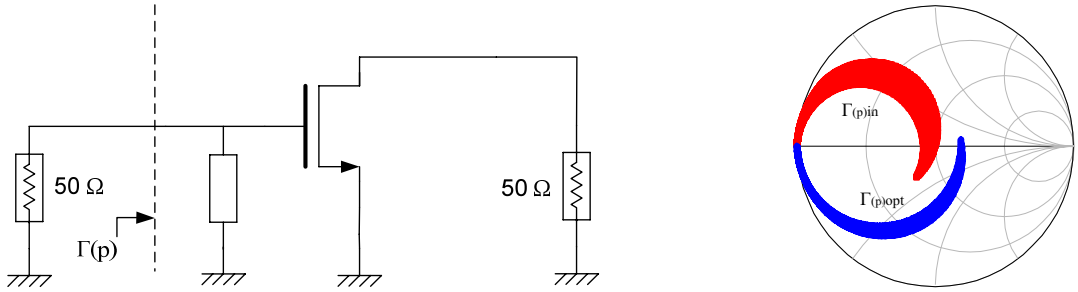


Figure IV.23. Simulated Γ_{in} and Γ_{opt} from 40GHz to 100GHz with parallel stub (bias not shown) ; Ids=150mA/mm; n-MOSFET, 48x1.33x0.06µm²

In order to achieve noise and gain matching simultaneously, a series T-line can be used as shown on *Figure IV.24*. Nevertheless, since the added T-line is not perfect, it must be small in order to not increase the overall noise.

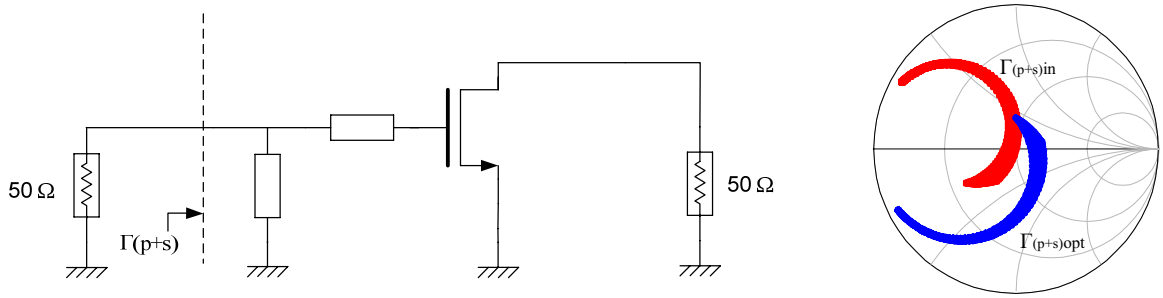


Figure IV.24. Simulated Γ_{in} and Γ_{opt} from 40GHz to 100GHz with parallel and series transmission lines (bias not shown) ; Ids=150mA/mm; n-MOSFET, 48x1.33x0.06µm²

As shown on *Figure IV.24*, the use of series and parallel T-lines brings Γ_{opt} and Γ_{in} close to 50Ω. The matching methodology uses the same method for inductor degenerated transistor (cf. *IV.3.2.c*).

IV.3.2.d.ii Inter-stage network in cascode topology

To improve the gain/noise performances of the cascode design, the parasitic capacitance at the drain M_1 can be shunt resonated by adding a matching network as shown on *Figure IV.25*. This inter-stage matching can be achieved with a serial inductor [10] or a parallel LC network [24]. In this work a serial T-Line has been used (*IV.5.1)*. However, high frequency stability evaluation becomes impossible with the K factor methodology describes in *IV.3.1.a*. Since the cascode has to be considered as a two stages amplifier, a normal approach should lead to a separate analysis for each stage. One important node prone to oscillation at high frequencies is the gate of the cascode transistor. Since the input impedance of a capacitively degenerated device has a negative part, a high Q parasitic inductance at the gate (coming from layout interconnects) can form a Colpitts oscillator [24]. To improve stability, a resistor can be added to the gate of the cascode to decrease the Q of the resonator. In order to not degrade the noise figure, the value of the resistor must be not too large.

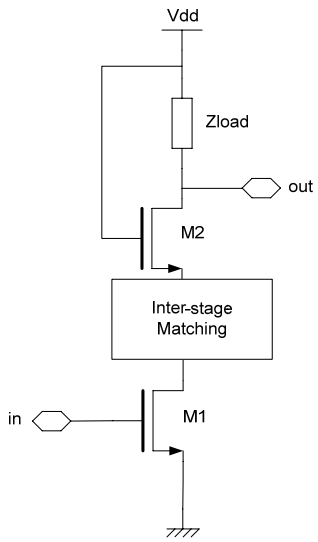


Figure IV.25. Cascode with inter-stage matching

IV.3.2.d.iii Output matching network

Once input matching is achieved, the output matching must be set up. In LNA design, in order to maximize the gain (contrary to PA design where high power is targeted) the complex conjugate impedance must be presented to the output of the amplifier (Γ_{out}*). The output matching network follows the same methodology described in *IV.3.2.d.i*. Serial and parallel T-lines (also used for power supply) are used in order to achieve the matching (*Figure IV.26*). If the length of L_s is not compatible with layout requirements, an additional $\lambda/4$ line can be used to achieve matching with L_s and L_p. However, this second solution adds extra output losses and additional chip area.

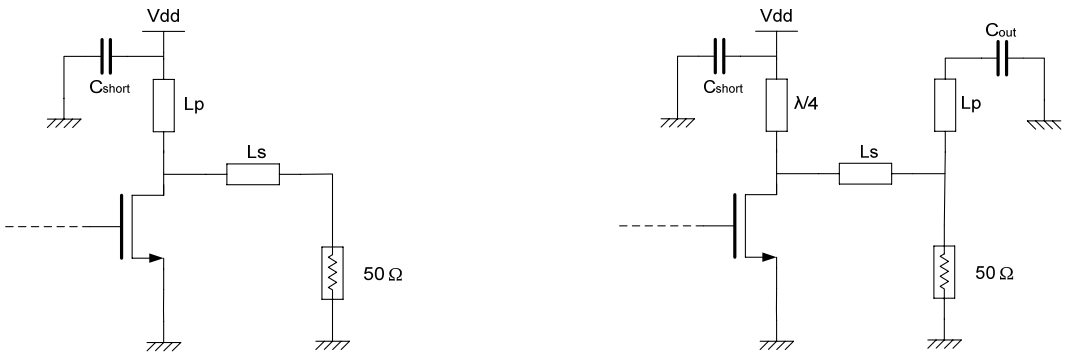


Figure IV.26. Output matching network options

IV.3.3. LNA design methodology summary

The following figure depicts the LNA design methodology applied in this work:

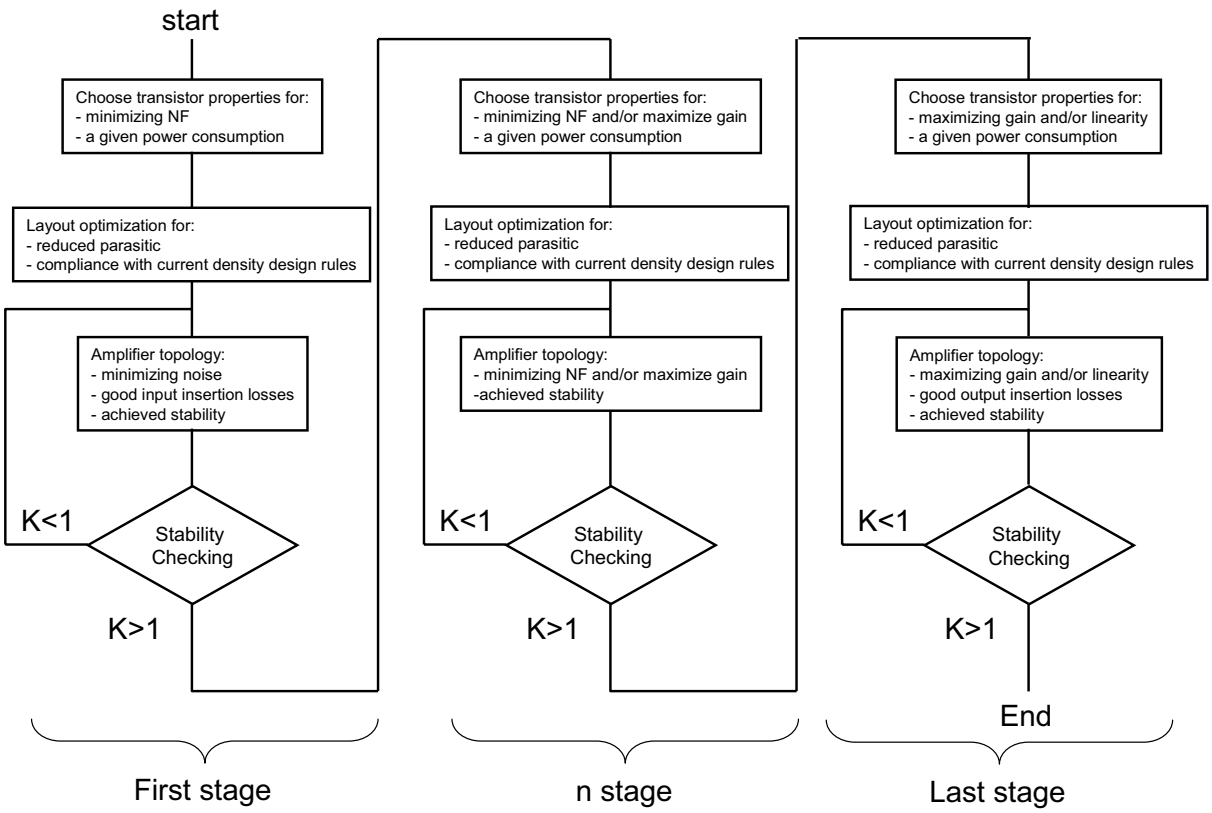


Figure IV.27. n-stages LNA design methodology

Following this design methodology, it is possible to achieve the best performance in respect with given specifications.

IV.4. Millimeter wave CMOS SOI building blocks

In this section, SOI CMOS LNA and mixer simulations and measurements results for 80GHz millimeter wave systems are presented. These circuits used active and passive devices presented in the previous chapters. Since a reduced RF design kit was available for this technology when the design was carried out, the models used are those presented in chapters II and III. The circuits were simulated with *Agilent* ADS simulator and the BSIM4 transistor model. Transmission lines were modeled using TLINP model from ADS library and an adapted RLCG model for multilayered silicon (cf. *Chapter III*). Input and output coplanar pads have been designed as coplanar lines with 50 Ohms characteristic impedances. The circuits were fabricated using the STMicroelectronics's manufacturing process SOI CMOS065 LP with a MOSFET physical gate length of 60nm and a 6 metal layers BEOL (5 thins, 1 thick). They were measured on wafer and all measurements were performed at a source and load impedance of 50Ω. S-parameters were measured using 0-110GHz network analyzer. The noise figure test bench consists of a noise figure meter, a test set extension and a mixer allowing accurate measurement from 75 to 110 GHz.

IV.4.1. 80GHz and 94GHz CMOS SOI single stage common source amplifier

The first design is a single stage common source amplifier (*Figure IV.28*). The main goal of this circuit is to calibrate the active and passive models previously studied and to benchmark the technology for mm-wave applications.

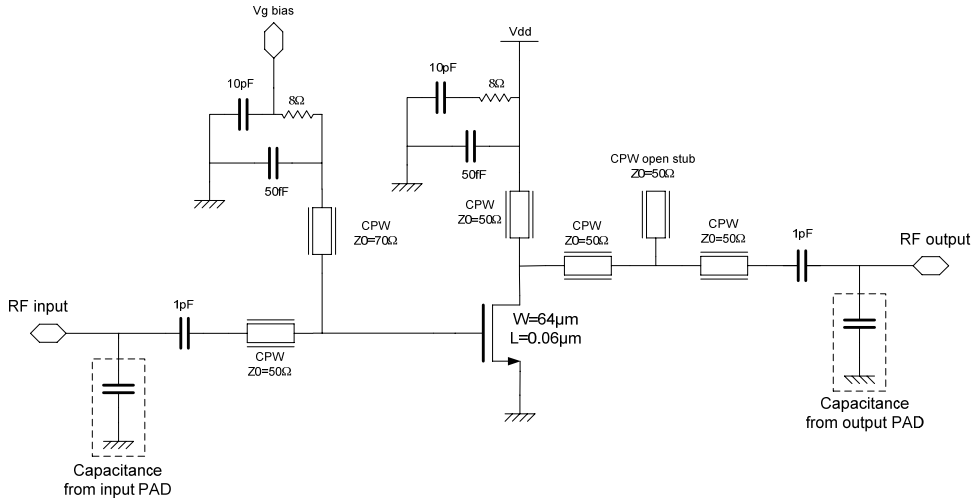


Figure IV.28. Single stage common source amplifier topology

The input matching consists of 50Ω series line and a 70Ω short circuited shunt stub. The matching network design follows the methodology described previously in *IV.3.2.d*. The transmission lines used are coplanar lines. Underpasses such as those described in *Chapter III* are used to insure a good coplanar mode for both ground plane sides. The centre conductor is made by using top level metallization (M6+Alucap). Alucap is a metal layer deposited on the top of the original top metal (*Figure III.2*). The two ground planes use all metals stacked. This structure described in *Figure IV.29* satisfies the industrial 65nm node density rules for manufacturing, while providing good ground references.

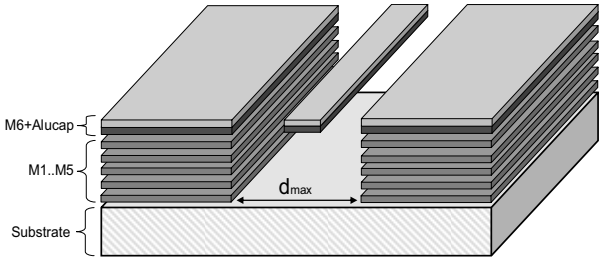


Figure IV.29. Coplanar Line realized by using top level metallization

The input parallel stub is also used for the input bias and is adjusted for optimum noise as explained in *IV.3.2.d.i*. The output matching is performed with open stub and 50Ω series lines. DC-blocking 1pF woven MOM capacitors (cf. *Chapter III- I.5.*) are used at input and output and are integrated in the coplanar lines as shown in *Figure IV.30*:

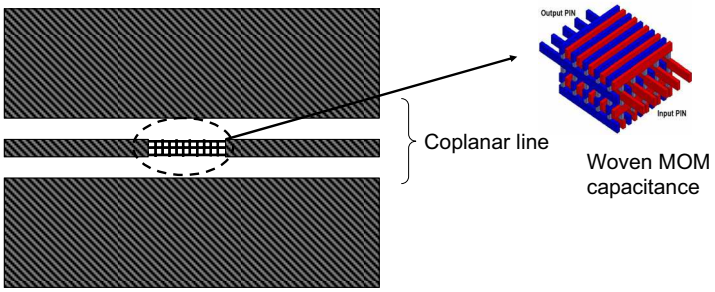


Figure IV.30. Woven MOM capacitance included in coplanar line

The out-of-band stability is controlled with resistive parallel network composed of short-circuiting capacitors (50fF) in the shunt stubs and two small value series resistors (8Ω). Additional large capacitors are also used for decoupling the bias lines (10pF). The NMOS transistor is composed of 2 unit transistors of 32µm width with double contacted gate and 1.33µm wide fingers (see *Figure IV.18* for the layout structure). A photograph of the circuit is presented in Figure IV.31. The occupied area is 0.64mm² including the pads.

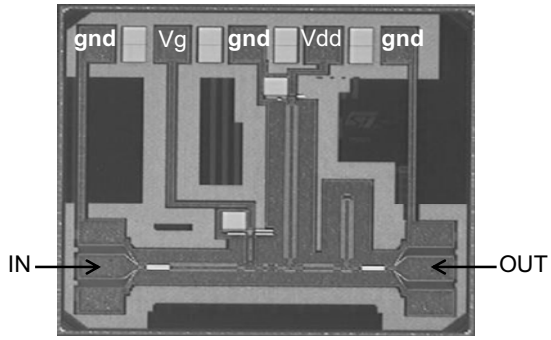


Figure IV.31. Die photograph of the single stage amplifier

Two versions of this circuit have been implemented. One with classical underpass such as those described in *Chapter III* and one with reduced underpass in order to decrease discontinuities [26]. The classical and reduced underpass layouts are described in *Figure IV.32*. The reduced underpass offers a quasi constant lineic capacitance because the conductor area over the underpass is reduced. Thus there is no impedance discontinuity on the transmission line.

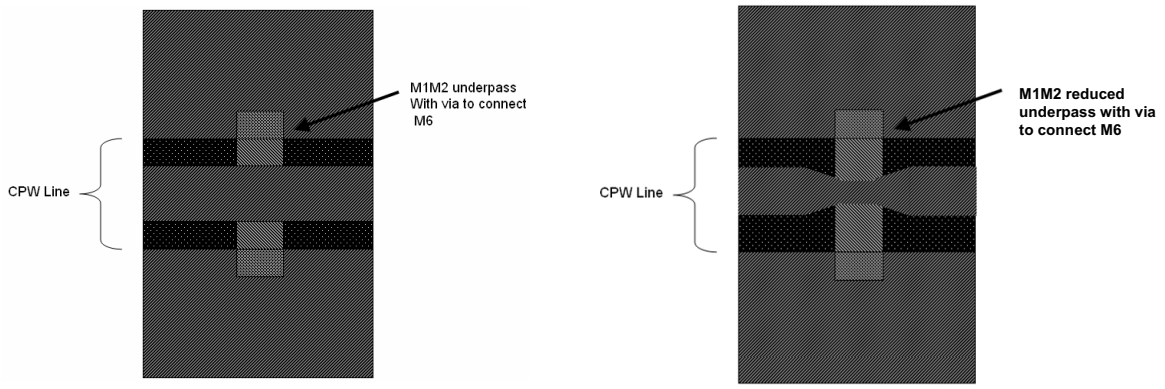


Figure IV.32. Classical underpass in CMOS technology (left) ; reduced underpass (right)

Since both designs use the same coplanar line length, the version with classical underpass presents higher capacitive transmission lines. It results that the effective epsilon of those T-lines is higher. As depicted in *Chapter III – I.6*, the wavelength is defined by $\lambda_d = \lambda_0 / \sqrt{\varepsilon_r}$. Because the effective epsilon increases, for a given T-line length, the electric length decreases. It outcomes that for two identical circuits (with the same area), one works at higher frequency (i.e. higher frequency matching).

IV.4.1.a. 80GHz CMOS SOI single stage amplifier simulations and measurements

The circuit using reduced underpass work at 80GHz. The simulated and measured S-parameters and Noise Figure are presented in *Figure IV.33* and *Figure IV.34*.

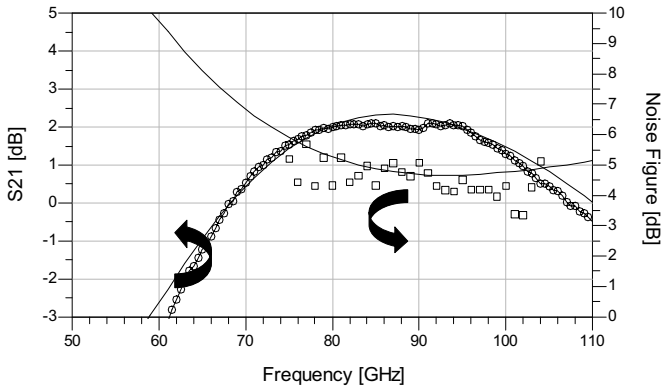


Figure IV.33. 80GHz single stage amplifier measured and simulated (dashed lines) Gain (S21) and Noise Figure

The circuit exhibits a flat gain of 2.1dB from 80GHz to 94Gz and an average noise figure of 4.5dB. The input and output return losses at 80GHz are -13dB and -6dB respectively (see *Figure IV.34*). This amplifier consumes 22mW from a supply voltage of 1.2V.A good fit between simulation and measurements is obtained for small signal parameters and also for noise figure over the whole frequency range. It can be noticed that this single stage amplifier still presents signal gain up to 106 GHz.

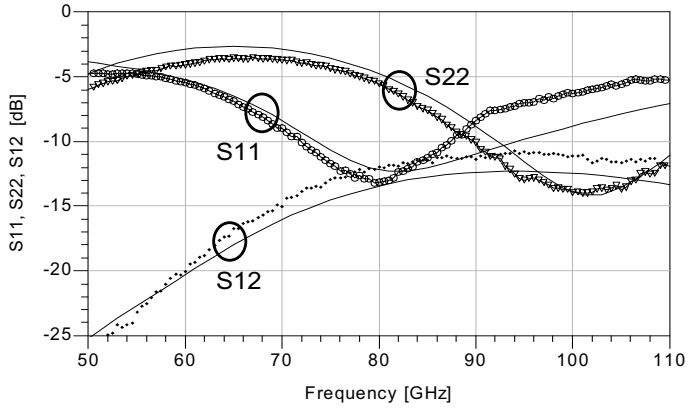


Figure IV.34. Measured input/output return losses and isolation. The dashed line represents the simulations

IV.4.1.b. 94GHz CMOS SOI single stage amplifier simulations and measurements

Contrary to the previous circuit, the circuit using classical underpass has a peak gain at 94GHz. The simulated and measured S-parameters and Noise Figure are presented in the following figure:

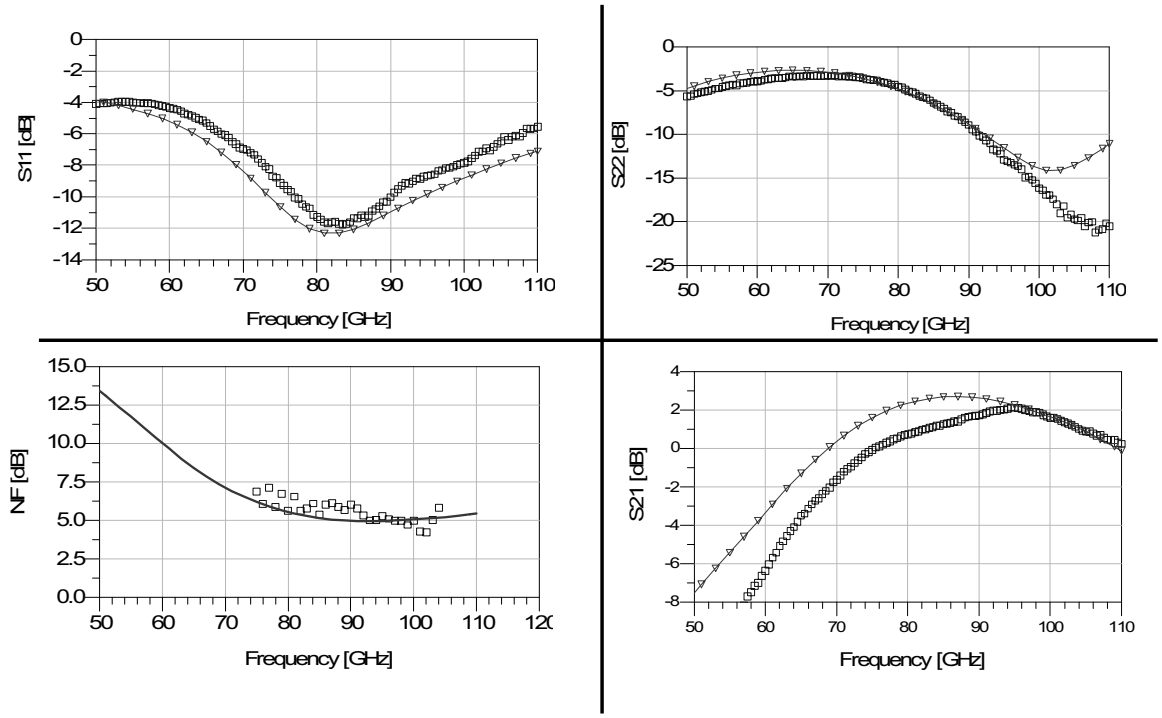


Figure IV.35. Measured and simulated S-parameters and Noise Figure. The squares represents the measurement

The noise figure is higher in comparison with the earlier circuit with an average noise figure of 5.5dB. The input and output return losses at 80GHz are -12dB and -5dB respectively (see *Figure IV.35*). This amplifier consumes 22mW from a supply voltage of 1.2V.

Those two circuits demonstrate the validity of the active and passive models and show the potentiality of the technology for mm-wave circuit. Moreover reduced underpass have been tested and compared with classical shape underpass. From those first measurement comparisons it turns out that there are no convincing results to justify the benefit of the optimized underpass except for noise figure. Nevertheless the noise figure benefit and the measurement accuracy are of the same order. The *Table IV.3* gives the performances summary of the two circuits:

Single stage common source CMOS SOI amplifier

Frequency	80GHz	94GHz
Maximum gain	2.1dB	2.3dB
Input/Output return losses	-13/-6dB	-9/-12dB
NF	4.5dB	5.5dB
ICP_1*	0dBm	0dBm
Power	22mW	22mW
Area	0.64mm²	0.64mm²

*Simulated

Table IV.3. Single stage CMOS SOI amplifier measured performances summary

IV.4.2. 80GHz CMOS SOI three stages LNA

A three stages LNA has been also implemented. This design follows the same methodology than the single stage amplifier (*Figure IV.37*). The input matching consists of 50Ω series line and a 70Ω short circuited shunt stub which is also used for the input bias and is adjusted for optimum noise. The output matching is performed with short circuit shunt stubs also used for biasing and 50Ω series lines. Inter-stage matching consists of 1pF DC-blocking capacitors and short circuit shunt stub from first output and second input bias lines. In addition to decoupling capacitors (10pF), short-circuit capacitors (50fF) in the shunt stubs and two small value series resistors (8Ω) are used to insure stability. NMOS transistors are identical and are composed of 2x24 fingers with double contacted gate and 1.33um-wide fingers. A die photograph of the complete circuit is presented in *Figure IV.36*; the occupied area is 0.98mm² including the pads.

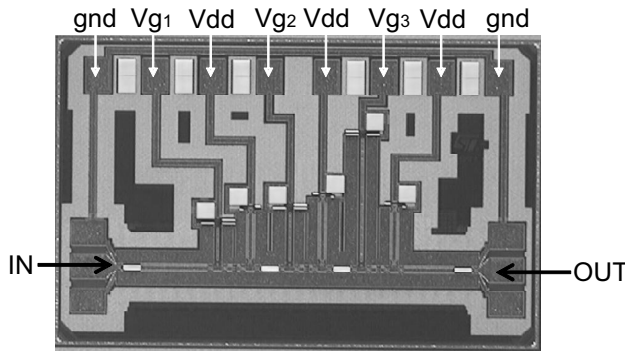


Figure IV.36. Die photograph of the three stages LNA

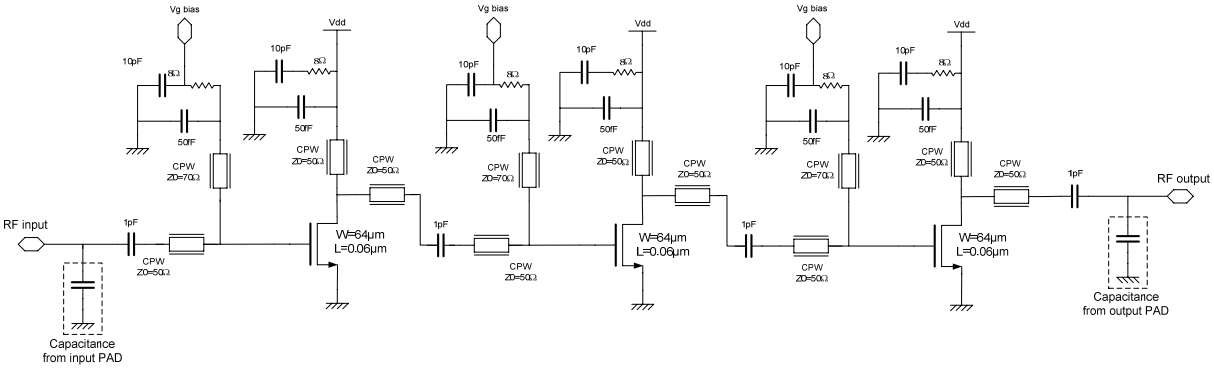


Figure IV.37. Three stages common source LNA

The circuit was designed for on wafer measurement by using RF probes in input/output and DC probes for biasing (*Figure IV.36*). However, some measurement issues demonstrated that DC probes present parasitic inductors which resonate with the bias network. By using this type of probes, the LNA suffers of instability. In order to overcome such a difficulty a specific board has been used. The circuit has been stuck on a metallic board and bonded to bypass capacitances as shown on *Figure IV.38*:

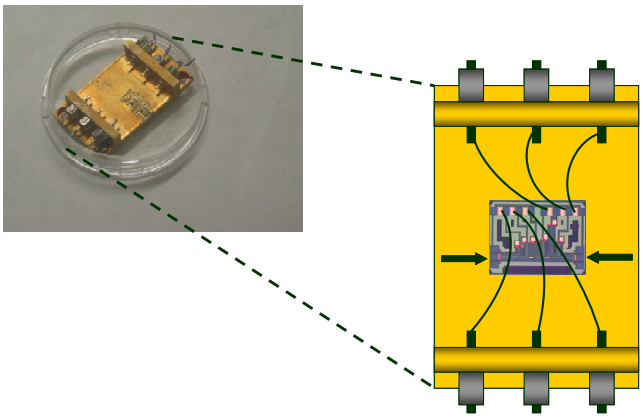


Figure IV.38. The three stages LNA on metallic board

Thanks to this assembling, the LNA became stable and thus measurements were enabled. Nevertheless, all gate biasing had been connected together as well as power supplies stages. The counterpart was less flexible in the biasing, thus non-optimal power consumption, gain and noise conditions.

IV.4.2.a. 80GHz CMOS SOI three stages LNA simulations and measurements

Measured S-parameters and Noise Figure of the three stages low noise amplifier are presented in *Figure IV.39*. Contrary to the single stage amplifier, the measurements and the simulations show a slight mismatch due to bonding coupling parasitic which are very hard to model and thus are not taken into account in simulation.

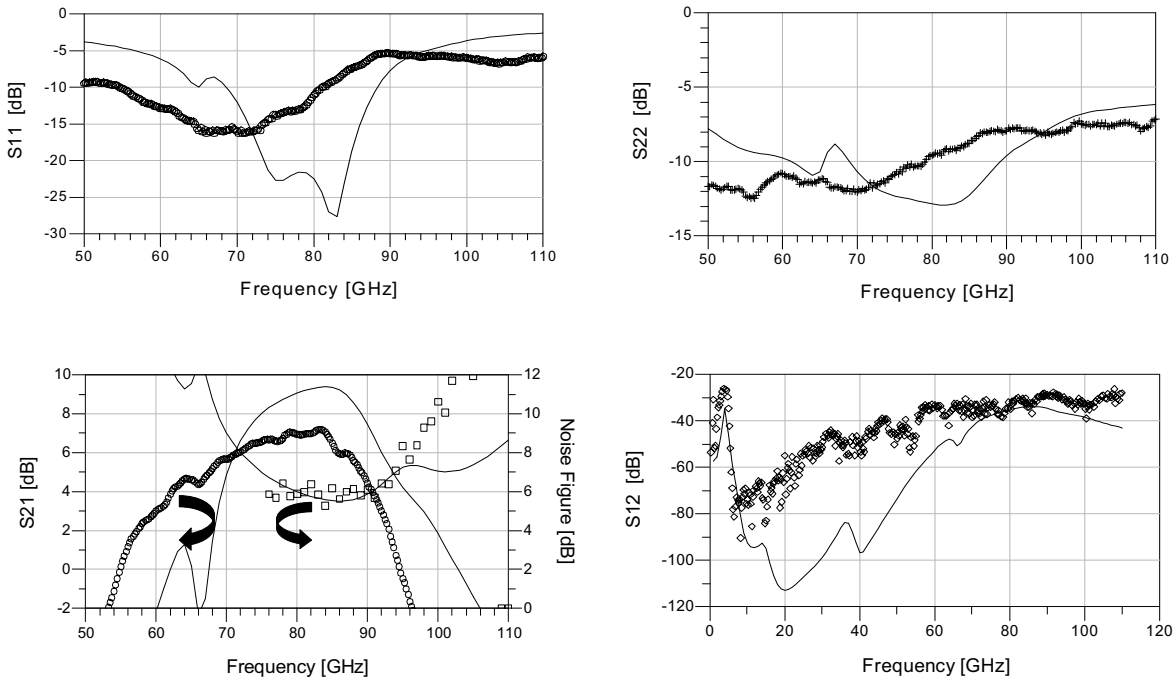


Figure IV.39. Measured and simulated (continuous lines) S-parameters and Noise Figure of the 3 stages LNA

The 3 stages LNA presents a gain of 7.2dB and a noise figure of 5.7dB at 80GHz with an input and output matching better than -14dB and -10dB respectively. Unfortunately the optimum bias was not applied for each stage decreasing performances and increasing the total power consumption. The 3 stages amplifier consumes 70mW from a supply voltage of 1V. Nevertheless, this LNA presents the best CMOS measured NF ever reported at 80GHz (cf.*Table IV.1*) with a good input and output matching. The *Table IV.4* gives the performances summary of the two circuits:

3 stages common source CMOS SOI LNA	
Frequency	80GHz
Maximum gain	7.2dB
Input/Output return losses	-11/-9dB
NF	5.7dB
ICP_1*	-3.75dBm
Power	70mW
Area	0.98mm²

Table IV.4. Three stages CMOS SOI LNA measured performances summary

IV.4.3. 60GHz CMOS SOI three stages LNA

As explained in *IV.3.2.c*, regarding the CMOS 65nm LP technology (bulk and SOI), for a frequency below 60GHz (i.e. the gain noise ration is high enough) multi-stages cascode architecture can be used in order to satisfy high gain and stability. Because fully integrated transceiver must be able to work from a distance of some centimeters to few meters, a variable gain LNA is required. At 60GHz the gain margin is high enough to achieve this type of LNA. The *Figure IV.42* shows three stages, variable gain LNA. Bias and gain are controlled by three current mirrors in order to adjust the current density as explained in *IV.3.2.b*.

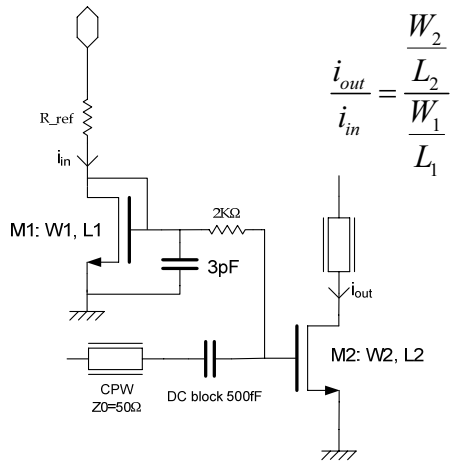


Figure IV.40. Current mirror biasing topology

The *Figure IV.40* gives the topology of the current mirrors used in each stage. R_ref is used as current reference driven by the "gain control" voltage. The current ratio between the output and the input is dictated by the width length ratio of each transistor. The 3pF capacitor and the 2KΩ resistor are used to insure DC to RF isolation. For a 700Ω R_ref resistor value and a 12x0.4µm² transistor (M_1) associated to a gain control variation of 0.6V to 1.2V the current density obtain for M_2 is from 75mA/mm to 280mA/mm as shown in :

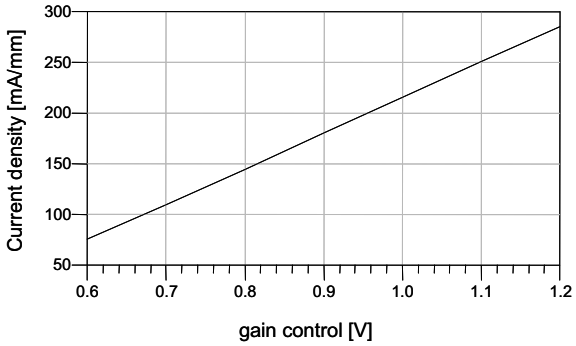


Figure IV.41. Current density in M2 transistor (Figure IV.40) versus gain control voltage

This current variation range has been chosen to impact noise as less as possible (cf. *Figure IV.13*). The input matching of the LNA (*Figure IV.42*) consists of 50Ω series line and also 50Ω parallel short circuited shunt stub. The stub is adjusted for optimum noise. The output matching is performed with a short stub and 50Ω series lines as well. The cascode structure of each stage adopts a serial 50Ω coplanar line (cf. *IV.3.2.d.ii*). DC-blocking 500fF MOM capacitors are used at input of each stage and at output of the circuit, integrated in the coplanar lines. The out-of-band stability is controlled with short-circuiting capacitors (500fF) and a small value resistor (8Ω) in the power supply rail of each stage. Transistors of each cascode stages are 64µm and 100µm width respectively. The layout of each transistor is optimized to reduced layout parasitic capacitances and resistances as explained in *IV.3.2.b.i.*

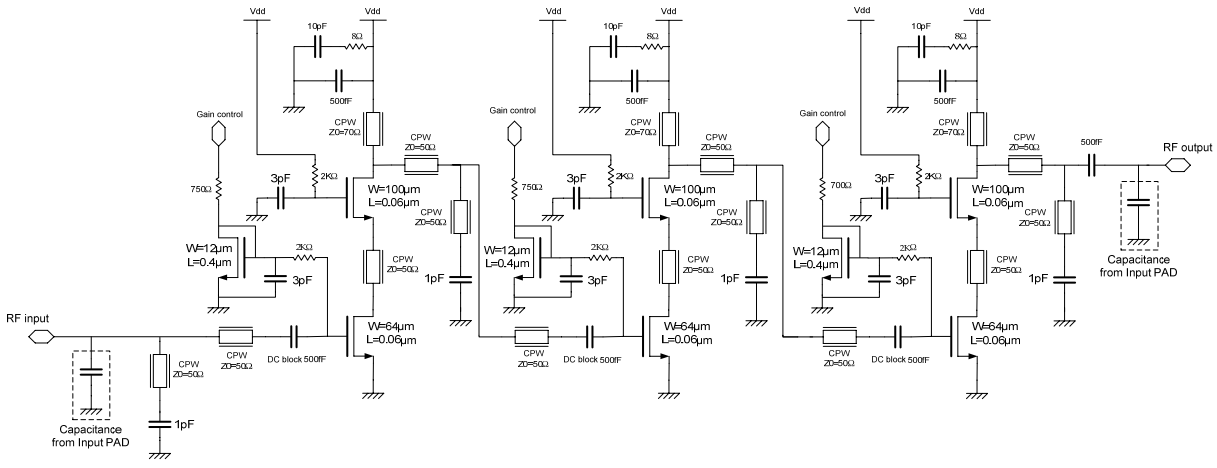


Figure IV.42. 60GHz three stages LNA schematic

The circuit was designed for on wafer measurements by using RF probes in input/output and DC probes for biasing *Figure IV.43*:

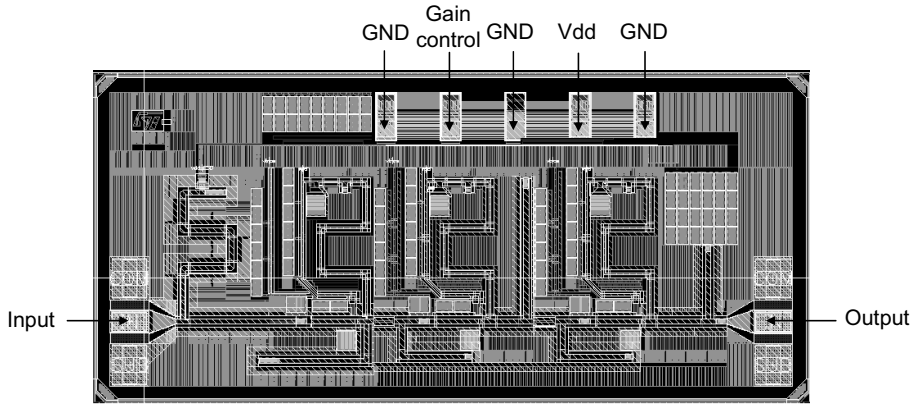


Figure IV.43. Screen shot of the 60GHz 3 stages variable gain LNA layout

A screen snapshot of the complete circuit is presented in *Figure IV.43*. The occupied area is 1.31mm² including the pads.

IV.4.3.a. 60GHz CMOS SOI three stages LNA simulations

The LNA is centered at 60GHz as shown in the *Figure IV.44*. For a voltage gain control set at 1.2V the LNA shows 20.5dB gain and 6.5dB noise with an associate power consumption of 20mW:

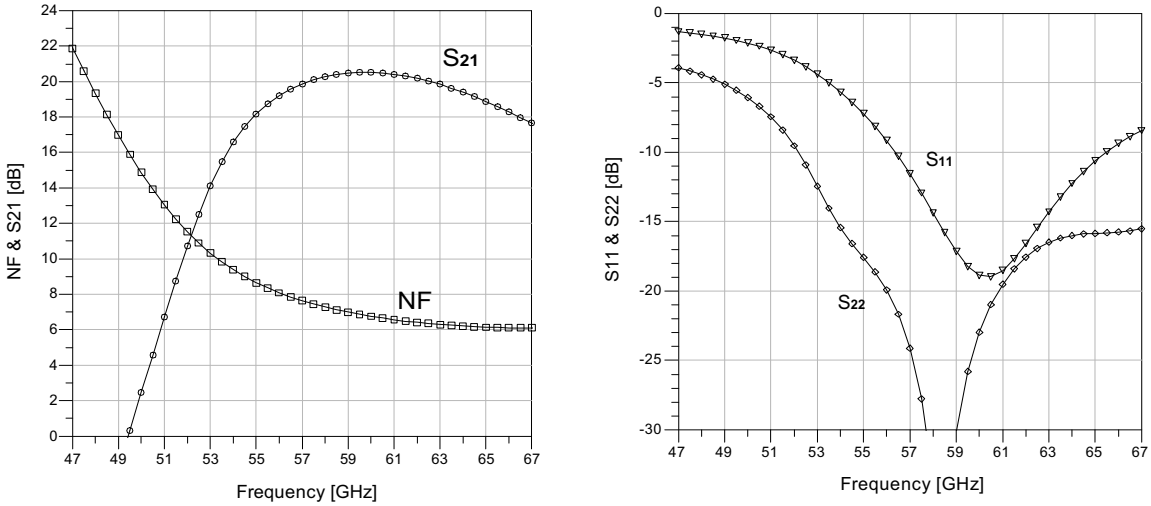


Figure IV.44. Simulated S-parameters and noise figure for a gain controlled voltage of 1.2V (i.e. P_{DC}=20mW)

The *Figure IV.45* summarizes the range of performances achievable for each gain step and the associate power consumption:

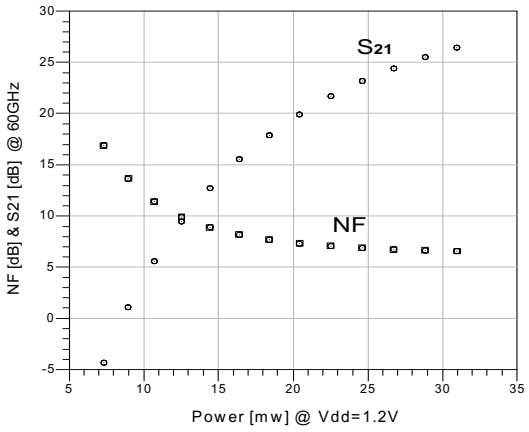


Figure IV.45. Simulated noise figure for each gain step and the associate power consumption for a frequency of 60GHz.

These results demonstrate the gain variation feasibility with a tuning range of 26dB and an associated noise figure from 12.5dB to 6dB. The linearity is estimated at -30dBm input compression point and -21dBm IIP_3 with 20dB associate gain. The *Table IV.5* gives the performances summary of the two circuits:

3 stages cascode 60GHz CMOS SOI LNA

Frequency	60GHz
Maximum gain	20.5dB
Input/Output return losses	-19/-21dBm
NF	6.5dB
IC_1*	-30dBm
IIP_3*	-21dBm
Power	20mW
Area	1.31mm²

*estimated

Table IV.5. 3 stages CMOS SOI LNA simulated performances summary

IV.4.4. 60GHz CMOS SOI drain pumped mixer

The resistive mixers present a very linear behavior and superior intermodulation properties. They have the advantage that they consume no DC power and guaranteed unconditional stability, making them very attractive for the integration in deep submicron CMOS low supply voltage technologies. The saved DC power allows to add a low-noise RF amplifier in front of the mixer or an IF amplifier behind the mixer. Their main drawbacks consist of conversion losses (instead of gain) and sometimes the need of a higher LO power with respect to the active mixers. In some implementations also the LO to RF isolation may also present reduced values. Nevertheless, thanks to the high resistivity substrate used in CMOS SOI, conversion losses can be decreased since passive components losses are reduced (cf. *Chapter III*). In order to evaluate the CMOS SOI advantage in this type of topology, a 60GHz resistive mixer has been designed. This work has been carried out in the context of

Sébastien Douyere[5] internship. The simplified schematic of the drain pumped mixer is shown in *Figure IV.46*. The FB NMOS transistor is biased in the linear area of DC drain current versus drain to source voltage characteristic. The LO signal is applied between drain and source while the RF is applied to the gate. Thus, the output conductance *gd* is a time variant function of LO and RF which will allow the signal translation from 60GHz (RF) to 5GHz (IF). The LO input matching is obtain with a 44fF capacitance and a series 50Ω coplanar line. The RF input is matched at 50Ω thanks to an 80fF capacitance, a series and parallel 50Ω coplanar lines. The 50Ω resistor and the 5pF capacitor are used to provide the DC biasing to the transistor gate.

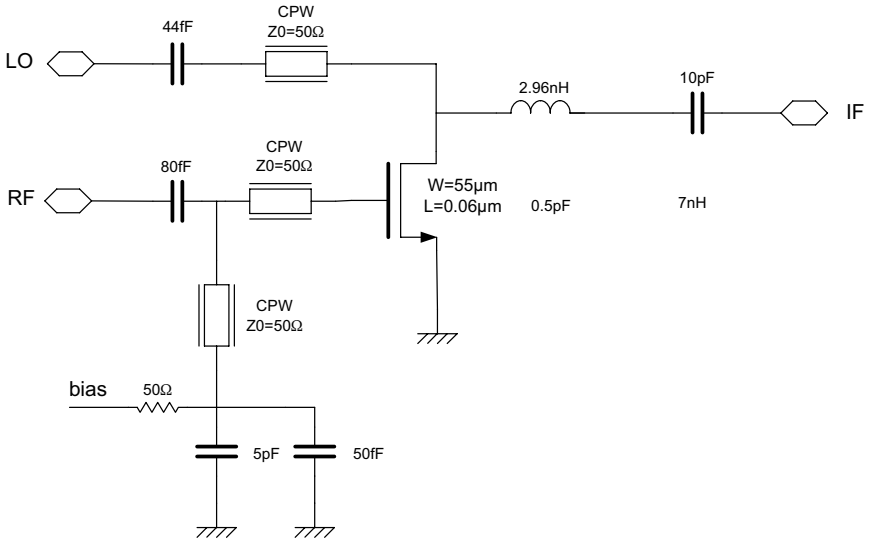


Figure IV.46. 60GHz drain pumped mixer schematic

The performances of the designed mixer are summarized in *Table IV.6*. As shown in *Figure IV.47*, for an LO power of -5dBm, the conversion losses are evaluated at -7.7dB. Moreover, the noise figure and the input compression point (*Figure IV.49*) are estimated respectively at 12.8 dB and -10 dBm (cf. *IV.1.1*).

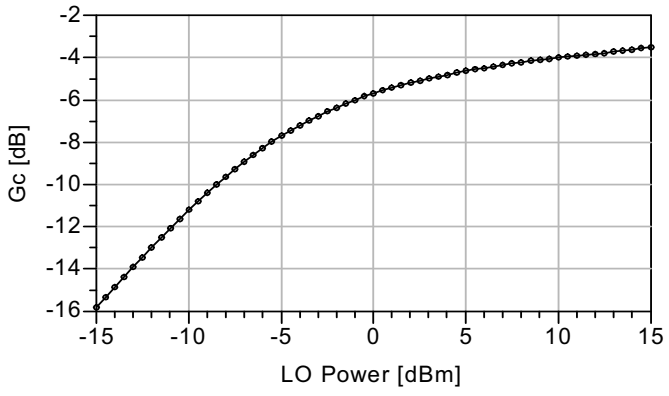


Figure IV.47. Simulated Gc vs. LO power

Mixer		
P_{OL}	-5dBm	0dBm
Gc	-7.7dB	-5.8dB
ICP1	-10dBm	-5dBm
IIP3	0dBm	4dBm
NF	9dB	7dB
LO-IF iso.	37dB	37dB
Power	10µW	10µW
LO/RF Return Loss	< -20dB	< -20dB

Table IV.6. Simulated CMOS SOI mixer performances

[5] Sébastien Douyere was a trainee (March –August 2007) in our team under my technical supervision

The *Figure IV.48* is a screen snapshot of the complete circuit *Figure*. The occupied area is 0.63mm² including the pads.

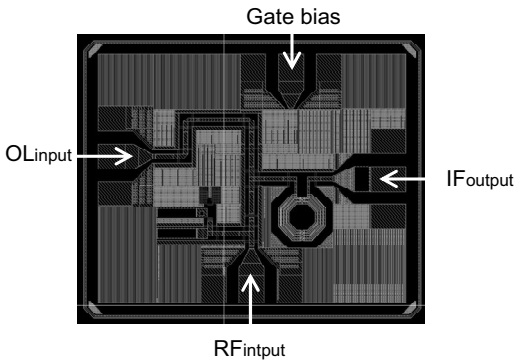


Figure IV.48. Screen snapshot of the 60GHz drain pumped mixer layout

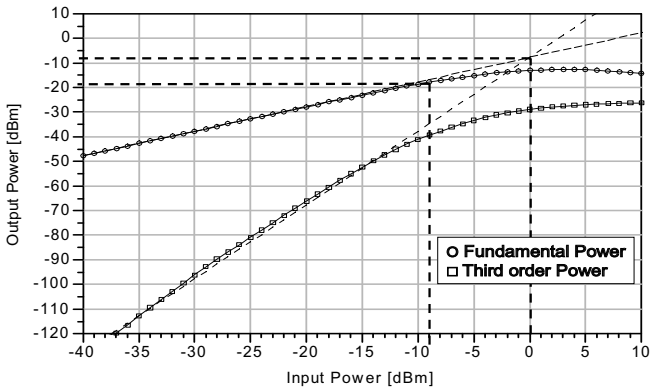


Figure IV.49. Simulated Mixer linearity (P_{OL}=-5dBm)

Those results are very promising for 60GHz applications. They highlight the SOI advantages in comparison with bulk for this type of topology [17], [18] and [20]. The conversion losses are close to performance achieve with active single ended mixer presented in [16] unlike the power consumption which is nil in this work.

IV.5. Millimeter wave bulk CMOS 65nm building blocks

In order to compare the SOI and bulk 65nm CMOS technology, some building blocks have been made in both substrates. As for SOI, CMOS bulk circuits were simulated with *Agilent* ADS simulator and the BSIM4 transistor model. Transmissions lines were modeled using TLINP model from ADS library and an adapted RLCG model for multilayered silicon (*cf. Chapter III*). Input and output pads have been taken into account in all designs. The circuits were fabricated using the STMicroelectronics's manufacturing process CMOS065 LP with a MOSFET physical gate length of 60nm and a 6 metal layers BEOL (5 thins, 1 thick). They were measured on wafer. All measurements were performed at a source and load impedance of 50Ω. Linearity was measured using two 60GHz synthesizers, a variable attenuator and a spectrum analyzer calibrated with a power meter. The test set-up connectivity was realized with V-band wave guides. The S-parameters were measured using 0-67GHz network analyzer. The noise figure was measured at 60GHz.

IV.5.1. 60GHz 4 stages bulk CMOS LNA with ESD protections

To bench mark the 60GHz LNA presented in *Table IV.4*, a 60GHz CMOS bulk LNA has been also designed. The *Figure IV.51* shows the schematic of the four stages LNA. As for the SOI 60GHz 3 stages LNA, this circuit uses coplanar lines. Performances of such lines are shown on *Figure IV.50*:

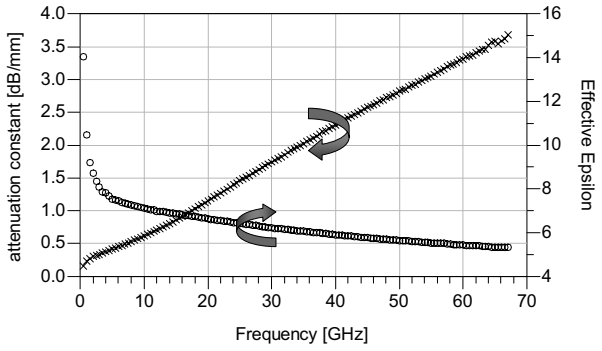


Figure IV.50. Attenuation constant and Effective Epsilon versus frequency for a coplanar wave guide made in CMOS 65nm technology

These performances are to be compared with the same T-lines in SOI (cf. *Chapter III*). The coplanar lines in bulk have 2.7dB/mm more losses (α) at 60GHz in comparison with SOI.

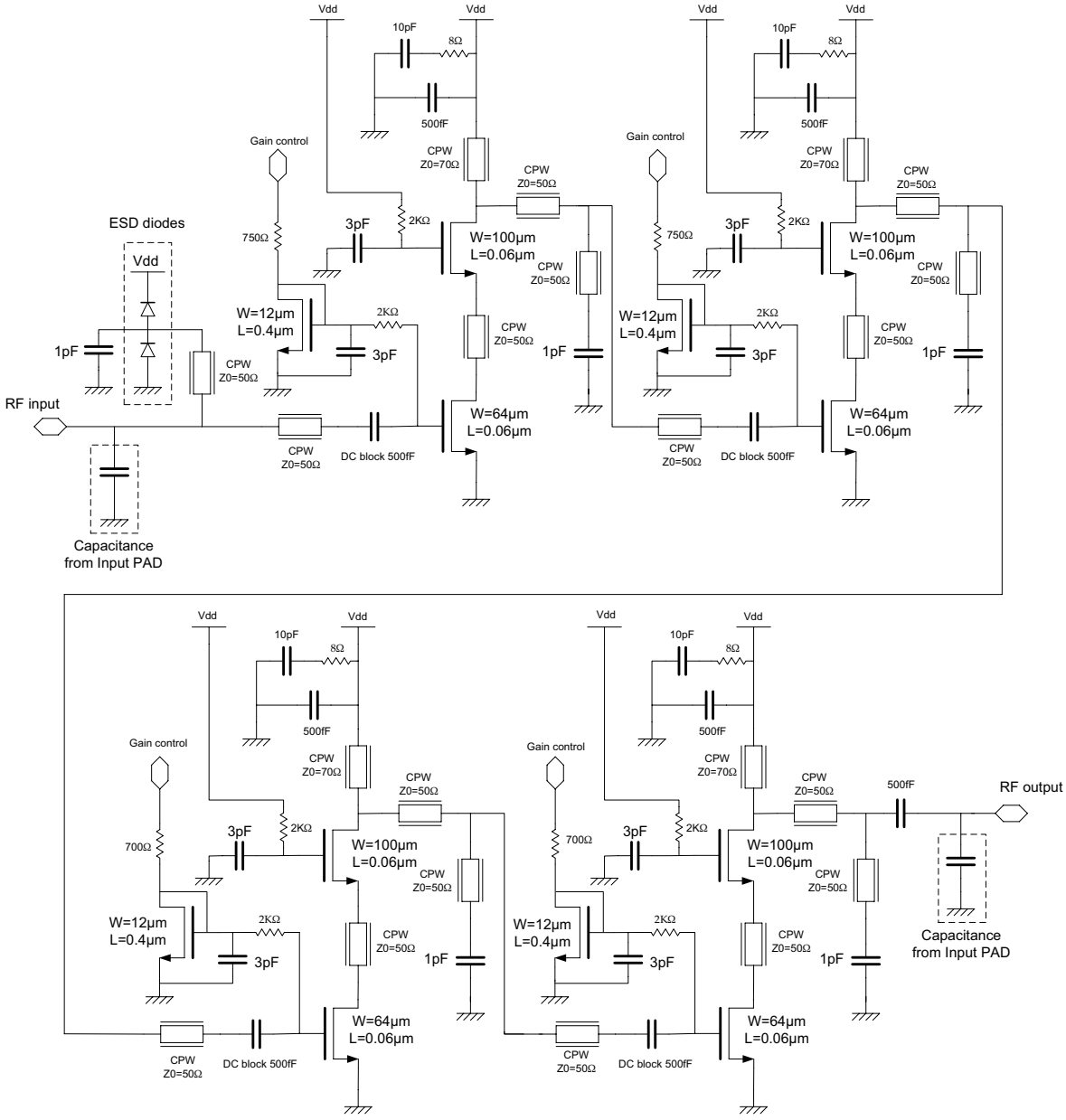


Figure IV.51. Four stages bulk CMOS LNA schematic (power supply ESD protections not shown)

In order to achieve quite the same gain this circuit uses 4 stages instead of the 3 uses in the SOI version. The input matching consists of 50Ω series lines and also 50Ω parallel short circuited shunt stub. The stub is adjusted for optimum noise and is used with diodes for RF ESD[6] protection. The output matching is performed with short stubs and 50Ω series lines as well. DC-blocking 0.5pF MOM capacitors are used at input and output and are integrated in the coplanar lines (*Figure IV.30*). The out-of-band stability is controlled with the short-circuiting capacitors (500fF) and a small value series resistor (8Ω) in the drain power supply of each stage. Bias and gain are controlled by four current mirrors in order to adjust the

[6] Electrostatic Discharge in the literature

current density (cf. *IV.4.3*). The current variation range is chosen to impact noise as less as possible (60 to 300 mA/mm). The gain control is obtained by voltage variation from 0.6 to 1.2V. Transistors of each cascode stages are 64µm and 100µm width respectively. The layout of each transistor is optimized to reduced layout parasitic capacitances and resistances as explain in the first part. The circuit uses ESD protection diodes in RF input, gain control and V_{dd} pads. A photograph of the circuit is presented in *Figure IV.52* ; the occupied area is 1.55mm² including pads.

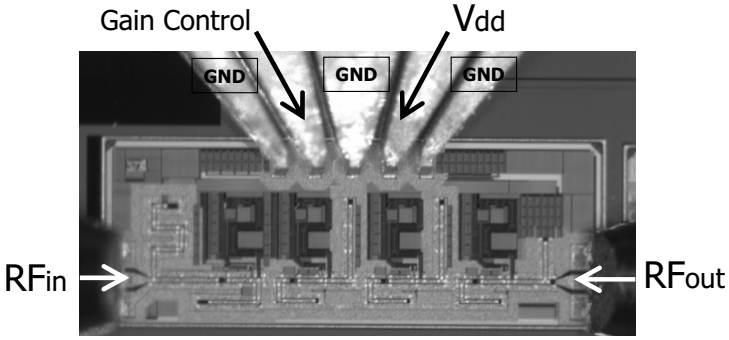


Figure IV.52. Photograph of the 4 stages bulk CMOS LNA including PADs

IV.5.1.a. Comparison between measurements and simulations

The following results show comparison between measurements and simulations after model corrections. Since only 60GHz frequency noise measurement was possible, simulation and measurement were compared for all biasing possibilities at this frequency as shown in *Figure IV.53*. Thus the noise model accuracy was demonstrated in order to evaluate the noise performance over all frequencies.

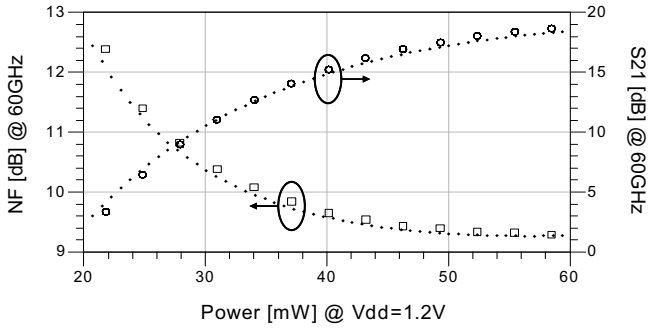


Figure IV.53. Measured and simulated (dot line) Noise Figure and S21 at 60GHz for all biasing possibility

This result demonstrates the validity of your models. The LNA is centered at 55GHz as shown in the *Figure IV.54*. For a voltage gain control set at 1.2V the LNA shows 22dB gain and 8dB noise with an associate power consumption of 50mW.

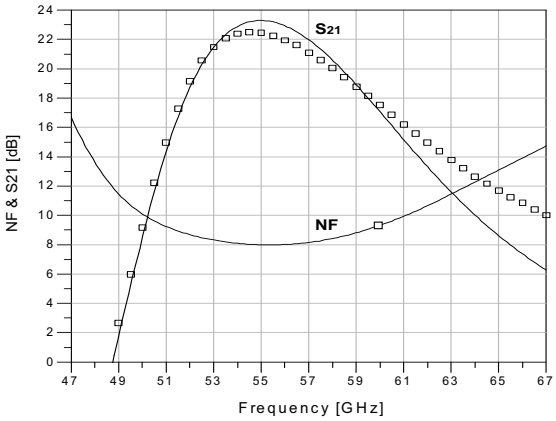


Figure IV.54. Measured and simulated (continuous line) noise figure and gain for a gain controlled voltage of 1.2V (i.e. P_{DC}=50mW)

At the same voltage gain setup, the *Figure IV.55* shows input and output insertion losses which are less than 10dB at 55GHz. *Figure IV.54* and *Figure IV.55* demonstrate also the model accuracy over a large frequency range.

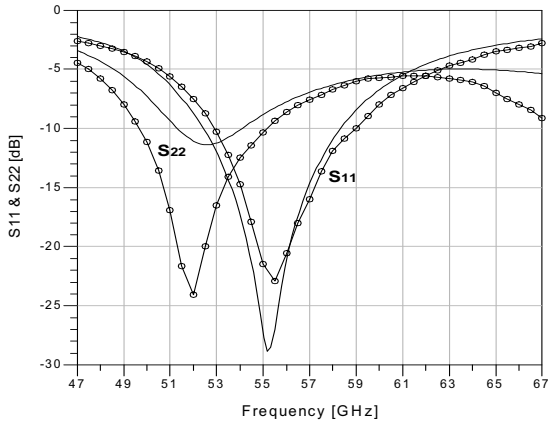


Figure IV.55. Measured and simulated (continuous line) input and output insertion losses for a gain controlled voltage of 1.2V (i.e. P_{DC}=50mW)

For a voltage gain control set at 1.2V the LNA shows -30dBm ICP_1 and -20dBm IIP_3 as shown in *Figure IV.56*:

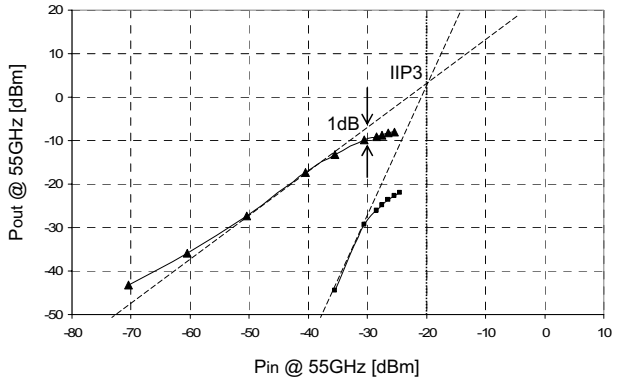


Figure IV.56. Measured input compression point and input third order interception point at 55GHz for a gain controlled voltage of 1.2V (i.e. P_{DC}=50mW)

The *Figure IV.57* summarizes the range of performances according to the voltage gain control variation and the associate power consumption:

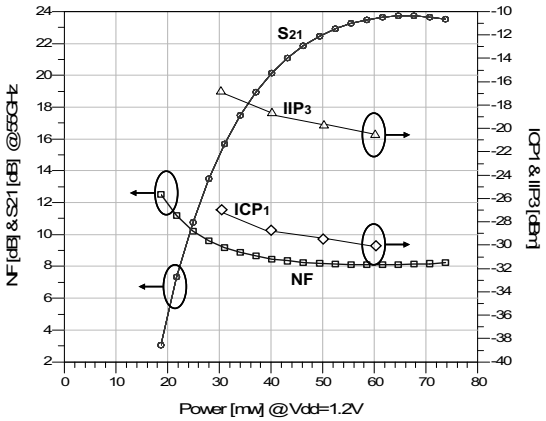


Figure IV.57. Measured noise figure and linearity according to the voltage gain control variation and the associate power consumption for a frequency of 55GHz.

These results demonstrate the gain variation feasibility with a tuning range of 21dB and an associate noise figure from 12.5dB to 8dB. The measured linearity shows an input compression point and an IIP_3 better than -30dBm and -21dBm respectively.

Measurements showed a discrepancy with a first set of simulations. The differences observed are in matching frequencies and noise figure. The *Figure IV.58* shows simulations with first models and corrected models after measurements:

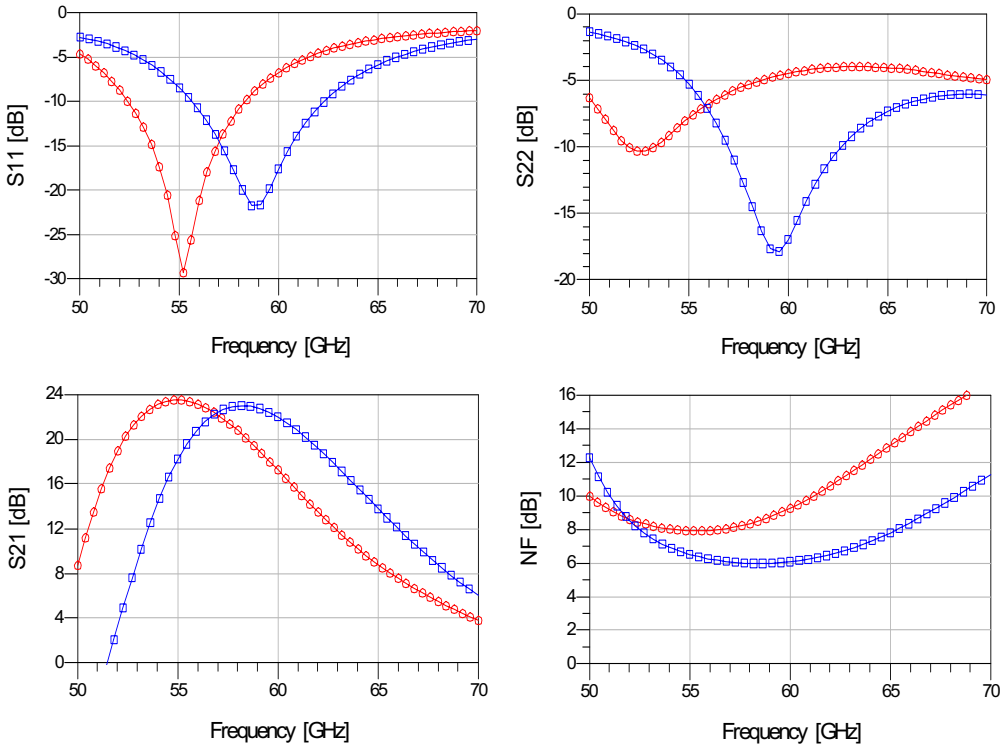
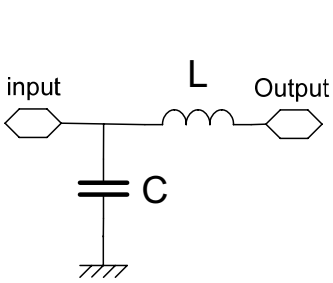


Figure IV.58. Simulated LNA results with original models (square) and modified models(circle)

As shown in *Figure IV.58*, first design was centered at 60GHz but after model correction the center frequency is 55GHz. These differences analysis shows two errors in the models used in the first simulations:

- Under-estimation of the pad+taper capacitance
- Not taking into account of the electrical wave propagation in the woven MOM capacitances

The *Table IV.7* show the model used for the pad+taper with the estimated and measured value of the model elements:

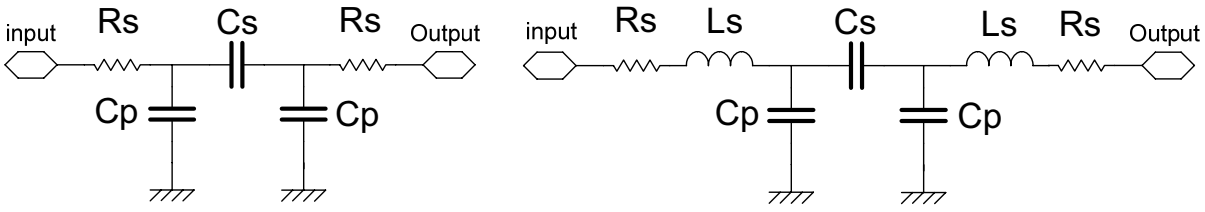


Estimated Values		Measured Values	
L	22 pH	L′	33 pH
C	136 fF	C′	160 fF

Table IV.7. Estimated and measured value of the series inductance and parallel capacitance of the PAD + taper

It appears that the capacitances were under-estimated by 17%. This can be explained because of the metallic plane used. As discussed in *Chapter III*, in order to respect the metal density rules, the levels of metallization must be perforated. Thus the capacitance estimation becomes difficult.

The second error is attributed to the first RF MOM capacitor model used. The RF design kit model of this capacitor is showed in *Figure IV.59 a).* Measurements of those capacitances demonstrated that propagation must be taken into account in order to model millimeter wave frequencies behavior. Thus a new lumped model has been developed *Figure IV.59 b)* by adding an inductance at input and output in order to improve the accuracy at millimeter wave frequency.



a) *b)*

Figure IV.59. Original RF model of the MOM capacitor (a) ; mm-wave model(b)

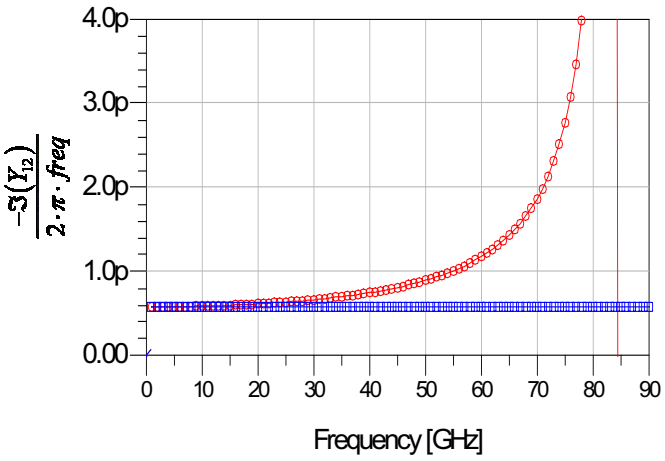


Figure IV.60. Simulated original RF model of the MOM capacitor (square) and the developed mm-wave model(circle)

The *Figure IV.60* shows a comparison between the extracted value of the serial capacitance using model *a)* and *b)*. As shown in this figure, thanks to the model developed the capacitance resonance can be evaluated.

IV.5.1.b. Performance summary of the 60GHz CMOS LNA for different power consumptions

The *Table IV.8* gives the performances summary of the circuit:

4 stages cascode bulk CMOS 60GHz LNA with ESD protections

Frequency	55GHz	55GHz	55GHz
Maximum gain	15dB	22.5dB	24dB
BW (-3dB)	6GHz	6GHz	6GHz
Input/Output return losses	-18/-11dB	-22/-11dB	-22/-11dB
NF*	9dB	8dB	8dB
ICP_1	-27dBm	-29dBm	-30dBm
IIP_3	-17dBm	-20dBm	-21dBm
Power	30mW	50mW	65mW
Area	1.55mm²	1.55mm²	1.55mm²

Table IV.8. 4 stages CMOS LNA measured performances summary

* Simulated based on one frequency point measurement (cf. *Figure IV.53*)

This circuit presents one of the best gains ever reported in CMOS technology at millimeter wave frequencies (*Table IV.1*). This performance has been achieved with a very good input and output insertion losses in comparison with [5], [9], [10] and [13].Nevertheless the noise figure performance is penalized by the coplanar line constant attenuation in CMOS bulk (cf. *Figure IV.50*). The use of microstrip lines may improves the noise figure, but special care must be taken in order to be compliant with current density rules, as these lines might be narrow. The noise figure and the linearity also suffer from the combination of cascode architecture and low supply voltage. These two points may be improved by using simple common source architecture for the first stage and the last stage.

IV.5.2. 60GHz bulk CMOS resistive mixer

As well as the 60GHz LNA, this circuit was designed in order to compare bulk and SOI performances. This work has been done within the context of *Sébastien Douyere* internship. The simplified schematic of the gate pumped mixer is shown in *Figure IV.61*. The FB NMOS transistor is biased in the linear area of DC drain current versus drain to source voltage characteristic. The LO signal is applied on the gate while the RF is applied to the drain. Thus, the transconductance *gm* is a time variant function of LO and RF which will allow the signal translation from 60GHz (RF) to 5GHz (IF). The RF input is matched at 50Ω with a 431fF capacitance and a series 50Ω coplanar line. The LO input matching is achieved with an 80fF capacitance, a series and a parallel 50Ω coplanar lines. The 50Ω resistor and the 4pF capacitor are used to provide the DC biasing to the transistor gate.

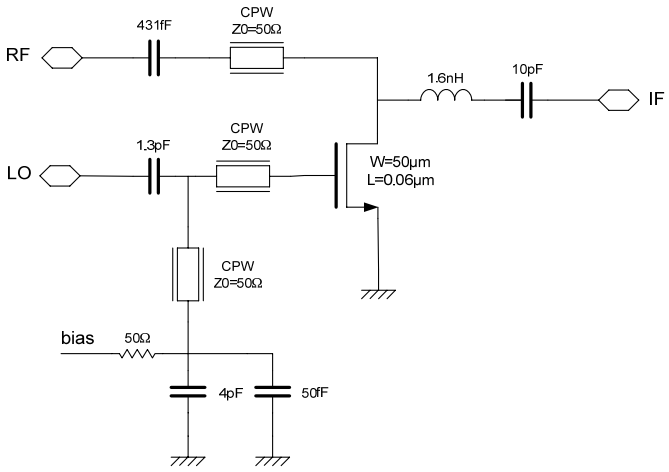


Figure IV.61. Gate pumped mixer

The Figure IV.62 is a die photograph of gate pumped mixer. The occupied area is 0.59mm² including the pads.

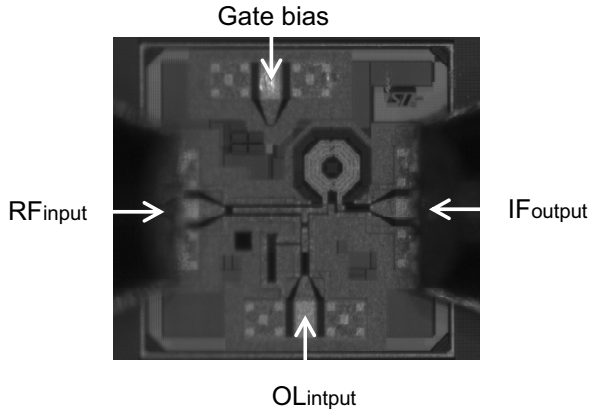


Figure IV.62. Photograph of the gate pumped 60GHz mixer

Measurements showed some discrepancies with respect to simulations (not shown). As for the previously presented LNA, the main discrepancy comes from the pad capacitances

and the MOM capacitor models. Because the circuit is not matched to 50Ω anymore, RF and LO ports have been de-embedded in order to evaluate the mixer performances. These results are summarized in *Table IV.9.* As shown in *Figure IV.63*, for an LO power of -5dBm, the conversion losses are evaluated at -18.8dB. In addition, the noise figure and the input compression point are estimated respectively at 20 dB and -2 dBm (cf. *IV.1.1*).

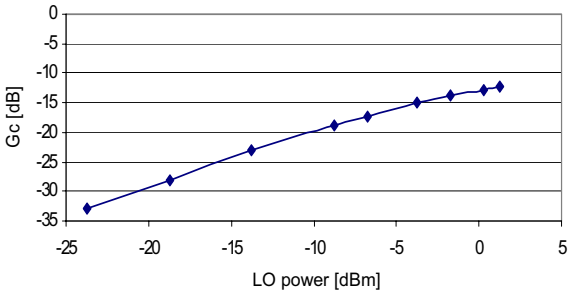


Figure IV.63. Measured Gc vs. LO power

Bulk CMOS mixer

P_{OL}	-5dBm	0dBm
Gc	-18.8dB	-14.85dB
ICP1	-2dBm	-4dBm
IIP3	8dBm	6dBm
NF*	19.8dB	16dB
LO-IF iso.	25dB	25dB
Power	-	-
LO/RF Return Loss	-	-

Table IV.9. De-embedded measured mixer performances

*Estimated from conversion losses cf. IV.1.1

These results demonstrate that this type of mixer is sensitive to passive performances. Thus this architecture is not the best for CMOS bulk integration. As for the noise performance in LNA, these results may be improved with microstrip lines. Moreover the model errors impact the design and not allow a detailed characterization. Nevertheless this topology shows a very good linearity not reachable with active mixer architecture.

IV.5.3. 60GHz bulk CMOS front-end co-integration

To evaluate the potentiality of the developed blocks in a reception chain, a co-integration between the previous LNA (*IV.5.1*) and the mixer has been achieved. The following die photograph shows the LNA and mixer with the bias pads and the LO input.

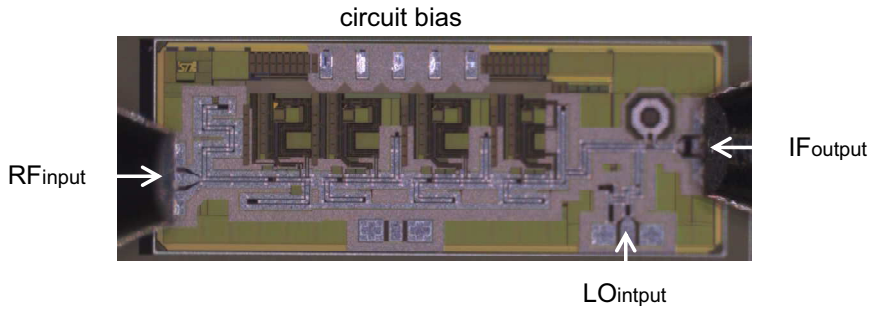


Figure IV.64. Photograph of the 60GHz integrated LNA+mixer

Performances are summarized in *Table IV.10.* As shown in *Figure IV.63*, for an LO power of -5dBm, the gain is 13.25dB. In addition, the noise figure and the input compression point are estimated respectively at 8 dB and -31 dBm (cf. *IV.1.1*).

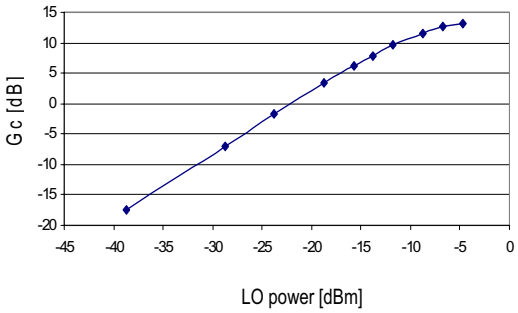


Figure IV.65. Measured LNA+Mixer gain vs. LO power

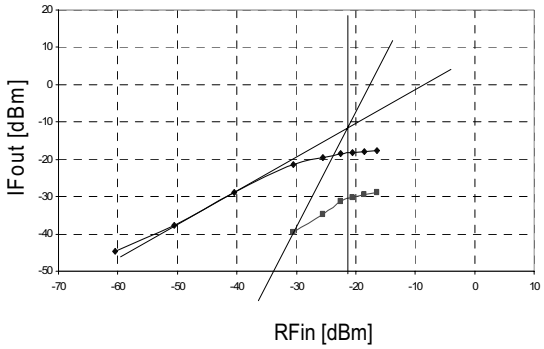


Figure IV.66. Measured input compression point and input third order interception point at 55GHz

The *Figure IV.66* shows the measured input compression point and the third order interception point at 55GHz. The sensitivity of the power measurement does not exceed -50dBm. At this power, measurements have showed that the third order non linearity starts to compress (the slope is less than 3:1 for the IM_3 products). In order to estimate the IIP_3 the relation given in *(4. 5)* has been used. The *Table IV.10* gives the measured performances summary of the integrated Rx front end:

LNA+Mixer	
P_{OL}	-5dBm
Gain	13.25dB
ICP1	-31.2dBm
IIP3**	-21.4dBm
NF*	8dB
LO-IF iso.	25dB
Power	60mW
LO/RF Return Loss	-

Table IV.10. Measured LNA+ mixer performances summary

**estimated noise from Friis expression*

***From (4. 5)*

These results are in line with the two previous circuit measurements. Unfortunately, the model errors impact the design and do not allow a detailed characterization. Nevertheless, from these first measurements it can be concluded that performances are very sensitive to passive performances. Thus for a given architecture the low resistivity substrate used in CMOS bulk technology decreased the overall performance in comparison with CMOS SOI. Therefore this architecture is not the best for CMOS bulk integration. In order to achieve good performances with CMOS bulk, the technology should show a reduced dependence on passive elements losses. Nevertheless this topology shows a very good linearity not reachable with an active mixer architecture.

IV.5.4. Comparison between CMOS bulk and SOI for mm-wave applications

The comparison of active and passive devices has been detailed in Chapters II and III. For low noise amplifiers and mixers, active device performances can be considered quite similar. Nevertheless, passives devices are very sensitive to substrate losses and thus have not the same performances in bulk and SOI. In LNA design, passive devices directly impact the noise figure and the gain performances. In a resistive mixer, the conversion losses are dictated by the matching passive devices used.

IV.5.4.a. Circuits comparison

Two circuits have been designed in order to benchmark the CMOS bulk and SOI at 60GHz. The following table illustrates the performances achievable with each technology:

CMOS SOI and bulk ~60GHz LNA

topology	CMOS SOI 3 stages cascode		CMOS bulk 4 stages cascode		
Frequency	60GHz*	60GHz	55GHz	55GHz	55GHz
Maximum gain	22.5dB*	26dB*	15dB	22.5dB	24dB
BW (-3dB)	14GHz*	14GHz*	6GHz	6GHz	6GHz
Input/Output return losses	-19/-21dBm*	-20/-21dBm*	-18/-11dB	-22/-11dB	-22/-11dB
NF	6.5dB*	6dB*	9dB	8dB	8dB
ICP_1	-30dBm**	-32dBm**	-27dBm	-29dBm	-30dBm
IIP_3	-21dBm**	-19dBm**	-17dBm	-20dBm	-21dBm
Power	22mW*	30mW*	30mW	50mW	65mW
Area	1.31mm²	1.31mm²	1.55mm²	1.55mm²	1.55mm²

*Simulated
**Estimated

Table IV.11. CMOS SOI and bulk LNA performances summary

In this first comparison the CMOS SOI offers clearly the best performances. For a given power consumption the CMOS SOI offers a gain increased of 46%, a doubled bandwidth, 48% less noise figure and 18% area saved. Moreover for a given gain the power consumption is 50% less. This comparison has been made with two circuits using the same topology (cascode) and the same type of transmission lines (coplanar wave guide). Simulations show that with microstrip lines instead of CPW for the CMOS bulk, the LNA benefits still are in favor of SOI with similar overall performances but only 3 stages in case of SOI.

The *Table IV.12* shows the CMOS SOI and bulk resistive mixer performances summary:

CMOS SOI and bulk ~60GHz resistive Mixers

Topology	CMOS SOI Resistive gate pumped*		CMOS bulk Resistive drain pumped	
P_{OL}	-5dBm	0dBm	-5dBm	0dBm
Gc	-7.7dB	-5.8dB	-18.8dB	-14.85dB
ICP1	-10dBm	-5dBm	-2dBm	-4dBm
IIP3	0dBm	4dBm	8dBm	6dBm
NF	9dB	7dB	20dB	16dB
LO-IF iso.	37dB	37dB	25dB	25dB
Power	10μW	10μW	-	-
LO/RF Return Loss	< -20dB	< -20dB	-	-

*Simulated (measurement pending)

Table IV.12. Simulated and measured mixer performances

For resistive mixer the CMOS SOI shows a great benefit. These results demonstrate also that this type of mixer is sensitive to passive performances. The conversion losses and the noise performance are twice better in CMOS SOI. Both technologies show very good performances in linearity. As for the LNA, CMOS bulk results may be improved with microstrip lines but the resistive architecture is probably not the best for CMOS bulk integration. CMOS SOI demonstrates here that performances achievable are comparable to III-V technology for this type of topology.

However, to fully demonstrate the benefit of the CMOS SOI, the comparison has to be performed with measured circuits in both technologies. Nevertheless, SOI active and passive models have shown a good enough accuracy (*IV.4.1*) to be confident with these results.

IV.6. Summary

We have shown in the *Introduction* that there are several potential applications in the frequency bands above and beyond 60GHz, such as 802.15.3 WLAN, WPAN (wireless HDMI/USB), automotive radar and imaging systems.

Several processes are candidates to address such applications. Since few years, the feasibility of (Bi)CMOS mm-wave low noise amplifiers has been demonstrated in the scientific literature [1]. Nevertheless, the millimeter-waves market segment has been historically held since decades by the III-V semiconductors. Two phenomena drive full silicon technologies as the technology integration platform for millimeter-waves designs. First of all, the performances of the active devices: f_T and f_{max} are close or even higher than 200GHz. And secondly, the market has expressed its need for low-cost consumer products in the millimeter-waves range.

We have seen millimeter wave building blocks considerations and especially low noise amplifiers and mixers. Stability issues, transistor matching and overall methodology to design multi-stages amplifier have been discussed.

We have exposed different blocks achieved in both CMOS SOI and bulk in order to benchmark the two technologies. The CMOS SOI has demonstrated that is a very promising technology for millimetre wave applications with state of the art CMOS noise performance at 80GHz. We have also illustrated the benefit of the CMOS SOI technology over bulk ones with a comparison of two blocks designed at the same frequency in both technologies. The CMOS SOI has demonstrated a very good improvement in term of power consumption and area saving.

In the near future, SOI is clearly one of the most promising solutions for applications at millimeter wave frequencies. As we have seen, wireless technologies require high-performance transistors and low-loss passive devices. Nevertheless a choice between benefits associated to SOI and additional cost of this technology has to be made.

IV.7. Bibliography

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IV.8. Appendix:

Example of MDS calculation:

The system diagrammed *Figure IV.67* resides at room temperature. The measurement bandwidth is 100 kHz:

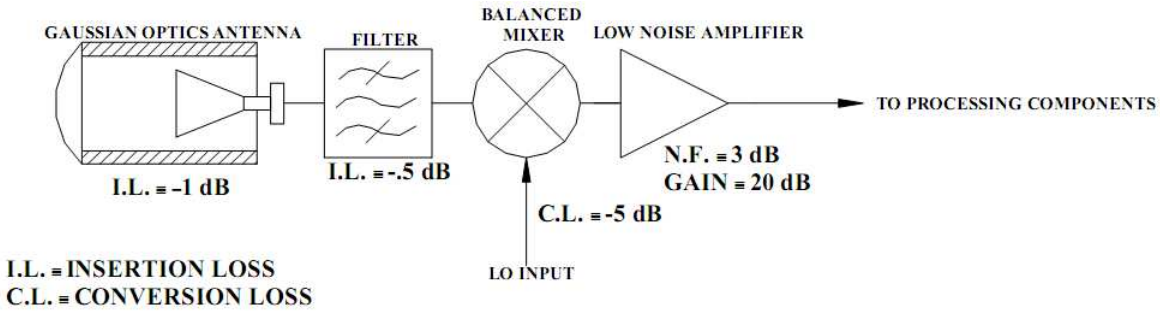


Figure IV.67. Receiver front end example [27]

The relative noise power at a measurement bandwidth of 100 kHz to that at 1 Hz is 50 dB $\left(10\log\left(\frac{10^5\ \text{Hz}}{1\ \text{Hz}}\right)=50\text{dB}\right)$. The white noise power contribution is then:

$$\left(10\log\left(k\times T\times BW\left[Hz\right]\right)\right)+50\text{dB}=-174+50=-124\text{dBm} \quad (4.\ 19)$$

Using the insertion loss or conversion loss to noise figure equivalence approximation at room temperature, the adding receiver noise figure for the components *Figure IV.67* is:

$$1+0.5+5+3=9.5\text{dB} \quad (4.\ 20)$$

Adding these two values yields an MDS value of –114.5 dBm.

Conclusion

The goal of this thesis is to highlight the 65nm CMOS SOI potentialities for millimeter wave wireless applications via the design of milestone building blocks for reception systems. We have shown that there are several potential applications in the frequency bands above and beyond 60GHz, such as 802.15.3 WLAN, WPAN (wireless HDMI/USB), automotive radar and imaging systems. As the 65nm CMOS SOI technology was not initially developed for millimeter wave design, this work demonstrates the advantages of using this technology for applications at such high frequencies. The demonstration has been focused on two parts. First active and passive devices have been studied in order to evaluate the potentiality for low noise and high gain performances at millimeter frequencies. Different figures of merit have been introduced for both actives and passives. Characterization and modeling techniques improvement developed in this work have been discussed. Then, reception millimeter wave building blocks have been designed such as low noise amplifiers and mixers.

We have seen that the advantages of SOI-MOSFETs in comparison with bulk are important not only for the digital world but also for analog/RF design. Today, for RF applications, the SOI technology allows lowering the total power consumption in both RF and Digital circuits (key for mobile communications). SOI permits also an easier co-integration of analog/RF and Digital circuits (lower cost by chip reduced area). We have also seen that the SOI technology is already used in the industry. The recent SOI consortium creation demonstrates the wish of numerous companies to develop the SOI technology for the mass market.

We have exposed the NMOS transistors millimeter wave performances from the 65nm SOI CMOS technology. First measurements up to 110GHz for SOI CMOS 65nm transistors have been carried out in this thesis work. The maximum f_T and f_{max} of the floating body and body contacted transistors are 155/200 GHz and 132/150 GHz respectively. The NF_{min} performance of the FB transistor is 3.5dB at 80GHz. In comparison with existing CMOS state of the art at that time (*Table II.3*), these measured performances showed the best noise performance reported.

This thesis work proposes millimeter wave frequencies models for passive components on a CMOS BEOL. Specific models for coplanar wave guides, discontinuities, inductors and capacitors have been developed. Each model has been associated with a specific layout cell compliant with industrial requirement. The electromagnetic simulator *MOMENTUM* has been

used at each step of the models development to insure a correct modeling. Finally, measurements at millimeter wave frequencies have completed the models validity.

The CMOS SOI 65nm technology for coplanar wave guide design has been also compared with the silicon transmission lines state of the art. The Electromagnetic simulations and measurement performed in bulk and SOI permitted to evaluate and compare the technology and the transmission line topologies (*Table III.1*). The High Resistivity substrate potentiality and interest for millimeter wave passive components have been demonstrated. Measurements and electromagnetic simulations have highlighted the increase performances by using SOI substrate instead of bulk.

We have then investigated the design of several millimeter wave building blocks. My contribution consists in the introduction of a systematic modeling of every possible layout interconnection. This methodology is very important in millimeter wave design in order to evaluate the layout limiting factors at each design step. For instance, it permits to take into account the impact of specific layout compliant with industrial design rules (dummies, metallic layer with holes, etc…). The result is a very good fitting between simulations and measurements for every designed circuit. This work has also contributed to the development of an optimized MOSFET layout topology (*FR patent filed ref: 07157371*). Stability issues, transistor matching and overall methodology to design multi-stages amplifier have been discussed. We have exposed different blocks achieved in both CMOS SOI and bulk in order to benchmark the two technologies. The 65nm CMOS SOI process proved to be a very promising technology for millimetre wave applications among other the 80GHz 3 stages LNA developed in this work which is state of the art in term of CMOS noise performance at 80GHz. We have also illustrated the benefit of the CMOS SOI with a comparison of two blocks designed at the same frequency in both technologies. The CMOS SOI has demonstrated a very good improvement in terms of power consumption and area saving. This work generated several publications in IEEE conferences such as ESSCIRC 2007, RFIC 2007, SOI International Conference 2007, IMS 2007, PRIME 2006 and so on.

In the near future, SOI is clearly one of the most promising solutions for applications at millimeter wave frequencies. As we have seen, wireless technologies require high-performance transistors and low-loss passive devices. One major point not studied in this work is the ability to design on-chip antenna in SOI. Today, the SOI CMOS silicon technology is the only one allowing this type of approach at millimeter wave frequency. Nevertheless, although a mass product should lower the cost of the SOI technology, a choice between benefits associated to SOI and additional cost in comparison with bulk have to be considered for each targeted applications.

Appendix

Author publications:

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Author patent:

Martineau, B.; Cathelin, A., "Optimized MOS topology on CMOS process for millimeter wave design", *FR Patent Application ref: 07157371* , Sept 2007.

RESUME EN FRANÇAIS

I. Introduction

La bande de fréquence millimétrique est définie de 30 à 300GHz, ce qui signifie une longueur d'onde associée allant de 1 à 10mm comme le montre la Figure 1 :

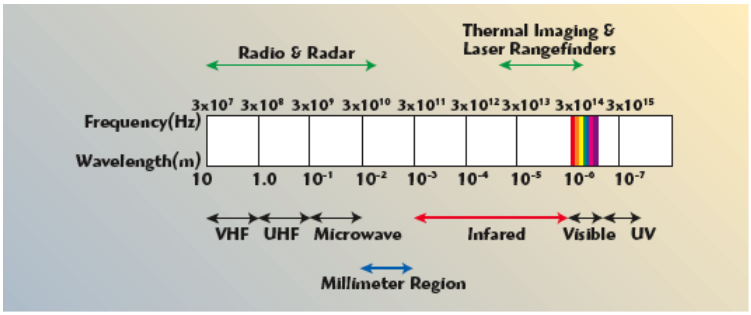


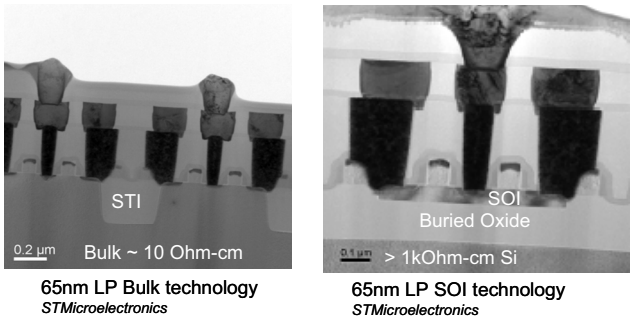
Figure 1. Région millimétrique du spectre électromagnétique

Dans cette gamme de fréquence, trois grands domaines d'applications peuvent être distingués. Tout d'abord, les réseaux de communication à hauts débits et les liaisons sans fils de type USB ou HDMI qui utilisent les fréquences autour de 60GHz. Le second marché lié aux fréquences millimétriques concerne les radars anticollisions pour l'automobile qui fonctionnent à 77GHz. Enfin, citons les systèmes de visualisation non-intrusive utilisés par exemple pour la détection d'armes dans les aéroports qui eux fonctionnent à 94GHz et au-delà.

Dans le contexte de ces futurs marchés pour l'industrie du semi-conducteur, cette thèse vise à démontrer les potentialités de la technologie CMOS SOI 65nm en termes de performances à des fréquences allant de 60 à 94GHz. Pour mener à bien cette démonstration ce travail est décomposé en trois parties. Tout d'abord les particularités et les avantages liés à la technologie CMOS SOI sont exposés. Ensuite, les performances et la modélisation des composants actifs et passifs sont présentés. Enfin, une dernière partie illustre à travers des amplificateurs à faible bruit et des mélangeurs les performances qu'il est possible d'atteindre avec la technologie CMOS SOI 65nm.

II. La technologie CMOS SOI

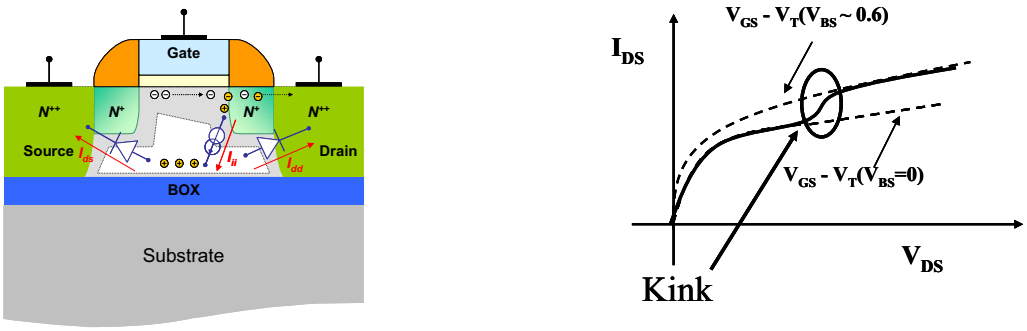
La technologie SOI présente la particularité d'avoir une couche d'oxyde enterré sous la zone active du substrat (Figure 2, *b*), ce qui permet une isolation diélectrique complète du transistor. Cette couche d'oxyde présente de nombreux avantages liés au comportement physique du transistor. Elle permet par exemple une meilleure immunité aux radiations et aux phénomènes de "latch-up", une diminution des courants de fuite et des capacités de jonctions (avantage très important pour les applications numériques) et enfin elle permet l'utilisation d'un substrat haute résistivité. Cette dernière particularité fait de la technologie SOI un candidat naturel pour les applications RF et millimétrique.



a) *b)*

Figure 2. Vue en coupe des technologies CMOS 65nm sur substrat massif (a) et SOI (b)

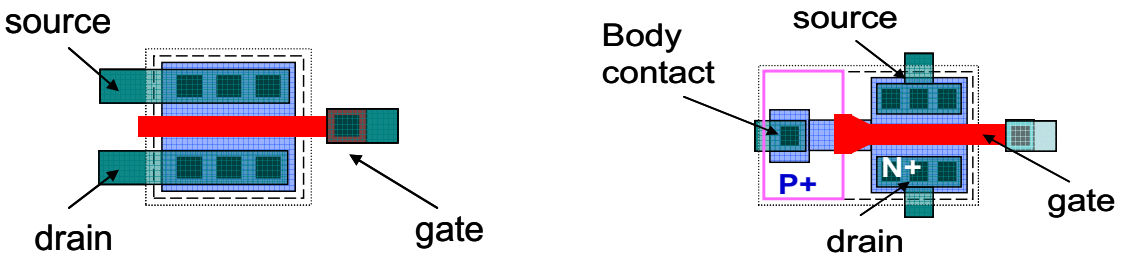
Le comportement DC du transistor sur substrat SOI diffère également avec l'apparition, entre autre, de l'effet "kink". Ce phénomène est dû au mécanisme d'ionisation par impact dans les régions de champs électriques élevés près du drain (Figure 3). Au-delà d'une certaine tension de drain les électrons possèdent suffisamment d'énergie pour générer des paires électrons-trous. L'accumulation des trous induit une augmentation du potentiel de la zone interne, ce qui va polariser la jonction substrat-source et permettre l'écoulement des charges positives générant un "kink" sur la pente de la caractéristique $I_{ds}=f(V_{ds})$ (Figure 3 *b*)



a) *b)*

Figure 3. Illustration de l'effet kink au sein du transistor (a) et son effet sur le comportement DC (b)

Lorsque les applications le requièrent, pour palier cet effet, un transistor spécifique à cette technologie existe. Il s'agit un transistor disposant d'une prise externe pour polariser la zone active du transistor. Ce transistor est appelé transistor à prise (*Figure 4 –b*) en opposition au transistor dit flottant (*Figure 4 –a*).



a) *b)*

Figure 4. Transistors de la filière CMOS SOI 65nm

III. Les éléments actifs dans la technologie CMOS SOI 65nm

La figure suivante représente le modèle petit signal non-quasi statique du transistor NMOS. Ce modèle permet entre autre d'évaluer les performances du transistor à partir des figures de mérite f_T et f_{max}. Il permet également de modéliser le bruit associé au transistor grâce à deux sources de bruit non-corrélées (e_g et i'_d).

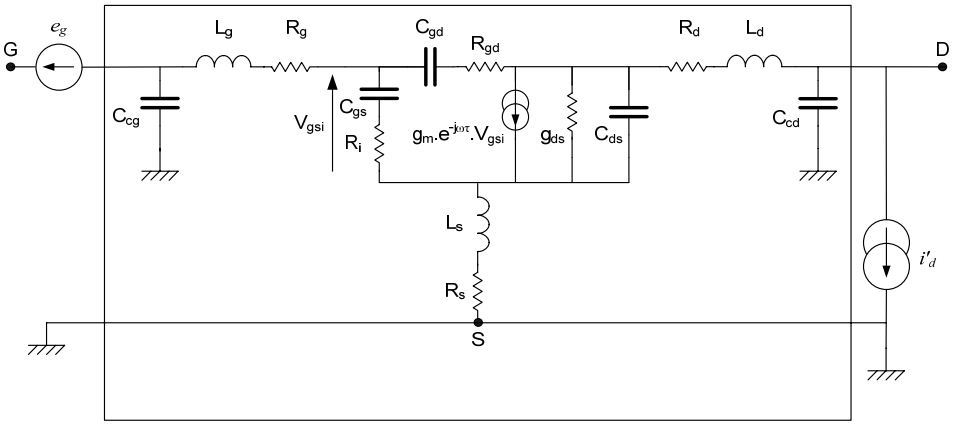


Figure 5. Modèle petit signal non-quasi statique du transistor NMOS incluant 2 sources de bruit non-corrélées

Ce modèle peut être extrait directement à partir de la mesure et permet d'évaluer la stabilité, le gain, le bruit ainsi que l'adaptation en petit signal. Dans ce travail les transistors de la filière CMOS SOI 65nm présentés dans la première partie (transistors flottants et à prises) ont été caractérisés sur une large gamme de fréquence. Ces mesures ont permis d'évaluer leurs performances pour des applications à très hautes fréquences et d'extraire un

modèle petit signal non quasi statique. La figure suivante montre les figures de mérite f_T et f_{max} ainsi que la figue de bruit minimum et le gain associé:

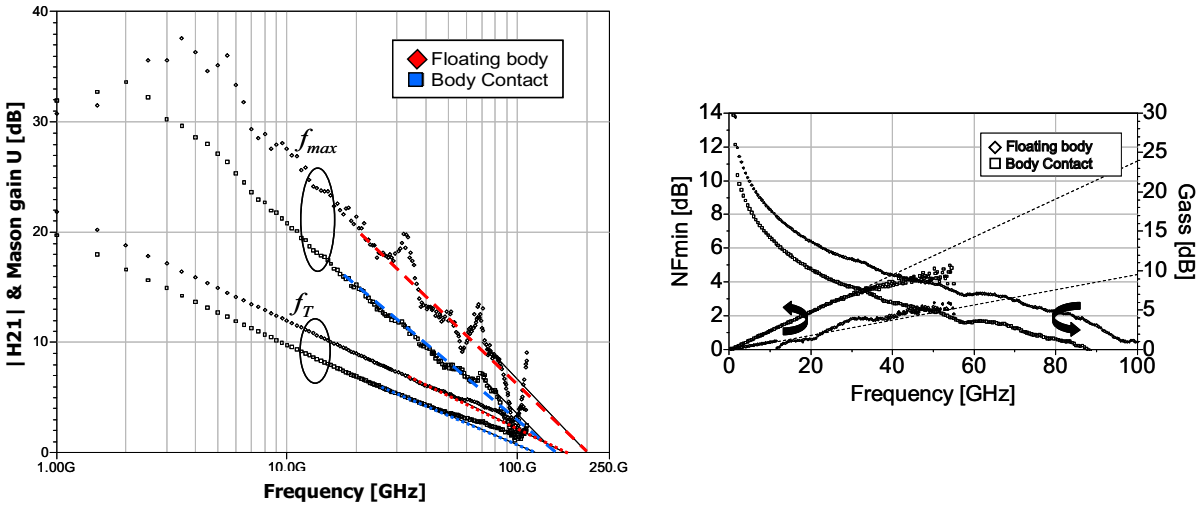


Figure 6. f_T , f_{max} , figure de bruit minimum et gain associé pour les transistors flottants et à prises de la filière CMOS SOI 65nm – V_{ds}=1.2V, Id=300mA/mm –NMOSFET 48x1.33x0.06µm²

La Figure 6 montre que le transistor flottant offre des meilleures performances avec un f_T et f_{max} de 160GHz et 200GHz. Ceci s'explique par la capacité parasite liée à la prise de contact sur le transistor à prise qui dégrade les performances en hautes fréquences. Il est à noter cependant que la géométrie optimum en terme de performances n'est pas la même pour les deux types de transistors.

La Table 1 résume l'état de l'art des performances f_T et f_{max} et NF_{min} pour les transistors CMOS *:*

References	Technology Nodes	Foundries	L_{poly} (nm)	f_T(GHz)	f_{max}(GHz)	NFmin @ 10GHz
Chapitre II [27]	CMOS SOI PD 130	IBM	70	141	98	<1.5
Chapitre II [28]	CMOS SOI PD DTMOS 130	Fujitsu	80	185	120	0.8
Chapitre II [29]	CMOS SOI LP PD 130	ST	80	96	150	1.3
Chapitre II [30]	CMOS SOI HP 90	IBM	45	243	208	-
Chapitre II [31]	CMOS SOI HP 65	IBM	32	220	320	1.4
Chapitre II [32]	CMOS 65	Intel	29	360	420	-
Ce travail	CMOS SOI LP 65	ST	60	160	200	0.5
Chapitre II [24]	CMOS LP 65	ST	60	160	200	0.5
Chapitre II [33]	CMOS SOI HP 65	IBM	27	360	-	1
Chapitre II [8]	CMOS LP 45	ST	40	220	-	-
Chapitre II [34]	CMOS 45	IBM	36	350	400	1

Table 1. Performances des transistors CMOS et CMOS SOI de différents fondeurs

IV. Les éléments passifs dans la technologie CMOS SOI 65nm

La réalisation d'éléments passifs avec un haut facteur de qualité constitue un des avantages majeurs de la technologie CMOS SOI (sur substrat haute résistivité) en comparaison avec la technologie CMOS sur substrat massif. La Figure 7 montre les constantes atténuations obtenues pour différentes topologies de lignes de transmission avec plusieurs technologies :

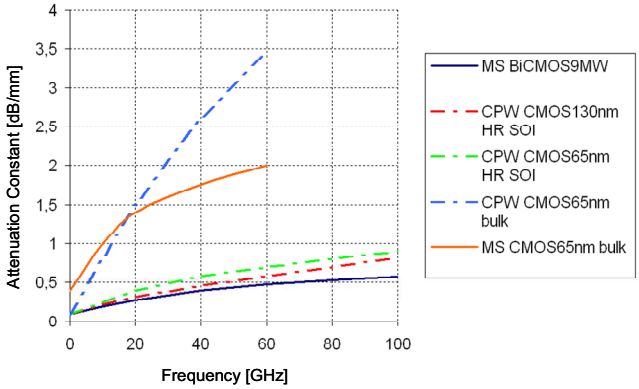


Figure 7. Constante d'atténuation de différentes lignes de transmission utilisant plusieurs technologies

Comme le montre cette figure le SOI permet un gain très important en comparaison avec la technologie CMOS standard. Seul des technologies dédiées aux applications millimétriques permettent d'atteindre de meilleures performances. Des résultats similaires ont été obtenus avec des éléments localisés comme les inductances [Chapitre III – 7].

Les lignes de transmission tel que les lignes micro-rubans ou coplanaires peuvent être modélisées à l'aide des paramètres r, l, c, et g comme le montre la Figure 8 :

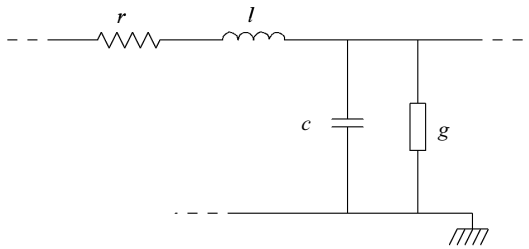


Figure 8. Circuit électrique équivalent d'une ligne de transmission

Dans le cas d'une technologie silicium multicouche comme la technologie CMOS 65nm cette modélisation requière une évaluation des éléments couche par couche. La Figure 9 illustre à travers l'élément capacitif cette distribution au travers les différents diélectriques composant une ligne coplanaire.

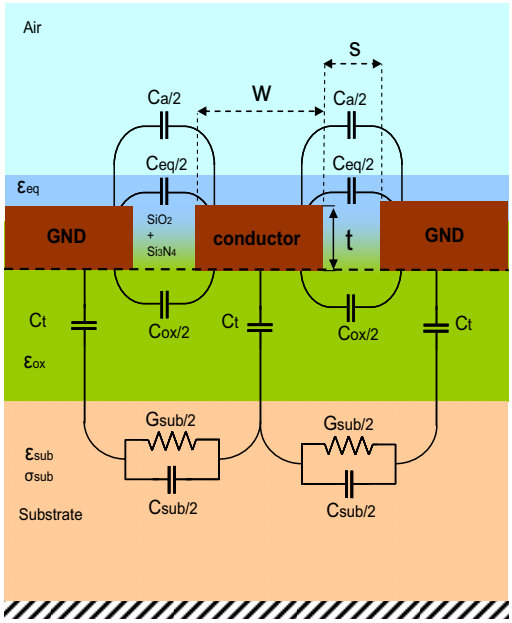


Figure 9. Elément électrique parallèle d'une ligne coplanaire

Dans cette étude un modèle analytique permettant de prendre en compte tous ces éléments à été développé. La figure suivant montre une comparaison entre le modèle développé et la mesure d'une ligne coplanaire:

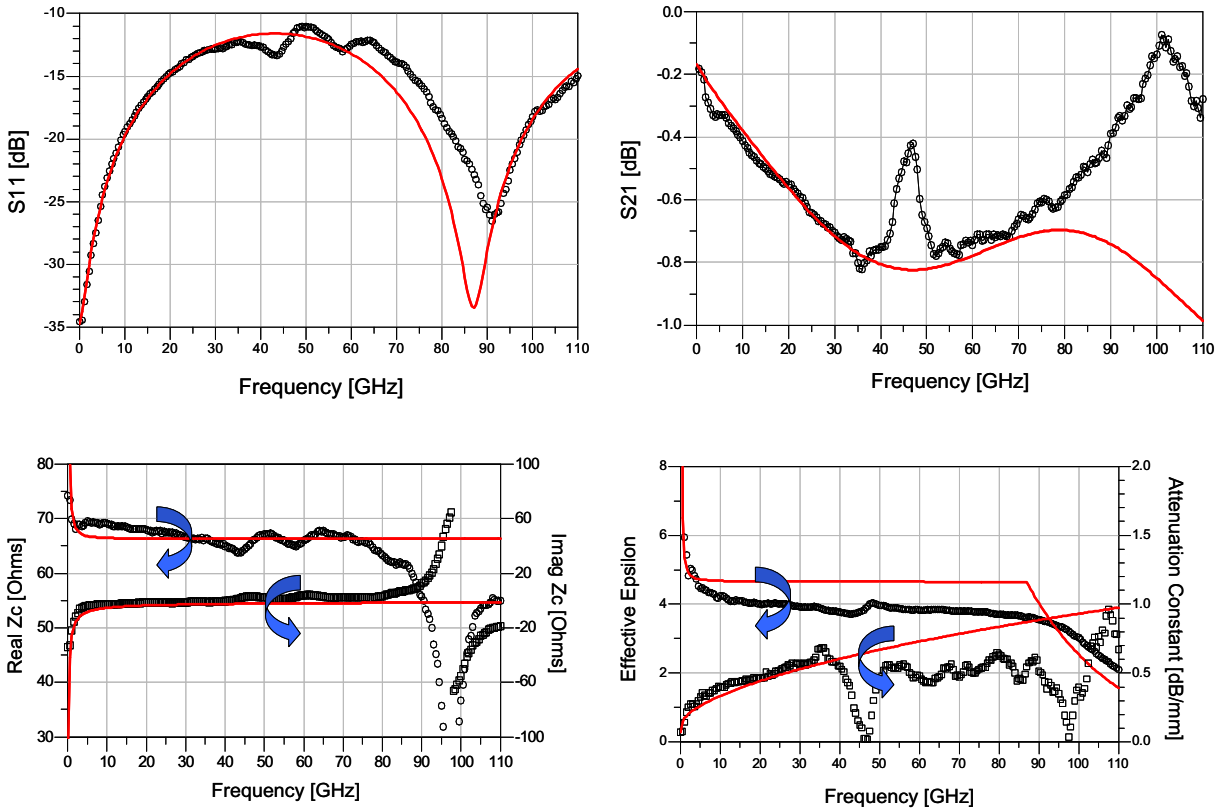


Figure 10. Modèle (ligne continue) et mesure d'une ligne coplanaire (largeur 12µm, inter-masse 22µm)

A partir d'un modèle de ligne de transmission les différentes discontinuités peuvent être aisément modélisées (coude, T de jonction, jonction croix, etc...)

V. La conception de blocs pour une chaîne de réception en bande de fréquence millimétrique

Dans cette partie, l'évaluation de la technologie ne porte plus les composants actifs ou passifs mais sur deux blocs d'une chaine de réception. Tout d'abord les Tables 2 et 3 dressent l'état de l'art des amplificateurs faibles bruits et des mélangeurs dans les technologies CMOS.

Nœud CMOS	f_T/f_{max} (GHz)	**Fréquence (GHz)**	**Gain (dB)**	**S_{11}/S_{22} (dB)**	**Puissance (mW)**	**Figure de bruit (dB)**	**Pin_{-1dB} (dBm)**	**IIP_3 (dBm)**	**Surface (mm^2)**	**Ref.**
130nm	140/135	57	12.0	-15/-15	54 @1.5V	8.8	-10.0	-0.36***	-	Chapitre IV [8]
130nm	108/91	55	24.7	-8/-5	79 @2.4V	8.0	-22.7	-12	0.48	Chapitre IV [9]
SOI 90nm	149/147	40	9.5	-6/-8	40.8 @2.4V	4	-7.9	1.74***	-	Chapitre IV [5]
90nm	107/180	61.3	17.9	-	21.6 @1.5V	5.2	-	-6.5***	0.86	Chapitre IV [4]
90nm	140/170	58	14.5	-6/-6	24 @1.5V	4.5*	-24.5	-6.8	0.14	Chapitre IV [10]
90nm	100/200	62	12.2	-12/-30	10.5 @1.5V	6.0*	-8.2	1.44***	0.48	Chapitre IV [11]
90nm	107/180	52	25	-20/-17	110 @1.5V	5	-20 @48GHz	-10***	1.13	Chapitre IV [12]
90nm	-	64	15.5	-25/-15	86 @1.65V	6.5	-11.7	-2.06***	0.52	Chapitre IV [14]
SOI 65nm	160/200	80	7.2	-14/-10	70 @1V	5.7	-3.75*	5.89***	0.98	Ce travail
65nm	-	60	11.5	-9/-7	104 @1.2V	5.6	-10	-0.36***	0.6	Chapitre IV [13]
65nm	160/190	55	15	-18/-11	30 @1.2V	9.0**	-27	-17	0.74	Ce travail
65nm	160/190	55	22.5	-22/-11	50 @1.2V	8.0**	-29	-20.5	0.74	Ce travail

* Simulé

** Simulé base sur la mesure d'un seul point de fréquence (cf. Chapitre IV)

*** Estimé à partir de la relation suivante : $ICP_1[dBm] = IIP_3[dBm] - 9.64[dBm]$

Table 2. Etat de l'art de différents amplificateurs à faible bruit conçus dans des technologies CMOS

Plusieurs points sont remarquables dans cette première table. Tout d'abord il apparaît que la meilleure performance est obtenue avec une technologie 90nm. Ceci s'explique de la manière suivante. Pour un nœud technologique donné le transistor peut être de type faible puissance ou haute performance ce qui conditionne le gain disponible. D'autre part plus le

nœud technologique est petit plus les couches métalliques qui composent les interconnections sont rapprochées réduisant les performances des composants passifs. Ainsi, pour un amplificateur, un nœud technologique 90nm peut très bien être considéré comme aussi performant qu'un nœud 65nm. L'autre point remarquable concerne les tensions d'alimentation utilisées et leurs impactes sur la robustesse des circuits. Certaine tension permettent d'atteindre de bonnes performances mais ne pourront jamais être utilisées dans un produit manufacturé.

La seconde table présente les performances obtenues pour différents mélangeurs:

Nœud CMOS	Fréquence (GHz)	Gain de Conversion (dB)	Figure de bruit (dB)	Puissance OL (dBm)	Isolation entre OL et RF (dB)	ICP_1 (dBm)	IIP_3 (dBm)	Topologie	Puissance (mW)	Ref.
180nm	24	13	-	-	-	-	-	Active single to balanced	6	Chapitre IV [15]
130nm	60	-2	11.5**	0	-12	-3.5	-	Active single ended	2.4	Chapitre IV [16]
90nm	60	-11.6	12.6*	4	-	6	16.5	Resistive single ended	~0	Chapitre IV [17]
90nm	31	-11	-	9.7	-27	-	3	Resistive Source pumped	~0	Chapitre IV [18]
SOI 90nm	27	-10.3	11.3*	0	-24	-	12.7	Resistive Gate pumped	~0	Chapitre IV [19]
65nm	60	-12.5	13.5*	8.7	-35	5	-	Resistive single to balanced	~0	Chapitre IV [20]
65nm	60	-14.8	20*	0	-20	-4**	6*	Resistive gate pumped	~0	Ce travail
SOI 65nm	60	-7.7	9*	-5	-20	-10	0	Resistive drain pumped	~0	Ce travail

* Estimé (cf. *Chapitre IV)*
** Simulé

Table 3. Etat de l'art de différents mélangeurs conçus dans des technologies CMOS

Il ressort de la Table 3 que les technologies CMOS avancées présentent peu d'avantages pour les mélangeurs. On constate cependant que les mélangeurs passifs offrent de meilleures performances en linéarité tout en offrant l'avantage d'avoir une consommation négligeable. Cependant, contrairement aux mélangeurs actifs ils présentent des pertes de conversion élevées. Ainsi suivant les spécifications dictées par le système une architecture ou une autre peut être privilégiées

Afin d'évaluer la technologie CMOS SOI 65nm dans la bande millimétrique, un premier amplificateur faible bruit a été conçu pour les fréquences allant de 80GHz à 94GHz. La figure

suivante montre le schématique de l'amplificateur réalisé. Il s'agit un amplificateur à source commune non dégénérée.

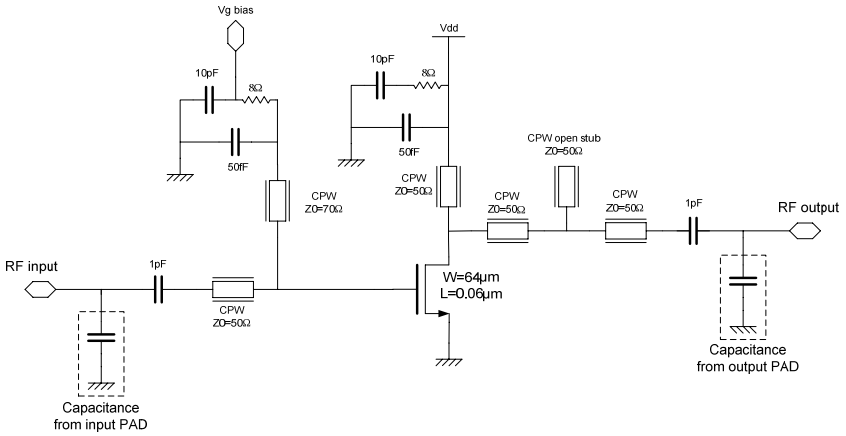


Figure 11. Amplificateur source commune

Les performances obtenues pour cet amplificateur sont résumées dans la table suivante :

Amplificateur CMOS SOI 65nm en source commune

Fréquence	80GHz	94GHz
Gain Maximum	2.1dB	2.3dB
Pertes d'insertion en entrée/sortie	-13/-6dB	-9/-12dBm
Figure de bruit	4.5dB	5.5dB
ICP$_1$*	0dBm	0dBm
Puissance	22mW	22mW
Surface	0.64mm²	0.64mm²

*Simulé

Table 4. Performance d'un amplificateur CMOS SOI 65nm à un étage en source commune

Ce circuit, qui sert de démonstrateur technologique, montre qu'il est possible d'obtenir 2dB de gain avec une figure de bruit associée d'environ 5dB pour des fréquences supérieures à 80GHz.

Le circuit suivant reprend la précédente architecture mais avec trois étages en sources communes. Le but étant d'augmenter le gain.

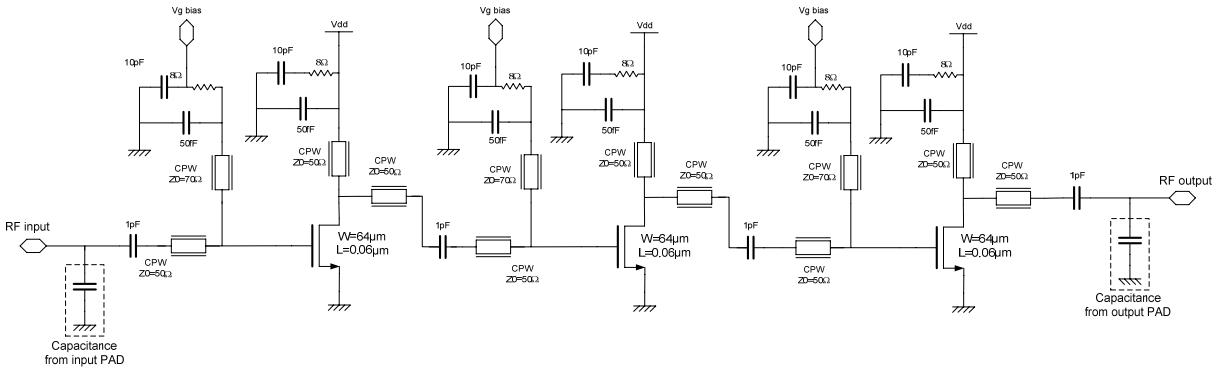


Figure 12. Amplificateur faible bruit à 3 étages

Les performances obtenues pour cet amplificateur à trois étages sont résumées dans la table suivante :

Amplificateur CMOS SOI 65nm à 3 étages en sources communes	
Fréquence	80GHz
Gain Maximum	7.2dB
Pertes d'insertion en entrée/sortie	-11/-9dBm
Figure de bruit	5.7dB
ICP$_1$*	-3.75dBm
Puissance	70mW
Surface	0.98mm²

Table 5. Performances d'un amplificateur CMOS SOI 65nm à 3 étages en source commune

Avec trois étages ce circuit présente plus de 7dB de gain tout en ayant une figure de bruit inférieur à 6dB ce qui représente l'état de l'art pour un circuit CMOS à 80GHz. Il est à noter que ce circuit présente également une bonne adaptation entrée/sortie. Afin d'évaluer également les performances pour des applications dans la bande 60GHz un autre amplificateur à trois étages a été conçu. Cette fois-ci les étages ne sont plus de type source commune mais de type cascode. En effet à 60GHz la contrainte bruit/gain étant plus relâchée cette topologie permet d'obtenir d'avantage de gain. La Figure 13 montre le schématique de cet amplificateur.

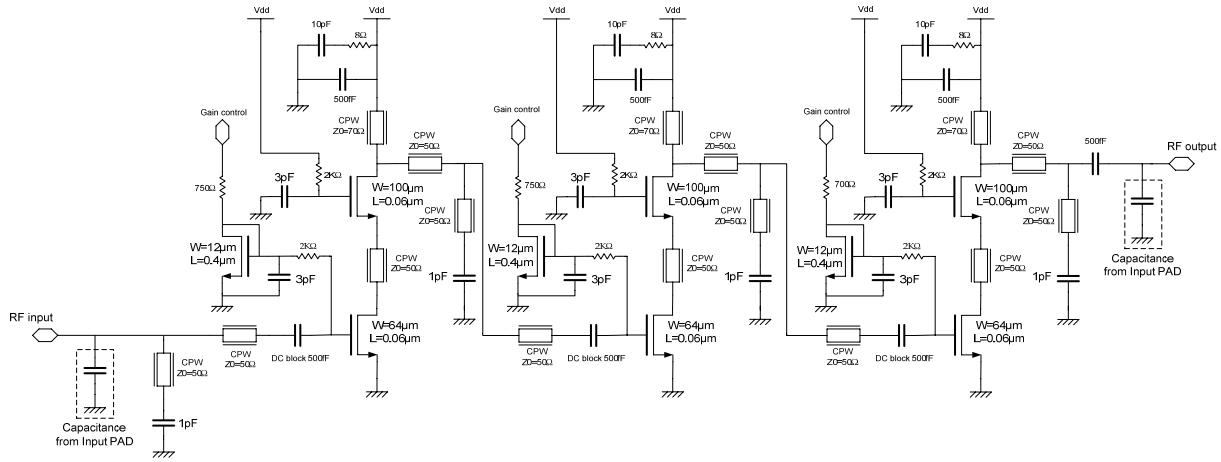


Figure 13. Amplificateur faible bruit à 3 étages cascode

La Table 6 résume les performances simulées :

Amplificateur CMOS SOI 65nm à 3 étages cascodes	
Fréquence	60GHz
Gain Maximum	20.5dB
Pertes d'insertion en entrée/sortie	-19/-21dBm
Figure de bruit	6.5dB
ICP$_1$*	-30dBm
IIP3*	-21dBm
Puissance	20mW
Surface	1.31mm²

*estimated

Table 6. Performances d'un amplificateur CMOS SOI 65nm à 3 étages cascodes

Ces performances simulées montrent qu'il est possible d'atteindre plus de 20dB de gain à 60GHz avec une figure de bruit de 6.5dB tout en consommant 20mW. Ces performances sont en ligne avec l'état de l'art pour ce type d'amplificateur.

La deuxième évaluation de la technologie CMOS SOI s'est portée sur le mélangeur. Pour des raisons pratiques de mesures, l'évaluation à portée sur un mélangeur non-différentiel de type résistif à pompage du drain. Le schématique de ce type de mélangeur est présenté Figure 14:

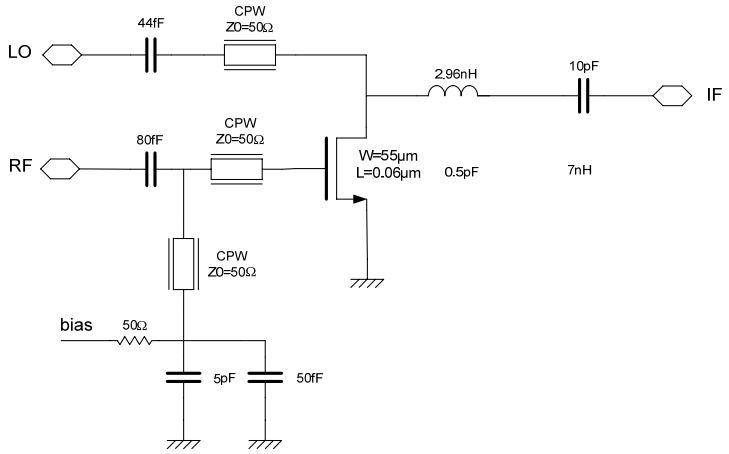


Figure 14. mélangeur à pompage de drain

Les performances simulées à 60GHz pour ce mélangeur sont résumées dans la table suivante:

Mélangeur sur SOI		
P_{LO}	-5dBm	0dBm
Gc	-7.7dB	-5.8dB
ICP1	-10dBm	-5dBm
IIP3	0dBm	4dBm
NF	9dB	7dB
OL-FI iso.	37dB	37dB
Puissance	10µW	10µW
OL/RF pertes	< -20dB	< -20dB

Table 7. Performances d'un mélangeur CMOS SOI 65nm à pompage de drain

Les performances simulées de ce mélangeur ont également montré l'intérêt de la technologie SOI avec des résultats proches de l'état de l'art

Afin de comparer la technologie CMOS 65nm sur substrat massif et SOI, un amplificateur faible bruit fonctionnent à 60GHz à également été réalisé sur substrat massif. Ce circuit à donné lieu à l'expérimentation de protections contre les décharges électrostatiques sur l'entrée RF. Cette expérimentation constitue une première en CMOS à ces fréquences. Le schématique de ce circuit est présenté à la Figure 15.

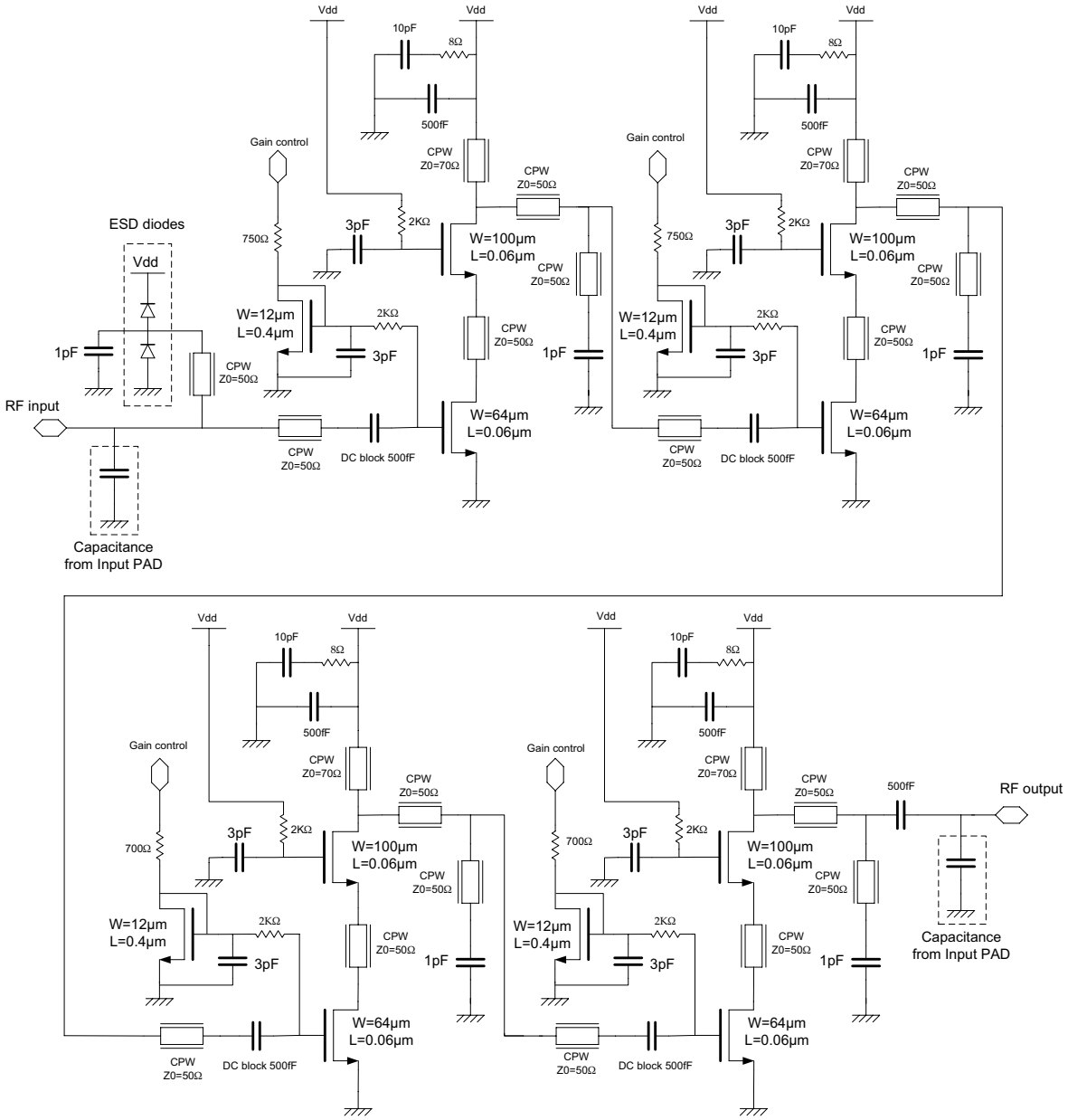


Figure 15. Amplificateur faible bruit à 4 étages cascode intégrant des protections ESD

Ce circuit possède un contrôle de gain extérieur. La Table 8 résume les performances mesurées pour plusieurs choix de gain.

Amplificateur CMOS 65nm à 4 étages cascodes avec protections ESD			
Fréquence	55GHz	55GHz	55GHz
Gain Maximum	15dB	22.5dB	24dB
Bande passante	6GHz	6GHz	6GHz
Pertes d'insertion en entrée/sortie	-18/-11dB	-22/-11dB	-22/-11dB
Figure de bruit	9dB	8dB	8dB
ICP_1*	-27dBm	-29dBm	-30dBm
IIP3*	-17dBm	-20dBm	-21dBm
Puissance	30mW	50mW	65mW
Surface	1.55mm²	1.55mm²	1.55mm²

Table 8. Performances d'un amplificateur CMOS 65nm à 4 étages cascodes

Ce circuit montre des performances en retrait en comparaison avec la version simulée en CMOS SOI. Cependant il démontre qu'il est possible d'utiliser des protections contre les décharges électrostatiques (ESD) sur l'entrée RF sans atténuer le signal si les diodes de protection sont placées en bout de ligne parallèle et non directement sur le plot d'entrée.

Suivant la même volonté de comparaison, un mélangeur passif a également été réalisé sur substrat massif. Celui-ci est de type résistif à pompage de grille. Cette topologie offrant des meilleurs résultats dans ce cas précis. La Figure 16 montre le schématique de ce circuit.

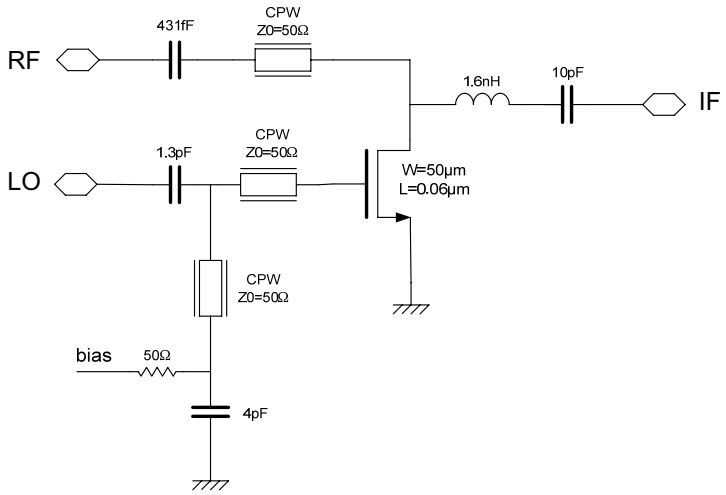


Figure 16. Mélangeur à pompage de grille

Les performances mesurées à 60GHz pour ce type de mélangeur sont résumées dans la table suivante. On observe que les performances sont en recul par rapport aux performances observées en CMOS SOI. Ceci s'explique principalement par l'atténuation liée aux éléments passifs qui est très élevée dans un substrat massif.

Mélangeur sur substrat massif

P_{LO}	-5dBm	0dBm
Gc	-18.8dB	-14.85dB
ICP1	-2dBm	-4dBm
IIP3	8dBm	6dBm
NF	19.8dB	16dB
OL-FI iso.	25dB	25dB
Puissance	-	-
OL/RF pertes	-	-

Table 9. Performance d'un amplificateur CMOS SOI 65nm à 3 étages cascode

Enfin un dernier circuit a été réalisé. Celui-ci intègre l'amplificateur et le mélangeur décrit précédemment sur substrat massif. Une photographie de ce circuit est donnée Figure 17:

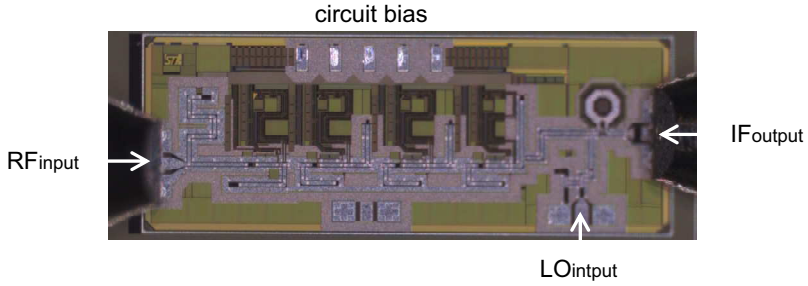


Figure 17. Photographie de l'intégration amplificateur + mélangeur

Les performances obtenues avec ce circuit sont résumées dans la table ci-dessous:

Amplificateur + mélangeur	
P_{LO}	-5dBm
Gain	13.25dB
ICP1	-31.2dBm
IIP3*	-21.4dBm
Figure de bruit*	8dB
LO-FI iso.	25dB
Puissance	60mW

Table IV.1. Performance de l'amplificateur combiné au mélangeur

**estimé*

Ces résultats sont en ligne avec les performances obtenues pour les blocs pris séparément. Les performances sont principalement dégradées par le mélangeur et les composants passifs. Une meilleure architecture pour ce type de technologie serait probablement d'utiliser un mélangeur actif ce qui permettrait d'augmenter le gain de la chaine complète.

VI. Conclusion

Au travers ces différentes parties nous avons vu les avantages liés à la technologie SOI aussi bien au niveau des composants (actifs et passifs) qu'au niveau des circuits. Grace à ce travail nous pouvons affirmer que la technologie CMOS SOI 65nm permet de réaliser des circuits proches de l'état de l'art à des fréquences millimétriques. Tous les démonstrateurs présentés ici ont été réalisés avec des contraintes industrielles en respectant les règles de conception (d'électromigration, densité métallique) afin d'évaluer de manière critique cette technologie.

Ce travail à également permis le développement de nouvelles méthodes de conception dans un environnement industriel. Ces résultats ont donné lieu à plusieurs communications internationales avec acte ainsi qu'un dépôt de brevet.