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par **Nicolas Delaunay**

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Linearization of a Transmitter Using an IC Digital/Analog Cartesian Feedback in 65nm CMOS for Advanced Communication Standards

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Après avis de :

M.	**Jean-Louis Cazaux**	Ingénieur (HDR)	Thales Alenia Space	Rapporteur
M.	**Jean-Michel Nebus**	Professeur	XLIM de Limoges	Rapporteur

Devant la commission d'examen formée de :

M.	**Didier Belot**	Ingénieur	STMicroelectronics	Tuteur industriel
Mlle	**Nathalie Deltimple**	Maître de conférences	IPB ENSEIRB-MATMECA	Co-directeur de thèse
M.	**Eric Kerhervé**	Professeur	IPB ENSEIRB-MATMECA	Directeur de thèse
M.	**Vincent Knopik**	Ingénieur	STEricsson	Invité
M.	**Dominique Dallet**	Professeur	IPB ENSEIRB-MATMECA	Examinateur

A ma famille et mes amis,

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Résumé:

Depuis la première génération de téléphone mobile, de nombreuses fonctions et outils ont été intégrés dans nos terminaux. Il y a vingt ans, nous utilisions nos téléphone pour émettre des appels et envoyer/recevoir des messages. Aujourd'hui, l'accès à internet, la radio, l'appareil photo, des jeux et de la musique sont des fonctionnalités que l'on retrouve dans nos téléphones mobiles.

Dans un contexte de téléphonie pouvant adresse plusieurs standards, l'objectif de cette thèse est de concevoir et de réaliser l'implémentation d'une architecture capable d'améliorer la linéarité de notre émetteur pour le standard 3G, utilisant des composants analogiques et numériques. Pour cela, notre étude se concentrera sur l'amélioration de la linéarité, tout en maintenant une consommation la plus faible possible mais également tout en évitant d'augmenter la taille d'une puce 3G. Nous allons démontrer qu'il est possible d'intégrer une technique de linéarisation tout en maintenant une consommation et une surface en silicium.

Le premier chapitre présente différentes architectures d'émetteurs et des techniques de linéarisation avec leurs avantages et inconvénients. Il est également présenté des moyens d'évaluer l'efficacité d'un émetteur par des simulations ou des mesures. L'objectif de cette partie est de choisir une technique de linéarisation à laquelle nous associerons une architecture d'émetteur afin de répondre le plus rigoureusement à notre application et ces contraintes émanant.

Le second chapitre détaille le fonctionnement du système complet, la partie numérique et la partie analogique, s'appuyant sur des études théoriques. Nous commencerons en détaillant les contraintes et les précautions qui doivent être prises en compte par le concepteur afin d'étudier l'instabilité et le bruit produit par l'émetteur. Nous décrierons alors deux algorithmes numériques permettant de réaliser la correction des signaux. Des simulations au niveau système de la boucle Cartésienne seront également présenté utilisant, dans un premier temps un amplificateur de puissance idéal, pour ensuite utilisé

un amplificateur de puissance réalisé en technologie BiCMOS, et finalement un amplificateur de puissance conçu en technologie CMOS, qui est celle choisie pour notre étude.

Le troisième chapitre présente la synthèse de la partie numérique en technologie CMOS des deux algorithmes précédemment cités, elle prend en compte toutes les étapes ; du code VHDL jusqu'au layout, permettant de réaliser un circuit numérique. Ensuite, il est décrit chaque composant de la boucle cartésienne, avec leurs propres simulations ou mesures. De plus, il est important de garder à l'esprit que l'objectif de cette thèse repose sur l'intégration du système complet (partie analogique et numérique) en technologie CMOS 65nm de STMicroelectronics, démontrant ainsi la faisabilité de la solution.

Dans un premier temps, nous décrirons la partie numérique permettant de réaliser les étapes de correction de phase et de soustraction des signaux en technologie ASIC. L'algorithme de CORDIC a pour avantage de minimiser la consommation et l'occupation en Silicium de la partie analogique. Par la suite, l'architecture et les spécifications de chaque brique de base constituant la partie analogique seront présentées. Dans notre cas, la chaîne directe est composée de filtres, de mélangeurs, et d'un amplificateur de puissance. Notre objectif est de réaliser ces trois fonctions avec le minium de consommation et une surface du circuit la plus faible possible, ceci permettant une intégration plus aisée.

Finalement, les simulations système seront présentées utilisant le logiciel de simulation ADC (Advanced Design Software) d'Agilent pour la partie analogique. Des co-simulations ont été réalisées sur le système complet, utilisant SystemVue pour la partie numérique. Les simulations réalisant ADS nous ont fourni les performances de chaque brique de base s'appuyant sur les caractéristiques des transistors.

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Introduction

Since the first generation of mobile phones, a lot of functions, standards and tools have been integrated on handsets. Twenty years ago, consumers could use their mobile phones only to call and to send messages. Nowadays, internet access, radio, cameras, games and music are included and available as options for every mobile phone.

All of these new services make the cost of production for a cellular phone more expensive. Despite that, industry has to find a solution to maintain their products the most attractive as possible including the large range of integrated functions.

Thus, compromises have to be made in order to integrate increasing numbers of chips in a mobile phone. Indeed, new standards impose specifications that make the design challenging in terms of linearity, output power, or even the power injected on the adjacent channel. These requirements make the transmitter less efficient, or less linear. A lower efficiency will increase the power consumption of the chip, and a lower linearity will lead to a lower data rate.

In the context of interaction with other standards, the aim of this thesis is to design and implement a chipset able to improve the linearity of a transmitter for third generation mobile phones, using both digital and analog technologies. For this purpose, the study will focus on the improvement of the linearity, keeping the consumption and the die area of the circuit as small as possible. We will prove that linearization on an integrated circuit is possible with almost the same consumption and die area occupation compared to a classic transmitter. Most importantly, even if a large literature about linearization techniques can be found, only a few show the entire integration in a single technology, as we will show.

The first chapter will present the different architectures used for a transmitter and various linearization techniques with their advantages and drawbacks. Some metrics are also presented in order to evaluate these architectures. The goal of this part is to choose a linearization technique associated to a transmitter in order to fit with our application and constraints.

The second chapter will explain the complete system, digital and analog parts, with theoretical studies. We will start by detailing the constraints and precautions that must be taken into account by the designer to study the instability and the noise generated by the transmitter. We will describe how two algorithms make signal corrections. In the last part we will show system level simulations of the Cartesian Feedback using, first, an ideal power amplifier (PA), then, a PA in a BiCMOS technology, and finally, a PA in a CMOS technology that will be used for the final integrated circuit.

The third and last chapter shows the digital synthesis in a CMOS technology of the two algorithms previously mentioned, considering all steps, from the VHDL code until the layout of the digital part. We will describe and simulate each analog building block of the Cartesian Feedback, with the measurement results for some of them. Each chapter will be working towards the goal of this study, demonstrated in this part: to make an integrated system, with its complete solution and simulations.

Finally a perspective for future work using the Cartesian Feedback will be shown. It concerns the issue of an increase of die area, and consequently cost, when using multi-chips on a mobile phone for different communication standards.

Chapter

1 Linearization of a Transmitter

Contents

Wireless communication standards are continually becoming more sophisticated with the increase of data rate. It remains a delicate operation to transmit data at a high rate without creating distortions through the antenna with a transmitter. That is why the choice of the transmitter architecture is very important for the quality of the communication, a decision that is directly linked to the modulation or the standard used. In the case of the W-CDMA standard, a modulation with non-constant envelope is employed, the HPSK (Hyper Phase Shift Keying) modulation.

It generates a signal varying in phase and amplitude. It is used to reduce the peak-to-average ratio of the signal avoiding the zero crossings and the zero degree phase transitions. As a consequence, special care has to be taken to avoid any distortions on the main signal, which creates unwanted information on the adjacent channel reducing the data rate of the communication.

In this chapter, different transmitter architectures are studied in order to choose the one which will fit better with the integration of radio-frequency components for our application, and also, that will reduce most of the die area and consumption of the whole solution. To improve performance of this transmitter and keep the minimum consumption and die area at the same time, a linearization technique has been chosen among many techniques that we will see below.

1.1 Mobile Communication Standards

Cellular communications have evolved for thirty years in terms of the modulation employed. The first generation used an analog modulation whereas the second generation used a digital modulation. For the next generations of standards, the modulation became more complex with the transmission of images or data. Indeed, from the first generation in Japan (with the standard called DoCoMo) to the third generation of cellular technology, wireless standards have had to handle internet access and other services, such as video streaming, making more complex the modulation employed.

The widespread use of mobile phones all over the world requires good management of the spectrum to avoid interferences. With added economic issues, the establishment of new standards is essential to define requirements for manufacturers and operators.

In Table 1.1, a non-exhaustive list of main standards is given from the first generation of mobile until the fourth generation in Europe. This comparison table shows main features that are more relevant for our study (frequency bands, modulation used, carrier spacing, access methodology).

	NMT [1]	GSM/ DCS [2]	GPRS/ EDGE[3]	UMTS [4]	HSDPA/ HSUPA[4]	HSPA+ [5]	LTE-Advanced [6]
Generation	1G	2G	2.5/2.75G	3G	3.5/3.75G or 3G+/3G++	Evolution 3G++	4G
Approximate Years	1981	1993	2001/03	2004	2007/08	2008/09	2009/10
Frequency bands (Hz)	0.45G-0.9G	0.9/1.8G	0.9G	1.92G/ 1.98G	1.92G/ 1.98G	1.92G/ 1.98G	2.57G / 2.62G
Carriers Spacing (Hz)	12.5/ 25k	200k	200k	5M	5M	5M	15k (sub-carrier)
Access Methodology	-	F/TDMA	F/TDMA	W-CDMA	W-CDMA	MIMO CDMA	OFDMA/ SC-FDMA
Modulation	FM	GMSK	8PSK	HPSK/ QPSK	QPSK/ 16QAM	QPSK/ 16QAM/ 64QAM	QPSK/ 16QAM/ 64QAM
Data Rates (bps)	-	270k	812.5k	0.8-2M	14M	28M	100M

Table 1.1: Evolution of main mobile phone standards

In the 1970s/1980s, the first analog wireless terminals started to appear in cars and in the business world. These mobiles had almost the size of a suitcase and did not cover a lot of territory.

This generation did not guarantee the confidentiality of communications and became saturated using a modulation technique similar to the FM radio. The development of this first generation was limited by the analog modulation used, short spectral resources, low battery lifetime and cost of mobile terminals.

Thus, the second generation became digital in order to increase the capacity and the data rate of wireless communications. This generation insured a better sound quality and confidentiality and reduced the size of terminals. At the beginning of the 1990s, the GSM standard for wireless communication (Global System for Mobile communication) was adopted in Europe. Since this date, the GSM operates around the world except for Japan, South America and North America (which have another standard).

In 2001, an important evolution of the GSM Standard was the GPRS (General Packet Radio Service, also called 2.5G). Concretely, the GPRS standard is an improvement of the GSM; the voice information remained on the GSM network, whereas data used the GPRS standard for a lighter internet access, as an e-mail without an attachment. The GPRS standard allowed a more comfortable connection with the WAP (internet access); however users of mobile phones were not convinced regarding the price and a limited internet connection.

Right after the GPRS, the GSM standard was developed towards the EDGE standard (Enhanced Data rate for GSM Evolution, also called 2.75G). Compared to the GPRS standard, the EDGE is able to send and receive data faster between a mobile phone and a base station. It can be considered as a complement of the future standard UMTS (Universal Mobile Telecommunication System), or a direct competitor of the 3G for a less expensive cost.

The UMTS standard exploits a new protocol of communication, called W-CDMA (Wide-Code Division Multiple Access), and new frequencies between 1900 and 2200MHz. This standard made it possible to reach high data rates for multimedia applications. Moreover, the standard allowed us to send parallel data with a higher data rate, comparing to the GSM and the GPRS. It is not a radical change compared to the second generation but it modified significantly the use of a mobile phone: high speed wireless internet, videophone and video streaming. In theory, the UMTS can reach 2Mbps from a fixed location and 384kbps from a moving point.

After many delays of the development of the 3G, its deployment has finally started in Europe in 2004. The UMTS/W-CDMA standard has been selected in Europe by the 3GPP Association (Third Generation Partnership Project) grouping main telecommunications companies. It required every interested operator to purchase a license issued by its state, and, in parallel, to develop the infrastructure for the GSM/GPRS network. In France in 2004, according to an analysis of users of the 2G by the Telecommunications Regulatory Authority *(Autorité de Régulation des Télécommunications - ART)* more than 70% of French people had a mobile phone.

The worldwide industry of telecommunication is currently developing the fourth generation of mobile phones called LTE-Advanced (Long Term Evolution). This new generation will probably use the OFDM technology (Orthogonal Frequency Division Multiplexing) reaching data rates up to 300Mbps. In order to prepare this generation, specialists developed the evolution of UMTS, called HSDPA (High Speed Downlink Package Access) and HSUPA (High Speed Uplink Package Access). The evolution of the UMTS offered a data rate of 14Mbps and the deployment in Europe began in 2006.

1.2 Transmitter Architectures

Transmitters are mainly composed of converters, filters, mixers, local oscillators and a power amplifier. Their goal is to modulate and up-convert the baseband signal into a higher frequency. The resulting signal is then strengthened by the power amplifier before driving the antenna [7]. A band-pass filter (or a multiplexer) is used to filter the desired channel and send it through the antenna. Nevertheless, it is complicated to determine the architecture of the transmitter without taking into account the architecture of the receiver. Indeed, unwanted frequencies and noise that are generated by the transmitter are injected into the receiver. Ideally, the transmitter and the receiver architectures should be considered at the same time, in order to optimize performance, die area and consumption of the RF circuit.

In this section, main architectures are evaluated. Among the most classic ones, we can find architectures based on a simple or on a double mixing frequency, as homodyne or heterodyne, or otherwise, transmitters based on a PLL (Phase-Locked Loop).

1.2.1 Heterodyne transmitter architecture

The heterodyne transmitter architecture is described in Figure 1.1.

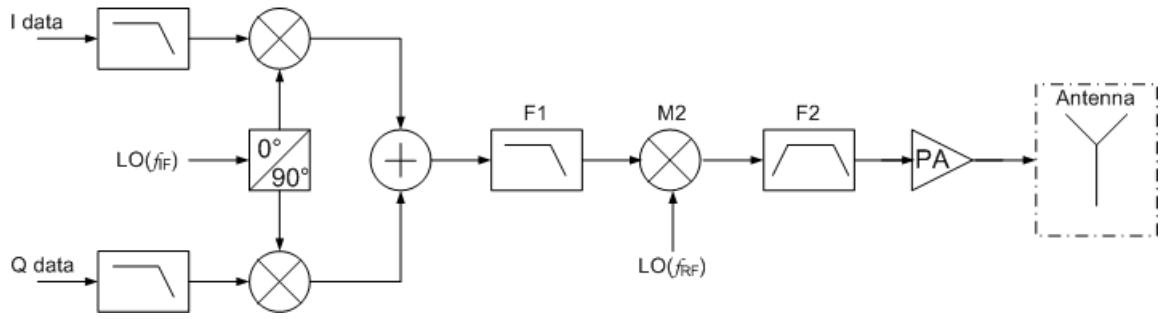


Figure 1.1: Heterodyne transmitter architecture

Analog baseband signals I and Q are up-converted to an intermediate frequency (f_{IF}) by two mixers in quadrature. The signal is then sent to a low-pass filter (F1) which deletes harmonics coming from the f_{IF} frequency. In order to avoid any other distortion coming from the baseband domain, it remains important to realize this operation before to transpose the baseband signal to another frequency ($f_{IF} + f_{RF}$) given by the mixer M2.
The mixer M2 produces two inter-modulations tones at $f_{IF} + f_{RF}$ and $f_{IF} - f_{RF}$ frequencies. As the frequency $f_{IF} - f_{RF}$ is a non-desired tone, a band-pass filter (F2) has to be used to remove it. The resulting signal is finally amplified and transmitted through the antenna.

This architecture works with constant and non-constant envelope modulations and the modulation of signals is made at a low f_{IF} frequency (which is about a few MHz). This architecture, thanks to its two-stages of frequency conversion, obtains good results in terms of sensitivity, selectivity and linearity according to the modulation used; however, it uses two local oscillators which increase the power consumption of the transmitter.

Moreover, as the $f_{IF} - f_{RF}$ tone has the same power as the $f_{IF} + f_{RF}$ tone, the band-pass filter of the second stage of conversion has to reject the signal of 40dB at least [8]. As this filter has to work at high frequency, it becomes complicated to obtain a good quality factor. In general, an external filter is used as a SAW filter (Surface Acoustic Wave). This filter adds area and cost, making this kind of architecture very expensive.

1.2.2 Direct conversion transmitter architecture

The direct conversion transmitter architecture, also called homodyne or Zero-IF (Zero-Intermediate Frequency, meaning without intermediate frequency), uses a single-stage of frequency conversion as shown in Figure 1.2.

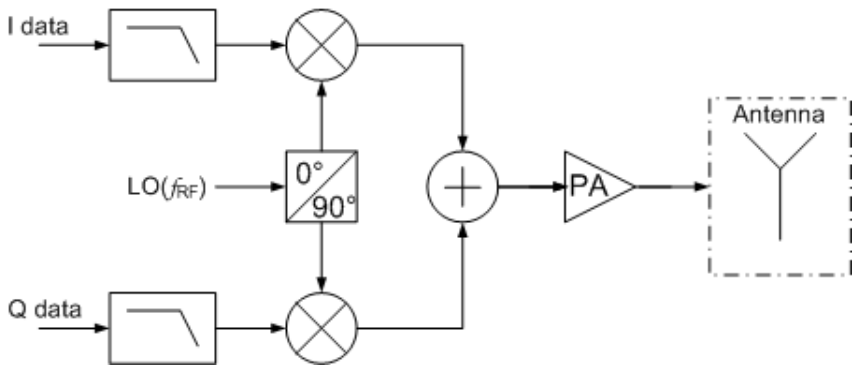


Figure 1.2: Direct conversion transmitter architecture

Like the heterodyne architecture, analog baseband signals are modulated and up-converted to RF frequency by mixers on quadrature, a PLL with a LO working at the RF frequency. In this case, the frequency of the resulting signal is directly transposed to the frequency of the standard.

This architecture takes less area than the heterodyne architecture because it uses fewer components reducing thereby the consumption. Moreover, the image rejection on the main channel is realized dynamically by summing the output of mixers (Cf. equation 1.1).

$$\begin{aligned}(\cos\omega_{BB}t * \cos\omega_{RF}t) + (\sin\omega_{BB}t * \sin\omega_{RF}t) &= \frac{1}{2}\left[\cos\left(\omega_{RF}t + \omega_{BB}t\right) + \cos\left(\omega_{RF}t - \omega_{BB}t\right)\right] \\ &+ \frac{1}{2}\left[\cos\left(\omega_{RF}t - \omega_{BB}t\right) - \cos\left(\omega_{RF}t + \omega_{BB}t\right)\right] \\ &= \cos(\omega_{RF}t - \omega_{BB}t) \qquad (1.1)\end{aligned}$$

As a consequence, we do not need the band-pass filter of the intermediate stage and release some constraints of the external filter.

Such architecture is compatible with a complex I/Q modulation as HPSK, but has some drawbacks concerning the mismatch in phase and amplitude between I and Q. The major issue is to realize a good quadrature generation at the RF frequency. If a weak quadrature occurs, we will have a bad rejection of the image frequency [9].

One of the major drawbacks for the direct conversion transmitter is the pulling phenomenon [10] [11]. In other words, when two oscillating components are close to each other, they are oscillating at the same frequency due to the coupling phenomena. In the case of the Zero-IF frequency, the local oscillator and the PA work at frequencies very close to each other and can be coupled by the substrate. The RF signal at the output of the power amplifier is much greater than the output power of the LO, therefore the working frequency of the LO will be shifted into the RF frequency. The isolation needed remains hard to quantify without considering the receiver associated with the Zero-IF transmitter [12].

Moreover, the direct conversion is sensitive to DC parasites. Indeed, parasites are mixed with the main signal for the receiver. In W-CDMA the baseband signal is spread around 3.84MHz. A high-pass filter with a cut-off frequency lower or equal to 10 kHz removes all of these DC parasites keeping the integrity of the W-CDMA signal.

1.2.3 Low-IF transmitter architecture

The pulling phenomenon disappears if we use two LO frequencies (frequencies of $LO_{\omega 1}$ and $LO_{\omega 2}$). Figure 1.3 shows the architecture of the low-IF frequency.

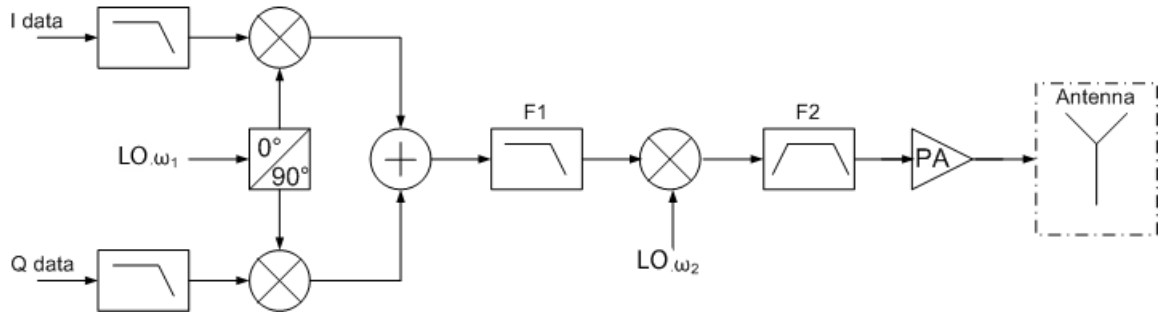


Figure 1.3: Low-IF transmitter architecture

The low-IF transmitter architecture is based on the same principle of a heterodyne transmitter, except that the LO_{ω_1} frequency is obtained by mixing and filtering two lower frequencies. As a consequence, the first mixing stage in the IF frequency can be realized in the digital domain. This method has the same advantages as the direct conversion transmitter, except that this transmitter is not sensitive for the pulling if the IF frequency is not too low.

Furthermore, an incorrect choice of LO frequencies produces harmonics at the output. A low-pass filter which follows the VCO (Voltage-Controlled Oscillator) has to be very selective in order to keep a good quality of the output signal.

1.2.4 Offset-PLL transmitter architecture

This architecture was developed to answer the strong constraints of the GSM standard for the noise in the reception band. The Offset-PLL transmitter architecture [7] is presented in Figure 1.4.

The offset-PLL transmitter [13] has the objective to mix the signal from the local oscillator with the output signal from the VCO (Voltage Control Oscillator). The resulting signal is then injected into a phase comparator to generate an error signal which, after being filtered, controls the VCO. This will work at the RF frequency. A current offset generator is needed to obtain a fast lock of the loop. Indeed, the output current of the phase comparator does not allow to lock the loop in a reasonable time. The time-locked can be improved by 26% [14]. Nonetheless, without adjustment of the current, the loop will become unstable.

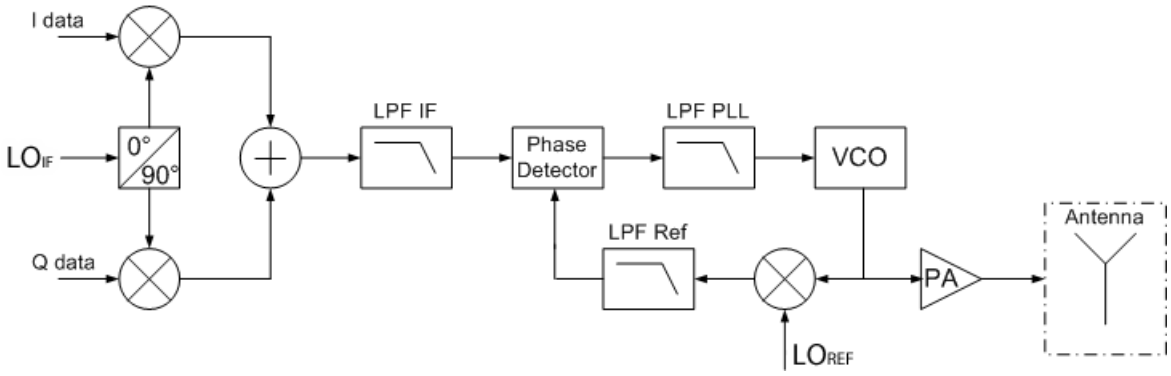


Figure 1.4: Offset-PLL transmitter architecture

The offset-PLL transmitter has a good IC integration because it does not use mixers to convert the baseband frequency to the RF frequency, neither external filter. Moreover, it does not consume a lot of power, which makes a very attractive solution for the cost reduction. On the other side, this solution works with constant envelope modulation and does not fit with our modulation which is the HPSK. This architecture also has the drawback of suffering from the pulling, thus a good isolation between the VCO and the PA has to be realized.

1.2.5 Summary of transmitter architectures

For the wireless communication in the context of mobile devices with the W-CDMA standard, it is very important to get a good integration level on the silicon area and a low consumption of our chip, as both reduce the cost of production. Furthermore, the architecture has to work with constant and non-constant envelope modulations considering the W-CDMA standard. Table 1.2 makes a comparison of transmitters previously studied according to these criteria.

Architecture	Integration	Consumption	Modulation
Heterodyne	Low	Medium	All
Homodyne	Good	Low	All
Low-IF	Medium	Medium	All
Offset-PLL	Good	Low	Constant envelope

Table 1.2: Comparison of transmitter architectures

Despite serious issues imposed by the Zero-IF architecture explained at the topic 1.2.2 and according to the previous table, this transmitter is the most appropriated to reduce consumption

and die area for W-CDMA communications. These criteria remain our first objective and it is for this reason that the Cartesian Feedback has been implemented on a Zero-IF transmitter.

1.3 Nonlinear Behavior of a RF Transmitter

To understand an RF transmitter, we must have the previous knowledge that it is composed of RF transistors.

In 1948[15], W. Shockley describes for the first time the principle of the bipolar junction transistor. However, it is only at the end of the 1950s that the first transistor able to amplify signals up to 1GHz was developed.

The term Radio Frequency (RF) refers to the electromagnetic waves with frequencies ranging from Gigahertz or higher. Until the 1980s, most applications for RF transistors were used only by the military. Since then, the appearance of wireless communication systems (Wi-Fi, Bluetooth and WLAN) for the costumers has completely changed the sales for mobile phones.

The conception of RF transmitters starts with the choice of the type of transistor depending of the targeted application. For our study, which is to improve the linearity of the transmitter, we opted for the characterization of a transmitter (e.g. power amplifier), using nonlinear model of transistor. This part shows the nonlinear behavior of a transistor (or component using transistors) and the metrics to measure it.

Furthermore, every RF transmitter architecture can be evaluated according to its integration on the silicon area, as well as the power consumption or the modulation used. Therefore, in order to validate the RF transmitter some requirements are given by the standard communication.

1.3.1 AM/AM and AM/PM conversion

The power amplifier is a very important component of a transmitter and defines the consumption and the linearity of the whole system. The behavior of the PA acts also directly on the receiver and can increase the bit error rate (BER) of the transceiver.

An ideal power amplifier has a linear response. In other words, the output signal is proportional to the input signal.

$$V_{out}(t) = a_0 + a_1.V_{in}(t) \tag{1.2}$$

Where a_1 is the voltage gain of the power amplifier.

For a low input voltage, the behavior of the power amplifier can be assimilated to an ideal power amplifier. However, for strong input voltage, the output signal suffers from distortions due to amplitude (AM/AM) and phase (AM/PM) conversions. Current sources are the first elements able to cause amplitude variation of the output signal according to the input signal. Moreover, nonlinear behavior gives an additional shifting of the output signal, which is also linked with the input signal from the power amplifier.

Figure 1.5 shows these conversions:

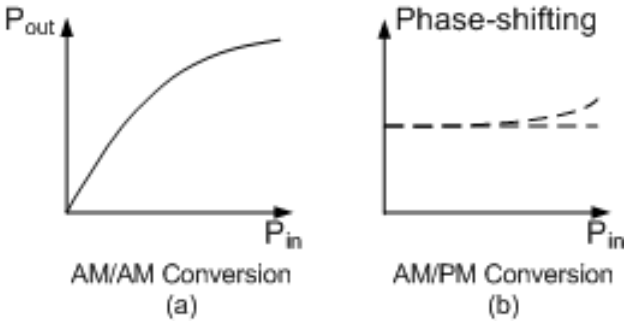


Figure 1.5: AM/AM and AM/PM conversion

Let's consider an input sinusoidal signal with an amplitude and phase modulation

$$V_{in} = A(t) . \cos[\omega_0.t + \phi(t)] \tag{1.3}$$

At the output of the power amplifier, we obtained

$$V_{out} = A^{'}(t) . \cos\left[\omega_0.t + \phi(t) + \phi^{'}(t)\right] \tag{1.4}$$

With

$$A^{'}(t) = F_{NL}[A(t)] \tag{1.5}$$

And

$$\phi^{'}(t) = G_{NL}[A(t)] \tag{1.6}$$

Where F_{NL} and G_{NL} are nonlinear functions.

The deflection of AM/AM and AM/PM curves, for strong input level power, explains the nonlinear behavior of the power amplifier.

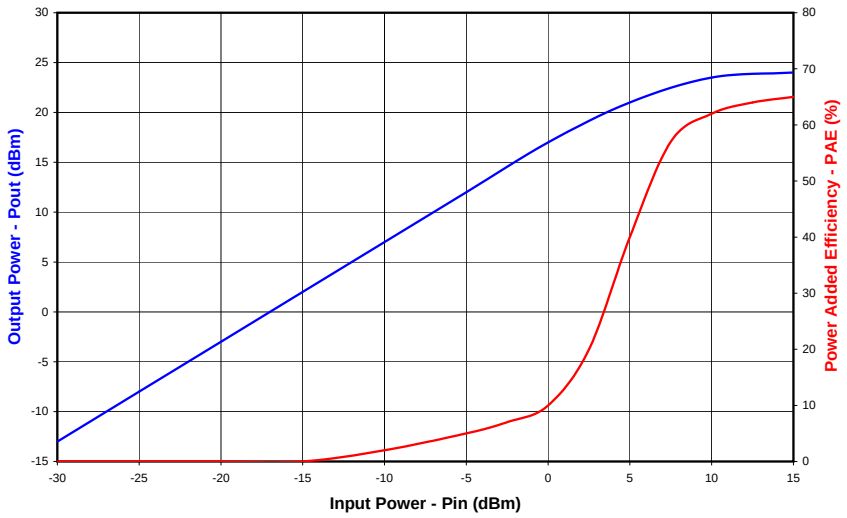


Figure 1.6: Output power and efficiency of a PA versus input power

However the efficiency η is defined as the ratio between the output power (in Watts) and the power supply consumed (in Watts). It will be maximal when the amplifier is used with high level signal (Cf. Figure 1.6). Thus, a nonlinear function and generation of spurious tones are produced when we will try to improve the saturation power or the efficiency of the power amplifier.

1.3.2 Carrier-to-Intermodulation ratio (C/In)

The analysis with two carriers is a simple method to evaluate the linearity of an amplifier and to show, at the same time, amplitude and phase distortions of the amplifier. This method focuses on the variation of the envelope's signal, using the amplifier over its entire dynamic range. It is a very severe test for the amplifier because the envelope ranges from zero to a maximum level, as shown in Figure 1.7(a).

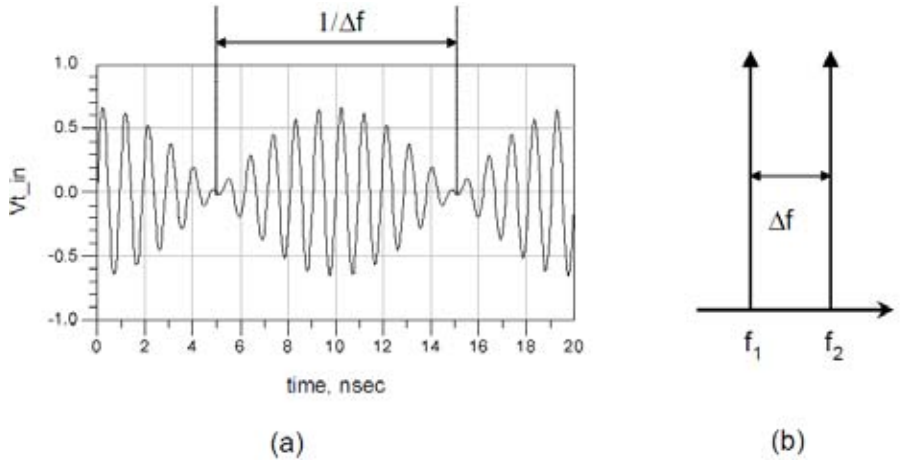


Figure 1.7: Signal with two carriers in time (a) and frequency (b) domains

Two signals at the frequency f_1 and f_2, with the same amplitude and non-modulated with $\Delta f = f_2 - f_1$, are applied at the input of the amplifier. On the time-domain, a signal with two carriers is represented in Figure 1.7 (a). The equivalent spectrum is given in Figure 1.7 (b).

As shown in the previous part, such signal going through the nonlinear amplifier generates intermodulation products.

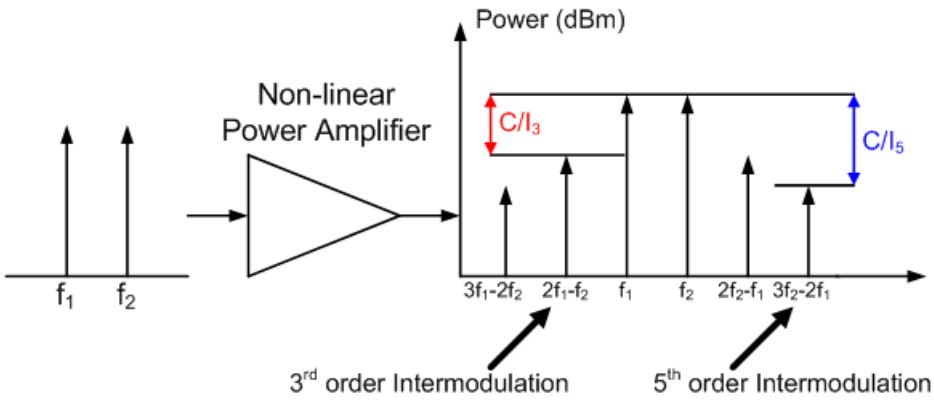


Figure 1.8: Carrier-to-Intermodulation ratio

The third-order ratio C/I (Carrier-to-Intermodulation ratio) is defined as being the difference between the power in dBm, of the carrier f_1 or f_2, and the intermodulation tone respectively at $2.f_1 - f_2$ or $2.f_2 - f_1$ frequency (Cf. Figure 1.8). In general, we define the n^{th} order ratio C/I as the difference between the power of the carrier f_1 or f_2 and the intermodulation tone at $p.f_1 + q.f_2$ with $p + q = n$.

1.3.3 Adjacent Channel Leakage Ratio (ACLR)

The ACLR measures the power level at the output of the power amplifier, between the adjacent channel and the main channel. It uses a modulated signal of the same type as the one that must be amplified for standard chosen. It is defined as the ratio between the average powers (in Watts) contained in a frequency band B_1 and B_2 to an offset f_0 of the carrier frequency f_c of the channel, and the average power (in Watts) contained in the frequency band B_0 around the carrier frequency f_c of the standard.

The concept of this measure is shown in Figure 1.9. It leads to the following expression:

$$ACLR_{dB} = \left(\frac{2. \int_{B_0} P(f) .df}{\int_{B_1} P(f) .df + \int_{B_2} P(f) .df} \right) \tag{1.7}$$

The output power according to the frequency is shown in Figure 1.9.

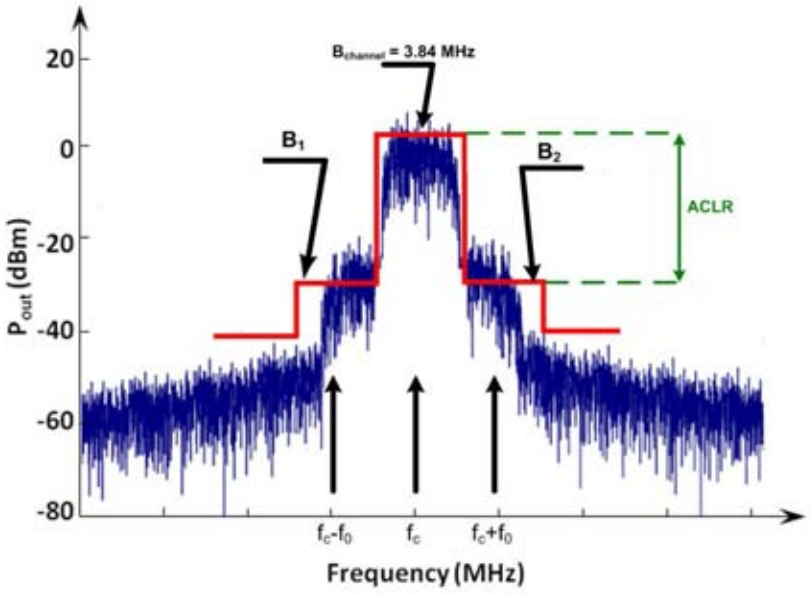


Figure 1.9: Adjacent Channel Power Ratio spectrum

Frequency bands B_0, B_1 and B_2 and the offset f_0 depend on the chosen standard of communication.

1.3.4 Noise Power Ratio (NPR)

The NPR is a power measurement of distortions on the channel caused by nonlinearities of the power amplifier. It can be evaluated by removing a frequency band of the input signal of the

channel, and measuring the output level of distortion in the frequency space left free. It is defined as the ratio between the maximum power of the signal on the channel and the power of distortions, where both are expressed in Watts.

$$NPR\,(dB) = 10 * \log\left(\frac{\int_{SLF} P\,(f)\,.df}{\int_{Carriers} P\,(f)\,.df}.\frac{BW_{Carriers}}{BW_{SLF}}\right) \tag{1.8}$$

Figure 1.10 illustrates the spectrum of the NPR on the modulated signal after the power amplifier.

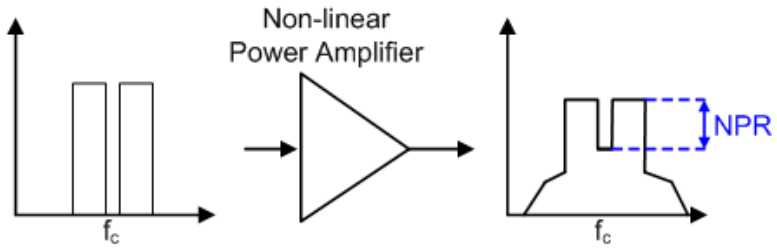


Figure 1.10: Noise Power Ratio

1.3.5 Error Vector Magnitude (EVM)

The EVM represents the difference between the effective demodulated signal after the transmission or amplification, and the signal as it should be if the system was perfectly linear. This measurement gives the information about the error of the phase and amplitude of the received signal [16]. Figure 1.11 represents the EVM definition for a modulated signal by two signals in quadrature I and Q.

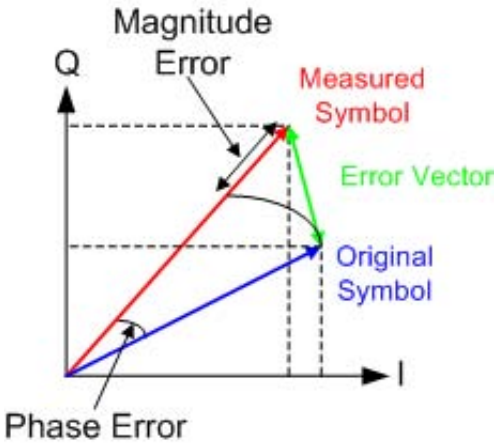


Figure 1.11: Error Vector Magnitude

The EVM represents the module of the error vector as followed:

$$Magnitude\ Error = \sqrt{I_{Measured}^2 + Q_{Measured}^2} - \sqrt{I_{Original}^2 + Q_{Original}^2} \quad (1.9)$$

$$Phase\ Error = \arctan\left(\frac{Q_{measured}}{I_{Measured}}\right) - \arctan\left(\frac{Q_{Original}}{I_{Original}}\right) \quad (1.10)$$

$$EVM = \sqrt{(I_{Measured} - I_{Original})^2 + (Q_{Measured} - Q_{Original})^2} \quad (1.11)$$

This criterion is generally used for signal processing to characterize the whole system of a couple modulator/demodulator. It helps to quantify the effect of the additive noise on the distortion of the transmitted signal's constellation.

1.4 Linearization Techniques

The HPSK modulation has a good spectral efficiency, but the power efficiency remains poor with linear power amplifiers. For mobile applications, a low efficiency increases the consumption of the transmitter, decreasing the lifetime of mobile phone battery.

To obtain, for the same device, a good linearity and spectral efficiency, we use linearization techniques such as EER (Envelope Elimination Restoration), Feedforward, Polar loop or Cartesian Feedback. On the other hand, a good linearity for components like an RF modulator or a power amplifier can be obtained with overconsumption. A linearization technique offers the possibility to use nonlinear components in order to reduce the consumption of the transmitter.

We have two categories of linearization techniques: those which improve the linearity of the transmitter and those which improve the efficiency of the whole system.

1.4.1 Tradeoffs between linearity and efficiency in power amplifier design

The challenge for the design of a power amplifier can be simplified by a system of two variables, in which we have to reach an output power imposed by the wireless communication standard while optimizing its efficiency. This must be done with respect to the given linearity constraints. Nevertheless, a compromise has to be made between the maximum output power and the efficiency of the power amplifier. According to specification given by the standard, we must distinguish among many topologies of power amplifiers.

1.4.1.1 Classes of power amplifier

In literature, classes of power amplifiers can be divided into two categories [17]:
- The first class is defined by the biasing given to the transistor and is called the “linear class”. They are designated by: Classes A, B, C, and AB.
- The other class is the commutation class because transistors work like switches. It is called the “highly efficient class”. They are designated by: Classes D, E, F and S.

Linear class of power amplifier:

For power amplifiers taken from the linear class, the transistor behavior can be assimilated as a current source. The output power is proportional to the input power. The gain is constant on a wide-band of power. This kind of class is well known and is required when a complex modulation is used (non-constant envelope, e.g. HPSK) in order to preserve the information contained into the envelope.

Commutation class of power amplifier:

For power amplifiers of the commutation class, the transistor works like a switch with the output non-proportional to the input. This kind of power amplifier is really efficient for constant envelope modulation (like GMSK used for the GSM standard). The consumption of the circuit is considerably reduced and the efficiency remains very high. Indeed, in theory, when the level of the input voltage of the transistor is high, the current is equal to zero and reciprocally. This advantage increases the time-to-talk of batteries implanted into a mobile device.

Important parameters able to define performance of a power amplifier are the efficiency and the nonlinearities. The values of these parameters are linked to the classes of the chosen power amplifier. Moreover, it is important to define their characteristics to understand how to correct or improve them.

1.4.1.2 Efficiency

The efficiency of a power amplifier can be evaluated as a drain efficiency (if the transistor is a field-effect transistor, otherwise, it is a collector efficiency for a bipolar junction transistor), a power added efficiency (PAE), or a whole efficiency.
The drain efficiency is defined as the ratio between the fundamental output power (P_{out}, W) and the power delivered by the continuous alimentation (P_{DC}, W).

$$\eta_{DE} = \frac{P_{out}}{P_{DC}} \tag{1.12}$$

The power added efficiency of a power amplifier is defined by equation 1.13. It represents the ability of a transistor to transform the energy delivered by continuous alimentation in a microwave energy. This efficiency can be calculated as the ratio between the added sine wave power of the power amplifier and the supply voltage applied to it. The added sine wave power is defined as the difference between the output power (P_{out}, W) and the input power (P_{in}, W) of the power amplifier.

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{1.13}$$

Finally, the whole efficiency represents the ratio between the energy available at the output of the power amplifier and the energy provided to the amplifier in order to insure the output power.

This efficiency is defined by equation:

$$\eta = \frac{P_{out}}{P_{DC} + P_{in}} \tag{1.14}$$

1.4.1.3 Nonlinearity

Power amplifiers suffer from nonlinearities, or distortions, when a certain level of the input signal is applied.

The amplitude distortions are divided in two categories:

– distortions making a compression effect on the power of the signal (compression point at 1dB); and

– distortions due to interferences between two signals which have frequencies close to the fundamental frequency.

The combination of the different frequencies creates intermodulation products. Distortions due to interferences have impacts only on the receiver. These two types of nonlinearity are described in the following section.

Compression Point at 1dB:

The sinusoidal signal at the input of the power amplifier is defined by equation 1.15

$$V_{in} = A.\cos(\omega t) \tag{1.15}$$

Where A is the maximum amplitude of the input signal and ω is the operating frequency.

Considering the output voltage as a temporal function of the input voltage, it is possible to express this voltage in polynomial form until the third-order nonlinearities term. The expression of the output voltage is:

$$V_{out} = a_1 V_{in} + a_2 V_{in}^2 + a_3 V_{in}^3 \tag{1.16}$$

After the development of equation 1.16, the expression of the amplitude at the fundamental will be:

$$a_1 A \left[1 + \frac{3}{4}\frac{a_3}{a_1} A^2\right]$$

The coefficient $a_1 A$ represents the linear gain of the system. If $a_3 > 0$, the power amplifier works on the linear region, but if $a_3 < 0$, the power amplifier suffers of the compression phenomenon at the fundamental frequency. The output power of the amplifier is often given at 1dB of compression, meaning that the gain is 1dB under the linear zone. The compression point is described in Figure 1.12.

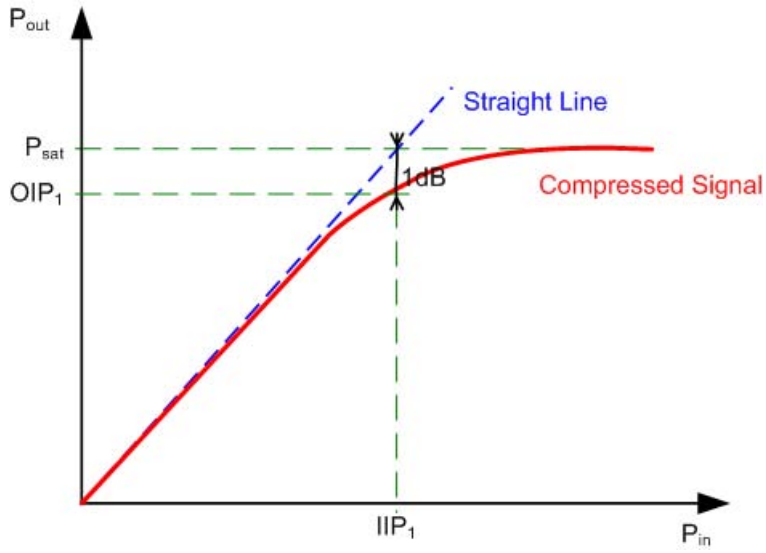


Figure 1.12: Definition of the compression point

Where OIP1 is the 1dB Output Intermodulation Point and IIP1 is the 1dB Input Intermodulation Point.

Evaluating the 1dB compression point (CP1) is not enough to quantify the nonlinearity of a power amplifier used on a communication system. For this reason, we must also study the intermodulation products in order to evaluate distortions of the same function. The knowledge of the 1dB compression point is important to determine the back-off level to take into account when complex modulation is brought into play (as the OFDM modulation).

Intermodulation products:

Intermodulation products represent a combination of fundamental frequencies. Spurious signals can disturb the wireless communication system if they are within the bandwidth of the system.

In order to characterize intermodulation products, we must consider the input signal (V_{in}) - Cf. equation 1.17 - composed of two sinusoidal signals with the same amplitude A but with different frequencies (f_1 and f_2).

$$V_{in} = V\left[\cos\left(\omega_1 t\right) + \cos\left(\omega_2 t\right)\right] \tag{1.17}$$

The output signal of the power amplifier is then defined in equation 1.18.

$$\begin{aligned} V_{out} &= a_1 V\left[\cos\left(\omega_1 t\right) + \cos\left(\omega_2 t\right)\right] + a_2 V^2\left[\cos\left(\omega_1 t\right) + \cos\left(\omega_2 t\right)\right]^2 \\ &+ a_3 V^3\left[\cos\left(\omega_1 t\right) + \cos\left(\omega_2 t\right)\right]^3 \end{aligned} \tag{1.18}$$

The output signal V_{out} can be decomposed as $n\omega_1 \pm m\omega_2$, n and m being integers. The order of the intermodulation products is defined by the relation:

$$i = |n| + |m| \tag{1.19}$$

Second-order intermodulation products are thus represented by tones at frequencies $f_1 + f_2$ and $f_2 - f_1$, and those of the third-order by frequencies $2f_1 + f_2$, $2f_1 - f_2$, $2f_2 + f_1$, and $2f_2 - f_1$.

Some of intermodulation products with an odd order (i being an odd number) perturbed the transmitted signal.

The third-order intermodulation product is represented in Figure 1.13.

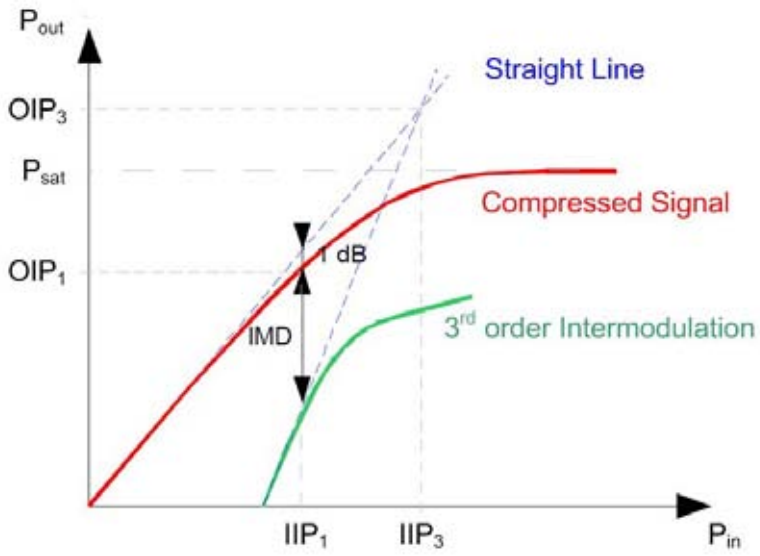


Figure 1.13: Definition of the third-order intermodulation point

In this graphic, we can deduce the third-order intermodulation point ($IP3$) at the input ($IIP3$) and at the output ($OIP3$). This point can be determined by calculating the intersection between the linear line of the fundamental power and the line of the third-order intermodulation products.

Figure 1.13 represents also intermodulation products, called IMD (InterModulation Distortions) and is expressed in dBc. This distortion is defined by equation 1.20 knowing that the power of the fundamental is defined at the 1dB compression point:

$$IMD_3 = P_{2f_2-f_1} - P_{f_1}(dBc) \tag{1.20}$$

The process is similar to determine i^{th} order intermodulation distortions. This time, it can be calculated by equation 1.21.

$$IMD_i = P_{mf2-nf1} - P_{f_1} \tag{1.21}$$

Where m, n, and i are integers numbers and linked by this expression: $i = m + n$.

Moreover from Figure 1.13 and [18], the IMD3 can be determined from equation 1.22, where P_{in} is the input power of the power amplifier at the fundamental frequency (f_1 or f_2):

$$IMD_3 = 3.P_{in} - 2.IIP3 \tag{1.22}$$

Third and fifth intermodulation products are, in most cases, within the bandwidth of the system and have sufficient power in order to have an influence on the output signal of the power amplifier.

The knowledge of the third and fifth intermodulation products is valuable for communication system using a complex modulation, as the HPSK for the UMTS Standard.

1.4.2 Power back-off

The easiest way to improve the linearity of a power amplifier is to use it in a Class A operation, reducing the power level needed by the amplifier (back-off) until that the desired level of linearity is reached. For a Class A power amplifier, third-order intermodulation products increases according to a factor 3 (Cf. Figure 1.13) , and those of fifth-order by a factor 5. A back-off of the input power can significantly reduce the intermodulation products, and especially if these intermodulation products have a high order.

An alternative of using a Class A power amplifier is employing a Class AB power amplifier, where the biasing level is usually between 10 and 50% of the Class A level. The linearity in this case depends largely on the characteristics of the RF component technology. Some technologies, such as the LDMOS, have also very good linearity performance for a Class AB [19].

The drawback of these very simple methods is the low efficiency and the need to have a power amplifier oversized for the application. Therefore, other methods are applied to increase the linearity without deteriorate the whole efficiency of the system.

1.4.3 Efficiency improvement

1.4.3.1 Envelope Tracking (ET)

Envelope tracking has an objective to keep the linearity of the power amplifier, and at the same time, increase the efficiency. The principle of this topology is to modify the biasing according to the envelope of the input signal. The envelope tracking system imposes the envelope signal at the drain of the power amplifier, and the PA is consequently working in a high efficiency region.

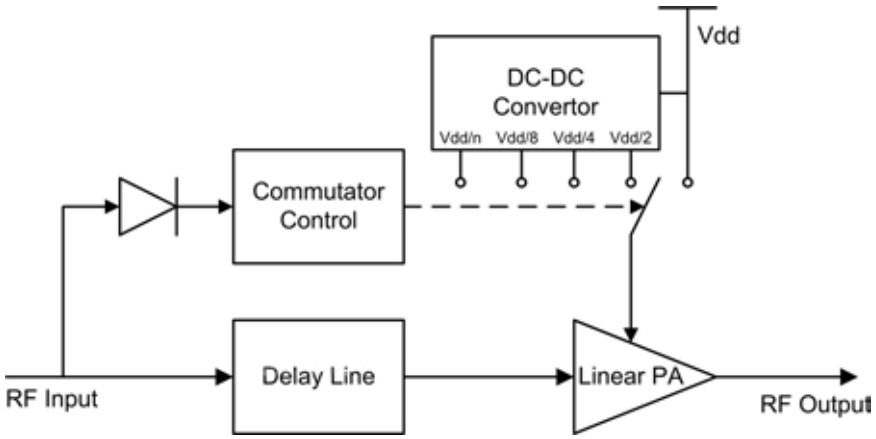


Figure 1.14: Discrete Envelope Tracking

The control of the biasing can be seen as a discrete (Cf. Figure 1.14) or a continuous (Cf. Figure 1.15) DC-DC converter. In the first case when the envelope of the signal is greater or lower than a certain value, the bias voltage can take a value previously fixed. In the other case, the ET works on the biasing, which makes a continuous adjustment of the amplitude according to the envelope signal in real-time.

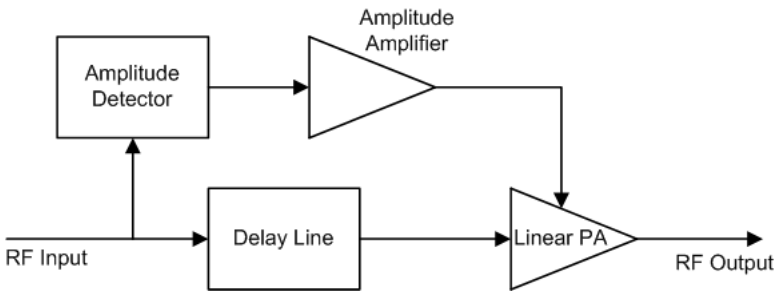


Figure 1.15: Continuous Envelope Tracking

The efficiency reached by the discrete or continuous ET is greater than the efficiency of a power amplifier with a fixed biasing. The current consumption of DC-DC converter and others control components reduce performance in the case of low signal envelope. It is a discrete control, easier to implement and taking less area than a converter can be used, but it does not reach an improvement like continuous correction. Moreover, the generation of different DC signals remains complex for an integrated solution. Nevertheless, dynamic biasing offers full use of the linearity performance of a Class A, while improving significantly the maximum efficiency, which is an attractive solution.

1.4.3.2 Envelope Elimination and Restoration (EER)

The Envelope Elimination and Restoration (EER) in Figure 1.16 has been developed by Leonard E. Khan in 1952 [20]. The goal of this technique is to amplify a non-constant envelope modulation with a nonlinear power amplifier. The input modulated signal at an intermediate frequency (IF) is decomposed in phase and amplitude through an envelope detector and a limiter. The constant envelope signal in amplitude is up-converted to the RF frequency in the mixer. The resulting signal is then amplified by the nonlinear power amplifier in saturation mode. The envelope of the signal is sent back modulating the voltage supply of the PA by the phase of the input signal.

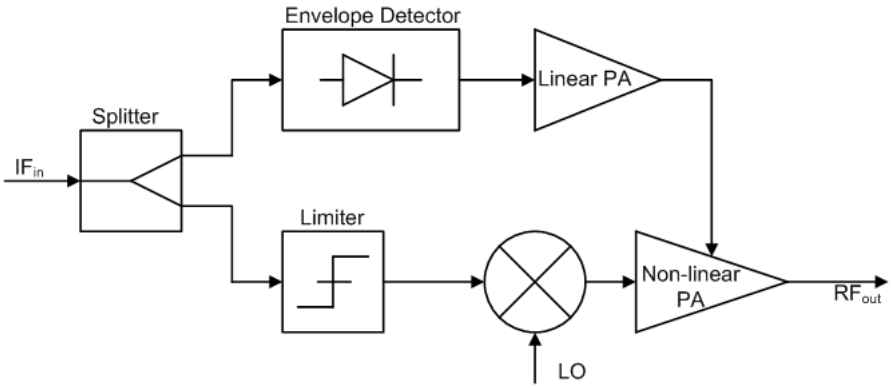


Figure 1.16: Envelope Elimination and Restoration

The advantage of the EER is to improve the linearity and the efficiency of the power amplifier. This technique remains a complex solution to implement for two reasons. First, it requires controlling perfectly the envelope power amplifier linearity. Secondly, the phase alignment between envelope and phase signals has to be guaranteed. Linearization performance of the EER is linked to the bandwidth of the envelope, but also the phase-shifting between the envelope modulation and the phase modulation. It is therefore crucial to control the variation of delay in both paths of the architecture, as well in temperature and for the process used for a good recombination of the output signal. In recent application of the EER [21], the DSP (Digital Signal Processor) splits the signal in phase and amplitude. This solution does not fit with the criteria of a system integrated on a single technology without using external devices.

1.4.3.3 LInear amplification with Nonlinear Components(LINC) / Combined Analog Locked-Loop Universal Modulator (CALLUM)

This technique uses the property of the decomposition of a non-constant envelope signal into two constant envelope signals, thereby splitting the input signal into two distinct parts. Each of these parts is separately amplified on the nonlinear region and they permit to get a high efficiency and a high output power before a recombination at the output (Cf. Figure 1.17(b)) [22, 23].

The LINC technique may use a DSP to generate two baseband signals modulated in phase and with constant envelope amplitude (Cf. Figure 1.17(a))

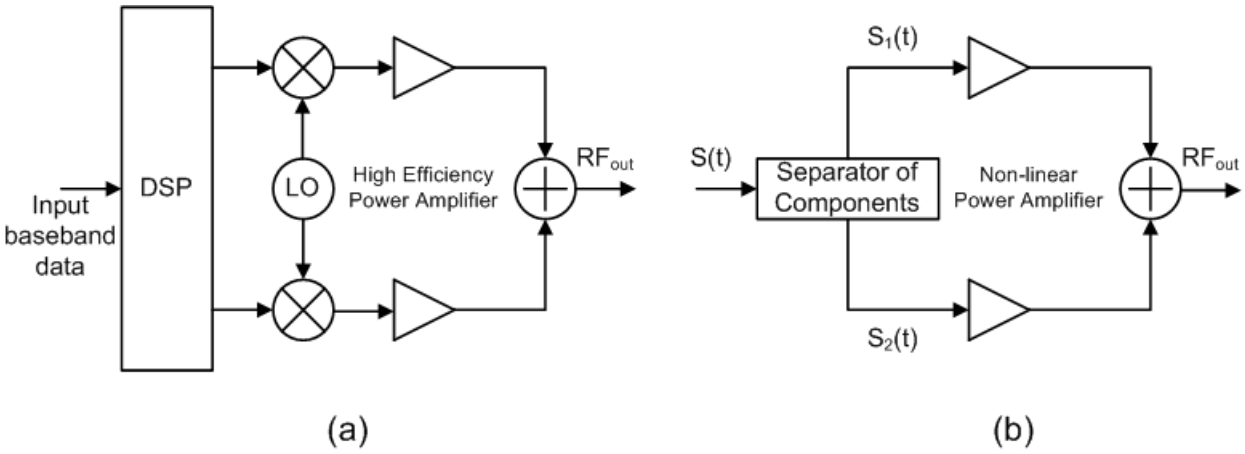


Figure 1.17: Principle of LINC technique

Thus an input signal $s(t) = a(t)\cos[2.\pi.f_c.t + \phi(t)]$

This signal can be described by two signals $s_1(t)$ and $s_2(t)$ with a constant amplitude such as:

$$s_1(t) = a_{max}.\cos[2.\pi.f_c.t + \phi(t) + \alpha(t)] \tag{1.23}$$

And

$$s_2(t) = a_{max}.\cos[2.\pi.f_c.t + \phi(t) - \alpha(t)] \tag{1.24}$$

With

$$2.s(t) = s_1(t) + s_2(t) \tag{1.25}$$

And

$$\alpha(t) = \cos^{-1}\left(\frac{a(t)}{a_{max}}\right) \tag{1.26}$$

These two signals are separately amplified by high efficiency power amplifiers, and then recombined to make an amplified copy of the input signal. Any nonlinear behavior appearing in the signal will be found in phase opposition and equal amplitude before the summation. Every nonlinear part will be canceled after summing. This method can use amplifiers in high efficiency commutation to approach an efficiency of 100%.

The two most important difficulties of this method are: to adjust both paths in phase and amplitude in order to obtain the elimination of any intermodulation; and to work with identical power amplifiers [24, 25, 26].

The CALLUM is a feedback technique with the objective to cancel problems in phase and gain of the LINC [27].

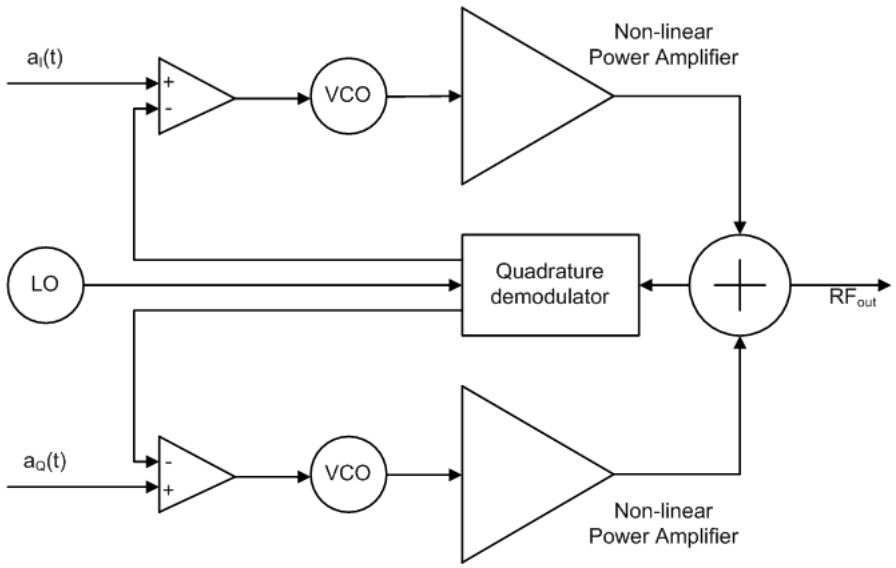


Figure 1.18: CALLUM technique

A Cartesian decomposition on the feedback path is used with the CALLUM method. The output signal is demodulated into two quadrature signals. These signals are compared in baseband domain with the two input signals and used to generate error signals. The main issue of this method is the stability of the system. For this reason, this method can be used only for straight bandwidth modulation.

1.4.3.4 Doherty technique

Performance of the power amplifier is mainly determined by the load impedance at the output of the transistor [28]. The Doherty technique allows the load impedance to be modified according to the input power thanks to the combination of two power amplifiers: a main and an auxiliary; and also with two lines λ/4 which Z_C and Z_{Cin} represent the impedance of these lines (Cf. Figure 1.19).

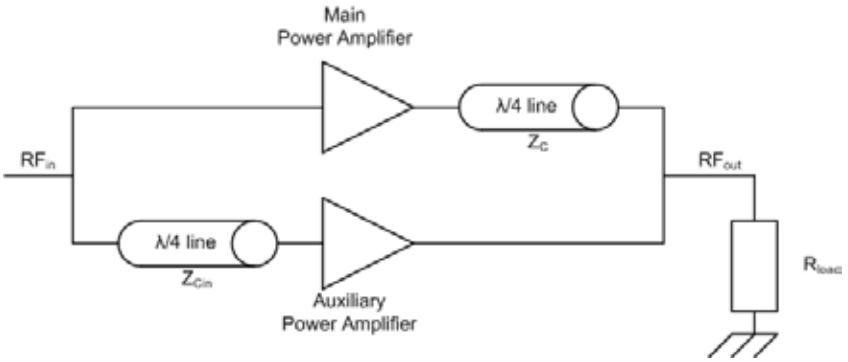


Figure 1.19: Doherty technique

The λ/4 line placed at the output of the main power amplifier realizes the impedance transformation needed to maintain the efficiency over an important variation of the output power. This line will, however, add a phase shift of 90°.

The second λ/4 line allows compensation of this phase shift between signals from power amplifiers. Thereby, the in-phase recombination of the output signal is possible.

The Doherty technique works as follows:
- For low input power, only the main power amplifier delivers an output signal. The auxiliary power amplifier is turned off.
- For an intermediate power level, the auxiliary power amplifier begins to deliver output power, while the main power amplifier starts to saturate. The fact that the auxiliary power amplifier is turned-on leads to the modification of the load impedance presented by the main amplifier.
- For strong power level, both amplifiers are saturated.

Assuming the same size of the two power amplifiers and the characteristic impedance of the λ/4 line $Z_C = 2.R_{load}$, load impedances of power amplifiers will vary according to the input power as follows:

- For a low power level, the auxiliary power amplifier is clamped. As a result, its drain current is then equal to zero. In this case, the impedance at the output of the main power amplifier is equal to $4.R_{load}$, and the one that is seen at the auxiliary is equal to an open circuit.
- For a high power level, both power amplifiers are saturated and its drain currents are equal. Both amplifiers will have the same load impedance equal to $2.R_{load}$.

The transition power P_α is the output power from which the auxiliary amplifier begins to operate. Table 1.3 summarizes the Doherty amplifier principle:

Power level	Main power amplifier mode	Auxiliary power amplifier Mode
Power $< P_\alpha$	Current sources controlled	Turned off
$P_\alpha <$ Power $< P_{Max}$	Saturated	Current sources controlled
Power $= P_{Max}$	Saturated	Saturated

Table 1.3: Doherty amplifier principle

Figure 1.20 represents the evolution of the efficiency, in case where the main and the auxiliary power amplifiers have the same size, versus the ratio between the load voltage and the supply voltage (Vload/Vdd).

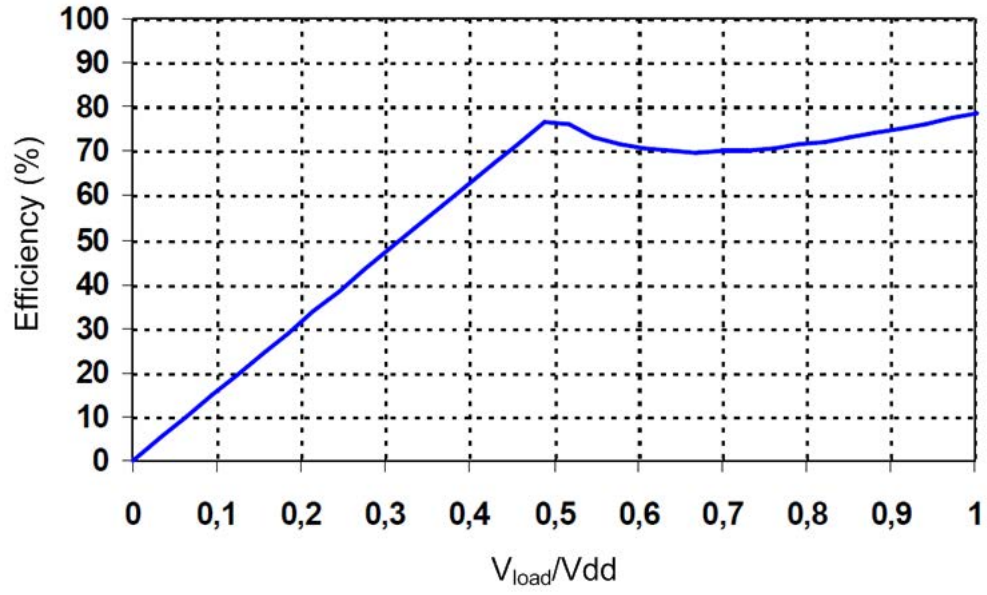


Figure 1.20: Evolution of the efficiency for a two-stages Doherty amplifier

The efficiency is evolving linearly to the point corresponding to the transition power P_α. Then, it decreases when the auxiliary power amplifier starts to operate. After that, it increases again until it reaches the maximum efficiency at the maximum power.

The size of the auxiliary power amplifier depends on the curve variation of the efficiency according to the power level. It imposes different shapes and moves the transition point. The choice of this stage size is related to the application and the shape of the signal to amplify.

This technique can also be realized with several auxiliary power amplifiers. As a consequence, different levels of transition can be obtained, being able to achieve and to maintain a strong efficiency over a wide dynamic output power [29].

The operation class of the auxiliary power amplifier has a strong influence on the power added efficiency of the whole amplifier [29]. An adjustment of the biasing of the auxiliary amplifier is then needed for every output power. A possible solution is to use a variation of the auxiliary power amplifier according to the power level available at the input of the amplifier [30].

1.4.4 Linearity improvement

1.4.4.1 Predistortion / Postdistortion

Predistortion technique deals with the RF signal before the power amplifier (Cf. Figure 1.21), and inversely to the postdistortion technique, which deals with the signal after the power amplifier. They can be used for wideband systems and for multi-carriers as amplifiers used for satellite communication.

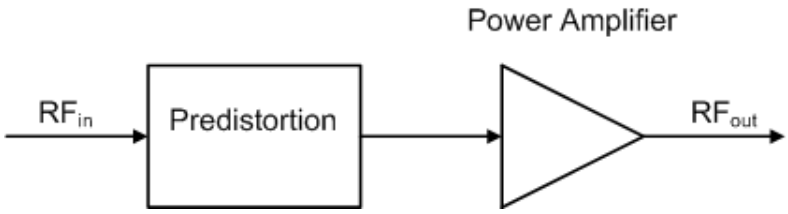


Figure 1.21: Predistortion technique

This approach involves the creation of a complementary function of distortion according to those of the power amplifier. The resulting system from the serialization of the predistortion (or postdistortion) will present few or no distortion at the output.

In the ideal case, the predistortion component generates a distorted signal which is the opposite of those created by the power amplifier (Cf. Figure 1.22). When this generator and the amplifier are cascaded together, distortion is cancelled [31].

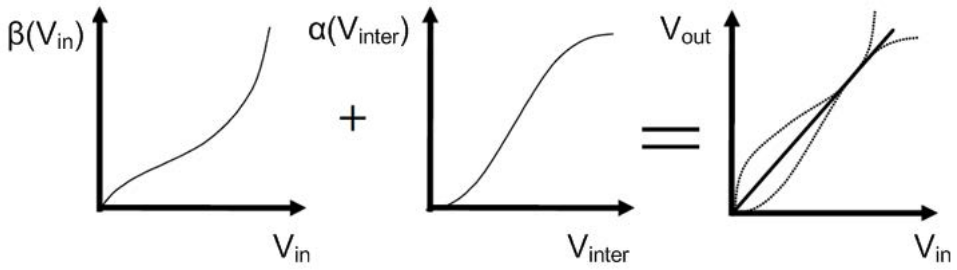


Figure 1.22: Signal before and after predistortion technique

The difficulty of this technique is the realization of a circuit able to provide a precise inverse distortion in phase and amplitude of the distortions given by the power amplifier. Meanwhile, due to the relative simplicity of its implementation, this technique is interesting for power amplifiers used for mobile system when the size, the cost and a low consumption are the most important parameters.

Different systems are based on a predistortion of the input signal and can be divided into three categories:

- High Frequency (HF) Predistortion: the component of predistortion works at the frequency of the carrier.
- Intermediate frequency (IF) Predistortion: the component of predistortion works at an intermediate frequency, allowing the design of a single predistortion for different carrier frequencies. The local oscillator frequency variation for the element of predistortion can be used with multiple carriers.
- Baseband Predistortion: before the appearance of DSP, this approach did not give a lot of advantages compared to an IF predistortion. It now becomes a very powerful tool. Predistortion characteristics are saved on a DSP in order to correct the baseband signal.

There is no feedback on this technique as the system works as an open-loop. This means that the distortion has to be known in advance and performance of this technique can be sensitive to variation due to the temperature, aging, process variation etc.

The improvement of the linearity obtained from the realistic case depends on many considerations, and more particularly on the behavior of the power amplifier. In general, the improvement of the linearity remains low compared to a Feedforward or a Cartesian Feedback. However, this improvement is satisfying for a lot of applications such as satellite communication systems.

These techniques do not make a dynamic correction according to the changes of the power amplifier behavior. For this reason a feedback path is added to the predistortion technique in order to make a dynamic correction.

1.4.4.2 Adaptive predistortion

Figure 1.23 shows an example of adaptive predistortion: it is the logical evolution of the classic predistortion due to a more often utilization of DSP. The idea comes from the main drawbacks of the predistortion technique, an inability to correct dynamically distortions of the power amplifier. The system, shown in Figure 1.23 [32], keeps a dynamic correction of the power amplifier. A predistortion table is computed based on the parameters of this model and from the comparison between the output signal from the PA and the transmitted signal from the input of the whole system. This system is able to react to any variations by periodically updating the predistortion table.

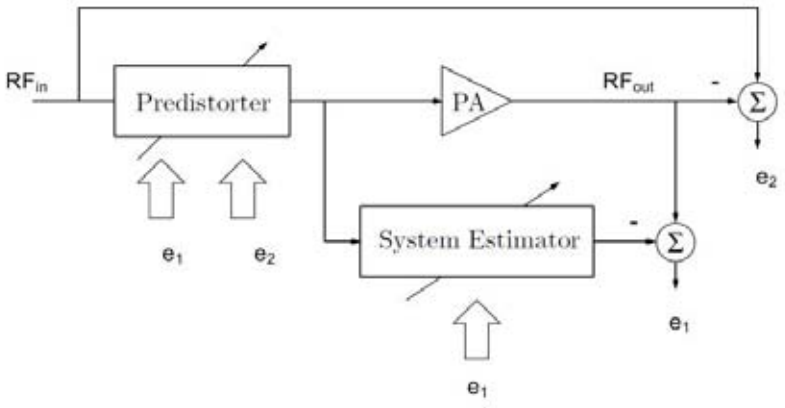


Figure 1.23: Example of an adaptive predistortion

The main drawback is the complexity of the adaptive part. Usually, this system requires high computing capacities, like a DSP where its required power can exclude the adaptive predistortion for mobile applications.

1.4.4.3 Feedforward

The popularity of this technique is due to its linearization potential of signals on multiple carriers and on a wide bandwidth application. The concept of this technique is simple but the implementation of it can be expensive. On the simplest configuration of this technique, two paths can be distinguished (Cf. Figure 1.24): a main RF path and a cancellation path. A hybrid divider is able to split the input signal and send it into both paths.

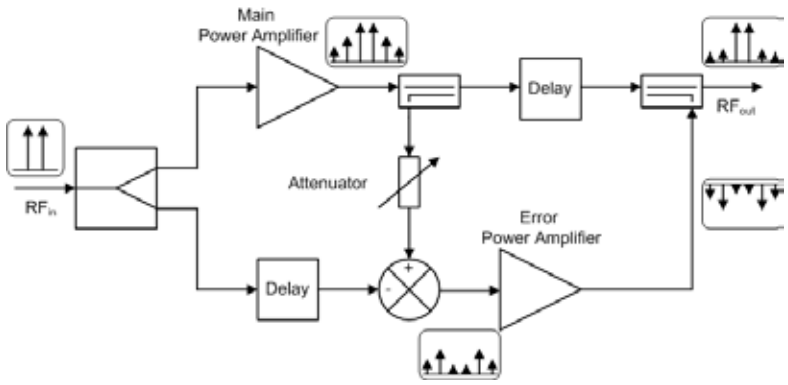


Figure 1.24: Feedforward technique

Part of the signal is delayed into a line in order to compensate the delay given by the power amplifier. The other part of the RF input power is amplified by a main power amplifier. Another part of the output signal is taken from a coupler, attenuated and sent into a hybrid combiner where it is compared with the signal coming from the delay line. With a variable attenuator to adapt the levels of RF signals, we recover only at the output of the hybrid combiner distortions generated by the power amplifier. These are then amplified in a highly linear Class A power amplifier. The signal coming from the error amplifier is ideally formed by the distortions created by the main power amplifier. The delay line of the main path is implemented to adjust the delay introduced by the second path; at the output of the last coupler, only the useful signal is conserved if the generated distortions by the main amplifier are well compensated.

The most critical component in the Feedforward technique is the error amplifier. It does not help itself to generate intermodulation products on one hand and have an important gain on the other. Furthermore, the delay and the gain are parameters that have to be carefully adjusted in this technique for a significant reduction of the intermodulation, and controls have to be implemented to realize these functions.

The technique has proven its efficiency for wide frequency bands and with multi-carrier signals

like the CDMA or W-CDMA. Used in the base stations and for satellites systems, this solution is not selected for portable systems, mobile, or low weight, die area and consumption.

1.4.4.4 Polar loop

The polar loop illustrated in Figure 1.25 has been presented by V. Petrovic [33] in 1979.

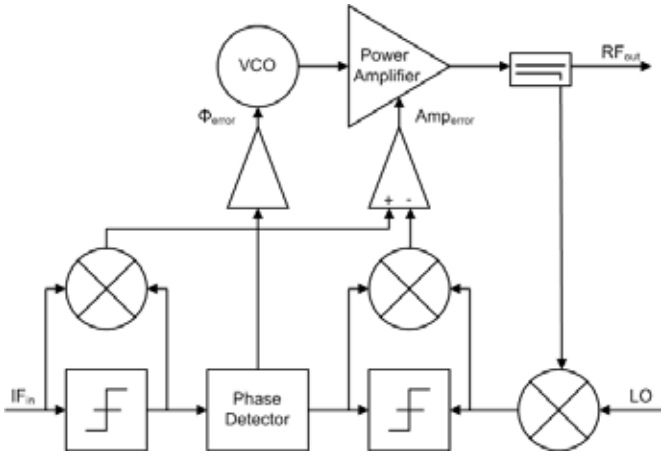


Figure 1.25: Polar loop technique

This technique is composed by two feedback loops: one for the phase and the other for the magnitude of the RF signal. A part of the output RF signal (RF_{out}) of the PA is taken and then demodulated to an intermediate frequency.

The input signal at the intermediate frequency IF (IF_{in}) is decomposed in amplitude and phase. These components are respectively compared with the amplitude and the phase from the output of the power amplifier. Error signals, Amp_{Error} for the amplitude and Φ_{Error} for the phase, are thus obtained (Cf. Figure 1.25).

The phase error signal control the VCO feeding the PA with a constant envelope signal but modulated in phase. The phase correction signal is equal to a classic PLL.

The amplitude error signal modulates the voltage supply of the PA by a simple feedback. These error signals are thus subtracted from the input signal correcting nonlinearities from the output of the power amplifier.

The polar loop is complex in terms of structural architecture. It can generate problems to lock the PLL for low level power.

As with all feedback systems, the polar loop has to present a sufficient phase margin on the loop to guaranty a good stability. This architecture suits all types of modulation, but it is more adapted for severe bandwidth modulation, regarding the polar representation of the signal, which involves an extension of the bandwidth.

1.4.4.5 Cartesian Feedback

Unlike the polar loop, the Cartesian Feedback works with signals decomposed in the Cartesian plan on the I and Q axis.

The linearization technique using a Cartesian Feedback was discovered by D. C. Cox in 1975 [34], then by V. Petrovic in 1979 [33]. Theoretically, this technique can reach an improvement of 40 dB on the adjacent channels.

According to Figure 1.26, I_{BB} and Q_{BB} baseband signals of the direct path are directly up-converted to the RF frequency. This frequency transposition is performed by quadrature mixers.

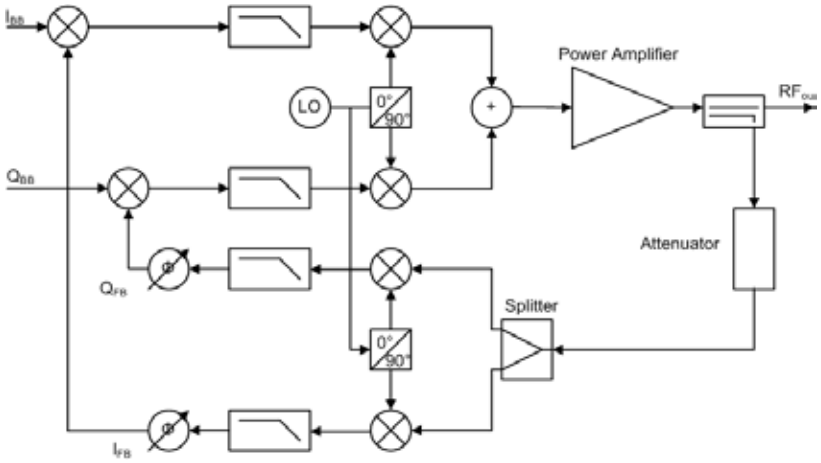


Figure 1.26: Cartesian Feedback technique

The RF signal is then amplified through a PA to reach the requested output power. The output signal of the power amplifier is attenuated and demodulated in quadrature (via down-conversion mixers) on the feedback path. Intermodulation products (at $2 * \omega_{LO}$), generated by the down conversion, are removed by low-pass filters. Demodulated and filtered signals of the feedback path are shifted in phase due to the components of the direct path. A phase correction is applied on the baseband signals to compensate phase distortions. These corrected signals are then subtracted from the original baseband signals giving as a result error signals for I and Q

baseband signals. Error signals carry information of the nonlinearities of the transmitter, and by loop effects the error signal will be revaluated according to the response of the direct path. Before low-pass filters of the direct path, input signals are predistorted signals. The resulting signal after the power amplifier is a linearized signal due to the compensation effect between the distortion of the amplifier and the predistorted signal.

The main issue of this architecture is to maintain its stability. To insure this, phase correction can be use guarantying an enough phase margin.

Compared to previous techniques, the Cartesian Feedback linearizes simultaneously the amplitude and the phase of the RF signals, using a single feedback path. This technique fits well with Zero-IF architecture. It allows linearizing not only the PA, but also the RF modulator.

However the linearization works correctly only within the bandwidth of the Cartesian Feedback. The system can be optimized in order to increase the bandwidth of the Cartesian Feedback. It corresponds to the bandwidth of the useful signal with its adjacent channels.

With only few more components, the Cartesian Feedback remains relatively easy to implement. This technique is very effective because it works with all types of modulation and offers good linearization performance.

Compared to other techniques presented, the Cartesian Feedback is the one which offers most assets in terms of cost (die area) and the consumption of the whole solution.

1.5 Conclusion

As demonstrated in this chapter, standards used for mobiles have been getting more and more complex; adding functions, decreasing the size and increasing the battery lifetime.

This evolution has been made with the interest of suppliers and sellers to decrease not only the size, but the cost to produce it, without forgetting that the cellular phone had to be fashionable enough to increase the sales for all consumers, and not only businessmen. A mobile able to please either the buyer who searches for capacity and efficiency to make phone calls and to text, or the purchaser who is looking for an accessory able to reflect prosperity and modernity even if it is not really efficient.

The development of cellular communications has several architectures of a transmitter with their pros and cons as announced in Table 1.2. As our goal was to focus on the integration, the consumption and the nature of the modulation, the homodyne architecture was highlighted as it matches with these criteria. It is an architecture which uses simple and few analog components, resulting in an integration that does not need a lot of silicon area and, thereby, does not need a high consumption of energy. Also, this topology can work with constant and non-constant envelope modulations, in other words, with any existent modulation on telecommunication standards nowadays.

Besides this, all transmitters in certain levels of output power will create interferences that must be decreased with a linearization technique. Some will increase the efficiency of the transmitter and other linearization techniques will increase the linearity of it:

– Increasing the efficiency of the transmitter but without the improvement of the linearity, with high or medium consumption and die area occupation: EER and LINC techniques; and
– Increasing the linearity of the transmitter but with different results regarding the flexibility, simplicity, consumption and die area occupation:

	Flexibility	Simplicity	Consumption	Die Area Occupation
Predistortion	No	Yes	Low	Low
Adaptive Predistortion	Yes	No	Medium	Low*
Feedforward	Yes	No	High	High
Polar Loop	Yes	No	Medium	Medium
Cartesian Feeback	Yes	Yes	Low	Low

*Needs an external component as a DSP.

Table 1.4: Comparison of linearization techniques

Please note that as mentioned in this chapter, our study considers only the most common techniques in the literature, the ones above.

We opted for a linearization technique as we did to select the transmitter architecture: the one that fitted with our criteria and goal. Ergo, the Cartesian Feedback remains a technique with a lower consumption and takes the less die area. Moreover, this technique has as advantages to be flexible and simple to implement, as we will demonstrate in the following chapters.

Chapter

2 Analysis and Specifications of the Cartesian Feedback

Contents

Every mobile communication system has to be led by a normalized standard able to define a lot of characteristics as power, linearity and noise generated at the output of the RF transmitter or at the input of the receiver. Unfortunately the standard does not determine the architecture that the designer has to use on his chip and does not give any specification about all the building blocks included in a transmitter. Hence, theory and simulations on system levels have to be realized before the design of the circuit and be in compliance with the standard used, in our case the W-CDMA.

In order to get an optimal solution, minimizing the die area and the consumption of the circuit, the study must consider the whole architecture of the transmitter, identify and resolve problems in the architectural design, from the digital process in baseband domain to the analog RF components. A model of the Cartesian Feedback will be explained to understand stability and noise issues capable to make an oscillating system.

From the perspective of the integration of our transmitter in 65nm CMOS technology, a mixed architecture has been developed [35] improving the linearity in real-time. The digital part will help the system correct distortions on the signal whatever is the result at the output of the transmitter.

2.1 Digital/Analog Partitioning Architecture of the Transmitter

A Cartesian Feedback able to linearize a power amplifier with only an analog circuit was designed few years ago [36, 37, 38]. In order to reduce the consumption and increase the level of integration of the solution, a previous study with STMicroelectronics proposed to move some functions to the digital domain [39]. The operations of phase correction and subtraction can be implemented in VHDL using DSP (Digital Signal Processing) [40]. The phase corrector and the subtractor are components of the feedback path and have to be the most linear as possible. Realizing these two functions with analog circuitry resulted in an increased power consumption and die area. Moreover, the main advantage of the mixed solution is to correct any signal from

the output of the power amplifier. The output signal of the power amplifier can change depending on aging or temperature, but if the output signal will change, the signal will be consequently different and a correction will have to be done. This will make an attractive solution with low cost and low power consumption, which has been the current trend in the past years for the industry.

A conversion stage is then added to the Cartesian Feedback architecture. This stage is composed by two digital-to-analog converters (DAC) for the direct path and two analog-to-digital converters (ADC) for the feedback path. The increased power consumption induced by these converters will be compensated by the improvement of the linearity in comparison with an analog solution. This architecture is presented in Figure 2.1 [41].

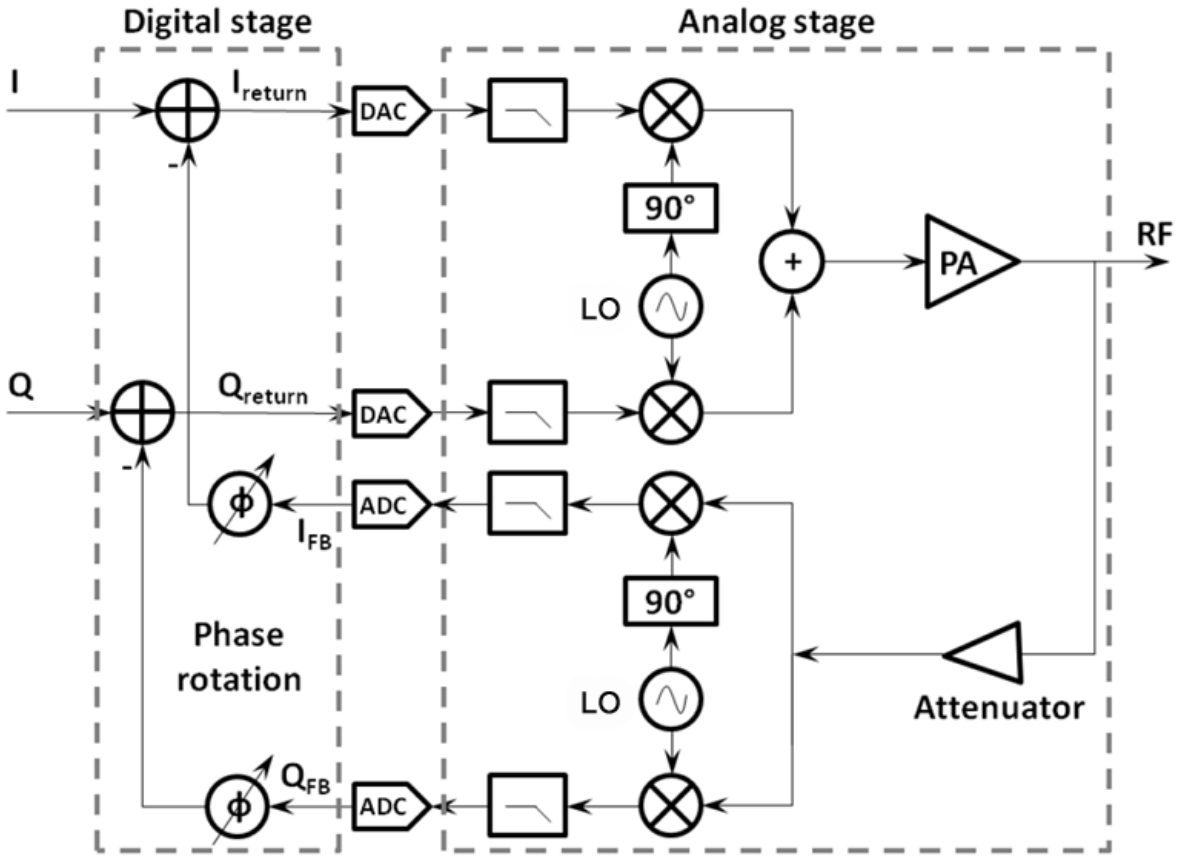


Figure 2.1: Mixed Cartesian Feedback architecture

In this architecture, low-pass filters have two objectives. They have to filter frequency image of all harmonics from the sampling frequency, and remove the $2.f_{LO}$ harmonics introduced by the down conversion in the feedback path.

These harmonics make the second-order term at the output of the RF modulator able to unbalance and deteriorate the image rejection of the modulated signal.

Low-pass filters of the feedback path remove the $2.f_{LO}$ intermodulation products given by the RF demodulator, and avoid the folding spectrum during the conversion of the analog signal to the digital signal.

2.2 Mathematical Analysis of the Cartesian Feedback Architecture

The problem of the stability appears with the feedback path. If the system is unstable the given correction will not be efficient and the system will oscillate. Therefore, a study about the stability, the noise and the effects of external or internal components has to be developed.

2.2.1 Stability study

It remains an important part to explain the phenomena of stability, noise and linearity capable to make an oscillating system. The study and the feasibility of the Cartesian Feedback have been proved by C. Tassin [35]. This study is based on the modeling of the Cartesian Feedback by using the Volterra Series.

2.2.1.1 Modeling of the Cartesian Feedback

The studies of M. Briffa and M. Faulkner [42, 43] propose a detailed analysis of the Cartesian Feedback. They present the evaluation of the stability through the response of the power amplifier for a little perturbation ΔV_i around a working point fixed by an input vector V_i. A simplified model of the transmitter in open-loop is presented in Figure 2.2.

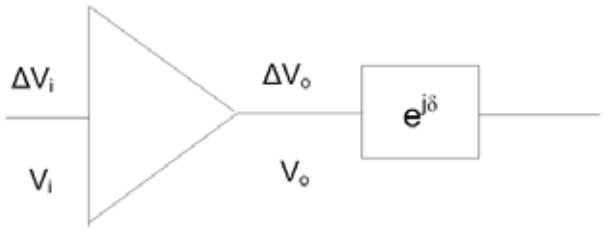


Figure 2.2: Simplified model of an open-loop transmitter

The phase-shifting between the direct and the feedback path is given by $e^{j\delta}$.

The large signal gain g is defined by equation 2.1:

$$g = \frac{\Delta V_o}{\Delta V_i} \tag{2.1}$$

As the Cartesian Feedback has multiple inputs and outputs, it can be considered as a MIMO system (Multiple-Input and Multiple-Output), with signals I_{in} and Q_{in} for the input path and I_{out} and Q_{out} for the feedback path (Cf. Figure 2.3).

$G(s)$ represents the gain of the loop and δ is the phase-shifting of the system.

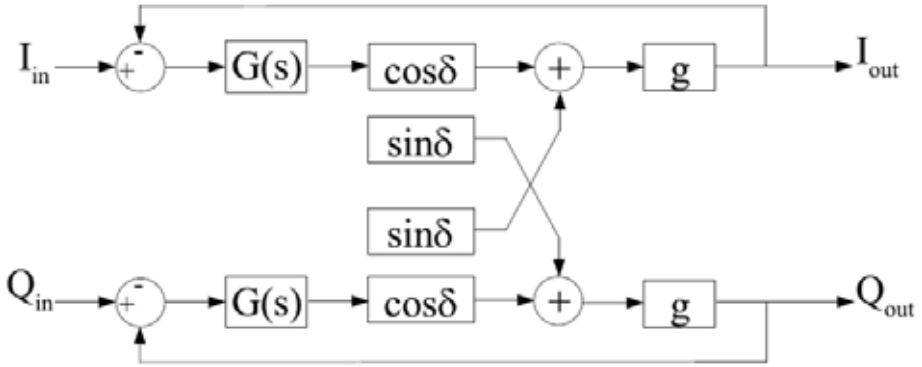


Figure 2.3: MIMO model of the Cartesian Feedback

The open-loop transfer function (OLTF) of the previous model is given by equation 2.2:

$$OLTF = \begin{bmatrix} gG(s)\cos\delta & -gG(s)\sin\delta \\ gG(s)\sin\delta & gG(s)\cos\delta \end{bmatrix} \begin{bmatrix} I \\ Q \end{bmatrix} \tag{2.2}$$

The model of the system becomes unstable when the gain margin is zero. The characteristics of the stability can be deduced from equation 2.3, where Id is the identity matrix and the absolute value represents the determinant.

$$\left| Id + \begin{bmatrix} gG(s)\cos\delta & -gG(s)\sin\delta \\ gG(s)\sin\delta & gG(s)\cos\delta \end{bmatrix} \begin{bmatrix} I \\ Q \end{bmatrix} \right| = 0 \tag{2.3}$$

Solutions of this stability equation are given by equation 2.4:

$$gG(s) = -\cos\delta \pm j\sin\delta \tag{2.4}$$

Thanks to the previous equation, we can deduce that the phase margin of the system is equal to $|\delta|$.

2.2.1.2 Influence of phase-shifting on the stability

The main problem of the angular distortion is a classic issue of all systems using a feedback path. The phase-shifting can be translated as a time delay which reduces the phase margin and can lead to the instability of the loop. In our case, signals from the feedback path are at high frequencies compared to the baseband signals and can cause a mismatch between I and Q signals.

J.L. Dawson [36] has mathematically expressed the RF phase-shifting using the schematic illustrated in Figure 2.4.

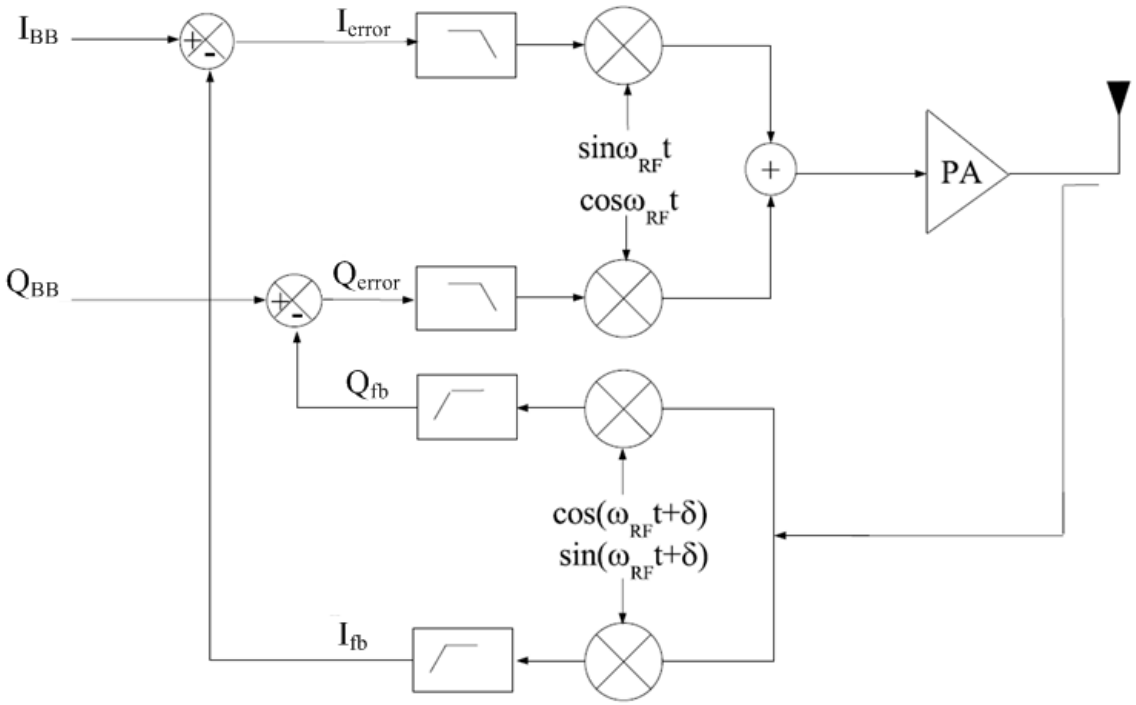


Figure 2.4: Coupling of the I and Q paths by phase-shifting

Mathematical expressions of I and Q path at the input of the system are:

$$I_{BB} = I.\sin(\omega_{BB}t) \tag{2.5}$$

$$Q_{BB} = Q.\cos(\omega_{BB}t) \tag{2.6}$$

After the RF modulation, the RF demodulation and the attenuation, we can observe the following expressions of I and Q feedback signals (I_{fb} and Q_{fb}):

$$I_{fb} = \frac{I}{2}\sin(\omega_{BB}+\delta) + j\frac{Q}{2}\cos(\omega_{BB}+\delta) \quad (2.7)$$

$$Q_{fb} = \frac{I}{2}\cos(\omega_{BB}+\delta) + j\frac{Q}{2}\sin(\omega_{BB}+\delta) \quad (2.8)$$

Finally, the subtraction between the original signals and feedback signals is:

$$I_{error} = \frac{I}{2}\sin(\delta) + j\frac{Q}{2}\cos(\delta) \quad (2.9)$$

$$Q_{error} = \frac{I}{2}\cos(\delta) + j\frac{Q}{2}\sin(\delta) \quad (2.10)$$

Mathematical expressions of error signals show the effect of the RF distortion. Each mathematical component is described as a function of the other. I and Q signals are coupled and they modified the initial gain (G_{fb}) margin of the Cartesian Feedback as shown in equation 2.11.

$$G_{fb\_coupling} = G_{fb}.\sin(\omega_{BB}t+\delta) - \frac{jG_{fb}^2}{2.(1+jG_{fb}.\cos(\omega_{BB}t+\delta))} \quad (2.11)$$

If $\delta = \pi$ then there is an inversion of I and Q channels, the response of the loop is greater than zero and the system becomes unstable.

If $\delta = \pi/2$, then $G_{fb\_coupling} = G_{fb}^2$ and the coupling is maximal.

2.2.1.3 Graphical criteria of the stability

The RF phase-shifting is mainly introduced by the AM/PM conversion of the power amplifier. The increase of the gain amplifies the phenomenon of the AM/AM conversion and reduces, therefore, the phase margin of the system. When the RF distortion is equal to the phase margin, the system becomes unstable.

The graphical explanation is illustrated in Figure 2.5 and expresses the RF phase-shifting as a function of the gain margin, specifying the instability areas.

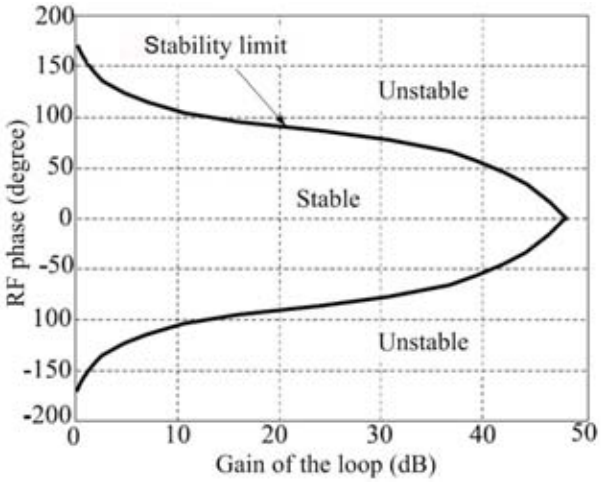


Figure 2.5: Graphical criteria of the instability

2.2.2 Noise study

For any communication system, we need a transmitter and a receiver. The receiver has to be as noiseless as possible in order to retrieve the data. However, the transmitter can not be noisy because the carried data will be harder to retrieve. Therefore noise performance of a transmitter have to be checked for the design. Strong levels of noise will degrade the sensitivity of the receiver and will lead the loss of useful information.

A noise study of the Cartesian Feedback has been made by P. B. Kenington [44]. This research uses an equivalent model of the Cartesian Feedback represented in Figure 2.6.

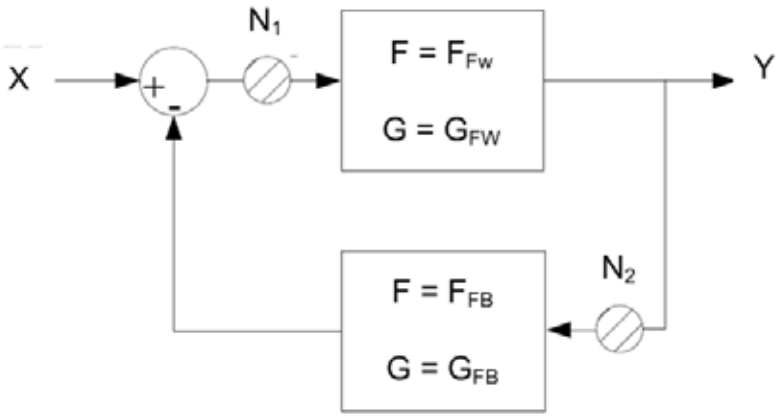


Figure 2.6: Noise model of the Cartesian Feedback

The noise level of the direct and the feedback path are defined as N_1 and N_2, respectively, where k represents the Boltzmann constant equal to $1,38.10^{-23}J/K$, T_0 is the reference temperature in $Kelvin$ (297 K, 24°C) and B represents the bandwidth of the noise in $Hertz$.

$$N_1 = F_{FW}kT_0B \tag{2.12}$$

$$N_2 = F_{FB}kT_0B \tag{2.13}$$

The output value Y as a function of the input value X and the noise values N_1 and N_2 are given by equation 2.14.

$$Y = \frac{X}{G_{FB}} + \frac{N_1}{G_{FB}} - N_2 \tag{2.14}$$

Equation 2.15 shows the output value Y as a function of the input value X and the noise factors F_{FW} and F_{FB}.

$$Y = \frac{X}{G_{FB}} + \frac{F_{FW}KT_0B}{G_{FB}} - F_{FB}KT_0B \tag{2.15}$$

This model realized by Kenington shows that the noise value of the direct path is attenuated by a factor equal to the gain of the loop. However, the noise of the feedback path is added directly to the noise level of the Cartesian Feedback. This conclusion is only valid within the bandwidth of the system and can not be the same out of band. The noise outside of the bandwidth is generated by RF components working at the frequency of the RF signals, such as mixers or power amplifiers.

2.2.3 Linearity

The linearization of a transmitter treats the linearity characteristics of its constituents. As the noise can degrade performance of the transmitter, the linearity can also deteriorate the carried data and the sensitivity of the receiver. If the levels of harmonic distortions are too high, the receiver will not be able to distinguish the real information in the signal. Therefore, it remains essential to analyze the linearity contribution of each block making the Cartesian Feedback.

For the linearity analysis of our system, we can use the Volterra series [45, 46] which form the model of a system using a feedback path according to the frequency used. The analysis of the Volterra model is strictly used for systems reasonably nonlinear with low-level signals, in order to stay on the linear region. It seems complicated to measure the efficiency of the Volterra Series,

as a consequence an analysis using a harmonic balance has to be done at the same time. This kind of simulation aims to equilibrate iteratively harmonics of a system until the convergence criteria are achieved.

The decomposition in Volterra series gives n^{th} order of the transfer function which are the n^{th} order of Volterra kernel. Figure 2.7 helps to calculate Volterra kernel of the Cartesian Feedback.

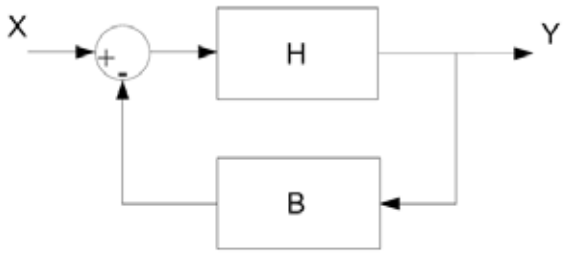


Figure 2.7: Linearity model of the Cartesian Feedback

From [45, 46], we can define the expression of i^{th} order of Volterra kernel of the Cartesian Feedback G_i according to i^{th} order kernels of the direct path H_i and of the feedback path B_i. The matrix identity is represented by Id.

$$G_i(X) = H_i(Id - B_i(G_i(X))) \tag{2.16}$$

For example, $G_1(f_1)$ is the voltage gain of the Cartesian Feedback and $G_3(f_1, f_1, f_1)$ represents the third-order kernel of harmonics distortions. In order to simplify the study, we will only consider the third-order nonlinearities and we will exclude the second-order nonlinearities which do not effect our useful channel.

Equations 2.17 and 2.18 can be found with the development of the previous equation until the third-order of kernels. $G_1(f_1)$ and $G_3(f_1, f_1, f_1)$ represent, respectively, the first-and the third-order of kernels for the Cartesian Feedback.

$$G_1(f_1) = \frac{H_1(f_1)}{1 + B_1(f_1).H_1(f_1)} \tag{2.17}$$

$$G_3(f_1, f_1, f_1) = \frac{H_3(f_1, f_1, f_1) - H_1(f_1)^3 B_3(f_1, f_1, f_1)}{(1 + H_1(f_1) B_1(f_1))^4} \tag{2.18}$$

The output spectrum of a Zero-IF transmitter has a useful component which is $f_{LO} - f_{BB}$, a LO signal and a third-order harmonic distortion (HD3). Figure 2.8 shows these signals, where

f_{BB} is the baseband frequency corresponding to the frequency f_1.

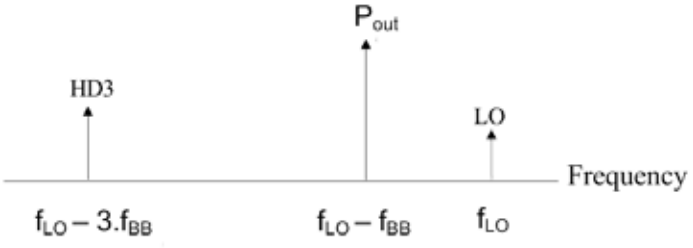


Figure 2.8: Output transmitted spectrum

The HD3 at the output of the Cartesian Feedback is defined by equation 2.19 [47], where V_{in} is the level of the input signal.

$$HD3_G = \frac{1}{4} G_3 \left(f_1, f_1, f_1\right) . V_{in}^3 \tag{2.19}$$

The expression of G_3 (Cf. equation 2.18) shows the linearization of the direct path using a feedback loop. The third-order Volterra kernel of the direct path H_3 is largely attenuated by a factor equal to the gain of the loop to the fourth power. This equation shows also that the value of the third-order kernel for the feedback path B_3 has to be weak to maintain the linearization.

2.2.4 Bandwidth of the loop

The W-CDMA standard has specifications linked to the ACLR at 5MHz from the carrier but also at 10MHz. For this reason, the Cartesian Feedback has to linearize both channels. The bandwidth of the main channel $B_{channel}$ of the W-CDMA signals is 3.84MHz and, in order to cover the required predistortion on the input signal, the bandwidth of the Cartesian Feedback (B_{CFB}) has to be 1.8 times larger (which represents $B_{channel}/2 + 5MHz = 6.92MHz$)[31].

Figure 2.9 shows the signal of the W-CDMA standard with its useful channel and the bandwidth of the Cartesian Feedback.

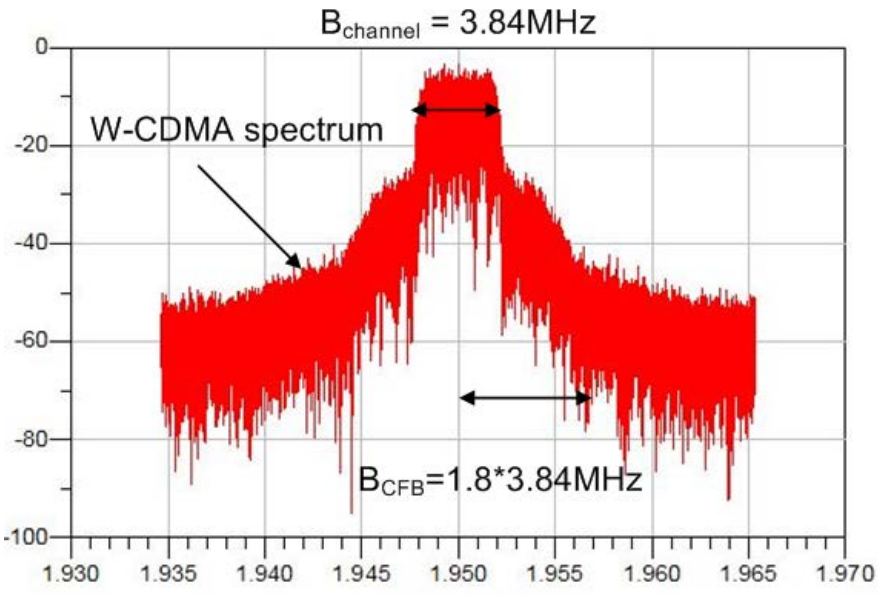


Figure 2.9: Bandwidth of the Cartesian Feedback

The transmitter using the Cartesian Feedback with filters for the direct and the feedback paths will have a bandwidth controlled by the bandwidth of the feedback filter.

2.2.5 LO pulling on Zero-IF architecture

For the Zero-IF architecture, using only one-stage for the frequency conversion from the baseband signals until the RF signal, some phenomena can interfere between internal components. At the output of the PA, the RF signal can disturb the local oscillator as it is shown in Figure 2.10.

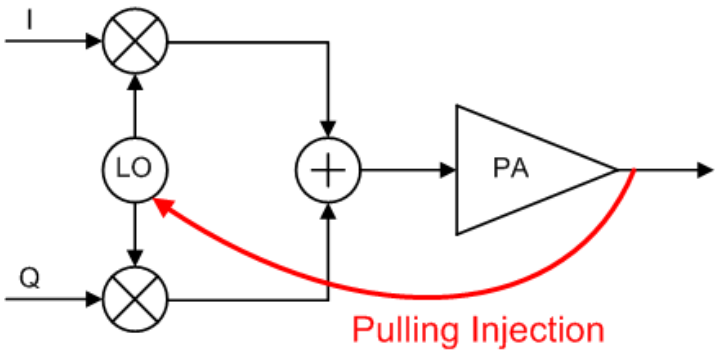


Figure 2.10: Pulling injection for a Zero-IF transmitter

As a consequence, the frequency of the local oscillator will be switched at the frequency of the output signal. Then, the system will be deteriorated and will lose data.

In our case, we propose to place the local oscillator off-chip in order to observe the improvement of the linearization on an integrated circuit.

2.2.6 DC offset

Another disturbance can be observed and is linked to the process technology. As a matter of fact, the mismatch of components can deliver a DC offset associated to the baseband signals with the useful information. This offset is transposed into the LO frequency in the RF modulator and represents the DC leakage as it is shown in Figure 2.11.

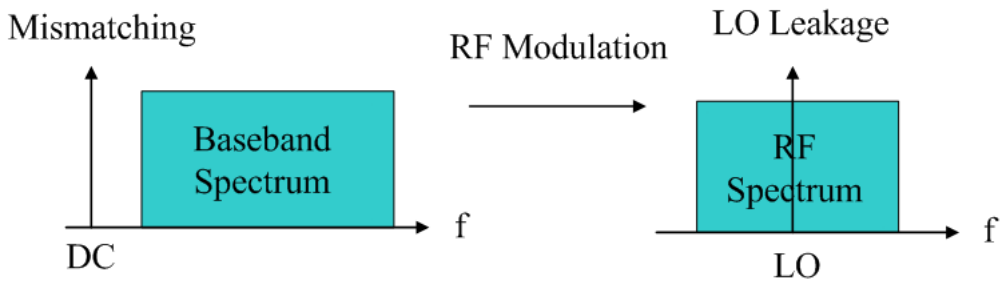


Figure 2.11: LO leakage for a RF transmitter

This leakage of the LO is impossible to cancel, because it is located on the main channel and can deteriorate the sensitivity of the receiver. One solution is to avoid this leakage during the design of the IC layout. If we design all critical paths (e.g. RF signals) the most symmetrical as possible, we can minimize this phenomenon inside an IC.

2.3 Digital Part

The digital part remains a critical section in order to insure the stability of the system. After a theoretical study, two solutions have been proposed to make the signal correction of the Cartesian Feedback, using LUTs (Look-Up Table) and a CORDIC (COordinate Rotation Digital Computer) algorithm [48].

2.3.1 Context and constraints

The main objective of the digital part is to put signals in phase, as we synchronize the transmitter and the receiver. The direct path can be compared to the transmitter and the feedback path to the receiver. Then, the digital part performs a subtraction operation to get the corrected signal. These operations must be the most accurate as possible in order to maintain the stability

of the system. Indeed, the delay of the digital part has to be controlled to respect real-time constraints of the application on one hand, and keep the system stable on the other.

For W-CDMA standard, the data rate is equal to 3.84Mcps. As a result, the entire delay can not be greater than the delay between two frames which is 260ns. The delay for the analog part is essentially caused by low-pass filters and can be estimated by simulation to 32ns and 45ns for the direct and the feedback filters respectively. From these results, the whole delay of the analog part can not exceed 77ns (32ns + 45ns) and, as a consequence, gives 183ns (260ns - 77ns) for the digital part. This constraint has to correspond to the sampling frequency fixed by converters (ADC and DAC) which is 240MHz.

It is from the digital delay of 183ns that the designer will choose the best solution for the implementation of the digital part on ASIC technology.

2.3.2 CORDIC implementation

The CORDIC algorithm is an iterative algorithm developed to make basic operations such as rotation on a vector. This algorithm was improved to process trigonometric functions (e.g.: exponential, cosines, sines. . .) by setting its inputs variables.

Figure 2.12 represents the different blocks to consider when the CORDIC algorithm is used.

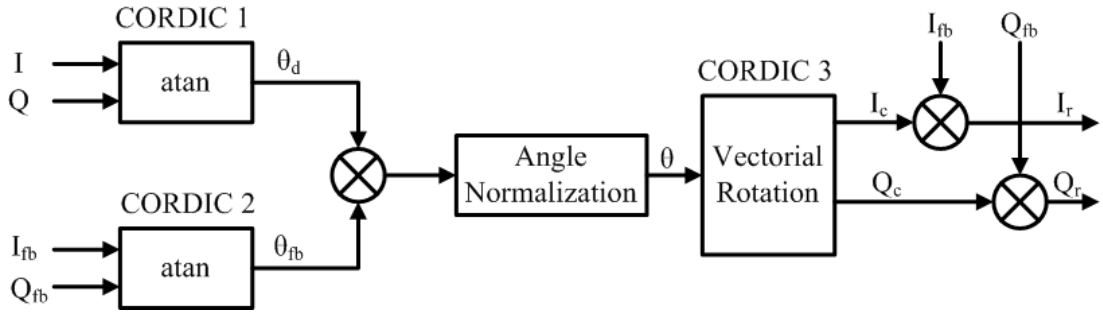


Figure 2.12: Solution based on CORDIC algorithm

2.3.2.1 CORDIC algorithm

Electronic computers have experienced a considerable expansion since the 1950s. They began to reach more diverse areas, such as aerospace, and the need for real-time calculations became stronger, especially for trigonometric calculations. In 1959, J. E. Volder created an algorithm which led to approximate trigonometric functions from basic operations (addition, subtraction

and multiplication) [49]. This algorithm is called "CORDIC" and is based on the calculation of a vector which is applied in the considered rotation. Thanks to its material integrability (the ingenuity of the algorithm allows a simple electronic connection), the algorithm is used for many applications such as mathematical coprocessors and scientific calculators [50].

The CORDIC algorithm is based on Givens rotation [51] as we can see in equation 2.20.

$$R = \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} X \\ Y \end{bmatrix} \tag{2.20}$$

This rotation is an iterative rotation with specific angle $\theta_i = arctan(2^{-i})$ as it will be shown further. This operation has as a consequence to produce a pseudorotation where the matrix is defined by equation 2.21. The pseudorotation appears only when θ is a sum of $\theta_i = arctan(2^{-i})$.

$$R_c = \begin{bmatrix} 1 & -\tan(\theta) \\ \tan(\theta) & 1 \end{bmatrix} \tag{2.21}$$

As previously mentioned, the CORDIC algorithm uses the vector rotation where the relation is given by the following equation:

$$\begin{bmatrix} X' \\ Y' \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} X \\ Y \end{bmatrix} \tag{2.22}$$

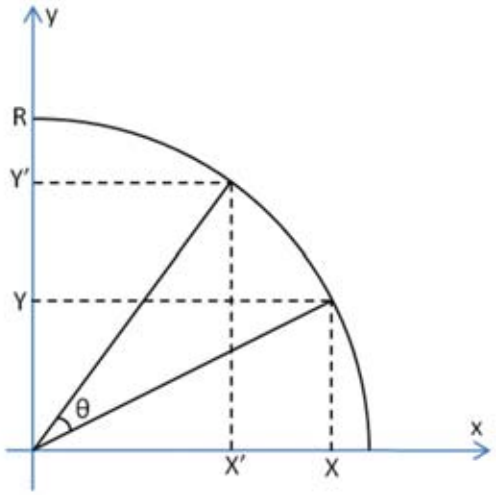


Figure 2.13: Vectorial rotation by a θ angle

The idea is to apply n angle rotations on a vector of coordinates $\begin{bmatrix} X \\ Y \end{bmatrix}$. For each iteration, the value of angle decreases until to be equal to 0. At the end of the n iterations, the sum of all angles is equal to θ.

If the initial vector is chosen such as $\begin{bmatrix} X_0 \\ Y_0 \end{bmatrix} = \begin{bmatrix} X_0 \\ 0 \end{bmatrix}$, the quotient $\begin{bmatrix} \frac{Y_n}{X_n} \end{bmatrix}$ represents the approximation of the $tan(\theta)$.

Moreover, if $X_0 = 1$ then X_n and Y_n are approximations of $cos(\theta)$ and $sin(\theta)$, respectively.

θ can be decomposed in a sum of $\theta_1 + \theta_2 + \ldots + \theta_n$, where $\theta_i = arctan(2^{-i})$ is small enough to insure the convergence and it can be used more than once on this decomposition. Figure 2.14 represents iterations that the CORDIC algorithm has to follow in order to converge into the θ.

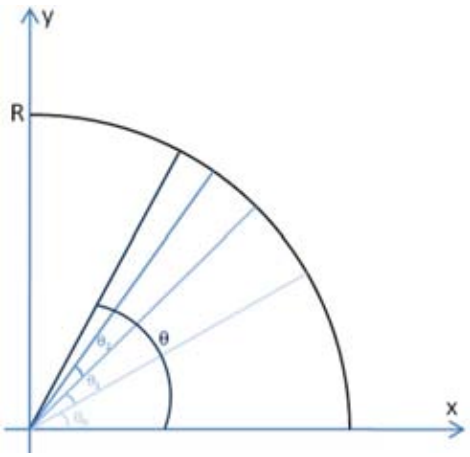


Figure 2.14: Iterative convergence of CORDIC algorithm

Subsequently, we have to calculate n intermediate coordinates, but to calculate them, we have to know how to calculate results of $cos(\theta_k)$ and $sin(\theta_k)$. This calculation introduces a problem because the algorithm has been made to calculate these latters. To avoid this issue, we transform these relations in order to bring up tangents and thus factorize $cos(\theta_k)$ as it is described in the following equations:

$$\begin{bmatrix} X_{n+1} \\ Y_{n+1} \end{bmatrix} = \begin{bmatrix} \cos(\theta_n) & -\sin(\theta_n) \\ \sin(\theta_n) & \cos(\theta_n) \end{bmatrix} \begin{bmatrix} \cos(\theta_{n-1}) & -\sin(\theta_{n-1}) \\ \sin(\theta_{n-1}) & \cos(\theta_{n-1}) \end{bmatrix} \cdots \begin{bmatrix} \cos(\theta_0) & -\sin(\theta_0) \\ \sin(\theta_0) & \cos(\theta_0) \end{bmatrix} \begin{bmatrix} X_0 \\ Y_0 \end{bmatrix} \tag{2.23}$$

$$\begin{bmatrix} X_{n+1} \\ Y_{n+1} \end{bmatrix} = \prod_{k=0}^{n} \cos(\theta_k) \begin{bmatrix} 1 & -\tan(\theta_k) \\ \tan(\theta_k) & 1 \end{bmatrix} \begin{bmatrix} X_0 \\ Y_0 \end{bmatrix} \tag{2.24}$$

$$= \prod_{k=0}^{n} \cos(\theta_k)\, Rc \begin{bmatrix} X_0 \\ Y_0 \end{bmatrix} \tag{2.25}$$

Where R_c is a pseudorotation matrix.

The development of equation 2.24 can be expressed as:

$$X_{n+1} = k * [X_n - \tan(\theta_n) * Y_n] \tag{2.26}$$

$$Y_{n+1} = k * [Y_n + \tan(\theta_n) * X_n] \tag{2.27}$$

Considering only elementary angles, we can replace $\tan(\theta)$ by $\pm 2^{-n}$.

$$X_{n+1} = X_n - d_i * 2^{-n} * Y_n \tag{2.28}$$

$$Y_{n+1} = Y_n + d_i * 2^{-n} * X_n \tag{2.29}$$

where d_i represents the decision function driven by the sign of registers.

In this case, we can ignore the k factor. Actually, the amplitude error can be rectified by multiplying only the result of the previous iteration by the inverse of the coefficient $\prod_{k=0}^{n} \cos(\theta_k)$. In order to know the direction and the angle of the rotation related to the actual iteration, we use another equation which gives a new value of the rotation angle as it is described in the next equation:

$$Z_{n+1} = Z_n - d_i * \arctan\left(2^{-i}\right) \tag{2.30}$$

The algorithm converges by setting the auxiliary variable Z_n from the start angle θ to zero. The Z_n is updated according to the direction of the rotation. The choice of the value d_i makes us consider the actual angle of the vector Z_{n+1} that we subtract from the wanted angle. We test the result, and, if it is positive, the rotation is in the direction of clockwise, and if it is negative, the rotation is in the direction of counterclockwise (Cf. Figure 2.15).

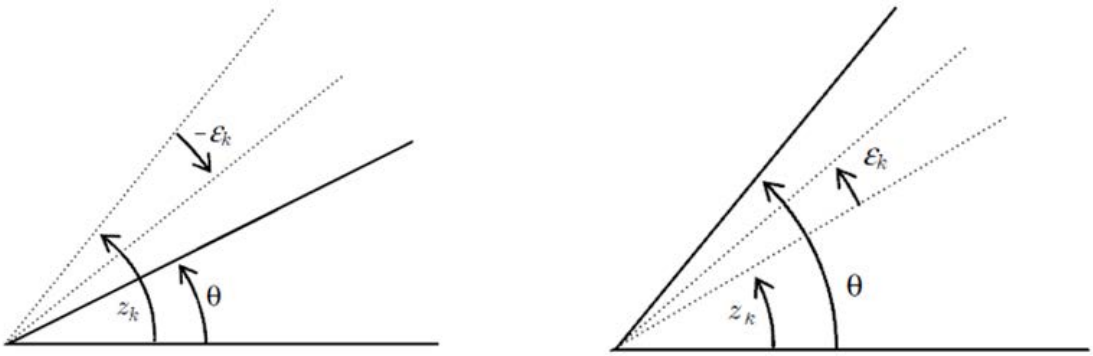


Figure 2.15: Updating of Z_k value

The arctangent such as $\theta = \arctan\left(\frac{Y}{X}\right)$, can be directly calculated using the vectoring mode according to [52].

The CORDIC rotation has two operating modes:

- The vectoring mode allowing to perform computation of inverse trigonometric functions such as the arctangent, arccosine, arcsine. X and Y are initialized respectively by coordinates x and y of the desired point, and Z is set to 0. The direction of the rotation is defined by Y [52, 49]. The algorithm converges when the value of Y is equal to 0.

- The circular mode (or rotation) representing the conventional working mode of the algorithm. X and Y are initially set to the coordinates of the point that we want to rotate, and Z is set to θ. The algorithm converges when the value of Z is equal to zero. Value of X and Y are initialized respectively to the coordinate (x, y) of the targeted point and Z is set to zero.

The implementation of this algorithm can be realized in several ways depending on the constraints. A compromise between the working frequency and the die area has to be done according to the targeted application. For our case, the phase calculation has to be done in real-time. The iterative solution, which uses a register at the output for one iteration, and then reuses the same resource, does not fit with our applications. As this architecture is slow, a parallel CORDIC with pipelined register is used as it shown in Figure 2.16 [52].

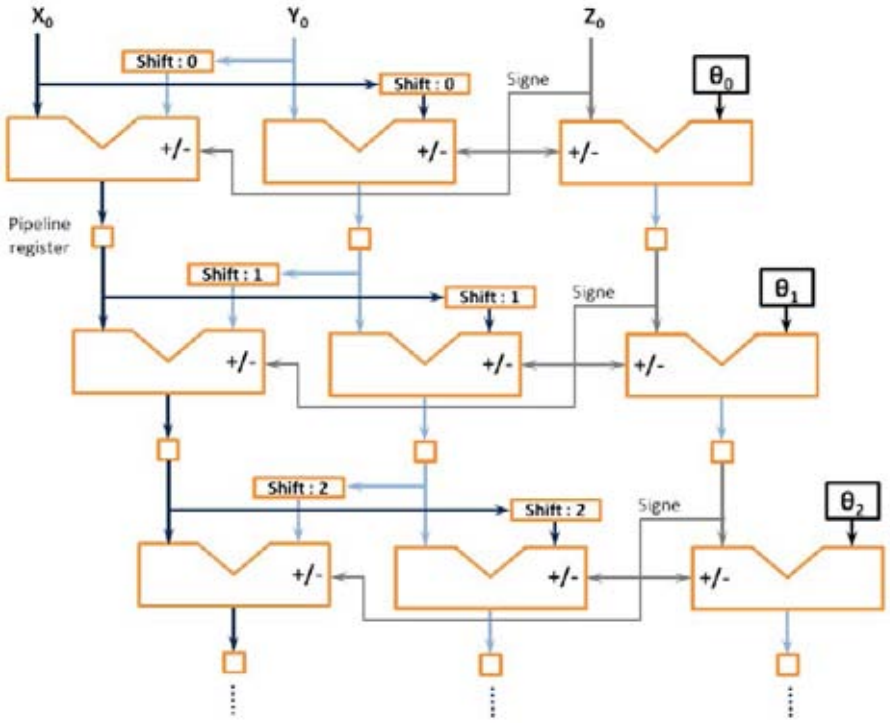


Figure 2.16: Parallel CORDIC with pipelined register

2.3.2.2 Normalization of the angle θ

After the calculation of the phase of the direct path (I/Q) and the feedback path (I_{fb}/Q_{fb}), we have to perform the subtraction of these two angles to find the desired phase-shifting.

$$\theta = \theta_d - \theta_{fb} \tag{2.31}$$

Once this subtraction is done, we need to normalize the angle θ_k in order to have an angle modulo 2π. The implementation of this function in VHDL is realized with successive tests and rotations. The main advantage of this function is that it does not use a lot of silicon area.

2.3.2.3 Subtraction

The digital subtraction is simple for the implementation in VHDL. It is sufficient to calculate the two complements of the second operand and then use an adder to get the result of this operation.

2.3.3 LUTs implementation

2.3.3.1 LUTs optimization

As it is illustrated in Figure 2.17, values of sine, cosine and arc-tangent used for the phase correction are stored in interpolation tables (LUT – Look-Up Table). To minimize the size of these tables, symmetrical properties are used (Cf. equations 2.32, 2.33, and 2.34).

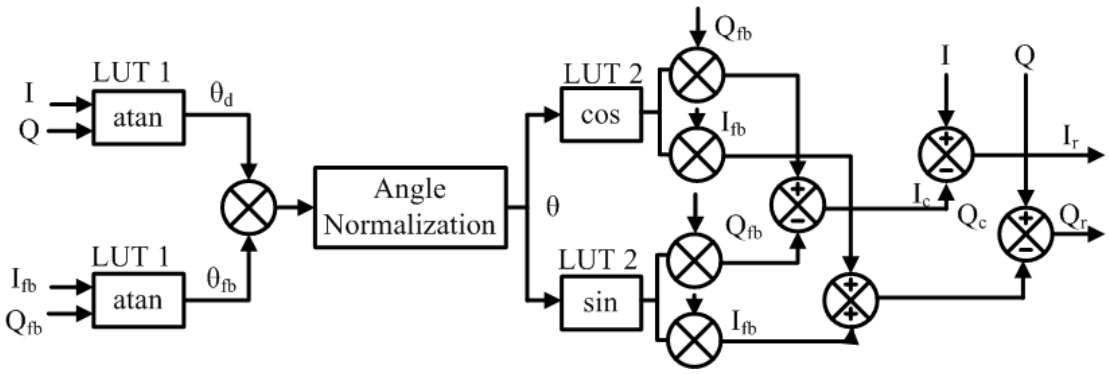


Figure 2.17: Solution based on LUT

$$\cos(-x) = \cos(x) \tag{2.32}$$

$$\sin(-x) = -\sin(x) \tag{2.33}$$

$$\arctan(-x) = -\arctan(x) \tag{2.34}$$

Thereby only values corresponding to positives angles are stored on LUTs. To avoid any overflow and keep an accurate precision (~1°) on the phase correction, the floating format used is 12bits including 11bits for the fractional part.

The LUT solution is implemented in VHDL as a ROM (Read-Only Memory). The VHDL syntax is a one-dimensional table which can be read by a simple value.

2.3.3.2 The Restoring Division Algorithm (RDA) divider

The phase error calculation, before the rotation of the signals, uses dividers (Cf. Figure 2.17). The division of two signed operands is realized in simulation owing to the operator "/". But this operation does not work with synthesis tools in VHDL, hence the need to create a division algorithm.

In the literature, we have found algorithms to implement a digital divider [53, 54]. The simplest solution is to use the algorithm of RDA (Restoring Division Algorithm). This algorithm forces into a value of operands strictly positives and also, a value of numerator greater than or equal to the denominator. A division by zero represents a saturation of the maximum value. In order to make the same operations for negative operands or numerators lower than the denominators, a special treatment has to be developed.

The algorithm used is iterative and has as objective to store the dividend in a register A, and the divider in a register B (note that the other registers are set to zero), and further make n iterations (n is the length of the quotient).

For each iteration:
- Shift the register (P, A) one bit to the left
- Subtract the value of B from P, and put the new result in P
- If the result is positive, put the most significant bit (MSB) of the register A to 1
- If the result is negative, put the less significant bit (LSB) of the register A to 0, and then restore the old value of the register P adding the value of B to P.

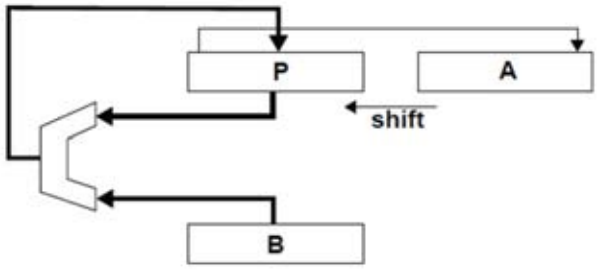


Figure 2.18: Restoring division algorithm

2.3.3.3 Conclusion of the digital part

The main parameter that the designer can work with is the frequency of the algorithm. The frequency has to be as high as possible to respect the real-time constraint of the application.

In this part, we investigated two solutions to work with the frequency to find which one will respect this constraint better. The first solution is based on the CORDIC algorithm and the second uses LUTs. A theoretical synthesis of both has been done and will be explained further in the next chapter. This study will give us some ideas of the maximum frequency that each solution can reach for the digital part.

We could think that the CORDIC solution needs less area than the LUT solution as this latter uses tables taking up area on the circuit. But, unfortunately, the normalization function of the angle puts limits on the working frequency of the solution. Simulation using ModelSim software with a synthesized circuit gave us a clock 8 times slower than the constraints defined by the standard. On that account, we can be confident of the realization of these techniques and they will be explained deeper with a complete synthesis.

2.4 Integration of the Cartesian Feedback on Silicon

The main objective of our study is to realize a single chip with the technology delivered by STMicroelectronics. It remains a good challenge for an IC to consider the stability issue without increasing consumption or area, advantages given by the Zero-IF architecture.
The two following examples taken from recent study [55, 56] illustrate the improvement of the Cartesian Feedback technique.

Automatic Phase Correction

On his thesis [55], J. L. Dawson realized a Cartesian Feedback in 0.25µm CMOS technology from National Semiconductor. This solution has an automatic phase corrector which is presented in Figure 2.19.

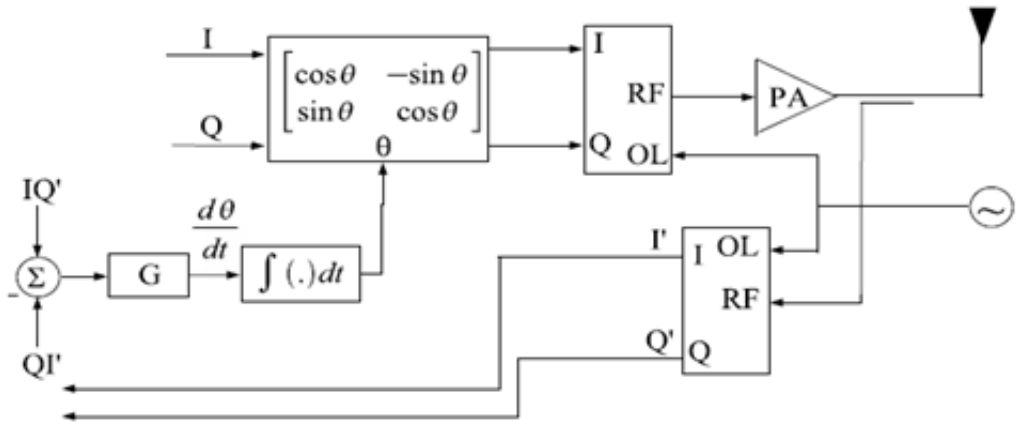


Figure 2.19: Automatic phase correction using a Cartesian Feedback

The goal of phase correction is to multiply I and Q signals by a matrix of circular rotation with an angle θ. The phase error θ is defined by the successive integration of the term IQ'-QI', where

I and Q are quadrature signals of the direct path and I' and Q' are quadrature signals of the feedback path. This correction requires the knowledge of the magnitude of the signal in order to adjust the gain of the integrator.

Moreover, if the gain of the integrator is fixed, the method will work only with constant envelope modulation.

WCDMA Transmitter from STMicroelectronics

The Cartesian Feedback is applied to the last stage of the heterodyne transmitter for the W-CDMA standard [57]. The circuit was realized in 0.8µm BiCMOS technology from STMicroelectronics and has a die area of 4mm². This work presents results in a linearization bandwidth of 60 MHz, and an ACLR improvement of 24dB at 5MHz from the RF carrier.

The phase-shifting introduced by components of the loop is compensated by adjustments on the LO signals (LO_I^* and LO_Q^*) of the feedback demodulator (Cf. Figure 2.20).

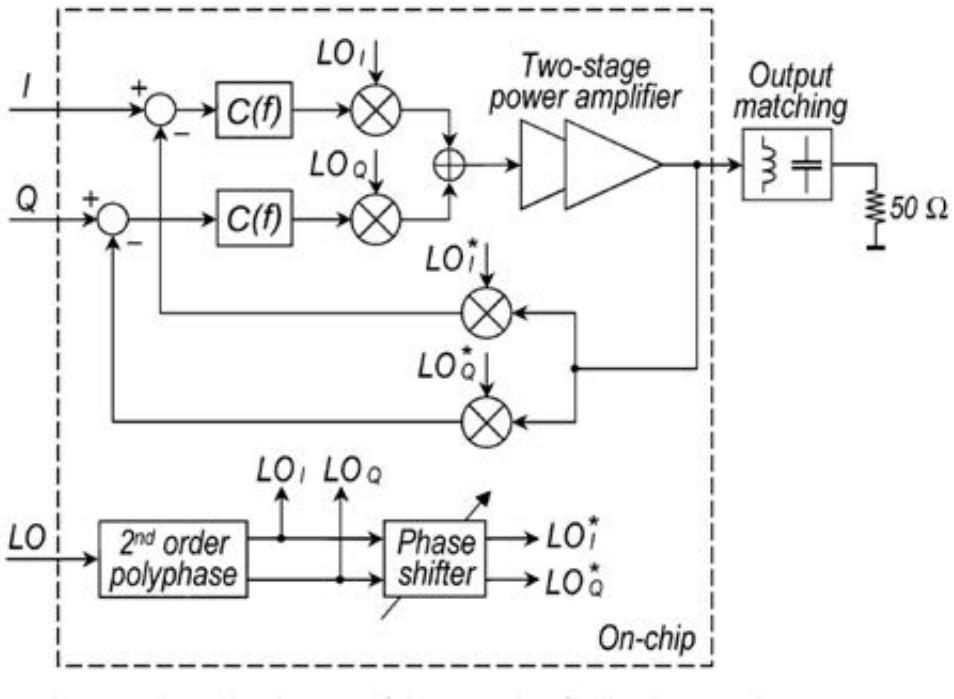


Figure 2.20: Heterodyne transmitter using Cartesian Feedback loop for W-CDMA standard

The settings of LO_I^* and LO_Q^* signals are performed using external voltage supply as shown in equations 2.35 and 2.36.

$$LO_I^* = k.\left(V_A.LO_I + V_B.LO_Q\right) \tag{2.35}$$

$$LO_Q^* = k.\left(-V_B.LO_I + V_A.LO_Q\right) \tag{2.36}$$

These examples demonstrate how the Cartesian Feedback can improve the linearity with different architectures. Our study presents a different approach of the linearity correction using the same principle.

2.5 System Level Behavior

The design of any electronic circuit has to pass through a first step called system level behavior. This step consists essentially in to fix characteristics of all building blocks of the circuit (transmitter, receiver or transceiver). ADS software from Agilent was used in order to have a first idea of the components' properties in this study of the Cartesian Feedback.

We performed simulations on the system level with different power amplifier designs to perform entire simulations of the mixed system at a transistor level.

The first analysis was a simulation using an ideal power amplifier from the library of ADS to validate our innovative approach. Its properties have a gain of 15dB for a saturation output power of 23dB and a compression power of 21dB. This latter value has been chosen with the purpose to be close to the saturation value in order to get more interference.

The second experiment was the test of this ideal Cartesian Feedback based on a power amplifier designed in BiCMOS7RF from IMS Laboratory [58]. This power amplifier has been simulated and measured with a gain of 25dB and a saturation power of 33dBm. The compression point is equal to 31dBm for a corresponding PAE of 20%.

Finally the third and last analysis used the Cartesian Feedback with power amplifier in 65nm CMOS technology [59]. Thereby, the final goal is to integrate the overall architecture on this technology.

All these simulations will be explained on the following part to show the evolution of the parameters of each block for the improvement of the Cartesian Feedback. A study that remains critical as it will determine the architecture to be used before the design of the CMOS chip.

2.5.1 System level behavior of the Cartesian Feedback according to the state-of-the-art

Figure 2.21 shows the simulated system behavior performed with ADS of the Cartesian Feedback. This schematic is composed of low-pass filters, up-conversion mixers, a power amplifier and a coupler for the direct path, and an attenuator, a splitter, down-conversion mixers, and low-pass filters for the feedback path. The correction of the system is made by an ideal phase shifter and a subtractor.

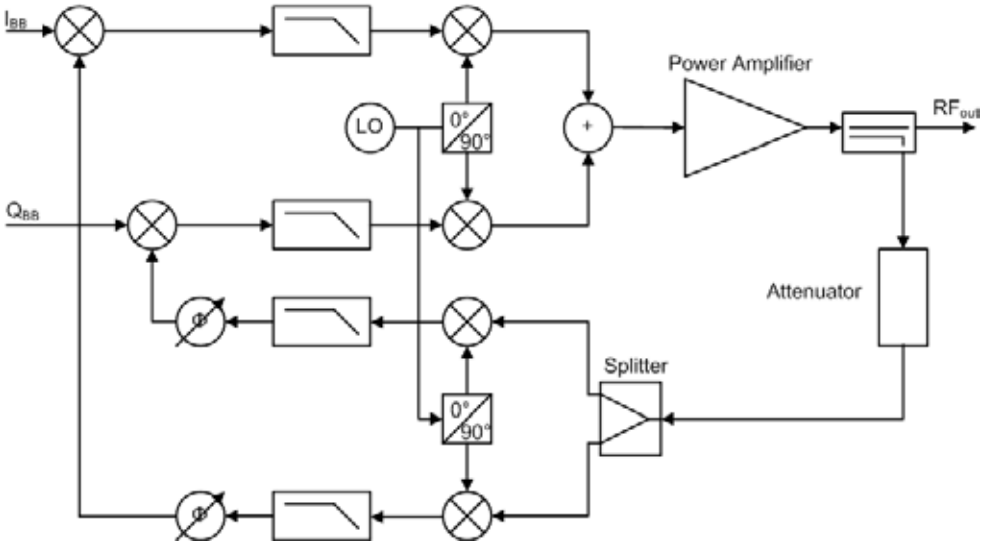


Figure 2.21: Cartesian Feedback technique

Table 2.1 shows parameters that we used to perform the simulation with ADS. In order to perform it, we used the parameters found in the state-of-the-art for each building block. As it is noticeable, the specification is not very aggressive but helps to give us a first idea of the improvement that the system will be able to reach.

Building blocks	Simulation Parameters
Active up-conversion mixer	Gain = 14dB & NF = 6.4 dB
Passive down-conversion mixer	Gain = -8 dB & NF = 8.4 dB
Active filter of the direct path	Second-order Butterworth low-pass, Cut-off frequency = 7 MHz
Passive filter of the feedback path	Third-order Butterworth low-pass, Cut-off frequency = 7 MHz
Attenuator	Insertion loss = 6 dB
Power Amplifier in 65nm CMOS	Gain = 15 dB Psat = 23 dBm & OCP1 = 21 dBm

Table 2.1: Blocks parameters of the Cartesian Feedback architecture

This first experiment gave the output spectrum of the power amplifier without and with the linearity correction using the Cartesian Feedback (illustrated in Figure 2.22).

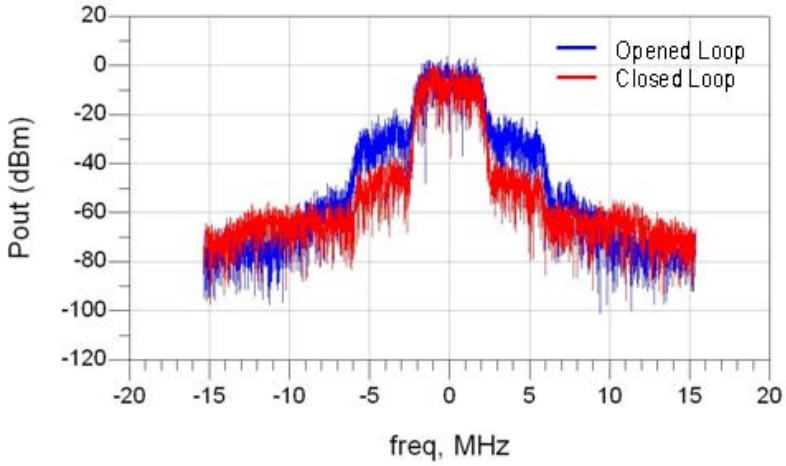


Figure 2.22: Spectrum with and without linearization

	ACLR @ +/- 5MHz from the carrier
Open-loop	- 25.1 / - 26.1 [dBc]
Closed-loop	- 40.7 / - 41.8 [dBc]

Table 2.2: Power on the adjacent channel with and without Cartesian Feedback

A W-CDMA signal was used for almost all simulations showing the behavior of the Cartesian Feedback with a real signal. Moreover, this modulated signal gave us results as we saw previously like the ACLR, the EVM, or the constellation of the standard. The improvement at 5MHz from the carrier is almost 16dB for an output power of 22dBm from the power amplifier, as it is illustrated in Table 2.2.

2.5.2 System level behavior of the Cartesian Feedback using a power amplifier in BiCMOS7RF technology

After encouraging results, we decided to simulate the system with a PA designed at the IMS Laboratory of Bordeaux [58]. The technology is different from our final integration objective in 65nm CMOS technology, but it helped us to observe more phenomena like the constellation, the phase-shifting and the ACLR curves.

The power amplifier was designed in BiCMOS7RF from STMicroelectronics (Figure 2.23). This technology is mainly dedicated to RF applications (cellular and wireless device; e.g. WiFi)

because of its performance and its cost.

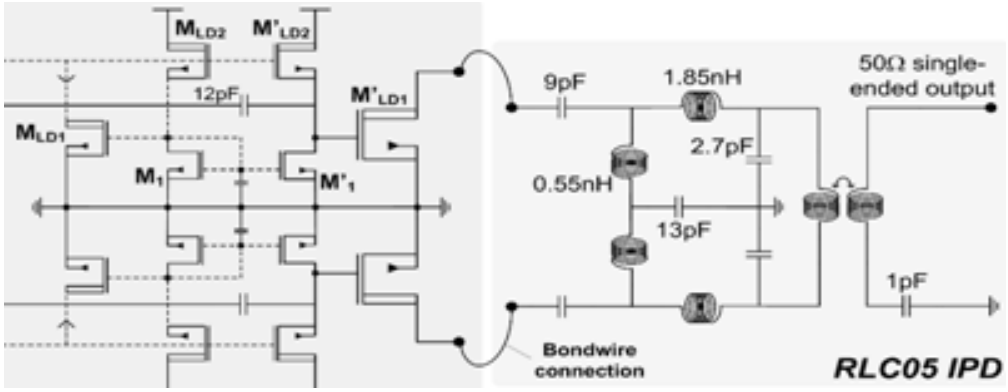
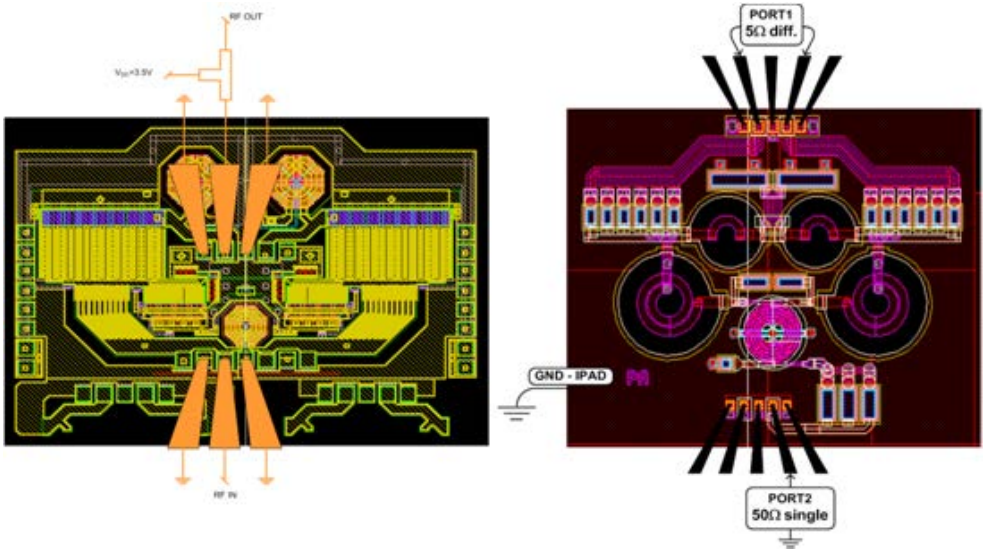


Figure 2.23: Schematic of the BiCMOS7RF power amplifier

For transmitter or receiver applications, this technology permits the use of components such as MOS/LDMOS and heterojunction bipolar transistor (HBT). Therefore, this technology offers advantages for two types of transistor:

- High operating frequencies and low noise factor for bipolar transistors; and
- A strong integration capability with a low consumption of MOS transistors. Moreover, LDMOS maintains easily a high output power on the operating frequency band.

The power amplifier is composed of two differential stages with nLDMA (laterally doped MOS).



(a) (b)

Figure 2.24: Layout of (a) the power amplifier and its (b) associated IPD

The matching network of the PA is off-chip and is implemented on a glass substrate (IPD technology process of STMicroelectronics, Cf. Figure 2.24). This particular substrate has as an advantage to limit its conversion loss, leading to a better efficiency.

This PA has already good linearity performance because it is able to dynamically adjust its output power according to its input power. This adjustment has an objective to decrease the consumption of the power amplifier and to enhance the PAE at low and medium power levels.

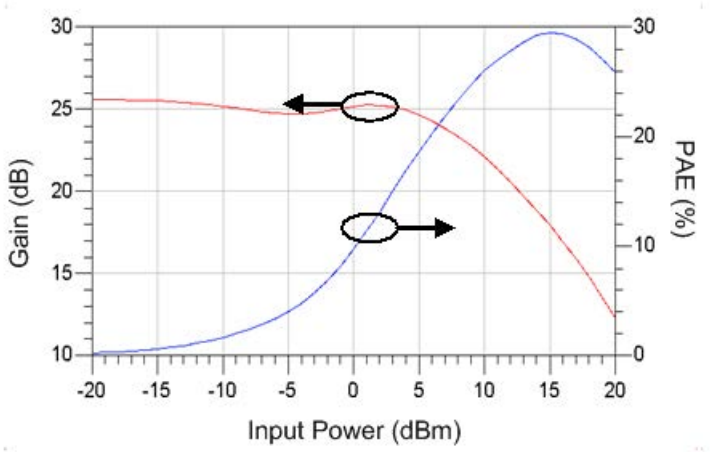


Figure 2.25: Gain and efficiency of the PA according to the input power

The power amplifier at the operating frequency has a gain of 25dB. Figure 2.25 shows the evolution of the gain and the efficiency of the power amplifier according to the input power. The saturation power of the PA is 33dBm for a compression point of 31dBm.

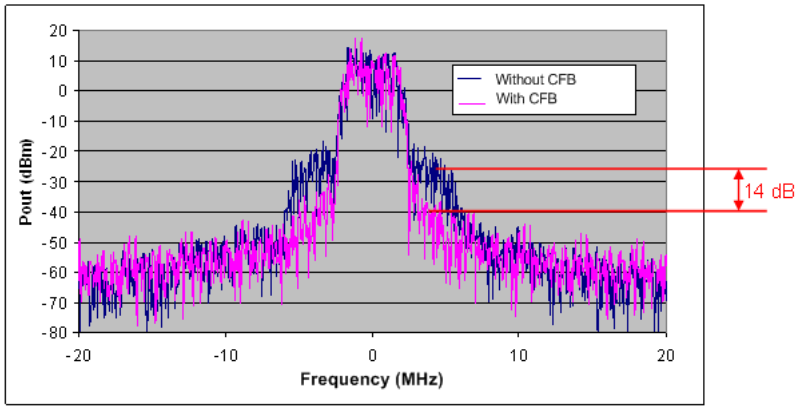


Figure 2.26: Spectrum with and without CFB

As a result, we can observe the spectrum with and without linearization technique in Figure 2.26. This result has already been observed in the previous part and confirms the theoretical study of the Cartesian Feedback [60].

The improvement of the linearity can also be observed with the EVM of the output signals. As explained in 1.4.4.5 Cartesian Feedback, the signal at the input of the power amplifier is predistorted. Nonlinearities given by the PA added with the errors signals (predistorted signals) are compensated and produce a linearized signal after the power amplifier. This phenomenon is illustrated in Figure 2.27 with the input signal of the power amplifier (left constellation) and with the output signal of the power amplifier (right constellation). The improvement of the EVM is equivalent to the ACLR improvement previously mentionned, where the right constellation represents a linear behavior of the power amplifier. From this result, the linearization of a power amplifier designed in transistor level is proved and can lead to a new simulation with another PA designed in our target technology.

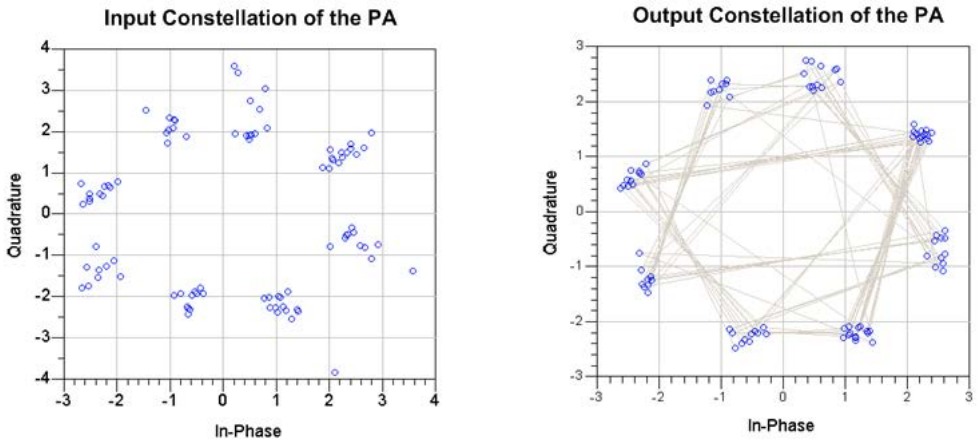


Figure 2.27: Input and output constellations of the power amplifier

2.5.3 System level behavior of the Cartesian Feedback using a power amplifier in 65nm CMOS technology

In this experimentation, a power amplifier designed in 65nm CMOS technology from STMicroelectronics was used (Cf. Figure 2.28).

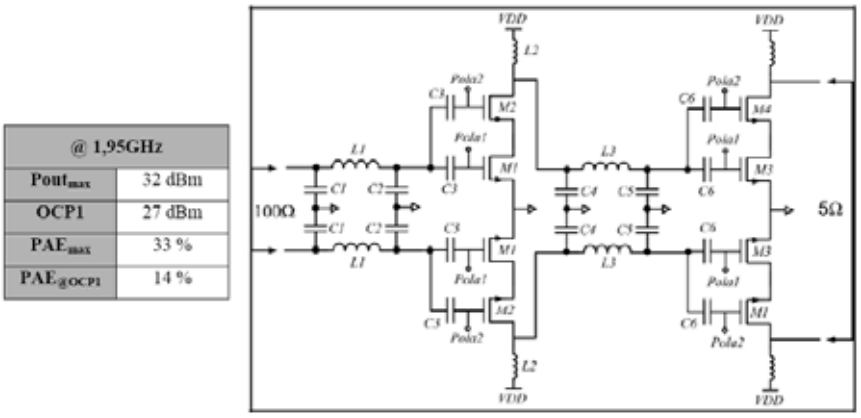


Figure 2.28: Schematic of the 65nm CMOS power amplifier

The power amplifier has been designed at the IMS Laboratory of Bordeaux in 65nm CMOS technology [59]. A simplified topology of the half Stacked Folded Fully Differential Structure (SFFDS) is presented in Figure 2.29, which is inspired by a push-pull structure. A high output power will result from this structure, even if a miniaturized technology is used. The two stacked transistors (M1 and M2) are in phase but biased with a different voltage. The drain degeneration is ensured by bonding and MIM capacitors (C1 and C2) are employed for coupling.

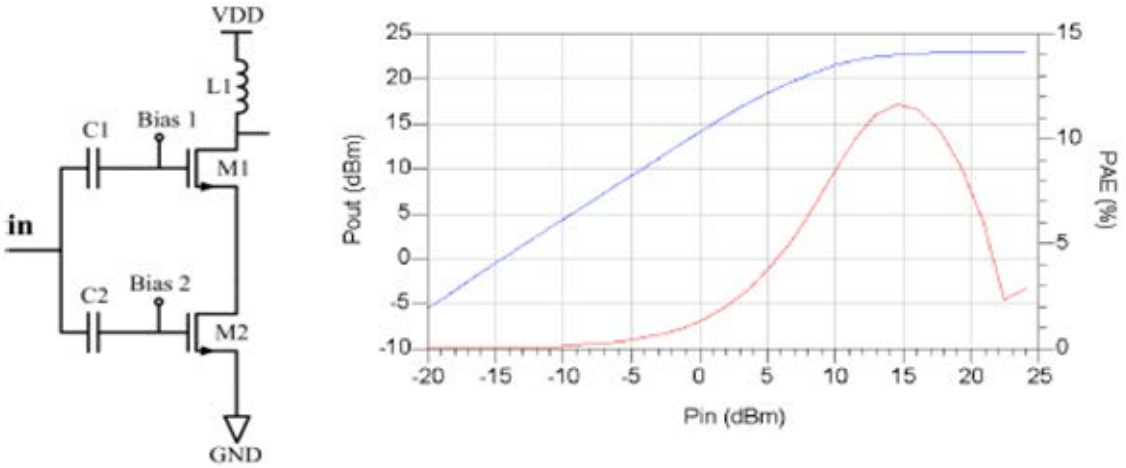


Figure 2.29: SFFDS structure and PA performance associated

At 1.95GHz, the power gain of the power amplifier is equal to 15dB. Figure 2.29 depicts the power gain and the PAE according to the input power. It offers a saturation power of 23dBm with an output compression point (OCP1) of 21dBm. These signal characteristics fulfill the W-CDMA standard (21dBm at 1.95GHz – Class 4) in terms of output power and operating

frequency.

Table 2.3 shows the improvement of parameters for each building block used from ADS simulation to Cadence simulation. These new parameters will lead naturally on new results in ACLR improvement, gain and architecture that will be used.

Components	ADS simulation	Cadence simulation
Active up-conversion mixer	Gain = 14dB & NF = 6.4dB	Gain = 16.3dB & NF = 14.2dB
Passive down-conversion mixer	Gain = -8dB & NF = 8.4dB	Gain = -4dB & NF = 14.6dB
Active filter of the direct path	second-order Butterworth low-pass, Cut-off frequency = 7MHz	third-order Leap-frog low-pass, Cut-off frequency = 8MHz
Passive filter of the feedback path	third-order Butterworth low-pass, Cut-off frequency = 7MHz	first-order Bypass, Cut-off frequency = 8MHz
Attenuator	Gain = -6dB	Gain = -12dB (easily variable)
Power Amplifier in 65nm CMOS	Gain = 15dB Psat = 23dBm & OCP1 = 21dBm	Gain = 13.2dB Psat = 32dBm & OCP1 = 27dBm

Table 2.3: Block parameters of the Cartesian Feedback architecture

The ADS simulation part is taken from the previous table made in the theoretical part according to the state-of-the-art. From this previous table, we can notice changes on several components. Simulations performed with Cadence on components taken from the 65nm CMOS library of STMicroelectronics show different results in the architecture and its performance. It brings to our study new results and the adjustment of parameters. Moreover, the attenuator becomes now variable giving a dynamic feedback path.

As results, a simulation of the power of the adjacent channel is shown in Figure 2.30. In order to make the comparison and evaluate the efficiency of the technique, ACLR simulation has been done with and without Cartesian Feedback. Figure 2.30 shows that the power amplifier is out of the specifications given by the standard for an output power greater than 28dBm. However with the Cartesian Feedback, the maximum output power reached by the system is 31dBm. The gain of this output power can be translated as lighter specifications on the power amplifier to get a power amplifier available for all classes of the specified standard [61].

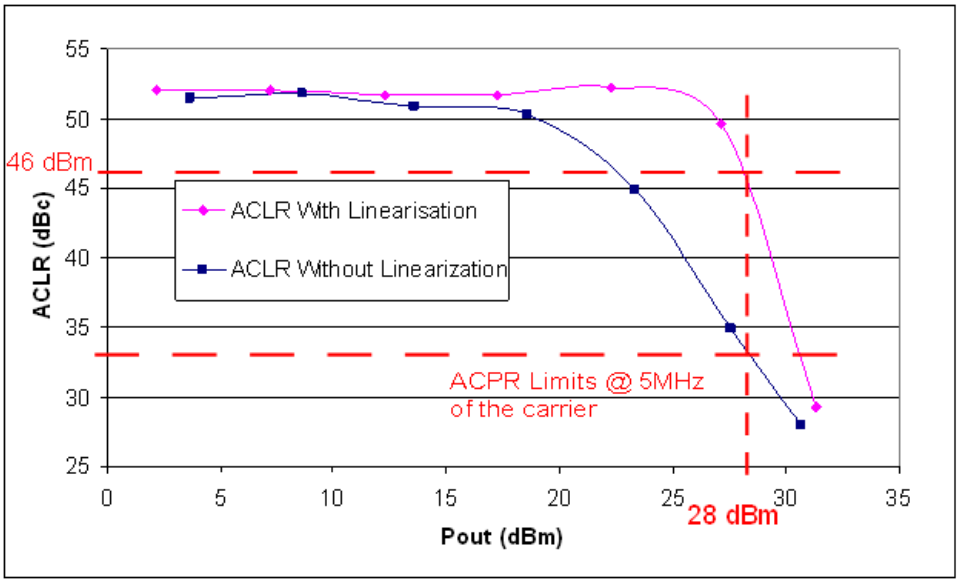


Figure 2.30: ACLR improvement with and without Cartesian Feedback

2.6 Conclusion

In the literature we can find the Cartesian Feedback architecture using exclusively analog circuits [34, 33]. In our case, we proposed to split this architecture in two parts: analog and digital. The analog part allows us to decrease the consumption and the die area, to realize the frequency conversion and to amplify the signal. Moreover, the digital part realizes the phase-shifting and the subtraction of signals coming from the direct and the feedback paths, with the main advantage that the correction is dynamical whatever is the response of the output of the transmitter.

Before the realization of the integrated circuit, we have to be aware of limitations and cares that must be taken into account when using the Cartesian Feedback. We must be sure that the system is stable, furthermore, that this architecture will not generate noise and will not degrade the linearity of the circuit. Regarding the drawbacks of the Cartesian Feedback, we have to deal with a limited bandwidth and the implicit effects of the pulling and the DC offsets. Therefore, mathematical representations were used to illustrate these limitations and cares.

Another point clarified was the real-time constraint of the digital part linked to a frequency higher as possible. We explained two solutions for it, the CORDIC algorithm and the LUT with their advantages and drawbacks.

For the digital part, we opted to use an ASIC integration whilst different solutions were illustrated on [55, 56]. These two publications exploited two ways to improve the linearity of the Cartesian Feedback. One applied a more mathematical approach with CMOS technology using only constant envelope modulation but our targeted application uses a non-constant envelope modulation. The other employed an analog technique using the Bi-CMOS technology with our targeted standard having a die area of $4mm^2$ and an ACLR improvement of 24dB at 5MHz from the RF carrier.

Nevertheless, before the realization of the overall integrated circuit, we must follow its characterization through different phases, from an ideal system to a more realistic transmitter. Thereby, we performed system simulations to determine the specification of each building block in the architecture. We will detail each building block in the next chapter.

Chapter

3

A Fully Integrated Transmitter Using a Digital/Analog Cartesian Feedback

Contents

This chapter presents the integration of the analog and digital Cartesian Feedback described previously in 65nm CMOS technology from STMicroelectronics.

First, the digital part generating the phase correction and subtraction will be shown in ASIC technology, with a CORDIC algorithm to reduce its consumption and size. The choice of this algorithm will be explained regarding the advantage of being more flexible than a classic algorithm based on LUT (Look-Up Table). Moreover, constraints (as frequency, latency...) will be described and the implementation of the digital part in VHDL (Very High Speed Integrated Circuit Hardware Description Language) from its description until the layout will be presented.

Secondly, the architecture and specification of building blocks will be shown. In our case, as presented before (Cf. Chapters 1 and 2), the direct path is composed of filters, RF modulator and a Power Amplifier. Our objective is to design these three functions to minimize the consumption and the silicon area of the integrated architecture. Moreover, we do not need to take into account the constraints in noise and in the linearity of the building blocks of the direct path because they will be improved by the Cartesian Feedback itself for the whole system. Nevertheless, for the feedback path, precautions have to be taken regarding the linearity and the noise to prevent distortion of the feedback signal. Moreover, unlike a classic system as the Zero-IF transmitter, our architecture has a feedback path which will not increase greatly the consumption and the silicon area, as it will be shown.

Finally, system level simulations will be presented using the ADS (Advanced Design Software) from Agilent for the analog part. Co-simulations have been done to analyze the whole system, with SystemVue for the digital part. The simulations using ADS will provide the performance of each building block on the transistors level. However, to reduce the time of simulations, some hypotheses had to be considered on the closed-loop mode where only converters (ADC and DAC) are not included in such co-simulations.

Also, a comparison with the state-of-the-art will be shown answering the needs of manufacturers in terms of consumption and silicon area, improving the linearity.

3.1 A Digital Solution for the Phase Alignment and Subtraction

In this part, we will focus on the synthesis algorithm and the ASIC integration of the digital part (Cf. Figure 3.1) for the Cartesian Feedback transmitter. Different steps have been realized from the RTL code to the final layout and were applied both to the LUT and CORDIC architectures.

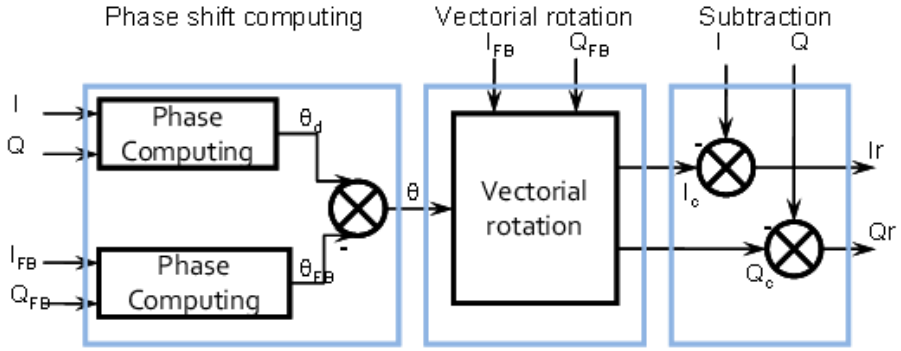


Figure 3.1: Synoptic of the digital part

3.1.1 Synthesis and implementation in 65nm CMOS technology

To be able to get the final synthesis of the digital part, three points have to be considered beforehand to accomplish the final circuit on ASIC technology (Cf. Figure 3.2):

- To check the HDL code to synthesis. This code has to be optimized and can not have heavy tables (e.g. LUTs technique). The number of registers used has to be controlled in order to not increase the dynamic consumption of the solution.
- To choose the technology responding to the constraints given by the customer. In our case, the technology is the 65nm CMOS technology. The selected technology has to insure that it fits with constraints given by the HDL code.
- To specify input/output delays, raising/falling times, giving all constraints allowing the synthesis of the HDL code.

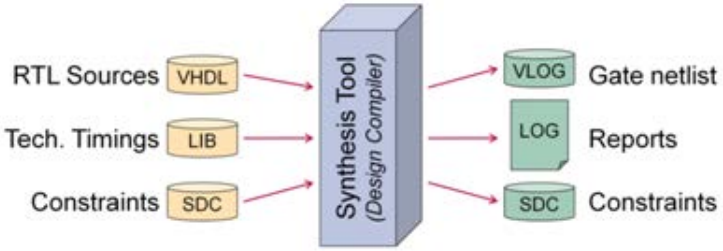


Figure 3.2: Graphical illustration of the synthesis tool

The ASIC synthesis and the mapping have been made with, respectively, Design Compiler tool from Synopsys and Cadence Encounter tool.

The synthesis of the digital part can be done in three steps:

- First, an analysis of the digital code is made with relaxed constraints where a long time period is chosen in order to check if the design is synthesizable or not.

- For the second step, an incremental synthesis is used, taking the previous result into account. This second analysis has as an objective to optimize the first step to get the optimal time period of the digital code.

- The final step performed a new incremental synthesis with severe constraints and an optimal period is found according to the second step.

3.1.1.1 Synthesis with relaxed constraints

The analysis with relaxed constraints has been performed with Synopsys software. This tool generates first Boolean equations from the RTL program, describing the design on the register levels (Cf. Figure 3.3).

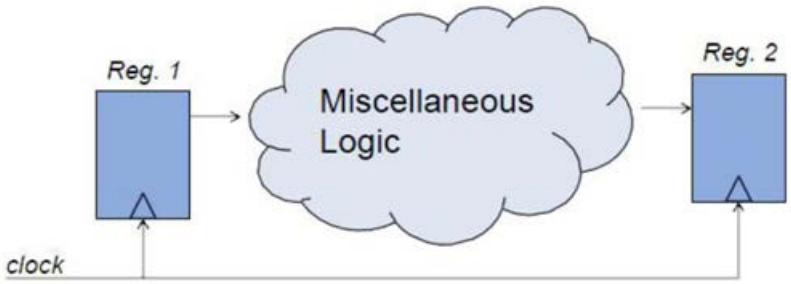


Figure 3.3: Register level descriptions

Hence, the compiler translates these Boolean equations in a logical circuit according to the technology used. The gate of transistors is not ideal and needed to include a response delay to approximate the behavior of an ASIC circuit.

In order to have a synthesizable design, the sum of delays generated by every logical gate on the critical path had to be less than the specified period for the synthesis (Cf. Figure 3.4).

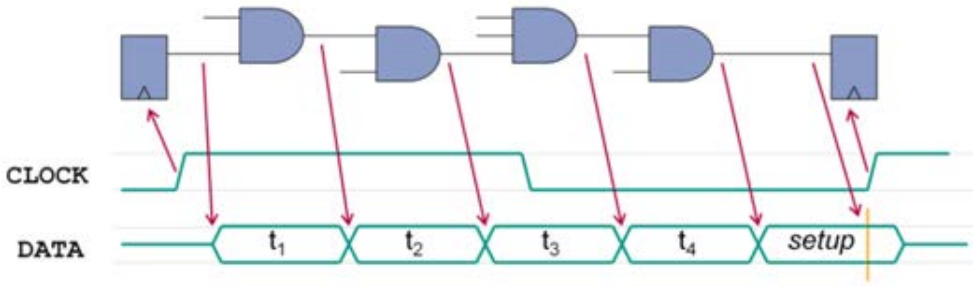


Figure 3.4: Time-driving step

At the end of the synthesis, an information file is generated on the slack time of the system. If the value is negative, the design or the constraints have to be modified. A positive value enables us to optimize the design using high frequencies constraints.

The synthesis with relaxed constraints consists in to use a chosen period (in our case, the period is 100ns). The maximal period reached by the system is the difference between the specified period and the slack time.

	Area (µm²)	Whole consumption (µW/MHz)	T_{min}(ns)	F_{max}(MHz)
LUT based	32100	130.9	63.5	15.7
Mixed CORDIC	30800	7.49	8.3	120.5
Pipelined CORDIC	33900	5.92	5.6	177.9
Non-pipelined CORDIC	17400	8.46	18.6	53.8

Table 3.1: Results of the relaxed constraints synthesis

According to Table 3.1, we observed that the synthesis needs 63.5ns for the solution based on LUTs. This did not allow us to have a high frequency compared to the pipelined solution. The pipelined solution can reach high-operating frequency, but it occupies the largest die area (Cf. Table 3.1). The mixed solution is able to reach a frequency of 120.5MHz, for a die area inferior to the solution based on LUT.

The synthesis tool did not optimize the entire design because the specified period is high (100ns) if we compare to the time period specified in the previous table. But, in the following point, the incremental synthesis will present results with a specified period of 15.4ns (reduction of 84.6% on the synthesis period).

3.1.1.2 Incremental synthesis

Results of the incremental synthesis are summarized in Table 3.2. The LUT-based solution remains synthesizable with a period of 15.4ns. Maximal frequency can be reached until 178MHz for the mixed solution and 291MHz for the pipelined solution.

	Area (µm²)	Whole consumption (µW/MHz)	T_{min}(ns)	F_{max}(MHz)
LUT based	53500	32.9	15.4	64.9
Mixed CORDIC	37800	17.6	5.6	178
Pipelined CORDIC	35900	23.1	3.4	291
Non-pipelined CORDIC	41900	26.4	5.8	172

Table 3.2: Results of the incremental synthesis

The only drawback of the incremental synthesis is that the compiler may no longer understand the logic circuit generated. Every time that we increased the frequency, the incremental synthesis optimized the circuit generated from the previous synthesis and updated the report. In order to obtain an explicable result, the synthesis must be made again with the same constraints used for the incremental synthesis.

3.1.1.3 Synthesis with severe constraints

Increasing the operating frequency once more, the LUT-based solution became non-synthesizable. The maximal frequency that the system reached was 65MHz. However, the mixed CORDIC solution gave a frequency up to 200MHz with a die area smaller than the LUT-based solution and the Pipelined CORDIC solution. These results are shown in Table 3.3.

	Area (µm²)	Whole consumption (µW/MHz)	T_{min}(ns)	F_{max}(MHz)
LUT based	53500	32.9	15.4	64.9
Mixed CORDIC	44600	19.2	4.3	233
Pipelined CORDIC	51500	28.6	2.5	400
Non-pipelined CORDIC	42500	26.8	5.8	172

Table 3.3: Results of the severe constraints synthesis

Based on these results, we can assume that a study targeting a FPGA device will be inconclusive. Tables used for the LUT solution will be replaced by logical connections. Increasing theses connections, the number of transistors will be increased and, as a consequence, the die area of the system and the consumption will also be significantly raised.

For our application, the mixed solution has to be used for three reasons. First, this architecture does not need pre-computed tables and thus the consumption will be increased according to the desired operating frequency. Then, the solution can reach a maximal frequency of 232.6MHz which fits better with the chosen architecture using ADC and DAC working at 240MHz. Third and last, the die area of the mixed solution remains small if we compare to the LUT-based solution: this latter occupies more die area for a frequency lower than 100MHz using 65nm CMOS technology.

3.1.2 Place & route (mapping) of the digital part

After the validation of the previous step, a software called Design Compiler is used. It takes the source code of the LIB file and the result file of the synthesis constraints at the input. At the end of the synthesis, Design Compiler delivers a logic circuit, a report with errors and new constraints making an optimized place & route (Cf. Figure 3.2).

We can distinguish five steps to make an efficient place & route of the logical circuit generated at the end of the ASIC synthesis:

Floorplan: It consists of specifying the die area of the digital part, new constraints, the numbers of layers that the circuit will have and the location of the input/output pins.

Power Grid: A grid has to be placed above the circuit to supply all transistors of the chip.

Place Design: According to the die area given previously, this step has to put all the design of the specified area during the floorplan step.

Tree Synthesis: After the design and the supply of the circuit were put in place, the clock tree can be placed.

Route Design: It is the final step which connects all devices of the entire design together .

3.1.3 Die area of the digital part

After the mapping operation, we can observe the layout of the digital part in Figure 3.5. The results of all these operations can be observed for the LUT and CORDIC techniques. Considering that we chose the same die area for both, we can find the best technique observing the operating frequency and the consumption of the solution (Cf. Table 3.3).

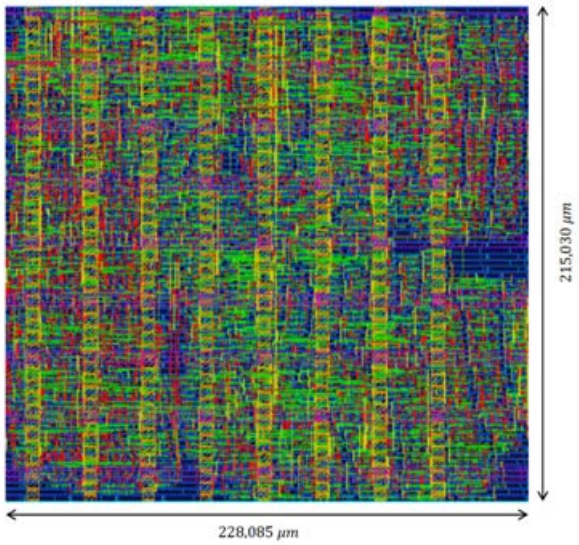


Figure 3.5: Die area of the mixed CORDIC solution

3.1.4 Conclusion of the digital part

Several steps were described to select the best architecture for the ASIC implementation of the digital part. The choice of the divider was validated comparing different digital architectures in accordance with the consumption and the die area. Between the LUT and the CORDIC techniques, a detailed architecture of the CORDIC solution has been presented and selected in conformity with the consumption and the area of the chip reduced by the modified technique.

The comparison of these architectures showed that the mixed CORDIC solution fitted better with the RF linearization technique of a power amplifier.

3.2 Details of the Analog Circuit in 65nm CMOS Technology from STMicroelectronics

As illustrated earlier (Cf. Chapter 1), the analog part of the Cartesian Feedback has two paths, the direct and the feedback path. Converters are used to make the interface between the analog and the digital part. A digital-to-analog converter is used in the direct path and the analog-to-digital converter in the feedback path.

The direct path is composed by:
- Gm-C filter with a variable gain and cut-off frequency.

- Mixers based on Gilbert Cell architecture. They are used to perform the up-conversion and the modulation of the I/Q baseband signals.
- A power amplifier, before the coupler, delivering a maximum output power of 27dBm, permiting to fit with 3 of 4 classes specified by the W-CDMA standard.

The feedback path is composed by:
- A variable attenuator, after the coupler, taken from [62] has been optimized for our application.
- A passive ring mixer to save power consumption and to keep a high bandwidth.
- Filters, after the demodulator, removing intermodulation products resulting from the down-conversion.

This part will detail blocks of the Cartesian Feedback for the direct and the feedback path. It will show the most significant parameters and results that we have to take into account for simulations and the realization of the whole system. All components presented were designed in 65nm CMOS technology from STMicroelectronics. It is important to observe that critical components such as the power amplifier or converters have been already measured before the integration on the Cartesian Feedback.

3.2.1 Digital-to-Analog Converter (DAC)

The architecture used for the digital-to-analog converter is a current-steering architecture, widely used for high-speed applications. It has the advantages of easy implementation, a good matching, and a fast response of the conversion [63, 64]. Figure 3.6 shows the classic current-steering DAC architecture.

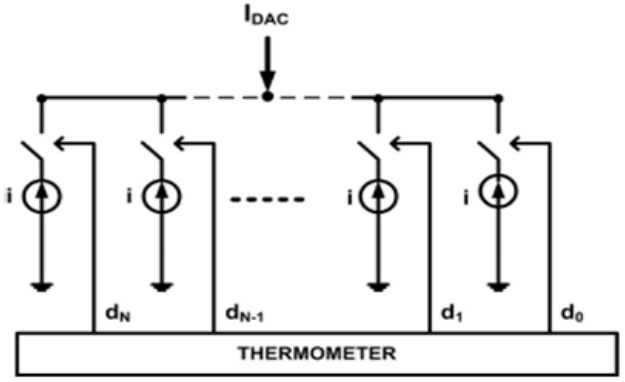


Figure 3.6: General unit-element current steering DAC

The converter is composed of an array of unit-element reference current sources. Every branch

of the DAC has the same reference source, and each branch current is switched ON or OFF depending on the input code. The main drawback of this architecture is the die area. For a unit-element DAC, 2n current sources are required to generate an accurate output signal. To resolve this limitation, a combination of binary and unit-element current-steering has been used to increase the resolution and the linearity.

Table 3.4 shows performance of the converter designed and measured by STMicroelectronics. The converter has differential current output having a full scale current from 6mA to 10mA by setting a proper reference resistor.

	Measurements
Technology	65nm CMOS
DAC resolution	12 bit
INL	+/- 2.5 LSB
DNL	+/-1.8 LSB
Output bandwidth	80MHz
Frequency sample	242MHz
Area	0.476mm^2
Consumption	Analog: 26mW | Digital: 2.5mW

Table 3.4: DAC measured performance

3.2.2 Active filter

The filter used is composed of three-stages (Cf. Figure 3.7) and it has been designed and measured by STEricsson.

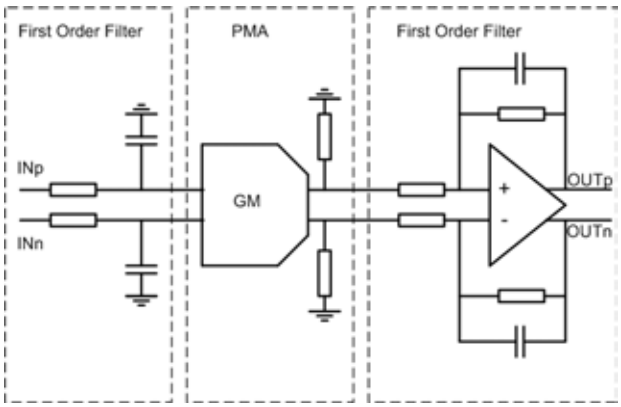


Figure 3.7: Architecture of the active filter

The input stage is a first-order passive filter without tuning frequency capability. This filter has a 3dB cut-off frequency equal to 10MHz. This stage is used to adapt the impedance between the block placed before the filter (the converter or the passive mixer) and the PMA (Pulse with Modulation Amplifier).

The second stage (PMA) is an amplifier designed with linear transconductance in order to increase the in-band linearity. It is the most restricting design because of the linearity and noise constraints applied to the feedback path.

Finally, the last stage is a first-order active filter with a 3dB cut-off frequency equal to 8MHz. This cut-off frequency can be tuned at +/- 10% to ensure the useful signal.

PMA design:

In the analog baseband (ABB) domain, two different transistors are used: the lvtlp (low Vt low power) and the hvtlp (high Vt low power). The inconvenience of the lvtlp is the inability to obtain a design with a large gain as we are using a small Rds value for transistors. Moreover, according to the design rule manual (DRM) of STMicroelectronics, these transistors have a very bad matching for the gate length higher than 0.2µm. For these reasons, we have used these transistors only when it was necessary. Thus, for the PMA design (as shown in Figure 3.8), all transistors have been chosen in hvtlp excepted two transistors, the M2 and M3 for stacking reasons.

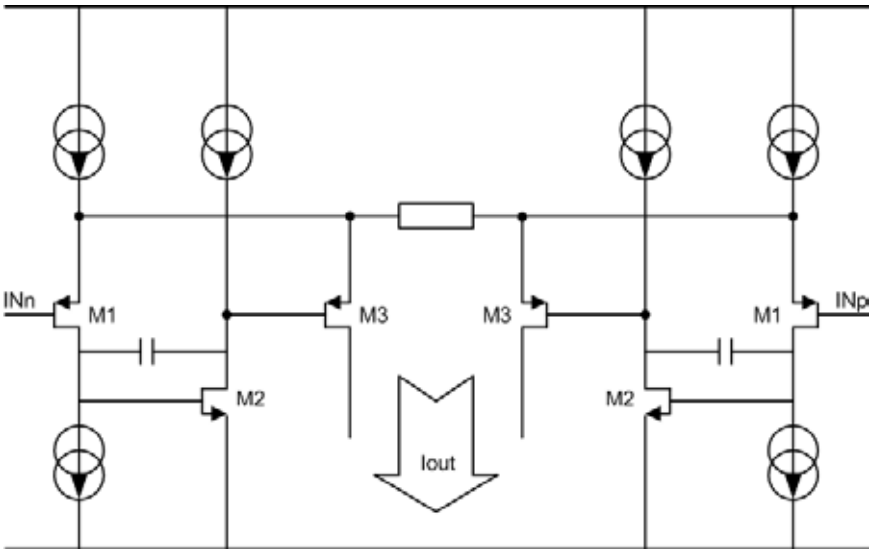


Figure 3.8: Schematic of the PMA

The loop carried out by transistors M1, M2 and M3 is used to control the current through the input transistor M1. This current is the first contributor for the nonlinearity of the PMA. Thereby, to insure the current control for frequencies higher than 20MHz, this loop must have a large gain and a large bandwidth (BW=80MHz).

First-order active filter:
This filter is a classic active filter which is used, on one hand, to select the useful channel and, on the other hand, to cancel the adjacent channel (higher than 10MHz) before the ADC.

For linearity and accuracy gain of the filter, the amplifier must have an efficient unit gain bandwidth (BW=150MHz) and a DC gain (50dB). Moreover, as explained before, the 3dB cut-off frequency can be adjusted at +/- 10% by switching resistors (Rc1, Rc2, Rd1 and Rd2 at the same time).

Figure 3.9 shows different gain delivered by the filter.

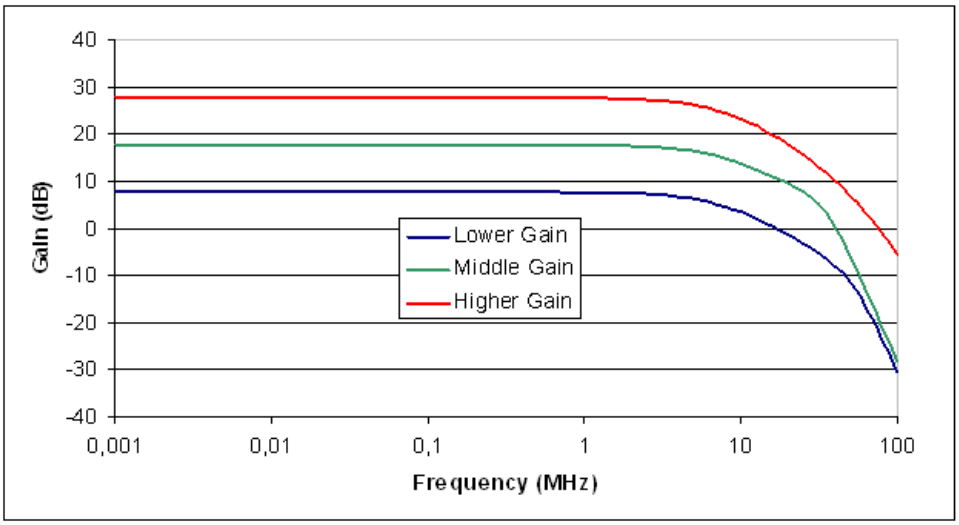


Figure 3.9: Gain of the filter according to the PMA operating mode

The gain of the filter can be controlled by a value at the input of the PMA. The filter can have a gain of 8dB, 18dB or 28dB according to the standard targeted. The cut-off frequency can be seen on the graphic for each gain value, and validate its value compared to our application, which is 8MHz.

Figure 3.10 shows the die area of the active filter used for the direct and the feedback path which is 360x360µm².

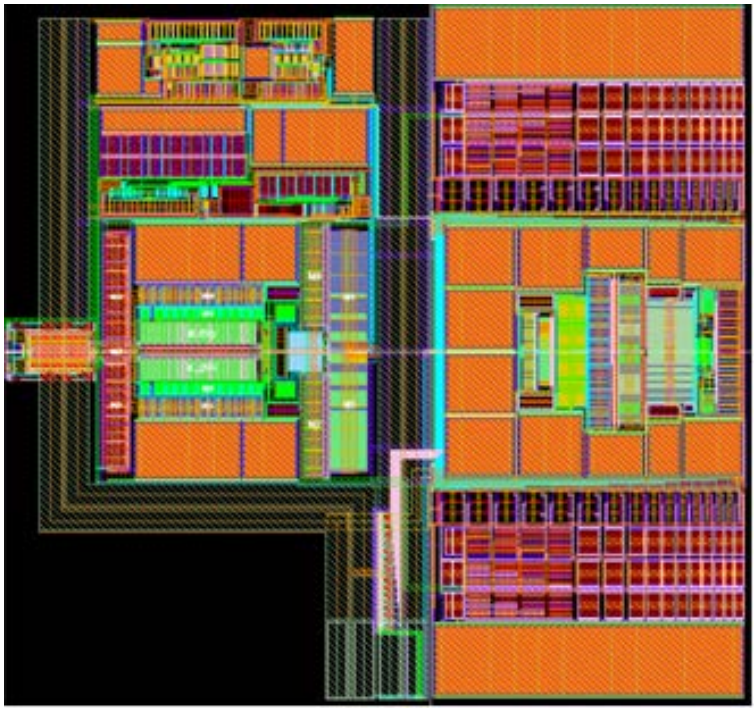


Figure 3.10: Die area of the active filter

3.2.3 Active up-conversion mixer

The up-conversion mixer is used to transpose the information from a low frequency to a higher frequency. In our case, using a Zero-IF architecture, this mixer shifts the information from the baseband to the RF frequency specified by the W-CDMA Standard.

Topologies of mixer can be distinguished as passive or active ones. Passive mixers are used for applications which require good linearity and dissipate no DC current. However, they have no gain and need a large LO signal.

For our application, an active mixer using the Gilbert Cell topology was chosen. This architecture provides a gain to amplify the error signal. The linearity of the mixer is not an issue because the system of Cartesian Feedback will correct nonlinearities.

Figure 3.11 shows the Gilbert Cell mixer designed in 65nm CMOS technology.

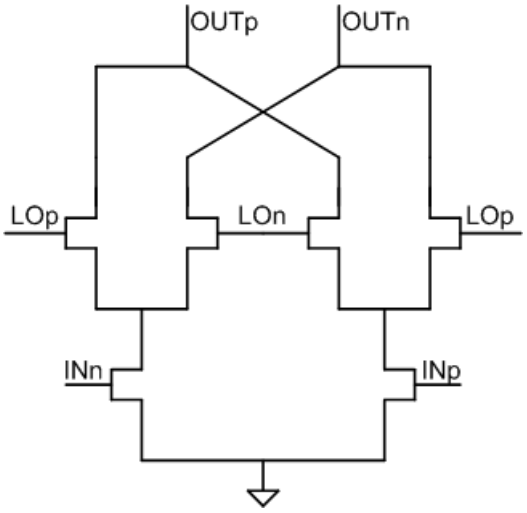


Figure 3.11: Schematic of the Gilbert cell

Figure 3.12 (on the left) shows the evolution of the gain conversion of the mixer according to the power delivered by the local oscillator. This power has been fixed to 0dBm according to the recent literature. It gives a gain of 16dB for the active mixer. Linearity simulation has been done in Figure 3.12 (on the right). Thereby, the mixer gives a gain of 16dB for a maximum output power of 10dBm and a compression point of -17dBm.

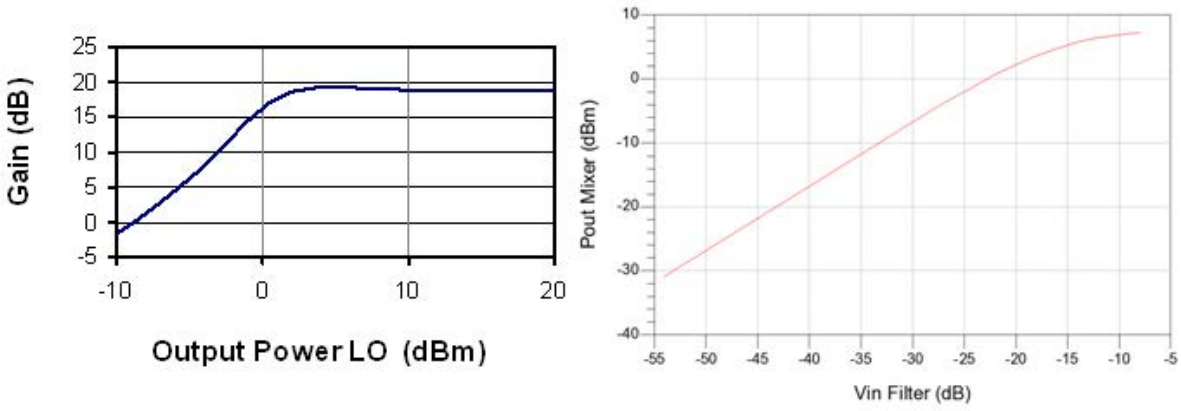


Figure 3.12: Gain conversion and linearity of the active mixer

As Gilbert Cell gives very homogeneous features, it fits perfectly with our application. Its architecture is easy to design and is also reliable as it has been shown previously.

Figure 3.13 shows the die area of the active mixer which is 270x380µm².

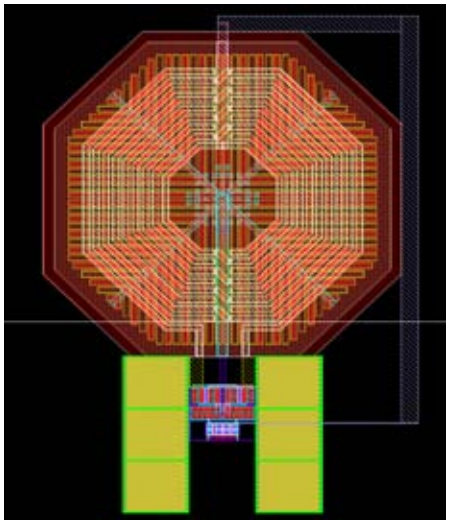


Figure 3.13: Die area of the up-conversion mixer

3.2.4 Power Amplifier (PA)

The power amplifier is made of active and passive components. The active ones, mainly transistors, determine the power amplifier class of operation, whereas the passives ones are used to realize the input and output matching networks.

A simplified architecture of the power amplifier is shown in Figure 3.14. The PA relies on two-stages, a driver stage and a power stage, based on cascode and differential structures. The power amplifier has been designed and measured by STEricsson.

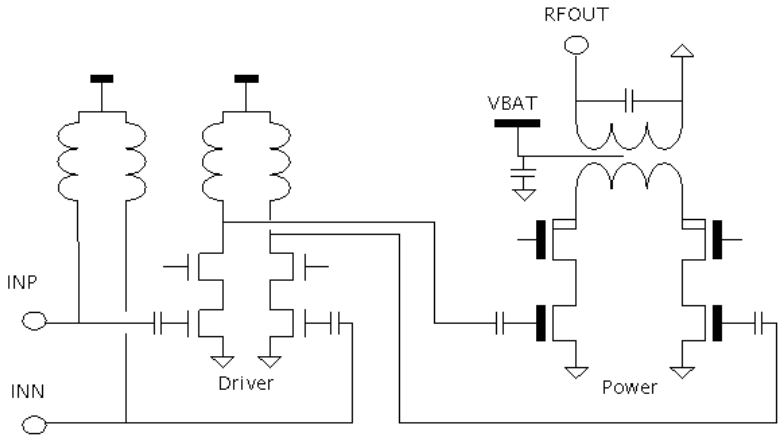


Figure 3.14: Topology of the power amplifier

Figure 3.15 shows the gain and the output power of the PA according to the input power. We can notice that the gain delivered by the PA is 24dB, that it is much more than we expected from the previous study. This major information will show us later that the higher gain will have an effect to make the correction of our circuit more efficient. The error signal will be more amplified and thus the nonlinearity of the signal will be easily compensated.

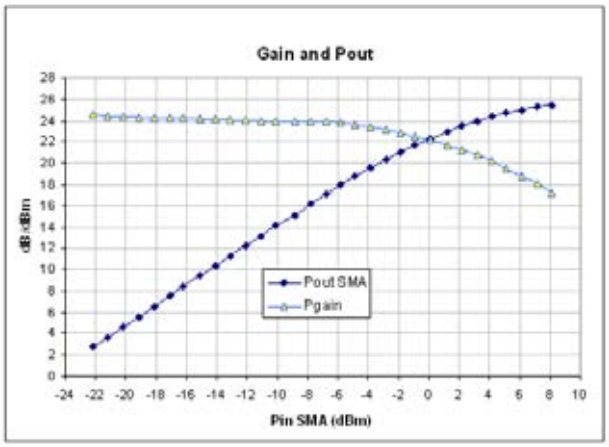


Figure 3.15: Gain and output power of the power amplifier

The consumption of the power amplifier is a crucial factor for the appreciation of the whole solution. We will observe that the consumption of the power amplifier will decide if the transmitter is relevant to make it into a product or not. In our case, we can observe the consumption of the PA in Figure 3.16. The consumption of the driver stage and the power stage called (ldrv for 1.2V supply voltage and Ibat for 3.6V supply voltage respectively) are plotted separately.

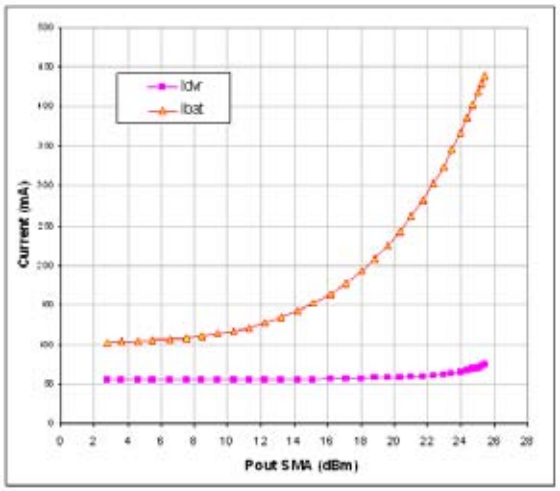


Figure 3.16: Current consumption of the PA

The total die area of the power amplifier is 1.3mm^2 for a consumption of 658.4mW.

The output matching of the power amplifier has been removed from the original circuit to cancel any mismatching phenomena and to reduce the die area of the transmitter. Therefore, the output matching has been realized on the PCB (Printed Circuit Board) as shown in Figure 3.17.

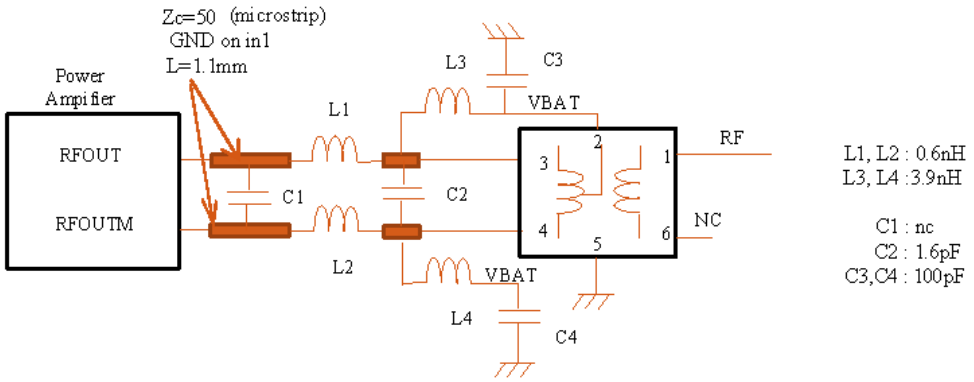


Figure 3.17: Schematic of PCB for the output of the PA

To perform the measurement of the circuit, we had to change the matching of the power amplifier from a differential output to a single output. As illustrated in Figure 3.18 the matching study was performed with Agilent software. The PCB shows that the differential output of the PA is coming from the left side of the power amplifier. Moreover we can see microstrip lines and the place for balun, capacitors and inductors.

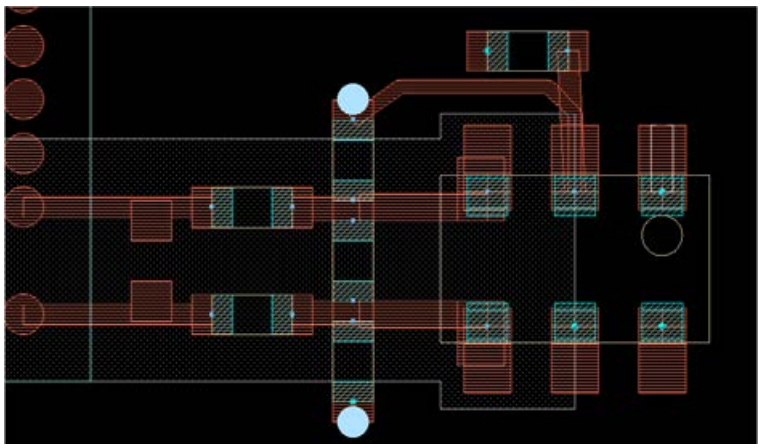


Figure 3.18: Realization of the PCB on ADS

3.2.5 Attenuator

A variable attenuator has been chosen to insure linearity and stability of the feedback path. Figure 3.19 represents the architecture of the variable attenuator [62]. Vctrl and Vmatch are used respectively to control the attenuation level and the input/output matching with the help of a DC feedback loop. The variable attenuator is a two-stage 50Ω equivalent to π-attenuator.

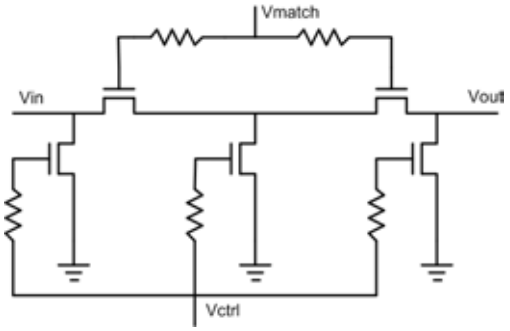


Figure 3.19: Schematic of the designed attenuator

The MOS transistors are used in their resistive region to realize voltage controllable resistors. Resistors at the gate of transistors are used to modulate the gate with the average of drain and source signal amplitudes. This has a consequence of creating a more uniform channel resistance with less distortion [65, 66]. Two π-stages are cascaded to achieve more attenuation for our frequency, which is 1.95GHz.

This attenuator is replicated in this structure and compared to a resistor of 50Ω illustrated in Figure 3.20.

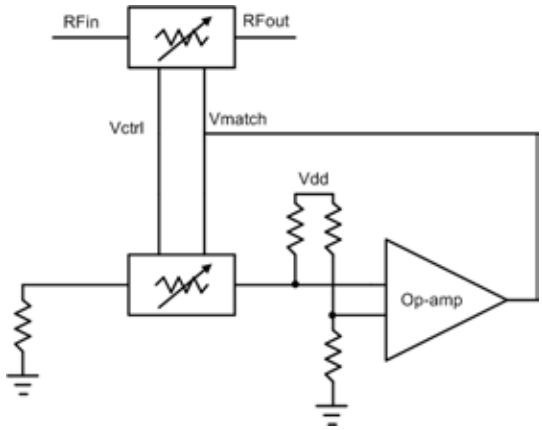


Figure 3.20: Feedback loop for impedance matching

Resistors connected to the gate are removed to reduce the die area of the circuit. As the Vctrl is variable, the equivalence impedance will be no longer 50Ω. Then the feedback path will force series devices to increase or decrease their resistance values. This will happen to compensate the change of the equivalent impedance of the attenuator. Figure 3.21 shows the attenuation varying at the output while the input power stays almost the same according to Vctrl.

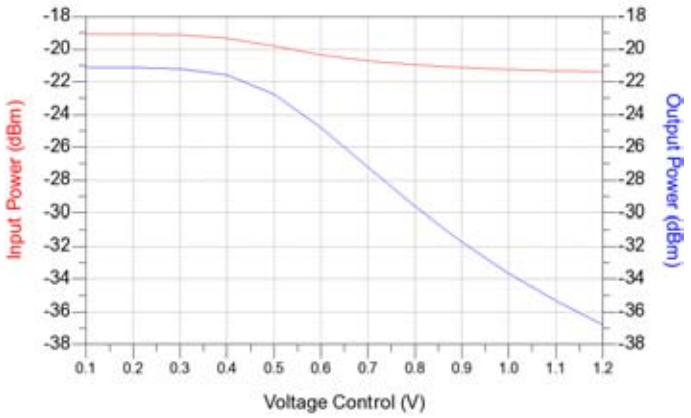


Figure 3.21: Input and output signals variation of the attenuator

The gain of the attenuator can be observed in Figure 3.22 and shows the variation range according to the voltage control. The circuit delivers attenuation going from -2dB to -16dB that will set the attenuation of the whole feedback path and may control the instability of the whole circuit.

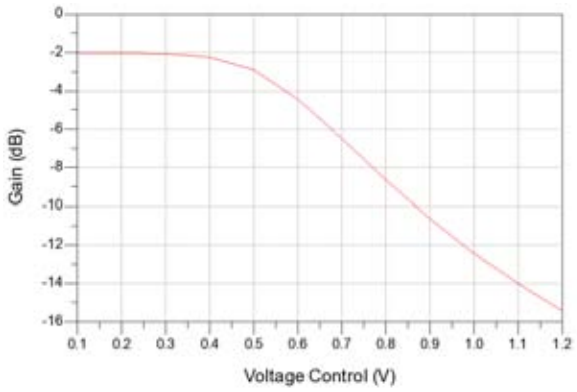


Figure 3.22: Gain according to the voltage control of the attenuator

Parallel devices are chosen to give a value of 50Ω when the control voltage of the attenuator is set to 1.2V. The voltage control drives the shunt devices (transistors) which are completely turned off for the minimum attenuation value. It improves the minimum insertion loss of the

attenuator. The gain of the attenuator is given by:

$$A = \left(\left(R_{shunt} - 50 \right) / \left(R_{shunt} + 50 \right) \right)^2 \tag{3.1}$$

where R_{shunt} is inversely proportional to the voltage control value (Vctrl).

Figure 3.23 shows the block diagram of the attenuator.

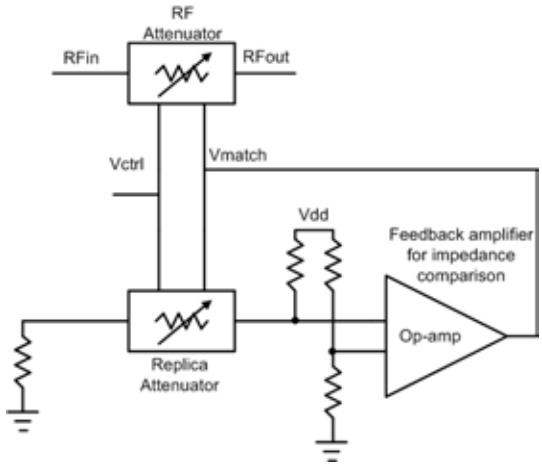


Figure 3.23: Whole topology of the attenuator

Finally, Figure 3.24 shows the layout of the attenuator with a die area equal to 71 x 63 µm².

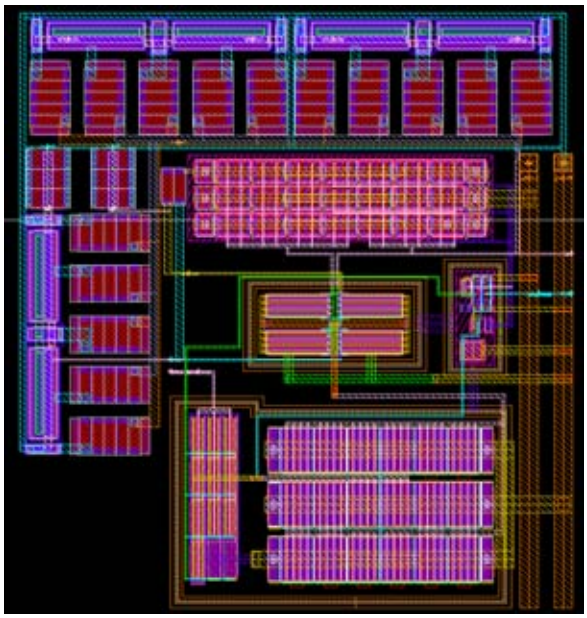


Figure 3.24: Die area of the attenuator

Table 3.5 resumes performance of the attenuator.

Operaiting frequency	1.95GHz
Minimum attenuation	-2dB
Attenuation range	16dB
Insertion loss at the input	2.4dB
Maximum input power	12dBm
Supply voltage	1.2V
Power consumption	1.25mW

Table 3.5: Simulated performance of the attenuator

3.2.6 Passive down-conversion mixer

Passive mixer of the feedback path is described in Figure 3.25. The topology chosen is the quadrature ring mixer with advantages to have a large bandwidth and work in the voltage domain.

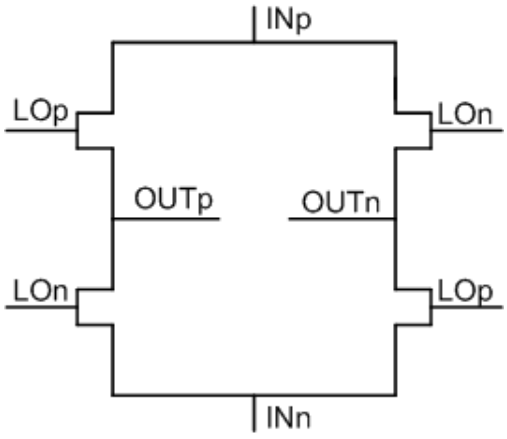


Figure 3.25: Topology of the passive mixer

Transistors switch from the active state (ON) to the passive state (OFF), according to the high and low LO levels. When the LO signal is positive (maximum voltage of the LO), the output of the mixer is positive and, when the LO signal is negative, the output of the mixer is also negative. This topology does not consume because it does not involve current supply (or outside bias voltage). The linearity of this mixer is high according to the constant gain for a large dynamic of the output signal.

As explained in the attenuator part, the maximum output power of the attenuator is -4dBm. Thereby, the mixer has to be linear for an input power of -7dBm minus 3dB because of the splitting of the signal towards the I and Q paths. This mixer has a conversion loss [67, 68] because the topology used is passive and is defined by equation 3.2:

$$G_c = \frac{2}{\pi} \tag{3.2}$$

The linearity of the mixer is related to its output impedance. In our case, the input impedance of the baseband filter is an open impedance which insures a good linearity of the mixer.

Figure 3.26 shows the die area of the passive down-conversion mixer and measures 5.5x24µm².

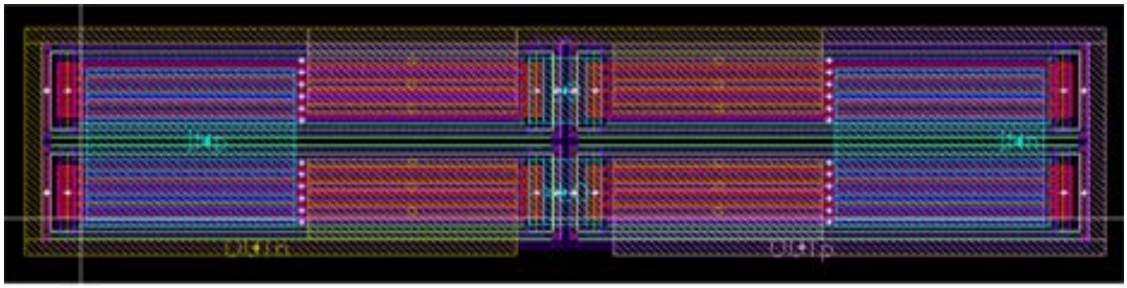


Figure 3.26: Die area of the down-conversion mixer

The filter of the feedback path is not described here because we are using the same filter that the direct path previously described in the active filter part.

3.2.7 Analog-to-Digital Converter (ADC)

The architecture of the analog-to-digital converter is a pipeline converter. The principle of the pipeline converter is that for every rising clock, the converter makes n parallel conversions, where each conversion is a part of the output code. Figure 3.27 describes the architecture of the parallel converter. For each clock period, a new digital code is performed according to n voltage values. As a consequence, this digital code has to be delayed to make the correct output code according to the number of stages of the converter.

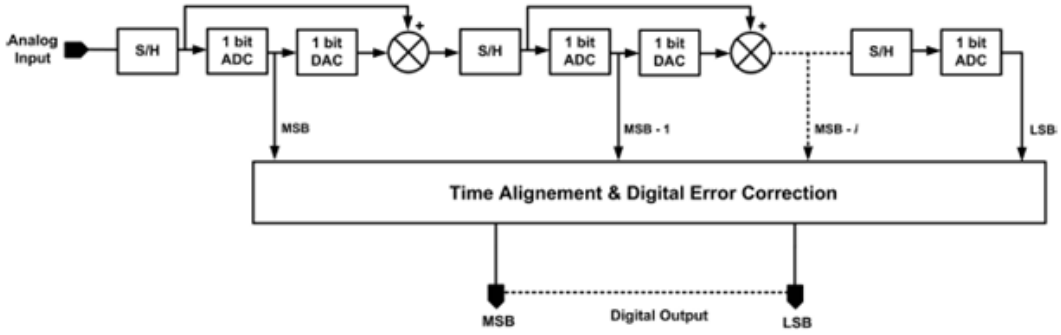


Figure 3.27: Classic architecture of a pipelined converter

The ADC is a parallel pipeline architecture with two identical internal pipeline units. Every internal pipeline unit is based on a double sampling architecture.

The first stage is a 1.5bit stage for high analog bandwidth constraint (130MHz). It is followed by four-stages of 2.5bit per stage resolution and finally a 3bit flash ADC.

A flash converter (Cf. Figure 3.28) is composed of parallel comparators. A n bits converter needs $2n-1$ comparators and $2n$ resistors. The conversion is performed for each clock period. This architecture has a drawback: occupy a large die area because of the number of comparators. But the main drawback of this architecture is the consumption, as for each supplementary bit the consumption is doubled. It is for this reason that a 3bit is employed, making a good compromise between performance and consumption.

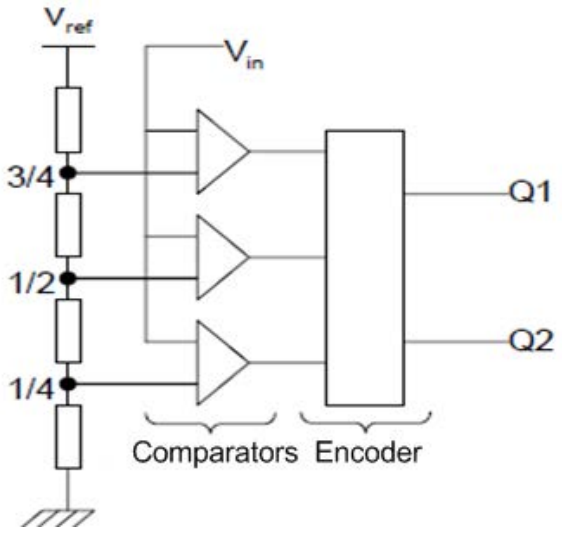


Figure 3.28: Flash converter architecture

A biasing is used to reduce power consumption adapting it to a wide sampling frequency range from 81MHz to 324MHz. Table 3.6 presents performance of the converters designed and measured by STMicroelectronics.

DAC resolution	12 bit
INL	+/- 2LSB
DNL	+/- 1LSB
Input bandwidth	130MHz
Fs	324MHz
Area	0.3mm^2
Consumption	Analog: 90mW/Digital 1mW

Table 3.6: Measured performance of the ADC

3.2.8 Schematic of the analog transmitter

The schematic of the whole architecture is illustrated in Figure 3.29. The Cartesian Feedback shows all the analog building blocks without converters.

Converters are not implemented on the chip because their supply options (GO2 are respectively equal to 1.8 and 2.5V) are different and thus it is impossible to put two types of supply on the same chip.

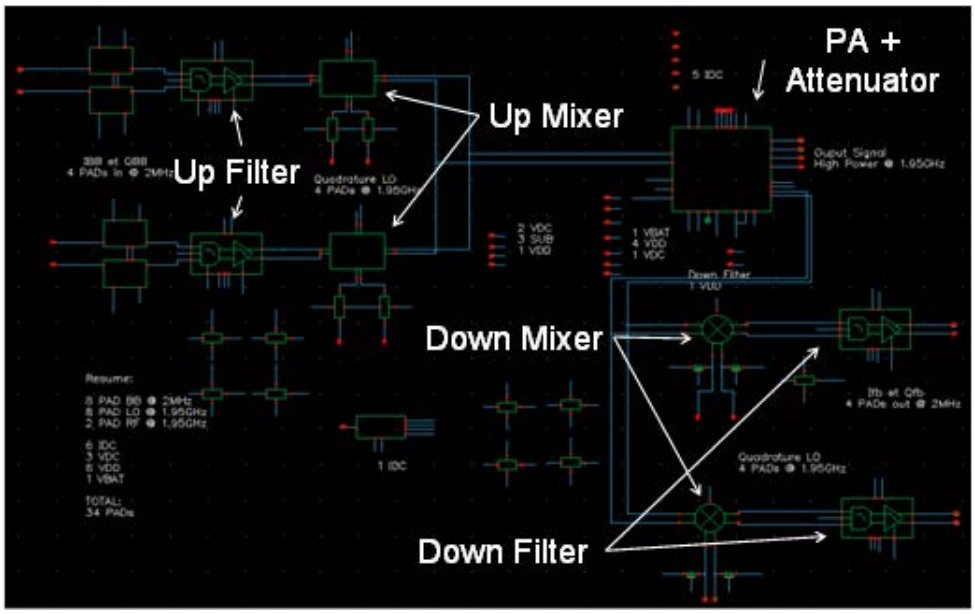


Figure 3.29: Whole schematic of the analog transmitter

The layout of the analog transmitter is presented in Figure 3.30. The IC solution includes the PAD ring with ESD (ElectroStatic Discharge) protection. As a precaution, we split the voltage supply and the ground according to the frequency-domain of the circuit. For example, the base-band feedback and direct path have separate supplies to reduce the voltage drop. By the same way, the supply and the ground of the power amplifier are separated from the others to insure an accurate voltage or current going on the main component of the chip.

The total analog transmitter die area is equal to 2 x 2 mm^2 for a DC/RF consumption of 480/765mW respectively.

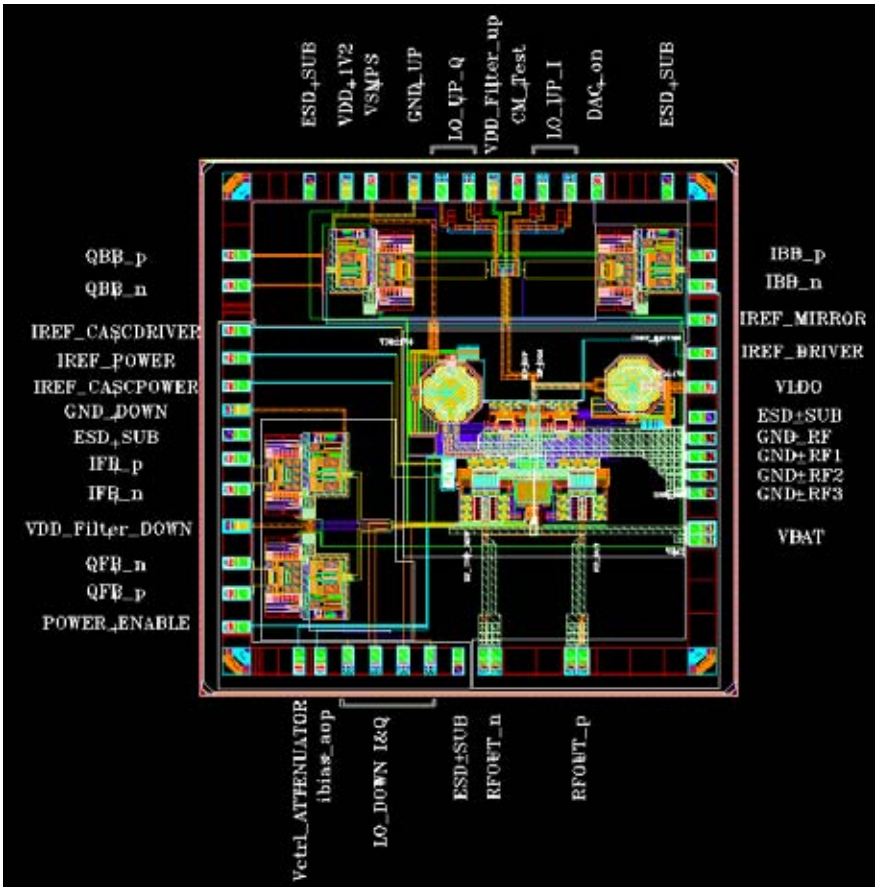


Figure 3.30: Die area of the analog transmitter

Table 3.7 and 3.8 summarize the die area and the DC/RF consumption of each component used to realize the linearization of a transmitter for the third generation of mobile communications.

COMPONENTS	DC consumption	RF consumption @$P_{out} = 23dBm$
Active filter	20.5mW	20.5mW
Up-conversion mixer	63.3mW	67.8mW
Power Amplifier	370mW	658mW
TOTAL	453.8mW	746.3mW

Table 3.7: Consumption of each building block of the direct path

COMPONENTS	DC consumption	RF consumption @$P_{out} = 23dBm$
Attenuator	1.25mW	1.25mW
Down-conversion mixer	-	-
Feedback filter	24.9mW	24.9mW
TOTAL	26.15mW	26.15mW

Table 3.8: Consumption of each building block of the feedback path

Figure 3.31 shows the photography of the realized IC and can be compared to the layout shown in Figure 3.30.

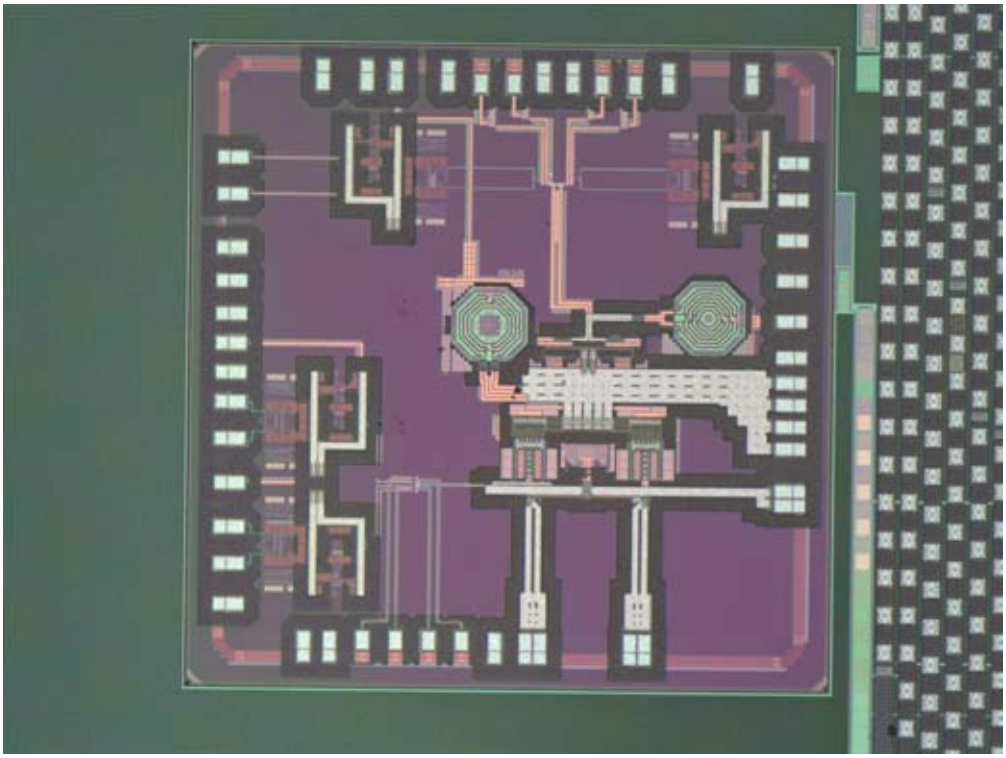


Figure 3.31: Photography of the IC Cartesian Feedback

3.3 Linearization Results

All RF systems have to pass through several steps before their integration on cell phones as a finalized product. In this part, simulation of the whole system will be done with digital, analog and mixed simulations.

First, the architecture of the transmitter has to be determined according to the wireless standard targeted (Cf. Chapter 1) which is, in our case, the W-CDMA used for the third generation of wireless communication. Taking in consideration the architecture adopted, the Cartesian Feedback technique has been chosen according to the criteria as the consumption, the size of the chip and the complexity of the solution which has to be integrated in 65nm CMOS technology.

Every transmitter has to be studied on a system level before beginning the design of each analog component. This step remains very important as all further decisions will result from it. The system level study has for objective to specify characteristics of each building block of the transmitter, in our case, the Cartesian Feedback architecture. We realized this study in Chapter 2.

Once parameters of each component are chosen, the design on the transistor level can be performed respecting specification given by the previous study. At the same time, the layout of each analog circuit is designed. The final step is to make the entire layout of the transmitter with the PAD ring associated in order to measure it after.

This section will illustrate linearization results of the circuit from simulation behavior using ADS software; to the transistors level using RFDE or GoldenGate software. To validate our system, which includes a digital and an analog part, simulations using SystemVue (with ModelSim) and ADS (via Dynamic Link) have been made showing the improvement given by the mixed IC Cartesian Feedback.

3.3.1 Methodology of co-simulations experiments

To complete our study, co-simulations between the analog and the digital parts have been performed. Several Agilent's softwares were used to get complete results. SystemVue and ADS were used for the digital part and the analog part, respectively.

The whole simulation is depicted in Figure 3.32 (co-simulation). The simulation is led by SystemVue according to results coming from ModelSim (for the VHDL code) and ADS (Ptolemy

+ Analog-RF for the entire circuit).

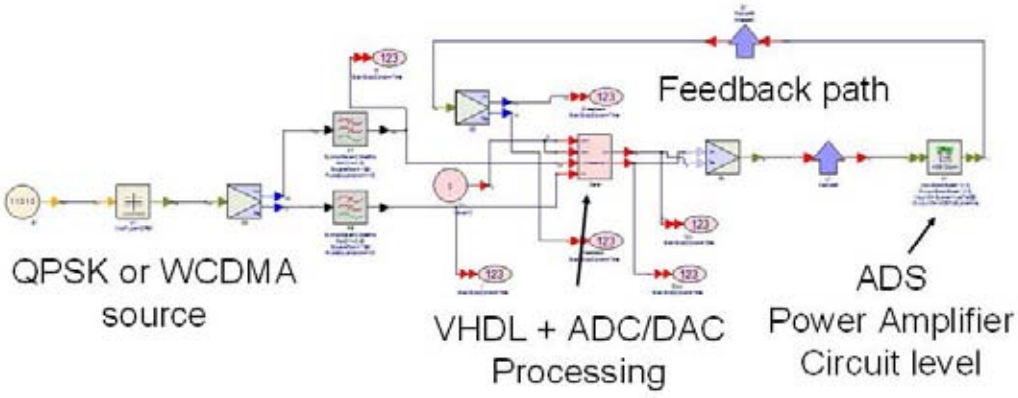


Figure 3.32: Whole co-simulation overview

Focusing on the digital part, the objective was to validate the behavior of the VHDL code with a modulated signal as the W-CDMA standard. Figure 3.33 shows the simulation of the digital part using SystemVue from Agilent.

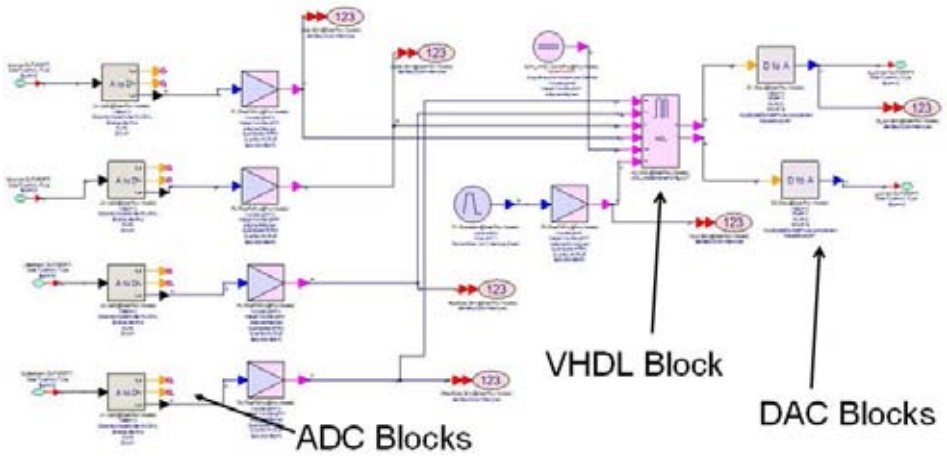


Figure 3.33: Simulation bench of the digital part

The simulation of the digital part allows to observe the behavior of the VHDL code. From this simulation, we were able to interpret results and some limitation of the code as it is represented in Figure 3.34. The right figure shows that the correction is effective when the delay is less than 10% to the period of the signal, but has an issue to make the correction in the other case (Cf. left figure).

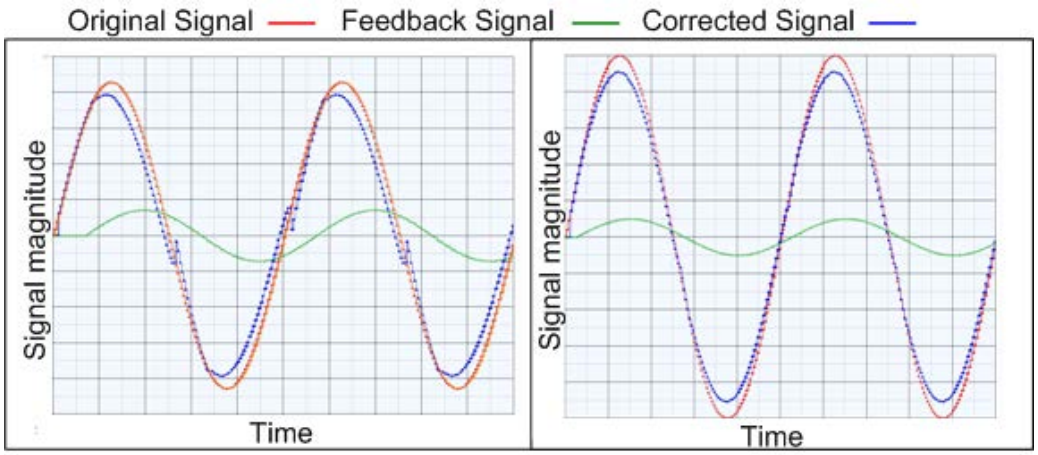


Figure 3.34: Digital signals simulated with SystemVue

This digital simulation is composed of converters (analog-to-digital and digital-to-analog) and a VHDL block. In order to reduce the simulation time, converters blocks with parameters taken from measurements of them are used. The VHDL code is implemented inside the VHDL block. It works with the simulator called ModelSim (simulator specialized in digital simulation). In the left Figure 3.34, original and feedback signals are coming, whereas corrected signals are coming out from the VHDL block (right side).

The analog part, as it is shown in Figure 3.35, is simulated by ADS from Agilent.

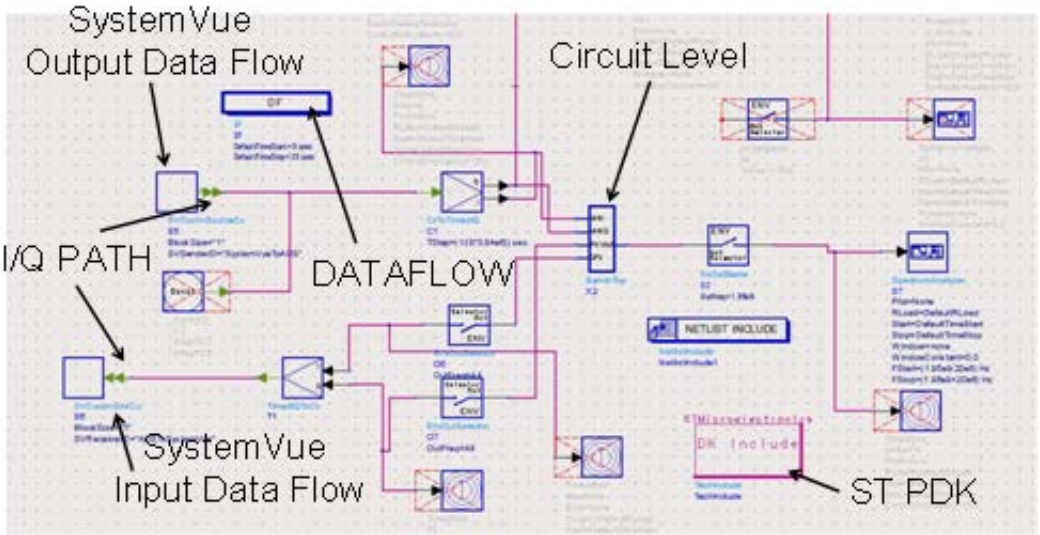


Figure 3.35: Simulation bench of the analog part

Two domains (analog and digital) exist for this new co-simulation. The digital part is working with Ptolemy, making the interface between the circuit realized on CMOS and the digital part.

The circuit level part is the same that was presented in the Part 3.2.8 - Circuit Assembly. The circuit includes all components and the PAD ring associated. As a consequence, the simulation of the entire circuit will show the whole behavior of the system.

3.3.2 Co-simulation results

From the methodology of simulations previously described (Cf. Chapters 1 and 2), several simulations can be performed in order to evaluate the whole circuit. We propose to show system level simulation results from different metrics presented on the first chapter as the spectrum, ACLR before and after linearization, or with and without linearization for the EVM.

Figure 3.36 presents the spectra from the input and the output of the power amplifier without linearization. As explained above (Cf. Section 1.3: Nonlinear Behavior of a RF Transmitter) the output spectrum of the power amplifier working in the nonlinear region shows the appearance of non-desired power on the adjacent channels.

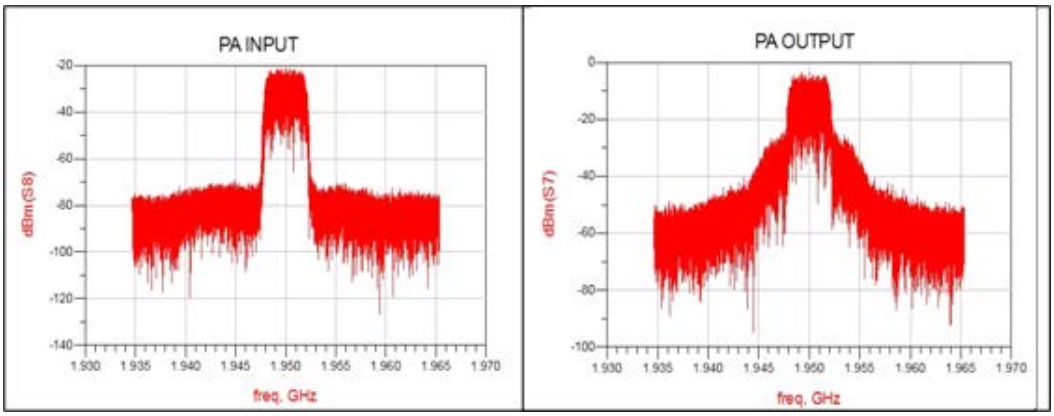


Figure 3.36: Input and output spectrums without linearization

The goal of the simulations is to reduce the power on the adjacent channels and can be observed in Figure 3.37. Figure on the left shows the phenomena of signal predistorted at the input of the power amplifier.

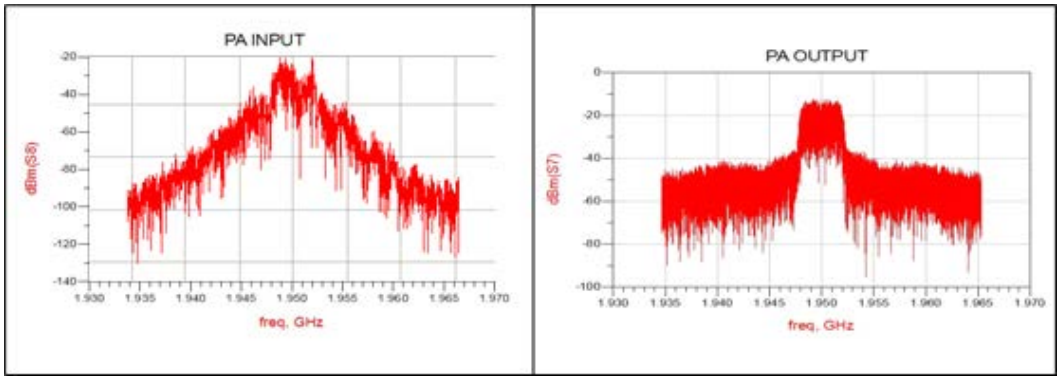


Figure 3.37: Input and output spectrums with linearization

From this spectrum, it looks difficult to provide a metric to this linearity's improvement. We propose to show the decreasing of the power on the adjacent channels in a different way. Figure 3.38 illustrates the ACLR level according to the output power of the power amplifier.

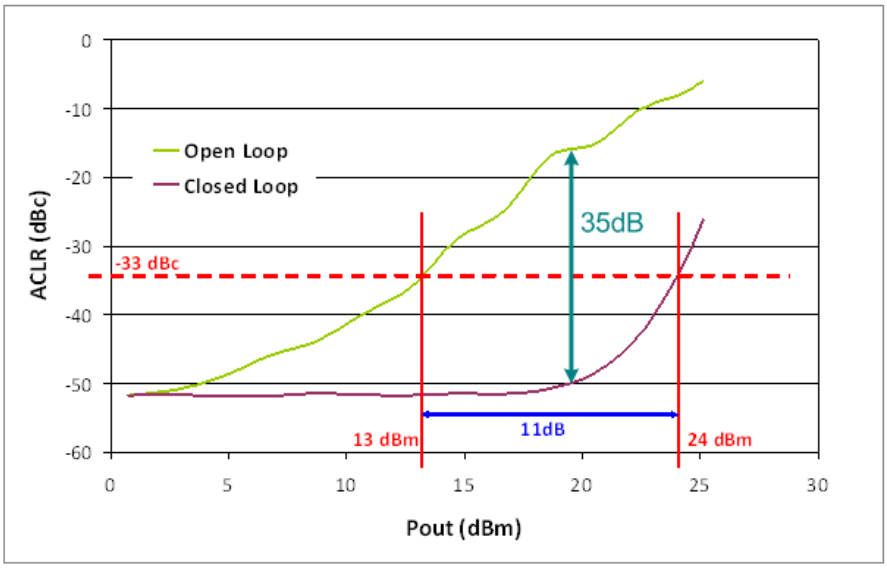


Figure 3.38: ACLR with and without Cartesian Feedback

The open-and closed-loop illustrate different configuration of the whole circuit designed in CMOS technology. The high level of the ACLR of the open-loop can be explained by the equation of the first chapter (IMDx). Then, the nonlinearity of the up-conversion mixer added to the nonlinearity of the power amplifier gives a supplementary effect that the designer has to take into account for the design of a stand-alone transmitter. In our case, it is not necessary to consider the nonlinearity behavior of the direct path because the whole system (more accurately the feedback path) will correct these nonlinearities. From this simulation, the most important

information can be seen as the improvement of the ACLR according to a fixed output power. But also, it can be the increasing output power that the system can reach staying in conformity with the targeted standard. In our case, if we fix the simulation to the requirement given by the standard (ACLR @5MHz from the carrier = -33dBc), the output power of the chip is going from 13dBm to 24dBm. Let's remember that the transmitter is highly nonlinear to prove our theory explained previously.

Another result of the predistortion of signals can be elucidated with the constellation at the input and output of the power amplifier. This phenomenon is presented in Figure 3.39 and has been simulated with Agilent tools.

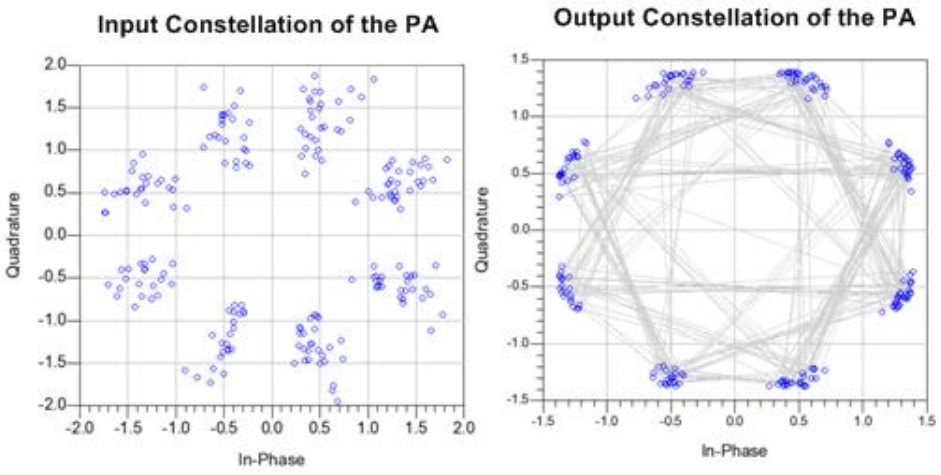


Figure 3.39: Input and output constellations of the power amplifier

The constellation in the left figure shows the nonlinearity of the signal at the input of the transmitter. Whereas the constellation in the right figure shows that the nonlinearity of the signals added to the nonlinearity given by the direct path result in a linearized signal (or spectrum).

3.4 Comparison with the State-of-the-Art

To conclude the study of our transmitter, a comparison can be performed with other architectures found in the literature, taking into account some precautions about the technology, the standard targeted, and the level of integration of the system on silicon.

All circuits presented in this part are only considering the RF part of the transmitter (without the frequency synthesis).

Reference	[69]	[40]	[57]	[35]	This Work
Technology	LDMOSFET	Mini-circuit	HSB 0.3µm	65nm CMOS	65nm CMOS
PA Class operation	AB	A	AB	PPA	AB
Frequency (GHz)	2.14	0.9	1.95	1.95	1.95
Standard / Modulation	W-CDMA	16-QAM	W-CDMA	W-CDMA	W-CDMA
ACLR improvement	15.3dB	10dB	24dB	27dB	35dB
Consumption	NC	NC	NC	45mW (w/o PA)	772mW (114mW w/o PA)
Die Area	NC	NC	2.9x1.5 mm^2	0.53mm^2 (w/o PA)	2 x 2 mm^2

Table 3.9: Comparison with the literature

It is important to notice that it seems hard to find the perfect literature for a realistic comparison with our system. Some publications are enunciated for the theoretical comparison and others for the consumption and the die area.

Table 3.9 presents a comparison of our system with a recent state-of-the-art. As we can see, references [69] and [40] are also using Cartesian Feedback correction. For the same PA class operation and the same standard, the ACLR improvement of our system is 7dB better than the reference [69]. Moreover, our work is a single circuit that offers a compact and cheaper system than other circuits earlier mentioned.

Finally to evaluate the die area and the consumption of our whole solution, we decided to compare it to [57] and [35]. The latter reference is a theoretical study based on prevision for each block contrary to our system which is an effective layout. We can see that our circuit offers a greater ACLR improvement for a similar die area than the reference [57].

Conclusion

This study presents the integration on silicon of an entire linearized transmitter using a Cartesian Feedback for the W-CDMA standard.

In the first chapter, transmitter architectures and different techniques to improve the linearity or the efficiency have been presented. Moreover, metrics to evaluate transmitters have been explained in frequency-and time-domain. An architecture with a linearization technique has been chosen according to the standard specification and the decrease of cost area and consumption that we imposed.

In the second chapter, theoretical study has been illustrated according to linearity and noise behavior making the transmitter unstable. Different digital architectures have been proposed and evaluated in the digital domain with theoretical results. Simulations performed with ADS have been shown to determine the value of every component making the final transmitter.

In the third chapter, each building block has been explained from the digital domain for the signals corrections, and to the analog domain for the direct and feedback path. Then we added the final circuit with PAD ring to make whole simulations to evaluate our system. Thanks to Agilent software, we were able to realize these simulations taking into account digital and analog specification. Therefore, our system including the digital part, the analog part and the PAD ring gave an ACLR improvement equal to 35dB at 5MHz from the carrier for an output power of 24dBm. Every analog building block have been designed and simulated in 65nm CMOS technology. Whole simulations have been realized from simulated and/or measured circuits, like the power amplifier. The analog part of the Cartesian Feedback brought us a consumption of 746mW for a die area of 1.77mm^2 for the direct path, whereas the feedback path gave us a die area equal to 0.211mm^2 for a consumption of 26.2mW, which represents 3.4% of the whole consumption. From theses simulations results, theoretical comparison has been made to appreciate the linearity improvement of the Cartesian Feedback.

Finally, a patented architecture will be detailed in order to make a single chip addressing a lot of standards, mainly for the mobile communications. This solution proposes to adapt the current Cartesian Feedback with few changes to linearize the whole transmitter. The new architecture has for advantages to relax some constraints of the components from the direct path. For example, the designer will focus on the maximum output power and the bandwidth of its components letting the Cartesian Feedback dealing with the linearity.

Perspectives: Multi-Standard Solution using the Cartesian Feedback Technique

Nowadays one of the main concerns on mobile firm is to integrate always more functions in the same chip. This concept is very attractive for a lot of companies and, in account of that, gives us the idea to adapt our system using the Cartesian Feedback for one standard to multi-standard applications. The proposed solution, which will be presented, has been patented in collaboration between the laboratory IMS and STMicroelectronics.

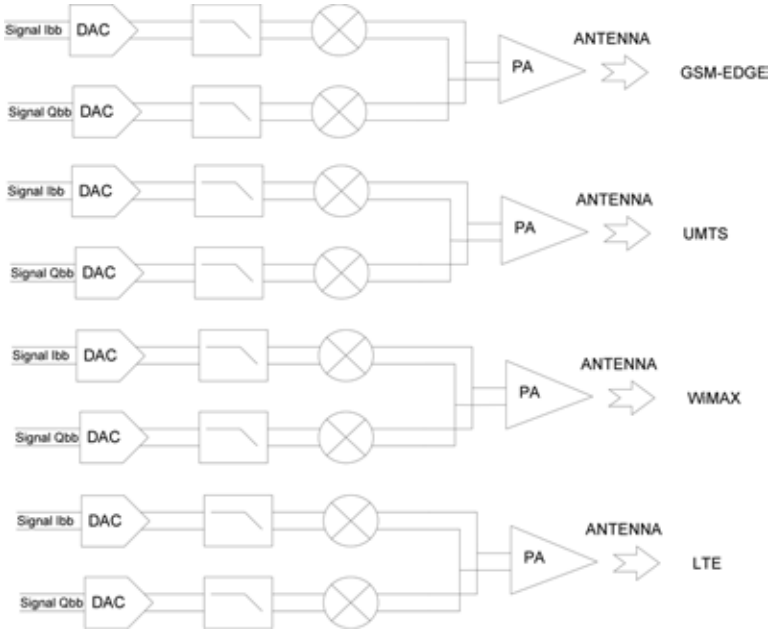


Figure 3.40: Parallel transmitter integrated on a mobile

The solution previously presented works perfectly for the integration on a system for a mono-standard application. However, mobile phone regarding its localization can change the standard used. For example, in a city it seems easy to find W-CDMA standard but in the countryside the preferred standard is the GSM. The common solution found in the literature is to duplicate

the transceiver for each standard that the mobile can address (Cf. Figure 3.40). This involves an over consumption in silicon and by consequence a higher cost of production.

The idea is thus to apply our correction system of nonlinearities for multi-standard applications.

Standards	Frequency (MHz)	Bandwidth	P_{out}Max	Data rate (bps)
GSM / GPRS	DCS1800: 1710 - 1785 PCS1900: 1850 - 1910	200kHz	33dBm	9.6k 21.4 - 171.2k
UMTS	Band I: 1920 - 1980	5MHz	27dBm	144k - 2M
WiMAX	3500 (Europe)	3.5 - 10MHz	21dBm	70M
LTE	2570 - 2620	1.25 - 20MHz	27.5dBm	100M

Table 3.10: Specifications of main communication standards

As a reminder, Table 3.10 shows the standard more usually used for integrated wireless system (or further integrated as LTE which is the next generation of communication standard also called 3.9G). These different standards were designed in order to meet an increase demand of consumers involving higher data speeds.

Proposed Solution

The solution to overcome this overhead of silicon is to integrate all of these standards in one single system, as it is presented in Figure 3.41.

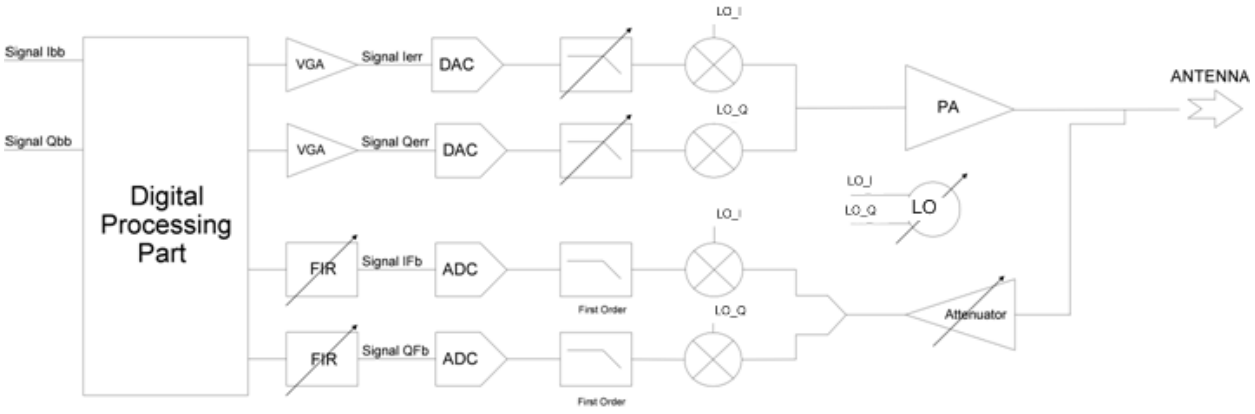


Figure 3.41: Architecture of the multi-standard Cartesian Feedback

From this new architecture we can notice that the main changes are on the filter of the direct and feedback path. Indeed, to address different standards in a single chip, the system must be able to select channels of the wanted standard.

This new architecture works as follow:

- First, the analog baseband filter of the direct path is replaced by an adaptive Gm-C filter [70]. The goal of this filter is the same than before, to expect that the cut-off frequency can be changed to select the right channel.

- Secondly, the analog filter of the feedback path placed before the ADC has relaxed constraints regarding its order cut-off frequency. It makes a first filtering of the useful signal. Moreover, the filter must have a large cut-off frequency in order to pass the useful channel with its associated adjacent channel of the larger bandwidth standard. The adjacent channel should certainly not be cancelled because it contains information of nonlinearity of the transmitted signals.

- Finally, Figure 3.42 shows the working principle of FIR (Finite Impulse Response) filter, which is the main component of this new architecture. This figure illustrates the extrema in terms of channels bandwidth that the system must deal with, i.e. GSM and LTE (Cf. Table 3.10). The FIR filter, thanks to its strict cut-off frequency, selects perfectly the desired channel and its adjacent channels providing us the possibility to correct distortions of the transmitter. The resulting spectrum will then be subtracted to the original signal in order to come back in the classic mode of the Cartesian Feedback. The use of this filter allows us to remove a lot of constraints of the analog filter which has a higher filtering order.

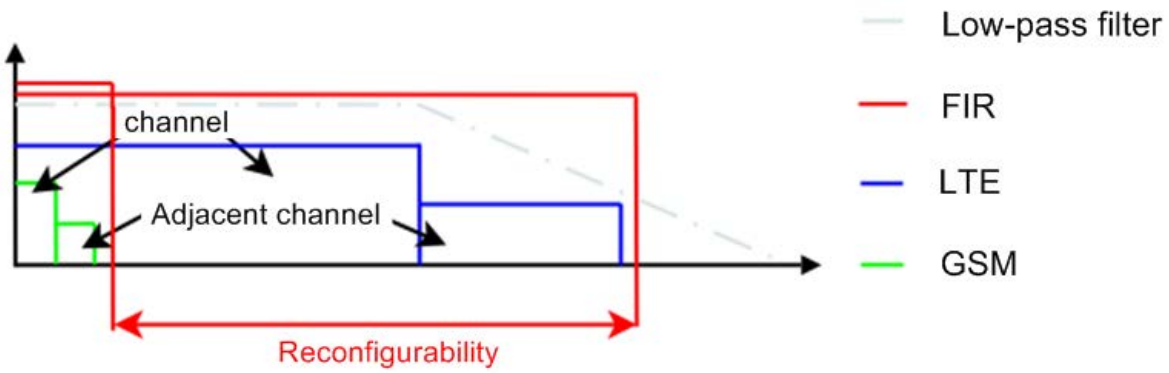


Figure 3.42: Working principle of FIR on the new architecture

Precautions and Specifications

In order to take advantages of the new architecture, we need to define specifications to the system:
- First, the local oscillator has to be able to cover all RF frequency bands defined by all standards.
- Second, a specific design has to be realized on mixers and on the power amplifier to increase their bandwidth. Typically, these components have a variation of the gain on a frequency band. This variation can make the system unstable, as a result, the designer has to check that mixers and power amplifier have a minimum variation of their gain in the bandwidth of all targeted standards.
- And finally, in a context of multi-standard application, the frequency band used is important for the Cartesian Feedback. This is not a problem for the feedback components, excluding the ADC, because they have been chosen to be the most linear as possible. Moreover, as the components making the feedback path are passive components, their bandwidths are large.

Bibliography

[1] J. Petersen, *The telecommunications illustrated dictionary.* CRC, 2002.

[2] "3GPP Group - official industry trade group representing GSM network operators worldwide - http://www.gsma.com/home/," 1993.

[3] "3GPP Group - the Mobile Broadband Standard - http://www.3gpp.org/," 2001 - 2003.

[4] L. Noël, A. Toskala, and D. Brunel, "Terminal radio-frequency design challenges," *WCDMA for UMTS*, pp. 507–533.

[5] M. Amit Kumar, J. Sengupta, and Y. Liu, "Technology evolution of 3GPP HSPA family."

[6] "3GPP Group - radio-electronics & 3GPP The Mobile Broadband Standard - http://www.3gpp.org/article/lte-advanced," 2010.

[7] B. Razavi, "RF transmitter architectures and circuits," pp. 197–204, 1999.

[8] M. Soderstrand, "Adaptive heterodyne filters," *Adaptive Filtering*, vol. Dr Lino Garcia (Ed.), ISBN: 978-953-307-158-9, InTech, Available from: http://www.intechopen.com/books/adaptive-filtering/adaptiveheterodyne-filters, 2011.

[9] P. Garcia and P. Saguet, "Contribution à l'étude et à la réalisation d'une architecture à basse-fréquence intermédiaire intégrée pour le standard GSM," Ph.D. dissertation, 2000.

[10] B. Razavi, "A study of injection locking and pulling in oscillators," *Solid-State Circuits, IEEE Journal of*, vol. 39, no. 9, pp. 1415–1424, 2004.

[11] R. Adler, "A study of locking phenomena in oscillators," *Proceedings of the IRE*, vol. 34, no. 6, pp. 351–357, 1946.

[12] B. Pellat, J. Blanc, F. Goussin, D. Thevenet, S. Majcherczak, F. Reaute, D. Belot, P. Garcia, P. Persechini, and P. Cerisier, "Fully-integrated WCDMA SiGeC BiCMOS transceiver," in *Solid-State Circuits Conference, 2005. ESSCIRC 2005. Proceedings of the 31st European.* IEEE, 2005, pp. 519–522.

[13] J. Hsu, "A 0.18-μm CMOS offset-PLL upconversion modulation loop IC for DCS1800 transmitter," *Solid-State Circuits, IEEE Journal of*, vol. 38, no. 4, pp. 603–613, 2003.

[14] A. Tae-Won and P. Byeong-Ha, "A Fast-Locking Up-Conversion Modulation Loop Transmitter," *Journal of the Korean Physical Society*, 2002.

[15] W. Shockley, "The theory of pn junctions in semiconductors and pn junction transistors," *Bell Syst. Tech. J*, vol. 28, no. 3, pp. 435–489, 1949.

[16] J. Pinto and I. Darwazeh, "Error vector magnitude relation to magnitude and phase distortion in 8-PSK systems," *Electronics Letters*, vol. 37, no. 7, pp. 437–438, 2001.

[17] N. Deltimple, "Etude et réalisation d'un amplificateur de puissance reconfigurable en technologie BiCMOS SiGe pour des applications multi-standards GSM/DCS/UMTS," Ph.D. dissertation, 2005.

[18] M. Integrated, "Use selectivity to improve receiver intercept point," vol. http://www.maximintegrated.com/app-notes/index.mvp/id/749, p. TUTORIAL 749, 2002.

[19] A. Wood, W. Brakensick, C. Dragon, and W. Burger, "120 Watt, 2 GHz, Si LDMOS RF power transistor for PCS base station applications," in *Microwave Symposium Digest, 1998 IEEE MTT-S International*, vol. 2. IEEE, 1998, pp. 707–710.

[20] L. Kahn, "Single-sideband transmission by envelope elimination and restoration," *Proceedings of the IRE*, vol. 40, no. 7, pp. 803–806, 1952.

[21] A. Diet, C. Berland, M. Villegas, and G. Baudoin, "EER architecture specifications for OFDM transmitter using a class E amplifier," *Microwave and Wireless Components Letters, IEEE*, vol. 14, no. 8, pp. 389–391, 2004.

[22] S. Ampem-Darkko and H. Al-Raweshidy, "A novel technique for gain/phase error cancellation in LINC transmitters," vol. 4, pp. 2034–2038, 1999.

[23] F. Casadevall and A. Valdovinos, "Performance analysis of QAM modulations applied to the LINC transmitter," *Vehicular Technology, IEEE Transactions on*, vol. 42, no. 4, pp. 399–406, 1993.

[24] B. Shi and L. Sundstrom, "A LINC transmitter using a new signal component separator architecture," in *Vehicular Technology Conference Proceedings, 2000. VTC 2000-Spring Tokyo. 2000 IEEE 51st*, vol. 3. IEEE, 2000, pp. 1909–1913.

[25] Q. Ren and I. Wolff, "Influence of some imperfect system performances on linearizers," in *Microwave Symposium Digest, 1998 IEEE MTT-S International*, vol. 2. IEEE, 1998, pp. 973–976.

[26] R. Conradi, CP Johnston and J. McRory, "Evaluation of a lossless combiner in a LINC transmitter," in *Electrical and Computer Engineering, 1999 IEEE Canadian Conference on*, vol. 1. IEEE, 1999, pp. 105–110.

[27] K. Chan and A. Bateman, "Analytical and measured performance of the combined analogue locked loop universal modulator (CALLUM)," in *Communications, IEE Proceedings-*, vol. 142, no. 5. IET, 1995, pp. 297–306.

[28] W. Doherty, "A new high efficiency power amplifier for modulated waves," *Proceedings of the Institute of Radio Engineers*, vol. 24, no. 9, pp. 1163–1182, 1936.

[29] N. Dubuc, "Modélisation électrothermique de transistors MESFET SiC et optimisation d'une architecture Doherty pour l'amplification de puissance à haut rendement," Ph.D. dissertation, 2003.

[30] N. Dubuc, C. Duvanaud, P. Bouysse, and J. Paillot, "Optimisation du Fonctionnement d un Amplificateur Doherty par Glissement de Polarisation," *Journées Nationales Micro-ondes*, 2003.

[31] A. Katz, "Linearization: Reducing distortion in power amplifiers," *Microwave Magazine, IEEE*, vol. 2, no. 4, pp. 37–49, 2001.

[32] Y. Kang, H.W. Cho and D. Youn, "On compensating nonlinear distortions of an OFDM system using an efficient adaptive predistorter," *Communications, IEEE Transactions on*, vol. 47, no. 4, pp. 522–526, 1999.

[33] V. Petrovic and W. Gosling, "Polar-loop transmitter," *Electronics letters*, vol. 15, no. 10, pp. 286–288, 1979.

[34] D. Cox, "Linear amplification by sampling techniques: A new application for delta coders," *Communications, IEEE Transactions on*, vol. 23, no. 8, pp. 793–798, 1975.

[35] C. Tassin, "Etude de faisabilité d'un émetteur radio fréquence à onversion directe pour le standard WCDMA avec boucle cartésienne de linéarisation en technologie CMOS 65 nm," Ph.D. dissertation, Universite de Bordeaux 1, 2006.

[36] J. Dawson, "Feedback linearization of RF power amplifiers," Ph.D. dissertation, Stanford University, 2003.

[37] S. Pipilos, Y. Papananos, N. Naskas, M. Zervakis, J. Jongsma, T. Gschier, N. Wilson, J. Gibbins, B. Carter, and G. Dann, "A transmitter ic for TETRA systems based on a Cartesian feedback loop linearization technique," *Solid-State Circuits, IEEE Journal of*, vol. 40, no. 3, pp. 707–718, 2005.

[38] M. Zanchi, J. Pauly, and G. Scott, "Frequency-Offset Cartesian Feedback Based on Polyphase Difference Amplifiers," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 58, no. 5, pp. 1297–1308, 2010.

[39] C. Tassin and P. Garcia, "Gain control for cartesian loop transmitter with digital processing," April 2006, US Patent App. 20,060/238,393.

[40] J. Chung, S.W. Holloway and J. Dawson, "Open-loop digital predistortion using Cartesian feedback for adaptive RF power amplifier linearization," pp. 1449–1452, 2007.

[41] C. Tassin, P. Garcia, J. Bégueret, Y. Deval, and D. Belot, "Emetteur zero-if wcdma à boucle cartésienne avec des traitements numériques," *JNRDM*, May 2005.

[42] M. Briffa and M. Faulkner, "Stability considerations for dynamically biased Cartesian feedback linearization," in *Vehicular Technology Conference, 1994 IEEE 44th.* IEEE, 1994, pp. 1321–1325.

[43] M. A. Briffa and M. Faulkner, "Stability Analysis of Cartesian Feedback Linearisation for Amplifiers with Weak Non-linearity," *IEEE proceedings on Communications*, vol. 143(4), 1996.

[44] R. Kenington, P.B. Wilkinson and K. Parsons, "Noise performance of a Cartesian loop transmitter," *Vehicular Technology, IEEE Transactions on*, vol. 46, no. 2, pp. 467–476, 1997.

[45] L. Bussgang, J.J. Ehrman and J. Graham, "Analysis of nonlinear systems with multiple inputs," *Proceedings of the IEEE*, vol. 62, no. 8, pp. 1088–1119, 1974.

[46] S. Narayanan, "Application of Volterra series to intermodulation distortion analysis of transistor feedback amplifiers," *Circuit Theory, IEEE Transactions on*, vol. 17, no. 4, pp. 518–527, 1970.

[47] W. Sansen, "Distortion in elementary transistor circuits," *Analog Design Essentials*, pp. 519–565, 2006.

[48] M. Abid, C. Rebai, and D. Dallet, "Conception et réalisation d un sous-système numérique de correction et de compensation des amplificateurs de puissances," Ph.D. dissertation, IMS Bordeaux and SUPCOM Tunis, 2010.

[49] J. Volder, "The CORDIC trigonometric computing technique," *Electronic Computers, IRE Transactions on*, no. 3, pp. 330–334, 1959.

[50] J. Meggitt, "Pseudo division and pseudo multiplication processes," *IBM Journal of Research and Development*, vol. 6, no. 2, pp. 210–226, 1962.

[51] P. Meher, J. Valls, T. Juang, K. Sridharan, and K. Maharatna, "50 years of CORDIC: Algorithms, architectures, and applications," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 56, no. 9, pp. 1893–1907, 2009.

[52] R. Andraka, "A survey of CORDIC algorithms for FPGA based computers," in *Proceedings of the 1998 ACM/SIGDA sixth international symposium on Field programmable gate arrays.* ACM, 1998, pp. 191–200.

[53] J. Moore, T. Lynch, and M. Kaufmann, "A mechanically checked proof of the correctness of the kernel of the AMD5K86 floating-point division algorithm," in *IEEE Transactions on Computers*. Citeseer, 1996.

[54] N. Aggarwal, K. Asooja, S. Verma, and S. Negi, "An improvement in the restoring division algorithm (Needy Restoring Division Algorithm)," in *Computer Science and Information Technology, 2009. ICCSIT 2009. 2nd IEEE International Conference on*. IEEE, 2009, pp. 246–249.

[55] J. Dawson and T. Lee, "Automatic phase alignment for high bandwidth Cartesian feedback power amplifiers," in *Radio and Wireless Conference, 2000. RAWCON 2000. 2000 IEEE*. IEEE, 2000, pp. 71–74.

[56] N. Sornin, N. Massei, L. Perraud, and C. Pinatel, "A robust Cartesian feedback loop for a 802.11 a/b/g CMOS transmitter," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2004. Digest of Papers. 2004 IEEE*. IEEE, 2004, pp. 145–148.

[57] A. Carrara, F. Scuderi and G. Palmisano, "Wide-band Fully Integrated Cartesian Feedback Transmitter," *IEEE CSICC*, 2003.

[58] L. Leyssenne, "Design of reconfigurable radiofrequency power amplifiers for wireless applications," Ph.D. dissertation, Universite de Bordeaux 1, 2009.

[59] L. Yohann, "Contribution à la réalisation d amplificateurs de puissance en technologie CMOS 65 nm pour une application au standard UMTS," Ph.D. dissertation, Université de Bordeaux 1, 2009.

[60] N. Delaunay, N. Deltimple, L. Leysenne, E. Kerhervé, and D. Belot, "Linéarisation d un Amplificateur de Puissance BiCMOS7RF par Boucle Cartésienne pour le Standard W-CDMA," *JNRDM*, 2009.

[61] N. Delaunay, N. Deltimple, D. Belot, and E. Kerhervé, "Linearization of a 65nm CMOS power amplifier with a Cartesian Feedback for W-CDMA standard," *Circuits and Systems and TAISA Conference, 2009. NEWCAS-TAISA'09. Joint IEEE North-East Workshop on*, pp. 1–4, 2009.

[62] H. Dogan, R. Meyer, and A. Niknejad, "A DC-10GHz linear-in-dB attenuator in 0.13 um CMOS technology," in *Custom Integrated Circuits Conference, 2004. Proceedings of the IEEE 2004*. IEEE, 2004, pp. 609–612.

[63] C. Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6 mm2," *Solid-State Circuits, IEEE Journal of*, vol. 33, no. 12, pp. 1948–1958, 1998.

[64] A. Mariano, "Mixed Simulations and Design of a Wideband Continuous-Time Bandpass Delta-Sigma Converter Dedicated to Software Defined Radio Applications," Ph.D. dissertation, Université de Bordeaux 1, 2008.

[65] K. Vavelidis, Y. Tsividis, F. Eynde, and Y. Papananos, "Six-terminal MOSFET's: modeling and applications in highly linear, electronically tunable resistors," *Solid-State Circuits, IEEE Journal of*, vol. 32, no. 1, pp. 4–12, 1997.

[66] R. Bayruns, K. Li, D. Osika, D. Stofman, M. Shokrani, P. Fowler, E. Ham, and J. Brand, "The bootstrapped gate FET (BGFET) - a new control transistor," pp. 136–139, 1995.

[67] S. Zhou and M. Chang, "A CMOS passive mixer with low flicker noise for low-power direct-conversion receiver," *Solid-State Circuits, IEEE Journal of*, vol. 40, no. 5, pp. 1084–1093, 2005.

[68] V. Knopik, D. Belot, and D. Gerna, "Transceiver front-end with integrated TX/RX commutator for bluetooth applications," in *Solid-State Circuits Conference, 2002. ESSCIRC 2002. Proceedings of the 28th European.* IEEE, 2002, pp. 167–170.

[69] J. Kim, Y. Woo, J. Moon, and B. Kim, "A new wideband adaptive digital predistortion technique employing feedback linearization," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 56, no. 2, pp. 385–392, 2008.

[70] D. Chalma, "Filtres acitfs gm-c reconfigurables pour récepteurs mobiles multi-standards," Ph.D. dissertation, Université de Lille, 2006.