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Binhong LI

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Ecole doctorale :
Génie Electrique, Electronique et Télécommunications (GEET)

Unité de recherche :
LAAS-CNRS

Directeur(s) de Thèse :
Sonia BEN DHIA (Maitre de conférences/HDR - INSA-Toulouse, LAAS-CNRS)
Alexandre BOYER (Maitre de conférences - INSA-Toulouse, LAAS-CNRS)

Rapporteurs :

Mr. Georges GIELEN (Professeur - K.U. Leuven) Rapporteur
Mr. Felice CRUPI (Professeur - University of Calabria) Rapporteur

Membre(s) du jury :

Mr. Etienne SICARD (Professeur - INSA de Toulouse) Président du Jury
Mr. Philippe PERDU (Senior expert/HDR, CNES) Examinateur
Mr. Raul FERNANDEZ (Maitre de conférences/HDR - UPC) Examinateur
Fabian VARGAS (Professeur, Catholic University - PUCRS) Examinateur

Abstract

With the continuous trend towards nanoscale technology and increased integration of complex electronic functions in embedded systems, ensuring the electromagnetic compatibility (EMC) of electronic systems is a great challenge. EMC has become a major concern of IC redesign. Meanwhile, ICs performance could be affected by the degradation mechanisms such as hot carrier injection (HCI), negative bias temperature instability(NBTI), gate oxide breakdown, which are accelerated by the harsh operation conditions (high/low temperature, electrical overstress, radiation). This natural aging can thus affect EMC performances of ICs.

The work developed in our laboratory aims at clarifying the link between ageing induced IC degradations and related EMC drifts, developing prediction models and proposing "time insensitive" EMC protection structures, in order to provide methods and guidelines to IC and equipment designers to ensure EMC during the lifetime of their applications. This research topic is still under-explored as research communities on "IC reliability" and "IC electromagnetic compatibility" often do not overlap.

The PhD manuscript introduces a methodology to quantify the effect of ageing on EMC of ICs by measurement and simulation. The first chapter gives an overview of the general context and the second chapter states the EMC of ICs state of the art and IC reliability issues. The experimental results of ICs EMC evolution are presented in the third chapter. Then, the fourth chapter is dedicated to the characterization and modeling of the IC degradation mechanism. An EMR model which includes the ageing element to predict our test chip's EMC level drift after stress is proposed.

Key words

Electromagnetic compatibility, Emission, Susceptibility, Degradation mechanism, Hot carrier injection, Negative bias temperature instability, Ageing, MOS Modeling, EMC models.

Résumé

Avec la tendance continue vers la technologie nanométrique et l'augmentation des fonctions complexes intègres dans les électroniques systèmes embarqués, Assurant la compatibilité électromagnétique (CEM) des systèmes électroniques est un grand défi. CEM est devenu une cause majeure de redesign des Circuits intègres (CI). D'ailleurs, les performances des circuits pourraient être affectés par les mécanismes de dégradation tels que hot carrier injection (HCI), negative bias temperature instability (NBTI), gate oxide breakdown, qui sont accélérés par les conditions d'exploitation extrême (haute/basse température, surcharge électrique, le rayonnement). Ce vieillissement naturel peut donc affecter les performances CEM des circuits intégrés.

Les travaux développés dans notre laboratoire vise à clarifier le lien entre les dégradations induites par le vieillissement et les dérives CEM, de développer les modèles de prédiction et de proposer des "insensibles au cours du temps" structures pour CEM protection, afin de fournir des méthodes et des guidelines aux concepteurs d'équipements et CI pour garantir la CEM au cours de durée de vie de leurs applications. Ce sujet de recherche est encore sous-exploré en tant que communautés de recherche sur la «fiabilité IC» et «compatibilité électromagnétique IC» n'a souvent pas de chevauchement.

Ce manuscrit de thèse introduit une méthode pour quantifier l'effet du vieillissement sur les CEM des circuits intégrés par la mesure et la simulation. Le premier chapitre donne un aperçu du contexte général et le deuxième chapitre est dédié a l'état de l'art de CEM des circuits intégrés et de problèmes de fiabilité IC. Les résultats expérimentaux de circuits CEM évolution sont présentés dans le troisième chapitre. Ensuite, le quatrième chapitre est consacré à la caractérisation et la modélisation des mécanismes de dégradation du CI. Un EMR modèle qui inclut l'élément le vieillissement pour prédire la dérive du niveau CEM de notre puce de test après stress est proposé.

Mots-clés:

Compatibilité électromagnétique, émission, immunité, mécanismes de dégradation, l'injection de porteur chauds, negative bias temperature instability, vieillissement, modélisation.

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General introduction

Thesis context

During the word war period and through the 1960s, Electromagnetic compatibility (EMC) was primarily a concern for military systems. In 1965 at the Special Weapons Center, based at Kirtland, New Mexico, USA, the American army was the pioneer in the field of integrated circuit (IC) EMC. They studied the effects of electromagnetic fields triggered by nuclear explosion on electronic devices used in missile launch sites [BEND06]. Due to their low production cost per unit and their high performances, ICs are largely used in electronic systems. The design technologies of ICs are in a continuous development process to increase the performance and the integration of different function within the same chip (system-on-chip) or within the same package (system-in-package, three-dimension circuit). This trend leads to bring closer different functions with a higher activity per surface unit and thus an increase of interference risks. The growing complexity aggravates the intra-system or intra-chip interferences. Besides, the higher operational frequencies also contribute to the increase of interference risks. Printed circuit board tracks and package leads can pick up the disturbing signal in Ultra High Frequency band with telecommunication (UHF 300MHz – 3GHz) and even Extremely High frequencies with radars (XHF 3GHz – 30GHz) [WHAL79], just as the long power supply lines which pick up the lower frequency noise and inject it into sensitive electronic devices. The design of ICs with low electromagnetic emissions and a high level of immunity is still a very challenging issue. Owing to the growing use of electronic equipment and more complex electromagnetic environment, EMC issues migrate from military domains to various applications: spatial, aeronautic, automobile, personal entertainment, medical…

Toulouse is the fourth largest city in France, which has benefited industrial decentralization policies since the First World War. Today Toulouse is a worldwide pole for aerospace industry: Airbus, Centre National d'Etude Spatial (CNES-Toulouse), EADS-Astrium, Thales Alenia Space… The great level of research in embedded electronic system in aerospace, led the development in automotive application, such as: Freescale semiconductor, Continental automotive (ex. Siemens VDO automotive). Under multi-projects with industries and research centers, our laboratory LATTIS (Laboratoire Toulousain de Technologie de d'Ingénierie des Systèmes) in INSA-Toulouse (Institut

National des Sciences Appliquées de Toulouse) investigates the design and modeling for EMC of ICs intended for aerospace electronics and automotive electronics. The research objectives concern:

- Electromagnetic emission: the characterization methods of conducted and radiated emission of ICs, the modeling and simulation of these issues at design level, and the proposition of design rules to minimize emission level and meet the emission level required by standards.
- Immunity or susceptibility to electromagnetic interferences: the characterization of the conducted/radiated immunity of IC to radiofrequency interference (RFI) , the modeling and simulation of these issues at design level, and the proposition of design rules to optimize immunity level and meet immunity level required by standards.

Meanwhile, during their lifetime, ICs are affected by different degradation mechanisms, such as hot carrier injection (HCI), negative bias temperature instability (NBTI), time-dependent dielectric breakdown (TDDB)… [WHIT08]. These degradation mechanisms can shift the properties of electronic devices and thereby affect the circuit performance and EMC margins of ICs. Furthermore the degradation mechanisms can be accelerated by harsh operation conditions (high/low temperature, electrical overstress, and radiation) which reduce the device lifetime [WHIT10]. Therefore, it is very difficult to guarantee the EMC compliance of the integrated circuits over the nominal lifetime.

For example, we can enumerate the operation environment for several critical applications and explain how the environment can threaten both circuit reliability and EMC:

- Spatial applications: a satellite works in unstable and extreme temperature (-115°C to +260°C depending on its position). In space, it is submitted to electromagnetic radiation and ionizing radiation from the sun and other stars. Moreover, due to its reduced volume, there are EMC problems caused by the interaction among different modules inside (as telecommunication or digital parts to analogical sensor) and outside (as Radar). The electronic device for spatial application must work for several years without any on-site repairs or replacement. During their operation period, the electronic devices undergo ageing which can be accelerated by extreme operation environment. Therefore, the impact of device degradations induced by ageing to the system EMC needs to be considered and predict before the satellite launching.

Figure 0-1: International Earth observation satellite: JASON-2 [WIKI09]

- Aeronautic applications: electronic devices have to be able to work under extreme temperature (from -55°C to +125°C according to MIL-STD-883B [MIL-STD]) for tens of thousands hours. An aircraft flying at an altitude of 12000m has little protection against cosmic radiation by Earth's atmosphere. The integration of different electronic equipment in airplane cabin results in complicated intra-system interferences. Lightning and Radar radiation create an external electromagnetic pollution. During their operation lifetime, it is important to ensure that electronic devices are still EMC compliant for safety reasons.

Figure 0-2: Airbus A380 aircraft and the electronic system [LAMO06]

- Automotive applications: In 2010, automotive electronic systems contain over 100 microcontrollers inside to support the growing need in safety, multimedia, telecommunication… [DAVI08]. The reliability and EMC are crucial problems to the whole system security. A car and its electronic systems are designed for over 10 years, with more extreme operation temperature range (-40°C to +125°C, +150°C at junction level) than commercial applications (0°C to +70°C). Thus the reliability and EMC for the automotive dedicated devices are popular and critical subjects to automotive electronics manufacturers. The interaction between both domains is also taken into the research agenda.

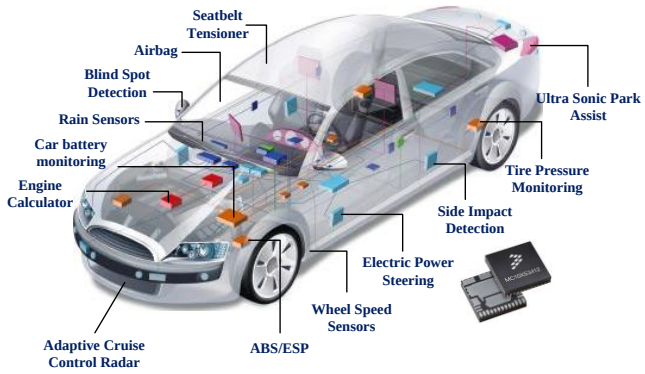

Figure 0-3: **Automotive microcontrollers**

The reliability design assures the long-term circuit functionality in certain margin, but not for EMC issue. Consequently, EMC of ICs needs to be quantified not only for components that passed infant mortality (as for the current EMC test in the industry), but also be quantified in the real-life condition [ARMS05], coupled with the reliability tests, to ensure its long-term safety.

The scope of this dissertation

Based on the contexts above, a new concept EMR (ElectroMagnetic Robustness) has been developed in the recent years to study and evolution the impact of circuit ageing on circuit EMC. This manuscript deals with the characterization of time evolution of integrated circuit EMC level under accelerated stress test and the development of a methodology to predict the integrated circuit EMC level variation after ageing by model simulation. We propose a model for the prediction electromagnetic robustness model, including EMC and reliability models to reproduce both circuit EMC performances and reliability degradation of circuit undergoing ageing.

The dissertation is organized as follows.

Chapter 1 details the most relevant state of the art for our research context. It begins by a description of the problematic of technology evolution, and especially EMC of ICs issues which include electromagnetic emission and immunity issues. Then IC reliability issues are introduced. A comparison between traditional reliability and physic of failure approaches is made. Four major degradation mechanisms are presented and analyzed. In the last part, the electromagnetic robustness of ICs concern will be introduced with some relevant works about this new topic.

Chapter 2 investigates the evolution of EMC level after device ageing. After an introduction of the characterization flow and experimental set-up used for emission and susceptibility measurements

and accelerated ageing test. Two case studies are used to show the variation of conducted emission and conducted immunity after different accelerated ageing tests.

Chapter 3 is devoted to the characterization of the device degradation induced by ageing at transistor level. Two major degradation mechanisms are studied: negative bias temperature instability on PMOS and hot carrier injection on NMOS. The transistor I-V characteristic degradation is modeled two different models: SPICE level 3 model and Nth power law mode. Model parameters evolution is extracted from measurements. These models can be used for the simulation of EMC at circuit level and its evolution after ageing.

Chapter 4 deals with the prediction of immunity level degradation after ageing. It firstly presents a simulation flow dedicated to electromagnetic robustness prediction which consists in embedding the device degradation model into the circuit EMC model. Then, two different case studies are given to show the modeling and simulation procedures of the circuit immunity evolution after ageing.

Finally, the general conclusion summarizes the contribution of this dissertation and offers perspective in regard to the future work.

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Chapter 1: Long term EMC issues

The steady miniaturization of integrated circuit and evolution of the circuit complexity not only improve circuit performance, but also cause side effects, such as tightening of the constraints in term of EMC, worsen the overall circuit reliability. Meanwhile, the intrinsic degradation mechanism can result a significant drift of physical parameters and circuit performances, thus the circuit electromagnetic compatibility.

In this chapter, we begin by introducing the technology evolution and its impacts. Then in the second section, the state of the arts of integrated circuit electromagnetic compatibility is given concerning circuit emission and immunity issues. The third section firstly compares the traditional reliability approach and physics of failure approach and discusses the four major degradation mechanisms. Finally, in the fourth section, by combination of circuit electromagnetic compatibility and circuit reliability, the circuit electromagnetic robustness concept is proposed.

1. ETECHNOLOGY EVOLUTION AND CRITICAL ISSUES FOR DEVICE MINIATURIZATION

1.1. Technology evolution: from history to present

Electronic device performances have improved dramatically over the decades, enabled by significant advances in integrated circuit (IC) technology evolution. Among the variety of the major IC manufacturing process technology, Complementary Metal-Oxide-Semiconductor (CMOS) used a combination of P-type and N-type Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET). They were well used in microprocessors, microcontrollers, memory (DRAM or FLASH) and other digital logic circuits. CMOS technology is also widely used for RF, analog and mixed circuits. As an example (Figure I-1), in 1997, the CMOS shared the 69% of the market, while Bipolar and other process shared 31%, in 2002, the CMOS occupied to 84% of the IC market. The unprecedented development of integrated circuit performance is led by the continued miniaturization of transistor.

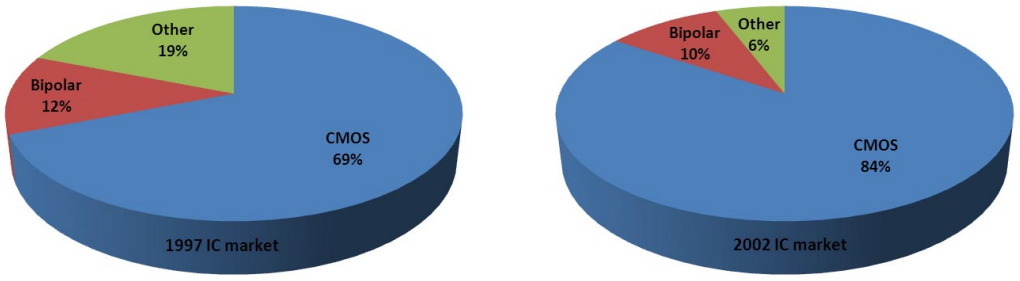

Figure I-1: CMOS dominate the IC market from year to year. (Source: ICE)

In 1965, Gordon E. Moore the co-founder of Intel sketched out his prediction of the pace of silicon technology [MOOR65]: the number of components in integrated circuits had doubled every year from the invention of the IC in 1958 until 1965. He predicted that the trend would continue "for at least ten years". After that, Moore slightly altered the formulation of the law over time, in 1975. He altered it to a doubling every two years. His prediction has been proved to be uncannily accurate in recent technology evolution and will continues, in part because this law is now used in the semiconductor industry to guide long term planning and to set targets for research and development, depicted in Figure I-2.

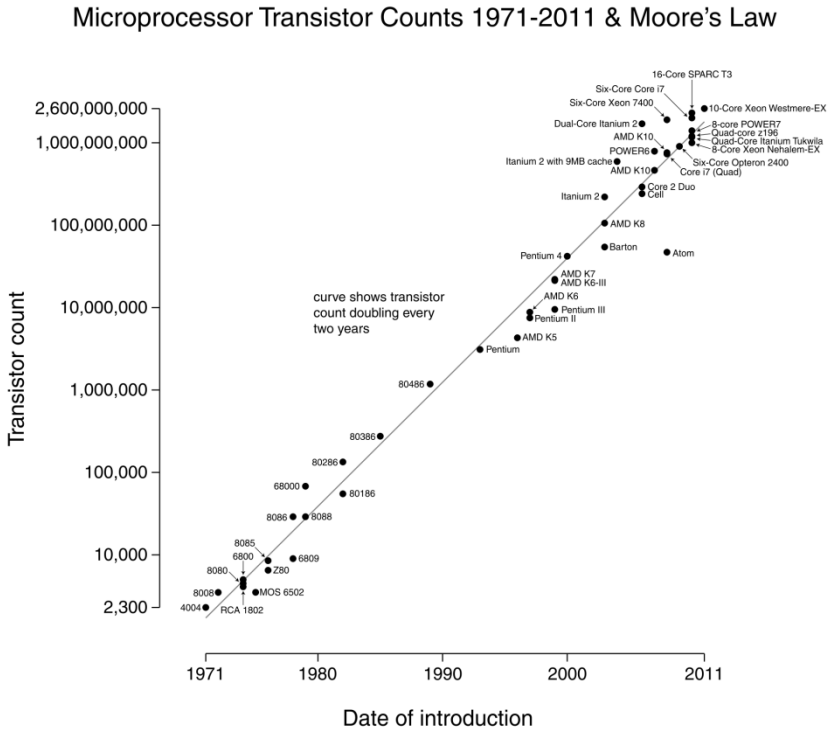

Figure I-2: CPU transistor counts against dates of introduction; vertical scale is on logarithm, and the fitted line corresponds to exponential growth: the transistor count doubling every two years

While Moore's Law only describes the rate of increase in transistor density, reduction of the physical MOS device dimensions has improved both circuit speed and density. Technology scaling is the critical parameter of transistor roughly scaled by a factor α (α ≈ 0.7) in every generation (2 years). In 1974, Dennard proposed a scaling rule: constant field scaling [DENN74], all device dimension are scaled by the same factor "α" and the supply voltage and other voltage (as threshold voltage) are also same scaled to maintain a constant electric field throughout the device. See Figure I-3.

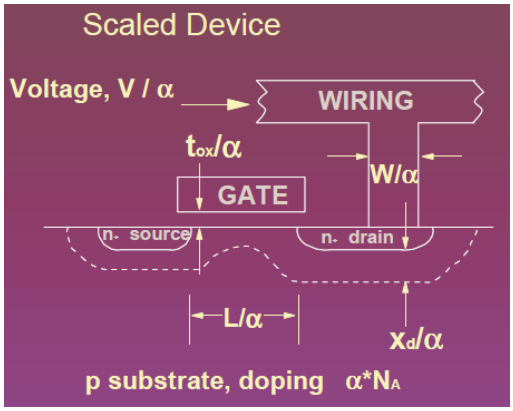

Figure I-3: Constant field scaling

The critical dimensions of transistor: gate voltage (Lg), gate width (Wg), equivalent gate oxide (SiO2) thickness Tox and Source/drain extension junction depth (Xd) are scaled by α α (L'=L/α). The power supply is scaled with the same trend. These lead to the advantage consequence in transistor performance, as illustrated in Table I-1.

Parameters	Constant field scaling	General scaling	Expression
Gate length: Lg	α	α	Scaling variables
Gate width: Wg	α	α	
Gate oxide thicαness: Tox	α	α	
Junction depth: Xj	α	α	
Supply voltage: Vdd	α	u (u < α)	
Substrate doping: Na	1/α	u/α²	
Resistivity: ρ	1	1	
Permeability : u	1	1	
Space between wires: s	α	α	
Wire thickness: tw	α	1	
Electric field(vertical/lateral)	1	u/α	Vdd/Tox or Vdd/Lg
Die area:A	α²	α²	W*L

Transconductance: β	1/α	1/α	(W/L)/Tox
Gate capacitance: Cox	α	α	W*L/Tox
Drain current: Ion	α	u^2/α	$\beta(Vdd - Vth)^2$
Resistance: Ron	1	α/u	Vdd/Ion
Gate delay: τ	α	α^2/u	Ron*Cox
Clock frequency: f	1/α	u/α^2	1/ τ
Power dissipation: P	α^2	u^3/α	Vdd*Ion
Power density: Pd	1	u^3/α^3	P/A
Wire sheet resistance: R□	1/α	1	ρ/tw
Metal resistance: Rw	1/α	1	R□*L/W
Metal inductance: Lw	α	α	u*s*L/W
IR drop	1	u^2/α	Ion*Rwire
L*DI/Dt	α^2	u^2	L*DI/Dt (t: constant)

Table I-1: Transistor scaling and its consequences

The original form scaling could reduce the gate delay and hold the power density constant. But for the reason of compatibility of power supply in the system design, the supply voltage needs to be consistent with the system specification. Constant field scaling was replaced with constant voltage scaling at 1980, and instead of remaining constant , the electric fields inside the device increased from generation to generation until the early 1990s, when excessive power dissipation and heating, some reliability degradations caused serious problems with the stronger electric field. Now, general scaling rule, the combination of the two scaling paradigms is used in practice (Table I-1).

1.2. Limitations of technology scaling and critical issues for circuit reliability

Due to the atomic limits, the key parameter as gate length could not scale indefinitely. Alternate process technology has been developed to continue the Moore's law.

The gate oxides have been shrinking in thickness right along with the gate length shrinks. With the gate length shorter than 90nm, the gate thickness is reaching to 2nm which only representing 6 to 7 atomic layers of silicon dioxide (SiO2). SiO2 is less and less as a good insulator and electrical leakage will become serious until unacceptable, which could increase the static power consumption of the

circuit. The required gate oxide thickness for a quality gate control depends on the capacitances of the film. It is proportional with dielectric constant value (k) and inversely proportional to the thickness. If an alternate material could be found with a higher k value, then the same capacitance could be achieved with a physically thicker film and potentially lower leakage. The concept of equivalent oxide thickness is introduced to compare performance of high-k dielectric gate with SiO2 based gate. For example, if the SiO2 k value is 3.9, shrink the EOT to 1nm would result from the use of a 10nm thick dielectric featuring k=39;

Even so, sustaining the pace of progress is not straightforward. Along with the advancement of circuit performance, several side-effects detrimentally affect the circuit performances.

In practice, we use the general scaling rule combination of constant field scaling and constant voltage scaling, where the scaling variables don't scale in the same way. Figure I-4 shows the trends of power supply voltage, threshold voltage, and gate oxide thickness versus channel length for high performance CMOS technologies [TAUR99].

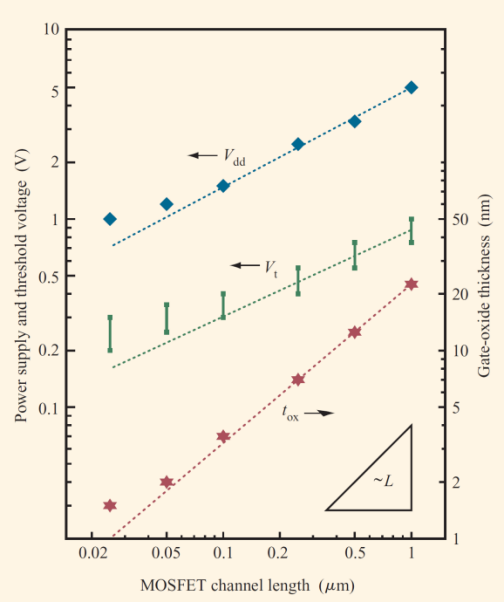

Figure I-4: History and trends of power supply voltage (Vdd), threshold voltage (Vth) vs. channel length for CMOS logic technologies.

With the scaling theory, threshold voltage (Vth) should scale at the same rate as the other device, however, with the consideration of static power consumption, Vth could not be reduced with the same trend. Sub-threshold current which dominates the total leakage current varies exponentially with Vth. Power supply voltage has to keep certain gap with Vth to maintain a reasonable gate over drive. That is why that the power supply voltage has not been decreased at a linear rate to the channel length and oxide thickness. It means that the electric field has been gradually rised over the generations. This induces some reliability problem as Negative Bias Temperature Instability (NBTI), Time Dependent Dielectric Breakdown (TDDB), Hot Carrier Injection (HCI), and Electro-Migration (EM)…The asymmetrical scale between power supply and device dimensions can also increase the power density of the chip, consequently raising the junction temperature. Furthermore, with the technology moving towards lower CMOS technology nodes, the new materials introduced additional

failure mechanisms and made existing aging effects more severe [GIEL11]. All of these above could accelerate the degradation of circuit reliability.

Even more, with the CMOS technology scaling, power supply voltage has a constantly decrease, associated noise margin which has been cut by a factor of 10. Although the voltage reduction slows down in the recent generations, the noise margin is expected to cross the 100mV line by 2015 (Figure I-5). A reduced noise margin means an increased sensitivity to interference in either time or frequency domain. On the other side, the increase of operation frequency and IC complexity create more switching noise (di/dt), which make the IC becomes the more important noise source.

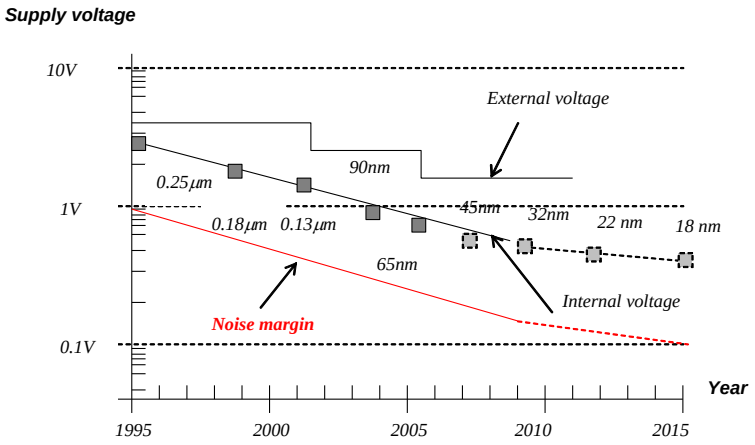

Figure I-5: The continuous decrease in supply voltage.

As mentioned above, with the technology evolution, along with the circuit performance improving, the IC design is subjected to more and more serious EMC and reliability problem. In the next two sections, we will give a detailed description of Electromagnetic compatibility and reliability problems of ICs.

2. ELECTROMAGNETIC COMPATIBILITY OF INTEGRATED CIRCUITS

Electromagnetic compatibility is the ability of a device or electronic system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to any other systems in that environment. The EMC expert must ensure the simultaneous operation of all nearby electric or electronic devices and the safety of users for a given electromagnetic environment: the control of device emission. (Figure I-6)

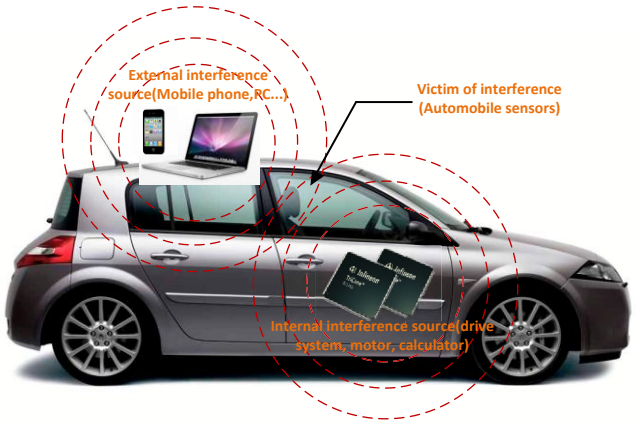

Figure I-6: The illustration of electromagnetic interference in an automobile system. (Device emission)

The personal electronic entertainment products like: laptop, cell phone… emit radiofrequency waves inside the car, whereas the high frequency microcontroller used in vehicle can also generate electromagnetic interference (EMI). More and more the wireless communications create interference with frequency up to 2.4GHz. All of these could make the electromagnetic environment more complicate. So it is important that at the design level, the emission is limited under certain level, to avoid not disturbing other equipment.

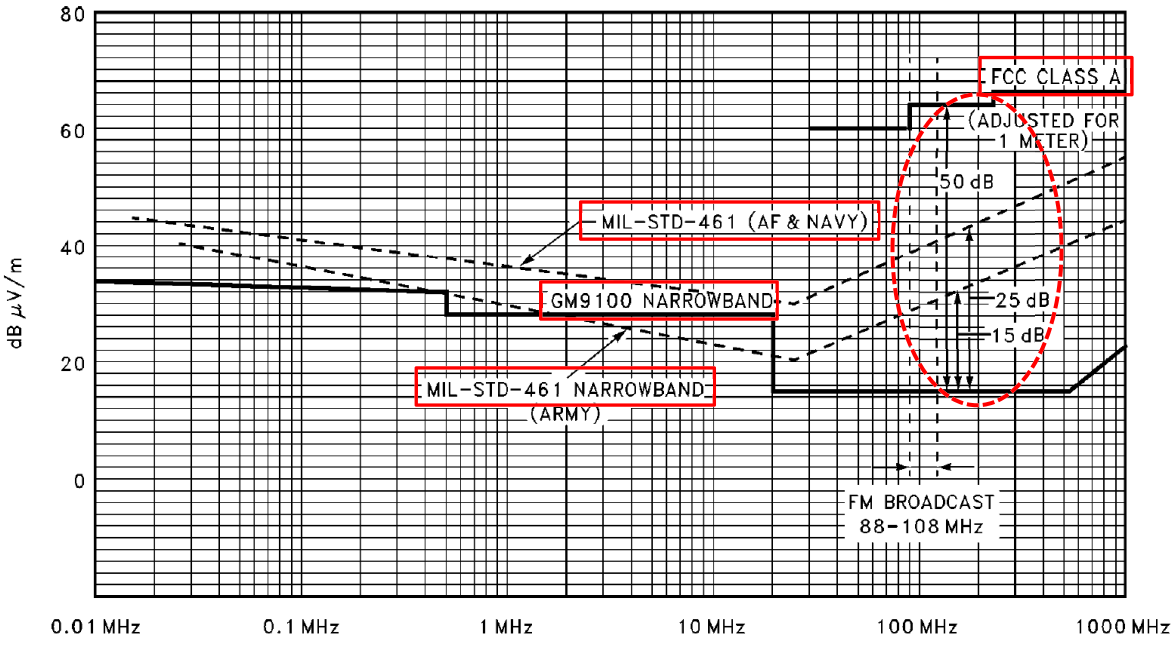

Figure I-7: Comparison of radiated emission specifications of commercial application (FCC), Military and Automotive [INTEL1996]

The radiated emission level is limited between 20dBuV to 80dbuV range (10μV to 10mV) according to the varieties of applications and operation frequency range. Figure I-7 compares the three standards of commercial FCC limits with both military (MIL-STD-461) with the general motors vehicle device limits (GM9100) for radiated emissions (all three sets of limits have been normalized to a 1 meter measurement distance). In the FM broadcast range (88 – 108MHz), the automotive limits are

about 6 µV/m (15dB µV/m), which is about 300 times (50dB) more stringent than corresponding commercial emission limits, and about 6 to 20 times (15-25dB) more stringent than corresponding military limits [INTEL 1996].

On the other side, integrated circuits are widely used in the electronic system making them become the ultimate victims of electromagnetic interference, as illustrated in Figure I-8.

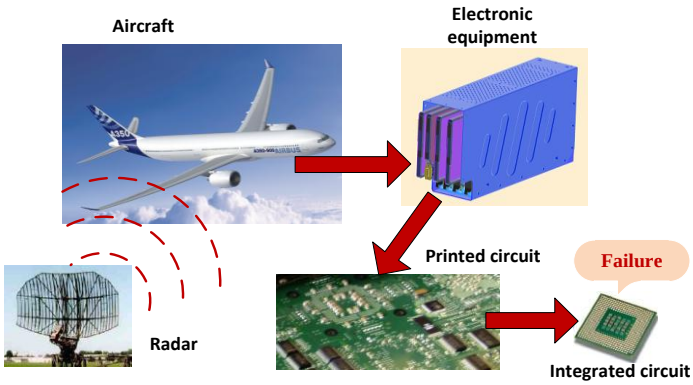

Figure I-8: The illustration of electromagnetic interference injected in electronic systems from a disturbance source and coupled in the end to the integrated circuit. (Device immunity)

The RF noises radiated from Radar could disrupt the electronic equipment on the aircraft, and these noise coupled on the track of Printed Circuit Board (PCB) could affect the operation of integrated circuit ultimately. The immunity of integrated circuit should be considered in its design level, to be able to resist a certain level of disturbance.

The study of EMC of ICs contains two aspects [IEC 61000]:

- Emission: The phenomenon by which electromagnetic energy emanates from a source.
- Immunity (or Susceptibility): The ability of a device, circuit or system to perform without degradation in the presence of an electromagnetic disturbance.

2.1. Origin and consequence of emission of ICs

2.1.1. Basic mechanisms of electromagnetic emission

Electromagnetic emission is first caused by power rail voltage bounce which is induced by switching activity of ICs[TANG02], transient current circulation within the circuit and its direct environment (PCB, cables). It is also known as *Simultaneous Switching Noise (SSN)*.

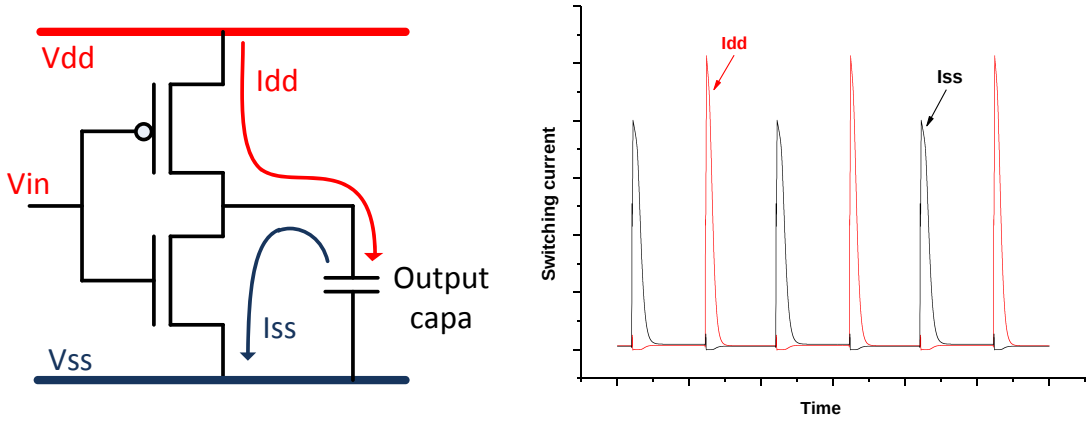

Figure I-9: CMOS inverter internal activity, transient current flow from Vdd to charge and from charge to Vss

Take CMOS inverter as an example, shown on Figure I-9, there is a current consumption during the short period corresponding to charge or discharge of the output capacitor, where the current peak value depends on the saturation current of each transistor and the number of the switching gates.

However, transient current itself does not produce directly voltage bounces. Suppose the gap between ideal power supply and ground voltage references should remain constant whatever the consumed current is. In practice, the IC is connected to a non-ideal voltage reference (battery, voltage regulator; ground plane) through interconnections formed by package leads, PCB tracks and cables. However, these interconnections are not perfect conductors, due to several parasitic effects represented by electrical elements such as resistor, inductor, and capacitor. Consequently interconnects cannot be considered as equipotential. Thus the wires can convert the transient currents into voltage drops on power and ground supplies (Figure I-10)

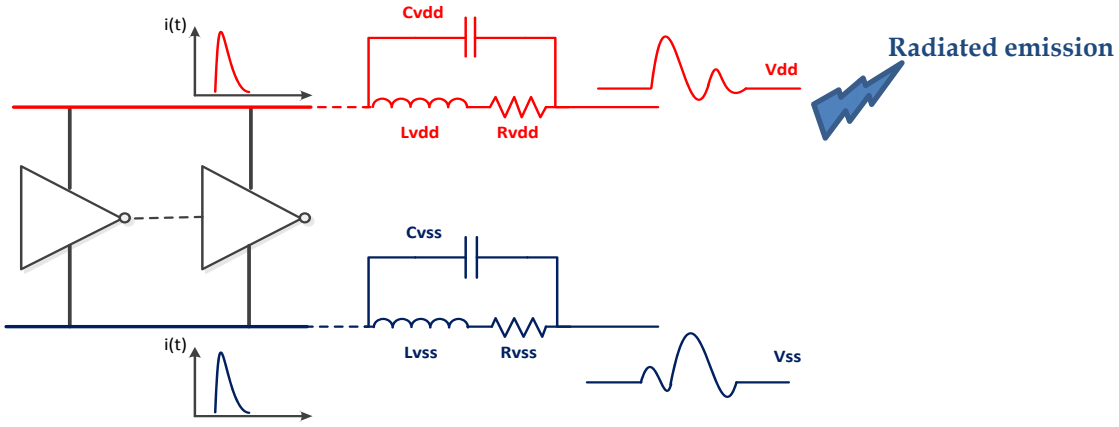

Figure I-10: IC parasitic emission due to switching activity and parasitic power supply interconnections

The power rails can be modeled by a lumped RLC circuit. Parasitic inductances of interconnections are the main response of voltage drops [SENT91]. The conversion of transient current to voltage bounces by inductances is called ΔI *noise*, given by Equation I-1

$$\Delta V_{\Delta Inoise} = L\frac{di}{dt} \qquad \text{Equation I-1}$$

Furthermore, the parasitic resistances on power rails, ranging from 100mΩ to 10Ω depend on the technology and the circuit size [VRIG05-a]. The noise due to transient current flows through the parasitic resistance called *IR noise*. While the Δ*I noise* leads to a voltage fluctuation, the IR noise results in a voltage drop and could degrade the switching speed of the logic gate [AJAM03]. However, the resistance on the power rails could damp the oscillations produced by the Δ*I noise*. Thus, the switching current is calculated from the accumulation of both effects as a function of switching current, as shown in Equation I-2.

$$V_{SSN} = R \cdot i + L\frac{di}{dt} \qquad \text{Equation I-2}$$

The *Simultaneous Switching Noise* induced by voltage bounce may propagate in circuit by the sharing power supply network, which causes conducted emission. Moreover, current flows and voltage bounce along the interconnections generate electromagnetic fields (according to Maxwell equations) which are responsible of radiated emission.

The electromagnetic emission is dependent on the parameters listed in Table I-2:

Influent circuit parameters	Comments
IC internal activity	The Internal Activity (IA) generates a parasitic transient current which flows within the circuit. Thus, a large digital core or parallel I/O buses generate a strong emission because of frequent charge/discharge cycles. The IA is characterized by the amount of current and the duration of current peak → di/dt. Both parameters are dependent on circuit technology and the number of switching elements.
Load connected to the circuit	A large capacitive load induces significant charge transfers and hence parasitic emission. Basically I = C*dV/dt = C* power supply/switching time. Thus if capacitance is large, transient current will be large.
Filtering effect of the circuit	Interconnections, on-chip decoupling capacitor and parasitic coupling paths have an influence on propagation of parasitic current flow within a circuit. They can contribute to keep parasitic current flow internal to the circuit and reduce supply voltage fluctuations in the best case, or create leakage paths which can disturb sensitive blocks. ΔV = Csw/ (Csw+Cdec)*Vdd, Csw is equivalent capacitance of the switching gate and Cdec is the decoupling capacitance.

Table I-2: Influent circuit parameters on electromagnetic emission [SICA09]

2.1.2. Influence of IC technological evolution on emission

The parasitic emission caused by the switching activity of ICs has increased significant with the tremendous progress in CMOS technology. According to the International Technology Roadmap for Semiconductors (ITRS) [ITRS05], the 32nm CMOS process would be available in 2010, featuring a standard operation frequency near 50GHz for processing units, and the capability to integrate within 3x3 cm silicon would be nearly one billion devices.

The main source of parasitic emission, switching current, depends on two main parameters: the transient current amplitude and the operation frequency clock of the IC. The trend of technology influences the operating frequency of the ICs with significantly large effects on current peaks. They become narrower and sharper, which in turn expand the noise frequency range on the emission spectrum.

With the progressive miniaturization of CMOS devices, even though the current peak produced per gate has continuously been reduced, the gate density and circuit complexity increase. Consequently, current peaks at circuit level increase for each generation (see Table I-3).

Technology	Power supply(V)	Density of gate (/mm²)	Current peak per gate (mA)	Current peak density (A/mm²)
1.2µm (1985)	5 V	8 K	1.1	8.8
0.8µm (1990)	5 V	15 K	0.9	13.5
0.5µm (1993)	5 V	28 K	0.75	21
0.35µm (1995)	5 – 3.3 V	50 K	0.6	30
0.25µm (1997)	5 – 2.5 V	90 K	0.4	36
0.18µm (1999)	3.3 – 2.0 V	160 K	0.3	48
0.12µm (2001)	2.5 – 1.2 V	240 K	0.2	48
90nm(2004)	2.5 – 1.0 V	480 K	0.1	48
65nm(2006)	2.5 – 0.7 V	1000 K	0.07	70
45nm(2008)	1.8 – 0.8 V	2000 K	0.05	100
32nm(2010)	1.8 – 0.8 V	3000 K	0.04	120

Table I-3: Evolution of current peak of the IC [BOYE07]

As ICs integrate numerous functions located in different blocks, often working in parallel, the global current peak corresponds to the sum of the current consumption of each elementary block. Consequently, the more gates are synchronous switching, the more global current amplitude increases. For normal typical processor, only a small portion of gates are active during one clock cycle, a typical value is given by a proportion between 10% and 30% [BEND06]. As an example of 16-bit microcontroller (Figure I-11), with i (i is the activity factor represents the number of switching gate) logic gates switching simultaneously, the theoretical result should be 0.45*i mA! At the present, gates and interconnect delays spread out and reduce the current peak by approximately a factor of j (j is the spread factor, j>1). Thus a peak of 0.45*i/j mA (<0.45*i mA) on 400*j ps is obtained.

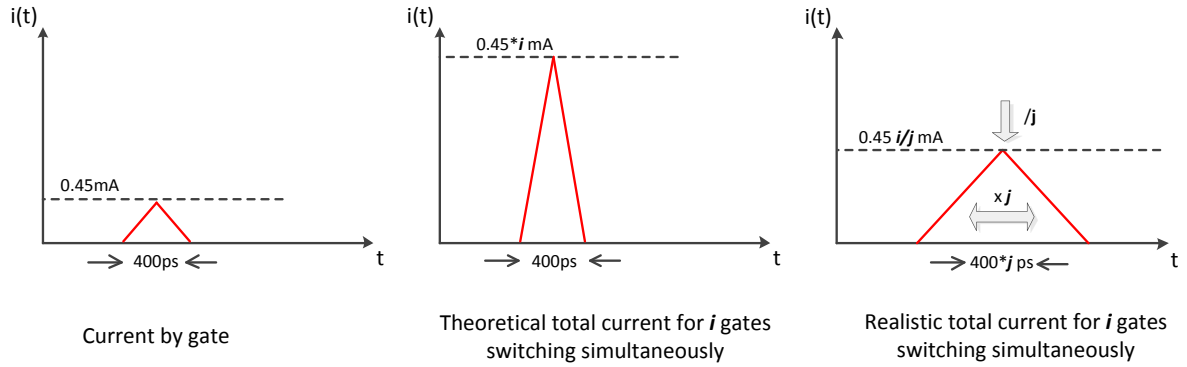

Figure I-11: Current peak generated by a core of i switching gates.

Due to this augmentation of transient current, the conducted and radiated parasitic emission generated by ICs become more and more important for both IC manufacturers and customers.

2.1.3. Measurement methods for the characterization of integrated circuit emission

Systems manufacturers using ICs must ensure that their emission levels do not exceed the authorized limitation. Therefore, they force more and more IC manufacturers to pay attention to the IC emission. To ensure the EMC compliance of their applications, the IC manufacturers had to follow the standards for measurement to characterize the noise generated by ICs. These standards are grouped under the IEC-61967 [IEC 61967]. Most of them are derived from measurement standard for system as CISPR25 used in the automobile electromagnetic emission characterization. The Figure I-12 shows the standard of IC emission measurement, which is detailed in Table I-4.

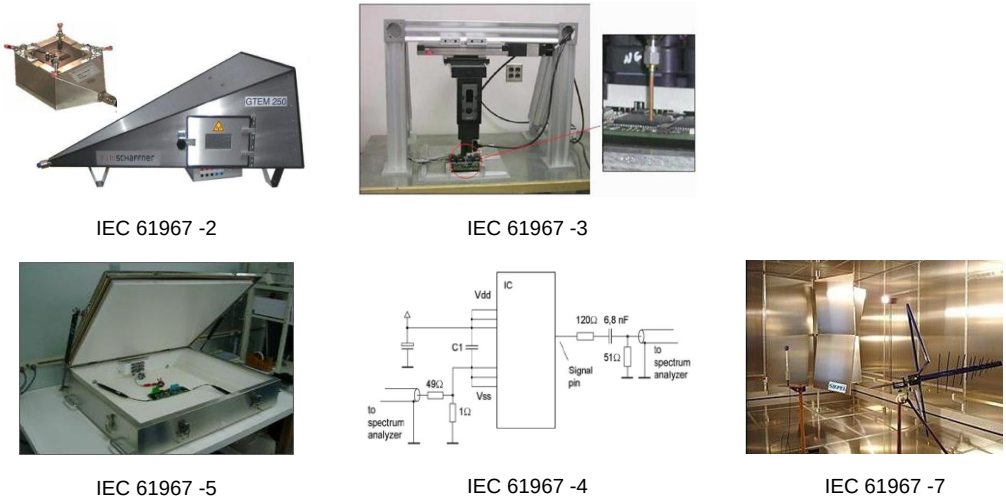

Figure I-12: IC emission measurement methods

Standard	Description	Type	Frequency range
61967-2	TEM/GTEM cell	Radiated	150kHz – 18GHz

61967-3	Surface scan	Radiated	10kHz – 3GHz
61967-4	1Ω/150Ω	Conducted	150kHz – 1GHz
61967-5	Workbench Faraday cage	Conducted	150kHz – 1GHz
61967-6	Magnetic probe	Conducted	150kHz – 1GHz
61967-7	Reverberant chamber	Radiated	100MHz – 18GHz
61967-8	IC stripline	Radiated	150kHz – 3GHz

Table I-4: Description of IC emission measurement standard IEC 61967

2.2. Origin and consequence of immunity of ICs

2.2.1. Basic mechanisms of susceptibility to radiofrequency interferences (RFI)

Susceptibility to electromagnetic noise has played a significant role in the design of ICs for many years and remains a major concern with the multiplication of powerful parasitic sources which can affect circuit behavior (Figure I-13), classified by artificial sources (as communication transmitters, AC high voltage power lines, radar…etc.) and natural sources (such as lightning, solar radio noise…etc.) [RAMD09].

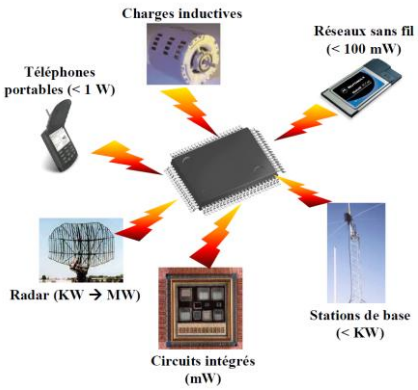

Figure I-13: Sources of electromagnetic noise of IC

The power level and frequency range are the main criteria which characterize an electromagnetic disturbance. (Figure I-14)

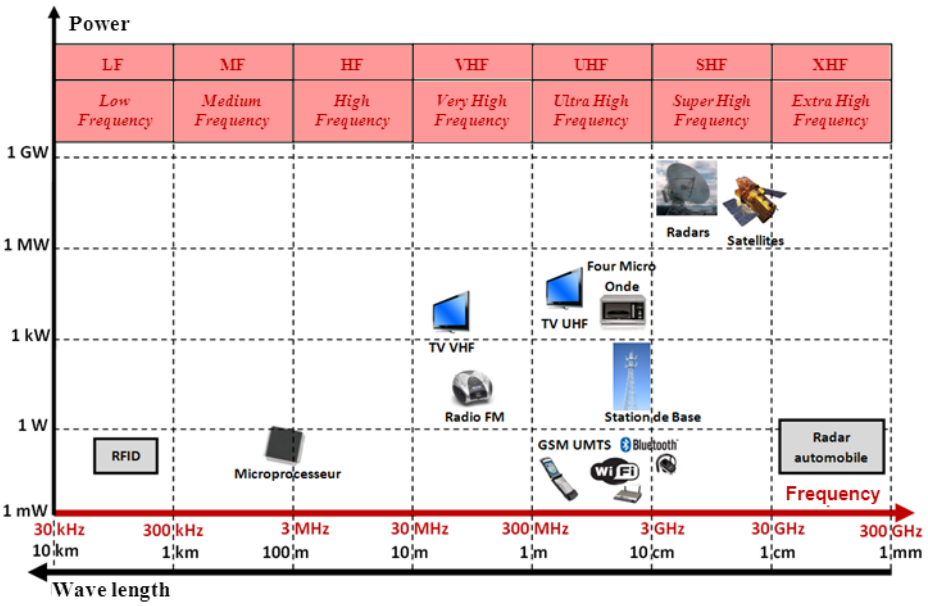

Figure I-14: Distribution of spectrum of electromagnetic noise

Below, we give a non-exhaustive but relatively representative of the interference mechanisms currently meeting in practice.

- The wireless communications:

As shown in Figure I-14, the radio frequency spectrum is used for many wireless telecommunications applications. First, for long distance television and radio broadcasting, the transmit power is very high (several kilowatts), but fortunately, the number of transmitter is small. Then, the transmit power of local networks or short distance wireless systems like Bluetooth or Wi-Fi, are much lower (only a few tens of milliwatts), but the number of sources in those scenarios is much more. With this type of communication, transmitter generates a continuous harmonic signal narrowband-modulated by frequency or amplitude. Thus the polluted frequency band is limited by the bandwidth of the emitter. Cell phone is also a main source of disturbances, more common than the two above. Several standards exist today: GSM (around 900MHz), DCS (around 1.8GHz) and UMTS (between 1.9GHz to 2GHz). The power depends on sources, either the base station or the cell phone. This means that the base station can emit signal up to several hundred watts, while the power emit by cell phone does not exceed 1W. The signal is also a sinusoidal carrier modulated by frequency and phase, but the emission is not continuous and within the form of impulse train or bursts. Finally, we can also mention the use of low power wireless links (a few tens of milliwatts) in application such as radio frequency identification (RFID) and pressure sensors embedded in the automobile tires.

- The Radars :

Unlike the radio and television broadcasting, radars are not the common disturbance sources. They are related with the risk of interference to electronic systems used in aviation or military. The radars are the source of high energy disturbances, their signals spectrum can cover from several hundred MHz to hundred GHz with very high power (a few kilowatts to several MW) and the radar

beams are focused on localized areas. Thus, their affected area could extend for several kilometers along the radar beam.

- Integrated circuits :

As we discussed in the previous parts, ICs are the sources of parasitic electromagnetic field due to their internal activities. The disturbance levels are low (a few milliwatts to several watts), but its spectrum covered widely. Unlike the other source of interferences present above, this is an internal disturbance of the system. The noise generated by logic cell, is coupled from the IC package to larger structures that act as antennas such as circuit boards planes, heatsinks or cables.

- Electrostatic discharge :

Electrostatic discharge is a sudden and momentary electric current that flows between two objects at different electrical potentials, caused by direct contact or induced by an electrostatic field. ESD is a high-voltage transient with fast rise time and fast decay time. When a static charge moves, it becomes a current that damages or destroys gate oxide, metallization, and junctions. ESD can occur mainly in three ways (see Figure I-15): a charged body touches an IC (Human body Model - HBM); a charged IC touches a grounded surface, causing sensitive devices damage in the discharging path (Charged Device Model – CDM); and a charged machine can touch an IC, discharging through a device to ground, than cause the damage (Machine Model- MM);

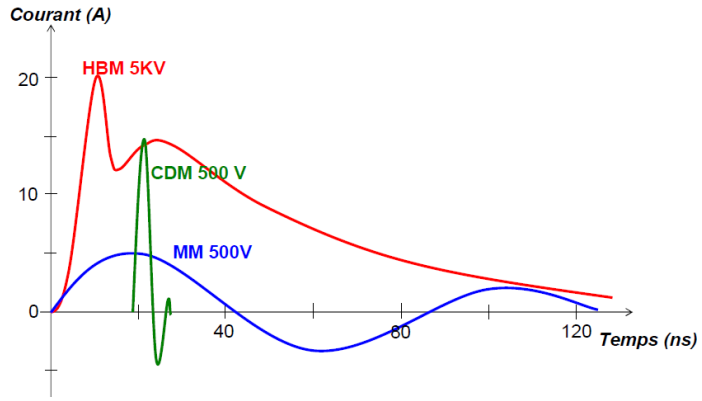

Figure I-15: Three electrostatic discharging models.

To avoid the consequences caused by this transient energy, many protection circuits are integrated into ICs. Nonlinear structures as diodes and transistors are regularly used in this protection design, especially for input/output blocks to prevent the destruction risk.

- Other electromagnetic interference sources :

Except the main sources mentioned above, there are some other sources of EMI. Lightning during the thunderstorm, it induces electromagnetic emission (EME) which propagates over distances ranging up to thousand kilometers, causing spikes or sharp random pulses in the electromagnetic spectrum. The spectral components of lightning span a wide range of frequency, from a few Hertz to over 100MHz. Another source is the cosmic radiation; it includes solar radiation as well as galactic noise, although the thin shield of Earth's magnetic field can trap charged particles and protect the Earth surface from the cosmic radiation, the satellites orbiting around the Earth and the aircraft in high altitude are vulnerable.

2.2.2. Interference coupling mechanisms

EMC issues associated with integrated circuit can generally be classified as externally-coupled and intra-chip.

- Externally-coupled EMC problems: when signal or noise is generated on an IC interfere with circuits or devices off-chip, or conversely when noise is generated externally interferes with the proper operation of the IC.
- Intra-chip EMC problems: when a signal or noise is created in one or more circuits interferes with the operation of another circuit on the same chip.

As for intra-chip or externally-coupled issues, the noise coming from the interference source transmits to the victim by principal three manners: radiative, conductive, or near field coupling; illustrated by Figure I-16:

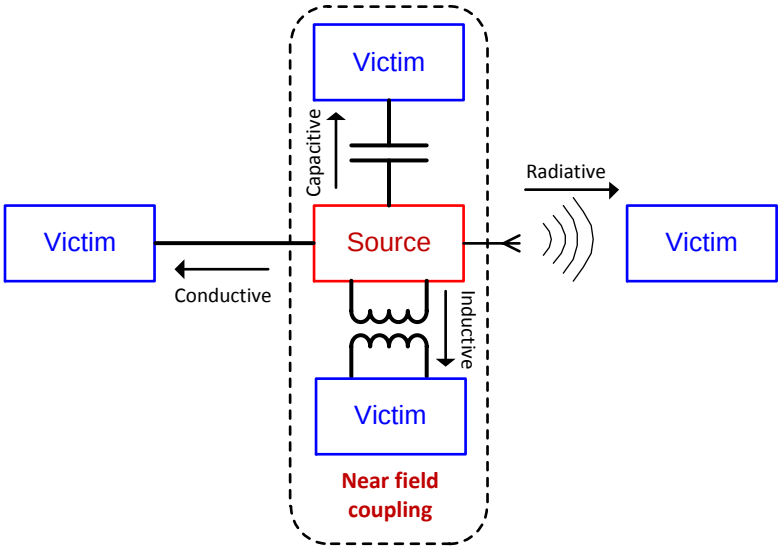

Figure I-16: Three electromagnetic interference coupling modes.

2.2.2.1. *Radiative coupling*

Radiative coupling or electromagnetic coupling is the transfer of electromagnetic energy over distances generally greater than a few wavelengths (far field), the metallic part of device can function as the antenna to transmit or receive the energy. As we introduced in the 2.2.1 paragraph, the frequency of the electromagnetic interference in our environment covers up to tens or hundreds GHz, the victim by electromagnetic radiation could be from the large scale system to the small chips. (Figure I-17)

From the theory of antenna, we use the usual criterion of one quarter of the wavelength ($\lambda/4$) as the scale. For the frequency range from 3 to 30 MHz, the disturbance may couple efficiently to very large metallic structures such as airplanes or cars. From 30 to 300 MHz, the most efficient antenna effect occurs for metal connectors around tens of centimeters, while from 3 to 30 GHz, the antenna size

is the order of some millimeters. At these frequencies, any metallic conductors (from PCB tracks to package leads) can act as an antenna and collect a large amount of noise [BOYE09].

But in interference source point of view, integrated circuit package or lead frames are too small to radiate effectively at frequencies below 10GHz. At frequencies where the packages are large enough to radiate efficiently, the thin metallic structures in the package tend to be very lossy. As a result, the radiation of electromagnetic energy directly from an IC is hardly a significant problem. If the radiation antenna made by the conductor outside the IC, it should be other coupling mechanisms as near field coupling or conducted coupling.

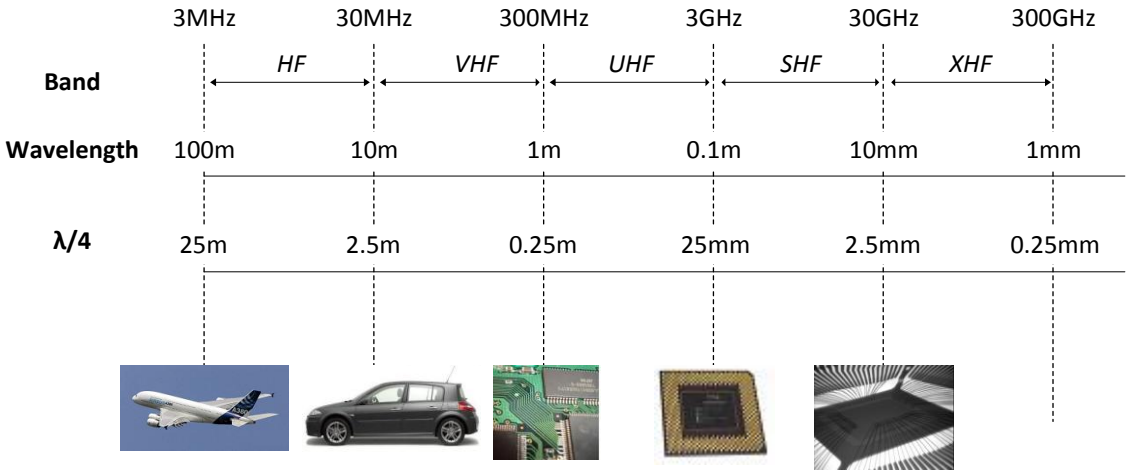

Figure I-17: Distribution of spectrum of electromagnetic noise

2.2.2.2. *Near field coupling*

There are two different energy transfer modes, electric field coupling (capacitive coupling) and magnetic field coupling (inductive coupling). The typical EMC problem crosstalk, which the voltage or current in one circuit is unintentionally coupled to another circuit. A part of crosstalk is caused by these capacitive and inductive couplings.

- Electric field coupling: occurs when electric field originates from one conductor in one device and terminates on the conductor in another circuit. This can be represented schematically by a parasitic capacitance between the two conductors. As an example in practice: coupling between closely signal conductors is illustrated in Figure I-18. Another example is the coupling between the IC surface and its heat sink due to voltage difference.

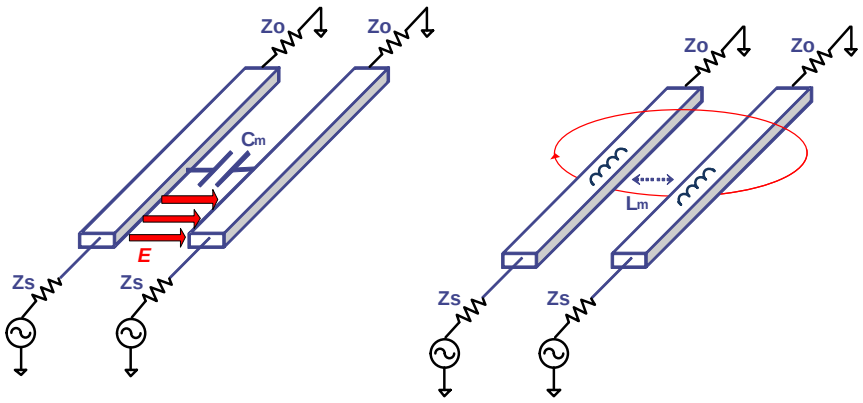

Figure I-18: Electric field coupling (left) and Magnetic field coupling (right) between two signal rails.

- Magnetic field coupling: occurs when magnetic fields produced by the time-varying current in a source circuit "couple" of a second circuit. This is similar to the coupling between the primary and secondary of a transformer, as one example in Figure I-18. Another example in practice is the magnetic field generated by device link to the circuit loop outside the chip, as the board trace or cable loops.

2.2.2.3. *Conductive coupling*

The conductive coupling (also called common impedance coupling) occurs when the coupling path between the source and the victim, e.g. PCB track or common ground plane. Common impedance coupling is one of the crosstalk mechanisms, as an example shown in Figure I-19.

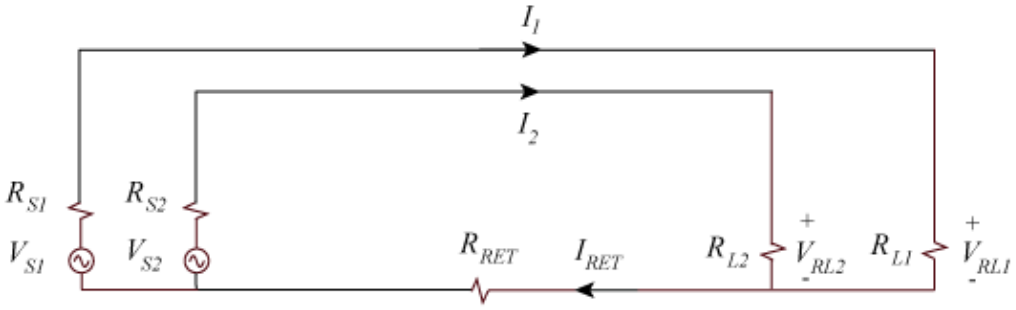

Figure I-19: Two circuits sharing a common signal return [BEND06]

Two circuits share the common ground bus. If the ground impedance is zero, the voltage across each circuit's load R_{L1} and R_{L2} would depend only on their source V_{S1} and V_{S2}. However, the finite impedance in their shared ground causes a voltage to appear R_{L2} when there is a signal in V_{S1} and vice versa. Another conductive coupling problem is due to Simultaneous Switching Noise (SSN) transmission on the shared power rails, which is mentioned in 2.1.1, also known as ground bounce, power bounce. When a circuit draws current from the power rails, a small voltage drop across the bus affects all the circuit shared in these power rails.

2.2.3. Effect of electromagnetic disturbance on IC

2.2.3.1. IC failure classification

The standard IEC 62132 [IEC 62132-1] gives the grade of electromagnetic disturbance effects on IC. The performance class has five levels based on their function resistance exposed to the interference. As shown in Table I-5.

Class	Description
A	All functions of the IC perform as designed during and after exposure to a disturbance
B	All functions of the IC perform as designed during exposure. However one or more of them may go beyond the specified tolerance. All functions return automatically to within normal limits after removing the disturbance.
C	A function of the IC doesn't perform as designed during exposure but returns automatically to normal operation after exposure is removed.
D	A function of the IC doesn't perform as designed during exposure and doesn't return to normal operation until exposure is removed and the IC is reset
E	One or more functions of an integrated circuit does not perform as designed during and after exposure and cannot be returned to proper operation

Table I-5: Description of IC emission measurement standard IEC 61967

Susceptibility of circuit is strongly dependent on the disturbed block type and circuit design. Facing to the electromagnetic interference, the main two types of IC, digital circuit and analog circuit are affected differently [REDO09]. So it is essential to understand the behavior of digital and analog circuit in the presence of EMI.

2.2.3.2. Digital circuits susceptibility

Digital circuits are inherently less susceptible to EMI than their analog counterparts, as they benefit the logical level threshold, and hereby predisposed to have a natural resistance against interference. However, it should be pointed out that although digital circuit exhibits a lower susceptibility to EMI, this does not mean that they are completely immune to it. EMI has been observed to have two distinct effects on digital circuit. The first is false switching or static error, which occurs when interference is of sufficient amplitude to cause logic state changing. The second effect is EMI-induced delay or dynamic error, which is the change of propagation delay owing to the EMI. It has been observed that the second effect occurs at much lower amplitude of EMI than the first effect [CHAP97].

2.2.3.2.1. *Static error*

Digital circuit's logic state stability relates to its static noise margin, which is the amount margin of the signal level for logic state "0" and "1". As illustrated in Figure I-20.

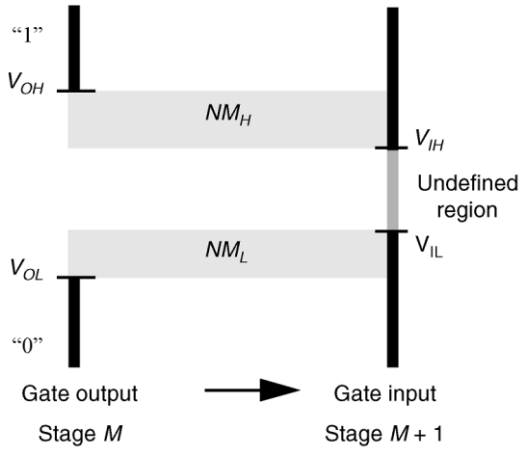

Figure I-20: Cascaded inverter gates: definition of noise margins [RADA03]

Take the simple example of invertor in digital circuit, for a gate to be robust and insensitive to noise disturbances, it is essential that the logic state margin should be as large as possible. A measure of the sensitivity of a gate to noise is given by the noise margins NML (noise margin low) and NMH (noise margin high), which quantize the size of the legal "0" and "1", respectively, and set a fixed maximum threshold on the noise value, as shown in Equation I-3.

$$NM_L = V_{IL} - V_{OL} \qquad \text{Equation I-3}$$

$$NM_H = V_{IH} - V_{OH}$$

The static noise margins represent the levels of noise that can be sustained when gates are cascaded, due to the noise or output load, the output signal of Stage M could deviate from the expected nominal value. If this deviation is inside the acceptable region (NML and NMH), the digital circuit could hold its proper operation, inversely, if this deviation exceeds the static noise margin, and goes inside the undefined region, the logic state of the circuit output could not be assured. See an example in Figure I-21:

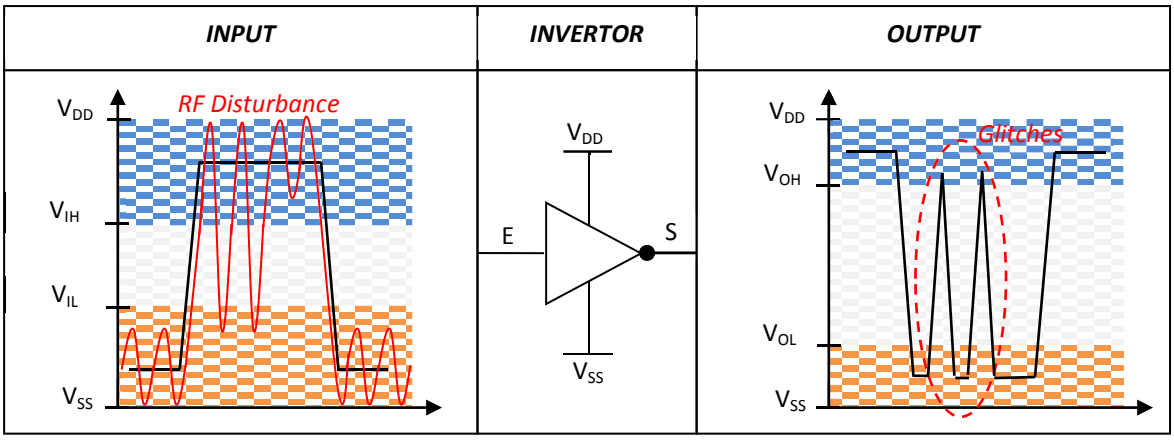

Figure I-21: False switching of the an invertor

The input signal of invertor coupled a RF disturbance, if the level of the signal sufficient to go out of the static noise margin, the output of the invertor will have some undesirable variations, as the error "glitch" in this example.

2.2.3.2.2. *Dynamic error*

If the EMI-induced RF disturbances are lower than the static noise margin limits, they would not change the digital circuit logic states. Yet, they may still affect the operation of the circuit by changing the propagation delay of the signal [CHAP97].

It defines the dynamic noise margin, delay margin, to be the maximum allowable change in the time of a signal which the circuit could continue to operate properly. A positive and a negative delay margin are associated with every signal transition, representing the latest and earliest allowable arrival times, respectively, relative to the nominal time of arrival of the transition. See an example in Figure I-22:

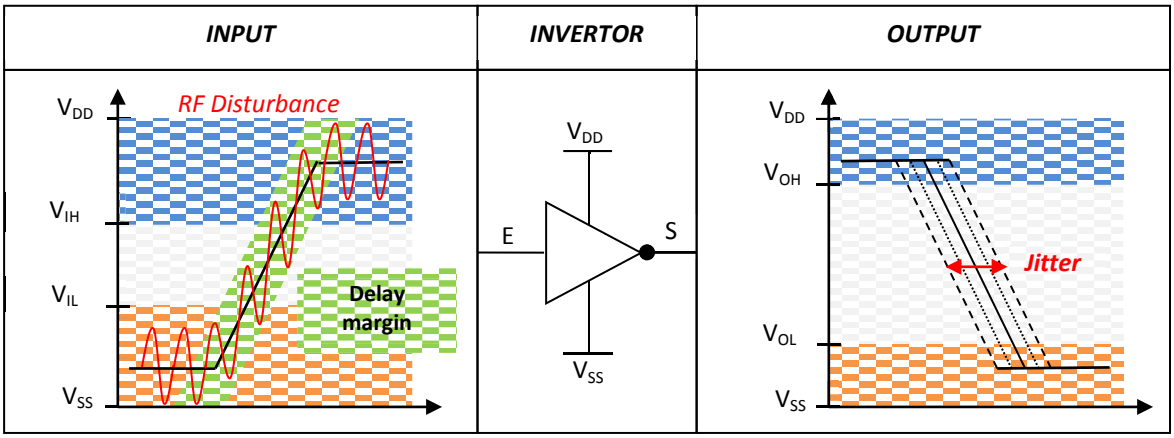

Figure I-22: Dynamic error of the an invertor

If the EMI-induced RF disturbance is positive at the moment of transition, then the input signal will arrive earlier than the nominal signal, oppositely. If the EMI-induced RF disturbance is negative at the moment of transition, then the input signal will cross the logic threshold later. The consequence to the output signal will be an amount of timing changing, which is called jitter.

2.2.3.3. *Analog circuits susceptibility*

Unlike digital circuits, analog circuits are more sensitive to electromagnetic disturbances. Their failure, are the particularity to be temporary and disappear as soon as the disturbances removed. Table I-6 gives an example of some analog blocks' sensitivities. It only requires some mV disturbance to disrupt the operation.

Analog blocks	Phase locked loop (PLL)	Analog comparator	Analog to digital converter (12 bits, VDD = 2.5 V)	RF amplifier

Sensible threshold	10 mV	1 mV	600 µV	10 µV

Table I-6: Analog blocks sensitive examples

When EMI is coupled on analog circuit input signal, the circuit treats the noise as an ordinary input signal. Depending on the to the cut-off frequency of the analog circuit, the noise may be in-band or out-of-band. It is difficult to remove in band noise from the input signal, but what we could do is to filter the out-of-band noise, to avoid the nonlinear distortion (rectification) which could induced DC shift [FIRO02].

The power supply fluctuation is another probable failure cause. Indeed, the power supplies are used as reference for analog-digital converter and the power source for the amplifier. Unlike the noise coupled on input of analog circuit, the power supply fluctuation could be easily filtered. Usually, the disturbances lead to a creation of offset. As many analog applications (regulator) are based on operational amplifier (OP-AMP), the offset could lead to their application saturation [FIRO02]. Different solutions related to the input structure of OP-AMP have been proposed to reduce the creation of output offset [RICH04]

2.2.4. Influence of IC technological evolution on immunity

The technology trend pushes towards noise margin lower and lower. Increasing integration of input/output structures and higher bus speed should lead to an increased susceptibility to RFI.

IC immunity strongly depends on its technology, and as we explained in the previous part, the immunity of IC relates to static margin and delay margin. With the technology evolution, static noise margin decreases to less than 0.1V in the 2015 (see Figure I-5). The sensitivity of IC to EMI is increased, and thus less power will be needed to create false switching error.

On the other hand, the period of signal is inversely proportional to the operation frequency. So the higher operation speed means the reducing of the signal period, and also reducing their delay margin. IC would be more vulnerable to the EMI due to the dynamic error.

2.2.5. Measurement methods for the characterization of integrated circuit immunity

Electronic manufacturers have to ensure the robustness of ICs against electromagnetic interferences. ICs must pass susceptibility test measurement suitable for their various applications. There exist two main types of Electromagnetic interference:

- Pulse or transient interference: arises from the source emitting a short-duration pulse of energy. The sources of this type of interference usually are the ESD, lightning, and digital circuit switching activity, motors…;
- Harmonics: arises from the source regularly emitting a given range of frequencies. The frequency range from DC to limit which constantly increases as technology pushes it higher.

This interference includes continue wave, or modulated signal. The typical source of this type of interference is the telecommunication transmission;

In general, the ICs suffer from the pulse or transient interferences in a real operation environment, as the automobile electronic component would be disturbed by pulse interference related to power device switching, load dumps. However, the interest of using harmonic interference allows us to take a harmonic analysis, i.e. how the system performs under a periodic disturbance by analyzing its behavior frequency by frequency. Therefore, in our research, we are interested in the harmonic interference, the coupling mode either conducted or radiated, and applied disturbance are either global or localized on one special part of the device under test (DUT). The characterization methods are defined by a group of test standard IEC 62132 [IEC 62132]. Figure I-23 shows the standards of IC emission measurements which are detailed in Table I-7.

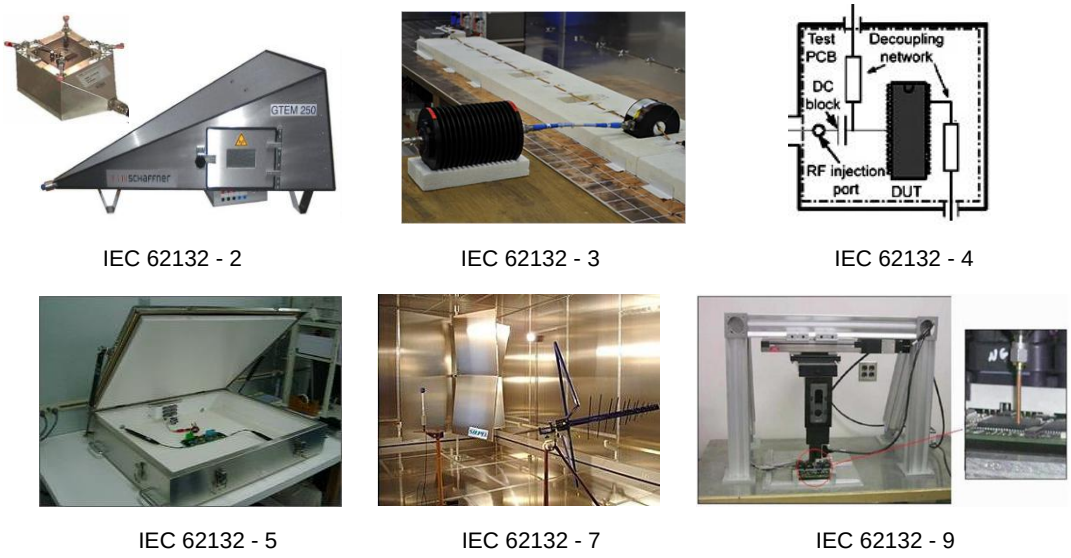

Figure I-23: IC immunity measurement methods

Standard	Description	Type	Frequency range
62132-2	Transverse Electromagnetic Cell (TEM), GigaHertz Transverse Electromagnetic Cell (GTEM)	Radiated	1MHz – 18GHz
62132-3	Bulk Curent Injection (BCI)	Conducted	1MHz – 400MHz
62132-4	Direct Power Injection (DPI)	Conducted	150kHz – 1GHz
62132-5	Workbench Faraday cage	Conducted	150kHz – 1GHz
62132-6	Local Horn Injection Antenna (LIHA)	Radiated	1MHz – 10GHz
62132-7	Mode Stirred Chamber (MSC)	Radiated	100MHz – 18GHz
62132-8	IC stripline	Radiated	150kHz – 3GHz

62132-9	Near field scan immunity	Radiated	150kHz – 1GHz

Table I-7: Description of IC immunity measurement standard IEC 62132

These test measurement methods are closed to the industry need, but mainly under 3GHz, even though the frequency range above 10GHz could be used MSC (Mode Stirred Chamber), it is not used for IC characterization, and the method use for IC has to be investigated in the next years.

2.3. The prediction of EMC for integrated circuits

2.3.1. EMC prediction requirement

With the development of IC in electronic system, the EMC issues have become major concerns of the semiconductor industry. In 1990s, the EMC of IC tests were characterized at the end of the IC design. The non-compliance to EMC regulations problem has become the 3rd re-design source in IC design flow [VRIG05-b] (Figure I-24). IC redesign increases the cost of products and delay the production time to market. It is essential to integrate EMC compliance verification by simulation before the chip fabrication. Moreover, in order to reduce the cost of development of new product, semiconductor industry usually re-uses existing blocks in the design libraries. By creating EMC model library for every functional block, they can simply optimize the EMC performance for the new product.

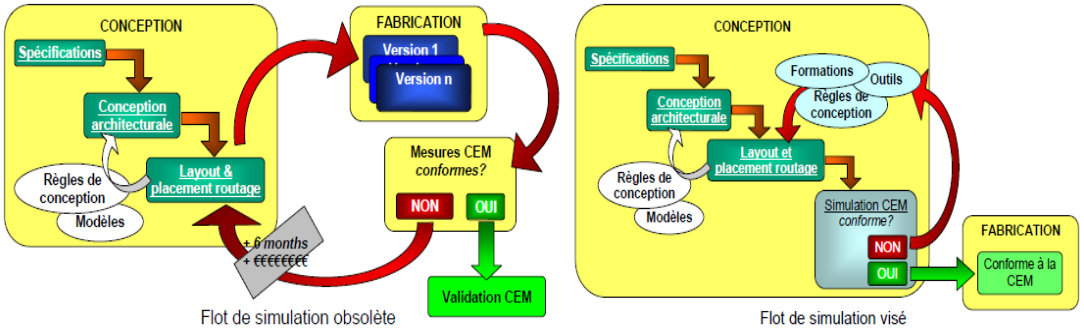

Figure I-24: IC design flow evolution

Additionally, for the system equipment manufacturers, they require the EMC characterization information of IC which will be integrated in their system. But normally, the architectures of the IC or IP (intellectual property) are confidential in the semiconductor industry. A simplified EMC model of the IC could be useful for system integration simulation.

Several standards and modeling techniques have been developed to study the emission and immunity simulation issues, such as ICEM model [IEC 62433], IBIS model [IEC 62014]…etc. All of these are addressed to industrial requirements.

2.3.1.1. *IBIS model*

IBIS (Input/output Buffer Information Specifications) model is originated from INTEL Corporation in 1990. It is based on the behavioral description of the digital I/O buffers, and includes RLC based package model. An IBIS model is formatted as human-readable ASCII text, mostly based on (black box) extracted tables versus connected structural elements as in SPICE models. The model file does not contain any proprietary information of the device, so neither process nor design information. And it enables reasonably accurate and fast signal integrity (SI) simulation. So it is supported by most semiconductor and EDA tool vendors. Figure I-25 shows the structure of the output block's IBIS model.

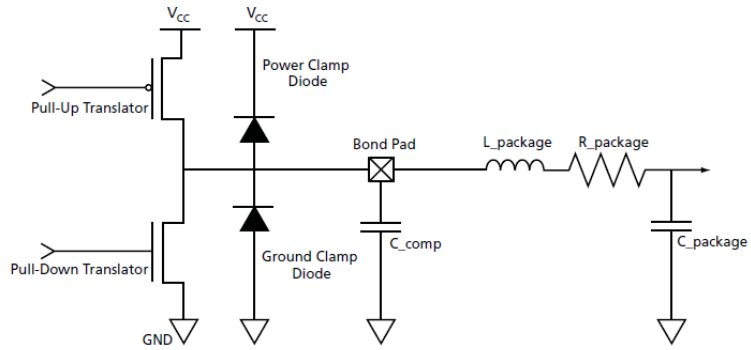

Figure I-25: IBIS models for output blocks with pin-specific package information.

It consists of three basic elements (see Figure I-25):

- Pull-down: keyword by [Pulldown], describes the current/voltage (I/V) characteristics of the buffer when the output drives low. The data is taken from $-V_{DD}$ to $2V_{DD}$ as that allows a behavioral model for signal reflections caused by improper termination, overshoot and undershoot situations when the protection diodes are forward biased.
- Pull-up: keyword by [Pullup], describes the pull-up state of the buffer when the output drives high. As pull-down, the voltage is tabulated on the table from $-V_{DD}$ to $2V_{DD}$.
- Ground and power clamps: keyword by [GND_clamp] and [POWER_clamp], describes the ground and power clamp diodes. The ground clamp curve is derived from the ground relative data gathered while the buffer is in the high-impedance state and illustrates the region where the ground clamp diode is active. The range is from $-V_{DD}$ to V_{DD}. The power clamp curve is derived from the V_{DD} relative data gathered while the buffer is in a high impedance state and shows the region where the power clamp diode is active. This measurement ranges from V_{DD} to 2 V_{DD}.
- Ramp: keyword by [ramp], describes the ramp time for the pull-up and pull-down devices to ensure proper AC operation of the model. The min and max columns represent the minimum and maximum slew rates for the buffers and the values represent the intrinsic values of the transistors with all package parasitic and external loads removed.

- Package: keyword by [Package], adds the component and package parasitic elements. C_comp is the capacitance of the die itself, excluding the package capacitance. Package characteristic resistance, inductance and capacitance are added by R_package, L_ package, and C_package, respectively.

The minimum and maximum values are determined by the minimum and maximum operating temperatures, supply voltages and process variations. Combining the highest current values with the fastest ramp time and minimum package characteristics, a fast model can be derived. A slow model can be derived by combining the lowest current with the slowest ramp time and maximum package characteristics.

However, IBIS model has some limitations:

- There is no information in IBIS file of the power and ground pins, while supply noise and ground bounce are in fact the major sources of EMI;
- The IC's internal activity has not been taken into account in IBIS. The switching noise from the cores coupled on power rails shared by I/O, which could generate additional noise.

2.3.1.2. ICEM model

The ICEM (Integrated Circuit Emission Model) was proposed by Union Technique de l'Electricité et de la communication (UTE) of the French section of the International Electro technical Commission (IEC) standardization group under the IEC 62014 -3 in 2005. And in 2006, ICEM and some competing models were included in a general standard called IEC 62433 [IEC 62433] dedicated to EMC of IC modeling. It could be used to predict conducted/radiated emissions at chip and printed circuit board level and also predict the auto-compatibility of the circuit (low level immunity analysis).

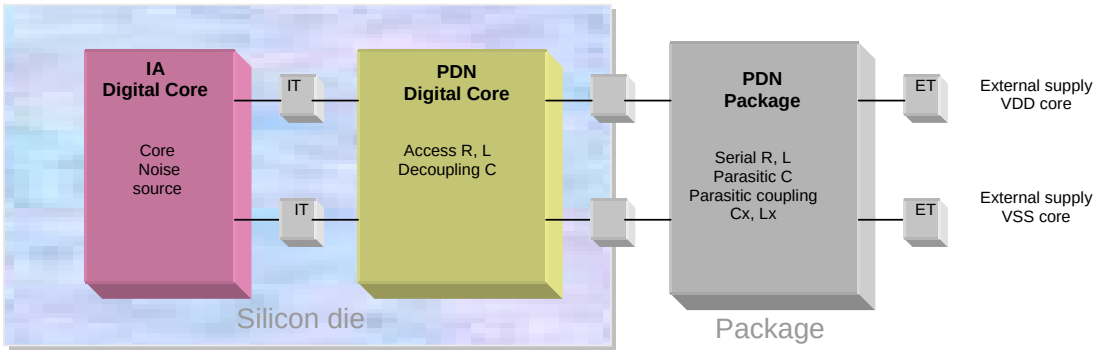

Figure I-26: The basic structure of the ICEM model of an IC [BOYE09]

There are five basic components in ICEM model (Figure I-26)

- The Internal Activity (IA) component describes the internal activity of IC by an independent current/voltage source.

- The Passive Decoupling Network (PDN), which describes the impedance network across one or several terminals, includes the package PDN, the on chip PDN.
- The Inter-Block Coupling (IBC) describes the coupling between 2 terminals (for example substrate coupling).
- The External Terminal (ET) connects with the external environment (I/O, equivalent dipole for radiated emissions).
- The Internal Terminal (IT) connects between other on-chip components.

The basic elements of an ICEM block are the PDN and IA. Different blocks are interconnected by IBC or transferred to the external of the circuit by ET. A generic and simple model is shown in Figure I-27.

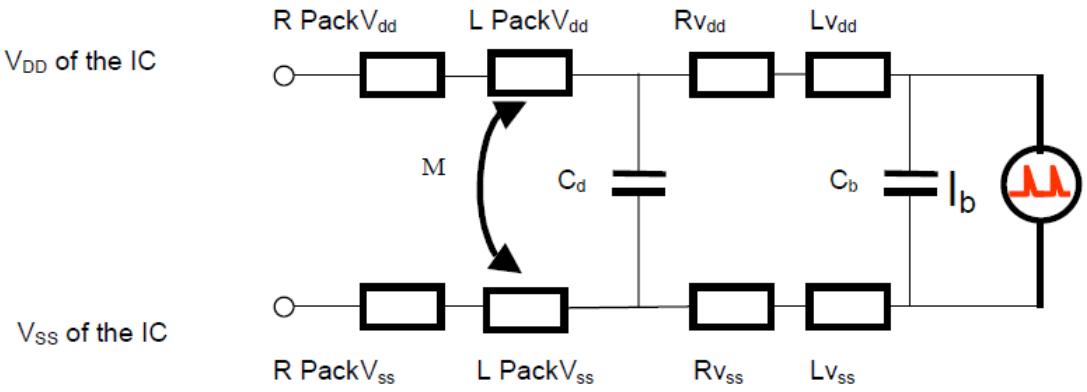

Figure I-27: The internal activity (IA) and Passive distribution Networks (PDN)

The sub-parameters of ICEM model is provided in Table I – 8

Symbol	function	Descriptions
IA	Current source, could be Pulse or Piece-wise-linear	Main source of parasitic emission considered in the model is the current source IA. The current shape may consist either of the time-domain description of the current versus time or as an equivalent triangular waveform. Typical values for IA current peak are [100 mA - 100 A] for the amplitude, 0.5 to 5 ns for duration, and 500 ps to 100 ns for the period.
Cd	Decoupling capacitance.	On-chip decoupling capacitance between VDD and VSS. Cd is a physical coupling between the internal supply rails VDD (positive supply) and the ground rail VSS (0V supply). The origin of the capacitance Cd is rail to rail or junction capacitance. Typical value ranges from 100pF (very small Ics) up to 100 nF (very large ICs).
LpackVdd, LpackVss	Equivalent supply inductance of the package.	The package inductance Lpack_vdd, Lpack_vss is the equivalent serial inductance of the supply path VDD and VSS. Typical value ranges from 0.1 nH (very short connection to supply, multiple supplies) up to 10 nH (long leads in DIL packages).
Lvdd_die,	Serial internal	The serial inductance Lvdd_die, Lvss_die, in serial with the local

Lvss_die	inductance.	block capacitance Cb creates a high frequency resonance effect. Typical value ranges from 0.1 nH (very short connection to supply) up to 10 nH (long connection).
Rvdd_die, Rvss_die	Serial internal resistance.	The serial resistance of the supply network models the path that connects the block supply to the main supply ring. Typical values for Rvdd, Rvss are 0.5 to 50 ohm.
Rpack_vdd, Rpack_vss	Equivalent supply resistance of the package.	The package resistance Rpack_vdd, Rpack_vss is the equivalent serial inductance of the supply path VDD and VSS.
Cb	Block decoupling capacitance.	The local block decoupling Cb is the local supply-to-ground capacitance placed in serial with the local current generator Id. It accounts for the equivalent decoupling capacitance of the block. Typical values range from 10 pF to 1 nF.
Lpack_M	Mutual inductance	Mutual inductance between the VDD and VSS wires, typical value range from 0 to 10nH

Table I-8: Description of IC immunity measurement standard IEC 62132

The IA block could be modeled by one or more current sources which represent the switching activity of the digital core. The internal current cannot be measured directly but could be extracted from the measurement of the external current. As Equation I-4, we assume that the PDN of IC is well known.

$$I_{int(f)} = I_{ext(f)} \cdot \frac{Z_c + Z_l}{Z_c} \qquad \text{Equation I-4}$$

The $I_{int(t)}$, $I_{ext(t)}$ are the internal and external current in time domain, respectively. After using FFT, $I_{ext(t)}$ is converted to $I_{ext(f)}$, and then $I_{int(f)}$ is computed. With the inverse FFT, we could obtain $I_{int(t)}$.

The PDN could be created by impedance measurement with Vector Network Analyzer (VNA) or extracted from the various measurements (VNA, TDR) or simulation (electromagnetic simulation, RC extraction).

2.3.1.3. ICIM model

As developing immunity models and simulation flows have become one of the major concerns of the EMC of ICs community. Based on the success of the integrated circuit emission model (ICEM) because of its simplicity and accuracy, an immunity model called Integrated Circuit Immunity Model for conducted immunity (ICIM-CI) has been proposed to International Electrotechnical Commission for standardization in the near future, as IEC62433-4 [IEC62433-4].

ICIM-CI aims at proposing a macro-model used to describe the behavior of an analog or digital circuit to conducted disturbances and thus simulating the immunity level. This macro-model uses general data about the circuit and can be implemented in various formats (SPICE, VHDL-AMS, IBIS,

mathematical description…). The philosophy of ICIM is to model each functional block of an IC by an ICIM macro model, composed of two main components (Figure I-28):

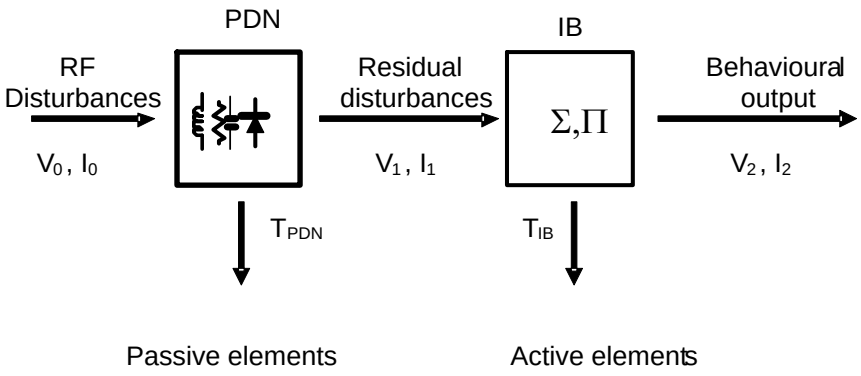

Figure I-28: ICIM model structure [IEC62433-4].

- The Passive Decoupling Network (PDN), the same as the one in ICEM model, includes all the passive devices of a circuit: package and on-chip interconnections, on-chip capacitances (gate oxide, junction, decoupling capacitances…) or substrate coupling. For small-signal disturbances, the PDN acts as a linear filtering function.
- The Immunity Behavioral (IB) block, as the IA block in ICEM, the IB in ICIM describes how the IC reacts to applied disturbances. IB covers both in band and out of band IC frequency response. The residual disturbances applied to the IB input are converted to a behavioral output, which can be either a waveform in time or frequency domain (voltage, jitter…) on which a failure criterion is applied, or directly a pass/fail result according to a failure criterion defined in the IB.

3. IC RELIABILITY ISSUES IN DEEP SUBMICRON TECHNOLOGY

3.1. IC reliability concerns

Reliability has been defined as:

The probability that an item perform a required function under stated conditions for a stated period of time;

For an IC, their period operation time (lifetime) always depends on the variety application. To avoid IC to be the bottleneck of the whole system reliability, the IC manufacturer should pay attention to address the IC reliability issues. Although in the electronics product customer point of view, the cost is the most important factor in IC design and manufactory, electronic product manufacturers should be only guaranteed several years' proper operation. Systems where reliability is a critical issue, as automotive, aeronautic systems, a nuclear plant…the reliability of ICs is always the critical problem which had to be dealt with.

3.2. Reliability: a statistic approach

From reliability' definition, the IC reliability is a statistical process and it is described as the probability *R (t)* for a number of N components to survive at a time *t*. (see Equation I-5)

$$R(t) = \frac{Number\ surviving\ at\ instant\ t}{Number\ at\ time\ t = 0} \qquad \text{Equation I-5}$$

$$R(0) = 1, \qquad R(\infty) = 0$$

All devices are assumed to be working properly at the beginning and will be broken at infinite time.

There are two important types of failure for semiconductor device:

- Degradation failures (soft failure): when an important parameter (as the saturation current or threshold voltage) of the component drift so far from its original value that exceed some specific limit.
- Catastrophic failures (hard failure): the sudden and complete failure of the device, recovery not possible, the end of the device.

The failure rate λ is defined as the number of appearing failed devices per unit time. It is always quantified by the number of devices failing in 10^9 hours. The unit of the failure rate is FIT (Failure in time) which is 1 failure per 10^9 hours.

There is another commonly used indicator to quantify component reliability: the MTBF (Mean time between failures), and sometimes described as Mean times before failure while usually in some semiconductor standards and which concern the irreversible failure. This is defined as the mean time to failures and assuming the failures occur randomly, at a constant rate λ, the MTBF is given by Equation I-6

$$MTBF = \frac{1}{\lambda} \qquad \text{Equation I-6}$$

The survival probability *R (t)* is related to MTBF by Equation I-7

$$R(t) = e^{\left(\frac{-t}{MTBF}\right)} = e^{(-\lambda t)} \qquad \text{Equation I-7}$$

R (t) is therefore an exponentially varying function of time (t) as shown in Figure I-29. We assume that the failure probability has a normal distribution. From the Figure I-29 we can see that after ½ MTBF, the probability *R (t)* that there will be no failures is 60% and after 1 MTBF this probability falls to 37%.

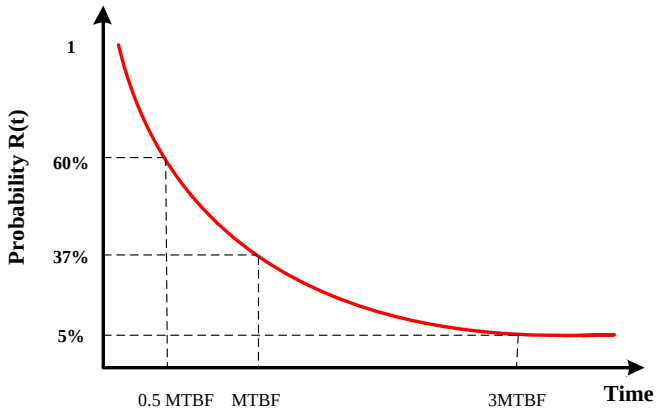

Figure I-29: The probability of component surviving vs. time

The more tested sample, the higher confidence that we have. In the normal distribution of the failure probability, if we have a large number of samples (usually recommended > 10^5 devices) that resulting in 10^3 failures in 10^{12} hours would indicate a λ of 1 FIT. This value of λ would have a much higher confidence limit than the situation that only one device operated continuously for 10^9 hours and had only 1 failure.

3.2.1. Bathtub curve

A common graphical interpretation of the failure rate is shown in Figure I-30. This model is known as the "Bathtub" curve and was initially developed to model the failure rate of mechanical equipment. However, it has been adapted by the semiconductor industry to model IC failure [AMER97].

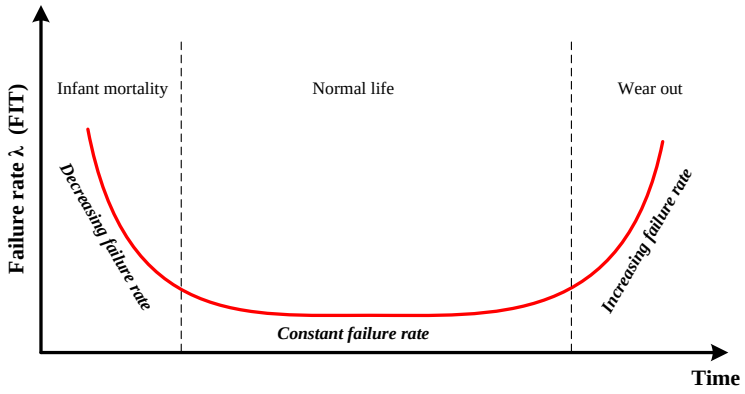

Figure I-30: The bathtub curve with three regions

The bathtub curve, displayed in Figure I-30 above, does not depict the failure rate of a single item, but describes the relative failure rate of an entire population of device over time. It consists of three regions:

- Infant mortality: in this region, the failure rate decreases rapidly, usually less than 1 year for ICs. Caused by the extrinsic mechanism, as the defects during the fabrication.
- Normal life: in this region, the failure rate is constant, during a period dependent on the technology of the integrated circuit.
- Wear out: after the normal life period, the device begins to fatigue and some wear-out failure mechanisms become obviously and with an increasing failure rate. The duration could last for years.

The device failures mainly occur at the first and third region.

The infant mortality can be eliminated by preliminary burn-in once the device is complete. Burn-in for semiconductors is almost always done with a short temperature and voltage stress. Sometimes both a wafer and module burn-in are performed. The wafer burn-in is done typically under elevated temperatures and very high voltages compared to the use conditions, and would last only a few seconds. The module burn-in conditions includes an elevated temperature and a voltage that is higher than nominal conditions, but lower than the wafer burn-in voltage, and will be applied for several hours.

After a long operation period, the devices begin to wear out because of intrinsic mechanisms, such as Electro Migration (EM), Hot Carrier Injection (HCI), Negative Bias Temperature Instability (NBTI), Time Dependent Dielectric Breakdown (TDDB), which are illustrated in Figure I-31

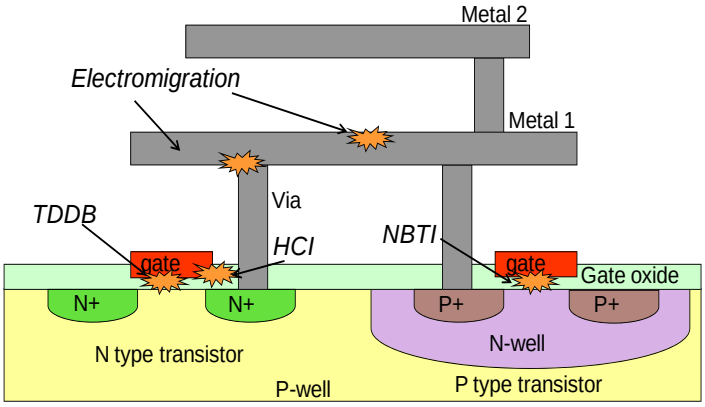

Figure I-31: CMOS intrinsic wear out failure mechanisms

The time to wear out or the lifetime of the device depends not only on the IC technology, but also on environment, as temperature, supply voltage, the operating frequency or clock duty cycle. All of them could accelerate the failure mechanism and reduce the device lifetime.

The traditional statistical reliability analysis approach consist of determine the MTBF or FIT which is a simple statistic model based on measurement and without the relation with failure mechanism. There are several limitations of this approach. First, in the real condition, the wear out step consists of different degradation mechanisms instead of single failure. Additional, with the technology evolution, the lifetime (the normal life) of the device would be much lower, as this statistical model is accurate of the device operate over decades, however for the device lifetime less than several year, the model could be not accurate enough. Furthermore, enter the submicron technology, the soft failure (degradation failure) are the main failures instead of catastrophic failures which the devices are totally destroyed. How to predict the system performance degradation due to the device parameter variation?

3.3. The physics of failure approach

To overcome the limitation of traditional approach, recently reliability researches proposed Physics of failure (PoF) approach [WHIT08] which identify the failure during design level as opposed to a traditional which analysis after failure are observed during qualification tests. It is based on separate study of the dominant failure mechanisms: their root causes, the failure modes and failures causing stresses. The procedure of physic of failure approach consists by firstly identifying the dominant failure mechanisms, then, creating the PoF models by combination the data gathered from acceleration test and statistical distributions. And in the end develop an equation for the failure mechanism for simulation and prognostics [MARI11].

3.3.1. Activation energy and Arrhenius equation

Activation energy comes from chemistry and is used to define the minimum amount of energy required to initiate chemical reactions. It is usually denoted by symbol ***Ea***. In context of semiconductor

device reliability, this concept has been reused and refers to the minimum amount of energy required to trigger a failure mechanism. In IC reliability, different failure mechanisms have different Ea.

The Bathtub curve shows that at the end of the device life, the device wear out caused by various failure mechanisms. Different failure mechanisms coexist, but they have different failure rates and different sensitivity to operation conditions. Their failure rates are related to the activation energy, the type of failure mechanism and the temperature. This relationship is characterized by Arrhenius equation (Equation I-8)

$$r = Ae^{(\frac{-E_a}{KT})} \qquad \text{Equation I-8}$$

Where r is the rate at which the failure mechanism occurs, A is the constant, Ea is the activation energy of the failure mechanism, k is the Boltzmann's constant ($1.38e^{-23}$J/K = $8.6e^{-5}$eV/K), and T is the absolute temperature in Kelvin (K) at which the device operate.

The activation energy Ea could be extract by experimentally. The failure evolution of a set of samples with the same and specific failure mechanism at different temperatures is analyzed. The measurement of the MTTF (Median time to failure), is the time that 50% of device failed and is plotted in a logarithms graph versus to 1/T (Temperature in Kelvin). If the curve is a straight line, the slope of the curve is equal to Ea/k.

There are four main basic degradation mechanisms for semiconductor devices, Electromigration, Hot carrier injection, Time dependent dielectric breakdown and the Negative bias temperature instability. In the following sections will bring out in brief, the root cause of each failure and the degradation model for the variation parameters.

3.4. Electromigration (EM)

3.4.1. Electromigration overview

In home circuitry, the bulk wires can support maximum 10^4 A/cm^2 due to the Joule heating limit, which is insufficient to driving an EM phenomenon. In IC domain, the interconnections, usually made by thin film Aluminum (Al) or copper metallization wires, the heat generated by electricity conduction is dissipated by the chip which works as the heat sink. But there could be sufficiently high current density (nearly 10^6 A/cm^2) available in the metallization tracks on the in interconnects, the continuous impact of electrons on the Al atoms causes the atoms to move in the direction of electron flow. A void is therefore created at one end of the track while metal is piled up at the other end. The depletion of metal causes circuit damage due to decrease electrical conductance as the cross sectional area is reduced. Increased resistance alone may result in device failure, yet, the resulting increase in local current density and temperature may lead to thermal runaway and catastrophic failure as opened circuit formation. In the other hand, the extrusion of material leads to form the Hillocks which

could break the oxide layer, allowing short circuit formation. Figure I-32 presents an example IC interconnect defects due to electromigration [CARC99].

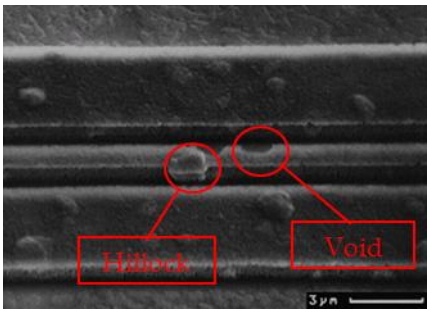

Figure I-32: IC interconnection defects due to electromigration [CARC99].

3.4.2. Failure physical analysis

With high current densities, the electron can transfer sufficient momentum to thermally activate metal atoms, forcing them break the electrostatic force and escape out of their lattice sites, then extracted atoms move under diffusion in the same direction as electron. This leads to interconnection electromigration.

In an ideal conductor, where atoms are arranged in a perfect lattice structure, electrical resistance is Zero, i.e. electrons moving through the conductor would experience no collisions. In a real conductor, defects in the lattice structure, as missing atoms (vacancies), impurities...and the random thermal vibrations of the metal atoms out of their positions cause electrons to collide with the atoms and scatter. The scattering event makes the electron change direction and also acceleration. In the other side, the electrostatic force in symmetric and uniform lattice has a resistance to collisions. But the metal atoms in an imperfect lattice with vacancies, grain boundaries and material interface, have weak bonds and could be easier pushed away from their position, and transported in the current direction. The direction is also influenced by grain boundaries itself, as atoms are transported along the direction of the boundaries.

The EM occurs not only in the metal interconnection, but also happens in some semiconductor materials if they are heavily doped, i.e. polycrystalline silicon.

The flux of metal atoms due to EM is expressed by Equation I-9, a flux *Jem* is the number of the moving metal atoms crossing a unit area per unit time [COEL89].

$$J_{em} = \frac{D}{KT}(Z^* q)\rho J_e N \qquad \text{Equation I-9}$$

Where the J_{em} unit is atoms/ ($cm^2 s$)

And Table I-9 lists the sub-equations for Equation I-9 and description of the variables used in the equations.

Magnitude	Sub-equations	Variables
Atomic flux	$J_{em} = \nu N$	ν: mean velocity of metal atoms

Atom mean velocity	$\nu = \mu E$	N: concentration of moving metal atoms Z^*: effective charge factor q: electron charge D_0: constant depends on diffusion mechanism KT: Boltzmann's thermal energy μ: atom mobility E: electric field ρ: metal resistivity J_e: electron current density
Atom mobility	$\mu = {QD}/{KT}$	
Diffusivity	$D = D_0 e^{(\frac{-E_a}{KT})}$	
Effective charge	$Q = Z^* q$	
Electric filed	$E = \rho J_e$	

Table I-9: Electromigration flux J_{em} Derivation

With this equation, we could identify variables that influence EM. The flux consists in concentration gradient diffusion and electrical bias diffusion. The EM induced flux is directly proportional to the current density, to the diffusion coefficient and to the concentration of diffusing atoms. Even low concentration doping may have great impact on EM features. As example, the EM activation energy of bulk AL is 1.4eV, while adding small amounts (0.3% to 5%) of Cu reduces this Ea by about 0.5-0.8eV [OHRI98]. EM is very sensitive to temperature. It is exponentially related to temperature in equation of the diffusion coefficient.

The atoms flux flows inside the interconnection. In the region where the mass loss is larger than the mass incoming, voids and open circuits can be formed. Conversely, where the region has more mass entering than leaving, extrusions will form short circuit or breaks in the passivation and provide an opportunity for corrosion. These regions are called flux divergences. Unfortunately, many opportunities exist for flux divergences in the IC process.

One example is the terminal of the Al interconnection: Si/Al interface, the diffusion of Al from Silicon (Si) is zero, and, the diffusion of Si into Al is the same. Therefore, since EM will be driving the Al away from the Si contact and stuff it into another terminal [CADENCE]. Another example is the end of the line connected to via, which usually made of Tungsten or there is a diffusion barrier between the Al interconnection and via [PARK01].

As device features continue to shrink, the thinner film brings fine grain size whose Ea become lower. The interconnect current densities growing, joule heating causes temperature increasing. The increased performance require that interconnects have to be more and more reliable under conditions where metallization is inherently less reliable [CADENCE]. Thus the EM will remain a critical wear out mechanism in future semiconductor design.

3.5. Hot carrier injection (HCI)

3.5.1. Hot carrier injection overview

Hot carrier injection is one of the primary wear out failure mechanism affecting the long term reliability of ICs. It has been aggravated due to continuous scaling of MOS transistor dimensions without proportional scaling of the operation voltage, which causes a significant increase of the gate electric field in both horizontal and vertical direction, as explained in the 1.1 paragraph and Figure I-33.

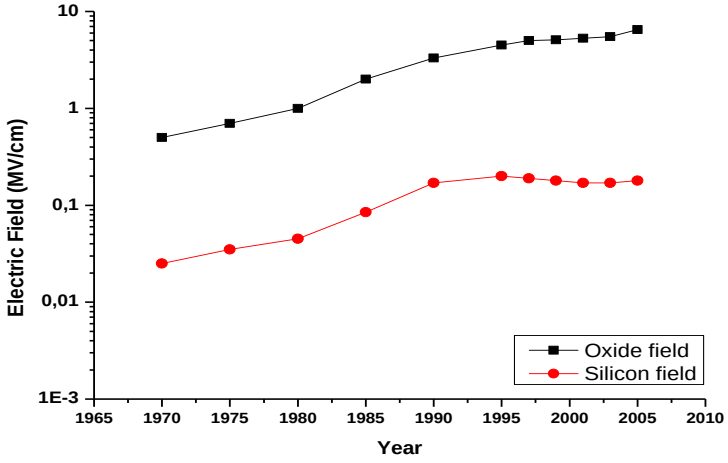

Figure I-33: Evolution of electrical fields in oxide and silicon [GROE01]

The carriers (electrons or holes) under these high electric fields gain enough kinetic energy which exceeds the average energy lost by the carrier through the scattering effects. The effective carrier temperature will be larger than the lattice temperature. Such a carrier is termed as "hot carrier" [JIAN98]. These hot carriers could be injected into the gate oxide, causing permanent changes to the charge distribution at the oxide-interface. It would induce device degradation as threshold voltage (Vt) shift and reduction of drain current.

Under the same electric field, holes require much higher drain voltage to activate the hot carrier effect due to the lower charge mobility (μ). Compared to electrons, holes need more energy(approximately 3.2eV for electrons and 4.7eV for holes) to surmount the energy barrier at the Si/SiO_2 interface and be injected into the gate oxide [WHIT08]. Traditionally, the hot electrons mechanism in N-type MOS transistor is considered as the major concern in HCI issues [HU85] [SIM0585], while hot holes mechanism in P-type MOS transistor is considered to be less severe than in N-type MOS transistor. However, with technology scaling down to submicron, HCI in PMOS is getting more significant [ROSA97] [MATS90]. Since they are similar mechanisms, the completion and model based on NMOS type HCI could be applied to PMOS transistor with minor modifications. We use hot electron in NMOS as the example to explain the principle of the hot carrier injection failure mechanism.

3.5.2. Failure physical analysis

3.5.2.1. Defects in Si/SiO2 interface

Most of the wear-out failure mechanisms relate to the Si/SiO_2 interface and gate oxide layer defects. Figure I-34 shows the typical charge distribution at the MOS transistor gate oxide-silicon interface.

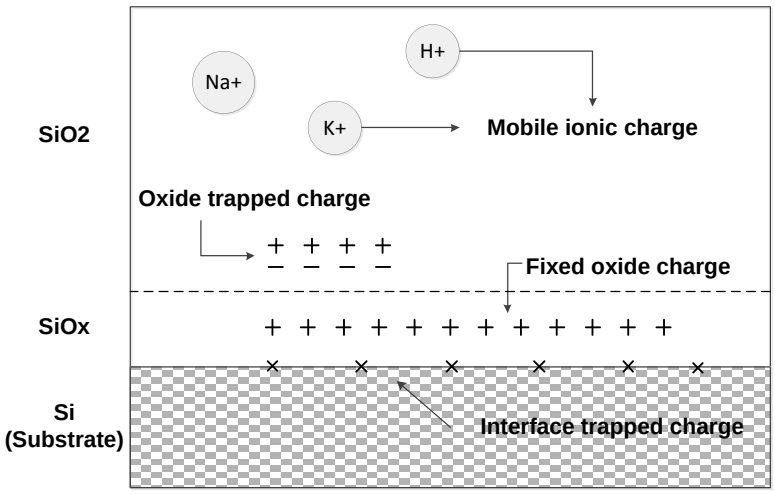

Figure I-34: Si/SiO_2 interface charge distribution [LEBL93].

There are four types of charges existing at the Si/SiO_2 interface.

- Mobile ionic charge: mainly caused by ionic impurities such as Na+, Li+, K^+, H+…, the mobile charges are usually mobile within the oxide. Some negative ions are also included but do not believe to be mobile at temperature below 500°C [SRIV09].
- Oxide trapped charge: could be positive and negative charges that are distributed within the oxide, resulted from ionizing radiation exposure or other mechanisms as avalanche injection.
- Fixed oxide charge: During the thermal oxidation, a thin SiOx layer near to the interface is sandwiched between SiO_2 and single silicon Si crystal. This layer is incompletely oxidized silicon in which positive fixed oxide charge (immobile to any applied electric field) may appear [PROD09].
- Interface trapped charge: nominally locate at the SiO_2/Si interface. Originate in structure defects, oxidation-induced defects, metal impurities or other defects caused by radiation or similar bond breaking processes, as hot carrier degradation [PROD09]. It could exchange charge with underlying silicon depending on the surface potential.

These charges are the main cause of the oxide based reliability issues. The Si/SiO2 interface is prone to dangling bonds and vacancies which could be carrier traps. It leads to mobility (μ) or transconductance (Gm) degradation by scattering interaction with channel carrier. The mobility degradation leads to the drain current degradation. The distribution of trapped charge and interface charges has an influence on threshold voltage [TAKE95].

3.5.2.2. *Hot carrier injection mechanism*

As we explained in the previous paragraph (Figure I-34), there are four types of charges inside the oxide and Si/SiO2 interface, among these charges, the fixed oxide charges and the interface trapped charges play an important role in the hot carrier issues. The interface trapped generation caused by HCI in 2 ways: one is due to recombination with already existing trapped charges, and the other is due to the break of Si-H bonds by energetic carriers.

There are four distinguished injection mechanisms [TAKE83a]:

- Channel hot electron injection (CHE)[ENTN07]

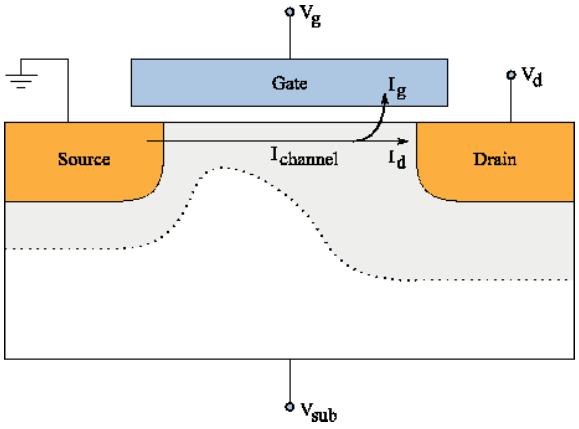

Figure I-35: Under CHE injection, gate voltage is approximately equal to the drain voltage, the "lucky electrons" gain enough energy and injected into the dielectric causing a gate current [ENTN07].

The CHE injection mechanism is illustrated in Figure I-35, it occurs when the gate voltage (Vg) is nearly equal to the drain voltage (Vd). The bias could be optimum for CHE injection of "lucky electrons" which gain sufficient energy to surmount the Si/SiO2 barrier without suffering energy lose due to collision in the channel. The induced gate current is responsible for device degradation as a result of carrier trapping. When Vg < Vd, the vertical electric field could not attract electrons. But for high drain voltage (Vd), the lateral electric field at the drain leads to avalanche multiplication due to impact ionization. Hot electrons and hot holes are injected. The replaced "lucky electrons" formed gate current.

- Drain avalanche hot carrier injection (DAHC)

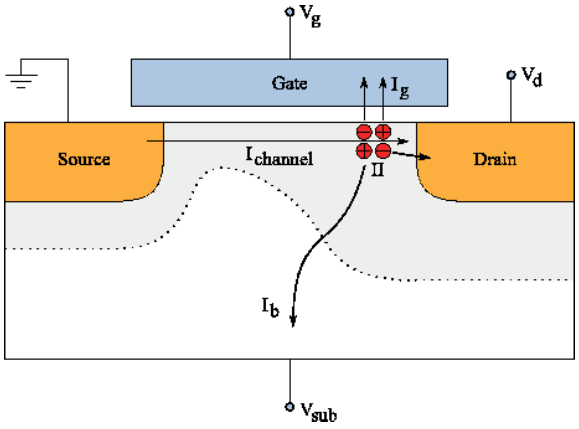

Figure I-36: Drain avalanche hot carrier injection, drain voltage are much bigger than gate voltage, the hot electrons and hot holes are injected into dielectric, additionally some of the carrier form a bulk current [ENTN07].

The DAHC injection (illustrated in Figure I-36) occurs when there is a high drain voltage and a small gate voltage. The bias condition results in very high lateral electric field near the drain which accelerate channel carrier travel to the drain. The accelerated carriers collide with Si lattice atoms and create electron-hole pairs, known as impact ionization. The electron-hole pairs could gain enough energy to surmount the Si/SiO2 barrier and inject electrons into the oxide while some holes flow back to the bulk, forming the substrate current. Thus the substrate current is an effective indicator of DAHC mechanism.

- Secondarily generated hot electron injection (SGHE)

  SGHE injection is caused by secondary minority carriers originating from the secondary impact ionization caused by the substrate current. The substrate hole current generated by DAHC injection creates further electron-hole pairs by the avalanche effect near the drain [KIM04].

- Substrate hot electron/hole injection (SHE/SHH)

  SHE/SHH are due to high positive or negative bias at the substrate (V_{sub}). This leads to the carriers in the substrate being driven to the Si/SiO_2 interface which gain further kinetic energy in the surface depletion region. The substrate carriers are either generated by optical generation or by electrical injection from a buried p-n junction. These carriers are eventually overcome the energy barrier at the inter face and are injected into oxide.

Among these injection mechanisms, DAHC injection causes the most stringent device degradation because both hot electron and hot holes are injected into the gate oxide in the same time. Under the normal operating temperature range, DAHC produce the worst device degradation [TAKE83a].

3.5.2.3. Device degradation induced by HCI

As mentioned above, the defects in oxide and Si/SiO2 interface induced by hot carrier injection are the main cause of the MOS degradation. For NMOS, threshold voltage increases and transconductance decreases (due to mobility decrease). No unanimous agreement about the origins of the transistor degradation exists and, various methods have been proposed. Among them, TAKEDA gave an empirical model of the parameter degradation with stress time and other stress condition relationship from the experimental results [TAKE83b].

The TAKEDA model is based on the two following assumptions:

- Avalanche hot carrier injection due to impact ionization at the drain, rather than channel hot electron injection composed of “lucky electrons “impose the severest constraints on device design.
- Device degradation (V_{th} shift and transconductance degradation) resulting from avalanche hot carrier injection has a strong correlation with impact ionization induced substrate current I_{BB}.

The V_{th} shift, ΔV_{th} or G_m degradation, $\Delta G_m / G_{m0}$, can be empirically expressed as a power law expression (Equation I-10)

$$\Delta V_{th}(\text{or } \Delta G_m/G_{m0}) = At^n \qquad \text{Equation I-10}$$

This expression is particularly valid for short stress times, while for long stress times, ΔV_{th} or $\Delta G_m / G_{m0}$, begins to saturate. The slope n or ΔV_{th}, in log – log plot is strongly dependent on V_G and little dependence on V_D. It suggests that n changes according to the hot carrier injection mechanism. The magnitude of degradation, A, is strongly dependent on V_D and a little dependence on V_G, as show in Figure I-37 [TAKE83b]:

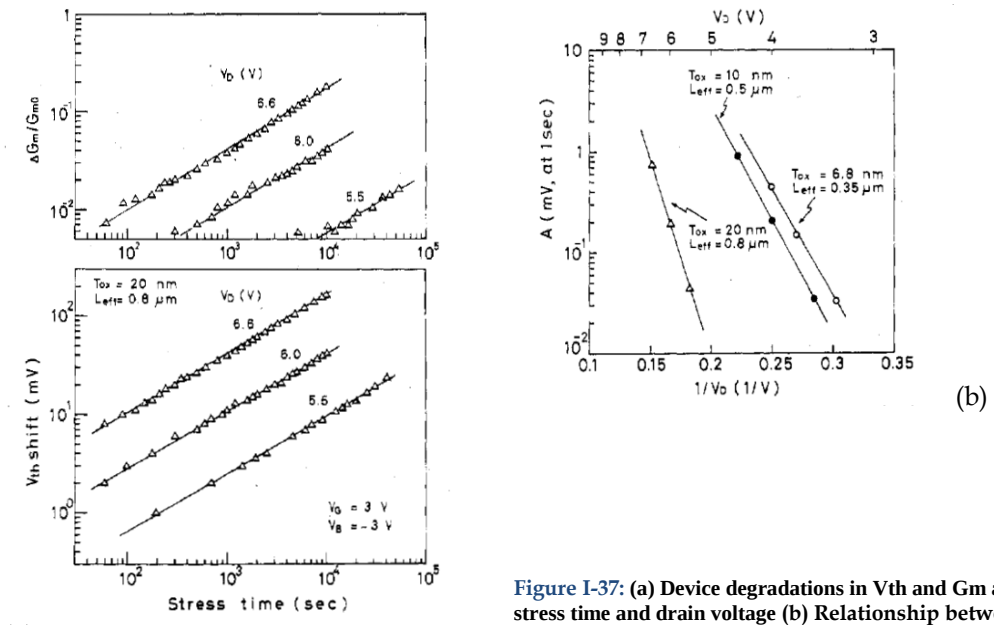

Figure I-37: (a) Device degradations in Vth and Gm are a function of stress time and drain voltage (b) Relationship between the magnitude of device degradation A and drain voltage V_D [TAKE83b]

The worst bias condition, which causes the most severe device degradation, corresponds to that which gives the peak to bell shaped substrate current I_{BB}, as shown in Figure I-38. The peak of substrate current I_{BB}^m, which indicates the number of electron-hole pairs generated by impact ionization at the drain, also is dependent on V_D.

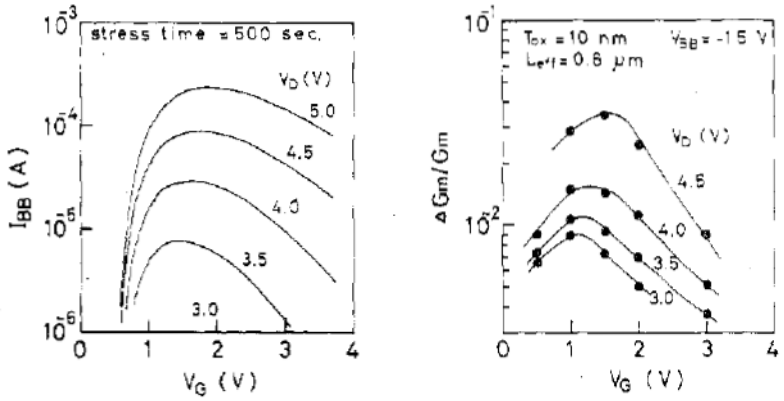

Figure I-38: Relationship between Gm degradation and substrate currents as a function of VG for long channel device. [TAKE83b]

The gate capacitance could also be affected by HCI. The trapped electrons from pre-existing defect in oxide layer and HCI effects could reduce the gate to drain (Cgs) and gate to source (Cgd) capacitances [SAGO09].

3.5.2.4. Environment and operation condition influence on HCI

HCI effects are enhanced at low temperature as its activation energy is negative (around -1eV), mainly explained by the increase of electron mean free path and impact ionization rate rising at low temperature. The research results show that substrate current at 77K is five times greater than that at room temperature (RT), and CHE gate current is approximately 1.5 orders of magnitude greater that that at RT[TAKE95]. At low temperature, the electron trapping efficiency increases and the effect of fixed charges becomes large. This accelerates the degradation of transconductance (Gm) at low temperature. [ACOV96].

As explained in previous paragraph, the operation voltage has great impact to hot carrier effect. The degradation is strongly depends on the electric field in the MOS transistor which directly relates to the operation voltage (Figure I-38). TAKEDA [TAKE83b] states, the worst bias case is under the relation of $V_G \approx 0.5V_D$ to obtain the maximum substrate current, while recent researches report that in short channel device ($L < 0.1\mu m$), the worst bias condition towards to the relation $V_G \approx V_D$[AMAT09] [LI99].

Other environmental condition like the radiation exposure (X- ray, gamma ray, solar proton…) can increase HCI degradation rate, as total dose damage, the produced damages have almost the same mechanism as the hot carrier injection [WOOD87].

3.5.2.5. HCI model overview

In order to evaluate circuit performance and reliability under hot carrier injection mechanism, the circuit models are used as the bridge connecting the gap between transistor level degradation and circuit level performance simulation. The underlying concept of the circuit models firstly proposes the lifetime model of device parameters variation and represents them by lumped circuit elements (resistors, transistors or dependent current sources, etc.). Therefor with this equivalent transistor model, we can compute the degradation magnitude at any time under different operation conditions. Then these transistor equivalent models can be incorporated into the circuit model and finally, electrical simulations such as SPICE can be performed to check the circuit functionality and analyze the impact of device degradation on circuit reliability.

There are several existing HCI circuit models in the past researches [BERN06]:

- BERT (Berkeley Reliability Tools) model: the MOSFET hot carrier damage effect on drain current reduction is directly modeled by a adding a bidirectional current source in parallel with the original MOSFET (Figure I-39) to simulate the forward and reverse mode (switching

the Drain and Source). The current source ΔI_d results from the channel mobility degradation caused by the HCI induced interface traps ΔN_{it}. The detailed ΔI_d model equations and parameters are defined in [QUAD91].

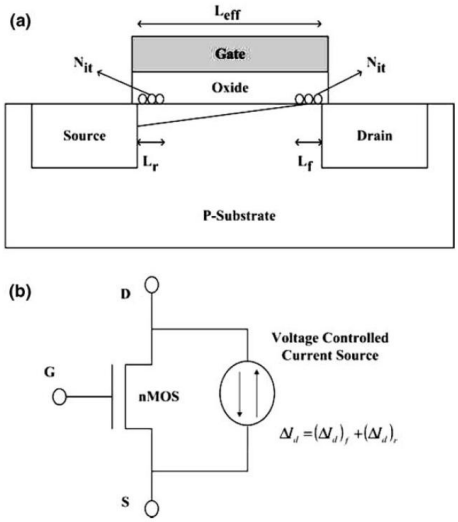

Figure I-39: BERT n-MOSFET HCI circuit model. (a) Bidirectional interface trap generation near both drain and source dependent on the bias configuration, Lf and Lr represent forward and reverse hot carrier damage regions (b) HCI drain current ΔId circuit model [LEBL92] [QUAD91].

- UIUC (University of Illinois at Urbana-Champaign) model: the model makes the assumption that interface traps are occupied only with electrons, i.e. only negative fixed charge localized only a section of the oxide near the drain junction above the channel are considered. The model uses two transistor HCI circuit model (Figure I-40)

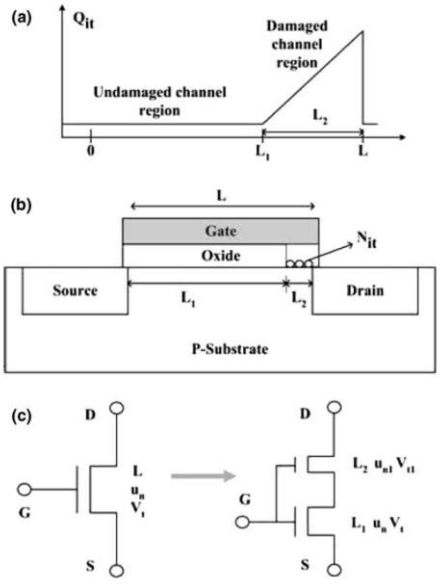

Figure I-40: UIUC HCI circuit model. (a)Triangular charge distribution with a sharp peak close to drain, the other part assume to be undamaged (b) Cross section of a nMOSFET with hot carrier damage in L2 section while the L1 is undamaged.(c) Two transistor series circuit model. The parasitic transistor reproduces degradation in section L2, while the origin transistor only decreases the channel length to L1 [LI94] [LEBL92] [BERN06].

It consists of an HCI damaged parasitic transistor with fixed channel length ($L_2 \approx 0.1\mu m$) which assume to be damaged region, and in series connection with the original transistor whose channel length was became to $L_1 = L - L_2$ with zero damage. The negative charges trapped in both equivalent transistors are given by Equation I-11.

$$Q_{it}(x) = 0 \qquad when \;\; 0 \leq x \leq L_1$$
$$Q_{it}(x) = \frac{Q_M}{L_2}(x - L_1) \qquad when \; L_1 \leq x \leq L_2 \qquad \text{Equation I-11}$$

Where Q_{it} is the interface trapped charge and Q_M is the maximum interface charge in L_2 section. The quantities can be measured by charge pumping measurement [ANCO88]. All the other device parameter could be derived from Q_M and L_2. The derivation of the parameter can be found in [LEBL92]

- HISREM (Hot Carrier Induced Series Resistance Enhancement Model): this simple HCI failure equivalent circuit model, also named ΔR_d model, is based on the fact that the drain current decrease caused by interface trap generation near the drain end and can be modeled by the increase of HCI induced series drain resistance. ΔR_d is a voltage dependent resistor in series with the original n-MOSFET (Figure I-41).

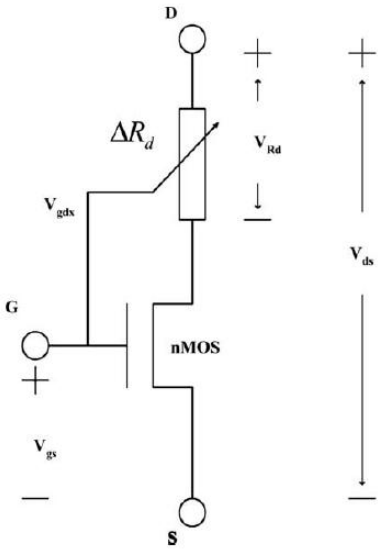

Figure I-41: HISREM HCI circuit model. A parasitic resistance ΔR_d in series with original NMOS, ΔR_d depends on Vgdx = Vgs – Vt – Vds, and V_{Rd} = Ids*ΔR_d, Vt is the transistor threshold voltage and Ids is the current flow through inside NMOS [BERN06].

The ΔR_d is also a function of the hot carrier induced interface trapped charge $\Delta N_{it.}$ and oxide trapped charge ΔN_{ox} which are time dependent. The derivation of parameters (μ, Ids, ΔN_{it}, ΔN_{ox}, etc.) can be found in [HWAN95].

3.6. Time dependent dielectric breakdown (TDDB)

3.6.1. Time dependent dielectric breakdown overview

TDDB is a significant gate oxide wear out phenomenon. It is caused by the formation of a conducting path through the gate oxide between the channel and the substrate due to electron tunneling current. The dielectric material of gate oxide has a maximum electric field strength that it can withstand intrinsically without break down (known as *dielectric strength*). It is directly

proportional to the thickness of the layer and inversely proportional to the operation temperature, switching frequency and humidity. A strong electric field (10MV/cm or above) could induce dielectric breakdown when it is applied on the gate oxide, as immediate break down caused by EOS and ESD; However, at lower electric field (3MV/cm) [SANYO], the dielectric layer can wear out after long term application and finally break down completely. This is the Time Dependent Dielectric Breakdown TDDB.

3.6.2. Failure physical analysis

3.6.2.1. TDDB failure mechanism

The TDDB failure mechanism takes place in two stages [CHEN85] [WANG07]: the first stage is built up stage which last over a long period of time. The gate oxide is slowly damaged and degraded due to the localized hole and bulk electron trapping inside the oxide and in the Si/SiO2 interface. The second stage begins when the increasing density of traps form a resistive conduction path (called percolation path) through the oxide and the localized high field/current density inside oxide reach a critical value. The formation of this conduction path may result in one of two types of failure [BERN06]. Once a conduction path forms, current flows through the path causing a sudden energy burst, which may cause runway thermal heating. At the beginning these conductive paths might disappear after an initial injection high current density which generates high temperature that could relocate some of the oxide traps and, break the conduction path and create other conductive path. The result may be a *soft breakdown* (SBD) i.e. the device continues to function with a small change of voltage or current after breakdown. The gate leakage current follows a power law with gate voltage [JONA05]. Local melting of the oxide can destroy the gate and cause an ohmic short circuit current across the gate (leakage gate current vs. gate voltage), which is denoted as *hard breakdown* (HBD) [ALAM02a]. The soft breakdown usually happens on thinner oxides under lower voltage, while the hard breakdown often happens on thicker oxides, the gate leakage flows current through the percolation path and created power dissipation that could heat up the oxide and leads to the abrupt voltage drop and gate current increasing exponentially and limited by series resistance [KACZ04]. With thin oxide and low operation voltage, sometimes, it could not store enough energy to trigger the hard breakdown. The earlier work showed that if the operation voltage decreased under 1V, the probability for hard breakdown was negligible [ALAM00].

The leakage current through the oxide could be characterized as:

- Direct tunneling current: if the gate voltage drop in the oxide layer (Vox) is small (less than barrier height), the electrons can move from inverted silicon surface to the gate (for NMOS) only by direct tunneling through the entire oxide thickness, as shown in Figure I-42(a). It happens only for thin oxide thickness (tox < 4nm).

- Fowler-Nordheim (FN) tunneling current: with high gate voltage, the band bending causes the potential barrier shape to become triangular, as in Figure I-42(b), electrons tunnel from the silicon inversion layer to SiO2 conduction band from where it travels to the gate contact. The FN tunneling is significant for thicker oxide and sufficiently high electric field.
- Stress induced leakage current (SILC): based on trap assisted tunneling mechanism at low gate voltage. The traps located inside oxide split the oxide in several parts which are easy to tunnel. They act just like the stones in the river to help carrier to cross over the barrier. SILC depends on the trap density and the electric field.

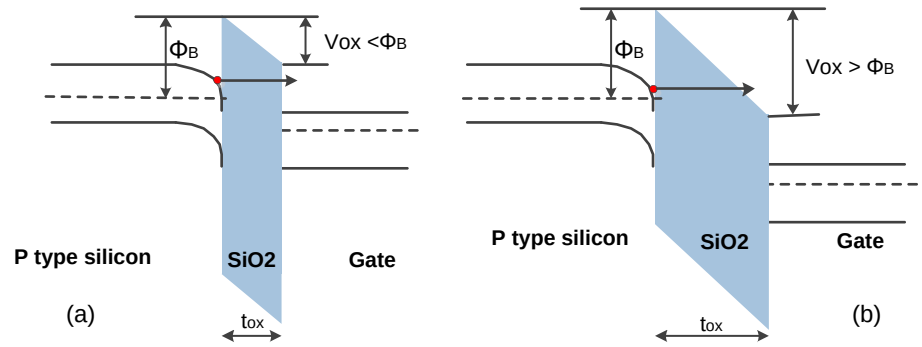

Figure I-42: Tunneling mechanism (a) direct tunneling; (b) Fowler-Nordheim tunneling.

Trap generation is the key factor to characterize the dielectric wear out and breakdown. Many models have been proposed and discussed in order to explain the TDDB physical mechanism under electrical stress condition [BERN06]:

- Anode hole injection (AHI or 1/Eox model): was proposed by Schuegraf and Hu [SCHU94]. This model suggests that breakdown is caused by holes that are injected from the anode. The injected electron gain high kinetic energy as they travel through the conduction band of the SiO2 layer. Upon reaching the anode (Drain for NMOS) these high energetic electrons release part of their energy as they fall back to the conduction band in the anode. Thus, it has a probability of creating a hot hole which can tunnel back into the oxide. These holes are suspected to create electron traps and will trigger the breakdown process [MOON07]. This model is commonly referred to as the 1/Eox model, since the logarithm of the mean intrinsic breakdown time (t_{BD}) is proportional to 1/E due to FN current conduction. (Equation I-12)

$$t_{BD} = t_0 \, exp\left(\frac{G}{E_{ox}}\right) \qquad \text{Equation I-12}$$

Where the Eox is the electric field across the oxide, t0 and G are constants.

- Thermo-chemical model (E model) is another widely cited dielectric breakdown model, reviewed by Mcpherson[MCPH98]. It is explained by the applied electric field interacts with the weak Si – Si bonds associated with oxygen vacancies in the amorphous SiO2 film. The applied electric field ultimately breaks the weak bond and creates a permanent defect or trap.

These traps can form a conduction subband in dielectric. The t_{BD} is proportional to Eox, see Equation I-13

$$t_{BD} = t_0 \, exp(-\gamma E_{ox})$$ Equation I-13

Where t0 and γ are constants.

- Anode hydrogen release (AHR) model: the energy released by the injected electrons at the anode may active hydrogen release at the anode, besides creating holes. The released hydrogen diffuses through the oxide and can generate electron traps.

The TDDB mechanism models are still an open question, especially for the acceleration law of the $t_{BD,}$ which depends on Eox model and 1/Eox model.

3.6.2.2. *Device degradation induced by TDDB*

With the technology scaling, the transistor oxide thickness continue to shrink to below 2nm. In previous TDDB failure mechanism part, we explained that in thin oxide transistors, the more common failure is soft breakdown. As Figure I-43, after the first step, the percolation path is created and transistors begin to suffer soft breakdown failure with gate leakage current slowly increasing. But the circuit could always function without failure. After the first SBD, the physical parameter of transistor as threshold voltage and transconductance would not strongly affect [WEIR97]. But in the second stage, transistor could be suffered multiple SBD, and the cumulative failure could attain 20% variation of threshold voltage. The absolute threshold voltage increase 75mV from its origin value 0.3V in the research of Haggag [HAGG06]. Transconductance and mobility follow the same trends. They decrease up to 30% after multiple SBD [LI01]. The result is a drain current decreases about 10% after multiple SBD [HAGG06] [LI01].

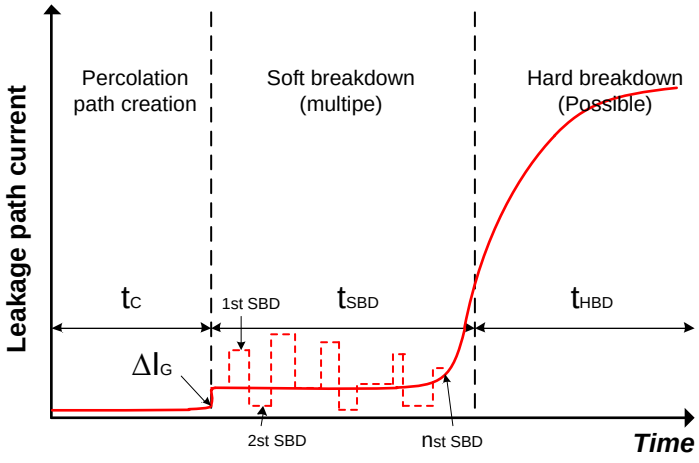

Figure I-43: Three stages of breakdown in thin oxide transistor [KAZC04]

When the gate leakage reaches a critical threshold, the breakdown evolves into the third stage: HDB which has a catastrophe level of leakage current through the oxide. Transistor gate lost its isolation and ability to control the channel current, thus accompany the decreasing of the gate

resistance, the drain current and gate capacitance. The increasing of traps around percolation path made more degradation on Vth and Gm. [POMP99]

Kaczer showed that time to oxide breakdown in PMOS is an order of magnitude higher than NMOS [KACZ02a]. The experimental showed that the first breakdown probability for NMOS in a ring oscillator was 87%, which proof that TDDB in NMOS is more important.

3.6.2.3. TDDB models overview

There exist numerous models dedicated to describe the degradation due to TDDB since the device post-breakdown behavior is extremely complicated. The device I-V characteristics after gate oxide breakdown rely on many parameters including: breakdown location, transistor type, voltage polarity, device operation mode (accumulation or inversion), oxide area and even poly-gate doping type. The models attempt to describe the behavior of the transistor and used for prediction the response of circuits to TDDB. As a bibliography, there are some representative models in the recent researches:

- Power law leakage current model: developed by Rodriguez et al. [RODR03], it models the oxide soft-breakdown as a progressive wear out phenomenon. They used a nonlinear voltage-dependent current source between gate and drain or gate and source depending on the breakdown location. They used this model in an inverter to model the oxide leakage current between the inverter input and output. (Figure I-44).

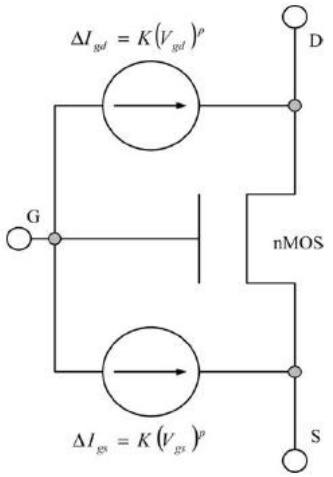

Figure I-44: Power law leakage current model. The exponent p varies from 5 to 2 as the degradation level increases. K reflects the "size" of the breakdown spot. [BERN06]

This model assumed that hard breakdown is part of a continuum of progressive soft breakdown.

- Two transistors model: A frequently discussed TDDB circuit model proposed by Kaczer [KACZ02b], based on NMOS with hard gate oxide breakdown. They considered two situations, with negative bias on gate and positive bias on gate. When VG < 0, the n-type gate/breakdown path and p-type substrate form a diode with forward bias. The oxide breakdown is due to electrons emitted from the n-type gate, which flow through the n-type breakdown path, diffuse along the substrate and are collected by the n-type source/drain

junctions. This mechanism is exactly that of a bipolar transistor with an emitter at the breakdown path, a base at the substrate and a collector at the source/drain. Therefore the NMOS with negative bias can be modeled with a gate resistor, two bipolar transistors and the original NMOS. Since NMOS in usual circuit is always bias with positive voltage, this bipolar based model is not of primary interest. When VG > 0, the n-type gate/breakdown path and n-type inversion channel is an ohmic contact. The electric field penetrates from the gate through the breakdown path and depletes the contact region of the breakdown path and substrate. This contact region serves as an electron sink and can therefore be treated as an additional drain of two small NMOS with their gate on gate of original MOS and sources on the source and drain of the original MOS respectively. as illustrated in Figure I-45

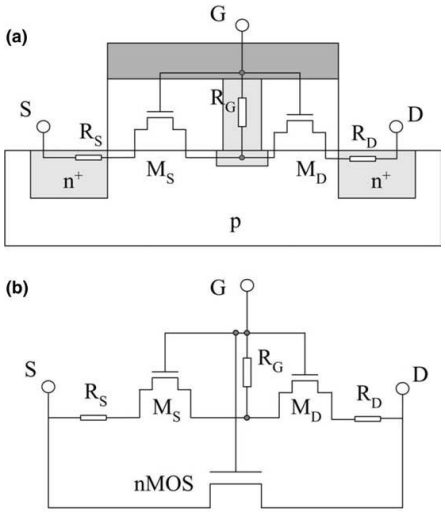

Figure I-45: TDDB two transistor model for NMOS with HBD and under positive gate voltage. (a) the cross-section view of breakdown structure. (b) Equivalent circuit model [BERN06

The gate resistance RG corresponds to the breakdown path. Two adjacent NMOS are characterized by level 1 SPICE model. Two resistors (R_S and R_D) are related to resistance in the source and drain extensions. The breakdown location is represented by the proportion of the length of both transistors. Gate to source/drain extension breakdowns are represented by logarithmically varying the extension resistances (R_S and R_D).

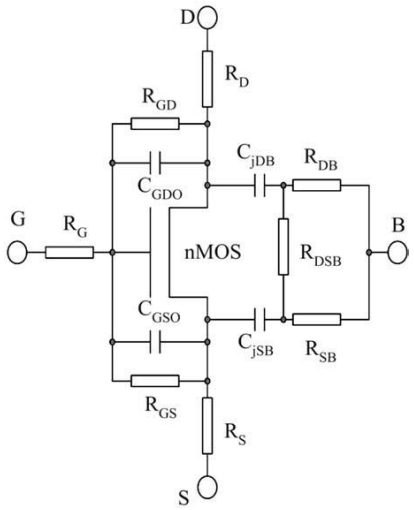

Figure I-46: TDDB RF equivalent circuit model [BERN06]

- RF failure circuit model: proposed by Yang [YANG03], it is dedicated for RF application. It consists in an original NMOS transistor, surrounded by terminal resistances (RG, RD, RS), substrate resistances (RDB, RSB, RDSB), overlap parasitic capacitances (CGDO, CGSO), junction capacitances (CjDB, CjSB), and two inter-terminal resistances (RGD, RGS), as illustrated in Figure I-46. RG and the "H" type substrate RC network are included for more accurate RF modeling. RGS and RGD vary in opposite directions representing different breakdown locations along the channel from source to drain. The inclusion variation of RGD and RGS represent the change of the device input S-parameter S11, providing an additional connection between gate and drain/source, which therefore degrades the reverse transmission coefficient S12 (thus the transconductance Gm), and changes the output impedance S22.

3.7. Negative bias temperature instability (NBTI)

3.7.1. Negative bias temperature instability overview

The bias temperature instability (BTI) is a degradation problem for MOSFETs, which has been studied since the 1960s. In the recent year, it became a widely concern issue in IC reliability, since the gate electric fields have increased with transistor dimension scaling, chip operating temperature increase, replacement of buried channel MOSFET by surface channel. The nitrogen was introduced into oxide to reduce gate leakage and to inhibit boron penetration in thin oxide device. In the BTI issue, the most important and interesting issue is the Negative bias temperature instability (NBTI) for PMOS. Under the negative bias and elevated temperature, there are interface traps and oxide charge created inside the oxide of PMOS. The NBTI phenomena could degrade transistor performance by increasing the absolute threshold voltage, decreasing the mobility, transconductance, drain current. (Figure I-47)

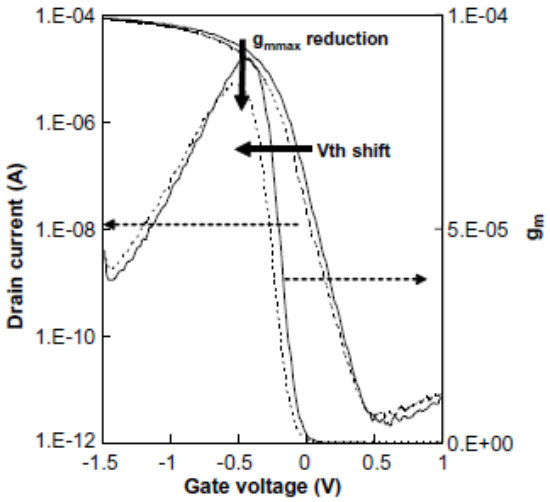

Figure I-47: Id – VG and Gm – VG curve for fresh device (full line) and after 10,000 s of stress (dashed line) for a PMOS with 2nm thick oxide at 125°C in the linear regime [HUAR06]

Similar to NBTI, the Positive bias temperature instability (PBTI) relates to under positive bias and elevated temperature for NMOS, but with the SiO2 based oxide transistor, the PBTI influence is less important compare to NBTI. (Figure I-48)

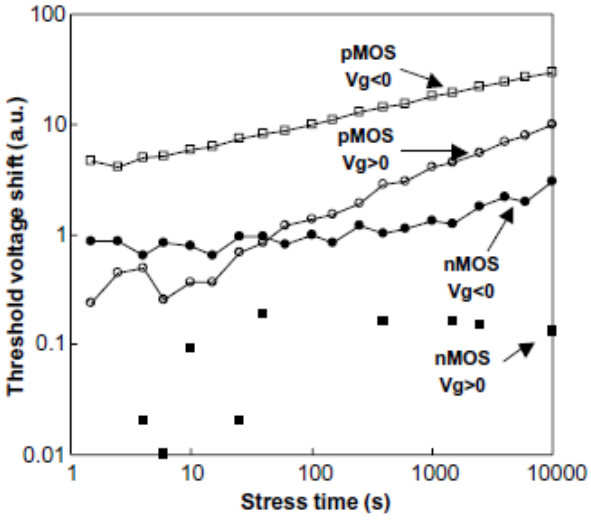

Figure I-48: Threshold voltage shifts as a function of stress time for both NMOS and PMOS devices under positive and negative bias stress conditions at 125°C [HUAR06]

The recent researches show that with the alternative high-k dielectrics, PBTI which is due to electron trapping in the high-k dielectrics layer could induce more significant degradation that NBTI [CRUP05].

3.7.2. NBTI Failure physical analysis

3.7.2.1. NBTI failure mechanism

Threshold voltage shift

In our research, we analyze the only NBTI mechanism. The transistor oxide defects impact the isolation of the dielectric and the transistor electrical characteristics. The PMOS threshold voltage could be expressed by Equation I-14

$$V_{TH} = V_{FB} - 2\Phi_F - |Q_B|/C_{ox} \qquad \text{Equation I-14}$$

Where $\Phi_F = \left(\frac{KT}{q}\right)\ln\left(\frac{N_D}{n_i}\right)$ and $|Q_B| = \sqrt{4q\varepsilon_{Si}N_D\Phi_F}$

Q_B is the semiconductor charge density, Cox is the oxide capacitance, Φ_F is the Fermi potential.

The flat band voltage V_{FB} is given by Equation I-15:

$$V_{FB} = \Phi_{MS} - Q_f/C_{ox} - Q_{it}/C_{ox} \qquad \text{Equation I-15}$$

Where Φ_{MS} is the work function difference between the gate and the substrate, the Q_f is the fixed charge and Q_{it} is the interface trapped charge. Since neither the gate nor substrate doping density nor oxide thickness change during stress, the threshold voltage shift is only due to the change of Q_f and Q_{it}. The net threshold voltage shift is given by (Equation I-16):

$$\Delta V_{TH} = \Delta Q_f / C_{ox} + \Delta Q_{it} / C_{ox} = q(\Delta N_f + \Delta N_{it}) / C_{ox} \quad \text{Equation I-16}$$

The interface traps increase could induce the mobility degradation due to the surface related scattering. So the root source of the parameter degradation is the oxide defects (N_{it} and N_f).

R-D model

The generation of interface trap was explained by Jeppson and Svensson [JEPP77] with the model of reaction – diffusion (R-D) model which described the device degradation as a combination of two effects. The first step, the field dependent electrochemical reaction at the Si/SiO2 interface can activate the defects that are electrical inactive at interface. The Si/SiO2 interface contains numerous dangling bands which are reduced by annealing procedure with hydrogen and forming Si-H bonds. The reaction breaks the Si-H bonds, generates interface state N_{it} and a mobile hydrogen is released, related species X are formed (Equation I-17)

$$S_i - H = S_i^+ + X_{interface} \quad \text{Equation I-17}$$

The actual diffusing species X have not yet been identified. Possibilities include interstitial atomic hydrogen (Hi), molecular hydrogen (H2), hydroxyl (OH) group, and proton [RASH01].

In the second phase, these species transport away from the interface into the dielectric and leave the $Si_3{\equiv}Si\cdot$ dangling bonds to be the interface traps. Also the reverse process is possible: transport of a diffusing hydrogen species back to the interface and re-passivation of a $Si_3{\equiv}Si\cdot$ dangling bond.

Saturation and recovery

NBTI induced physical parameter shift is not unlimited and it would trend to saturate over time. One possible reason is the reaction limitation mechanism, the generation of $Si_3{\equiv}Si\cdot$ decreases as the number of available Si-H bonds reduces with time. (Figure I-49)

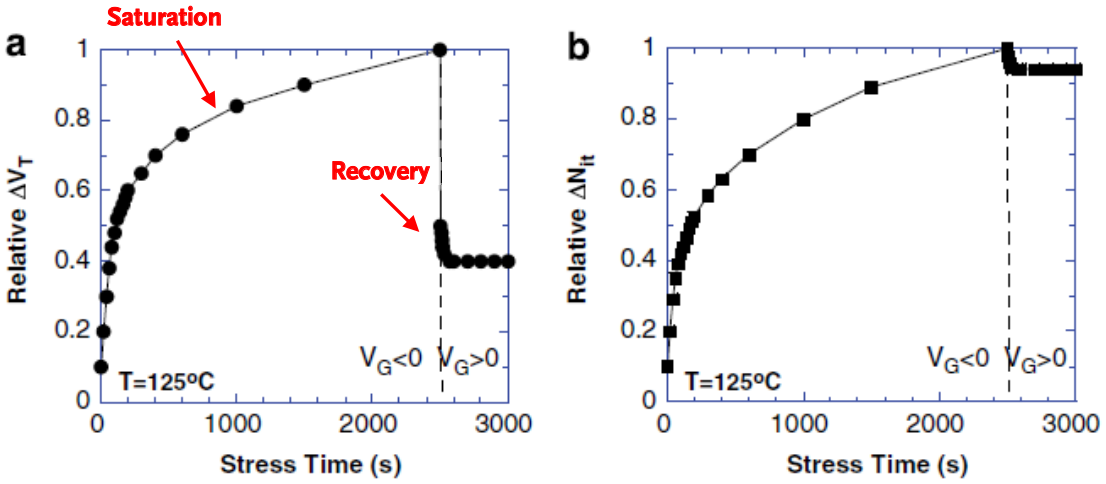

Figure I-49: Relative shifts for (a) ΔVT and (b) ΔNit versus stress time for negative and positive gate voltage. [SCHR06]

Degradations due to NBTI tend to recover after the stress removed. The mechanism of recovery is always an open question for researchers. Huard at al. have done extensive measurements and find partial recovery [HUAR06]. They attribute NBTI degradation due to interface trap generation and hole trapping. As explained in previous paragraph, threshold voltage shift depends on the oxide defects (interface traps charge Nit and fixed oxide charge Nf). Like the interface traps generation Si3≡Si·, the positive fixed oxide charges O3≡Si+ is generated from the dissociation of Si-H bonds by holes in the Si inversion layer during the NBTI. When the stress on gate removed or change to positive voltage could reduce the degradation of the device (as Figure I-49), as the X species might move back from the oxide to interface forming the repassivation of the Si dangling bonds and the holes trapping in oxide could be neutralized. The experiments made by Huard [HUAR06] showed that the interface trap density remains largely unchanged during the recovery phase. The recovery of NBTI degradation mainly due to the hole trapping relaxed during recovery, the positive voltage could neutralize the trapped holes.

The recovery phase makes the measured degradation due to NBTI is more relax than the real degradation as there is always a delay time between the stress and characterization for recovering. Also under interrupted stress or AC stress, the net degradation is less than for the same DC equivalent stress time without relaxation intervals (Figure I-50). The ratio of AC to DC degradation is affected by the duty cycle. At 50% duty cycle, the net ΔV_{TH} is less than one-half of the variation observed after DC stress.

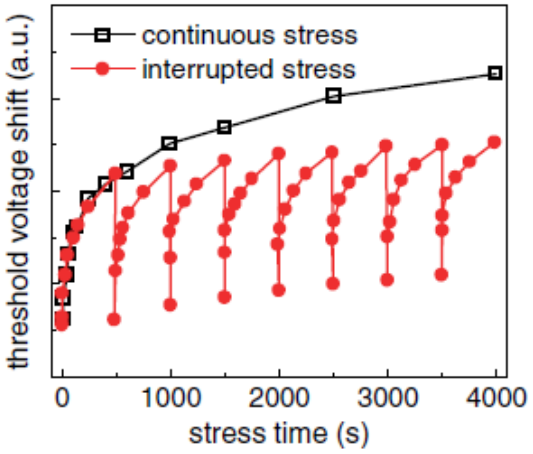

Figure I-50: Threshold voltage shifts for a continuous stress (open squares) and for interrupted stress with an positive bias interval [HUAR06]

The time dependence of the threshold voltage shift (ΔV_{TH}) is found to follow the power law model (Equation I-18)

$$\Delta V_{TH}(t) = At^n \qquad \text{Equation I-18}$$

Where A is a constant that depends on oxide thickness, field and temperature. n is a variation parameter (0.2 – 0.3) according to the diffusion equations and depending on the stress type, the n increase by the delay time increasing. The temperature dependence of NBTI follows the Arrhenius law with activation energies ranging from 0.18V to 0.84V [CHAP06] [STAT06].

3.7.2.2. Device degradation induced by NBTI

The NBTI could degrade the MOSFET (especially PMOS) physical parameters. Generation of interface states and oxide charge could reduce the mobility and increase the absolute value of threshold voltage. The increase of threshold voltage absolute value leads to a decrease of the channel leakage current (Ioff). The linear drain current (Idlin) and saturation current (Idsat) would be also reduced due to the degradation of hole channel mobility (μ) and threshold voltage (V_{TH}). The formation of NBTI damages in the source/gate and drain/gate overlap region could result in an increase source and drain channel resistance (Rds). The gate to drain (Cgd) and gate to source (Cgs) overlap capacitances increase due to generated interface traps.

3.7.2.3. NBTI model overviews

The NBTI equivalent model is used for circuit simulation. The most severe NBTI degradation is PMOS threshold voltage absolute value increase ΔV_{TH}, which is equivalent to PMOS absolute gate to source voltage decrease. White [WHIT08] proposed an equivalent model for NBTI effect on PMOS, depicted in Figure I-51. A gate resistance R_G is added between the original gate biasing point G and the PMOS NBTI model effective gate terminal G′. This allows inclusion of a gate leakage current sources between gate and drain /source, so that the NBTI model can be included with the TDDB model without a conflict developing by having a voltage source and current source at the same node.

The current flowing through the gate resistance could lead to an increase the voltage difference between G and G', thus a decrease of the effective G' terminal voltage. In the model, RG is a voltage dependent resistance because gate leakage currents are voltage dependent, while the gate to diffusion leakage current follows the power law dependence with V_{GD} and V_{GS}. The default value of p is set to 5 and K is $3 \cdot 10^{-6}$ [RODR03].

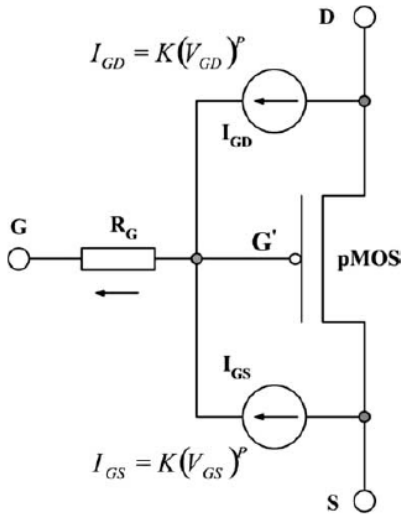

Figure I-51: NBTI circuit model. NBTI induced PMOS threshold voltage shift modeled as absolute gate to source voltage decrease by adding a gate resistance and voltage controlled current source. [WHIT08]

For PBTI on NMOS, a similar structure to Figure I-49 can be constructed, except that all current flowing directions are reversed and the model fitting parameters (threshold voltage and leakage current) would be different. [LEE04]

3.8. Degradation mechanisms impact conclusion

In the previous paragraphs, we introduced four important degradation mechanisms: Electromigration (EM), Hot carrier injection (HCI), Time dependent dielectric breakdown (TDDB), and Negative bias temperature instability (NBTI). In the wear-out phase, they could degrade interconnection and gate oxide integrity. And thereby induce circuit functionality failure.

EM mainly happens in metal interconnection. It could cause the rupture of interconnects and the creation of open circuits, or short circuits between the neighbor wires. Other three degradation mechanism relate to the defect of the gate oxide of transistor which affects the transistor physical parameters. Table I-10 sums up the characteristics of the three main transistor related mechanisms [WU05] [SCHR03]:

	HCI	TDDB	NBTI
Origin	High kinetic energy carrier induced interface trap and fixed oxide charge	Formation a conducting path through gate to substrate	Bias induced interface trap and fixed oxide charge creation.

	generation		
Activation energy	-1.0eV	0.7eV	0.4eV
Transistor type	Primarily on NMOS	NMOS/PMOS	Primarily on PMOS
Recovery	no	no	yes
Threshold voltage (abs) (|VTH|)	Increase	Increase	Increase
Acceleration factors	High Vds Low temperature	High absolute Vgs High temperature	High absolute Vgs High temperature
Transconductance (Gm)	Decrease	Decrease	Decrease
Mobility (μ)	Decrease	Decrease	Decrease
Gate oxide capacitance (Cgs/Cgd)	Decrease	Decrease	Increase
Channel resistance (Rds)	Increase	no	Increase
Drain saturation current (Idsat)	Decrease	Decrease	Decrease
Transistor linear current (Idlin)	Decrease	Decrease	Decrease
Other	Substrate current (Ib) increase	Gate leakage current (Ig) increase/input impedance decrease	Channel off current (Ioff) increase

Table I-10: Oxide defects based degradation mechanism impact conclusion

In our Ph.D. research, we firstly focus on the last three oxide/interface defects based degradation which closely relate to the transistor parameters degradation. These degradations of the transistor parameter could lead to circuit characteristic changes thus could induce change of circuit electromagnetic emission or susceptibility to interferences.

4. ELECTROMAGNETIC ROBUSTNESS OF INTEGRATED CIRCUITS

As our stated in the previous two paragraphs, the EMC have risen in importance as low emissions and high immunity to interference have emerged as key differentiators in overall IC performance. Advances in process integration, higher switching speeds, and more complex circuits tend to increase the amount of parasitic emissions generated by ICs. Reduced supply voltage and an increased number

of interfaces tend to decrease the immunity to radio frequency interference. EMC has become a major cause of IC redesign, mainly due to inadequate design methods and lack of expertise in parasitic noise reduction and immunity improvement.

Simultaneously, devices working in extreme environments (as over voltage, high/low temperature) could suffer from wear out failure. Even under normal operation condition, after several years' operation, the components would move to their wear-out phase in the reliability bath-tub curve. The wear out degradation mechanisms could result in circuit functionality failure. Even sometimes the device could continually work without fail (soft failure), their performances would be degraded since the transistor's physical parameter has been shifted due to the wear out mechanisms. Among these circuit performances (operation frequency, static noise margin…), Electromagnetic compatibility margins could also be modified with time, increasing the risk of compliance failure to the EMC standards, as immunity decreases under certain level or emission increase exceeds the limitation.

As an example of immunity variation after aging in Figure I-52, after aging, the immunity level of device could decrease below the initial immunity standard limit, cause safety problem. From the statistical point of view, the immunity level of all components has a Gaussian distribution. At the beginning of releasing of the product, only few of them has EMC problem as the small probability failure. However, if the average of immunity level decreases with time increase, the probability failure risk proportion increases. The products could be considered not safety any more.

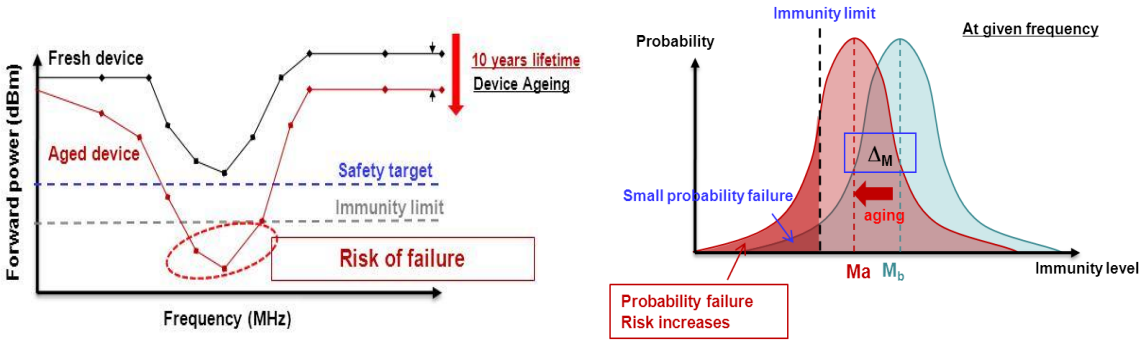

Figure I-52: Immunity level decrease with device aging (left) worst case, (right) statistical view [LI10]

In nowadays, the EMC qualification tests are often carried out on the fresh devices (or only primary burn-in), but do not verify or considered reliability impact along their lifetime.

In this context, a new request from electronic equipment suppliers aiming at ensuring the electromagnetic robustness (EMR) of embedded systems appeared recently with emphasis on going further in electromagnetic behavior improvement at the IC level [PFAF05]. The proposed research topic forms a bridge between two communities: "IC reliability" and "IC electromagnetic compatibility" communities which are often not overlapped before. The goals of the topic are to firstly prove the aging effects on EMC of ICs and then clarify the link between ageing induced IC degradations and related EMC drift. With a series projects, we hope to provide the EMR

characterization and simulation methods, propose the guidelines to IC and equipment designers to ensure EMC during lifetime of their applications.

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Chapter 2: Experimental investigations about ageing effect on EMC

In this chapter, we will explore the evolution of electromagnetic robustness (EMR) with two devices under test. In the first section, we begin with presenting the methodology used to characterize the evolution of EMR, the EMC of ICs (Conducted emission and conducted immunity) measurement methods, the environmental reliability tests used for ageing component, in the fourth and fifth part of this section, the measurement uncertainties calculation and experimental results statistical analysis methods are described. The second section gives a comparison of tested device' conducted emission before and after high temperature and low temperature operating life tests, test results show a reduction of emission level after both types of ageing and a simple model is given to explain the decrease of emission for an inverter. The third section deals with the evolution of conducted immunity before and after ageing. Two test devices are used to evaluate the degradation of immunity level. Significant degradations have been observed and among different test blocks, the analog part is more critical than the digital ones. Finally, the emission and immunity evolution results are summed up and the research perspectives are discussed.

1. DEVELOPMENT OF EMR CHARACTERIZATION METHOD

There is a growing demand for high performance, reliable and safe electronic devices around all application fields. In semiconductor reliability aspect, since it is often more difficult to improve the reliability of device after it has been released, as more efforts as possible should be exerted to design units that inherently reliable, as known as "Design for reliability" or DFR. The products should follow several reliability design rules and could evaluate their reliability with model to guarantee product lifetime under operation condition. The predicable model for reliability simulation needs to consider the dominant failure mechanisms evaluation which could be gained by device reliability qualification. The reliability research for semiconductor device could provide a guard band between the "real life" of the device and customer's specification.

We are also concerned about the variation of EMC performance of the device along their lifetime. As the current EMC test standards only consider the EMC compliance at the beginning life of the device, the reliability test flow is not included in the EMC test to evaluate the device aging induced EMC compliance variation. We proposed a new electromagnetic robustness (EMR) characterization flow to combine the EMC and reliability together [BOYE09].

1.1. General principle of characterization

The EMR characterization of a circuit consists in measuring the evolution during time of its parasitic emission and/or its susceptibility to radiofrequency interferences (RFI) before and after circuit ageing. To be efficiently, as in reliability research, the aging test always compress the test duration scale by a stress which accelerates the intrinsic degradation mechanisms. The flow of EMR qualification is illustrated in Figure II-1.

The objective of the EMR qualification is to compare circuit emission and immunity level before and after an accelerated ageing test. In order to characterize accurately the small variation in the test, the error caused by measurement need to be limited: taking the precautions in the experimental protocol, using of equipment with long term stability.

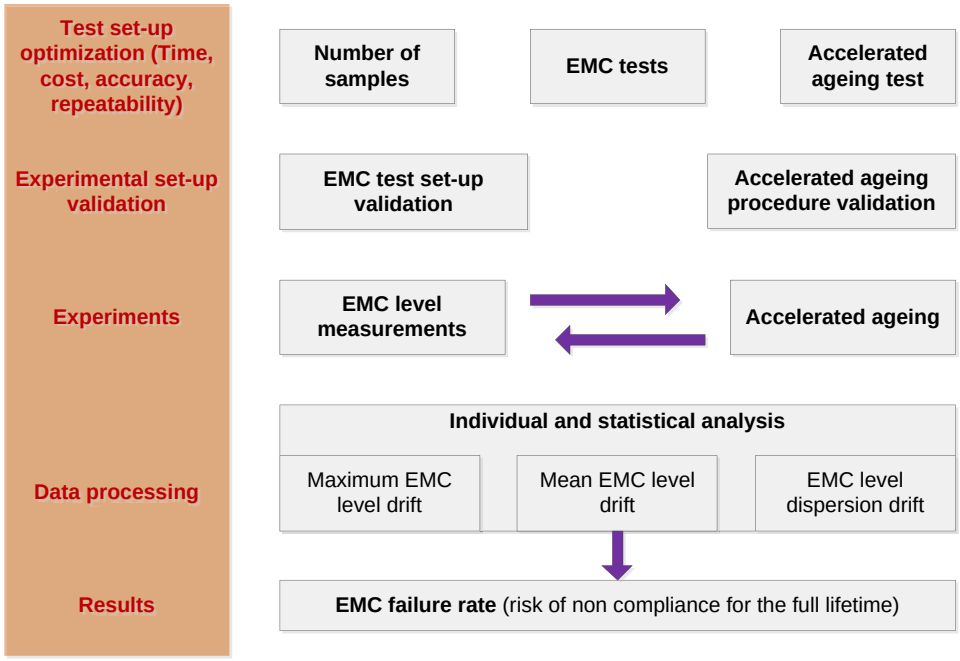

Figure II-1: EMR qualification flow

The first step is linked to the choice and the optimization of the different parts of the set-up, in order to save both time and costs of the set-up, and improve the accuracy and repeatability of the measurements. First, a compromise on the number of tested samples in found to ensure a sufficient level of confidence in measured EMC drifts and avoid too long characterization time. EMC test bench

contains several error sources which prevent from the extraction of ageing effects on EMC so that it must be carefully planned. The design of EMC test board, the choice of passive components with low tolerance and the EMC test procedure (e.g. the susceptibility threshold extraction algorithm during immunity test) should be carefully optimized to reduce both repeatability and uncertainty issues.

The accelerated aging phase adds also uncertainties. As several samples are used to characterize the EMR of a component, the aging stress must be identical for all the samples. Moreover, the applied stress on each component must be controlled over all the stress duration. Thus, the stress conditions and the activity of circuits under test have to be accurately monitored. As the number of measurements can be large and as the delay between the end of aging procedure and EMC tests should be reduced, detailed tests plan is mandatory.

Once the EMC and the accelerated aging procedure set-ups have been completely defined, they have to be validated experimentally. The validation step must prove that aging procedure can only have an impact on the DUT. The EMC validation step must ensure that the EMC measurements are enough repeatable to extract precise information concerning the EMC drifts related to aging effects. Measurement repeatability and uncertainties set a limit for the consistency of EMC level drifts.

At the end of the measurement campaign, the EMC measurement results obtained before and after aging are processed to extract statistical data concerning the EMC level drifts, such as the worst case or mean drifts. These data are required to predict the risk that a component becomes incompliant after aging.

1.2. EMC of ICs measurement method selection adapted to EMR

We have chosen measurement methods dedicated to ICs and proposed by international standards such as IEC 61967 and IEC 62132. The conducted measurement methods are preferred because they offer a better repeatability than radiated measurement methods. The disadvantages of the radiated measurements: for emission test, the coupling is strongly influenced by the configuration of component under test respected to the measuring apparatus (distance, orientation), highly dependent to the test environment (significant difference if the measurement is made in anechoic chamber or reverberation chamber). In addition, the radiated emission levels of the circuit are lower, the dimensions of the circuit and its package are electrically small, and the measured level is much noisy. The PCB track, the ground plane, and the cables constitute the more important radiated sources. However, our interest is the emission of the circuit which needs to isolate from the emission from the system. For immunity, the problems are same with emission. The aggression that we applied is global, thus do not allow an isolated aggression.

In EMR characterization flow, we chose conducted EMC measurements which consist:

- Emission: 1Ω/150Ω test (IEC 61967-4); [IEC61967-4]

- Immunity: Direct power injection (IEC 62132-4); [IEC62132-4]

1.2.1. Conducted emission test

Most EMC problems in IC originate from the RF current due to IC transient activity which propagates outside the circuit along power supply and ground paths. IEC 61967-4 defined the method with two probes placed on a test board to characterize IC conducted emission.

The direct RF current measurement, as 1 Ω conducted measurement, defined in the IEC 61967-4 standard [IEC61967-4], is dedicated to the measurement of the conducted emission on one or more ground pins of a component up to 1GHz. The amplitude of the total current return to the circuit ground can then be characterized. Figure II-2 describes the principle of this measurement.

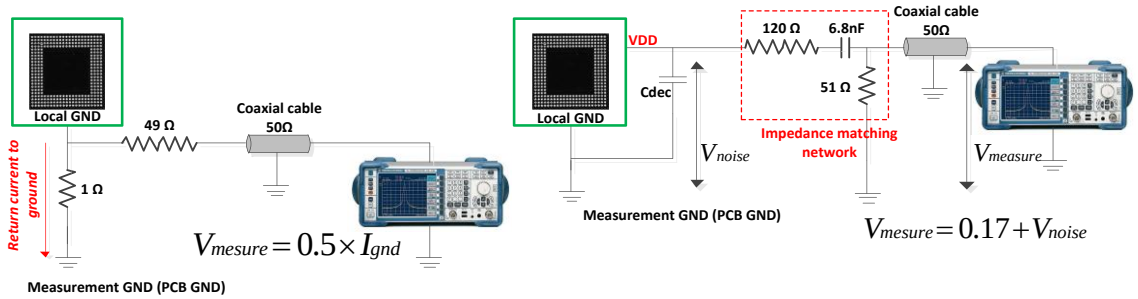

Figure II-2: Conducted emission methods 1Ω (left)/150Ω (right)

The current flows out of local ground of the IC to the measurement ground through a 1 Ω resistance placed between the local and the measurement grounds. The current is converted to voltage by this resistive probe and measured by a spectrum analyzer, thus giving us a current image. A 49 Ω resistor is placed in series with 1 Ω resistor to ensure a 50 Ω matching. The impedance of this resistor or probe must remain as stable as possible throughout the measurement, so that the design quality of the probe and the passive component selection (tolerance of 1% on resistance values is required) is critical.

To characterize the conducted emission along power pin and I/O up to 1GHz, the RF voltage measurement, known as 150 Ω conducted method, defined in the standard IEC61967-4 is proposed. This test is used to identify the contribution of emission of the chip pin which connect directly to long (longer than 10cm) PCB traces or wiring harness. As shown in Figure II-2, the combination of 2 resistors and a capacitor provides an equivalent output load impedance as typical antenna impedance 150 Ω and an input impedance of the spectrum analyzer to 50 Ω adaptation above 150 kHz over a wide frequency band.

Conducted emission measurement set-up is controlled by Labview program, the algorithm of the program is explained by Figure II-4-left. At each frequency sampling point, we measure the voltage drop of the 1 Ω probe or the voltage on the terminal of 150 Ω impedance matching networks.

1.2.2. Conducted immunity test

Direct power injection (DPI) is a standard method used to characterize IC immunity to RF interference coupled on one or several pins of a circuit, as defined in IEC 62132 - 4 [IEC62132-4]. It consists in injecting conducted disturbances on IC pins, such as I/O, power supply, clock… it can characterize the minimum of electromagnetic immunity level of the IC pin over a frequency range up to 1GHz.

Figure II-3 shows the typical DPI set-up for injection on a power supply pin. The RF disturbance is generated by the combination of a synthesizer signal and a power amplifier. In general, the maximum forward power is set between 17 and 30dBm, depending on the type of aggressed pin [IEC62132-4]. In our experiment, as we try to trigger component failure, we can exceed the standard limit and increase the amount of forward power up to the saturation limit of the power amplifier. A directional coupler is used to extract forward and reflected waves in the injection path which are then measured by using a double channel power meter. This measurement allows a control of the power injected during injection. The RF disturbance is finally superimposed on the useful signal (DC power or input signal) and applied to tested pin using a decoupling network or bias tee, composed of a capacitor or DC block and a choke inductor or a resistor, which isolates the source of the useful signal from RF disturbance. The value of the bias tee configuration depends on the useful signal frequency range. The component choice and the bias tee design have to be carefully done to ensure a low reflection loss between the RF disturbance source and the IC pin (S12 > -3dB) and a high isolation between RF disturbance source and useful signal source (S12 < -10dB).

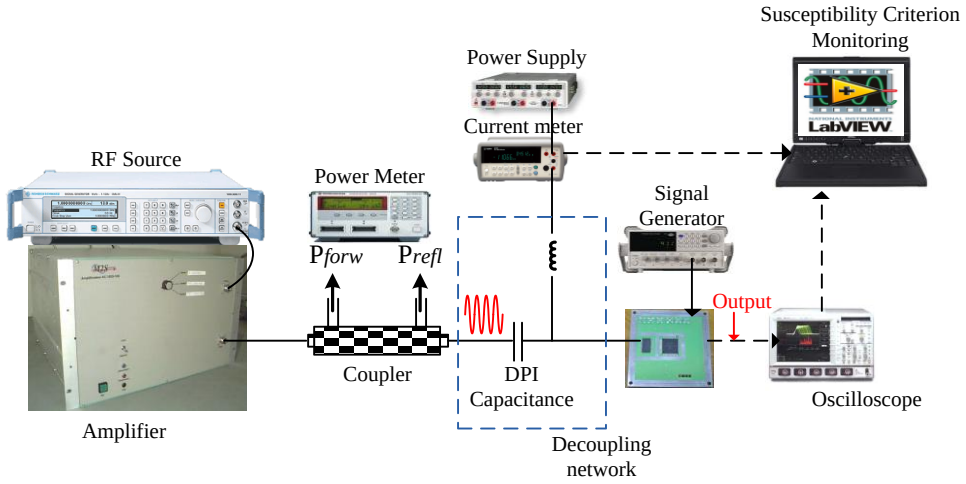

Figure II-3: DPI configuration

One or several susceptibility criteria have to be defined before susceptibility tests. They define what is considered as a circuit failure (e.g. a rest, noisy digital level, jitter amount, voltage offset…). During injection, the failure appearance is detected by an oscilloscope. The current consumption of the

circuit is also monitor by a digital meter. For different blocks, the susceptibility criteria are not the same. They will be defined in the case study paragraph, according to the test chip.

Conducted immunity measurement set-up is controlled by Labview program, the algorithm of the program is explained by Figure II-4-right. At each frequency sampling point, the RF source power is always increased by step 1dB until failure firstly, then by 0.1dB to find a more accurate amount of forward power value by step 0.1dB. The failure types for each frequency point are not the same. For part of frequency range, the major failure would be dynamic failure (such as jitter) and some other frequency points show static failure. In the case that on most part of frequency, the power reaching to maximum, we can adjust the maximum power to a higher level.

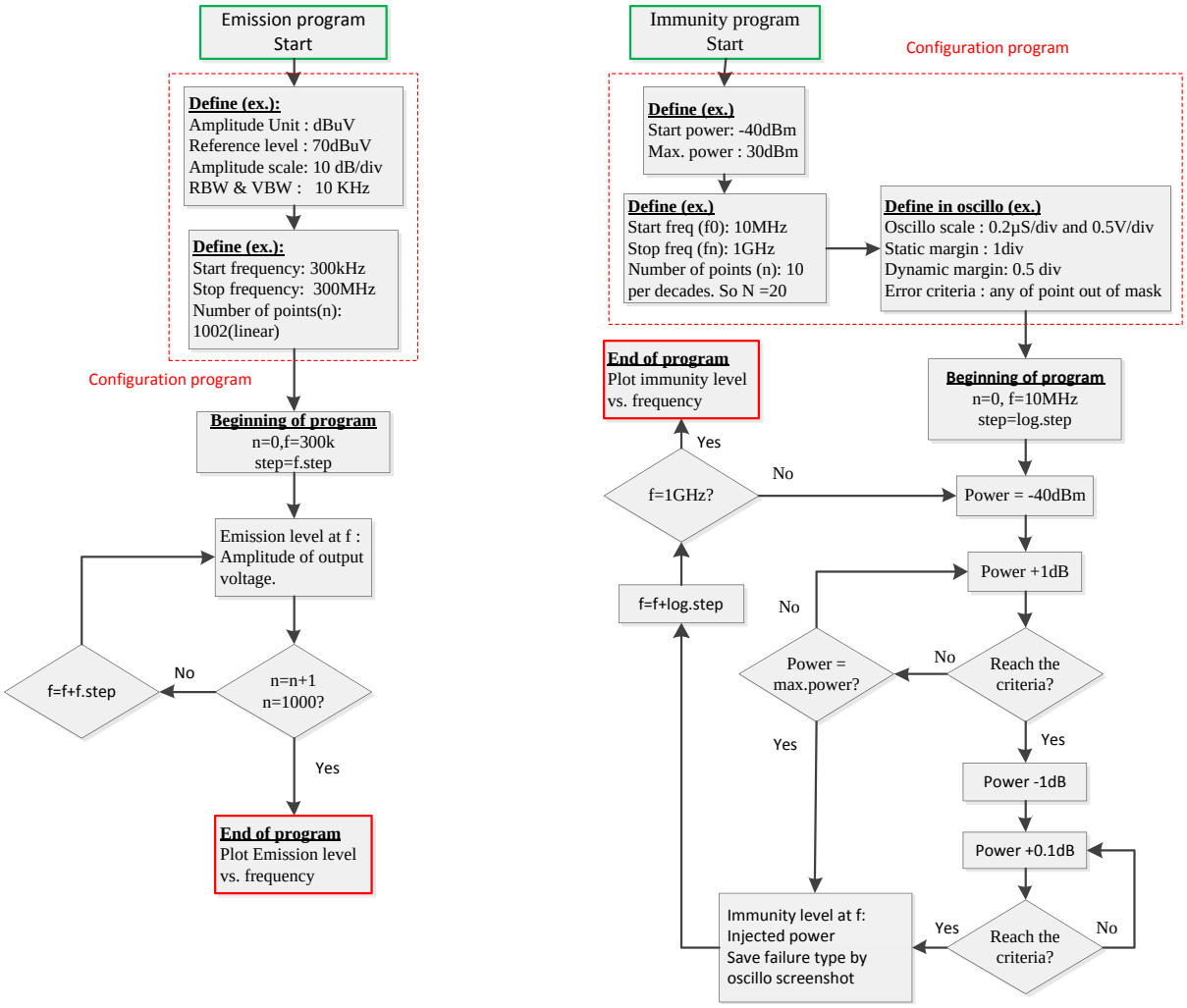

Figure II-4: Automatic measurement controlled by Labview program. The algorithm of program of conducted emission (left) and conducted immunity test (right)

1.3. Accelerated lifetime test

Accelerated lifetime tests are required to qualify ICs and guarantee the quality and robustness of applications. To scale the qualification test, it always applies acceleration lifetime test, e.g. applying over voltage on the input and power supply in high or low temperature during a relative short period. With this test, we can extrapolate the behavior of the device under test (DUT) after several years. The ratio of real products' lifetime and stressed test time is defined by acceleration factor. The stress level should be reasonable. Over-stress could induce direct failure or incorrect lifetime prediction. The concept is illustrated in Figure II-5.

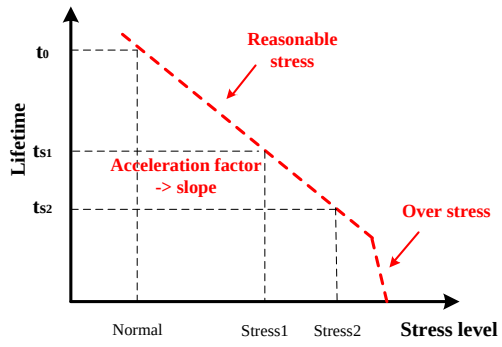

Figure II-5: With different stress level, different accelerate lifetime could be obtained. Under reasonable stress range, the normal operation lifetime could be calculated with stress related acceleration factor.

1.3.1. Temperature acceleration

Most of wear out failure mechanisms can be accelerated by using temperature stress (high or low). The thermal acceleration factor is determined from the Arrhenius equation. See Equation II-1,

$$AF_T = e^{\frac{E_a}{K}(\frac{1}{T_0}-\frac{1}{T_s})} \qquad \text{Equation II-1}$$

Where:

Ts: Accelerated stress temperature in Kelvins

T0: Typical operating temperature in Kelvins

Ea: Activation energy in eV. For different failure mechanism, activation energy is different, see section 2.6.

K: Boltzmann's constant, 8.61e-5 eV/K

For example, a device with 0.18µm which suffers an oxide defect (NBTI), has activation energy Ea is equal to 0.3eV, for a typical operation temperature of 55°C. If the temperature is increased up to 150°C, the thermal acceleration factor is equal to 10.86. [JEDEC 122] [LOUG01].

1.3.2. Voltage acceleration

The voltage stress is more complicated. Depending on the device type and failure mechanism, the model can be very different. For MOS device with gate oxide related failure, the Eyring-exponential model works well. The voltage acceleration factor can be calculated as follow (Equation II-2):

$$AF_V = e^{\beta(V_s - V_0)}$$ Equation II-2

Where:

Vs: Accelerated stress voltage

V0: Typical operating voltage

β: Experimentally determined constant based on dielectric integrity data. It depends on the failure mechanisms and oxide thickness.

For example, a device with technology 0.25µm, the β is around 3. The circuit typically operates at 2.5V and is stressed at 3.5V, the voltage acceleration factor is 20.09.

1.3.3. Overall acceleration

The combination of thermally stress and voltage stress could make a further acceleration. The overall acceleration factor can be obtained by multiply two independent acceleration factors AFT and AFV where the Ea and β are assumed stress-independent [JIN06]. As shown in Equation II-3:

$$AF_O = AF_T \times AF_V = e^{\frac{E_a}{K}\left(\frac{1}{T_0} - \frac{1}{T_s}\right) + \beta(V_s - V_0)}$$ Equation II-3

We combine the two example of voltage stress and temperature stress in section 1.3.1(AFT = 10.86) and 1.3.2(AFV = 20.09). The overall acceleration factor is equal to 218. If the DUT is estimated to 10 years, with the combination of voltage and temperature stresses, the test duration would be 400 hours (17days), as illustrate in Figure II-6.

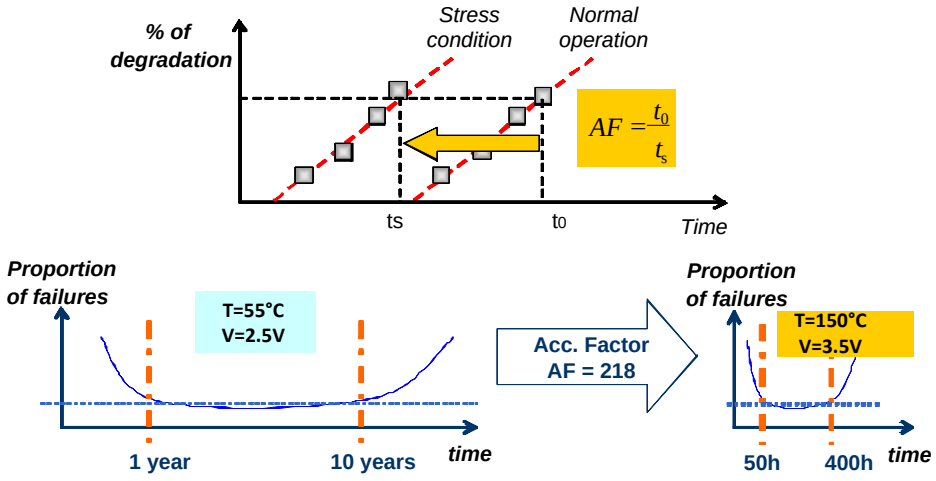

Figure II-6: **principle of accelerated ageing obtained by combination of high voltage and temperature stress**

1.3.4. Acceleration aging methods

There exist different reliability aging methods which have been standardized by several organizations, such as IEC standards, JEDEC standards (specified for commercial devices), and AEC standards (specified for automotive devices)… They were usually derived from the common source MILSTD – 883. Below lists the aging methods that we chose, they are defined in JEDEC and AEC standards. [AEC-Q100] [JEDEC22].

- High temperature operating life (HTOL): DUT works in a dynamic or static mode. The operation condition is under high temperature and bias to overvoltage input terminals. They include: supply voltage, clock frequencies, input signals, etc. They may be operated even outside their specified values, but resulting in predictable and nondestructive behavior of the DUT. HTOL test is typically test for EM, NBTI, and TDDB failure mechanism.
- Low temperature operating life (LTOL): is basically just the low temperature equivalent of the HTOL test. It is intended to look for failures caused by hot carriers.
- Electrical stress: under room temperature, with overvoltage stress on special terminal and special configuration to active different failure mechanism.

1.4. Measurement uncertainties

The EMR test aims at extracting the EMC level drifts induced by aging as accurately as possible. The measurement uncertainties due to both the set-up and the device under test must be reduced and controlled. Before the test, we have to calculate the uncertainty budget to estimate interval between the measurement result and the true value. This uncertainly budget contains the likely error sources and their individual uncertainty limits and probability distribution. The sources of uncertainty can be grouped into two types [SCHAFFNER]:

- Random effects: random variation due to measurement set-up (antenna position, cable form, room temperature…), which can be evaluated by repeated measurements. This type of contribution is in the form of a "standard uncertainty", so that it does not need further treatment when all the uncertainties contributions are summed.
- Systematic effects: error remains unchanged (a constant offset from the true value) when a measurement is repeated under constant conditions. The systematic error can be given by calibration certificates, case references, manufacturers' specification… It remains constant during the measurement but may change if the measurement conditions, methods or equipment are altered. The combined uncertainty can be calculated with the summation of all different contribution sources. The standard uncertainty for each contribution source can calculates with different probability distribution factor according the type of source: Normal

distribution (factor equal to 2 when giving confidence level of 95%, e.g. the calibration certificates…), rectangular (factor equal to √3, e.g. the manufacturers' specification value…), U-shaped (factor equal to √2) and triangular (factor equal to √6). The standard uncertainty can be calculated with expanded uncertainty (for each source) divided by probability distribution factor [LAB34].

The combined uncertainty, Uc, is obtained for m contributions by taking the square root of the sum of squares of the individual standard uncertainties. (See Equation II-4)[CISPR16]:

$$U_c = \sqrt{\sum_{i=1}^{m} U_i^2} \qquad \text{Equation II-4}$$

The uncertainty result is usually given in term of expanded uncertainty. It is calculated by multiplying the standard uncertainty (Ui) by a coverage factor k equal to 2, providing a level of confidence of approximately 95%. (Equation II-5) [CISPR16].

$$U_{exp} = 2 \times U_c \qquad \text{Equation II-5}$$

1.4.1. Conducted emission uncertainties

With the conducted emission set-up defined in section 1.2.1, we can calculate the uncertainty of our conducted emission test bench. The measurement error budget is described in Table II-1[CISPR16] [LAB34].

	Contribution	Value		Probability distribution	Divisor	Ui	Ui²
1	Spectrum analyzer reading	0.71	dB	Normal	2	0.25	0.0625
2	Cable loss	0.3	dB	Normal	2	0.15	0.0225
3	Measurement repeatability	0.5	dB	Uniform	1	0.5	0.25
						√(∑Ui²)	∑Ui²
Combined standard uncertainty			dB	Normal		0.63	0.398
Expanded uncertainty			dB	Normal k=2		**1.26**	

Table II-1: Conducted emission measurement uncertainty calculation

In this calculation, we firstly assume that the system measurement repeatability is 0.5dB. According to different DUT and set-up, this value could be variable. The total conducted emission measurement uncertainty is ±1.26dB expressed at 95% confidence level using a coverage factor k=2.

As in our experiments, the EMC test set-up remains the same before and after ageing test, we interest only in the drift of emission level, thus the measurement uncertainty can be simply characterized by using directly repeatability test. For instance, with the same set-up and same DUT, the measurement is repeated n times. The standard deviation σ_R (expressed by Equation II-6) is used as the standard uncertainty, and U_R expresses the measurement uncertainty with 95% confidence level (coverage factor of 2).

$$\sigma_R = \sqrt{\frac{1}{n-1}\sum_{1}^{n}(S_i - M_R)^2} \qquad \text{Equation II-6}$$

$$U_R = 2 \times \sigma_R$$

Where n is the number of repeatability measurement on the same component, the larger number of repeat measurement, the more that the result converges to the real repeatability value. Si is each repeatability measurement results. M_R is the mean value of n measurements.

1.4.2. Conducted immunity uncertainties

With the conducted immunity set-up defined in section 1.2.1, we can calculate the uncertainty of conducted immunity. The measurement error budget is described in Table II-2 [SCHAFFNER].

	Contribution	Value		Probability distribution	Divisor	Ui	Ui²
1	Power meter reading	0.4	dB	Normal	2	0.2	0.04
2	Signal generator	0.2	dB	Rectangular	√3	0.115	0.013
3	Amplifier	0.5	dB	Rectangular	√3	0.289	0.083
4	Oscilloscope	0.4	dB	Normal	2	0.15	0.0225
5	Coupler	0.75	dB	Normal	2	0.375	0.1406
6	Cable loss	0.3	dB	Normal	2	0.15	0.025
7	Measurement repeatability	0.5	dB	1	1	0.5	0.25
						Ui	∑Ui²
Combined standard uncertainty			dB	Normal		0.645	0.4156
Expanded uncertainty			dB	Normal k=2		**1.289**	

Table II-2: Conducted immunity (DPI) measurement uncertainty calculation

In this calculation, we firstly assume that the system measurement repeatability is 0.5dB. According to different DUT and set-up, this value could be variable. The total conducted immunity measurement uncertainty is ±1.289dB expressed at 95% confidence level using a coverage factor k=2. In case of our immunity test for EMR qualification, the measurement uncertainty, as we defined in conducted emission, we use directly the sample standard deviation (σ_R) as the measurement standard uncertainty, and U_R expresses the measurement uncertainty with 95% confidence level (coverage factor of 2) (Equation II-6).

.

1.5. Statistical analysis

In the EMR qualification flow, we select a sample of DUT from the whole group of device and measure their EMC level before and after aging. With the statistical analysis of the samples results, we can make inferences about the characteristics of the whole population which is assumed to follow Gaussian distribution.

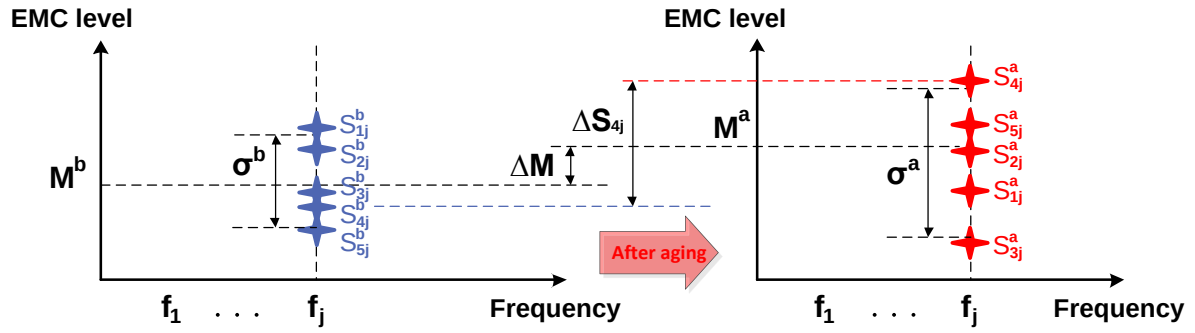

Figure II-7: Measurement of EMC level drift after aging with a set of samples

During the EMC measurement, the EMC levels (Emission/Immunity) are measured on each sample at each frequency point. (Sampled frequency points distribute uniformly on log/linear frequency scale). Illustrate in Figure II-7. The statistical analysis can be done by a matrix calculation (Equation II-7).

$$\underbrace{\begin{vmatrix} S^a_{11} & \cdots & S^a_{1j} \\ \vdots & & \\ S^a_{i1} & \cdots & S^a_{ij} \end{vmatrix}}_{\text{After aging}} - \underbrace{\begin{vmatrix} S^b_{11} & \cdots & S^b_{1j} \\ \vdots & & \\ S^b_{i1} & \cdots & S^b_{ij} \end{vmatrix}}_{\text{Before aging}} = \underbrace{\begin{vmatrix} \Delta S_{11} & \cdots & \Delta S_{1j} \\ \vdots & & \\ \Delta S_{i1} & \cdots & \Delta S_{ij} \end{vmatrix}}_{\text{Aging drift}}$$

Samples (i) × Frequency (j)

Equation II-7

The first i by j matrix presents the measurement results after aging, the second matrix is the results before aging. The element S_{ij}^{a} indicates the EMC level of ith sample at frequency point j after aging. ΔS_{ij} shows the EMC level drift of ith sample at frequency point j after aging.

The statistical analysis of EMR qualification consists in extracting mean and maximum drift values, and standard deviation variation.

1.5.1. Mean drift

With two EMC level matrixes, we can obtain the **average EMC level drift for all N samples at each frequency point (j)** after aging, It is equal to the average of j_{th} column of the aging drift matrix, as shown in Equation II-8:

$$\Delta M_j = \frac{1}{N}\sum_{i=1}^{N}(S_{ij}^{a} - S_{ij}^{b}) \qquad \text{Equation II-8}$$

Where N is the number of the sample, j means at j_{th} frequency points.

The **average EMC level drift for all N samples over all frequency range** is: (Equation II-9)

$$\Delta M = \frac{1}{M}\sum_{j=1}^{M}\Delta M_j \qquad \text{Equation II-9}$$

Where M is the number of the frequency sampling point. j means j_{th} frequency points.

1.5.2. Standard deviation (St.Dev.)

Emission and immunity levels cannot be accurately known as they are subjected to statistical distributions due to measurement errors and process variability among components. The standard deviation is a good indicator of variation or dispersion in the measurement statistical distribution. If a set of samples is measured, we can estimate the standard deviation for the whole population with the sample standard deviation. The sample standard deviation (SSD) after ageing and sample standard deviation drift could be calculated by Equation II-10

$$\Delta\sigma_j^{a} = \sqrt{\frac{1}{N-1}\sum_{i=1}^{N}(S_{ij}^{a} - \Delta M_j)^2} \qquad \text{Equation II-10}$$

$$\Delta\sigma_j = \Delta\sigma_j^{a} - \Delta\sigma_j^{b}$$

1.5.3. Maximum drift

Emission and immunity level drift worst cases are also be characterized. The **maximum drift after aging on certain frequency** point is, given by Equation II-11:

$$D_{max} = Max.(\Delta S_{ij}) \qquad \text{Equation II-11}$$

2. CHARACTERIZATION OF AGING IMPACT ON EMISSION: CASE STUDIES

In order to characterize the impact of aging on emission, we study the evolution of the emission with time through several study cases. We measured emission of a series of DUT samples before and after aging and analyzed the evolution of emission level with the statistical methods mentioned in the previous session.

2.1. Case study 1: Digital input/output in CMOS 65nm

2.1.1. Device under test description

The DUT is a 65nm low power CMOS circuit designed by ST Microelectronics at Crolles in France. It is mounted on an 8mm x 8mm LFBGA package (Low profile fine pitch ball grid array) with 64 pins. The DUT is composed of various types of bidirectional I/Os with different current drive abilities and optional Schmitt trigger to reduce the susceptibility to input interferences, and pull-up/pull-down resistive structures. Table II-3 summarizes the characteristics of the I/O structures. The DUT is supplied by two separate supply networks, VDDE/GND for I/O buffer part and VDD/GND for I/O internal part (Core) logical core supply.

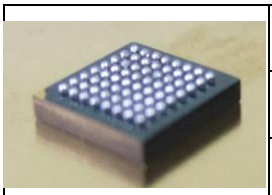	Technology	CMOS low power 65nm
	Package	LFBGA 64 8x8mm
	I/O power supply (VDDE)	2.5V
	Core power supply (VDD)	1.2V
Input pin	Input buffer structure option	Output drive current
IN1	Schmitt trigger and pull down	2mA
IN2	Schmitt trigger and pull up	4mA
IN3	Non Schmitt trigger and pull up	8mA
IN4	Non Schmitt trigger and pull down	2mA

Table II-3: ST 65nm test chip technical description

The test board is a 6 layer 100mm x 100mm PCB board designed according the TEM format defined by IEC standard 61967-1 [IEC61967-1] and dedicated to EMC measurements of ICs. The board used material with reference 4000-7 SI which is resistant to high temperature up to 150°C. The DUT and test connectors are situated separately on the top side and back side of board. In the center of top side of the board, the DUT is connected and surrounded by ground plane.

2.1.2. Conducted emission test set-up description

Figure II-8 presents the set-up of the measurement conducted emission along the power supply of the DUT. The measurement set-up consists of a regulated power supply 2.5V/1.2V, 2 signal generators to apply input signals to DUT, a metallic ground plane and a spectrum analyzer to measure the ground noise level. The global ground of the DUT is connect to the PCB board ground which share the same the ground plane with all the measurement apparatus by the metallic plane. In contrast, for the 1Ω conducted emission set-up, the ground of test block is separated with common ground plane by the 1Ω emission probe. All the cables which likely influence the measurement result are fixed on the metallic plane to reduce the test repeatability error.

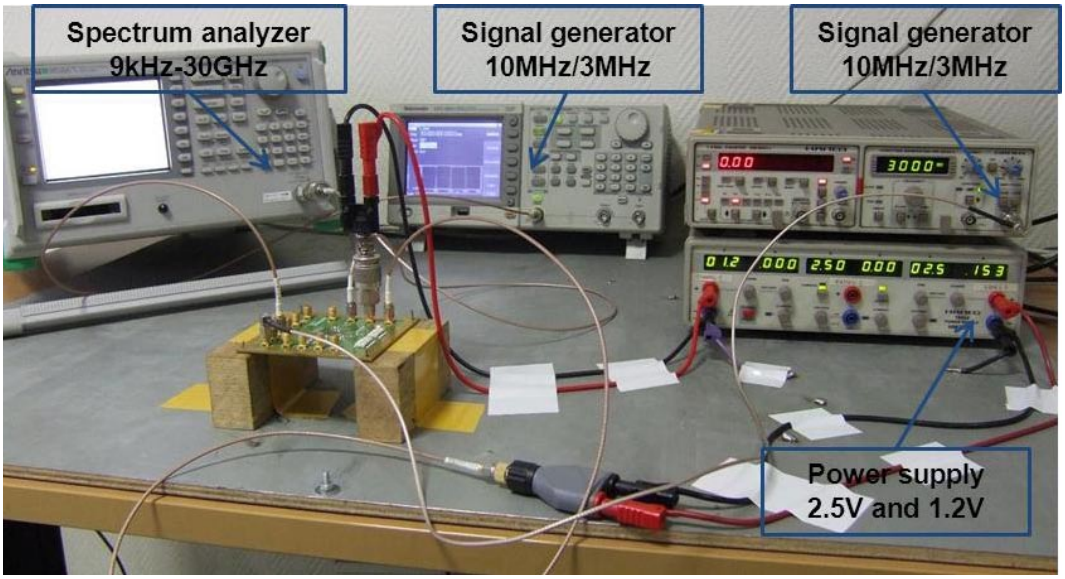

Figure II-8: Conducted emission 1Ω/150Ω equipment set-up

In the emission test, we activate the I/O blocs by applying on input a square signal with 2.5V peak to peak amplitude, as depicted in Figure II-9.

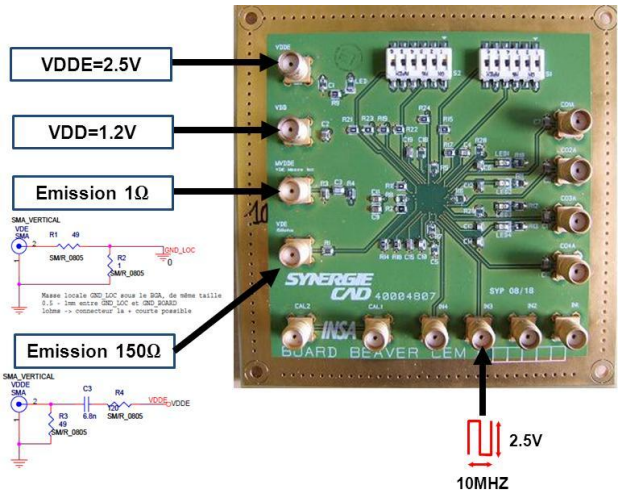

Figure II-9: Schematic of conducted emission measurement

The 1Ω conducted emission, in which the sum of ground current is measured. The measurement before ageing test is presented in Figure II-10-left. I/Os IN1 and IN3 are actived by applying respectively 3MHz and 10MHz 2.5V square signals. Local ground current spectrum is gathered with 1 Ω probe. In the emission spectrum measurement results, amplitude peaks appear at harmonic frequencies of 3MHz and 10MHz related to the activity of I/O blocks. Since the I/O IN3 has bigger current drive ability than IN1, the amplitude of 10MHz fundamental peak is higher than the one of 3MHz.The harmonics of the 3MHz and 10MHz peaks appear in their integer multiple frequencies and spread in the measurement range up to 300MHz. Moreover, peaks linked to intermodulation appear.

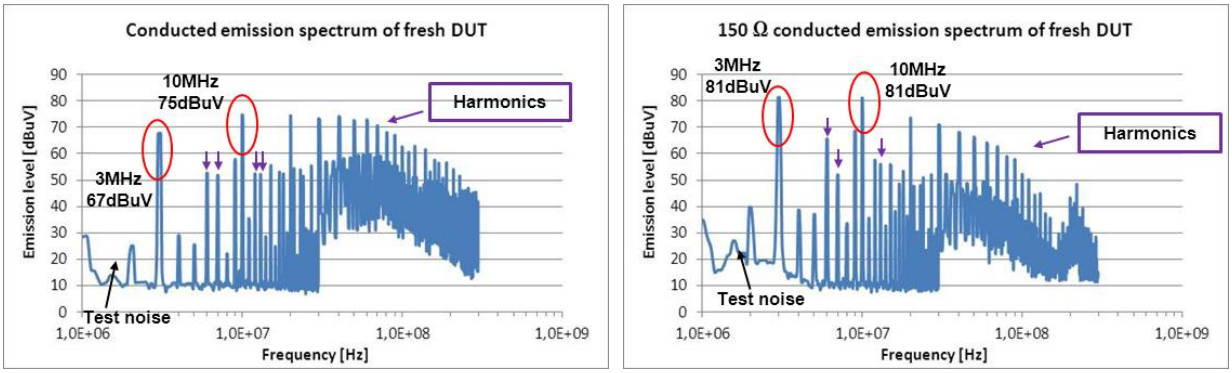

Figure II-10: conducted emission spectrum of the local ground (left) and of the power supply VDDE (right) for fresh DUT with 3MHz on input signal IN1 and 10MHz on IN3.

With the 150 Ω method, the contribution of power rail VDDE to emission can be identified. Figure II-10-right presents the emission measurement for the fresh DUT. I/O IN1 and IN3 are active by applying 3MHz and 10MHz 2.5V square signals. Emission due to analog power rail (VDDE) voltage fluctuation is measured via an impedance adaption network. Two fundamental peaks at 3MHz and 10MHz related to the activity of I/O blocks appear in the measured emission spectrum. The harmonics of the 3MHz and 10MHz peaks appear in their integer multiples frequency and spread in the measurement range up to 300MHz.

To improve the measurement, for both 1 Ω and 150 Ω methods, we apply only on IN3 the 10MHz input signal and extract the envelope of the amplitude of the emission spectrum for the harmonics of 10MHz. Since the measurement noise level is around 40dBuV, we focus only on harmonics with amplitude larger than 40dBuV.

2.1.3. Accelerated aging test set-up description

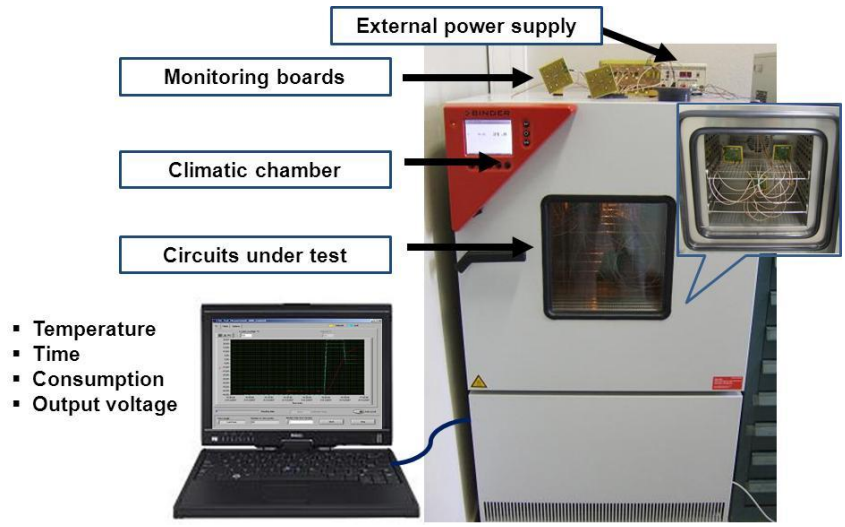

Figure II-11: Schematic of the principle conducted emission measurement configuration

For accelerated aging which we defined in section 1.3.4., with a climatic chamber, we are able to perform HTOL or LTOL (Figure II-11). The DUT is supplied by an external regulated power supply during the aging test. The DUT operation is monitored via specified circuits that external of the chamber.

The evolution of emission is qualified with 2 lots (5 DUT per lot) according to two different accelerated aging methods. The accelerated stress conditions for 65nm test chip are listed below in Table II-4:

Test type	Number of Sample	Description
LTOL	5 (1st-5th)	Low Temperature Operating Life, -40°C, total duration 408 hours, power supply at nominal Vdd + 10%, circuit digital inputs activated by a square signal with amplitude equal to nominal Vdd + 10%.
HTOL	5 (6th-10th)	High Temperature Operating Life, 150 °C, total duration 408 hours, power supply at nominal Vdd + 10%, circuit digital inputs activated by a square signal with amplitude equal to nominal Vdd + 10%.

Table II-4: ST 65nm test chip accelerated stress conditions

2.1.4. 1 Ω conducted emission evolution after ageing

2.1.4.1. Repeatability

To evaluate the repeatability of the 1 Ω conducted emission, this measurement has been repeated 10 times on the same component. The repeatability errors defined by Equation II-6 for each frequency before and after aging test are shown in Figure II-12.

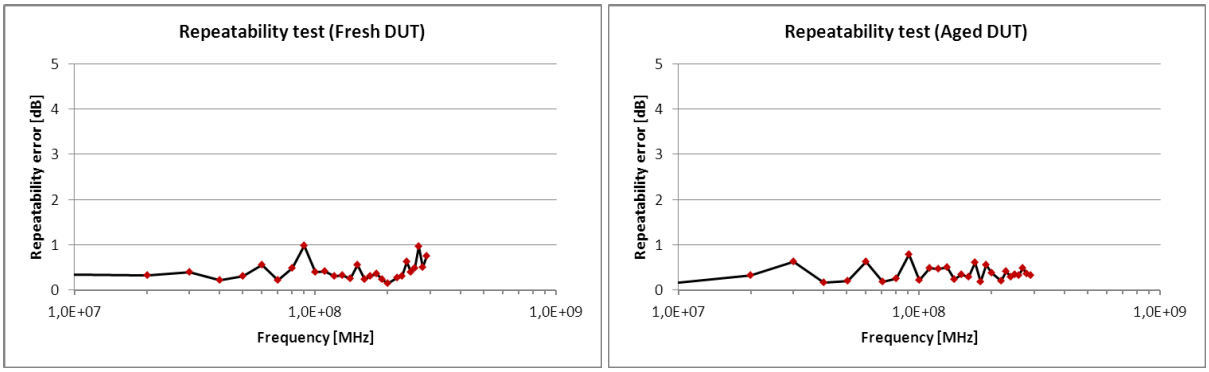

Figure II-12: 1Ω conducted emission measurement repeatability error for each frequency point before (left) and after aging (right).

The repeatability error is expressed by sample standard deviation (SSD). For the test before aging (Figure II-12-left), the maximum repeatability error is 0.97dB at 89.8MHz, thus the maximum repeatability measurement uncertainty (multiply by coverage factor of 2, see Equation II-6) is 1.94dB at 89.8MHz. The average of repeatability error over all the frequency range is 0.42dB, thus the mean repeatability measurement uncertainty over all the frequency range is ±0.84dB.

The same repeatability test procedure is performed on the aged component (Figure II-12-right). The maximum repeatability error is 0.78dB at 90.4MHz, thus the maximum repeatability measurement uncertainty (multiply by coverage factor of 2, see Equation II-6) is 1.56dB at 90.4MHz. The average of repeatability error over all the frequency range is 0.37dB, thus the mean repeatability measurement uncertainty over all the frequency range is ±0.74dB, which is similar to the repeatability measurement uncertainty before ageing.

2.1.4.2. *Experimental results before and after aging*

We compare the emission level evolution before and after different types aging by comparing the emission amplitude envelope when apply on input a 10MHz 2.5V square signal. 1st – 5th samples are dedicated to LTOL aging and 6th – 10th are dedicated to HTOL. Figure II-13 gives two examples of the most obvious variation among the samples aged according to LTOL or HTOL.

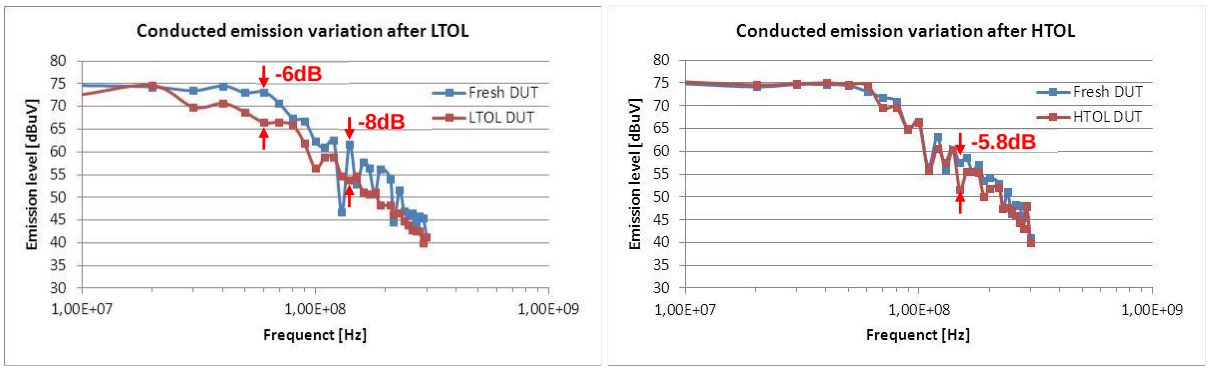

Figure II-13: 1Ω conducted emission measurement evolution after aging: 3rd sample after LTOL aging (left) and 6th sample after HTOL aging (right).

In these two examples, for both LTOL and HTOL test, the local ground emission levels tend to decrease after aging. After LTOL, between 40MHz and 70MHz, the emission level reduction can reach to 6dB at 60MHz. The maximum reduction of the 3rd sample is -8.05dB at 140MHz. HTOL does not induce the same reduction as LTOL. Emission level after HTOL has slightly decreased and could reach up to -5.8dB at 150MHz.

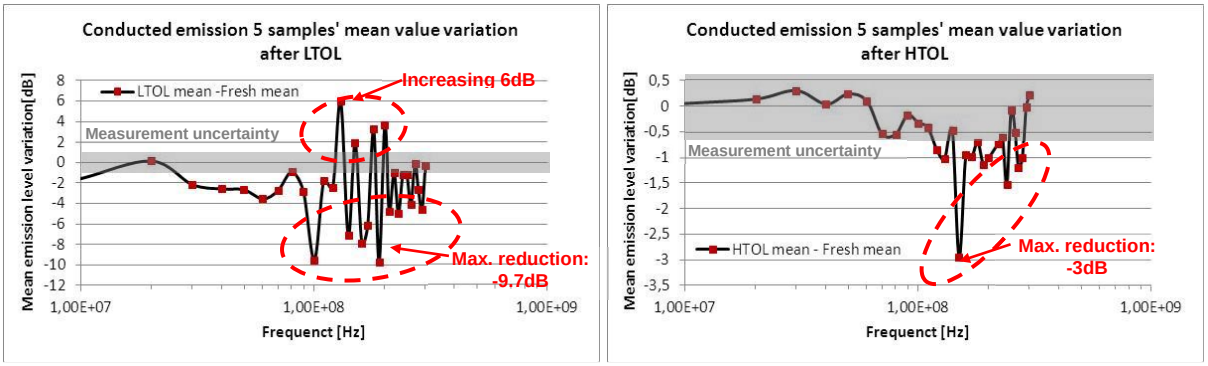

Figure II-14: Mean emission level variation for all 5 samples at each frequency after aging: 1st – 5th sample comparison after LTOL (left) and 6th – 10th samples comparison after HTOL (right).

For statistical analysis, we compare the mean emission values for all samples at each frequency point (calculate mean value for each column of the aging drift matrix, see Equation II-7) before and after different aging, as shown in Figure II-14. For the emission variation after LTOL, the comparison of mean emission level for five samples shows a big fluctuation, except in 4 frequency points showing increasing. Most of harmonic tend to decrease and the mean decreasing could reach to -9.6dB at 190MHz. After HTOL, the variation is more unified. Most harmonics tend to decrease and the maximum mean reduction could reach -3dB at 150MHz.

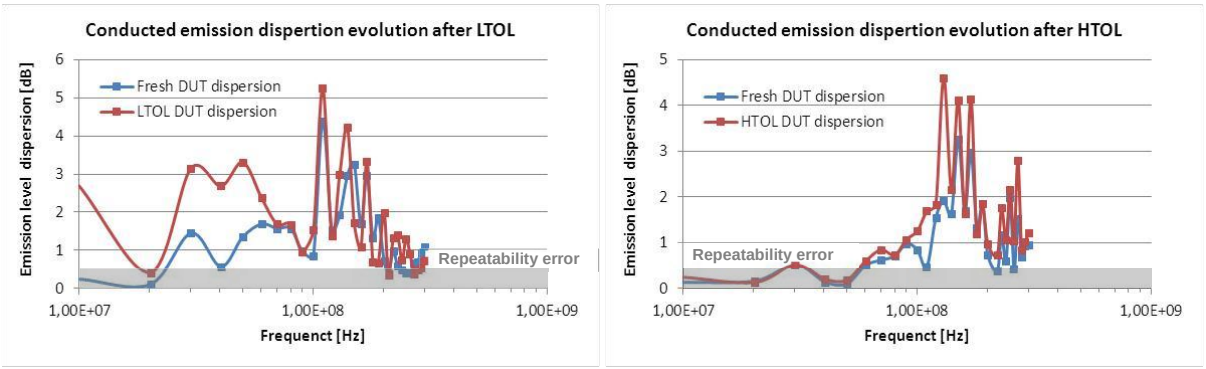

Figure II-15: 5 samples' emission level dispersions are compared before and after aging: 1st – 5th samples dispersion after LTOL (left) and 6th – 10th samples dispersion after HTOL (right)

To analyze the dispersion among the samples, we calculate the sample standard deviation (SSD) defined in Equation II-10. The comparison of the dispersion of five samples for LTOL and HTOL is given in Figure II-15. For LTOL, over the whole range of frequency, the dispersion of five samples after LTOL expands for most harmonics and the maximum increasing is 2.4dB at 10MHz. For HTOL, the comparison result shows the same trend with LTOL, the dispersion among five samples enlarge after HTOL. The maximum increasing is 2.7dB at 130MHz. The dispersion of emission level for the

fresh test samples is due to their process variation and measurement error (≈0.42dB, as explained in section 2.1.4.1). The enlargement of dispersion after aging could relate to various sources: the non-uniform aging for each sample; due to the process variation, the responses of components to degradation are not the same; …etc.

2.1.5. 150 Ω Emission results

2.1.5.1. Repeatability

150 Ω conducted emission repeatability characterization has been analyzed by repeating 10 times the measurement on the same component. The repeatability errors defined by Equation II-6 for each frequency before and after aging test are shown in Figure II-16.

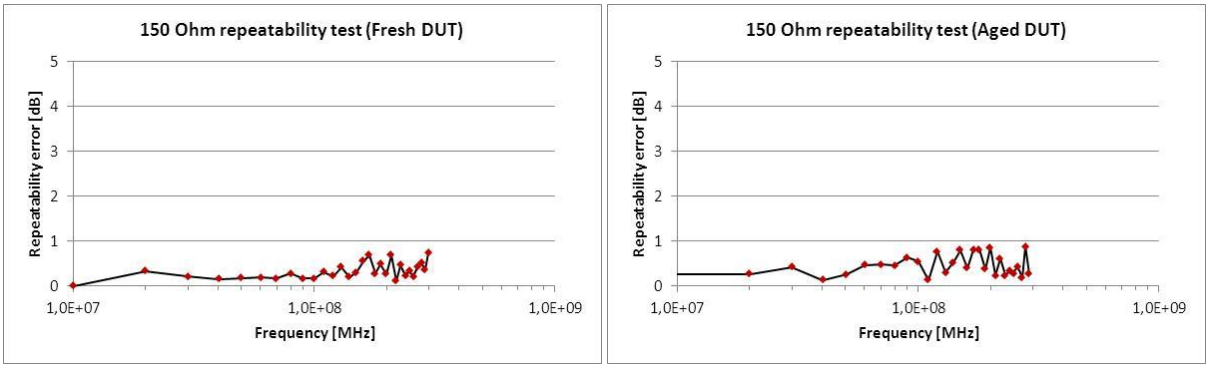

Figure II-16: 150Ω conducted emission measurement repeatability error for each frequency point before (left) and after aging (right).

The repeatability error is expressed by sample standard deviation (SSD). For the test before aging (Figure II-16-left), the maximum repeatability error is 0.74dB at 300MHz, thus the maximum repeatability measurement uncertainty (multiply by coverage factor of 2, see Equation II-6) is 1.48dB at 300MHz. The average of repeatability error over all the frequency range is 0.33dB, thus the mean repeatability measurement uncertainty over all frequency range is ±0.66dB.

And the same for the test after aging (Figure II-16-right), the maximum repeatability error is 0.88dB at 280MHz, thus the maximum repeatability measurement uncertainty (multiply by coverage factor of 2, see Equation II-6) is 1.66dB at 280MHz. The average of repeatability error over all the frequency range is 0.46dB, thus the mean repeatability measurement uncertainty over all frequency range is ±0.92dB.

2.1.5.2. Experimental results before and after aging

We compare the envelope of emission level before and after different types of aging procedure, the 1st – 5th samples are dedicated to LTOL aging and the 6th – 10th are dedicated to HTOL. Figure II-17 shows two examples of the most obvious variation among the samples for LTOL and HTOL.

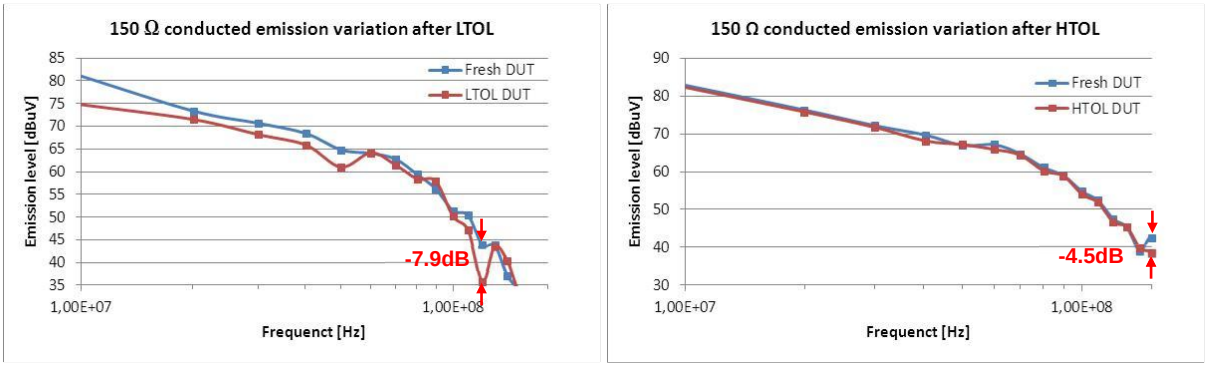

Figure II-17: 150Ω conducted emission measurement evolution after aging: 3rd sample after LTOL aging (left) and 10th sample after HTOL aging (right).

In these two examples, for both LTOL and HTOL test, the power supply emission levels tend to decrease after aging. After LTOL, in 10MHz to 50MHz range, the emission level reduction can reach to 6.3dB at 10MHz. The maximum reduction of the 3rd sample is 7.9dB at 120MHz. The reduction of the emission level measured after HTOL is not as pronounced as the variation measured after LTOL. Emission level after HTOL has slightly decreased and could attain to -4.5dB at 150MHz.

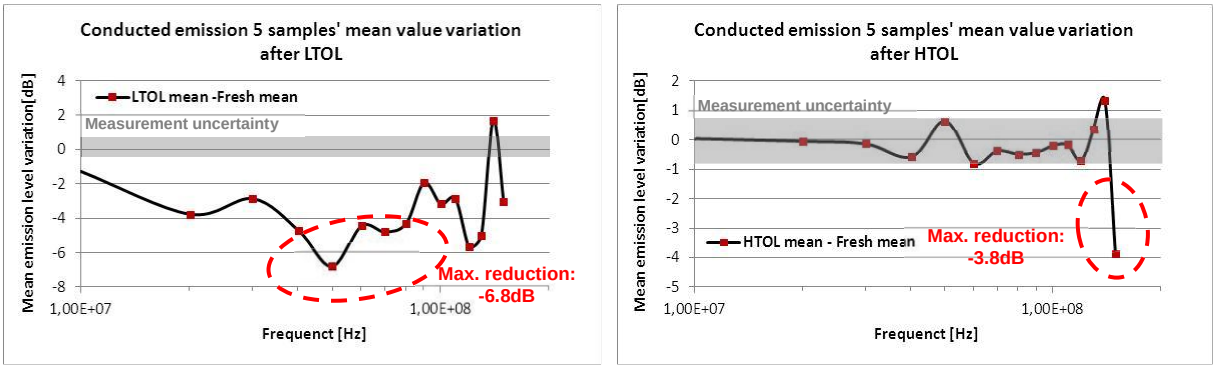

Figure II-18: Mean 150 Ω emission level for all 5 samples at each frequency after aging: 1st – 5th sample comparison after LTOL (left) and 6th – 10th samples comparison after HTOL (right).

For statistical analysis, the mean variation of emission level for all samples is plotted at each harmonic frequency (calculation of the mean value for each column of the aging drift matrix, see Equation II-7) before and after different aging, as shown in Figure II-18. For the emission variation after LTOL, the comparison of mean emission level for five samples has a big fluctuation, except in one frequency point showing increase at 140MHz. The harmonic amplitude level tends to decrease and the mean decrease reaches to -6.8dB. After HTOL aging, the variation is negligible since most of points fall into the measurement uncertainty zone. The maximum mean reduction appears at 150MHz and reaches -3.8dB.

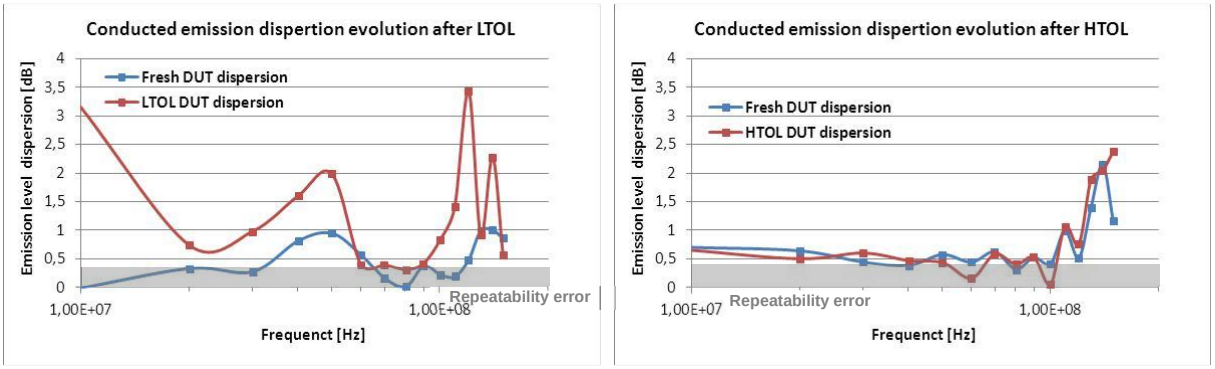

Figure II-19: 5 samples' emission level dispersions are compared before and after aging: 1st – 5th samples dispersion after LTOL (left) and 6th – 10th samples dispersion after HTOL (right)

Due to the process variation and repeatability error, there is dispersion among the emission levels for fresh DUTs measurement and aged DUTs measurement. The sample standard deviations (SSD) defined in Equation II-10 is characterized to quantify the dispersion among samples (Figure II-19). For LTOL, over the whole range of frequency, the dispersion of five samples after LTOL expands for most of the harmonics and the maximum increase is 3.1dB at 10MHz. For HTOL, the variation of dispersion before and after aging is negligible.

2.1.6. Conducted emission evolution conclusion

With the comparison of aging evolutions for ground current noise emission (1Ω method) and power supply conducted emission (according to 150 Ω method), we could summarize the effect of LTOL and HTOL on conducted emission of the studied digital I/O.

- According to the results shown in Figure II-14 with Figure II-18, the conducted emissions level tend to decrease significantly over a large frequency range after different types of ageing procedures (HTOL and LTOL).
- Dispersions among samples rise after aging for both LTOL and HTOL.
- LTOL has more important effects than HTOL on conducted emission level reduction for the studied component.

The observed emission level evolution after ageing allows us to conclude about the conducted emission issues induced by this component at a larger system level. From statistical point of view, we can assume that the emission level measured at a given harmonic frequency for a given component behaves as a random variable that follows a normal distribution (as depicted in Figure II-20). The mean value of emission levels decreases after aging driving the bell curve far away from the emission limit fixed to ensure system EMC. The risk of non-compliance of the circuit to the emission level is equal to the probability that a sample has an emission level larger than the emission limit. It can be computed by integrating the area under the distribution curve above the emission limit. Although the standard deviation of the distribution enlarges after ageing, as the variation of standard deviation is less than the decrease of the mean value of the distribution, the risk of non-compliance to emission

limit decreases after different aging. Thus the conducted emission problem of this component tends to relax after aging.

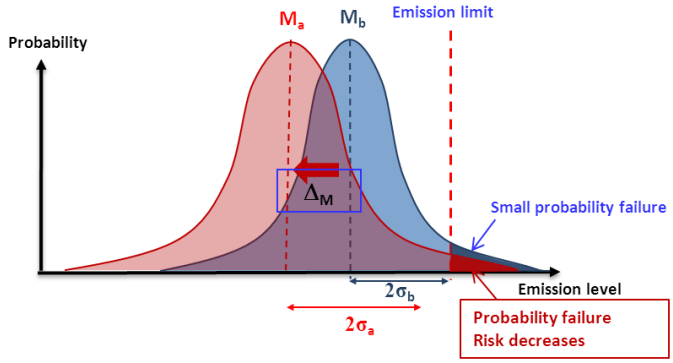

Figure II-20: Conducted emission level statistical distribution moving away from the emission limitation. The probability failure risk decreases after aging

What could be the origin of the measured reduction of the conducted emission level? We can try to propose hypothesis about this variation. First, the influence of the circuit degradation on the emission level reduction must be underlined. Indeed, in the previous test, both circuit and PCB have been aged. However, previous work has demonstrated that the evolution of the characteristics of the PCB board and passive devices was negligible compared to measured variation [AMAD08]. Thus we can conclude that the variation originates mainly from the IC itself. The conducted emission level reduction can be explained by a reduction of transient current amplitude and a slowing down of components switching.

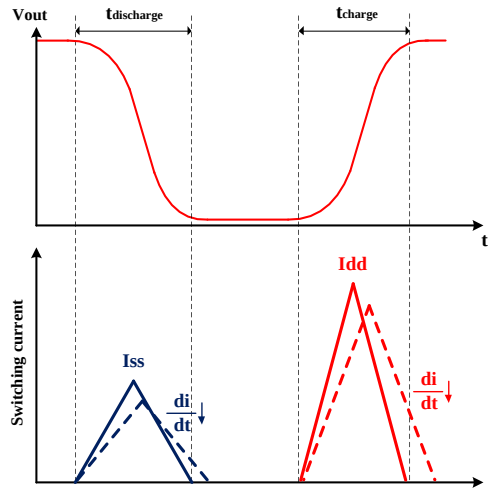

Figure II-21: Transient current peak in an inverter when charge/discharge the load (solid line) and after aging, due to the degradation of transistor parameters, the current peak decrease and the charge and discharge time increase (dotted line).

After aging, due to the degradation mechanism, the transistor parameters could be degraded, such as drain current and mobility decrease, threshold voltage increases. Take a simple CMOS inverter as an example. The switching noise defined in Equation I-2 relates to the current peak and the gate charge/discharge time. The current peak depends on the saturation of PMOS and NMOS which

are reduced after aging (section I-2.6) (Figure II-21). The gate charge/discharging time can be expressed by Equation II-12

$$t_{discharge} = C_L \frac{V_{out}}{I_D} = C_L\left(\int_{V_{dd}-V_{THn}}^{V_{dd}} \frac{dV_{out}}{I_{DSATn}} + \int_{0}^{V_{dd}-V_{THn}} \frac{dV_{out}}{I_{DLINn}}\right) \qquad \text{Equation II-12}$$

$$t_{charge} = C_L \frac{V_{out}}{I_D} = C_L\left(\int_{0}^{V_{THp}} \frac{dV_{out}}{I_{DSATp}} + \int_{V_{THp}}^{V_{dd}} \frac{dV_{out}}{I_{DLINp}}\right)$$

Where C_L is load capacitance, composed by internal MOSFET contributions and external load. In the I/O case, the load capacitance is dominated by the external ceramic capacitive load equal to 100pF. The C_L variation due to aging can be ignored because ageing at board level is negligible. However, due to increasing of absolute value of threshold voltage and decreasing of carrier mobility, the drain currents in saturation and linear region are reduced after aging. Thereby, the discharge/charge times rise. The decreasing slope of peak current variation would reduce the ΔI noise, thus the switching noise and conducted emission.

If we take an example of simulation of saw tooth signal, as depicted in Figure II-22, the smaller peaks represent the ground discharging current peak while the higher peaks represent the power charging current. After computing by Fast Fourier Transform (FFT), the time domain signal is converted into frequency domain spectrum.

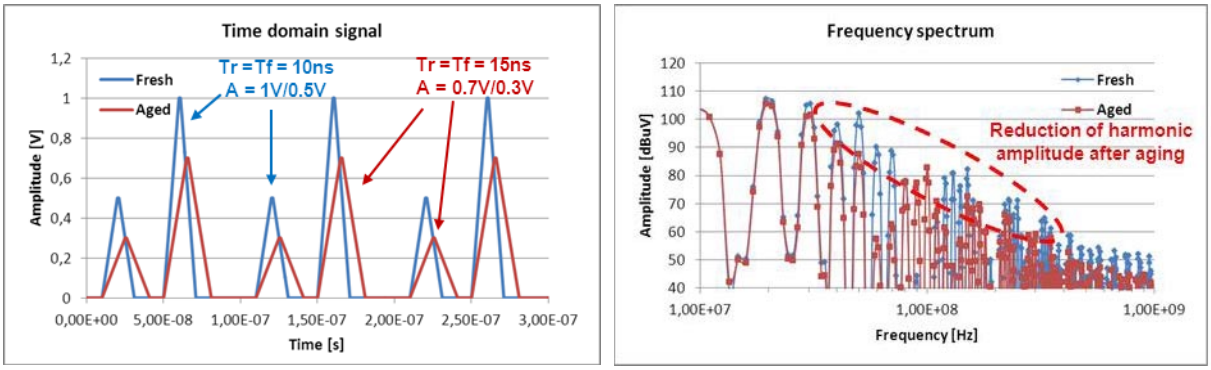

Figure II-22: Simulation of inverter power rail noise by a saw tooth signal: (left) the comparison of fresh and aged inverter's noise in time domain and (right) the comparison in frequency spectrum after computing with FFT.

From the simulation, after aging, in time domain, the charging and discharging current decrease due to the drain current degradation. Simultaneously the width of the saw tooth wave increases since the charge/discharge time rise. With the conversion of FFT, since the amplitude axis is in dB scale, the amplitude variations of the first harmonics are not obvious. The decreases of harmonics in high frequency range after aging mainly due to the variation of temporal waveform (rise time and fall time). Thus, the degradation mechanism such as HCI active by LTOL, TDDB/NBTI induced by HTOL could degrade the transistor parameters, making the reduction of drain current and CMOS logical gate slow down, especially changing the waveform temporal profile. Finally, weaken the IC conducted emission problem.

2.1.7. Some interesting points in future research

2.1.7.1. *Increased emission level in some frequency points after aging*

During the analysis of the emission evolution after different types of aging, we found there are some frequency points where the emission level increases after aging (Figure II -14 and Figure II -19). Additionally, as shown in Figure II-23, the envelop analysis only considers the highest harmonics produced by 10MHz active IN3. The decreasing of emission level after ageing mainly happened in this area. The harmonics generated by 3MHz active IN1 and the intermodulation harmonics (3MHz with 10MHz) always have lower amplitude and far away below the envelope. However, in some frequency points, they could rise after aging. These increasing of emission level could not be explained by the conclusion in the previous section. Future research could test the I/O blocks with low driving current ability.

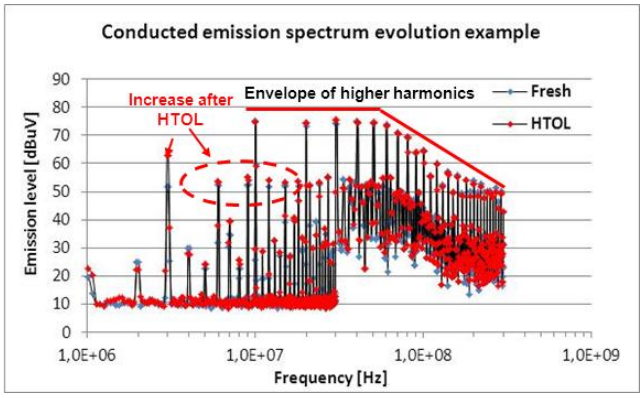

Figure II-23: The comparison of 1 Ω conducted emission spectrum for fresh DUT and DUT after 408 hours HTOL aging with 3MHz on input signal IN1 and 10MHz on IN3.

2.1.7.2. *Dispersion increasing*

The comparison of samples measurement results dispersion in Figure II-15 and Figure II-20 shows that dispersion due to process variation and measurement error would enlarge more or less after LTOL and HTOL, excluding the measurement errors which do not have obvious difference before and after aging. The enlargement of sample dispersion is mainly due to the non-uniform responses to aging stress. The extreme example is observed after aging, where some components can completely lose their functions. Further research could apply the Monte Carlo simulation to take into account of transistor parameter process variation.

2.1.7.3. *New method to distinguish the fresh and aged component*

As the emission levels would decrease after device ageing, the emission measurement can provide a way to differentiate between the fresh component and aged component. With the knowledge of the average characteristics (conducted emission or radiated emission) of the component, it would be possible to determine the probability of circuit status (fresh or aged).

3. CHARACTERIZATION OF AGING IMPACT ON IMMUNITY: CASE STUDY

3.1. Case study 1: input/output in CMOS 65nm

3.1.1. Device under test and test set-up description

In the immunity study case 1, the same test chips are reused for comparing the evolution immunity with aging. Figure II-24 depicts the immunity test set-up using direct power injection (DPI) method that is introduced in section 1.2.2 and defined by International Electrotechnical Commission as IEC 62132 – 4 [IEC62132-4].

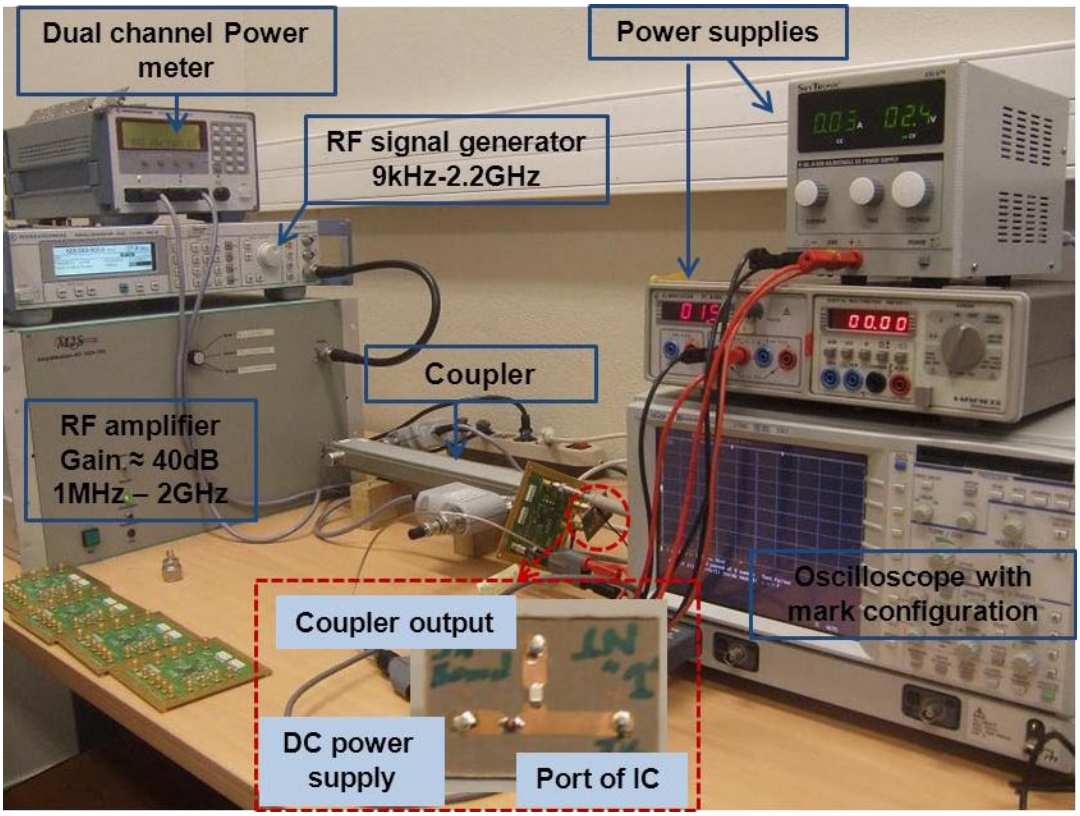

Figure II-24: Direct power injection test for ST 65nm test chip set-up

The RF disturbance is firstly generated by RF generator and amplified by a RF power amplifier. The conducted disturbance is coupled on DUT pins by a directional coupler and a bias-tee. The directional coupler and the dual channel power meters are used to measure the forward power injected into the DUT and the reflected power which come back from DUT to the source. The RF disturbance signal is usually superimposed to a low frequency signal as a digital signal or a power supply, through a bias-tee which is made of two parts:

- A DC block capacitor which aims at avoiding applying a DC voltage across the RF amplifier output.
- A choke inductance, to prevent from getting RF power to the DC power supply by placing a large impedance (more than 400Ω is recommended by IEC 62132 – 4 standard).

Generally, the bias-tee should be located closer to the DUT on the test PCB test board. Since the immunity level strongly depends on the transmission characteristics of bias-tee, to avoid aging effect on the bias-tee parameters, the bias tee is designed on a daughter board.

During the susceptibility tests, the DUT operation is monitored by a digital storage oscilloscope. As described in DPI algorithm in Figure II-4, for each disturbance frequency, the power of injection signal increases step by step until circuit failures arise. Here, a failure is detected each time. The output signal exceeds a specified mask defined in oscilloscope. All the test apparatus are controlled by central PC via GPIB cables.

Two types of injection are carried to study the aging effects on conducted immunity of power supply and digital input pin of the circuit, as depicted in Figure II-25:

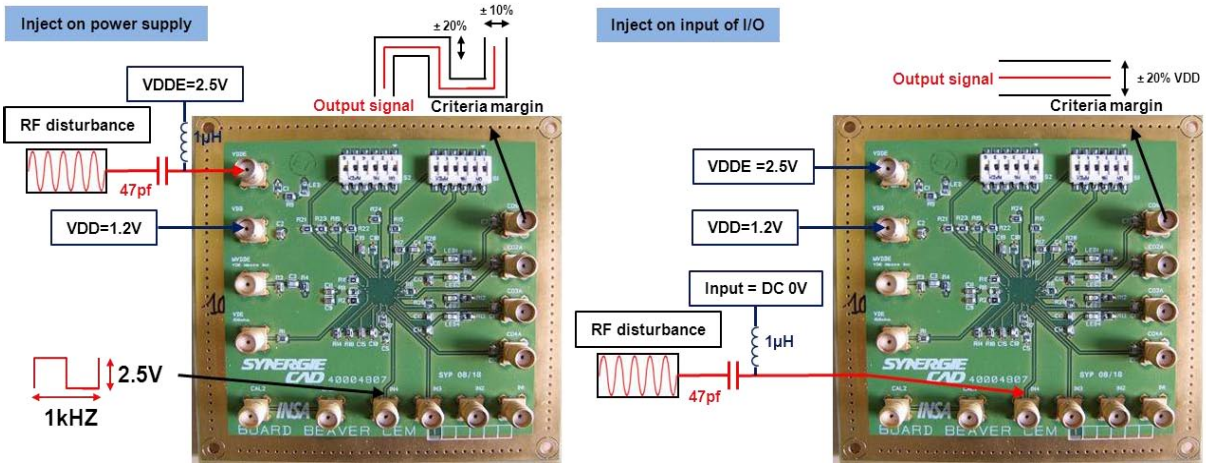

Figure II-25: Schematic of the configuration DUT for direct power injection test: conducted injection on power supply of DUT (left) and on input of DUT (right)

- Conducted injection on power supply: a sinusoidal signal which is superimposed on the DC power supply and injected on the VDDE pin. A 1 kHz with 2.5V peak to peak amplitude square signal is applied on IN1 and the output signal called CO1A is monitored by a pattern-generating oscilloscope. The failure criteria contain a static margin (±20% of power supply, thus ±0.5V) and a delay margin or dynamic margin (±10% of input period, thus ±0.1ms). The test frequency range is from 10MHz to 1GHz, and the maximum inject forward power is set to 40dB (10W).
- Conducted injection on a digital input: a sinusoidal signal which is superimposed on a digital signal and applied on the IN2 pin. The logical level of the input pin is arbitrarily set to 0. Only this logical state will be studied. The failure is monitored by creating a mask of criteria around

the output signal (nominal voltage is 0V) with static margin (±20% of power supply, thus ±0.5V).

As the conducted emission test, HTOL and LTOL accelerated aging tests are applied to the DUTs. The number of samples and the configuration during the ageing test are the same than the conducted emission tests. (Refer to Table II-4)

3.1.2. Evolution of the conducted immunity of the power supply pin after aging

3.1.2.1. Repeatability

The repeatability characterization of DPI test applied on power supply pin (VDDE) has been done by measuring 10 times the conducted susceptibility of the same component. The repeatability errors defined by Equation II-6 for each frequency before and after aging test are shown in Figure II-26.

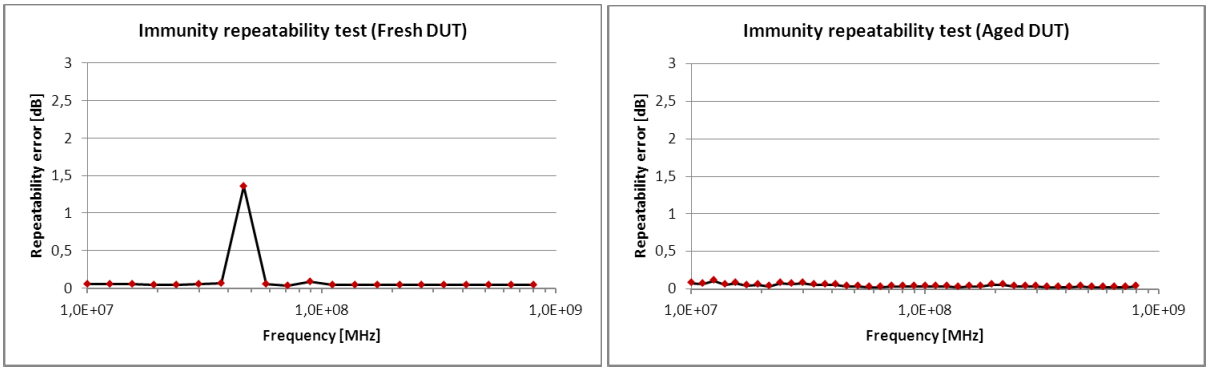

Figure II-26: DPI on power supply measurement repeatability error for each frequency point before (left) and after aging (right).

The repeatability error is expressed by sampling standard deviation (SSD). For the test before aging (Figure II-26-left), except at 46MHz shows a significant dispersion of 1.36dB, all the other frequency points offers a good repeatability. The mean value of SSD over the whole range is 0.11dB, thus the mean repeatability measurement uncertainty over all frequency range is ±0.22dB.

The same repeatability procedure is done after aging (Figure II-26-right), over all frequency range, the repeatability errors are quite flat. The average of repeatability error over all frequency range is 0.05dB, thus the mean repeatability measurement uncertainty over all frequency range is ±0.1dB.

3.1.2.2. Experiment results before and after aging

We compare the immunity level before and after different types ageing. The 1st – 5th samples are dedicated to LTOL aging and the 6th – 10th are dedicated to HTOL. Figure II-27 shows two examples of the most obvious variation among the samples for LTOL and HTOL.

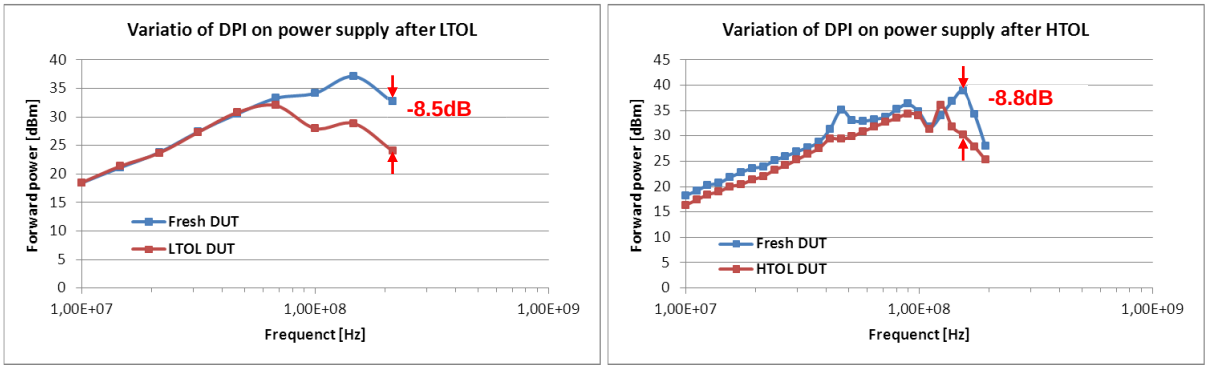

Figure II-27: Evolution of conducted immunity of power supply pin after aging: 1st sample after LTOL aging (left) and 8th sample after HTOL aging (right).

In these two examples, for both LTOL and HTOL test, the immunity levels tend to decrease after aging. After LTOL, within the 10MHz to 70MHz range, the immunity level keeps unchanged after aging. From 70MHz to 200MHz, immunity level degrades and the reduction can reach 8.5dB at 200MHz. For HTOL effect, in the range of 10MHz to 100MHz, immunity level has slight degradation around 1.3dB. The maximum degradation appears at 155MHz and could reaches -8.8dB.

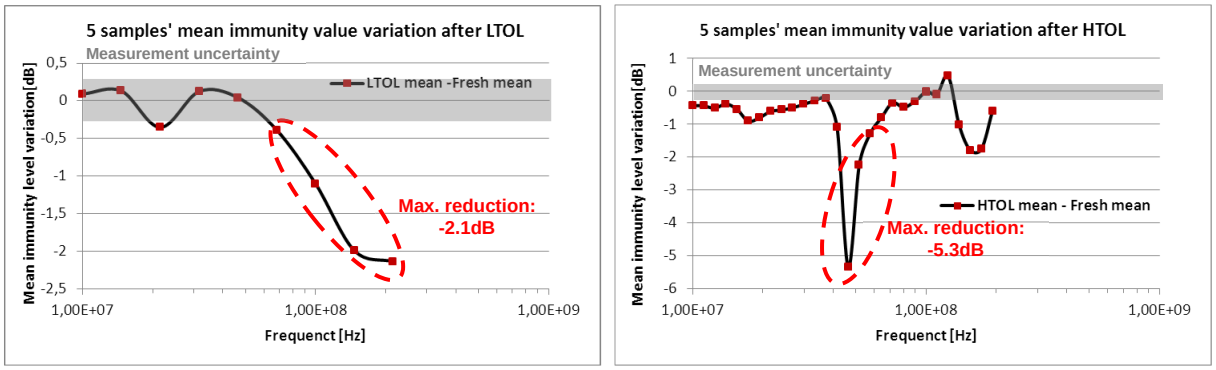

Figure II-28: Mean variation of conducted immunity level of power supply pin VDDE for all 5 samples at each frequency after ageing: 1st – 5th sample comparison after LTOL (left) and 6th – 10th samples comparison after HTOL (right).

For statistical analysis, the mean variations of conducted immunity for all samples are compared at each injection frequency point (we calculate the mean value for each column of the aging drift matrix, (Equation II-7) before and after different aging, as shown in Figure II-28. After LTOL, the mean immunity level measured on five samples is significantly reduced above 70MHz. The mean decreasing reaches up to -2.1dB. The HTOL aging makes more serious degradation than LTOL. The maximum mean reduction takes place at 46MHz and reaches up to -5.3dB. From 140MHz to 200MHz, the immunity level also decreases around 1.8dB.

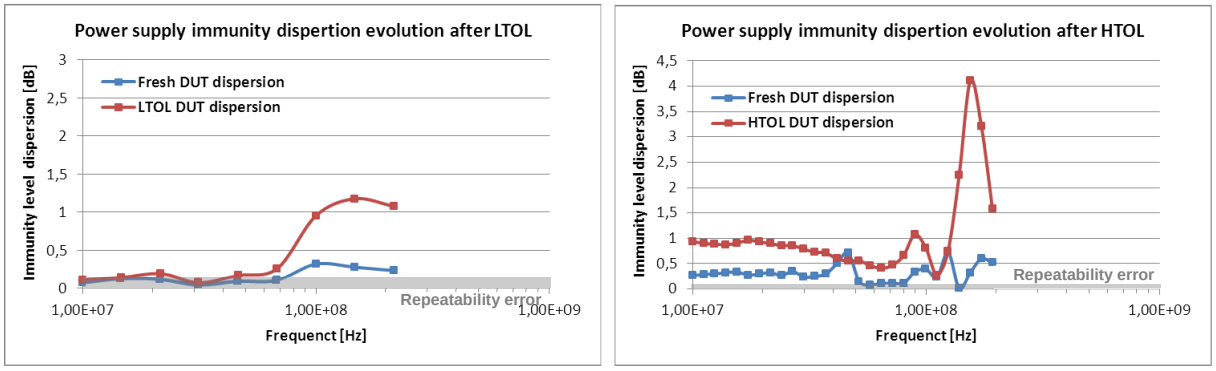

Figure II-29: DPI on power supply measurement evolution after aging: 1st sample after LTOL aging (left) and 8th sample after HTOL aging (right).

As conducted emission test, some dispersion between measurement results on different samples is observed, for both fresh and aged DUTs. The sample standard deviations (SSD) defined in Equation II-10 is computed to quantify the dispersion among samples (Figure II-29). After LTOL, the dispersion measured on five samples expands significantly from 70MHz to 200MHz and the maximum increase is 0.9dB at 147 MHz. For HTOL, the variation of dispersion before and after aging is more obvious. Between 10MHz and 110MHz, the dispersion increase is around 0.6dB and the maximum enlargement is 3.8dB at 155MHz.

3.1.3. Evolution of the conducted immunity of the digital input pin after aging

3.1.3.1. Repeatability

DPI on input (IN1) repeatability characterization has done by measuring 10 times the same component. The repeatability errors defined by Equation II-6 for each frequency before and after aging test are shown in Figure II-30.

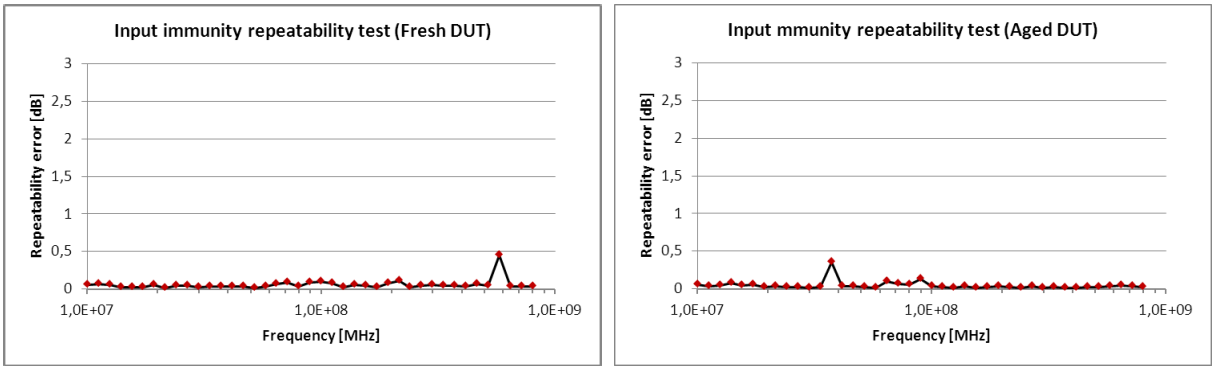

Figure II-30: DPI on input measurement repeatability error for each frequency point before (left) and after aging (right).

The repeatability error is expressed in term of sampling standard deviation (SSD). For test before ageing (Figure II-30-left), except at 576MHz, a good repeatability is ensured. The mean value of SSD over the whole range is 0.06dB, thus the mean repeatability measurement uncertainty over all frequency range is ±0.12dB.

The same repeatability characterization procedure is performed after ageing (Figure II-30-right). Except at 37MHz, the repeatability errors are negligible. The average of repeatability error over all frequency range is 0.04dB, thus the mean repeatability measurement uncertainty over all frequency range is ±0.08dB.

3.1.3.2. Experimental results for fresh DUT

The interference-induced defaults that we used in power supply immunity test relate to the output static and dynamic margin. However, during the input immunity test, we found that at some frequency points, with injection disturbance on input port, the power supply current can exceed tens mA where the normal current consumption is 0.5mA. With the consideration to prevent thermal damage of the DUT, we added a new susceptibility criterion on the power supply current consumption. Figure II-31 compares the typical output margin criteria and the combination with current consumption criteria immunity level measurement results of the same sample.

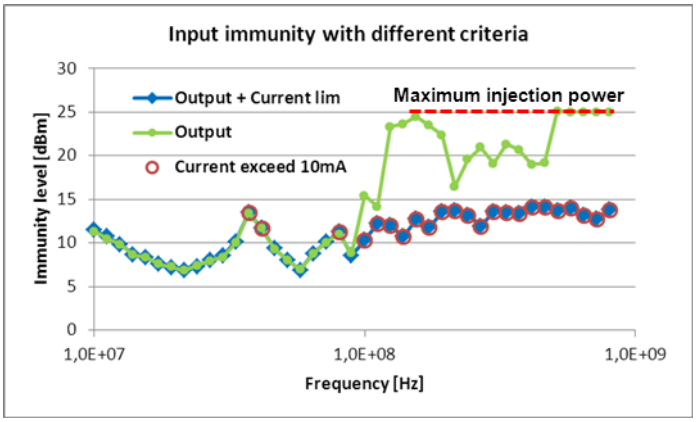

Figure II-31: Input immunity level with different failure criteria: (Green line) typical failure criteria with the output static and dynamic margin. (Blue line) improved failure criteria with combination of output margin and current limitation of 10mA. (Red circles) are the points where the current consumption reaches to10mA.

3.1.3.3. Experiment results before and after aging

We compare the immunity level of the digital input, when the logical input state is pulled down, before and after different types aging. The 1st – 5th samples are dedicated to LTOL aging and the 6th – 10th are dedicated to HTOL. Figure II-32 shows two examples of the most obvious variation among the samples for LTOL and HTOL.

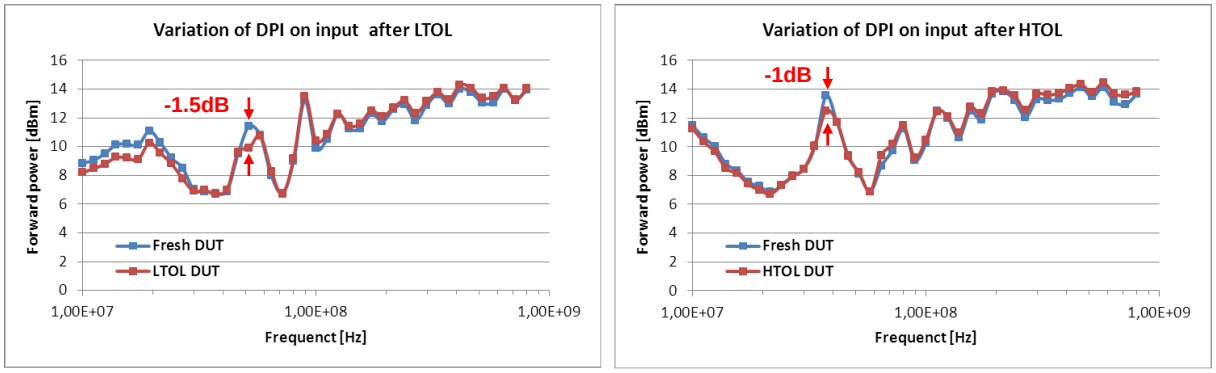

Figure II-32: DPI on power supply measurement evolution after aging: 1st sample after LTOL aging (left) and 10th sample after HTOL aging (right).

In these two examples, for both LTOL and HTOL tests, the immunity levels of the digital input pin do not change as well as the immunity level of power supply pin. After LTOL, in 10MHz to 50MHz range, the immunity level slightly decreases and has a maximum reduction of 1.5dB at 50MHz. Above 50MHz, the immunity level rises a little rather than decreases. For HTOL effect, between 10MHz and 40MHz, the immunity level has a slight reduction about 1dB. The maximum reduction appears at 37MHz and reaches -1dB.

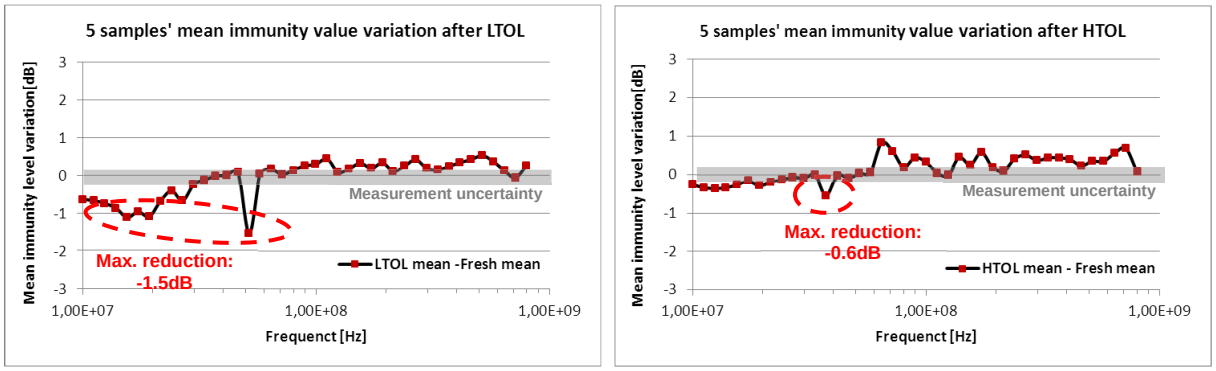

Figure II-33: Mean input immunity level for all 5 samples at each frequency after aging: 1st – 5th sample comparison after LTOL (left) and 6th – 10th samples comparison after HTOL (right).

For statistical analysis, the mean input immunity values variation for all samples are compared at each injection frequency point (we calculate the mean value for each column of the aging drift matrix, see Equation II-7) before and after different aging, as shown in Figure II-33. For the immunity variation after LTOL, the reductions mainly appear between 10MHz to 50MHz with maximum mean reduction -1.5dB at 50MHz. While above 50MHz, immunity level tends to slightly increase around 0.5dB. The HTOL aging makes less immunity variation than LTOL. The maximum mean reduction takes place at 37MHz and attain to -0.5dB. Above 50MHz, the immunity level of the digital input pin rises after aging.

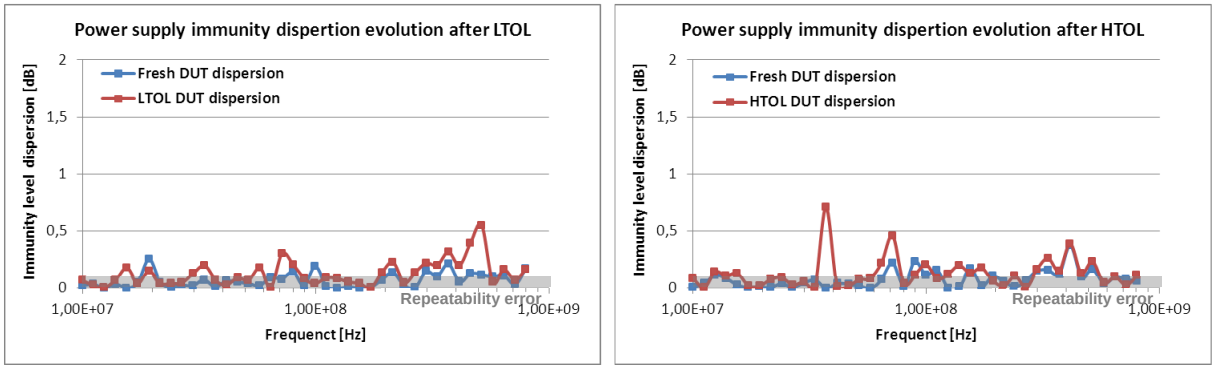

Figure II-34: DPI on power supply measurement evolution after aging: 1st sample after LTOL aging (left) and 8th sample after HTOL aging (right).

The dispersion of measurement results among samples for both fresh DUTs and aged DUTs is computed in term of sample standard deviations (SSD) defined in Equation II-10 (Figure II-34). The evolution of dispersion is not very significant after ageing tests (HTOL or LTOL).

3.1.4. Immunity ST 65nm conclusion

From the previous results, we can conclude that:

- From results shown in Figure II-28, the conducted immunity of power supply pin decreases in most of frequency points after different ageing, the degradation after HTOL is more important than LTOL. However, for the conducted immunity of the digital input, as shown in Figure II-33, the degradation is not significant. For LTOL and HTOL slight reductions of immunity levels appear in the low frequency range, while the immunity level tends to rise after both types of aging above 50MHz.
- Dispersions among samples rise after aging for both two types of accelerated ageing test. The variation for power supply immunity is more important than digital input.
- The influence of ageing on conducted immunity is more important for the power supply pin than for the digital input immunity.

The observed immunity level evolution after ageing allows us to conclude about the conducted immunity issues of this component induced by conducted interference from a larger system level. From statistical point of view, we can assume that the immunity level measured at a given disturbance harmonic frequency for a given component behaves as a random variation that follows a normal distribution (as depicted in Figure II-35). The mean value of immunity levels decreases after aging and drives the distribution bell curve towards the immunity lowest limit fixed to ensure the component EMC. The risk of non-compliance of the circuit to the immunity level is equal to the probability that a sample has an immunity level less than the immunity limit. It can be computed by integrating the area under the distribution curve below the immunity limit. Furthermore the standard deviation of the distribution enlarges after aging which could make the degradation worsen, the risk of non-

compliance to immunity limit increases after different ageing. Thus the susceptibility of this component to the external conducted noise tends to worsen after ageing.

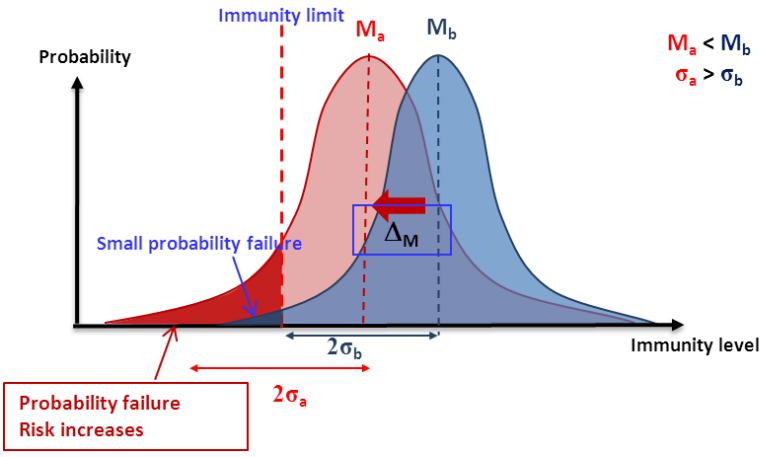

Figure II-35: Conducted immunity level statistical distribution moving towards the immunity limitation. The probability failure risk increases after ageing

3.2. Case study 2: mixed signal circuit in CMOS 0.25µm (MIXITY)

3.2.1. Device under test and test set-up description

To study the influence of aging on different blocks of IC, we developed a test chip with various structures to measure the propagation of external RFI along the power supply rails and evaluate the influence of immunity level by HTOL. In this second case study, the EMR characterization is applied to a mixed signal test chip in 0.25 µm SMARTMOS 8 technology from Freescale Semiconductor (Toulouse – France), dedicated for automotive applications. The die is packaged in 64 pin QFP (Quad Flat Package) and mounted on a specific 150mm x 150mm 4 layers board (according to IEC 62132 standard) through a RF socket dedicated to susceptibility tests (See Figure II-36). Table II-5 describes the different blocks included in the DUT. The test chip includes three digital cores, a digital I/O and a 25 MHz phase locked loop (PLL).

Block	Power supply pin names	Description
Digital core	V_{dd_core} = 2.5V	▪ Core0 : normal clock tree ▪ Core1 : Core0 + additional on-chip capacitor ▪ Core2 : Core0 + substrate isolation
Digital I/O buffer	$V_{dd\_I/O}$ = 2.5V	A chain of an input and output buffer supplied under 5V
Phase locked loop (PLL)	V_{dd} (Ph) = 2.5V V_{dd} (VCO) = 2.5V V_{dd} (Div) = 2.5V	A PLL block subdivided in three sub-blocs with separated power suppliers: ▪ Phase comparator (Ph) ▪ Voltage controlled oscillator (VCO)

		▪ Frequency divider (Div)

Table II-5: Description of the blocks included in MIXITY

The DPI test set-up illustrated in Figure II-3 is reused in the MIXITY project. The test frequency ranges are from 10MHz to 1GHz with a maximum injection power limited to 45dBmW. The failure criteria are defined for the different blocks of the test chip:

- Conducted injection on I/O power supply pin: The failure criteria defined by a static margin (±10% of power supply, thus ±0.25V) and a delay margin or dynamic margin (±10% of input period). The current consumption limitation is set to 25mA.
- Conducted injection on cores power supply pin: static margin is ±10% of power supply amplitude and a delay margin is ±10% of clock period. The current consumption limitation is set to 25mA.
- Conducted injection on PLL power supply pin: for this analog circuit we use a smaller static margin of ±10% of power supply amplitude (thus ±0.25V around 2.5V) and a delay margin of 10% of the reference signal period (thus for an input reference signal with a frequency equal to 25MHz, the margin is set to ±4ns). The current consumption limitation is set to 100mA.

10 samples were tested before and after HTOL aging to evaluate their immunity variation due to aging. As we explained in section of II - 2.1.3, the test chips were operated under the 150°C ± 2.5°C in a climatic chamber and were applied 110% of the nominal power supply by external sources, the test lasted 408 hours (about 3 weeks). The experimental set-up used three boards, shown in Figure II-36:

- EMC test board: the circuit is mounted on the test board with a RF socket to measure the immunity level before and after accelerated aging. This board did not use during the aging test, to prevent from board degradation.
- Aging board: this board is used during the aging test in the climatic chamber, with sockets dedicated to high temperature burn-in test.
- Monitoring board: this board is placed outside the climatic chamber, in order to supply and monitor the DUT during the accelerated aging.

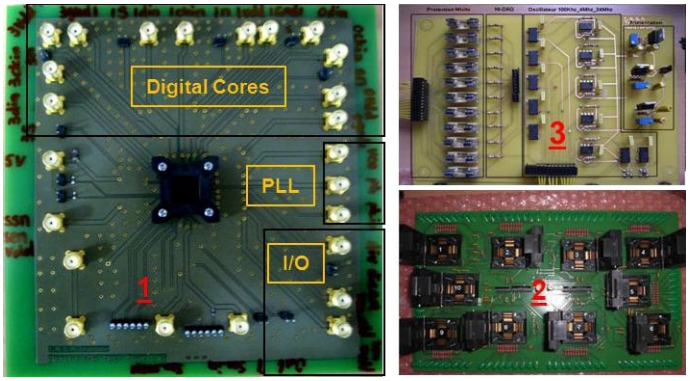

Figure II-36: Three boards used to characterize MIXITY EMR: (1) EMC measurement board with RF dedicated socket; (2) Burn in test board with high temperature adapted socket; (3) aging monitoring board, monitor the functionality of the test blocks and provide power supply to DUT.

3.2.2. Experimental results analysis

3.2.2.1. *Repeatability*

The repeatability test is tested firstly to quantify the measurement uncertainty and repeatability error. The validation of the test bench was done by measuring the immunity level 10 times on the same sample for the three different blocks.

	Core	I/O	PLL
Mean repeatability error	0.57dB	0.46dB	0.27dB
Measurement uncertainty	±1.14dB	±0.92dB	±0.54dB

Table II-6: Repeatability of the blocks included in MIXITY

The mean value of the sample standard deviation for all frequency points and the mean measurement uncertainly over all frequency range are calculated and listed in Table II-6.

3.2.2.2. *Experiment results before and after aging*

Table II-7 summarizes the experimental results for the five different blocks, the statistical analysis are applied on measurement results. As explain in section II -1.5, various parameters are computed for the 10 samples:

- Maximum drift D_{max}: the maximum drift among ten samples which is indicated by Sx (Sample number) and frequency.
- Maximum mean drift *Max (*ΔMj*)*: the mean value of drift ΔMj is calculated by computing the average drift of ten samples for each frequency point. Among the tens samples, the maximum mean drift *Max (*ΔMj*)* is extracted by indicating the frequency.
- The average drift for all frequency range ΔM: The average of the mean drift ΔMj among all frequency points
- Standard deviation of mean drift $\sigma_{\Delta Mj}$: the standard deviation of a set of mean drift ΔMj for all frequency points.

	Dmax [dB]	Max (ΔMj) [dB]	ΔM [dB]	$\sigma_{\Delta Mj}$ [dB]
Core0	-17.8 S10 @ 200MHz	-7.66 @ 200MHz	0.1	1.35
Core1	-7.02 S4 @ 224MHz	-2.36 @ 63 MHz	-0.35	1.45

Core2	-15.73 S1 @ 282MHz	-4.67 @ 112MHz	0.49	2.04
IO	-18.85 S9 @ 200MHz	-7.85 @ 112MHz	0.51	1.21
PLL	-15.88 S8 @ 158MHz	-4.21 @ 282MHz	-2.57	3.64

Table II-7: Immunity drifts statistical analysis for different blocks

After 408 hours HTOL accelerate test, all the blocks of 10 samples are still functional, no particular degradation or failure can be noticed on the output signal under nominal operation condition. However there are remarkable changes in immunity level for each block. The maximum negative variations in the ten samples for different blocks are listed in the second column of Table II-7. The maximum immunity degradation could exceed -18 dB. After calculating the mean drift (ΔMj) of the ten samples at each frequency (j), the statistical calculation of (ΔMj) for all frequency points are listed on the three last columns. The average of ΔMj shows the variation of immunity level over all frequency range. The PLL shows the worst degradation. Moreover the standard variation σΔMj indicates that PLL immunity drift spreads out over a largest range of variation to the ΔMj.

Figure II – 37 is an example of immunity level when the RF disturbance is injected on the VCO power supply of the 6th sample. Between the 10MHz and 280MHz, the immunity level decreases around -5dB and the maximum reduction is -10.3dB at 160MHz.

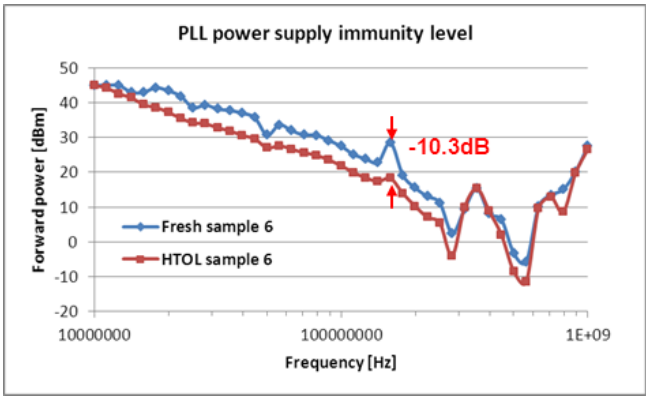

Figure II-37: PLL power supply immunity level variation after HTOL of sample 6.

The dispersion of measurement results among samples for both fresh DUTs and aged DUTs are characterized by sample standard deviations ($\Delta\sigma_j^a$) on each frequency point. The average of $\Delta\sigma_j^a$ for all frequency points are computed and listed in Table II-8.

	Mean dispersion for all frequency points before ageing[dB]	Mean dispersion for all frequency points after ageing[dB]

Core0	0.69	1.07
Core1	0.9	1.0
Core2	1.23	1.34
IO	0.89	0.73
PLL	1.64	4.83

Table II-8: Measurement dispersion among samples before and after aging

The comparison of measurement dispersion before and after aging shows that the after aging, except I/O blocs presents a slight reduction, the dispersion of all the other blocks increases after aging, especially for PLL.

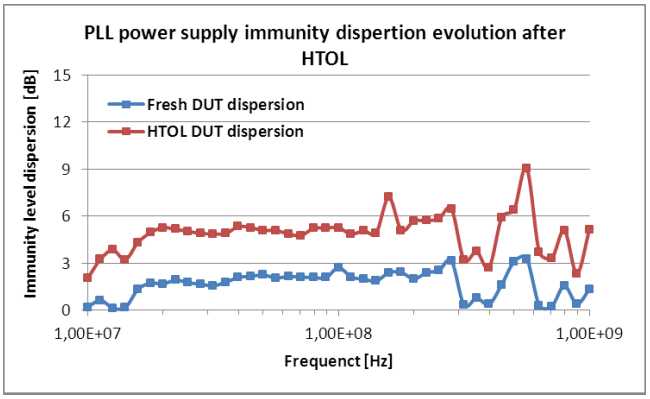

Figure II-38: PLL power supply immunity level dispersion before and after HTOL test

Figure II-38 compares the enlargement of dispersion of the conducted immunity measurement of Vdd (VCO) pin, computed from 10 samples. Over the whole frequency range, the dispersion of measurement increases after HTOL.

3.2.3. Analysis of the statistical distribution of the immunity level measurements as a normal distribution

In the previous parts, the measured emission and susceptibility levels appear as random variables. They cannot be characterized accurately due to measurement errors. Besides, an EMC measurement done on one sample among a lot of identical components does not guarantee that we know the EMC levels of the other components, because of process dispersion and ageing process effects.

We have assumed that the EMC levels (emission or susceptibility) of a circuit follow a normal distribution. We propose in this part to verify this assumption experimentally. The extraction of the statistical distribution of a random process requires a large collection of measurements that we cannot afford since we have only a maximum of ten samples. Even if we will not ensure a high confidence in

the statistical distribution extracted from the EMC level measurements, it can help us to consolidate the assumption of a normal distribution.

Before analyzing the MIXITY measurement results, let us recall a little theory about normal distribution. Let consider a set of variables that identically cluster around a single mean value μ. The distribution of these variables tends toward a normal distribution with a probability density function (PDF) defined by (Equation II-13)

$$f(x) = \frac{1}{\sqrt{2\pi\sigma^2}} e^{-\frac{(x-\mu)^2}{2\sigma^2}}$$ Equation II-13

Where μ is the mean and the σ is the standard deviation.

Figure II-39 presents several examples of normal distribution for three sets of variable: set1 (μ = 2.5, σ = 0.5), set2 (μ = 2.2, σ = 0.8) and set2 (μ = 2.5, σ = 0.8). The probability density function is plotted in two different ways: the x axis is either linear or logarithmic (expressed in dB). This last representation is important since our measurements are often plotted in logarithmic scale. In a logarithmic scale, the distribution loses its symmetry around the mean value.

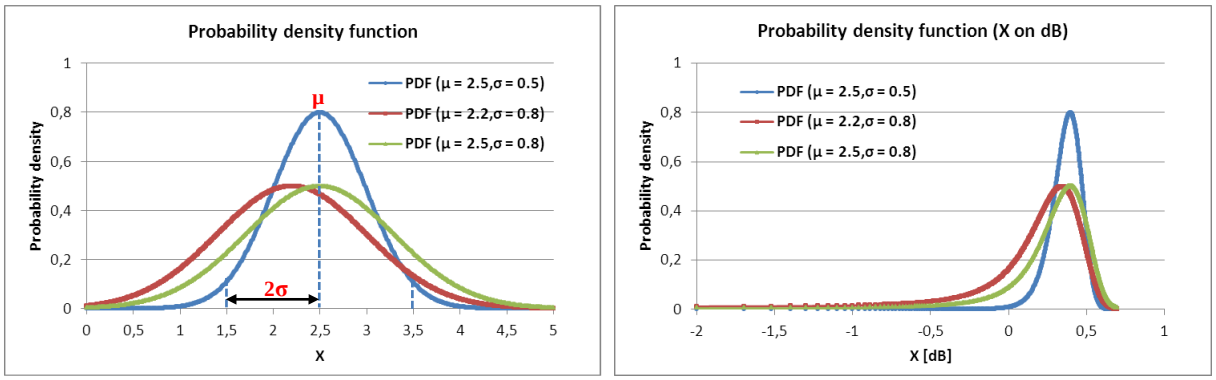

Figure II-39: Example of probability density function for three sets of variables: (left) x is in linear and (right): x is converted into dB

There is another way to characterize the normal distribution as cumulative distribution function (CDF) which describes the probabilities for a random variable to fall in the intervals of the form (-∞, a] Equation II-14). It is the integral of probability function over the range (-∞,a]

$$\varphi(x) = \int_{-\infty}^{a} f(x)dx = \int_{-\infty}^{a} \frac{1}{\sqrt{2\pi\sigma^2}} e^{-\frac{(x-\mu)^2}{2\sigma^2}} dx$$ Equation II-14

Where μ is the mean (location of the peak) and the σ is the standard deviation, *a* is the interval limitation. Figure II-40 plots the cumulative distribution function of the three sets of data used in Figure II-39. The vertical axis is the probability to obtain X<=a. The cumulative density function is plotted in two different ways: the x axis is either linear or logarithmic (expressed in dB). In a logarithmic scale, the distribution loses its symmetry around the mean value.

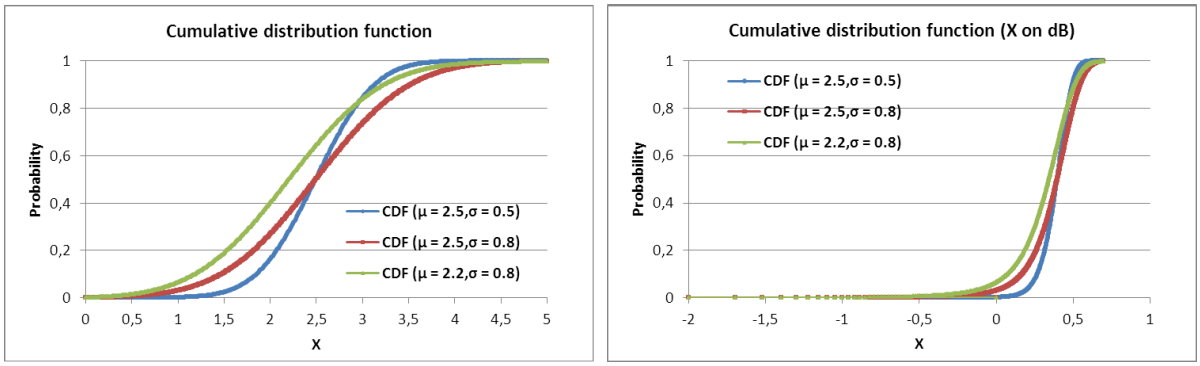

Figure II-40: Example of cumulative distribution function for three sets of variation: (left) x is in linear and (right): x is converted to dB

If we consider the conducted immunity measurement leaded on of MIXITY PLL power supply pin at 100MHz before and after HTOL test, as shown in (Figure II-41-left), the mean values of 10 samples are 28.6dBm before HTOL and 24.5dBm after HTOL where the mean decreases about 4.1dB. The standard deviations are 2.7 dB before HTOL and 5.3dB after HTOL. Each plotted point is the susceptibility threshold of one sample at 100MHz before or after ageing. The ten samples are distributed around a mean value. From this plot, it is quite difficult to identify the type of distribution. But the type of distribution can become much clearer if the CDF is plotted (Figure II-41-right). Quantitative conclusions about the distribution remain hazardous, but qualitatively, the CDF measured before and after ageing is similar to the CDF of a normal distribution. This comparison gives similar result for all the other frequency and both EMC tests.

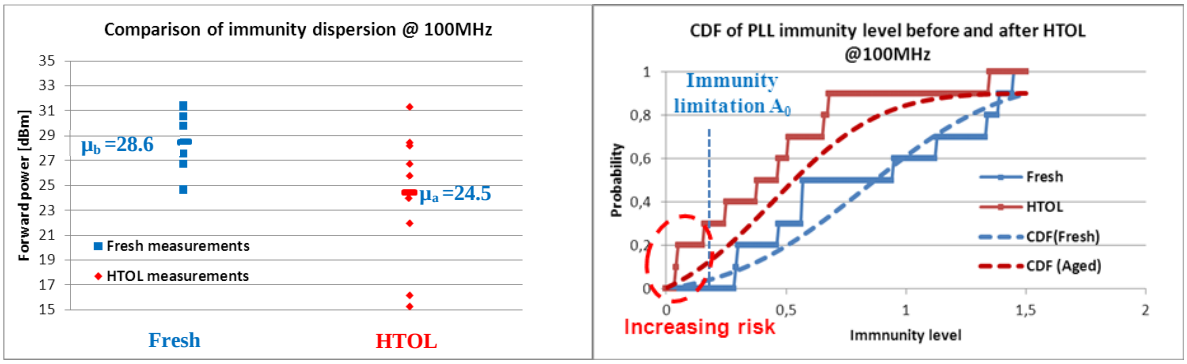

Figure II-41: Comparison of MIXITY PLL power supply immunity levels of ten components at 100MHz before and after ageing (left) and transfer to cumulative distribution functions of the immunity level of the ten components before and after ageing (right).

From the (Figure II-41-right), the CDF of power supply immunity level shifts towards left after HTOL which could cause the increase of failure risk the RF disturbance. The difference between the CDF with aged components and the measurement of ten samples is mainly due to the limitation of the samples size. This can lead to overestimated of risk increase. If the nominal immunity level is set to A0, according to the Equation II-14 the increasing risk R($x<A_0$) of failure due to evolution of immunity level after HTOL would be (Equation II-15)

$$R(x < A_0) = \varphi(x_a) - \varphi(x_b) = \int_{-\infty}^{A_0} [f(x_a) - f(x_b)]dx \qquad \text{Equation II-15}$$

The calculation could be done by standardizing the normal distribution of immunity level set (X) with the mean value μ_x and the standard deviation σ_x to the standard normal distribution set (Z) which $\mu = 0$ and $\sigma = 1$. (Equation II-16):

$$Z = \frac{X - \mu_x}{\sigma_x} \qquad \text{Equation II-16}$$

Thus the immunity limitation (above limit of the integration in Equation II-15) is replaced by standard normal distribution (A'_0) that can be calculate as $A'_0 = (A_0 - \mu_x)/ \sigma_x$. The probability can be obtained by checking standard normal distribution CDF value table.

3.2.4. Conclusion about the conducted immunity tests leaded on MIXITY power supply pin

After HTOL aging test, the functions of all the blocks of the tested samples are preserved. The variation of current consumption and output signal integrity are kept in acceptable range, proving the excellent robustness of the Freescale SMARTMOS 8 technology. However, some significant changes in immunity levels have been observed for some blocks on a large number of components. Accelerated aging tests tend to decrease the immunity level of analog blocks such as VCO in PLL, while the digital blocks seem to be more robust. The process dispersion after aging rises for most of the blocks except for I/O which has slightly decreasing. It demonstrates that the process variation becomes more important as the non-uniform process could involve different evolution of degradation mechanisms during the operation.

4. CONCLUSION AND RESEARCH PERSPECTIVES

In this chapter, we studied the evolution of EMC level which includes conducted emission level and conducted immunity level after Low temperature (LTOL) and High temperature (HTOL) accelerated ageing through several case studies.

Conducted electromagnetic emission test performed on input/output buffers designed in ST 65nm technology shows that both ground current noise emission (measured with 1Ω method) and power rail emission (measured with 150 Ω method) decrease after LTOL and HTOL. The emission problem would be relaxed after aging. It can be explained by the reduction of drain saturation/linear current and the increase of charge/discharge time of switching blocks due to the intrinsic degradation mechanisms accelerated by ageing test.

The comparison of conducted immunity level of power supply and digital input pins in the ST 65nm case study shows that the effects of aging on power supply pin immunity are more important than input pin immunity. The conducted immunity level of power supply pin decreases over a large frequency range after HTOL and LTOL, while the variation of input pin immunity after different

aging is negligible. In parallel, the measurement of immunity level dispersion among all the test samples is enlarged after different aging which intensify the variation of immunity level.

In the MIXITY case study, we focus on the evolution of the conducted immunity of power supply pin for different blocks after high temperature (HTOL). The comparison of digital blocks and analog block in MIXITY test chip shows that the analog blocks are more vulnerable to ageing.

Finally, the different case studies demonstrate that IC ageing has an impact on electromagnetic emission and immunity to RFI. The emission relaxation and immunity aggravation, especially the degradation of analog block when conducted interferences are coupled on their power supply pins, leads us to focus on the impact of ageing on immunity of circuits with interferences coupled on power supply pin. The further research aims at correlating the immunity level drift to the IC intrinsic degradation mechanisms, in order to understand the origin of the observed drift, and predict in which extent the immunity threshold could change. In the next two chapters, we will deal with the modeling of effects of degradation mechanism on transistor physical parameters and the relation with circuit immunity model. Chapter III will be focused on the characterization and modeling of intrinsic degradation mechanisms, with a special emphasis about hot carrier injection and negative bias temperature instability. In chapter IV, we will try to take into account to IC intrinsic degradation mechanisms in IC susceptibility simulation, in order to reproduce the susceptibility level variations observed experimentally.

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Chapter 3: Characterization and modeling of transistor degradation mechanisms

In the previous chapter, we have demonstrated the impact of ageing on EMC at circuit level, such as conducted emission and conducted immunity. The variation of EMC levels of IC could be induced by device degradation and the associated transistor parameters shift. The need of the prediction the circuit EMC variation promotes the development of EMR model. It is composed of the EMC model of the circuit and also the source of EMC variation: transistor degradation model for different mechanisms. In the next two chapters, we will deal with the transistor degradation modeling and circuit EMC modeling aware of degradation mechanisms respectively.

1. EMR MODELING METHOD

1.1. General principle of modeling

After EMR characterization, we have demonstrated and quantified the variation of EMC level after aging. The prediction of the degradation of immunity level after aging has a major importance. To predict the impact of IC aging on EMC level, different levels of model are developed. Figure III-1 illustrates the general flow of EMR modeling method.

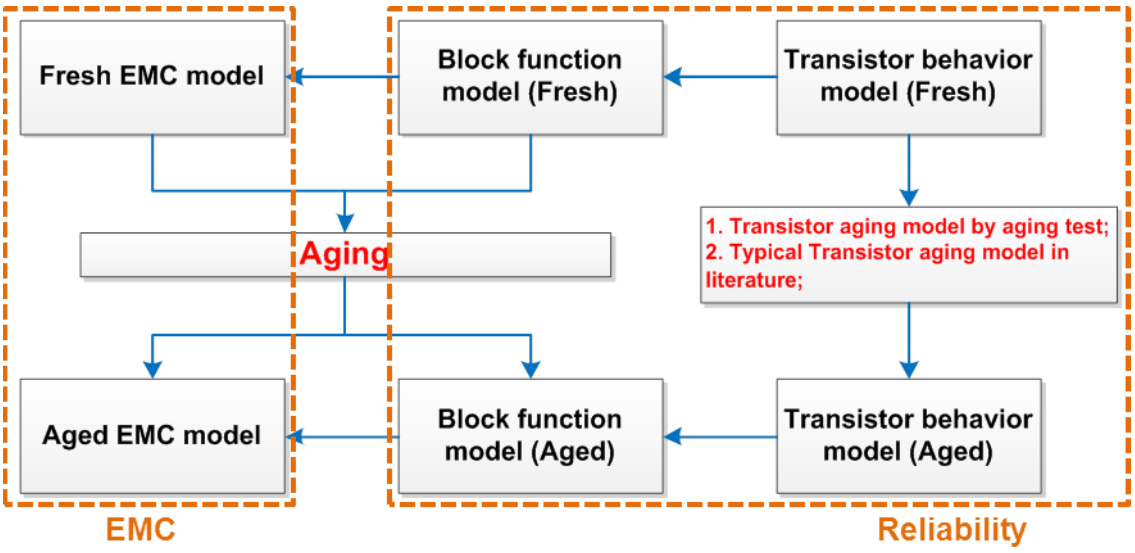

Figure III-1: EMR modeling flow

In this figure and in the rest of the manuscript, we will distinguish "fresh" and "aged" devices or circuits, according to the degradation degree. Contrary to an aged component, a fresh component has not been submitted to any stress or accelerated aging test, so that its electrical and physical properties have not been altered.

EMR modeling is the combination of EMC modeling and reliability modeling. The EMC modeling usually relies on an equivalent electrical model (combined with electromagnetic modeling) to model the whole electronic system (IC component, PCB and test environment). The construction of EMC model for IC can be based on standards such as ICEM (IEC 62433-2) [IEC 62433-2] for emission prediction or ICIM (IEC 62433-4) [IEC 62433-4] for immunity prediction. The validity of the EMC model of a circuit can be verified by comparison between simulation and measurements obtained on "fresh" components. Once the IC EMC model is validated, the same model could be reused for simulation of aged circuits as we assume that only the integrated circuit in the system undergoes aging. The degradation of component functionality could be explained by behavior change of its basic element, i.e. transistor. Therefore, the two main issues are to develop transistor degradation models to evaluate the effect of ageing at transistor level, and then modify the properties of the transistors of a circuit depending on the applied stress. In this chapter, we will focus on the first issue. The degradation of transistor behavior is induced by different degradation mechanisms during the circuit operation. In chapter 1, we have identified three main degradation mechanisms which can alter considerably the electrical characteristics of a MOS transistor: Negative Bias Temperature Instability (NBTI), Hot Carrier Injection (HCI) and Time Dependent Dielectric Breakdown (TDDB). In the following parts, only the two first mechanisms will be studied.

1.2. CMOS inverter degradation modes

IC could suffer different degradation mechanisms which could induce transistor parameter shift, such as the HCI, NBTI and TDDB described in Chapter 1. They are activated by different stress conditions. For the CMOS technology around 0.25µm technological node, the traditional stress conditions for these three mechanisms are listed below (Table III-1) [TAKE83b] [SCHR06]

Degradation mechanism	NMOS	PMOS
HCI	High lateral electrical field where V_{GS} is taking into account, normally V_{GS}@ Peak I_{sub}, with tech. developing below 0.25µm, this condition move to $V_G = V_{DSTRESS}$	High lateral electrical field where V_{GS} is taking into account, normally V_{GS}@ Peak I_G, with tech. developing below 0.25µm, this condition move to $V_G = V_{DSTRESS}$
NBTI		Negative gate bias stress compare to source, thus $\|V_{GS}\| > V_{DDMAX}$

TDDB	Constant high gate voltage compares to bulk potential $\|V_G\| > V_{DDMAX}$	Constant negative gate voltage compares to bulk potential $\|V_G\| > V_{DDMAX}$

Table III-1: Typical stress conditions of activation of HCI, NBTI and TDDB degradation mechanisms

During the circuit operation, the operation condition could meet one of these above stress conditions and activated one or several degradation mechanisms listed in the above table. To illustrate it, let's consider the operation of a CMOS inverter, as shown in Figure III-2.

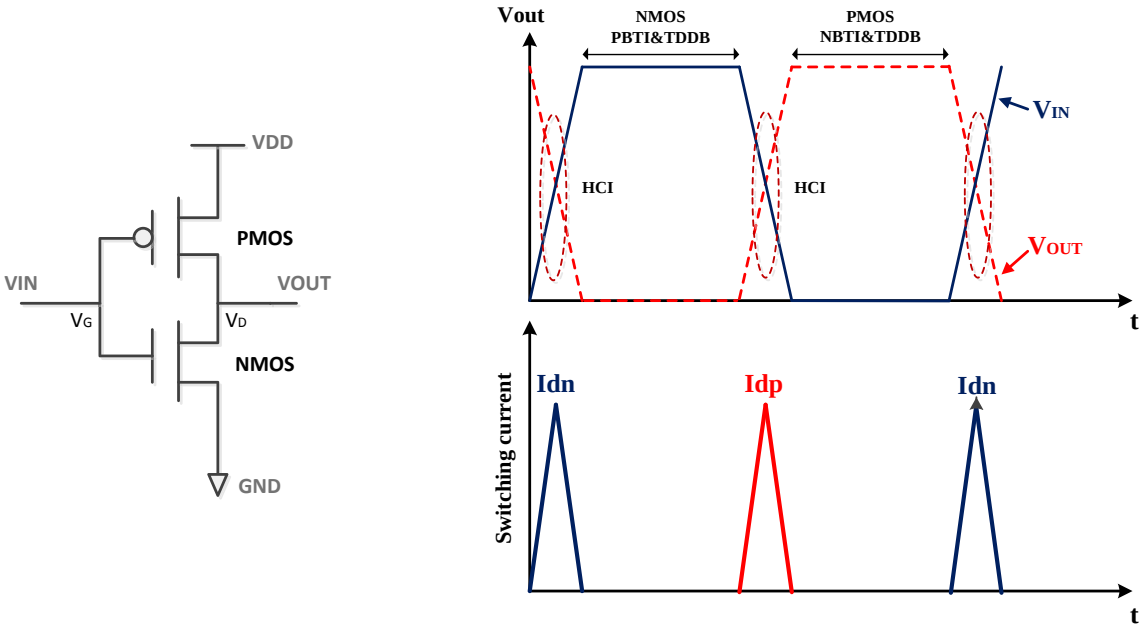

Figure III-2: CMOS inverter suffers different degradation mechanisms during its operation (left) inverter schematic; (right) the different activated degradation mechanism vs. the operation

The degradation mechanisms stress conditions are inherent in CMOS circuit operation. When V_{IN} is high (V_{DD}) and V_{OUT} is low (GND), the high gate voltage and low source voltage make the NMOS under PBTI and TDDB stress conditions. Conversely, PMOS suffers NBTI and TDDB, when the V_{IN} is low (0V) and V_{OUT} is high, since the gate voltage (V_G) is negative with respect to both drain and source voltages. NMOS and PMOS suffer HCI only during the switching period. As V_G of the NMOS transistor switches from low to high, the load capacitance is discharging, the drain bias, $V_D = V_{OUT}$, begins to decrease. When $V_G \approx V_D/2$, the bulk current reaches its maximum value, the NMOS transistor goes through the maximum HCI condition. Oppositely, while the load capacitance is charging up, the PMOS experiences HCI stress.

From the comparison explained in the second part of Chapter 1, NBTI and TDDB for PMOS are the dominant degradation mechanisms comparing with PBTI and TDDB for NMOS during inverter static state of the CMOS inverter. While the HCI impact on NMOS is prominent as electrons face a smaller potential barrier than holes at Si/SiO2 interface. For time reason, we will focus only on the characterization and the modeling of NBTI mechanism in PMOS devices and HCI mechanism in

NMOS devices, although other mechanisms can affect these devices. The experimental characterization of these mechanisms will be done independently by applying different stress conditions. From transistor characterization, the variations of transistor electrical parameters can be extracted in order to model the impact of these degradation mechanisms at transistor level.

1.3. Degradation mechanism characterization

The complete transistor characterization includes DC behavior, small signal and noise performance. In the first time, we characterize the impact of transistor intrinsic degradation mechanisms, such as NBTI on PMOS and HCI on NMOS, on transistor the DC behavior variation.

1.3.1. Characterization of NMOS degradation due to HCI

NMOS parameters are shifted due to hot carrier injection induced by the large electric field in channel near the drain region. The hot carriers which gained enough energy could break the bonds at the Si/SiO2 interface and some of them can be trapped in the oxide. The trapping or bond breaking creates interface traps and oxide charge that affect the transistor performance, such as modify threshold voltage (V_{TH}), mobility (μ)…etc.

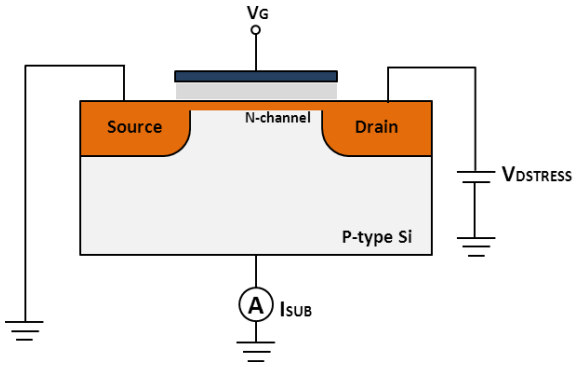

Figure III-3: Stress condition for NMOS Hot carrier injection test

Figure III-3 illustrates the stress conditions used to activate, HCI in NMOS transistor. Although low temperature accelerates HCI, the HCI characterization is performed at room temperature in order to simplify our experimental set-up and consider only one acceleration factor. We apply on the transistor drain a stress voltage $V_{DSTRESS}$ comprised between the maximum power supply voltage V_{DDMAX} and oxide breakdown voltage $V_{BD.}$ Once the $V_{DSTRESS}$ is selected, the corresponding gate bias is adjusted to induce the maximum possible bulk current (measured with a precision ampere meter). The bulk and source are connected to the ground.

1.3.2. Characterization of PMOS degradation due to NBTI

Negative bias temperature instability effect on PMOS is mainly due to the generation of interface traps and positive oxide charges in Si/SiO2 interface under negative gate bias, in particular at elevated temperature. The NBTI could degrade PMOS transistor parameters, such as shift threshold voltage (V_{TH}) and reduction of mobility (μ). The degradation could be accelerated by temperature, the oxide electric field and the nitrogen concentration. NBTI measurement suffers from the recovery problem, which make the NBTI characterization difficult. After the stress procedure, the stress voltages are removed in order to characterize the PMOS transistor in nominal conditions. During this step, the interface traps generated during NBT stress are partially annealed and the induced degradation is partially recovered. An alternative to NBTI quantification method is fast ΔI_D method proposed by Kaczer [KACZ05]. The method can reduce both the measurement time in the stress-measure-stress flow and the recovery time during the device parameters monitoring.

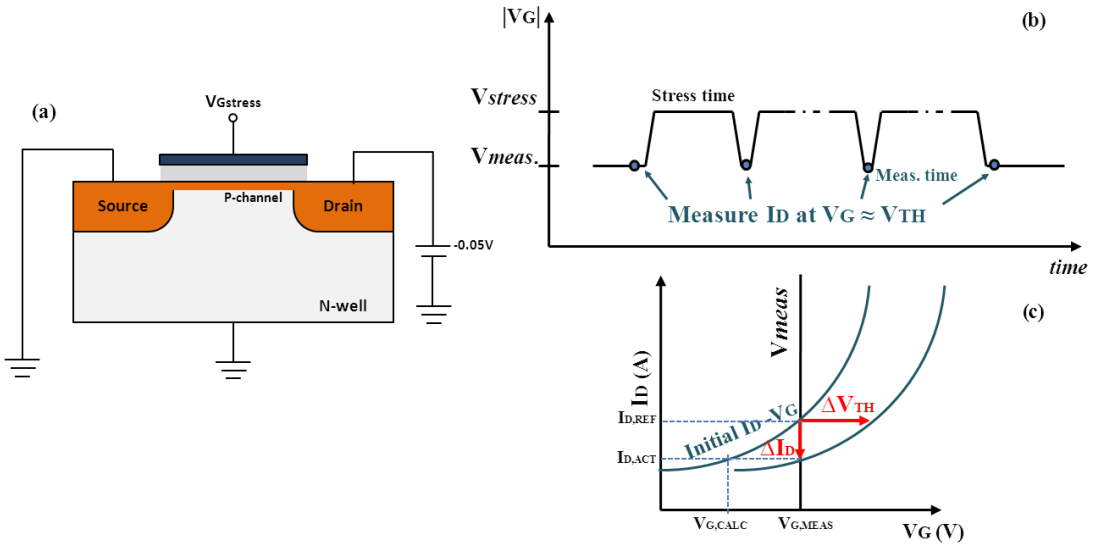

Figure III-4: PMOS NBTI evaluation method: (a) DUT stress condition during the measurement (b) PMOS NBTI fast ΔI_D method, where V_G bias at Vstress during the stress step and bias at Vmeas during the characterization step. (c) ID is monitored and subsequently converted to ΔV_{TH} by horizontally shifting the initial I_D-V_G curve.

Figure III-4 (a) depicts the PMOS NBTI measurement, the DUT is bias with a small drain – source voltage V_{DS} (typically -0.05V) to ensure that the stress voltage applied across the gate dielectric is nearly uniform. The fast NBTI evaluation method begins with an initial I_D-V_G characterization to obtain a conversion "table" for all subsequent I_D measurement. The threshold voltage (V_{TH}) is calculated by the extraction of the maximum transconductance G_M versus the gate voltage V_G. The gate voltage value which induces a maximum transconductance G_M is then set to $V_{G,MEAS}$ and the drain current is set to $I_{D,\,REF}$.

The rest experiment is then divided in two steps:

1) The stress step: a negative gate stress voltage is applied, the gate voltage is between the maximum power supply voltage V_{DDMAX} and the breakdown voltage V_{BD}, while V_{DS} keeps -0.05V;

2) Drain current I_D characterization step: the V_{DS} bias is unchanged to minimize any unaccounted stressing of the DUT, and I_D-V_G curve is measured only up to $V_{G,MEAS}$. The initial PMOS drain current should be monitored for 100s before stress voltage is applied (as Figure III-4 (b)). The first blue point is the initial characterization. The measurement delay could keep as short as possible to reduce the NBTI degradation relaxation phenomena. Measurement delay is determined of the rise/fall time of the voltage source and measurement response time.

For each stress step, the variation of V_{TH} (ΔV_{TH}) is calculated from the difference of $V_{G,\,MEAS}$ and $V_{G,\,CALC}$ which is extrapolated from the actual measured $I_{D,\,ACT}$ by using the slope near V_{TH} of the initial I_D-V_G curve (the conversion "table" obtained from the initial I_D-V_G characterization) (Figure III-4 (c)). The new guessed V_{TH} (ΔV_{TH} + V_{TH}) can be corrected after each step to obtain a very good approximation within 1 mV of the real V_{TH} [REIS07].

1.4. Transistor models and parameters extraction method

To be able to simulate the behavior of the electrical circuit, we need to model the transistors with models which are compatible with electrical simulator such as SPICE (Simulation program with integrated circuit emphasis). The SPICE type circuit simulators calculate the current-voltage characteristics of the devices (device model) to conform a circuit network, where currents in each branch and voltages at each node are determined. Transistors are modeled model by equations that describe the behavior in term of the current vs. voltage from a set of parameters. The SPICE device model could be grouped in two different types of models [ALTU10]:

- Threshold voltage model: the I-V characteristics are divided into several parts or regions, with different sets of equations for each region: e.g. subthreshold, above threshold, linear and saturation regions; Example of these first models are the empirical models: SPICE level 1[SHIC68], level 2[MEYE71]; the semi-empirical models: level 3, the first generation of BSIM models [SHEU87]; the alterative simplified model: nth power law model [SAKU91].
- Compact model: currents are obtained from only one equation that works in different operation regions. They are based either the calculation of mobile charge or surface potential. Examples are the BSIM3v3 and its extension BSIM4 [LIU01], and the EKV model [ENZ95].

Each transistor model has a set of parameters which consists of three types of model parameters:

- Technological parameters: transistor dimensions, oxide thickness, source or drain area…
- Electrical parameters: threshold voltage, mobility, gate, drain or source terminal resistor…;
- Fitting parameters: used to fit the model to the experimental data.

During the study of hot carrier and negative bias temperature instability degradation effects on the MOS transistor performance, we evaluate the evolution of the threshold voltage (ΔV_{TH}) and the relative mobility variations (μ'_n/μ_n) from the measured I_D – V_G curves after each stress cycle [MART10] [KACZ05].

1.4.1. Extraction of the threshold voltage of a MOS transistor

There exist various methods to extract threshold voltage, as constant current (CC) and extrapolation of the linear region (ELR), where the MOSFET is biased in the linear region. With the extrapolation in the saturation region (ESR) method, as suggested by its name, the transistor is biased in saturation region. In our research, we choose the most popular and simplest ELR threshold voltage extraction method. It consists in extracting the threshold voltage V_{TH} experimentally from the I_D – V_G characteristics. In the linear mode of operation ($V_{DS} < V_{DS}$), the I_D – V_G characteristics for long channel devices can be expressed using: (Equation III-1)

$$I_{DS} = \frac{W}{L}\mu C_{ox}\left[(V_{GS} - V_{TH})V_{DS} - \frac{{V_{DS}}^2}{2}\right] \qquad \text{Equation III-1}$$

For small drain voltage (the I_D – V_G characteristics is usually measured with V_{DS} = 50mV) the channel current is given by the following expression (Equation III-2).

$$I_{DS} = \frac{W}{L}\mu C_{ox}(V_{GS} - V_{TH})V_{DS} \qquad \text{Equation III-2}$$

The Equation III-2 predicts that by plotting I_D versus V_{GS} at a constant small V_{DS}, a straight line must be obtained. Due to the subthreshold conductance at low V_{GS} and short channel effects as effective mobility degradation at high V_{GS} (the large electric field induces the carrier velocity saturation) the actual curve is not a straight line. As shown in Figure III-5:

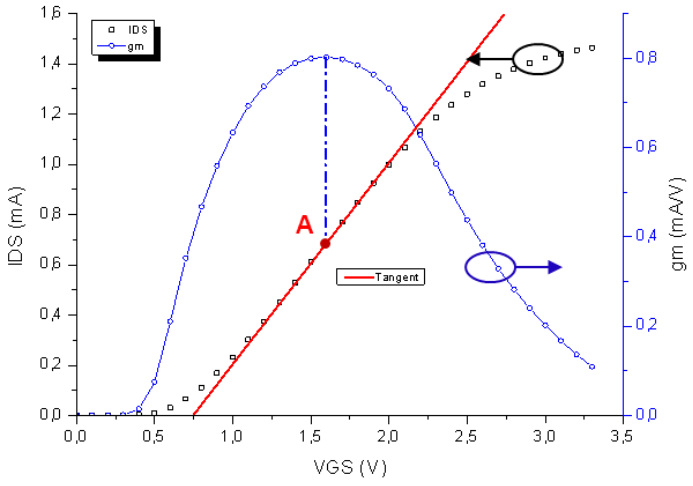

Figure III-5: VTH extraction using extrapolation of the linear region method for a short channel device operated in linear region

The threshold voltage can be extracted from a linear extrapolation of the I_D – V_G curve at its maximum first derivative point (the slope at point A in Figure III-5), i.e. the point of maximum

transconductance gm. The threshold value is found at the intercept of the tangent at the maximum I_D – V_G slope point (point A in Figure III-5) with the V_{GS} axis [TSIV87]. This deduced V_{TH} value is also dependent on the source/drain series parasitic resistances. As we are interested in the variation of threshold voltage (ΔV_{TH}), and as we can assume that the parasitic resistances are not affected by voltage stress, their influence can be removed by the subtraction of measurements done after and before stress.

1.4.2. Extraction of the transconductance and carrier mobility of a MOS transistor

The channel transconductance is defined as the rate of change of drain current as a function of the gate bias at a given drain bias [PAGE02] (Equation III-3)

$$G_m(V_{DS}) = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{W}{L}\mu C_{ox} V_{DS} \qquad \text{Equation III-3}$$

By taking first derivative of drain current with respect to the gate bias using the I_D – V_G curve, we can easily get the transconductance. Unfortunately, a short channel device does not behave like a long channel one. The derivative of drain current does not have a constant value and shows a non-monotonic relation with V_{GS} (the blue dash line plotted in Figure III - 5). The channel transconductance in short channel devices is usually taken at the maximum value. The variation of carrier mobility can be calculated by relative variation under the assumption that all the other parameters do not change after stress (Equation III-4).

$$\frac{G_m(t = t_s)}{G_m(t = 0)} = \frac{\mu_n(t = t_s)}{\mu_n(t = 0)} \qquad \text{Equation III-4}$$

2. DEGRADATION MECHANISM CHARACTERIZATION

2.1. Device under test description

The DUT dedicated to the in degradation mechanism characterization is called ELMER (ELectroMagnetic Enhanced Robustness) designed in Freescale's CMOS 90nm process at Toulouse, France. It contains two different categories of experimental structures:

- Probe experiments: NMOS and PMOS transistors with various geometries and oxide options. The access to their terminals is done by probes. The die is bare. (Figure III-6-left)

- Bonded experiment: NMOS and PMOS transistors with various geometries and oxide options. Their terminals are connected is connected to bonding pads and the die is encapsulated within a SOIC28 package. (Figure III-6-right)

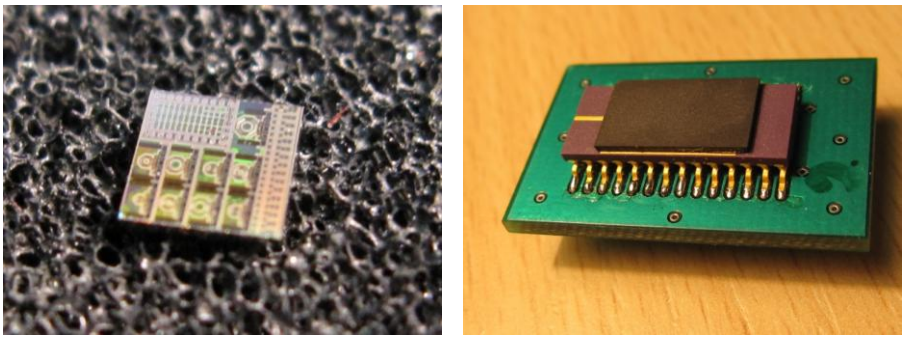

Figure III-6: die without package for probe experiment (left) and die encapsulated within package for bonded experiment (right)

The designed transistors have different geometries, with two kinds of operation voltages depending on gate oxide thickness: low operation voltage with high threshold voltage dedicated to low power consumption, and high operation voltage with standard threshold voltage. The dimensions of the transistors are listed in Table III-2.

	Low voltage 1.2V high V_{TH}		**High voltage 3.3V Standard V_{TH}**	
NMOS (W/L)	10µ/0.1µ	10µ/0.4µ	10µ/0.38µ	10µ/1.52µ
PMOS (W/L)	10µ/0.1µ	10µ/0.4µ	10µ/0.38µ	10µ/1.52µ

Table III-2: Typical stress conditions for the three degradation mechanisms

The DUT was built on a continuous low doping P epitaxial layer deposited over a highly doped P wafer. The N/P junction breakdown voltage is around 10V.

2.2. HCI characterization on NMOS transistor

2.2.1. Experimental set-up description

To analyze the impact of HCI on NMOS, we use the method described in section III-1.3.1. A power supply voltage source and an Agilent digital multimeter are connected to the drain of NMOS as a source meter (V_{DS}) and the current meter (I_{DS}). A NI-DAQ acquisition board is used to control the gate voltage (V_{GS}). The Keithley 2602A source meter is able to measure bulk current, with a 1pA resolution, as shown in Figure III-7. V_{DS} is set to different values above V_{DDMAX}. V_{GS} stress voltage is defined as the gate voltage corresponding to the maximum substrate current I_{sub} value on the I_{sub} – V_{GS} curve. Table III-3 summarizes the different stress voltages applied to the different types of NMOS

transistor. The four terminals of the transistor are accessed with DC probes and Cascade probe station. The experiment was under room temperature 29°C ±1°C.

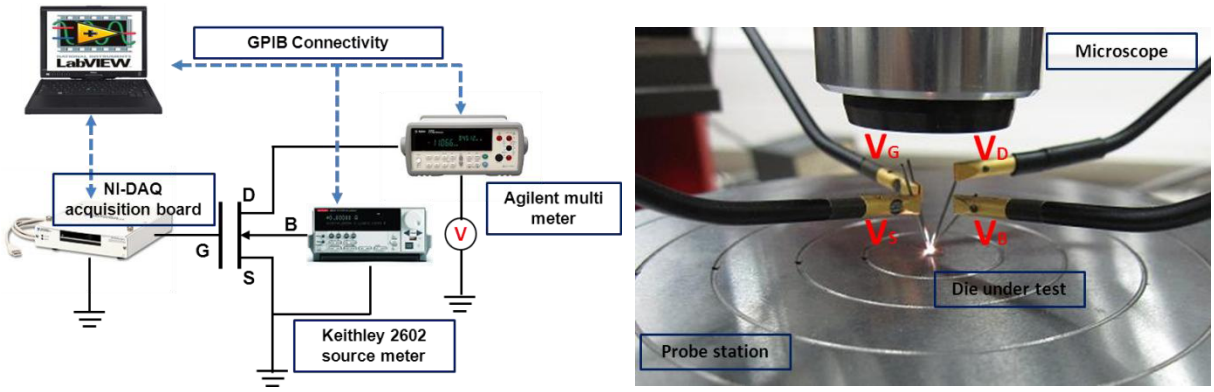

Figure III-7: HCI on NMOS experimental set-up (left) and probe measurement with Cascade probe station (right)

NMOS (W/L)	$V_{DS,STRESS}$ (V)	$V_{GS,STRESS}$ (V)
High voltage (10µ/1.52µ)	8	3.06
Low voltage (10µ/0.4µ)	4	1.05

Table III-3: HCI experiments transistor under test type and stress conditions

All apparatus are connected to PC with GPIB cables and the measurement is controlled by Labview program which integrates the data processing program such as the V_{TH} calculation. The measurement flow of HCI degradation test is described in Figure III-8.

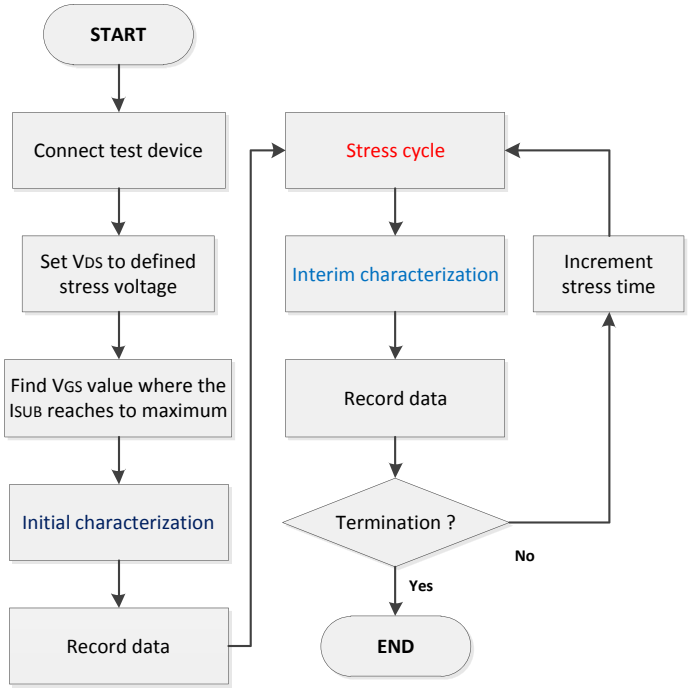

Figure III-8: HCI degradation test measurement flow

2.2.2. Experimental results

In the HCI degradation measurement, the low voltage long channel NMOS and high voltage NMOS are stressed under a bias condition which induces a maximum substrate current. The stress is 1500s and 4500s respectively. The following paragraphs present two obvious degradation examples for each type of NMOS transistors.

2.2.2.1. Low voltage (10µ/0.4µ) NMOS

Firstly, the gate stress conditions are defined by finding the gate to source voltage which induces the maximum substrate current whatever the drain stress voltage. The I_{SUB} – V_{GS} characterization is shown in Figure III-9.

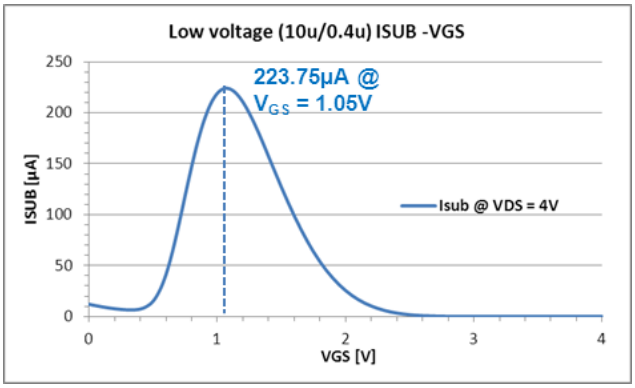

Figure III-9: low voltage transistor gate stress condition is defined by the voltage which optimizes the substrate current

With drain stress voltage equal to 4V, the maximum substrate current is 223.75µA at 1.05V, so the applied stress condition is $V_{GSstress}$ = 1.05V and $V_{DSstress}$ = 4V. With default channel length, the stressed lateral electrical field is 10e^6 V/m. (Equation III-5)

$$E_{lateral} = \frac{V_{DS}}{L_{channel}} \approx \frac{4}{0.4 \times 10^{-6}} = 10^7 V/m \qquad \text{Equation III-5}$$

The stress is applied during 1500s. The drain currents measured with a gate voltage equal to 1.2V are compared after every stress cycle (Figure III-10-left). The right part of figure presents the relative degradation of drain current along the stress time (Figure III-10-right).

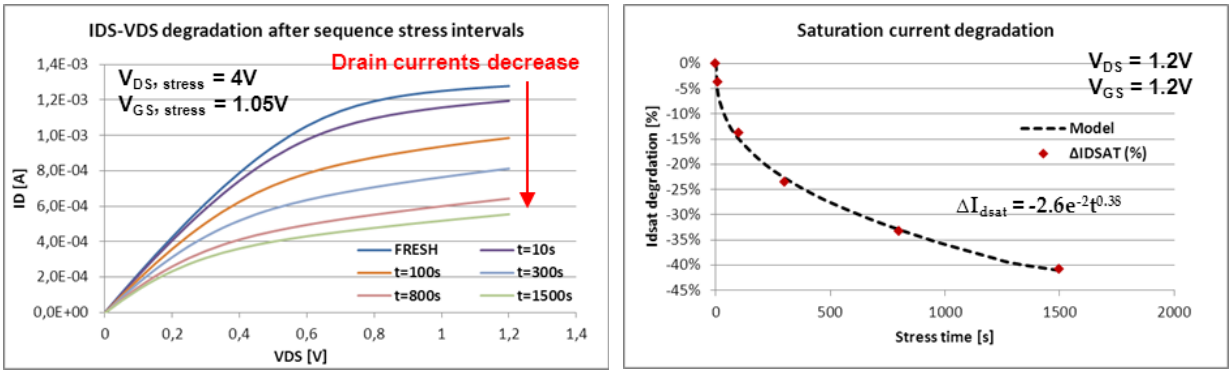

Figure III-10: IDS – VDS degradation after sequences stress (left) and IDSAT degradation as a power relation with time (right)

Under $V_{GSstress}$ = 1.05V and $V_{DSstress}$ = 4V, the drain saturation current measured at $V_{DS} = V_{GS}$ = 1.2V decrease with stress time according to a power law. An empirical models using power law equation to fit the variation of saturation current with stress time t is given by Equation III-6.

$$\Delta I_{dsat} = At^{n} \qquad \text{Equation III-6}$$

Where A is a fitting constant and n is the exponent that controls the time dependence of the reduction of drain current. They are strongly dependent on stress voltage applied on the drain. The coefficient values extracted from the experimental results given in the Figure III-9, are n=0.38, A = -2.6e-2;

The threshold voltage and mobility are also extracted after each stress cycle. The threshold voltage variation given in mV and mobility relative variation are presented in Figure III-11.

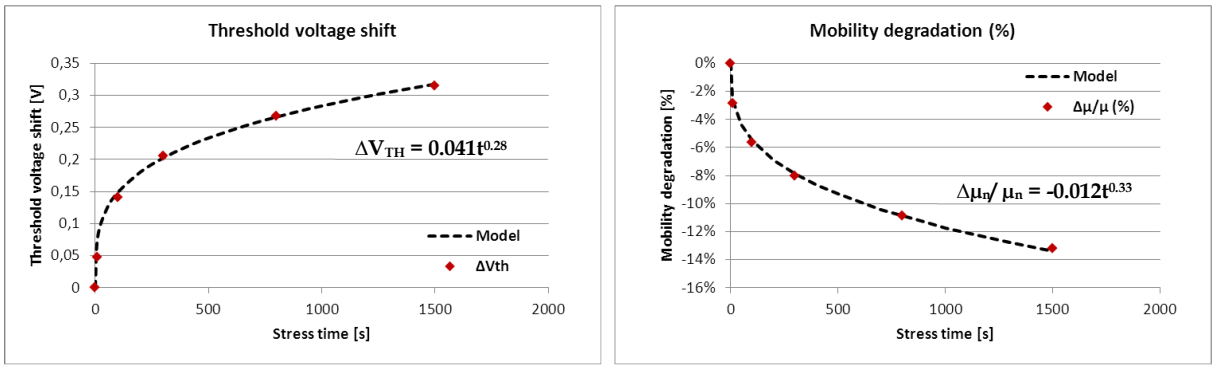

Figure III-11: Threshold voltage shift (left) and mobility relative degradation vs. stress time (right)

After applying a constant voltage stress during 1500s, the threshold voltage variations reaches up to 0.32V. The evolution of the threshold voltage can also be modeled with a power law equation (indicated in the Figure III-11). The mobility decreases about -13.2%. The shift of threshold voltage and the variation of mobility are important.

2.2.2.2. *High voltage (10µ/1.52µ) NMOS*

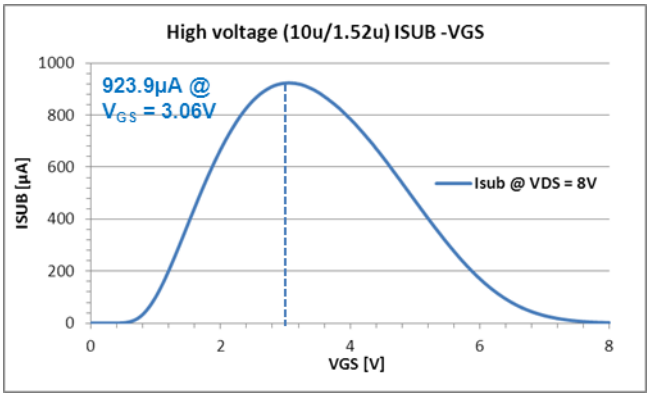

Figure III-12: High voltage long channel transistor gate stress condition is defined by the gate to source voltage which optimizes the substrate current.

For the high voltage NMOS, we apply a stress voltage equal to 8V on the drain stress. The maximum substrate current reaches 923.9µA at 3.06V, therefore the stress condition is $V_{GSstress}$ = 3.06V and $V_{DSstress}$ = 8V (Figure III-12). The stressed lateral electrical field can be calculated with the default channel length (Equation III-7)

$$E_{lateral} = \frac{V_{DS}}{L_{channel}} \approx \frac{8}{1.52 \times 10^{-6}} = 5.3 \times 10^{6} V/m \qquad \text{Equation III-7}$$

The drain currents measured with a gate voltage equal to 3.3V are compared after every stress cycle up to 4500s. (Figure III-13-left). The right part of the figure presents the degradation of drain current along the stress time (Figure III-13-right).

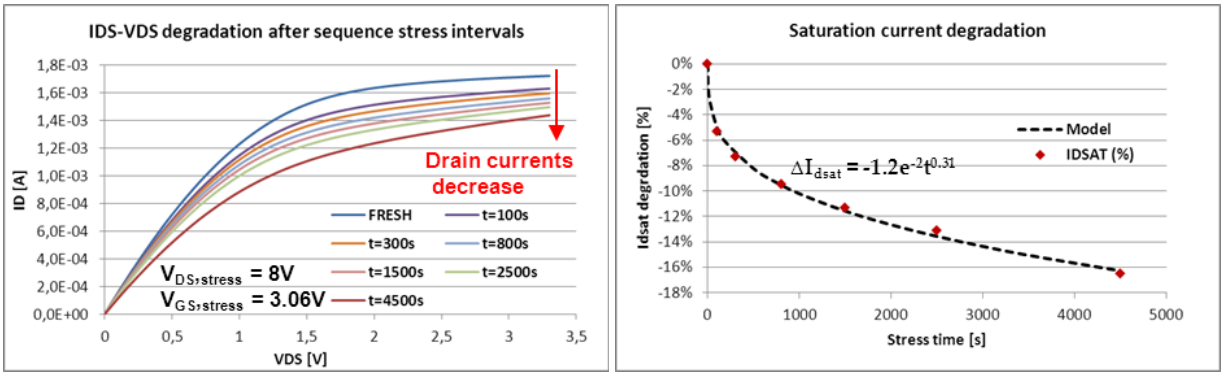

Figure III-13: IDS – VDS degradation after sequences stress (left) and I_{DSAT} relative degradation which follows a power relation with time (right)

The degradation of saturation current has a power relation with the stress time. According to Equation III-6, the parameters of the saturation current degradation model are A=-1.2 and n=0.31. Since the lateral electrical field induced during stress is weaker (two times lesser), the degradation of the saturation current in high voltage long channel NMOS is less than in low voltage short channel.

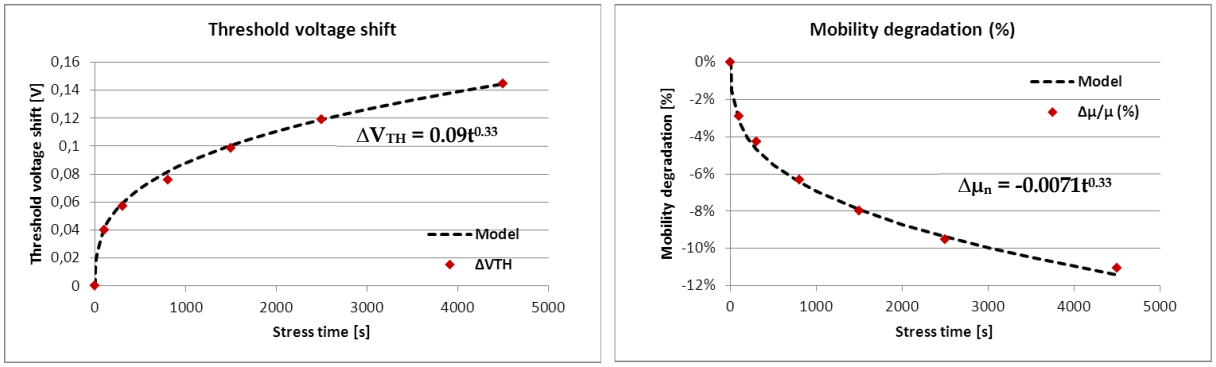

Figure III-14: Threshold voltage shift (left) and mobility relative degradation vs. stress time (right)

After applying a constant voltage stress for 4500s, the threshold voltage increases about 0.15V. This evolution can also be modeled by a power law equation (indicated in the Figure III-14). The mobility decreases ratio reaches -11% after 4500s. From the degradation equation shown in the Figure III-14, the shift of threshold voltage and the variation of mobility are important.

2.3. NBTI on PMOS characterization

2.3.1. Experimental set-up description

In order to analyze the impact of NBTI on PMOS, we use the method described in section III-1.3.2. The experimental set-up is depicted in Figure III-15. A Keithley 2602A source meter is connected to the drain of PMOS to set the drain to source voltage (V_{DS}) and measure the drain current (I_{DS}). With a 1pA resolution and settling time less than 50 µs, we can consider that it is able to measure the drain current variation instantaneously and that recovery phenomenon remains negligible during transistor characterization. A NI-DAQ acquisition card is used to control the gate voltage (V_{GS}). The test set-up is depicted in Figure III-15. V_{DS} is set to -50mV and the V_{GS} stress voltages for the different types of PMOS transistor are defined in Table III-4. The four terminals of the transistor are accessed with DC probes and Cascade probe station. The experiment was done under room temperature (29°C ±1°C).

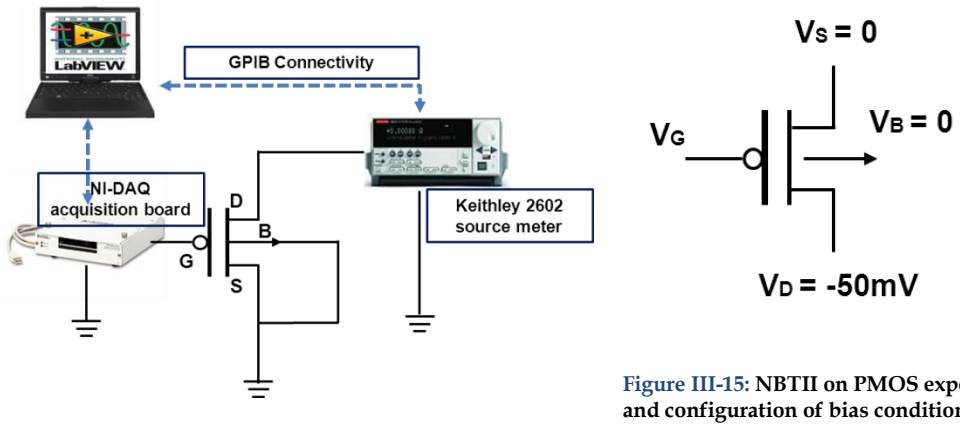

Figure III-15: NBTII on PMOS experimental set-up (left) and configuration of bias condition (right)

PMOS (W/L)	$V_{DS,STRESS}$ (V)	$V_{GS,STRESS}$ (V)
High voltage (10µ/1.52µ)	-0.05	-6
Low voltage (10µ/0.4µ)	-0.05	-3.2

Table III-4: NBTI experiments transistor types and stress conditions

All apparatus are connected to PC with GPIB cables and the measurement is controlled by Labview program which integrates the data processing program as the V_{TH} calculation. The measurement flow of NBTI degradation test is shown in Figure III-16.

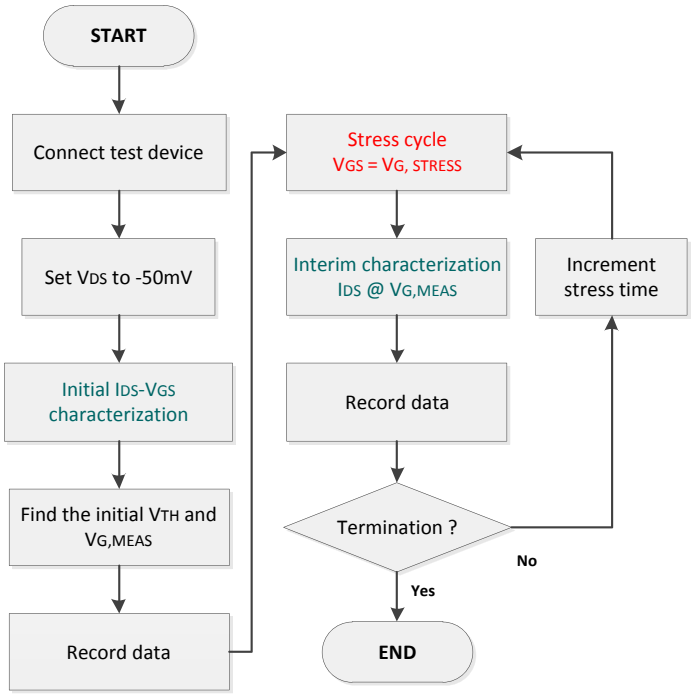

Figure III-16: NBTI degradation measurement flow

2.3.2. Experimental results

Due to the relaxation phenomenon and process variation between components, the variations of threshold for each component are not the same. We measured 3 components with the same transistor geometry and under the same bias condition. The average variation of V_{TH} is calculated from the measurements performed on 3 samples. The variation of the V_{TH} is expressed in percentage, as the ΔV_{TH} is proportional to but different from the conventional ΔV_{TH} (obtained from the IV characterizations), as the mobility degradation is not taken into account.

2.3.2.1. *Low voltage (10µ/0.4µ) PMOS*

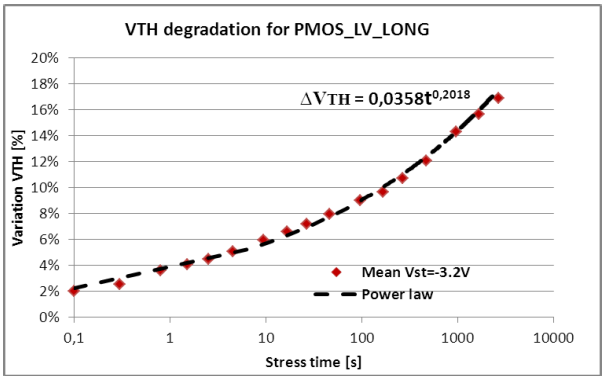

Figure III-17: ΔVTH of the low voltage PMOS transistor as a power law function of stress time for NBTI stress.

Figure III-17 shows the variation of threshold voltage for the low voltage transistor with the following aspect ratio (10µm/0.4µm). The evolution of threshold voltage ΔV_{TH} has a power law dependence with stress time (As expressed in Equation III-6). Where n = 0.2018 and constant fitting parameter A is 0.0358. After 2700s stress, the threshold voltage could increase 17% from its origin value.

2.3.2.2. *High voltage (10µ/1.52µ) PMOS*

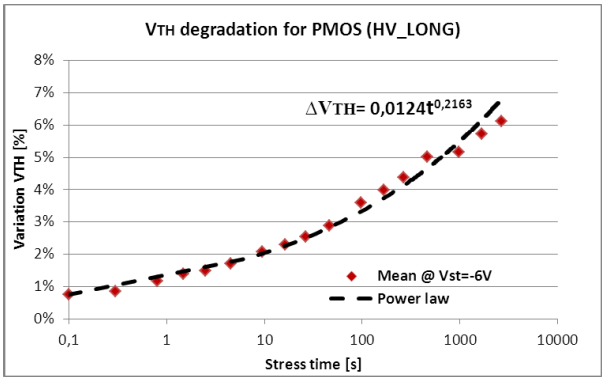

Figure III-18: ΔVTH of the high voltage PMOS transistor as a power law function of stress time for NBTI stress.

Figure III-18 shows the variation of threshold voltage for the low voltage transistor with aspect ratio (10µm/1.52µm). The evolution of threshold voltage ΔV_{TH} has power law dependence with stress time. The parameters of the model can be extracted from measurements: n = 0.2163 and constant fitting parameter A is 0.0124. After 2700s stress, the threshold voltage could increase 6% from its origin value. The comparison of the results for low voltage PMOS with aspect ratio (10µm/0.4µm) and high voltage one with aspect ratio (10µm/1.52µm) shows that the threshold voltage variation has the dependence of transistor geometry. The variation equation of two transistors has the same n value and the A fitting parameter of small transistor is 3 times bigger than the large transistor.

In the session of NBTI characterization, the threshold voltage was assumed to be the only parameter varied due to NBTI degradation. From the experimental results, the threshold voltage

increases after stress whatever the type of transistor. The evolution of the variation follows power law dependence with the stress time.

3. MODELING OF MOS TRANSISTOR MODELS DEGRADATION

This part aims at building transistor models which takes into account intrinsic degradation mechanism effects, from experimental characterization. The primary objective of integrating intrinsic degradation mechanism in transistor model is to transfer the stress effects from the device level up to the circuit level.

After NBTI characterization, the experimental algorithm assumes that only threshold shift after aging. The NBTI degradation model can be obtained by simple modification of the threshold voltage according to the power law evolution of the threshold voltage. Therefore in this section, we will focus only on the modeling of the hot carrier injection effect on transistor.

As the design kit of test circuit (ELMER) involving in the confidential and proprietary information that we cannot access to the original transistor model directly. We will compare two different models which could reproduce the evolution of the I-V characteristics due to hot carrier injection. We create ourselves simplify models with SPICE level 3 model and Takayasu nth power law model to describe the hot carrier degradation to transistor IV characteristic variation.

3.1. SPICE level 3 model

Although the BSIM (Berkeley short channel IGFET model) is developed for submicron short channel transistor, the construction of such a model based on experimental extraction of its parameters and curve fitting remains impractical due to the hundreds of parameters involved in the model.

Our objective is to extract a simple model that can reproduce well the transistor DC behavior with fewer parameters.

SPICE level 3 has fewer parameters and can be easily extracted from curve fitting. Therefore, it can be a good candidate for transistor modeling, even if the accuracy is sacrificed a little [ANTO93]. We use SPICE level 3 to model the transistor IV characteristic degradation due to HCI. With the software ADS (Advanced Design System) the main parameters of the model (V_{TH}, K_P, R_D, R_S, PHI, THETA) are adjusted to provide a reasonable fit to measured device I-V characteristics.

The low voltage long channel transistor (W=10µm and L=0.4 µm) measured and simulated I_{DS} – V_{DS} curves for both fresh device and aged device (after 1500s stress) are shown in Figure III-19.

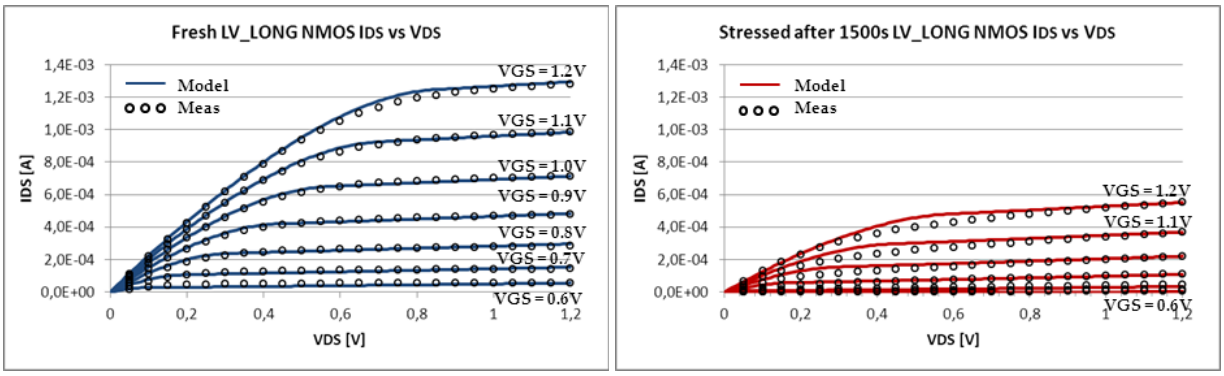

Figure III-19: Comparison of measurement and simulation with SPICE level 3: Fresh device (left) and device stressed after 1500s (right)

From Figure III-19 left, the original SPICE model (continuous lines) fits well with fresh measurement (circles). After 1500s stress, the key parameters threshold voltage (V_{TH}) and transconductance (KP) could reproduce the degradation of the current in saturation region (Figure III-19 and Figure III-20). The fitting between measurement and simulation is acceptable, despite a difference in linear regime, the maximum error between measurement and model simulation is 42.9µA for fresh component and 58.3 µA for aged component. An additional increase of the drain resistance could improve the fitting of current in linear region. The drawback of this model is the discontinuity in the drain current between the linear region and saturation region (transition region). Therefore the simulation in the transition region is not very accurate.

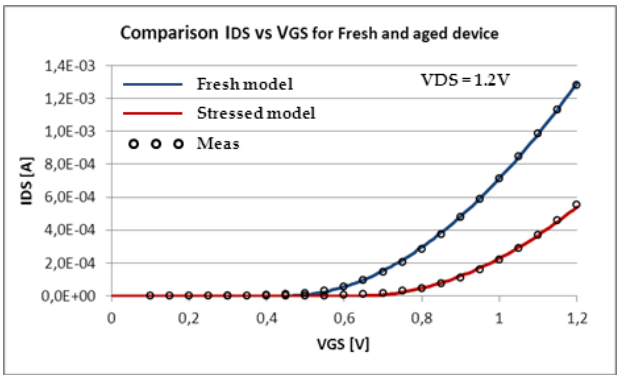

Figure III-20: IDS-VGS characteristic for fresh and stressed (HCI stress) device (low voltage long transistor model W=10µm and L=0.4 µm).The comparison between model (circle) and simulation (line) shows a good accuracy in saturation region

Figure III-20 presents the comparison between measured and simulated I_{DS} – V_{GS} characteristic, with V_{DS} biased under 1.2V. The result demonstrates that the SPICE model level 3 is able to reproduce the degradation of drain current in saturation region. The variation of key fitting model parameters are listed in Table III-5,

	VTH (V)	KP (A/V²)	RD (Ω)
Fresh	0.48	0.000235	185

Stress after 1500s	0.75	0.00019	240
Variation	+0.27	-19%	+30%

Table III-5: The variation of the key parameters of SPICE level 3 model obtained from the fitting with of the experimental data (low voltage long transistor W=10µm and L=0.4 µm)

The variation of fitting parameters such as the threshold voltage (V_{TH}) and transconductance (G_m) are consistent with the mathematically extraction done on the measured results. The drain series resistance increase after hot carrier degradation due to the negative charges trapped in the gate oxide. These charges could deplete the underlying silicon and give rise to the drain side parasitic resistance RD [RAYC96]. In the other hand, it could also increase the potential barrier to electron injection into the oxide, thus slightly decreases the surface potential (PHI).

The same procedure is applied on High voltage long channel transistor (W=10µm and L=1.52 µm). Figure III-21 presents the comparison between experimental I_{DS} – V_{DS} curve and model simulation for fresh and device after 4500s stress.

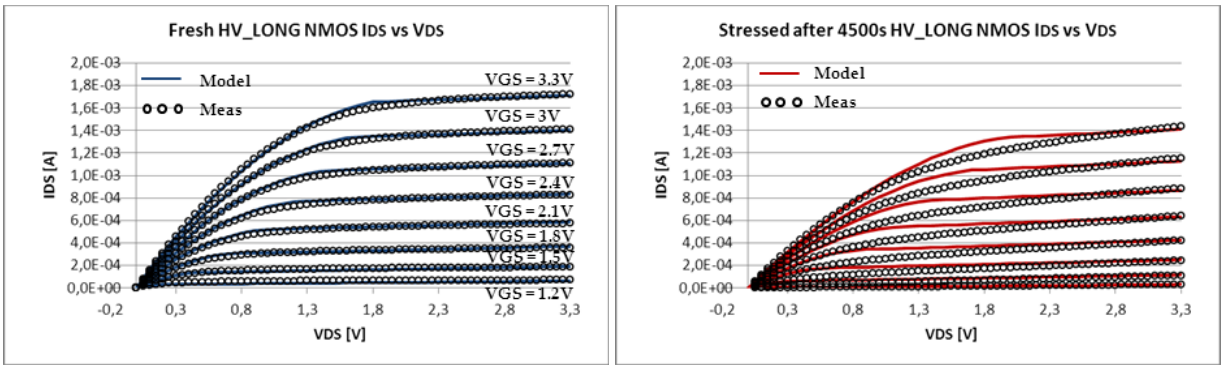

Figure III-21: Comparison between measured and simulated of I-V characteristics of high voltage long channel transistor: fresh device (left) and device stressed after 4500s (right).

As the example of the low voltage long transistor, the original SPICE level 3 is able to approximate with a good accuracy the fresh measurement. After a stress of 4500s, the modified SPICE model reproduced the degradation of channel current by hot carrier effect roughly. Large errors appear in linear region. The measured degradation of drain current is larger than the prediction. The maximum error between measurement and model simulation is 53.7µA for fresh component and 114.4 µA for aged component. Compared with fitting in linear region, a better result is obtained in the saturation region. Figure III-22 shows, the I_{DS} – V_{GS} curve for the drain voltage biased at 3.3V. Predictions and measurements correlate very well in saturation regime before and after stress.

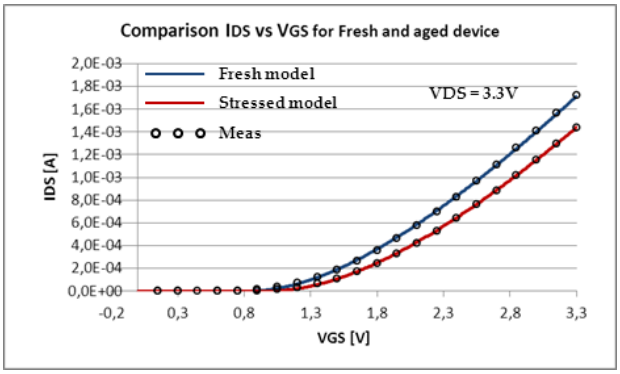

Figure III-22: IDS-VGS characteristic for fresh and stressed device. The comparison between model (circle) and simulation (line) shows a good accuracy in saturation region.

The main fitting parameters in the modified SPICE model are threshold voltage, transconductance and drain resistance. They are listed in Table III-6,

	VTH (V)	KP (A/V²)	RD (Ω)
Fresh	0.9	0.000174	230
Stress after 1500s	1.1	0.000149	310
Variation	+0.2	-14.4%	+39%

Table III-6: The key variation of parameters obtained for the fitting of the experimental data of high voltage transistor model

The comparison of fitting parameters variation shows that variations of model parameters are consistent with mathematically extraction from the measured results. Except the variation of these three main parameters, some parameters as THETA and ETA are slightly increased to improve the curve fitting, but the variation is small compared to the main parameter variation.

3.2. Nth power law model

Owing to develop a simple model suitable for short channel device, Sakurai [SAKU90] [SAKU91] proposed a new simple model called: Alpha-power law or Nth power law MOSFET model. It aims at filling the gap between the inaccurate but simple Shockley model and the complete compact models. It uses only six main parameters and could provide a good accuracy for short channel devices, especially in linear region and saturation voltage. The equations of the n_{th} power law model are given below (Equation III-8 to Equation III-12)

$$V_{DSAT} = K * (V_{GS} - V_{TH})^m \quad \text{Equation III-8}$$

$$I_{DSAT} = B * (V_{GS} - V_{TH})^n \quad \text{Equation III-9}$$

For $V_{GS} < V_{TH}$ (cut-off region):

$$I_{DS} = 0$$ Equation III-10

For $V_{GS} >= V_{TH}$ and $V_{DS} < V_{DSAT}$ (triode region):

$$I_{DS} = I_{DSAT} * (1 + \lambda V_{DS}) * \left(2 - \frac{V_{DS}}{V_{DSAT}}\right) * \left(\frac{V_{DS}}{V_{DSAT}}\right)$$ Equation III-11

For $V_{GS} >= V_{TH}$ and $V_{DS} >= V_{DSAT}$ (saturation region):

$$I_{DS} = I_{DSAT} * (1 + \lambda V_{DS})$$ Equation III-12

Where V_{GS} and V_{DS} are the gate/source and the drain/source voltages, V_{TH} denotes the threshold voltage, V_{DSAT} the drain saturation voltage and I_{DSAT} the drain saturation current. K and m control the linear region characteristics while n determines the saturated region characteristics. B is related to the transconductance, λ is the finite drain conductance in the saturation region.

The extraction of parameters can start with the selection of 11 fitting points, which are used to solve the sub equations for each parameter [SAKU91]. We process these calculations with Matlab programs, then, these initial parameters are provided into SPICE model under ADS tuning function to improve manually their tuning. We reuse the previous measurements made on the low voltage and high voltage NMOS transistors.

I_{DS} – V_{DS} curve of measurement and Nth power law model are compared for fresh device and device after 1500s stress (Figure III-23).

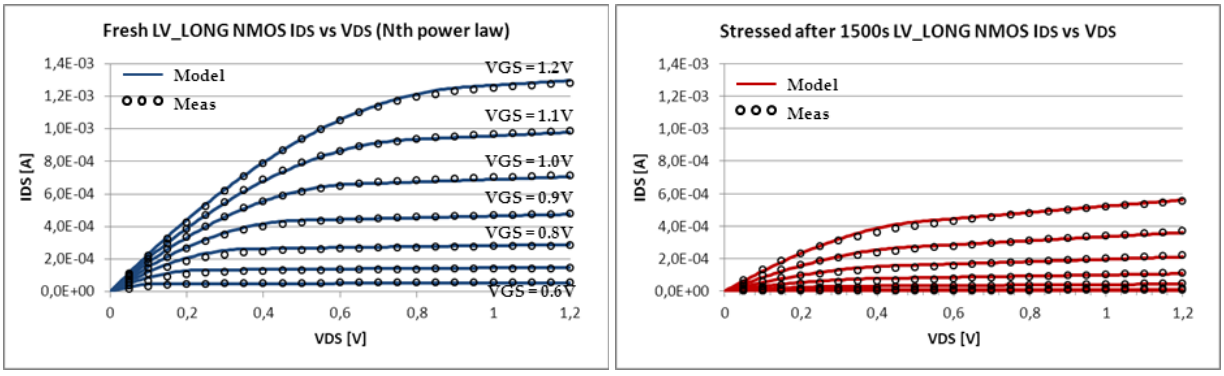

Figure III-23: Comparison of measurement and simulation with nth power law: Fresh device (left) and device stressed after 1500s (right)

The six main parameters of the Nth power law model are extracted from the automatic extraction program for fresh and aged (after 1500s stress) device respectively. Compared with SPICE level 3 model, the correlation between measurement and simulation is improved in linear region with the Nth power law model. The maximum error between measurement and model simulation is 24μA for fresh component and 28.4 μA for aged component. The six main varied fitting parameters are listed in Table III-7.

	λ	V_{TH}	n	B	m	K
Fresh	0.127	0,453	1,957	0,002	1,243	1,342
Stress after 1500s	0.182	0.567	2.587	0.00107	1,03	0.957
Variation	+43%	+25%	+32%	-46.5%	-17.1%	-28.7%

Table III-7: The variation of parameters of Nth power law model obtained from the fitting with the experimental data of high voltage NMOS transistor

A comparison can be made with the results obtained with SPICE 3 model. With the Nth power law model, the rise of threshold voltage and a decrease of transconductance meaning related parameter B are observed, which indicates the degradation induced by hot carrier injection.

The same model extraction is done for the high voltage transistor. The measurement and nth power law model results are compared for fresh and aged devices (after 4500s) (Figure III-24).

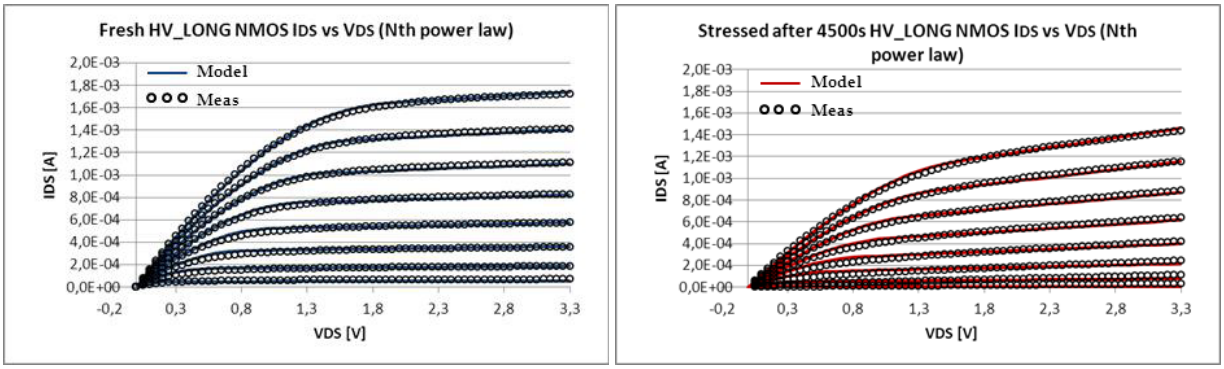

Figure III-24: Comparison of measurement and simulation with nth power law: Fresh device (left) and device stressed after 4500s (right)

Once again, the nth power law model provides an excellent correlation with measurement in linear region. The maximum error between measurement and model simulation is 31µA for fresh component and 36.3 µA for aged component. After 4500s stress, the six main fitting parameters are compared in Table III-8.

	λ	V_{TH}	n	B	m	K
Fresh	0.048	0,91	1,552	0,000396	0.864	0,927
Stress after 1500s	0.105	1.17	1.572	0.000266	0.734	0.917
Variation	+118.8%	+28%	+1.3%	-32.8%	-15%	-0.1%

Table III-8: The variation of parameters of Nth power law model obtained from the fitting of the experimental data of high voltage NMOS transistor

After aging, in accordance with the other result, the threshold voltage increase and the transconductance decrease. However, the drain conductance λ increase largely after 4500s stress which indicates a significant change of the output conductance of the device.

Compared with SPICE level 3 model construction, the extraction of the 6 parameters of the Nth power law model is easier. The Nth power law offers a better modeling both in linear and saturation region. The parameter λ in nth power law could well model the output conductance which is the weakness in SPICE level 3. However, the fitting parameters are strongly depended on the position of the fitting points in I_{DS} – V_{DS} curve, thus the parameters extraction might yield to values that are not consistent with their physical intent. Furthermore, due to the assumption of zero subthreshold current, a convergence problem could be induced during the simulation. To settle this problem, a more accurate model of subthreshold current needs to be created to ensure the continuity of the channel current for all the operation regions.

4. CONCLUSIONS AND DISCUSSIONS

In this chapter, we started with the simulation of EMR, i.e. the evolution of EMC levels of an integrated circuit with time, linked to the modification of internal properties due to intrinsic degradation mechanisms. This modeling and simulation work starts with the extraction of the model of transistor degradation, which can be inserted in the circuit netlist.

A complete characterization of degradation mechanisms which affect transistors designed in a given technology is a long and tedious task, so that we have to limit our experimental and modeling studies only on NBTI in PMOS and HCI in NMOS transistors. The experimental results show that HCI provokes a positive shift of threshold voltage and a decrease of transconductance induced by mobility degradation. The equations that describe the evolution of these parameters have been extracted for transistors with different geometries and gate oxide thickness, under different bias conditions. Whatever the transistor geometry and the stress bias conditions, the evolution of threshold shift and transconductance degradation follows power law dependence with stress time. For the NBTI degradation, according to the fast ΔI_D method, we assume that only threshold voltage varies with the stress time. The experimental results show also that the variation of threshold voltage follows power law relation with the stress time.

With these simple transistor ageing model, we are able to determine the age of one transistor with given geometry and under specific stress conditions. We can predict the variations of its parameters and their impact on the circuit and on the EMC.

Because of the lack of experience about the characterization of transistor degradation mechanisms and the limitation of the number of available device under test, many improvements can be brought in future:

- A minimum of three stress conditions, selected according to the actual circuit stress conditions, should be tested to extract accurately the dependence of stress condition in the evolution equation of transistor parameters.
- During a stress period, at least 3 sample points should be acquired per decade.
- The test should be done at different temperatures to accelerate the degradation with temperature, not only under the room temperature. The dependence of degradation with temperature, which has a significant importance in power devices, can also be extracted.
- Measure several samples with same bias condition and evaluate the parameter variation by average value.
- Other degradation mechanisms can be included. PBTI for NMOS, HCI on PMOS, and TDDB characterization should be added to our test list, since they can affect significantly circuit performance [CRUP05] [AMAT10] [CHOU10].

From characterizations, models of degraded transistors have been proposed, based on two methods: the nth power law and SPICE level 3 transistor models. Both of them are able to reproduce the transistor I-V characteristics accurately. The Nth power law offers a more accurate modeling of transistor I-V characteristics both in linear and saturation regions, with an easier parameter extraction method. However, Nth power law model have some drawbacks: the variations of model parameters have less physical meaning and are more defined by curve fitting. Using this type of model in order to simulate the degradation of a circuit needs to characterize a set of reference simple transistor to obtain a degradation parameter table. The other important problem is the simulation convergence due to the discontinuity of drain current between the different operation regions (subthreshold, linear and saturation). To solve this problem, a more accurate subthreshold current model needs to be introduced. The variations of SPICE level 3 parameters are consistent with the theory, in spite of the difficulty to fit parameters from measurements and the deviation between simulation and measurement results, especially in linear region. These errors could lead to simulation accuracy loss error or over-estimated degradation prediction at circuit level. The weakness in output conductance modeling could introduce inaccuracy of analog circuit simulation.

This study is a first attempt to obtain realistic degraded transistor models to predict the evolution of circuit performances, and especially parasitic emission and susceptibility to electromagnetic interferences. For this preliminary study, even if we have not developed high precision degradation model, we can simulate the trend of the evolution of transistor degradations and thus the evolution of circuit characteristics. In order to improve the accuracy of our models, an investigation about more complicated model such as BSIM4 can be leaded, but at a price of a more complex extraction.

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Chapter 4: Modeling and simulation of EMC level drift induced by ageing

In the previous chapter, we have characterized the hot carrier induced degradations and negative bias temperature instability degradations at transistor level. The experimental results show that the transistor DC characteristic degrades after continuous constant stress. The maximum saturation current and extracted parameters such as threshold voltage and mobility decrease after stress. The variation has power law dependence with the stress time. We successfully model the transistor DC characteristic degradation with SPICE compatible model.

In this chapter, we deal with the prediction of the immunity level degradation after ageing. In Chapter 2, we have proved that circuit aging has a more critical impact on immunity to electromagnetic disturbances than on circuit emission. First, we will propose a simulation flow dedicated to EMR prediction of a circuit. Our approach consists in to embedding the device degradation model into the circuit EMC model. As we are focused on the immunity prediction of a circuit, we will use the modeling approach suggested in the standard proposal ICIM [IEC62433-4]. Then, we will present two different case studies in which the evolution of circuit immunity due to device aging are modeled and simulated. The first case study concerns the DC offset induced by electromagnetic interference coupling on a CMOS 90 nm NMOSFET transistor terminals. The accurate prediction of this effect called EMI-induced DC offset is critical since it is the main source of susceptibility issues in analog circuits. The second case study reuses the phase-locked loop developed in CMOS 0.25 µm and introduced in Chapter 2. Experimental characterizations of its immunity before and after accelerated life test have shown significant variations of susceptibility level over large frequency ranges. After the presentation of the construction of a susceptibility model of the PLL based on ICIM approach, we will use the proposed EMR simulation approach to propose an explanation and reproduce the observed immunity level degradation.

1. ELECTROMAGNETIC ROBUSTNESS SIMULATION

1.1. Development of simulation flow for EMC level drift prediction

The experimental results in Chapter 2 showed that the ageing can affect significantly the circuit EMC level. The conducted emission level decreased while the conducted immunity level fell off after

accelerated ageing tests (such as LTOL or HTOL). The effects on transistor DC characteristic and transistor parameters induced by voltage stresses were analyzed. These degradations can have an impact at circuit level and thus EMC level can be affected. For conducted emission, the reduction of transistor drain saturation current leads to the reduction of dynamic current consumption and the increase of digital gate switching time, which induce a general reduction of the emission level of the circuit. Besides, the increase of threshold voltage and the decrease of the mobility can degrade circuit noise margin and power supply rejection ratio (PSRR), which have direct consequences on circuit immunity to EMI.

In this context, we expect to develop an electromagnetic robustness (EMR) model to predict the variation of circuit EMC level induced by aging in design level. The preliminary prediction model relies on:

- EMC model: an EMC model that could reproduce the circuit immunity to EMI/emission of interference in a given frequency range. In our study case, we are focused on the frequency range [150 KHz – 1 GHz] targeted by EMC standard related to ICs (IEC 62132 -4 [IEC 62132-4] and IEC 61967 [IEC 61967]).
- Circuit reliability model: In our study, we focus on the impact of ageing on integrated circuit: regardless the impact of ageing on printed circuit board and associated passive components (in particular decoupling capacitors, ferrites) and the chip package. The circuit reliability model which can reproduce evolution of the characteristics of the circuit.

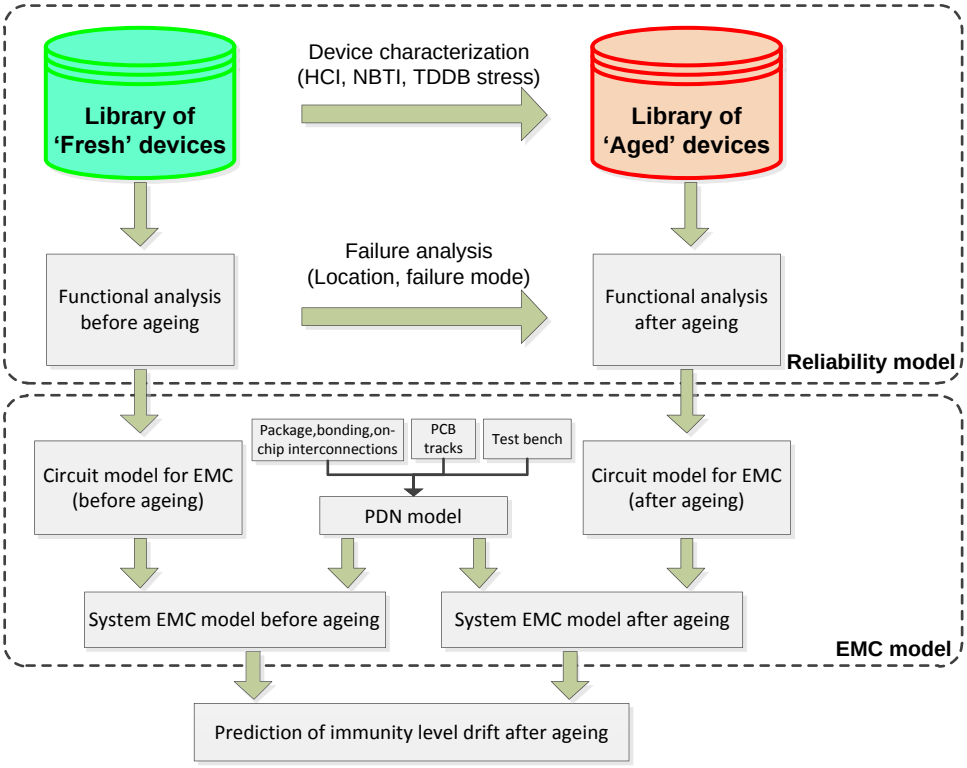

Figure IV-1: Long term immunity prediction simulation flow

Figure IV-1 illustrates the proposed methodology to simulate the circuit immunity degradation induced by ageing.

As in the first section of chapter 3, device library for "fresh" and "aged" transistor can be extracted by device characterization before and after different type of ageing, which are hot carrier injection effect on NMOS and negative bias temperature instability effect on PMOS. The failure model could be a SPICE compact model with modified parameters or a failure equivalent circuit model (described in Chapter 1).

The second step aims at identifying the critical transistors in the circuit (location and activated failure mechanisms) by the analysis of the voltage at transistor terminals. The circuit reliability model is created by incorporating the corresponding transistor failure models into circuit and substituting the identified transistors with failure models. The schematic of the actual circuit is preserved in the model.

In the third step, the EMC blocks are created for fresh and aged circuit. The EMC models are the internal activity model for emission and immunity behavioral model for immunity respectively. They could be a structure model which is the same with the reliability model, or could use a behavior model to reproduce the EMC behavior of a circuit. The emission model could be a current source which can well reproduce circuit internal activity. While for immunity, the immunity model could be a sensitivity table of injection disturbance voltage which induces circuit fail and the disturbance frequency. By combination with PDN model of the whole system: package passive element, bonding, on chip interconnections, PCB tracks and test bench, the system EMC models are generated and variation of EMC can be extracted from the comparison the two EMC models simulation results.

1.2. Description of EMC simulation flow

1.2.1. Flow of emission simulation

The ICEM model [IEC62433-2] could be used to model circuit conducted emission, as explained in Chapter 1 (section 2.3.1.2). It consists of two main blocks: internal activity (IA) and passive distribution network (PDN). The internal activity block models the switching noise produced byone or several blocks of a circuit. The passive distribution network presents the characteristics of the propagation paths of electromagnetic noise from the source block to the measurement instruments (oscilloscope or spectrum analyzer).

The simulation steps for simulation conducted emission under IC-EMC are described in Figure IV-2-left. IC-EMC is a software developed by E. SICARD and A. BOYER in our lab [SICA09]. It is dedicated to simulate the parasitic emission and susceptibility of ICs and ease the comparison with measurements. IC-EMC is based on SPICE simulation using the freeware WinSpice derived from

SPICE Berkeley for analog simulation. The flow of simulation can also be implemented under other simulation environment such as ADS (advanced design system) from Agilent.

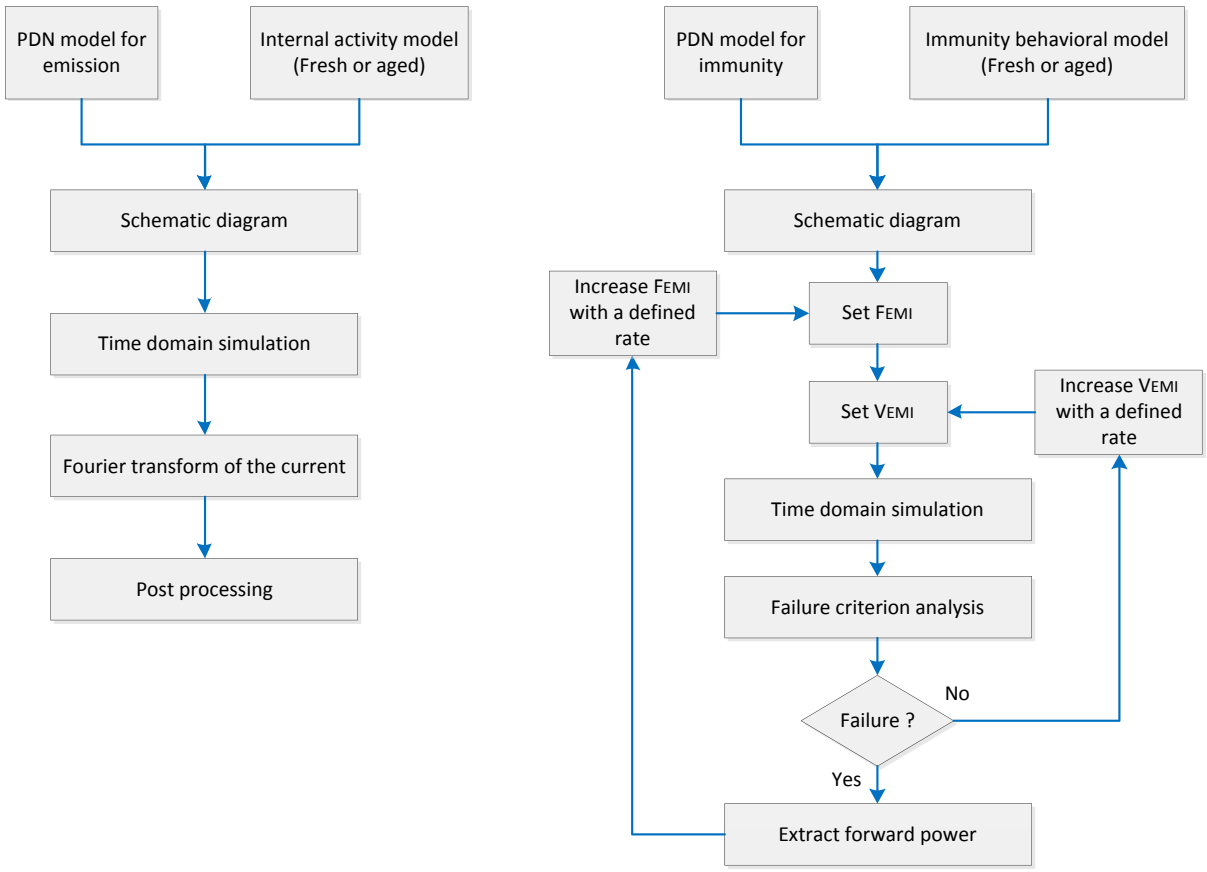

Figure IV-2: Simulation flow of EMC model: (left) emission simulation with ICEM and (right) immunity simulation with ICIM model;

With SPICE simulator, the circuit is simulated in time domain to get its current and voltage variations which are converted into frequency domain by fast Fourier transform since the emission measurement are traditionally performed in frequency domain.

1.2.2. Flow of immunity simulation

The ICIM model [IEC62433-4] is used to model circuit conducted immunity, as described in Chapter 1 (section 2.3.1.3). It includes two parts: immunity behavioral (IB) block and passive distribution network (PDN). The immunity behavioral describes the response of one or several blocks of a circuit disturbed by an incoming EMI. The passive distribution network describes the coupling path of the EMI to the sensitive nodes of the block under test.

The general flow used to simulate circuit susceptibility to a harmonic RFI is described in Figure IV-2-right. The susceptibility simulation is based on an iterative process with a varying frequency. For each frequency point, the time domain simulation under SPICE simulator is taken to extract the amplitude of voltage fluctuation coupled on the sensitive nodes of the block under test. The amplitude

of the disturbance is increased until one of the susceptibility criteria reaches a defined limit. The susceptibility criterion is consistent with the measurement susceptibility criterion.

2. CASE STUDY 1: MODEL OF THE IMPACT OF HCI TO THE EMI-INDUCED DC SHIFT IN NMOS TRANSISTOR.

2.1. Case study description

In the previous section, we explained the flow for EMC level drift prediction. The first case study is focused on the impact of HCI on the EMI-induced DC shift at transistor level.

A typical failure source of analog circuits (differential pair, common source output, bandgap voltage reference, voltage regulator…) exposed to EMI is linked to EMI induced offsets [REDO09] [FIOR02]. Due to their nonlinear characteristics, transistors rectify the voltage fluctuations produced by EMI coupling on their terminals, resulting in DC shifts that affect circuit operation points and performance degradations. An example of DC shift in nonlinear device, a diode connected NMOS transistor is illustrated in Figure IV-3, the average of V_{D0} shifts downward owing to the EMI AC current superposed on DC of I_{IN}.

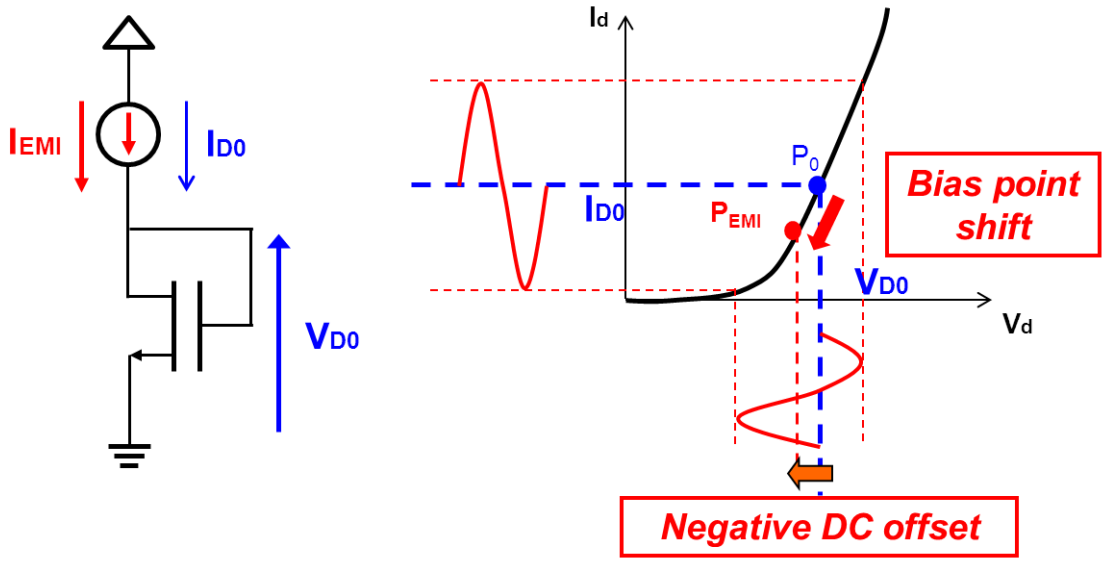

Figure IV-3: DC shift in the diode connected NMOS transistor.

In the case study 1, the device under test is a 90nm NMOS transistor with aspect ratio (W=10µm and L=1.52µm). A harmonic disturbance is coupled on the terminals of NMOS transistor and the drift of the average drain current for different voltage fluctuation amplitudes is measured. The test set-up is described in Figure IV-4:

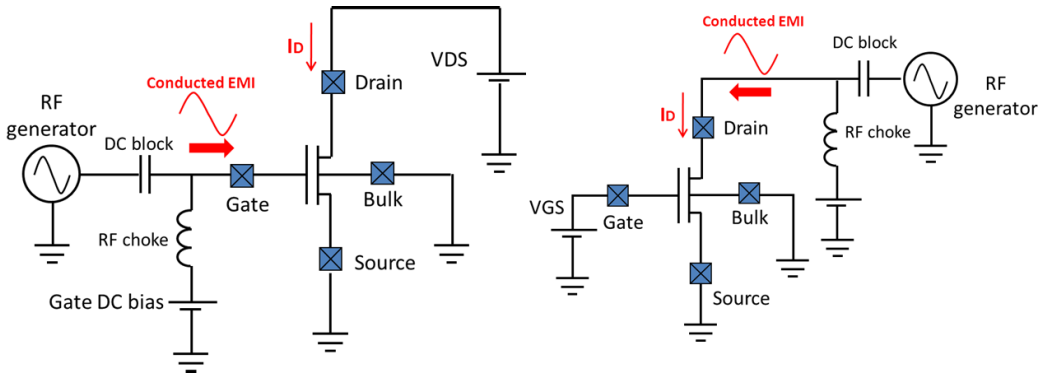

Figure IV-4: Test set-up used to measure EMI-induced DC shift on drain current for conduced injection on gate (left) and on drain (right)

The RF interference is superposed on the DC bias signal by a decoupling network (to prevent RF disturbances to flow into DC supply) and coupled to the NMOS transistor terminals: gate or drain. The interference is a sinusoidal signal generated by a RF signal synthesizer. The mean drain current I_{DS}, is measured by a DC current meter with 100nA accuracy. The bulk and source of the NMOS are connected to the ground. After immunity test, the NMOS transistor is submitted to voltage stress to accelerate HCI degradation mechanism, defined in the section 2.2.1 of Chapter 3. After 4500s stress, the same immunity measurement was done and the measurement results are compared with the simulated with Nth power law model [LI11].

2.2. Model of NMOS transistor before and after HCI stress

After HCI stress, the I_{DS} vs. V_{DS} curve was characterized once again as before stress. The nth power law model parameters are extracted from the measurement for fresh and aged component. They are listed in Table IV-1,

	λ	V_{TH}	n	B	m	K
Fresh	0.031	0,84	1,503	0,00052	0,894	0,997
Stress after 1500s	0.047	1.01	1,503	0.00042	0.772	0.951
Variation	+53%	+20%	+1%	-20%	-14%	-4%

Table IV-1: The key variation of parameters obtained for the fitting of the experimental data for DUT before and after stress

The transconductance (B) is reduced about 20%. Meanwhile the threshold voltage (V_{TH}) and the channel length modulation (λ) are increased about 20% and 53% respectively.

The comparisons between measurement and model simulation for fresh and stressed components are shown in Figure IV-5 and Figure IV-6. After 4500 seconds of HCI stress NMOS's IV curve has significantly changed due to obvious degradation induced by oxide interface state generation at the peak substrate current bias condition [FANG98] [GROE95].

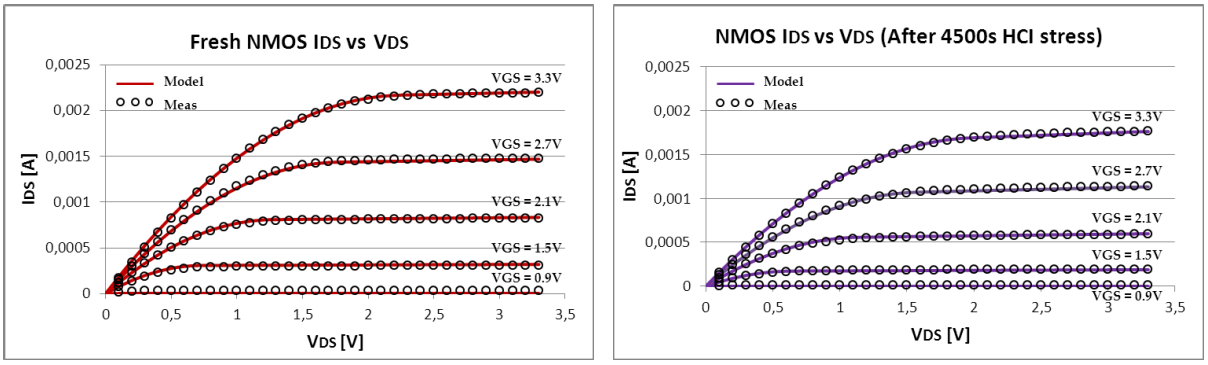

Figure IV-5: Comparison between simulation and measurement of I_{DS} vs. V_{DS} curve: before HCI stress (left) and after HCI stress (right)

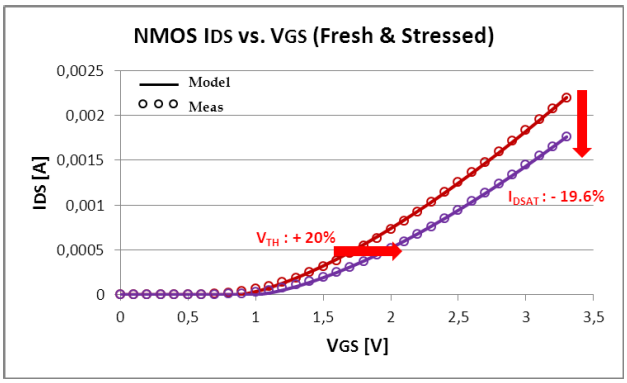

Figure IV-6: Comparison of measured and simulated of I_{DS} vs. V_{GS} curve (V_{DS}=3.3V) for fresh and stressed NMOS

2.3. Measurement and simulation of EMI induced DC offsets

2.3.1. EMI coupling on NMOSFET gate

We apply on the gate of NMOS a set of harmonic voltage fluctuations at 1MHz with different amplitudes (V_{EMI}) ranging from 0.5V to 0.7V. These voltage fluctuations simulate the coupling of an EMI on the transistor terminal. V_{GS} is biased at 2.1V. With this disturbance, the average drain current I_{DS} is measured before and after the HCI stress. The EMI-induced DC shift is extracted by computing the difference between average drain current with and without EMI. Figure IV-7-right presents the variation of the EMI induced DC shift vs. V_{DS} for different voltage fluctuation amplitude V_{EMI}. The variation of drain current depends on transistor regime and increases with EMI amplitude. The EMI coupling on the gate with an amplitude of 0.7V induces a DC offsets on drain current which reach 45µA, i.e. 8% of the drain current measured without EMI.

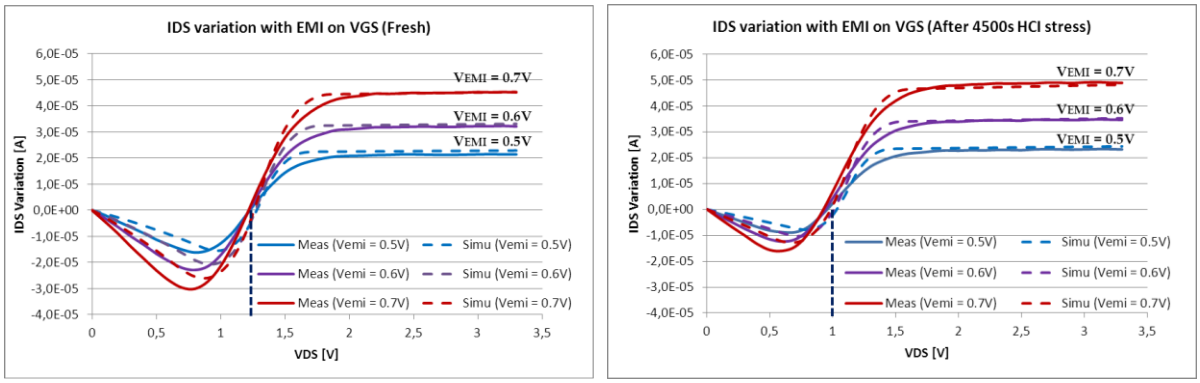

Figure IV-7: Comparison of simulation and measurement of the evolution of the average drain current I_{DS} when an EMI is applied on the gate of fresh (left) and stressed NMOSFET (right)

The same measurement was done after HCI stress. The comparisons between simulation and measurement for fresh and aged component were shown in Figure IV-7. The simulation reproduces the right trend of the variation of the EMI-induced offset.

After HCI stress, with the same EMI amount, stressed component has a large DC drift than fresh one in the saturation regime, while the DC offset is reduced in linear regime. This trend is confirmed by simulation. In linear regime, the maximum DC offset varies from -29.7µA to -16 µA, i.e. a decrease of 47% after HCI stress. This is mainly due to the reduction of 20% of the mobility. In saturation regime, the maximum DC offset varies from 45 µA to 50 µA, i.e. an increase of 11% of EMI induced DC offset on I_{DS}, linked to the increase of 53% of the parameter λ. By comparison of average drain current offset vs. drain source voltage curves shown in Figure IV-7-left and right, the saturation voltage shifts from 1.23V to 1.02V, due to the augmentation of threshold voltage and reduction of m and K.

2.3.2. EMI coupling on NMOSFET drain

We apply on the drain of NMOS a set of harmonic voltage fluctuations at 1MHz with different amplitudes (V_{EMI}) ranging from 0.5V to 0.7V. These voltage fluctuations simulate the coupling of an EMI on the transistor terminal. The drain is biased at 2.1V. The previous procedure is reused to measure the EMI-induced DC offset. Figure IV-8-left presents the EMI-induced DC shift before HCI stress.

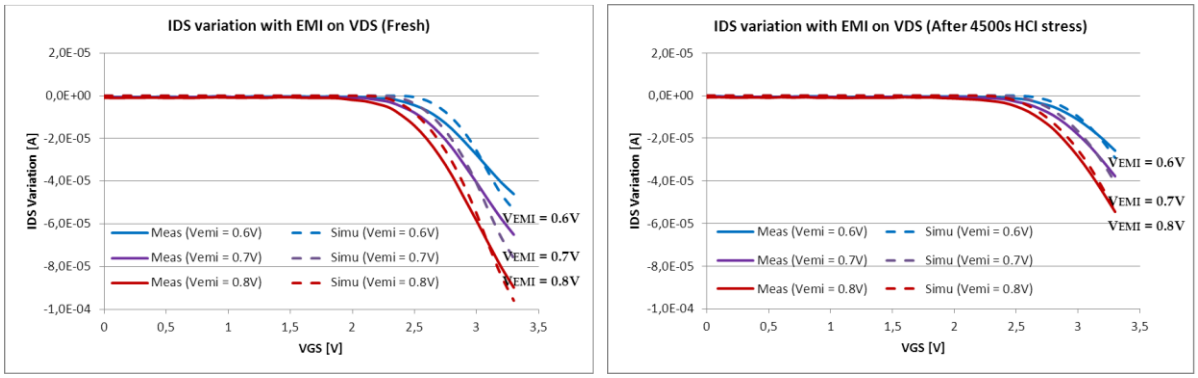

Figure IV-8: Comparison of simulation and measurement of the evolution of the average drain current I_{DS} when an EMI is applied on the drain of fresh (left) and stressed NMOSFET (right)

The same measurement was done after stress test. The comparison between simulation and measurement for fresh and stressed component is shown in Figure IV-8. EMI induced DC offsets appear for both linear and saturation regimes, and become obvious when $V_{GS} > V_{DS}$. It can be explained by the reduction of mobility and increase of threshold voltage V_{TH}. When $V_{GD} > 0$, the effect of channel modulation is reduced, and thus the role of increase of λ is weakened. The absolute value of the DC offset increases with the EMI amplitude. Conversely to EMI injection on gate, the DC offset induced by EMI coupling on the drain varies from -89.9 µA to -54.5 µA, i.e. a decrease of 39.3% of EMI induced DC offset on transistor drain current.

In the first case study, we focus on the DC offset induced by EMI coupling on transistor terminal, and its evolution after transistor degradation (e.g. due to hot carrier injection). The experimental results have shown that EMI-induced DC shifts can change after device degradations: the drain current shift is reduced in both linear and saturation regimes when EMI coupling on the drain. When the gate is exposed to EMI, the drain current is decreased in linear regime, while it is enhanced in saturation regime.

3. CASE STUDY 2: MODELING OF PLL IMMUNITY DRIFT INDUCED BY AGEING

3.1. Case study description

3.1.1. Phase-locked-loop in MIXITY test chip

In chapter 2, we described the conducted immunity method (DPI) that we used for immunity characterization and briefly introduced the test vehicle called MIXITY. The test chip contains several types of analog and digital blocks and their conducted immunity has been characterized before and after a HTOL accelerated life test. Among the different blocks, the PLL shows the worst degradation (a

decrease of 10 dB of the immunity level observed for some components). In this part, we use the PLL as case study to create an EMR model and try to explain qualitatively the origin of immunity level drift observed experimentally.

The PLL is embedded in a test chip developed in 0.25 µm technology. Figure IV-9 presents the PLL schematic, it is based on a first order filter, and consists of three sub-blocks: phase detector (PH), voltage-controlled oscillator (VCO) and frequency divider (DIV) which have separated power supply pairs.

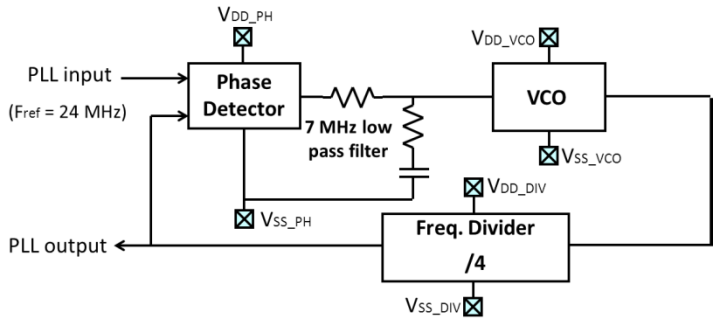

Figure IV-9: Schematic of the PLL. The three sub-blocks: Phase detector, VCO, and frequency divider have separated power supply pairs.

The VCO is a delay controlled ring oscillator, designed to operate nominally at 112MHz (Figure IV-10), the frequency divider divides by 4 the VCO output signal frequency. In the following test, the reference signal applied on PLL input has a frequency of 24 MHz.

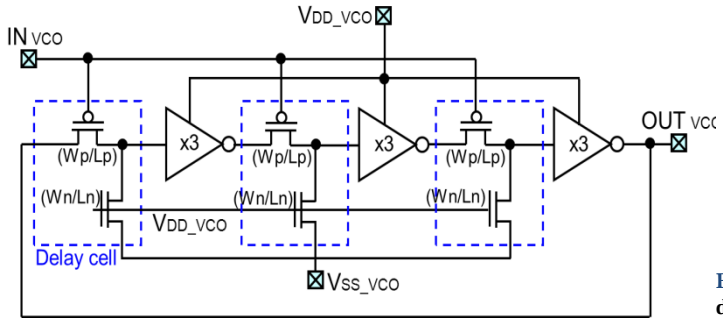

Figure IV-10: Transistor level schematic of the delay controlled VCO

The PLL power distribution network is unconventional but the separation of power supplies of each sub-block has been chosen to characterize internal coupling between different power supply domains and identify the role of each sub-block in the PLL susceptibility. The different power supply pairs are written V_{DD_VCO}/V_{SS_VCO} for the VCO, V_{DD_PH}/V_{SS_PH} for the phase detector, and V_{DD_DIV}/V_{SS_DIV} for the frequency divider.

3.1.2. Characterization of PLL immunity

The experimental results of the three sub-blocks' immunity are compared by applying DPI on VCO, phase detector or frequency divider power supply rails. The test set-up is described in Chapter 2, and the immunity levels measured in these 3 blocks performed on the same component are compared in Figure IV-11.

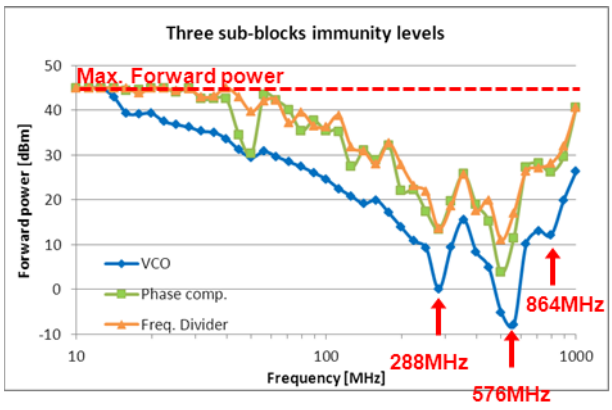

Figure IV-11: Conducted immunity of the PLL: injection on VCO, phase comparator and frequency divider power supply pins

While the immunity levels of phase comparator and frequency divider are similar, the immunity of VCO is 10 to 15dB lower. This difference demonstrates that the most sensitive situation of PLL is when the conducted disturbance is applied on the VCO power supply. Our study will be only focused on conducted injection on VCO power supply pin.

Two failure types are detected during DPI tests performed on VCO power rail:

- Jitter related failure: the period jitter exceeds 2ns (arbitrary criterion which corresponds to a deviation of 5 % of the PLL output signal frequency). This failure occurs at low frequency (< 100MHz) where the VCO is very sensitive to VCO power supply fluctuations, but also at particular frequency points: 288MHz, 576MHz and 864MHz which are respectively the 3rd, 6th , and 9th harmonics of the VCO operating frequency (96MHz). It can be explained by the synchronization of oscillation frequency to aggression noise frequency phenomena of oscillator [DUBO09]. The multiple of 3 is due to VCO structure which contains 3 delay cells. The duty cycle of VCO output oscillation frequency is not equal to 50%, but nearly equal to 33% [BOYE11]. In this configuration, the VCO can be locked on a parasitic signal with a frequency close to three times the VCO oscillation frequency.
- PLL unlocking failure: the PLL unlocks directly without a large increase of jitter. This kind of failure occurs at high frequency (above 100MHz), the variation of VCO phase is enough large to exceed the capture range of PLL which is related to the output voltage range of phase detector and the operating frequency range of VCO.

The immunity threshold of the PLL depends on three parameters:

- Board decoupling, which is the most efficient around 10MHz.
- Circuit passive decoupling network, which affects noise propagation within the circuit. The lowest immunity level is measured over the range 400-800 MHz because of the primary resonance of the VCO PDN, which induces an efficient transfer of noise on VCO power supply.
- The VCO and PLL behaviors, for example, in low frequency, the VCO converts efficiently the power supply voltage fluctuation into jitter.

3.1.3. Variation of the immunity level of VCO induced by accelerated ageing

In Chapter 2, we have shown that the VCO immunity level decreased after 408 hours HTOL accelerate test. The statistical analysis showed that there is an average reduction of immunity (ΔM, in section 1.2.2) of -2.57dB over the whole frequency range and a large standard deviation with 3.64dB. The worst case happened in sample 6, in which the immunity level largely fall off after ageing, the maximum reduction is -10.3dB. This leads to a higher sensitivity to voltage fluctuations induced on VCO power supply. The standard deviation (3.64dB) in statistical analysis demonstrates that a dispersion of the immunity variation exists after ageing. All the samples do not follow the same evolution during the ageing, as shown in Figure IV-12. Immunity average variations larger than 2 dB have been measured on half of the samples, while the other samples have less reduction. A slight improvement of the immunity level has been observed on only one sample.

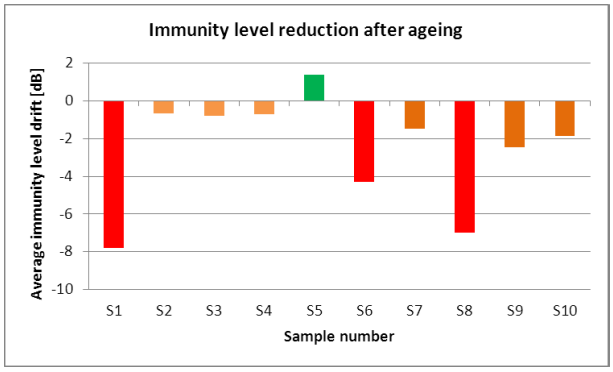

Figure IV-12: Average variation of the immunity level measured per sample

The reduction of the immunity level of the VCO in PLL can be correlated to the reduction of the free running oscillation frequency, shown in Figure IV-13.

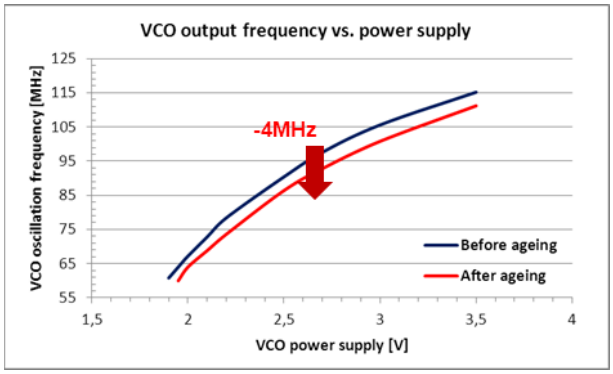

Figure IV-13: Reduction of the VCO free running oscillation frequency of the VCO observed after aging.

This reduction is linked to the alteration of VCO characteristics induced by intrinsic degradation mechanisms, which have been accelerated during the aging test. They have contributed to slow down the VCO and consequently the locking range of the PLL. In order to verify the influence of aging on the PLL characteristics, we have done the following measurement before and after accelerated aging test: a 24 MHz clock signal is applied on the input of the PLL and the power supply voltage is changed. As the VCO frequency range depends on the power supply voltage, the measurement of the

power supply voltage range on which the PLL is locked provides information about the characteristics of the PLL. Figure IV-14 presents the evolution of the power supply voltage locking range before and after aging.

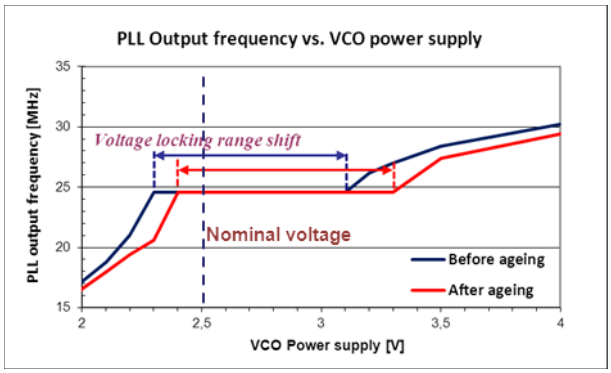

Figure IV-14: Measurement of the power supply voltage locking range before and after aging voltage before and after aging

The comparison shows that after ageing, the PLL power supply voltage locking range shifts towards right. It means that the power supply voltage has to be increased to compensate the slowing down on the VCO induced by internal degradations. In nominal operation conditions, the degradation induced by ageing are not enough large to lead to PLL failure, since the PLL is still locked on 24 MHz when the power supply voltage is equal to 2.5 V. However they have seriously narrowed the margin to voltage fluctuations and decreased the immunity of the PLL to EMI.

3.2. PLL immunity model construction

3.2.1. Construction of PDN block and test environment model

3.2.1.1. Interference source and directional coupler modeling

The first part of the immunity model is the source of EMI. We consider harmonic source produced by the combination of a signal synthesizer and a power RF amplifier. This RF source is modeled by a Radio-frequency interference (RFI) source [IC-EMC]. It consists of an alternating current (AC) source and a default 50Ω output resistance, as illustrated in Figure IV-15-right. The RFI source generates a sinusoidal wave with a programmable voltage amplitude increase from V0 to V1 for a given duration T0.

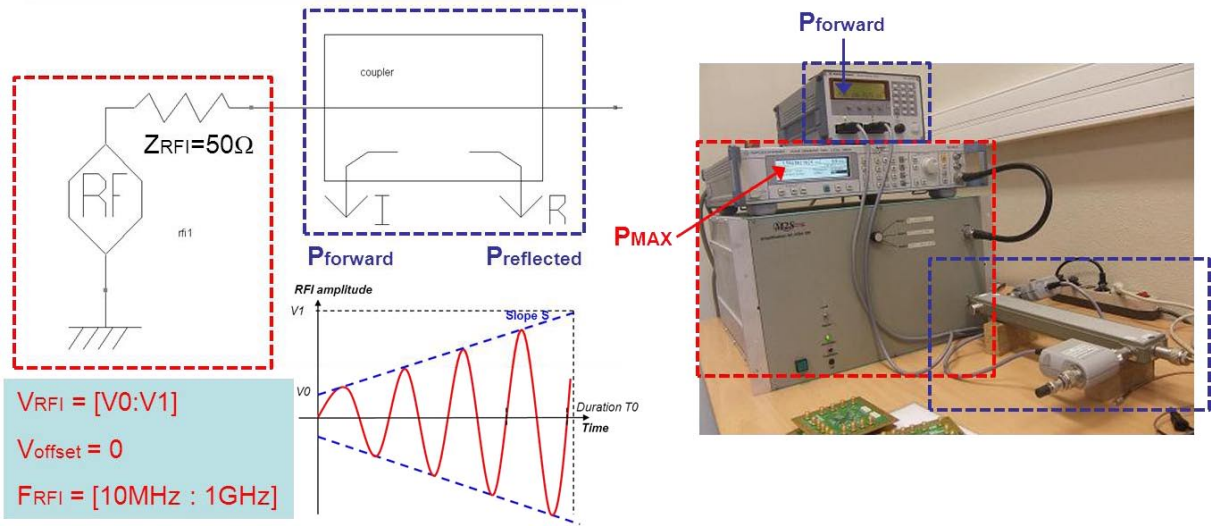

Figure IV-15: Model of the disturbance source and directional coupler which measures the injection power: the RF source and coupler model (left) and corresponding test set-up (right)

The power displays in signal generator is the RMS value of the maximum available power which is computed by Equation IV-1 and Equation IV-2.

$$P_{MAX} = \frac{{V_{RFI}}^2}{4 \times Z_{RFI}} \qquad \text{Equation IV-1}$$

$$P_{MAX}(RMS) = \frac{V_{RFI}^2}{8 \times Z_{RFI}} \qquad \text{Equation IV-2}$$

The directional coupler which is connected between the output of amplifier and the DUT is used to measure the amplitude of the forward reflected wave induced along the transmission line connected between the power amplifier output and the DUT. This device is recommended by the Direct Power Injection standard [standard DPI]. As the mismatch between the load impedance and the characteristic impedance in the transmission line, a part of the forward wave in effectively transmitted to the load whereas the other part of the original wave is reflected and comes back to the source. The power meter is used to convert the forward wave voltage to the forward power with the 50Ω characteristic resistance (Zc). The forward voltage and reflected voltage are computed with the following formulas (Equation IV-3 and Equation IV-4):

$$V_{forward} = \frac{V_{in} + Z_c \times I_{in}}{2} \qquad \text{Equation IV-3}$$

$$V_{reflected} = \frac{V_{in} - Z_c \times I_{in}}{2} \qquad \text{Equation IV-4}$$

Where

$V_{forward}$ is the forward voltage (V)

$V_{reflected}$ is the reflected voltage (V)

V_{in} is the complex voltage at the input of the coupler (V)

I_{in} is the complex current at the input of the coupler (A)

Z_C is the characteristic impedance of the coupler (Ω)

The forward and reflected powers in dBm are computed by Equation IV-5 and Equation IV-6:

$$P_{forward} = 10 \times log\left[\frac{1}{Z_c} \times \left(\left(\frac{real(V_{in}) + Z_c \times real(I_{in})}{2}\right)^2 + \left(\frac{imag(V_{in}) + Z_c \times imag(I_{in})}{2}\right)^2\right)\right] + 30 \quad \text{Equation IV-5}$$

$$P_{reflected} = 10 \times log\left[\frac{1}{Z_c} \times \left(\left(\frac{real(V_{in}) - Z_c \times real(I_{in})}{2}\right)^2 + \left(\frac{imag(V_{in}) - Z_c \times imag(I_{in})}{2}\right)^2\right)\right] + 30 \quad \text{Equation IV-6}$$

Where

$P_{forward}$ is the forward power in dB-milliwatt (dBm)

$P_{reflected}$ is the reflected power in dB-milliwatt (dBm)

The power measured with power meter is a RMS value. For harmonic signal, the conversion can be expressed in Equation IV-7 and Equation IV-8:

$$P_{forward}(RMS) = P_{forward} - 3dB \quad \text{Equation IV-7}$$

$$P_{reflected}(RMS) = P_{reflected} - 3dB \quad \text{Equation IV-8}$$

3.2.1.2. *Injection path modeling*

DPI injection path at board level consists of a bias tee and the PCB tracks connected to the power supply pin of the VCO, as illustrated in Figure IV-16.

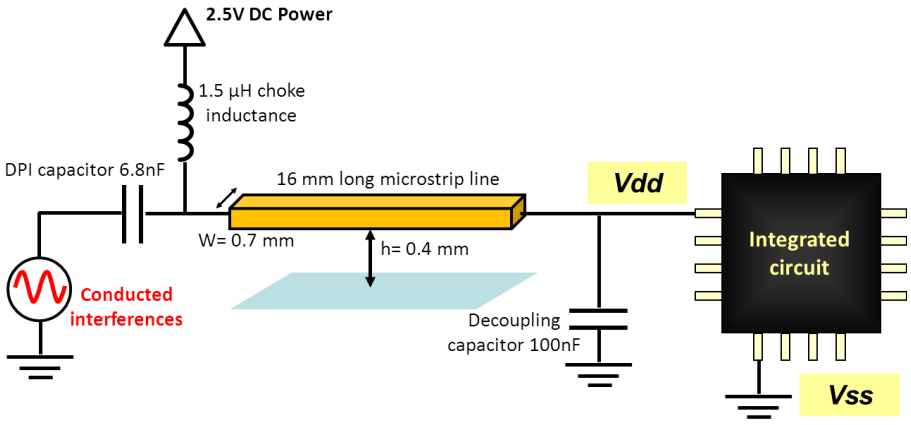

Figure IV-16: Schematic of conducted interference injection path at board level

The bias tee is a decoupling network used to superimpose the high frequency disturbance signal on the DC power supply. It is composed with a 1.5µH choke inductance which isolates the DC power supply source from high frequency signal and a 6.8nF DPI capacitor which cuts low frequency signal.

The DPI capacitor is a X7R ceramic capacitor. ESR (equivalent serial resistor) and ESL (equivalent serial inductance) values are provided by the manufacturer: ESL = 0.6nH and ESR = 0.025Ω. the contribution of the small length of tracks and vias which connect the decoupling capacitor to the power supply and ground planes have to be taken into account as they add non negligible parasitic inductances (about 2.5 nH) which degrade the decoupling efficiency.

The model of the choke inductance is extracted from VNA measurement. The model includes the 1.5µH inductance with a serial resistor (1Ω) and a parallel capacitance (6pF) which take into account the parasitic winding capacitances. This capacitance is required to reproduce the intrinsic resonance of this passive device. In order to reduce the sharpness of the resonance a large parallel resistance Rp (4.5KΩ) is added, which models the loss in the inductor core.

The PCB track is a 16mm long and 0.7mm wide long microstrip line between the output of the Bias tee and the DUT power supply package pin. The PCB track could be modeled with a lumped model which is based on a Π structure of discrete R, L, and C. This approximation is valid in low frequency until the conductor is considered electrically small compared to the wavelength of the considered frequency. The criterion of the length of the conductor is expressed in Equation IV-9:

$$L < \frac{\lambda}{10} = \frac{C}{10 \times \sqrt{\epsilon_r} \times f} \qquad \text{Equation IV-9}$$

Where:

L is length of the conductor

λ is the wavelength

ε_r is the dielectric permittivity

C is the speed of the light

In our case, the model of the 16 mm microstrip line consists of two RLC cells so that it is valid up to 1.5GHz. Figure IV-17 presents the final model of the injection path at board level, including the Bias tee and PCB track.

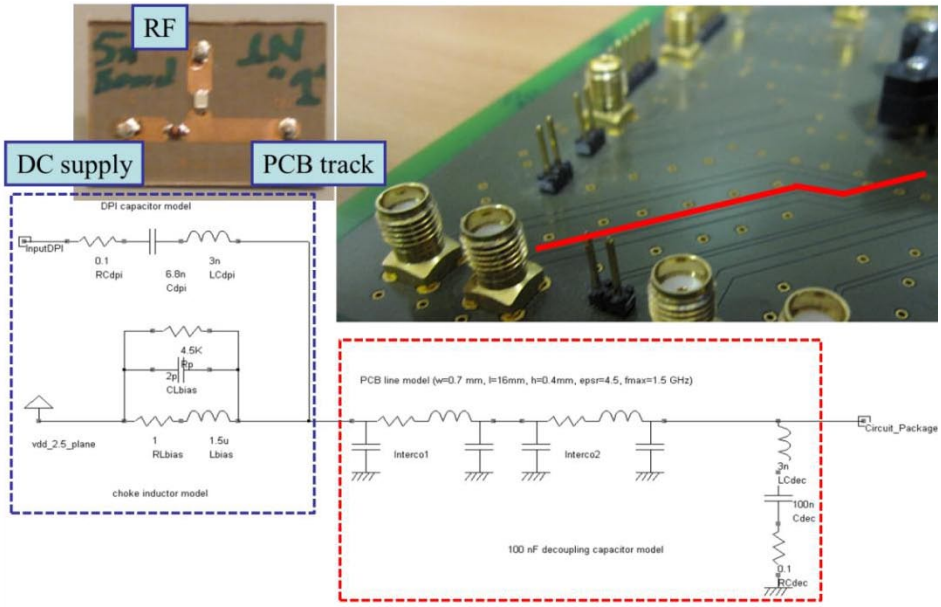

Figure IV-17: Electrical model of conducted interference injection path at board level, including Bias-tee and PCB track

3.2.1.3. PLL PDN modeling by VNA measurements

The PDN of the PLL is made of the power distribution network of the VCO, the phase detector and the frequency divider. It also includes the distribution network of the PLL input/output (I/O). However, PLL and I/O do not share the same the power plane (I/Os are 5V supplied, while the PLL core is 2.5V supplied) and the substrate separation isolate both blocks. As the coupling between the PLL and I/Os power distribution networks is weak, we can ignore the I/O PDN in our case study.

The PDN model of the PLL is an impedance network which links the power and ground pins of the PLL sub-blocks. Each sub-block counts one power supply and one ground pins, thus a total of 6 pins.

A specific test board has been designed to extract the impedance network of the PLL PDN by 2-ports S parameter measurements (Figure IV-18).

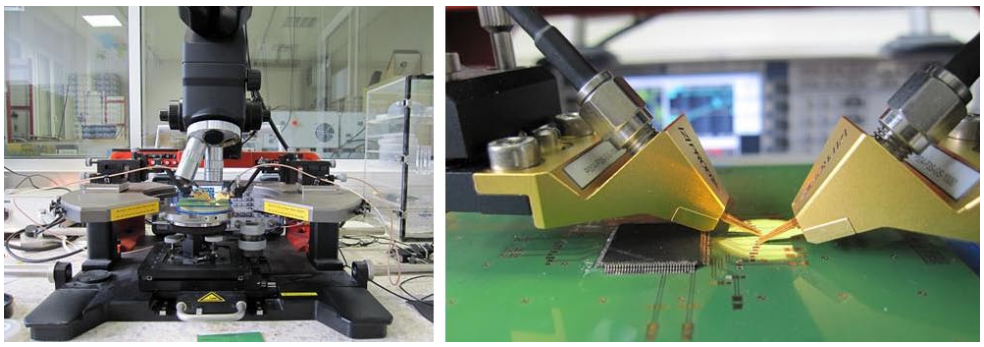

Figure IV-18: PLL PDN model extraction by S parameter measurements: experiment set-up (left) and S parameters are measured with a specific board and GS probes

The circuit is connected to a Vector network analyzer (VNA) by high frequency coplanar GS probes dedicated to RF measurements on printed circuit board up to 4 GHz [ref]. The probes are connected to PCB pads placed as close as possible to the circuit under test pins. The probes can be placed on each pins of the PLL PDN, so package inductances, block equivalent capacitances, substrate coupling… can be extracted from measurements. Moreover, the ground pins can be connected or suspended to the test board ground plane in order to extract the interaction between the die and the test board.

Therefore, a complete characterization of the impedance network that links the power supply and ground pins of the PLL can be done. The PLL PDN includes:

- The coupling between the power and ground rails of the sub-blocks, which is modeled by an impedance written Zi;
- The coupling between the die and PCB grounds which is modeled by an impedance written Zd;
- The bond wire and lead frame model which includes the capacitance to the PCB, Cw, as well as the inductance and resistance, Lw and Rw, associated with the structure.

An example of PDN model structure with two sub-blocks is illustrated in Figure IV-19 [KOO09].

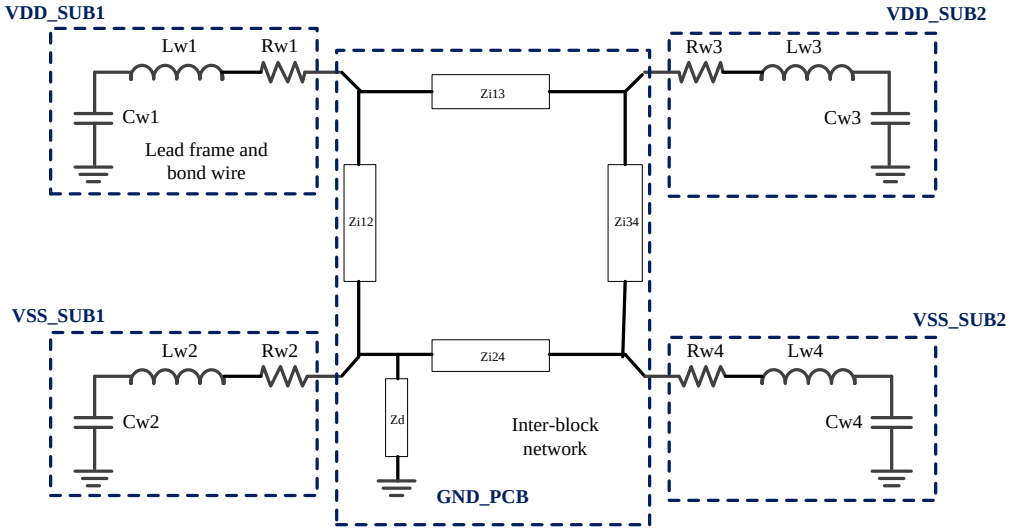

Figure IV-19: PDN model structure example of a circuit with two sub-blocks

A large number of 2 ports measurements have been done between the 6 pins of the PLL PDN. Not all the measurement results will be shown. We take the VCO block as the example to show the PDN modeling process:

- The reflection coefficient S11 measurement on VDD_VCO with all the other VSS are connected to the PCB ground plane allows the extraction of the internal capacitance of the VCO and the serial inductance and resistance of package pins and power supply and ground

interal rails. The input impedance is mainly capacitive due to the equivalent on-chip capacitance of the VCO, as shown in Figure IV-20.

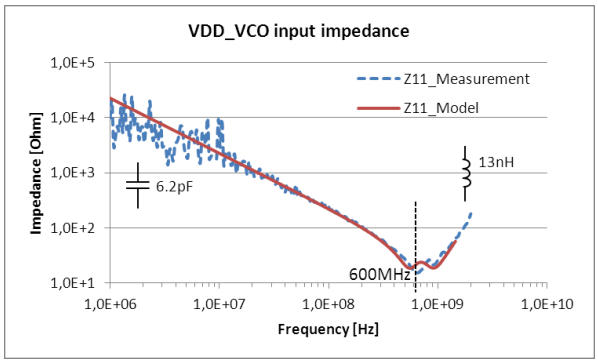

Figure IV-20: Comparison between measured and simulated input impedance to VCO_VDD.

The resonance appears around 600MHz due to the package inductance and the on-chip capacitance of the VCO.

- Although the power supply rails of the different sub-blocks are internally separated, they are not isolated perfectly. A small capacitive coupling appears, as shown in Figure IV-21. S12 transmission coefficient measurements between two power supply pins (VDD_VCO and VDD_PH here) are done. The value of capacitance is fitted to measurement. The model could reproduce well the coupling effect up to 1GHz.

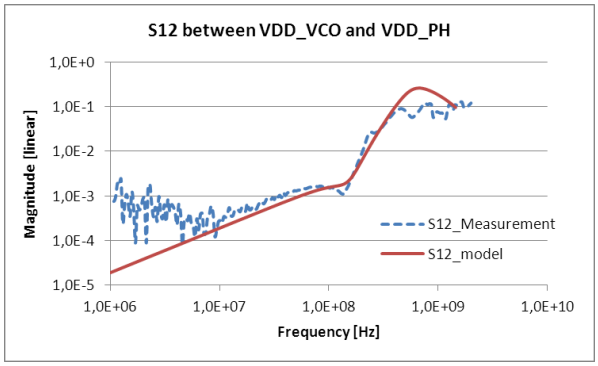

Figure IV-21: Comparison of measured and simulated transmission coefficient S12 between VDD_VCO and VDD_PH

- A capacitance exists between the die and the PCB, which can be estimated by measuring the reflection coefficient S11 seen from the VSS pin, while all the other pins are floating. The S11 parameter is converted to input impedance Z11, as shown in Figure IV-22. The impedance is mainly capacitive in low frequency (before the resonance between this capacitance and package pin inductance).

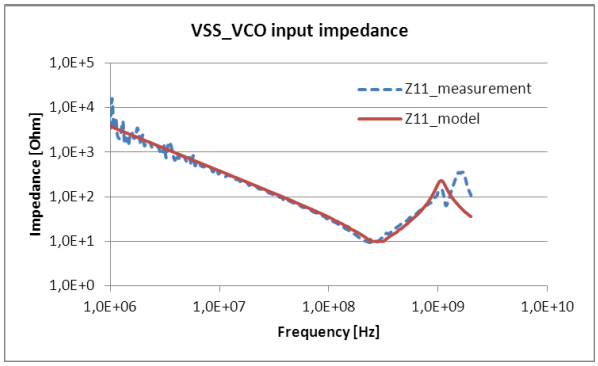

Figure IV-22: Comparison of measured and simulated input impedance of VSS_VCO when all the other pins are floated

- The couplings between the ground pins are also verified, as shown in Figure IV-23(here VSS_VCO and VSS_PH).

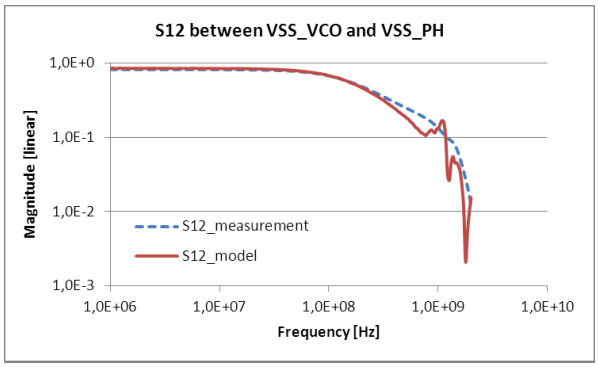

Figure IV-23: Comparison of measured and simulated transmission coefficient S12 between VSS_VCO and VSS_PH

The different ground pins are resistively coupled by the substrate. Between the ground pins of each block, a resistor about 20Ω can be measured with Ohm meter. As these different blocks share the same P+ substrate, a significant substrate coupling exists between their ground connections.

With the same procedure, the PDN of phase detector and frequency divider can be extracted from the S parameter measurement, the electrical elements values are tuned to fit every cross measurements. The complete model of the PDN is shown in Figure IV-24. In the model, the protection elements between the different power supply and ground rails are omitted because they were not triggered during immunity tests. Otherwise, they should be added in the model to take into account the non-linear effects induced by ESD protection activation.

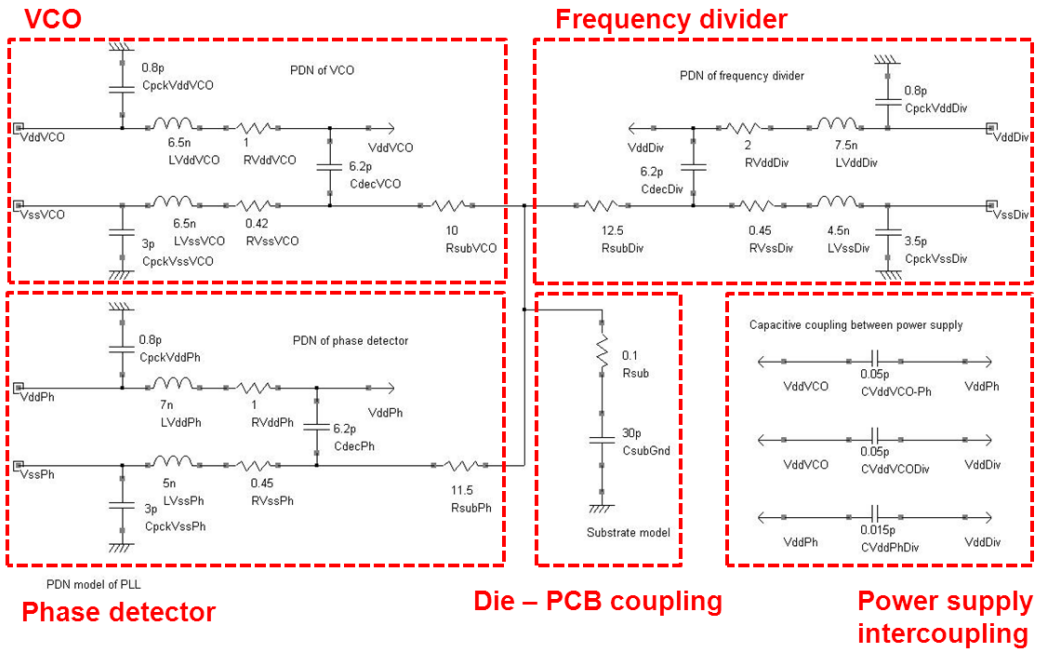

Figure IV-24: Equivalent electrical model of PLL PDN extracted by S parameter measurements

3.2.2. Validation of PDN modeling with the measurement of conducted interference coupling

The model presented in the Figure IV-17 is able to reproduce the impedance profile seen from any terminals of the PLL PDN. It is also important to ensure the model is able to reproduce the coupling of an external conducted disturbance within the circuit. In other words, for a given disturbance amount (i.e. a known forward power at a given frequency when the circuit immunity is tested using a DPI test bench), can the entire model (the PDN model and the test environment model) predict accurately the amplitude of the voltage fluctuation on a specific internal node of the circuit? It is a critical point since immunity of a circuit is directly related to the amount of voltage fluctuation induced across sensitive nodes.

3.2.2.1. Conducted interference coupling transfer function

Since the impedance profile of the PLL PDN is frequency dependent, PLL PDN is equivalent to a filter of the voltage fluctuation induced by the coupling of an EMI. The filtering effect can be expressed by a transfer function that relates the induced voltage fluctuation ΔV to the amount of injected disturbance. In DPI test, the conducted disturbance amount is given in term of forward power P_{forw}. The coupling of the conducted interference is characterized by an "EMI transfer function" H_{EMI} of a given IC internal pin, as expressed in Equation IV-10 [BOYE11]. It is an indicator of the coupling efficiency of the conducted interference on this pin.

$$H_{EMI}(V/W) = \frac{\Delta V}{P_{forw}}$$ Equation IV-10

3.2.2.2. *Measurement of EMI coupling function*

In order to characterize the EMI transfer function of the PLL PDN to conducted injection on VCO power supply, the voltage fluctuation on VDD_VCO induced during DPI test is measured for each injection frequency. The experimental set-up is described in the Figure IV-25. For different frequencies ranging from 1MHz to 1GHz, harmonic disturbances are generated and conducted to the VDD_VCO pin. For each frequency, the forward power of the disturbance is set to induce a certain voltage fluctuation, measured respectively with an internal sensor placed on the VCO power supply rail inside the chip and with active probe connected to an oscilloscope and placed on the VDD_VCO package pin. The bandwidth of the active probe is equal to 2.5 GHz and the sampling frequency of the oscilloscope is 10 G samples/s. The amplitude of the voltage fluctuation should be large enough to ensure an accurate measurement, but not too large to ensure small signal conditions. The amplitude criterion is set to 0.25V.

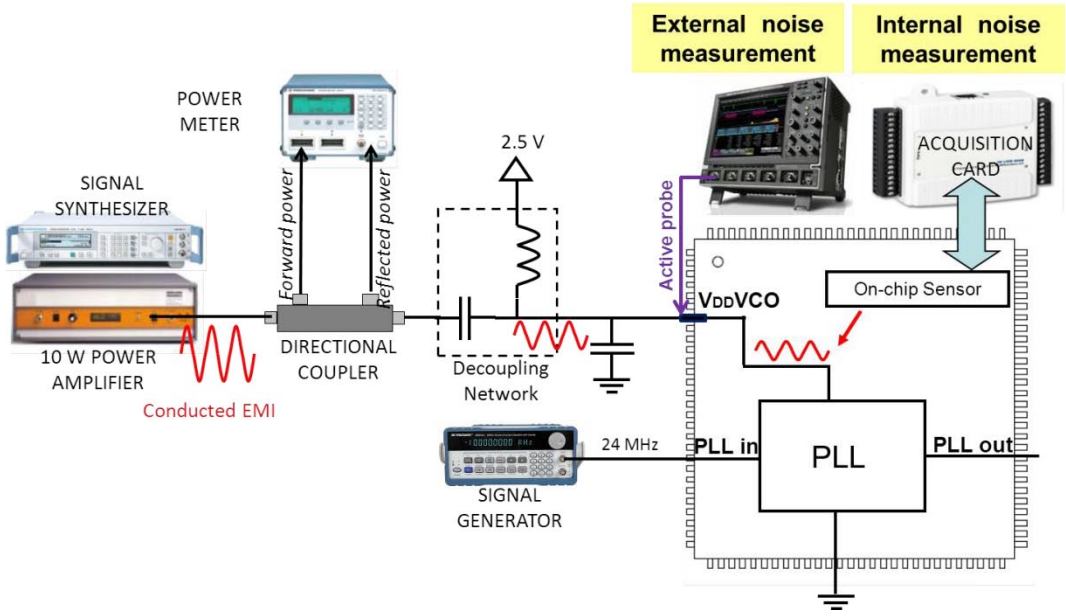

Figure IV-25: Experimental set-up to measure the EMI coupling transfer function [BOYE11]

Three on-chip voltage sensors are placed on the VCO, the phase detector and the divider power supplies in order to characterize external interference coupling within the circuit PDN and extract the actual sensitivity level of each sub-block. The sensor is based on a wideband sample and hold (S/H) cell which works in subsampling conditions and directly probes the voltage on a given internal node without introducing any disturbances (Figure IV-26). The bandwidth of the sensor reaches 2.5GHz [DEOB09] [BEND11]. To prevent from any disturbances of the on-chip sensor operation by external

interferences, the sensor is designed on the isolated substrate, has separated power rails and an internal built-in voltage regulator.

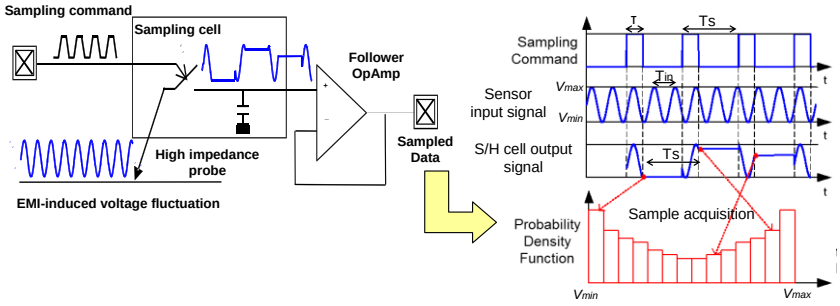

Figure IV-26: On chip voltage sensor and random acquisition of EMI induced voltage fluctuation [Deobarro09]

In our case study, the S/H cell is not synchronized on the external EMI, so the acquisition of the internal voltage fluctuation is randomly preformed and the time domain waveform cannot be reconstructed. But the statistical distribution of the voltage fluctuation, its amplitude and standard deviation can be extracted. If the induced voltage fluctuation remains sinusoidal, it is enough to characterize the peak to peak amplitude of voltage fluctuation induced by the interference coupling.

Figure IV-27 presents the experimental results. The external noise measured with the active probe is compared with the internal noise measured with the on-chip sensor. Ideally, both measurements should give the same result because the same node is probed (VDD_VCO). However, this ideal vision ignores the impedance between the 2 measurement points: package inductance, IC interconnects… which explains the difference observed between both measurements above 100MHz.

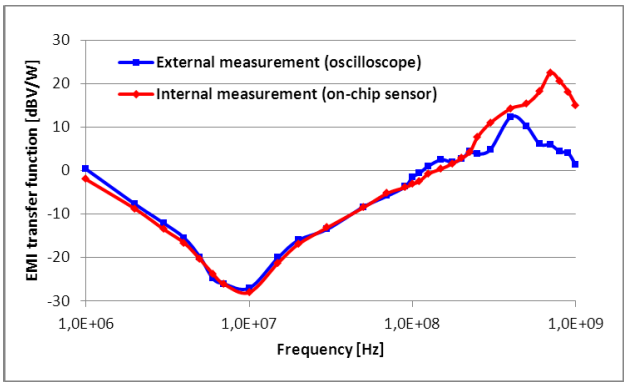

Figure IV-27: Comparison of external and internal EMI transfer function [BOYE11]

3.2.2.3. Simulation of EMI coupling transfer function

In order to simulate the EMI coupling transfer function, the entire model which includes the test environments (DPI injection system, the test board) and circuit PDN is used. A voltage probe placed on the VDD_VCO to monitor the failure criterion which is 0.25V, as illustrated in Figure IV-28.

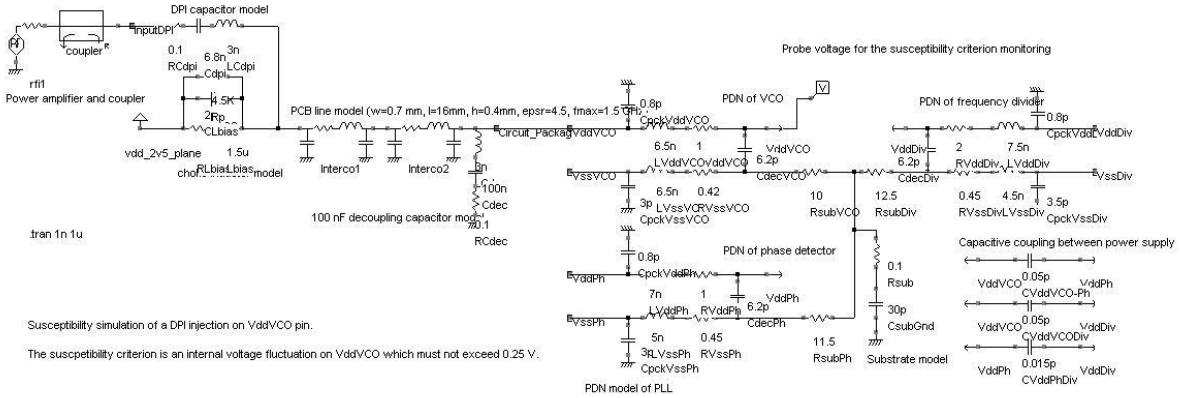

Figure IV-28: Model for the simulation of EMI transfer function

Figure IV-29 presents the comparison of the measured and simulated EMI transfer function of VDD_VCO pin. The excellent agreement demonstrates that the PLL PDN model is able to predict the amount of voltage fluctuation coupled on the VCO power supply up to 1GHz.

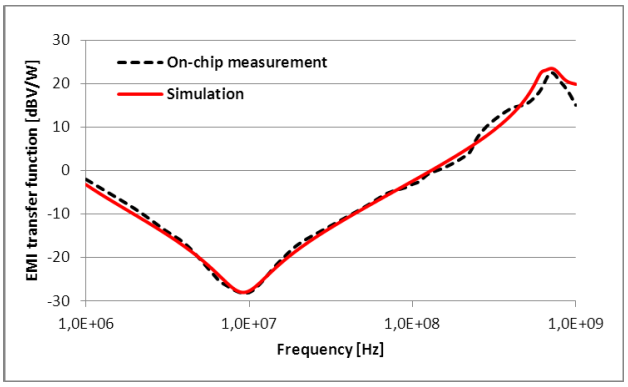

Figure IV-29: Comparison between the on-chip measurement and simulation of the EMI transfer function.

3.2.3. Construction of the IB block

The IB model construction relies on the transient simulation of the transistor level schematic of the PLL for two reasons (The detail of IB model construction will introduce in the 3.3 section):

- Ensuring an accurate modeling of PLL failure mechanisms induced by VCO power supply voltage fluctuation.
- Including transistor degradation mechanisms by changing transistor model parameters.

However, adding the PLL PDN and circuit nearby environment models can increase the simulation time. Parasitic inductances associated to board and package interconnects and decoupling capacitances induce a long transient state. An alternative method is used to overcome this issue: using a two steps simulation in which the IB model and PDN model are simulated separately. First, for different harmonic disturbance frequencies, the PLL model and its PDN are isolated and we search the voltage fluctuation amplitude to be applied on Vdd VCO terminal and to induce a failure. As PLL is

extremely sensitive to VCO power supply voltage fluctuations, the voltage fluctuation amplitude across the VDD_VCO node which could induce circuit failure is gathered for each frequency.

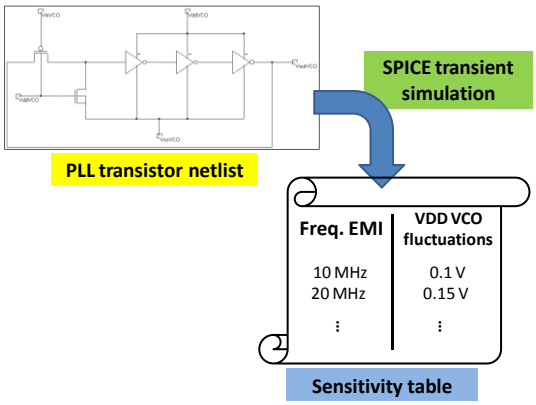

Figure IV-30: Generation of a sensitivity table: sensitivity of the PLL to VCO power supply fluctuations vs. EMI frequency

Then, these voltage amplitudes are recorded in a sensitivity table (Figure IV-30). This table gives for each harmonic disturbance frequency the maximum allowable voltage fluctuation on Vdd VCO. Then in the ICIM model, the IB model is replaced by a simple voltage probe placed on the internal VCO power supply which monitors the voltage fluctuation during the immunity simulation. When this voltage will exceed the limit given by the sensitivity table, a failure is detected in simulation.

3.2.4. PLL immunity model validation

The immunity model of the PLL includes the circuit PDN model, the test environment model and the sensitivity level extracted from the transient simulation of the PLL netlist. Figure IV-31 presents the comparison between the measured and the simulated susceptibility level of the PLL.

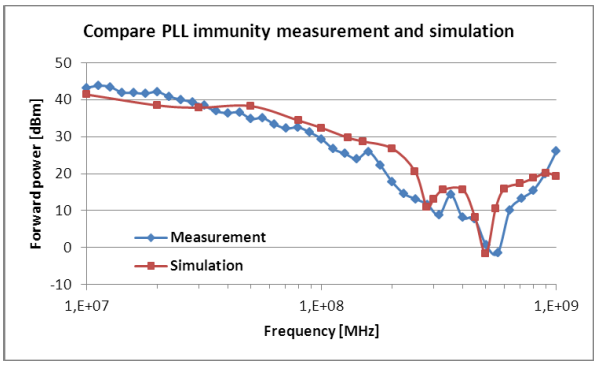

Figure IV-31: Comparison between measured and simulated immunity level of PLL

A good correlation is observed between 10MHz and 1GHz. The efficient EMI filtering around 10MHz, the low immunity between 400 and 800MHz due to the efficient coupling of the conducted disturbance on the VCO power supply, and the susceptibility peaks around 288, 576 and 864 MHz are well reproduced in simulation.

3.3. PLL reliability model construction

During the construction of the SPICE model of the PLL, some simplifications have been done to speed up the simulation. For example, behavioral models have been built for the phase comparator and frequency divider. As the evolution of PLL characteristics after aging is mainly linked to VCO transistor degradations, transistor netlist models are not necessary for the phase comparator and frequency divider. However, the schematic at transistor level of the VCO is reused for its SPICE model.

As explained in Figure IV-1, the flow of long term immunity simulation, a quantitative prediction of the effect of ageing on immunity relies on the identification of the critical transistor and the extraction of variation law for transistor electrical parameters vs. stress conditions and time. In MIXITY study case, for confidentiality reasons, we can't access to the design kit nor characterize simple transistors to obtain the transistor parameter evolution law with certain stress condition and stress time.

To solve the design kit confidential problem, we used a typical SPICE model of 0.25 µm provided by the software Microwind [SICA09]. Then the transistor characteristics have been tuned to obtain a good fit between simulated and measured VCO and PLL performance. . In the previous Chapter (Chapter 3), we have focused on two degradation mechanisms: Negative Bias temperature on PMOS and Hot carrier injection on NMOS. They have significant impacts on circuit performance by modifying transistor parameters: an increase of the threshold voltage, and a decrease the carrier mobility and degradation of drain current. In MIXITY project, despite the lack of information about transistor parameter evolution during ageing, we attempt to use CAD simulation to propose and consolidate assumption about the origins of immunity decrease. With CAD simulation, different scenarios of transistor degradation can be supposed: the location of degraded transistors and device parameters affected by degradation mechanisms can be changed in order to observe the impact of the degradation of specific transistors on the whole circuit immunity.

3.3.1. Failure analysis

In the section 2.1.3, experimental results have shown that the immunity fall off is correlated with VCO slowing down, so the degradation can be located on the transistors which have a major contribution on the VCO oscillation frequency.

Let us consider the ageing impact on the delay in one stage of VCO, which consists in one delay cell and 3 inverters, as illustrated in Figure IV – 32.

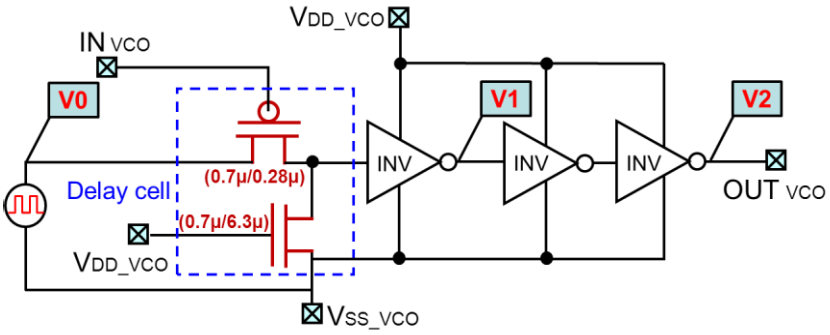

Figure IV-32: Schematic of one stage of VCO which consists in one delay cell and 3 stage inverters

As the VCO oscillation frequency is mainly linked with the delay introduced by the delay cells [BEND98], the variation of the oscillation frequency is certainly due to degradations of the transistors which form the delay cells. We can assume the most likely degradation mechanisms that affect these transistors from a simulation of the voltage conditions across their terminals.

IN_VCO is the output of filter loop. Its amplitude range is comprised between 0.2V and 0.8V. A transient simulation of the circuit shown in Figure IV-32 shows that the PMOS is usually negatively biased respect to the source, thus it is under NBTI stress. The NMOS in the delay cell undergoes an HCI stress because of the positive drain to source bias during the high state level of the oscillation and the high voltage applied to its gate.

The assumption that delay cell transistor degradations have major consequences on VCO oscillation frequency change can be consolidated by the following SPICE simulation. The results of this simulation are shown in Figure IV-33. It consists in simulation the delay introduced by the delay cell for different scenarios of aging.

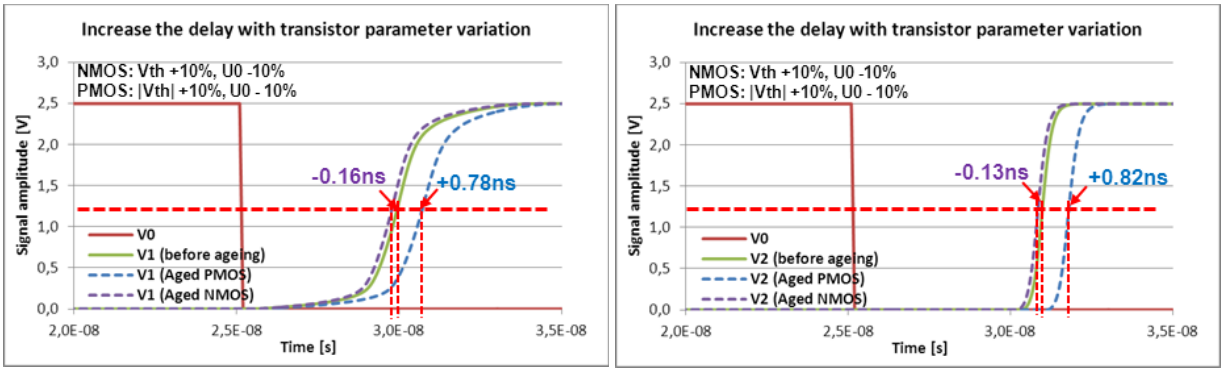

Figure IV-33: Increase the delay with all PMOS parameter variation in one stage VCO: signal after first stage inverter V1 (left) and signal after the third stage inverter V2 (right).

In the simulation, two situations are compared:

- The delay cell and inverter model with the "fresh" transistors
- The delay cell and inverter model with the "aged" transistors. Two cases are compared: 1) the threshold voltage and 2) the mobility of either the NMOS or the PMOS are changed.

The variation consists of an increase of 10% for the threshold voltage and a decrease of 10 % for the mobility. From Figure IV-33, the parameters shift of the PMOS induces a delay variation (+0.78ns) which is nearly 5 times greater than the NMOS degradation effect (-0.16ns). Additionally, the signal after the first stage inverter (V1) and the signal at the output of the third inverter are compared. As the evolution of delay after three inverters remains negligible, the inverters have not a significant contribution to the delay increase. The variations of the parameters of the PMOSFET of the delay cell dominate the VCO oscillation period increase.

Another explanation can consolidate the assumption that the degradations of the NMOSFET of the delay cell can be neglected. Indeed, this transistor has a large channel length. As the degradation of HCI exhibits strong channel length dependence, the large channel length leads to weaker damage [NISH89].

3.3.2. Simulation of the evolution of the immunity level of the PLL

The experimental results in Chapter 3 of the NBTI effect on PMOS exhibited the degradation of drain current. In Chapter 3, the method to characterize the NBTI degradation that we used assumed that only the threshold voltage varies after NBTI stress and the other parameters such as the mobility degradation are not modified. The real situation is that not only the threshold voltage but also the carrier mobility are altered and they may both contribute to the transistor degradation in various degrees. Based on the hypothesis of a degradation localized on the PMOSFET of the delay cell, the effect on the PLL immunity is simulated. Figure IV-34 presents the evolution of the immunity level at 550MHz for different types of degradation: either the threshold voltage VTH is increased, or the carrier mobility U0 is decreased, or both parameters are changed. The amount of relative variation for VTH and/or U0 is marked as X (expressed in percent). In each case, transistor degradations lead to a reduction of the immunity level which reaches up to 6dB, before a complete failure of the PLL in nominal operation (The PLL is unable to lock on a signal with a frequency equal to 24 MHz, even without conducted EMI coupled on VCO power supply). The result shows also that the immunity level drift of the PLL is more sensitive to mobility change.

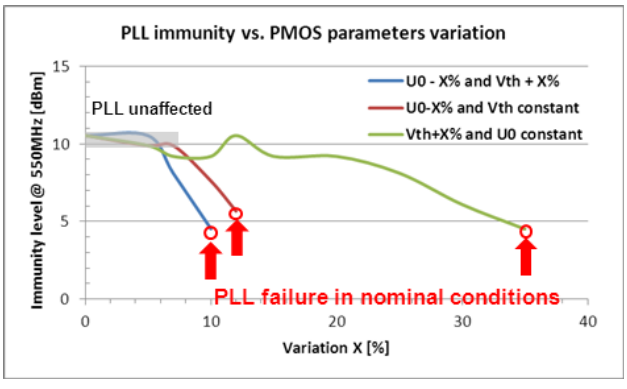

Figure IV-34: Analysis of the sensitivity of the PLL immunity level at 550 MHz vs. variation of threshold voltage and carrier mobility of the delay cell PMOS FET parameters

It is interesting to notice that the reduction of immunity level remains unaffected up to a certain amount of transistor degradation. Above this amount of transistor degradation, the immunity level starts falling rapidly. For example, if the variation of the threshold voltage V_{TH} is less than 8% of its nominal value and if the mobility remains constant, the reduction of immunity level is not significant (less than 1dB). Above 8%, the immunity level reduction reaches up to 5dB before a complete failure of the PLL. This simulation result can be compared to the experimental result presented in the Figure IV-31 which shows the average immunity level variation per sample. The measured immunity levels of the samples exhibit a large dispersion after ageing. The immunity of one half of the samples has not changed significantly while the other half of the samples becomes more susceptible. This simulation result can explain the large dispersion of immunity level measured after ageing. As dispersion process exists between samples and as all the samples are not degraded at the same rate, the deviations of transistor parameters are not identical for all the samples. If this deviation exceeds a given level, the immunity of the sample starts to increase considerably.

A compromise degradation scenario is now considered: the mobility is decreased while the threshold voltage is increased by 10% of their nominal value. Figure IV-35 presents the simulation of the VCO oscillation frequency for different power supply voltage, before and after the degradation of the PMOS transistor of the delay cell. This simulation result can be compared with the measurement result shown in Figure IV-13. In simulation, the degradation of the PMOS transistor of delay cell leads to a reduction of the VCO frequency, which is also observed in measured samples. The amount of frequency drift predicted in simulation depends on the variations of carrier mobility and threshold voltage.

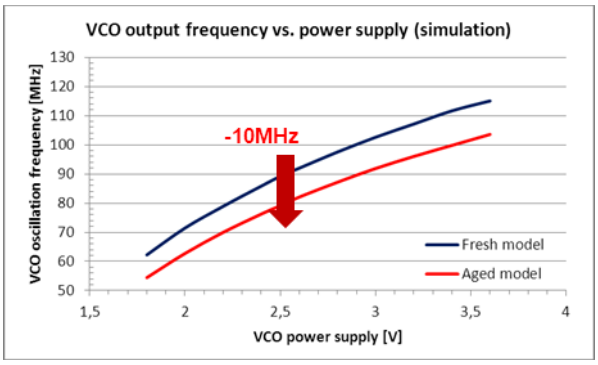

Figure IV-35: VCO oscillation frequency vs. VCO power supply simulation for fresh model and aged model.

The PLL susceptibility level is now simulated between 10MHz and 1GHz with the compromised degradation scenario (mobility is decreased 10% while threshold voltage is increased 10%). Figure IV-36-left presents the comparison between the simulated immunity level of fresh and aged PLL. The simulation predicts a reduction of the PLL immunity over a large frequency range, which is similar to the immunity level decrease observed in measurement (Figure IV-36-right)

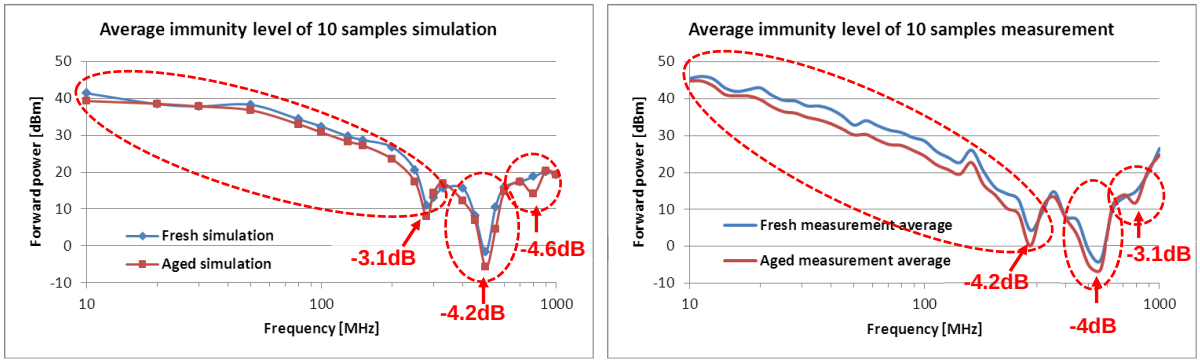

Figure IV-36: Comparison of PLL reliability model simulation and measurement: PLL reliability model simulation for fresh and aged model (left) and average of immunity level for 10 samples measurement before and after ageing (right).

The simulation succeeds in predicting the reduction of the immunity level over three frequency ranges (inside the red dashed circle, in Figure IV-36). The average reduction of the simulated immunity level over the range 10 – 1000 MHz is about 1.7dB while the measured reduction is about 2.6dB. In the frequency range of 10MHz to 200MHz, the simulation drift is less than the measured result. The difference is explained by the lack of accurate information about the actual degradation mechanisms which arise within the VCO. However, the proposed model reproduces qualitatively the evolution of the immunity level of the PLL to conducted disturbance and confirms that transistor intrinsic degradation mechanisms can lead to significant change of susceptibility of a circuit.

4. CONCLUSION AND DISCUSSION

In this chapter, we firstly introduced the methodology of EMR (electromagnetic robustness) modeling and simulation which aims at predicting the EMC level drift of a circuit caused by device ageing. Two case studies have been presented and analyzed in order to predict the immunity level drift induced by circuit aging with EMR model simulation.

The first case study concerns the prediction of the evolution of EMI-induced DC offset of simple NMOSFET which undergoes HCI stress. DC-induced offset is a typican failure mechanism in analog circuits disturbed by EMI. Measurements of conducted injection made on the gate and the drain of the NMOS transistor have shown that the EMI-induced DC offset evolves after the aging. The variation of EM-induced DC offset caused by ageing have been simulated with a nth power law model, which is able to predict both the amount of EMI-induced DC offset and its evolution according to transistor parameter changes..

In the second case study, we have successfully predicted the impact of circuit ageing on conducted immunity of an entire circuit. By applying the EMR modeling methodology, we can model and explain the variation of the immunity level of a phase-locked loop measured after an accelerated-life test. The EMC model of the PLL has been developed to simulate the immunity level of the PLL to

conducted disturbances coupled on the VCO power supply pin. During the circuit reliability model creation, some hypotheses have been proposed about the location and the type of intrinsic degradation mechanisms. The degradation of carrier mobility and threshold voltage of the PMOS transistor in the VCO delay cell due to NBTI failure mechanism can slow down the VCO, modify the VCO free running frequency and thus decrease the immunity margin of the PLL to conducted disturbances. With the introduction of transistor reliability model into the EMC model of the PLL, a similar reduction of immunity level as the one observed experimentally has been simulated. The simulation results have confirmed that the immunity level of the PLL is sensitive to the parameter variation of its constituting transistors. Moreover, the simulation results have also shown that different combinations of parameter variation can lead to large difference in term of immunity level change. This effect can explain the large dispersion of immunity drift observed in measurement of aged circuit. Because of the process dispersion between fresh components and the non-uniform ageing among the samples, the transistors of each sample are not degraded similarly, leading to differences of immunity level evolution.

Although the presented simulation results remain qualitative, the characterization and the modeling process of transistor degradation mechanisms (such as the one presented in chapter 3) will allow a quantitative prediction of the susceptibility level drifts. The accuracy of the prediction of immunity level drift can be improved by:

- An improvement of the EMC model: a more accurate PDN model which includes RF models of the SMA connector and Socket (used in MIXITY case study to facilitate DUT ageing) can be developed, the coupling effects between different sub-blocks' power rails have to be modeled accurately, such as the coupling between different power supplies, the substrate coupling or the coupling between the die and PCB ground plane.
- An improvement of the reliability model: a more precise transistor model under specific stress conditions. The ageing model have to not only fit to IV characteristic after certain stress time with specific stress condition, but also could give accurate value of the small signal quantities such as transconductance, output conductance and capacitances. Moreover, advanced failure analysis methods such as laser stimulation can help to locate precisely the root cause of susceptibility increase [DEYI10].

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General conclusion

Technology evolution leads to the improvement of integrated circuit performance and the growth of circuit complexity. However, the EMC problem has become a major concern at IC level simultaneously. The process integration, higher switching speeds and the use of multi clock frequencies tend to increase the amount of electromagnetic emission generated by ICs. Moreover, reduced supply voltage and increased number of interfaces tend to decrease the immunity to electromagnetic interference. Standardized measurement methods are used by IC manufacturers and customers to characterize the EMC of components. In order to reduce IC redesign costs and time to market, the EMC model and simulation tools compatible with the design flow are developed to evaluate the compliance to standard EMC tests before IC fabrication.

Besides, during their lifetime, ICs are affected by failure mechanisms such as negative bias temperature instability (NBTI), hot carrier injection (HCI), and time dependent dielectric breakdown (TDDB), which are accelerated by harsh environmental conditions such as high temperature of electrical overstress. Even if they trigger soft failures which do not compromise the circuit operation, they can have a significant impact on IC performances (leakage current, noise, operating frequency…). EMC issues at IC level such as electromagnetic emission and susceptibility to voltage fluctuations induced by EMI can be also strongly affected. Therefore, we proposed the electromagnetic robustness concept in the recent research which is an extension of the electromagnetic compatibility for the full lifetime of the device.

The primary contribution of this thesis was the development of a methodology to predict the variation of circuit EMC level after ageing. To achieve this goal, the study presented in this manuscript was divided in three main parts:

- Characterization the evolution of the EMC of an integrated circuit, including the conducted emission and conducted immunity test, during its lifetime. Accelerated life tests have been used to accelerate the aging process of integrated circuits.
- Characterization of MOS transistor intrinsic degradation mechanisms and extraction of preliminary transistor level ageing models.
- Development of electromagnetic robustness model to predict the circuit EMC level drifts after ageing. The EMR is also used to find a correlation between the EMC level drift and the device

intrinsic degradation mechanism, such as hot carrier injection and negative bias temperature instability.

The first chapter consists of three sections. We have been firstly interested in the advantages of technology evolution and the critical reliability issues. Although the integration efforts have greatly improved the integrated circuits performance and increased their functionality, their electromagnetic compatibility can be severely degraded if there is no efficient EMC-oriented design. To better understand the origins and consequences of the circuit emitting electromagnetic interferences (emission), we have analyzed the source of electromagnetic emission and the circuit parameters which affect emission. The impacts of technology evolution on electromagnetic emission have also been discussed. The standard emission characterization methods currently used in the IC manufacturers have been listed. As emission, origins and consequences of the electromagnetic interference coupled on the circuit (immunity) have also been studied. The main sources of interference and coupling modes have been identified. The effects of EMI on circuit can be totally different according to its nature and function (digital or analog circuit). The impact of technology evolution on immunity has also been analyzed and the standard characterization methods used for circuit immunity evaluation have been introduced. In the end of first section, we have presented the modeling methods that have been proposed until now to predict the emission and immunity level of the integrated circuit in the design level. The second section has made a state of the arts of the reliability analysis approach and the intrinsic degradation mechanism of the transistor. Compared the traditional reliability approach which predict circuit lifetime with statistical methods, the physics of failure approach has the advantage to identify the root cause of failures and to use accurate mathematical formula to model degradation mechanisms. Next, four semiconductor failure mechanisms that exist in silicon-based and that can significantly modify electrical performances have been presented: electromigration (EM), hot carrier injection (HCI), time dependent dielectric breakdown (TDDB), and negative bias temperature (NBTI). The failure principles and the induced device degradation have been analyzed. For reliability simulation, recent equivalent models for each degradation mechanism have been introduced. By combination of the EMC and reliability of integrated circuit, the electromagnetic robustness concept has been proposed in the third section. It aims at studying the impact of device intrinsic degradation on the circuit electromagnetic compatibility.

The second chapter is devoted to the characterization of the evolution of conducted emission and conducted immunity levels after accelerated-life tests, such as low temperature (LTOL) and high temperature (HTOL) through two case studies. The “EMR” qualification flow has been given in the beginning of the chapter: the most adapted EMC characterization methods, accelerated lifetime test, the statistical analysis methods used in the flow have been detailed. The experimental results demonstrate that ageing has a significant impact on electromagnetic compatibility. The emission test

performed on the input/output buffer designed in 65nm shows that conducted emission level decreases after LTOL and HTOL test. It can be explained by a combined reduction of the drain current and an increase of charge/discharge time after accelerated ageing tests. The conducted immunity test made on this case study showed that the conducted immunity of power supply pins has been degraded while the conducted immunity of digital input remains unaffected. In a second case study, the effects of circuit aging on the susceptibility of various digital and analog blocks have been compared. The analog blocks have been more vulnerable to ageing than digital parts. Reductions of up to 10 dB of immunity level have been observed on PLL. However, it is difficult to make a general conclusion about aging impact on circuit immunity since the evolution depends on the nature of circuit and the type of stressed pins. In parallel, a large dispersion of the immunity level measured on several test samples has been observed that tends to enlarge after ageing. This difference in term of circuit evolution makes difficult a pure deterministic prediction approach of EMC level variation.

To fill the gap between the circuit EMC level drift and circuit ageing, the device degradation mechanisms which occurs in a CMOS 90 nm technology has been characterized and SPICE compatible models have been extracted in the third chapter. Two typical degradation mechanisms have been studied: NBTI in PMOS and HCI in NMOS. After ageing, the drain current in saturation and linear regimes decreases. The ageing provokes a positive shift of device threshold voltage and a reduction of transconductance induced by mobility degradation. The degradation of these parameters follows a power law with respect to stress time. From the characterization results, two SPICE compatible models (nth power law and SPICE level 3) have been proposed and compared in the end of the third chapter.

In the last chapter, we have proposed a methodology of EMR modeling which is used to simulate circuit EMC level drift caused by device ageing. The first case study concerns the prediction of the evolution of EMI-induced offset for a simple NMOSFET. By using nth power model extracted from the transistor IV characteristic, the DC offset induced by EMI coupled on transistor terminals are accurately simulated. After hot carrier injection stress, the aged transistor IV characteristics have been modeled with a modified nth power law model to take into account device aging. The comparison of immunity simulation with nth power model of “fresh” and “aged” devices has provided an excellent correlation with the measured DC offset variation caused by ageing. In the second case study, we have successfully simulated the impact of circuit ageing on conducted immunity of a phase locked loop. The EMC model of PLL has been developed to model accurately the immunity level of the PLL to conducted disturbances coupled on the voltage-controlled oscillator (VCO) power supply pin. From the analysis of the VCO, the identification of critical transistor and the likely degradation mechanisms which affect them have been done. Hypotheses have been proposed to explain the drift of immunity level measured after circuit aging: the reduction of immunity level is linked to the degradation of the

PMOS transistor in the voltage controlled oscillator delay cell and this transistor undergoes NBTI. The degradation of transistor mobility and threshold voltage slows down the VCO, thus leads to a reduction of the immunity of the PLL to voltage disturbances applied to its power supply. Based on this hypothesis, a reliability model of PLL has been created and combined with the EMC model. The simulation of the entire EMR model can predict the negative shift of PLL immunity.

This thesis has been mainly focused on the characterization of the integrated circuit electromagnetic compatibility variation caused by circuit ageing, and the prediction of this variation with an "EMR" model of IC. Through the presented case studies, the dissertation has validated the flow of EMR modeling and proposed a preliminary prediction model of immunity level variation of a complete circuit. To improve the accuracy of the simulation results and the modeling and simulation flow, some improvements and perspectives can be done in future researches:

- During the extraction device ageing model step, experiments have to be done under different stress conditions and with transistors with different geometry in order to extract more accurate aged device models which include the dependence of stress voltage and geometry. Automatic parameter extraction programs need to be developed and the parameter tuning range could be defined in an empirical small variation range to reduce human decided error. Other degradation mechanisms can be added, such as HCI to PMOS, PBTI to NMOS, and TDDB. The objective is to create a set of transistor ageing models under specific technology. For each type of degradation mechanism, if the stress condition is defined, an approximate model could be provided for simulation.
- The improvement of EMR modeling focus on the circuit reliability model. The failure analysis step is composed of the localization of the most sensible transistor and the definition of the degradation mechanisms that transistors undergo. The validation of the hypothesis could be done with advanced failure analysis methods (such as laser stimulation) to identify the transistors which have the most critical influence on circuit EMC levels.

Device degradation mechanisms do not only affect circuit functionality, but also degrade circuit performance, especially the circuit electromagnetic compatibility that we concern. The designers have done a lot to limit circuit electromagnetic emission and susceptibility in order to comply with EMC standard, and improve circuit reliability. As more problems arise, more solutions are being proposed. While the circuit EMC level drift after ageing has been predicted, the consideration of the combination of both issues should be implemented. The research will continue to dig a path forward.

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Invited talk:

- "Electromagnetic robustness in deep-submicron technology" on CNES DSM reliability and failure analysis projects workshop, CNES Toulouse, Jan. 2011.

Etude de l'effet du vieillissement sur la compatibilité électromagnétique des circuits intégrés

Le développement de l'électronique dans les systèmes embarqués pour les applications aéronautique, spatial, automobile… est très significatif. L'augmentation des performances des systèmes électronique est la conséquence de l'évolution technologique des circuits intégrés. Néanmoins, cette évolution rapide nécessite une remise en cause permanente des industriels des systèmes embarqués qui doivent assurer la maitrise du comportement de leur électronique dans des environnements sévères. En particulier, la maitrise du domaine de la compatibilité électromagnétique (CEM) est un élément clé de la réussite des challenges d'intégration et d'évolution technologique. L'évolution technologique, c'est-à-dire l'intégration de plus en plus poussée de fonctions différentes dans un système plus réduit, tend à aggraver les problèmes d'émission électromagnétique parasite et de susceptibilité aux interférences électromagnétiques.

De plus, l'évolution technologique tend à dégrader la fiabilité des composants et réduire leur durée de vie. Les performances des circuits sont affectées prématurément par les mécanismes de dégradation intrinsèque tels que l'injection de porteurs chauds (HCI), Negative bias temperature instability (NBTI), Time dependent dielectric breakdown (TDDB). Ceux-ci sont accélérés par les conditions d'exploitation extrêmes (haute/basse température, surcharge électrique, rayonnement).

Ce travail de thèse est dédié à l'étude de l'effet du vieillissement sur la compatibilité électromagnétique des circuits intégrés. Il consiste à caractériser la dérive des niveaux d'émission et d'immunité des composants induite par leur vieillissement et proposer des modèles représentatifs de l'évolution au cours du temps des performances CEM.

Dans ce manuscrit, la première partie est consacrée à la présentation du contexte et de la problématique de ce travail de thèse. Dans la seconde partie, l'impact du vieillissement sur l'émission et l'immunité conduite de circuits intégrés est caractérisé expérimentalement. Dans la troisième partie du manuscrit, l'effet du vieillissement sur les transistors MOS est étudier et des modèles électriques sont extraits, afin de simuler l'impact du vieillissement sur les performances CEM. Finalement, dans la dernière partie, avec la méthode que nous avons proposée, nous développons un modèle qui peut reproduire la variation du niveau d'immunité d'un composant après vieillissement.

1. INTRODUCTION

1.1. Evolution technologique des semi-conducteurs

1.1.1. Théorie de la miniaturisation

La miniaturisation des circuits intégrés (CI) correspond à la réduction des dimensions des transistors MOS, qui s'accompagne d'une diminution des niveaux de tension. Cette tendance a permeis l'amélioration des performances des nouvelles générations de circuits CMOS, d'augmenter la densité de transistors et de réduire la consommation de puissance. La miniaturisation à champ électrique constant (CE) a été proposée par Dennard en 1974 [DENN74]. Elle consiste en une réduction linéaire par un facteur α des dimensions d'un transistor et des tensions qui lui sont appliquées. Elle permet de conserver les champs électriques constants dans le canal de conduction du transistor. En raison des problèmes de compatibilité des tensions d'alimentation du système et des tensions

requises pour garantir une miniaturisation à champ électrique constant, une nouvelle approche appelée miniaturisation à tension constante (CV) a été proposée. Elle suit les mêmes règles que la théorie de la miniaturisation a champ constant, excepté pour les tensions de fonctionnement qui demeurent invariantes. La miniaturisation des Cis selon cette approche fait apparaitre des champs électriques élevés et des courants importants. Depuis 1990, un compromis entre les approches «CE» et «CV» est largement utilisé dans l'industrie : tensions et dimensions sont réduites dans des proportions différentes.

1.1.2. L'impact de la miniaturisation sur la fiabilité

La miniaturisation effectuée selon un compromis entre les approches « CE » et « CV » implique une réduction différentes entre les tensions et les dimensions. Le champ électrique tend donc à augmenter progressivement au fil des générations technologiques. La **Figure 1-1** illustre l'évolution de la tension d'alimentation (V_{DD}), de la tension de seuil (Vth) en fonction du nœud technologique (exprimée en terme de longueur de canal).

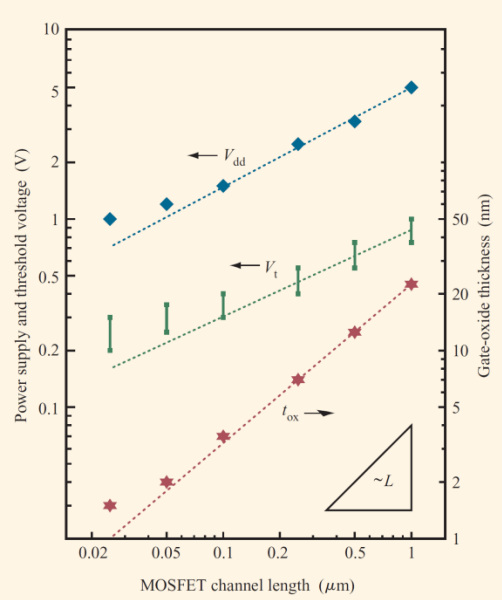

Figure 1-1: Histoire et tendance de la tension d'alimentation (VDD), tension de seuil (VTH) versus la longueur de canal pour les technologies de la logique CMOS [TAUR99].

L'augmentation du champ électrique horizontal et vertical dans le canal induit des problèmes de fiabilité, causés par différents mécanismes de dégradation tels que Negative bias temperature instability(NBTI), Time dependent dielectric breakdown (TDDB), Hot carrier injection (HCI), and Electro-migration (EM)…Entre, l'évolution asymétrique de l'alimentation et des dimensions du transistor peut également augmenter la densité de puissance de la puce et par conséquent, augmenter la température de jonction conduisant à une accélération de la dégradation des performances du circuit.

Des informations sur l'évolution technologique des semi-conducteurs sont livrées par l'ITRS (« international technology roadmap for semiconductors ») et montrent la tendance sur 15ans. Les vitesses de fonctionnement des microprocesseurs et microprocesseur augmentent d'année en année avec la réduction technologique, avec une tendance à saturer après 2015 [ITRS05]. L'augmentation de la fréquence de fonctionnement et la complexité de CI accroît le bruit de commutation (di/dt), qui fait du CI une source de « bruit électromagnétique » de plus en plus importante. Par ailleurs, avec la réduction des tensions d'alimentation, la marge de bruit associé a été diminuée. Bien que la réduction de tension ralentisse dans les générations récentes, la marge de bruit est prévue de tomber en dessous

de 100mV en 2015 (Figure 1-2). La réduction de la marge de bruit signifie une sensibilité accrue aux interférences électromagnétiques.

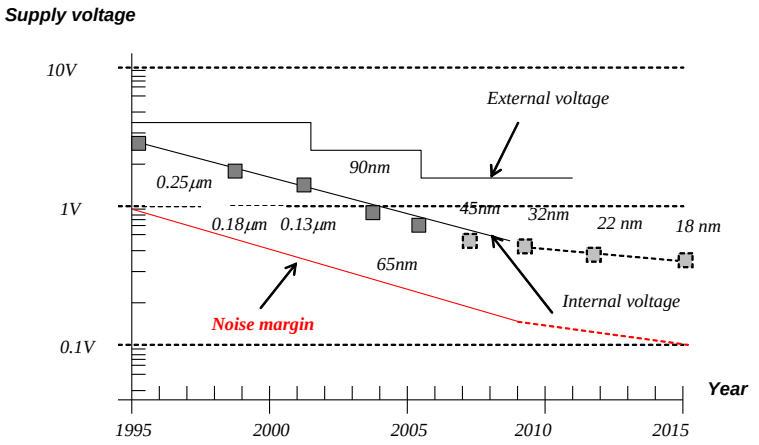

Figure 1-2: Diminution continue des tensions d'alimentations et des marges de bruit en fonction du nœud technologique et de leur année d'apparition

Comme mentionné ci-dessus, avec l'évolution technologique, avec l'amélioration de la performance du circuit, la conception de circuits intégrés est soumise à de nombreux problèmes de CEM et de fiabilité.

1.2. La compatibilité électromagnétique des circuits intégrés

La compatibilité électromagnétique (CEM) est depuis longtemps appliquée aux systèmes électroniques. Elle permet d'assurer que ceux-ci restent insensibles aux agressions électromagnétiques extérieures qui viennent polluer son environnement et que sa propre activité ne vienne pas dégrader l'environnement électromagnétique et perturber les systèmes environnants. Cependant, depuis plusieurs années, la CEM doit aussi être assurée au niveau du circuit intégré. La CEM peut se décomposer en 2 problèmes : l'émission parasite et la susceptibilité (ou immunité).

Assurer à la fois une faible émission électromagnétique et une faible susceptibilité permet de garantir une compatibilité entre des systèmes électroniques voisins et donc une bonne sureté de fonctionnement.

1.2.1. Emission électromagnétique des circuits intégrés

Les émissions électromagnétiques trouvent leur origine dans le courant consommé lors de la commutation des circuits élémentaires du composant électronique. La Figure 1-3 illustre le phénomène du bruit de commutation produit par un circuit élémentaire, représenté par un inverseur CMOS.

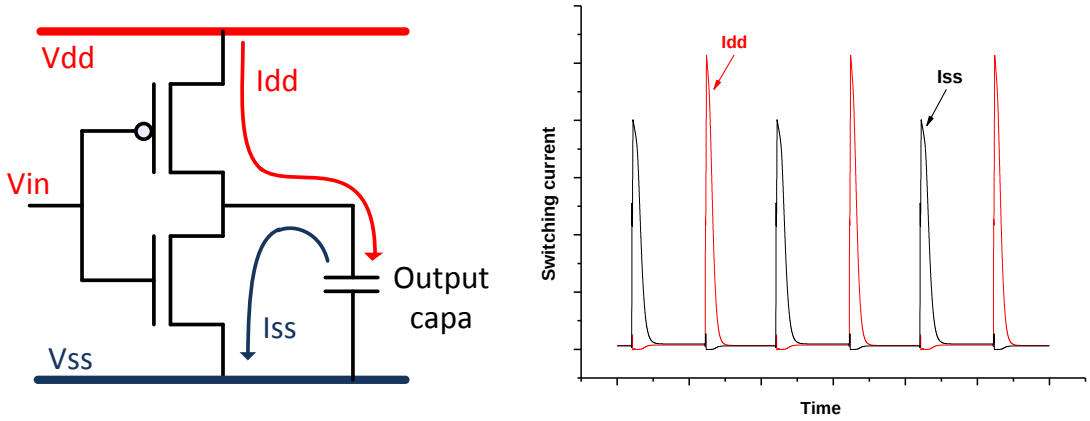

Figure 1-3: Courant consommé par un circuit élémentaire

Lors du passage de la sortie de l'inverseur du niveau logique bas au niveau logique haut, le courant venant de l'alimentation V_{DD} charge la capacité de la sortie de l'inverseur, à travers le transistor PMOS. Inversement, lors du passage de la sortie du niveau logique haut au niveau logique bas, le courant circule par le transistor NMOS vers la masse VSS déchargeant ainsi la capacité en sortie de l'inverseur. La variation d'amplitude brutale et rapide du courant traversant le chemin d'alimentation provoque des fluctuations de la tension d'alimentation à cause de l'inductance parasite des pistes du circuit intégré, des fils de « bonding » qui relie la puce à son boitier, des broches « lead » du boitier lui-même, ainsi que des éventuelles des pistes du circuit imprimé « PCB track ». Au niveau d'un circuit, le boitier représente le contributeur majeur de l'inductance parasite, tandis que le réseau de distribution d'alimentation interne est plus résistif. Le bruit lié au passage du courant de commutation des circuits au travers des inductances parasites des différentes interconnexions est appelé « ΔI noise ». Son amplitude peut être évaluée à partir de la valeur de l'inductance et du profil temporel du courant. Le bruit lié au passage du courant appelé « IR noise » est déterminée par la valeur de la résistance et l'amplitude du courant.

1.2.1.1. Effet de l'évolution technologique sur l'émission électromagnétique

L'évolution technologique conduit à une augmentation du pic de courant transitoire et donc accroit l'amplitude du ΔI noise. La commutation des entrées/sorties est un des principaux contributeurs du bruit de commutation. Le nombre de l'entrées/sorties croissant pose également de sérieux problèmes à cause du nombre important de commutations simultanées et des forts courants qui sont véhiculés. L'accroissement du nombre de portes logiques à l'intérieur des circuits digitaux implique une consommation de courant plus importante et une augmentation des pics de courants transitoires. Enfin, la généralisation de microprocesseurs performants utilisant plusieurs horloges de fréquences différentes ainsi que l'augmentation des fréquences de fonctionnement des circuits intégrés ont étalé et décalé le spectre des émissions parasites vers les hautes fréquences.

1.2.2. Susceptibilité des circuits intégrés

Les agressions conduites et rayonnées se traduisent par des courants et tensions parasites dans les circuits intégrés, pouvant entrainer un dysfonctionnement qui peuvent aller jusqu'à une destruction. Ces perturbations peuvent être classifiées suivant leurs niveaux d'énergie, leur bande de fréquence par rapport à celle du fonctionnement du circuit victime et enfin par la nature de l'agression (impulsionnelle ou continue). La gamme des effets produits par ces perturbations sur les circuits intégrés est très vaste. Dans les circuits numériques une agression impulsionnelle dont la durée est au moins égale au temps de réponse du circuit victime et qui se propage à l'intérieur des couches

logiques, entraine des commutations supplémentaires ou prématurées des signaux internes concernés. Ces dernières peuvent générer des fautes dans la transmission de données, provoquant un arrêt du circuit. Les circuits analogiques sont parmi les plus susceptibles car leur marge de bruit est très faible [RICH04]. Dans les circuits analogiques, par exemple, une agression continue agit par augmentation du plancher de bruit du composant entrainant une dégradation du rapport signal/bruit ainsi qu'une déviation des caractéristiques par modification de la composante continue de polarisation.

1.2.2.1. Effet de l'évolution technologique sur la susceptibilité des circuits intégrés

La réduction des tensions d'alimentation a des lourdes conséquences sur la vulnérabilité des circuits aux agressions électromagnétiques puisqu'elle s'accompagne d'une réduction des marges de bruit des circuits ainsi que des seuils de commutation des circuits numériques, les rendant plus vulnérables aux interférences électromagnétiques (EMI). De plus, la montée des fréquences de fonctionnement des circuits a aussi un impact sur la susceptibilité des circuits intégrés. Les circuits digitaux sont caractérisés par une marge de délai ou dynamique. Elle définit le délai maximal admissible sans entrainer de pertes de synchronisation ou d'apparition d'états indésirables. Celle-ci est fixée pour assurer une durée minimale à l'apparition et à l'établissement des signaux. Plus les circuits rapides, les périodes d'horloge sont plus faibles, et plus ces marges seront réduites. Les circuits sont plus sensibles à l'agression.

1.2.3. Techniques de mesure et de modélisation de la compatibilité électromagnétique des circuits intégrés

Diverses approches de mesures d'émission parasite et d'immunité aux ondes électromagnétiques ont été développées au début des années 90 et standardisées, tels que les standards IEC 61967 [IEC 61967] pour les mesures d'émission et IEC 62132 [IEC 62132] pour les mesures d'immunité.

Simuler les performances électromagnétiques d'un circuit intégré avant sa fabrication est un facteur essentiel pour éviter des phases de « redesign » très couteuses. Des outils de simulation et des modèles CEM sont donc nécessaires pour prédire les performances des circuits en termes d'émission et de susceptibilité. Il existe des modèles standards : ICEM défini par [IEC 62433-2] pour l'émission du CI et ICIM défini par [IEC 62433-4] pour l'immunité du CI.

1.3. La fiabilité des circuits intégrés

1.3.1. Défauts dans une structure MOS

Le comportement électrique du transistor MOS dépend fortement de la qualité de l'interface SiO2/Si. Les interactions des porteurs du canal avec les défauts réduisent les performances électriques du dispositif.

Dans les structures MOS, on distingue différents types de défauts (**Figure 1-4**) :

- Des états d'interface (pièges de charges positives/négatives ou piège neutres)
- Des défauts de l'oxyde (charges fixes près de l'interface, des ions mobiles dans le volume ou encore pièges de charges)

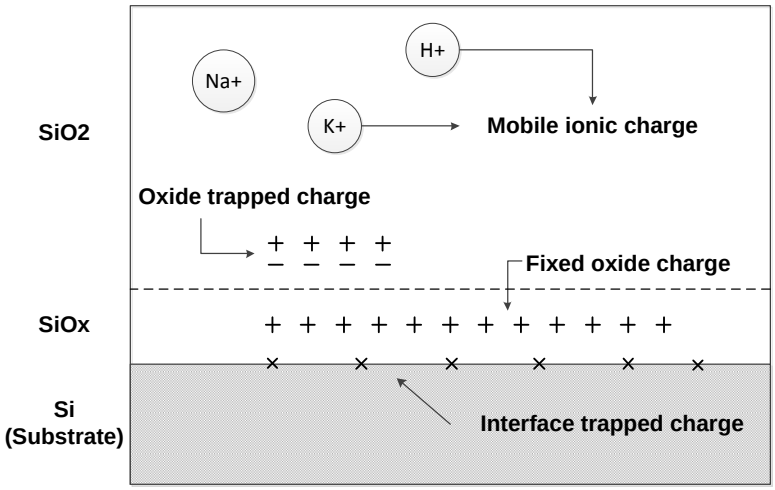

Figure 1-4: Différents pièges de charges dans la structure de MOS [LEBL93].

Ces charges sont la principale cause des problèmes de la fiabilité d'oxyde. L'interface Si/SiO2 a tendance à présenter des liaisons pendantes et des lacunes interstitielles qui ont une capacité à capturer des porteurs de charge. Elle conduit à la dégradation de la mobilité (µ) ou transconductance (Gm) par la diffraction d'interaction avec les porteurs dans le canal. La dégradation de la mobilité conduit a la réduction de courant de drain. La répartition des charges piégées dans l'oxyde et les pièges d'interface ont une influence sur la tension de seuil [TAKE95].

1.3.2. Injection de porteurs chauds (HCI)

Le rapport entre les dimensions géométrique (Lg) du transistor et la tension d'alimentation (VDD) n'est pas conservé au fil des technologies et les champs électriques à travers le canal sont de plus en plus forts. Ce fort champ électrique peut conduire au mécanisme de dégradation appelé injection de porteurs chauds. Un porteur chaud désigne un porteur qui a été accéléré par un fort champ électrique latéral et injecté dans l'oxyde de grille.

On distingue quatre mécanismes de génération et d'injection de porteurs chauds [TAKE83a]. L'ionisation par impact ou drain avalanche hot carrier (DAHC) et Porteurs énergétiques du canal ou Channel Hot Electron (CHE) sont les plus importants:

- ***Porteurs énergétiques du canal ou Channel Hot Electron (CHE)*** :

Au voisinage du drain, région de champ électrique transversal intense, et à condition d'avoir acquis suffisamment d'énergie lors de leur parcours dans le canal, des électrons peuvent franchir la barrière d'énergie Si/SiO2 et être directement injectés dans l'oxyde de grille. Ces électrons sont à la base de la création d'un courant de grille, et leur action est maximale lorsque Vg≈Vd. (**Figure 1-5**)

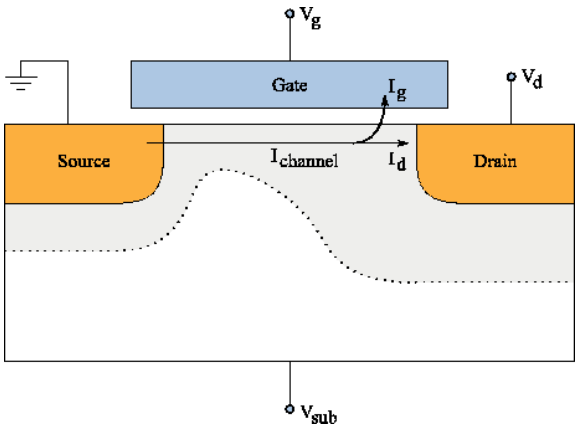

Figure 1-5: Porteurs énergétiques du canal ou Channel Hot Electron (CHE) : [ENTN07].

- ***Ionisation par impact ou Drain Avalanche Hot Carrier (DAHC)***

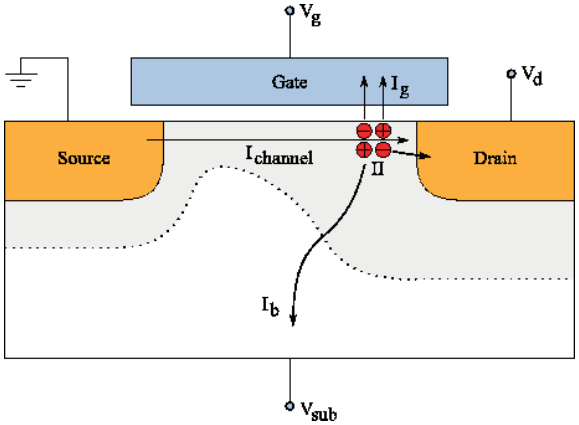

Figure 1-6: Ionisation par impact ou Drain Avalanche Hot Carrier (DAHC) [ENTN07].

Sous l'action d'un fort champ électrique latéral, les porteurs du canal issus de la source sont fortement accélérés et gagnent de l'énergie, énergie qu'ils cèdent aux atomes du réseau cristallin lors des collisions. Si l'énergie cédée est supérieure à l'énergie d'ionisation, il y a alors génération de paires électrons-trous qui se dissocient de façon instantanée. L'ionisation primaire se produit près du drain qui collecte les électrons et repousse les trous vers le substrat. Un certain nombre d'électrons peuvent être injectés dans la grille, un piégeage de porteurs dans l'oxyde est aussi très probable dégradant ainsi l'oxyde. Pour Vg≈Vd/2 (Si massif), on a ainsi affaire à la condition de courant de substrat maximal. Ce phénomène entraîne le plus de dégradation pour des températures normales. (Figure 1-6)

L'injection DAHC provoque la dégradation plus sévère à température ambiante. Il y a deux types de porteur (électrons chaud, trou chaud) qui sont injectés dans l'oxyde de grille.

1.3.2.1. Dégradation sur les performances du composant et phénomène d'accélération

Le mécanisme trouve son origine au niveau du drain du transistor et conduit à l'injection de charges dans l'oxyde de grille, qui provoque :

- la dégradation de la tension de seuil Vt
- la dégradation de la mobilité des porteurs dans le canal
- la dégradation de la transconductance
- la création d'un courant de fuite dans le substrat, qui peut déclencher des transistors parasites et donner naissance à un phénomène de latch-up

Le phénomène de porteurs chauds est dépendant de la température, mais augmente à basse température. Il a ainsi une énergie d'activation négative. En effet, quand la température diminue, la probabilité de collision entre les électrons et les atomes de Si du réseau cristallin est réduite et le nombre de porteurs chauds augmente.

Ensuite, il dépend de la tension de drain, qui augmente le champ électrique latéral. Ainsi, plus la tension de drain Vd est grande, la dégradation est plus rapide.

1.3.3. Time Dependent Dielectric Breakdown

Le mécanisme de TDDB est lié à l'intégrité de l'oxyde de grille. Il s'agit d'un phénomène de dérive de paramètres (Soft BD) suivi par un claquage d'oxyde de grille soudain dû à la création d'un chemin conducteur à travers l'oxyde, qui conduit à une montée brutale de la conductance de la grille. Celui-ci peut alors conduire à la destruction de l'oxyde (Hard BD) et à une panne du circuit. Le TDDB dépend du nombre de défauts dans l'oxyde créés au cours de la fabrication. Il reste indépendant des conditions de polarisation, mais dépend de la densité de courant qui va circuler à travers l'oxyde de

grille par effet tunnel. Ainsi, utiliser des tensions très grandes qui font augmenter le courant d'oxyde réduit la durée de vie d'un composant.

Une fois que les électrons ont franchi la barrière de potentiel de l'oxyde, ils sont accélérés par le champ électrique vertical, qui dépend de la tension appliquée et de l'épaisseur d'oxyde. Pour les technos submicroniques, pour un oxyde de moins de 2 nm d'épaisseur, le champ électrique peut atteindre 4 à 5 MV/m. L'oxyde est capable de supporter des champs de plus de 10 MV/m sans claquer.

Néanmoins, l'énergie apportée par ces charges peut briser localement les liaisons chimiques Si-SiO2 et créer des pièges d'interface. Ceux-ci modifient les propriétés du canal et contribuent à réduire la mobilité des porteurs dans le canal. De plus, le piégeage de ces charges peut accroître le champ électrique localement et accroître encore plus le courant d'électrons par effet tunnel. Il y a donc une sorte d'effet feedback qui accélère le processus de dégradation.

Le TDDB est accéléré par la température et le champ électrique ou la tension suivant l'épaisseur de l'oxyde. Suivant la tension de grille et l'épaisseur, différent types de courant passe à travers l'oxyde et ces courants ont des dépendances différentes au champ électrique (E model ou 1/E model) [BERN06].

1.3.4. Negative Bias Temperature Instability (NBTI)

Ce phénomène dégrade principalement les transistors PMOS. Il est activé par des tensions négatives sur la grille qui engendrent un champ vertical fort et par de fortes températures. Il est fortement lié à l'épaisseur d'oxyde et à la longueur du canal. Il cause un piégeage de charge à l'interface oxyde de grille – silicium, qui conduit à une dérive de la tension de seuil Vt, de la mobilité et à une réduction des courants de drive Ion. Les dérives de Vt dues au NBTI sont nettement plus graves pour les technos avancées car les tensions d'alimentation diminuent et les épaisseurs d'oxyde se réduisent. On parle aussi de PBTI pour les NMOS, mais celui-ci est moins sensible aux contraintes NBT/PBT que le transistor PMOS.

Un phénomène de relaxation est présenté. Une partie de la dégradation s'autoguérit lorsqu'un potentiel électrique positif (phase de relaxation) est appliqué sur la grille après une contrainte NBT. Ils ont mis ainsi en évidence un piégeage/dépiégeage de trous lors des phases NBT/Relaxation. Lorsque la polarité de la grille est inversée, la densité de pièges est réduite, expliquant pourquoi les caractéristiques sont recouvrées. Cependant, cela n'est plus vrai à haute température. Ainsi, l'effet d'un stress DC conduit à une dégradation plus rapide qu'un stress AC, provoquant des problèmes de caractérisation électrique. Ce phénomène est particulièrement problématique pour la caractérisation de la dégradation des dispositifs MOS à oxyde fin. En effet, la plupart des techniques de caractérisation sont basées sur des mesures I(V) pour lesquelles la contrainte est arrêtée pour pouvoir effectuer les mesures.

Les contraintes NBT sur les PMOS sont à l'origine d'une augmentation de la tension de seuil Vt ainsi que d'une diminution de la transconductance Gm. La mobilité des trous à l'interface est réduite à cause de la réduction de Gm, et le courant dans le mode linéaire est aussi réduit à cause de l'augmentation de Vt et la diminution de la mobilité [Denais 2005].

1.3.5. Synthèse des effets des mécanismes dégradations sur un transistor MOS

Les trois mécanismes de dégradation liés au défaut de l'oxyde de grille du transistor affectent les paramètres électriques d'un transistor MOS. Le **Table 1-1** résume les caractéristiques de ces trois mécanismes sur le transistor [WU05] [SCHR03].

	HCI	TDDB	NBTI
Origine	Porteurs accélérés par le champ latéral	Piégeage de charges dans l'oxyde de grille Trou dans l'oxyde pouvant causer la destruction	Défauts d'interface libérant un ion H+ et piégeant des charges
L'énergie d'activation	-1.0eV	0.7eV	0.4eV
Transistor	Surtout NMOS	NMOS/PMOS	Surtout PMOS
Autoguérison	no	no	Oui
Tension seuil (abs) (|VTH|)	Augmentation	Augmentation	Augmentation
Facteurs d'accélération	Basse température Forte tension de drain	Forte température Forte tension de grille	Forte température Forte tension négative sur la grille
Transconductance (Gm)	Diminution	Diminution	Diminution
Mobilité (μ)	Diminution	Diminution	Diminution
Capacitance de l'oxyde de grille (Cgs/Cgd)	Diminution	Diminution	Augmentation
Channel résistance (Rds)	Augmentation	non	Augmentation
Drain courant saturation (Idsat)	Diminution	Diminution	Diminution
Transistor courant linéaires (Idlin)	Diminution	Diminution	Diminution
Autre	Le courant de substrat(Ib) augmente	Le courant fuit de l'oxyde (Ig) augmente/l'impédance d'entrée diminue	Le courant de canal en état off (Ioff) diminue

Table 1-1: Synthèse dès l'impact des dégradations des paramètres en fonction du vieillissement

1.4. La robustesse électromagnétique des circuits intégrés

Comme nous l'avons indiqué dans les deux paragraphes précédents, les problèmes de CEM ont augmenté et assurer faible émission et une haute immunité aux interférences est devenue indispensable. Dans le même temps, les dispositifs travaillant dans des environnements extrêmes (surtension, haute/basse température) voient les mécanismes de dégradation activées, qui peuvent entrainer un dysfonctionnement du circuit. Parfois, le système peut travailler continuellement sans échec, bien que ses performances soient dégradées, puisque les paramètres physiques des transistors le constituant ont été dégradés par les mécanismes dégradation intrinsèques. Parmi ces performances du circuit, les marges de CEM peuvent également être modifiées avec le temps, augmentant le risque de défaillance et de non conformité aux normes CEM.

Une demande nouvelle est apparue fin 2005 de la part des constructeurs automobiles visant à assurer la « **robustesse électromagnétique** » (Electromagnetic Robustness EMR) des systèmes embarqués. Ce concept est une extension de la CEM pour la durée de vie complète du produit. Ce domaine est encore peu exploré, les communautés « fiabilité » et « CEM composants » étant assez cloisonnées. Cependant, il est fondamental pour assurer la sûreté de fonctionnement à long terme de systèmes électroniques. En effet, si un circuit respecte les limites CEM au début de sa vie, quand les caractéristiques internes

du circuit évoluent au cours du temps en raison de mécanismes de dégradation internes, le respect des limites CEM n'est peut-être plus garanti quelques années plus tard.

2. EFFET DU VIEILLISSEMENT DES CIRCUITS INTEGRES SUR LA CEM

Dans cette partie, on utilise le cas de circuits intégrés de test en technologie 65nm pour montrer l'impact du vieillissement sur l'émission et le cas d'un circuit mixte pour comparer l'impact du vieillissement sur l'immunité.

2.1. Le vieillissement accéléré des circuits intégrés

Le vieillissement accéléré est une méthode pour déterminer la durée de vie qui permet de mettre en évidence les comportements internes des structures des composants, dans les conditions réelles de vieillissement, en un temps très réduit. Cette approche permet d'éviter les longues attentes de vieillissement qui peuvent être de 10, 15 ans ou même plus suivant le cas d'étude. L'objectif du vieillissement accéléré est de forcer le taux d'accumulation des dommages d'échecs et d'usures qui sont produits dans les conditions de cycle de vie. La mesure de l'accélération, généralement appelée facteur d'accélération (AF), est définie comme étant le rapport entre la vie sous les conditions normales et celle prévue par les conditions d'essais accélérés. Il existe différentes approches, par rapport aux types de stress, et la durée de vieillissement de test peut calculer avec le facteur d'accélération. L'expression mathématique du facteur d'accélération [**Equation 2-1**] est définie :

$$AF_O = AF_T \times AF_V = e^{\frac{E_a}{K}\left(\frac{1}{T_0}-\frac{1}{T_s}\right)+\beta(V_s-V_0)} \qquad \textbf{Equation 2-1}$$

Les conditions de stress est la surtension et stress thermique, en supposant qu'ils sont indépendants, et l'accélération est illustrée par **Figure 2-1**:

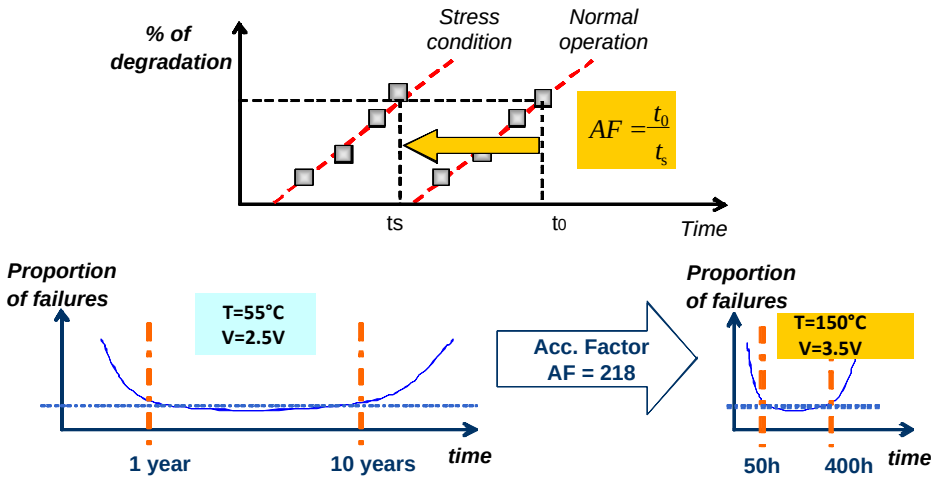

Figure 2-1: L'accélération vieillissement par surtension et haute température

L'accélération du vieillissement est effectuée par les stress de surtension (stress électrique) et thermique (-40°C et 150°C) à l'aide d'une enceinte climatique (HTOL et LTOL) [AEC-Q100] [JEDEC22]. :

- High température operating life (HTOL): le composant sous test fonctionne en mode statique ou dynamique. L'état de fonctionnement est sous haute température (150°C) avec une polarisation en surtension (20% supplémentaire). Les broches comprennent : la tension

d'alimentation, l'horloge, l'entrée, etc. Le test HTOL active généralement les mécanismes de dégradation : EM, NBTI, et TDDB ;

- Low temperature operating life (LTOL): est fondamentalement juste l'équivalent au test HTOL mais avec une température basse (-40°C). Il est destiné à la recherche des défaillances causées par porteurs chauds (HCI).
- Electrical stress: à température ambiante, avec le stress de surtension sur les broches testées et une configuration spéciale pour différents mécanismes de défaillance.

Le banc de vieillissement est présenté dans la **Figure 2-2**

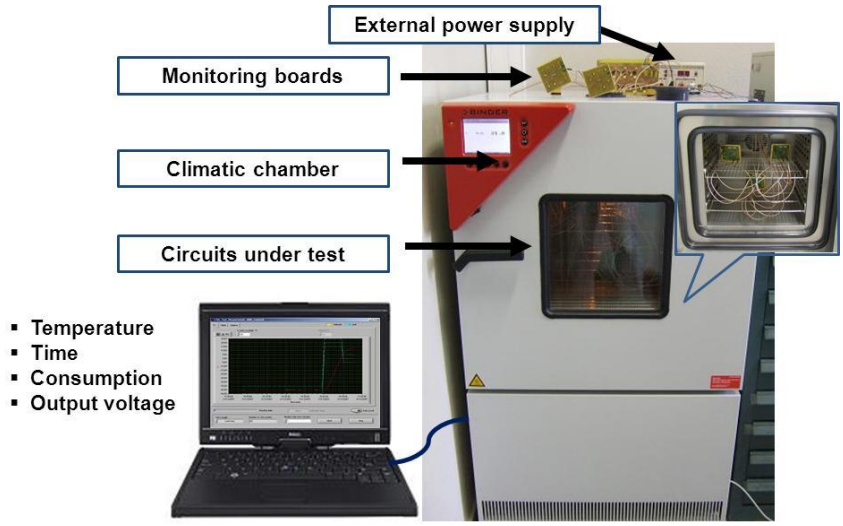

Figure 2-2: Banc de vieillissement accéléré

2.2. Banc de caractérisation de l'émission conduite

La méthode qu'on a utilisée dans notre cas d'étude est l'émission conduite selon la norme IEC 61967-4 « méthode de 1Ω/150Ω ». Les émissions électromagnétiques des systèmes électroniques proviennent du bruit de commutations simultanées généré par les appels de courant apparaissant lors des changements d'états logiques des portes et les entrées-sorties. La **Figure 2-3** décrit le banc expérimental permettant de caractériser l'émission conduite d'une entrée/sortie digitale sur la bande 150 KHz – 1 GHz [2]. Le test consiste à mesurer le spectre du courant transitoire de masse qui est produit par le composant sous test.

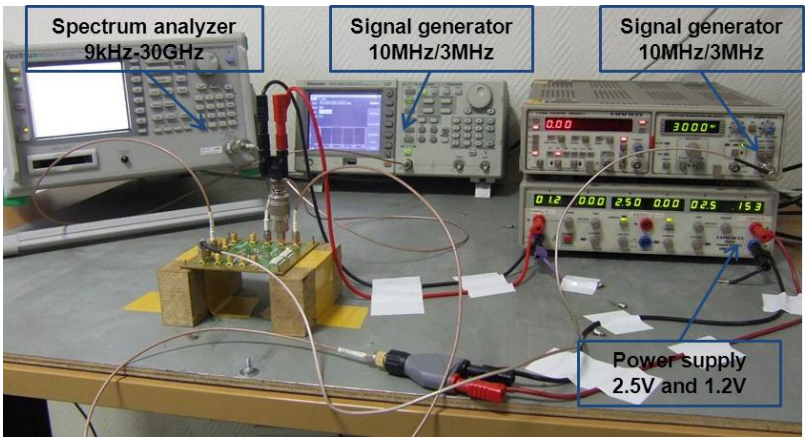

Figure 2-3: Banc de mesure l'émission conduit avec méthode 1Ω

2.3. Banc de caractérisation de l'immunité conduite

La méthode de caractérisation de l'immunité conduite ou DPI (Direct Power Injection) est une méthode d'injection conduite de perturbations radiofréquences RF appliquée directement sur une entrée ou sortie du circuit intégré, référencée par la norme de mesure [IEC-62132] (**Figure 2-4**). Cette caractérisation suivant ce standard est valide sur la bande de fréquence 1 MHz - 1 GHz, elle inclut une capacité que nous appelons communément la capacité d'injection pour transmettre au circuit intégré sous test la puissance de la perturbation.

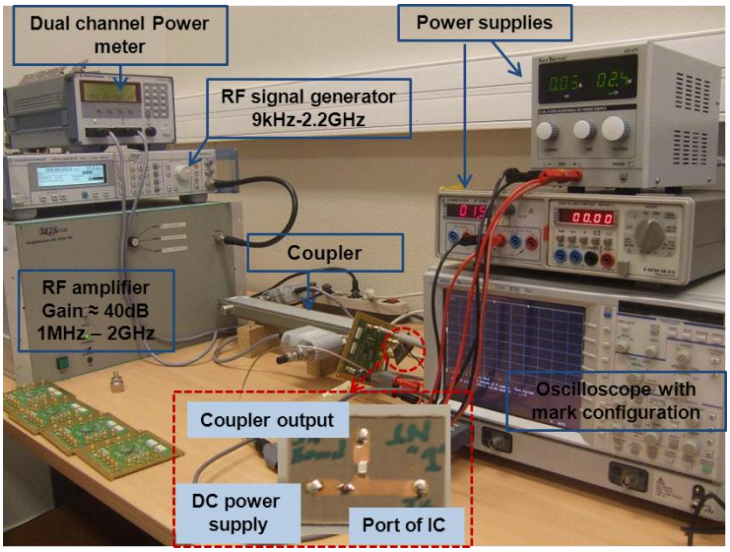

Figure 2-4: Banc de mesure d'immunité conduit selon la méthode DPI

2.4. L'impact du vieillissement sur l'émission conduite

Dans le but de caractériser l'effet du vieillissement sur l'émission, nous avons étudié le cas d'un circuit intégré de test fabriqué en technologie CMOS 65nm, contenant différentes structures d'entrée/sortie. Afin de faire une analyse statistique, nous avons considéré un lot de 5 composants. La mesure de répétabilité est effectuée par mesure sur le même composant sur 10 fois. La différence est inférieure à 1dB sur toute la bande de fréquence.

La **Figure 2-5**, présente le spectre d'émission (son enveloppe) avant et après vieillissement.

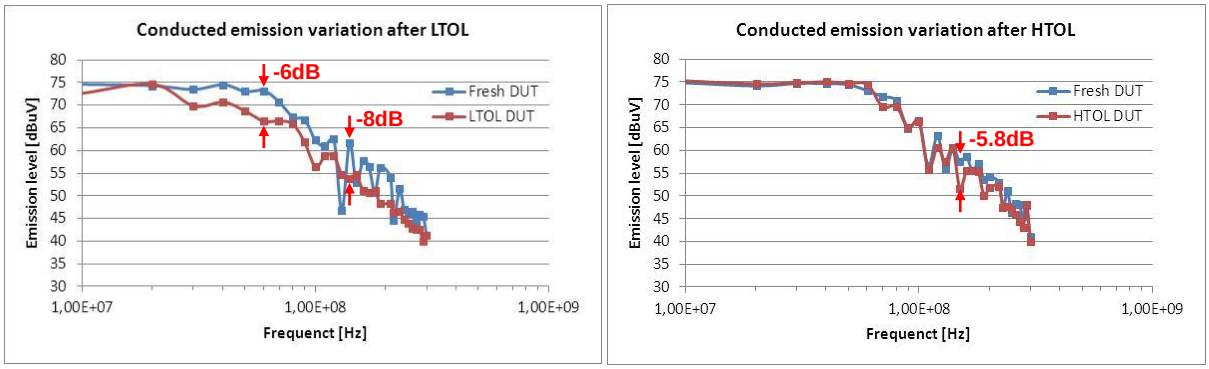

Figure 2-5: L'émission conduit de l'alimentation avant et après vieillissement (HTOL & LTOL)

Apres tous les deux types de vieillissement accéléré, nous constatons une diminution de l'émission conduite qui peut aller jusqu'à 8dB après le LTOL et 5.8dB après le HTOL (**Figure 2-6**).

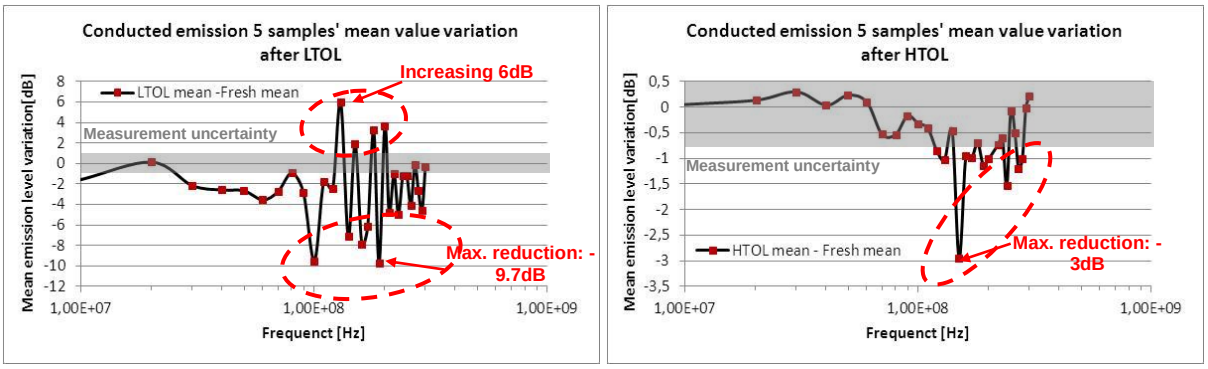

Figure 2-6: Niveau moyen de l'émission pour les 5 échantillons après différente type de vieillissement

La comparaison des niveaux moyenne sur 5 échantillons monte que l'émission varie largement sur les harmoniques. Il y a aussi une dispersion entre les 5 échantillons, à cause des variations de procès affectant les circuits. Ce type de dispersion a été étendu après les deux types de vieillissement (**Figure 2-7**).

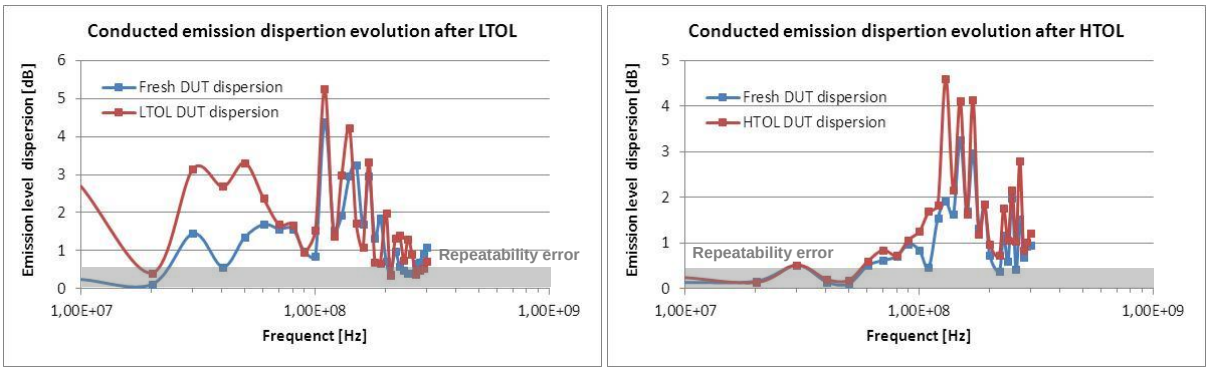

Figure 2-7: Dispersion sur les 5 échantillons avant et après vieillissement

La réduction de l'émission est principalement induite par la diminution du courant de transistor après vieillissement. A cause des mécanismes de dégradation du transistor, après vieillissement, l'amplitude de courant pour charger et décharger la capacité de la sortie est réduite, et le temps de chargement et déchargement est élargie. Le profil de signal temporel ainsi que le spectre s'en trouvent modifiés. (**Figure 2-8**)

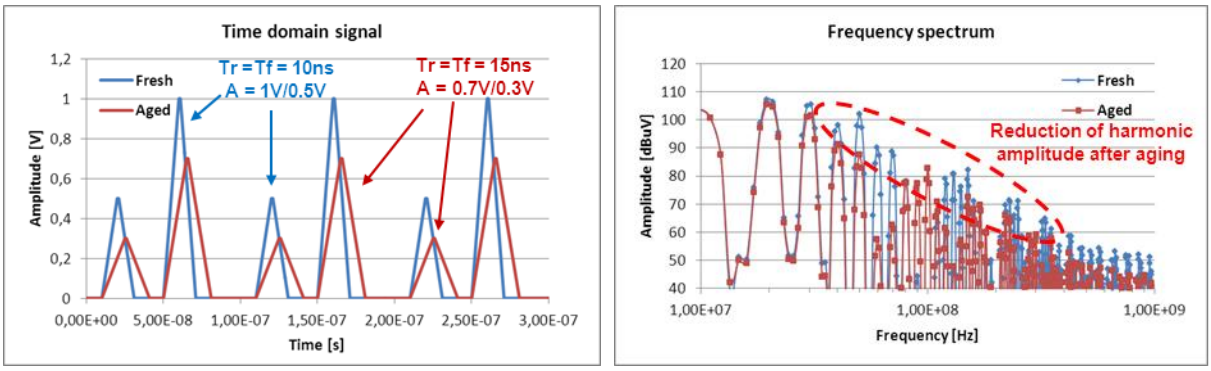

Figure 2-8: Simulation du bruit sur l'alimentation de l'inverseur avant et après vieillissement

2.5. L'impact du vieillissement sur l'immunité conduite

Dans le but de caractériser l'effet du vieillissement sur l'immunité, nous avons étudié le cas d'un circuit intégré de test fabriqué en technologie CMOS 65nm. Les perturbations sont injectées sur

l'alimentation et l'entrée du bloc. Le bloc testé est un buffer d'entrée/sortie. La défaillance est définie par le signal de sortie qui dépasse le critère tension de sortie +/- 20% lors des caractérisations d'immunité. Afin de faire une analyse statistique, nous avons considéré un lot de 5 composants. Le banc de mesures d'immunité est identique avant et après vieillissement. La mesure de répétabilité est effectuée par mesure sur le même composant répétée 10 fois. La différence est de moins de 2dB sur toute la bande de fréquence de la perturbation.

Après avoir appliqué le stress « HTOL et LTOL », nous avons constaté que le niveau de l'immunité de l'alimentation diminue après vieillissement accéléré. Et la maximum peut atteindre -8.5dB après LTOL et -8.8dB après HTOL. (Figure 2-9)

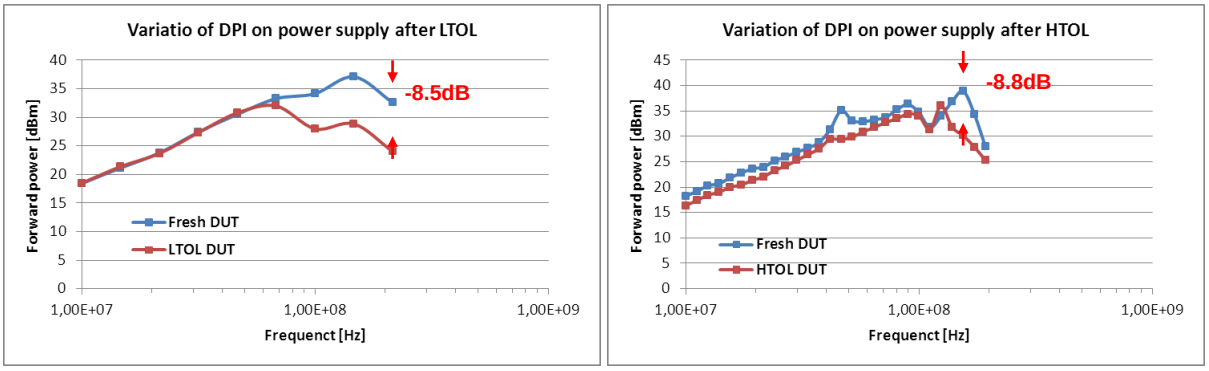

Figure 2-9: Réduction de l'immunité conduite sur l'alimentation après différents types de vieillissement

La réduction du niveau moyen sur 5 échantillons est aussi significative (Figure 2-10).

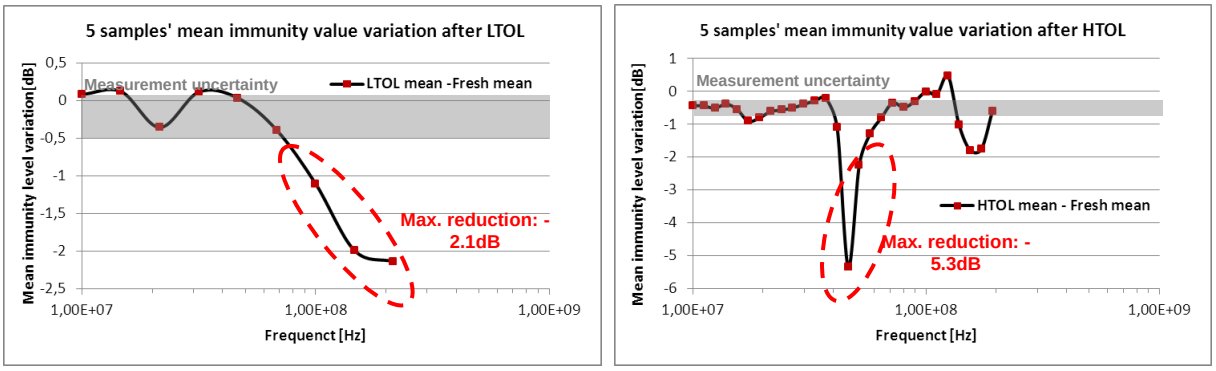

Figure 2-10: Niveau moyen de l'émission pour les 5 échantillons après différents types de vieillissement

La comparaison des niveaux moyens sur 5 échantillons montre que l'immunité varie largement après LTOL et HTOL. Il y a aussi une dispersion entre les 5 échantillons, à cause des variations de procès de fabrication. Ce type de dispersion augmente après les deux types de vieillissement (Figure 2-11).

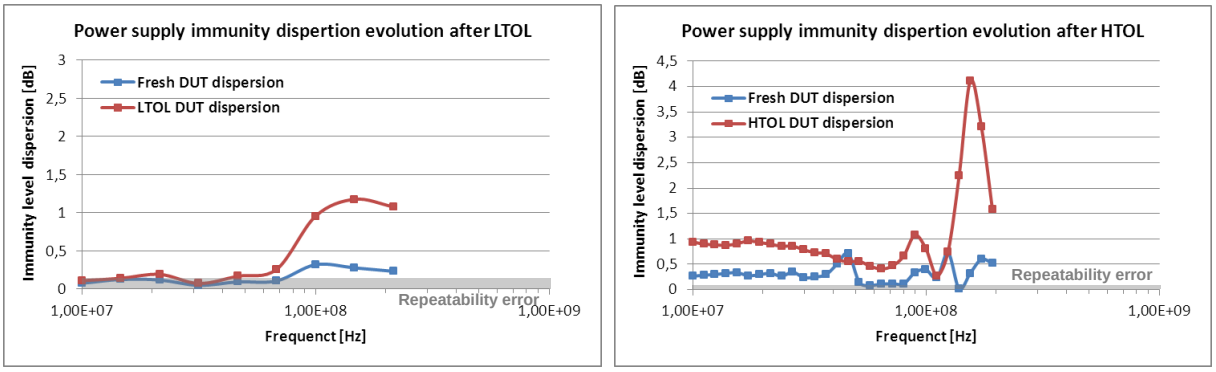

Figure 2-11: Dispersion de l'immunité sur les 5 échantillons avant et après vieillissement

L'analyse statistique montre que le niveau moyen d'immunité diminue et la dispersion entre les différents échantillons augmente. Celui-ci peut aggraver le problème de l'immunité aux perturbations extérieures, comme l'illustre la **Figure 2-12**.

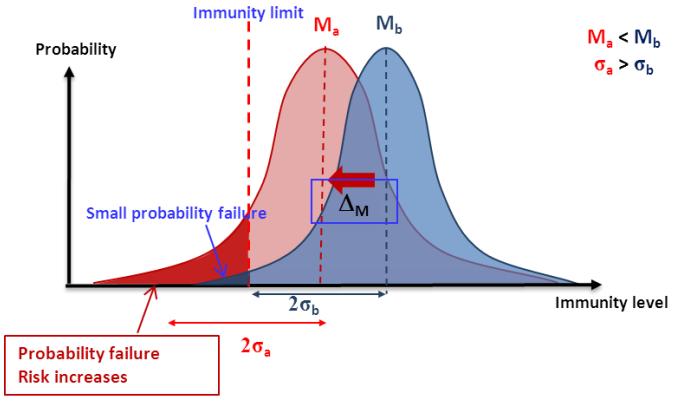

Figure 2-12: L'analyse statistique et la distribution des niveaux d'immunité montrent que l'immunité conduite s'oriente vers une diminution. Le risque de défaillance augmente donc après vieillissement.

Le deuxième cas d'étude est effectué sur un circuit en technologie 0,25 µm. Il comprend différents blocs : des cœurs digitaux, une E/S et une boucle a verrouillage de phase (PLL). Pour chacun de ces blocs, des perturbations harmoniques sont appliquées sur la broche d'alimentation. A partir de mesures effectuées sur 10 échantillons, l'analyse statistique montre que la boucle à verrouillage de phase set le bloc le plus sensible. La **Figure 2-13** présent le pire cas de la dérive du niveau d'immunité de la boucle a verrouillage de phase après HTOL.

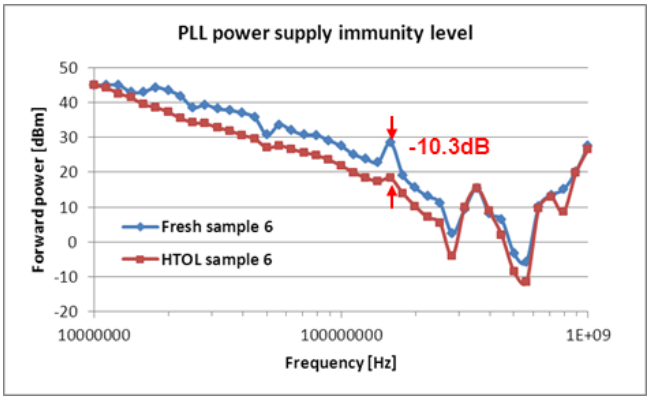

Figure 2-13: Mesure de la réduction du niveau d'immunité conduit de PLL après HTOL (échantillon pire cas)

Après HTOL, le niveau de l'immunité diminue sur toute la bande de fréquence. Le circuit sous test devient plus susceptible après le vieillissement, avec une dérive maximum de -10dB sur la bande de 10MHz -300MHz et 400MHz-800MHz.

3. ETUDE DE L'EFFET DU VIEILLISSEMENT DES TRANSISTORS

Pour prédire la dérive d'immunité due à la dégradation des transistors, nous caractériser l'effet des mécanismes de dégradation et extraire le modèle du vieillissement du transistor. Les vieillissements HTOL et LTOL sont capables d'accélérer des mécanismes de dégradations apparaissant dans l'oxyde de grille des transistors MOSFET, tels que le NBTI (Negative Bias

Temperature Instability) et HCI (Hot Carrier Injection), qui sont les deux principes mécanismes de dégradation pendant l'opération du circuit (Figure 3-1).

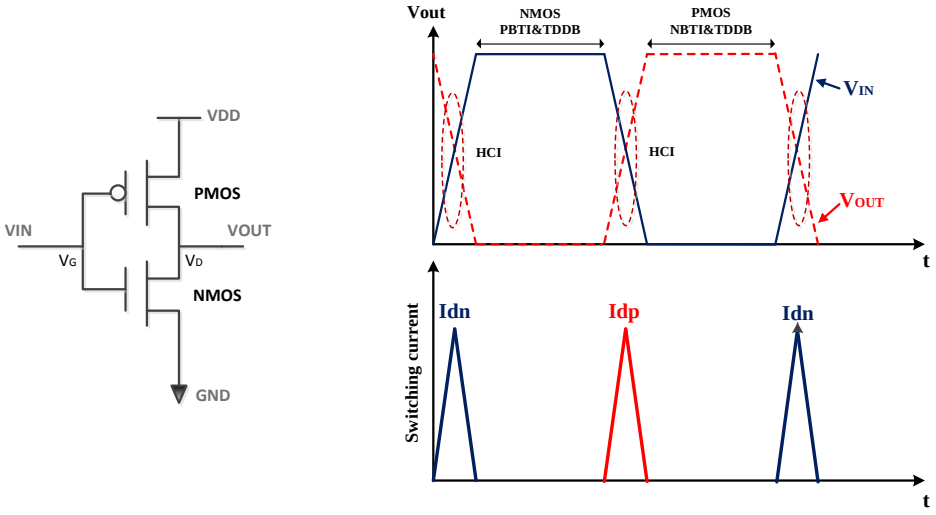

Figure 3-1: Mécanismes de dégradation activés lors de l'opération d'un inverseur

Afin de caractériser l'impact de ces mécanismes de dégradation sur les propriétés des transistors, un circuit de test a été développé en technologie CMOS 90 nm. Plusieurs transistors NMOS et PMOS, présentant différentes géométries et épaisseurs d'oxyde, ont été implémenté. Pour caractériser les deux mécanismes (NBTI sur PMOS et HCI sur NMOS), des stress électriques ont été appliquée aux transistors par mesures sous pointes (Figure 3-2).

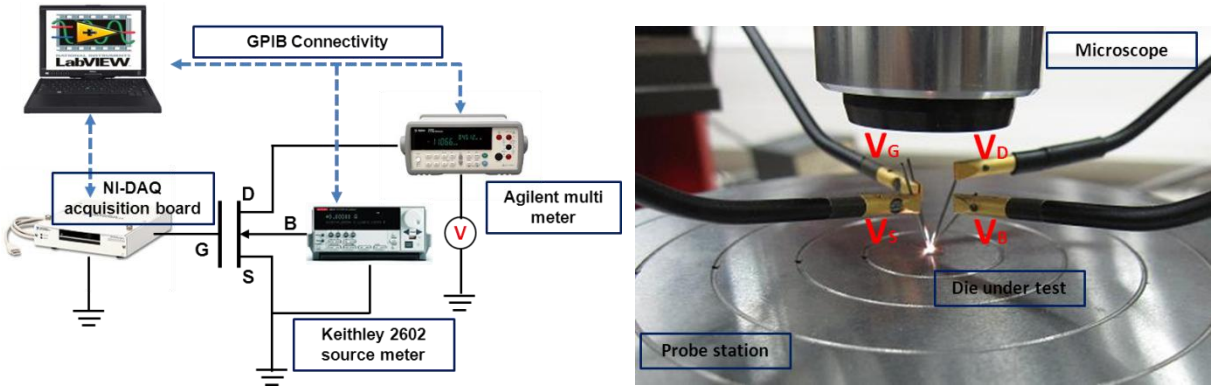

Figure 3-2: Mesure sous pointes pour caractériser la dégradation HCI sur un transistor NMOS

3.1. Les résultats expérimentaux sur la dégradation HCI d'un transistor NMOS

Pour évaluer le pire cas, le stress électrique est appliquée sur un NMOS avec la taille 10µm/0.4µm. Les conditions de stress sont fixé à 4V pour la tension VDS, et 1,05V pour la tension VGS (dépendant de la tension où le courant de substrat est maximum). Après 1500s de stress, l'injection de porteurs chauds a conduit à une diminution de 40 % du courant de drain. (Figure 3-3)

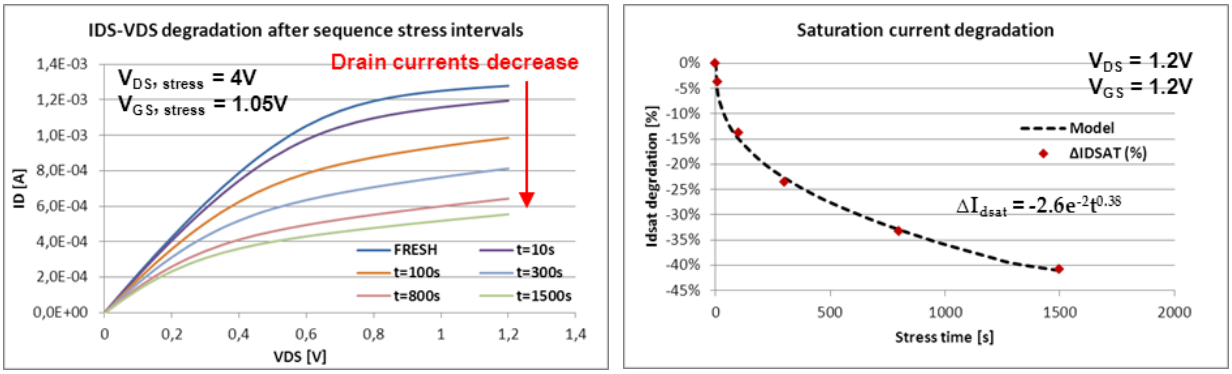

Figure 3-3: Dégradation du courant de drain sous contrainte HCI en fonction du temps

Après l'extraction des paramètres physiques des transistors, l'évolution de la tension seuil et de la mobilité au cours du vieillissement suit une loi de puissance, comme présenté sur la Figure 3-4.

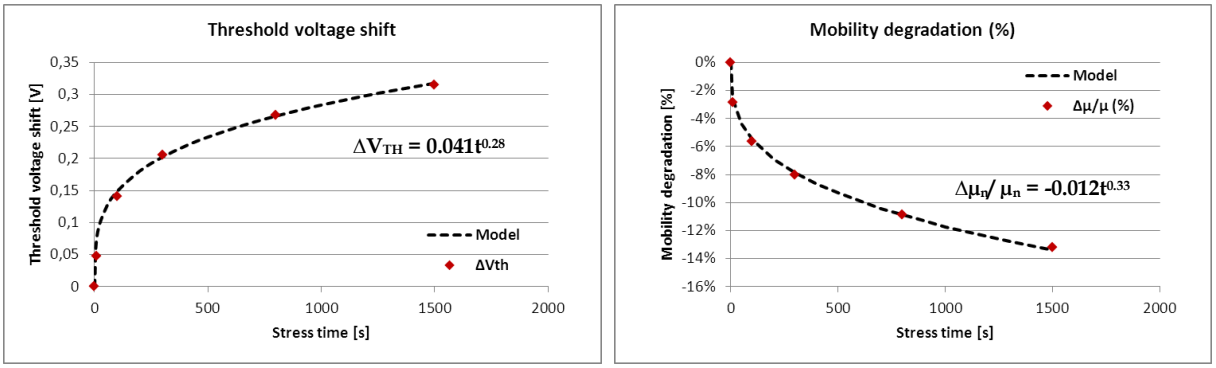

Figure 3-4: Evolution des paramètres physiques d'un transistor NMOS sous contrainte HCI

Les résultats expérimentaux montrent que le mécanisme HCI provoque un changement sur les paramètres physiques du transistor. Après 1500s de stress électrique, la tension de seuil augmente de 0,3V et la mobilité diminue de 12% par rapport à sa valeur d'origine.

3.2. Les résultats expérimentaux sur la dégradation du PMOS due au NBTI

La Figure 3-5 montre l'effet d'une contrainte NBTI sur des transistors PMOS avec le taille 10µm/0.4µm (VGS = -6V et VDS = -0,05V). Après un stress de 2700s, la valeur absolue de la tension de seuil tend à augmenter, la valeur moyenne sur les 3 échantillons peut varier jusqu'à 16 % de la valeur initiale.

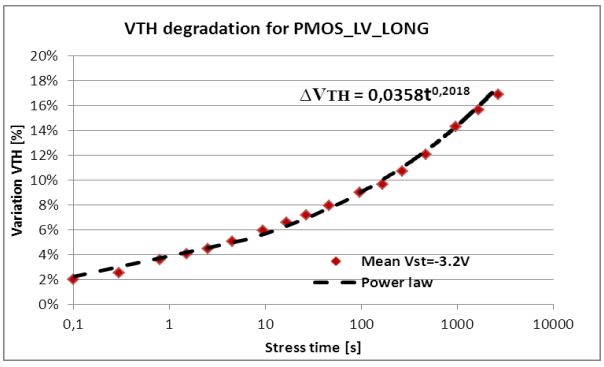

Figure 3-5: Evolution de la tension seuil (ΔVTH) sous contrainte NBTI

Lors d'une dégradation NBTI sur un transistor PMOS, selon la méthode de caractérisation, nous supposons que la tension seuil varie avec le temps de stress. Les résultats expérimentaux montrent également que la variation de la tension seuil suit une loi de puissance avec le temps de stress.

3.3. Les modèles pour la simulation des dégradations des transistors MOS

Pour simuler la dégradation du comportement des transistors, des modèles SPICE sont proposées. Deux modèles SPICE level 3 sont utilisées, correspondant aux transistors avant après stress. Le modèle du transistor vieilli est obtenu en apportant des modifications sur certains paramètres du modèle de transistors non vieillis. (Figure 3-6).

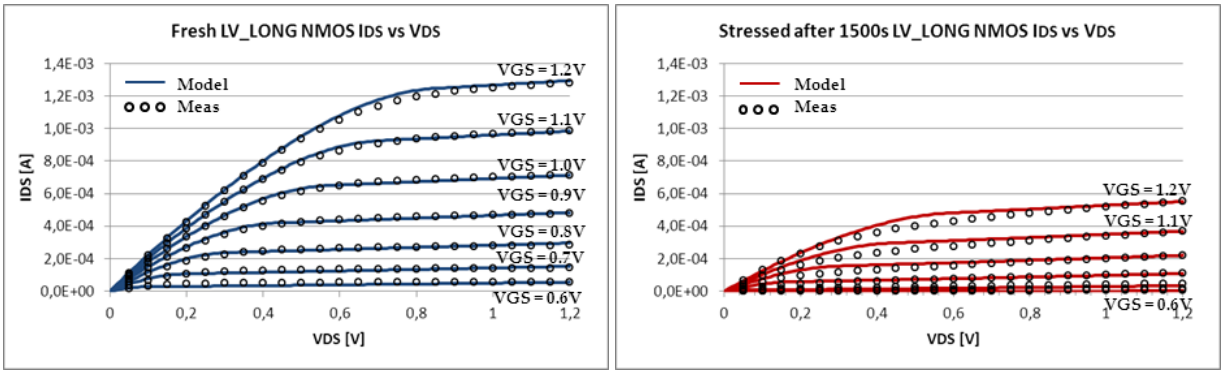

Figure 3-6: Comparaison des mesures du transistor et simulation des modèle SPICE level 3 pour NMOS avant et après stress électrique

Les paramètres du transistors pour le modèle vierge et modèle vieilli sont données par le Table 3-1

	VTH (V)	KP (A/V²)	RD (Ω)
Fresh	0.48	0.000235	185
Stress after 1500s	0.75	0.00019	240
Variation	+0.27	-19%	+30%

Table 3-1: Les variations des paramètres clé du modèle SPICE level 3 pour des transistors avant et après vieillissement

Les comparaisons entre simulations et mesures montrent que le modèle SPICE level 3 est capable de reproduire les caractéristiques IV des transistors avec précision. Les variations des paramètres dans le modèle correspondent bien à la théorie, en dépit de la difficulté à corréler des paramètres a partir des mesures. Il y a en effet un écart entre la simulation et les résultats des mesures, en particulier dans la zone de fonctionnement linéaire des transistors.

4. ETUDE DE LA MODELISATION DE L'IMMUNITE D'UNE PLL

Dans ce chapitre, nous cherchons à développer un modèle de robustesse électromagnétique (EMR) pour prédire la variation du niveau CEM du circuit induite par son vieillissement. Le modèle préliminaire se compose de :

- Modèle CEM : un modèle CEM qui peut reproduire l'immunité aux interférences/ l'émission d'interférences dans une bande de fréquence donnée ;

- Modèle de fiabilité : dans notre étude, nous nous concertons sur l'impact du vieillissement sur les circuits intégrés : quel que soit l'impact du vieillissement sur les circuits imprimés et les composant passifs associés (en particulier des capacités découplage, les inductances) et le boitier du circuit.

Le flot de modélisation illustré dans **Figure 4-1** :

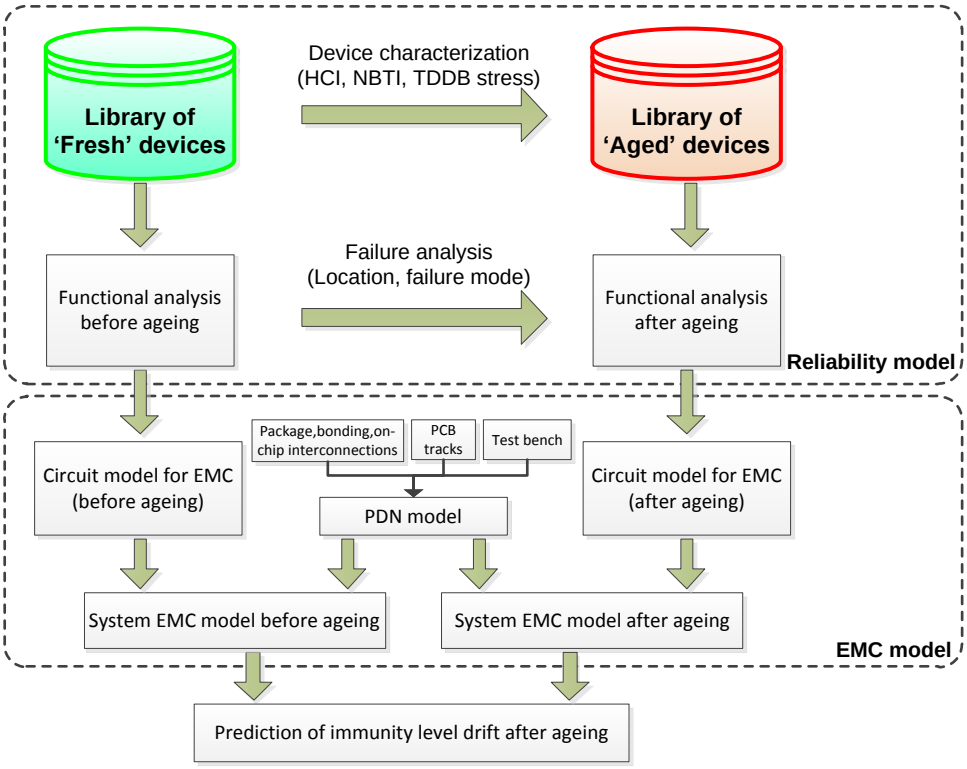

Figure 4-1: flot de modélisation et prédiction d'immunité à long terme des circuits

Dans ce cas d'étude, nous prédisons et analysons la dérive d'immunité d'une PLL. La PLL se compose d'un comparateur de phase, un VCO (Oscillateur contrôlé en tension), et un diviseur de fréquence. Il est fabriqué en technologie CMOS 0,25µm. Le VCO consiste en trois cellules de délai et de 3 inverseurs. Le schéma de principe de cette PLL est dans la **Figure 4-2**

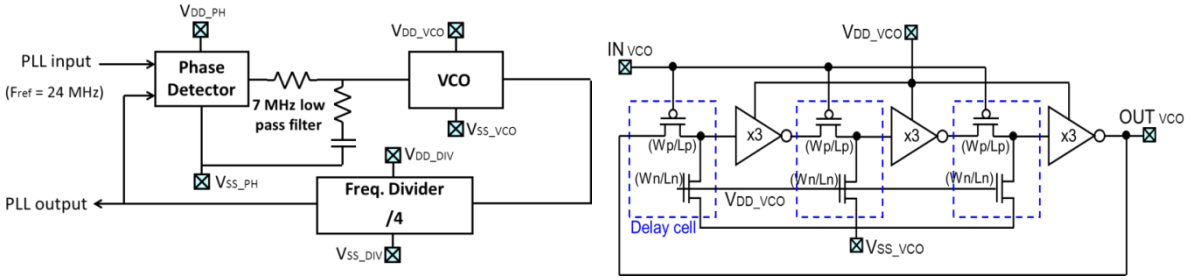

Figure 4-2: Schéma de principe de laPLL et du VCO

Les modèles de dégradation des transistors sont inclus dans les modèles d'immunité. Le formalisme de ces derniers est basé sur le standard ICIM-CI [IEC62433-4]. Le modèle est constitué par un ensemble de 2 composants (**Figure 4-3**) : le réseau de distribution passif (Passive distribution Network PDN) qui modélise la propagation du bruit externe vers les nœuds sensibles du circuit, et le bloc de comportement interne (Internal Behavior IB) qui modélise la réponse du circuit à une perturbation électromagnétique.

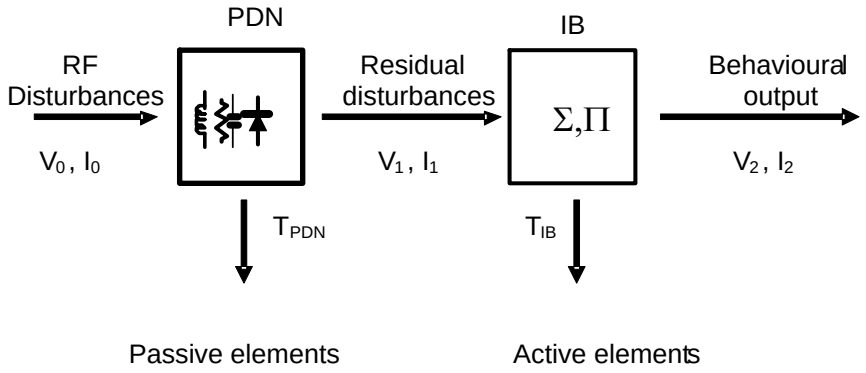

Figure 4-3: Architecture générale d'un modèle d'immunité selon le standard "ICIM-CI"[IEC62433-4].

Pour analyser la dérive du niveau d'immunité de la boucle à verrouillage de phase, la schématique au niveau transistor est employé pour le bloc IB (**Figure 4-2**). Le modèle du PDN est extrait à partir de mesures à l'analyseur de réseau entre les différentes broches de la PLL. Le modèle complet de l'environnement de test (DPI) et du PDN de bloc est illustré dans **Figure 4-4** :

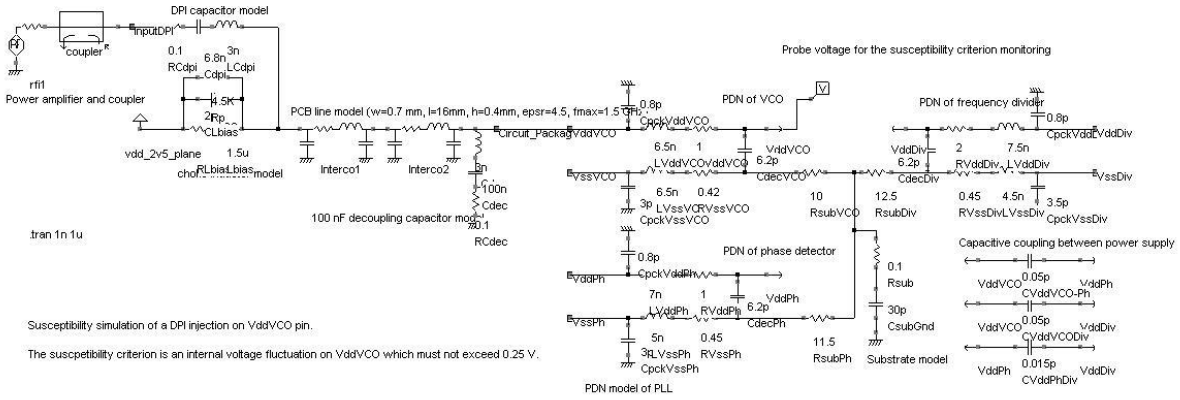

Figure 4-4: Modèle complet de l'environnement de test et du PDN des trois sous blocs de la PLL

Figure 4-5 présente la comparaison de la simulation et de la mesure du bruit couplé sur l'alimentation du VCO lors d'un test DPI. Une excellente corrélation démontre que le modèle du PDN de la PLL est capable de prédire le niveau en puissance de la perturbation pour induire un niveau de fluctuation de tension sur l'alimentation du VCO jusqu'à 1GHz.

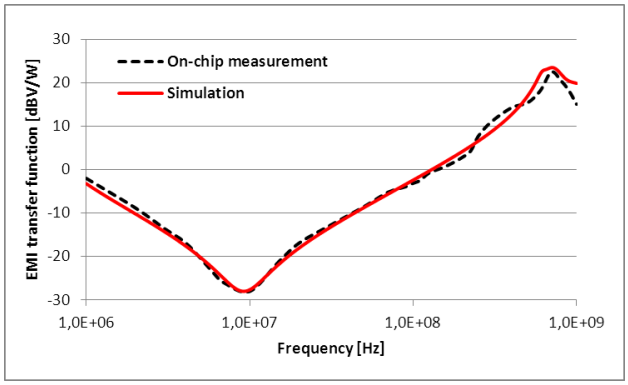

Figure 4-5: Comparaison entre mesure et simulation du bruit couplé sur l'alimentation de la PLL lors d'un essai DPI

Une fois le modèle d'immunité validé, les paramètres des transistors atteints par les mécanismes de dégradation sont modifiés. La **Figure 4-6** compare la mesure et la simulation de l'évolution de la

fréquence de sortie de l'oscillateur contrôlé en tension (VCO) en fonction de la tension d'alimentation. Malgré le manque d'information sur l'évolution des paramètres du transistor au cours du vieillissement du PLL, nous avons fait des hypothèses sur la dégradation des transistors PMOS dans la cellule de délai, en augmentant de 10 % la valeur absolue de la tension seuil augmente et en diminuant de 10 % la mobilité.

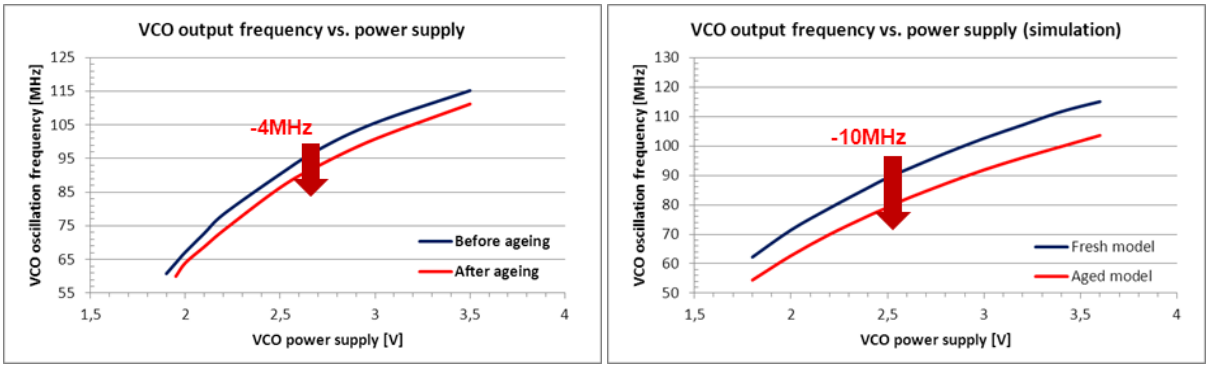

Figure 4-6: Comparaison des mesures (gauche) et des simulations (droite) de la fréquence de fonctionnement du VCO avant et après vieillissement (gauche).

La Figure 4-6 présente la simulation de la fréquence d'oscillation du VCO pour des tensions de l'alimentation variée, avant et après la dégradation du transistor PMOS de la cellule de retard. Dans la simulation, la dégradation du transistor PMOS entraine une réduction de la fréquence du VCO, qui est également observé dans les échantillons mesurés. Le montant de la dérive de fréquence dépend des variations de la mobilité et de la tension de seuil.

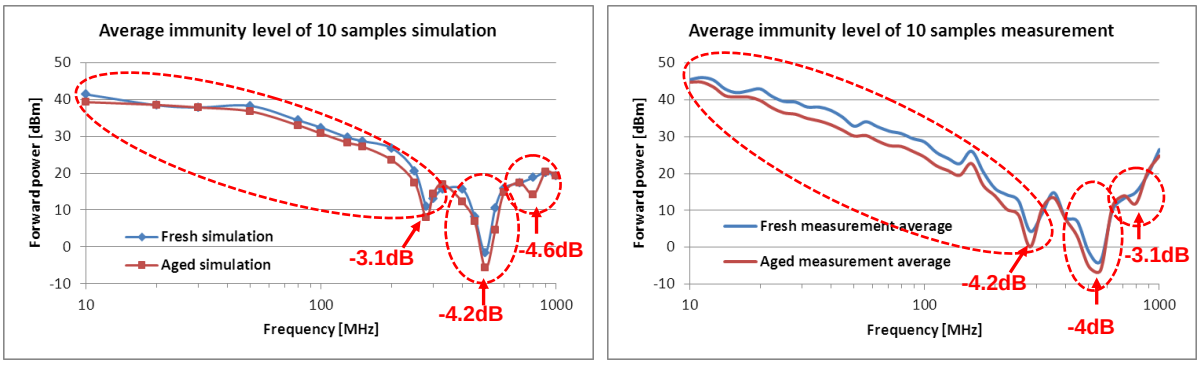

Figure 4-7: Comparaisons de l'immunité de l'alimentation du VCO avant et après vieillissement: (gauche) simulation avec modèle REM; (droit) la valeur moyenne des mesures sur 10 échantillons

En ajoutant le modèle du PDN et l'environnement du test, le niveau d'immunité peut être simulé. La Figure 4-7 présente la comparaison entre la simulation et la mesure avant et après HTOL du seuil d'immunité de la PLL.

En comparant les résultats de mesure (Figure 4-7-droite) et de simulation (Figure 4-7-gauche) de la dérive de l'immunité de la PLL, on observe que le modèle reproduit les diminutions du niveau d'immunité sur les mêmes bandes de fréquence. La valeur moyenne de la réduction d'immunité observée en mesure sur 10 échantillons sur 10-100MHz est de 2.6dB, ce qui est proche de la diminution simulée (1,7dB). La différence s'explique par le manque d'informations précises sur les mécanismes de dégradation réels qui apparaissent au sein du VCO. Toutefois, le modèle proposé reproduit qualitativement l'évolution du niveau d'immunité de la PLL aux perturbations conduites et confirme que les mécanismes de dégradation intrinsèques des transistors peut conduire à des changements significatifs de la susceptibilité d'un circuit.